Decreasing Graphene Contact Resistance by Increasing Edge Contact Length

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Graphene is a two dimensional material which has combination of unique mechanical, electrical and optical properties. Due to the unique properties of graphene, it has potential for several applications such as radio frequency applications and ultrafast photodetectors. Reducing contact resistance of metal-graphene is important for further improvement of graphene devices and for realization of graphene based electronics. Contact between graphene and metal can be improved by edge contact length. Edge contact length improves coupling between metal and graphene; therefore, contact resistance is reduced. Edge contact length can be introduced by generating nanostructures under metal.

Fabrication of graphene based devices requires special treatment due to graphene's two dimensional natures. In this thesis, fabrication process for graphene devices is discussed in details. Main attention is given to reducing contact resistance. The fabrication process includes e-beam lithography; choosing right metals and metallization techniques; etching of graphene; lift-off issues; and reducing resist residues.

In this research, graphene under the metal contacts was patterned by electron beam lithography with series of holes of 100nm to 300nm radius etched by oxygen plasma etching. The holes were patterned by electron beam lithography, and metallization was carried out by electron beam evaporation followed by lift-off process. The effects of the geometrical parameters of the holes and different graphene length under the metal are investigated experimentally. This research can be used as source of graphene device fabrication for the beginners.

Acknowledgements

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Dedication

To my father Cholponbek Burzhuev

Table of Contents

List of Figures

Chapter 1
INTRODUCTION

1.1 Graphene

Graphene is two-dimensional material composed of carbon atoms with atomic thickness. Carbon atoms in graphene are arranged in honeycomb structure [1]. Graphene has combination of unique properties such as extremely high electrical conductivity[2], highest mechanical strength[3], extremely high thermal conductivity[4] and high transparency[5]. Graphene doesn't have band gap and can be considered as a semimetal (Figure 1). It is also very flexible crystal [3].

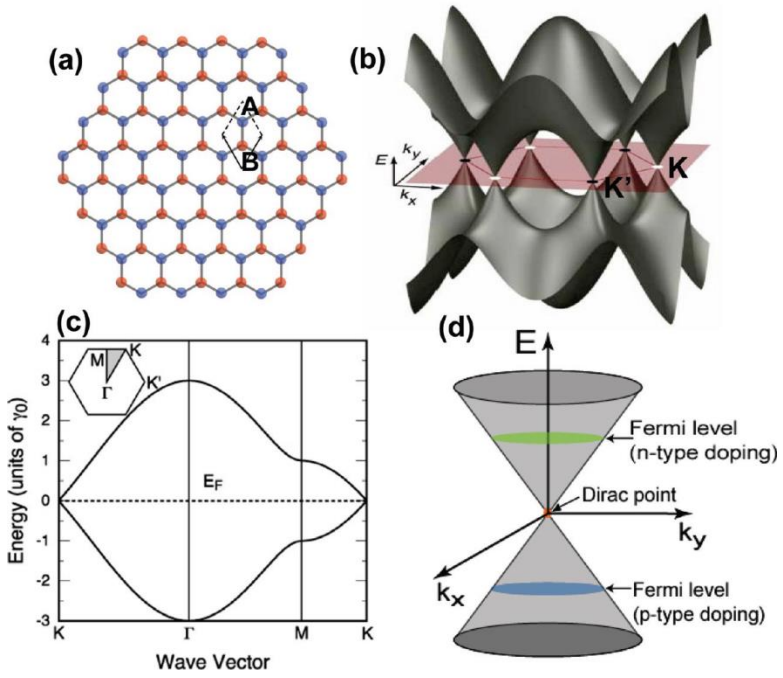


Figure 1 a) Graphene honeycomb structure composed of two atoms, A and B, in unit cell. b) Graphene's band structure. c) Electronic energy dispersion of graphene, and d) energy band structure at low energies. Dirac point is where conduction and valance cones are touching each other. Figure is taken from[5]**.**

1.1.1 Graphene properties

Mobility of charge carriers in graphene is extremely high due to ballistic transport which shown to be 200,000 $\frac{cm^2}{Vs}$ [2].Mechanical strength is also very high due to the sigma ponds and delocalized pi

bond and experimental observation show that Young's modulus of graphene is 1TPa [3]. In principle ideal single layer graphene $1m \times 1m$ can hold one cat[6]. Graphene also have interesting optical properties. For example, graphene has interband absorption in the range of visible to infrared of the electromagnetic field spectrum [7] and its optical transmission is about 97.7% of incident light[8].

1.1.2 Graphene types

There are many different way to produced graphene. Among them mechanical exfoliation using scotch tape , chemical exfoliation from reduced graphene oxide (rGO)[9], epitaxial growth of graphene[10], and chemical vapor deposition (CVD) graphene[11] are most popular. Most striking properties of graphene such as extremely high mobility have shown in scotch tape graphene[2]. Scotch tape graphene is a method were graphene flakes can be peeled off by scotch tape from graphite. Although scotch taped graphene has outstanding properties, it cannot be used for real world applications because the graphene flakes size are in the range of several micrometer[12] and continues film cannot be obtained by this method. On the other hand, the CVD graphene has capability to be used in the real world applications because large and continuous graphene layers can be obtained.

1.1.3 Graphene applications

Graphene can be used in various applications such as transistors and touch screens devices. In addition, it can be used in photonic devices such as photodetector, electro optic modulators, and LEDs[13]. Graphene field effect transistor (GFET) is considered to be one of the most important applications of this two-dimensional material. However, single layer graphene doesn't have bandgap; therefore, ON/OFF ratio is very low about 10-100[14]. Although, bandgap can be introduced by modifying graphene, e.g., by make graphene nanoribbons, mobility of the channel is significantly reduced. In large area CVD graphene charge carrier mobility is also low compared with III-V semiconductors. However, short channel affects in transistors can be reduced if graphene is used due to its ultimate thickness. [14]

Nevertheless, graphene transistors can be used in radio frequency (RF) applications where the ON/OFF ratio is not very important [14]. In high speed graphene transistors, bandwidth of the device is limited by resistive-capacitive (RC) delay. Resistance in short channel device which are required for high speed applications is limited by contact resistance[5].In the next chapter, reduction of contact resistance in GFET will reviewed.

Chapter 2

Contact resistance in graphene devices

2.1 Contact resistance

Total resistance of transistor channel can be given by[15]:

$$R_T = 2R_m + 2R_c + R_{semi} \quad (1)$$

where R_{semi} is the channel resistance, R_m is the metal to metal contact resistance, R_c is the contact resistance and R_T is the total resistance.

Contact resistance occur when two different materials comes in to contact. Transfer length method (TLM) is used to measure contact resistance of metal-semiconductor junction[16]. In this method, total resistance of devices having different channel length is measured. Metal-metal resistance can be omitted because it is generally much lower than contact resistance of metal-semiconductor contact resistance, so equation 1 can be approximated as equation 2. Then, by plotting R_T vs L(distance between two contacts) one can find transfer length, sheet resistance and contact resistance of the device (Figure 2, equation 4).

$$R_T = 2R_m + 2R_c + R_{semi} \approx 2R_c + R_{semi} \quad (2)$$

$$R_{semi} = \frac{R_s L}{W} \quad (3)$$

$$R_T = 2R_c + \frac{R_s L}{W} \quad (4)$$

Transfer length is the length where the potential drops between metal and semiconductor by factor of $1/e$. Transfer length is important property of devices because of the planar geometry of contacts. Even though, current through the channel is generally be uniform it is not flow uniformly to contacts (Figure 4).

$$R_c = \frac{\rho_c L_t}{W} \quad (5)$$

$$R_T = R_s \frac{L}{W} + 2R_c \quad (6)$$

$$R_T = \frac{R_s}{W}(L+2L_t) \tag{7}$$

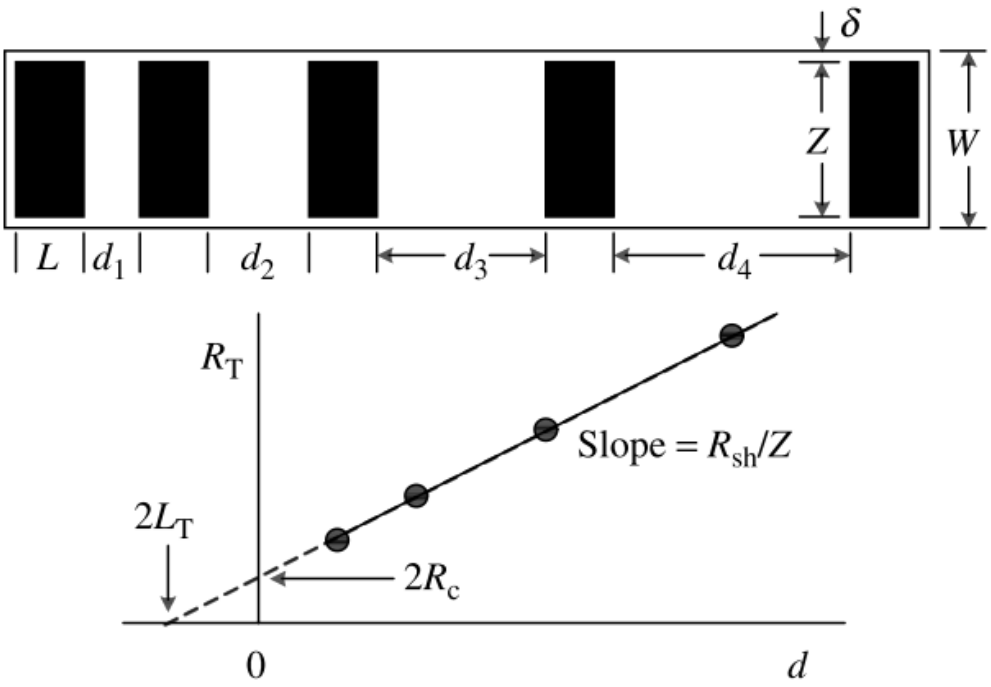


Figure 2: Schematic of graphene channel. Total resistance versus channel length of the device is plotted. Figure is taken from [15]**.**

$$R_T = 2R_c + \frac{R_s L}{W}$$

Contact resistivity is given by [15]:

$$\rho_c = R_c A_c \tag{8}$$

where A_c is area of the contact. Current will mainly flow through the area near the contact with channel which is:

$$I\,(x) \propto e^{-x/L_t} \tag{9}$$

where L_t is the transfer length. Transfer length is given by:

$$L_t = \sqrt{\frac{\rho_c}{R_s}} \tag{10}$$

where R_s is sheet resistance of the channel.

2.1.1 Metal-graphene contact

In the metal-semiconductor junctions Fermi energy, $E_{F,}$ of metal and semiconductor will be equalized. Therefore, Schottky barrier will appear which is $\varphi_B = \varphi_1 - \chi$ (φ_1 and χ are work function and electron affinity of semiconductor) as shown in the Figure 3a. On the other hand, metal-metal contact don't have potential barrier due to large amount of carrier density. Even though, charge transfer will occur between metals, the junction will have small screening length. Hence, potential difference changes abruptly at the interface of two metals as shown in the Figure 3 b).

Graphene does not have band gap; therefore, graphene-metal junction is analogous to metal-metal junction. In the Figure 3 d) and e), energy and density of states relation (DOS) is shown before and after contact. Charge transfer will occur from graphene to metal if metal work function is higher than graphene. These charges can shift E_F of graphene leading to doping near the metal contact and potential difference ΔV as shown in the Figure 3 c) and e). Due to the fact that graphene have limited DOS, screening length of graphene-metal junction is much larger than screening length of metal-metal junction.

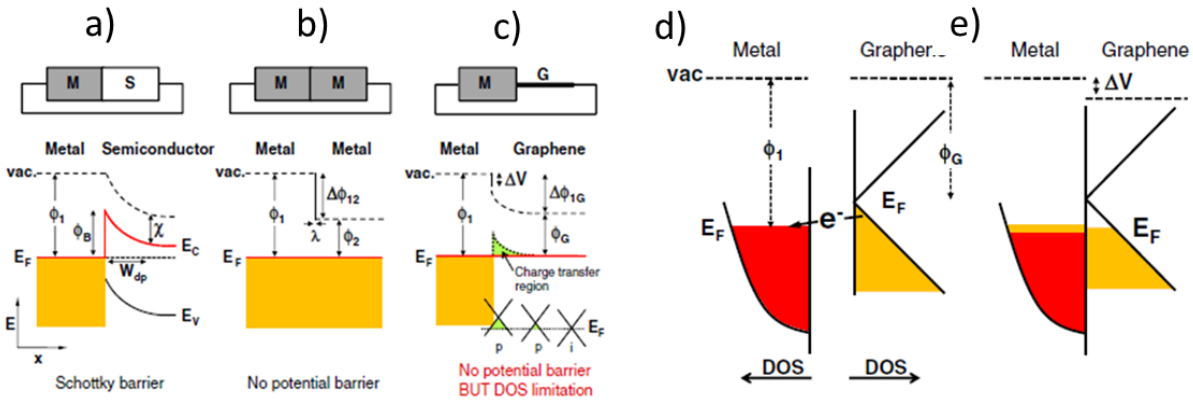


Figure 3 a) Metal-semiconductor b) Metal-metal c) metal-graphene contact energy band diagram. Energy and DOS of graphene/metal before d) and after e) contact. The figure was taken from [17]**.**

2.1.2 Contact resistivity in graphene

Transfer length in graphene devices is less than 1 micron[17], [18]. Contact resistivity in graphene devices is changing with the contact area; however, it is constant when width of the channel is changed[17]. This is happens due to short transfer length, L_t in graphene-metal junction. Therefore, the contact resistivity for graphene devices can be given by $\rho_c(\Omega\mu m) = R_c W$ (Figure 4).

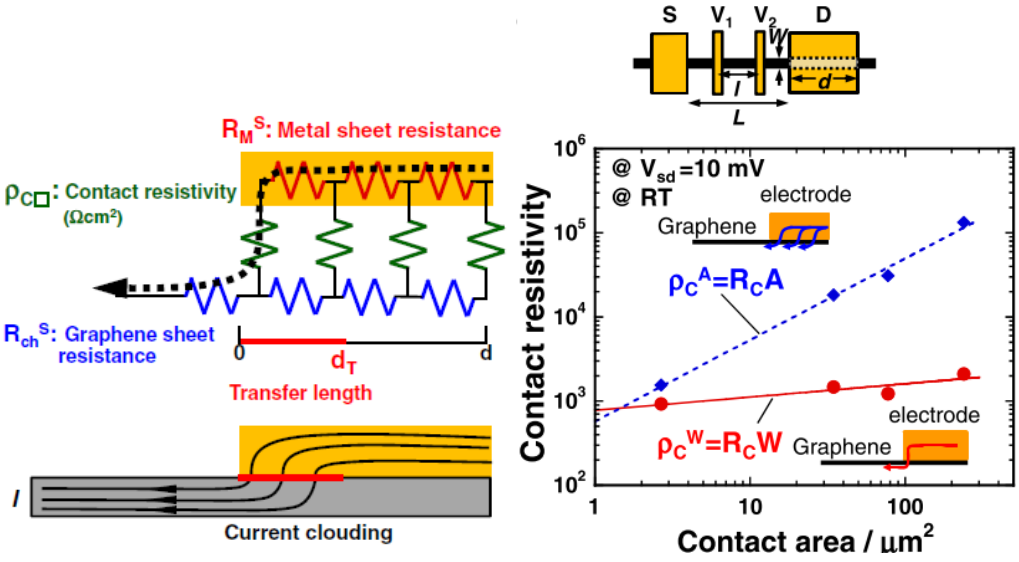


Figure 4: Left: Current is flowing from metal contacts to channel is not uniform through contact. Right: Contact resistivity of graphene is characterized by width of the channel. Figure was taken from[17]**.**

2.1.3 Contact resistivity limitations

Contact resistance in graphene devices is high due to the limited density of state in graphene (2D material)[17]. In comparison silicon devices have contact resistivity of $80\Omega\mu m$ [19] while in graphene device contact resistance varies from several hundreds to thousands $\Omega\mu m$. The minimum contact resistance, assuming all no scattering, a graphene-metal contact is given by[20][21]:

$$RW = \frac{h}{2e^2}\sqrt{\frac{\pi}{2n}} = 16.28\ k\Omega/\sqrt{n} \qquad (11)$$

where W is the width of the cannel, h is the Planck's constant and n is the carrier density. Carrier density in graphene is in the orders of $1 \times 10^2\ cm^2$, which results in contact resistance of $160\Omega\mu m$[20]. Nevertheless, lower contact resistivity values have been shown experimentally.

2.1.4 Contact resistance versus gate bias

It was shown by Xia et al. [22] that contact resistance varies as a function of gate bias. Interestingly, contact resistance has same behavior as channel resistance; it increases when gate bias is close to Dirac point and decreases when it is away from it. It is important to note that contact resistance variations are huge near the Dirac point at room temperature as shown in Figure 5.[22]

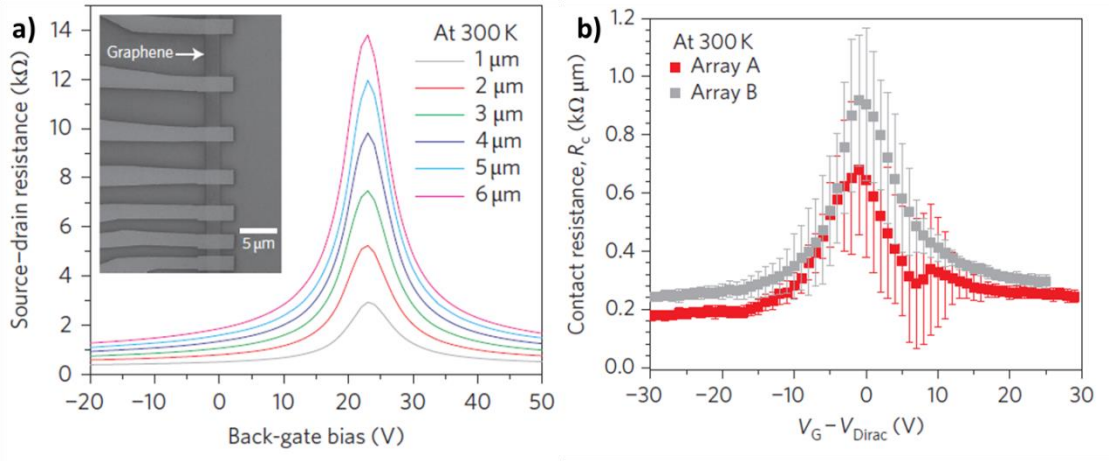


Figure 5: a) Total resistance of the channel versus V_g. b) Contact resistance versus V_g-V_{Dirac}. V_g and V_{Dirac} are gate bias and Dirac point voltages respectively. Figure was taken from [22].

2.2 Reducing contact resistance

2.2.1 Work function and Surface roughness effect

There are several methods for reducing contact resistance between metal and graphene. Watanabe et. al[23] studied the contact resistance between metal and graphene (scotch taped) by using metals with different work functions . They show that work function of metal does not affect contact resistance, while surface roughness of the metal can affect the contact resistivity of the graphene devices as shown in (Figure 6 c) [23]. Particularly, Co, Ni and Pd show lower contact resistivity due to smooth surface, film uniformity and smaller grain sizes which increase the contact area(Figure 6) [23].

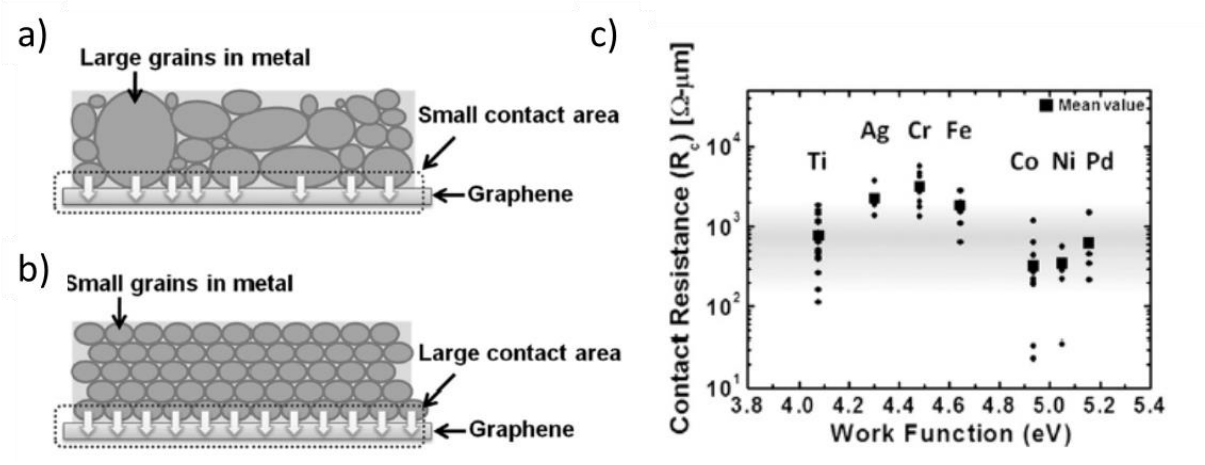


Figure 6: Contact resistance of graphene devices as a function of metal work function . c)Schematic of metal graphene contact Figure was taken from[23]**.**

Nonetheless, graphene doped with metal near the contacts $(0.2 - 0.3\ \mu m)$ due to the work function difference between graphene and metals as was experimentally observed in the scanning photocurrent study [24]. This feature of metal graphene contacts can be used as photodetectors which can operate at ultrahigh frequencies[25].

Purity of metal contacts is another important parameter for obtaining low contact resistance. Zhong et.al[26] used high purity Pd contacts by depositing Pd at high vacuum level (~10^{-7} Torr) and measured the Pd-graphene contact resistivity as low as $100\Omega\mu m$ which was attributed to high purity of the deposited metal, quality of graphene and clean interfaces. [26]

2.2.2 Metal deposition type

Nagashio et al. used four- probe measurement in order to measure contact resistivity of graphene devices. In this case the contact resistivity (ρ_s) is given by:

$$R_c = 1/2(R_t - R_{ch} \times \frac{L}{l}) \quad (12)$$

$$\rho_s = R_c \times \mathrm{W} \quad (13)$$

where R_c is the contact resistance, R_t is the total resistance of the channel, R_{ch} is the resistance of the channel, L is the distance between source and drain, l is the distance between two voltage probes, $\rho_s$is the resistivity and wis the width of the channel [17] (Figure 7 b). In the Figure 7 b, μ_{4p}/μ_{2p} versus

contact resistivity is shown, where the μ_{2p} is the two probe mobility which includes contact resistivity and the μ_{4p} is the four probe mobility.

By using sputtered Ti and Cr layers, as adhesion layer for Au contacts, the contact resistivity increases while using Ni contact without any adhesion layer resulted in lower contact resistivity as shown in Figure 7 . RF sputtered contact damages graphene, while thermal Ti doesn't damage[17]. It can be concluded that the contact metal types and deposition technique should be chosen carefully when considering device fabrication. For example, Xia et al. measured contact resistivity of Pd contacts in an exfoliated graphene as low as $180\Omega\mu m$ without using adhesive layer at room temperature[22].

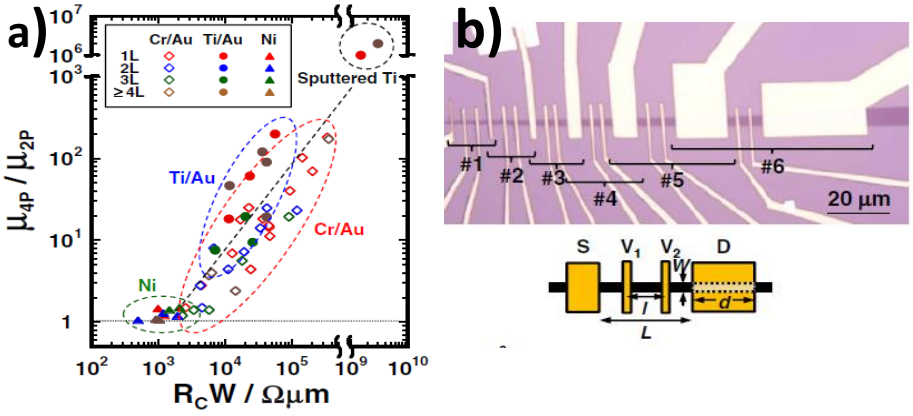


Figure 7: a) Contact resistivity of the Cr/Au, Ti/Au and Ni contacts as a function of μ_{4p}/μ_{2p}. b) Optical image of graphene devices used for the measurements and schematic of the structure. Figure was taken from[17]**.**

2.2.3 Photoresist residues

Residue on graphene surface due to micro-nanofabrication process increases contact resistivity because it does not allow graphene to have immediate contact with metal and increase the surface roughness. Photoresist residues can be removed by Ultraviolet/Ozone treatment. Reduction of the photoresist residue was observed in AFM studies where surface roughness of the graphene layer was reduced after Ultraviolet/Ozone treatment. In addition, this process damages graphene surface which can be shown by Raman spectra where the D band and G band ratio increases after certain exposure

time. The minimum contact resistance was measured by this method was as low as $184\Omega\mu m$ where Ti (20 nm)/Au (80nm) was used as contact [27].

Oxygen plasma etching is also capable to improve contact resistivity. This process should be done before metallization of graphene contacts. Schematic of process development is shown in the Figure 8. In this case the improvement of the contact resistivity between graphene and metal was not only attributed to removing the photoresist residue but also due to creating defects in graphene. In addition, the contact resistivity can be improved further by annealing at 450-475 ^{0}C for 15 min after metallization process [28] .

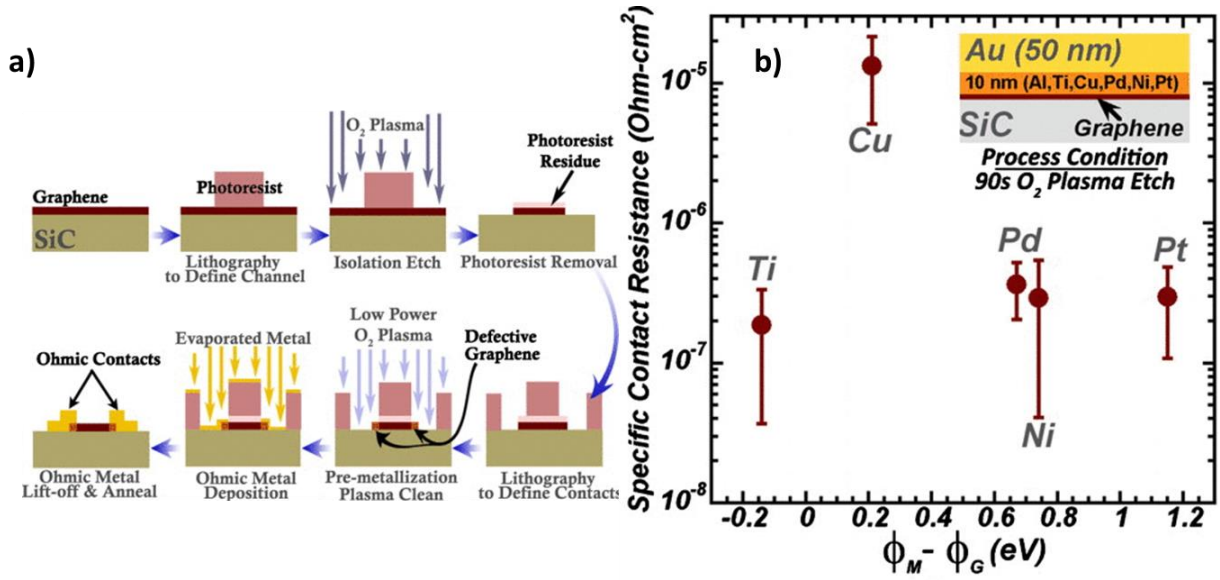


Figure 8: a) Schematic diagram of graphene device fabrication process where oxygen plasma etching was used to improve contact resistance. b) Specific contact resistivity of various metal contacts measured after oxygen plasma treatment. Figure was taken from [28]

Graphene devices fabricated by photolithography and electron beam lithography (EBL) have different contact resistance values. This difference was attributed to the presence of residual layer after development process of resist. It was shown that after using a photoresist like AZ5214E, 3-4 nm residual layer remains on the graphene surface after development process. While, ~1nm residual layer is observed for EBL resist Poly(methyl methacrylate) ,PMMA,. Therefore, metal-graphene contact resistance of device fabricated by EBL is generally lower than that fabricated by photolithography as shown in Figure 9. [29]

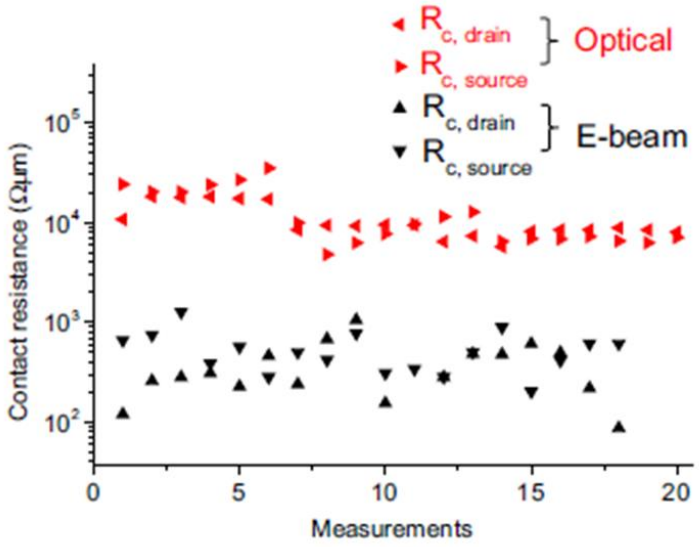


Figure 9: Contact resistance values for graphene devices fabricated with optical and electron beam lithography. Figure was taken from [29]

Leong et al. shown that present of PMMA residue doesn't affect contact resistivity too [30]. This discrepancy between previously stated results might be due different type of resist and fabrication process. Li et. al [27] and Robinson et.al[28] were used optical lithography followed by ultraviolet/ozone treatment and oxygen plasma cleaning to improve the contact resistance of the fabricated devices which is different from the Leong et.al technique.

Although, Leong et al. [30] show that residual layer doesn't affect contact resistance, metallization was done after first lithography step. Fabrication process of graphene devices may require more steps; as a result, residual thickness will more thicker and can affect contact resistance.

2.2.4 Aluminum sacrificial layer

The graphene surface and metal-graphene contact interface can be protected from the resist residue by using a thin layer of Al as sacrificial layer. The Al can be etched by using Tetramethylammonium hydroxide (TMAH), which can be found in several photoresist developers, without damaging the graphene surface ,and the contact resistivity obtained by this method can be varied in the range of $200\ \mu m - 500 \Omega \mu m$ by using Ti(1.5 nm)/Pd(45 nm)/Au(15nm) as contacts[31]. While without sacrificial layer it was measured in the range of 2000 Ω µm to2500 Ω µm[31] . AFM studies reveal that using Al sacrificial layer between the graphene and resist in the device fabrication resulted in a smoother surface comparable to that before any fabrication process as shown in Figure 10. As can be

seen from figures 10 a and 10b, the amount of resist residue in the fabricated structure using Al sacrificial layer is much smaller than that without using Al sacrificial layer. By using the Al sacrificial layer, the surface roughness of the graphene films was measures as low as 0.2 nm after standard development process which is similar to that measured in the a bare graphene film before standard development process while, the surface roughness in the graphene film was measured as 1 nm after standard development process without using Al sacrificial layer. [31]

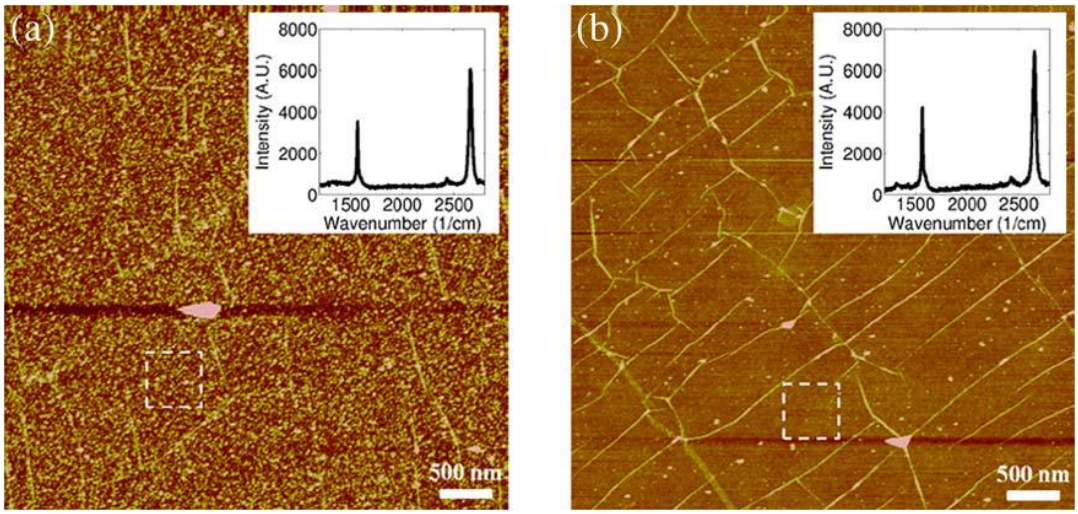


Figure 10: AFM images of graphene (a) without sacrificial layer and (b) with sacrificial layer after standard development process using lithography resist. Figure was taken from [31]**.**

2.2.5 Annealing

PMMA is generally used for transferring graphene from copper substrate to another substrate. Moreover, it is used as resist in EBL, which resulted in the presence of residue on the graphene surface and hence might increasing the metal-graphene contact resistance. The amount of the PMMA residue in the graphene surface can be reduced by annealing the graphene sample. This process is generally carry out using different temperature and environment conditions such as vacuum at 300 ^{0}C[32] , underH_2/Ar atmosphere at 400 ^{0}C [33] and under CO_2 atmosphere and temperature larger than 200 ^{0}C[34]. It was also reported that the graphene surface can be cleaned from resist residue by using rapid thermal annealing process under N_2 environment at 250 ^{0}C.This process is much shorter than thermal annealing process[35].

Unfortunately, annealing process cannot be used in the standard lift-off processes because the resist reflow it at high temperatures. In the lift-off process, resist is patterned by lithography and after

development, metallization is done. Before metallization, substrate is covered by resist and annealing at high temperatures will result in reflow of resist to the patterned structures. For example, glass transition temperature (T_g) of PMMA, is ~ 106 ^{0}C and it is reflowing on the graphene surface during the rapid thermal annealing process at temperature close or higher than its T_g. So, annealing after development and before metallization cannot be used to remove resist residuals.

However, annealing process can be used after metal deposition. Annealing after metalization improves contact resistance in graphene devices[28][20][19]. The reason for this process is due to dissolution of carbon from the graphene to the metal which result in generation of end contact[36]. This should not be confused with removal of resist residual, which are already underneath the metal contacts. Leong et. al.[30] show that diffusion of carbon atoms into the metal contact (e.g. Ni) leads to reduce the contact resistivity, which can be attributed to the formation of end contact between the graphene and metal that result in have lower resistance.

Balci et al. show that contact resistivity of graphene can be improved by rapid thermal annealing. Significat improvement was observed in Cu contacts while less improvement was observed in Pd (Figure 11). [20]

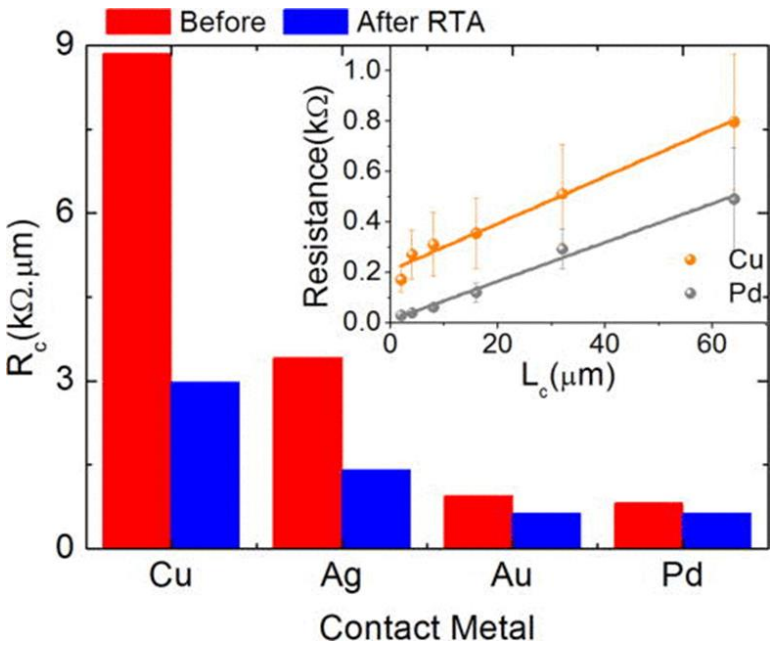
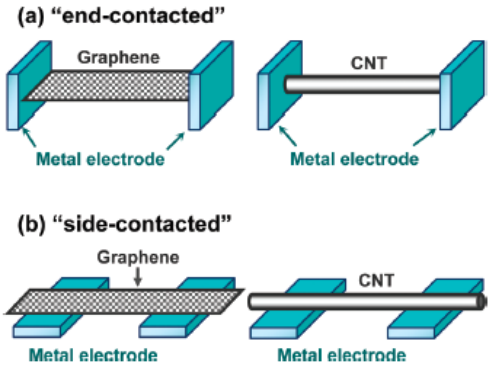


Figure 11: Contact resistivity of graphene before and after thermal annealing of different metal contacts. Figure was taken from[20]**.**

2.3 End-contact for reducing graphene contact resistance

2.3.1 Theoretical and numerical predictions

There are two different type of metal-graphene contacts; side contact and end contact as shown in Figure 12. In the side contact mode the metal is directly placed on top of the graphene; while, in the end contact mode at the edge of graphene is in contact with the metal surface as shown in Figure 12a. It was numerically shown that the edge contact mode offers lower contact resistivity and higher mechanical stability of the contacts compare to that in end contact mode [37].



	Ti	Pd	Pt	Cu	Au
"end-contacted" per unit cell (kΩ)	13.3	17.8	18.6	31.7	23.3
"end-contacted" per C atom[b] (kΩ)	106.5	142.4	148.5	253.5	186.8
"side-contacted" per C atom[c] (kΩ)	938	8566	34 689	630 352	1 261 002

Figure 12: Left: Schematic presents of (a) end contact mode and (b) side contact mode in a metal-graphene / -carbon nanotube device. Right: corresponding values of contact resistance for both end contact and side contact modes using different metal contacts. The contact resistance is significantly reduced when end contact mode is used. Figure was taken from[37]**.**

The contact resistance at the metal-graphene interface is also strongly depends on the interaction energy between metallic atoms such as Ti, Pd, Pt, Cu and Au[37]. When the metallic atom is in end contact mode the distance between metal and carbon is smaller than that in the side contact mode, and hence the interaction energy is significantly higher in the end contact geometry as it is evident from Figure 13. The largest difference between side contacted and end contacted interaction energies was observed for the Cu (323 times), Pt(259 times), Au(247 times), Pd (199 times), and Ti (12.9) times. So, more contact resistance improvements can be observed for Cu, Pt and Au rather than Pd and Ti when end contacted mode is used. Improvement of the contact resistivity from side contacted to end contacted mode for Cu and Pd observed as 32% and 22%, respectively[19].

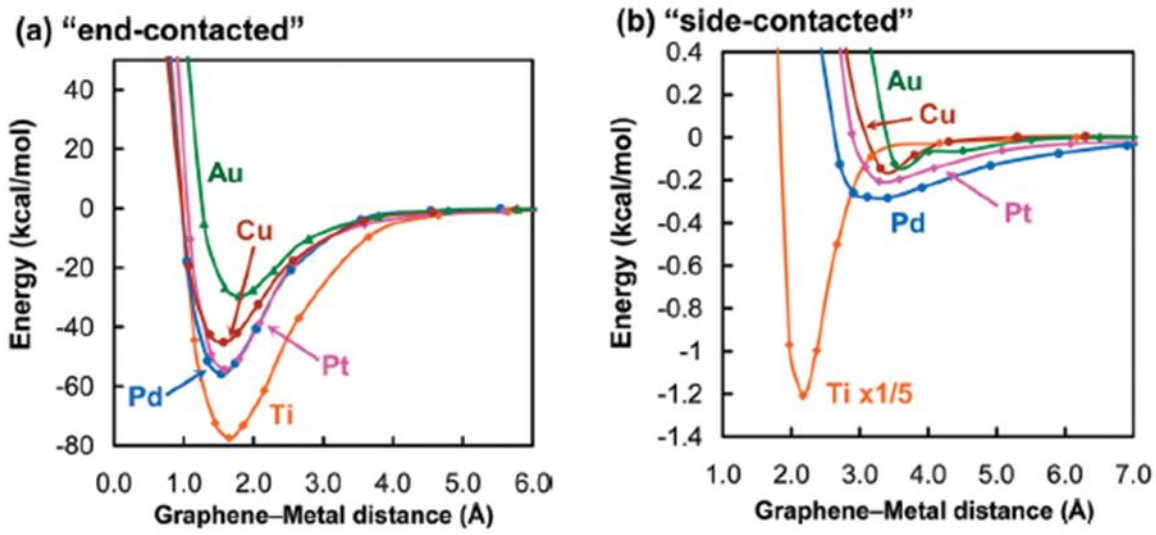


Figure 13: Interaction energy per carbon atom in a) end contact mode graphene and b) side contact mode graphene (Ti is multiplied by 1/5). Figure was taken from[37]

2.3.2 Experimental results

Recently, Smith et. al and co-worker [19] experimentally show that increasing edge contact length can reduce contact resistance graphene devices. This can be achieved by introducing cuts in graphene under the metal area to increase edge contact length as shown in Figure 14a, and the contact resistance improvement was observed after annealing process. However, after certain number of cuts (e.g. 8 cuts) the graphene channel under metal becomes thin (less than 40 nm), which increases the contact. This phenomenon observed due to the scattering of electrons and band gap widening[19]. Epitaxial graphene was used in this study and measurement was done for short channels (<1.5 micron) Cu contacts and for longer channels (> 1micron) for Pd contacts. E-beam lithography (PMMA resist) and lift-off process was used for fabrication of the devices.

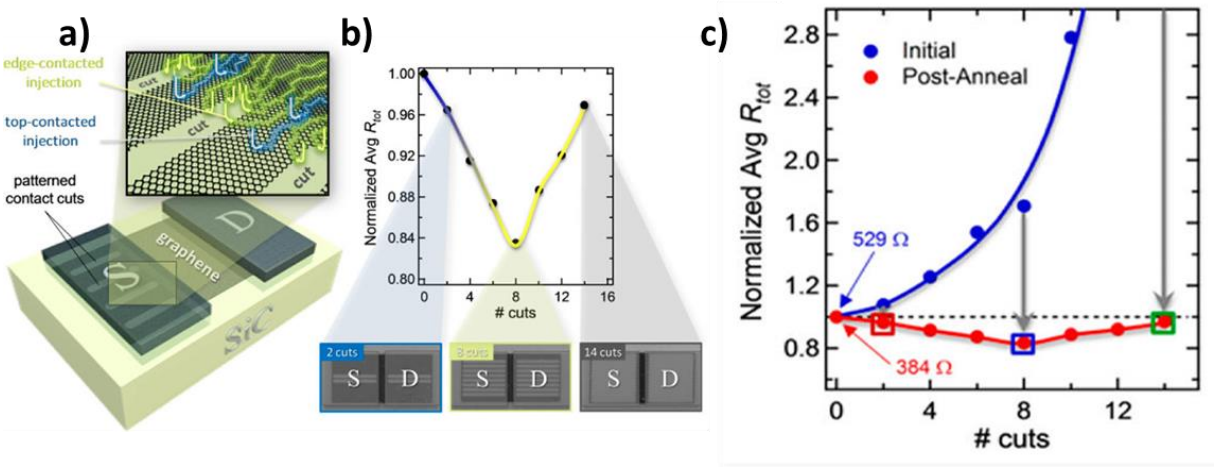


Figure 14: a) Schematic of patterned contact cuts under metal contact. b) Total resistance change as a function of number of cuts. c) Total resistance of graphene devices before and after annealing process. Figure was taken from [19]**.**

However, all of improvements in contact resistivity were observed after annealing process (Figure 14 c). The annealing process was carried out in a high vacuum chamber at 350 ^{0}C for 15 hours. The contact resistivity between Cu-graphene where improved by 32%, while for Pd-graphene the contact resistivity was improved by 22% after annealing process. By using epitaxial graphene and Cu contacts the minimum contact resistivity was recorded as low as$180\Omega\mu m$. It was also reported that a contact resistivity variation in a patterned graphene device was improved [19].The ratio of peripheral length to area effect is another parameter that affect thee contact resistivity, and it was reported that in the Au-graphene structure the end contact mode offer contact resistance 8.1×10^5 times lower than the side-contacted mode[38].

2.3.3 Transfer length increase due to edge contacts

Transfer length is another parameter that could affect the contact resistance in a graphene based devices. Recently, Song et al. [39]reported that by introducing nanoholes in graphene surface the transfer length is increased as shown in Figure 15a. Nanostructures were patterned by using EBL, where PMMA is used as a resist, and samples were annealed in vacuum at 300 ^{0}C for two hours before measurements. Using nanoholes with radius of 0.38 micron radius inside graphene under the metal contacts resulted in minimum contact resistance of $180\Omega\mu m$, in a CVD graphene and Pd (20 nm)/Au (30nm) structure.

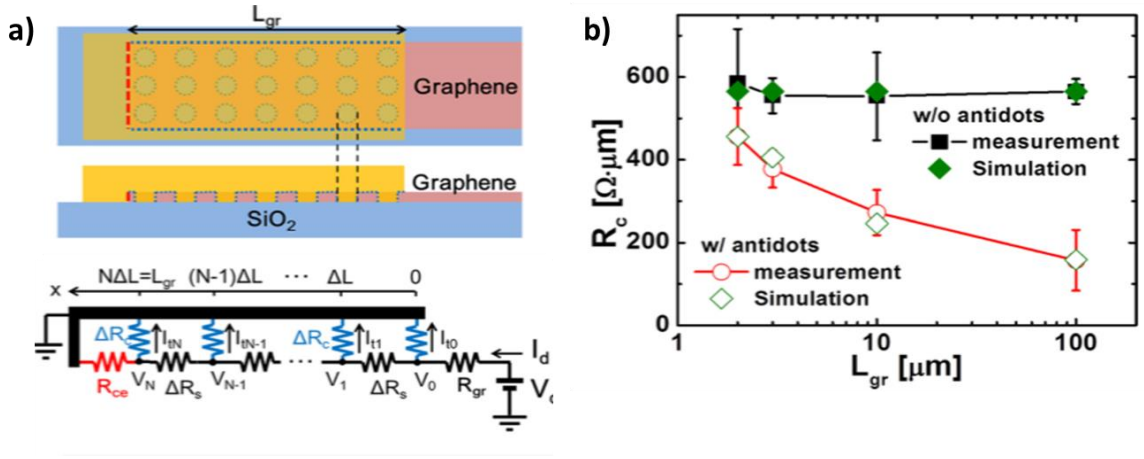


Figure 15: a) Schematic demonstration of top and side view of graphene based device. Bottom: one dimensional model for metal graphene contact b) Contact resistance as a function of length of graphene under channel. Transfer length was $20\mu m$, nanoholes radius are 0.38 μm. The transfer length in contacts without nanholes is $1\mu m$. Figure was taken from[39] **.**

In the Figure 15b, contact resistivity as a function of graphene length under the metal is shown. Reduction of contact resistance with respect to the length of the graphene under the metal indicates that transfer length is large which was not observed on the devices without nanoholes. Transfer length for their devices was shown to be $\sim 20\mu m$ (nanoholes with radius of 0.38 micron), while in contacts without nanholes is $\sim 1\mu m$. [39]

2.3.4 Metal catalyzed etching for low contact resistance

Leong et. al.[40] demonstrated that metal catalyzed etching of graphene can significantly decrease contact resistivity of the graphene devices . E-beam lithography, oxygen plasma etching and thermal evaporation were used for graphene devices fabrication. In order to obtain the graphene etch pits, a thin metallic layer up to 2 nm (e.g. Ni) is deposited by using electron beam evaporation followed by annealing process at temperature of 580 ^{0}C for 30 min in Ar/H_2 environment. Then, 100 nm thick Ni is deposited as contacts as it is shown in Figure 16 a. The chemical reaction between the carbon atoms in graphene and etchant gas (i.e. H2) during the etching process is given by;

$$C(solid) + 2H2(gas) \rightarrow CH4(gas)$$

where Ni acts as catalyst. This process provides with zigzag edge of the graphene which is the major reason for reduction of graphene contact resistivity. Hexagonal etch pits were observed after annealing process as shown in Figure 16 b and 16c. The average contact resistance by using this

technique was reported as low as $89\Omega\mu m$ and no significant improvement was observed after annealing process[40].

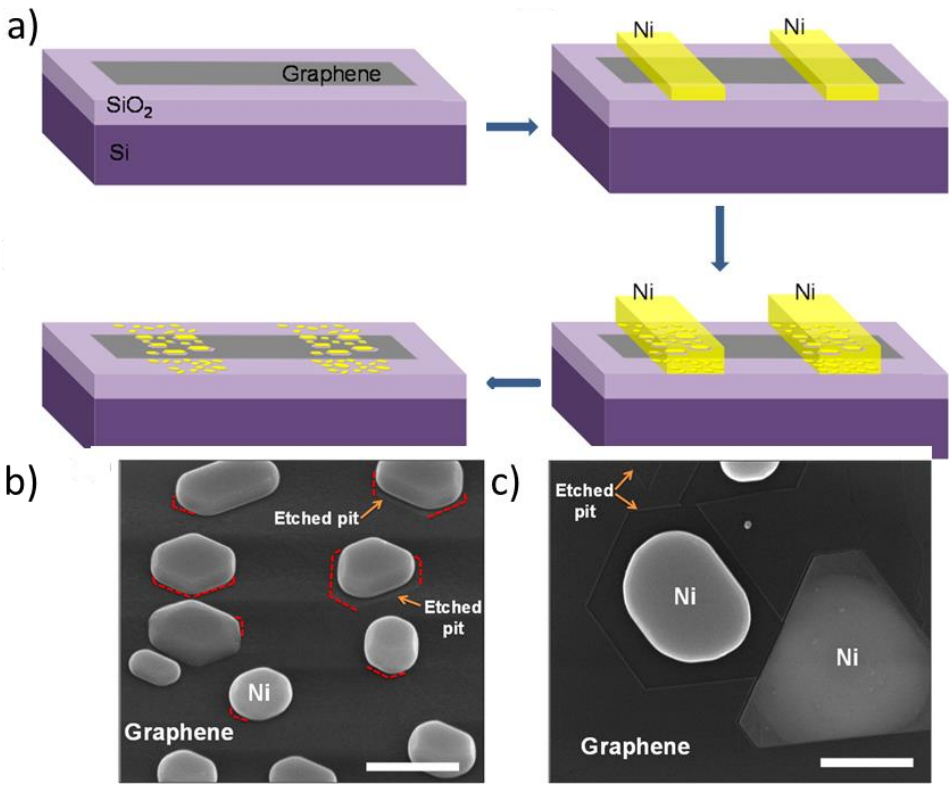


Figure 16: a) Schematic diagram of fabrication process of nickel-etched-graphene contacts. b) The SEM image of etched pits on few layer graphene at 45^{o}. C) SEM image of hexagonal etched pits etched pits. Scale bar is 500nm. Figure was taken from [40]**.**

2.3.5 N-type doping and edge contact for Ti, Cu, Pd

Recently, Park et. al.[41] reported that contact resistivity of graphene can be considerably reduced when combination of n-type doping and edge contact mode patterning is used. It was reported that by using poly(4-vinylphenol)/poly(melamine- co -formaldehyde) (PVP/ PMF) as dopant, N-type doped graphene was achieved when PMF concentration is larger than 200%. CVD graphene was used in this process and PVP/ PMF was spin coated on graphene before transferring it to the SiO_2/Si substrate. Optical lithography was carried out to isolate graphene and EBL was used for edge contact patterning. Contact resistance for side contact geometry was found to be lowest for Pd (Figure 17 a). While, the difference in contact resistivity between Ti, Cu and Pd after n-type doping by PVP/ PMF

was very small (Figure 17 b). Interestingly, it was shown that Ti contacts provide lowest contact resistivity following by Cu, Pd. Further reduction of contact resisitivity for edge contact mode is observed when n-type doping is used which is shown in the Figure 17 d.

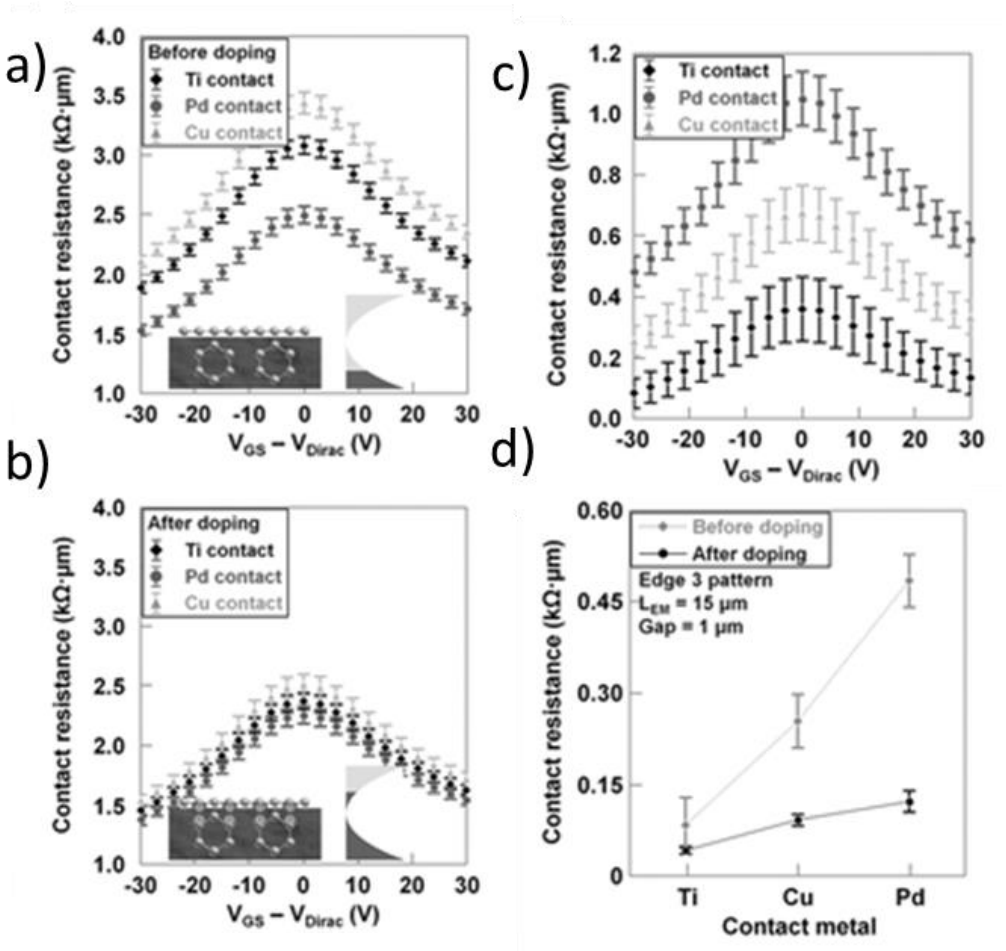


Figure 17: Contact resistance as a function of V_{gs}-V_{Dirac} for Ti, Pd and Cu. a)side contact mode, b) side contact mode and n-type doping, c) edge contact mode and d) contact resistivity for Ti, cu, Pd for edge contact mode before and after n-type doping. The V_{gs} and V_{Dirac} are gate bias voltage and Dirac point voltage respectively. Figure was taken from [41].

2.4 Conclusion

Reduction of graphene-metal contact resistance can be achieved by clean interfaces, selection of the metals, and edge contact. Reduction via edge contact mode seems to be very promising because it enables to achieve very low contact resistivity values. Length of the edge contact can be controlled by using lithographic methods which is desirable for having consistent results through process. Further, research can be done for achieving lower contact resistance values. This may include increasing edge contact length by creating smaller nanostructures in graphene also different shapes can be used. Comparative study using different metals should be done for edge contact mode such as Au, Ni, Co.

Chapter 3
Experimental

3.1 Introduction

Fabrication process for graphene devices should be carefully considered. In this chapter, fabrication process of back-gated graphene transistors will be discussed in detail.

. Single layer CVD graphene placed on top of 285 nm thermally grown SiO_2/p-Si wafer was purchased from Graphene Supermarket where. p- Si substrate will be used as back gate. The CVD graphene is polycrystalline since it was grown on a polycrystalline Cu foil.

The SEM image of single layer graphene used in this study is shown in Figure 18. In lens detector senses low energy electrons which are generally emitted from the very surface. Blue arrows indicate graphene wrinkles, while yellow multilayer graphene islands as shown in the Figure 18

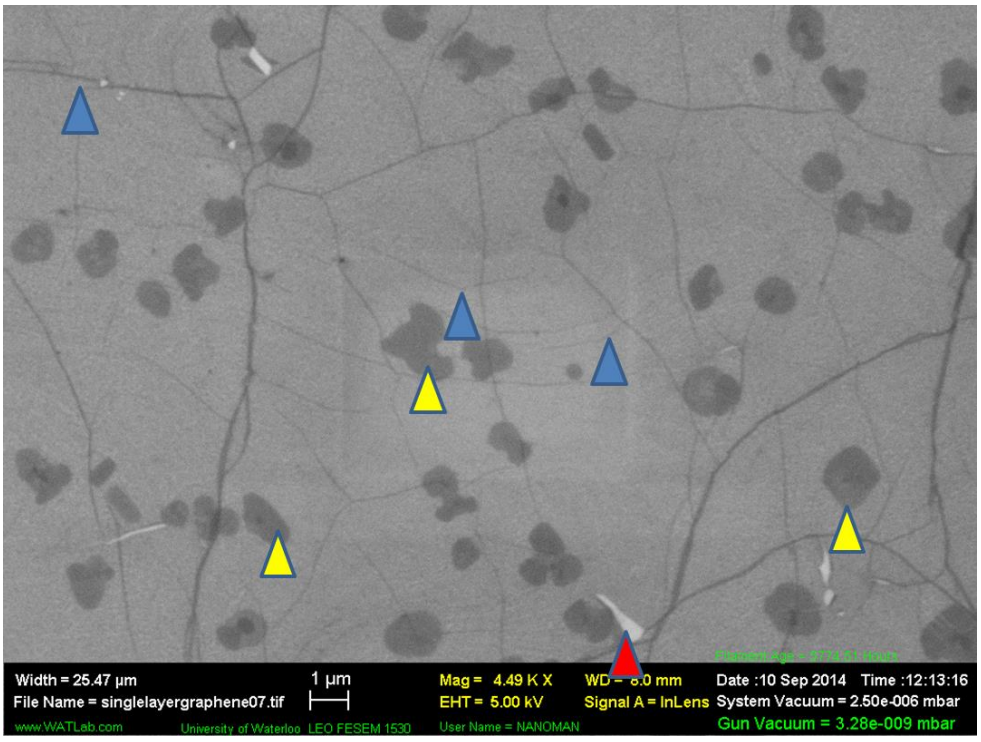


Figure 18: The SEM image of single layer CVD graphene on SiO_2/p-Si. Yellow triangles indicate: multilayer domains of graphene. Blue triangles shows graphene wrinkles due to thermal expansion mismatch between graphene and copper and red triangle shows cracks

.

3.2 Fabrication Steps

3.2.1 Alignment markers

The alignment markers were patterned using electron beam lithography followed by reactive ion plasma (RIE) etching process and metallization. A 180nm thick PMMA (950K MW, A3) was spin coated at speed of 2000 rpm and post baked at 180 ^{0}C for 15 min on the graphene sample. Alignment markers were exposed using exposure dose of 120 $\frac{\mu C}{cm^2}$ at 10kV acceleration voltage, and 30 μm aperture. Then sample was developed using Methyl Isobutyl Ketone (MIBK)1: isopropyl alcohol (IPA3) for 30 second . The reactive ion plasma etching process was carried out using oxygen as etchant gas at flow rate of 10sccm, power of 50W, platen diameter 200 mm, for 20 sec and pressure of 100 mTorr to etch graphene and to improve the adhesion of alignment markers to the substrate. In the next step, the electron beam evaporation (EBE) was used to deposit Ti (1 nm)/Au(20 nm) with the rate 0.05 and 0.1 nm/s respectively . In the last step, samples were immersed in acetone overnight for lift of process to be completed. Figure 19 shows optical images fabricated alignment markers in a graphene/SiO_2/Si wafer

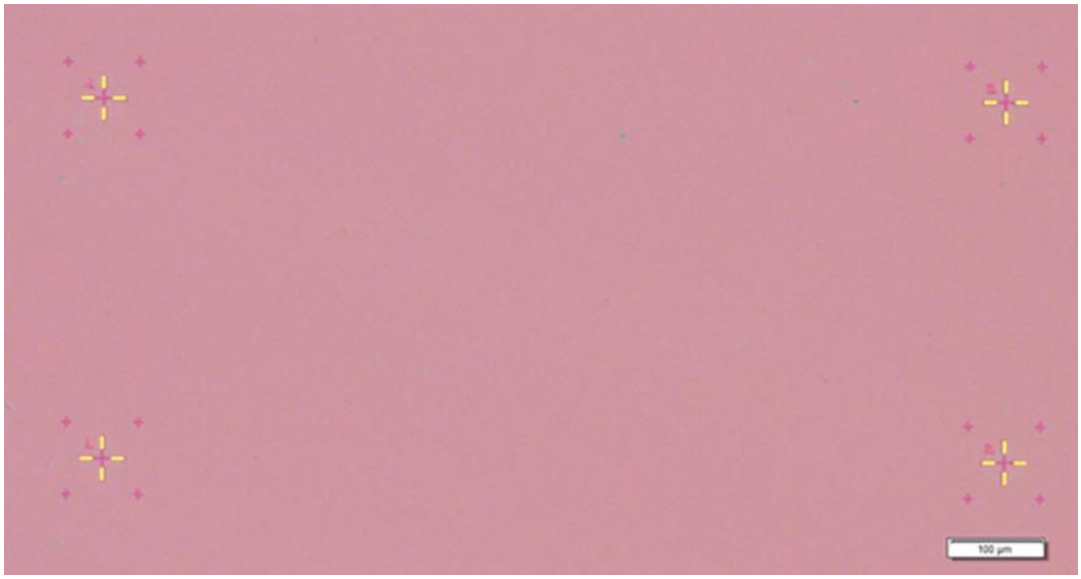


Figure 19: Optical images of alignment markers. Large crosses are alignment makers, while small ones alignment markers for write field alignment.

We also tried to depositing alignment markers and contact pads at the same time in order to reduce number of fabrication steps. In this scenario, 430 thick PMMA (950K, A6) was spin coated at speed of 5000 rpm and baked at 180 ^{0}C for 1 min to higher thickness is needed for lift-off process where our metal thickness is ~100nm . The sample was exposed with electron beam at exposure does of 160 $\frac{\mu C}{cm^2}$., at 10kV acceleration voltage, and 30 μm aperture. Then, oxygen plasma etching process was carried. Afterwards, Ti (1-5nm)/Au(100nm) was deposited using EBE technique at deposition rate of 0.05nm/s and 0.1 nm/s respectively for Ti and Au. In the last step, samples were immersed in the acetone overnight for lift off process.

3.2.2 Fabrication of holes in graphene and isolation

Graphene antidots were fabricated 200 nm thick PMMA (950K, A3) was coated on the graphene samples using spin casting technique at speed of 2000 rpm for 35 sec and was used as a mask and resist. The EBL was carried out to pattern a series of nanoholes with different diameters in the range of 100 nm to 300 nm. It is known that exposing the resist with higher acceleration voltage and smaller aperture improve the resolution of the structures due to the less scattering and higher depth of focus. Therefore, acceleration voltage of 25kV and 20 $\boldsymbol{\mu m}$ aperture was used to expose PMMA resist and.. Exposure dose test was performed before fabricating actual devices. The optimum exposure does and preset hole diameter were obtained as 311.84 $\boldsymbol{\mu C/cm^2}$, 90 nm, 311.84 $\frac{\boldsymbol{\mu C}}{\boldsymbol{cm^2}}$, 190 nm and 283.52$\boldsymbol{\mu C/cm^2}$ with designed structures 90,180, 280 nm respectively for nanoholes with diameter of 100 nm, 200 nm, and 300 nm (Figure 20).

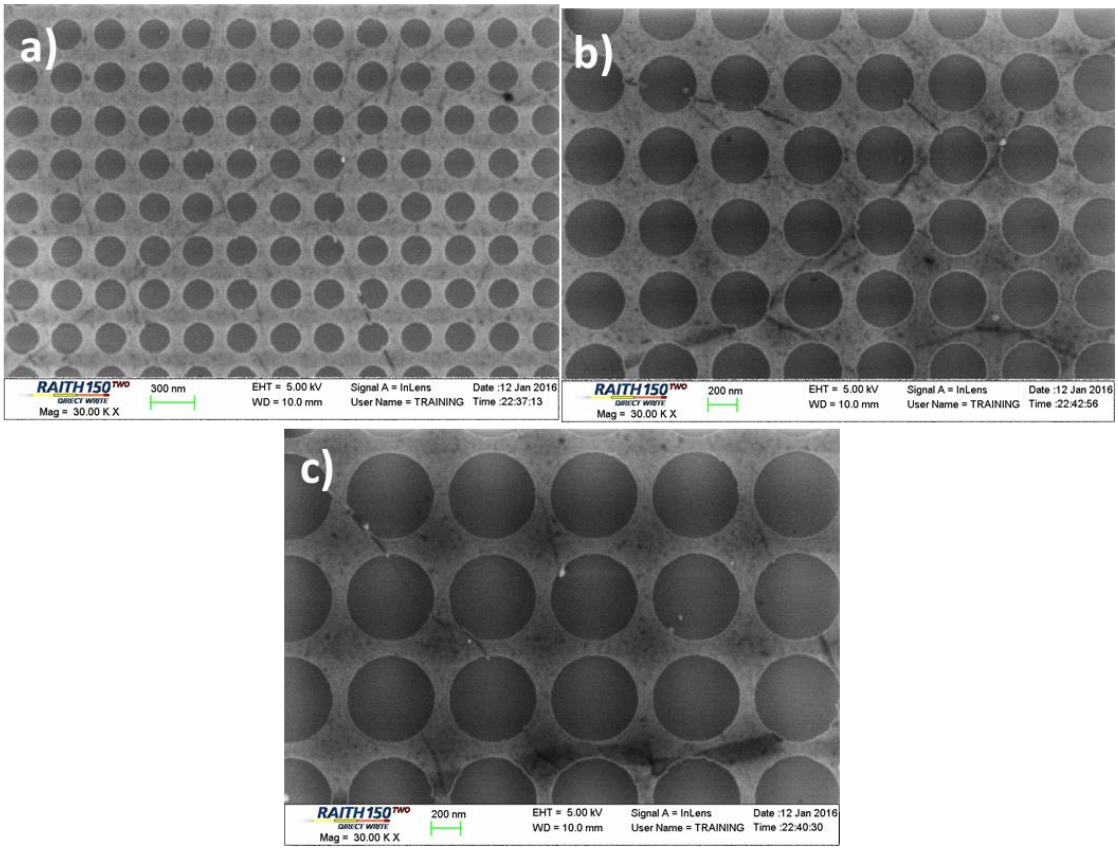


Figure 20 SEM image of graphene with holes of a)100nm , b) 300nm and c) 300nm radius.

In the next step, graphene was isolated as shown in Figure 21. It is possible to do it together with antidots; however, this graphene isolation process is a long time because of the small size of the aperture. In this process, the exposure was carried out at 10kV acceleration voltage, aperture size of 30 μm and exposure does of 120 $\frac{\mu C}{cm^2}$. After that the development process was carried out using MIBK1:IPA3 for 30 sec. followed by oxygen plasma etching which was described before.

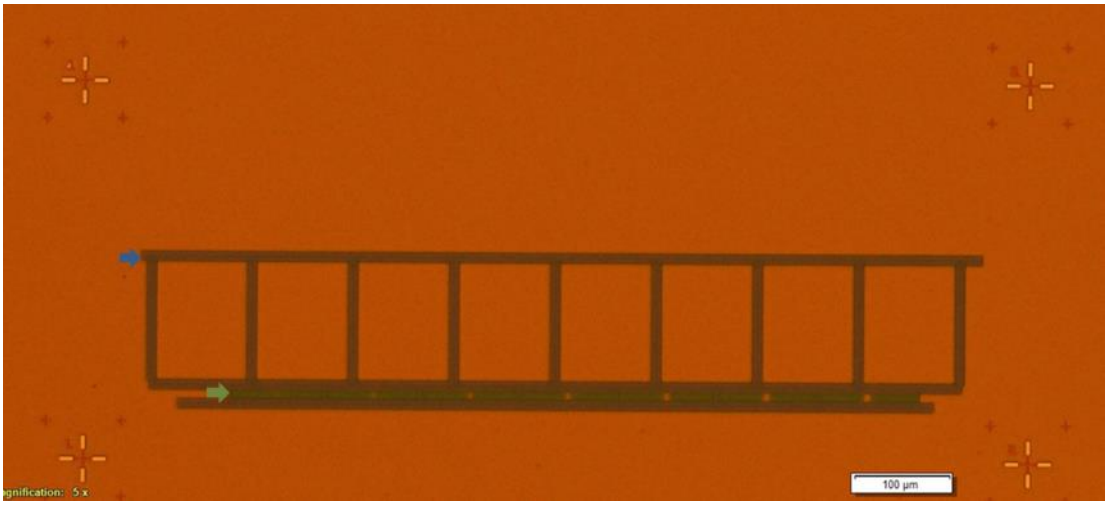


Figure 21: Optical image of graphene samples with antidots (green arrow) and isolation of graphene(blue arrow) where PMMA was used as a mask.

3.2.3 Metallization

In this step, a 180 nm thick PMMA was spin coated using the aforementioned parameters. The electron exposure does was set as 120 $\frac{\mu C}{cm^2}$ at 10kV acceleration voltage and aperture size of 30μm. After exposing the sample the development process was carried out using MIBK1:IPA3 for 30 s .Then, the Pd (20nm) /Au(30 nm) contacts were deposited using EBE technique at deposition rate of 0.05nm /s and 1nm/s respectively. In the final step the lift-off process was carried out by immersing the sample in acetone for one day. Figure 22shows the patterned contact on top of the graphene surface after lift-off process.

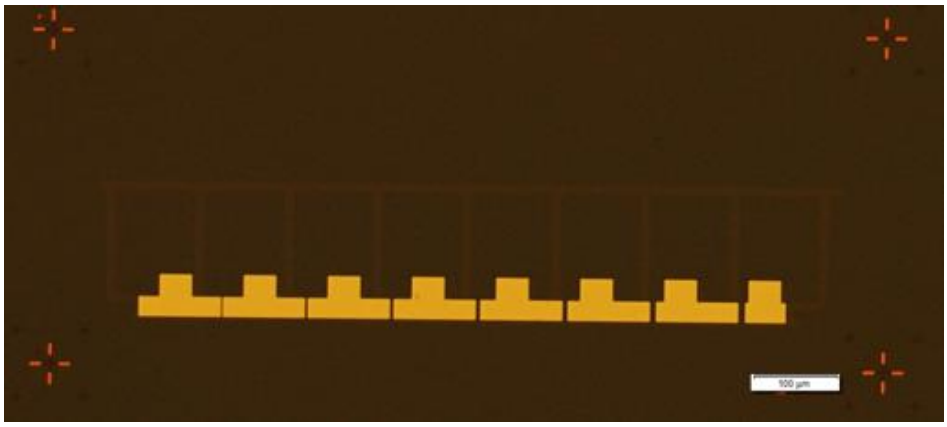


Figure 22: Optical image of contacts on top of graphene.

3.2.4 Contact pads

In the third lithographic step the metallic contact pads were fabricated using a 430 nm thick PMMA. The PMMA(950k and A6) was coated using spin coating technique at speed of 5000 rpm followed by baking at 180^{o}Cfor 1min min. The coated lithography resist was exposed by electron beams at electron dose of 160 $\frac{\mu C}{cm^2}$, 10kV acceleration voltage and aperture size of 60 μm. A higher aperture was used to obtain more current which allows reducing the writing time. After that, the development process was utilized by using MIBK1:IPA3 for 30 sec followed by reactive ion etching process using oxygen as described before. Then, Ti (1-5nm) as adhesion layer and 100 nm thick Au was deposited as metal contact using EBE at deposition rate of 0.05 nm/s and 0.1 nm/s respectively. Figure 22 shows the optical image of deposited metal contact after lift-off process.

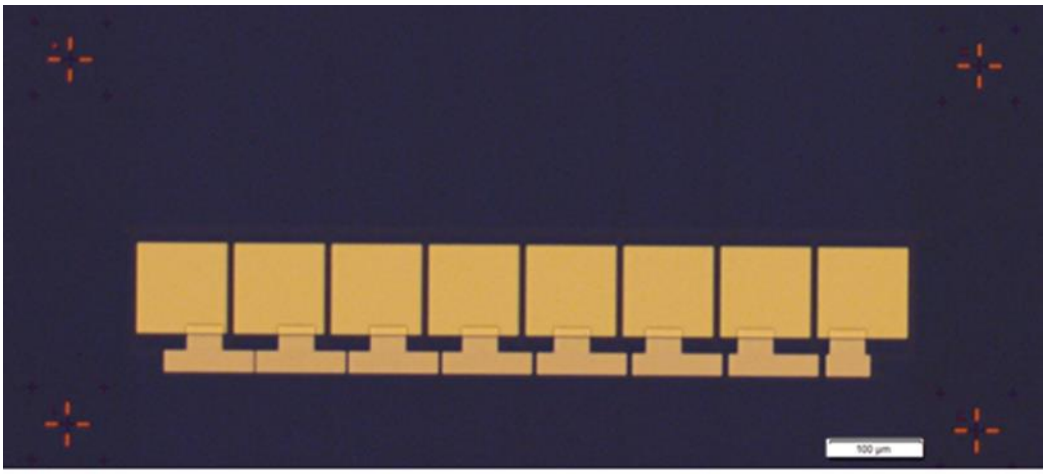


Figure 23: Optical image of contact pads. Large squares are contact pads

3.2.5 Passivation layer

Passivation layer were studied; however, TLM measurements were not done for devices with passivation layer due to some challenges which will be described in Chapter 4.

To protect the surface structure of the fabricated device from the ambient environment the passivation layer is required. Presence of H_2O and O_2 in the ambient environment can change the graphene to P-doped graphene through redox reaction $O_2 + H_2O + 4e^- \rightarrow 4OH^-$ [42]. By protecting the surface through passivation layer the hysteresis was reduced during the electrical measurements and more reliable results can be achieved[43].

Graphene devices without passivation layer were also measured and will be discussed in Chapter 4. Herein, Al seed layer of 2-3nm was deposited on top graphene by using EBE method and ~78nm of Al_2O_3 was used as passivation layer which was be deposited by using atomic layer deposition (ALD) technique (Figure 24).

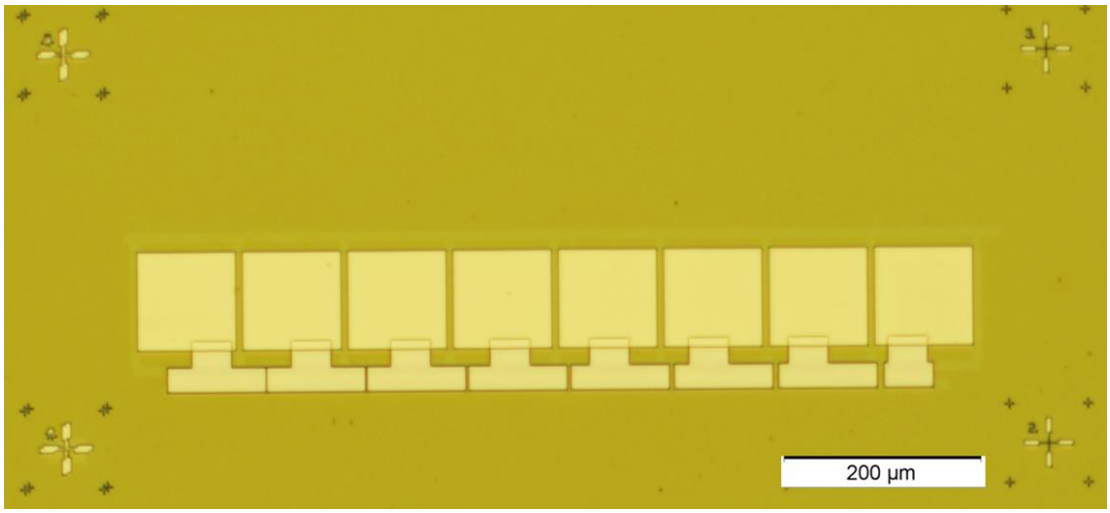


Figure 24 Optical image of TLM structure after Al_2O_3 deposition.

Because passivation layer will cover whole device structure including contact pads, one more lithography step followed by etching process will be required to etch Al_2O_3 from the metal contacts. Both wet etching and reactive ion etching process was tried. Wet etching was carried out by using MIF 319 developer which consists of 2.45% TMAH. This process was also used for removing 5 nm Al which was deposited as sacrificial layer in the beginning of the fabrication process [31].

Reactive ion etching process was carried out using Cl_2 and BCl_3 gas precursors as etchant gas. This process was also etched the PMMA very quickly. Therefore, thick PMMA (i.e. 1100 nm) was used as etching mask to protect the graphene surface during the etching process. Patterning was carried out using EBL at acceleration voltage of 25 kV, aperture size of 60 μm and exposure dose of 293$\frac{\mu C}{cm^2}$. It should be noticed that due to the high thickness of PMMA, high acceleration voltage was required to expose such a thick layer. High aperture size was used to reduce exposure time by achieving larger currents.

3.2.6 Gate fabrication

The substrate, P-doped Si, was used as gate because it is conductive. In GFETs without passivation layer SiO_2 (285 nm) was etched, while devices with passivation layer Al_2O_3(~78nm) and SiO_2(285nm) . Dry etching process was used for this process. PMMA(~430nm) layer together with thick photoresist (~Shipley 1811) was used as mask for this process. SiO_2 (285 nm) etching was done in RIE a process using O_2 and C_4F_8 as etchant gas at flow rate of 15 and 40 sccm, RF power of 200 W, ICP power of 2500 W, platen diameter 200 mm for 90 sec. Al_2O_3(~78nm) etching was done in RIE a process using Cl_2 and BCl_3 as etchant gas at flow rate of 10 and 40 sccm, RF power of 150 W, ICP Power 800 W platen diameter 200 mm for 90 sec.

3.3 Measurements

The probe station with Keithley 4200-SCS semiconductor parameter analyzer and Agilent 4155 C was used for electrical characterization. Measurements were carried out in ambient conditions. Resistance values are extracted from applied voltage in the range of -1 V to 1V where the I-V behavior was mainly linear. The bias voltage between source and drain was applied by 0.2 V step and gate bias was not used during these measurements. All measurements were carried out before and after annealing process.

Chapter 4
Results and Discussions

4.1 Fabrication issues

4.1.1 Resist residues

The resist residue is one of the most common issues in fabrication of graphene based devices as shown in Figure 25. There is no effective way to remove it by using solvents. The CVD graphene film is grown on Cu substrate then transferred to SiO2 (90 nm to 300 nm)/Si substrate. Generally PMMA is used as a mechanical support layer for graphene transfer[44]. PMMA residues also observed after transfer as discussed elsewhere [45] .One common technique which is used to remove the PMMA residue is annealing process in the Ar/H_2 environment at 250 ^oC and higher[46]. However, this process cannot be used after development process because it will exceed PMMA glass transition 106 ^oC); as a result, PMMA will flow to the structures. Amount of the resist residuals is increased after each lithography step and decreasing the number of lithographic steps is promising way to reduce the amount of resist residual. Also, reducing baking time and temperature of PMMA reduces amount of residues on the surface[45].

Descum process is common technique to remove resist residuals. This process involves O_2 plasma etching which is effective way to remove organic materials from the substrate. However, this process is also used to etch graphene. Also, slightly etching graphene can improve contact resistivity[28]. However, contact resistivity may change significantly because oxygen plasma treatment is not a controllable process.

Interestingly, residual layer can be observed on smaller structures when they are fabricated with higher electron doses in electron beam lithography followed by O_2 plasma etching.

In our initial trials to fabricate graphene transistor the resist residue were observed in a several cases. Therefore, reactive ion etching process was carried our using oxygen as etchant gas at low rate of 10 sccm, working pressure of 100mTorr , RF power of 50W for 5s to remove 3.5-5 nm PMMA residue before metallization. In order to fully remove graphene it was found that 20 s of etching is required. This process was used only in initial devices to avoid effect of plasma etching on contact resistance.

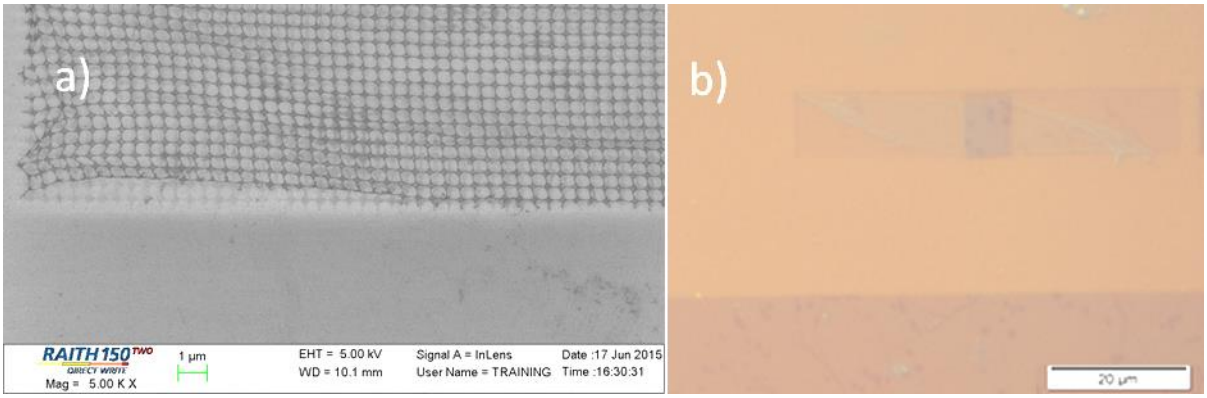


Figure 25: PMMA residues on top of graphene after patterning graphene. a) The SEM image of patterned structure with residual layer. b) Optical image of patterned graphene, the thin transparent layer on top of the structures is residual layer.

Further fabrication was optimized and reactive ion etching process before metallization was omitted in order to avoid any effects of plasma etching on contact resistivity of graphene transistors. Decreasing baking time of PMMA from 20 min to 1min after spin coating, result in reduction of PMMA residuals. In addition, graphene samples should not be reused. Reusing graphene samples leads to more number of steps which will result in more resist residuals. With considering these points, the resulted r structures on top of graphene was resist residue free as can be seen from Figure 26.

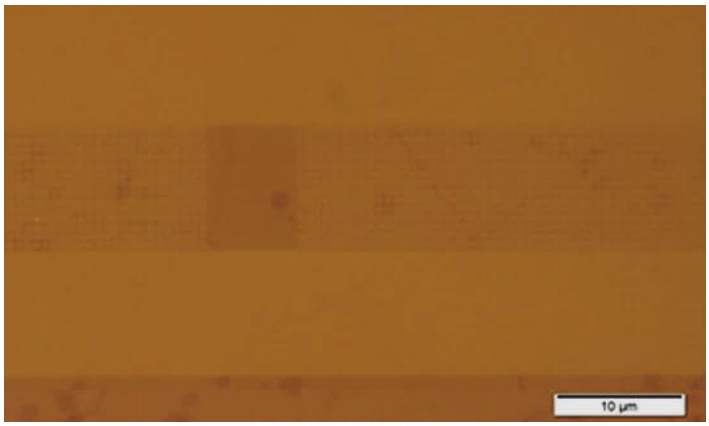


Figure 26: The optical image of fabricated graphene structure without resist residues

We have also tried to use sacrificial layer in order to avoid direct contact of graphene with resist Al sacrificial layer can be used[31]. Al sacrificial layer can be removed by light concentration (2.5%) of TMAH, which is also found in some developers [31]. By using this process clean graphene surfaces

can be obtained. However, several issues was faced during this process, one of the problems is wrapping of graphene after removing Al sacrificial layer. In the Figure 27 a), wrapping of graphene can be observed while for Figure 27 b) wrapping is not observed. In both of the cases graphene surface is clean. Graphene wrapping might appear due to thermal stresses. Wrapping is not observed Figure 27 b) because graphene is supported from the all sides. Also, this effect might be avoided by optimizing fabrication steps.

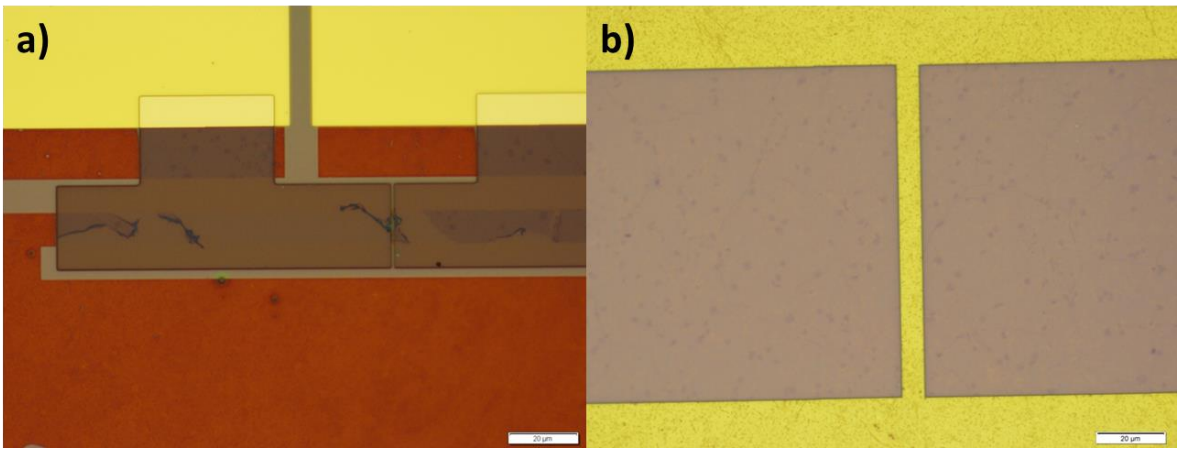


Figure 27: Optical image of graphene devices fabricated by using Al sacrificial layer. a)After removing Al sacrificial layer from the graphene channel where graphene was wrapped. B) after removing Al sacrificial layer from the contact pad area.

Even though, the problem with wrapping might be overcome, resist residue might appear in the surface especially if sample is reused several times. The reason for residual is due to the RIE etching of Al sacrificial layer which is used for fabrication of the holes. Some recipe as for Al_2O_3 RIE etching was used except time which is 12 sec. RIE process sometimes leave residues which then cannot be removed even with oxygen plasma etching process. In the Figure 28, residual layer for patterned structure can be seen, while no residual layer is observed for the structure without holes.

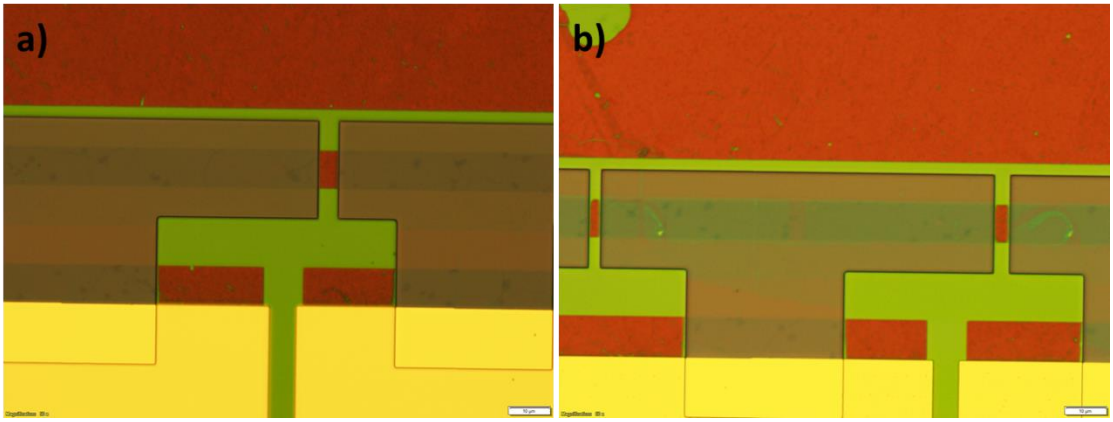


Figure 28 Optical images after removing Al sacrificial layer from the contact area a) for without holes b) with holes.

The presence of the resist residue in the fabricated structures could be due to the that heavily exposed PMMA and which behaves like a negative resist [47]. However, the electron doses that was used for exposure is less than those expected, which is about ten times more. Interestingly, this process usually occurs after oxygen plasma etching which is used to make holes in the graphene. Oxygen plasma etching may also contribute to scission of top ~0.5 micron layer [48] which means that PMMA is exposed during the reactive ion etching process. This might result in obtaining thin negative PMMA layer which cannot be removed by acetone.

In one of the cases, we tried to reduce number of steps leaving PMMA after generating nanoholes. After making nanoholes in graphene by using oxygen plasma etching where PMMA was used as mask, one more exposure was done for metallization. In this case as shown in Figure 29, the PMMA residues were observed in most of the structures. This might be due to the fact that leftover PMMA between structures was slightly exposed due to scattering in high density structures. Then reactive ion etching was resulted in more exposure. Finally, exposure for metallization might generate negative thin PMMA layer on top the graphene.

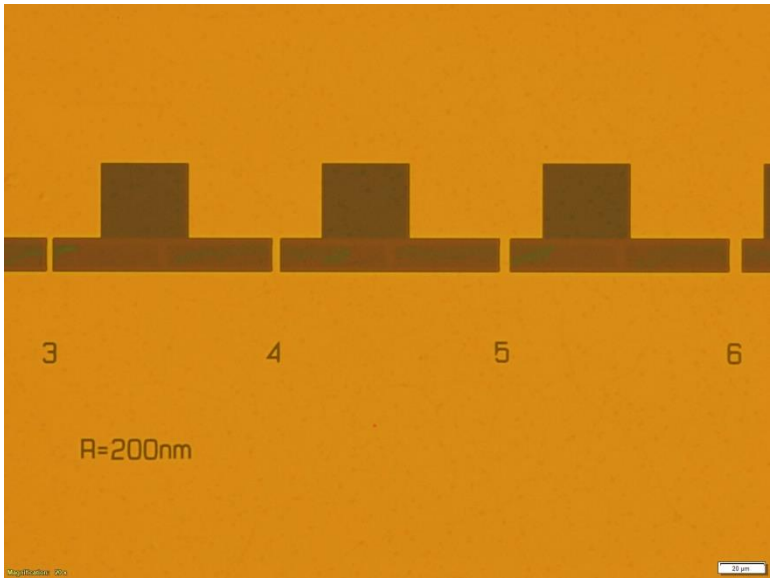


Figure 29 : The optical microscope images of graphene TLM structure after development process and metallization. Green residues can be observed on top of the structures.

4.1.2 Lift-off process

Samples were left in acetone for one day for lift-off process. Lift-off process is very sensitive in graphene substrate. Sonication process cannot be used in lift-off process because it may damage graphene as well as removing the patterned nanostructure from the graphene surface due to low adhesion between graphene and metals. Squirting acetone by pipette was done to help complete lift-off process after leaving samples in acetone for one day. This should be carried out carefully because high pressure can damage structures on top of graphene. Another method of improving lift-off process is to coat larger thickness of PMMA for better undercut; however, it cannot be a solution if small structures are required. Bi layer resists such as PMMA/MMA (copolymer), could be used to improve the lift-off process due to the better undercut. Also, hot acetone can be used for lift-off process.

4.1.3 Metallization

Pd(30nm)/Au(20nm) contacts were deposited using electron beam evaporation (INTLVAC-Ebeam) at deposition rates of 0.5Å/s and 1 Å/s for the Pd and Au respectively. Proper selection of deposition

rate and thickness of the metals is very important. Robinson et al.[28] reported that Al, Pt and Pd delamination was observed for the thickness more 15nm [28] without using adhesive layer.

Nevertheless, this issue was not reported by other authors probably due to different rate of deposition. Lower rates will result in low thermal stresses which will allow depositing thicker metals.
Metals generally do not adhere very well to graphene. It is very easy to clean graphene surface from Au metals just by touching it. Adhesive thin layer such as Ti and Cr can be used to improve adhesion of metals contact to graphene. In our previous studies Cr was used as a contact; however, a lot of cracks were observed after deposition 50 nm thick Cr at rate of 1 Å/s due to thermal stresses as shown in Figure 30. However; by reducing the deposition rate to 0.5 Å/s and metal thickness to 3 nm the effects of thermal stress can be improved and crack free film can be deposited.

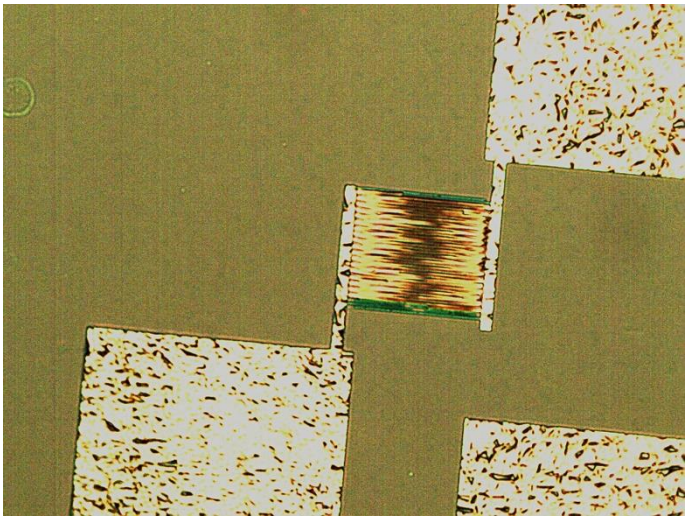


Figure 30: Cr contacts on graphene film with cracks. The Cr was deposition at deposition rate of 1Å/s and the total thickness of Cr is 50 nm.

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In this study Pd/Au was chosen because it shows lowest contact resistivity compare to the other metallic combination contact[22]. This Pd/Au contact layer could be easily damaged during measurement using probe station as it is shown in Figure 31.

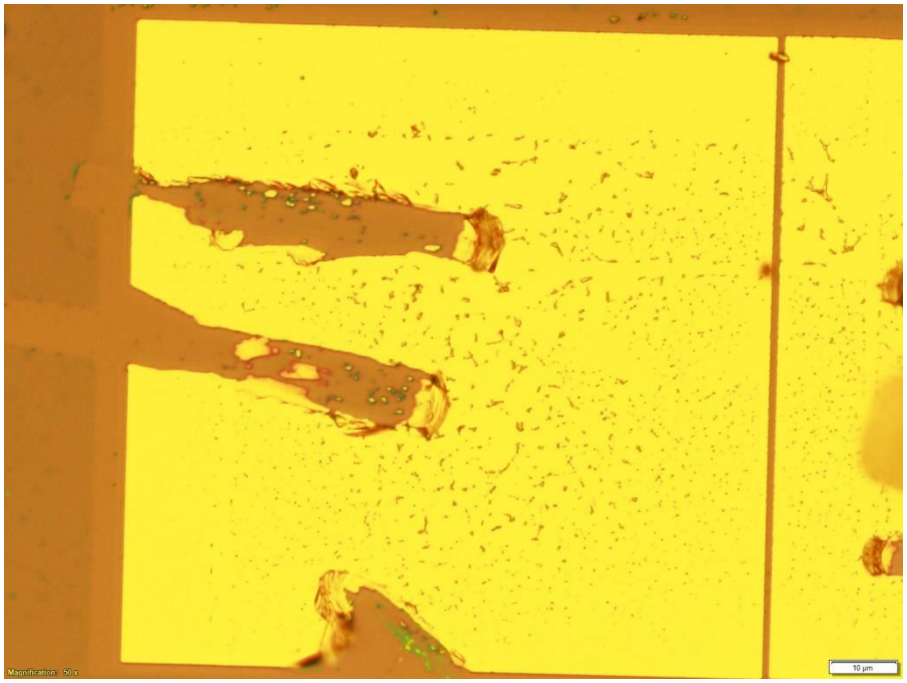

Figure 31: Pd/Au contact pads after measurement. Contact pads are damaged due to low adhesion to graphene which was easily scratched with the probes.

In order to avoid this issue, another metallization step was carried out after Pd/Au deposition where Ti (1-2nm)/Au(100nm) metal layer was deposited on top of SiO_2, where Ti is used to improve adhesion to the substrate.

4.1.4 Passivation layer

Passivation layer was used to protect graphene channels from the H_2O and O_2. Al_2O_3 layer grown by ALD is one of the best passivation layers for this purpose. After covering whole structure by Al_2O_3 (as shown in

Figure 24), alumina layer from the contact should be etched. PMMA has very low adhesion to Al_2O_3 which affects the etching process results. MIF 319, which is used to etch. Al_2O_3 can penetrate trough the edge of metal to graphene and wash it away. This problem can be used by improving adhesion between resist and Al_2O_3. For example, baking PMMA for the longer time (>15min).

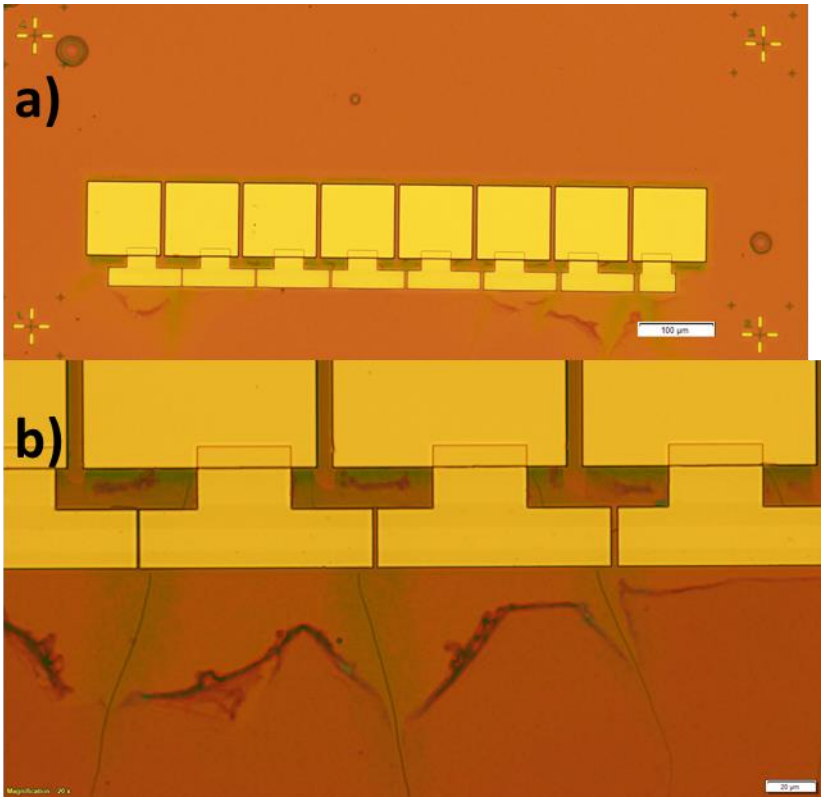

Figure 32 Optical images of TLM structures after Al_2O_3 wet etching from the contact pad area a) after annealing b) before annealing.

In addition, this process generates bubble like structures on top Al_2O_3 as shown in Figure 32 a) which was grown after annealing process. This problem can be solved by improving adhesion of resist to Al_2O_3. Improving adhesion between Al_2O_3 and graphene can be improved to avoid this issue. For example, thicker Al seed layer ~ 5nm can be used as adhesive layer.

Another way to etch Al_2O_3 is to use dry etching process. This process was successfully etched graphene. However, during measurements high gate leakage currents were observed. This problem was attributed to high DC bias during Al_2O_3 etching which was about ~390 V, breakdown voltage for 285 nm SiO_2 is about ~285V. Etching step should be optimized.

4.2 Electrical characterization

4.2.1 Preliminary work

In this section, preliminary results will be discussed. A series TLM structures were fabricated without optimized fabrication process and sacrificial layer. Resist residue was observed in most of the structure as shown in Figure 25 and oxygen plasma was used to remove it which was discussed previously in 4.1.1. Also, Al_2O_3 passivation layer was not used in these devices. Electrical measurements were carried out using probe station and semiconductor parameter analyzer (Keithley 4200-SCS and Agilent 4156C). Current between source and drain as function of bias voltage between source and drain was measured for all of the devices. In the Figure 33, the I-V curves of different channels with nanohole with diameter of 300 nm are compared. As can be seen from this Figure 33 a) the current was reduced by using longer channels as expected.

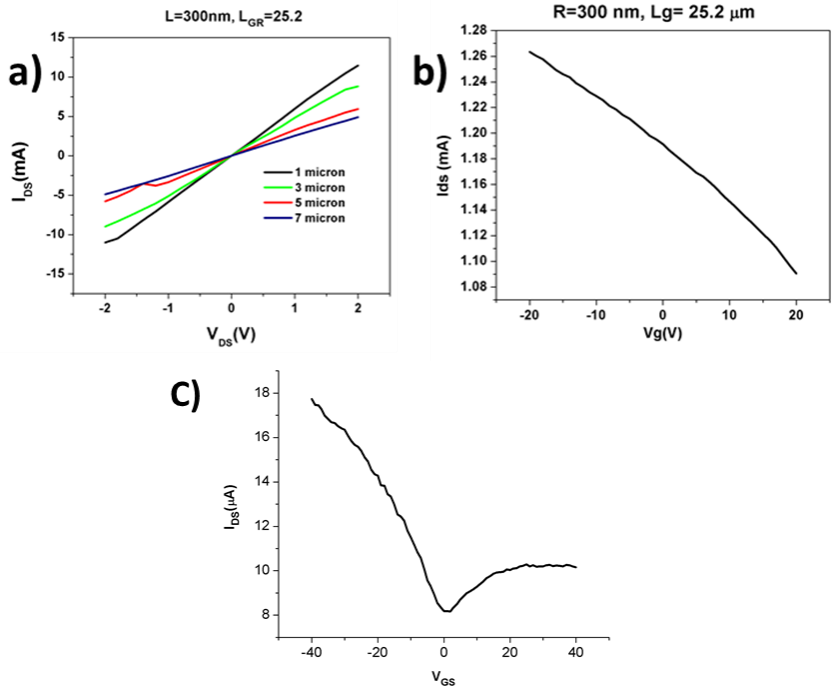

Figure 33: a) The measured current as a function of bias voltage between source and drain. b) The measured current form source and drain as a function of gate bias. The Lgr is graphene length under metal contact.c) The measured current form source and drain as a function of gate bias of GFET with passivation layer.

As can be seen from Figure 28, the graphene shows p-type behavior in all devices which might be due to the present of H_2O/ O_2 and resist residuals on graphene surface. In the Figure 33 c), GFET with passivation layer was measured, ambipolar behavior, where Dirac point is near to 0 V is observed because graphene channels are protected from the ambient. When the positive bias applied p-n-p junction is formed while for negative bias p-p-p junction; therefore, asymmetric behavior of the Figure 33 c) [17].

Total resistance as a function of channel length is shown in Figure 34. It was found that the total resistance was reduced by increasing the channel length as it is evident from Figure 34. It is also clear that there are small deviations from linear behavior which could be attributed to the non-uniformity of graphene film. The measurements are done after annealing. In some devices extremely high resistance were recorded which was due to the fact that channels was damaged during fabrication and annealing process.

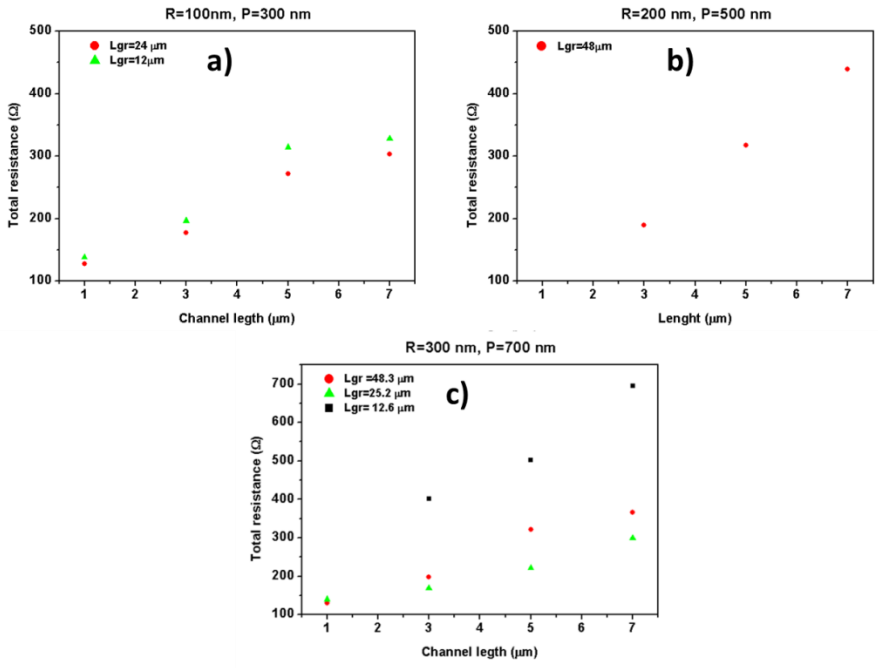

Figure 34 Total resistance as a function of channel length in graphene devices having antidots with radius of a) 100 nm, b) 200 nm and c) 300 nm. All measurements were carried out after annealing process.

In series of characterization the sheet resistances was calculated before and after annealing process by using transfer length method described in Chapter 2. It was found that calculated sheet resistance values were changed slightly after annealing process. Change in sheet resistance might due to the damage during annealing process. The annealing process was carried out using working pressure of 3×10^{-5} Torr and temperature of 300 ^{o}C for 2 hours Usually, annealing process was carried out at higher vacuum conditions where pressure is around $10^{-6}\ Torr$. It should be noticed that most of the short channels were damaged due to the thermal stress between metal and substrate. Figure 35 shows the calculated sheet resistance of survived samples before and after annealing process. The increase in sheet resistance after annealing might be attributed to damage during annealing process.

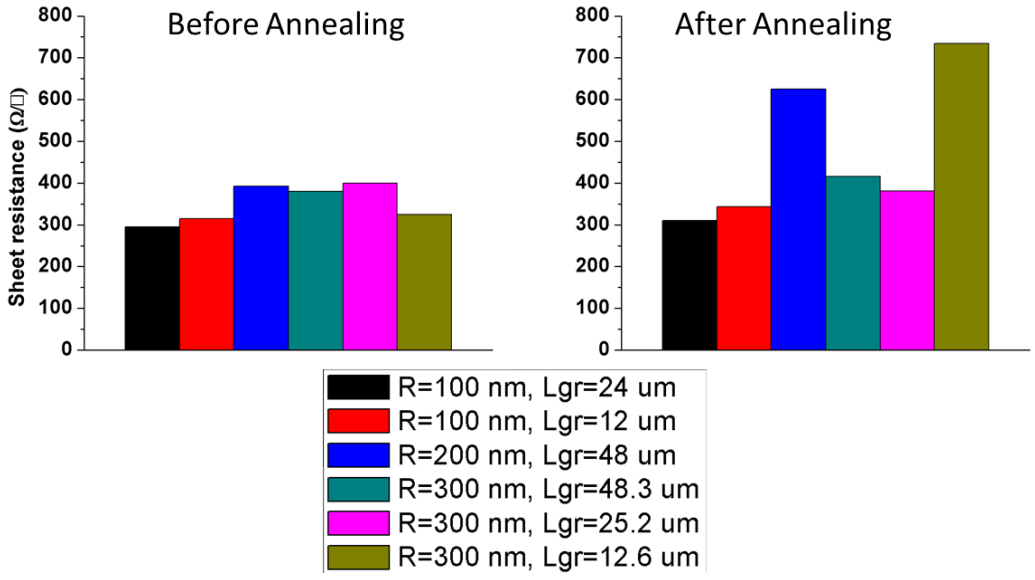

Figure 35: The calculated sheet resistance of fabricated devices before and after annealing extracted from TLM measurements.

The measured contact resistivities of different samples before and after annealing are compared in Figure 36. As can be seen from this figure there is no reduction pattern in the measured contact resistivity before annealing However, after annealing the measured contact resistivity was reduced for the longer graphene length under metal as it is clear from Figure 36. The reduction in the measured contact resistivity could be attributed to increasing the transfer length as result of present of antidots in the structure. This also supports the idea that transfer length is increased when antidots are present [39]. Interestingly, in one of the structures contact resistivity as low as $14\Omega\mu m$ were measured for

antidots with radius of 200 nm. Although, the lowest contact resistivity is observed for 200nm radius antidots, more study is required to confirm the low contact resistivity in the proposed structure. Also, slight plasma etching might affect contact resistivity.

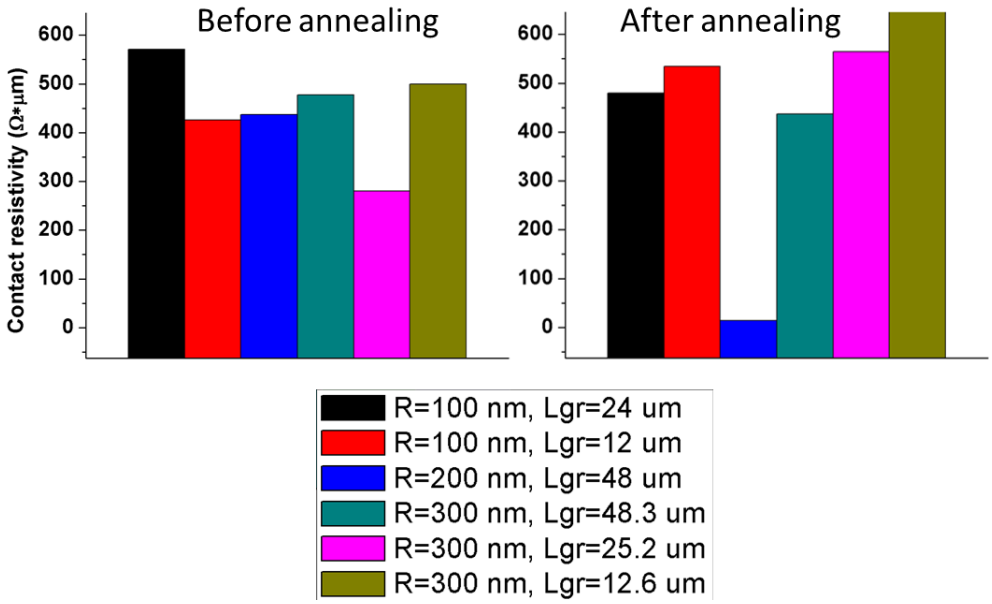

Figure 36: The measured contact resistivity of graphene field effect transistor before and after annealing. The Lg is graphene length under metal contact.

4.2.2 Devices with optimized fabrication process

In this section, results of electrical characterization of TLM structures fabricated by optimized process are presented. In the optimized process, clean interfaces were obtained through the reduction of baking time and minimizing number of PMMA depositions. Produced TLM structures have nanoholes with radius of 100 and 300 nm, and graphene length under metal contacts is ~48μm and ~48.3μm, respectively. Channel length of graphene devices varies between 1 and 7 micron with 7 different channels. More channels were fabricated to produce more reliable results. Graphene surface before metallization was relatively cleaner as shown in the Figure 26. Although I-V curves are linear for the longer channels, non-linear curves were observed for shorter channels as seen in curves taken between -1V and 1V, Figure 37 a).. Total resistance was also observed to be linearly dependent on channel length as previously seen in specimens before annealing. However, after annealing at 300 ^{o}C for 2 hours under vacuum environment, the deviation of data points from fitted linear curve is

reduced. Therefore, the total resistance becomes more linearly dependent on channel length (Figure 37 b)). Moreover, the results are more linear compared with preliminary results which are given the Figure 34. The improvement in electrical properties of optimized structures is attributed to clean interfaces, free of residual layer.

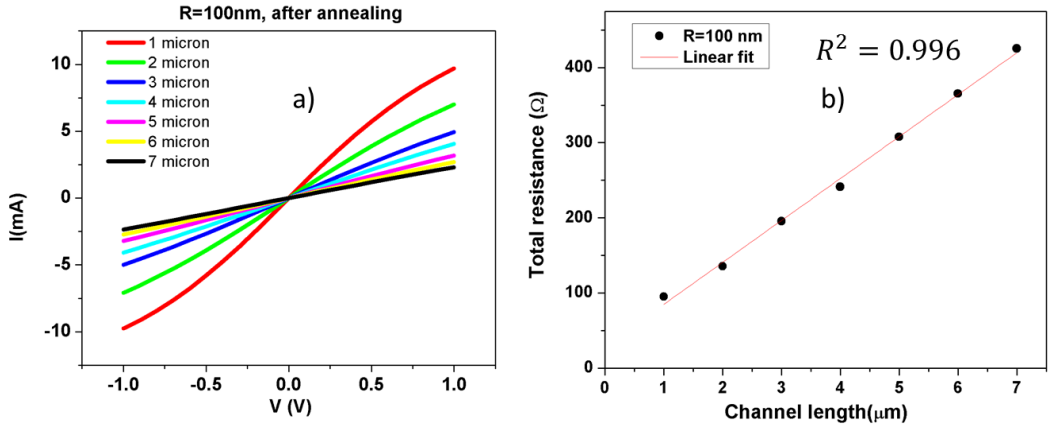

Figure 37 a) I-V curves for various channel lengths between 1 and7 micron. b) Total resistance versus channel length. These measurements were done after annealing. Both graphs are taken from graphene devices having nanoholes with radius of 100nm.

Sheet resistance and contact resistance values obtained after annealing at 300 ^{o}C for 2 hours as described in preliminary studies are shown in Figure 38. Sheet resistance values ~450 – 550 Ω/sq are close to the values provided by vendors. Significant reduction in contact resistivity is observed in the graphene devices with holes (Figure 38a)). In addition, remarkable improvement is observed in optimized process compared to preliminary work (see Figure 36 and Figure 38). Lowest contact resistivity, ~ 150$\Omega\mu m$, values are observed for graphene devices with holes of radius 100 nm. This result supports the idea that contact resistivity can be improved by increasing end contact length by having smaller hole radius.

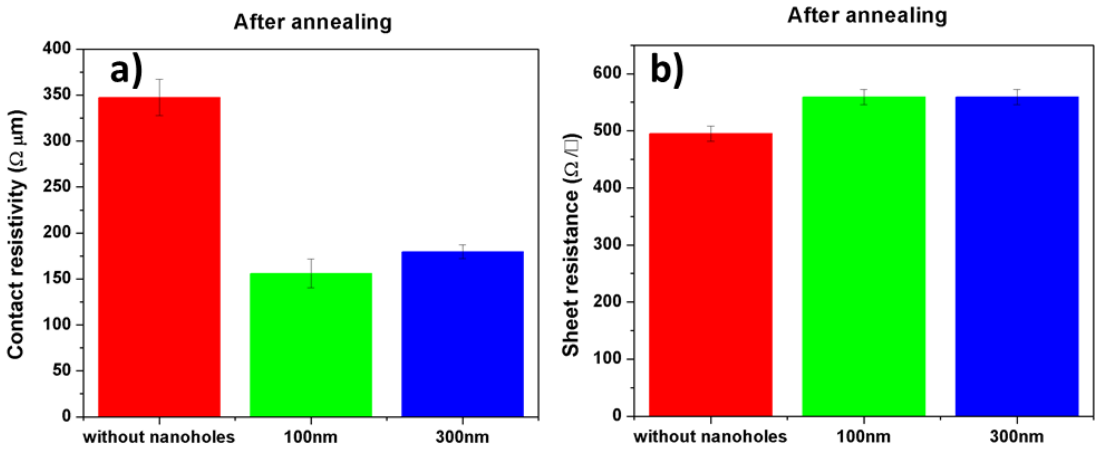

Figure 38 Dependence of a) Contact resistivity and b) sheet resistance on nanohole radius for graphene devices.

Chapter 5
Conclusion and Future work

5.1 Conclusion

Unique properties of graphene such as high charge carrier mobility can be used in various high speed electronic and photonic applications. One of the important challenges is to reduce graphene contact resistance .The contact resistance plays a significant role especially in the short channel devices. Clean surface should be achieved before metallization in order to have lower contact resistivity values. Therefore, special attention should be given during fabrication process including baking time and temperature of resist, and number of resist depositions on top of graphene. Moreover, contact metallization process variables should be carefully optimized to avoid cracking and delamination mainly due to thermal stresses. Since contact resistivity is also influenced by the type of metal, it is crucial to select proper metal for metallization. One of the promising methods to reduce contact can be achieved by increasing edge contact length. Furthermore, contact resistivity can be improved substantially through end contact mode geometry which can be achieved by introducing nanoholes in the graphene under metal. In this thesis, graphene devices with the hole radius of 100, 200, 300 nm were fabricated with different graphene length under metal contacts. Experimental results reveal that transfer length is increased in the presence of nanoholes under metal contacts. Furthermore, graphene devices fabricated using optimized process display lower contact resistance values due to the clean interfaces. It was shown that contact resistance as low as ~150 $\frac{\Omega}{sq}$ was obtained in devices with 100nm holes. These results obtained after annealing is more consistent probably due to enhancement of interaction between metal and graphene.

5.2 Future work

More TLM structures should be fabricated in order to make reliable statistical analysis and draw a general conclusion about contact resistance. In the current study, sheet resistance variations were measured in TLM structures. Since those variations may affect the calculated contact resistivity values, different measurement methods such as four-probe method should be utilized for comparison. Additionally, the effect of various metals like Ni and Co on contact resistivity should be studied by following the same fabrication process used in the current study. Because the effect of aforementioned metals have not been reported using the current fabrication process. Graphene

devices with passivation layer should also be studied to observe gate bias dependence of contact resistance. Passivation layer may reduce hysteresis during measurements. Although, it is possible to reduce contact resistivity by patterning graphene with EBL, this process is very expensive and cannot be used for large area fabrication. Lithography by self-assembly such as nano-shpere lithography and anodized aluminum oxide template (AAO), large area and cost effective production techniques, can be utilized for patterning of graphene. To the best of our knowledge, there is no work that shows reduction of contact resistance by using self-assembly lithography. Nevertheless, there are studies on patterning graphene by using nano-sphere lithography [49][50][51] and AAO [52][53][54]. Most of these studies concentrated on fabricating small neck in order to introduce band gap to graphene [52][53][54][50]. Introducing band gap should improve On/OFF ration of graphene transistors.

5.3 Published paper and Conference presentation

M. Irannejad, W. Alyalak, S. Burzhuev, A. Brzezinski, M. Yavuz, and B. Cui, "Engineering of Bi-/Mono-layer Graphene Film Using Reactive Ion Etching," Trans. Electr. Electron. Mater., vol. 16, no. 4, pp. 169–172, Aug. 2015.

S. Burzhuev, M. Irannejad, M. Yavuz,"Decreasing contact resistance in graphene devices by optimizing edge contact under metal", Graphene & 2D Materials International Conference and Exhibition, Montreal, Canada, 14-16 October, 2015.

Appendix A

Recipe for bottom gated graphene transistor

1. Obtain single layer CVD graphene on SiO_2(285 nm)/p-Si
2. Spin coat with PMMA
    a. PMMA A3,#steps=2, thickness about 180nm
        i. Speed=1000rpm, ramp=200rpm/s, time=1s
        ii. Speed=2000rpm, ramp=1500rpm/s, time=35s
    b. PMMA A6,#steps=2, thickness about 430nm
        i. Speed=1000rpm, ramp=200rpm/s, time=1s
        ii. Speed=5000rpm, ramp=1500rpm/s, time=35s
3. Baking at 180 ^{o}C for 1min on hot plate
4. E-beam lithography at EHT=10kV using 30 micron aperture
    a. $120\mu C/cm^2$ dose for large structures and thin PMMA film (180nm)
    b. $160\mu C/cm^2$ dose for large structures and thick PMMA film (430nm)
5. E-beam lithography at EHT=25kV using 20 micron aperture
    a. 311.84, 311.84 and 283.52$\mu C/cm^2$ with designed structures of 90, 180, 280 nm to obtain 100, 200 and 300nm holes, respectively.
6. Development
    a. MIBK1:IPA3 for 30s
    b. Rinse in IPA for 30s
7. Oxygen plasma etching to etch graphene
8. E-beam evaporation
    a. Ti/Au
        i. Thickness 1-0.5/20nm, rate 0.05/0.1 nm/s, respectively.
    b. Pd/Au
        i. Thickness 20/30nm, rate=0.05/0.1 nm/s, respectively.
    c. Ti\Au
        i. Thickness 1-2nm/100nm,rate=0.05/0.11 nm/s, respectively.
9. Lift-off
    a. Leave samples in acetone overnight
    b. Squirt acetone by pipette

Details of Steps for production of bottom gated transistor

1. Alignment markers
    a. Spin coat PMMA(2a)
    b. Bake (3)
    c. E-Beam lithography(4a)
    d. Development (6)
    e. Etching graphene (7)

f. Metallization (8a)
g. Lift-off (9)

2. Isolation, and nanoholes
    a. Spin Coat PMMA (2a)
    b. Bake (3)
    c. Expose (4a,5c)
    d. Development (6)
    e. Oxygen plasma etching (7)
    f. Remove PMMA with acetone (9a)

3. Metallization
    a. Spin Coat PMMA(2a)
    b. Bake (3)
    c. Expose(4a)
    d. Development (6)
    e. Metallization (8b)
    f. Lift-off (9)
4. Contact pads
    a. Spin Coat PMMA(2b)
    b. Bake (3)
    c. Expose(4b)
    d. Development (6)
    e. Metallization (4b)
    f. Lift-off (9)

5. Etching SiO_2 on backside (refer to experimental section for details)
    a. Spin coat by thick PMMA or photoresist
    b. Bake
    c. Etch by using RIE

    or

    a. Spin coat Photoresist (you can't use PMMA, use AZ photoresist)
    b. Bake
    c. Etch by using BHF

Bibliography

[1] a K. Geim and K. S. Novoselov, “The rise of graphene.,” *Nat. Mater.*, vol. 6, no. 3, pp. 183–91, Mar. 2007.

[2] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. L. Stormer, “Ultrahigh electron mobility in suspended graphene,” *Solid State Commun.*, vol. 146, no. 9–10, pp. 351–355, 2008.

[3] C. Lee, X. Wei, J. W. Kysar, and J. Hone, “Measurement of the Elastic Properties and Intrinsic Strength of Monolayer Graphene,” *Science (80-.).*, vol. 321, no. 5887, pp. 385–388, 2008.

[4] A. a. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, “Superior thermal conductivity of single-layer graphene,” *Nano Lett.*, vol. 8, no. 3, pp. 902–907, 2008.

[5] P. Avouris, “Graphene: Electronic and Photonic Properties and Devices.,” *Nano Lett.*, pp. 4285–4294, Sep. 2010.

[6] Y. Kopelevich and I. A. Luk’yanchuk, “Graphite vs graphene: scientific background,” *Nature*, vol. 50005, no. October, pp. 0–10, Nov. 2010.

[7] F. Xia, H. Yan, and P. Avouris, “The Interaction of Light and Graphene: Basics, Devices, and Applications,” *Proc. IEEE*, vol. 101, no. 7, pp. 1717–1731, Jul. 2013.

[8] T. Ando, Y. Zheng, and H. Suzuura, “Dynamical Conductivity and Zero-Mode Anomaly in Honeycomb Lattices,” *J. Phys. Soc. Japan*, vol. 71, no. 5, pp. 1318–1324, 2002.

[9] G. Eda, G. Fanchini, and M. Chhowalla, “Large-area ultrathin films of reduced graphene oxide as a transparent and flexible electronic material.,” *Nat. Nanotechnol.*, vol. 3, no. 5, pp. 270–274, 2008.

[10] W. a. de Heer, C. Berger, X. Wu, P. N. First, E. H. Conrad, X. Li, T. Li, M. Sprinkle, J. Hass, M. L. Sadowski, M. Potemski, and G. Martinez, “Epitaxial graphene,” *Solid State Commun.*, vol. 143, no. 1–2, pp. 92–100, Apr. 2007.

[11] A. Reina, X. Jia, J. Ho, D. Nezich, H. Son, V. Bulovic, M. S. Dresselhaus, and J. Kong, “Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition,” *Nano Lett.*, vol. 9, no. 1, pp. 30–35, 2009.

[12] K. S. Novoselov, a K. Geim, S. V Morozov, D. Jiang, Y. Zhang, S. V Dubonos, I. V Grigorieva, and a a Firsov, "Electric field effect in atomically thin carbon films.," *Science*, vol. 306, no. 5696, pp. 666–9, Oct. 2004.

[13] K. S. Novoselov, V. I. Fal'ko, L. Colombo, P. R. Gellert, M. G. Schwab, and K. Kim, "A roadmap for graphene.," *Nature*, vol. 490, no. 7419, pp. 192–200, Oct. 2012.

[14] F. Schwierz, "Graphene transistors," *Nat. Nanotechnol.*, vol. 5, no. 7, pp. 487–496, Jul. 2010.

[15] D. K. Schroder and L. G. Rubin, "Semiconductor Material and Device Characterization," *Phys. Today*, vol. 44, no. 4, pp. 135–149, 1991.

[16] H. H. Berger, "Contact Resistance and Contact Resistivity," *J. Electrochem. Soc.*, vol. 119, no. 4, p. 507, 1972.

[17] K. Nagashio and A. Toriumi, "Density-of-States Limited Contact Resistance in Graphene Field-Effect Transistors," *Jpn. J. Appl. Phys.*, vol. 50, no. 7, p. 070108, Jul. 2011.

[18] H. Xu, S. Wang, Z. Zhang, Z. Wang, H. Xu, and L. M. Peng, "Contact length scaling in graphene field-effect transistors," *Appl. Phys. Lett.*, vol. 100, no. 10, 2012.

[19] J. T. Smith, A. D. Franklin, D. B. Farmer, and C. D. Dimitrakopoulos, "Reducing contact resistance in graphene devices through contact area patterning," *ACS Nano*, vol. 7, no. 4, pp. 3661–3667, 2013.

[20] O. Balci and C. Kocabas, "Rapid thermal annealing of graphene-metal contact," *Appl. Phys. Lett.*, vol. 101, no. 24, p. 243105, 2012.

[21] S. Datta, *Electronic Transport in Mesoscopic Systems*, vol. 3. 1995.

[22] F. Xia, V. Perebeinos, Y. Lin, Y. Wu, and P. Avouris, "The origins and limits of metal-graphene junction resistance.," *Nat. Nanotechnol.*, vol. 6, no. 3, pp. 179–184, 2011.

[23] E. Watanabe, A. Conwill, D. Tsuya, and Y. Koide, "Low contact resistance metals for graphene based devices," *Diam. Relat. Mater.*, vol. 24, pp. 171–174, 2012.

[24] T. Mueller, F. Xia, M. Freitag, J. Tsang, and P. Avouris, "Role of contacts in graphene transistors: A scanning photocurrent study," *Phys. Rev. B*, vol. 79, no. 24, p. 245430, Jun. 2009.

[25] T. Mueller, F. Xia, and P. Avouris, "Graphene photodetectors for high-speed optical

communications," *Nat. Photonics*, vol. 4, no. March, pp. 297–301, 2010.

[26] H. Zhong, Z. Zhang, B. Chen, H. Xu, D. Yu, L. Huang, and L. Peng, "Realization of low contact resistance close to theoretical limit in graphene transistors," *Nano Res.*, vol. 8, no. 5, pp. 1669–1679, 2015.

[27] W. Li, Y. Liang, D. Yu, L. Peng, K. P. Pernstich, T. Shen, a. R. Hight Walker, G. Cheng, C. a. Hacker, C. a. Richter, Q. Li, D. J. Gundlach, and X. Liang, "Ultraviolet/ozone treatment to reduce metal-graphene contact resistance," *Appl. Phys. Lett.*, vol. 102, no. 18, 2013.

[28] J. a. Robinson, M. Labella, M. Zhu, M. Hollander, R. Kasarda, Z. Hughes, K. Trumbull, R. Cavalero, and D. Snyder, "Contacting graphene," *Appl. Phys. Lett.*, vol. 98, no. 5, pp. 2011–2014, 2011.

[29] C. Alvarado, C. Abhay, and D. Neumaier, "On the origin of contact resistances in graphene devices fabricated by optical lithography," *Appl. Phys. A*, pp. 2–6, 2016.

[30] W. S. Leong, C. T. Nai, and J. T. L. Thong, "What Does Annealing Do to Metal − Graphene Contacts ?," pp. 1–15, 2014.

[31] A. Hsu, H. Wang, K. K. Kim, J. Kong, and T. Palacios, "Impact of Graphene Interface Quality on Contact Resistance and RF Device Performance," *IEEE Electron Device Lett.*, vol. 32, no. 8, pp. 1008–1010, Aug. 2011.

[32] a. Pirkle, J. Chan, a. Venugopal, D. Hinojos, C. W. Magnuson, S. McDonnell, L. Colombo, E. M. Vogel, R. S. Ruoff, and R. M. Wallace, "The effect of chemical residues on the physical and electrical properties of chemical vapor deposited graphene transferred to SiO2," *Appl. Phys. Lett.*, vol. 99, no. 12, pp. 10–13, 2011.

[33] M. Ishigami, J. H. Chen, W. G. Cullen, and M. S. Fuhrer, "Atomic Structure of Graphene on SiO 2," 2007.

[34] C. Gong, H. C. Floresca, D. Hinojos, S. McDonnell, X. Qin, Y. Hao, S. Jandhyala, G. Mordi, J. Kim, L. Colombo, R. S. Ruoff, M. J. Kim, K. Cho, R. M. Wallace, and Y. J. Chabal, "Rapid selective etching of PMMA residues from transferred graphene by carbon dioxide," *J. Phys. Chem. C*, vol. 117, no. 44, pp. 23000–23008, 2013.

[35] C. W. Jang, J. H. Kim, J. M. Kim, D. H. Shin, S. Kim, and S.-H. Choi, "Rapid-thermal-annealing surface treatment for restoring the intrinsic properties of graphene field-effect

transistors.,” *Nanotechnology*, vol. 24, no. 40, p. 405301, 2013.

[36] C. Gong, S. McDonnell, X. Qin, A. Azcatl, H. Dong, Y. J. Chabal, K. Cho, and R. M. Wallace, “Realistic metal-graphene contact structures,” *ACS Nano*, vol. 8, no. 1, pp. 642–649, 2014.

[37] Y. Matsuda, W. Deng, and W. A. G. Iii, “Contact Resistance for ‘ End-Contacted ’ Metal - Graphene and Metal - Nanotube Interfaces from Quantum Mechanics,” pp. 17845–17850, 2010.

[38] C. Cho, S. K. Lee, J. W. Noh, W. Park, S. Lee, Y. G. Lee, H. J. Hwang, C. G. Kang, M.-H. Ham, and B. H. Lee, “Contact resistance improvement by the modulation of peripheral length to area ratio of graphene contact pattern,” *Appl. Phys. Lett.*, vol. 106, no. 21, p. 213107, 2015.

[39] S. Min Song, T. Yong Kim, O. Jae Sul, W. Cheol Shin, and B. Jin Cho, “Improvement of graphene–metal contact resistance by introducing edge contacts at graphene under metal,” *Appl. Phys. Lett.*, vol. 104, no. 18, p. 183506, 2014.

[40] W. S. Leong, H. Gong, and J. T. L. Thong, “Low-contact-resistance graphene devices with nickel-etched-graphene contacts,” *ACS Nano*, vol. 8, no. 1, pp. 994–1001, 2014.

[41] H.-Y. Park, W.-S. Jung, D.-H. Kang, J. Jeon, G. Yoo, Y. Park, J. Lee, Y. H. Jang, J. Lee, S. Park, H.-Y. Yu, B. Shin, S. Lee, and J.-H. Park, “Extremely Low Contact Resistance on Graphene through n-Type Doping and Edge Contact Design,” *Adv. Mater.*, vol. 28, no. 5, pp. 864–870, Feb. 2016.

[42] L. Zheng, X. Cheng, D. Cao, Z. Wang, C. Xia, Y. Yu, and D. Shen, “Property transformation of graphene with Al2O3 films deposited directly by atomic layer deposition,” *Appl. Phys. Lett.*, vol. 104, no. 2, pp. 3–8, 2014.

[43] A. A. Sagade, D. Neumaier, D. Schall, M. Otto, A. Pesquera, A. Centeno, A. Z. Elorza, and H. Kurz, “Highly air stable passivation of graphene based field effect devices.,” *Nanoscale*, vol. 7, no. 8, pp. 3558–64, 2015.

[44] J. W. Suk, A. Kitt, C. W. Magnuson, Y. Hao, S. Ahmed, J. An, A. K. Swan, B. B. Goldberg, and R. S. Ruoff, “Transfer of CVD-grown monolayer graphene onto arbitrary substrates.,” *ACS Nano*, vol. 5, no. 9, pp. 6916–24, Sep. 2011.

[45] G. Borin Barin, Y. Song, I. de Fátima Gimenez, A. G. Souza Filho, L. S. Barreto, and J. Kong,

"Optimized graphene transfer: Influence of polymethylmethacrylate (PMMA) layer concentration and baking time on graphene final performance," *Carbon N. Y.*, vol. 84, pp. 82–90, Apr. 2015.

[46] Y. C. Lin, C. C. Lu, C. H. Yeh, C. Jin, K. Suenaga, and P. W. Chiu, "Graphene annealing: How clean can it be?," *Nano Lett.*, vol. 12, pp. 414–419, 2012.

[47] I. Zailer, J. E. F. Frost, V. Chabasseur-Molyneux, C. J. B. Ford, and M. Pepper, "Crosslinked PMMA as a high-resolution negative resist for electron beam lithography and applications for physics of low-dimensional structures," *Semicond. Sci. Technol.*, vol. 11, no. 8, pp. 1235–1238, 1999.

[48] M. a. Hartney, "Oxygen plasma etching for resist stripping and multilayer lithography," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 7, no. 1989, p. 1, 1989.

[49] C. X. Cong, T. Yu, Z. H. Ni, L. Liu, Z. X. Shen, and W. Huang, "Fabrication of Graphene Nanodisk Arrays Using Nanosphere Lithography Fabrication of Graphene Nanodisk Arrays Using Nanosphere Lithography," no. March, pp. 6529–6532, 2009.

[50] N. S. Safron, A. S. Brewer, and M. S. Arnold, "Semiconducting two-dimensional graphene nanoconstriction arrays," *Small*, vol. 7, no. 4, pp. 492–498, 2011.

[51] X. Zhu, W. Wang, W. Yan, M. B. Larsen, P. Bøggild, T. G. Pedersen, S. Xiao, J. Zi, and N. A. Mortensen, "Plasmon–Phonon Coupling in Large-Area Graphene Dot and Antidot Arrays Fabricated by Nanosphere Lithography," *Nano Lett.*, vol. 14, no. 5, pp. 2907–2913, 2014.

[52] J.-H. Lee, Y. Jang, K. Heo, J.-M. Lee, S. H. Choi, W.-J. Joo, S. W. Hwang, and D. Whang, "Large-Scale Fabrication of 2-D Nanoporous Graphene Using a Thin Anodic Aluminum Oxide Etching Mask," *J. Nanosci. Nanotechnol.*, vol. 13, no. 11, pp. 7401–7405, 2013.

[53] D. Choi, C. Kuru, Y. Kim, G. Kim, T. Kim, R. Chen, and S. Jin, "Uniformly Nanopatterned Graphene Field-Effect Transistors with Enhanced Properties," *Nanoscale Res. Lett.*, vol. 10, no. 1, p. 289, 2015.

[54] Z. Zeng, X. Huang, Z. Yin, H. Li, Y. Chen, H. Li, Q. Zhang, J. Ma, F. Boey, and H. Zhang, "Fabrication of graphene nanomesh by using an anodic aluminum oxide membrane as a template," *Adv. Mater.*, vol. 24, no. 30, pp. 4138–4142, 2012.