Amorphous Transition-Metal-Oxides for Transparent Flexible Displays: Device Fabrication and Characterization

by

Alireza Tari

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Author’s Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

This Ph.D. dissertation presents the development and demonstration of optically transparent back-channel etched flexible InGaZnO (IGZO) thin-film transistors (TFTs) using a conventional TFT process flow implemented at low-temperatures. The study includes the development of the transition metal oxide (TMO) channel layers by relating the materials properties, surface topography, and chemical composition of the channel layer to the process integration of IGZO TFTs. Investigation of the process parameters included process temperature and post processing thermal-anneal on the electronic properties of the semiconductor and the effect of the chemical composition of the gate-dielectric layer on the active channel layer of TMO TFTs.

A bi-layer SiO_x/SiN_x gate dielectric was found to be an effective structure for high-performance IGZO-based TFTs compared to single dielectric layers. The SiO_x capping layer within the dual dielectric structure was found to be an effective hydrogen (H) diffusion barrier, preventing H contamination into the overlying semiconducting IGZO layer during the IGZO deposition, minimizing the generation of H induce oxygen vacancy (V_o) formation in the active IGZO channel. A low-temperature, 150˚C plasma-enhanced chemical vapor deposition (PECVD) process was used to produce TFTs having field-effect mobility, μ, of 5.7 cm^2/V.sec, sub-threshold swing, S.S., of 0.54 V/decade, and $I_{on/off} > 10^6$.

The same dual-dielectric stack was also found to be an effective passivation layer for back-channel etched IGZO TFTs. A low-temperature approach employing a thin room-temperature-deposited e-beam SiO_x barrier layer directly deposited onto the IGZO back-channel to prevent both the plasma damage and unintentional hydrogen (H) doping of the IGZO channel region.

In order to complete the process integration for fully transparent flexible TFTs, the development of the dielectric layers of the TFT structure were augmented by an investigation of ohmic transparent contacts patterned using selective wet-chemical etching. A high-selectivity wet-etch patterning process was developed to take advantage of the etch-rate differences between polycrystalline Al-doped ZnO (AZO) and amorphous (IGZO) TMO thin-films. This patterning technique resulted in the fabrication of back-channel etched flexible transparent IGZO TFTs using a conventional TFT process flow implemented at low-temperatures. A selectivity of nearly 20 was found for dilute HCl solution in water for patterning AZO source/drain electrodes on IGZO channel layers. The resulting patterned electrodes had a low contact resistance of < 19 KΩ and

high optical transparency of ~85%. The transparent back-channel etched flexible IGZO TFTs exhibited a μ of ~9.3 $cm^2/V.sec$, V_T of <5 V, and $I_{on/off}$ ratio of ~10^7.

Finally, the integration of the transparent semiconductor, dielectric, and conductive electrodes onto a flexible platform was demonstrated. Through a combination of the low-temperature processes developed in this work, the integration of transparent flexible TFTs onto polyethylene naphthalate (PEN) substrates was accomplished. The flexible IGZO TFTs had current-voltage (I-V) characteristics similar to their rigid counterparts. The fully encapsulated transparent devices had μ of ~6.7 $cm^2/V.sec$, V_T of ~1 V, and $I_{on/off}$ ratio of >10^6.

Electrical stability measurements of the flexible devices under tensile and compressive mechanical strain showed no appreciable change in the I-V characteristics during bending. The electrical characteristics under mechanical bending suggest that carrier transport is unaffected during mechanical strain due to the overlapping spherical s-orbitals in the IGZO conduction band. Testing under dc gate bias conditions, the electrical stability of the TFTs showed a positive V_T shift of 3.8 V after 3600 s without any change in subthreshold-swing (S.S.). Pulsed-gate recovery measurements also showed rapid recovery of the drain current, both of which suggest that the dominant aging mechanisms is charge trapping in the back-channel etched transparent flexible IGZO TFTs.

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Dedication

To my lovely uncle, Mr. Saeed Khalili, who showed me the meaning of life and taught me a lot.

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Chapter 1

1. Introduction

1.1. Introduction

Transparent flexible electronics have recently received great attention in active-matrix organic light-emitting diode (AMOLED) displays for large-area electronics applications ranging from heads-up displays and smart windows to flexible sensor arrays [1]. One of the main challenges in this area is fabricating high-performance transparent flexible thin-film transistor (TFTs).

Different active layer materials such as amorphous silicon (a-Si), low temperature polysilicon (LTPS), and organic semiconductors can be used as active layers of TFTs. A-Si has the advantages of both uniformity over a large-area and maturity in its fabrication process. However, due to the insufficient field-effect mobility of this material system, it is not possible to apply this class of TFTs to fabricating large-area (> 70 inches) OLED and high performance (resolution: 4000×2000 pixels, frame rate: 240Hz) LCD displays, which require a field-effect mobility of at least 3 cm^2/V.sec [2]. The electrical instability of a-Si is another drawback that restricts its application in the display industry. LTPS has been found to be a promising alternative for a-Si in the fabrication of AMOLED displays of mobile devices such as cellular phones, laptops, and navigation tools, due to its superior field-effect mobility (μ) and electrical stability. However, the electrical properties of LTPS suffer from large-area nonuniformity. Thus, in LTPS-based AMOLED displays, even of a small size (< 5 inches), uniform image quality requires the presence of compensation pixel circuits [2]. Higher processing cost is another limitation for developing LTPS-based displays [3]. On the other hand, due to the poor electrical stability and field-effect

mobility of organic materials, there is less possibility of this class of TFTs being used as an alternative for a-Si and LTPS in the near future. Several research groups have reported that grain boundary is the dominant factor in the deterioration of short-range uniformity, as is the case in polycrystalline silicon (p-Si) TFTs [4]. Hence, high-field-effect mobility amorphous semiconductors will be an ideal candidate in developing high-performance large-area electronics. However, researchers used to believe that the field-effect mobility of metal-oxide semiconductors significantly deteriorates after switching from crystalline structure to the amorphous phase. This degradation had been attributed to the strong scattering from the disordered structures, and deterioration of μ from 1500 $cm^2/V.sec$ in crystalline silicon (c-Si) structures to less than 2 $cm^2/V.sec$ in amorphous structures had been considered the main proof for this assumption.

However, in 1996, Hosono *et al*. changed this understanding by demonstrating high carrier mobility amorphous metal oxides (MO) composed of heavy metal cations [5, 6]. They later completed this study and demonstrated that these MOs, by taking advantage of the spherical shape of the s-orbitals in the conduction band, are insensitive to spatial directionality and exhibit large band-dispersion and overlaps even in amorphous structures. In turn, this large band dispersion results in high mobility in the amorphous structure of this material system [4]. This phenomenon is in contrast with the electronic structure of covalent semiconductors, whose valence band maximum (VBM) and conduction band minimum (CBM) are made up from the anti-bonding ($sp^3\sigma^*$) and bonding ($sp^3\sigma$) states of hybridized orbitals, respectively, and are highly sensitive to spatial directionality. Large spatial directionality results in the formation of the strained chemical bonds and large amount of traps and scattering centers in amorphous structures, and explains why much lower field-effect mobility is observed in conventional amorphous structures such as hydrogenated amorphous silicon (a-Si:H) than in crystalline ones [4].

The above unique electronic properties of metal oxides have attracted much interest in several transition metal oxides such as In_2O_3, ZnO, and SnO_2, all of which have large spherical shape s-orbitals in their conduction bands. These oxides in nature are polycrystalline and cannot be considered as an appropriate TFT channel layer material due to their poor electrical uniformity. However, taking advantage of different crystalline structures and different coordination numbers to the oxygen, each multi-component of the above mentioned oxides can result in the formation of amorphous structures with a large spherical shape s-orbital in their conduction band [2]. As an example, ZnO and In_2O_3, by having wurtzite and bixbyite structures, respectively, and demonstrating different coordination numbers to oxygen as ZnO_4 and InO_6, can result in the formation of a high field-effect mobility amorphous InZnO (IZO) structure. This structure can be considered as both transparent electrodes and semiconductor channel layers, depending on its chemical composition. The higher the In content, the higher the electrical conductivity. Although amorphous IZO shows high field-effect mobility (> 20 cm^2/V.sec) and superior uniformity in its electrical properties, the presence of high carrier concentration in this material system even at low In content results in a large off-current (I_{off}) and small $I_{on/off}$ ratio, which hinders its application as a TFT channel layer. This problem has been overcome by the incorporation of Ga into the IZO structure and results in the formation of an amorphous InGaZnO (IGZO) channel layer. Nomura *et al.* [7] showed that Ga ions tightly bind oxygen ions, thereby supressing the formation of oxygen deficiency, which are considered to be shallow donors in the IGZO channel layer material. IGZO TFTs have superior field-effect mobility and electrical stability than those of a-Si. The superior electrical stability is due to the presence of lower density of states in their sub-bandgap energy [4]. Amorphous metal oxides also have much better electrical uniformity than LTPS. As a consequence of these benefits, the semiconducting oxides have been suggested as one of the most promising

candidates for large-area electronics during the past few years. Metal oxides also demonstrate high optical transparency due to their large band-gap energy, which makes them one of the key components in the field of transparent electronics. Their amorphous structure is also better suited for large-area processes due to absence of the grain boundaries [4]. All of these unique advantages have resulted in such rapid development of IGZO TFT technology that almost eight years after Hosono *et al.* [7] introduced high-performance working-TFTs based on amorphous IGZO active layer in 2004, Sharp demonstrated the first IGZO TFT-based LCD display [8]. However, a large number of scientific reports have continued to be published since demonstration of the first LCD panels incorporating IGZO TFTs that continue to address remaining problematic areas. According to the Scopus database results, there was an upward (~27%) trend in the number of such publications from 2013 to 2014. Both the volume and the upward trend of these publications suggest that although many developments have occurred in the field of MO TFTs, some issues remain in developing a conventional and low-temperature process for fabrication of large-area flexible transparent electronics based on IGZO TFTs.

Reports have shown the out-diffusion of hydrogen (H) atoms from plasma-enhanced chemical vapor deposition (PECVD) dielectrics into adjacent IGZO channel layers during deposition [9, 10] results in the formation of shallow donors [11, 12] and a degradation of the TFT I-V characteristics. In addition, ion bombardment of the IGZO channel layer during the plasma-enhanced processing is found to result in the formation of shallow donors due to creation of oxygen deficiencies, which increases the channel conductivity in MO-TFTs and degradation of the TFT characteristics [12-15]. Thus, tuning the hydrogen and oxygen concentration of IGZO channel layers is one of the key points in developing high-performance IGZO TFTs. High-temperature deposition and high-temperature post-annealing have been identified as key solutions in adjusting the hydrogen [16]

and oxygen [17] concentration of IGZO channel layers. Lack of high-selectivity etchants between the transparent conductive oxides and semiconductors is another issue which hinders conventional wet-etch patterning of source/drain (s/d) electrodes. Table 1-1 exhibits the I-V characteristics of relatively high-temperature (≥ 250°C) processed IGZO TFTs fabricated on rigid substrates. As can be seen, there is a large variation in terms of field-effect mobility ($0.07 < \mu < 21.8$), threshold-voltage ($-9.5 < V_T < 11$), subthreshold-swing ($0.17 < S.S. < 7.37$), on-off ratios ($10^4 < I_{on/off} < 10^{10}$), and off-current ($10^{-9} < I_{off.} < 10^{-13}$), mainly arising from different deposition and annealing temperature, different annealing environments, different materials and device structures.

Table 1-1 Device characteristics of the previous works on IGZO TFTs.

Reference #:	**μ ($cm^2/V.sec$)**	**V_T (V)**	**S.S. (V/decade)**	**$I_{on/off}$ (A)**	**I_{off} (A)**
[18]	11.4-21.8	0.83-3.0	0.17	$\sim 10^7$	$\sim 10^{-11}$
[19]	2.4-4.21	2.9-5.8	0.4-1.51	$\sim 10^6$	$\sim 10^{-12}$
[20]	6.6	2.43-5.44	1.098-1.283	$\sim 10^7$	$\sim 10^{-13}$
[21]	7.2	-9.5	0.3	$\sim 10^7$	$\sim 10^{-13}$
[22]	0.072	28	1.4	$\sim 10^4$	$\sim 10^{-9}$
[23]	21.79	-0.15	0.26	$\sim 10^8$	$\sim 10^{-11}$
[24]	1.4-3.1	7-11	2.4-4.4	$\sim 10^5$	$\sim 10^{-9}$
[25]	0.18-9.36	2.22	0.21-7.37	$\sim 10^4$ to 10^{10}	$\sim 10^{-9}$ to 10^{-12}

Recently, a few research groups have reported the feasibility of fabricating high-performance *flexible* IGZO TFTs. Table 1-2 shows recent work on flexibles IGZO TFTs on different flexible substrates such as polymeric substrates, metal foils, and flexible glasses. It also compares these studies in terms of the conventional dielectric layers used, optical transparency, source/drain

patterning techniques, and their electrical stability, to the current manufacturing specifications of the display industry.

Table 1-2 Some of the processing steps and device characteristics of the previous works on flexible IGZO TFTs. (Y stands for Yes, N stands for No, and NA stands for Not Applicable).

	Reference #:											
	[26]	[27]	[28]	[29]	[30]	[31]	[32]	[33]	[34]	[35]	[36]	[37]
Using conventional PECVD dielectric materials?	Y	N	N	N	Y	N	N	N	N	N	Y	N
Low-temperature (≤220°C) process?	N	Y	Y	NA	N	Y	Y	Y	Y	NA	Y	Y
Transparent?	Y	N	N	N	N	N	N	N	N	N	N	N
Conventional wet/dry etching patterning?	N	N	N	NA	N	N	NA	N	N	N	N	N
Long-term bias instability measurements (Aging test)?	Y	N	N	N	N	N	Y	N	N	Y	N	Y
Long-term bias instability measurements (Recovery test)?	N	N	N	N	N	N	N	N	N	N	N	N

The results show that almost all these flexible TFTs suffer from the poor optical transparency and a lack of a direct wet/dry etching process for TFT manufacturing. In addition, it can be seen that only a few groups have used conventional PECVD nitride and oxide dielectric layers while almost all reports use high-melting point substrates and a high-temperature process in order to fabricated high-performance devices. There is also a lack of understanding with regards to the electrical stability of these devices where long-term aging and recovery tests would provide insight to the operational lifetimes for flexible MO-TFTs.

A closer look at the findings of these reports concludes that their fabrication processes involve three main approaches: (a) non-conventional dielectric materials and deposition techniques, (b) applying high-temperature processes that limit fabrication to high melting-point substrates such as metal foil, polyimide, and flexible glass substrates, and (c) the requirement for lift-off patterning or shadow-mask techniques to define device features.

Passivation materials such as $SiO_2/TiO_2/SiO_2$ and $HfO_2/TiO_2/HfO_2$ [29], TiO_2 [38], $MgO_{0.3}BST_{0.7}$ [39], and Y_2O_3 [7] typically require advanced deposition techniques such atomic layer deposition (ALD) [35] that are not compatible with the current large-area electronic process tools. Additionally, high-melting point substrates such as metal foil [40] and polyimide [19] are not transparent, preventing their application in the field of transparent electronics. Alternative flexible platforms such as thin-glass substrates [26] are highly brittle and are not appropriate solutions for large-area manufacturing due to potential low yield due to substrate fracture. Finally, the lack of a reliable high-selectivity etchant has also hindered the development of transparent electronics where many research groups are using either lift-off or shadow-mask methods, which are not favorable patterning techniques in industry. The opaque electrodes used in many studies are another bottleneck to developing transparent flexible electronics. Greater understanding of the electrical instability of the flexible TFTs is also needed.

Thus, it is clear that if large-area flexible transparent electronics based on IGZO TFT backplanes are to be developed, it will be critical to overcome the engineering and scientific challenges to enable low-temperature fabrication processes for high-performance flexible transparent IGZO TFTs that take advantage of the current device structure, processing equipment, and process flows that enable the current state-of-the-art large-area electronic systems.

1.2. Organization of dissertation

This Ph.D. dissertation studies the factors that affect transition-metal-oxide transistor performance, covering different aspects demonstrating the relationship between materials processing and characterization, device processing and characterization, to integrate these transparent metal-oxide devices onto flexible platforms. Finally, it describes a novel back-end encapsulation process for passivating the device and demonstrates its performance under mechanical bending. These factors,

which are explained below, culminate in the demonstration of optically transparent back-channel etched flexible IGZO TFTs using a conventional TFT process flow implemented at low-temperatures.

Chapter 2 briefly reviews the device physics of thin-film transistors, device operation, thin-film deposition, patterning techniques, and then introduces metal oxide (MO)-TFTs to provide the necessary background for the experimental work of the thesis. The beginning of Chapter 3 investigates the effects of different sputtering deposition parameters on the electrical properties of the metal-oxide channel layers followed by studies into the electrical dependence on the material properties, surface topography, and chemical composition of the metal oxide channel layer for ZnO and IGZO TFTs as a function of deposition temperature and annealing environments. The current-voltage (I-V) characteristics of the fabricated TFTs are correlated to the surface morphology, structural characteristics, and the chemical composition of the TFT channel layers. Chapter 4 considers the effect of the chemical composition of the plasma-enhanced chemical vapor deposition (PECVD) and thermally grown gate dielectrics on the surface roughness and chemical composition of the channel layer and their effect on TFT performance. In the end, a low-temperature ($\leq$ 150°C) process is developed to fabricate high-performance opaque IGZO TFTs using conventional PECVD gate dielectrics. In Chapter 5, optically transparent high-performance IGZO TFTs are fabricated using IGZO contacts and a lift-off patterning technique. Applying sputtered IGZO as the source/drain electrodes gives the opportunity to deposit channel layers and contact electrodes using the same sputtering target in IGZO TFT fabrication, which results in a simplified fabrication process and with higher-quality electrical contacts between the semiconductor and source/drain electrodes. The conductivity of IGZO thin-films is tuned by controlling the sputtering power, pressure, and temperature during the film deposition.

Transmission line measurement (TLM) is also used to determine the contact resistance of the IGZO electrodes. In order to better understand the electrical instability of the fabricated TFTs, dc gate-bias stress measurements and pulsed-gate recovery tests are also carried out. Chapter 6 demonstrates the feasibility of fabricating optically transparent flexible IGZO TFTs using a wet-etch patterning technique. Contact resistance is again studied using the TLM method. In addition, the electrical instability of the fabricated TFTs is investigated using dc gate-bias stress and pulsed-gate recovery measurements. Furthermore, the effect of mechanical bending on the TFT I-V characteristics is measured under uniaxial tensile and compressive strain applied along the channel length of the devices (parallel to I_D) by bending the samples in concave and convex sample holders at room temperature. In Chapter 7, a simple, low-temperature, and relatively low-cost approach is demonstrated to passivate back-channel etched transparent IGZO TFTs. Finally, Chapter 8 summarizes the contribution of this Ph.D. thesis to the field of flexible transparent electronics and points out suggestions for future work.

Chapter 2

2. Background Review

2.1. Brief Background on Thin-Film Transistors

Typical thin-film transistors (TFTs) are composed of a gate, gate dielectric, active layer, back channel passivation and source/drain (s/d) electrodes. Figure 2-1 shows a schematic of a TFT device. In a n-type (p-type) TFTs when an appropriate positive (negative) gate voltage (V_G) applies, the conductivity of channel layers increases. (Note: in this dissertation, all fabricated TFTs are based on an n-channel device.)

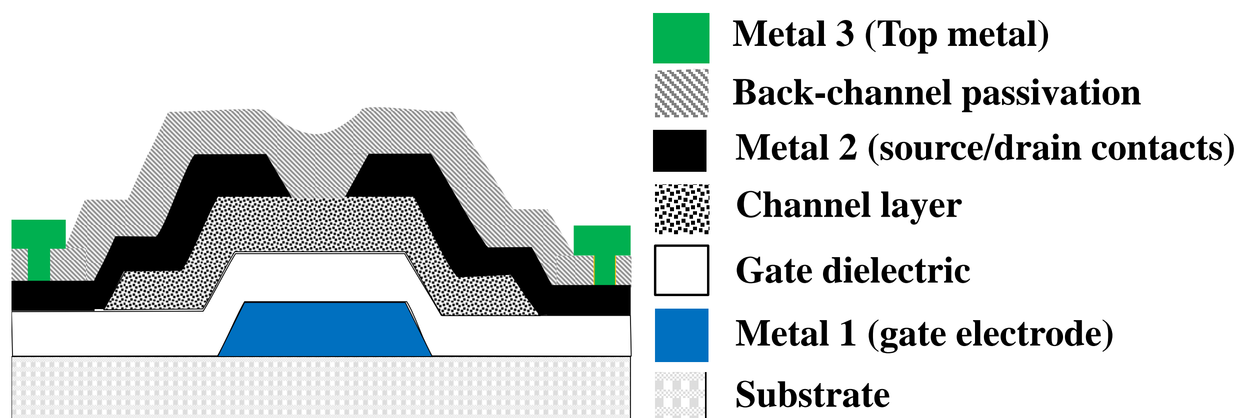

Figure 2-1 Typical thin-film transistor (TFT) structure.

In an n-type TFT, applying a negative V_G leads to the formation of an electric field, which in turn, results in the formation of a depletion region in the channel layer. In this case, the semiconductor layer acts like a high resistance (insulating) material where current flow between the source and drain contacts reduced to very low values (ideally, $I_D < 10^{-12}$ A) and the transistor is considered to be Off.

In contrast, when a positive potential is applied to the gate electrode in an n-channel TFT, an accumulation of electrons occurs in the channel layer within 5 to 15 nm of the gate dielectric, and the conductivity of channel layer increases in this region. In this case, when the applied V_G is greater than the threshold voltage (V_T) (the minimum potential required to turn the device strongly ON), electrons can flow from the grounded source to the biased drain [41].

Band diagrams of a TFT in accumulation mode under various gate bias conditions can be seen in Figure 2-2. When no gate voltage is applied (ideal condition) the band diagram is assumed to be flat, Figure 2-2 (a). Applying a negative gate bias results in the formation of a depletion region (depleted of mobile charge) in TFT channel layer. Depletion of mobile charge gives rises to the creation of a positive charge region which results in a positive (upward) bending of the valence and conduction bands, as it can be seen in Figure 2-2 (b). In contrast, a positive gate bias attracts (accumulates) electrons to the gate dielectric/channel layer interface. As it is illustrated in Figure 2-2 (c), the negative charges which are created in channel layer leads to a negative (downward) bending of the valence and conduction band. Based on the type of the gate bias (positive or negative), TFTs can be classified into two categories: a) enhancement mode, and b) depletion mode devices. In enhancement mode devices, a positive gate voltage is needed to accumulate the channel layer and turn the device on. In contrast, for the depletion mode, a negative gate voltage is needed to turn on the device [41].

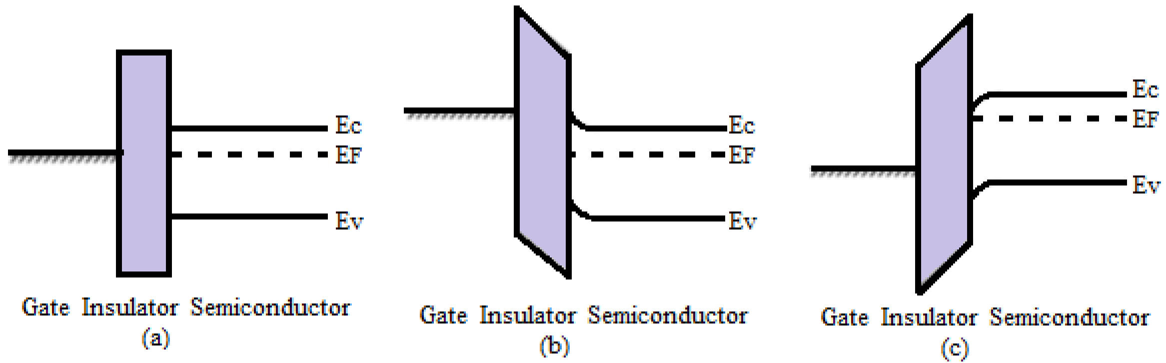

Figure 2-2 Band diagrams of an n-type accumulation mode TFT under various gate bias conditions; a) No gate bias, b) Negative gate bias c) Positive gate bias.

Both drain voltage (V_D) and gate voltage (V_G) can be controlled independently. When the V_G is held constant and the V_D is swept, the output characteristics of the device are generated. By sweeping the V_G, with V_D constant, the generation of the transfer I-V characteristics may be obtained, as is shown in Figure 2-3(a,b). The ratio of the maximum drain current (sometimes referred to as the on-current (I_{on})) divided by the minimum drain current (leakage current or I_{off}) is commonly referred to the $I_{on/off}$ ratio. The majority of the high-performance MO-TFTs introduced in the previous chapter (Chapter 1) usually demonstrate $I_{on/off}$ ratio $>10^5$. Subthreshold Swing (S.S.) is another parameter which determines the electrical performance of TFTs. S.S. can be calculated by inverting the maximum slope of the transfer characteristics, and it shows the V_G required to induce a decade increase in the I_D. Small values of S.S. result in higher speeds and lower power consumption in the fabricated device. Since both interface and bulk traps degrade S.S. in MO TFTs, optimizing the fabrication process flow plays a dominant role in developing high-speed and low-power consumption MO-TFT switches for large-area electronics, especially portable devices. According to the finding of this Ph.D. study and the findings of the other research groups, it seems that the majority of MO-TFTs demonstrate S.S. in the range of ~0.2 and ~4 V/decade, depending

on the fabrication process flow, deposition and annealing temperature, annealing environment, and the applied materials.

When $V_D < V_G$-V_T, TFT works in linear mode and when $V_D > V_G$-V_T device works in the saturation mode [41]. The linear and saturation mobility of TFTs can be determined using the gradual-channel approximation (Eq. 2.1 and 2.2):

$$I_D = \frac{W}{L}\mu C[(V_G - V_T)V_D - \frac{V_D{}^2}{2}] \qquad \text{Linear } (V_G\text{-}V_T) > V_D \qquad (2.1)$$

$$I_D = \frac{W}{L}\mu C[\frac{(V_G - V_T)^2}{2}] \qquad \text{Saturation } (V_G\text{-}V_T) < V_D \qquad (2.2)$$

where μ is the field-effect mobility, C is the specific capacitance of the gate dielectric, (W/L) is the channel width to length aspect ratio of the device, V_T is the threshold voltage, V_G is the gate voltage, and V_D is the drain to source voltage.

At a low V_D, the squared term in equation (2.1) is insignificant and the device behaves like a variable resistor with the I_D proportional to the V_D. As V_D increases, electrons in the region surrounding the drain are depleted; creating a pinch-off point and the I_D will be constant for increasing V_D. The device is operating in saturation when V_G-$V_T < V_D$. In saturation mode, the device functions as a constant current source where the drive current is dependent on the gate voltage. V_T can be determined using different methods such as linear extrapolation of the I_D-V_G plot in linear mode, as illustrated in Figure 2-3 (b), or of the $I_D^{1/2}$-V_G plot in saturation mode [41].

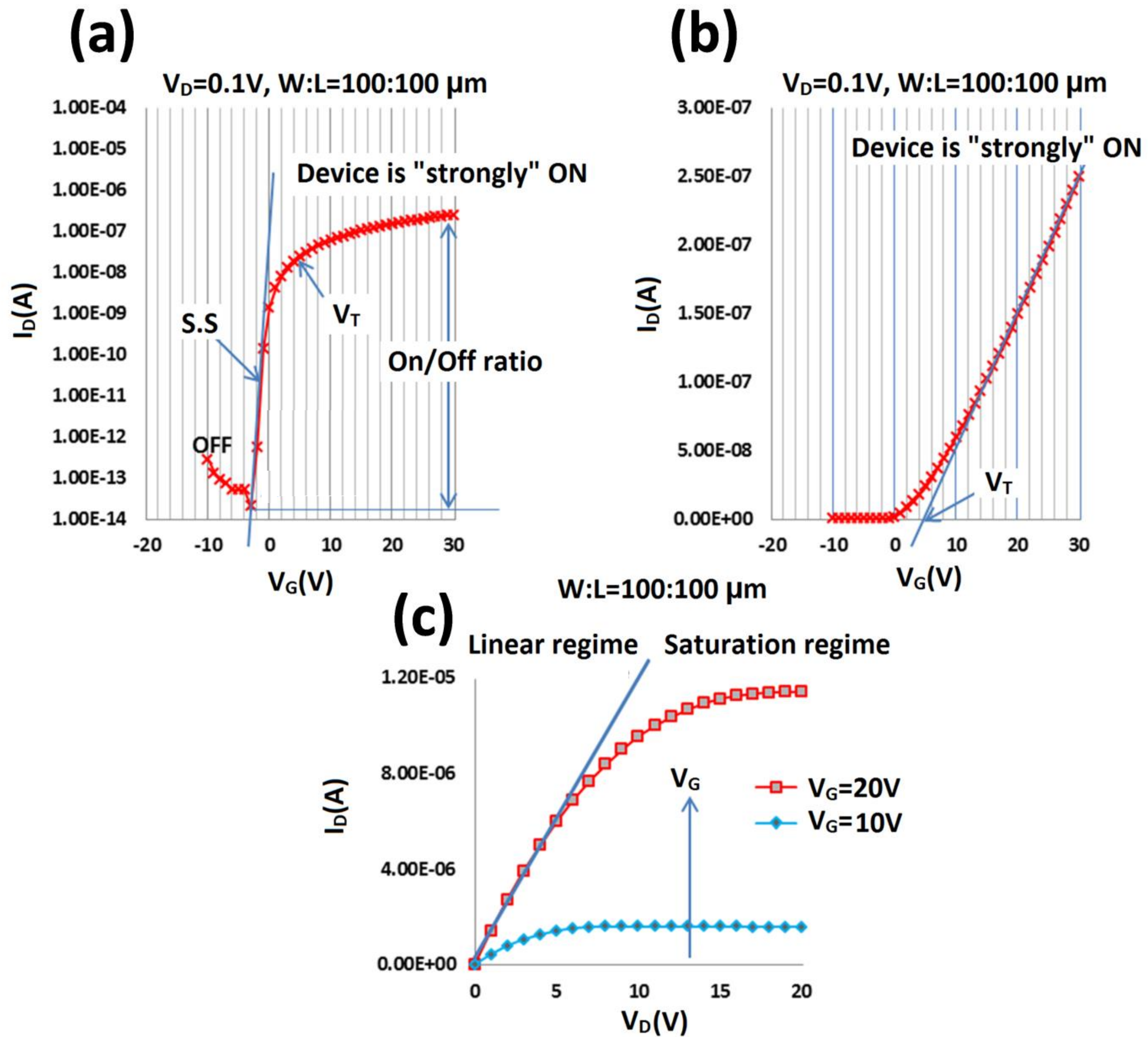

Figure 2-3 Transfer characteristics of IGZO TFTs in in the (a) log and (b) linear scales. (c) output characteristics, W/L=100/100 µm.

2.2. Thin-film deposition and patterning techniques

In order to fabricate thin-film transistors (TFTs), several thin-film layers need to be deposited and patterned back to back. In this section, the main thin-film deposition methods and thin-film patterning techniques, which are used in this Ph.D. research, are briefly introduced.

2.2.1. Sputtering

All the semiconductors and transparent conducting oxides studied in this Ph.D. research are deposited using sputtering and a general overview of this deposition technique is given in this sub-section. A simple structure for a sputtering system consists of a simple Direct Current (DC) diode. In this structure, the material source (sputtering target) is placed on the negative electrode, while the substrate is placed on the positive electrode. The anode is usually grounded, and the cathode is placed within the vacuum chamber. The chamber is backfilled with an inert gas and a DC field between the anode and cathode is applied. Due to the applied electric field, electrons and ionized gas species are attracted toward the positive (substrate) and negative (sputtering target) electrodes, respectively. Positively charged ions strike the target material on the cathode electrode that results in the emission of secondary electrons from the target surface, which sustains the glow discharge. Due to the much smaller mass of the electrons than that of the ions, the secondary electrons are quickly accelerated away from the target surface, resulting in the formation of a high-field region, which is called the Crooke's dark space, in front of the target material [42]. In this dark region, which accounts for most of the voltage drop between the substrate and target material, positively charged ions accelerate toward the target material (cathode electrode) and result in the ejection of atoms from the target and deposition on the substrate. It should be mentioned that DC configurations are only applicable when the target materials are conductive and the secondary electrons have a chance to continuously sustain the glow discharge. In the case of non-conductive materials, the presence of an alternating current (AC) field is necessary. The applied AC field, by formation of a self-biased voltage located in front of the target material, results in a deposition mechanisms similar to the DC configuration. The short positive portion of the excitation, by attracting the electrons towards the target, can replenish the lost secondary electrons and results in

sustaining the glow discharge when an insulating target materials are used. It is worth noting that in practical applications, in order to increase the chance of ionization, strong magnets usually are put behind the sputtering target (cathode) to gyrate electrons in loops parallel to and confined near the target material.

In some cases such as oxide deposition, reactive sputtering can be used in order to adjust the material and electrical properties of the sputtered films. In reactive sputtering, in addition to an inert gas, a reactive gas such as oxygen can also be employed. Figure 2-4 shows the AJA sputtering system used in this research to deposit channel layers and contact electrodes.

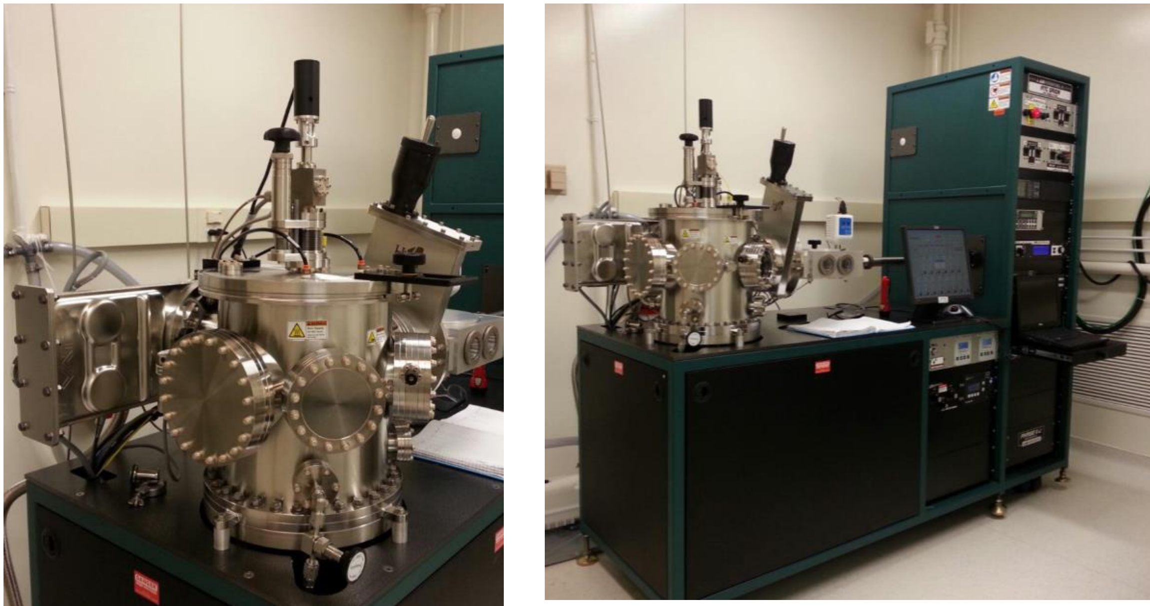

Figure 2-4 The AJA sputtering system used in this research to deposit MO-thin-films.

2.2.2. Plasma-enhanced chemical vapor deposition (PECVD)

Dielectric materials are one of the key elements of TFT structures, and they are usually used as gate dielectrics and passivation layers in TFT fabrication processes. Since the ultimate goal of this Ph.D. study is integration of our fabricated TFTs on a flexible platform, finding a low-temperature deposition technique was one of the first steps in our device fabrication process. PECVD is one

the sub-branches of the chemical vapor deposition (CVD) process, in which purely thermal energy is employed to generate the reactive species. However, in the PECVD process, high-quality films can be deposited at much lower substrate temperatures than those of the conventional CVD process, by using glow discharge during the deposition process. In addition, PECVD technique is currently being used in the a-Si and LTPS TFT industries, which makes this deposition technique one of the most favorable compared to other unit-process techniques such as ALD. Due to the above advantages, PECVD was chosen for deposition of the gate dielectric in this research. However, current display industries usually use a relatively high-temperature (~300°C) process for deposition of high quality PECVD SiN_x or SiO_x dielectrics. However, this approach is not compatible with the low-melting point conventional polymeric substrates. Hence, understanding the problems involved in fabrication of TFTs using low-temperature conventional PECVD nitride and oxide dielectrics and proposing a solution will be very helpful in developing the next generation of large-area flexible electronics. Figure 2-5 exhibits the PECVD system used in this research to deposit insulator materials.

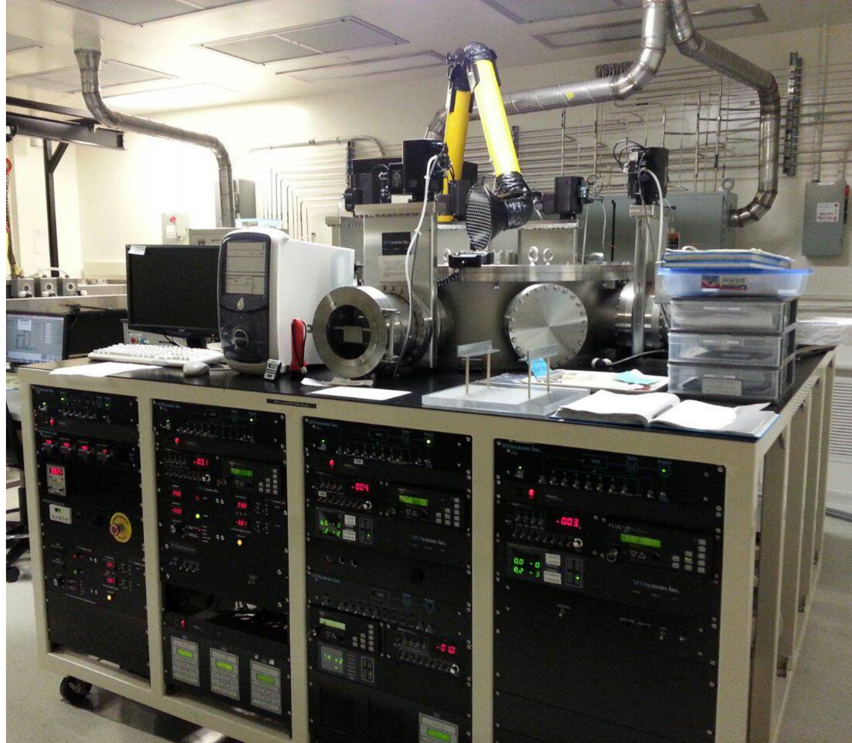
Figure 2-5 PECVD system used in this research to deposit insulator materials.

2.2.3. Electron beam evaporation (EBE)

It is reported that hydrogen (H) and oxygen deficiencies are two of the main sources of the unintentional doping of metal oxide channel layers, which could result in a highly conductive channel layer and degradation of TFT performance. Plasma damage has been found to be one of the main origins of oxygen deficiency formation. On the other hand, H-based gases such as SiH_4, and NH_3 are recognized as among the main causes for the unintentional doping of H during fabrication. Both are considered big issues for the PECVD deposition technique, which takes advantage of both glow discharge and H-rich gases for deposition of conventional nitride and oxide materials. Hence, in this study, in order to prevent unintentional doping of the IGZO channel layer, and to get away from plasma damage and hydrogen contamination during the deposition, electron beam evaporation (EBE) technique was selected. In this method the deposition of thin-films involves the evaporation of materials from a solid into a vapor that condenses back to the solid

state to form a thin-film on a separate substrate. There is no need to use glow discharge and H-based gasses. It is worth noting that in EBE deposition technique a high energy electron beam is used to heat the source material. Figure 2-6 shows the EBE system used in this Ph.D. study to deposit the oxide dielectric layer.

Figure 2-6 EBE system used in this research.

2.2.4. Thin-film patterning

Fabricating semiconductor devices requires that deposited thin-films be patterned. Common thin-film patterning techniques include (1) photolithography, (2) lift-off processes, and (3) shadow mask patterning. When an appropriate etching-process is available, having etch-selectivity between different layers, photolithographically patterned etch masks provide a direct approach to pattern different layers in a device structure. However, when a suitable etch-process is not available and the etch-selectivity between the device layers is poor, a lift-off patterning technique needs to be employed. As an example, MO-TFT device fabrication process typically do not have high etch

selectivity between the oxide semiconductor and the gate dielectric for TFT fabrication. This property of the two layers prevents the use of conventional photolithographic patterning and etching to define different layers in the device structure. This problem is magnified when the layers used for electrical contact to the semiconductor are the same such as the use of semiconducting IGZO channel layer and conducting IGZO transparent contacts that will be described in later chapters. In order to fabricate optically transparent IGZO TFTs using IGZO transparent contacts, a lift-off process for the source and drain patterning is typically required. Alternatively, shadow mask patterning, which is not the focus of this research, may be used to define the patterns in which a physical mask is used to block the path of incoming atoms during the deposition process and to define the patterns. However, the resolution of this technique is not as good as photo lithographically defined etch masks.

2.3. Flexible Electronics

Flexible electronics is an emerging technology consisting of robust, light weight, conformal, bendable, and low-cost electronic systems. Due to these unique properties, flexible electronics enables applications in advanced large-area electronics for displays, sensors, medical devices, solar cells, and smart electronic textiles that can bend and fold [43, 44]. The first step in the fabrication of flexible transparent electronic devices is choosing an appropriate flexible substrate. The ideal flexible substrate needs to be rollable, low cost and transparent. In addition, it needs to be resistant against chemical attack, have low permeability to water and oxygen, and to be dimensionally stable under thermal processing steps.

Flexible substrates can be divided into three main categories: (1) metal foils [40], (2) flexible glasses [26], (3) and polymeric substrates [19]. Metal foils can tolerate much higher processing temperature and much higher dimensional stability than polymeric substrates [45]. They have

strong resistance to water vapor and oxygen diffusion. In addition, metal foils have a low coefficient of thermal expansion (CTE). All these advantages make this category of flexible substrates one of the most promising candidates in the field of flexible electronics where optical transparency is not required. However, due to the relatively rough surface of metal foils (originated from rolling mill marks) and their high conductivity, they need to be coated by an insulating spin-on-glass (SOG) planarization layer before being applied as flexible substrates in device fabrication processes. Another category of flexible substrate is thin glass sheets (thickness < 100 μm). Flexible glass substrates offer superior optical transparency and perfect barrier layer properties against water vapor and oxygen atoms [45]. They have a low CTE and demonstrate ultra-smooth surface topography. However, this class of flexible substrates is highly sensitive to breaking and cracking, preventing their application in mass-production of large-area flexible electronics. The third category of flexible substrates is the polymeric substrates, among which polyethylene terephthalate (PET), polycarbonate (PC), polyethylene napthalate (PEN), and polyethersulfone (PES) have been extensively studied as flexible substrates for the development of flexible devices. Of the above-mentioned candidates, PEN substrates are favored due to its high Young's module, high transparency, compatibility with microfabrication processes, and low cost. In addition, its thermal and dimensional properties are better than those of PET substrates. However, due to the low thermal resistance and high thermal expansion of polymeric substrates, the maximum process temperature needs to be lower than 150°C if it is to be used for low-cost transparent organic substrates.

Having a low-temperature processed high-performance TFT is one of the most challenging areas in developing large-area flexible electronics. Several reports have demonstrated fabrication of TFTs on flexible substrates based on different channel layer materials such as amorphous silicon

(a-Si), organic semiconductors, low-temperature polycrystalline silicon (LTPS) and metal semiconducting oxides. However, many of these materials do not possess all the ideal requirements for high-performance large-area advanced devices [2, 46-48]. Organic and a-Si based TFTs are not acceptable due to their low field-effect mobility. On the other hand, although LTPS demonstrates high mobility, its processing complexity and cost along with its nonuniform grain size over large areas make LTPS a less than optimal choice for low-cost high-performance flexible electronics. On the other hand, MO TFTs have demonstrated acceptable electrical characteristics with high field-effect mobility, low threshold voltages and excellent uniformity even when deposited at relatively low temperatures. Recently, a few research groups have reported the feasibility of fabricating *flexible* metal-oxide based TFTs. Table 2-1 compares these studies in terms of the type of flexible substrate, dielectric material used, gate dielectric deposition technique, optical transparency, maximum process temperature, and source/drain patterning techniques. Taking advantages of both the function of transparency and the superior electrical properties of MO TFTs at low temperature, MO TFTs are one of the most promising candidates for the development of large-area transparent flexible electronics.

Table 2-1 Materials, deposition and patterning techniques, maximum process temperature and optical transparency of the previous works on flexible IGZO TFTs.

Type of substrates?	Polymeric substrates	Metal foils [40]	Flexible glasses [26]	Glossy paper [49]
Type of gate dielectrics?	Al_2O_3: [28, 35, 50], SiN_x:[19], SiO_x:[51], $HfO_2/TiO_2/HfO_2$: [29]	SiO_x	SiN_x	Methyl-siloxane based dielectric
Deposition technique?	ALD: [28, 35, 50], PECVD: [19], e-beam evaporation: [29]	PECVD	PECVD	Spin coating
Optically transparent?	No	No	Yes	No
Maximum process temperature?	150°C: [28, 35, 50], 200°C: [51], 350°C: [19]	300°C	300°C	150°C
Patterning approach?	**Wet or dry etching:** No[28, 35, 50, 51], **Wet or dry etching:** Yes [19]	Not applicable	No	Not applicable

2.4. Metal oxide-based TFTs

Transparent electronics may be discussed in two main categories: one is based on transparent electrodes and the other on transparent thin-film transistors (TFTs). The first group is a mature technology that has utilization in transparent electrodes such as indium tin oxide (ITO) that enables the fabrication of liquid-crystal displays (LCDs), organic light-emitting diodes (OLEDs), solar cells, and touch panels. Likewise, development of transparent TFTs has opened a new window to the second class of transparent electronic devices. In this category, MO-TFTs, having a large band-gap in the channel layer and electrodes, enables applications in transparent electronic systems such as optically transparent displays, heads-up displays, flexible transparent active-matrix organic light-emitting diodes (AMOLEDs), and potentially transparent windows with integrated high-definition displays [1, 2].

2.4.1. Channel Layer Materials

High-mobility transparent materials which can be deposited at a relatively low-temperature (≤150°C) are promising candidates for developing the next generation of high-performance large-area transparent flexible electronics. Among the different types of materials, transition metal oxides, by satisfying the above requirements, have attracted lots of interest during the past few years. This subsection briefly introduces some of the material properties of two of the most favorable: crystalline (ZnO) and amorphous (InGaZnO (IGZO)) transition metal oxides.

2.4.1.1. ZnO

Zinc oxide (ZnO) is a direct bandgap semiconductor with a bandgap of 3.44 eV, which makes it transparent in the visible range of the electromagnetic spectrum [52]. Some of the basic properties of zinc oxide are shown in Table 2-2 [53]. As can be seen, ZnO has a melting point of 2240 °C, density of 5.67 g.cm^{-3}, and optical transparency of >80%.

Table 2-2 Some of the basic properties of zinc oxide material.

Material	Melting point (°C)	Density (gcm^{-3})	Optical transparency (%)	Crystal structure	Band-gap (eV)
ZnO	2240	5.67	>80	Wurtzite	3.44

Among different possible crystal phases of the ZnO, the wurtzite (hexagonal) structure is thermodynamically favored at room temperature. Regardless of the deposition methods, ZnO is almost always polycrystalline. In the hexagonal wurtzite structure, each Zn cation is surrounded by four oxygen anions at the corners of a tetrahedron, and vice versa. The ZnO crystal structure is composed of alternating planes of Zn^{2+} and O^{2-} ions stacking along the c-axis. Figure 2-7 illustrates the schematic diagram of ZnO crystal structure. It is worth noting that ZnO shows a highly ionic characteristic due to the large difference in electronegativity of the Zn and O atoms.

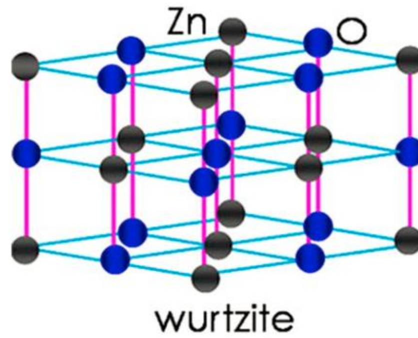

Figure 2-7 A schematic illustration of ZnO crystal structure (wurtzite). The Zn and O atoms are marked as well in the schematic with ash and blue circles, respectively [45].

The calculated formation enthalpy of the intrinsic defects, such as oxygen vacancy (V_o), zinc interstitial (Zn_i), zinc antisites (Zn_o), zinc vacancies (V_{Zn}) and oxygen interstitial (O_i), showed that the formation enthalpy of Zn_i and V_o is lower compared to other defects. [54]. Doping in ZnO thin-films traditionally was attributed to native point defects such as V_o and Zn_i. However, recent studies have shown that native defects, alone, cannot explain n-type doping of ZnO materials [55]. Formation of strong bonds between the oxygen and hydrogen atoms and incorporation of hydrogen

impurity atoms into ZnO is suggested to be another possibility for n-type conductivity of intrinsic ZnO [56]. But, hydrogen is highly mobile and is unstable at temperatures where n-type conductivity is known to persist (>500°C) [57]. In addition, H impurity *alone* cannot explain the dependence of conductivity on the oxygen partial pressure [58, 59]. Recently, it is reported that substitutional hydrogen on V_o sites and formation of V_o-H complex (H induce V_o) may be the main origin of n-type conductivity in ZnO thin-films [58]. Very recent studies have further confirmed the role of V_o in n-type conductivity of ZnO thin-films by correlating the n-type conductivity of this material system to the formation of complexes of V_o-Zn_i [60, 61].

The findings of other groups have shown that when the electron density in ZnO film is low, electron transport is characterized by grain boundary scattering mechanisms. On the other hand, when the electron density in the ZnO film is high, ionized impurity scattering, which is a columbic interaction between conduction electrons and positively charged donors, is the dominant mechanism. In this case, the potential barrier at the grain boundary is narrow enough for electrons to quantum mechanically tunnel.

2.4.1.2. InGaZnO (IGZO)

It was once believed that the compound semiconductors (because of their strong ionic bonds) would not have suitable long-term stability and carrier doping properties due to the easy formation of defects. These problems, consisting of poor stability and difficulty in making p-type ZnO, were observed for ZnO, but recent studies have shown that the poor electrical stability of ZnO originates from grain boundary effects [62, 63]. In contrast, amorphous metal oxides (MO) owing to their amorphous structures do not show any grain boundary effects and present superior uniformity and electrical stability compared to crystalline structures. Amorphous hydrogenated silicon (a-Si:H) compared to that of crystalline silicon (c-Si) have poorer transport properties because of its

disordered structure and large number of scattering. This drawback of amorphous materials restricted their use in advanced high-performance electronics, which typically require high carrier mobility as well as suitable electrical uniformity and stability.

The finding of high carrier mobility in highly-doped amorphous metal oxides (MO) in 1996 opened a new window to advanced electronics and corrected the previous misunderstanding [5, 6]. Interestingly, high mobility of this category of materials is correlated to the strong ionicity of the metal oxides, which was believed to be the drawback of conventional oxides. Based on the Madulang potential, when a metal atom and an oxygen atom are apart in vacuum, as in Figure 2-8 (b), the highest occupied atomic orbital (HOAO) energy of the oxygen atoms and metal atoms are almost the same, and they demonstrate neutral atom states that are stable. When metal and oxygen atoms get closer to each other, due to the difference in electron affinities, charge transfer occurs, which results in the formation of ionized atoms. The ionized atoms form a positive electrostatic potential at the anion sites and negative electrostatic potential at the cation site, thereby stabilizing the ionized states in ionic materials, Figure 2-8(c). The Madelung potential raises and lowers the energy levels of metal cations and oxygen ions, which results in the formation of fully-occupied O 2p orbitals in valence band maxima (VBM) and formation of empty orbitals of the metal cation in the conduction band minimum (CBM) [4]. The spherical shape and large spatial size of the s-orbitals of the heavy metal cations in the conduction band gives rise to large band dispersion and overlaps which, in turn, leads to small electron effective mass and higher electron mobility. It is worth noting that the large overlaps of the s-orbitals in the conduction band do not change if the structure is amorphous, Figure 2-9(c,d). Therefore, this unique structure of amorphous metal oxides gives rise to a high mobility, excellent electrical stability, and large band-gap. In contrast, the VBM and CBM of the covalent semiconductors are made up from the anti-

bonding ($sp^3\sigma^*$) and bonding ($sp^3\sigma$) states of hybridized orbitals, respectively (Figure 2-8(a)), and have large spatial directionality (Figure 2-9(a,b)) that affect the electronic transport properties.

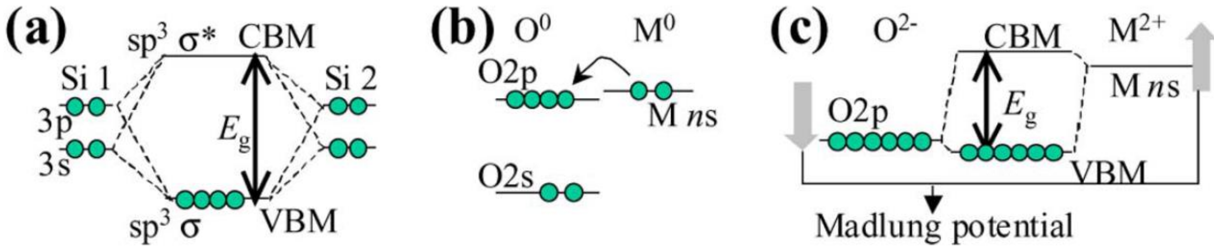

Figure 2-8 Different formation mechanisms of bandgaps in covalent (a) and ionic (b,c) semiconductors [4].

Due to the large spatial directionality of chemical bonds in covalent semiconductors, strained chemical bonds in amorphous semiconductors such as a-Si:H demonstrate much lower mobility compared to the crystalline ones because of the formation of traps states and scattering centers [4]. Therefore, the difference between the electrical properties of oxide semiconductors and silicon originates from the different electronic structures of these two categories of materials.

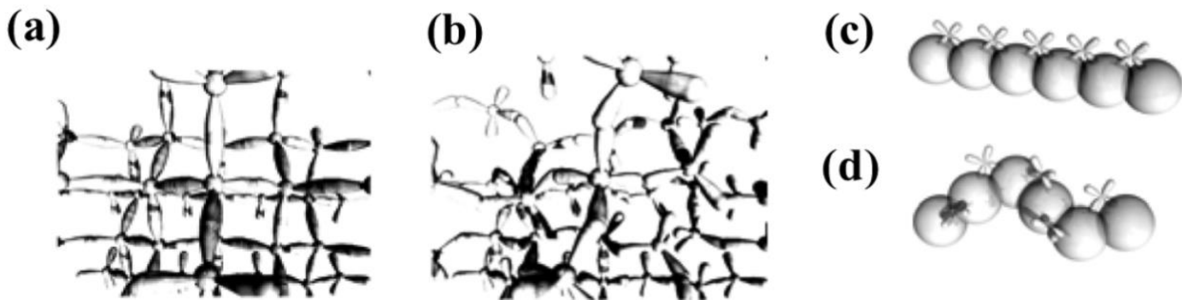

Figure 2-9 Illustrative images of carrier conduction paths in (a) c-Si, (b) a-Si, (c) crystalline oxide, and (d) amorphous oxide.

Interestingly, AMOs show thermally-activated behaviors in the degenerate state. This unique electrical property occurs due to the percolation mechanisms in AMO semiconductors [64]. Based

on this model, because of long average-distance between the monoenergetic states, quantum mechanical hopping is not the dominant conduction mechanism in this material.

When the Fermi energy level is lower than the highest energy barriers, electron conduction is dominated by percolation mechanisms and electrons trickle between the potential energy barrier valleys, as is depicted in Figure 2-10. In contrast, when the Fermi level goes above the mentioned conduction band potential energy barriers, the concentration of the free carriers is enough to completely fill the valleys in the tail states, giving rise to the temperature-independent carrier transport [64].

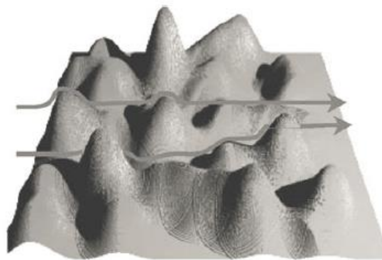

Figure 2-10 Percolation mechanisms in IGZO.

Oxygen deficiency and unintentionally incorporated hydrogen (H) atoms are the two major hypotheses used to explain the origin of free electrons [54, 56]. Due to the difficulty in removing the hydrogen atoms from vacuum system, unintentional incorporation of hydrogen atoms occurs during the deposition of metal oxides, resulting in the creation of free electrons in intrinsic metal oxide during oxide deposition.

The structures of amorphous indium gallium zinc oxide (IGZO), including crystalline In_2O_3 and crystalline $InGaZnO_4$ (c-IGZO), are illustrated in Figure 2-11. As seen in Figure 2-11(d), the CBM of IGZO is mostly made of indium (In) ions, which are responsible for the high mobility [65]. The neighboring In ions are connected by an edge-sharing network of (InO_6) octahedral (drawn as red

polyhedra). The structure of IGZO demonstrates that the edge-sharing networks of (InO_n) polyhedra are preserved even in an amorphous structure.

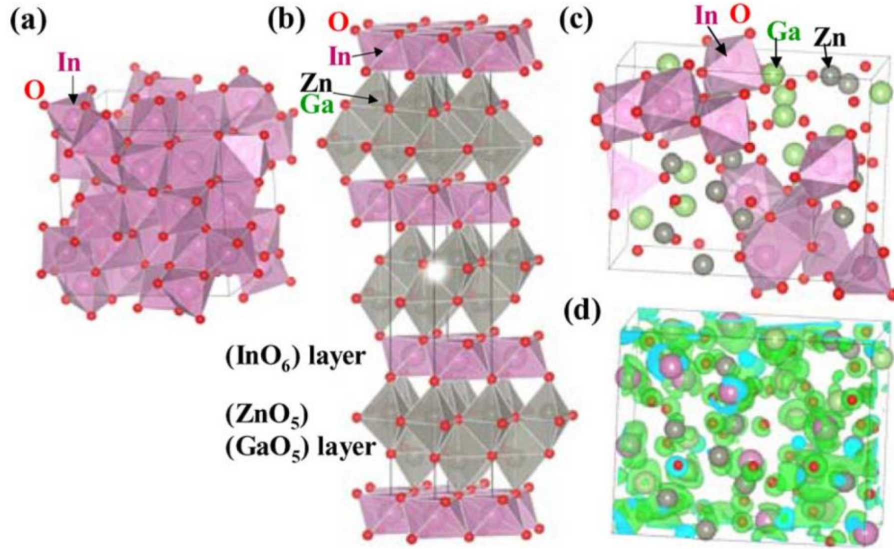

Figure 2-11 Polyhedral views of crystal structures of (a) In2O3, (b) InGaZnO4, (c) amorphous IGZO. [Red and gray polyhedra show (InOn) and (Zn/GaOn) polyhedra. In2O3 and c-IGZO are made of the edge-sharing network of (InO6) octahedra and the corner-sharing sharing network between (InO_6) and (Zn/GaO_5) polyhedra. In amorphous IGZO, the edge-sharing network structures are preserved.], (d) CBM wave function in amorphous IGZO is drawn superimposed on (c) by green surfaces [4]

Higher In content in IGZO films gives rise to a larger mobility, which is directly related to the IGZO structure. In contrast, gallium (Ga) incorporation results in a lower free carrier concentration and mobility. Furthermore, it has been found that controlling free-carrier concentrations in Ga-free films is too difficult. These results have been explained as due to the difference in the formation energy of oxygen deficiency [66]. Ga-Ga bonds in IGZO structure are much stronger than Ga-M, and M-M bonds around the V_o defects, where M=In and Zn. So, oxygen deficiency will be generated more easily at the oxygen site surrounded by In atoms. In contrast, formation of V_o around Ga atoms needs much higher energy [66]. Although Ga incorporation leads to a lower mobility, due to the difficulty in controlling the free carrier concentrations in Ga-free films, this

incorporation is necessary in fabricating high-performance MO-TFTs with small leakage current [4, 65].

It is worth noting that if the previously introduced polycrystalline (ZnO) and amorphous (IGZO) transition metal oxides are to be used in the next generation of flexible electronic applications, in addition to having proper electrical properties, they need to satisfy the requirements of flexible electronics in terms of mechanical properties. Recently, the mechanical properties of ZnO, IGZO, and a-Si-TFTs with similar structural components were compared using COMSOL numerical modeling [67]. The findings of this research study demonstrated the formation of lower levels of stress and strain in transition metal oxide layers (ZnO and IGZO) compared to the a-Si, the material most favoured in the current flexible electronics industry. This superior mechanical properties of the metal oxides over a-Si have been correlated to the slightly lower Young's modulus of ZnO (E=137 GPa) and IGZO (E=137 GPa) compared to a-Si (E=150 GPa), respectively. The results for mechanical properties further confirm that transition metal oxides are one the best candidates in the field of flexible transparent electronics.

2.4.2. Electrical dependence on the chemical composition of the ZnO-based channel layer in MO-TFTs

This section briefly discusses how oxygen deficiencies and hydrogen (H) incorporation change the electrical properties of ZnO-based channel layers.

2.4.2.1. Oxygen deficiency

The effect of oxygen partial pressure during sputtering was investigated by Yabuta *et al.* [68]. They showed that the conductivity of the IGZO films decreased logarithmically when oxygen pressure increased. Noh *et al.* showed that the formation energy of V_o is strongly related to

neighboring atoms [69], and that Ga and In atoms increase and decrease the formation energy of V_o, respectively. They demonstrated that V_o can act both as a deep and a shallow donor in IGZO material. These findings indicate that both deep and shallow V_o defects are partly responsible for the positive V_T shift under positive dc gate-bias stress. The authors also showed that although some defects can be recovered at room temperature, high annealing temperature, up to 400°C, was sometimes required. Kang *et al.* demonstrated that IGZO TFTs are very sensitive to surface adsorption and can be used as oxygen or pressure sensors [70].

Kwon *et al.*, while studying the effect of oxygen flow rate on the conductivity of IGZO films [71], found that when no oxygen is supplied (0 sccm), the IGZO film is highly conductive and the conductivity of the channel layer cannot be tuned by the gate bias; TFTs always show ON-state behavior. On the other hand, IGZO thin-films demonstrated insulating properties at a high oxygen flow rate (10 sccm). These results were correlated to the lower concentration of V_o in the film deposited at higher oxygen flow (10 sccm).

Other research groups studied the effect of oxygen partial pressure on the conductivity of IGZO thin-films and found that the resistivity can be systematically varied by almost orders of magnitude by varying the oxygen partial pressure during sputtering [72]. At high oxygen partial pressure, chemical composition of IGZO channel layer became close to the stoichiometry and the IGZO TFTs showed no switching properties. These results were correlated to the formation of low V_o concentration and a negligible carrier concentration in the IGZO channel layer. Barquinha *et al.* showed that in order to obtain high-performance as-deposited IGZO TFTs, only a little or no oxygen in the sputtering chamber is crucial to quality of channel layer [17]. In addition, they reported that regardless of the oxygen content in the sputtering chamber, a high temperature thermal anneal, in which the oxygen content is adjusted to an equilibrium point in IGZO thin-

films, results in almost the same TFT I-V characteristics. Moreover, increasing the deposition power from 50W to 150W resulted in a highly conductive IGZO channel layer, where the device exhibited an always ON-state behavior. This finding was correlated to the ion bombardment of the IGZO channel layer by highly energetic Ar^+ ions, which results in the formation of an oxygen-deficient region and high conductivity. Huang *et al.* studied the effect of rapid thermal annealing of the IGZO channel layer at 250°C in N_2 and O_2 environments [25]. In this study, a higher concentration of V_o was observed after N_2 annealing than O_2 annealing, demonstrating that the annealing environment can also affect the chemical composition of IGZO thin-films. Ahn *et al.* showed that ion bombardment of an IGZO surface during Ar plasma treatment, by preferential sputtering of oxygen by Ar^+ bombardment, results in the formation of V_o and higher film conductivity [12]. Kang *et al.* demonstrated that Ar plasma treatment of IGZO back-channel, which increases the channel carrier concentration, results in higher field-effect mobility in IGZO TFTs [13]. In this study, higher carrier concentration of a plasma-treated IGZO channel layer was correlated to the formation of V_o. Furthermore, dry-etching of transparent metal oxides, by breaking the metal-oxygen bonds, resulted in the formation of oxygen-deficient regions and higher carrier concentration and conductivity in IGZO thin-films [14, 15]. A N_2O plasma treatment was tried by Kim *et al.* [14] to repair the back-channel damage to IGZO TFTs caused by the dry-etching process; however, they were not successful. On the other hand, they reported that the I-V characteristics of IGZO TFTs can be repaired by removing the etch-damaged layer using a shallow wet-cleaning treatment. Park *et al.* showed that the electron carrier concentration of IGZO channel layers increased from 10^{14} to 10^{20} upon their exposure to the Ar plasma treatment [15]. This dramatic change in the carrier concentration was related to the formation of the oxygen deficient region in the IGZO film surface rather than a change in the chemical composition of the cations.

It was suggested that, as a result of the physical momentum transfer between the plasma ions and the surface material atoms, Ar ion bombardment results in the preferential sputtering of the relatively light oxygen atoms from the surface and formation of oxygen deficiencies. Although many research groups have correlated the origin of IGZO conductivity to V_o shallow donors, recently a few reports have shown that V_o cannot explain the n-type conductivity in IGZO thin-films and it just work as deep fully occupied states [73]. These groups believe that the addition of hydrogen atoms converts the V_o into shallow donors, and raises the Fermi level. Thus, they have correlated the origin of n-type conductivity to the formation V_o-H complex. These findings are very similar to what was observed for the ZnO thin-films [58] shown in the previous section (2.4.1.1).

2.4.2.2. Hydrogen (H)

Kamiya *et al.* studied the role of hydrogen atoms in IGZO thin-films using density functional theory (DFT) [11]. They found that hydrogen doping of IGZO material, through formation of –OH bonds, with small energy formation, results in the generation of free electrons in this material system. Shao *et al.* reported that the formation of a highly conductive IGZO thin-film at room temperature is possible, using a hydrogen plasma treatment [74]. These results were attributed to the capability of the H-plasma treatment to generate a high-density of electrons even at room temperature. Ahn *et al*. reported the possibility of formation of a source/drain region in IGZO TFTs undergoing a H_2 plasma treatment [12]. They reported that hydrogen by itself works as a shallow donor and results in a lower sheet resistance in IGZO films. It has been demonstrated that hydrogen diffusion from a PECVD SiN_x layer to the oxide materials increases the carrier concentration in this material system [10]. In addition, it is also found that the IGZO thin-films covered by a high SiH_4/N_2 ratio shows lower resistivity. Park *et al.* also showed that the

concentration of H atoms in IGZO film increased after covering by PECVD SiO_x [9]. The higher conductivity was correlated to the diffusion of H atoms dissociated from SiH_4 in the plasma to the IGZO film. Ahn *et al.* reported that water vapour annealing of IGZO TFTs results in better I-V characteristics [75]. These improvements were correlated to the formation of V_o or –OH bonding in IGZO channel layers, resulting in the formation of higher carrier concentration in the water-vapour annealed IGZO channel layer and reduction of the conduction band offset.

Chapter 3

3. Effect of material structure, surface topography, and chemical composition of ZnO and IGZO channel layers on the current-voltage (I-V) characteristics of ZnO and IGZO TFTs

3.1. Introduction

During the past few years, metal oxide TFTs have attracted remarkable attention both in academia and industry. ZnO is the crystalline material most frequently reported as an oxide TFT channel layer. In addition, ZnO-based multicomponent amorphous metal oxides, especially IGZO, due to their unique properties such as high mobility even at low-temperature process, optical transparency, amorphous structure, and smooth surface have opened a new window to large-area transparent flexible electronic devices [46-48]. In this section, electrical dependence on the material properties, surface topography, and chemical composition of the metal oxide channel layers in ZnO and IGZO TFTs are investigated by varying the channel layer deposition temperatures (RT and 150°C) and the annealing environments (air and vacuum).

It has been reported that surface roughness of the gate dielectric adversely affects the current-voltage (I-V) characteristics of ZnO and IGZO TFTs through the introduction of interfacial defects at the semiconductor/dielectric interface [76]. In addition, hydrogen atoms are shown to work as shallow donors and result in a higher conductivity in ZnO and IGZO channel layers [11]. Hence, in order to exclude the effects of surface roughness of the gate dielectric and the out-diffusion of hydrogen (H) atoms from PECVD conventional gate dielectrics to the IGZO channel layer during fabrication processes, bottom gate MO-TFTs were fabricated on thermally grown SiO_2 with a very smooth surface topography, having a minimum concentration of H atoms.

3.2. Experimental

Six separate sets of ZnO and six separate sets of IGZO bottom-gate TFT configurations were fabricated on a highly p-type doped (ρ ~10^{-3} ohm.cm) silicon substrate with a 100 nm thick thermal SiO_2 layer used as the gate dielectric for the TFT device. A 2-inch diameter ZnO (composition: ZnO, purity: 99.99%) and a 2-inch diameter IGZO (composition: InGaZnO4, purity: 99.99%) targets were used to deposit the ZnO and IGZO channel layers by rf-sputtering. In the first, second, and the third ZnO TFT sample sets, the channel layer configuration consisted of a 50 nm thick ZnO film sputtered at room temperature (RT), 150˚C and 220˚C, respectively. In the fourth, fifth, and the sixth ZnO sample sets, the TFT channel layers consisted of air-annealed RT ZnO, vacuum-annealed RT ZnO, and vacuum-annealed 150˚C ZnO thin-films, respectively. On the other hand, in the first, second, and the third IGZO TFT sample sets, channel layer configurations consisted of 50 nm thick as-deposited RT IGZO, air-annealed RT IGZO, and vacuum-annealed RT IGZO, respectively. In the fourth, fifth, and the sixth IGZO TFT sample set, the TFT channel layer consisted of 50 nm thick as-deposited 150˚C IGZO, air-annealed 150˚C IGZO, and vacuum-annealed 150˚C IGZO, respectively. For all the samples, vacuum-annealing was done at 150°C at a base pressure of ~10^{-7} Torr; and air-annealing was performed at 150˚C under atmospheric pressure. Both ZnO and IGZO thin-films were sputtered under the same sputtering conditions (power=100W, pressure: 5mTorr, and Ar:O_2 ratio of 12:1) developed in the beginning part of this chapter. A 200 nm molybdenum thin-film was sputtered at room temperature directly onto the ZnO and IGZO channel regions as source/drain contact electrodes. For all the samples, individual islands were patterned onto the ZnO and IGZO layer to define the TFT active area followed by photoresist patterning of the source and drain contacts. Following the contact definition, the ZnO

samples went through a post-thermal annealing process in a vacuum (~10^{-7} Torr) at 150°C for 1 hour in order to improve the contact resistance.

3.3. Results

3.3.1. The effects of different sputtering deposition parameters on the resistivity of the metal oxide channel layers

The electrical resistivity of metal oxide (MO) channel layers plays a key role in the current-voltage (I-V) characteristics of the fabricated TFTs. It is reported that IGZO TFTs with a highly conductive channel layer (carrier concentration (n) >10^{19}) do not exhibit switching properties and demonstrate always ON-state behavior, regardless of the applied gate voltage [4]. On the other hand, when the conductivity of the channel layer is too low, the TFTs do not switch on. In addition, in the case of working-TFTs, the electrical conductivity of the channel layer strongly affects the off-current and the $I_{on/off}$ ratio of the fabricated device. As an example, when the device is switched off, increasing the channel layer conductivity promotes the amount of current flow from the source (s) to the drain (d) in TFT structures, which in turn, increases the off-current and decreases the $I_{on/off}$ ratio. Hence, before the TFT fabrication processes are described in the rest of this chapter, this subsection investigates the effects of different deposition parameters such as deposition power (60, 80, 100 W), deposition pressure (5,8,10 mT), and Ar/O_2 ratio (0,7.69,14.28%) on the resistivity of metal oxide thin-films. The resistivity was measured from current-voltage (I-V) characteristics of the deposited films in air ambient and under dark conditions. As can be seen in Table 3-1, ZnO films deposited under different sputtering conditions demonstrate a large variation in terms of their resistivity (~ 8 orders of magnitudes). It is generally accepted that a large number of thin-film grain boundaries gives rise to the formation of increased concentration of defect and trap states, which results in higher resistivity [62, 63]. Therefore, one of the dominant factors in the variation of

resistivity seen in ZnO films deposited under different sputtering conditions is related to the grain size within these films.

Table 3-1 ZnO films with different deposition recipes.

Recipe:	**Ar/O_2 ratio (%)**	**Deposition Temperature (˚C)**	**Deposition Power (W)**	**Deposition Pressure (mTorr)**	**Resistivity (Ω.cm)**
#1	7.69	150˚C	60	5	4.3×10^{10}
#2	7.69	150˚C	80	5	1.5×10^{9}
#3	7.69	150˚C	100	5	2.9×10^{8}
#4	7.69	150˚C	100	8	7.2×10^{9}
#5	7.69	150˚C	100	10	1.1×10^{11}
#6	0	150˚C	100	5	8.4×10^{3}
#7	14.28	150˚C	100	5	8.4×10^{11}

To investigate the possible influence of the sputtering parameters on the grain size and the electrical properties of ZnO thin-films, the surface topography of the deposited films were analyzed by AFM. As can be seen in Figure 3-1, excluding the recipe#7, the smaller grain size resulted in higher resistivity. In recipe #7 and recipe #6, due to variation in the oxygen flow rate, the concentration of the oxygen deficiencies [58] also might play a key role in different film resistivities, which will be discussed in the next sections. Hence, the resistivity data correlates very well with the grain boundary concentration obtained by AFM and proves our previous suggestion.

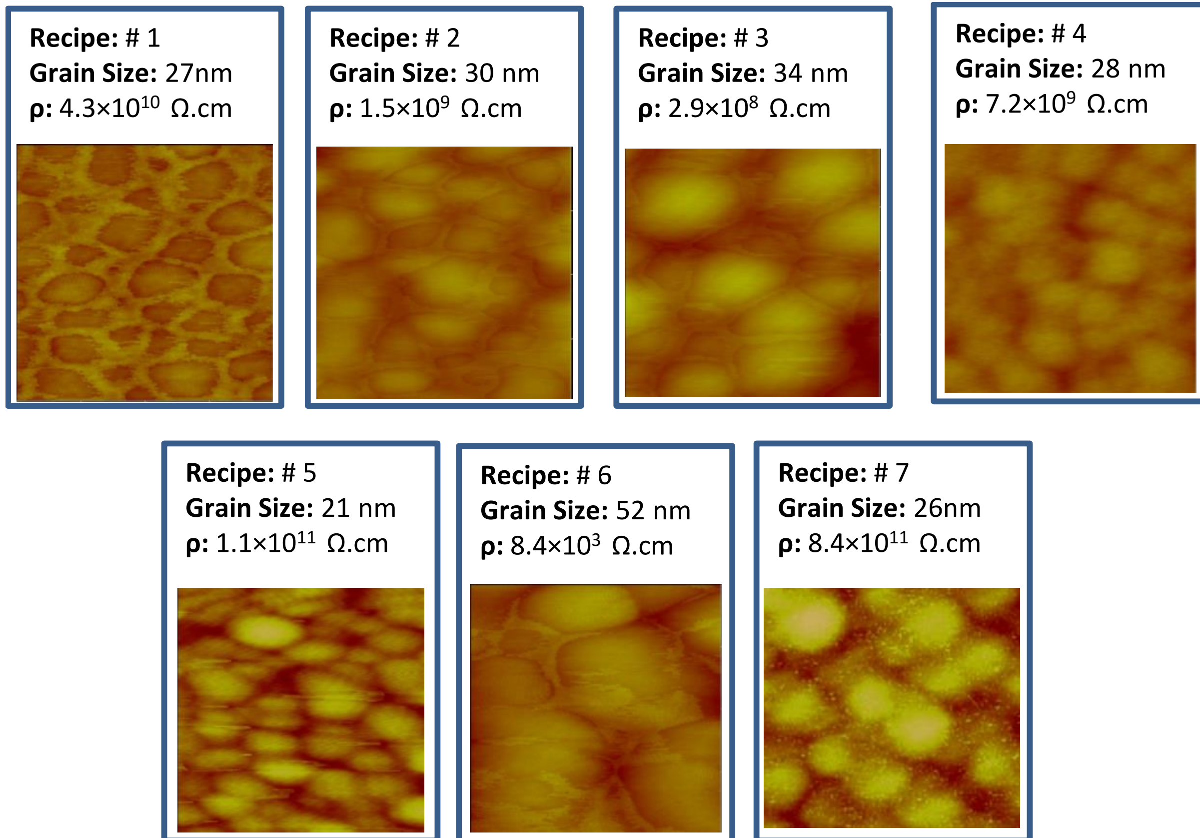

Figure 3-1 The AFM images of ZnO thin-films deposited under different deposition recipes.

Some research groups have reported that when the resistivity of the ZnO channel layer is in the range of 5×10^7 [77] and 10^8 Ω.cm [78], which is very close to recipe #3, ZnO TFTs usually show their optimum I-V characteristics. Hence, in order to not be too far from the resistivity window of the TFT channel layer, the sputtering power, sputtering pressure and Ar/O_2 ratio were kept to be the same as those of recipe #3 in all device fabrication processes.

3.3.2. Effect of the crystalline structure, surface topography, and chemical composition of ZnO channel layer on the I-V characteristics of ZnO TFTs

In order to change the crystalline structure, surface topography, and chemical composition of ZnO thin-films, two different sets of experiments are designed. The first set investigated the effect of different deposition temperatures, and the second set explored the effects of a low-temperature annealing process on the crystalline structure, surface topography, and chemical

composition of ZnO channel layers. Results are correlated to the I-V characteristics of the ZnO TFTs.

3.3.2.1. Channel layer deposition temperature

In this subsection, the effect of a low-temperature annealing on the crystalline structure, surface topography, and chemical composition of ZnO thin-films are investigated and correlated to the I-V characteristics of the ZnO TFTs. Figure 3-2 shows the SEM images and XRD patterns of ZnO thin-films sputtered at different deposition temperatures.

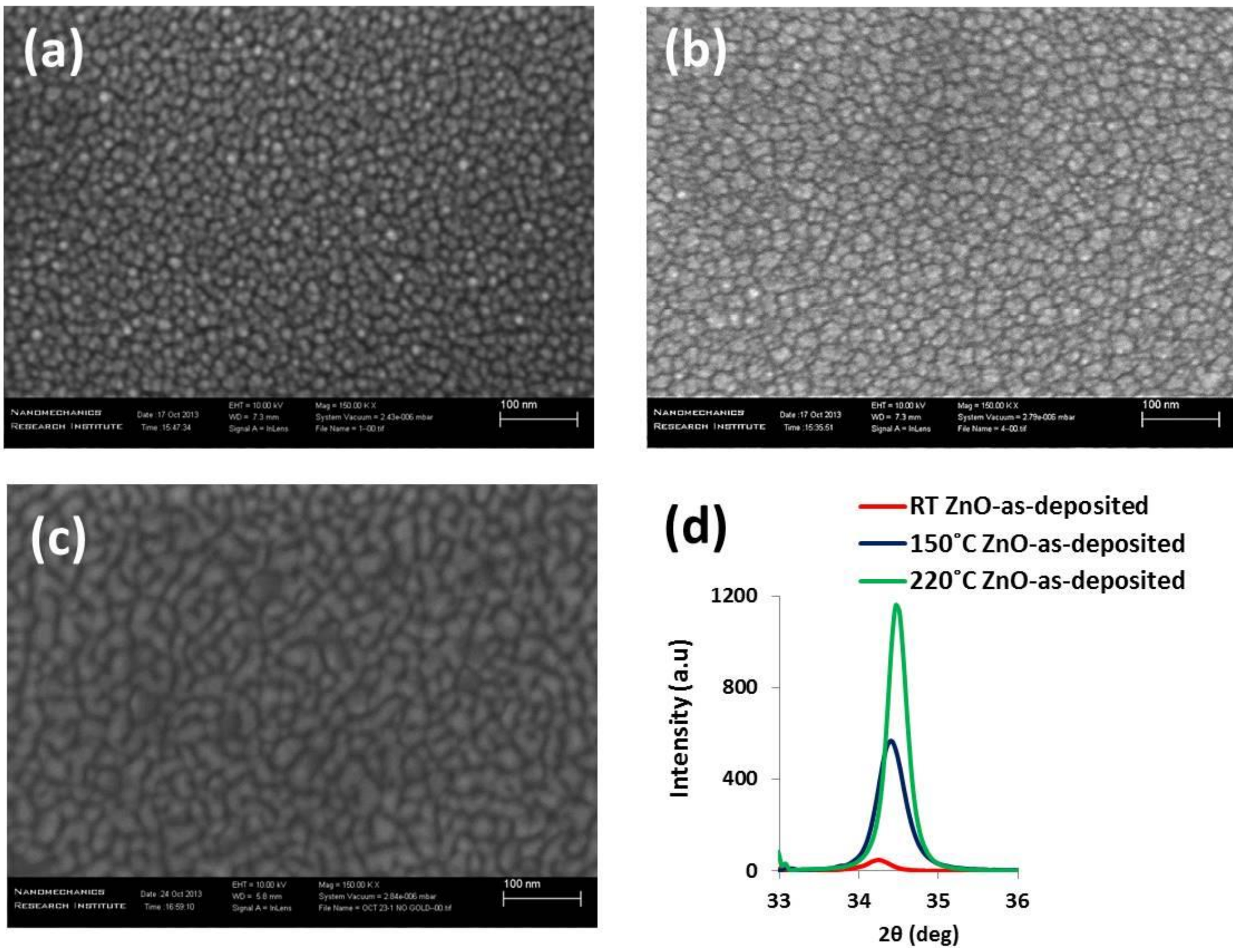

Figure 3-2 The SEM images (a,b,c) and XRD patterns (d) of ZnO thin-films sputtered at different deposition temperatures.

As seen in SEM images, at a higher deposition temperature (220˚C) (Figure 3-2(a)), the grain size of the ZnO film is found to be larger than the grain size of the 150˚C (Figure 3-2(b)), and room temperature (RT) (Figure 3-2(c)), ZnO thin-films, respectively, which is similar to the AFM grain size trend observed in this study.

These findings can be correlated to the higher diffusive ability of atoms or molecules at higher deposition temperature, giving rise to larger grain size. The XRD patterns of the ZnO films are shown in Figure 3-2(d). All the ZnO films demonstrated hexagonal wurtzite crystal structure with a sharp peak at ~32.44° which is correlated to the (002) plane of ZnO. XRD patterns of the (002) plane showed an increase in peak intensity as well as a decrease in the full width at half maximum (FWHM) from RT ZnO to 150˚C processed structures, and the 220˚C ZnO films, respectively. These results reveal that higher deposition temperature leads to better crystallinity in the ZnO thin-films, probably due to the higher kinetic energy of the sputtering species which determines the adatom mobility for crystallite growth. The average grain size (D) of the ZnO thin-films was calculated using Debye–Scherrer formula [79] (Eq. (3.1)) (extracted from the XRD data)

$$D=\frac{0.9\,\lambda}{\beta Cos\theta} \qquad (3.1)$$

where $\lambda = 0.154$ nm is the wavelength of the X-ray radiation used, θ is the Bragg diffraction angle of the XRD peak, and β is the measured broadening of the diffraction line peak at an angle of 2θ, at FWHM in radians. It is found that the average grain size increased from 16 nm to 23 nm, and to 29 nm, for RT ZnO, 150˚C ZnO, and 220˚C ZnO thin-films, respectively, which confirms the earlier SEM results.

It is reported that different concentration of hydrogen (H) atoms, oxygen deficiencies (especially $H\text{-}V_o$ complex), and Zn:O ratios can affect the conductivity of ZnO thin-films [56-59]. Thus, in addition to the film crystallinity and the thin-film grain size measurements, to further determine

the effect of deposition temperature on the material and electrical properties of ZnO thin-films, the chemical composition of ZnO thin-films, from the surface to the bulk, were investigated using X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry (SIMS) depth profiles measurements. The metal ratio of the bulk material was also analyzed quantitatively by survey analysis of XPS data using CasaXPS software.

In the first step, the chemical composition of the 150°C and 220°C ZnO films was analyzed by XPS depth profile. After energy calibration to surface carbon, the XPS peak binding energy of Zn, $2P_{3/2}$, in both 150°C and 220°C films exhibited a positive shift in the binding energy compared to Zn-Zn bonds (1021.5) [80] and were recorded at 1022.29 eV and 1022.31 eV, respectively, both of which are very close to the binding energy of Zn^{2+} in the ZnO thin-films. This shift to higher energy indicates that the Zn-O bonds seem to be dominant in both films, regardless of the annealing process [5]. The O 1s spectra of ZnO films may be fitted into three peaks, one located at low-binding energy (O_L), one at medium-binding energy (O_M), and the third at high-binding energy (O_H) through a Gaussian profile, Figure 3-3. The O_L peak is attributed to the oxygen atoms in the oxide lattice without oxygen vacancy (V_o), O_M is attributed to the V_o, and the O_H peak is surface oxygen [21, 81].

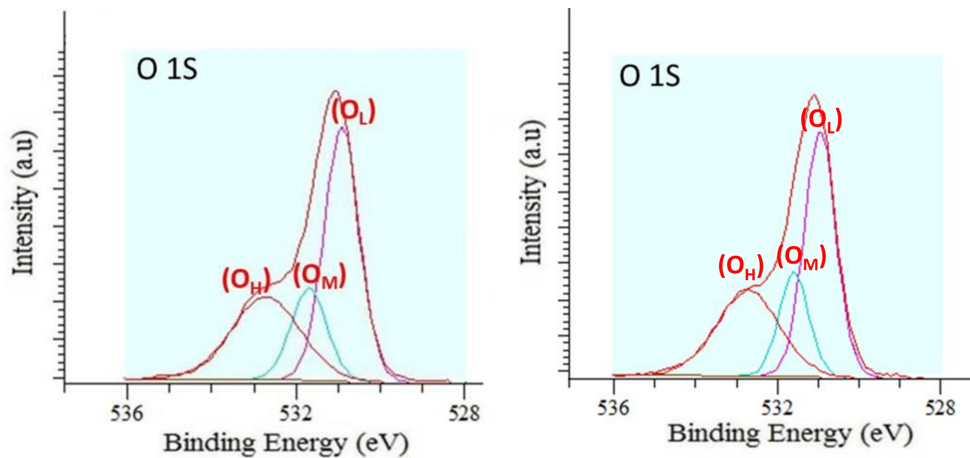

Figure 3-3 O 1s XPS spectra of (a) 150 °C and (b) 220 °C ZnO films after surface contamination cleaning.

In order to investigate the effect of deposition temperature (150°C and 220°C) on the concentration of oxygen deficiencies in ZnO films, the O 1s spectra of the above films were analyzed before surface contamination cleaning (depth = 0 nm), after surface contamination cleaning (depth= 0.2 nm), and deep in the bulk (depth=45 nm). As seen in Figure 3-4, very similar results were observed for the oxygen deficiency concentration in the bulk (depth=45 nm) of both 150°C (19.53 %) and 220°C (19.93 %) ZnO films. In addition, it is worth noting that both 150°C (13.21 %) and 220°C (14.18 %) samples exhibited lower concentration of oxygen deficiencies on the surface (before surface contamination cleaning) compared to the bulk. On the other hand, a similar concentration of oxygen deficiencies was observed in the bulk and the surface of the both 150°C ZnO (19.53 vs. 18.75 %) and 220°C (19.93 vs. 19.04%) films, after surface contamination cleaning with mild ion etching.

XPS measurements before surface contamination cleaning (Depth= 0 nm)

As-deposited 150°C ZnO			As-deposited 220°C ZnO		
Zn (At %)	O (At %)	V_o (%)	Zn (At %)	O (At %)	V_o (%)
19.66	80.34	13.21	21.9	78.1	14.18

After surface contamination cleaning with mild ion etching (Depth= 0.2 nm)

As-deposited 150°C ZnO			As-deposited 220°C ZnO		
Zn (At %)	O (At %)	V_o (%)	Zn (At %)	O (At %)	V_o (%)
43.9	56.1	18.75	45.68	54.32	19.04

XPS depth profile measurements deep in the bulk (Depth= 45 nm)

As-deposited 150°C ZnO			As-deposited 220°C ZnO		
Zn (At %)	O (At %)	V_o (%)	Zn (At %)	O (At %)	V_o (%)
49.88	50.12	19.53	50.2	49.8	19.93

Figure 3-4 XPS depth profiles of zinc (Zn), oxygen (O), and oxygen vacancy (V_o) for as-deposited 150°C and 220°C ZnO thin-films.

XPS survey analysis of the bulk films also demonstrated a similar atomic ratio for zinc (Zn) and oxygen (O) in both 150°C (Zn:O=49.88:50.12 (At%)) and 220°C (Zn:O=50.2:49.8 (At%)) films. After comparing the concentration of oxygen deficiency and the Zn:O atomic ratio, in the next step, hydrogen concentrations of the deposited films were also analyzed and compared using SIMS depth profiles measurements. As seen in Figure 3-5, a similar hydrogen depth profiles were observed deep in the bulk (~30-50 nm) of the both ZnO films.

Hence, according the XPS and SIMS depth profiles findings, it can be stated that the variation in the chemical compositions (especially different concentration of H atoms and oxygen deficiency (H-V_o complexes))[58] is not the dominant factor in the different electrical properties of 150°C and 220°C ZnO films.

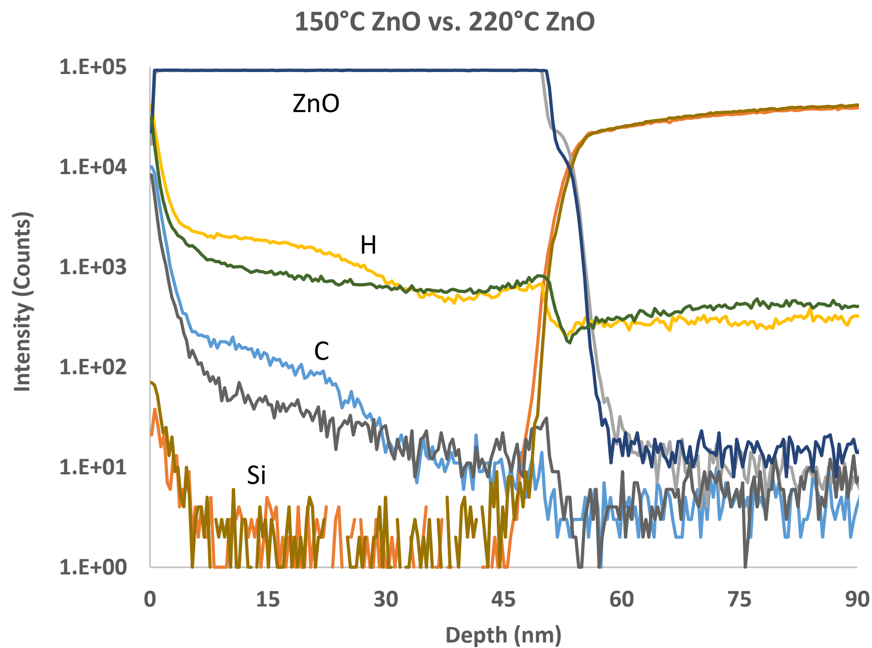

Figure 3-5 SIMS depth profiles of hydrogen (H), zinc oxide (ZnO), silicon (Si), and carbon (C) for as-deposited 150°C and 220°C ZnO thin-films.

Hence, the resistivity data obtained in this study, using I-V measurements, which showed that the lower resistivity ($\rho = 5.7\times10^{6}$) for 220°C compared to 150°C film ($\rho = 2.9\times10^{8}$) can be correlated to the SEM and XRD results, which exhibit larger grain size for the film deposited at higher temperatures [62, 63].

To further investigate the effect of deposition temperature on the materials properties of ZnO thin-films, the optical transparency of the ZnO thin-films were measured using a UV-Vis spectrometer, and the band-gap energy of the studied samples is estimated using the Tauc plot [82].

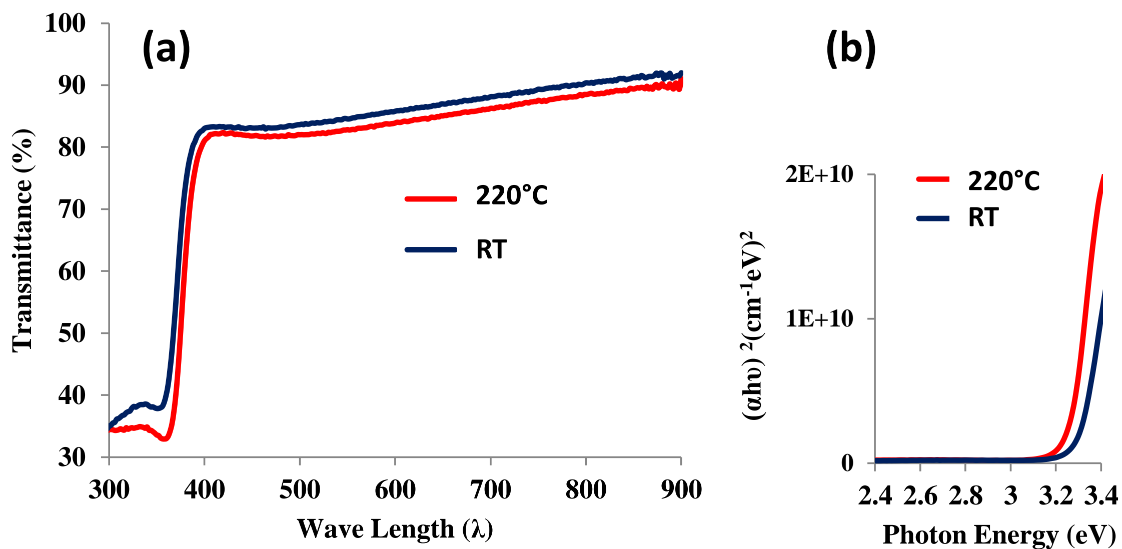

Figure 3-6 Optical transmittance (a) and the band-gap energy (b) of the ZnO thin-films deposited at different temperature.

As can be seen in Figure 3.6, 220˚C ZnO films exhibited slightly lower transparency and a small positive shift in the band edge (Bandgap=3.25 eV) compared to the film deposited at RT (E-gap=3.28 eV). The relationship between absorption coefficient and the concentration of free electrons is shown in Eq. 3.2.

$$\alpha = \frac{N_e q^2 \lambda^2}{8\pi \varepsilon_0 n \tau c^3 m^*}, \qquad (3.2)$$

where α, N_e, q, λ, ε_0, n, τ, $m*$, and c are the absorption coefficient, the concentration of the free electron, the electron charge, the absorption wavelength, the dielectric constant in the vacuum, the refractive index, the relax time, the effective mass of the free electron, and the optical velocity, respectively [83]. It can be seen that the optical absorption/transmittance increases/decreases with concentration of the free electrons, respectively. Thus, lower transparency and smaller bandgap energy in 220˚C ZnO film might also be correlated to the formation of higher carrier concentration in the film, which could be due to a lower concentration of trap centers and grain boundaries in the 220˚C ZnO film. Thus, the optical characteristics also correlate well with the previous SEM, XRD, and AFM results.

Finally, a comparison is made on the I-V characteristics of the TFTs consisted of ZnO channel layers with different crystallinity, surface topography, and chemical compositions. The I-V characteristics of the fabricated TFTs were extracted using the gradual channel approximation. As can be seen in Figure 3-7, RT ZnO device did not show any switching properties, and showed OFF-state behavior regardless of the applied gate voltage. These results suggest that the RT ZnO channel layer has a low carrier concentration similar to a dielectric material, which is insufficient to be the active layer of the TFT. On the other hand, it was found that increasing the channel layer deposition temperature from RT to 150˚C resulted in working TFTs with μ=0.38 cm^2/V.sec, V_T =13 V, $I_{on/off}$ ~10^6, and $I_{off} < 10^{-11}$.

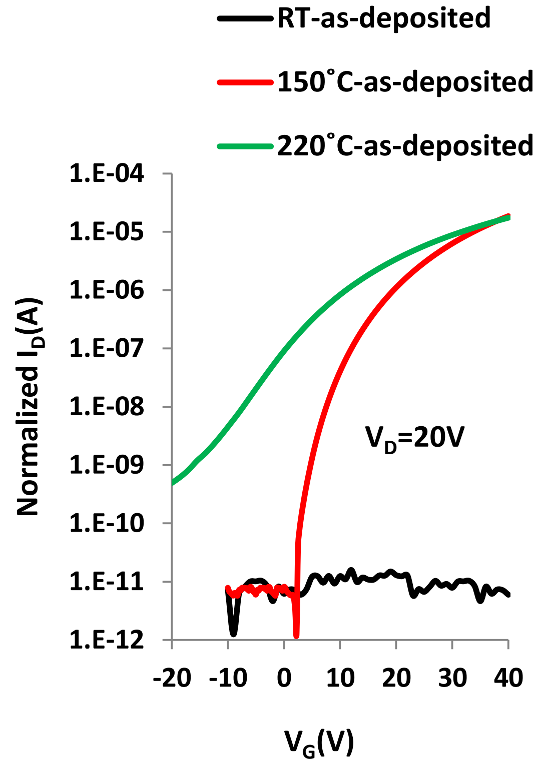

Figure 3-7 Transfer characteristics of the TFTs consisted of ZnO channel layers deposited at different temperatures.

Thus, it is concluded that increasing the channel layer deposition temperature from RT to 150°C improved the film crystallinity and reduced the concentration of grain boundaries, resulting in improved TFT electrical characteristics. However, increasing the channel layer deposition temperature from 150°C to 220˚C resulted in a large negative shift in V_T (~ 10V), a degradation in S.S., lower $I_{on/off}$ ratio (~10^4A), and a higher off-current (> 5×10^{-10} A). The off-current can be correlated to the channel layer conductivity based on the following equation, (Eq. 3.3):

$$I_{Doff} = V_D\,(\sigma W d/L) \qquad (3.3)$$

where σ is the electrical conductivity, d is the thickness of the channel layer, W and L are the width and length of the conduction channel respectively, and V_D is the source-drain voltage. According

to the equation 3.3, the higher channel conductivity gives rise to higher off-state current [84]. As both 150°C and 220˚C ZnO thin-films demonstrated a very similar concentration of oxygen deficiency, the chemical composition of the ZnO channel layer could not be the dominant factor in degradation of the I-V characteristics of 220˚C ZnO TFTs. As mentioned earlier, grain boundaries work as a barrier layer against electron transport in ZnO channel layers [62, 63]. Thus, higher off-current and a large negative shift in V_T for the 220°C device could be attributed to the formation of larger grain size in the 220°C channel layer, which results in a highly conductive channel layer with a larger number of carrier concentration.

The roughness of the IGZO channel layer could be a function of underlying interface roughness, which may indicate the introduction of interfacial defects at the semiconductor/dielectric interface, resulting in poor TFT characteristics. This interface roughness may propagate through the semiconductor layer onto the surface of the back-channel of the TFTs. Hence, atomic force microscopy (AFM) was used to compare the surface roughness of IGZO channel layers deposited at 150°C and 220°C. The root-mean square (RMS) roughness, which could be a function of the underlying gate dielectric's surface roughness, for the 150°C and 220°C ZnO thin-films were measured to be 0.81 nm and 1.18 nm, respectively. Thus, the S.S. degradation and poor current-voltage (I-V) characteristics in 220°C TFTs might also be attributed to the higher concentration of interface traps between the channel layer and the gate dielectric.

In addition, several reports have shown that the contact resistance plays a key role in the degradation of S.S. and TFT current-voltage (I-V) characteristics. Thus, rougher surface of the 220°C ZnO channel layer, by formation of higher concentration of interface traps between the channel layer and source/drain (s/d) electrodes, could be another possible reason for degradation in S.S. and I-V characteristics in 220°C ZnO TFTs.

3.3.2.2. Low-temperature thermal annealing

In this subsection, the effect of low-temperature annealing on the crystalline structure, surface topography, and chemical composition of ZnO thin-films is investigated and correlated to the I-V characteristics of the ZnO TFTs. In the previous section (3.3.1.1), it was found that ZnO TFTs with as-deposited RT channel layer did not work as a switch; however, it showed TFT I-V characteristics when the deposition temperature of the channel layer increased to 150°C. In order to investigate the effect of low-temperature (150°C) thermal annealing on the crystalline structure, surface topography, and chemical composition of ZnO channel layer, and electrical performance of ZnO TFTs, I-V characteristics of ZnO TFTs with as-deposited and annealed channel layer were compared together.

As seen in Figure 3-8, TFTs with air and vacuum-annealed RT ZnO channel layer did not show any switching properties and demonstrated always OFF-state behavior, suggesting that even after air and vacuum annealing the conductivity of RT ZnO channel layer is still insufficient to work as a TFT active layer. On the other hand, 150°C ZnO TFTs demonstrated higher μ (1.55 vs. 0.38 cm^2/V.sec) and lower V_T (11 vs. 13 V) after the vacuum annealing process. In addition, it was found that vacuum-annealing treatment decreased the resistivity of 150°C ZnO thin-films from 2.9×10^8 to 6.9×10^7 ohm.cm.

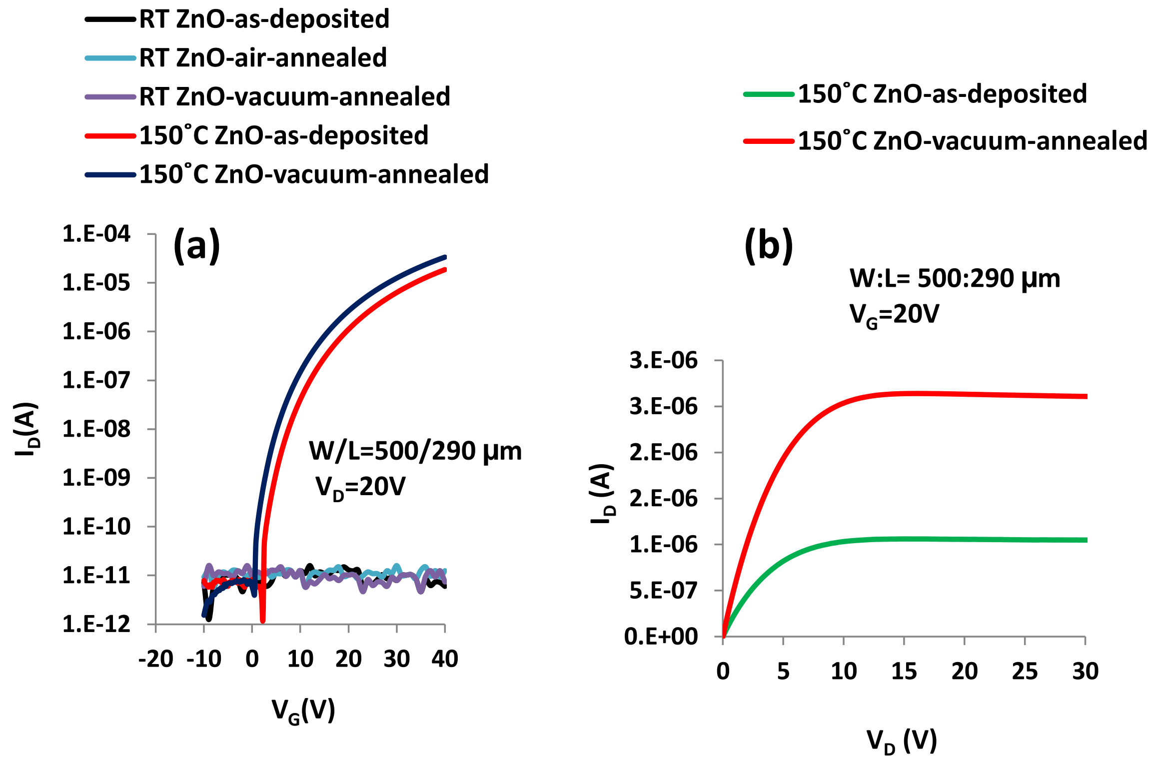

Figure 3-8 Transfer, and (b) out-put characteristics of the ZnO TFTs under different channel layer deposition temperature and annealing conditions.

Atomic force microscopy was used to determine the effect of vacuum annealing on the channel roughness and potential degradation of the metal/semiconductor interface. The surface roughness of the ZnO thin-films before and after vacuum annealing was 0.814 nm and 0.615 nm (Figure 3-9(a,b)), respectively, suggesting that vacuum-annealing results in improved channel layer/gate dielectric and channel layer/(s/d contacts) interface properties. To investigate the effect of vacuum annealing on the crystallinity of the ZnO channel layer, XRD measurements were carried out on the as-deposited and vacuum-annealed films, deposited at 150˚C. Both samples demonstrated a sharp peak at ~32.44°, which is correlated to the (002) plane of ZnO crystallinity (Figure 3-9(c)). According to the XRD results of the ZnO films, (002) plane showed an increase in peak intensity as well as a decrease in FWHM. This finding reveals that low-temperature vacuum-annealing

results in a better crystallinity in ZnO thin-films. The average grain size (D) of the ZnO thin-films was calculated using Debye–Scherrer formula [79]. The average grain size was found to increase with vacuum annealing, from 23 nm for as-deposited film to 25 nm for the vacuum-annealed sample.

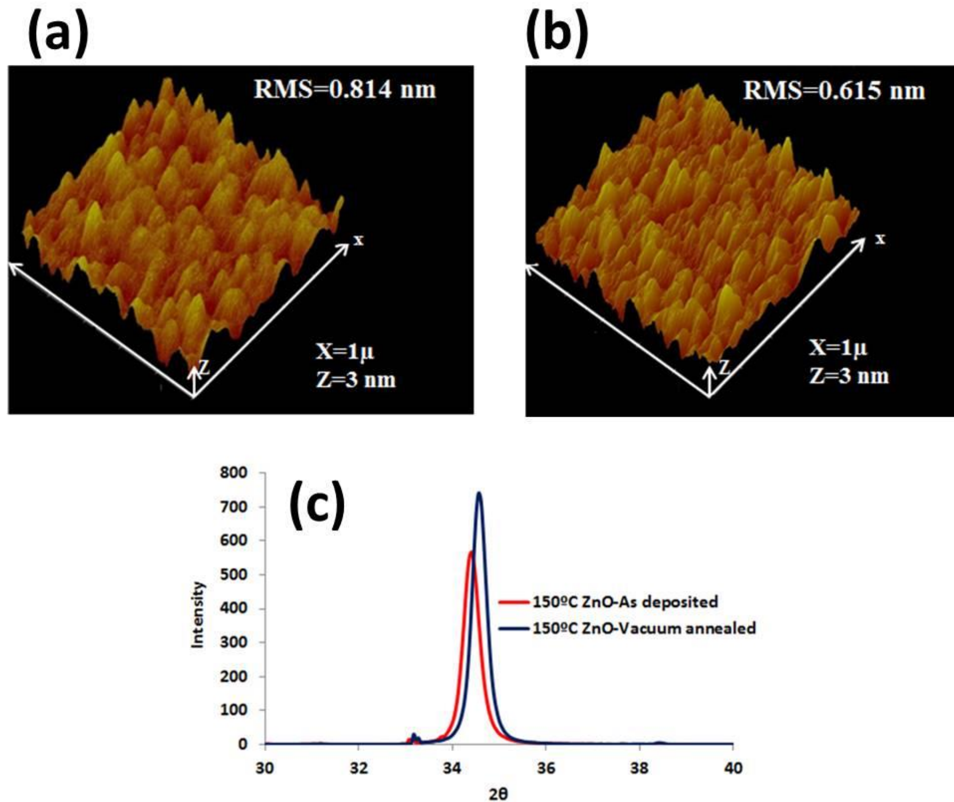

Figure 3-9 AFM images of surface morphology of the (a) as-deposited, and (b) vacuum-annealed ZnO films, and (c) XRD patterns of the as-deposited and vacuum-annealed ZnO films deposited at 150°C.

The decreased resistivity of the vacuum-annealed film is also suggestive of ZnO films with different concentrations of H [55] or H induce oxygen deficiencies (H-V_o complex) [58]. To investigate the possible influence of the thermal annealing on the concentration of H and H-V_o in ZnO thin-films and the electrical performance of ZnO TFTs, the chemical composition of the as-deposited and vacuum-annealed 150°C ZnO films was analyzed by XPS depth profile, XPS survey analysis, and SIMS measurements. According to the XPS results, the peak binding energy of Zn,

$2p_{3/2}$, in both as-deposited and annealed ZnO films exhibited a positive shift toward a higher binding energy compared to the Zn-Zn bonds (1021.5 eV) [80]. This shift to higher energy indicates that the Zn-O bonds seem to be dominant in both films, regardless of the annealing process [5]. The O 1s spectra of ZnO films may be fitted into three peaks, one located at low-binding energy (O_L), one at medium-binding energy (O_M), and the third at high-binding energy (O_H) through a Gaussian profile, Figure 3-10. The O_L peak is attributed to the oxygen atoms in the oxide lattice without oxygen vacancy (V_o), O_M is attributed to the V_o, and the O_H peak is surface oxygen [21, 81].

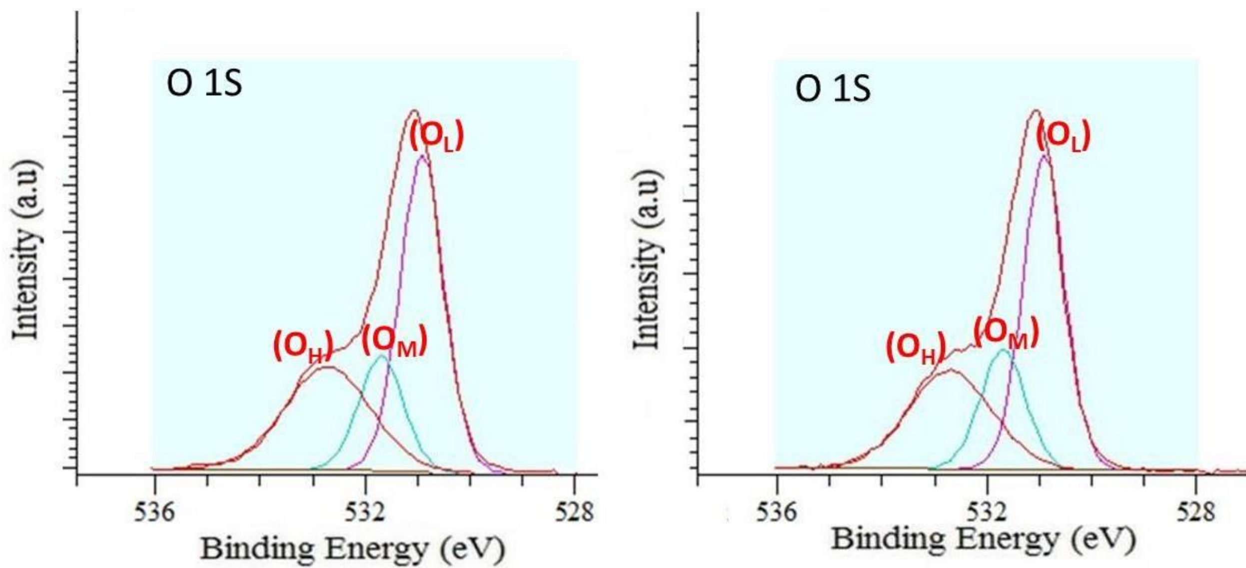

Figure 3-10 O 1s XPS spectra of (a) as-deposited and (b) vacuum-annealed 150°C ZnO films after surface contamination cleaning.

In order to investigate the effect of 150°C vacuum annealing on the concentration of oxygen deficiencies in ZnO films, the O 1s spectra of the above films were analyzed before surface contamination cleaning (depth = 0 nm), after surface contamination cleaning (depth= 0.2 nm), and deep in the bulk (depth=45 nm). As seen in Figure 3-11, very similar results were observed for the

oxygen deficiency concentration in the bulk (depth=45 nm) of both as-deposited (19.53 %) and vacuum-annealed (19.93 %) 150°C ZnO films. In addition, it is worth noting that both as-deposited (13.21 %) and vacuum-annealed (14.63 %) samples exhibited lower concentration of oxygen deficiencies on the surface (before surface contamination cleaning) compared to the bulk. On the other hand, a similar concentration of oxygen deficiencies was observed in the bulk and the surface of the both as-deposited (19.53 vs. 18.75 %) and vacuum-annealed (20.12 vs. 19.2 %) films, after surface contamination cleaning with mild ion etching.

XPS measurements before surface contamination cleaning (Depth= 0 nm)

As-deposited 150°C ZnO			**Vacuum-annealed 150°C ZnO**		
Zn (At %)	O (At %)	V_o (%)	Zn (At %)	O (At %)	V_o (%)
19.66	80.34	13.21	23.39	76.61	14.6 3

After surface contamination cleaning with mild ion etching (Depth= 0.2 nm)

As-deposited 150°C ZnO			**Vacuum-annealed 150°C ZnO**		
Zn (At %)	O (At %)	V_o (%)	Zn (At %)	O (At %)	V_o (%)
43.9	56.1	18.75	47.2	52.8	19.2

XPS depth profile measurements deep in the bulk (Depth= 45 nm)

As-deposited 150°C ZnO			**Vacuum-annealed 150°C ZnO**		
Zn (At %)	O (At %)	V_o (%)	Zn (At %)	O (At %)	V_o (%)
49.88	50.12	19.53	50.38	49.62	20.12

Figure 3-11 XPS depth profiles of zinc (Zn), oxygen (O), and oxygen vacancy (V_o) for as-deposited 150°C and vacuum-annealed 150°C ZnO thin-films.

XPS survey analysis of the bulk films also demonstrated a similar atomic ratio for zinc (Zn) and oxygen (O) in both as-deposited (Zn:O=49.88:50.12 At%) and vacuum annealed (Zn:O=50.38:49.62 At%) 150°C ZnO films. After comparing the oxygen deficiency concentration and the Zn:O atomic ratio, in the next step, hydrogen concentrations of the deposited films were also analyzed and compared using SIMS depth profiles measurements. As seen in Figure 3-12, a similar hydrogen depth profiles were observed deep in the bulk (~30-50 nm) of the both ZnO films.

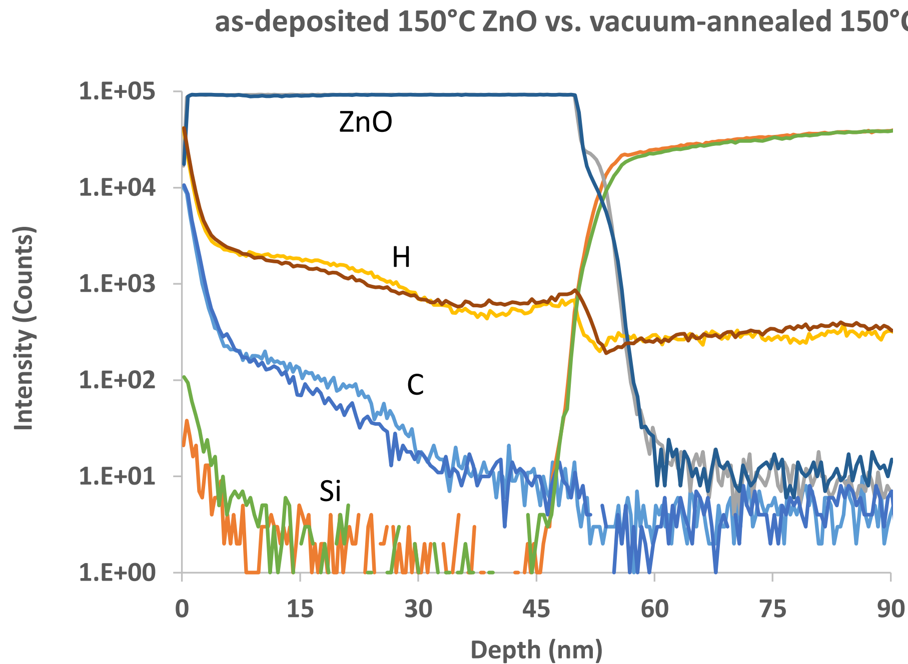

Figure 3-12 SIMS depth profiles of hydrogen (H), zinc oxide (ZnO), silicon (Si), and carbon (C) for as-deposited 150°C and vacuum-annealed 150°C ZnO thin-films.

Because as-deposited 150°C ZnO and 150°C vacuum-annealed 150°C ZnO channel layers demonstrated similar chemical composition, it can be concluded that improving the film crystallinity of the channel layer and the better interface properties (as discussed in the previous

section (3.3.2.1)) are the dominant factors in the superior I-V characteristics of the low-temperature thermal-annealed ZnO TFTs.

3.3.3. Effect of chemical composition and surface topography of IGZO channel layer on the I-V characteristics of IGZO TFTs

In this section, the effect of the chemical composition and surface topography of IGZO channel layers on the I-V characteristics of the IGZO TFTs is investigated. In order to change the chemical composition and surface topography of IGZO thin-films, two different sets of experiments were designed. The first investigation studied the effect of different deposition temperatures (RT and 150°C), and the second studied the effects of low-temperature (150°C) thermal-annealing on the surface topography and chemical composition of IGZO thin-films. The results of both sets were correlated to the I-V characteristics of the IGZO TFTs (Figure 3-13).

As seen in Figure 3-13(a), similar to ZnO TFTs, as-deposited RT IGZO TFTs did not show any switching properties, and demonstrated always OFF-state behavior regardless of the applied gate voltage, suggesting that the as-deposited RT IGZO thin-film, deposited on the thermal SiO_2 dielectric, has a low carrier concentration, which is insufficient as a TFT channel layer.

On the other hand, TFTs with as-deposited 150˚C IGZO channel layers exhibited switching properties with μ=8.8 cm^2/V.sec, V_T=4.2 V, S.S.=0.42 V/decade, and $I_{on/off}$ ratio of higher than 10^6, (Figure 3-13 (b)). In addition, unlike the ZnO TFTs, 150˚C IGZO TFTs demonstrated a huge negative-shift in V_T after vacuum-annealing and exhibited poor switching properties with always ON-state behavior, suggesting that vacuum-annealing had resulted in a highly conductive IGZO channel layer. A similar trend was observed for the RT IGZO TFTs. RT IGZO TFTs demonstrated an appropriate I-V characteristic with μ=8.1 cm^2/V.sec, V_T=3.5 V, S.S.=0.51 V/decade, and an

$I_{on/off} > 10^6$ after the vacuum-annealing process, suggesting formation of more carrier concentration in the channel layer.

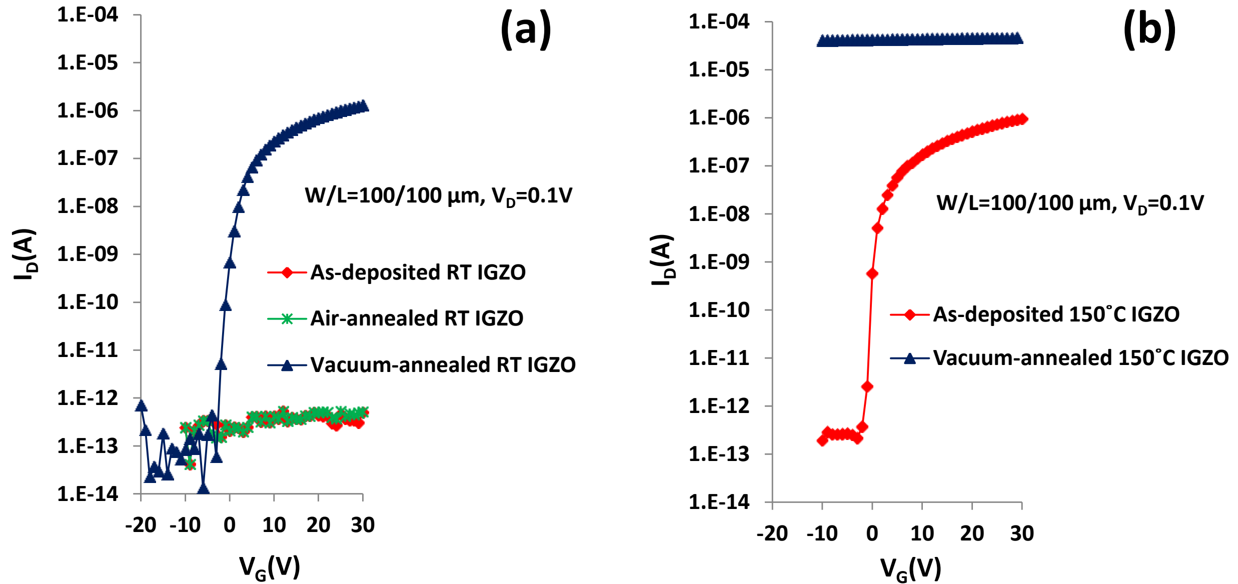

Figure 3-13 The effect of the post-annealing process on the transfer characteristics of the IGZO TFTs with (a) RT, and (b) 150°C channel layers.

Hydrogen atoms, oxygen deficiencies (especially H-induce V_o), and metal ratios are three main causes of conductivity difference in IGZO thin-films [4, 73]. In order to correlate the I-V characteristics of the IGZO TFTs with chemical composition of the IGZO channel layer, in the first step, the atomic concentration of as-deposited RT IGZO, as-deposited 150°C IGZO, and vacuum-annealed 150°C IGZO were compared together using XPS depth profile, Figure 3-14. As can be seen, while similar depth profiles and atomic concentrations were observed for In, Ga, and Zn, an obvious change was observed in the atomic ratio of oxygen, where the as-deposited RT IGZO demonstrated the highest and vacuum annealed 150°C IGZO exhibited the lowest concentration of oxygen, respectively.

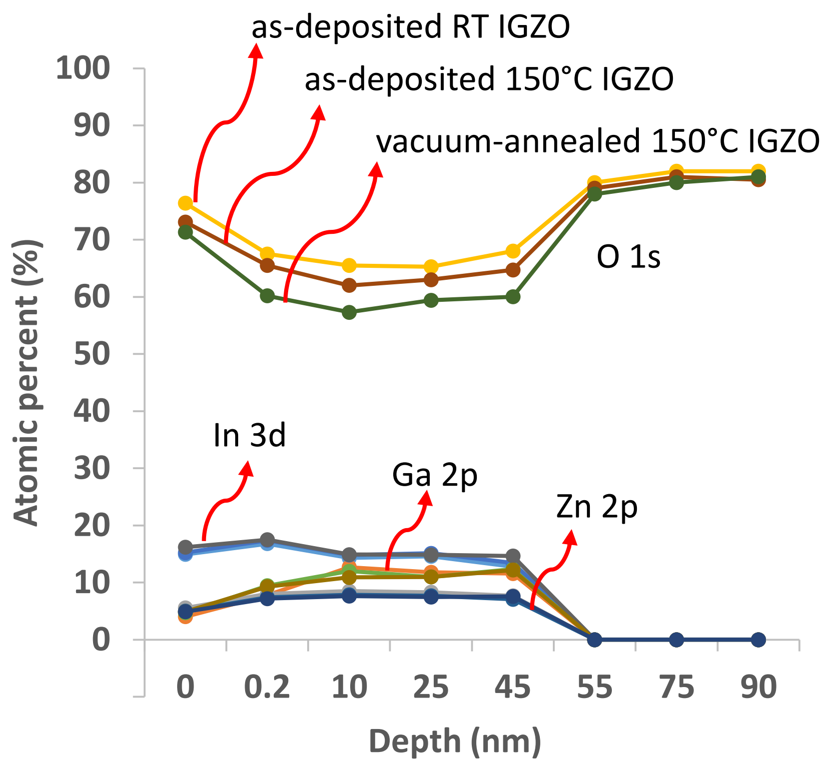

Figure 3-14 XPS depth profiles of indium (In), gallium (Ga), zinc (Zn), and oxygen (O) for as-deposited RT IGZO, as-deposited 150°C IGZO, and vacuum-annealed 150°C IGZO thin-films.

The O 1s spectra, from the XPS characterization, obtained in different depths, are fitted into three peaks, centered at 530.7 eV (O_L peak), 531.5 eV (O_M peak), and 532.5 eV (O_H peak) using a Gaussian profile (Figure 3-15), where the O_M correlates to the oxygen deficiencies in the IGZO films.

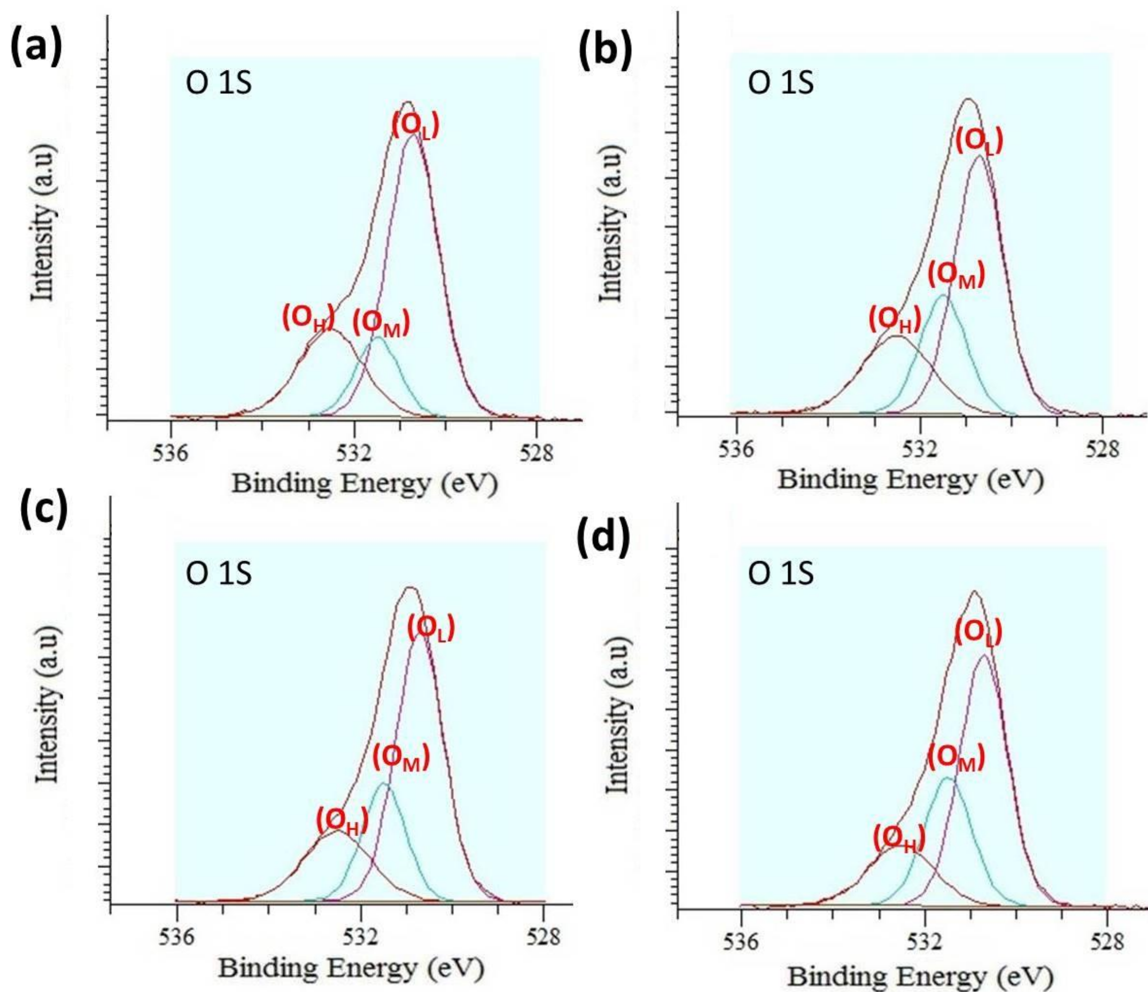

Figure 3-15 O 1s XPS spectra of the (a) as-deposited RT IGZO, (b) vacuum-annealed RT IGZO, (c) as-deposited 150°C IGZO, and (d) vacuum-annealed 150°C IGZO films after surface contamination cleaning.

In order to investigate the effect of deposition temperature (RT and 150°C) and thermal-annealing process on the concentration of oxygen deficiencies in IGZO films, the O 1s spectra of the above films were analyzed before surface contamination cleaning (depth = 0 nm), after surface contamination cleaning (depth= 0.2 nm), and deep in the bulk (depths=10, 25, and 45 nm).

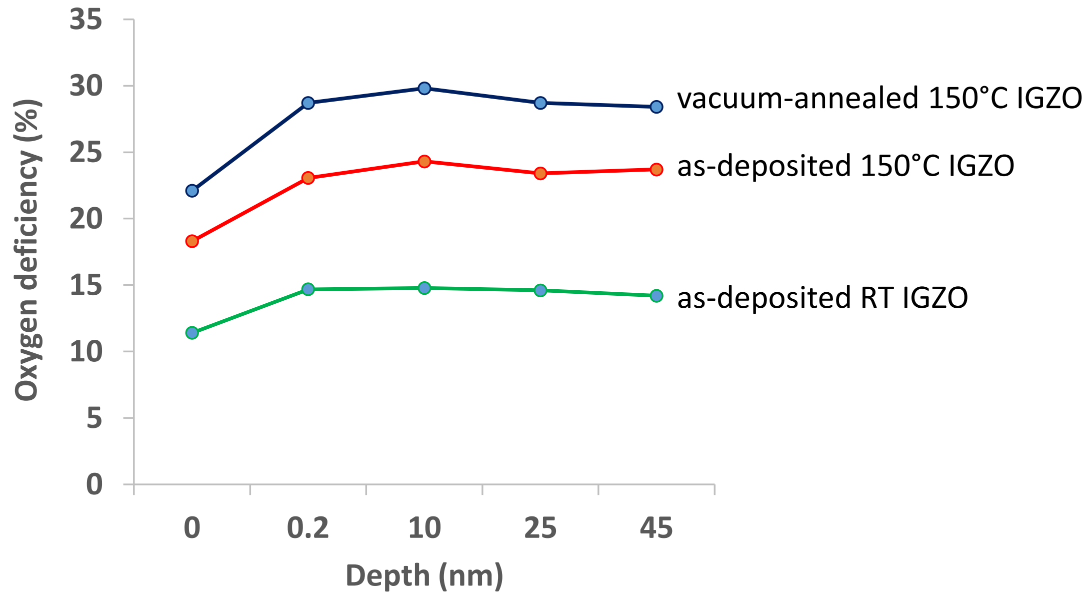

Figure 3-16 Concentration of oxygen deficiency (%) at different depths in as-deposited RT IGZO, as-deposited 150°C IGZO, and vacuum-annealed 150°C IGZO thin-films.

As seen in Figure 3-16, as-deposited RT IGZO and vacuum-annealed 150°C IGZO thin-films demonstrated lower (~14.68 %) and higher (~28.71%) bulk concentrations of oxygen deficiencies than those of as-deposited 150°C IGZO (~23.06) and vacuum-annealed RT IGZO (~23.42) (results are not shown here) thin-films.

In addition, it is worth noting that, similar to ZnO thin-films, before surface contamination cleaning, all the samples exhibited higher concentration of oxygen deficiencies in the bulk compared to the surface. On the other hand, as can be seen in Figure 3-16, a similar concentration of oxygen deficiencies was observed in the bulk and the surface of the IGZO films, after surface contamination cleaning with mild ion etching. Figure 3-13 shows while TFT with vacuum-annealed RT IGZO channel layer demonstrates an expected I-V characteristic, it does not exhibit

any switching properties after air annealing, suggesting presence of a lower concentration of oxygen deficiencies in air-annealed samples than in the vacuum-annealed ones. This observation may be attributed to the higher possibility of adsorption and/or diffusion of O_2 molecules in air than in the vacuum. Findings obtained for oxygen deficiencies correlate very well with our I-V characteristics results. However, oxygen deficiencies are not the only reason for different conductivities in IGZO thin-films. Other origins such as metal ratios and hydrogen concentration also need to be taken into account. In the next step, the metal ratio of the IGZO thin-films was analyzed quantitatively by survey analysis of XPS data and showed a similar atomic ratio (In:Ga:Zn=14.1:12.1:7.7 (%At)) in the bulk of IGZO thin-films, processed under different conditions. After quantitative analysis of the metal ratio, the concentration profiles of hydrogen, In, Ga, and ZnO were also analysed, using SIMS measurements, Figure 3-17.

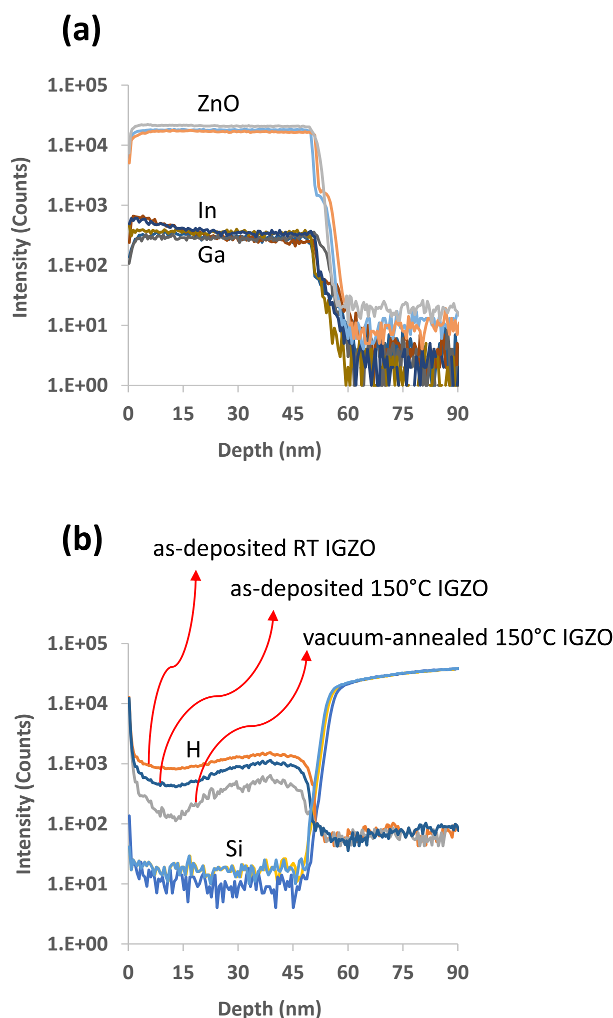

Figure 3-17 SIMS depth profiles of (a) zinc oxide (ZnO), indium (In), and gallium (Ga), and (b) hydrogen (H) and silicon (Si) in as-deposited RT IGZO, as-deposited 150°C IGZO, and vacuum-annealed 150°C IGZO thin-films.

Results obtained from the SIMS depth profiles demonstrated nearly constant concentration-depth profiles for In, Ga, and ZnO in IGZO thin-films processed under different conditions. However, a slightly higher H concentration was observed in IGZO film deposited at RT than in IGZO deposited at 150°C. In addition, vacuum-annealed film exhibited an even lower H concentration than the as-deposited 150°C IGZO film.

Although the as-deposited RT IGZO contained higher H concentration, it showed lower conductivity and its TFT demonstrated always OFF-state behavior (Figure 3-13 (a)), regardless of

the applied voltage. This finding suggest that the H was mostly inactive as an electron donor. It has been reported that IGZO can incorporate excess weakly-bonded oxygens as detected by TDS [85]. Hence, it can be suggested that the free electrons, generated by the formation of –OH bonds [86], are compensated for by the excess oxygen ($O \rightarrow O^{-}/O^{2-}$) in as-deposited RT IGZO films. On the other hand, higher conductivity of the vacuum-annealed film can mainly be attributed to the desorption of the O- and H-related species as detected by TDS. This result is in agreement with the findings of other groups [87], which demonstrated a similar curve for the H_2O desorption and electrical conductivity variation of IGZO thin-films. It is worth noting that although as-deposited 150°C IGZO demonstrates slightly lower H concentration compared to as-deposited RT IGZO, it shows higher conductivity. Similar to our previous arguments, the higher conductivity of 150°C IGZO thin-films can be correlated to the lower concentration of excess weakly-bounded oxygen in films deposited at a higher temperature. Hence, the XPS and SIMS depth profile results correlate very well with the previous IGZO TFT I-V characteristics.

Similar to the discussion of ZnO TFTs in previous sections, the roughness of the IGZO channel layer could be a function of underlying interface roughness, which may indicate the introduction of interfacial defects at the semiconductor/dielectric interface, resulting in poor TFT characteristics. This roughness may propagate through the semiconductor layer onto the surface of the back-channel of the TFTs. Hence, atomic force microscopy (AFM) was used to compare the surface roughness of IGZO channel layers deposited and annealed under different conditions (Figure 3-18).

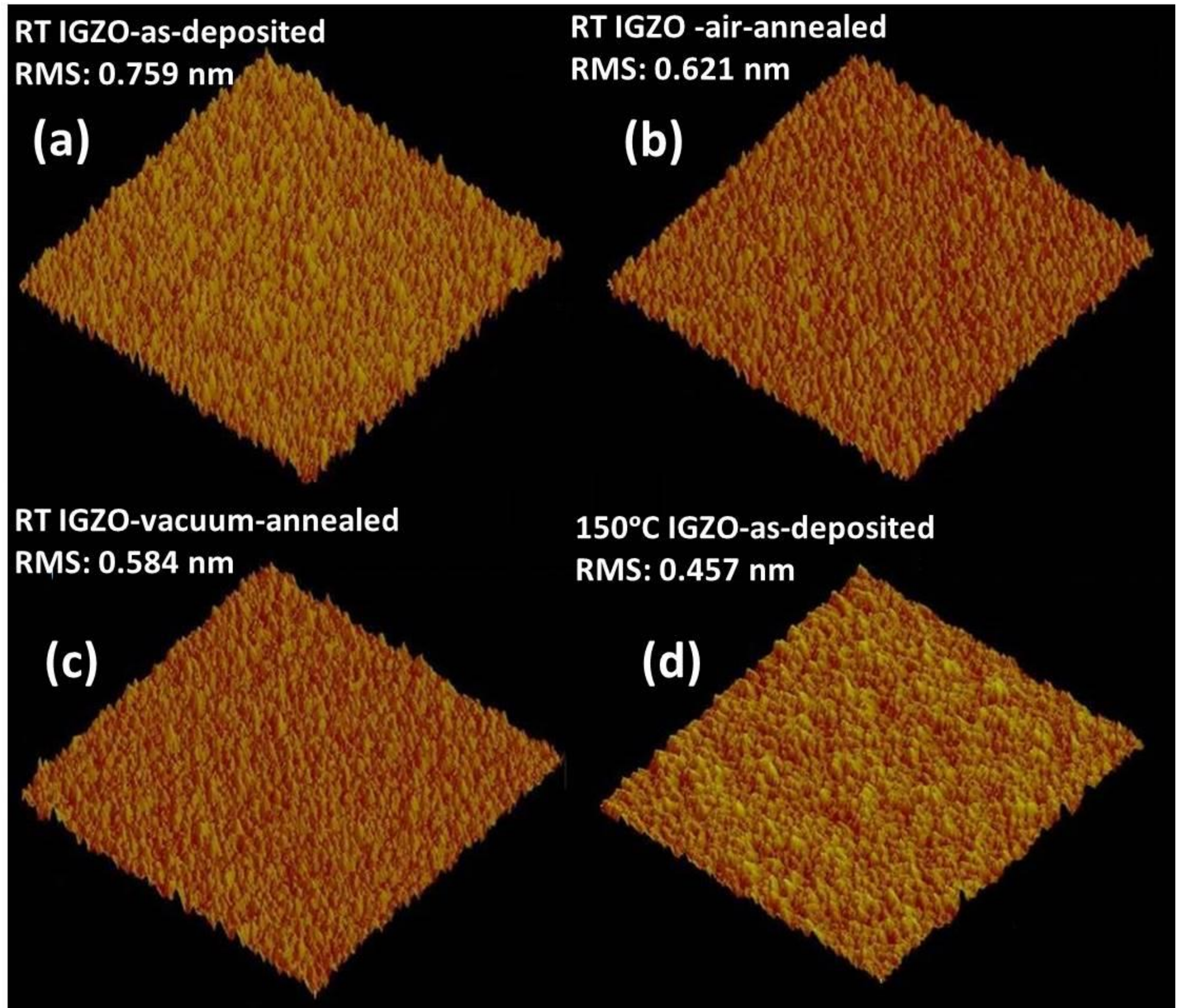

Figure 3-18 AFM images of surface morphology of the (a) as-deposited RT-IGZO, (b) air-annealed RT-IGZO, and (c) vacuum-annealed RT-IGZO, and (d) as-deposited 150°C-IGZO films.

A rougher channel layer surface would indicate a possible rough underlying interface that is the origin of the increased interfacial defect density. The root-mean square (RMS) roughness for the IGZO thin-films deposited at RT and 150˚C were 0.759 nm and 0.457 nm, respectively. In addition, RT IGZO thin-films demonstrated smoother surface after both the air (0.621 nm) and vacuum-annealing (0.584 nm) processes.

According to the AFM topography images of IGZO thin-films, a slightly smoother surface was observed for the films deposited at higher temperature (150°C) and after thermal annealing. Hence, formation of a smoother surface with a smaller number of interface traps may be another factor in the improved I-V characteristics of the IGZO TFTs.

If the I-V characteristics of the IGZO TFTs in Figure 3-13 are compared with those of the ZnO TFTs in Figure 3-8, much better TFT performance with higher μ (8.8 vs. 1.55 cm^2/V.sec), lower V_T (4.2 vs. 11V), and higher $I_{on/off}$ (10^7 vs. 10^6) can be observed for the low-temperature processed IGZO TFTs. These electrical improvements may originate from the different material structures of IGZO and ZnO thin-films. ZnO thin-films form a polycrystalline phase even if they are deposited at room temperature [52, 88]. Hence, grain boundaries work as a barrier layer against carrier transport and can deteriorate the electrical performance and uniformity of the polycrystalline ZnO TFTs [62, 63]. Due to the better electrical properties of amorphous IGZO over the polycrystalline ZnO channel layer, the focus of this Ph.D. dissertation will be on IGZO TFTs in the following chapters.

3.4. Conclusion

This chapter has studied the effect of both channel layer deposition temperature and low-temperature thermal-annealing on the I-V characteristics of ZnO and IGZO TFTs. Both polycrystalline ZnO and amorphous IGZO channel layers demonstrated higher conductivity after thermal-annealing and when they were deposited at higher temperatures. In both low-temperature deposition processes and thermal-annealing, changes to the film crystallinity and interface properties were found to be the dominant factors in different I-V characteristics of ZnO TFTs. On the other hand, changing the chemical composition of the channel layer proved to be responsible for the different I-V characteristics in IGZO TFTs [89].

Chapter 4

4. Electrical dependence on the chemical composition of the gate dielectric in indium gallium zinc oxide thin-film transistors

4.1. Introduction

In the previous chapter, the effects of material structure, surface topography, and chemical composition of channel layer on the electrical performance of crystalline and amorphous MO TFTs were investigated. In addition, in order to study the influence of channel layer property on TFT performance, the effects of gate dielectric surface roughness and hydrogen out-diffusion to the IGZO channel layer were minimized by fabricating MO TFTs on thermally grown SiO_2 with smooth surface and a negligible H concentration. However, thermal SiO_2 dielectric cannot be integrated on the flexible substrates due to its high-temperature process and lack of a Si template for SiO_2 growth, and therefore a low-temperature integration processes are required using conventional PECVD gate dielectric materials.

Several reports have demonstrated that improving the channel layer/gate dielectric interface properties, by decreasing the trap center densities, results in a smaller charge trapping and better TFT performance and electrical stability. Hence, several research groups have studied the effect of different gate dielectric materials and deposition techniques on I-V characteristics of TFTs. Li et *al.* studied the effect of SiO_x interlayer on the performance of a-IGZO-TFTs with AlOx gate dielectric. It was observed that using a SiO_x with interlayer modified AlO_x gate insulator improved TFT performance. This improvement was ascribed to better channel layer/gate dielectric interface properties [90]. Lee et al. published their results, evaluating the threshold voltage instability for various gate dielectrics (SiN_x and SiO_x) in a-IGZO TFTs. It was found that higher hydrogen content in SiN_x led to the more charge trap sites, which would produce a large number of shallow

hydrogen-related states, giving rise to poor TFT performance and higher threshold voltage instability [16]. Lee et *al.* observed a steeper subthreshold slope for IGZO TFTs with Al_2O_3 gate dielectric compared to devices with Al_2O_3/SiN_x gate dielectric layers. This degradation in S.S. has been correlated to the higher density of trap states at the IGZO/SiN_x interface. It was suggested that trapped electrons are located at energetically shallower states or spatially closer to the interface in SiN_x dielectric layers [91]. Plasma-enhanced chemical-vapor deposition (PECVD) of SiO_x gate dielectric layers has been used to fabricate TFTs that are electrically stable and insensitive to light exposure compared to devices having PECVD SiN_x gate dielectric layers. The higher performance is attributed to reduced interface charge trapping within the SiO_x gate dielectric [92] where high hydrogen concentration in the SiN_x gate dielectric layers increases shallow trap states, resulting in increased conductivity of the channel layer.

Although several reports have studied the effect of different gate dielectric materials [16, 91, 92], deposition techniques (ALD [28, 50], PECVD [19], e-beam evaporation [29], solution-based processes [49]), annealing processes [17, 25, 75], and plasma treatments [12, 13, 15, 74] on the I-V characteristics of IGZO TFTs, the effect of the gate dielectric on the chemical composition of IGZO channel layer and the TFT performance has not been well studied. For example, higher In concentrations in IGZO films gives rise to increased field-effect mobility, while increased gallium (Ga) incorporation has been found to reduce the free-carrier concentration and degrade carrier transport properties [4, 65] due to the formation energy of oxygen deficiency [66]. The resulting chemical composition of the IGZO films then determines the formation of oxygen deficiency.

In this chapter, the effect of the gate dielectric on the chemical composition of channel layer is first investigated. Then, by controlling the diffusion of different atomic species in the

semiconductor and dielectric, the conductivity of IGZO channel layer is tuned to fabricate high-performance IGZO TFTs using conventional PECVD gate dielectric at low-temperatures.

4.2. Experiments

Bottom-gate IGZO TFT device structures were fabricated on separate gate-dielectric layers. The TFT fabrication was performed using highly-doped ($\rho \sim 10^{-3}$ ohm.cm) p-type c-Si substrates as the common gate electrode. Three different test structures were fabricated to compare the effect of the dielectric thin-film on the TFT performance. The first test structure (TS1) consisted of a 300 nm SiN_x PECVD thin-film deposited at 150°C. The second and third structures consisted of a PECVD bilayer dielectric with SiO_x(50 nm)/SiN_x(300 nm) deposited at 150°C (TS2) and 260˚C (TS3), respectively. A fourth TFT test structure (TS4) was fabricated on 100 nm thermal SiO_2 on p-type c-Si wafers. The cross-section of the bottom-gate TFT structure is shown in Figure 4-1(a) inset. Following the dielectric deposition, a 50 nm IGZO layer was deposited by RF reactive sputtering (target composition: InGaZnO4, purity: 99.99%) at 150˚C. All IGZO channel layers deposited under the same sputtering conditions (power=100W, pressure: 5mTorr, and Ar:O_2 ratio of 12:1). Individual islands were then patterned to define the active area followed by patterning of the source and drain contacts. A 100 nm thick room temperature (RT) sputtered Mo contact was defined using a standard lift-off process.

4.3. Results and discussion

The transfer characteristics of the IGZO TFTs having structures TS1–TS4 are shown in Figure 4-1(a). The TS1 devices, fabricated on the 150˚C SiN_x layer exhibited no switching behavior and had high conductivity compared to the other IGZO films on PECVD SiO_x and thermal SiO_2. The transfer characteristics of the TFTs were measured in the linear regime with a

source/drain voltage (V_D)=0.1V; and the field-effect mobility (μ) of the fabricated TFTs were extracted using the gradual channel approximation.

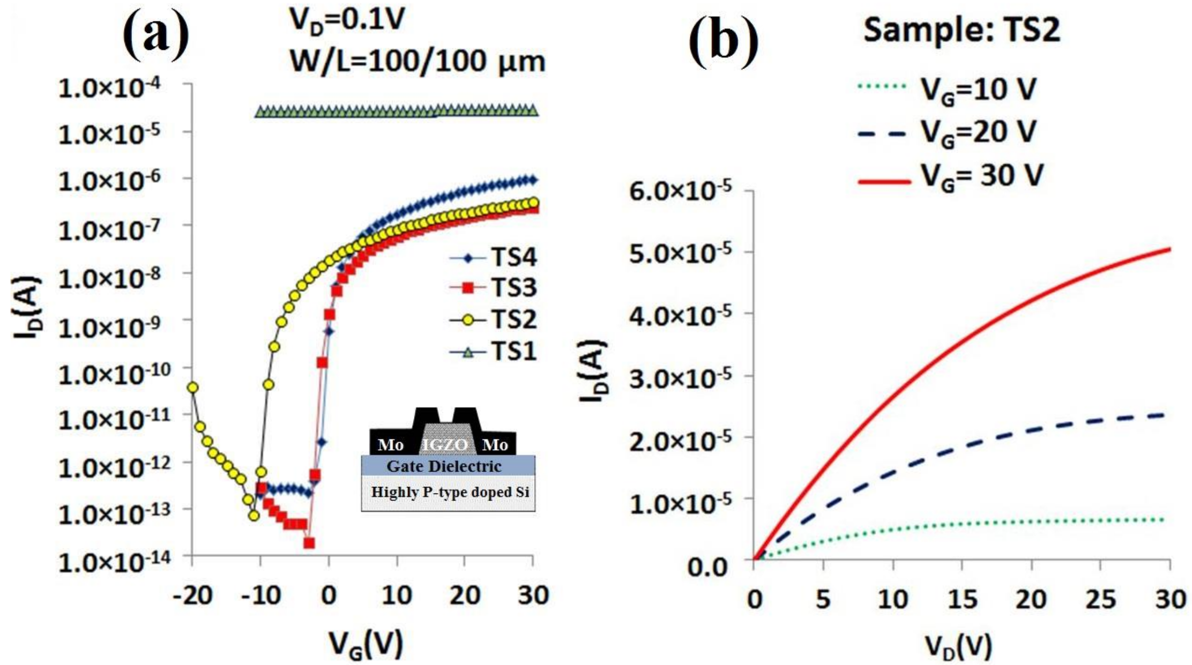

Figure 4-1 Transfer characteristics of IGZO TFTs with different gate dielectrics along with the schematic of IGZO TFT structure (inset), (b) Output characteristics of IGZO TFTs with 150˚C PECVD SiO_x/SiN_x gate dielectrics (TS2).

The low-temperature-processed dual-dielectric TFTs (TS2) had a μ=5.7 cm^2/V.sec, V_T=-0.5 V, and a sub-threshold swing (S.S.) of 0.54 V/decade. Devices from TS3, having the same device stack as TS2 but processed at 260˚C, resulted in a V_T=3.8 V and a μ=6.3 cm^2/V.sec. In comparison, devices fabricated on thermal SiO_2 (TS4) showed slightly improved I-V characteristics compared to TS3, with μ=8.8 cm^2/V.sec, V_T=4.2 V, and S.S.=0.42 V/decade (Table 4-1). Structures TS2–TS4 had similar on/off ratios of approximately 10^6. The higher current of the TS4 device is due to the higher gate-dielectric capacitance compared to the TFTs with the bilayer dielectric (TS2&3), where $C_{Thermal\ SiO2}$ ~30 nF/cm^2 and $C_{PECVD\ bilayer\ dielectric}$~16 nF/$cm^2$. The higher specific capacitance results in a larger field acting in the channel, which results in a higher current. The output

characteristics showed linear behavior at low V_D, indicating good ohmic contacts independent of the dielectric layer (Figure 4-1(b)).

Table 4-1 TFT I-V performance characteristics and XPS results.

Structure	**Gate dielectric**	**μ (cm²/V.sec)**	**V_T (V)**	**S.S. (V/decade)**	**O_M (%)**	**Dielectric Capacitance (nF/cm²)**
TS1	150ºC SiN_x	---	---	---	29.84	~18
TS2	150ºC SiO_x/SiN_x	5.7	-0.5	0.54	26.00	~16
TS3	260ºC SiO_x/SiN_x	6.3	3.8	0.42	23.72	~16
TS4	Thermal SiO_2	8.8	4.2	0.42	23.06	~30

The roughness of the channel layer may indicate the introduction of interfacial defects at the semiconductor/dielectric interface resulting in poor TFT characteristics as studied in the previous chapter. The AFM scans of the IGZO surface morphology on different gate dielectric layers are shown in Figure 4-2. The root-mean square (RMS) roughness, which could be a function of the underlying gate dielectric's surface roughness, for the IGZO thin-films on TS1, was ~0.72 nm, whereas TS2, TS3, and TS4 were measured to be 1.54 nm, 1.71 nm, and 0.46 nm, respectively. The AFM measurements do not show a clear correlation to the TFT performance and the surface roughness of the channel layer, suggesting the dielectric/semiconductor interface is not dominating the TFT performance. The elevated conductivity may also be due to IGZO films with high concentration of oxygen deficiency[21, 81, 93]. Our previous results (Figure 3-4,3-11, and 3-16) in Chapter 3 showed that, after surface contamination cleaning with mild ion etching, the

concentration of oxygen deficiencies on the surface and in the bulk is very similar in IGZO and ZnO thin-films. Thus, in this section, after surface contamination cleaning with mild ion etching, the chemical composition of the IGZO thin-films was analyzed by XPS to compare the trend of oxygen deficiency concentration in IGZO channel layers deposited on the different dielectric layers.

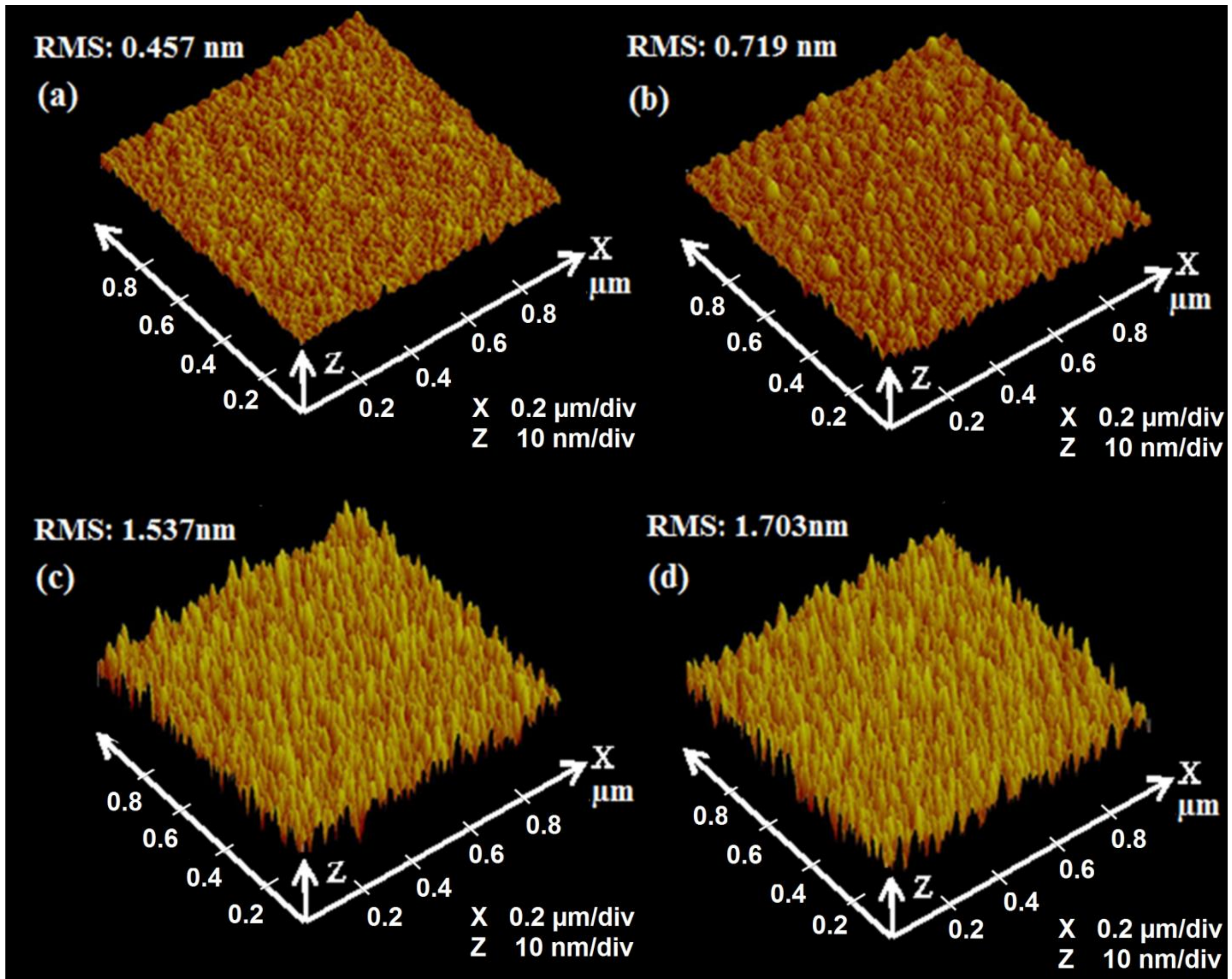

Figure 4-2 AFM images of surface morphology of the IGZO films deposited onto the different gate dielectrics of (a) Thermal SiO_2, (b) 150˚C PECVD SiN_x, (c) 260˚C PECVD SiO_x/SiN_x, and (d) 150˚C PECVD SiO_x/SiN_x.

The peak binding energies of In $3d_{5/2}$, Ga $2p_{3/2}$, and Zn $2p_{3/2}$ showed a positive shift toward higher binding energy compared to those of the In-In (443.8 eV), Ga-Ga (1117.4 eV), and Zn-Zn bonds (1021.5 eV), suggesting that the In-O, Ga-O, and Zn-O bonds are dominant in the IGZO

films, regardless of the underlying gate dielectric [80]. The O 1s spectra for the IGZO films deposited onto the different gate dielectrics are fitted into three peaks, centered at 530.7 eV (O_L peak), 531.5 eV (O_M peak), and 532.5 eV (O_H peak) using a Gaussian profile (Figure 4-3).

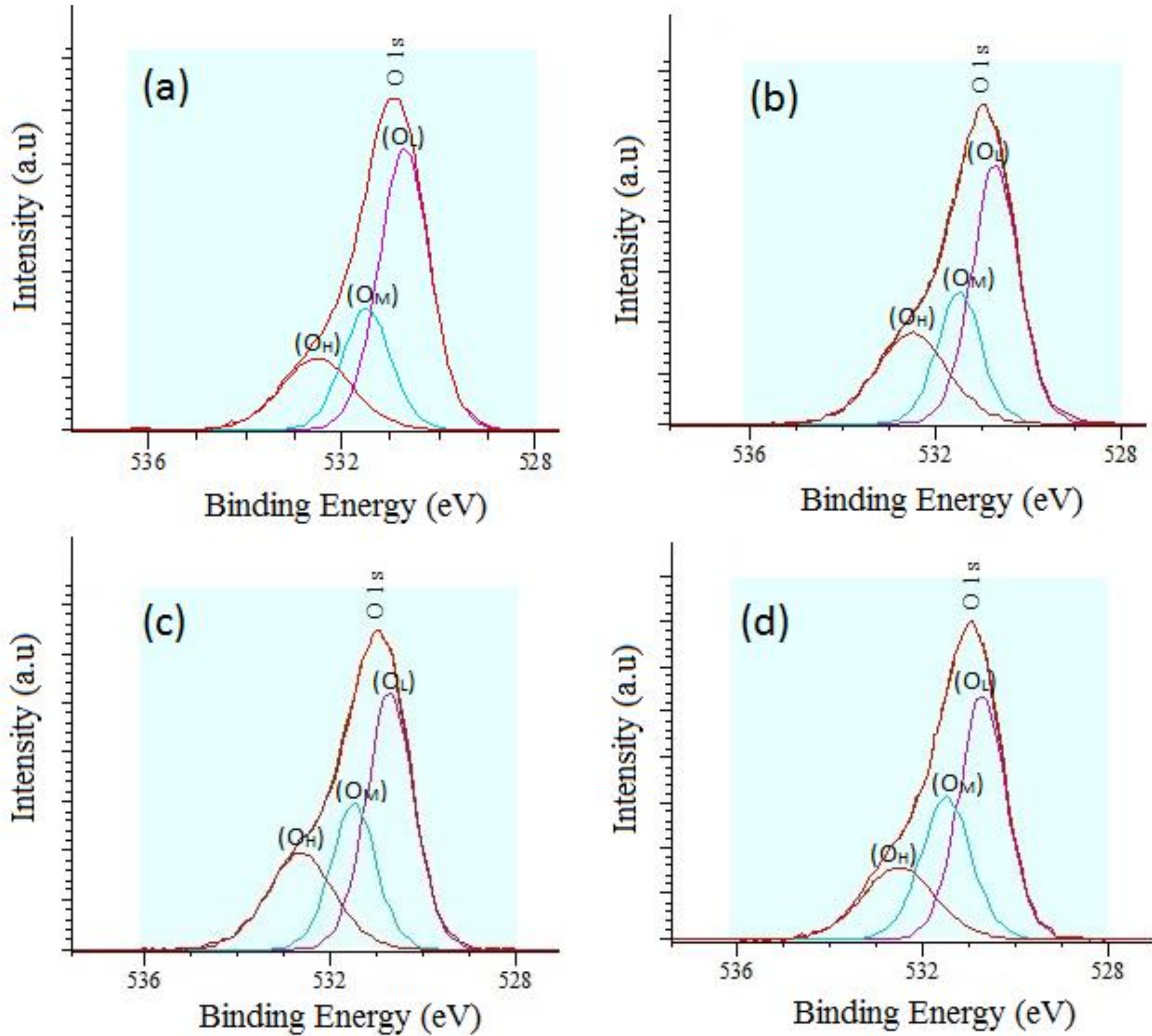

Figure 4-3 O 1s XPS spectra of IGZO films deposited onto the different gate dielectrics: (a) Thermal SiO_2, (b) 260˚C PECVD SiO_x/SiN_x, (c) 150˚C PECVD SiO_x/SiN_x, and (d) 150˚C SiN_x, after surface contamination cleaning.

The O_M, correlating to the V_o in the IGZO film, had measured values of 23.06, 23.72, 26.00, and 29.84 for TS4, TS3, TS2, and TS1, respectively. The increasing oxygen deficiency

concentration in the IGZO films was dependent on the underlying dielectric material, with TS1 having the highest oxygen deficiency concentration (22% higher than IGZO on SiO_2) and highest conductivity of the test devices studied. A similar transformation from semiconducting to metallic-like conductivity due to increasing oxygen deficiency concentration (also measured by XPS) has been reported after thermal annealing of IGZO films in a nitrogen ambience [21]. The TFT I-V performance characteristics and XPS results are summarised in Table 4-1.

The IGZO photoluminescence (PL) spectra of TS4 and TS1 are shown in Figure 4-4. A broad green defect-related emission was observed for TS1 and was more than 100× greater than that of TS4, with a 14% broadening of the full-width at half maximum (FWHM). Although the main cause of this broad green emission peak is not fully understood yet and there are several different opinions and reports [94-96] on this peak, the origin of this peak might be due to the formation of higher fully occupied deep oxygen deficiencies and this explanation best describes the findings of this Ph.D. study.

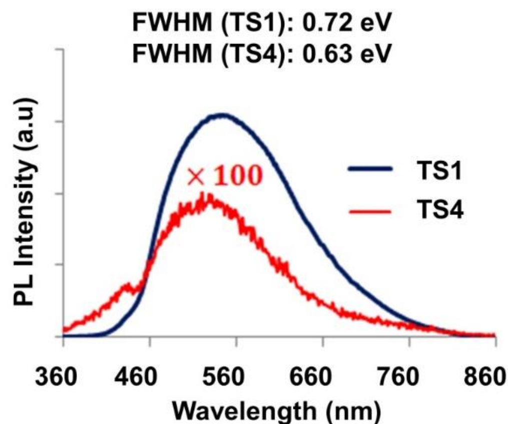

Figure 4-4 Photoluminescence emission spectra for the IGZO films deposited onto the different gate dielectrics: thermal SiO2 (TS4) and 150˚C PECVD SiNx(TS1).

One explanation for the increased oxygen deficiency concentration may be due to hydrogen-related V_o formation [73], which has been identified to generate free electron carriers in IGZO. Hydrogen diffusion into IGZO channel layers may increase the conductivity of the IGZO channel [11]. For the devices fabricated in this study, the source of hydrogen contamination in the IGZO may be from the underlying gate dielectric. The devices fabricated on thermal oxide (TS4) have the lowest hydrogen concentration and the highest IGZO resistivity, with better TFT device performance, suggesting that the absence of hydrogen diffusion into the active channel region affects TFT performance.

The IGZO directly deposited onto the nitride gate dielectric (TS1) had the highest concentration of oxygen deficiency, where the high hydrogen concentration in the underlying film diffuses into the channel layer during the IGZO deposition, resulting in the higher channel conductivity.

To further investigate this hypothesis, the dual-dielectric TFTs (TS2 and TS3) were deposited with a SiO_x diffusion barrier having much lower hydrogen content compared to the nitride layers. The SiH_4 flow during the SiO_x deposition was more than 3× less compared to the SiN_x deposition. To further minimize the hydrogen content, SiH_4-N_2O gases were used for the PECVD oxide compared to SiH_4-NH_3 for the nitride deposition. The IGZO layers on the dual-dielectric stacks had higher resistivity compared to the nitride only layers. Additionally, by considering the deposition temperature, a higher concentration of oxygen deficiency in the IGZO was found on the 150ºC PECVD SiO_x/SiN_x (TS2) compared to the 260ºC PECVD SiO_x/SiN_x (TS3) gate dielectric, correlating to the expected lower hydrogen concentration in the films deposited at higher temperature [91]. This effect may explain the success of other groups [97] who implemented SiN_x gate dielectrics for IGZO TFTs using a high process temperature to limit

hydrogen diffusion into the IGZO channel layer. The electrical stability of the dual-dielectric devices was also comparable to devices on thermal oxide.

However, to fabricate IGZO TFTs on flexible substrates, the fabrication process needs to be done at low deposition temperature (≤ 150˚C). As seen in Figure 4-1, IGZO films deposited on 150°C PECVD SiN_x showed highly conductive properties and exhibited always on-state behavior regardless of the applied voltage. This high conductivity is correlated to the out-diffusion of H atoms from layer underneath and formation of oxygen deficiency in the channel layer. However, in the previous chapter (3.3.2), it was observed that room temperature deposition results in the formation of lower oxygen deficiency concentration in the IGZO thin-films and, in turn, higher resistivity. Hence, in order to tune the conductivity of the IGZO thin-films, the channel layer deposition temperature was decreased. The resulting low-temperature processed TFTs demonstrated very poor I-V characteristics, with a low I_{on} and a high V_T, suggesting formation of lower carrier concentration in IGZO channel layers, thereby resulting in a poor TFT performance [4], Figure 4-5. According to our previous findings in Chapter 3, in order to increase the carrier concentration in the channel layer, pre-fabricated TFTs were annealed in both air and vacuum environments at 150°C for 1 hour. The TFT channel layer became highly conductive after a 1 hour vacuum anneal. However, suitable I-V characteristics were obtained after thermal annealing in air, suggesting appropriate channel conductivity. These results correlate well to our previous findings, where it was found that vacuum annealing, by formation of higher oxygen deficiency concentration in IGZO channel layers, results in higher conductivity. In addition, the annealing process may also result in out-diffusion of H atoms from the PECVD gate dielectric layers to the IGZO channel layer, both of which could result in higher carrier concentration in air-annealed devices and a higher mobility, probably due to the reduction of the conduction band offset [4, 17,

75]. After air annealing, room-temperature deposited IGZO TFTs demonstrated improved TFT I-V characteristics with a μ=5.47 cm^2/V.sec, V_T=3.1 V, and S.S.=0.43 V/decade.

These results suggest that by combining and controlling the effects of chemical composition, channel layer deposition temperature, and thermal annealing, fabrication of low-temperature-processed high-performance IGZO TFTs using conventional PECVD gate dielectrics are possible.

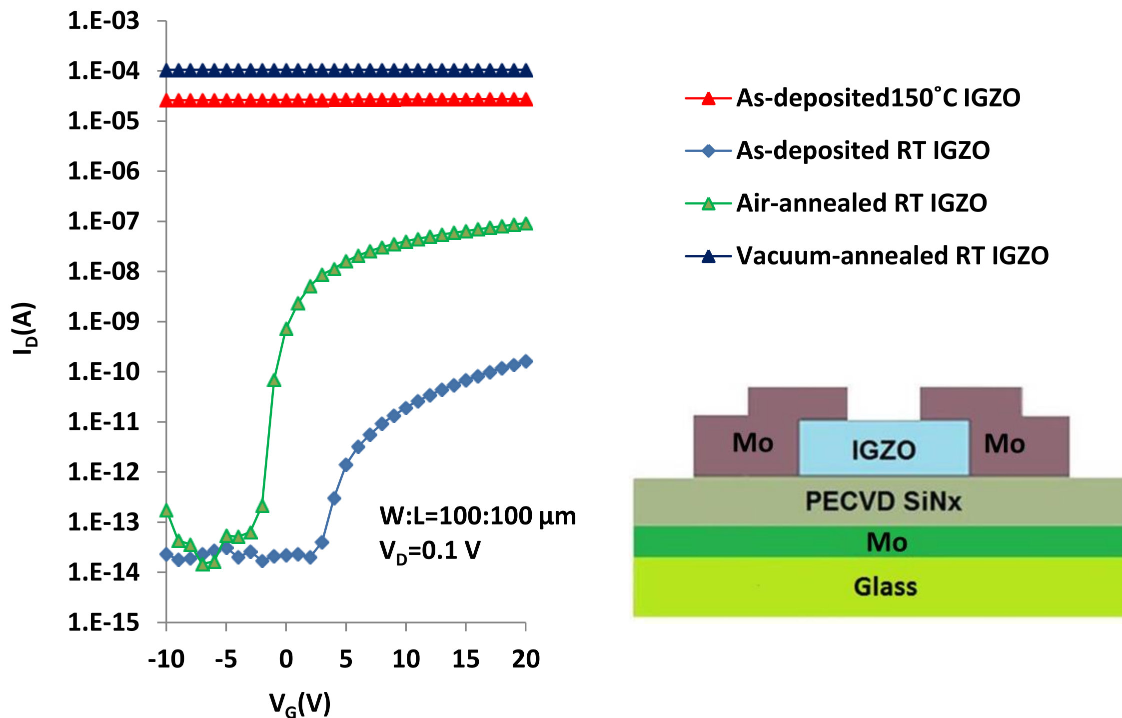

Figure 4-5 Transfer characteristics of the low-temperature processed IGZO TFTs using conventional PECVD gate dielectrics. (inset) The cross-section of the fabricated IGZO TFTs with a bottom gate structure.

4.4. Conclusions

It was found that a bi-layer dual gate SiO_x/SiN_x IGZO TFT structure was more effective for fabricating high-performance IGZO-based TFTs than fabricating directly onto SiN_x dielectric layers [98]. The observed improvement in the IGZO films and the measured improvement in the electrical characteristics were due to minimization of oxygen deficiency formation due to hydrogen diffusion into the overlying semiconducting IGZO layer. The SiO_x capping layer was

also found to be an effective hydrogen diffusion barrier between the silicon nitride and IGZO channel, demonstrating the efficacy of using the bi-layer PECVD-grown dielectric structures to improve the performance of the transition metal oxide (TMO) TFT devices [99]. In the end, by controlling the combined effects of the channel layer deposition temperature and post-thermal annealing with the chemical composition of the gate dielectrics, the conductivity of the channel layer was tuned, to produce a high-performance, low-temperature processed working TFT, using conventional PECVD gate dielectrics.

Chapter 5

5. Controlled conductivity of sputtered IGZO for low-temperature transparent thin-film transistors

5.1. Introduction

Chapter 4 demonstrated the feasibility of fabricating high-performance IGZO TFTs using conventional PECVD gate dielectrics and opaque Mo source/drain (s/d) contacts. However, in order to fabricate transparent flexible electronics, developing low-temperature transparent contacts is critical. Several oxide-based alloys such as an indium tin oxide (ITO) [100], amorphous indium zinc oxide (a-IZO) [101, 102], and amorphous gallium zinc oxide (GZO) [103] have already been considered as transparent electrodes for IGZO TFTs.

By applying sputtered IGZO as the s/d electrodes, both channel-layer and contact electrodes can be sputtered using the same target, resulting in a relatively simpler TFT fabrication process and possibly better interface properties between channel layer and s/d electrodes.

Recently, a few research groups have tried to implement IGZO as s/d electrodes to fabricate optically transparent IGZO TFTs. However, the majority of these studies have used high-temperature process such as 250°C nitrogen annealing [104], 300°C oxygen annealing [102], and 400°C rapid thermal annealing [105, 106], none of which are compatible with plastic substrates. Ar and H_2 plasma treatments [12] and P-doping [107] of s/d regions have also been reported by other research groups. However, the plasma treatment and doping processes of s/d regions usually need relatively complicated facilities and are not suitable for large-area fabrication.

Given the range of the electrical conductivity of IGZO thin-films, the IGZO conductivity was tuned to deposit both the channel layer and contact electrodes using the same sputter target, thereby enabling simplified device fabrication and potentially allowing for improved interface quality

between the channel layer and the source/drain contact electrodes. Transmission line method (TLM) results were presented for the contact resistance. In addition, the electrical instability and recovery behavior of the fabricated TFTs were investigated using long-term dc gate bias stress and pulsed-gate measurments.

5.2. Experimental

Bottom-gate IGZO TFT device structures were fabricated on glass substrates. An 80 nm IGZO layer was sputtered at 150°C as the transparent gate electrode (power=100W, pressure: 2mTorr, and Ar:O_2 ratio of 12:0), which was followed by a thin-layer of transparent Mo as a wet-etch protective layer. A plasma-enhanced chemical-vapor deposition (PECVD) bilayer dielectric with SiO_x(50 nm)/SiN_x(300 nm) was deposited at 260°C over the gate electrode followed by a 50 nm thick RF reactive sputtered IGZO channel layer (power=100W, pressure: 5mTorr, and Ar:O_2 ratio of 12:1) deposited at 150°C. Individual islands were then patterned by wet etching to define the active area using a dilute HCl solution. Finally, a 200 nm thick RT sputtered IGZO contact (power=100W, pressure: 2mTorr, and Ar:O_2 ratio of 12:0), covered by a thin layer of transparent Mo, was defined using a standard lift-off process. A variety of TFT geometries were fabricated; this study focused on devices with a channel width (W) to length (L) ratio of 1 (W/L=100 µm/100 µm).

5.3. Results and discussion

Chapter 3 demonstrated that the deposition temperature of IGZO channel layers and the annealing environment can significantly change the I-V characteristics of IGZO TFTs from an always Off-state behavior to an always ON-state behavior. These findings were correlated to the different concentrations of oxygen deficiency in the IGZO channel layers that was responsible for the variation in the channel layer conductivity. Thus, in order to develop an IGZO recipe for

transparent ohmic contacts, the effect of oxygen ratio on the electrical resistivity/conductivity of deposited films was examined. The resistivity of the deposited films was measured using four-point probe measurements in air ambient and under dark conditions.

Figure 5-1(a) shows that the resistivity decreases with a decreasing O_2 ratio, due likely to the formation of a higher oxygen deficiency concentration in these films. A well-known doping mechanism in IGZO thin-films is the formation of oxygen deficiency [108], which generates free electrons in the conduction band, resulting in a decrease in the resistivity of IGZO thin-films.

After the determining the appropriate oxygen flow rate for the required IGZO conductivity, the effects of sputter power, pressure, and deposition temperature on the conductivity of IGZO thin-films was investigated at a fixed oxygen ratio of zero. Figure 5-1(b) shows that increasing the deposition pressure results in a smaller conductivity, probably due to the kinetic energy of the sputtering species, which determines the adatom mobility for thin-film growth [109]. More sputtered species are collided when the sputtering gas is under increased pressure. As a consequence, the adatoms have only limited energy for surface diffusion. Hence, it can be suggested that with increasing the deposition pressure, the energy of sputtered species decreases, resulting in a porous material with more defects and lower conductivity. Several process conditions were explored to test this approach to controlling the film conductivity.

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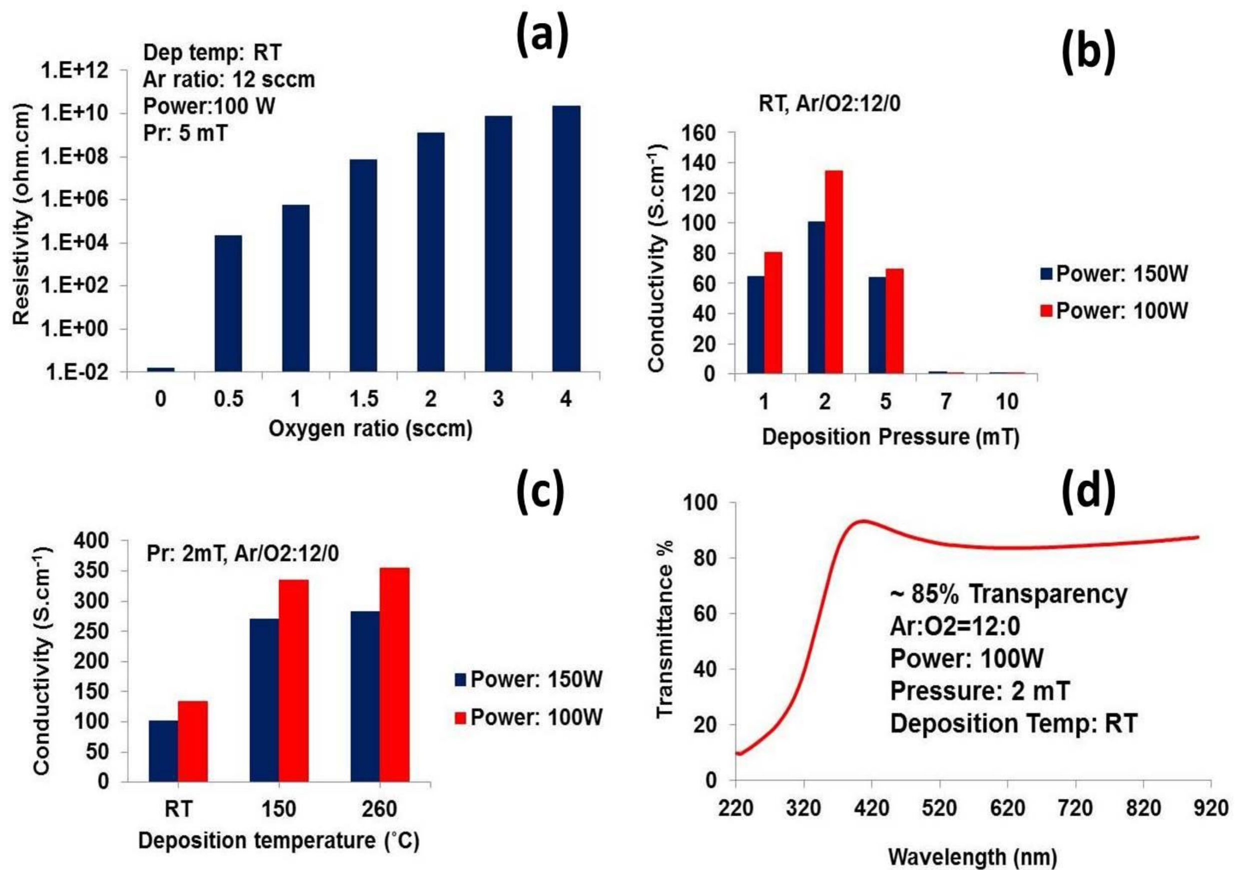

Figure 5-1 The effects of (a) oxygen ratio, (b) deposition pressure, and (c) deposition temperature on the electrical properties of IGZO thin-films. (d) The optical transmittance of the highly-conductive IGZO thin-film deposited using the optimum recipe at RT.

It was also found that at the same deposition pressure (2mT) and room-temperature, the film deposited at lower sputtering power (50 W) resulted in much lower conductivity (44 $S.cm^{-1}$) compared to IGZO films deposited at 100 W (134 $S.cm^{-1}$) and 150 W (101 $S.cm^{-1}$), respectively. These results may originate with the low energy system of sputtered species (ionized particles) at low deposition power, which, in turn, results in the formation of more defects and lower conductivity. On the other hand, higher deposition power leads to ionized particles with higher energy, which promotes the diffusion of sputtered species on the surface and leads to the formation of a better film quality with improved transport properties. However, increasing the power from

100W to 150W slightly decreases the conductivity of the IGZO thin-films, which might be correlated to the anti-sputtering phenomenon [110] and formation of a rougher surface. This effect was verified with AFM characterization, which showed the surface roughness of high-power and low-power deposited film as RMS=0.934 nm and. 0.621 nm, respectively. Figure 5-1(c) shows the effect of deposition temperature on the conductivity of IGZO thin-films. As can be seen, higher deposition temperature results in higher conductivity, suggesting the formation of higher oxygen deficiency concentration in the channel layer. IGZO thin-films deposited at the optimum deposition power (100 W) and deposition pressure (2 mT) demonstrated conductivities of 134, 335, and 355 $S.cm^{-1}$ at room temperature, 150°C, and 260°C, respectively.

The metal ratio of the bulk material for the highly conductive and semiconducting IGZO was also analyzed quantitatively by survey analysis of XPS data using the CasaXPS software. The findings of this measurement revealed an obvious change in the In:Ga atomic ratio of these two films, where In:Ga ratio of 1.87 and 1.16 were obtained for the 150°C highly conductive IGZO (power:100W, Pr: 2mT, $Ar:O_2$=12:0) and the semiconductor IGZO (power:100W, Pr: 5mT, $Ar:O_2$=12:1), respectively. The higher In:Ga ratio in the highly conductive IGZO film further describes the origin of the huge variation in the bulk electrical properties ($\rho=4.2\times10^{-3}$ vs. $\rho=3.4\times10^{4}$ ohm.cm) in these two films. Higher In content in the conductive films leads to a higher carrier concentration and higher mobility, which is directly related to the IGZO structure. In contrast, gallium (Ga) incorporation results in a lower free carrier concentration and mobility. These results have been explained due to the difference in the formation energy of oxygen deficiency [66]. Ga-Ga bonds in IGZO structure are much stronger than Ga-M, and M-M bonds around the V_o defects, where M=In and Zn. So, V_o will be generated more easily at the oxygen site surrounded by In atoms. In contrast, formation of V_o around Ga atoms needs much higher energy [66].

UV-Vis spectrometry measurements data showed a greater than 85% transparency in the visible regime for the IGZO thin-film deposited using the optimum recipe at room temperature, Figure 5-1(d).

To investigate the feasibility of fabricating IGZO TFTs with IGZO electrodes, optically transparent IGZO TFTs were fabricated using the optimized highly conductive transparent IGZO contact process obtained earlier. The I-V transfer characteristics of the transparent devices were measured in the linear regime (Figure 5-2(a)) with a source/drain voltage (V_D) of 0.1V. The field-effect mobility (μ) of the fabricated TFTs was extracted using the gradual channel approximation. Optically transparent TFTs exhibited a μ of ~9.4 cm^2/V.sec, V_T of ~3 V, S.S. of 0.42 V/decade, and $I_{on/off}$ ratio of > 10^6. The fabricated TFTs also demonstrated ohmic behavior at low V_D (Figure 5-2(b)).

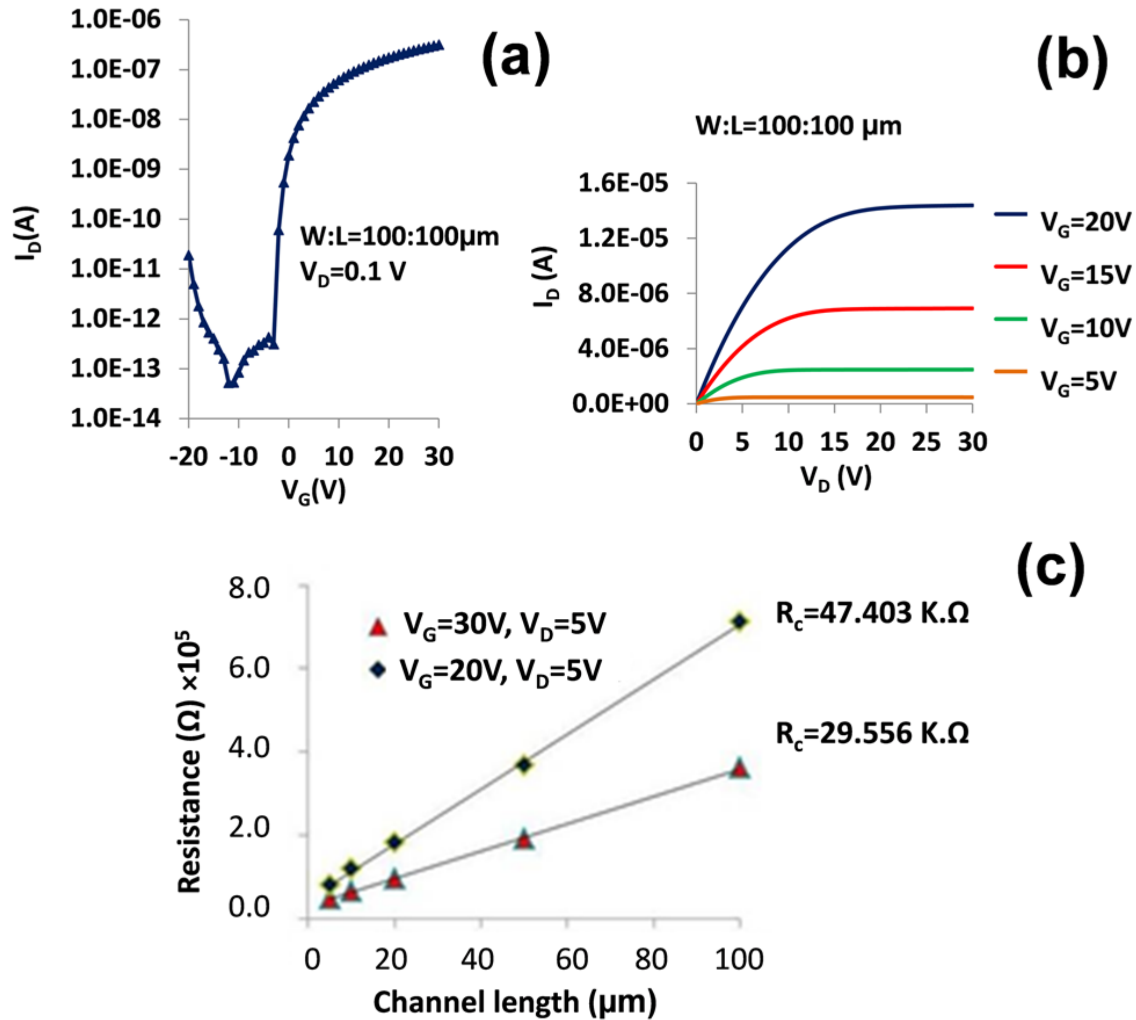

Figure 5-2 Transfer (a) and output (b) characteristics of the lift-off processed transparent IGZO TFTs. (c) Contact resistance of the fabricated TFTs extracted using the transmission line model.

Transmission line measurement was used to determine the contact resistance of the IGZO electrode. The I-V output characteristics of several TFTs with the same channel width (100 µm) and different channel lengths, ranging from 5 to 100 µm were measured. The total resistance of the fabricated TFTs was determined from the slope of the linear regime of the I_D-V_D curves at two different gate voltages (20 V, 30 V) at a drain voltage (V_D) of 5 V. The total resistance (R_T) is a function of the contact resistances of the two contacts and the sheet resistance of the channel shown in Eq. 5.1.

$$R_T=2R_c+\frac{Rs}{W}d \qquad (5.1)$$

where R_C is the contact resistance between channel and source/drain electrodes, R_S is the sheet resistance of the semiconducting layer outside the contact, d is the separation of the electrodes, and W is the electrode width fixed at 100 µm in this study.

From Figure 5-2(c), R_c was found to be dependent on the gate voltage (V_G). Contact resistance decreased from ~47 KΩ to 29 KΩ, by increasing V_G from 20 V to 30 V, respectively. The results are due to increasing carrier concentration in the IGZO channel layer as V_G increases [111, 112]. For V_G=30 V, the width normalized R_CW was found to be in the range of 0.29 kΩ.cm (channel width is 100 µm). This value is comparable with common contact resistance values reported for lift-off patterned Ti/Au (0.10 kΩ.cm) and Ti (0.05 kΩ.cm) [101] shadow mask patterned ITO (0.10 kΩ.cm) [113], and is much better than the findings of other groups which have reported width normalized values of 2 kΩ.cm and 3 kΩ.cm for the shadow mask patterned [113] and lift-of patterned [114] Al contacts, respectively.

An electrical instability in the drain current (I_D) of the TFTs was measured while applying a constant bias overdrive voltage ($V_{OV}=V_G-V_{T0}$) of 10V with V_D of 0.1V under dark conditions in air. After a stress time of 3.6×10^3 s, the bias was removed and the recovery of I_D was measured using a pulsed gate signal (pulse width ~25 ms) and gradually lengthening the rest intervals from 10^{-1}s to 10^2 s (with $V_{G(on)}=V_{OV(on)}$, $V_{G(off)}$=0 V, and V_D=0.1 V).

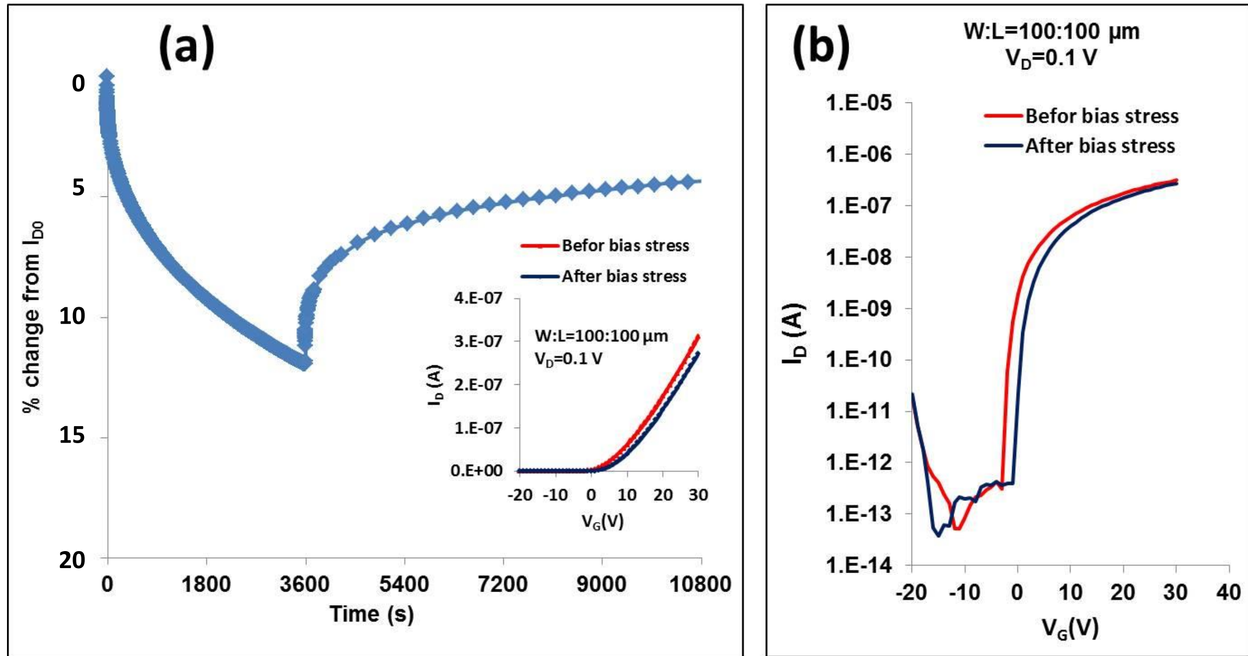

Figure 5-3 Degradation in I_D with bias stress (V_{ov}=10 V and V_D=0.1 V) with TFT transfer curves before and after bias stress in linear (inset) and log(b) scales.

Following the removal of the dc gate-bias, a rapid increase of I_D was measured during pulsed-gate recovery measurements as shown in Figure 5-3(a). This degradation and fast recovery is likely due to shallow interface trap states. The percentage of released charge after 2 hours of recovery time at room temperature was > 75%, which suggests that the dominant aging mechanism is charge trapping. The inset of Figure 5-3(a) shows the V_T shift of ~2 V. The slope of the transfer curves did not show a measurable change in the field-effect mobility. The sub-threshold swing was also found to remain the same before and after the bias stress, which further confirms the previous suggestion regarding the charge trapping bias instability mechanisms (Figure 5-3(b)).

5.4. Conclusions

By tuning the sputtering parameters such as the deposition power, deposition pressure, Ar/O_2 ratio, and deposition temperature, optically transparent high performance IGZO TFTs were fabricated using IGZO thin-films as channel layer and contact electrodes [115]. The transparent TFTs

exhibited a μ of ~9.4 cm^2/V.sec, V_T of ~3 V, a S.S. of 0.42 V/decade, and an $I_{on/off}$ ratio of > 10^6. No current crowding behavior was observed for the TFTs under the low drain-source voltage (V_D) regime. Transmission line method (TLM) results were also presented for the contact resistance. Electrical instability measurements of the TFTs exhibited a V_T shift of ~2 V after 3600 s of dc gate bias (V_{ov}=10 V and V_D=0.1 V). Pulsed-gate recovery measurements also demonstrated rapid recovery of the drain current, suggesting that the dominant aging mechanism is charge trapping.

Chapter 6

6. Selective wet-etch processing of optically transparent flexible IGZO TFTs

6.1. Introduction

The feasibility of fabricating optically transparent IGZO TFTs using low-temperature PECVD gate dielectrics, IGZO source/drain (s/d) contacts, and lift-off process was demonstrated in the previous chapter.

However, a lift-off process is not the ideal patterning candidate in conventional microfabrication processes due to disadvantages such as resettling of unwanted particles on the substrate surface and difficulties in dissolving the negative resist during lift off.

But, due to the lack of etch selectivity between transparent conductive oxides and semiconductors, the top-contact patterning is typically accomplished through lift-off or shadow mask processes [26, 101, 113, 116] instead of conventional dry etching, due to the high sensitivity of the IGZO TFT back-channel layer to plasma damage [9, 117, 118]. Wet-etch patterning approaches have recently been developed with Ta [119] and Ag [120] but these materials are typically opaque and hinder the transparent properties of the oxide semiconductor devices. The effect of grain boundaries on the wet-etch selectivity of transition metal oxides has been shown in previous reports [121] while very few studies have used this effect for the fabrication of flexible IGZO TFTs. In this chapter, a high-selectivity wet-etch patterning process that takes advantage of the etch-rate differences between polycrystalline and amorphous transition metal oxide (TMO) thin-films is described to fabricate back-channel etched flexible transparent IGZO TFT structures. The wet-etch process enables an alternative process integration approach that greatly reduces the complexity of

patterning large-area TMO TFTs and allows the direct integration of fully transparent flexible TMO TFTs onto plastic platforms.

6.2. Experimental

Bottom-gate IGZO TFT device structures were fabricated on flexible polyethylene naphthalate (PEN) (thickness of 125 μm) and glass substrates. An 80 nm aluminum-doped zinc oxide (AZO) layer was sputtered at 150°C and patterned using dilute HCl to define the bottom-gate electrode. A 300 nm SiN_x PECVD gate dielectric ($C_{PECVD\ SiNx}$~18 nF/cm^2) was then deposited at 150°C over the gate electrode followed by a 50 nm thick RF reactive sputtered IGZO (power=100W, pressure: 5mTorr, and $Ar:O_2$ ratio of 12:1) channel layer deposited at room temperature. Individual islands were then patterned by wet etching to define the active area using a dilute HCl solution. A 200 nm 150°C thick sputtered (power=80W, pressure: 2mTorr, and $Ar:O_2$ ratio of 15:0) AZO film, with a resistivity of 3×10^{-3} Ω.cm, was deposited as the top contact layer, followed by photolithography of the AZO source/drain contacts, and lastly a dilute HCl wet etch. A thermal annealing was performed at 150°C in air and under atmospheric pressure for 1 hour to complete the TFT fabrication.

6.3. Results and discussion

Figure 6-1(a) shows the etch rate of IGZO and AZO as a function of HCl concentration in water. At high HCl concentrations, the etch rate of the AZO was found to be much more dependent on the HCl concentration than the IGZO, providing an etch selectivity between AZO to IGZO of nearly 20, Figure 6-1(b). The selectivity of the etchant is based on the polycrystalline nature of the AZO compared to the amorphous IGZO film. The grain boundaries of the polycrystalline AZO enhances the diffusion of the etchant into the AZO layer, providing the HCl solution with additional interfaces whereby the etchant can penetrate the film [121]. Figures 6-1(c,d) are atomic

force microscopy scans of the surface morphology of two different AZO films. Figure 6-1(c) shows a film, deposited at 150°C, consisting of ~127 nm long grains; the etch rate of this film structure was~700 nm/min. Figure 6-1(d) shows a film deposited at 85°C with smaller grains (~73 nm in length) that had an etch rate of ~1200 nm/min using an etch solution containing 0.3% HCl. The measured etch rates correlate well with the grain size of the AZO film where the smaller grain films having the faster etch rates.

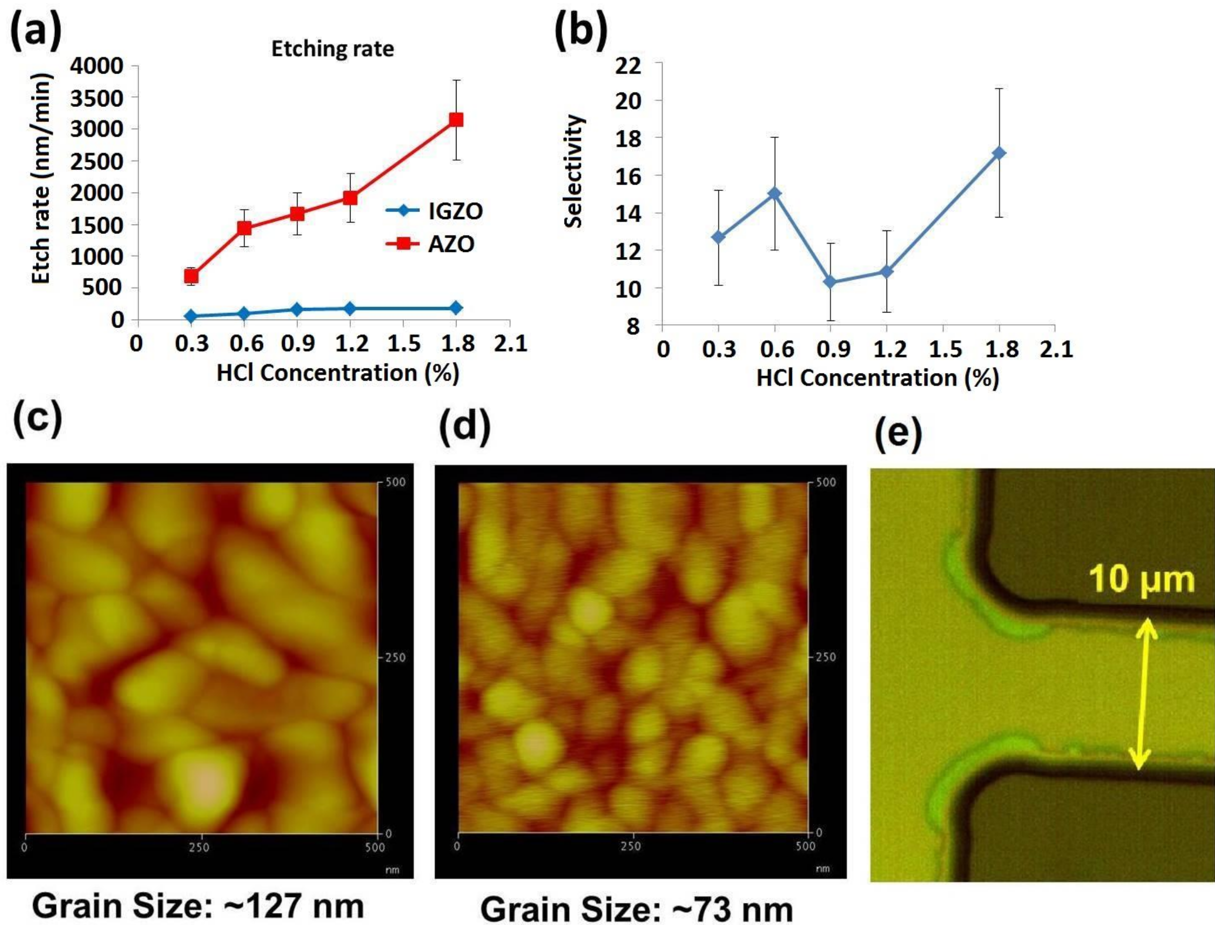

Figure 6-1 Comparison between polycrystalline AZO and amorphous IGZO in terms of (a) etching rate, and (b) selectivity. ((c) and (d)) AFM characterization of AZO thin-films with two different grain sizes; the smaller grain films have faster etch rates. (e) Optical micrographs of a patterned AZO structure after showing the lateral etching of the AZO underneath a patterned photoresist layer at 70% over-etching process in 0.3% HCl solution.

The optical micrograph of a patterned structure after a 15% timed over etch of the AZO, underneath a patterned photoresist etch mask, showed very little or no lateral undercutting of the AZO from the overlying mask layer. It is only after a 70% timed over etch when an observable (~1.3 µm) lateral undercut is observed, Figure 6-1(e).

Figure 6-2(a) shows the electrical characteristics of the AZO contact on IGZO channel layers. From transmission line measurements, contact resistance (R_c) was found to be dependent on the gate voltage, V_G. Contact resistance decreased from ~35 KΩ to 23 KΩ, and to 19 KΩ, by increasing V_G from 20 V to 30 V, and 40 V, respectively. The results are due to increasing carrier concentration due to accumulation of charge in the IGZO channel layer as V_G increases [111, 112].

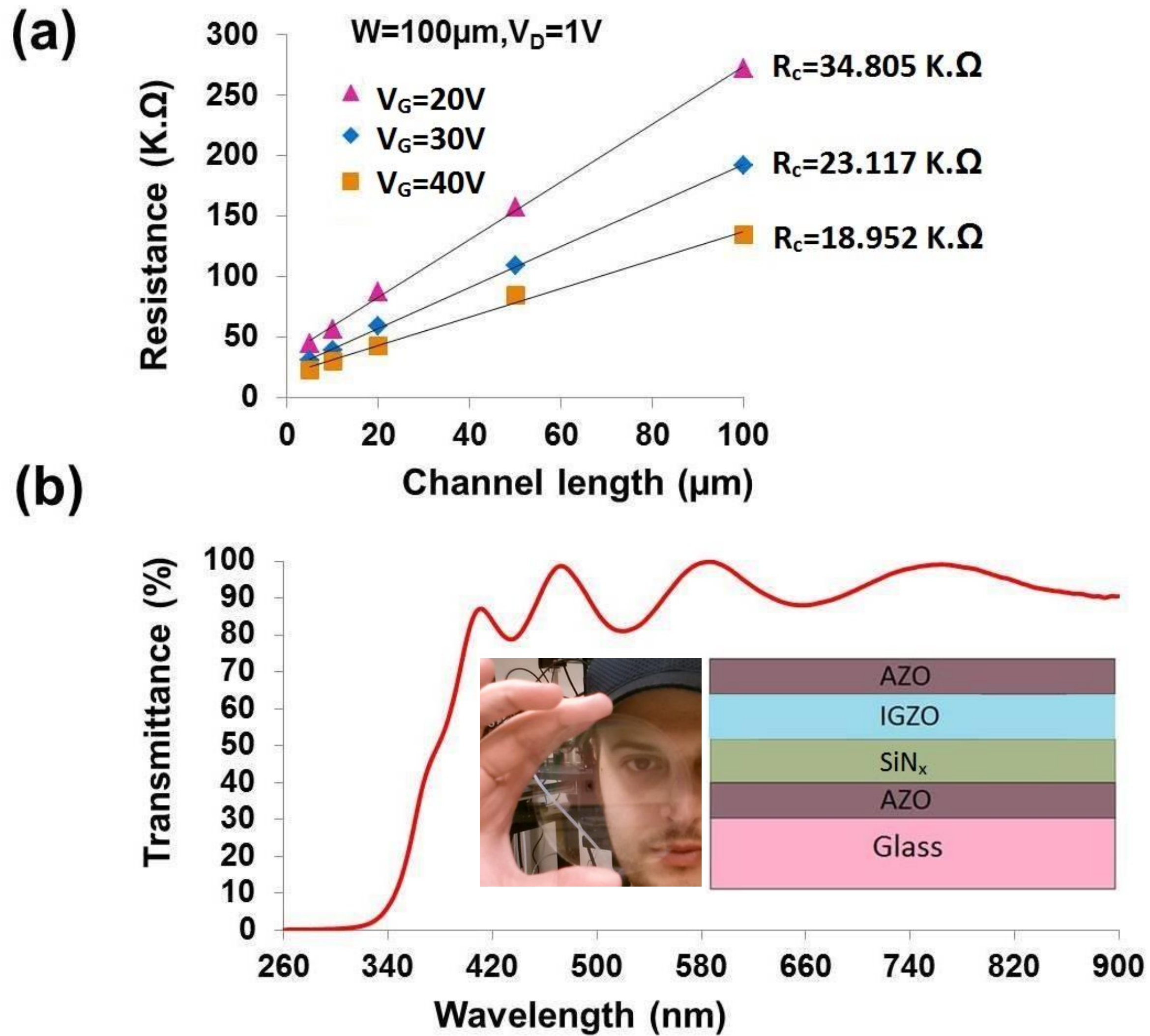

Figure 6-2 (a) Contact resistance of the fabricated TFTs extracted using the transmission line model. (b) Optical transmittance of the fabricated device.

For V_G=40 V, the width normalized R_CW value was found to be 0.18 kΩ.cm (channel width is 100 µm). This is comparable with common contact resistance values reported for lift-off patterned Ti/Au (0.10 kΩ.cm) and Ti (0.05 kΩ.cm) [101] shadow mask patterned ITO (0.10 kΩ.cm) [113], and is much better than the findings of other groups which have reported width normalized values of 2 kΩ.cm and 3 kΩ.cm for the shadow mask patterned [113] and lift-of patterned [114] Al contacts, respectively.

The UV-Vis optical characteristics of the transparent TFT stack, excluding the glass substrate, was measured to be more than 85% transparent (Figure 6-2(b)) in the visible regime.

The I-V transfer characteristics of the transparent devices were measured in the linear regime (Figure 6-3(a)) with a source/drain voltage (V_D)=0.1 V from device structures shown in the inset of Figure 6-3(a). The field-effect mobility (μ) of the fabricated TFTs was extracted using the gradual-channel approximation. The flexible IGZO TFTs showed a μ of ~9.3 cm^2/V.sec, V_T of ~5 V, sub-threshold swing (S.S.) of 0.8 V/decade, and $I_{on/off}$ ratio of 10^7. Fabricated TFTs showed ohmic behavior at low V_D (Figure 6-3(b)), confirming the previous contact resistance measurements.

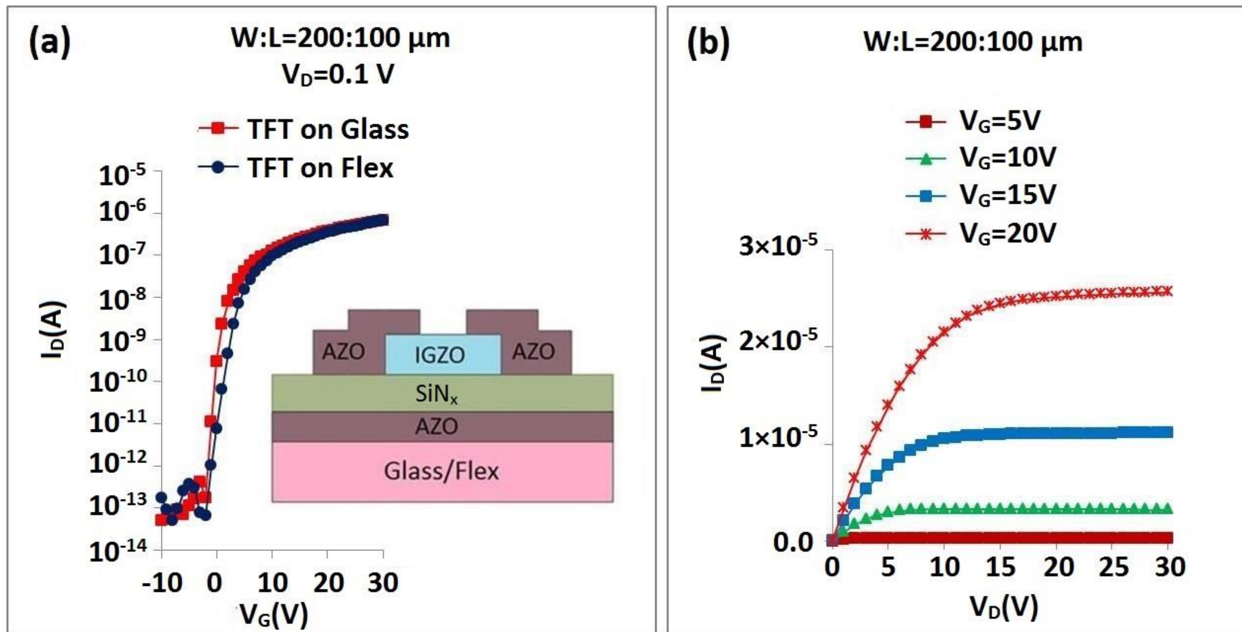

Figure 6-3 (a) Transfer characteristics of the flexible transparent IGZO TFTs along with the schematic of the IGZO TFT structure (inset), (b) output characteristics.

In comparison with the flexible TFTs, TFTs on glass had very slightly improved I-V characteristics with μ of ~9.5 cm^2/V.sec, V_T of ~4 V, S.S. of 0.5 V/decade, and $I_{on/off}$ ratio of 10^7. This negligible difference between the TFTs on glass and plastic demonstrate the feasibility for scaling the wet-etch approach to both rigid and flexible platforms.

In order to better understand the electrical stability of the fabricated TFTs, dc gate-bias stress measurements were performed for 3.6×10^3 s bias times. Connection setup and schematic of applied gate voltage (V_G), drain voltage (V_D), and the recovery test during the bias stress measurements are shown in Figure 6-4(a) and Figure 6-4(b), respectively. The degradation in drain current (I_D) of the TFTs was measured while applying an overdrive voltage ($V_{OV}=V_G-V_{T0}$) of 15 V with V_D of 0.1V, under dark conditions in air, Figure 6-4(a). After a stress time of 3.6×10^3 s, the bias was removed and the recovery of I_D was measured using a pulsed-gate signal (pulse width ~25 ms) and gradually lengthening the rest intervals from 10^{-1}s to 10^2 s (with $V_{G(on)}=V_{OV(on)}$, $V_{G(off)}$=0 V, and V_D=0.1 V), Figure 6-4 (b). Following the removal of the dc gate-bias, a rapid increase of I_D was measured during pulsed-gate recovery measurements as shown in Figure 6-5(a).

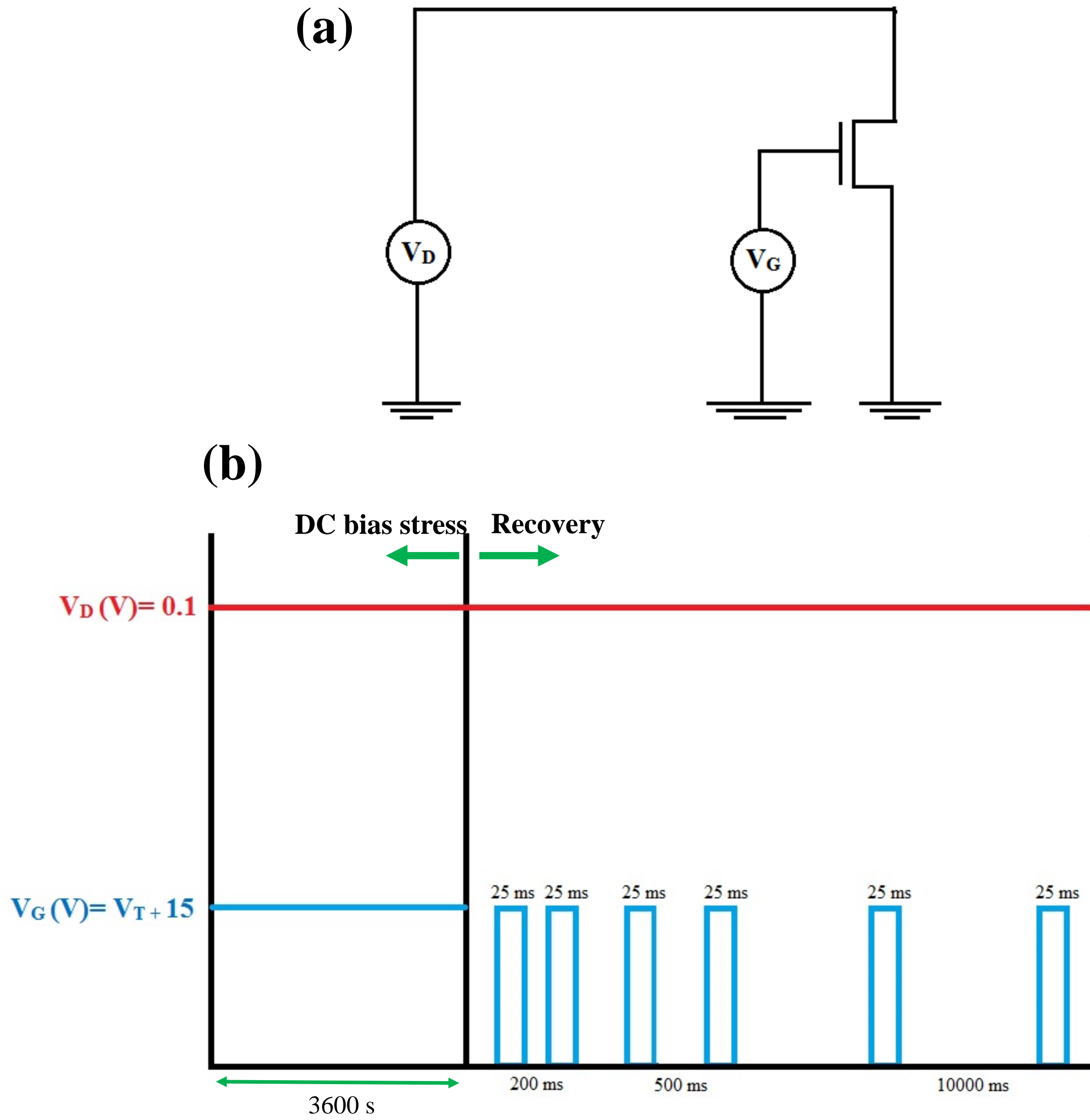

Figure 6-4 (a) Connection setup and (b) schematic of applied gate voltage (V_G) and drain voltage (V_D) and the recovery test during the bias stress measurements

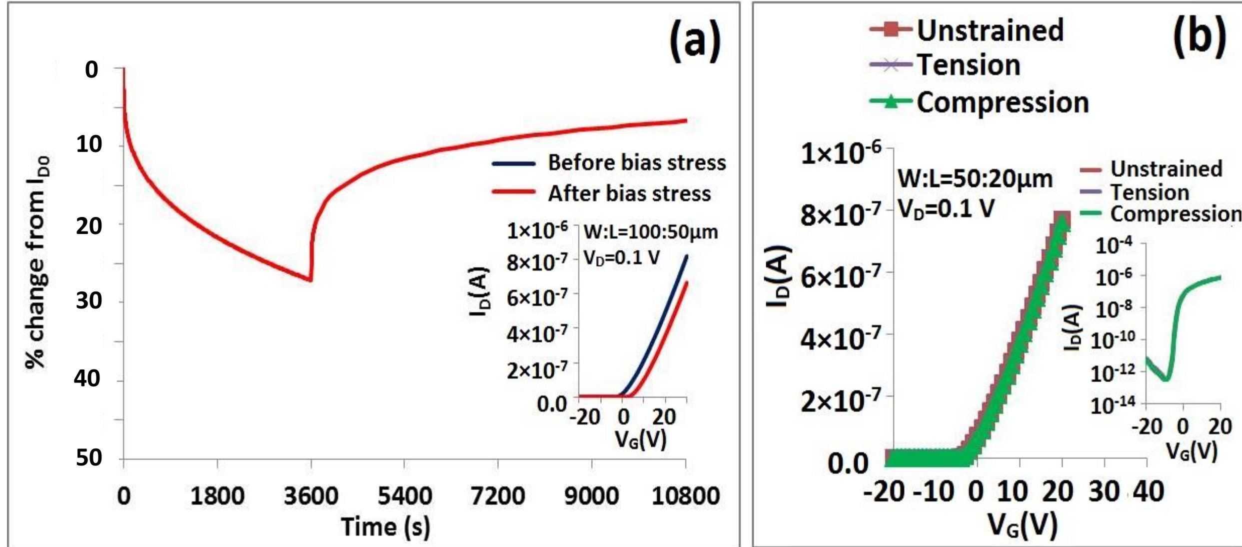

Figure 6-5 Degradation in I_D with bias stress (Vov=15 V and V_D=0.1 V) with TFT transfer curves before and after bias stress (inset). (b) Transfer characteristics for transparent TFTs showing instantaneous effects of applied strain.

This degradation and fast recovery is likely due to shallow interface trap states, which was observed in fabricated IGZO TFTs previously. The percentage of released charge after 2 hours of recovery time at room temperature was roughly 80%, which, similar to lift-off patterning technique, suggesting that the dominant aging mechanism is charge trapping. The inset of Figure 6-5(a) shows the V_T shift of ~3.8 V. The slope of the transfer curves did not show a measurable change in the field-effect mobility. The sub-threshold swing was also found to remain the same before and after the bias stress.

The effect of mechanical bending on the I-V characteristics of the TFTs fabricated using the selective wet-etch process and transparent contacts was also studied. The effect of mechanical bending on the instantaneous TFT I-V characteristics was measured under uniaxial tensile and compressive strain applied along the length of the devices (parallel to I_D) by bending the samples in concave and convex orientations with an 11 mm radius of curvature at room temperature. The bending radii (R) is converted to percent strain (ε) using equation 6.1 [51]:

$$\varepsilon = (\frac{1}{R})(\frac{d_f + d_s}{2})(\frac{\chi\eta^2 + 2\chi\eta + 1}{\chi\eta^2 + (1+\chi)\eta + 1}) \quad (6.1)$$

where d_f and d_s are the corresponding thicknesses of the film (including all layers in Figure 6-3(a) (inset)) and the PEN substrate. Y_f and Y_s are the respective Young's modulii. The values of Y_f and Y_s are 137 GPa [67] and 5.5 GPa [51], respectively. Moreover, $\chi = Y_f/Y_s$, and $\eta = d_f/d_s$. According to the above formula, it was found that the percent stain (ε) under bending radii (R) of 11 mm is 0.62 %.

As can be seen in Figure 6-5(b), the fabricated TFTs had the same instantaneous I-V characteristics when unstrained and under tensile and compressive strain states. The lack of change in the electrical characteristics may be due to the overlapping s-orbitals in the IGZO conduction band. The mechanical strain on the thin-film does not significantly affect these overlapping orbitals and the electronic properties of the semiconductor, unlike previous reports of flexible a-Si: TFTs [122]. This observation provides optimism that the semiconducting oxide TFTs may have an advantage over organic and silicon-based TFT devices.

6.4. Conclusions

The findings of this study demonstrate the fabrication of fully transparent flexible IGZO TFTs using a wet-etching process that takes advantage of the selective etching of amorphous and polycrystalline transition metal oxide thin-films [123]. A selectivity of nearly 20 was found for a dilute HCl solution in water for patterning AZO source/drain electrodes on IGZO channel layers [124]. The resulting patterned electrodes had a low contact resistance (R_c~19 kΩ) and high optical transparency of ~85%. Flexible IGZO TFTs measured under tensile and compressive mechanical strain demonstrated similar I-V characteristics. The similar I-V characteristics are due to the overlapping spherical s-orbitals in the conduction band of IGZO channel layer. Testing of the electrical stability of the TFTs showed a V_T shift of ~3.8 V after 3600 s of dc gate bias (V_{ov}=15 V

and V_D=0.1 V). Pulsed-gate recovery measurements showed rapid recovery of the drain current, suggesting that the dominant aging mechanism is charge trapping. The resulting electrical characteristics of TFTs demonstrate the effectiveness of selective wet-chemical etch processes for fabricating transparent electronics using a simple, low-cost, and scalable patterning process.

Chapter 7

7. SiO_x thin-film plasma damage and hydrogen diffusion barriers for high-performance flexible transparent IGZO TFTs and circuits

7.1. Introduction

The previous chapter demonstrated the feasibility of fabricating optically transparent high-performance flexible IGZO TFTs using a conventional PECVD gate dielectric and selective wet-etch patterning onto flexible substrates. However, in order to integrate flexible IGZO TFTs with other electronic components, passivation of the IGZO TFTs is necessary.

The effect of the back channel passivation layer on the performance of the MO based TFTs, and bias stability has been studied by several research groups [18, 32, 125-131]. It is demonstrated that charge trapping at the channel layer/gate dielectric layer and/or charge injection into the underlying gate dielectric layer, by itself, cannot explain the TFT instability. It is also proposed that the adsorption/desorption of oxygen and water onto the TFT back channel layer, dramatically, affects the bias instability of fabricated TFTs.

Yang et al. evaluated the impact of passivation layer on the performance of Al–Sn–Zn–In–O thin-film transistors. Obtained results showed that temperature and bias-induced stability of the bottom-gate TFT structure were considerably improved by applying an appropriate passivation layer of Al_2O_3 thin-film deposited by atomic-layer deposition (ALD) method. It was believed that back channel passivation layer by annihilation of ambient molecule-related deep states, on the TFT back channel layer, can supress the density of bulk traps that gives rise to improved TFT performance and stability. The obtained results also demonstrated that charge trapping at the channel layer/gate dielectric layer and/or charge injection into the underlying gate dielectric layer, by itself, cannot

explain the TFT instability [126]. Yoo et al. reported the effect of magnesium oxide (MgO) and silicon oxide (SiO_2) back-channel passivation layer on the performance of a-IGZO thin-film transistors. MgO and SiO_2 were deposited by pulsed-laser deposition (PLD) method in this research. It was proposed that the adsorption/desorption of oxygen and water onto the back channel layer of TFTs dramatically affected electrical instability of fabricated TFTs. By comparing the performance of unpassivated, SiO_2, and MgO passivated TFTs, it was found that TFTs with MgO passivation layer demonstrated the minimum change in V_T during the bias stress. This optimum result was attributed to the hygroscopic nature of the MgO passivation layer which can dramatically supress adsorption (desorption) of oxygen (water) molecules and improve TFT performance under bias stress [127]. Other groups have reported adopting of sputtered SiO_x [128], organic layer (CYTOP) [32], organic photoacryl (PA) [18], PECVD SiO_x [18], polymethyl methacrylate [48], and inductively coupled plasma chemical vapor deposited (ICP-CVD) SiO_x [49] as back channel passivation layers. It was believed that the passivation layers by suppressing the interactions between external environment and oxide surface gives rise to a better TFT performance and stability. Hsieh et al. reported that different measurement environments (vacuum and atmosphere) resulted in different V_T shifts. They suggested that only electron-trapping cannot explain the V_T shift under bias stress. It was believed that adsorption of oxygen also needs to be taken into the account to describe the V_T shift after bias stress [52].

Some researchers have reported that the IGZO channel layer becomes conductive after passivation of the backchannel if conventional PECVD insulator materials such as SiN_x [132] and SiO_x [9] are used. It has also been reported that out-diffusion of H atoms from plasma-enhanced chemical vapor deposition (PECVD) dielectrics to the IGZO channel layer during the deposition [9, 10] forms shallow H donors [11, 12] that increases the semiconductor conductivity and degrades the TFT I-

V characteristics. In addition, ion bombardment of the IGZO channel layer during the deposition produces plasma damage by forming oxygen deficiency shallow donors, thereby increasing the channel conductivity in MO-TFTs and resulting in inferior TFT performance [12-15]. High-temperature deposition and high-temperature post-thermal-annealing processes have been shown crucial in adjusting the hydrogen [16] and oxygen [17] concentration of IGZO channel layers in both academia and industry. However, these approaches are not compatible with conventional low-melting point polymeric substrates. Other studies have solved back-channel passivation issues by using exotic materials, expensive unit process deposition methods [35], and not-repeatable back-channel treatment techniques [14], none of which are compatible with the current large-area electronics industry. This chapter proposes a simple, low-temperature, and relatively low-cost approach that uses a SiO_x hydrogen diffusion barrier that also protects against subsequent plasma-related damage of the thin-film for fabricating low-temperature processed back-channel etched transparent IGZO TFTs.

7.2. Experimental

Bottom-gate IGZO TFT device structures were fabricated on flexible (polyethylene naphthalate (PEN) with a thickness of 125 µm) and rigid (glass and highly p-type doped Si) substrates. An 80 nm aluminum-doped zinc oxide (AZO) layer was sputtered (power=80W, pressure: 2mTorr, and $Ar:O_2$ ratio of 15:0) at 150°C and patterned using dilute HCl to define the bottom-gate electrode. A 50 nm thick RF reactive sputtered IGZO (power=100W, pressure: 5mTorr, and $Ar:O_2$ ratio of 12:1) channel layer was deposited at room temperature (RT). Individual islands were then patterned by wet etching to define the active area using a dilute HCl solution. A 200 nm thick 150°C sputtered AZO film (power=80W, pressure: 2mTorr, and $Ar:O_2$ ratio of 15:0) was deposited as the source/drain (s/d) contact (Metal 2) layer followed by photolithographic patterned AZO

source/drain contact followed by a dilute HCl wet etch. In order to study the effect of backchannel plasma damage, two different passivation structures were introduced. In the first structure, a 300 nm SiN_x layer was directly deposited over the backchannel at 150°C, and in the second structure a 30 nm SiO_x barrier layer was deposited by room temperature (RT) electron-beam evaporation onto the intrinsic IGZO channel followed by a 270 nm 150°C PECVD SiN_x to form a bilayer SiN_x/SiO_x passivation layer over the TFT. To distinguish the effect of the backchannel plasma damage from gate dielectric material on the TFT performance, three different gate dielectric structures were applied. The first test structure consisted of a 300 nm SiN_x PECVD thin-film deposited at 150°C. The second structure consisted of a PECVD bilayer dielectric with SiO_x(50 nm)/SiN_x(300 nm) deposited at 150°C, and the third TFT test structure was fabricated on 200 nm thermal SiO_2 on highly p-type doped c-Si wafers. A via contact opening in the dielectric passivation layer was created using buffered hydrofluoric (BHF) acid solution. Finally, a 300nm AZO layer was sputtered (power=80W, pressure: 2mTorr, and Ar:O_2 ratio of 15:0) at 150°C, and patterned as the top metal (Metal 3) contact and etched using a dilute HCl solution. Figure 7-1 shows the fabrication process flow and device image obtained from optical microscopy. Applied materials, deposition techniques, and the patterning methods used in this chapter are also shown in Table 7-1.

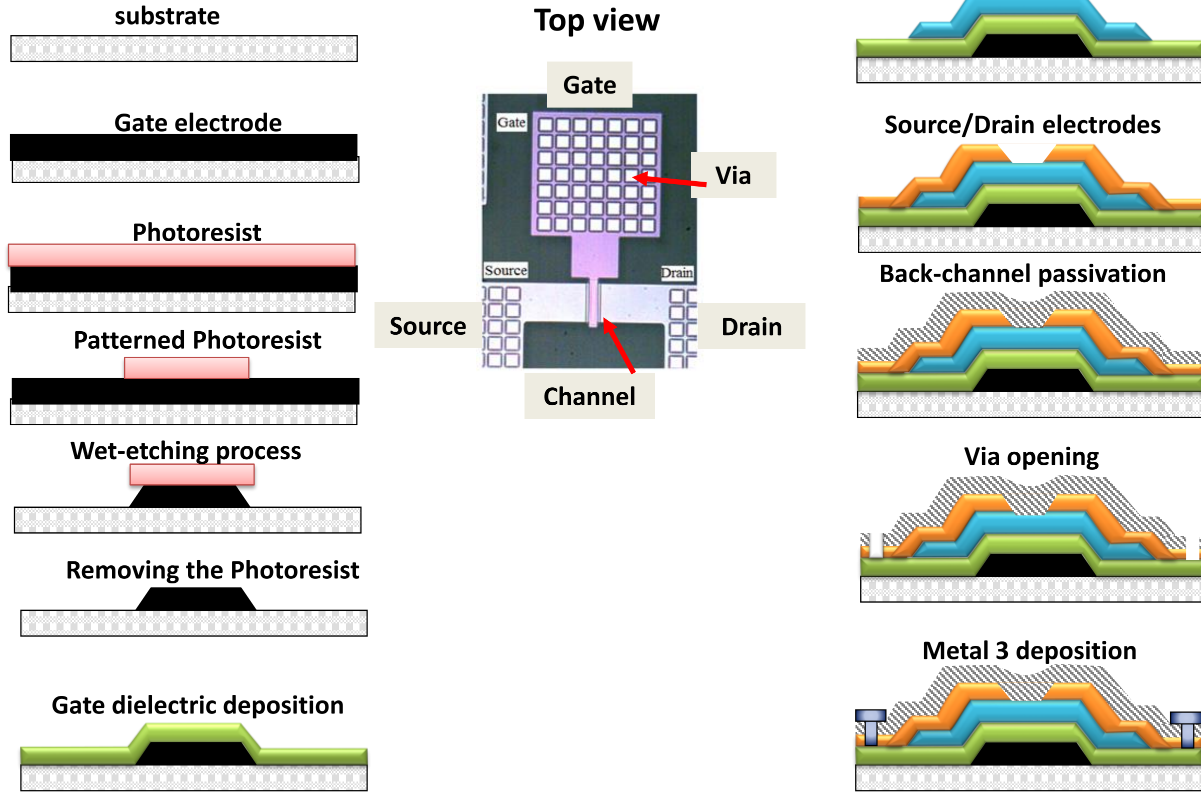

Figure 7-1 Fabrication process flow.

Table 7-1 Thin film materials, deposition and patterning techniques used in this chapter to fabricate optically transparent flexible IGZO TFTs.

	Materials:	**Patterning process:**
Gate electrode	150°C AZO (Sputtering)	Photolithography and wet-etch patterning (using positive PR)
Gate dielectric	150°C PECVD SiN_x/SiO_x	----------
Channel layer	RT IGZO (Sputtering)	Photolithography and wet-etch patterning (using positive Pr)
Source/Drain	150°C AZO (Sputtering)	Photolithography and wet-etch patterning (using positive Pr)
Passivation layer	RT e-beam SiO_x/150°C PECVD SiN_x	Photolithography and wet-etch patterning (using positive Pr)
Final metal	150°C AZO (Sputtering)	Photolithography and wet-etch patterning (using positive Pr)

7.3. Results and discussion

Figure 7-2 shows the cross section and the I-V characteristics of non-passivated IGZO TFTs fabricated using a selective wet-etch process and transparent AZO contacts.

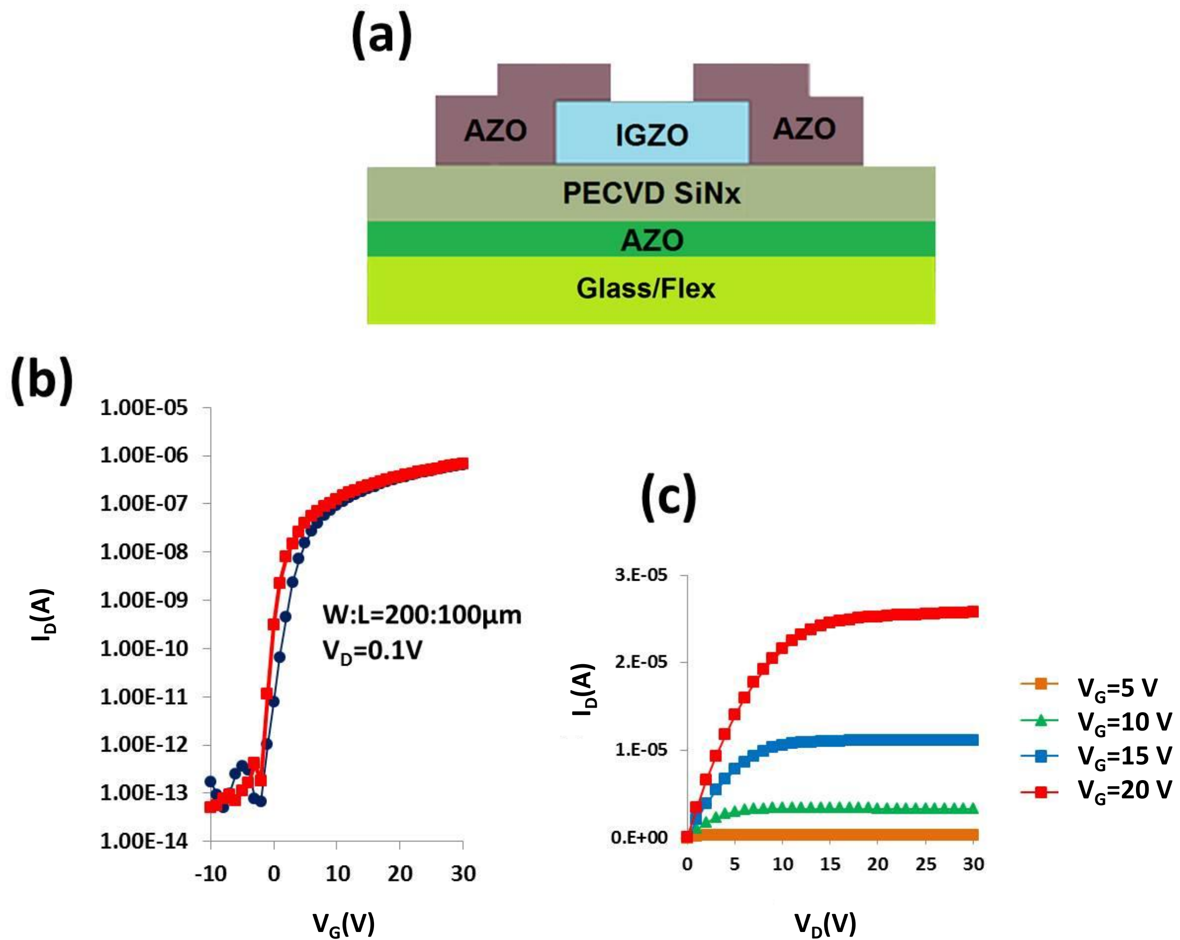

Figure 7-2 The cross-section (a), transfer (b), and output characteristics (c) of the flexible transparent IGZO TFTs.

The I-V transfer characteristics of the TFTs were measured in the linear regime with a source/drain voltage (V_D)=0.1V. The field-effect mobility μ of the fabricated TFTs was extracted using gradual channel approximation. The fabricated TFTs showed a μ of ~9.3 cm^2/V.sec, V_T of ~4 V, sub-threshold swing (S.S.) of 0.8 V/decade, and $I_{on/off}$ ratio of ~10^7. The output characteristics also showed linear behavior at low V_D, which indicates good ohmic behavior at the

contacts. However, in order to fabricate advanced electronic devices and circuits, single TFTs need to be integrated with other electronic components through back-channel passivation deposition, etched via openings, and contact metals to electrically connect different devices. Figure 7-3 shows the I-V transfer characteristics of our fabricated TFTs after 300 nm PECVD SiN_x passivation layer deposition and the via opening. In this TFT structure, which we call "Structure #1", PECVD SiN_x was directly deposited onto the IGZO backchannel.

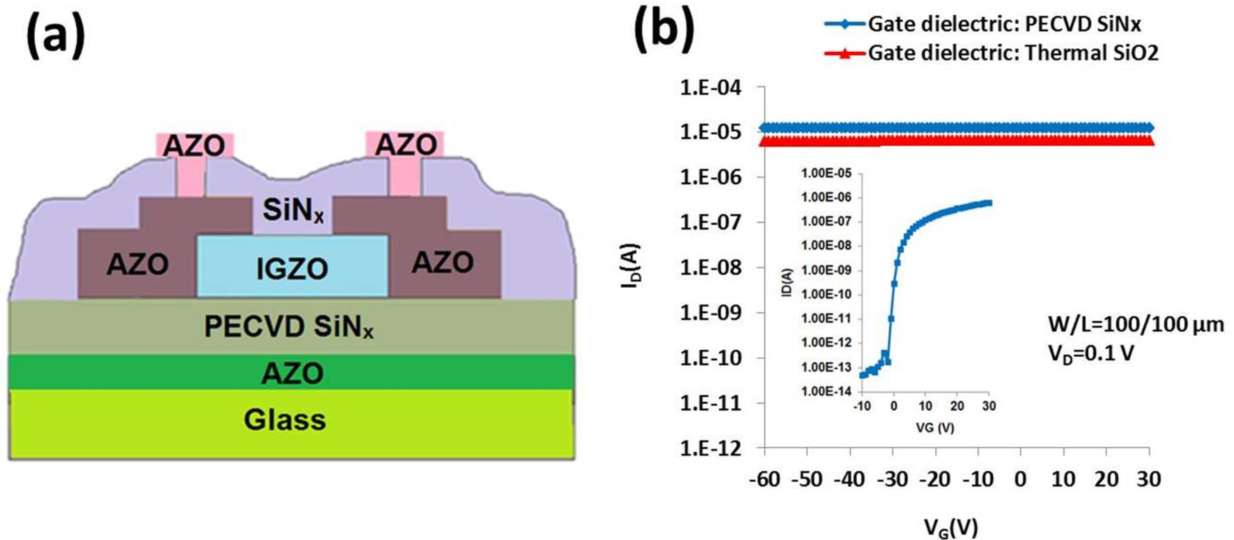

Figure 7-3 The cross-section (a), and transfer characteristics (b) of the bottom-gate low-temperature processed PECVD passivated transparent IGZO TFTs; with the TFT transfer curve before passivation deposition (inset).

As can be seen, the TFTs showed no switching behavior due to the highly conductive channel layer. Similar behavior has been observed by other research groups [14] and is suggested to be due to the plasma damage of the back-channel and the out-diffusion of hydrogen atoms from the PECVD plasma to the IGZO channel layer. To distinguish the effects of the front channel from those of back-channel during the next thermal-processing steps, IGZO TFTs were also fabricated on thermal SiO_2 dielectric material. A similar trend in degradation of I-V characteristics was

observed for the TFTs fabricated on thermal SiO_2 dielectric material, and IGZO TFTs showed an always ON-state behavior.

In order to prevent the back-channel plasma damage and diminish the out-diffusion of H atoms to the channel layer, another passivation structure was designed, and called "Structure #2". In this structure, a thin layer (30 nm) of RT e-beam SiO_x was deposited directly onto the IGZO back-channel layer and followed by a 270 nm PECVD SiN_x layer. As can be seen in Figure 7-4, the new passivation structure (Structure #2) resulted in switching characteristics in both TFTs fabricated on thermal SiO_2 and PECVD SiN_x gate dielectrics. However, the TFTs fabricated on PECVD SiN_x showed a large negative V_T shift (> 20 V), a poor S.S. (3.04 V/decade), and about one order of magnitude increase in I_{off} compared to the TFTs fabricated on thermal SiO_2.

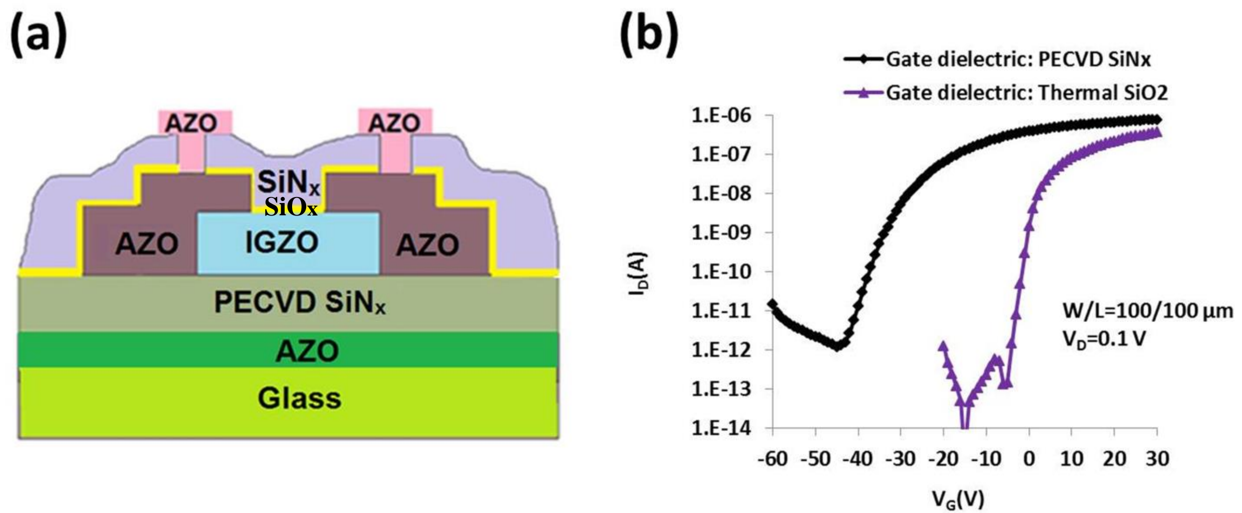

Figure 7-4 The cross-section (a), and the transfer characteristics (b) of the passivated low-temperature processed transparent IGZO TFTs with back-channel damage barrier structure.

These results show that although back-channel damage is the dominant factor in the degradation of TFT I-V characteristics, it is not the only reason; the front-channel also contributes to this

degradation effect during the subsequent thermal process and integration steps. The origin of this degradation may be due to H diffusion as was reported earlier in Chapter 4.

In Chapter 4, we reported that different gate dielectric materials by changing the chemical composition of the IGZO TFT's active layer, especially the oxygen deficiency contents and hydrogen (H) concentrations, can result in different primary I-V characteristics in this materials system. Thus, the increasing thermal budget and subsequent processing steps result in the out-diffusion of H atoms from the PECVD SiN_x gate dielectric and formation of more oxygen deficiency in the IGZO channel layer. This out-diffusion resulted in a highly conductive channel layer and poor device characteristics with a negative shift in V_T, higher I_{off}, and degradation in S.S. To test this hypothesis, a thin PECVD SiO_x diffusion barrier, with much lower hydrogen content than the underlying nitride layers, was inserted between the nitride and the channel layer. The SiH_4 gas flow during the SiO_x deposition was more than 3× less than during SiN_x deposition. In addition, to further minimize the hydrogen content, SiH_4-N_2O gases were used for the PECVD oxide rather than the SiH_4-NH_3 used for the nitride deposition.

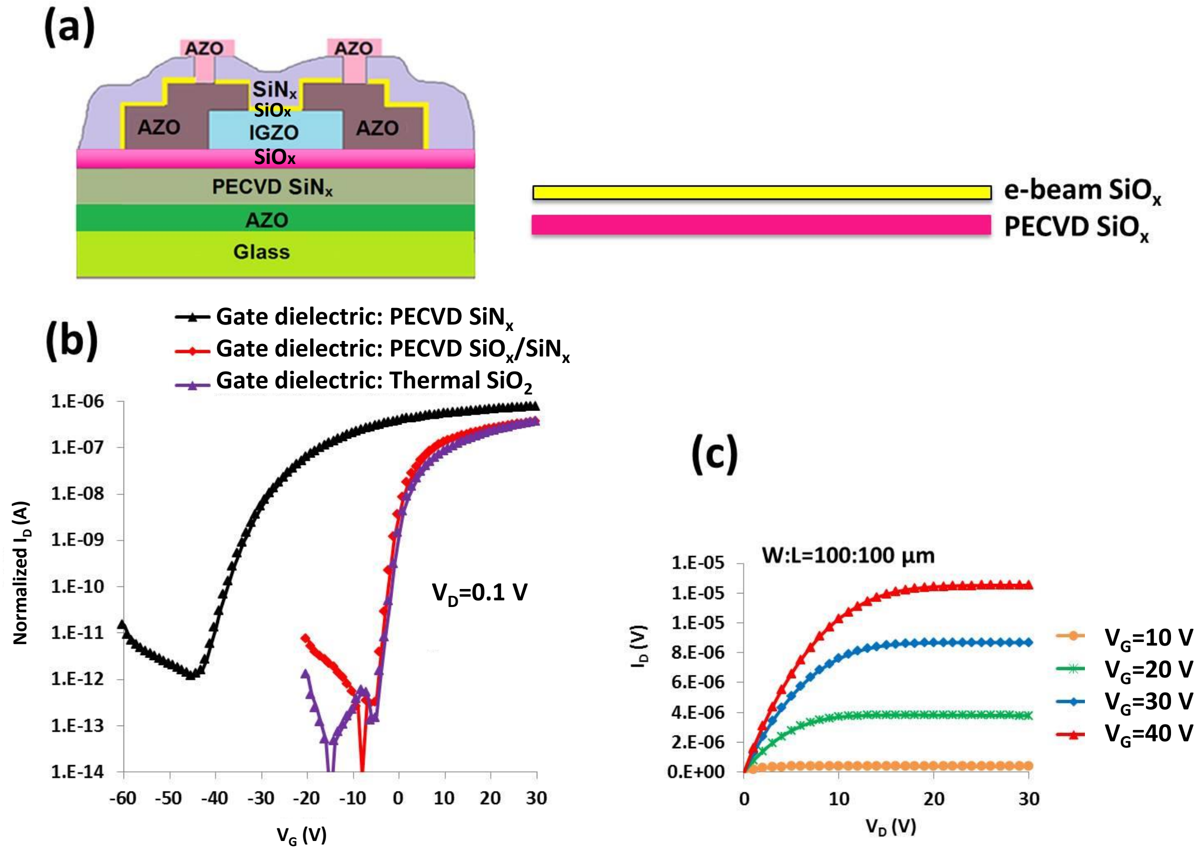

Figure 7-5 The cross-section and (b) the transfer characteristics of the passivated low-temperature processed transparent IGZO TFTs fabricated on different gate dielectrics. (c) The output characteristics of the passivated TFTs on bilayer PECVD SiOx/SiNx dielectric

The I-V characteristics of the encapsulated TFTs with bilayer passivation structure (e-beam SiO_x/PECVD SiN_x) and bilayer gate dielectric (PECVD SiO_x/PECVD SiN_x) structure showed improved electrical characteristics and behaved similarly to the TFT fabricated on thermal SiO_2 dielectric materials (Figure 7-5). The passivated IGZO TFTs showed a μ of ~ 6.7 cm^2/V.sec, V_T of ~ 1V, S.S. of 0.8 V/decade, and $I_{on/off}$ ratio of $>10^6$. These results confirm that chemical composition of gate dielectric materials not only affect the primary results of unpassivated IGZO TFTs but also contribute to TFT performance degradation during the next thermal-process and integration steps.

In order to better understand the electrical stability of the low-temperature processed encapsulated TFTs, using structure #2, dc gate-bias stress measurements were performed for 1 hour dc bias time. The degradation in drain current (I_D) of TFTs was measured while applying an overdrive voltage ($V_{OV}=V_G-V_{T0}$) of 15 V with V_D of 0.1V under dark conditions in air. After a stress time of 3.6 $\times 10^3$ s, the bias was removed and the recovery of I_D was measured using a pulsed gate signal (pulse width ~25 ms) and gradually lengthening the rest intervals from 10^{-1}s to 10^2 s (with $V_{G(on)}=V_{OV(on)}$, $V_{G(off)}=0$ V, and $V_D=0.1$ V). Following the removal of the dc gate-bias, a rapid increase of I_D was measured during pulsed-gate recovery measurements as shown in Figure 7-6. This degradation and fast recovery is likely due to shallow interface trap states, which were observed in fabricated IGZO TFTs previously. The percentage of released charge after 15 minutes of recovery time at room temperature was roughly 87%, which, similar to the recovery of the non-passivated device developed in Chapter 6, suggesting that the dominant aging mechanism is charge trapping in the gate dielectric, near the dielectric/semiconductor interface, or at the top interface between IGZO channel layer and encapsulation layer, as can be seen in the cross-sectional diagram of the device in the inset of Figure 7-6.

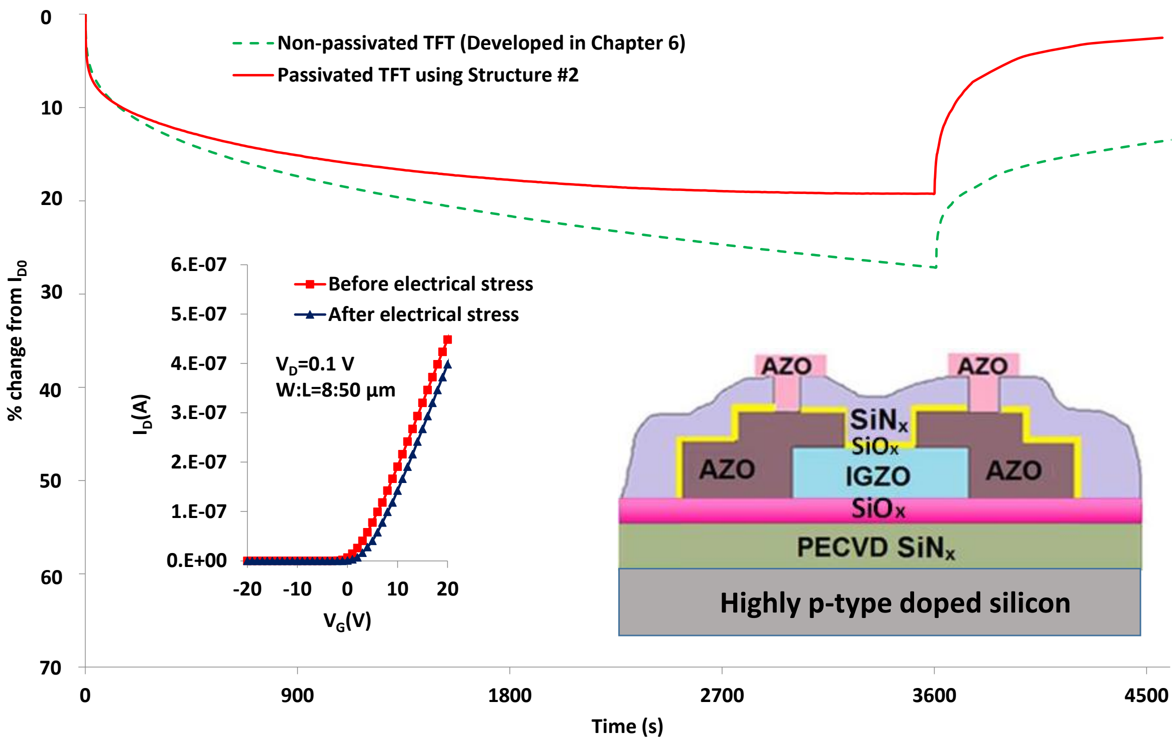

Figure 7-6 Degradation in I_D with bias stress (V_{ov}=15 V and V_D=0.1 V). (inset) TFT transfer curves before and after bias stress (mechanically flat) and (inset) cross-sectional diagram of the device.

As can be seen in Figure 7-6, passivated TFT demonstrated ~11% less degradation in I_D after 1 hour bias stress and showed a faster recovery compared to the non-passivated device. The inset of Figure 7-6 also shows a V_T shift of 2.3 V, which is less than the V_T shift (3.8 V) observed for the non-passivated device developed using a single PECVD SiN_x gate dielectric in Chapter 6. These findings suggest that encapsulation of fabricated TFTs using a low-temperature processed e-beam SiO_x/PECVD SiN_x bilayer passivation layer and bilayer gate dielectric (PECVD SiN_x/PECVD SiO_x) could be an effective approach to reducing the charge trapping of back and front channels, respectively, resulting in better bias stability in fabricated TFTs.

7.4. Conclusions

To prevent the effect of plasma damage and out-diffusion of H atoms during the PECVD passivation process, a thin RT e-beam SiO_x barrier layer was directly deposited onto the IGZO back-channel layer prior to a thick PECVD SiN_x passivation layer [133]. It was found that although the back-channel damage is the dominant factor in degradation of TFT I-V characteristics during the passivation/integration process, the chemical composition of the gate dielectric material also plays a key role in the electrical performance of the passivated device. To diminish the degradation effects of the PECVD SiN_x gate dielectric layer in the next passivation and thermal processing steps, and to minimize the out-diffusion of hydrogen atoms to the IGZO channel layer and formation of oxygen deficiency, a thin layer of PECVD SiO_x was deposited prior to the IGZO channel layer [134]. The fabrication process was performed at a maximum temperature of 150°C and took advantage of a high wet-etch selectivity between AZO and the insulator, and channel-layer materials in the BHF and HCL solutions, respectively. Low-temperature processed TFTs with bilayer passivation (e-beam SiO_x/PECVD SiN_x) and bilayer gate dielectric (PECVD SiO_x/PECVD SiN_x) structures demonstrated a μ of ~6.7 cm^2/V.sec, V_T of ~1 V, S.S. of 0.8 V/decade, and an I_{on}/I_{off} ratio of $> 10^6$.

Chapter 8

8. Conclusion and future work

8.1. Conclusion

This Ph.D. dissertation has addressed and overcome engineering and scientific challenges in developing large-area flexible transparent electronics based on IGZO TFTs. It was proposed that a low-temperature industry-friendly approach to fabricating high-performance flexible transparent IGZO TFTs is viable using industry standard device structures, process equipment, and process sequences that are similar to those of existing conventional a-Si TFT processing. The above contributions to the field of flexible transparent electronics would not have been possible without covering different factors that affect transistor performance, such as materials processing and characterization, device processing and characterization, the process of integration onto flexible platforms, and the development of a simple back-end encapsulation process. The following were investigated:

- ✓ The current-voltage (I-V) characteristics of IGZO TFTs were studied as a function of deposition temperature and annealing environments in order to establish a basis for the investigations of this research. In both cases of low-temperature deposition temperature and thermal-annealing, changing the chemical composition of the channel layer was found to be the dominant factor in different I-V characteristics of IGZO TFTs.
- ✓ It was found that a bi-layer dual gate SiO_x/SiN_x IGZO TFT structure was more effective for fabricating high-performance IGZO-based TFTs than fabricating directly onto SiN_x dielectric layers. The observed improvement in the IGZO films and the measured improvement in the electrical characteristics were correlated to minimization of oxygen deficiency formation due to hydrogen diffusion into the overlying semiconducting IGZO

layer. The SiO_x capping layer was also found to be an effective hydrogen diffusion barrier between the silicon nitride and IGZO channel, demonstrating the efficacy of using the bi-layer PECVD-grown dielectric structures to improve the performance of the TMO TFT devices.

- ✓ By controlling the combined effects of the channel layer deposition temperature and post-thermal annealing with the chemical composition of the gate dielectrics, the conductivity of the channel layer was tuned, to produce a high-performance, low-temperature processed working TFT, using conventional PECVD gate dielectric layers.
- ✓ Optically transparent high-performance IGZO TFTs were fabricated using IGZO thin-films as the channel layer and contact electrodes by tuning the sputtering parameters such as deposition power, deposition pressure, Ar/O_2 ratio, and deposition temperature. The transparent TFTs exhibited a μ of ~9.4 $cm^2/V.sec$, V_T of ~3 V, a S.S. of 0.42 V/decade, and an $I_{on}/_{off}$ ratio of > 10^6. No current crowding behavior was observed for the TFTs under the low drain-source voltage (V_D) regime. Transmission line method (TLM) results were also presented for the contact resistance. Electrical instability measurements of the TFTs exhibited a V_T shift of ~2 V after 3600 s of dc gate bias (V_{ov}=10V and V_D=0.1V). Pulsed-gate recovery measurements also demonstrated rapid recovery of the drain current, suggesting that the dominant aging mechanism is charge trapping.
- ✓ Optically transparent flexible IGZO TFTs were fabricated using a wet-etching process that takes advantage of the selective etching of amorphous and polycrystalline transition metal oxide thin-films. A selectivity of nearly 20 was found for a dilute HCl solution in water for patterning AZO source/drain electrodes on IGZO channel layers. The resulting patterned electrodes had a low contact resistance (R_c~19 kΩ) and high optical transparency of ~85%.

Flexible IGZO TFTs measured under tensile and compressive mechanical strain demonstrated similar I-V characteristics. The similar I-V characteristics were correlated to the overlapping spherical s-orbitals in the conduction band of the IGZO channel layer. Testing the electrical stability of the TFTs showed a V_T shift of ~3.8 V after 3600 s of dc gate bias (V_{ov}=15 V and V_D=0.1 V). Pulsed-gate recovery measurements showed rapid recovery of the drain current, suggesting that the dominant aging mechanisms is charge trapping. The resulting electrical characteristics of TFTs demonstrate the effectiveness of selective wet-chemical etch processes for fabricating transparent electronics using a simple, low-cost, and scalable patterning process.

- ✓ A thin room-temperature-deposited e-beam SiO_x barrier layer was directly deposited onto the IGZO back-channel layer prior to a thick PECVD SiN_x passivation layer in order to prevent plasma damage of the IGZO channel region. It was found that although back-channel plasma damage is the dominant factor in degradation of TFT I-V characteristics during the passivation/integration process, it is not the only reason, and the chemical composition of the gate dielectric material also plays a key role in the electrical performance of the passivated device. In order to diminish the degradation effect of the PECVD SiN_x gate dielectric layer in the next passivation and thermal processing steps and decrease out-diffusion of hydrogen atoms to the IGZO channel layer, a thin layer of PECVD SiO_x was deposited prior to the IGZO channel layer. The fabrication was performed at a maximum temperature of 150°C and took advantage of a high wet-etch selectivity between AZO and the insulator and channel layer materials in the BHF and HCL solutions, respectively. Optically transparent flexible TFTs with bilayer passivation (e-beam SiO_x/PECVD SiN_x) and bilayer gate dielectric (PECVD SiO_x/PECVD SiN_x)

structures demonstrated a field-effect mobility (μ) of ~6.7 $cm^2/V.sec$, threshold voltage (V_T) of ~1 V, and an $I_{on}/_{off}$ ratio of > 10^6, which satisfies the TFT requirements for developing large-area high-performance see-through flexible displays.

8.2. Future work

According to data obtained in this Ph.D. study, some suggestions for future research in the field of transparent flexible electronics area are briefly addressed below:

1-In order to further improve the I-V characteristics of the passivated flexible transparent IGZO TFTs, it might be possible to further prevent (a) out-diffusion of hydrogen atoms from the passivation layer, proposed in this study, to the IGZO channel layer, and (b) the formation of the oxygen deficiency during the backchannel layer deposition. This modification can be done by optimization of the deposition parameters of the e-beam SiO_x layer. It is expected that the lower energy of the deposited atoms in the modified recipe might reduce the oxygen deficiency concentration, due to the lower kinetic energy of the evaporated atoms. Further improvement can be observed by adjusting the distance of the e-beam/PECVD interface layer from the IGZO back-surface. In addition, PECVD SiN_x can be replaced by the PECVD SiO_x to further reduce the H diffusion from PECVD layer to the IGZO channel layer.

2-The surface states of the backchannel layer play a key role in the long-term electrical stability of the transition metal oxide TFTs. Hence, it would be a good idea to study the effect of the proposed passivation structure on the long-term electrical stability of our fabricated transparent flexible TFTs.

3-If the TFTs fabricated in this study are going to be used as the backplane TFTs of large-area flexible displays, their I-V characteristics need to be fully studied under long-term bending conditions. Aging and recovery measurements under constant bending conditions will give better

insight into their capabilities before these material systems are applied in transparent flexible displays.

4-This Ph.D. dissertation has demonstrated the feasibility of fabricating back-channel etched transparent flexible IGZO TFTs using a simple, low-cost, and scalable patterning process. One of the key applications of developed TFTs is in the driving circuits of AMOLED displays. In general, OLEDs are current driven devices that require high and uniform current to emit light. The driving circuits of OLED displays can be fabricated and designed with other available TFT technologies such as low-temperature polycrystalline silicon (LTPS) or amorphous silicon. Although LTPS TFTs demonstrate high mobility and electrical stability, their uniformity is limited and therefore they are not suitable for large-area display applications. On the other hand, amorphous silicon TFTs show good uniformity, but their low mobility and low stability limit their application in AMOLED displays. In comparison to those TFT technologies, transition-metal-oxide TFTs have high mobility, excellent uniformity, and high stability, all of which make them strong candidates for AMOLED driving circuits. Hence, fabrication of optically transparent flexible circuits, based on our developed IGZO TFTs, will be an interesting topic of research; and it will be interesting to integrate these TFTs with OLEDs and study the operational behavior of both. For example, research is needed on how mobility variation and threshold voltage shift in TFTs possibly affect performance of the TFT circuit and the OLEDs (e.g. OLED degradation and efficiency) during long-time operation. The outcome of this research topic will open an opportunity to develop optically transparent flexible OLEDs that can be used in advanced consumer electronic products such as smart watches, smart phones, and heads-up displays. In addition, fabricated circuits based on IGZO TFT structures, as proposed in this research, by having the functions of both transparency and flexibility can be integrated with flexible solar cells, with a very low optical absorption.

Furthermore, investigating the electrical stability of fabricated devices under mechanical strain could result in the development of conformal flexible electronics that are electrically stable. Hence, investigating and overcoming the engineering and scientific challenges behind these integration processes should be a rewarding focus for future work.

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