Modified Differential Cascode Voltage Switch Logic Optimized for Sub-threshold Voltage Operation

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Ultra-low sub-threshold voltage research has become increasingly important with the recent shift in consumer electronics towards low power designs for mobile, wearable, and implantable technologies. These applications are able to trade-off speed for reduced power consumption and reduced minimum operating voltage. This thesis studies circuit design solutions that focus on achieving the lowest minimum operating voltages. These applications are likely to be ones where the supply voltage may come from energy harvesting sources that are only able to source ultra-low voltages.

The logic circuit presented in this thesis is a modified implementation of differential cascade voltage switch logic (DCVSL). Differential logic has improved ultra-low voltage performance over static CMOS logic and the modification to DCVSL offers a logic structure that can implement multi-input AND/NAND and OR/NOR gates while maintaining a stack height of one. This logic circuit is referred in this thesis as MOD-DCVSL. The modification requires the use of capacitive boosting to allow for normal logic operation.

The results of this thesis show that differential logic styles are able to perform at lower minimum operating voltages compared to static CMOS logic styles but at the cost of larger delay and power compared to static CMOS. On average the differential implementations could operate at a minimum supply voltage 5 mV lower than CMOS for two input implementations and 10 mV lower for three input implementations. The delay of differential implementations was approximately double for both two and three input implementations. The power of the differential implementations are approximately 20% higher than static CMOS for two input implementations but this gap is narrowed to approximately 10% for three input implementations, here the lower minimum operating voltages allowed for decreased power consumption. Due to the consistently lower delay, static CMOS had a lower power delay product than the differential logic. When comparing only the differential logic, MOD-DCVSL offered negligible difference for two input implementations but was able to improve delay by 7% and power by 11% in the three input implementations.

Acknowledgements

Thanks to Professor Sachdev for giving me the opportunity to pursue my Masters at the University of Waterloo as well as providing advice and guidance that was essential in the success of my thesis.

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Chapter 1

Introduction

The continued improvements in integrated circuit (IC) design has made computing widely available and increasingly affordable. IC innovations have also been instrumental in the ability to make battery operated mobile devices. This shift from desktop computing to mobile computing, wearable technology, and other low power devices has led to an increase in the importance of ultra-low voltage research. This chapter will discuss the motivation of the thesis, the history of scaling, the theory behind the thesis and an outline of the chapters that follow.

1.1 Motivation

The motivation for this thesis is to find an alternative logic style that can operate at a minimum operating voltage in the sub-threshold voltage range with the intention of consuming less power. This solution would address two issues that are becoming significant in the IC industry. Those two issues are the power wall and the emergence of wireless devices.

1.1.1 The Power Wall

The IC industry has continued to find a way to keep Moore's law on track overcoming hurdles, however, the industry is fast approaching another hurdle. This hurdle is the power wall and as the number of transistors per unit of area increases the power density,

and ultimately heat per unit area are approaching a physical limit known as the power wall.

It is because of the power wall that some have referred to the state of semiconductors as dark silicon. This is because the limits of power density have limited the percent of the processor that can be on at a time and as a result large areas of chips are powered down to reduce power density.

The power wall is one of the reasons that there has been a shift of focus for IC design to look to new ultra-low voltages solutions. This may be achieved through many different solutions varying from software implementations to changing the physical design of transistors and everything in-between.

1.1.2 Emergence of Wireless

With the increased prevalence of wireless devices and low voltage applications, the need for devices that can operate at lower supply voltages is becoming increasingly important. These applications range from the increase in wearable technology and the interest in implantable technologies. These applications are able to trade-off speed for a decrease in power. This has resulted in a change in focus from increasing performance by scaling devices sizes and increasing switching speeds to looking for alternatives to decrease the power consumption of the devices.

When looking at sub-threshold circuits there are specific applications that are interested in minimum power. The first is a situation where you need an always-on circuit that will be used to wake-up other circuits, an example might be a sensor used to measure very infrequent events. In this situation a reduction of supply voltage will result in a reduction of power. The second main application are sensors that rely on energy harvesting as their voltage supply. In this case the maximum supply voltage of different types of energy harvesting devices limit the choice of circuit that is able to operate under the voltage constraint. In this situation there would be an advantage to a circuit that could operate at a minimum supply voltage that the energy harvesting can supply.

1.2 Low Voltage to Achieve Low Power

A solution that is studied in this thesis is low voltage to achieve low power. The advantage of operating at the lowest possible supply voltage is the positive linear relationship that

supply voltage and power have. This means that the minimum power consumption occurs at the minimum operating voltage. A downside of operating at the lowest supply voltage is the negative exponential relationship that supply voltage has with delay, as the supply voltage is reduced the delay increases exponentially. The power consumed over this period of time, a measure of energy, will start to be dominated by the exponentially increasing delay and the energy consumption will not be at the minimum operating voltage. These relationships are discussed in more detail in Chapter 2. Depending on the application this is a useful design compromise.

1.3 Outline

The remainder of this thesis is organized into 6 chapters as follows. Chapter 2 provides background information with a summary of semiconductor history, overview of device physics, and the current state of the art design in both semiconductor and IC design. Chapter 3 is an outline of the test benches and figures of merit used to determine the performance of the circuits under test. Chapter 4 is an analysis of simulation results for each of the different logic circuits tested. Chapter 5 is a comparative analysis of the figures of merit to determine the viability of the logic circuit proposed. Chapter 6 is the conclusion with a summary of the results and a discussion of the future research opportunities. ultra-low sub-threshold voltage operation.

Chapter 2

Background

The idea of operating in the sub-threshold region is not a new concept and research dates back to the early 1970s. This early research was built upon over the years, but, aside from a few industries, the need for ultra-low power was overshadowed by the demand for faster processors and larger memories, achieved by decreasing delay and increasing the density of devices.

Starting from the lowest level, the semiconductor industry has focused on year over year improvements to large-scale integration. This year over year improvement was primarily focused on scaling the devices physical size as well as scaling the voltage to reduce the electric field and increase the speed of the devices. The principles of scaling did provide some improvements in design that allowed for better ultra-low voltage design but this was not the main intention.

From a circuit design perspective, research focus has been shifting as industry realizes that the biggest markets are no longer in desktop computing and servers but rather are in mobile devices. These applications have put an increased focus on power efficient designs that can offer adequate performance while increasing battery life.

Ultra-low power design spans all levels of an electrical system. The focus of the research done in this thesis is circuit design where it is assumed that the only device parameters that can be manipulated are the length and width of the transistors. This chapter will provide a brief history of the research done both in semiconductor and circuit design with respect to ultra-low power sub-threshold voltage region of operation. It will then summarize the fundamental equations that are used to develop ultra-low power designs and modifications. Lastly it will give an overview of the current state of the art technology, and a brief look at what research is being done into future designs.

2.1 History of Semiconductor Scaling

Since the founding work of the transistor, done by Bardeen, Brattain and Shockley at Bell Labs in 1947, there has always been an incentive for smaller, faster, and lower power transistors. Soon after the transistor was integrated into silicon the principles of generalized scaling were laid out by Roberd Denard [4]. Generalized scaling works by scaling all of the dimensions, the voltage, and increasing doping concentrations. This results in improvements in the power, density, and delay. The other noticeable benefit was that the MIPS/watt scaled with a cubic relationship to the scaling factor. This was an effective method of increasing the performance but eventually additional manufacturing techniques were required to be able to continue the performance gains.

The 90 nm node saw the introduction of strained silicon. This is a technique used to improve performance that is used to augment scaling. There are a few different methods to achieve strained silicon but the basic idea behind it is that the crystalline structure that silicon forms is created in a way that the structure is pulled or pushed to achieve a tensile or compression strain and as a result of this, the electrons in the device will see an improvement in mobility. It is shown in Figure 2.1 that the use of strained silicon is used from the 90 nm node through to the 22 nm node.

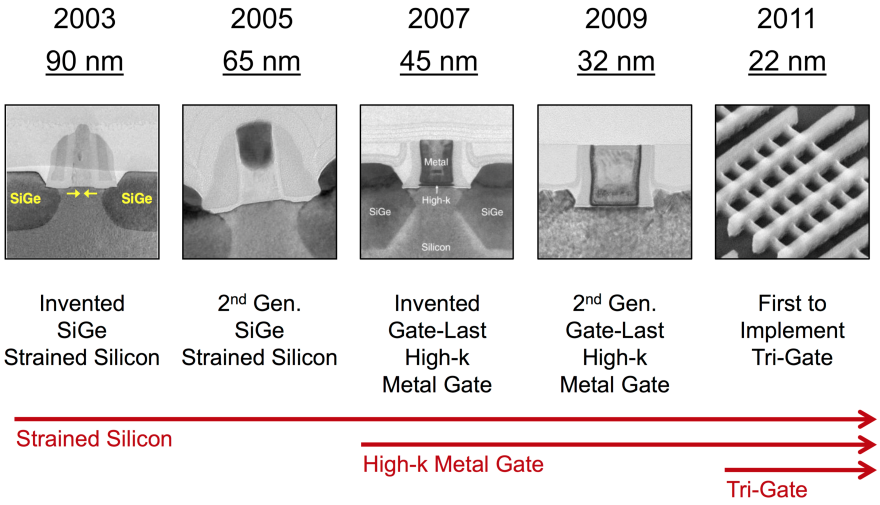

Figure 2.1: Progression of Transistor from 90 nm down to 22 nm[1]

The next major innovation in transistor design was the use of high K dielectrics, first introduced in the 90 nm node. High K dielectrics allowed for further scaling of the gate

oxide. This also allowed for further reduction of the supply voltage as thinner oxides reduce the supply voltage required to achieve an appropriate electric field.

Deviation from the traditional 2D bulk CMOS design came at the 22 nm node with the introduction of the tri-gate or 3D transistor that allowed for better control of the gate by increasing the surface area that the gate has with the channel. Multi-gate designs including double-gate, tri-gate and FINFET are referred to as 3D transistors. This is the technology that Intel is currently using as their processor technology [source].

To move beyond the technology node that we are currently at there are a few areas of research that would allow for scaling to continue.

As traditional scaling methods are coming closer to theoretical limits the effort to continue semiconductor scaling has moved to alternative areas of research. The use of new materials such as germanium and III-V elements could be used on top of silicon substrate. Additionally novel transistor designs could allow for continued scaling. Examples are tunneling FETs that use band to band tunneling that allow for a steeper sub-threshold slope, ideal when working at low supply voltages and ultra-low power.

2.2 Development of Sub-Threshold Models

The work done by R. M. Swanson and J. D. Meindl in [5] and Masuhara in [6] are some of the first papers to develop the models of sub-threshold operation and to understand the diffusion mechanisms of the sub-threshold devices. With this information they were able to determine a minimum operating voltage of a transistor. This research was continued by Eric Vittoz in 1977 to better understand devices operating in the sub-threshold region [7]. The paper provided examples of a variety of analog circuits that could take advantage of operation in this region [8]. The biggest applications at the time for operation in the sub-threshold region was the watch industry and the hearing aid industry, both very big industries in Switzerland where Vittoz was doing his research. The next section is a summary of the device physics that are used today.

2.3 Regions of Operation

The MOSFET regions of operation are depicted in Figure 2.2, they are the saturation region, triode region, and the cutoff/sub-threshold region. Each of these regions are discussed in detail.

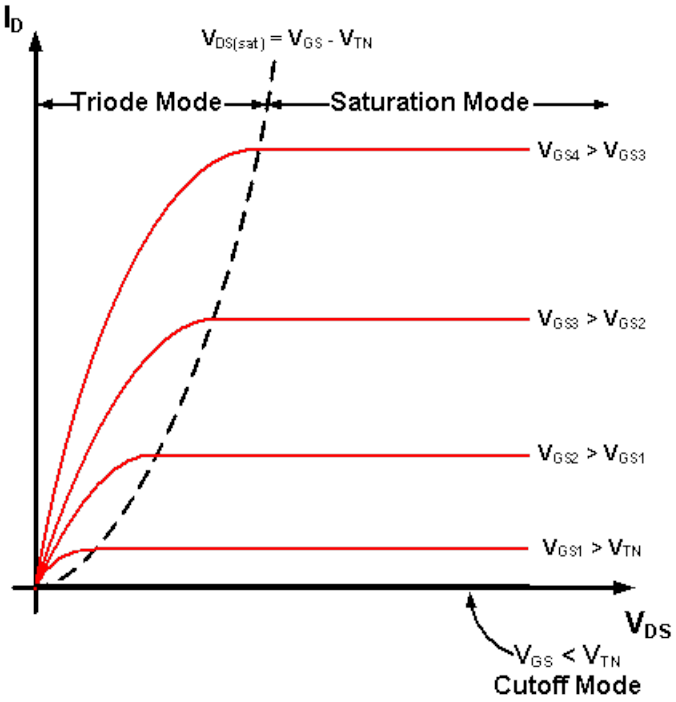

Figure 2.2: MOSFET Regions of Operation [2]

2.3.1 Saturation Region

The saturation region condition is, $V_{GS} > V_{TH}$ and $V_{DS} \geqslant (V_{GS} - V_{TH})$. With these conditions met the device is 'on'. The current in the saturation region, I_D, is described by Equation 2.1. In this equation, μ_n is the effective mobility of the charge carrier, C_{ox} is the capacitance of the oxide, W/L is the ratio of the width to the length of the transistor, V_{GS} is the gate to source voltage, V_{TH} is the threshold voltage, λ accounts for the channel length modulation, V_{DS} is the drain to source voltage, and V_{DSat} is the voltage at which the MOSFET enters the saturation region.

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + (\lambda V_{DS} - V_{DSat})) \tag{2.1}$$

2.3.2 Triode Region

The conditions for triode region are, $V_{GS} > V_{TH}$ and $V_{DS} < (V_{GS} - V_{TH})$. In this region the device still allows current to flow through a channel but the channel does not conduct as much as in the saturation region. The current in this region is shown in Equation 2.2. The equation uses all the same parameters discussed in the saturation region.

$$I_D = \mu_n C_{ox} \frac{W}{L}((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}) \tag{2.2}$$

2.3.3 Cut-off/Sub-threshold Region

In Figure 2.2 the cut-off/sub-threshold region is shown as having no current flowing, below V_{TH} the drain current I_D is zero and the device is off. In an ideal MOSFET this would be the expected behavior, however, this is not the case and the device does still conduct a small amount of current below the threshold voltage.

The equation for sub-threshold current is shown in Equation 2.3. Here, V_{GS} is the gate to source voltage, V_{DS} is the drain to source voltage, v_t is the thermal voltage which is defined as kt/q, m is the sub-threshold swing coefficient, V_{TH} is the threshold voltage of the device and I_0 can be further expressed as shown in Equation 2.4.

$$I_{sub-th} = I_0 e^{(V_{GS}-V_{TH})/mv_t}(1 - e^{-V_{DS}/v_t}) \tag{2.3}$$

$$I_0 = \mu_0 C_{ox} \frac{W}{L}(m-1)v_t^2 \tag{2.4}$$

In Equation 2.4, μ_0 is the zero bias mobility, C_{ox} is the capacitance of the gate oxide, W/L is the width over length ratio, and m is the sub-threshold swing coefficient. The exponential relationship between current and the gate to source voltage is important to note. This relationship means that as the voltage is scaled the drive current of the device is reduced exponentially and this results in an exponential increase in the delay. When looking at the power delay product this becomes significant.

The general equation for power consumption in sub-threshold circuits is shown in Equation 2.5 where the total power is the sum of the dynamic power (also referred to as switching power) and the leakage power.

$$P_{total} = P_{dynamic} + P_{leakage} \tag{2.5}$$

The dynamic power is the power consumed when the circuit is switching. The leakage power is the power that is dissipated when the devices are not experiencing any change to the outputs but the devices that are off arent completely turned off and a small amount of current still flows. The leakage power is simply the leakage current multiplied by the supply voltage V_{DD}. The equations for leakage and dynamic power are shown in Equation 2.6 and Equation 2.7 respectively.

$$P_{dynamic} = \alpha f C_{eff} V_{DD}^2 \tag{2.6}$$

To minimize the dynamic power each of the parameters need to be understood. In Equation 2.6, α is the activity factor, f is the frequency of operation, C_{eff} if the effective capacitance, and V_{DD} is the supply voltage. The activity factor is a number normalized between 0 and 1 that represents a percentage of time that a transition at the input results in a transition at the output, this is not a parameter that can be manipulated at the circuit design level. Frequency of operation f is the speed at which the circuit operates at, the maximum frequency of operation is determined by the minimum delay of the circuit. The effective capacitance C_{eff} is determined by the devices size and the design and is the capacitance that the supply voltage must charge and discharge during switching. The larger the devices are the larger C_{eff} will be. The supply voltage V_{dd} is set depending on the application and is limited by the maximum voltage the transistors can withstand and the minimum voltage that still allows the devices to operate normally. Reducing V_{dd} it a very effective way to reduce dynamic power because of the squared relationship. This does come at the cost of increased delay.

The leakage power defined in Equation 2.7 is only a function of the supply voltage and the leakage current where the leakage current is from the equation for sub-threshold current previously defined in Equation 2.3. For leakage current the main concern is that as the supply voltage is scaled down the difference in *on* current to off current reduces to the point where leakage current becomes a significant contributor to the total power consumption. The ratio of *on* current to off current can be expressed using the equation for sub-threshold slope, Equation 2.8, where m is the sub-threshold slope coefficient, Boltzmanns constant k, temperature T, and the elementary charge q. The theoretical maximum slope, resulting in the largest *on* current to off current ratio, is $60mV/dec$. To minimize the power the work done in papers [9], [10], and [11] found that the minimum power did not occur at minimum operating voltage but rather an optimal point below the threshold voltage.

$$P_{leakage} = V_{DD} I_{leakage} \tag{2.7}$$

$$S = 2.3 \frac{mkT}{q} \tag{2.8}$$

The newly proposed circuit will be studied to understand how the circuit design compares to other logic circuits with respect to dynamic power, power delay product and other metrics.

2.4 State of the Art Semiconductor Design

A few main competing technologies in industry for state of the art semiconductor design are silicon on insulator (SOI) and multi-gate devices. SOI is a modification of bulk CMOS where a layer of oxide is buried in the substrate, this layer is referred to as the BOX. There are then two variations on this, one where the layer is partially depleted (PDSOI) and one where the layer is fully depleted (FDSOI).

Examples of multi-gate transistors include pi-gate, tri-gate, omega-gate, finFET, and gate-all-around (GAA) transistors. This advancement in technology provides better control over the gate of the device by increasing the area in which the gate can control the channel. Compared to traditional bulk CMOS, the gate is a single plane above the channel that when turned on attracts electrons to the gate creating a channel for the electrons the travel through. In the multi-gate configurations the channel is built up and a gate is wrapped around this 3D channel. Instead of the gate touching one face of the channel it can now touch two, three, or in some configurations all 4 faces of the channel, providing better control of the channel. Each extra wall that the gate controls provides increased flow and decreases the threshold of the devices.

When looking specifically at finFET devices, the benefits of this design over bulk CMOS are the increase drive current of the devices that reduces the delay of circuits. Decreasing delay is incredibly important as was determined in the analysis of the low-power equations for sub-threshold devices.[12] Decreasing the delay will result in a shift in the minimum energy point, faster operating speeds at similar voltages compared to bulk CMOS. This makes finFET more desirable for sub-threshold design compared to bulk CMOS. The challenges with finFET devices are in the fabrication of the structures.

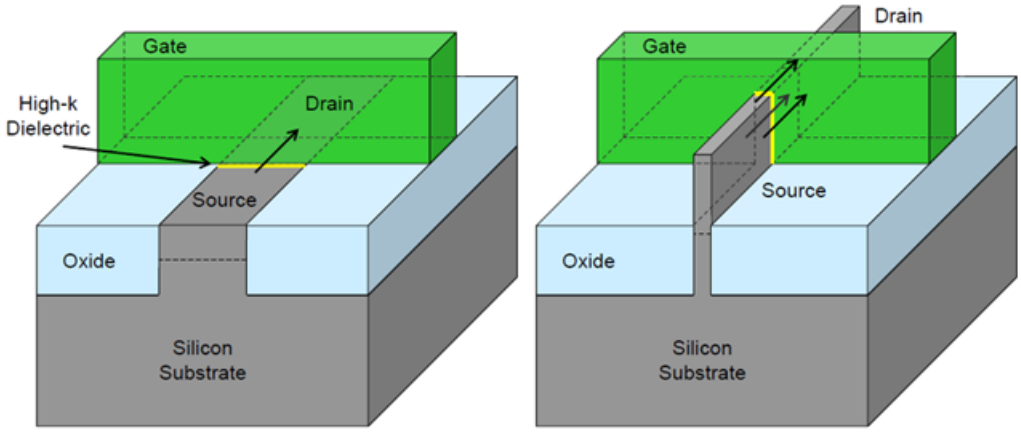

Figure 2.3: Comparison of Traditional Planar and Tri-gate [1]

Other structures have been suggested for improved low voltage applications. Deep N-Well is a structure that provides (improvements). Gallium arsenide (GaAs) is an alternative materials that, although more costly, (improvements).

A novel alternative to bulk MOSFET is the Carbon Nanotube Field Effect Transistor or CNFET. Carbon nanotubes are made by rolling sheets of graphene. These carbon nanotubes are then placed on a bulk dielectric. A gate dielectric and metal gate are built above the carbon nanotube in a similar fashion to bulk MOSFETs. To increase the throughput of an individual gate the number of carbon nanotubes that are underneath each gate can be increased. Simulations found in [13] that there were performance benefits to using the CNFET.

2.5 Current Low Power CMOS Design

The motivation behind current low voltage research is very similar to that of the original research done in the 1960's and 70's. The motivation was previously hearing aids, watches and calculators, and is now mobile devices that benefit from low power to increase battery life. Examples of these mobile devices include smart phones, tablet computers, laptop computers, smart watches, heart monitoring wristbands and other wearable sensors that can be used to monitor the body.

2.5.1 Sizing in Sub-Threshold Region

A core component of the research done in this thesis is determining the optimal sizing of devices in the sub-threshold region of operation. The traditional sizing techniques learned in digital circuit design need to be adjusted. The device sizing also depends on if the design is interested in achieving the absolute minimum operating voltage or the minimum energy consumption.

When designing in the sub-threshold region the standard assumptions that are usually made about sizing are no longer valid. Research done by [9] into understanding the optimal PMOS to NMOS ratios required to achieve minimum operating voltage determined that in the 0.18 µm technology kit a ratio of PMOS to NMOS of 12 resulted in a minimum operating voltage of 50 mV. The optimal sizing for minimum energy was determined to be minimum sized devices. This is because increasing the device sizes will increase the C_{eff} of the circuits and result in unwanted power dissipation.

2.5.2 Stack Height in Sub-Threshold Region

A design parameter that has not been studied as thoroughly is the effect of stack height on sub-threshold circuits. The research done in [14] showed that an increase in stack height resulted in a significant decrease in leakage current. This, however, came at a cost of increased delay. The research suggested that using a forced stack height was only of benefit for non-critical paths.

This metric will be of interest for this thesis as the proposed logic style is able to maintain a stack height of one for AND, OR, NAND and NOR implementations regardless of number of inputs. Also with the simplicity of the logic gates there is not a non-critical path where forced stack height would offer any benefit.

2.6 State of the Art Circuit Design

2.6.1 Dual Threshold Logic

Dual threshold circuits, often referred to DTMOS, take advantage of the input voltages to vary the body bias such that the on currents are increased. This behavior is obtained by connecting the gates of NMOS and PMOS devices to their substrate. For example, looking at transistor M0 in figure 2.4, when the gate voltage is '0' transistor M0 is off and the

voltage of the body will be '0' as well. This does not change the behavior of the the device compared to the normal CMOS inverter. The case of interest is when the gate voltage is '1', here transistor M0 is on and the body is biased with the '1' input. This differs from the normal CMOS inverter where the body would always be tied to ground. This body to source voltage increases the mobility of the carriers, improves the sub-threshold slope, and decreases the threshold voltage. As a result the on current is increased [15].

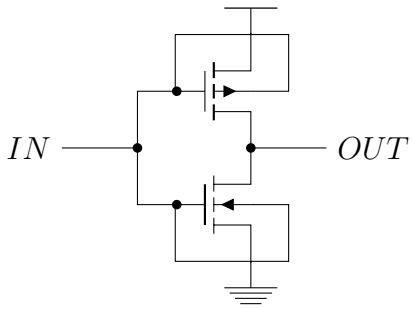

Figure 2.4: DTMOS inverter

2.6.2 Schmitt-Trigger Logic

One of the most interesting sub-threshold designs to have been proven in silicon is Schmitt-trigger logic, first proposed in [3]. The most successful outcomes of this research is the ability to operate the logic circuit at a supply voltage of 62 mV in a 13 µm technology kit. The inverter implementation of the Schmitt-trigger logic is shown in Figure 2.5. The use of Schmitt-trigger structures in logic allows for the design to reduce the leakage current in the stack of off transistors with the goal of improving the on/off ratio of the current. Ultimately it was determined that being able to improve this parameter was instrumental in being able to operate the logic circuit at ultra-low sun-threshold voltages.

The Schmitt-trigger logic design procedure starts with the basic static CMOS logic and duplicates the logic such that the stack height is doubled and in between the duplicated logic, a transistor is placed in such a way that it will turn on when the stack in question is off. In the Schmitt-trigger inverter circuit shown in Figure 2.5, transistors $M1$ and $M2$ are the traditional static CMOS logic devices that are duplicated. $M1$ and $M2$ are duplicated with transistors $M0$ and $M3$ respectively. Then transistors $M4$ and $M5$ are placed with the gate connected to the output and the source connected to the node between the duplicated devices. This will push the voltage of the intermediate node such that the voltage across the devices closest to the output will be reverse biased. When the input is low, the path

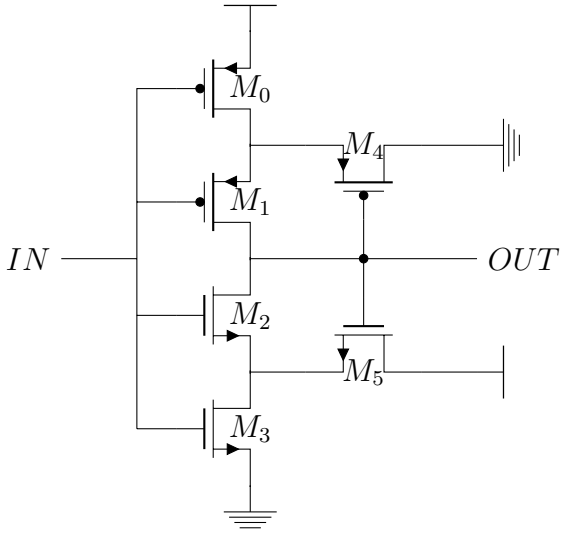

Figure 2.5: Schmitt-trigger inverter [3]

through the NMOS devices $M2$ and $M3$ will be off and would only be leaking current, which becomes more significant in sub-threshold circuits. This is counteracted with the NMOS device $M5$ whose gate is connected to the output voltage and source is connected to the intermediate node between $M2$ and $M3$. This device will be turned on and will push that intermediate node voltage to the supply voltage such that the source to drain voltage of the NMOS device closest to the output will be close to 0 and more importantly the gate to source voltage will be negative, offering an improvement in the leakage current.

The downsides to this design is the increase in number of transistors. A static CMOS inverter would typically be implemented with two devices but with Schmitt-trigger logic the design is a six device implementation and in general for all logic circuits the Schmitt-trigger implementation requires $2(N + 1)$ as many transistor as static CMOS. The stack height of the design is also larger but this issue is mitigated by the use of the intermediate transistors that reduce the leakage current in the stack.

2.6.3 Sub-Threshold Fast Fourier Transform

A sub-threshold fast Fourier transform (FFT) circuit in [16] was demonstrated to work at 180 mV. In this work specific sub-threshold design techniques were used to help achieve a minimum supply voltage of 180 mV. As mentioned in the paper the concerns at sub-threshold is the ability to reach rail-to-rail voltages. Increasing PMOS width with respect

to NMOS improves the PMOS drive current but increases the leakage and degrades the ability to achieve a low output voltage. The paper also discusses parallel leakage, sneak leakage and stacked devices all as sources of problems in sub-threshold design.

These issues were addressed individually. The use of a tiny XOR gate was not ideal due to its three leaking devices and significantly degraded output swing under worse case conditions. This was addressed with the use of transmission gate logic, which also provided better process variation immunity due to the use of both NMOS and PMOS devices in the logic. Sneak leakages were reduced with the use of inverters and buffers. Stacked devices were avoided by not using cascaded MUXs.

When these design practices were put into use, as mentioned already, the design was able to run at a minimum voltage of 180 mV and at an optimal operating point of 350 mV.

Chapter 3

Test Bench and Figures of Merit

This chapter describes the details of the simulation environment including the test bench circuits as well as the figures of merit that are used in the evaluation of the logic circuits under test. The figures of merit are explained using a simple inverter circuit for example output.

3.1 Test Bench

3.1.1 Technology Kit and Simulation Software

All simulations are done using the 65 nm technology kit provided by TSMC. The TSMC kit has several options for transistor models, such as low threshold, or high threshold MOS variants. However, this thesis is more interested in understanding the comparative performance of the logic circuits and therefore the specific transistor model is not important. For simplicity the standard NMOS and PMOS models are used. For these devices the minimum length is 60 nm and the minimum width is 200 nm.

The simulation software has the ability to vary the temperature and the process corners. Temperature can be varied to verify that a circuit can maintain its performance across a range of temperatures. Process corners can be varied to better understand the effects variations that occur in the manufacturing process. These process variations are a result of not being able to fabricate devices to their exact dimension. The variation in dimensions result in different drive strength than would be under the ideal conditions. For the purposes of this thesis the nominal temperature and the typical NMOS and typical PMOS ("TT") corners are sufficient in being able to provide a meaningful comparative analysis.

3.1.2 Test Bench Schematic

An example test bench circuit is shown in Figure 3.1. The test bench in the figure is setup to test a single ended two input static CMOS NAND gate. To make the test bench more representative of a real world circuit, the voltage sources are setup with a rise time of 50 ps, the output of the voltage source is connected to an inverter buffer and then connected into the input of the circuit under test, and the outputs are terminated with a 10 pF capacitive load.

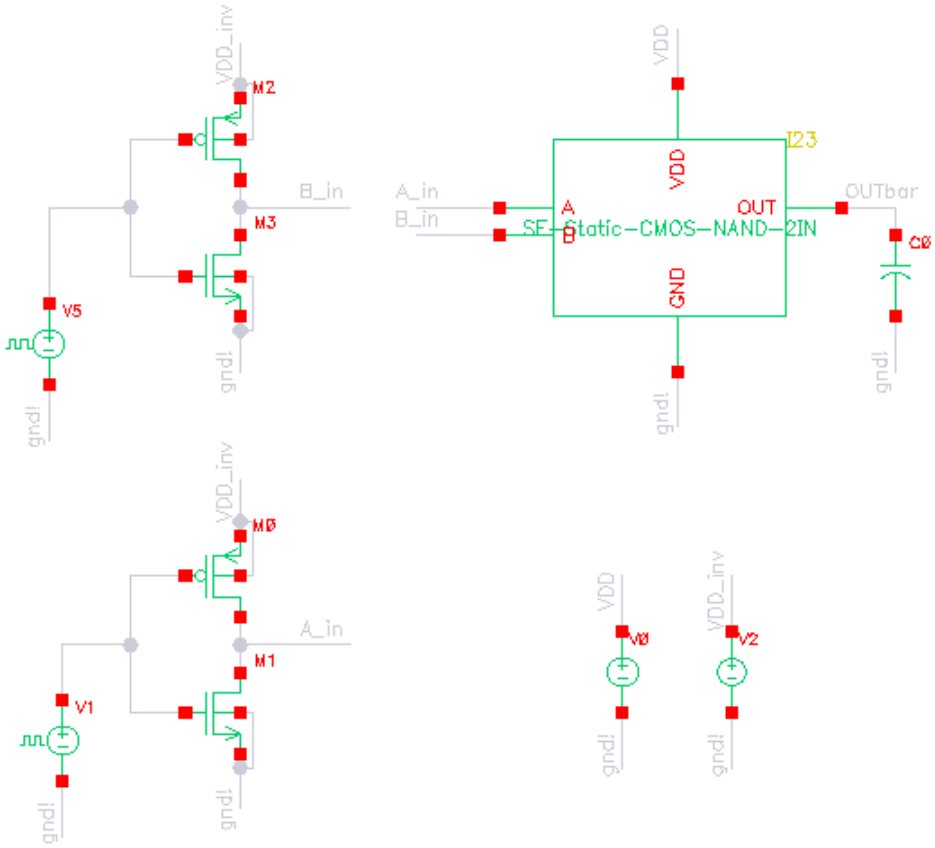

Figure 3.1: Two Input Static CMOS Test Bench

Two voltage sources are used in the test bench, This is to isolate the voltage supplied to the circuit under test from the voltage source for the buffer circuits. The current from

the voltage source for the circuit under test is used in the calculation of the power figures of merit, discussed later in the chapter.

The test benches differ depending on the specifics of the circuit. There is a different test bench used for each of the inverter and single-ended CMOS, however the same test bench is used for differential cascode voltage switch logic and the logic circuit introduced in this thesis. Additional test benches are required to accommodate logic circuits with increased number of inputs; this requires an additional input source and buffer for each additional input.

3.2 Operational Criteria

Operational criteria is the specification used when determining the limits of delay and minimum operating voltage. The criteria is that, for a given voltage, the output swing of the circuit must be able to achieve an output voltage of at least 90% of the supply voltage for output high and an output voltage of at most 10% of the supply voltage for output low. If the circuit is able to meet these criteria then it is determined to be operational.

To determine operational criteria output swing is measured, it is important to note that when an output is transitioning from high to low the output swing is measured as follows, $(1 - V_{out})/V_{DD}$. This normalization means that the operational criteria is successful when both transitions of high to low and low to high see a value of 90%.

3.3 Figures of Merit

The figures of merit that are measured in this thesis are propagation delay, minimum operating voltage, power, and power delay product. Additionally these figures of merit are measured again as the number of inputs to the logic circuits are increased from two to three. Each of these figures of merit will be discussed in detail.

These figures of merit were chosen as it was determined that they provided all of the data required to determine the viability of each of the circuits for the specific goals of this thesis. Other common figures of merit, such as size, are not included as they do not fit the goal of this thesis which was simply to design a circuit that is able to operate at the lowest possible voltages.

3.3.1 Propagation Delay

Propagation delay is a figure of merit used to determine the speed of circuits. A circuit that has a smaller delay is able to transition faster. Delay has an inverse relationship with frequency and the minimum delay is used to determine the maximum operating frequency of a circuit. In this thesis circuits are operating at ultra-low voltages and we know that delay increases exponentially as the supply voltage is decreased.

For this thesis the delay metric is included but it is not as important as power or minimum operating voltage. In theory the applications that would benefit from a reduced supply voltage would not be as concerned with speed, however, it is still important to determine the minimum delay (maximum operating frequency) of the circuits at the supply voltages for which this thesis is interested in. The delay metric will also be used in calculating the power delay product (PDP) discussed later in this chapter.

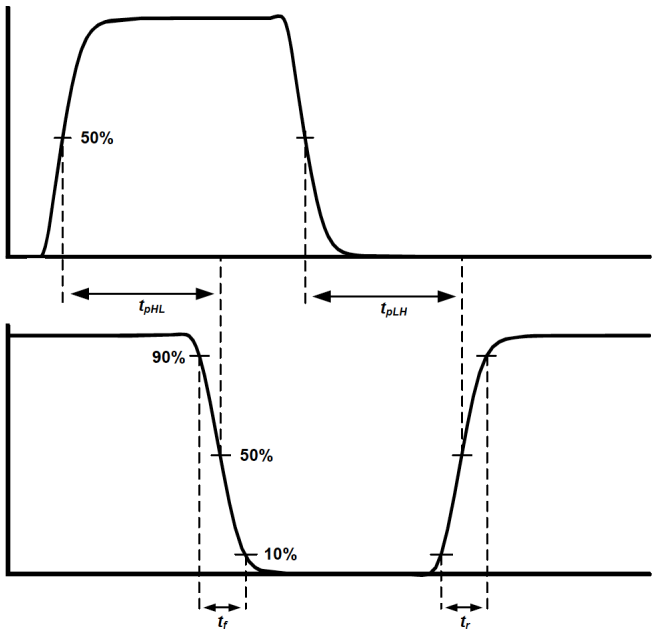

Figure 3.2: Delay Figures of Merit

The delay parameters can be seen visually in Figure 3.2. The parameters are rise time, t_r, which is the time it takes for the output to rise from 10% to 90% of the supply voltage. The fall time, t_f, is the time it takes to fall from 90% to 10% of the supply voltage. Propagation from high to low, t_{pHL}, is the time it takes for the input to rise to 50% of

the supply voltage to the time it takes for the output to fall to 50% of the supply voltage. Propagation from low to high, t_{pLH}, is the opposite and is the time it takes for the input to fall to 50% of the supply voltage to the time it takes for the output to rise to 50% of the supply voltage. The last parameter is propagation delay, t_p, which is the arithmetic mean of t_{pHL} and t_{pLH}.

These parameters are not directly measured in simulations but rather are determined by measuring the output voltage and determining the minimum delay that allows for the output to satisfy the operational criteria. This allows for a simpler approach to measuring delay, specifically for the logic circuit proposed in this thesis as they do not follow the typical delay curve shape due to the use of capacitive boosting in its design.

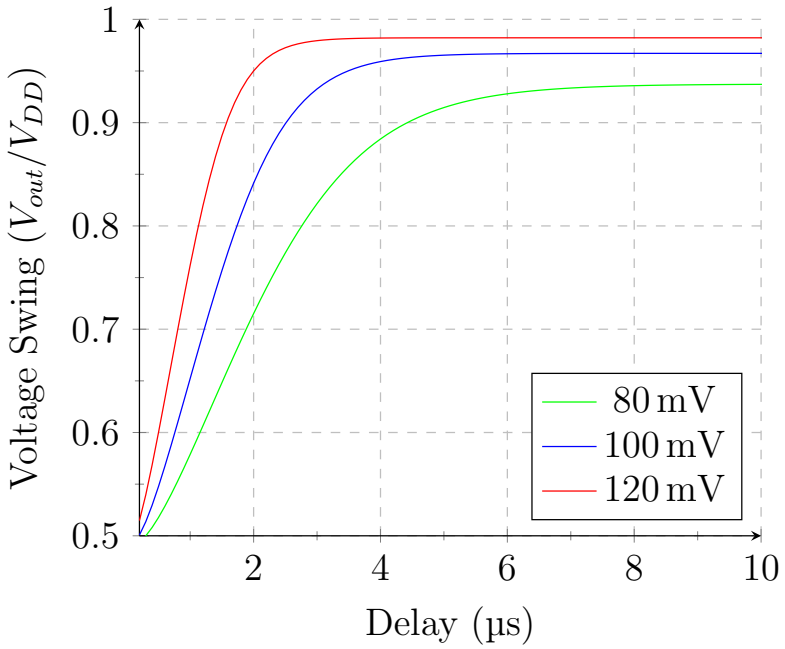

Figure 3.3: Example Simulation Data for Minimum Delay Calculation

An example of simulation data is shown in Figure 3.3. The set of data in the graph is from an inverter. The curves in this graph are for three different supply voltage values that show the maximum output voltage, normalized to the supply voltage, across a range of periods. The intersection of the curves with the 90 % horizontal indicates the minimum delay, or maximum frequency, that the circuit under test is able to operate at while still satisfying the operational criteria. For each circuit the propagation delay would be measured in 5 mV intervals from 120 mV down until the circuit is no longer able to satisfy the

operational criteria.

When measuring the delay data both the delay for output high and output low needed to be measured. As will be discussed in the next chapter, most of the design work is in balancing the propagation delays such that they are able to reach the 90% output voltage at approximately the same delay. What was found was that finding the optimal sizing at a given voltage would not be the optimal sizing at another voltage. As a result a simplification was made where if the circuit was balanced in the middle of the range of test voltages the average propagation delay, t_p, is able to offer a reasonable estimate of the optimal delay.

3.3.2 Minimum Operating Voltage

Minimum operating voltage is the lowest voltage at which the operational criteria is met. Operating at a lower supply voltage will reduce the power consumption, it is of interest to know which circuit designs offer an improved lower limit and at what cost.

The minimum operating voltage is determined using roughly the same procedure as delay. The supply voltage is swept in 0.1 mV increments down until the circuit no longer satisfies the operational criteria. It is understood that this is not a realistic degree of resolution for a simulation tool, but, for the purposes of this thesis it is assumed that with all the simulations being done under the same conditions it is still meaningful data.

An example of how this figure of merit is measured is shown in Figure 3.4. The plot shows three curves simulated at 65.5 mV, 65.6 mV, and 65.7 mV. The smallest voltage that is still able to meet the functional operation requirement is the blue 65.6 mV curve. The intersection of this curve with the 90 % horizontal occurs at approximately 6.8 µs so we can say that the circuit under test can operate at a minimum voltage of 65.6 mV at a minimum delay of 6.8 µs.

3.3.3 Power and Energy Consumption

Power can be broken down into two components, static and dynamic. The static power, or leakage, is the power the circuit consumes when the circuits outputs are not changing. It was not measured in this thesis. The dynamic power is the power consumed when the outputs of the circuit are switching. Both measurements are the product of the supply voltage and the average current through the circuit under test, this is shown in Equation 3.1.

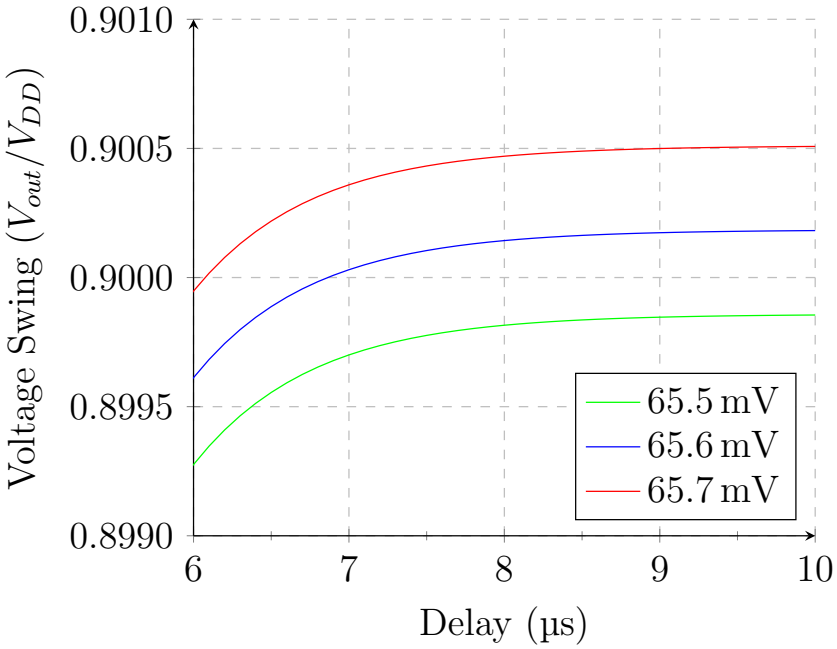

Figure 3.4: Voltage Swing vs Delay

To measure only the dynamic power the test bench needs to be set up in such a way that the output is always switching and the period needs to be set such that the output is transitioning over the entire period. This is easily setup as this is the minimum delay measurement that is already known from the delay figure of merit.

$$P = \mathrm{V} \times avg(I)(\mathrm{W}) \tag{3.1}$$

Power is calculated using the static supply voltage and the average current and is thus independent of the delay. It is understood that as the voltage is decreased the power will linearly decrease but the delay will exponentially increase. The circuits in this thesis are tested at the lowest limits of supply voltage where the delay starts to become the dominant factor for energy.

Power delay product, PDP, is simply the product of the power and a delay measurement, shown in Equation 3.2. The power measurements from above are all measured at a voltage with the minimum delay figure of merit so these two parameters are used to calculate the PDP. This means the PDP figure of merit is the energy consumed during one transition of the output.

$$PDP = P \times Delay(\mathrm{J}) \tag{3.2}$$

An example of power and energy measurements are shown in Figure 3.5. The axis on the left is used for power and the axis on the right for energy. In this example the power decreases with decreasing supply voltage, this is what we expect as the power equation has a linear relationship with voltage. The energy measurement decreases with decreasing supply voltage until approximately 70 mV, this is the minimum energy point of the circuit. After this point the energy starts to increase rapidly. This is the point where the delay starts to increase exponentially and becomes the dominant factor in PDP .

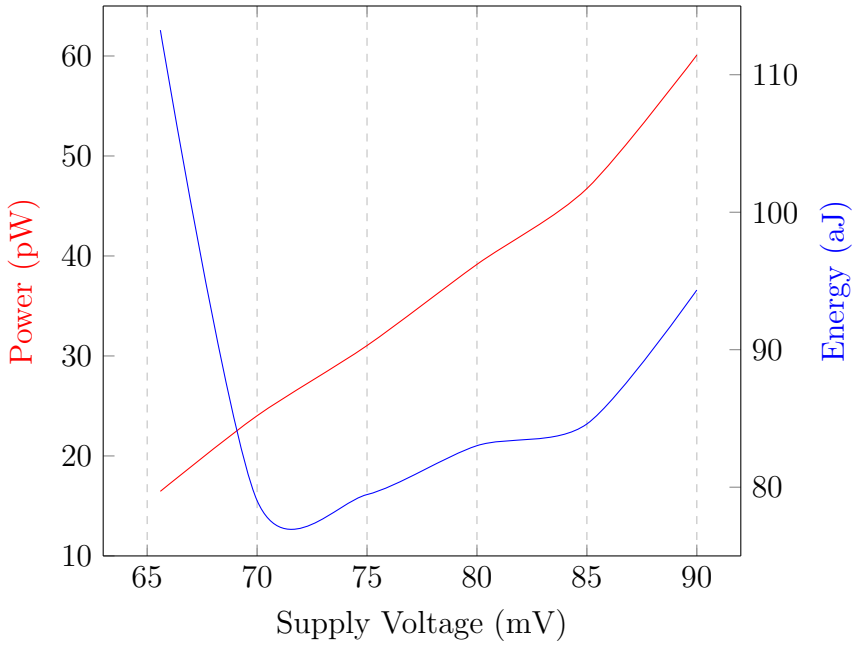

Figure 3.5: Power and Energy vs Supply Voltage Example

3.3.4 Performance at Increased Inputs

Performance at increased inputs looks to compare the performance of the logic circuits under test across each of the figures of merit previously discussed in this chapter for logic gates implemented with three inputs. The theory behind the structure of the logic circuit proposed in this thesis is that the reduced stack height should have some trade-offs for

two input implementations but as the number of inputs is increased and traditional logic structures stack height increases linearly but the proposed logic maintains stack height of one. This should have noticeable performance benefits. The data gathered will provide a basic understanding of the change with increased inputs and can be used to extrapolate a trend that can determine a break-even point where the newly proposed circuit performs better than the other logic circuits tested.

Chapter 4

Logic Circuits Design and Simulation

This chapter is an overview of the logic circuits that are tested. The static CMOS, DCVSL and a modified implementation of the DCVSL circuit are the logic styles discussed. To better understand the effects of stack height only simple logic functions are implemented, this includes OR, NOR, AND and NAND implementations. Additionally, knowing that logic functions can be broken down into NAND-NAND or NOR-NOR logic, the NAND and NOR implementations were simulated for the single ended static CMOS logic style. For the differential circuits, either AND/NAND or OR/NOR could be implemented however to obtain one from the other is simply an inversion of all of the inputs and the performance of the circuits would be identical. Because of this it was arbitrarily chosen to implement the OR/NOR logic.

For each circuit an explanation of the operation, design methodology, optimized design, optimized design for larger fan in, and simulation results are presented. The explanation of the operation will be a logic level discussion of how the devices function, highlighting the important transitions. The design methodology discusses the process that was used to arrive at the optimized circuit designs. The extension for larger fan-in is a discussion of how the two input circuits can be extended to three or more input circuits highlighting any differences in the design methodology for the two input circuits.The optimized design discusses the finalized parameters of the logic circuits that have been selected for the best low voltage performance.

4.1 Inverter

The simplest CMOS logic device is the inverter. The inverter schematic is shown in the Figure 4.1. Implemented with only two transistors, one PMOS M_0 and one NMOS M_1, the inverter has a stack height of one. The inverter is used to set a benchmark performance for delay, minimum operating voltage and power that the other logic circuits can be compared against.

The inverter circuit is simulated in a test bench circuit similar to the one discussed in chapter 3. The difference is the test bench for the inverter does not include a buffer stage and only requires the use of one input.

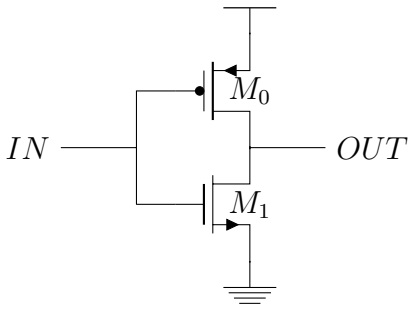

Figure 4.1: Inverter

A modification can be made to the inverter so that it is implemented with two NMOS devices and two PMOS devices. The implementation of this modified circuit is shown in Figure 4.2. This implementation can give a better understanding of the effects of stack height in the technology kit used.

4.1.1 Circuit Operation

The inverter circuits in Figure 4.1 and Figure 4.2 are the only circuits simulated that have only one input. This means that the only two possible inputs are high and low. Specifically for the inverter in Figure 4.1, When the input is high, transistor M_0 is off and M_1 is on, this creates a path from the output to ground and the output is pulled low. Alternatively when the input is low, transistor M_0 is on and M_1 is off, this creates a path from the supply voltage to the output and the output is pulled high.

This is the same for the circuit it Figure 4.2 except both transistors M_0 and M_1 are on when input is low and both M_2 and M_3 are off. Transistors M_0 and M_1 are off when input is low and both M_2 and M_3 are on.

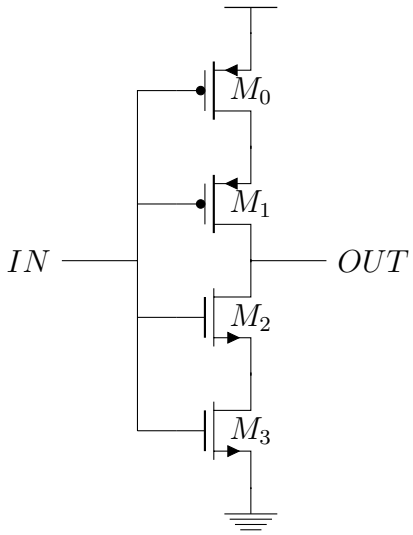

Figure 4.2: Doubled Inverter

4.1.2 Design Methodology

The parameters available to the designer are limited to the size of the devices. Knowing that the NMOS devices have better drive strength than the PMOS, the design methodology is to sweep the PMOS width while the NMOS devices are minimum sized. This determines the width at which the propagation delays, t_pHL and t_pLH, of the inverter are balanced. As mentioned in the figure of merit section, the optimal size will change depending on the supply voltage which is why when the measurements are made and the average of t_pHL and t_pLH, t_p is used.

4.1.3 Optimized Design

Figure 4.3 shows the optimal PMOS width to balance the propagation delays. As the voltage is scaled down the optimal PMOS width increases from approximately 406 nm at 120 mV to 412 nm at 65 mV. This variation of approximately 6 nm is considered to be negligible and will not significanltly impact the t_p. The optimal value was chosen in the middle of this range and rounded to the nearest 5 nm which resulted in an optimal PMOS width of 410 nm at an NMOS width of 200 nm. The inverters used as buffers in the test benches are sized according to these results as well.

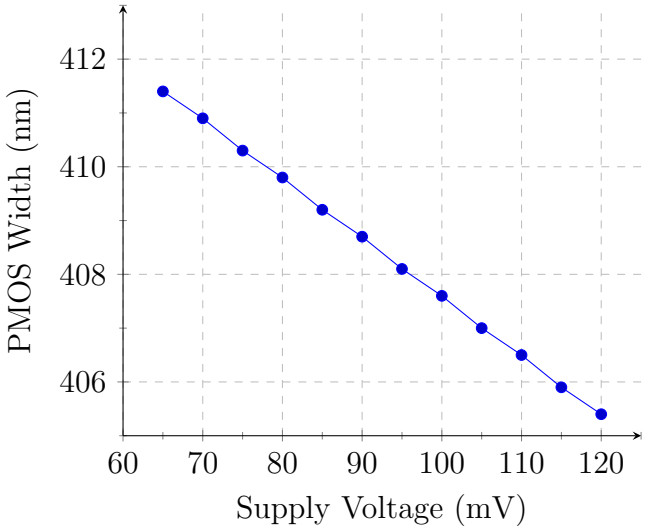

Figure 4.3: PMOS Width for Balanced
Voltage Swing Across Range of Supply Voltage

4.1.4 Simulation Results

The simulation results for the inverter are summarized in Table 4.1. The data shows that the minimum operating voltage is 65.6 mV at a minimum delay of 6.13 µs and minimum power of 17 pW. The delay ranged from 0.76 µs at 120 mV to 6.13 µs at the minimum operating voltage. The PDP decreased until around 70 mV and then increases sharply at the minimum operating voltage. The minimum energy point does not occur at the minimum operating voltage.

The simulation results for the inverter with stack height two are summarized in Table 4.2. The minimum operating voltage is 65.9 mV at a delay of 15.77 µs and a minimum power of 8.4 pW. The minimum PDP occurs at 70 mV and 75 mV,

4.1.5 Comparison of Inverter Circuits

When comparing the results of the two inverter circuits, one with stack height of one and the other stack height of two, the largest differences in performance are in the delay figure of merit and not as much in the minimum operating voltage. The difference in minimum operating voltages was only 0.3 mV. However, the difference in delay is more significant, a

Table 4.1: Simulation Results for Inverter Circuit

V_{DD} (mV)	Delay (µs)	Power (pW)	PDP (aJ)
65.6	6.13	17.0	104.1
70.0	3.25	24.1	78.5
75.0	2.53	31.2	78.9
80.0	2.10	39.3	82.6
85.0	1.80	48.9	87.9
90.0	1.56	60.3	94.0
95.0	1.37	73.7	100.9
100.0	1.21	89.6	108.5
105.0	1.07	108.8	116.4
110.0	0.95	131.4	124.8
115.0	0.85	158.0	134.3
120.0	0.76	189.5	144.0

difference of 8.89 µs. This is 2.3 × larger delay, which is roughly what would be expected as the drive strength of the circuit would be approximately half.

The graphical representation of the delay data is shown in Figure 4.4, this plot shows both inverter circuits on the same plot, the inverter with stack height two is labeled as "Inverter SH2". The data follows the exponential behavior that is expected as supply voltage is reduced.

Table 4.2: Simulation Results for Inverter with Stack Height Two

V_{DD} (mV)	Delay (µs)	Power (pW)	PDP (aJ)
65.9	13.45	8.4	113.1
70.0	6.88	11.9	82.1
75.0	5.32	15.4	82.1
80.0	4.41	19.5	85.8
85.0	3.76	24.2	91.0
90.0	3.26	29.8	97.1
95.0	2.85	36.5	104.0
100.0	2.51	44.4	111.5
105.0	2.23	53.7	119.8
110.0	1.98	64.8	128.4
115.0	1.77	77.9	137.8
120.0	1.58	93.3	147.5

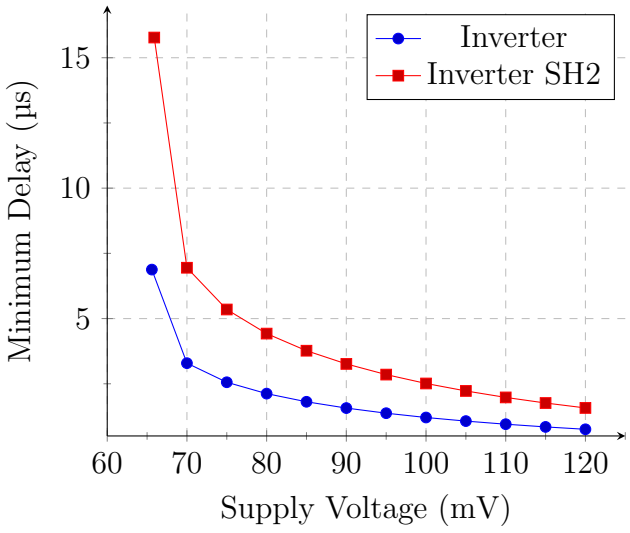

Figure 4.4: Minimum Delay vs Supply Voltage for Inverter and Inverter Stack Height Two

4.2 Static CMOS

Static CMOS logic is a common and basic logic family. The logic that is implemented in NMOS devices is complemented using De Morgan's and that function is implemented in PMOS. Static CMOS implements AND, OR, NAND, and NOR logic with only four transistors, each of these four gates are shown in Figure 4.5 and 4.6. From the figures it can be seen that the NOR gate and AND gate share the same schematic with the only difference being that the AND gate has all of the inputs inverted relative to the NOR gate. Similarly the NAND gate and OR gate share the same schematic with the only difference being the OR gate having its inputs inverted relative to the NAND gate. The simulation results for the NOR and NAND gate would be identical as would the results for the OR and AND gate as the orientation of the inputs has no effect on the performance of the circuit.

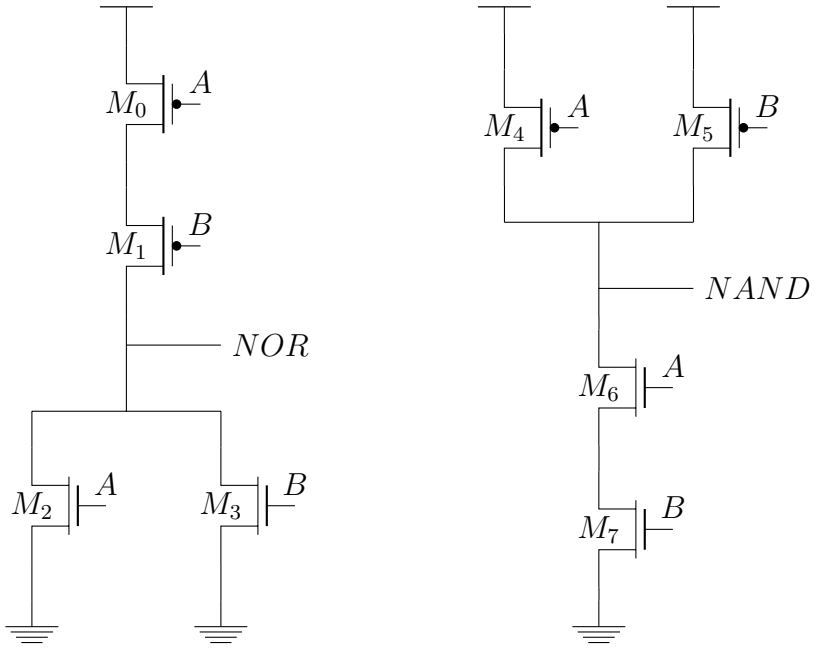

Figure 4.5: CMOS NOR and NAND Logic

The biggest difference in implementation is the distribution of stack height. In the NAND circuit the stack height of the NMOS devices is two and the stack height of the PMOS devices is only one. This is the opposite for the NOR circuit. Knowing that the drive strength of PMOS devices are typically less than that of NMOS devices it is more important to keep the PMOS stack height to a minimum so if a designer had the choice

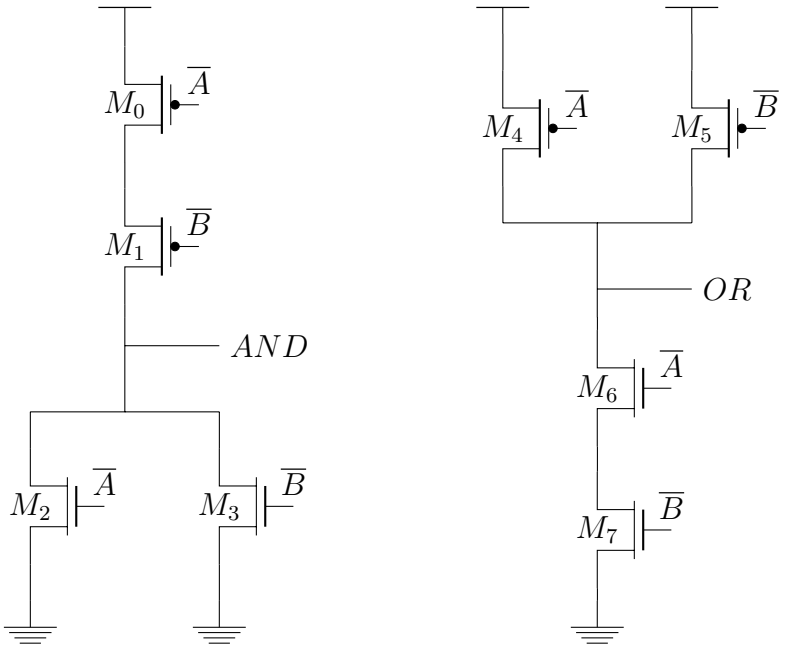

Figure 4.6: CMOS AND and OR Logic

they would implement the logic as NAND-NAND but for a better understanding both implementations will be analyzed.

4.2.1 Circuit Operation

For NOR logic, the critical path is the PMOS stack height of two consisting of transistors $M0$ and $M1$. Only when these two devices are on will the output be non-zero. In order for that to happen the input A and B must be low. For any input vector with either A or B high, either $M2$ or $M3$ will be on and pull the output low. Alternatively for the NAND implementation, the NMOS devices $M6$ and $M7$ are the critical path. The only input vector that will pull NAND output low is when A and B are both high and transistors $M6$ and $M7$ are both on.

4.2.2 Design Methodology

The design methodology for static CMOS is very similar to the design methodology for the inverter. The goal is to find the device ratio such that the current when the PMOS

branch is on is balanced to match the current when the NMOS branch is on which, this will result in balanced propagation delays. The ratio determined for the inverter is used as a starting point and the branch with stack height of two is varied to determine the point where the delays balance.

4.2.3 Extension for Larger Fan-in Circuits

The same design methodology was used to implement the three input NAND and NOR gates. The branch with the increased stack height is sized up proportionally to the increased number of inputs, 3/2 larger, and then again the width is swept around this value to narrow in on the optimal width.

For improved performance the design could implement a progressive stack height where the devices in the stack increase in size as the devices are further from the output and closer to either the supply voltage or ground. For simplicity this was not implemented in this thesis.

4.2.4 Optimized Design

A sweep of the PMOS width determined that the optimized sizing for the two input NOR gate is 900 nm PMOS width and minimum sized 200 nm NMOS devices. Increased to a three input NOR gate, the optimized design is 1350 nm PMOS and 200 nm NMOS.

The optimized sizing for the two input NAND gate is 410 nm PMOS width and 625 nm NMOS width. The three input NAND gate is 410 nm PMOS width and 920 nm NMOS width. Again as the PMOS stack height is increased from two to three the optimal PMOS size for three input is approximately 3/2 as big.

4.2.5 Simulation Results

The simulation results for the two input NOR circuit are summarized in Table 4.3. The circuit is able to satisfy the operational criteria at a minimum voltage of 89.7 mV with an associated delay of 4.98 µs. At the minimum voltage the power was 53.7 pW. The minimum PDP of 167.94 aJ occurs at 100 mV.

The simulation results for the two input NAND circuit are summarized in Table 4.4. The circuit is able to satisfy the operational criteria at a minimum voltage of 89.4 mV with

Table 4.3: Simulation Results for Two Input CMOS NOR

V_{DD} (mV)	Delay (µs)	Power (pW)	PDP (aJ)
89.7	4.98	53.7	267.3
90.0	3.84	57.5	220.8
95.0	2.25	76.3	171.6
100.0	1.80	93.3	167.9
105.0	1.51	112.6	170.0
110.0	1.30	134.9	175.4
115.0	1.13	161.1	182.0
120.0	0.99	191.8	189.9

an associated delay of 4.15 µs with a minimum power of 54.9 pW. The minimum PDP of 159.06 aJ occurs at 100 mV.

Table 4.4: Simulation Results for Two Input CMOS NAND

V_{DD} (mV)	Delay (µs)	Power (pW)	PDP (aJ)
89.4	4.15	54.9	227.9
90.0	3.32	58.9	195.7
95.0	2.13	76.2	162.3
100.0	1.71	93.0	159.1
105.0	1.44	112.1	161.4
110.0	1.24	134.1	166.3
115.0	1.07	160.5	171.7
120.0	0.94	190.8	179.4

The simulation results for the three input NOR circuit are summarized in Table 4.5. The circuit is able to satisfy the operational criteria at a minimum voltage of 101.1 mV with an associated delay of 3.78 µs with a minimum power of 99.2 pW. The minimum PDP of 258.4 aJ occurs at 110 mV.

The simulation results for the three input NAND circuit are summarized in Table 4.6. The circuit is able to meet the operational criteria at a voltage of 101.4 mV with an associated delay of 3.83 µs with a minimum power of 95.2 pW. The minimum PDP of 225.8 aJ occurs at 115 mV.

The increase in number of inputs saw a sizable decrease in minimum operating voltage. Both NAND and NOR implementations saw in increase in minimum operating voltage of approximately 11 mV.

Table 4.5: Simulation Results for Three Input CMOS NOR

V_{DD} (mV)	Delay (µs)	Power (pW)	PDP (aJ)
101.1	3.78	99.2	374.8
105.0	2.15	126.2	271.3
110.0	1.69	152.9	258.4
115.0	1.42	182.1	258.6
120.0	1.22	215.6	263.0

Table 4.6: Simulation Results for Three Input CMOS NAND

V_{DD} (mV)	Delay (µs)	Power (pW)	PDP (aJ)
101.4	3.83	95.2	364.7
105.0	1.99	121.5	241.8
110.0	1.55	147.0	227.9
115.0	1.29	175.0	225.8
120.0	1.11	206.5	229.2

4.3 Differential Cascode Voltage Switch Logic

Differential cascode voltage switch logic (DCVSL) is a logic family that uses cross-coupled logic to provide a differential logic gate. The differential nomenclature of DCVSL means that it is a two output logic circuit where one output is non-inverted and the other is inverted. This is achieved by using only NMOS devices in the same configuration as static CMOS logic, described in the section above, and then using a PMOS device above each stack which is cross-coupled with the outputs. This allows for a logic gate that is able to compute both NOR/OR or NAND/AND with only six devices. If the output is to be OR and NOR, we used the NMOS devices from the static CMOS OR gate and NOR gate, in this case two series NMOS devices with $\overline{A}$ $\overline{B}$ as inputs and two parallel NMOS devices with inputs A B. The outputs are cross-coupled to corresponding PMOS devices. The DCVSL implementation of NOR/OR gate is shown in Figure 4.7. To implement the NAND/AND circuit follow the same procedure and it can be shown that this is done by simply inverting all of the inputs. The NOR/OR implementation is shown in Figure 4.7.

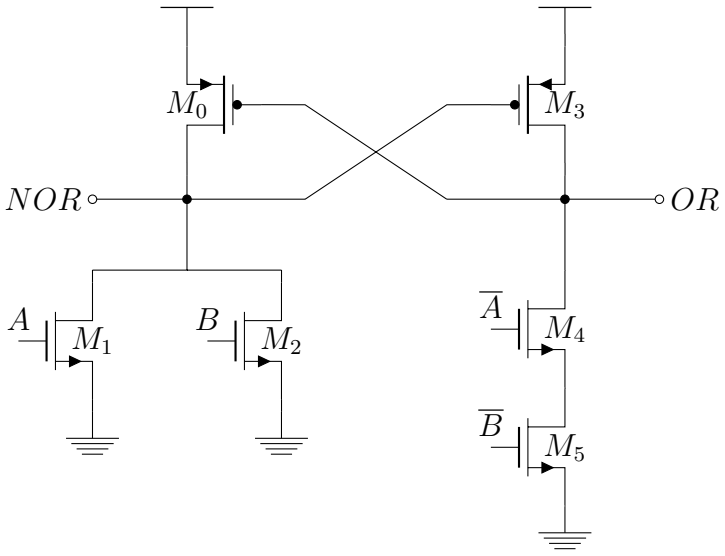

Figure 4.7: DCVSL NOR OR Gate

4.3.1 Circuit Operation

The two states of this circuit are when A and B are low or either A or B are high. In the first case, when A and B are low, the transistors M_1 and M_2 are off and transistors M_4 and M_5 are on. M_4 and M_5 create a path to ground and node OR is pulled low. This will turn on transistor M_0 pulling NOR high, which ensures that M_3 is off. This is the latching behavior that enables DCVSL to implement all logic in NMOS devices. The second case is when either A or B are high. If we assume only A is high, transistor M_1 will be on and the path from NOR to ground will be pulled low. This node is also connected to transistor M_3 and will turn on the device pulling output OR high. This turns off transistor M_0 and completes the latching.

4.3.2 Design Methodology

The design methodology for the DCVSL circuit is more involved than that of the CMOS circuits. The critical path for the circuit is the transition when transistors M_4 and M_5 turn on an the output OR is pulled low and NOR pulled high. This is again because the stack height in the OR NMOS branch is two and the drive strength will be less than that of the NOR NMOS devices. The additional complexity comes from the PMOS devices as that are still required to transition the opposing output. The PMOS sizing used in the inverter,

410 nm as well as leaving the NMOS devices minimum sized is good staring sizing. Varying each of the transistors around that size will give an understanding as to the impact on each outputs propagation delay both low to high and high to low. An iterative process is then used to sweep individual device parameters until an optimal point is found.

4.3.3 Extension for Larger Fan-in Circuits

The design methodology for three input designs uses the sizing used in the two input implementation as a starting point. The only change to the schematic is the introduction of an additional NMOS device in the horizontal stack in the NOR branch and an additional NMOS in the vertical stack of the OR branch. These devices should be immediately sized up and then again an iterative process is used to find the optimal sizing.

4.3.4 Optimized Design

The optimized design for the two input DCVSL circuit is as follows. Transistor M_0 have a width of 630 nm. The NOR NMOS transistors M_1 and M_2 have a width of 200 nm. The OR PMOS device M_3 have a width of 300 nm. The OR NMOS devices M_4 and M_5 have a width of 225 nm. For the three input device, the OR NMOS devices width is increased to 560 nm and the NOR PMOS device width is increased to 800 nm.

4.3.5 Simulation Results

The simulation results for the DCVSL circuit are summarized in Table 4.7. The circuit is able to meet the operational criteria at a minimum voltage of 84.6 mV with an delay of 10.84 µs. At the minimum voltage the power was 72.4 pW. The PDP minimum of 604.3 aJ occurs at 90 mV.

The simulation results for the three input DCVSL circuit are summarized in Table 4.8. The circuit is able to meet the operational criteria at a minimum voltage of 89.9 mV with an delay of 9.7 µs. At the minimum voltage the power was 109.2 pW. The PDP minimum of 737.9 aJ occurs at 100 mV.

The difference in the two input to three input DCVSL circuit showed an increased minimum operating voltage of approximately 5 mV.

Table 4.7: Simulation Results for Two Input DCVSL

V_{DD} (mV)	Delay (µs)	Power (pW)	PDP (aJ)
84.6	10.84	72.4	784.6
85.0	9.39	76.0	713.9
90.0	6.07	99.5	604.3
95.0	4.97	122.0	606.0
100.0	4.25	147.9	628.4
105.0	3.71	178.0	659.8
110.0	3.28	213.4	699.1
115.0	2.92	254.9	743.6
120.0	2.61	303.4	792.4

Table 4.8: Simulation Results for Three Input DCVSL

V_{DD} (mV)	Delay (µs)	Power (pW)	PDP (aJ)
89.9	9.70	109.2	1058.8
90.0	8.65	112.4	972.3
95.0	4.98	148.4	739.0
100.0	4.12	179.1	737.9
105.0	3.56	214.1	762.2
110.0	3.14	254.6	799.4
115.0	2.81	301.3	846.7
120.0	2.53	355.8	900.2

4.4 MOD-DCVSL

The circuit presented in this thesis is a modified DCVSL circuit. The theory is that DCVSL has advantages over static CMOS and this can be improved upon further by being able to implement a DCVSL circuit with a stack height of one. Starting with the DCVSL circuit in Figure 4.7, De Morgan's is applied to the NMOS devices in the NOR branch. This process is shown in Equations 4.1, 4.2, 4.3 and 4.4. Implementing the result of Equation 4.4 will result in the circuit shown in Figure 4.8.

$$\overline{(\overline{A} \bullet \overline{B})} \tag{4.1}$$

$$Sub\ \overline{A} = A\ and\ \overline{B} = B \tag{4.2}$$

$$\overline{(A \bullet B)} \tag{4.3}$$

$$(\overline{A} + \overline{B}) \tag{4.4}$$

The issue with the circuit in Figure 4.8 is that in its current state it is not able to fully function. If the input vector is $A = 0$ and $B = 0$ transistor M_1, M_2, M_3 and M_4 are all be off. In this situation the circuit has no way of transitioning the outputs. This is resolved with the use of boosting capacitors. For each input a capacitor is needed to provide a small boost to the input of transistor M_0 or M_5 to start to latch the appropriate output.

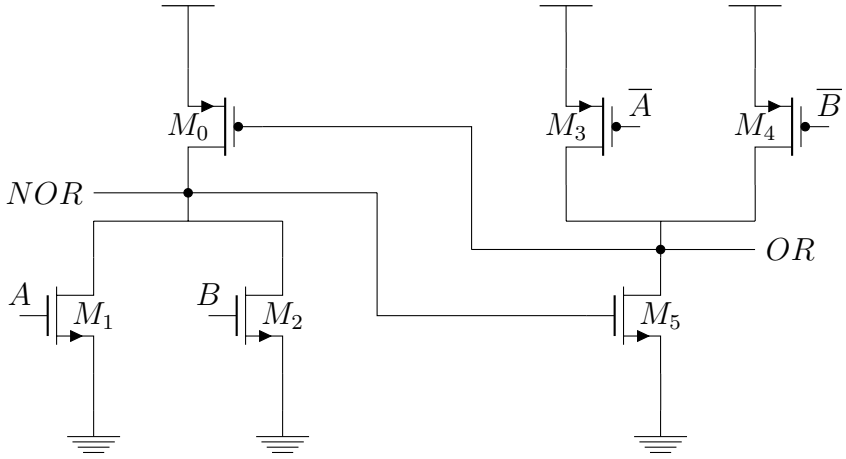

Figure 4.8: Modified DCVSL Circuit NOR OR Gate

The implementation with the boost capacitors is shown in Figure 4.9. The capacitors do not need to be connected in the exact configuration shown, it is also possible to connect both capacitors to the same output node. The input connected to the opposite node of the capacitor needs to be inverted from the inputs connected to the transistors of the same output node.

4.4.1 Circuit Operation

The modification to the DCVSL circuit makes the operation of MOD-DCVSL simpler. If either A or B are on, transistors M_1 and M_3 or M_2 and M_4 will be on, respectively, and a

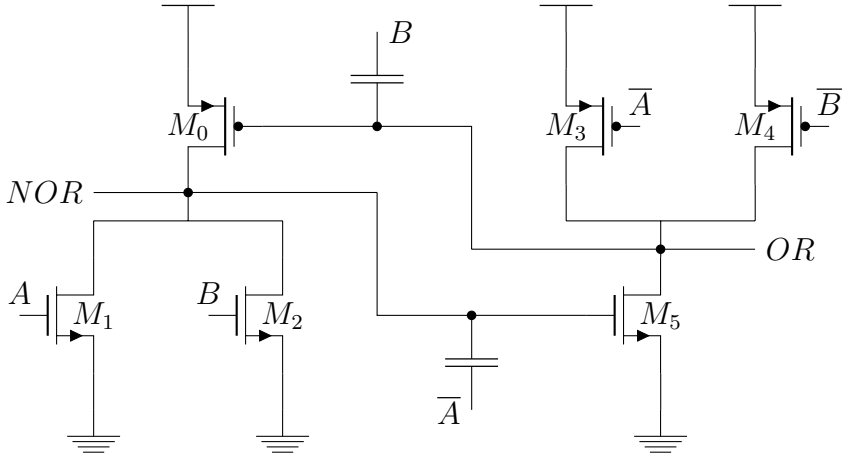

Figure 4.9: Modified DCVSL Circuit with Boost Capacitors

direct path from NOR to ground and OR to supply voltage are created. The input vector of concern is when $A = 0$ and $B = 0$ and the circuit needs to latch in the appropriate outputs. If, for example, $B = 0$ and A is transitioning from $1- > 0$ the circuit will be as shown in Figure 4.10. As the input A starts to transition to 0 the $\overline{A}$ will provide a positive boost to the input of transistor M_5 which will as a result pull the OR output low which turns on transistor M_5 and reinforces the positive NOR output.

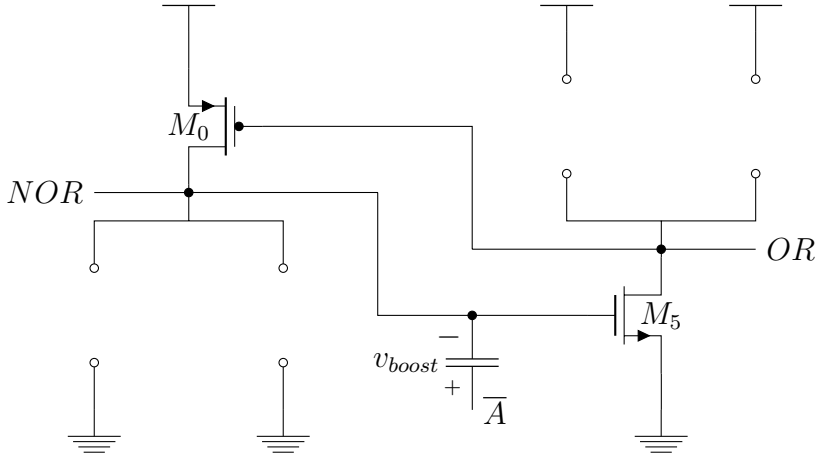

Figure 4.10: Modified DCVSL Critical Path Transition

4.4.2 Design Methodology

Although the circuit shares a lot of the design with DCVSL the design methodology differs due to the use of capacitive boosting. From the circuit operation the critical path is depicted in Figure 4.10. The transistors M_0 and M_5 are sized up. Both of these parameters are swept and the optimal point determined.

4.4.3 Extension for Larger Fan-in Circuits

A big benefit to the modified circuit is the simplicity of extending the number of inputs beyond a two input implementation. The design of MOD-DCVSL means that the circuit simply adds additional devices to the horizontal stack. For each additional input an additional boosting capacitors is required to account for the logic case where only one input transitions and results in an output change.

4.4.4 Optimized Design

The sizing that was determined to be the optimal for minimum operating voltage was such that the NOR PMOS device M_0 width is sized up to 550 nm. The OR output NMOS device M_5 width is sized to 220 nm. In the three input implementation, the optimum size has the NOR PMOS with is increased to 680 nm and the OR NMOS device is sized up to 250 nm.

4.4.5 Simulation Results

The simulation results for the MOD-DCVSL circuit are summarized in Table 4.9. The circuit is able to meet the operational criteria at a minimum voltage of 86.6 mV with an delay of 10.31 µs. At the minimum voltage the power is also at a minimum of 71.2 pW. The PDP minimum of 599.0 aJ occurs at 95 mV.

The simulation results for the MOD-DCVSL circuit are summarized in Table 4.9. The circuit is able to meet the operational criteria at a minimum voltage of 89.8 mV with an delay of 9.04 µs. At the minimum voltage the power is also at a minimum of 98.0 pW. The PDP minimum of 741.8 aJ occurs at 95 mV.

The supply voltage where the minimum PDP for the MOD-DCVSL circuit does not change when implementing a two or three input logic circuit.

Table 4.9: Simulation Results for Two Input MOD-DCVSL

V_{DD} (mV)	Delay (µs)	Power (pW)	PDP (aJ)
86.6	10.31	71.2	733.9
90.0	7.63	80.3	612.6
95.0	6.58	91.1	599.0
100.0	5.97	102.0	608.6
105.0	5.53	113.2	625.8
110.0	5.18	125.0	647.8
115.0	4.84	137.2	664.5
120.0	4.65	150.0	697.5

Table 4.10: Simulation Results for Three Input MOD-DCVSL

V_{DD} (mV)	Delay (µs)	Power (pW)	PDP (aJ)
89.8	9.04	98.0	885.6
90.0	8.42	99.5	838.0
95.0	6.45	115.0	741.8
100.0	5.80	128.9	747.6
105.0	5.36	143.2	767.6
110.0	5.03	158.0	794.7
115.0	4.76	173.6	826.3
120.0	4.54	189.7	861.2

Chapter 5

Comparative Analysis

This chapter compares the simulation results of the logic circuits discussed and simulated in the last chapter. Each of the circuits are compared with respect to minimum operating voltage, delay, power, and PDP.

5.1 Minimum Operating Voltage

The minimum operating voltages for each of the circuits are summarized in Table 5.1. The CMOS implementations have roughly the same minimum operating voltage. The MOD-DCVSL circuit is able to operate at a supply voltage approximately 3 mV lower than CMOS and DCVSL approximately 5 mV lower than CMOS.

This was not the expected result as it was thought that the reduced stack height of the MOD-DCVSL would offer an advantage in this specific figure of merit. Although it did not offer an advantage the cost of the implementation was only a 2 mV difference in this figure of merit.

Table 5.1: Summary of Minimum Operating Voltage

Logic Circuit	V_{MIN} (mV)
CMOS NOR	89.7
CMOS NAND	89.4
DCVSL	84.6
MOD-DCVSL	86.6

5.2 Delay

The minimum delay for each logic circuit is summarized in Figure 5.1. The delay for the CMOS NAND and NOR are comparable and are also the best performing logic circuits. The benefit to the DCVSL circuit and the MOD-DCVSL circuit are their ability to perform at lower minimum voltages.

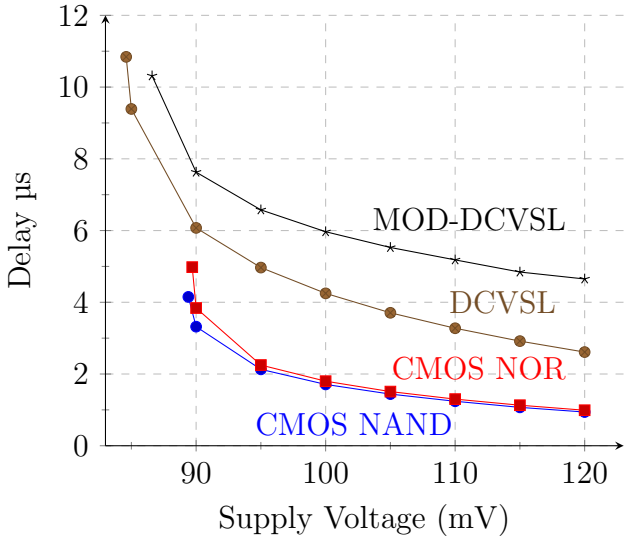

Figure 5.1: Minimum Delay vs Supply Voltage for Various Logic Families

Figure 5.1 is a comparison of the circuits where they are compared within the range of voltages where all circuit are operational and then normalized to the circuit with the minimum delay, CMOS NAND. This give a better understanding of the circuits performance. Looking at the resulting curves in Figure 5.2 the NAND NOR have very similar delay values, DCVSL is approximately three times slower and MOD-DCVSL is between three to six times slower. The interesting thing to note is that between 95 mV to 95 mV all but the MOD-DCVSL have a relatively consistent delay where as MOD-DCVSL improves with decreasing voltage. This is an interesting behavior of the circuit.

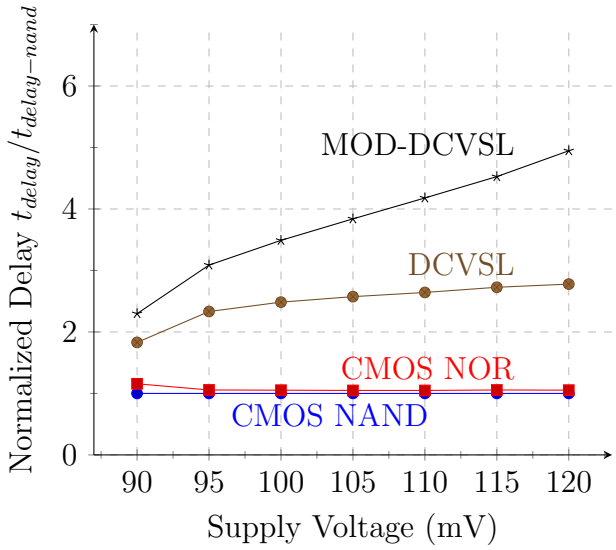

Figure 5.2: Normalized Delay

5.3 Power

The comparison of the power consumption for the two input circuits is shown in Figure 5.3. The CMOS NAND and NOR implementations have very similar power consumption with almost no visual difference on the plot. This is due to the design methodology. Because the initial sizing for the CMOS was the balanced inverter all branches of CMOS NAND and NOR are balanced to match that of the inverter. The result is very similar delay, as shown in the previous section, and very similar power, as can be seen in Figure 5.3.

DCVSL has the largest power consumption and follows a similar trend to the CMOS circuits. It consumes about 50% more power than the CMOS implementations. This is what would be expected of a differential circuit that is implemented with more transistors.

Interestingly the curve for MOD-DCVSL does not have a similar shape as the other logic styles, the slope of the curve is much shallower and appears to be more linear. MOD-DCVSL has lower power consumption than DCVSL for the entire range of data and above about 105 mV it has lower power consumption than the CMOS implementations.

A summary of the PDP is shown in Figure 5.4. As is expected, due to the similar delay and power measurements, the CMOS NAND and NOR have very similar PDP. PDP highlights the trade-offs that are made with the use of a differential implementation. Both DCVSL and MOD-DCVSL have significantly higher PDP effected by both higher

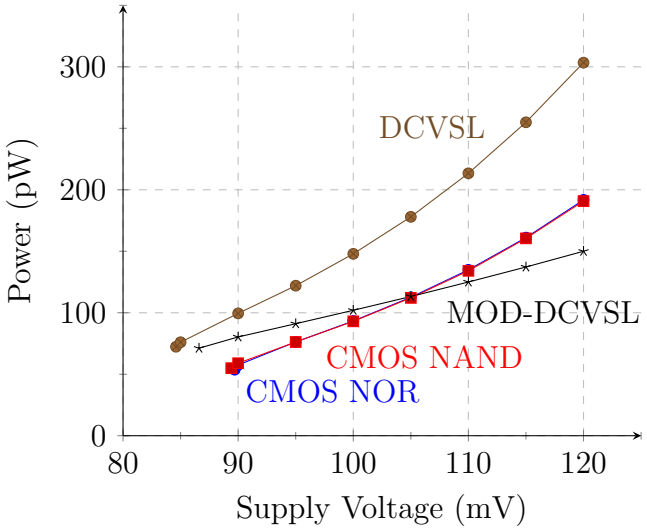

Figure 5.3: Comparison of Power Consumption

power consumption and significantly larger delay.

When comparing between just DCVSL and MOD-DCVSL, they exhibit similar PDP measurements. The MOD-DCVSL does offer a lower PDP above approximately 95 mV and larger delay below 90 mV.

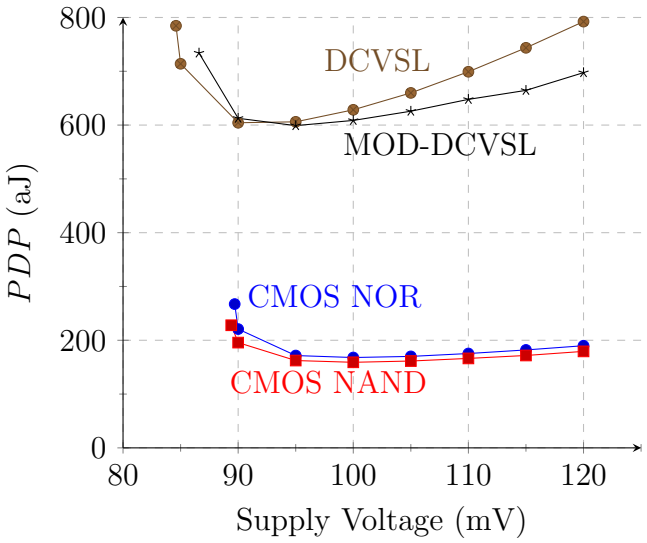

Figure 5.4: Comparison of PDP

5.4 Increased Number of Inputs

This section is a comparison of the three input implementations of the logic circuits for minimum operating voltage, delay, and power. Additionally each individual logic circuit is measured on percentage change from the two input to three input implementations.

5.4.1 Minimum Operating Voltage

The change in minimum operating voltage is shown in Figure 5.5. This plot shows that both the NAND and NOR CMOS implementations are very similar in minimum operating voltage and both have approximately the same rate of change in minimum operating voltage as the inputs are increased from two to three. DCVSL has the next lowest rate of change and as the inputs are increased to three the minimum operating voltage is very comparable to the MOD-DCVSL. The MOD-DCVSL has the lowest rate of change, this is expected as the modification to the circuit is horizontal rather than vertical as with the other logic circuits compared in this thesis. The low rate of change means that the MOD-DCVSL is able to match DCVSL at a three input implementation. From this the conclusion can be made that for inputs of three the MOD-DCVSL is comparable to DCVSL and for inputs greater than three, the MOD-DCVSL would be able to achieve a lower minimum operating voltage.

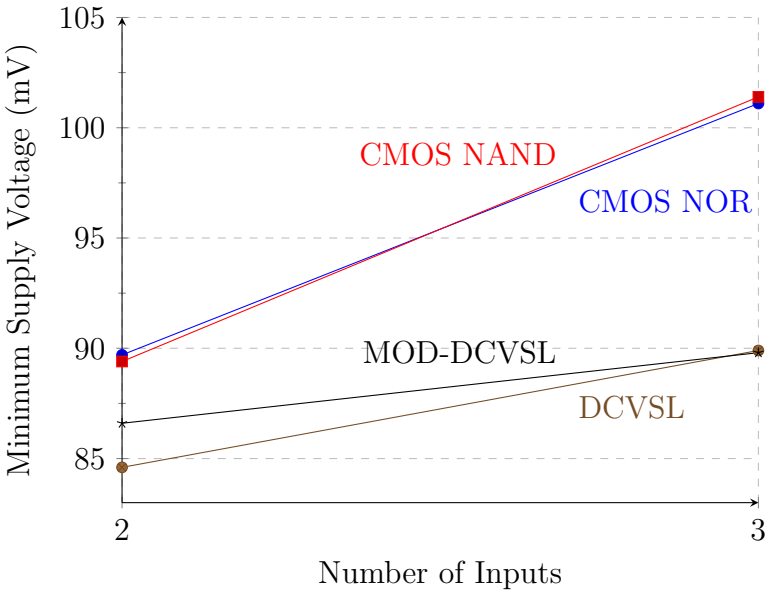

Figure 5.5: Change in Minimum Operating Voltage with Number of Inputs

5.4.2 Minimum Delay

The delay data for the three input logic circuits is shown in Figure 5.6. As was determined the minimum operating voltage for the static CMOS was a higher minimum and the effect on delay is that the delay starts to increase exponentially at this higher supply voltage. The delay at this minimum voltage is comparable to the delay of DCVSL. The MOD-DCVSL has a larger delay over almost the entire range of voltage, at the minimum operating voltage the MOD-DCVSL has a delay that is minimally lower than that of DCVSL.

The difference in the delay for the three input over the two input implementation is shown in Figure 5.7. This figure shows how each of the circuits delay is effected by increasing the number of inputs. This shows how both DCVSL and MOD-DCVSL delay are not as effected by the increase in delay. The CMOS NAND and NOR circuits have a larger increase in delay, between approximately 20 % to 40 % larger delay in the three input implementation.

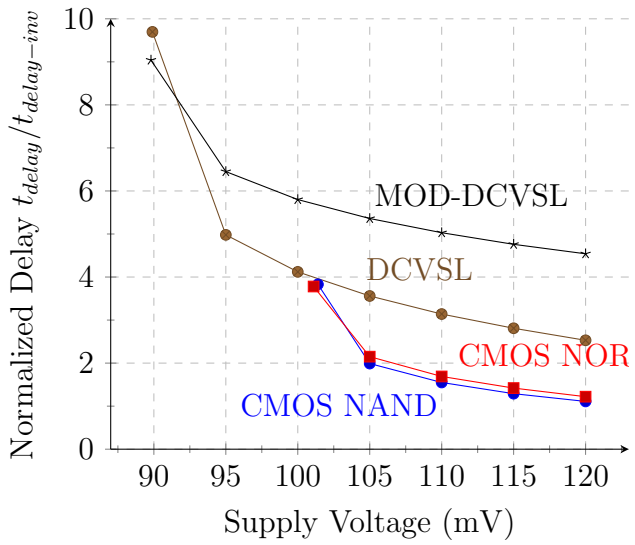

Figure 5.6: Comparison of Three Input Delay

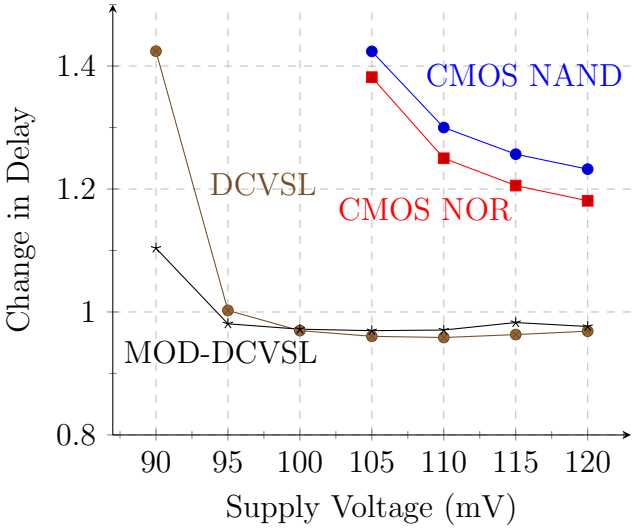

Figure 5.7: Change in Delay From Two Input to Three Input

5.4.3 Power

The power consumption data for the three input implementation is shown in Figure 5.8. The results for the three input circuits do not show a significant difference from the observations made for the two input implementation. Again DCVSL has the largest power consumption. MOD-DCVSL has comparable power to CMOS NOR and NAND with a shallower slope.

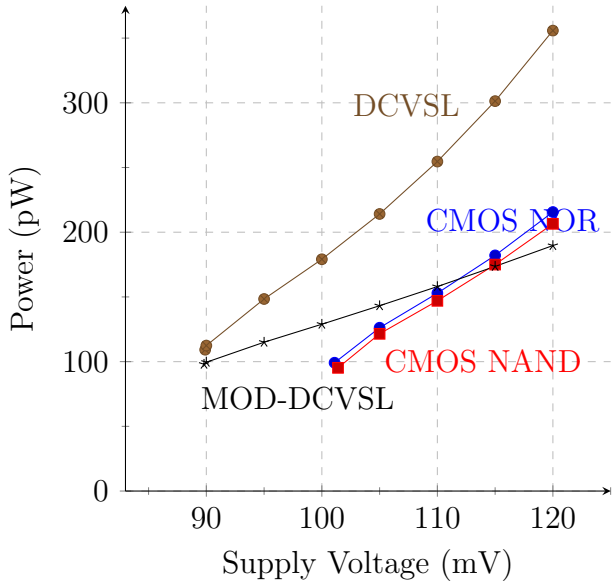

Figure 5.8: Three Input Power Consumption

The PDP data for the three input implementations are shown in Figure 5.9. The figure shows that again CMOS is a better performing implementation. Comparing DCVSL and MOD-DCVSL it can be seen that in the three input implementation the MOD-DCVSL has a lower PDP or comparable PDP to DCVSL across the whole range of supply voltages.

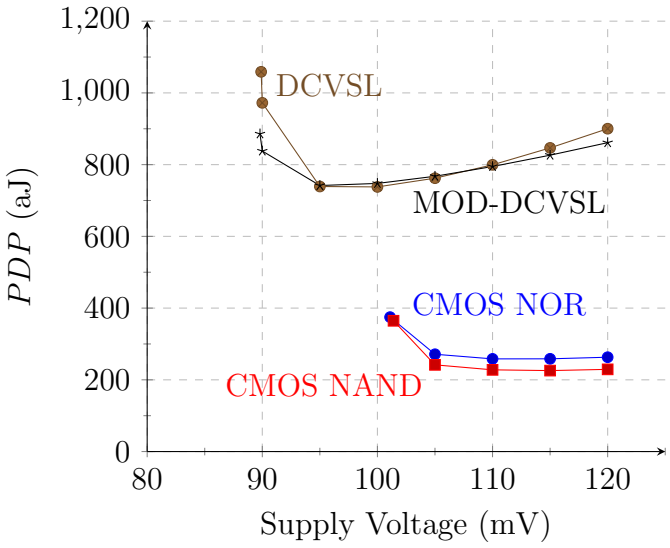

Figure 5.9: Comparison of Three Input PDP

Chapter 6

Conclusion

In this thesis static CMOS was able to demonstrate the lowest overall power consumption, delay, and PDP but was not able to operate at as low a minimum operating voltage as either DCVSL or MOD-DCVSL. This is mostly due to the simplicity of the single ended static CMOS circuits which are implemented with at least half the number of transistors as the differential logic circuits. Static CMOS is however affected by number of inputs, increasing from two to three inputs resulted in an increase in delay of around 20-30% for supply voltage range of 90 mV to 120 mV and an increase of minimum operating voltage of around 10%. It is not entirely justified to compare CMOS to the differential circuits in this thesis as the differential circuits have additional benefits that are not easily quantified in a simulation environment. The most obvious benefit is that a differential implementation has two outputs which provide common mode noise rejection which becomes an increasingly important issue when designing in the sub-threshold voltages range.

Comparing the differential implementations more closely, the two input implementations for MOD-DCVSL and DCVSL are very similar in all metrics measured. The minimum operating voltages are 86.6mV and 84.6mV respectively, only a 2mV variation. The minimum power of MOD-DCVSL was lower than DCVSL with power measurements of 71.2pW and 72.4pW respectively. The minimum power delay product for MOD-DCVSL was 599aJ occurring at a supply voltage of 95mV where DCVSL minimum power delay product was 604aJ occurring at 90mV, a negligible difference. The advantage of the modifications made to DCVSL to obtain MOD-DCVSL become more apparent when comparing the three input implementations, specifically at low supply voltages. The minimum operating voltages for the three input implementations for MOD-DCVSL and DCVSL are 89.8mV and 89.9mV respectively. The 2mV advantage that DCVSL has over MOD-DCVSL for the two input implementations is reduced to a negligible 0.1mV. MOD-DCVSL does have lower delay and

power compared to DCVSL at the minimum operating voltage with delay of 9.04us and 9.7us respectively and power of 98pW and 109.2pW respectively. Extrapolating beyond three inputs would suggest that MOD-DCVSL would be able to operate at lower minimum operating voltages at lower power consumption compared to DCVSL.

An unexpected outcome of this thesis was the effect that supply voltage has on power consumption of the new circuit. The other logic circuits simulated all displayed more of a squared relationship with supply voltage but MOD-DCVSL displayed a linear relationship. This suggests that at larger supply voltages, beyond the supply voltage range tested in this thesis, the power consumption could be significantly less.

The results in this thesis suggest that the modification made to DCVSL to obtain MOD-DCVSL do offer interesting performance benefits and trade-offs. Future research into possible improvements in delay through the use of more complex boosting circuitry may be able to add more value to the design. Although it was not the original intention, MOD-DCVSL showed potential at the upper limit of the range of voltages studied in this thesis and additional research into the performance at larger voltages may also yield positive results. The fabrication of a physical test chip would be useful in understanding the circuit.

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