A Comparative Analysis of 6T and 10T SRAM Cells
for Sub-threshold Operation
in 65nm CMOS Technology

by

Seyed-Rambod Hosseini-Salekdeh

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Abstract

The aggressive approach of the integrated electronics industry towards scaling and the growing trend of low-power applications have led to major research interest in ultra-low power integrated circuits. One of the integrated circuit areas most affected by this revolution is computer memory. In this thesis, a 10-Transistor Static Random Access Memory is compared to a 6-Transistor Static Random Access Memory in the subthreshold region of operation for a 65nm technology node. This comparison focuses primarily on the stability of memory cells in performing read and write operations. The use of 3-dimentional graphs in this thesis is to better compare differences and to give a feedback to memory designers about the design possibilities. A low-power Write Margin improvement method is proposed for the 10-Transistor cell to bring its stability to a standard comparable to that of its 6-transistor counterpart.

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Chapter 1

Introduction

Since the 1960s, the price of one-bit semiconductor memory has dropped hugely, and this trend continues. The resulting constant drop in the price of semiconductor devices has increased their application and affected the human society to the point where electronics and computer devices are now essential for human activities and the development of civilization. The main reason for this rapid price drop is electronic miniaturization. As the building blocks of the electronic universe are now smaller, more components can be fabricated on each silicon wafer, and consequently the price of electronic components drops.

To follow "Moore's Law," which is a crisp description of the persistent periodic increase in the level of miniaturization in electronic components (made from Gordon Moore's empirical observation in the 1960s), scientists constantly try to decrease device sizing. This endless chase has led to the creation of many semiconductor technology generations, including the 180nm, 130nm, 90nm, 65nm, 45nm, 32nm, 28nm, and 22nm generations. Circuit designers using any of these technology generations always try to optimize their designs for chip real estate (area), stability, power consumption, and speed.

In today's world, with the rapid appearance and popularity of portable electronic devices, low power consumption electronics have become highly important. One of the most innovative ways of reducing chip power consumption in electronics is through the creation of sub-threshold devices and architectures. In sub-threshold operation, the supply voltage is lowered to below the threshold voltage of a transistor, thus enabling major power savings where energy is the primary constraint rather than speed. Sub-threshold operation has a lot in common with above-threshold operation but also demonstrates differences such as susceptibility to process variation and decrease in stability of the device. This thesis is intended to demonstrate the process of designing a stable sub-threshold 10-transistor device, with a focus on device stability in the 65nm technology node.

1.1 Motivation

The emerging and growing market for portable electronic devices has led the electronics designers to be more conscious of power and energy constraints in their circuit designs. Designers are forced to design more energy-aware circuits and started to develop methods and design rules to increase energy savings. In the sub-threshold region of operation, the power supply voltage of the circuit is lowered below to transistor's threshold voltage. As a consequence, its active and leakage power is reduced dramatically. However, this advance comes at the cost of circuit switching speed. One of the central areas of micro electronic design that is affected by such design methodology is memory design. This thesis compares a 10T SRAM Cell with an improved write margin to a conventional 6T SRAM Cell operated in the subthreshold region in 65nm technology node. The two SRAM cells are compared based on their Static Noise Margins, Read Currents, Leakage Currents, and Static Write Margins, while considering the effects of process variations. This comparison gives future designers an insight for future 10T cell designs.

1.2 Static Random Access Memory

Static Random Access Memory (SRAM) is a type of semiconductor memory that uses a bi-stable latching circuit to store each bit of data [1]. A Conventional SRAM cell is created with the use of six Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFET) connected in a particular fashion, as shown in Figure 1. A single SRAM cell is designed to store a single bit of data. Each bit in a SRAM is stored on four transistors connected to one another as two cross-coupled inverters. Figure 1 illustrates the crossed-coupled inverters along with two extra pass transistors that control the access to internal cell nodes. The SRAM cell has two stable states that are used to represent logic 0 and 1. The two additional access transistors control access to the SRAM cell during read and write operations.

The 6 transistor cell or 6T SRAM cell is the best known and most studied cell. There are many other SRAM cells with 4, 7, 8, 9, 10, and 11 transistors for storing a single bit. Dynamic Random Access Memory (DRAM) cells such 3T or 1T are also possible, but they store data on a capacitor as electronic charge. DRAM cells require frequent charge replenishing, and, their designs are not

suitable for SRAM-like operation. Each cell has associated benefits and drawbacks that dictate its usage. Read stability, write stability, read current, leakage current, power dissipation, and area among the usage parameters to consider in each design.

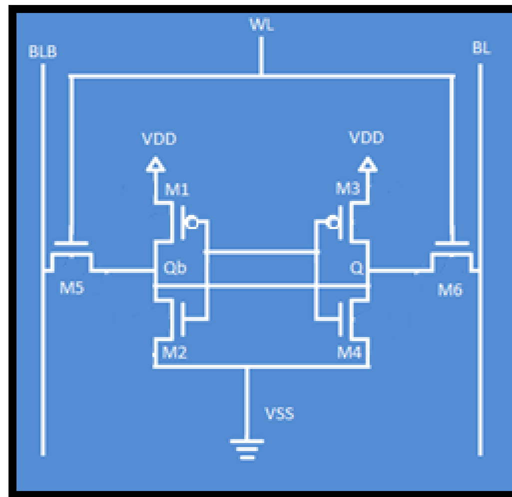

Figure 1: A Conventional 6T SRAM cell.

In the subthreshold regime, a Nano-scale SRAM cell design faces significant challenges because of reduction in noise margins and increased sensitivity to threshold voltage. The 6T SRAM cell is thus a bad choice for subthreshold designs, in terms of reliability and stability. Therefore, in this research, a differential 10-transistor SRAM design is considered and is compared to the 6T SRAM.

1.3 Subthreshold Operation

The sub-threshold regime of MOSFETs is one of the interesting topics in digital design for low-power research. In the sub-threshold region of operation, also known as the weak-inversion region, the ratio of trans-conductance to current is very high, making it a very efficient operating region, (Weak inversion formulation predicts that g_m will hit a maximum value as current density is reduced) [2]. Thus, in this region of operation gain in digital circuitry, a transistor can be in one of the two states: "on", or "off". In the "off" state, the applied Gate to Source voltage (VGS) of the MOS transistor is usually kept at 0 V to ensure that the transistor is fully switched off. However, to turn the transistor "on," the VGS is kept at a lower voltage than its threshold voltage (V_T). Of note, in the sub-threshold regime, the drain current (ID) reduces exponentially with respect to the applied VGS. Therefore, with VGS close to VT, a transistor does conduct, and this transistor behavior can be exploited in low-power, low-energy designs. [3] [4]

1.4 Process Variation

In an ideal world, it is assumed that a designed device is modeled by a defined set of parameters. However, in reality, the parameters of a micro electronic device (particularly MOSFET transistors in this thesis) vary wafer to wafer or even between devices on a single die. This situation suggests that manufacturing processes are affected by processing variations and are in fact imperfect. This phenomenon results in manufactured devices that vary physically and that consequently will perform differently, although they follow the same design and manufacturing rules and methods.

Variations in process parameters, such as impurity concentration densities, oxide thickness, and diffusion depths, caused by non-uniform conditions during the deposition and/or the diffusion of the impurities result in diverging values for sheet resistances, and transistor parameters such as threshold voltage. Also, variations in the dimensions of devices, mainly resulting from the limited resolution of the photolithographic process particularly in advanced nano-meter technologies, cause deviation in the aspect ratios of MOSFET transistors and the widths of interconnect wires.

The measurable effect of process variations may be a substantial deviation of the circuit behavior from the nominal or expected response, and this could be in either positive or negative directions. This effect poses an economic dilemma for the designer. When a designer designs a transistor base device such as a SRAM or a microprocessor, it is important that the majority of the manufactured dies meet a set performance requirement. One way to achieve that goal is to design the circuit assuming worst case values for all possible device parameters. This results in a very complex and extremely over designed device which is not economically sound.

In reality, the worst case conditions occur only very rarely. The probability that all parameters would assume their worst case value simultaneously is very low, and most designs will display a performance centered around the nominal design. The art of designing manufacturability is to center the nominal design so that the vast majority of fabricated circuits will meet performance specifications, while keeping the area overhead minimal [5].

Specialized design tools to help meet this goal are available. For example, the Monte Carlo analysis approach simulates a circuit over a wide range of randomly chosen values for device parameters. In this paper, Monte Carlo analysis is the backbone of variation simulations using Cadence Virtuoso Spice tools.

1.5 Six Sigma Analysis

As discussed, manufactured electronic devices such as transistors are susceptible to process variations. This means when a large number of these devices are manufactured, each device illustrates a slight difference in characteristics and performance compared to others. Therefore, standards for device performance and characteristics have to be set by the designer so that manufactured devices that do not meet expectations are rejected. Six Sigma statistical analysis is a ?methodology used to address these quality concerns. The Six Sigma process has proven to be an effective method for tackling manufacturing imperfections. The Six Sigma scale is a universal measurement methodology of how well a critical characteristic preforms compared to a set of

requirements. A higher sigma score means more capable characteristic. A Six Sigma process will have 3.4 or less per million parts that are out of specification range. For a process to be at Six Sigma level, it needs to have +/- 6 standard deviations within the specification limits in the short term and +/- 4.5 standard deviations within the limits in the long term [6]. When underlying disturbances are added to the natural short-term variation, the overall combination is called the long-term variation of the process. As opposed to random, short-term variation, these underlying disturbances are *non-random* over the long term and can be approximated with a line, a step, a curve, or a repeated pattern.

1.6 Thesis Contribution and Organization

Previous work has demonstrated a limited comparison between 6 transistor and 10 transistor cell designs. This thesis presents an in depth comparison between 6 transistor and 10 transistor SRAM cells for a wide range of operating voltages and transistor widths so as to present a 3-dimensional comparison map while considering device variations.

Chapter 2 demonstrates and analyses previous work done related to the material covered in this thesis. This comes in the form of a literature review of past scientific research done in the areas related to this work.

Chapter 3 describes the transistor sizing methods used for Static Noise Margin simulations. A Static Noise Margin simulation methodology for each of the examined SRAM cells is demonstrated. Also a 3-dimentional comparison of SRAM cells' Static Noise Margin and read failure is established while also considering device process variations.

Chapter 4 describes the transistor sizing methods used for read current simulations. A read current simulation methodology for each of the examined SRAM cells is demonstrated. Also a 3-dimentional comparison of SRAM cells' read currents is established while also considering device process variations.

Chapter5: Leakage Current Comparison

Chapter 5 describes the transistor sizing methods used for leakage current simulations. A leakage current simulation methodology for each of the examined SRAM cells is demonstrated. Also a 3-dimentional comparison of SRAM cells' leakage currents while considering device process variations is established.

Chapter 6 describes the transistor sizing methods used for Write Margin simulations. A write margin simulation mythology for each of the examined SRAM cells is demonstrated. Also, a power efficient method to improve write margin of the 10T SRAM is provided. Finally a 3-dimentional comparison of SRAM cells' Write Margin and write failure is carried out while also considering device process variations.

Chapter7 demonstrates an overall conclusion and a conclusive review of the findings and highlights of this thesis.

Chapter 2

Background

This chapter explores the background of designing ultra-low power integrated circuit technology and its adaptation to SRAM designs.

2.1 Background (1960-2009)

Since 1925, when Canadian physicist Julius Edgar Lilienfeld filed a patent for a field-effect transistor (FET) device, researchers have extensively researched transistor devices and examined their device physics and electrical behaviour. However, it was not until the 1970s that researchers showed an interest in the operation of FET devices in the weak inversion region also known as the subthreshold regime. Initially, in 1969, in "Complementary-MOS Low-Power Low-Voltage Integrated Binary Counter" [7], operation in weak inversion mode was considered as an approach to creating low-power devices. In a 1972 paper, "Ion-implanted Complementary MOS Transistors in Low-Voltage Circuits" [8], the operation of the MOS device in weak inversion mode was investigated. This paper examined the theoretical limits to supply voltage scaling. It was found that a minimum supplied voltage of 2 to 3 times the thermal voltage is necessary for an inverter device to have sufficient gain. This is the point at which a basic understanding of subthreshold behaviour was developed.

In 1991, in a paper presented at the 3rd NASA symposium on VLSI design, "Ultra Low Power CMOS Technology" [9] , it was illustrated that minimum energy operation occurs in the subthreshold region. Also "Characterization of CMOS process variations by measuring subthreshold current" [10] investigated the effect of process variation in subthreshold region. In a 1997 paper, "Supply and Threshold Voltage Scaling for Low Power CMOS" [11] Using a first-order model of the energy and delay of a CMOS circuit, the authors show that lowering the supply and threshold voltage is generally advantageous, especially when the transistors are

velocity saturated and the nodes have a high activity factor. The 2001 paper "Robust Subthreshold Logic for Ultra-Low Power Operation" [12] demonstrates that digital subthreshold logic circuits can be used for applications in the ultra-low power end of the design spectrum, where performance is of secondary importance. In this paper, the authors proposed two different subthreshold logic families, variable threshold voltage subthreshold CMOS and subthreshold dynamic threshold voltage MOS logic. A 2002 paper, "Optimal Supply and Threshold Scaling for Sub-threshold CMOS Circuit" [13], plotted constant energy contours while varying the supplied voltage and threshold voltage of a device. The minimum energy point is shown to be in the subthreshold region.

In a 2005 paper, "A feasibility study of subthreshold SRAM across technology generations", has explored the feasibility of designing a SRAM array in the subthreshold domain of device operation. The authors have performed a nominal corner analysis of power and stability and a statistical analysis of the different failure probabilities of subthreshold SRAM. Their analysis shows that subthreshold SRAM gives significant reduction (~100×) of operating and standby power at iso-performance (~100MHz) compared to a super-threshold counterpart. Since sub-threshold currents are exponentially dependent on threshold voltage, the increase in variations in recent process nodes gave rise to a new research focus [14]. In aDARPA-funded research paper in 2005, "Analyzing Static Noise Margin for Subthreshold SRAM in 65nm CMOS", theauthors evaluate the static noise margin (SNM) of 6T SRAM bit-cells operating sub-threshold. They analyze the dependence of SNM during both hold and read modes on supply voltage, temperature, transistor sizes, local transistor mismatch due to random doping variation, and global process variation in a commercial 65nm technology [15]. The 2006 paper, "A256-kbit Subthreshold SRAM in 65nm CMOS" addresses the problem of SNM variation in 65nm cell [16].

2.2 Recent Research (2010-2015)

In recent years, continuous technology scaling and the growing trend of low power applications have led to an extra focus on ultra-low voltage operating memories. The 2012 paper, "A 300 mV

10 MHz 4 kb 10T subthreshold SRAM for ultralow-power application" proposes a 10T differential bit-cell that can effectively separate the read and write operation paths. The authors used a high Vth NMOS in the write operation path to reduce the bit-line leakage current in 90nm technology [17].

The 2011 Paper "Static Noise Margin Analysis of Various SRAM Topologies" compares the static noise margin and its improvements in various SRAM topologies [18]. In the 2014 paper "Statistical Analysis of Read Static Noise Margin for Near/Sub-Threshold SRAM Cell" a fast statistical method for the analysis of the Read SNM of a 6T SRAM cell in near/subthreshold region is proposed. The method is based on the nonlinear behavior of the cell. DIBL and body effects are thoroughly considered in the derivation of an accurate closed form solution for the Read Static Noise Margin (SNM) of a near/subthreshold SRAM cell. This method uses the state space equation to derive the Read SNM of the cell as a function of the threshold voltage of cell transistors. This function shows the dependency of the Read SNM on sizing, VDD, temperature, and threshold voltage variations. It provides a fast reliability analysis for a cell array of a given size and a supply voltage. It also calculates the accurate value of failure probability of the cell. The analytical results are verified using Monte-Carlo simulations in 45 nm Predictive Technology Models [19].

In the 2014 paper "A 32kb 90nm 10T-cell sub-threshold SRAM with improved read and write SNM" a 10T cell structure has been proposed with 90% read and 50% write SNM improvement in comparison to the conventional 6T cell. The hold SNM value is about the 6T cell SRAM. Also using differential read method in the proposed structure results in a high read performance and simpler sense amplifier. The symmetric configuration of this structure provides the SRAM with a simpler layout and lower transistor mismatch. Using 90nm TSMC CMOS, 32kb 10T cell SRAM in the sub-threshold area is simulated and confirms the proposed structure's performance [20].

A 2014 DARPA funded paper, "An Ultra-Low Energy Subthreshold SRAM Bitcell for Energy Constrained Biomedical Applications", analyzes various double ended SRAM topologies in the

subthreshold domain. It compares the topologies with respect to Static Noise Margin, Write Margin, Read Current, and Leakage Current [21].

The 2015 paper, "Device bias technique to improve design metrics of 6T SRAM cell for subthreshold operation", proposes a new way to design a SRAM cell. The proposed cell functions properly even below subthreshold region. Therefore, it can be useful for ultralow-power applications. The robustness/reliability of the proposed design is investigated by estimating the read static noise margin (RSNM). The estimated results are compared with those of its conventional counterpart. The proposed 6T SRAM cell offers 1.83× faster read operation. It is also less affected by PVT fluctuations (by 1.47×) during read operation compared to conventional 6T SRAM cells. The proposed SRAM cell exhibits 1.40× higher RSNM compared to a conventional 6T SRAM cell, proving its reliability during read operation. It also shows 3.86% faster write operation. It is 18.4% less affected by PVT fluctuations. It has 2.33% higher write static noise margin (WSNM) than the conventional 6T SRAM cell [22] .

Chapter 3

Static Noise Margin Comparison

The goal of this chapter is to analyze the design process of a conventional subthreshold 6 transistor SRAM cell (Figure2) along with a 10 transistor SRAM structure proposed by Chang et al. (A cell described to have a high static noise margin in 90nm technology node) [23] (Figure3) with respect to their Static Noise Margins. The ultimate purpose is to compare these designs with respect to their Static Noise Margin in a 3-dimentional fashion. These comparisons then can provide a vision to designers for finding an optimal width and supply voltage for a particular design while minimizing the design's susceptibility to process variation. Figure 2 to 4 will be used as references for the rest of this chapter.

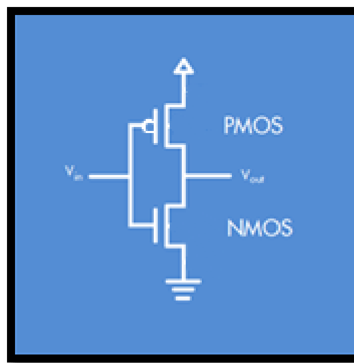

Figure 2: Simple CMOS inverter

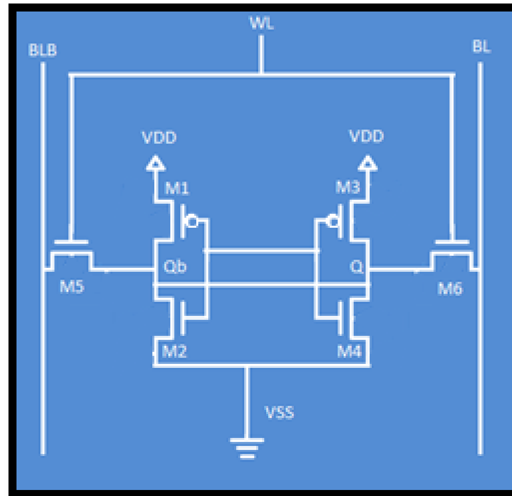

Figure 3: A schematic for 6T SRAM cell.

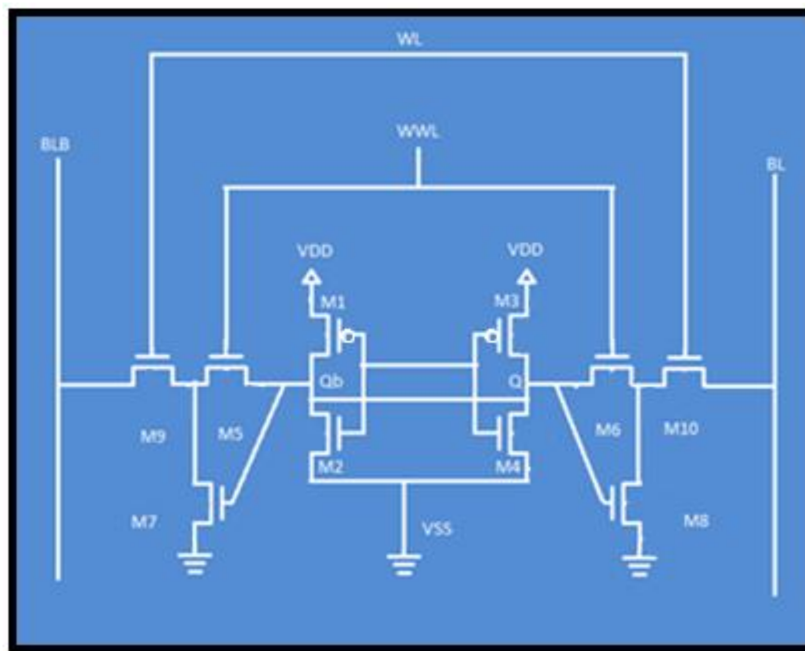

Figure 4: A schematic for the 10T SRAM cell.

3.1 Sizing of SRAM Cells

This section describes the methodology used for sizing the 6 transistor and 10 transistor SRAM cells discussed in this paper to achieve an optimal Static Noise Margin for each cell. The sized devices are then used to collect a comparable set of data to be analysed and used to draw conclusions.

3.1.1 Invertor Sizing

The variation in the ratio of PMOS and NMOS widths (β) in a CMOS invertor will have a direct effect on the energy and the delay of an inverter.

(1)
$$\beta = \frac{PMOS\ width}{NMOS\ width}$$

In above-threshold operation, it is known that the PMOS device is the weaker device, and its size has to be adjusted to balance the current strength ($\beta > 1$). However, research shows that the sub-threshold current of an NMOS device is weaker than the PMOS; therefore, NMOS has to be upsized to achieve a current balance. This means the PMOS to NMOS width ratio β has to be less than or equal one ($\beta \leq 1$). In fact, it has been demonstrated that the optimal value of β in sub-threshold operation for minimum energy is one (β=1) [24]. Therefore, In the process of designing a sub-threshold SRAM, normally a β value of one is considered. This value will be considered in the sizing of the devices in subthreshold regime.

3.1.2 6T SRAM Cell Read-Path Sizing

In 6T SRAM read operation, initially both bit lines are precharged to the voltage VDD. During read, the wordline (WL) is turned on and the ground voltage VSS is low. Therefore, one of the bit lines connected to the internal node (Q or Qb) holding a 0 will be discharged. This discharge

will then be sensed by a sense amplifier to register a read operation. For example, a 1 is stored at Q in Figure 3. The read cycle is started by pulling the wordline to VDD, which opens M5 and M6 paths. During a correct read operation, the values stored in Q and Qb are transferred to BL and BLB respectively. This means BLB will be discharged through the M5-M2 path. But this correct operation needs carful sizing of the transistors in the read path. If correct sizing is not considered, the read operation will not happen correctly, and in some cases, a read upset will occur (a 1 accidentally will be written into the cell).

Initially, upon the rise of word line, the intermediate node between two NMOS transistors on the left side of the cell, Qb, is pulled up toward the precharged value of BLB. This voltage rise of Qb must stay low so as not to cause a substantial current flow through the M3-M4 cell, which in the worst case scenario will cause a cell to flip. Therefore, it is necessary for the resistance of M5 to be higher than that of M2. Thus, the NMOS transistors in inverters have to be stronger than the NMOS pass transistors in the cell. This can be translated into having a higher width for the invertor NMOS than for the pass transistor. The variation in the ratio of pull-down NMOS (invertor NMOS) and pass NMOS widths (CR), which is called the cell ratio in a SRAM cell, will have a direct effect on the read capability of the device. This ratio has to be greater than 1 [5].

(2) $$CR = \frac{pull\text{-}down\ NMOS\ width}{Pass\ NMOS\ width} > 1$$

3.1.3 10T SRAM Cell Read-Path Sizing

In 10T SRAM read operation, initially both bit lines are precharged to the voltage VDD. During read, the read-wordline (WL) is turned on and the ground voltage VGND is low. Also, the write-wordline (WWL) is pulled down to ground to turn off the read path through the M6 and M5 transistors. With M5 and M6 turned off, storage nodes are isolated from bit lines to prevent bit line interference. In this case, the M8 and M7 transistors act as read buffers. For example, a 1 is

stored at Q. A read cycle is started by pulling read-wordline to VDD and write-wordline to ground, which opens the M9 and M10 paths and closes the M5 and M6 paths. During a correct read operation, the M8 transistor will be ON because of the 1 stored in Q. Therefore BL will be discharged through the M10-M8 transistor path. The differential sense amplifier will detect the generated differential signal on the bit line pair and amplify the signal into full swing voltage. The 10T cell structure is able to inherit the fully-differential read scheme for more reliable read operation, and enable better SRAM cell read SNM.

The sizing of read path transistors will affect the read current and the speed of the operation, making this sizing important. The ratio of pull-down NMOS (M8 and M7) and pass NMOS (M9 and M10) transistor widths is defined to be the cell ratio (CR) in the 10T SRAM cell. This ratio has to be greater than 1.

(3)
$$CR\alpha = \frac{pull\text{-}down\ NMOS\ width}{Pass\ NMOS\ width} > 1$$

3.1.4 Static Noise Margin Calculation Method

The VTC behaviour of cross coupled inverters is commonly called a butterfly curve. The butterfly curve is a very sophisticated way of addressing and quantifying the stability of designed cells in presence of noise. The Static Noise Margin or SNM of an inverter device can be graphically represented by this butterfly curve, as seen in Figure 5. In this figure, two squares are fit inside of the voltage transfer characteristics of the cross coupled inverters. The SNM can be calculated by measuring the side length of each of these squares, and the smaller of two side lengths becomes the actual SNM of the designed cell, which is a good representation of the device's switching strength. In an Ideal case, these squares should be of equal size; however, transistor mismatch and process variation may cause the VTC curves not to mirror each other and cause a change in the overall SNM [25].

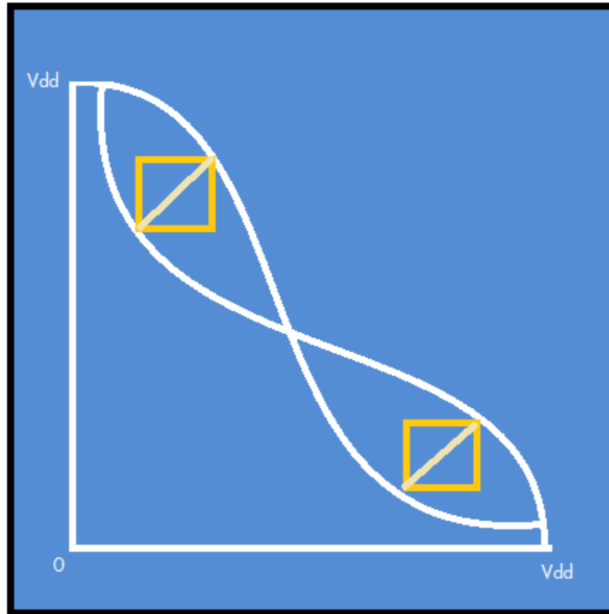

Figure 5: Butterfly curve for a crossed coupled inverter system.

It is easy to obtain the SNM from the VTC curves graphically; however, graphically calculating SNM for large amounts of device variation sample is extremely difficult. Therefore, a systematic method of calculation must be developed.

The SNM can be found analytically by solving the Kirchhoff equations and applying one of the mathematically equivalent noise margin criteria [26]. But since all calculation will be based on simulated results from acomputer aided design tool (Cadence Virtuoso), it is better to find a way to find SNM from the simulated DC sweep results from Cadence. To estimate SNM values, a procedure is needed that finds values for the diagonals of the maximum squares, as shown in Figure 5. A method which is quick and easy to use was developed for use together with a standard dc circuit simulator [27]. Figure 6 shows a stylized version of Figure 5 in two coordinate systems which are rotated 45° relative to each other. In the (u, v) system, subtraction of the u values of normal and mirrored inverter characteristics at a given u yields curve A, which is a measure of the diagonal's length. The maximum and minimum of curve A represent the required maximum squares.

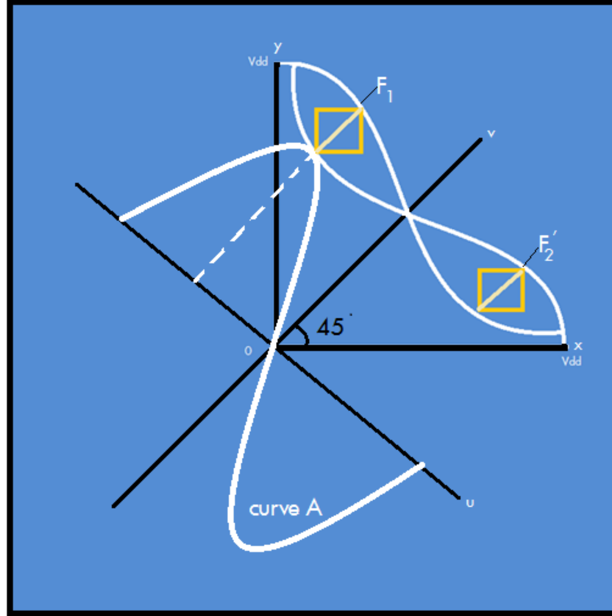

Figure 6: SNM estimation based on the maximum square, using a 45° rotated coordinate system.

Assume that the normal and mirrored inverter characteristics are defined by the functions y = $F_l(x)$ and y = F_l'(x) ,where the latter is the mirrored version of y = $F_2(x)$. To find F_1 in terms of u and v, the (x, y) coordinates must first be transformed into the (u, v) system. The required transformation is

(4a) $$x = \frac{1}{\sqrt{2}}u + \frac{1}{\sqrt{2}}v$$

(4b) $$y = -\frac{1}{\sqrt{2}}u + \frac{1}{\sqrt{2}}v$$

Substitution of (4) in y = $F_l(x)$ gives

(5) $$v = u + \sqrt{2}\,F_1\left(\frac{1}{\sqrt{2}}u + \frac{1}{\sqrt{2}}v\right)$$

For F_2', first F_2 is mirrored in the (x, y) system with respect to the u axis, and then it is transformed to the (u, v) system. The required coordinate transformation is now the same as (4) but with x and y exchanged; Substituting in y = F_2 (x) gives

$$v = -u + \sqrt{2}\, F_2\left(-\frac{1}{\sqrt{2}}\, u + \frac{1}{\sqrt{2}}\, v\right) \quad (6)$$

Equations (5) and (6) represent the inverters comprising the flip-flop cell. They give u as an implicit function of u. Solutions can be found with a standard dc circuit simulator by translating the equations into circuits, using voltage-dependent voltage sources in a feedback loop as shown in Figure 7. The solutions of (5) and (6) are represented by v_1 and v_2 in Figure 7 (a) and (b), respectively. The difference between the two solutions, $v_1 - v_2$, is calculated by the simulator and is represented by curve A in Figure 6.

The absolute values of the maximum and minimum are the values of the diagonals of the maximum squares. Multiplying the smaller of the two by $1/\sqrt{2}$ yields the SNM of the flip-flop.

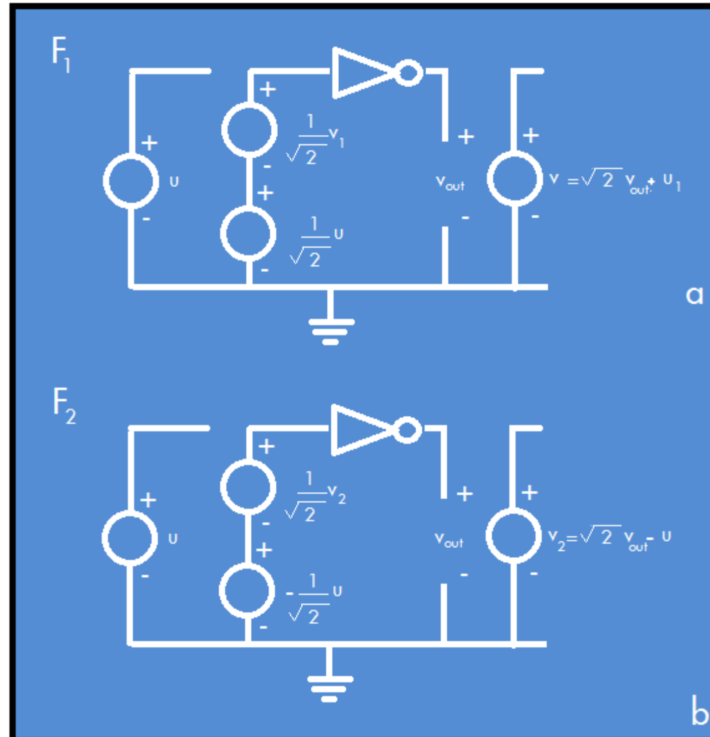

Figure 7: The cross coupled inverter test bench designed with the use of this SNM calculation methodology in Cadence computer aided design tool.

With use of the cross coupled inverter test bench circuit, which is the circuit equivalent to the graphical transform of VTC curves, extraction of "curve A", and measurement of the best fitted square diagonal size, the value of SNM can be measured for 6 transistor and 10 transistor cells. This method essentially separates the cell into two invertor sides and measures the VTC of each side. Then it adds two VTC curves and calculates the size of each square's diagonals. This method not only decreases the work of dealing with graphic calculations, it provides a computer aided friendly solution that can be implemented easily [27].

3.3 SNM Simulation

This section shows the simulation steps and results for the Static Noise Margin of 6 transistor and 10 transistor cell designs. To identify the difference between the read ability of these designed cells, this section also discusses and compares the simulated SNM and SRAM read failure of these SRAM cells.

3.3.1 Simulation Methodology

To calculate the butterfly curve, a DC sweep will be performed from –VDD to +VDD on the "u" DC voltage source discussed in section 2.1.4. The DC sweep of the test bench circuit connected to the SRAM cell will output a Voltage Transfer Characteristic curve for each side of the SRAM cell (each inverter side). Figure 8 shows the Voltage Transfer Characteristic curves of both sides of the cell superimposed on a single scale, which is also called the butter curve.

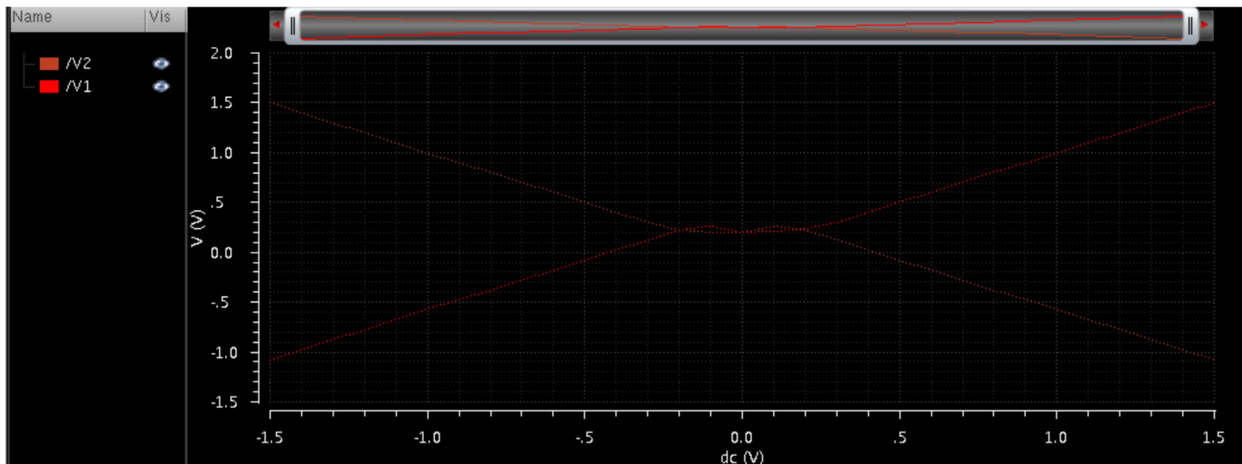

Figure 8: Rotate butterfly curve for 6T SRAM cell with minimum size devices.

To find the Static Noise Margin following the section 2.1.4 methodology, the "difference curve" of the two components of the butterfly curve is calculated. Figure 9 show the difference curve. The maximum and the minimum of the resulting difference curve, which are equal to the diagonals of the best fitted squares in the butterfly curve, are found. The diagonal values are then used to find the size of the side of each fitted square by multiplying the value by $\frac{1}{\sqrt{2}}$. The side of the smaller square is considered to be the Static Noise Margin of the device.

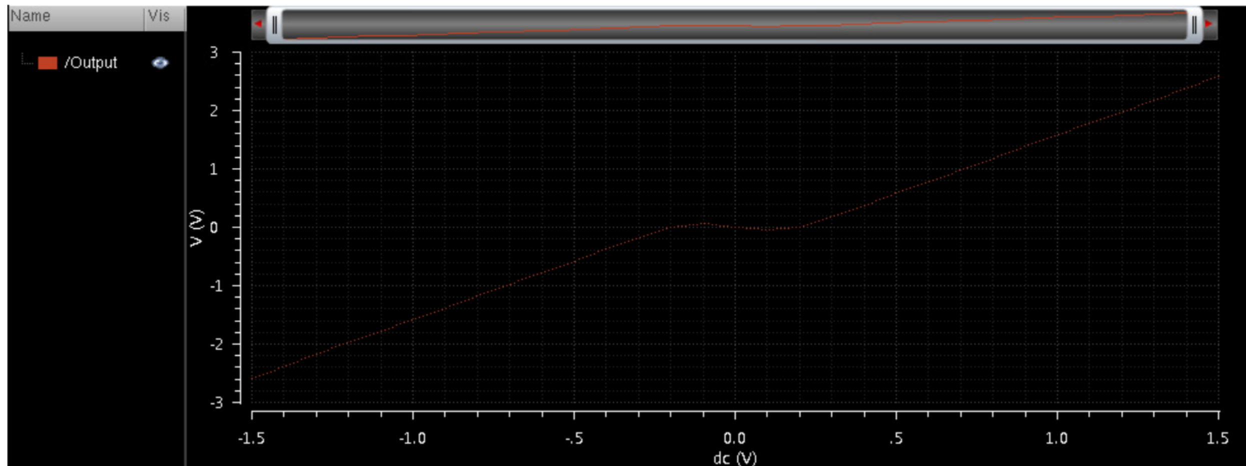

Figure 9: The cumulative curve for 6T SRAM cell with minimum size devices.

To find a realistic measure for the SNM of a designed and sized device, a broader picture of device functionality has to be considered. As discussed in the introduction of this paper, the presence of device variations and mismatches in the real world can cause many problems. These problems appear in the transition between design and manufacturing of the actual device. Therefore, process variation and mismatch have to be considered as limiting factors in a design stage, and the final design has to be free of any susceptibility to these factors. To achieve this task for the designed SRAM cells, a 5000 sample Monte Carlo analysis for variation and mismatch was performed on the SRAM designs for different setups. This analysis simply generates 5000 random variation and mismatch scenarios for the same device. To satisfy this chapter's purpose, the Monte Carlo analysis was formed with a SNM output, resulting in a different SNM output for each variation scenario.

Hysteresis graphs were drawn to the Static Noise Margin against a number of samples (5000 in total). Figure 10 shows the hysteresis graph generated for a minimum sized 6T SRAM cell. In the hysteresis graph any negative noise margin is considered to be a read failure. Therefore, from each of the Hysteresis graphs, a percentage failure for that particular setup for a specific SRAM cell can be calculated.

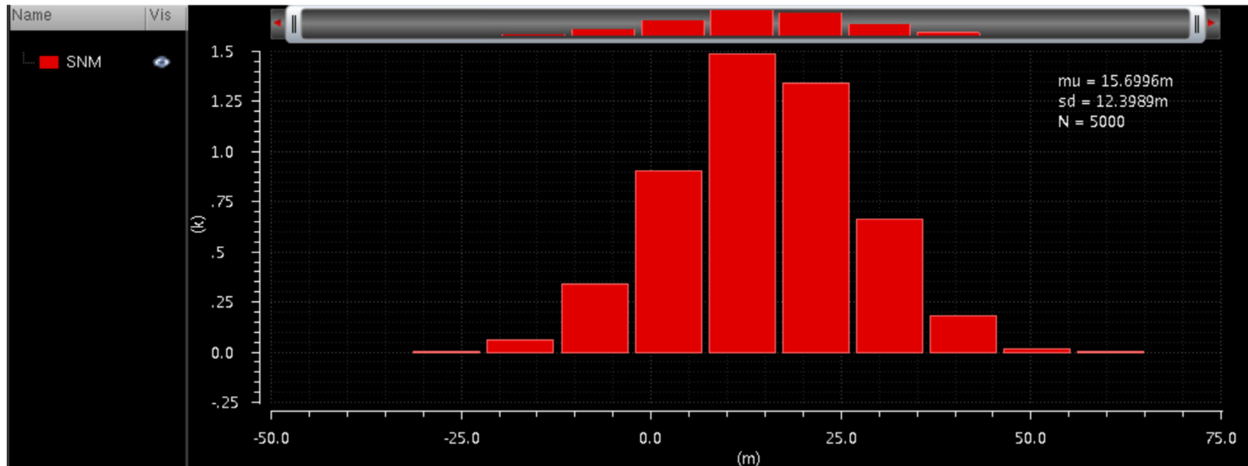

Figure 10: The SNM variation hysteresis graph generated for a minimum sized 6T SRAM cell @ 0.3V.

3.3.2 6T Cell Read Failure Simulation

To investigate 6 transistor read failure, the 6 transistor SRAM cell is evaluated at different applied voltages (VDD). The supplied voltage is varied, starting from 0.2 volts and going up to 0.5 volts. All voltages are chosen to be in the subthreshold domain, as the subthreshold behavior of the device is desired. In each round of simulations for each supplied voltage, a fixed pass transistor width is chosen, the cell ratio will be varied by changing the sink transistor width each time, and Monte Carlo analysis will be performed. The cell ratio will be changed each time until the failure rate of transistors due to variation susceptibility becomes zero in the defined 5000 Monte Carlo variation simulations. For the next round of simulations, the pass transistor size will be changed to a new value, and the cell ratio will be varied again, but this time according to the new pass transistor value. Figures 11 to 15 show the results of Monte Carlo simulations for the 5000 variation samples at 0.3 volts VDD while varying the pass transistor width and cell ratio of the 6T device, .

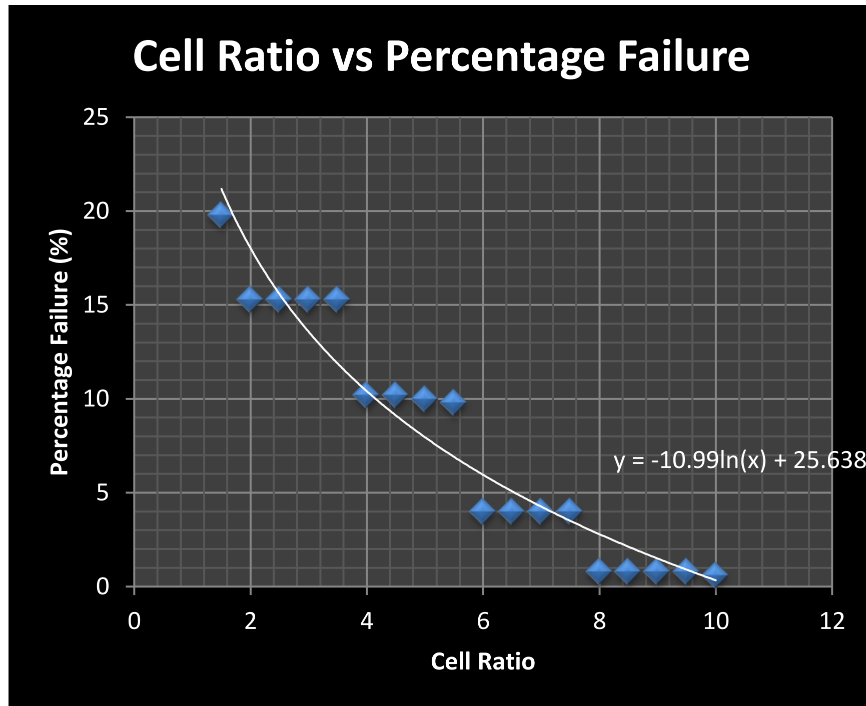

Figure 11: Cell Ratio vs Percentage Read Failure for a 6T transistor cell with pass transistor width of 150nm at VDD=0.3V.

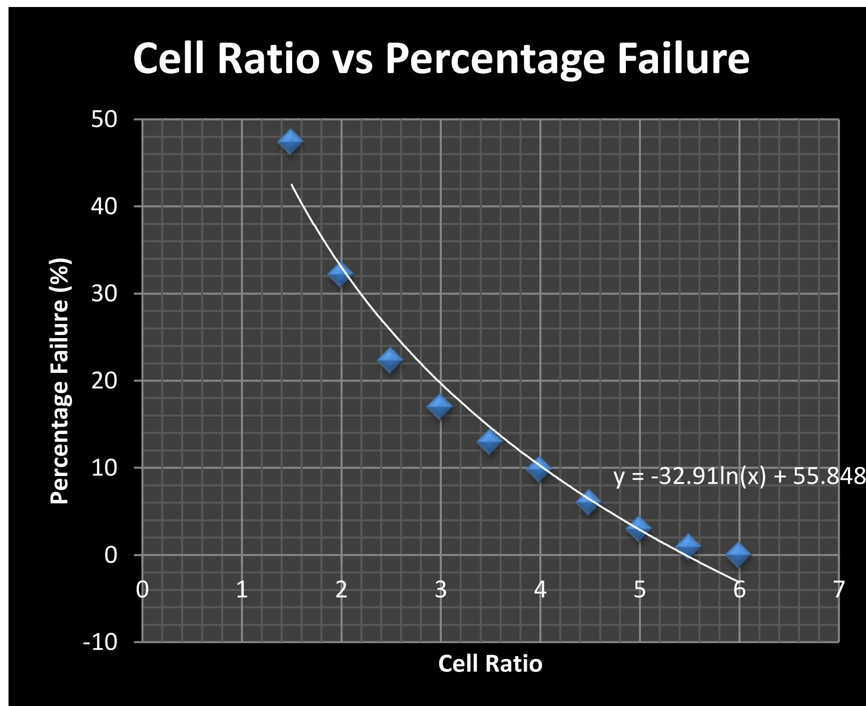

Figure 12: Cell Ratio vs Percentage Read Failure for a 6T transistor cell with pass transistor width of 200nm at VDD=0.3V.

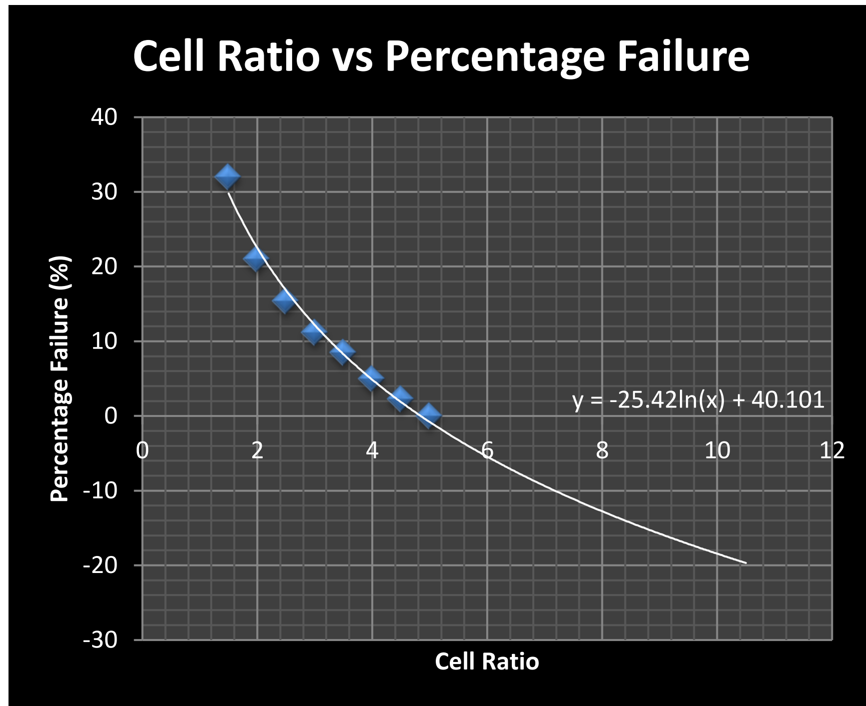

Figure 13: Cell Ratio vs Percentage Read Failure for a 6T transistor cell with pass transistor width of 300nm at VDD=0.3V.

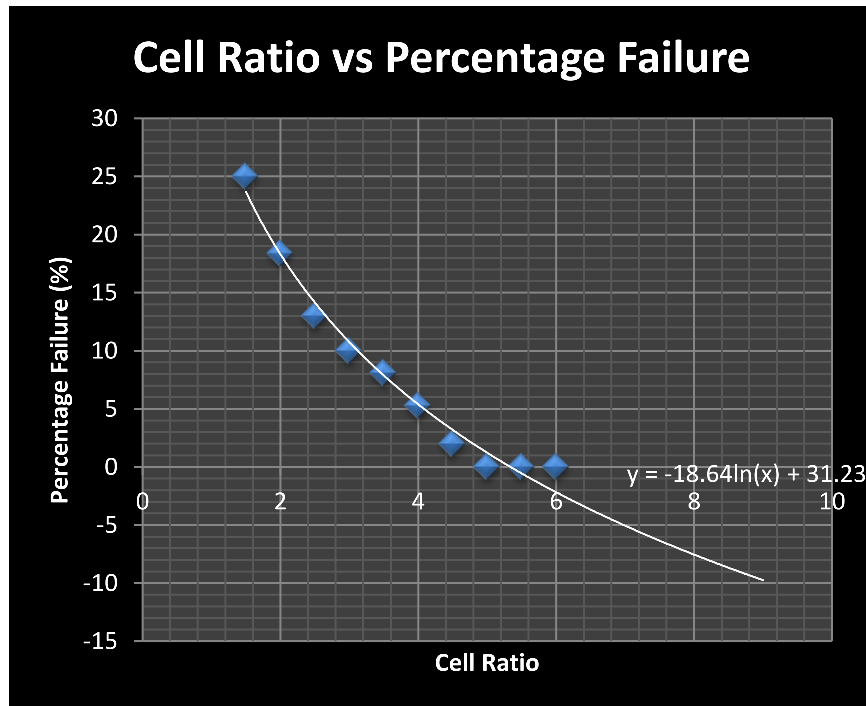

Figure 14: Cell Ratio vs Percentage Read Failure for a 6T transistor cell with pass transistor width of 400nm at VDD=0.3V.

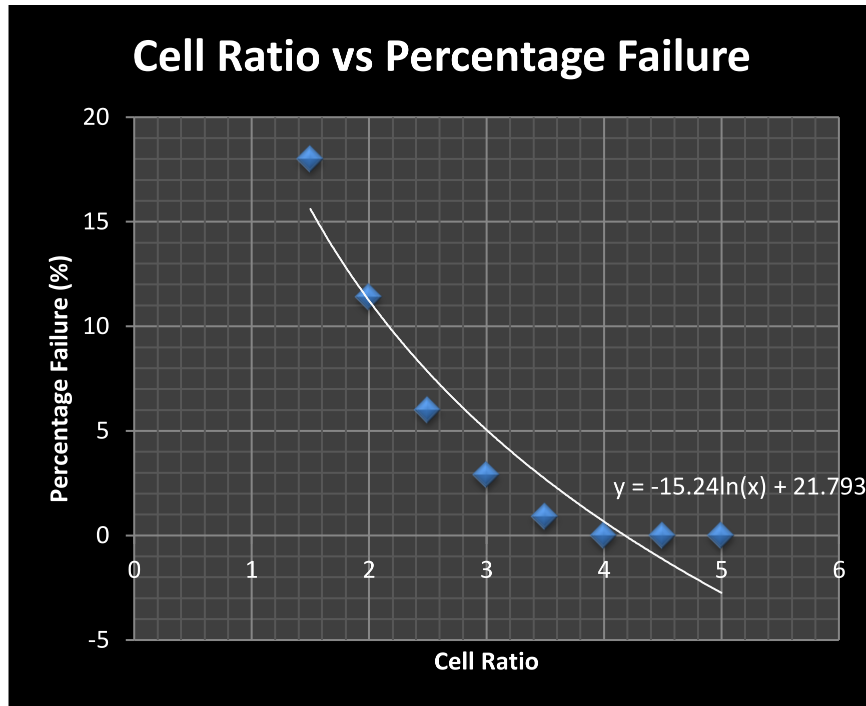

Figure 15: Cell Ratio vs Percentage Read Failure for a 6T transistor cell with pass transistor width of 500nm at VDD=0.3V.

From the analysis, the approximate function that relates the Cell ratio and percentage failure can be derived.

(7) $$Percentage\ Failure = -a\ lnx + b$$

where a and b are constants dependent on the transistorwidth and x is the cell ratio.

Therefore, it can be concluded that for a fixed device voltage, the percentage failure and cell ratio always have an exponential relationship in 6T SRAM cells in 65nm technology.

Putting all the results together, a 3D graph can be generated relating the percentage failure, pass transistor width, and cell ratio, in a 6T cell for VDD of 0.3 volts. Figure 16 illustrates this relationship.

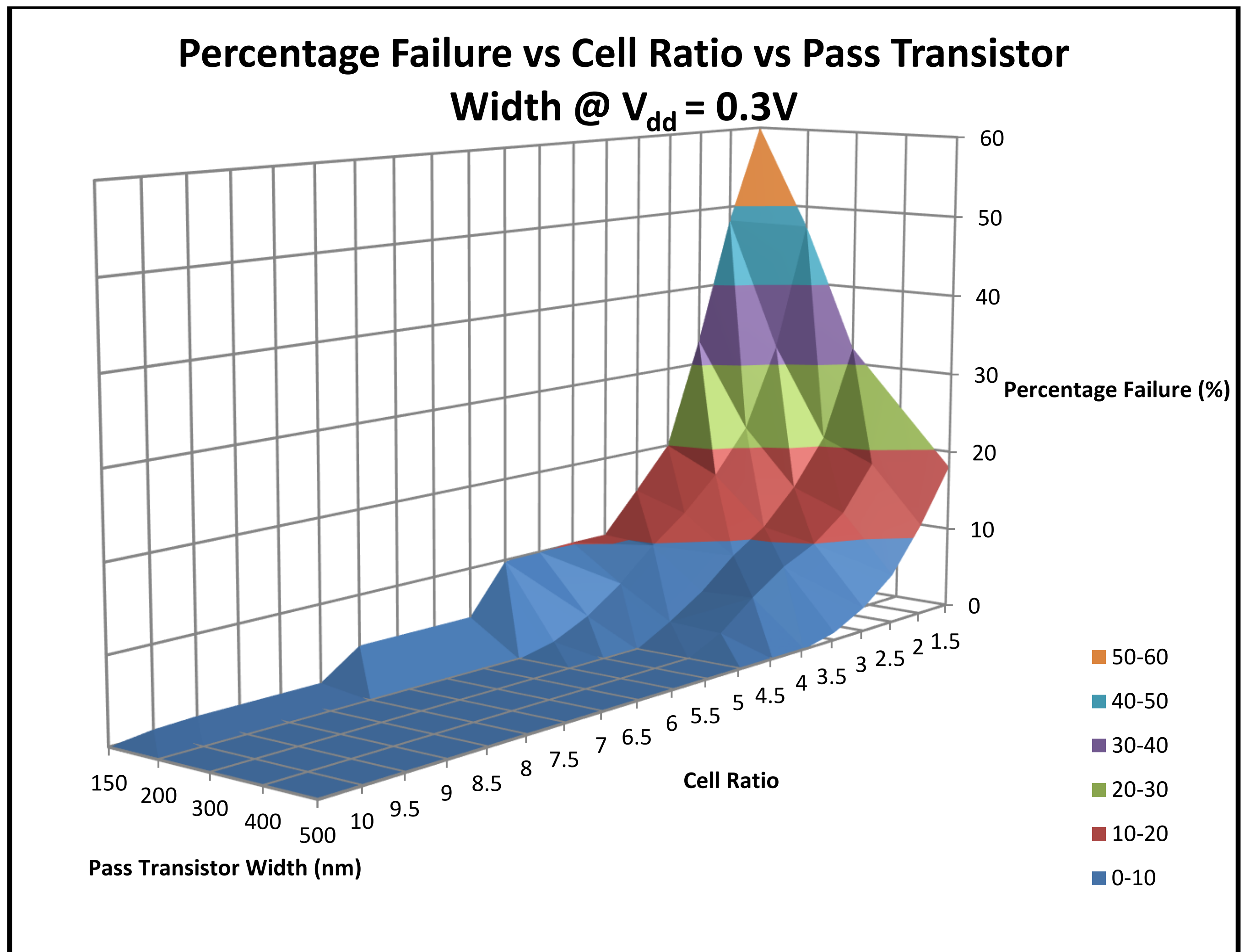

Figure 16: A 3-dimentional illustration of Percentage Read Failure vs Cell Ratio vs Pass Transistor Width for a 6T cell at VDD=0.3V.

The same methodology was used to generate similar curves for the VDD voltages higher than 0.3 volts up to 0.5 volts. Figures 17 and 18 illustrate the simulation results graphically.

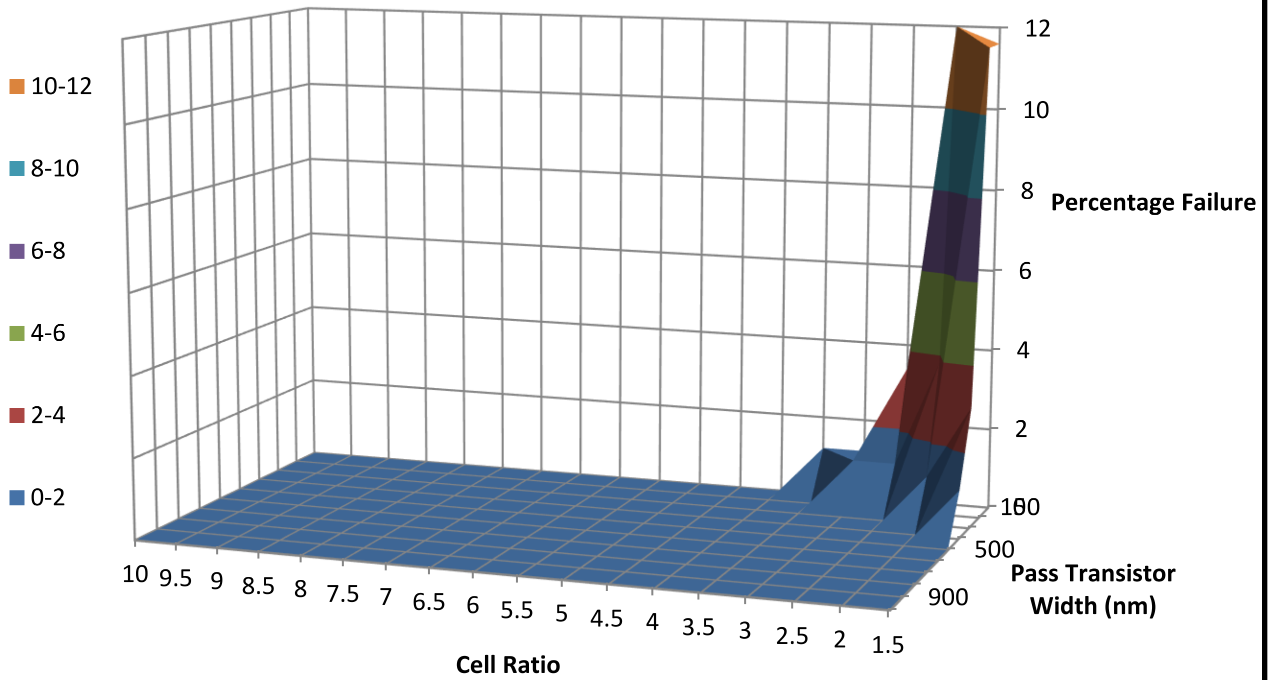

Figure 17: A 3-dimentional illustration of Percentage Read Failure vs Cell Ratio vs Pass Transistor Width for a 6T cell at VDD=0.4V.

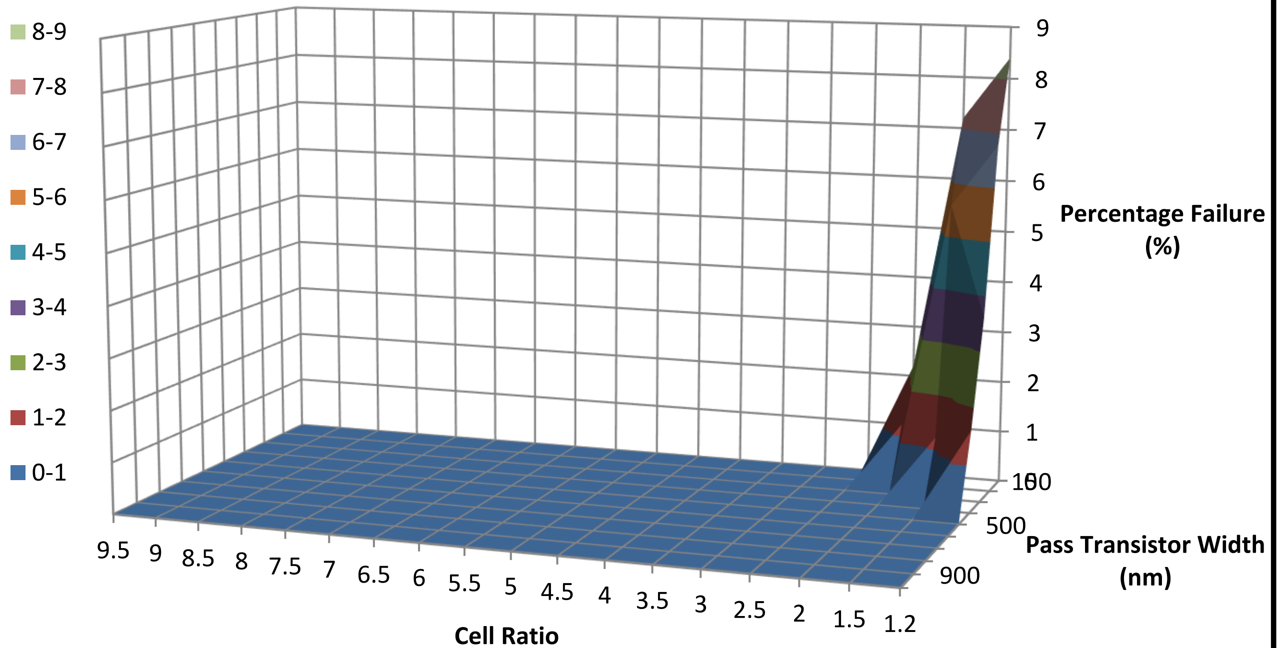

Figure 18: A 3-dimentional illustration of Percentage Read Failure vs Cell Ratio vs Pass Transistor Width for a 6T cell at VDD=0.5V.

As it is illustrated, as the voltage increases, the percentage read failure decreases dramatically. The device is more susceptible to failure at lower voltages and smaller transistor sizes.

3.3.3 10T SRAM Cell Read Failure Simulation

To investigate the 10T SRAM cell's read failure, the 10T cell is evaluated at different applied voltages (VDD). Initially, at minimum voltage (VDD = 0.3v) and minimum inverter transistor width (W=150nm) the cell ratio was varied and SNM and percentage failure was measured.

To further investigate the Percentage Read Failure of the 10T Cell, the inverter transistor width is varied from 150nm to 300nm for each set supplied voltage ranging from 0.3V to 0.5V and the Percentage Failure is measured. The Percentage Read Failure is measured upon a 5000 sample Monte Carlo variation and mismatch simulation on the Static Noise Margin of each setup. Figure 19 illustrates the simulation results graphically in a 3-dimentional fashion at theVDD = 0.3V.

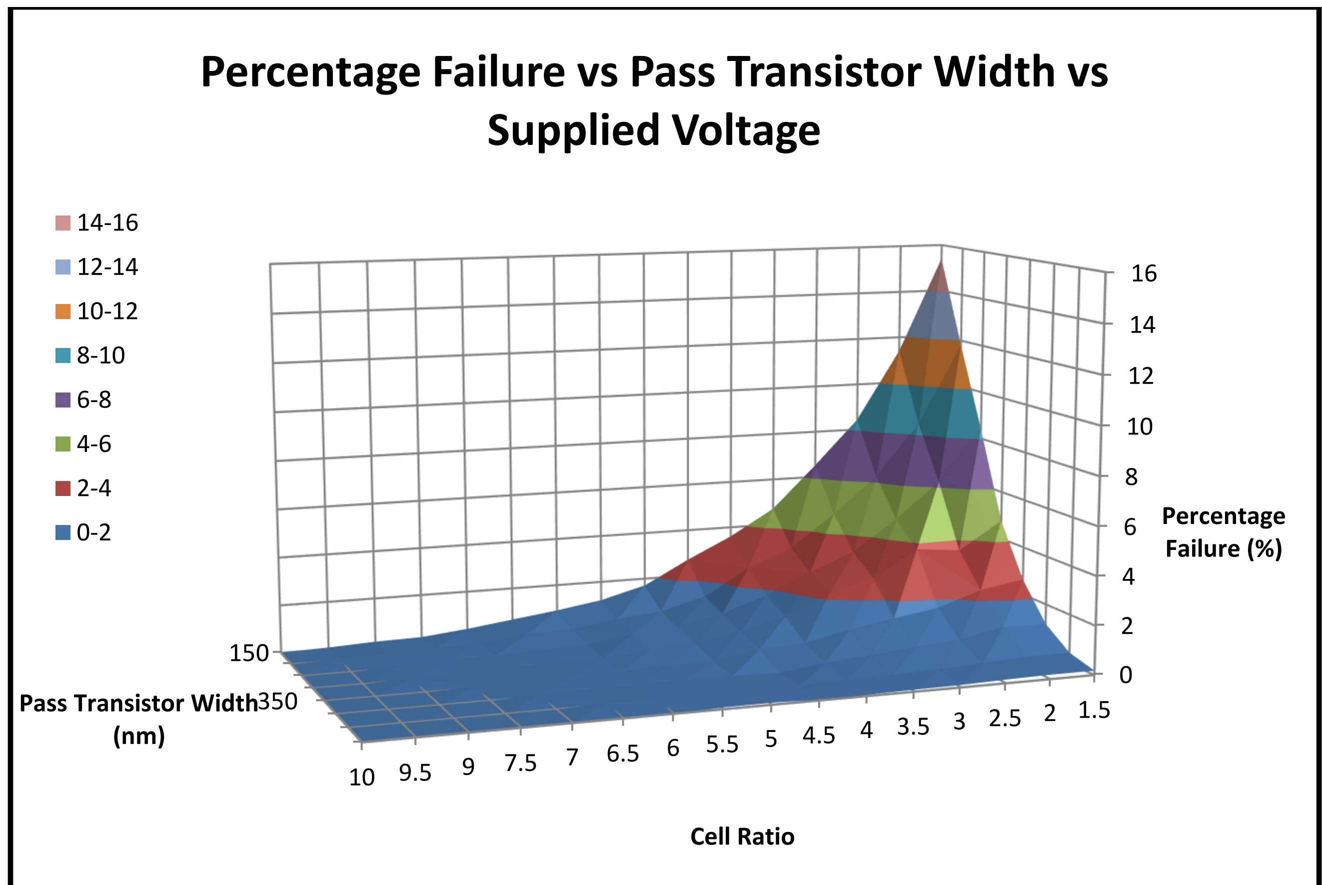

Figure 19: A 3-dimentional illustration of Percentage Read Failure vs Cell Ratio vs Pass Transistor Width for a 6T cell at VDD=0.3V.

3.3 Comparing SNM Simulations

After analysing 6T and 10T cells, it is revealed that in the 10T cell the read failure will be significantly lower than that of the conventional 6T SRAM Cell. This happens because in the 10T cell the entire read is decoupled from the internal node of the device, which gives the 10T higher noise margin values. Figures 20 and 21 illustrate the comparison of Percentage read failure values of 6T and 10T cells for a wide range of simulations.

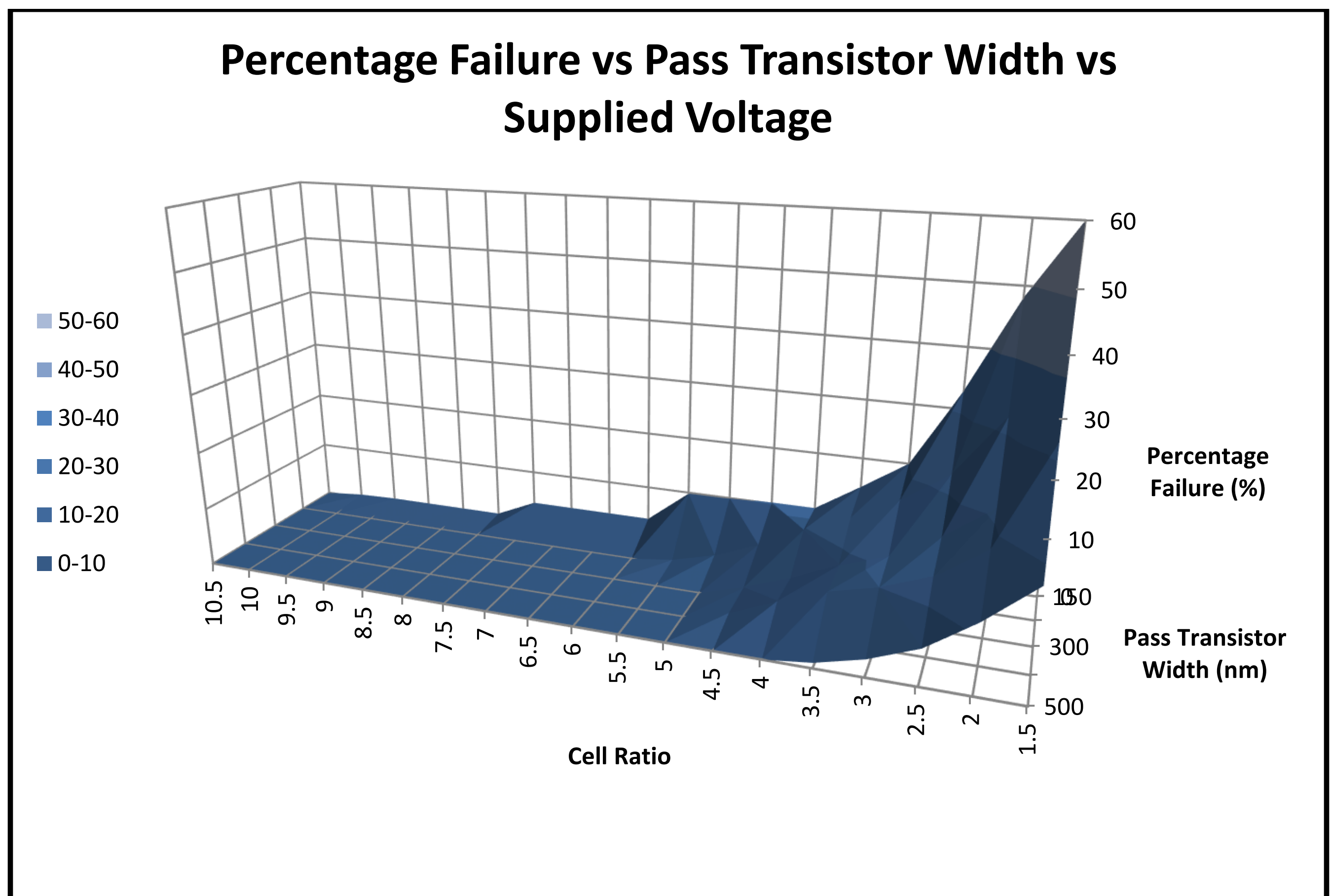

Figure 20: A 3-dimentional illustration of Percentage Read Failure vs Cell Ratio vs Pass Transistor Width for a 6T cell at VDD=0.3V (for comparison).

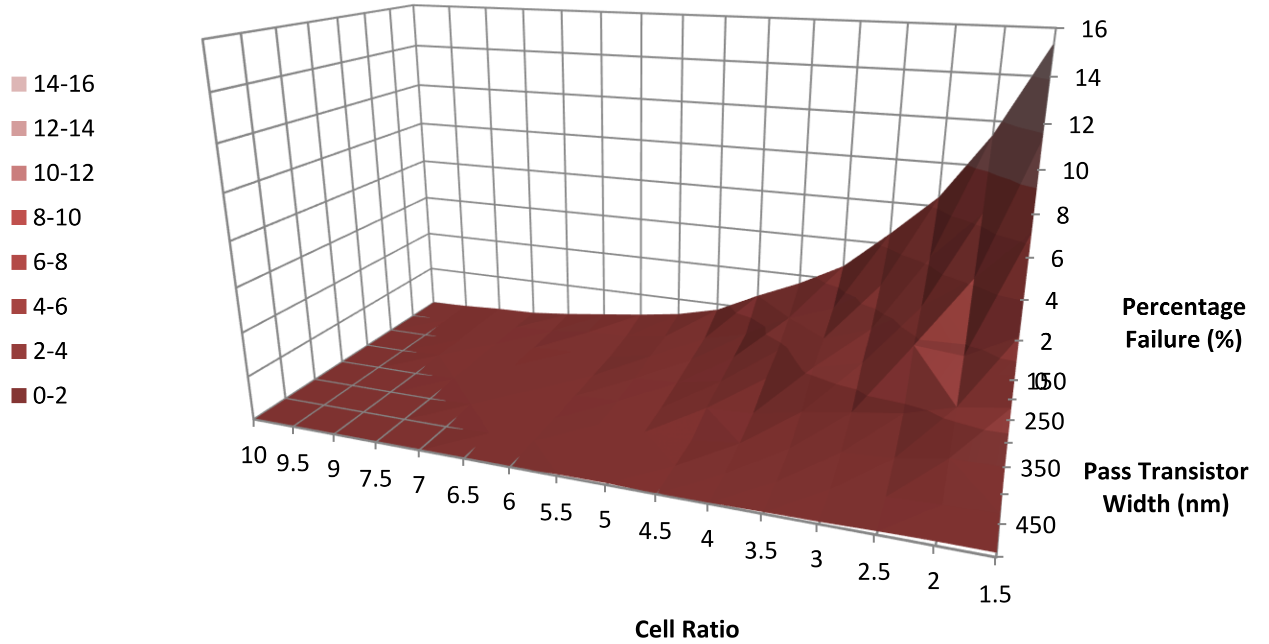

Figure 21: A 3-dimentional illustration of Percentage Read Failure vs Cell Ratio vs Pass Transistor Width for a 10T cell at VDD=0.3V (for comparison).

Chapter 4

Read Current Comparison

The ultimate goal of this chapter is to design a conventional subthreshold 6T cell along with a subthreshold 10T SRAM cell and compare their Read Current in a 3-dimentional fashion. These comparisons then can provide a vision to help designers find optimal designs based on read current criteria. Figures 22 to 24 will be used as a reference for the rest of this chapter.

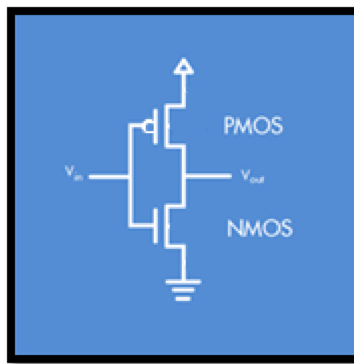

Figure 22: Simple CMOS inverter.

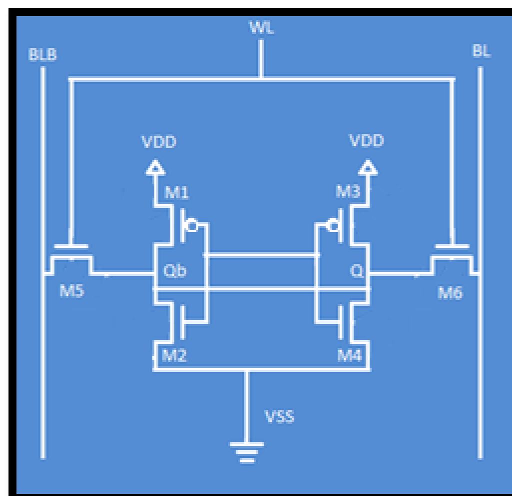

Figure 23: A schematic for 6T SRAM cell.

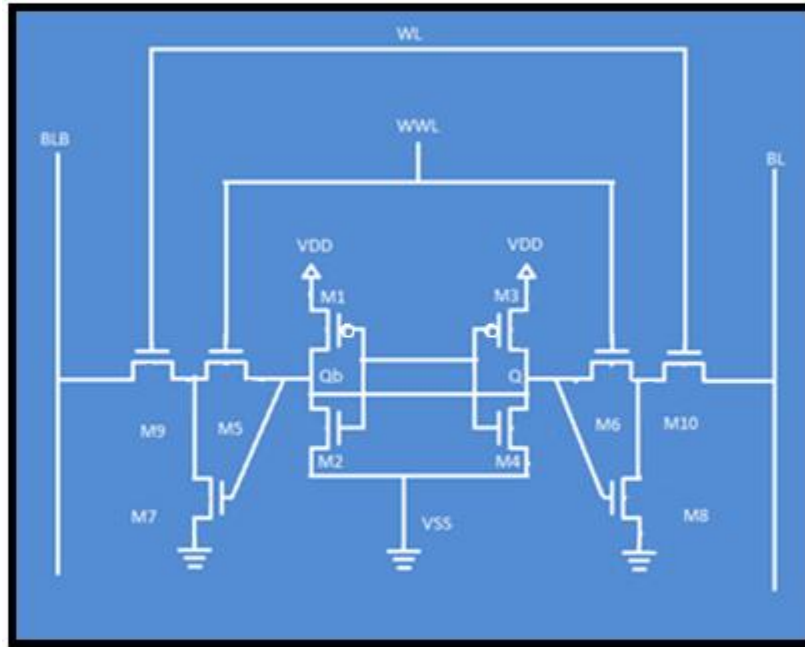

Figure 24: A schematic for the 10T SRAM cell.

4.1 Device Sizing for Simulation

This section describes the methodology used for sizing the 6 transistor and 10 transistor SRAM cells discussed in this paper to collect a comparable set of read current data from each design.

4.1.1 6T Cell Sizing for Simulation

To keep the unity in design methodology throughout this paper and to generate comparable results, the PMOS (pull-up) to NMOS (pass-transistor) ratio of the 6 transistor SRAM cell design was chosen to be one (β=1). In the process of simulation for each fixed VDD, the inverter transistor sizes were set to 150 nm as the minimum width and were varied to 500 nm in different simulation setups. In each simulation with a fixed VDD and fixed inverter transistor width, the cell ratio (CR) was varied between 1.5× to 10.5× of the inverter transistor width. This helps to

create a 3-dimentional graph of read current vs pass transistor width vs cell ratios at a fixed supplied voltage.

4.1.2 10T Cell Sizing for Simulation

In the 10T cell design, to keep the unity in design methodology throughout this paper and to generate a comparable result to the 6 transistor design, which has a fundamentally different approach for controlling the read current, the PMOS to NMOS ratio (β) was chosen to be one (β=1) just like in the 6T cell. In the process of simulation for each fixed VDD the inverter transistor sizes were set to 150nm as the minimum width and were varied to 500nm in different simulation setups. In each simulation with a fixed VDD and fixed inverter transistors width, the cell ratio was varied between 1.5× to 10.5× of the inverter transistor width. This helps to create a 3-dimentional graph of the read current vs pass transistor width vs cell ratio at a fixed supplied voltage which is comparable to the 6 transistor graphs.

4.2 Read Current Simulation

This section shows the simulation steps and results for the read current of 6 transistor and 10 transistor SRAM cells and discusses the comparison between the read current of the designs.

4.2.1 Simulation Setup for 6T Cell

To calculate the read current in a 6T cell design, the node Q was pre-set to the value 0 (0 Volts) and node Qb was set to 1 (VDD). Then read operation was done by pre-charging the bit line and bit line Bar (BL, and BLB) to VDD voltage. The word line (WL) was set to VDD to open the M6 gate. The current through M6-M4 was measured at VSS. Figure 25 illustrates the described setup.

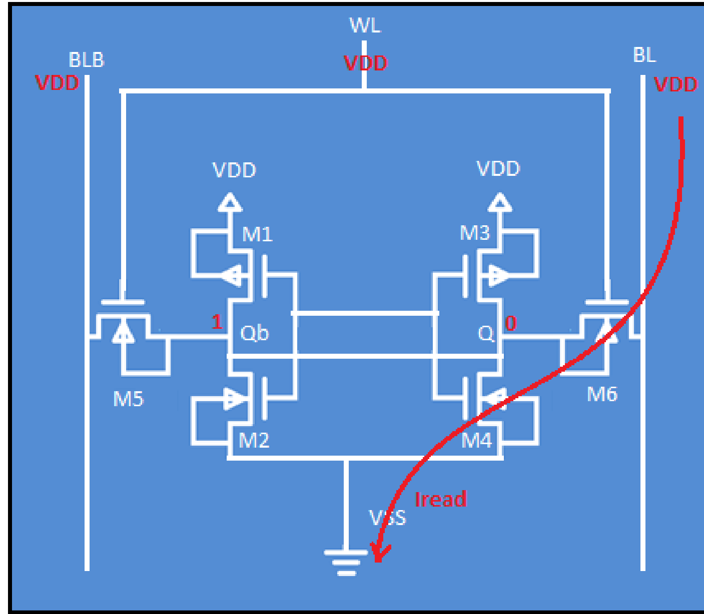

Figure 25: A read operation in a 6T SRAM cell.

The 6T cell was simulated at two different VDD voltages, 0.2 volts and 0.3 volts. For each of these voltages the sizing methodology described in section 3.1.2 was used to generate a wide range of current data. For each setup, a 5000 sample Monte Carlo analysis for variation and mismatch was performed on the SRAM Cell. Hysteresis graphs were drawn comparing the read currents against the number of samples. The "mean" read current was extracted from the hysteresis graphs and was used for graphing and compression. Figures 26 and Figure 27 show the read current variation in 0.2V and 0.3V VDD respectively.

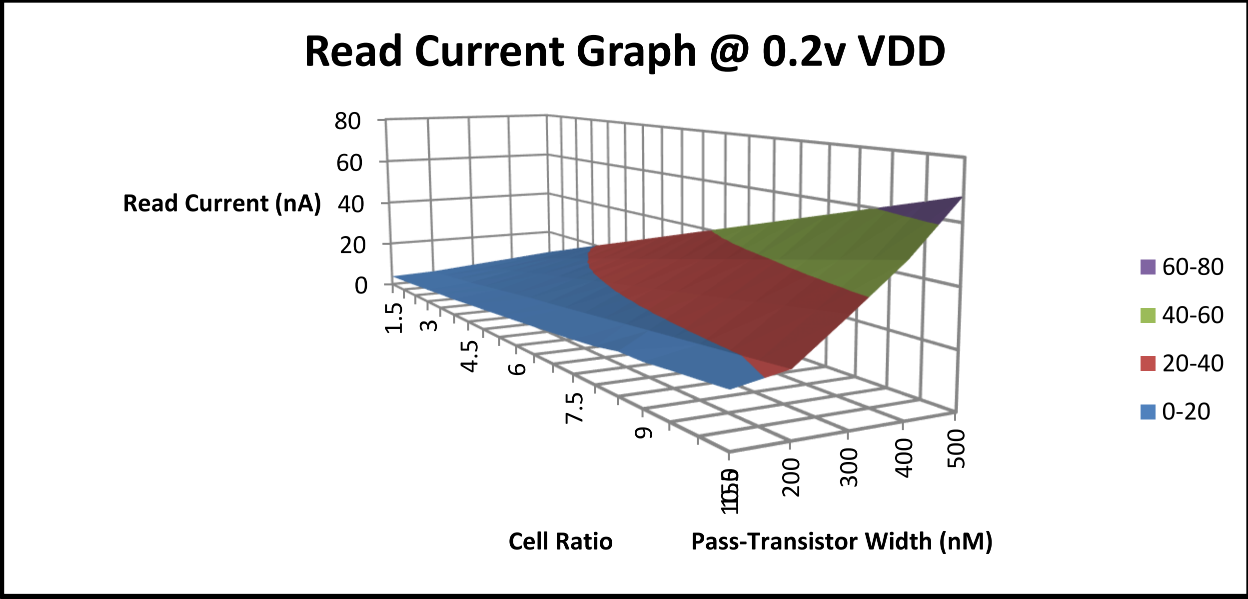

Figure 26: A 3-dimentional illustration of Read Current vs Cell Ratio vs Pass Transistor Width for a 6T cell at VDD=0.2V.

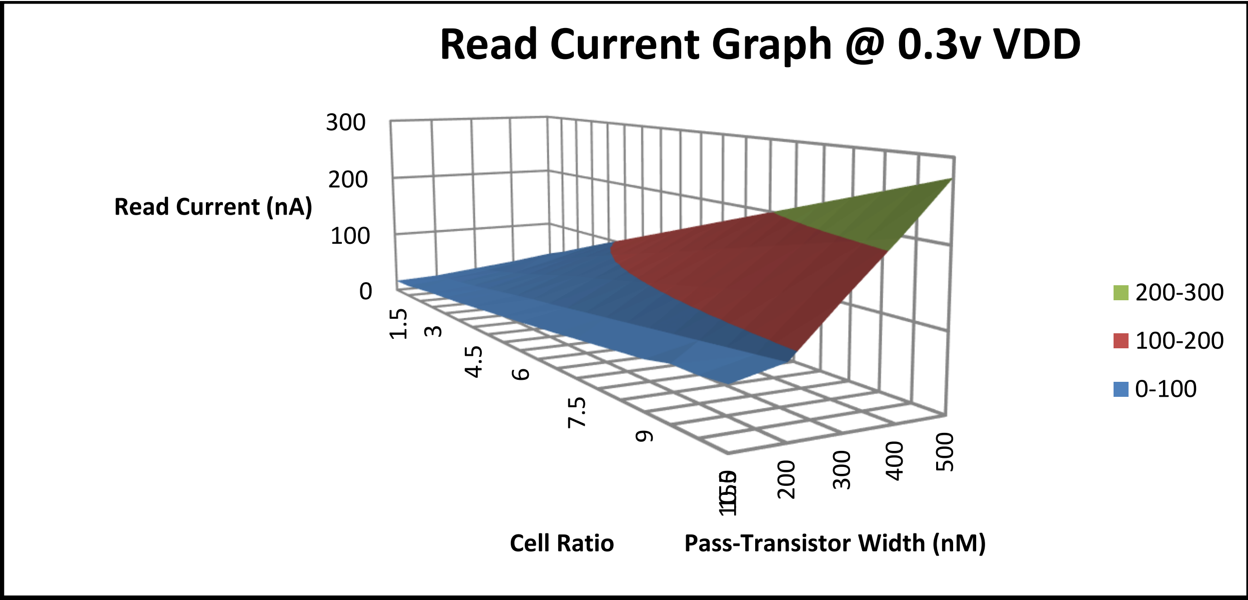

Figure 27: A 3-dimentional illustration of Read Current vs Cell Ratio vs Pass Transistor Width for a 6T cell at VDD=0.3V.

To further analyze the current behavior in the 6T SRAM, it is possible to closely investigate the cell current behavior in a fixed voltage and pass-transistor width condition while varying the cell ratio. Further analysis shows a quadratic relationship in the form of $ax^2 + bx + c$ between the read current and cell ratio. This illustrates that as the cell ratio increases, the read current

increases in a quadratic fashion. Figure 28 shows the read current and cell ratio relationship in a 6 transistor cell with a Vdd of 0.3V, with the devices set at minimum width.

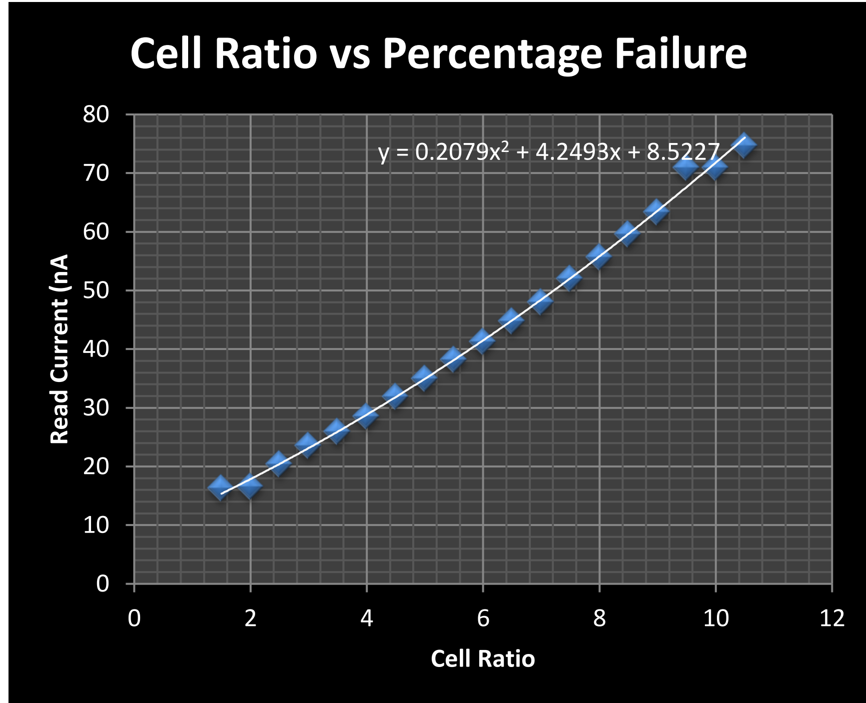

Figure 28: Cell Ratio vs Read Current for a 6T transistor cell at pass transistor with of 150nm at VDD=0.3V.

4.2.2 Simulation Setup for 10T Cell

To calculate the read current in a 10 transistor Alpha cell design, node Q was pre-set to the value 0 (0 volts) and node Qb was set to 1 (VDD). Then the read operation was done by pre-charging the bit line and bit line Bar (BL, and BLB) to VDD voltage. The write word line (WWL) was set to 0 to close the read path through M6. The read word line (WL) was set to VDD to open the read path through M10. The current through M10-M8 was measured at VSS. Figure 29 illustrates the described setup.

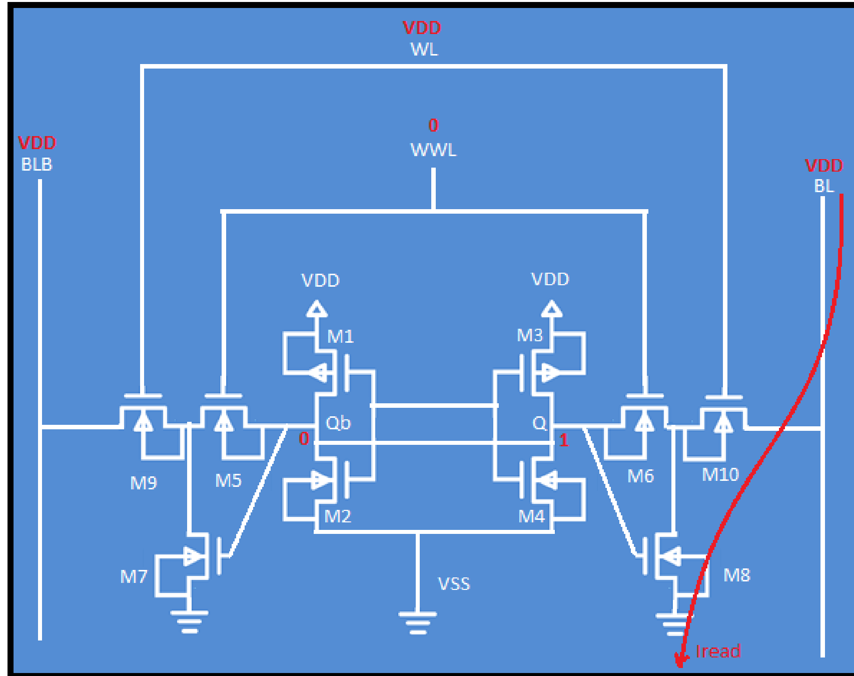

Figure 29: A read operation in the 10T SRAM cell.

The 10T Alpha cell was simulated at two different VDD voltages, 0.2 volts and 0.3 volts. For each of these voltages, the sizing methodology described in section 3.1.3 was used to generate a wide range of current data. For each setup, a 5000 sample Monte Carlo analysis for variation and mismatch was performed on the SRAM design. Hysteresis graphs were drawn comparing the read currents against a number of samples. Then the "mean" read current was extracted and was used for graphing and compression. Figure 30 and Figure 31 show the read current variation in 0.2V and 0.3V VDD respectively.

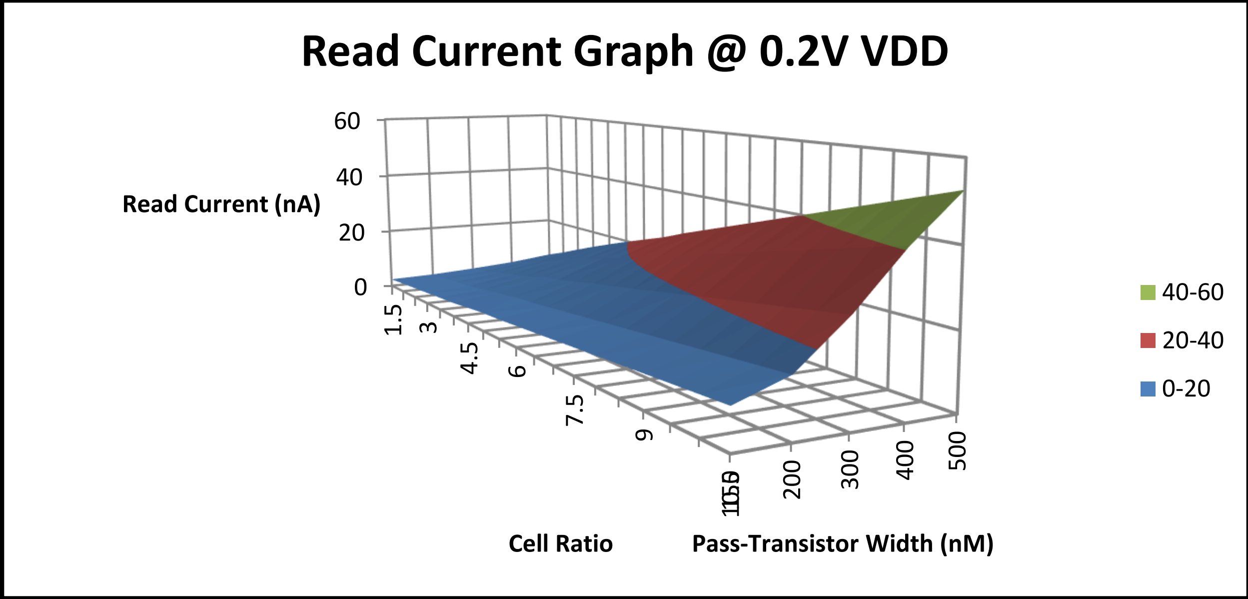

Figure 30: A 3-dimentional illustration of Read Current vs Cell Ratio vs Pass Transistor Width for the 10T cell at VDD=0.2V.

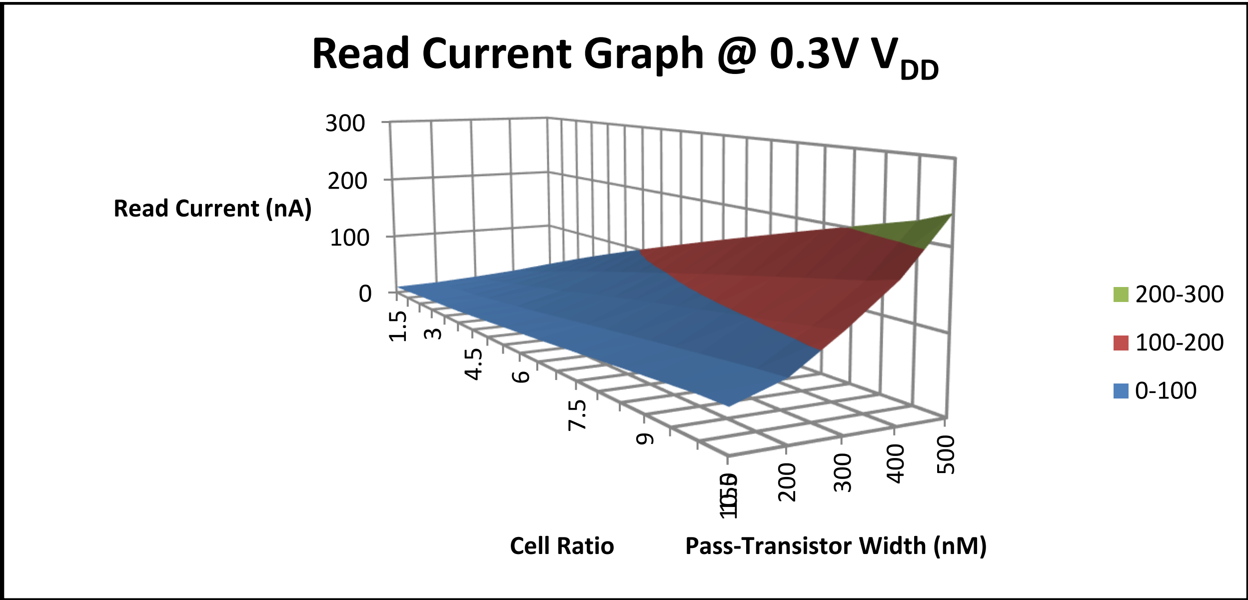

Figure 31: A 3-dimentional illustration of Read Current vs Cell Ratio vs Pass Transistor Width for the 10T cell at VDD=0.3V.

To further analyze the current behavior in the 10 transistor Alpha SRAM, It is possible to closely investigate the cell's current behavior in a fixed voltage and pass-transistor width condition while varying the cell ratio. Further analysis shows a quadratic relationship in the form of $ax^2 +$

$bx + c$ between read current and cell ratio which is already seen in 6T SRAM design. This illustrates that as the cell ratio increases, the read current increases in a quadratic fashion.

4.3 Read Current Comparison

Figure 32 and Figure 33 show the comparison between the 6T and 10T cells' read currents, respectively. The comparison shows that in the 65nm technology class, the 6T cell has a higher read current than the designed 10T cell. Therefore, it can be concluded that the 6 transistor cell has a faster read operation with the same Cell Ratio and Pass-transistor width. However, 6T designs illustrate lower read stability, even though their performance is slightly higher than that of their 10T counterparts. But this higher read current is not remarkable, being in the order of tens of nano amps. On the other hand, 10T cells show a lower read current with the same Cell Ratio and Pass-transistor width. This fact is very significant when designing with power optimization in mind. The more stable 10T cells also consume lower static power due to their lower read current. This is an extremely valuable characteristic, as the ultimate goal of a subthreshold design is to reduce overall power usage in the designed device.

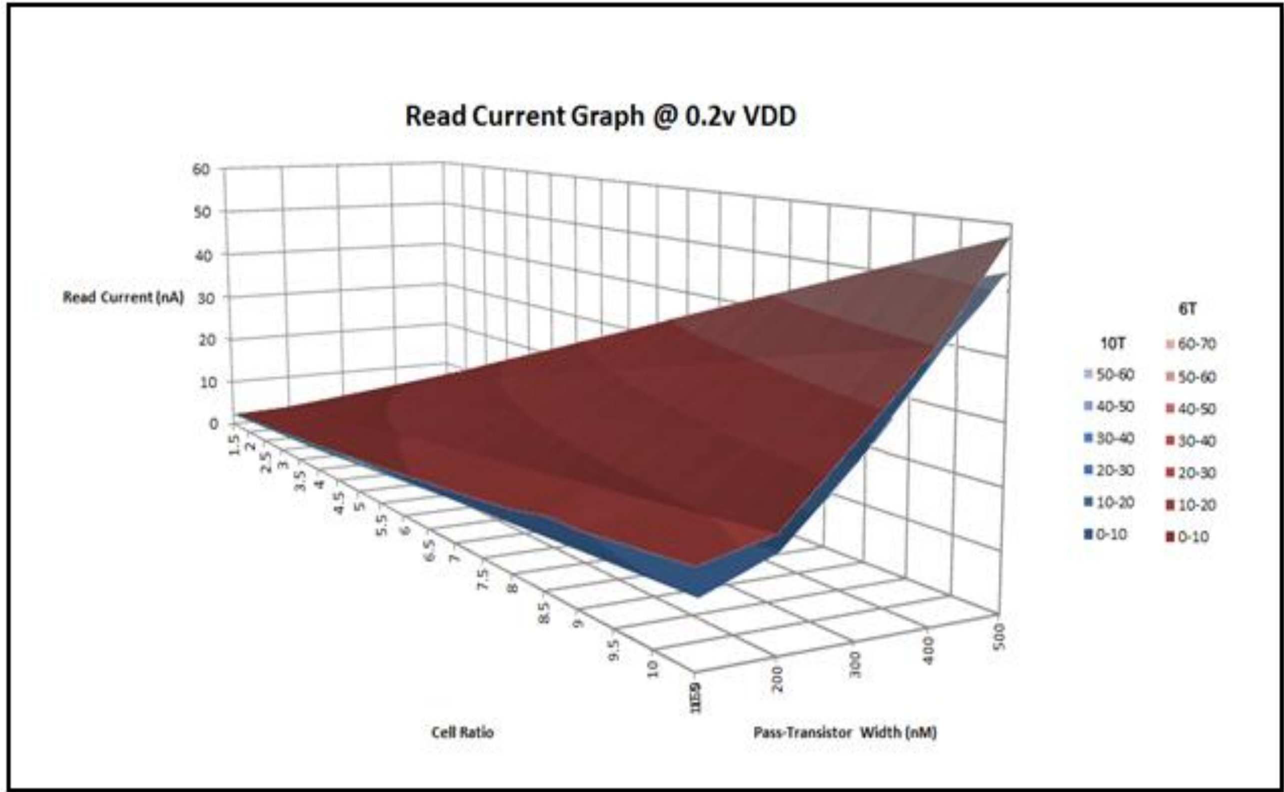

Figure 32: A 3-dimentional comparison of Percentage Read Failure vs Cell Ratio vs Pass Transistor Width graphs of 6T and 10T cells at VDD=0.2V.

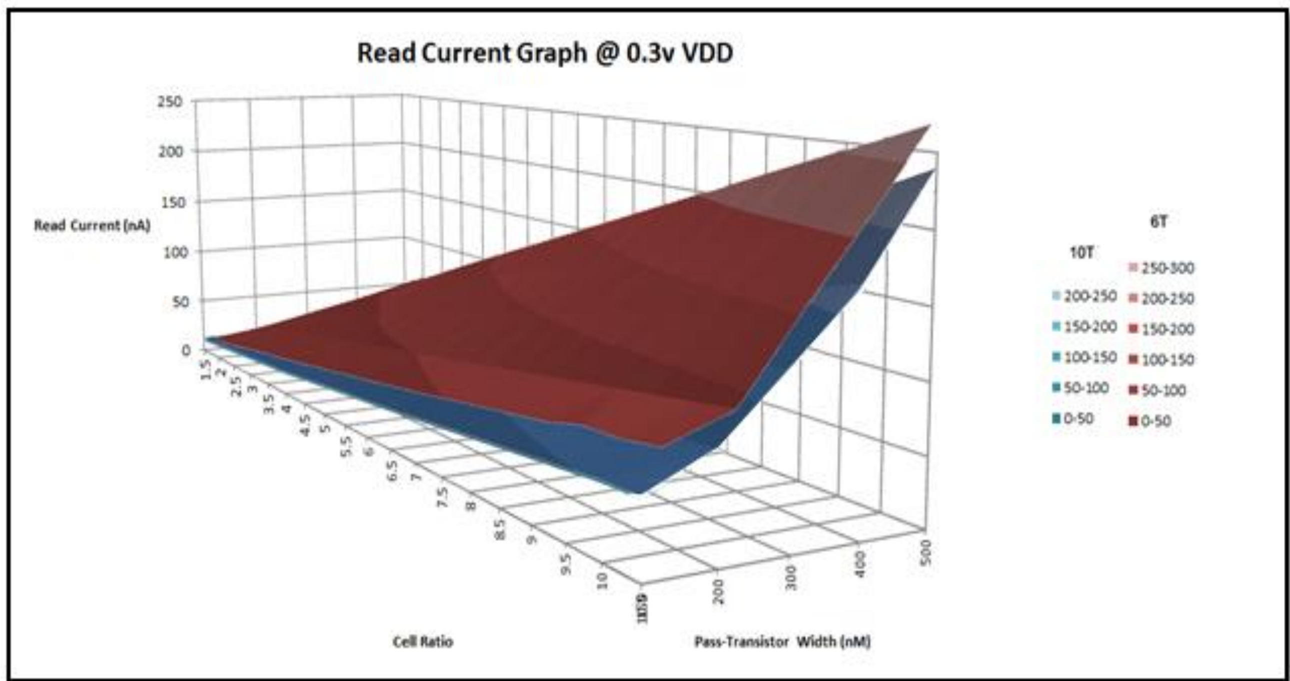

Figure 33: A 3-dimentional comparison of Percentage Read Failure vs Cell Ratio vs Pass Transistor Width graphs of 6T and 10T cells at VDD=0.3V.

Chapter 5

Leakage Current Comparison

The ultimate goal of this chapter is to analyse the standby leakage current of a subthreshold 6T cell to that of the subthreshold 10T design. It then compares these cells' "Leakage Current" in a 3-dimentional fashion. These comparisons then can help designers in finding optimal designs based on "Leakage Current" criteria. Figure 33 to 35 will be used as a reference for the rest of this chapter.

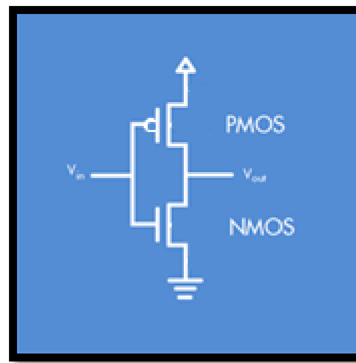

Figure 34: Simple CMOS inverter.

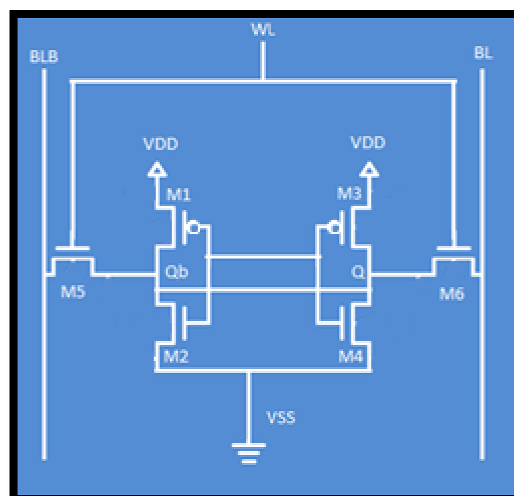

Figure 35: A schematic for 6T SRAM cell.

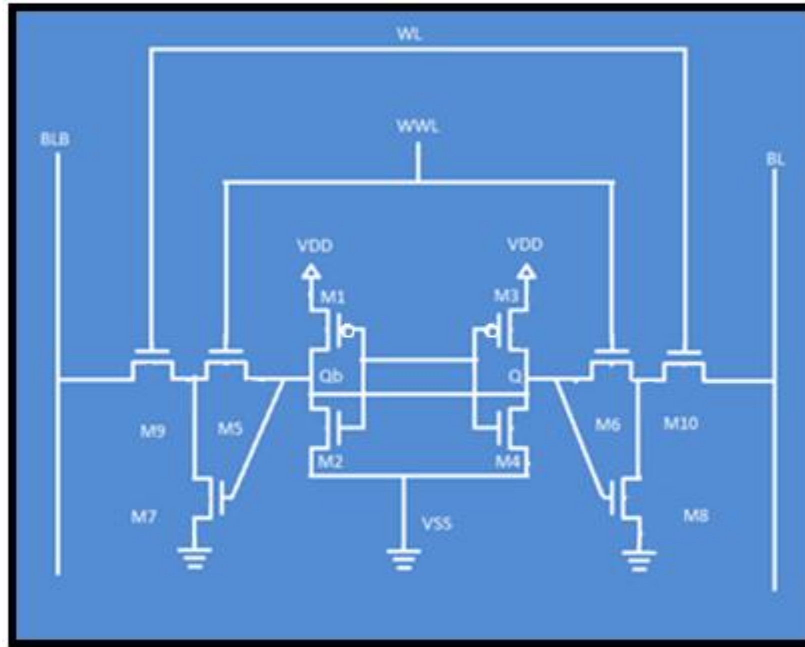

Figure 36: A schematic for the 10T SRAM cell.

5.1 SRAM Leakage Current Fundamentals

Figure 36 shows the structure of the conventional 6T SRAM cell with highlighted leakage currents. This figure demonstrates the four main sources of major leakage current in 6T SRAM cells, based on a complementary metal oxide semiconductor design. The first major leakage current, is Gate Leakage due to a very thin gate oxide, $I_{LeakageGate,\ which}$ becomes the dominant leakage source for CMOS technologies beyond 45nm. As the gate oxide becomes extremely thin, gate leakage increases dramatically. The second current component is the Junction Leakage current ($I_{JunctionLeakage}$). $I_{JunctionLeakage}$ occurs due to the heavily doped halo doping profile [28]. The junction leakage occurs from the source or drain to the substrate through the reverse biased diodes when a transistor is OFF. It is an exponential function of doping concentration and reverse biasing voltage across the junction. The third main leakage source is the Gate Induce Drain Leakage current ($I_{GIDLeakage}$). $I_{GIDleakage}$ is due to high field effect in the Drain junction of a MOS transistor. Both $I_{GIDLeakage}$ and $I_{JunctionLeakage}$ also decrease dramatically with an increase in supply voltage. The fourth major leakage component is the subthreshold leakage current

($I_{SubthresholdLeakage}$). $I_{SubthresholdLeakage}$ is produced when the gate to sources voltage (V_{GS}) is lower than the Threshold voltage (V_T). Supply voltage scaling can effectively reduce the total cell leakage current and the subthreshold leakage current due to Low Threshold voltage (V_T).

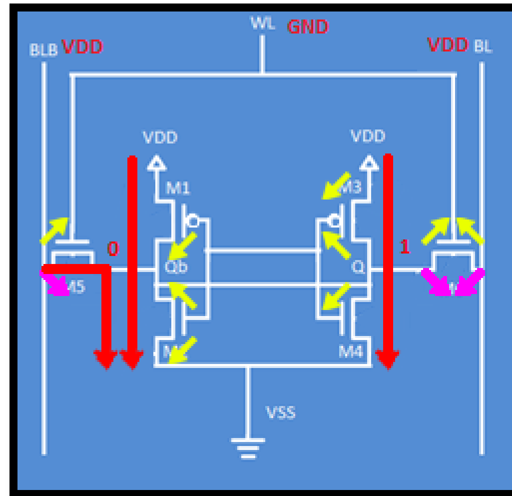

Figure 37: Four main sources of major leakage current in 6T SRAM cell base on CMOS design (Red=Subthreshold Leakage Purple=Junction Leakage Yellow = Gate Leakage).

5.2 Subthreshold Leakage

Subthreshold leakage current is the drain-source current of a transistor when the gate-source voltage is lower than the threshold voltage. With these conditions, transistors are in weak inversion mode. The subthreshold current is mainly composed of diffusion current [29]. For sub threshold leakage power reduction, optimal transistor sizing is essential. Another important consideration is transistor threshold voltage. With successive technologies, supply voltage is being uniformly scaled down. The transistor delay is inversely proportional to the difference of supply and threshold voltage [30]. V_T must be scaled down proportionally with each technology node to maintain circuit performance. This leads to exponential increase in sub threshold leakage current, making the subthreshold component of leakage current the dominant factor among the three leakage components. In a 6T SRAM cell as in Figure 35, the components of the subthreshold current are the VDD to ground components, and the bit-line to ground component. When logic ‘0’ is stored in node Q, there is a significant subthreshold leakage through transistor

M1 to the ground, and from M2 though pass-transistor M5 to the ground. This happens because of voltage deference created between node Q and two high voltage nodes V_{DD} and BL. The other component of subthreshold leakage is from V_{DD} through M3 to the ground. Because node Qb is storing logic ‘1’, the voltage difference between this node and V_{DD} and BL is low. Therefore, this component of subthreshold leakage is extremely small and negligible.

After analysing the sources of leakage current in the 6T SRAM cell, the same method can be used to analyse the leakage in the 10T SRAM cell. It is clear that the 10T SRAM adds more leakage paths by the introduction of transistors M7 and M8. Two additional leakage routes are introduced from the bit-line to the ground. Therefore, it is expected that the 10T will have a higher leakage than a 6T design.

5.3 Device Sizing for Simulation

This section describes the methodology used for sizing the 6 transistor and 10 transistor SRAM cells discussed in this paper to collect a comparable set of leakage current data form each design.

5.3.1 6T Cell Sizing for Simulation

To keep the unity in design methodology throughout this paper and to generate a comparable result, the PMOS to pass NMOS ratio (β) of the 6 transistor SRAM cell design was chosen to be one (β=1). In the process of simulation for each fixed $V_{DD,}$ the pass-transistor sizes were set to 150nm as the minimum width and were varied to 500nm in the different simulation setups. In each simulation with a fixed V_{DD} and fixed pass-transistor width, the cell ratio (CR) was varied between 1.5× to 10.5×. This approach helps to create a 3-dimentional graph of the leakage current vs pass transistor width vs cell ratio at a fixed supplied voltage.

5.3.2 10T Cell Sizing for Simulation

In the 10T cell design, to keep the unity in design methodology throughout this paper and to generate a comparable result to the 6 transistor design. which has a fundamentally different approach for controlling the read current, the PMOS to pass NMOS ratio (β) is chosen to be one (β=1). In the process of simulation for each fixed VDD the pass-transistor sizes are set to 150nm as the minimum width and were varied to 500nm in different simulation setups. In each simulation with a fixed VDD and fixed pass-transistor width, the cell ratio ($CR\alpha$) was varied between 1.5× to 10.5× of the inverter transistor width. Doing so helps to create a 3-dimentional graph of the leakage current vs pass transistor width vs cell ratio at a fixed supplied voltage which is comparable to the 6 transistor graphs.

5.4 Leakage Current Simulation

This section shows the simulation steps and results for the leakage current of 6 transistor and 10 transistor SRAM cells and compares the leakage current of the designs.

5.4.1 Simulation Setup for 6T Cell

To calculate the leakage current in a 6T cell design, node Q was pre-set to the value 0 (0 volts) and node Qb was set to 1 (VDD). The bit-line and bit-line Bar (BL, and BLB) were kept at VDD voltage. The word line (WL) was connected to ground to close the M6 gate. The current through M4 was measured at VSS. Figure 38 illustrates the described setup.

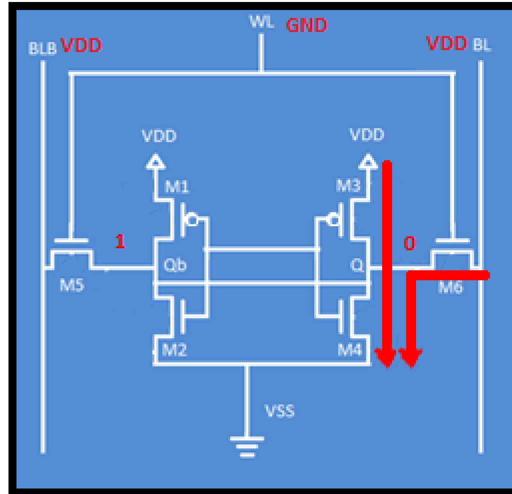

Figure 38: Major leakage currents in 6T SRAM cell base on CMOS design.

The 6T SRAM cell was simulated at two different VDD voltages, 0.2 volts and 0.3 volts. For each of these voltages, the sizing methodology described in section 3.1.2 was used to generate a wide range of current data. At each chosen VDD, for a set pass transistor width, the cell ratio was varied and the leakage was calculated for each setup. Figure 39 illustrates the leakage current measurements' result for a 6T SRAM cell under supply voltage of 0.3V and with the use of minimum sized devices (pass-transistor width of 150nm). For each measurement, a 5000 sample Monte Carlo analysis for variation and mismatch was performed on the SRAM design. Hysteresis graphs were drawn comparing the leakage currents against number of samples, and the "mean" leakage current was extracted and used for graphing and compression.

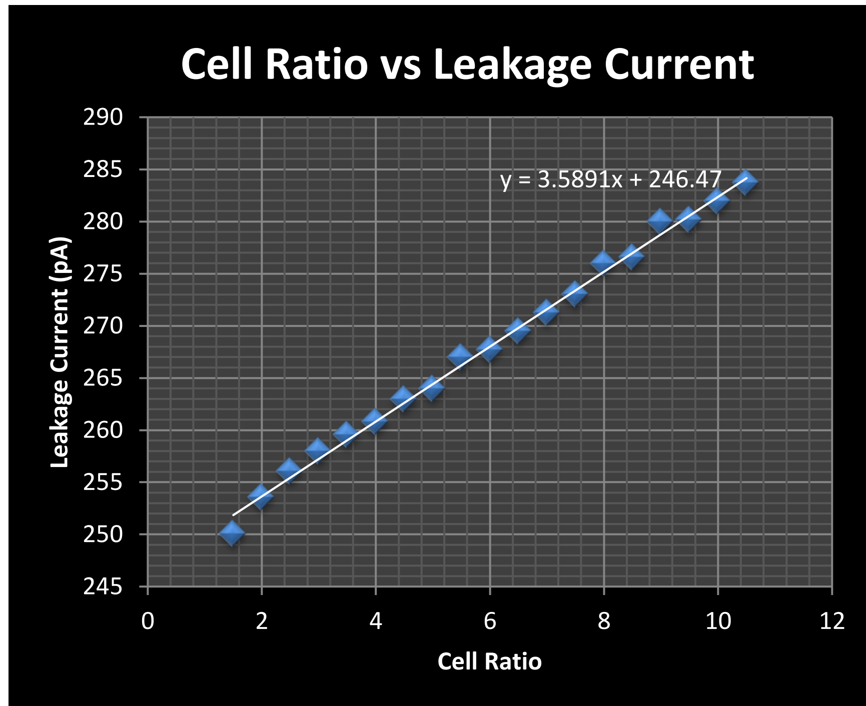

Figure 39: Cell Ratio vs Leakage Current for a 6T transistor cell with pass transistor width of 150nm at VDD=0.3V

From the analysis, the approximate function that relates the leakage current and CR can be drived.

(8) $$Leakage\ Current = a\,x + b$$

where a and b are constants dependent on the transistors' width, and x is the pull-down ratio.

From analysing the generated graphs, it can be concluded that for a fixed device voltage, the leakage current and CR have a linear relationship in 6T SRAM cells in 65nm technology.

If the result of similar simulations for different widths of the pass transistors (from 150nm to 500nm) are combined, 3-dimentional graphs can be generated to shows the change in leakage current value for different simulation setups. Figure 40 shows this 3-dimentional graph @ VDD=0.2V. Figure 41 shows this 3-dimentional graph @ VDD=0.3V.

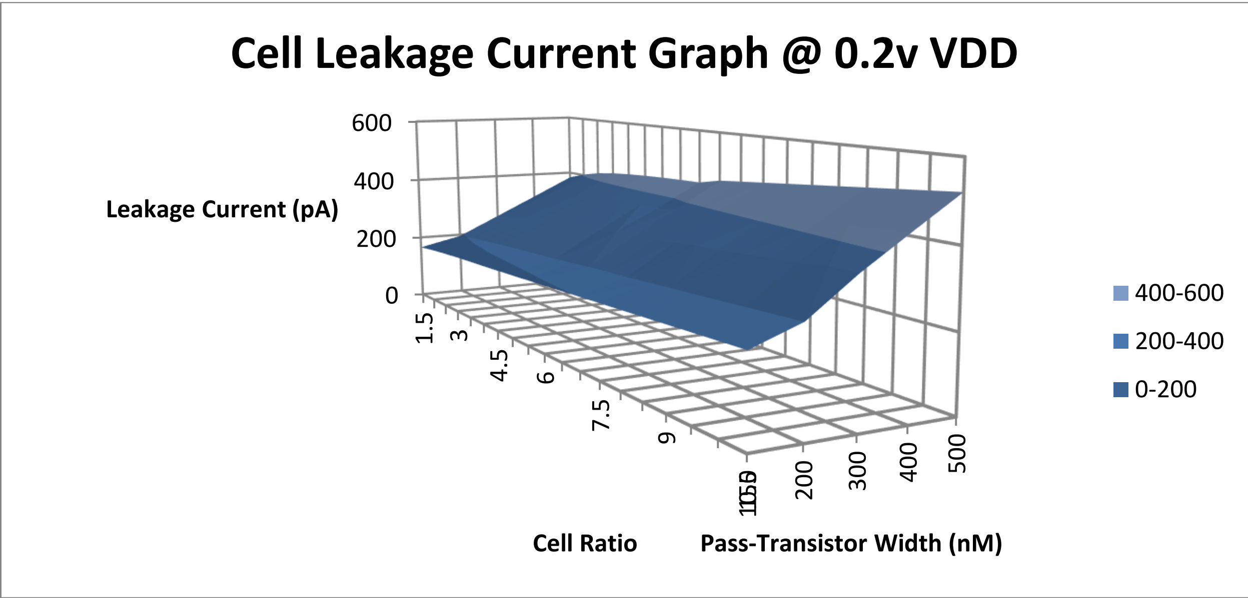

Figure 40: A 3-dimentional illustration of Leakage Current vs Cell Ratio vs Pass Transistor Width for the 6T cell at VDD=0.2V.

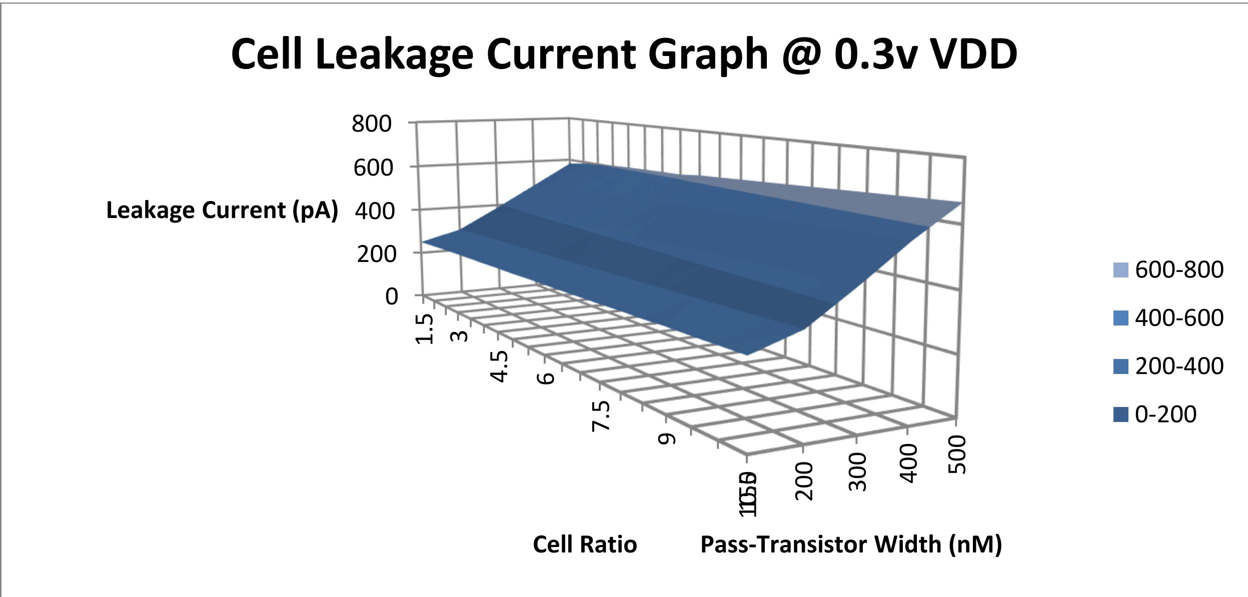

Figure 41: A 3-dimentional illustration of Leakage Current vs Cell Ratio vs Pass Transistor Width for the 6T cell at VDD=0.3V.

5.4.2 Simulation Setup for 10T Cell

To calculate the leakage current in the 10T design, node Q was pre-set to the value 0 (0 volts) and node Qb was set to 1 (VDD). Then the bit line and bit line Bar (BL, and BLB) were pre-charged to VDD voltage. The write word line (WWL) was connected to the ground to close the read path through M6. The read word line (WL) was connected to the ground as well to close the read path through M10. The current through M7 and M2 was measured at VSS. Figure 42 illustrates the described setup.

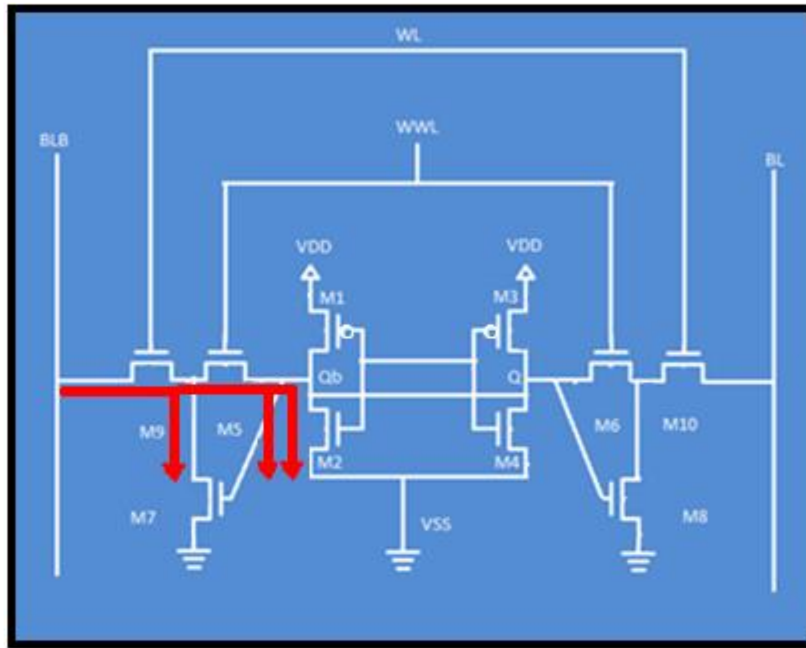

Figure 42: Major leakage currents in 10T SRAM cell base on CMOS design.

The 10T SRAM cell was simulated at two different VDD voltages, 0.2 volts and 0.3 volts. For each of these voltages a sizing methodology described in section 3.1.3 was used to generate a wide range of current data. At each chosen VDD, for a set pass transistor width, the cell ratio was varied and the leakage was calculated for each setup. Figure 43 illustrates the leakage current measurements' result for a 10T SRAM cell under a supply voltage of 0.3V and with the use of minimum sized devices (pass-transistor width of 150nm). It should be noted that for each measurement, a 5000 sample Monte Carlo analysis for variation and mismatch was performed on

the SRAM design. Hysteresis graphs were drawn comparing the leakage currents against number of samples, and the "mean" leakage current was extracted and was used for graphing and compression.

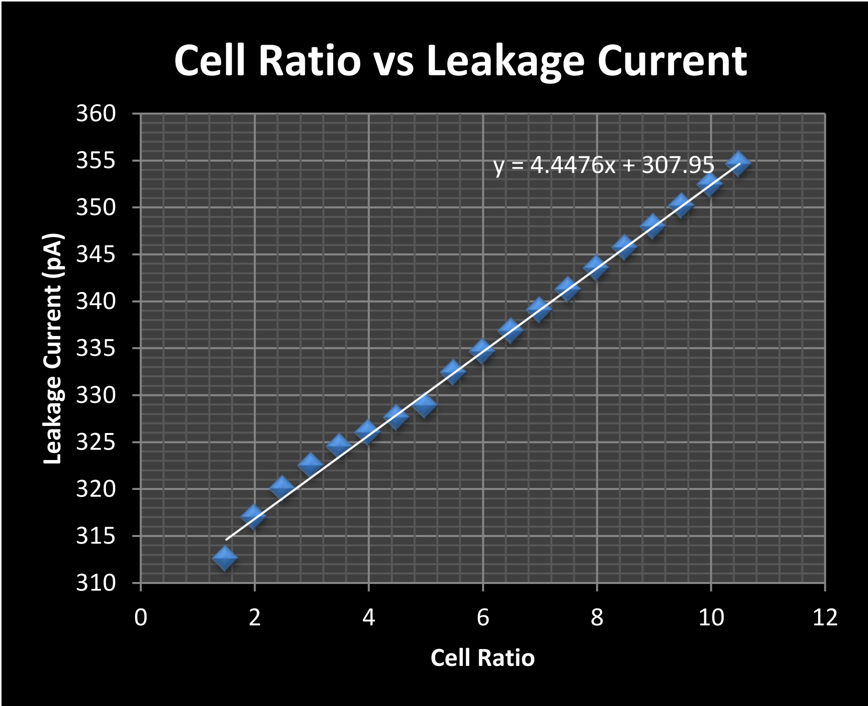

Figure 43: Cell Ratio vs Leakage Current for a 6T transistor cell with pass transistor width of 150nm at VDD=0.3V.

From the analysis, the approximate function that relates the leakage current and CR can be derived.

(9) $$Leakage\ Current = a\,x + b$$

where a and b are some constants dependent on the transistors' width, and x is the pull-down ratio.

On analysing the generated graphs, it can be concluded that for a fixed device voltage, the leakage current and CR have a linear relationship in 10T SRAM cells in 65nm technology.

If the result of similar simulations for different widths of the pass transistors (from 150nm to 500nm) are combined, 3-dimentional graphs can be generated and shows the change in leakage current value for different simulation setups. Figure 44 shows this 3-dimentional graph @ VDD=0.2V. Figure 45 shows this 3-dimentional graph @ VDD=0.3V.

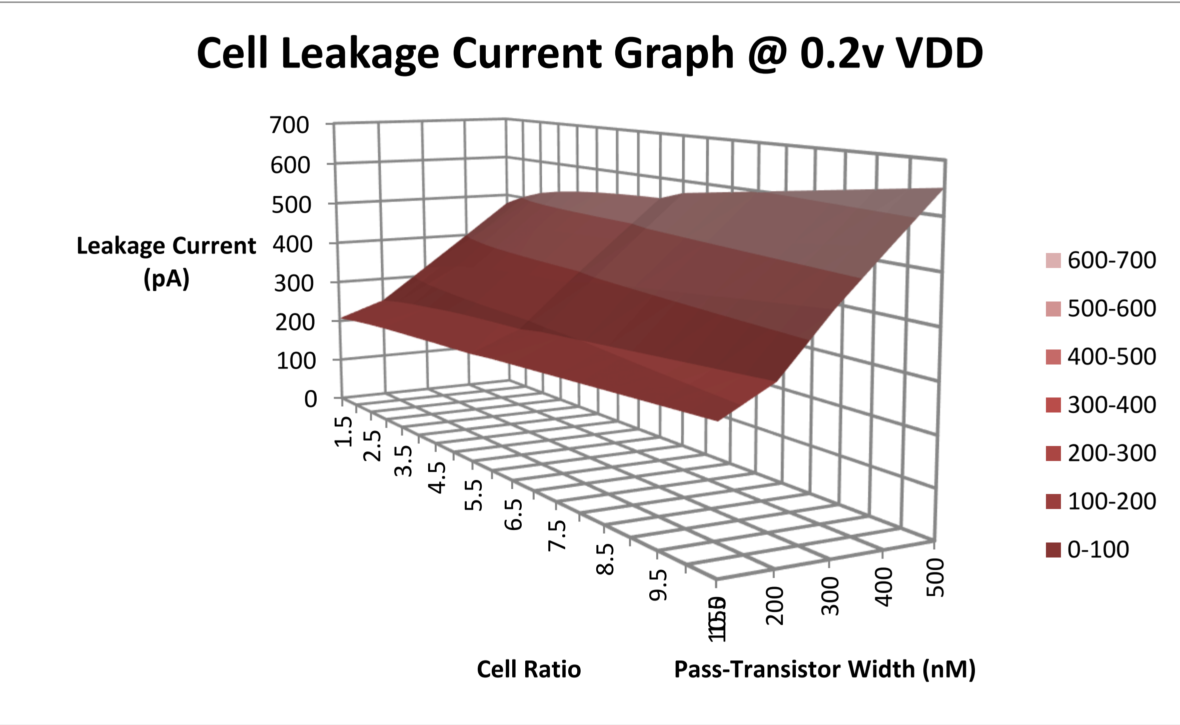

Figure 44: A 3-dimentional illustration of Leakage Current vs Cell Ratio vs Pass Transistor Width for the 10T cell at VDD=0.2V.

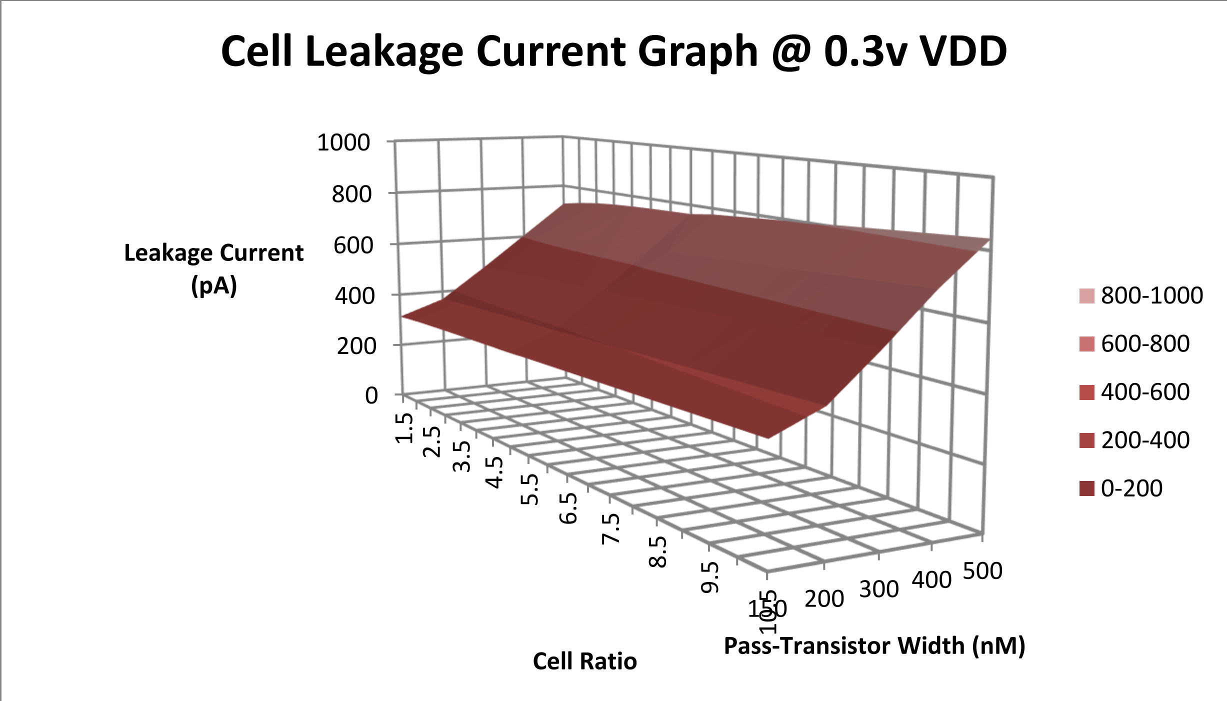

Figure 45: A 3-dimentional illustration of Leakage Current vs Cell Ratio vs Pass Transistor Width for the 10T cell at VDD=0.3V

5.5 Leakage Current Comparison

Figure 46 and Figure 47 show the comparison between 6T and 10T cells leakage current respectively. In the 65nm technology class, the 10T cell has higher leakage currents than the 6T cell design. The difference is around 20 percent. This is an extremely valuable characteristic, as the ultimate goal of a subthreshold design is to reduce overall power usage in the designed device.

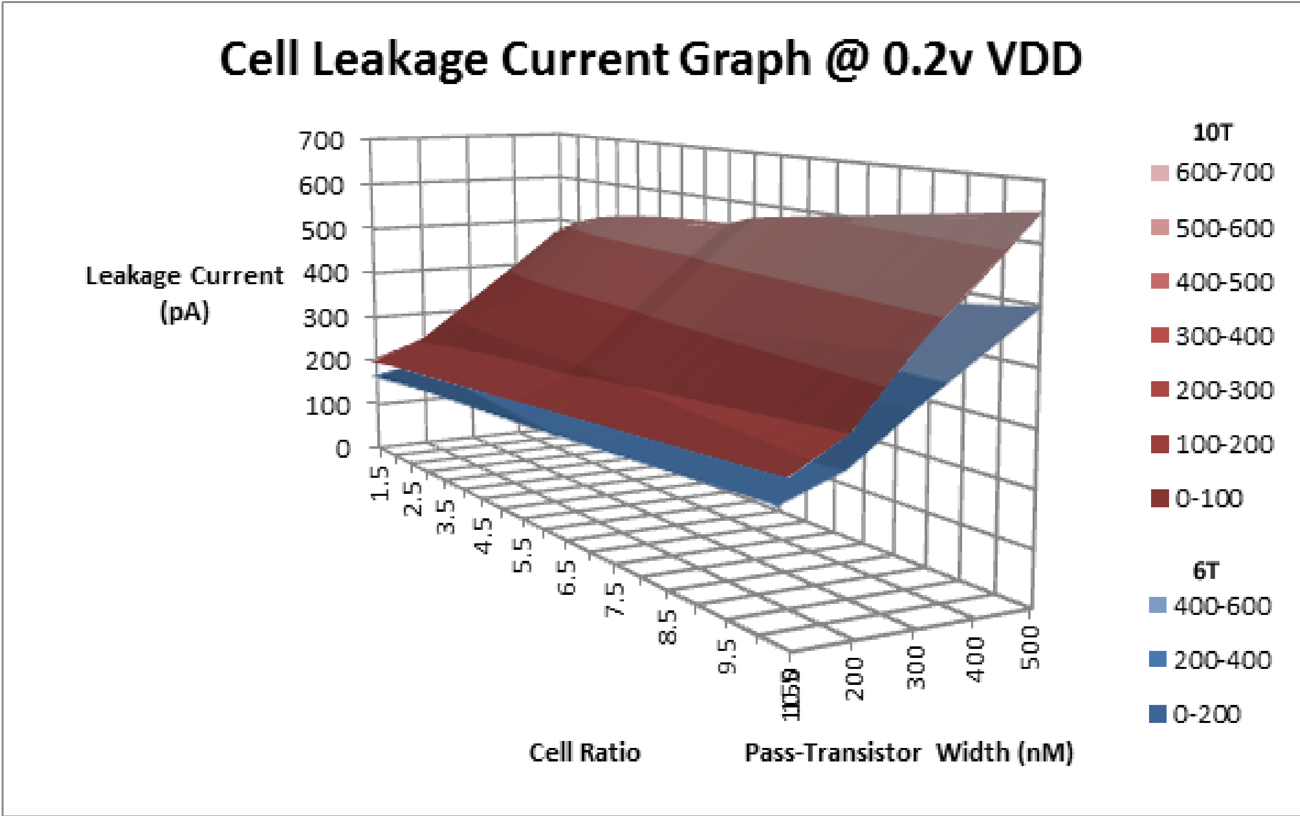

Figure 46: A 3-dimentional comparison of Leakage Current vs Cell Ratio vs Pass Transistor Width graphs of 6T and 10T cells at VDD=0.2V.

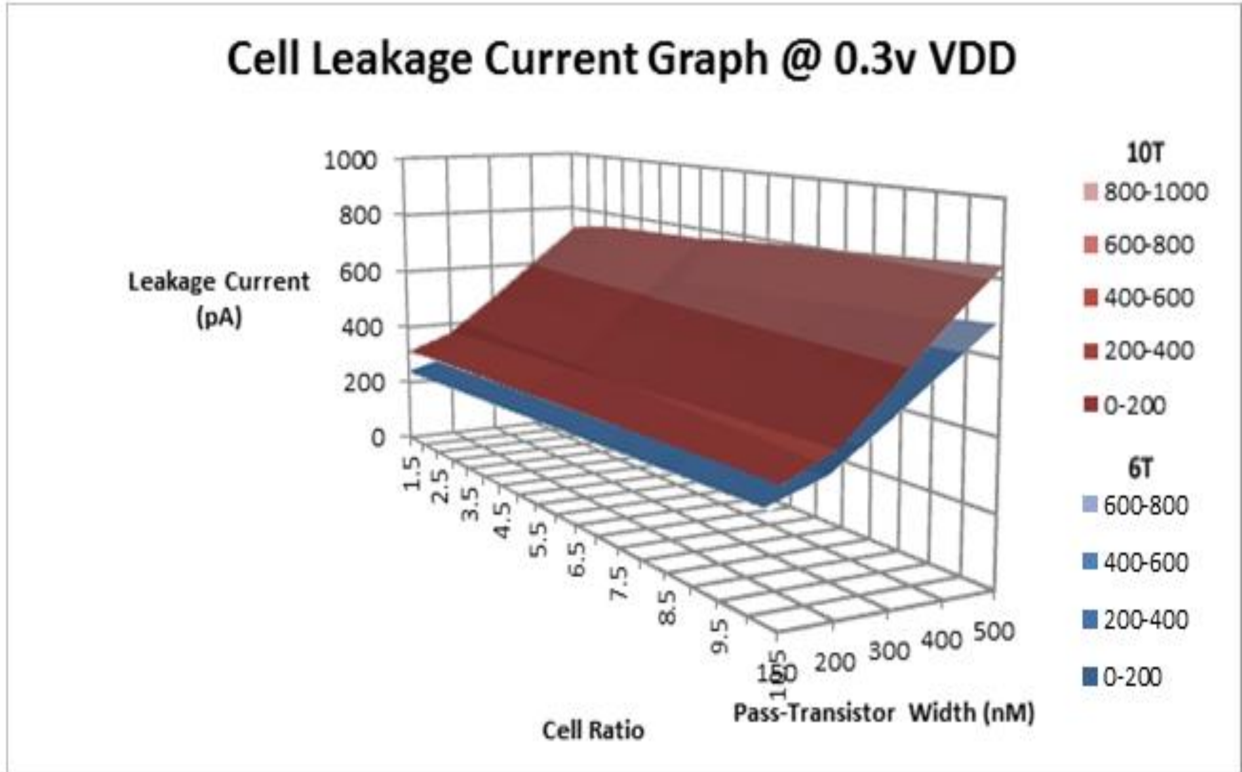

Figure 47: A 3-dimentional comparison of Leakage Current vs Cell Ratio vs Pass Transistor Width graphs of 6T and 10T cells at VDD=0.3V.

Chapter 6

Static Write Margin Comparison

The goal of this chapter is to analyze the design process of a conventional subthreshold 6 transistor SRAM cell (Figure 49) along with the subthreshold 10 transistor SRAM structure (Figure 50) with respect to their Write Margin. The ultimate purpose is to compare these designs with respect to their Write Margin in a 3-dimentional fashion. These comparisons then can help designers find an optimal width and supply voltage for a particular design while minimizing the design's susceptibility to process variation. Figure 49 to 50 will be used as a reference for the rest of this chapter.

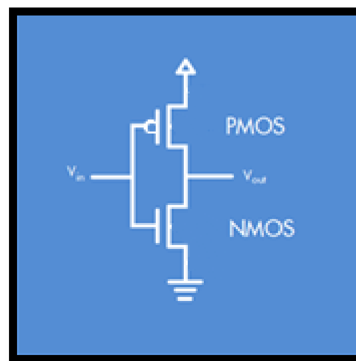

Figure 48: Simple CMOS inverter.

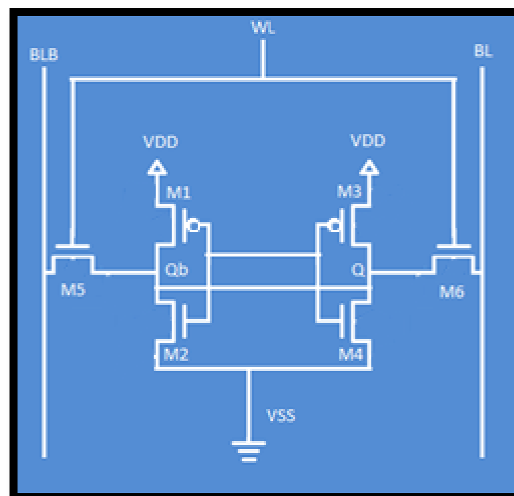

Figure 49: A schematic for 6T SRAM cell.

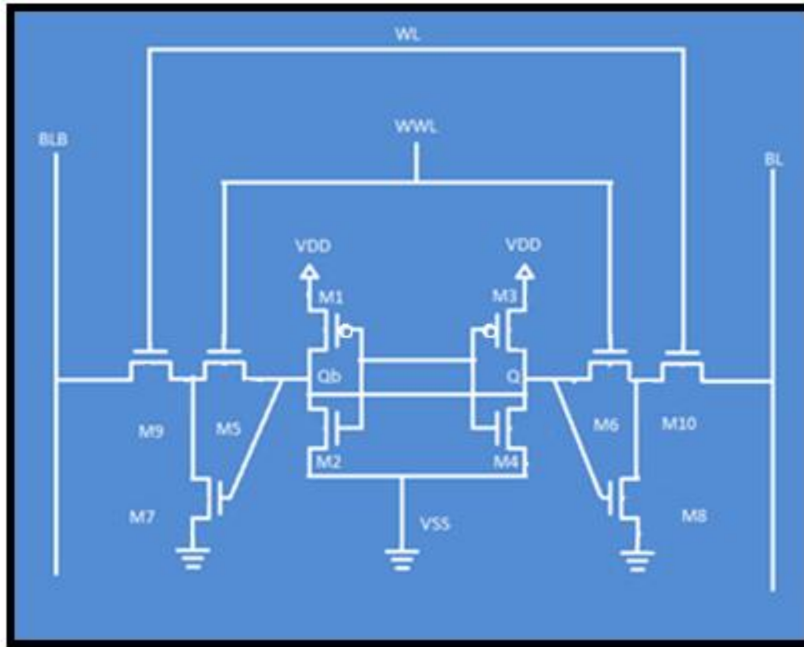

Figure 50: A schematic for the 10T SRAM cell.

6.1 Device Operation and Sizing

This section describes the methodology used for sizing 6 transistor and 10 transistor devices discussed in this paper to achieve an optimal Write Margin for each device. The sized devices are then used to collect a comparable set of data to be analysed and used to draw conclusions.

6.1.1 6T SRAM Cell Write Operation and Write-Path Sizing

In 6T SRAM write operation, for example for writing 1, initially one of the bit-lines is pre-charged to the voltage VDD and the other is connected to GND. While writing, the wordline (WL) is turned on and the ground voltage VGND is low. Therefore, the bit line connected to the

internal node (Qb to Q) holding a 1 will be discharged, and conversely, the other internal node holding a 0 will be pulled up to VDD. For example, writing a 1. A value 0 is stored at Q. The write cycle is started by pre-charging the node BL to VDD and setting node BLB to GND. Then the wordline is pulled to VDD, which opens the M5 and M6 paths. During a correct write operation, BL is precharged to VDD, which makes a M5-M2 path that will pull the node Q to VDD. On the other hand, BLB is set to GND; therefore, a M3-M6 path will discharge the node Qb. Writing a 0 will happen by pre-charging the BLB to VDD and setting BL to GND.

The pull up ratio affects the stability of SRAM cells during write operations. during which, the critical part of the circuit is the voltage divider formed by the pull up and access transistors whose size ratio defines the pull-up ratio. The pull up ratio is nothing but a ratio between sizes of the load transistor (pull up) to the size of pass transistor

$$PR = \frac{pull\text{-}up\ PMOS\ width}{Pass\ NMOS\ width} \quad (11)$$

The bit-line pulled to GND pulls the node storing ‘1’ to GND to flip the state. The strength of the pull-up transistor determines the difficulty of writing data or flipping the state of cells. With an increased pull-up ratio, it is more difficult to write or pull the node to GND and hence the write margin and write trip voltage is decreased. Thus increasing the pull up ratio during write operations is of no good as it increases the difficulty in writing data into the SRAM Cell.

$$PR = \frac{pull\text{-}up\ PMOS\ width}{Pass\ NMOS\ width} < 1 \quad (10)$$

6.1.2 10T SRAM Cell Write Operation and Write-Path Sizing

The 10T SRAM has a decoupling read/write operation. During write mode, both WL and WWL word lines are enabled with some boost voltage higher than VDD to maintain good write ability, because in the sub-threshold region, write ability is a critical issue. However, in this work, we achieved similar performance by keeping WWL at VDD and boosting the other word line by only 0.1 volts higher than VDD. There are two access transistors on each side which also affect write ability, and both should be ON to successfully transfer the data from the bit line to node Q . By giving boost voltages on word lines, more write margin and less write time are achieved, without an area overhead penalty. To save more area, the ground lines of all transistors are connected to common VGND. The pull up ratio affects the stability of SRAM Cells during write operations just like in a 6T cell.

(12)

$$PR\alpha = \frac{pull\text{−}up\ PMOS\ width}{Pass\ NMOS\ width} < 1$$

6.2 Static Write Margin

6.2.1 Static Write Margin Calculation Method

The VTC behaviour of cross coupled inverters when preforming write operation can be illustrated as butterfly curve just like the read operation. The butterfly curve is an accurate approach with the calculation of the write margin of a particular SRAM cell. The Write Margin or WM of an SRAM cell device can be graphically represented by this butterfly curve as seen in Figure 51. In this figure, one square is fitted inside of the voltage transfer characteristics of the cross coupled inverters of a 6T SRAM cell. The WM can be calculated by measuring the side length of the largest square that can be fitted between two voltage transfer characteristic curves. The rite margin is a good representation of the device's write ability. A bigger square means a larger noise margin and ultimately better write ability of the device [27].

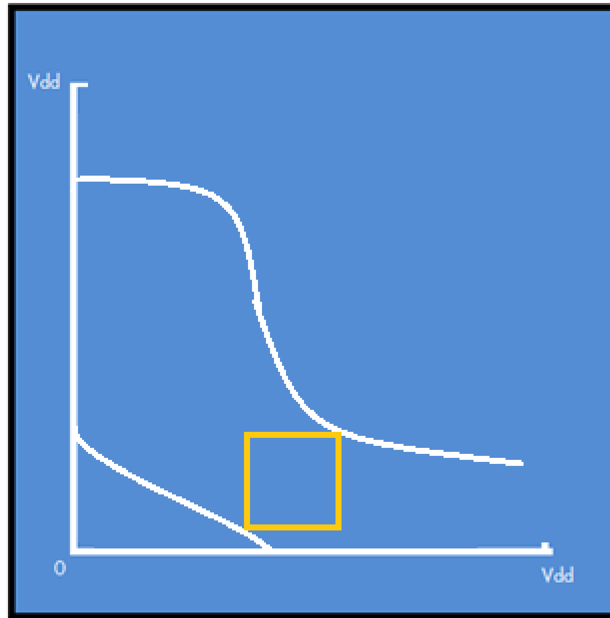

Figure 51: Butterfly curve for a crossed coupled inverter system of a 6T SRAM cell.

It is easy to obtain the WM from the VTC curves graphically; however, calculating WM for a large device variation sample is extremely difficult to calculate graphically. Therefore, the same systematic approach that is used for the calculation of SNM is used [27].

The WM can be found analytically by solving the Kirchhoff equations and applying one of the mathematically equivalent noise margin criteria. But since all calculations will be based on simulated results from a computer aided design tool (Cadence Virtuoso), it is better to find a way to find WM from the simulated DC sweep results from Cadence. To estimate WM values, a procedure is needed that finds values for the diagonals of the largest square as shown in Figure. 51. A method that is quick and easy to use was developed for use together with a standard dc circuit simulator. Figure 52 shows a stylized version of Figure 51 in two coordinate systems which are rotated 45° relative to each other. In the (u, v) system, subtraction of the u values of the normal and mirrored inverter characteristics at a given u yields curve A, which is a measure of the diagonal's length. The maximum and minimum of curve A represent the required maximum squares [27].

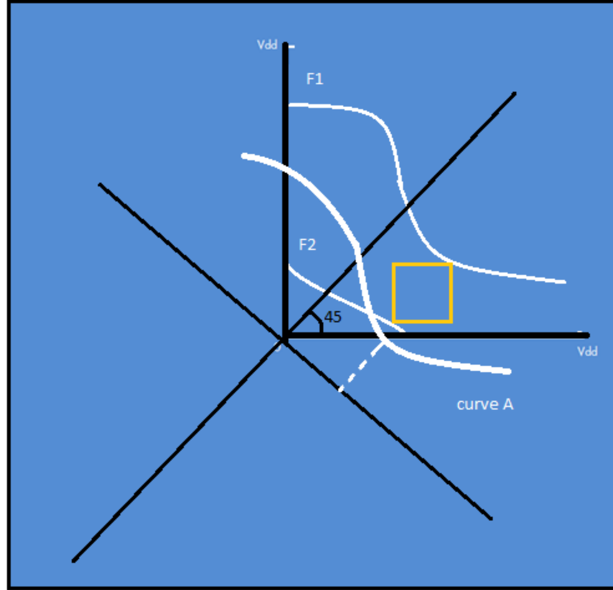

Figure 52: SNM estimation based on the maximum square, using a 45° rotated coordinate system.

Assume that the normal and mirrored inverter characteristics are defined by the functions $y = F_l(x)$ and $y = F_l'(x\ )$,where the latter is the mirrored version of $y = F_2(x)$. To find F_I in terms of u and v, the (x, y) coordinates must first be transformed into the (u, v) system. The required transformation is

(13a)
$$x = \frac{1}{\sqrt{2}}\,u + \frac{1}{\sqrt{2}}\,v$$

(13b)
$$y = -\frac{1}{\sqrt{2}}\,u + \frac{1}{\sqrt{2}}\,v$$

Substitution of (13) in $y = F_l(x)$ gives

(14)
$$v = u + \sqrt{2}\,F_1\left(\frac{1}{\sqrt{2}}\,u + \frac{1}{\sqrt{2}}\,v\right)$$

For F_2', first F_2 is mirrored in the (x, y) system with respect to the u axis, and then it is transformed to the (u, v) system. The required coordinate transformation is now the same as (13) but with x and y exchanged; Substituting in $y = F_2(x)$ gives

$$v = -u + \sqrt{2}\, F_2\left(-\frac{1}{\sqrt{2}}\, u + \frac{1}{\sqrt{2}}\, v\right) \quad (15)$$

Equations (14) and (15) represent the inverters comprising the flip-flop cell. They give u as an implicit function of u. Solutions can be found with a standard dc circuit simulator by translating the equations into circuits, using voltage-dependent voltage sources in a feedback loop as shown in Figure 53. The solutions of (14) and (15) are represented by v_1 and v_2 in Fig. b(a) and (b), respectively. The difference between the two solutions, $v_1 - v_2$, is calculated by the simulator and is represented by curve A in Figure 52 [27].

The value of the minimum point in curve A is the value of the diagonals of the maximum square. Multiplying it by $1/\sqrt{2}$ yields the WM of the SRAM cell.

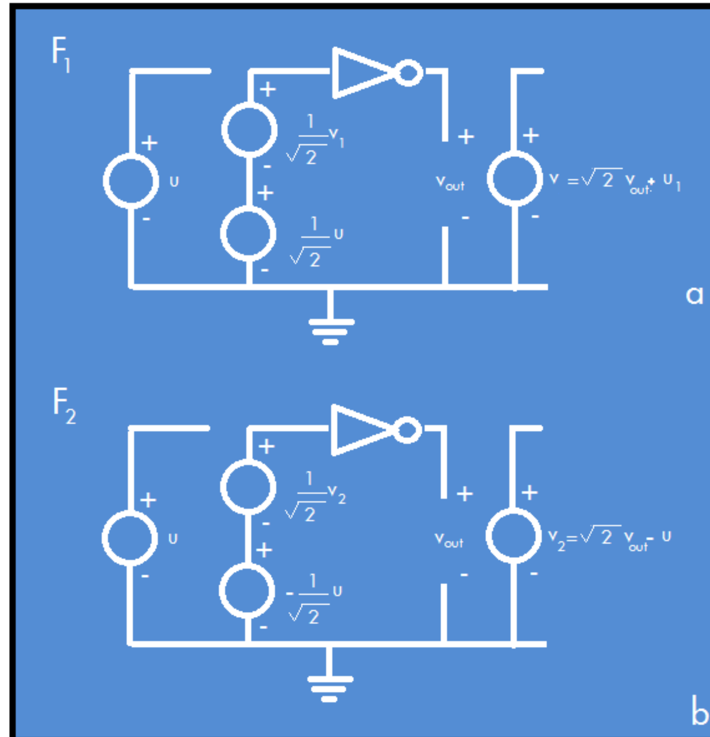

Figure 53: shows the designed cross coupled inverter test bench with the use of this WM calculation methodology in Cadence computer aided design tool.

With use of the cross coupled inverter test bench circuit, which is the circuit equivalent to the graphical transform of VTC curves, extraction of "curve A", and measurement of the best fitted square diagonal size, the value of WM can be measured for 6 transistor and 10 transistor cells. This method essentially separates the cell into two invertor sides and measures the VTC of each side in the same fashion of SNM calculation. Then it subtracts two VTC curves and calculates the diagonal length of the largest fitted square. This method not only decreases the effort of dealing with graphic calculations, it provides a computer-aided friendly solution that can be implemented easily.

6.3 WM Simulation

This section shows the simulation steps and results of Write Margin simulations of 6 transistor and 10 transistor cell designs. To identify the differences between the write ability of these

designed cells, this section also discusses and compares the simulated WM and SRAM read failure of these SRAM cells.

6.3.1 Simulation Methodology

To calculate the butterfly curve, a DC sweep will be performed from –VDD to +VDD on the "u" DC voltage source discussed in section 6.2.1. The DC sweep of the test bench circuit connected to the SRAM cell will output a Voltage Transfer Characteristic curve for each side of the SRAM cell (each inverter side). Figure 54 shows the Voltage Transfer Characteristic curves of both sides of the cell superimposed on a single scale, which is also called the butterfly curve.

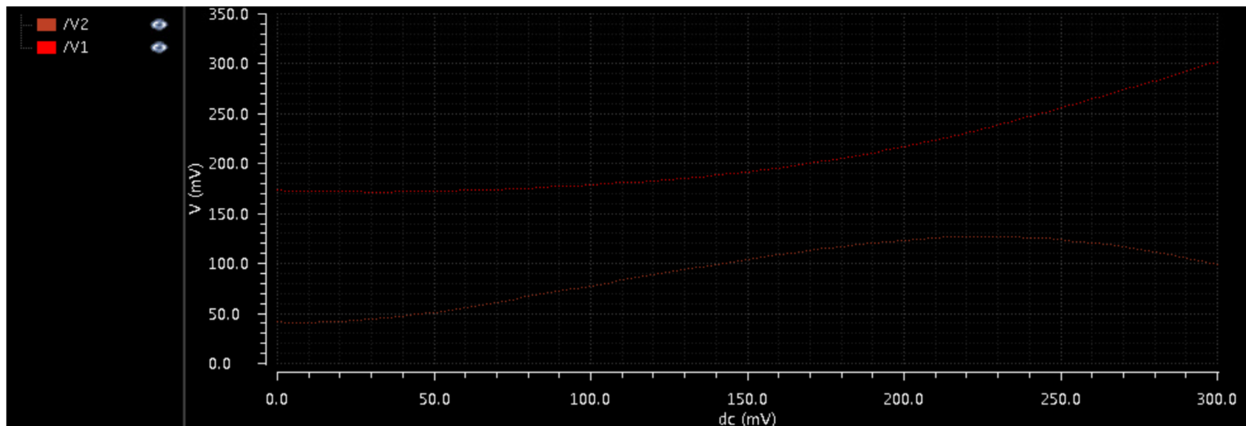

Figure 54: Rotate butterfly curve for 6T SRAM cell with minimum size devices @ 0.3V.

To find the Static Noise Margin following section 6.2.1 methodology, the "difference curve" of the two components of the butterfly curve is calculated. Figure 55 show the difference curve. The minimum of the resulting difference curve which is equal to the diagonal of the best fitted square in the butterfly curve is found. The diagonal value is then used to find the size of the side of each fitted square by multiplying the value by $\frac{1}{\sqrt{2}}$. The side of the best fitted square is considered to be the Write Margin of the device.

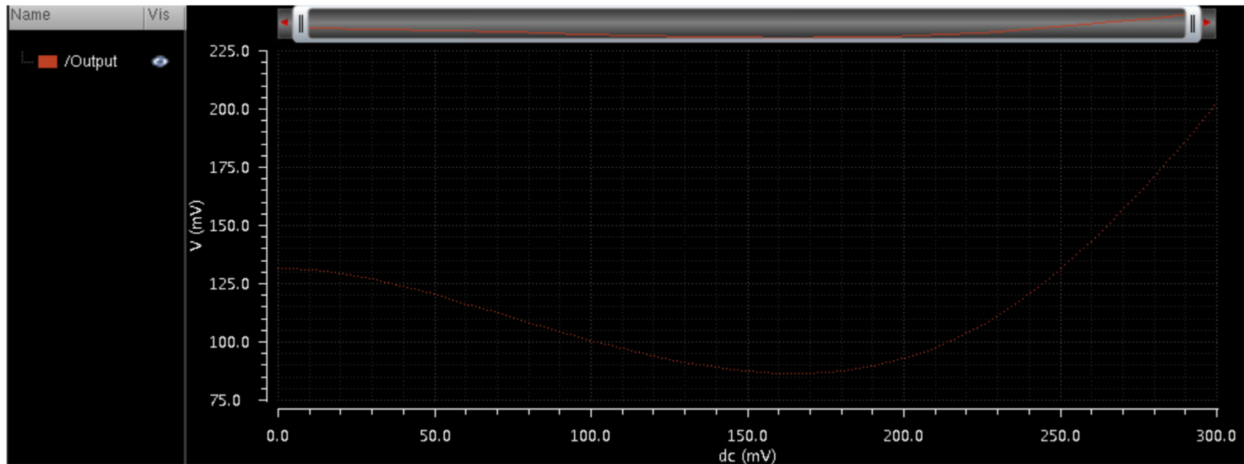

Figure 55: The cumulative curve for 6T SRAM cell with minimum size devices.

To find a realistic measure for the WM of a designed and sized device, a broader picture of device functionality has to be considered for its write ability as well. As discussed in the other sections of this thesis, the presence of device variations and mismatches in the real world can cause a lot of problems that can affect the write ability of a device as well. These problems appear in the transition between design and manufacturing of the actual device. Therefore, process variation and mismatch have to be considered as limiting factors in a design stage, and the final design has to be free of any susceptibility to these factors. To achieve this task for the designed SRAM cells, a 5000 sample Monte Carlo analysis for variation and mismatch was performed on the SRAM designs for the write margins of different setups of the cells. This analysis simply generates 5000 random variation and mismatch scenarios for the same device. To satisfy this chapter's purpose, Monte Carlo analysis was performed on the calculated write margin of each device.

Hysteresis graphs were drawn to illustrate the Write Margins against a number of samples (5000 in total) under device variations and mismatch. Figure 56 shows the hysteresis graph generated for a minimum sized 6T SRAM cell. For each iteration of the simulations, a hysteresis was generated, and from the hysteresis the mean WM and its standard deviation were calculated. At this point, to compare the functionality of the different designs and to demonstrate the improvement of one device through the change of parameters, a 6 sigma analysis was performed

on the data extracted from the hysteresis curves. In the calculation of the 6 sigma, the lower limit for the WM was set to be 100mV, which is considered an extremely desirable noise margin in devices operated in the subthreshold regime. The 6 sigma calculation gives us a vision about the design's robustness and ensures that the rate of operation failure is negligible in billions of samples.

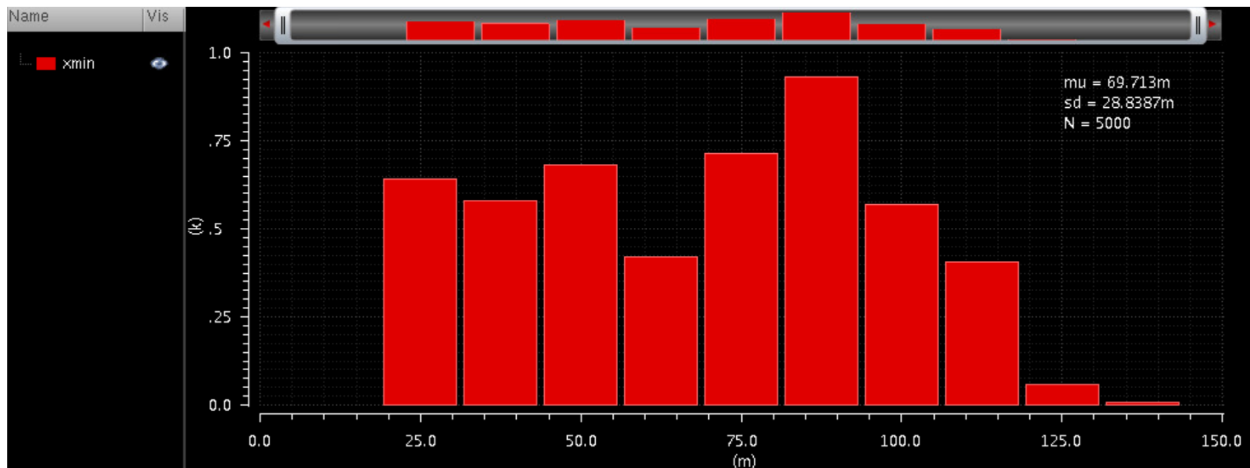

Figure 56: The WM variation hysteresis graph generated for a minimum sized 6T SRAM cell.

6.3.2 6T Cell Read Failure Simulation

To investigate 6 transistor write failure, the 6 transistor SRAM cell is evaluated at different applied voltages (VDD). The supplied voltage is varied from 0.3 volts to 0.4 volts. These voltages are chosen to be at the extremes of the subthreshold domain, as the subthreshold behavior of the device is desired. In each round of simulations for each supplied voltage, a fixed PMOS transistor width is chosen and the pull-up ratio will be varied by changing the pass transistor width each time by a set ratio "a". The sink NMOS widths are chosen to be "2a" to satisfy the read stability criteria. For each setup the WM is calculated. Figure 57 illustrates the WMs of the 6T cell under a voltage of 0.3 volts and with the use of minimum width devices (150nm) while PR is varied.

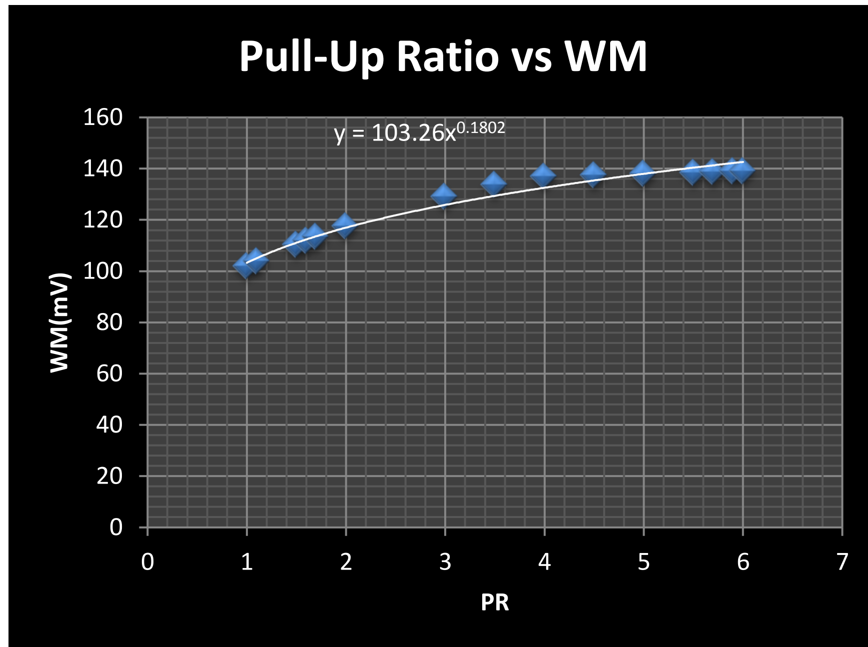

Figure 57: Pull-Up Ratio vs WM for a 6T cell with pass transistor width of 150nm at VDD=0.3V.

From the analysis, the approximate function that relates the WM and PR can be driven.

(16) $$WM = -a\,x^{b}$$

Where a and b some constants dependent on the transistor width and x is the pull-up ratio.

From analysing the generated graphs, it can be concluded that for a fixed device voltage, the WM and PR have a power relationship in a 6T SRAM cell in 65nm technology.

Considering the write margins calculated for each setup, a Monte Carlo analysis is performed to analyse the effect of process variation and mismatch of the devices and their associated parameters. The Monte Carlo analysis is set to have 5000 samples. The Monte Carlo gives us a mean value for WM of the samples, and also a standard deviation of these WMs. This information is used to perform 6Sigma analysis on the data with a lower bond set to be 100mV.

Figure 58 and Figure 59 illustrate the 6Sigma analysis result and percentage failure results respectively for a 6T SRAM cell under a supply voltage of 0.3V and with the use of minimum sized devices (150nm).

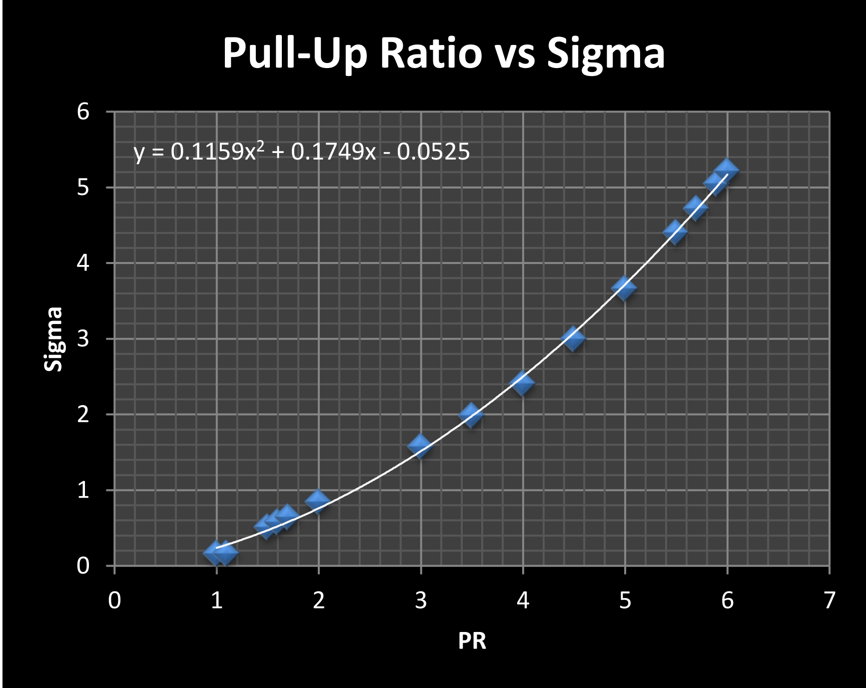

Figure 58: Pull-Up Ratio vs Sigma for a 6T cell with pull-up transistor width of 150nm at VDD=0.3V.

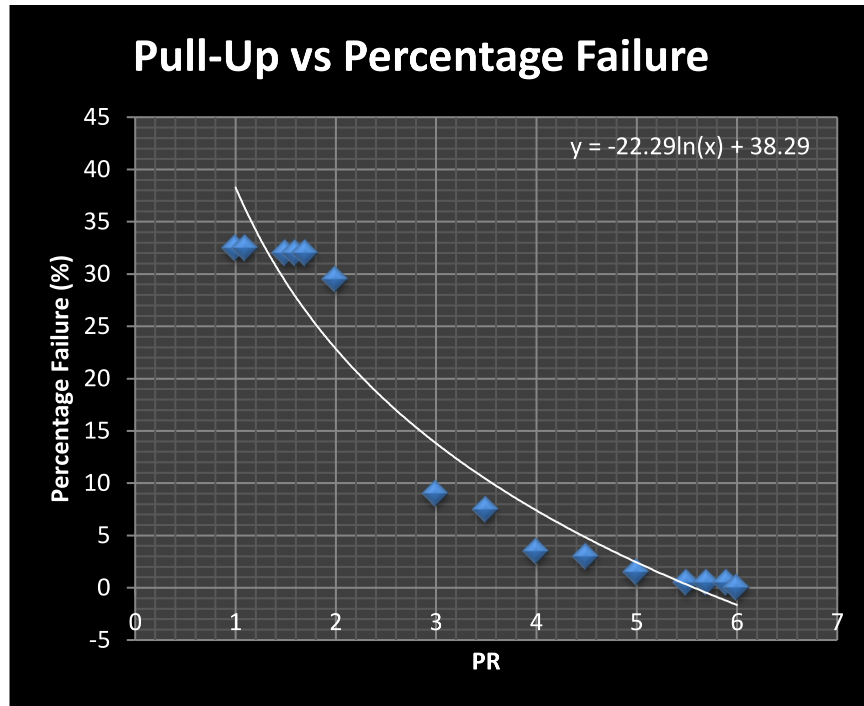

Figure 59: Pull-Up Ratio vs Percentage Write Failure for a 6T cell with pull-up transistor width of 150nm at VDD=0.3V.

From the analysis, the approximate function that relates the Sigma and PR can be driven.

(17) $$WM = a\,x^2 + bx + c$$

where a and b are constants dependent on the transistor width and x is the pull-up ratio.

Also, the approximate function that relates the Percentage Failure and PR can be driven.

(18) $$WM = -a \ln x + b$$

where a and b are constants dependent on the transistor width and x is the pull-up ratio.

Analysing the generated graphs, it can be concluded that for a fixed device voltage, in a 6T SRAM cell in 65nm technology, the Sigma and PR have a quadratic relationship and the Percentage Failure and PR have a logarithmic relationship.

If the results of similar simulations for different widths of the PMOS transistors (from 150nm to 500nm) are combined, 3-dimentional graphs can be generated that show the change in WM, Sigma, and Percentage Write Failure values for different simulation setups. Figure 61, Figure 62, and Figure 63 show these 3-dimentional graphs @ VDD=0.3V. Figure 64, Figure 65, and Figure 66 show these 3-dimentional graphs @ VDD=0.4V.

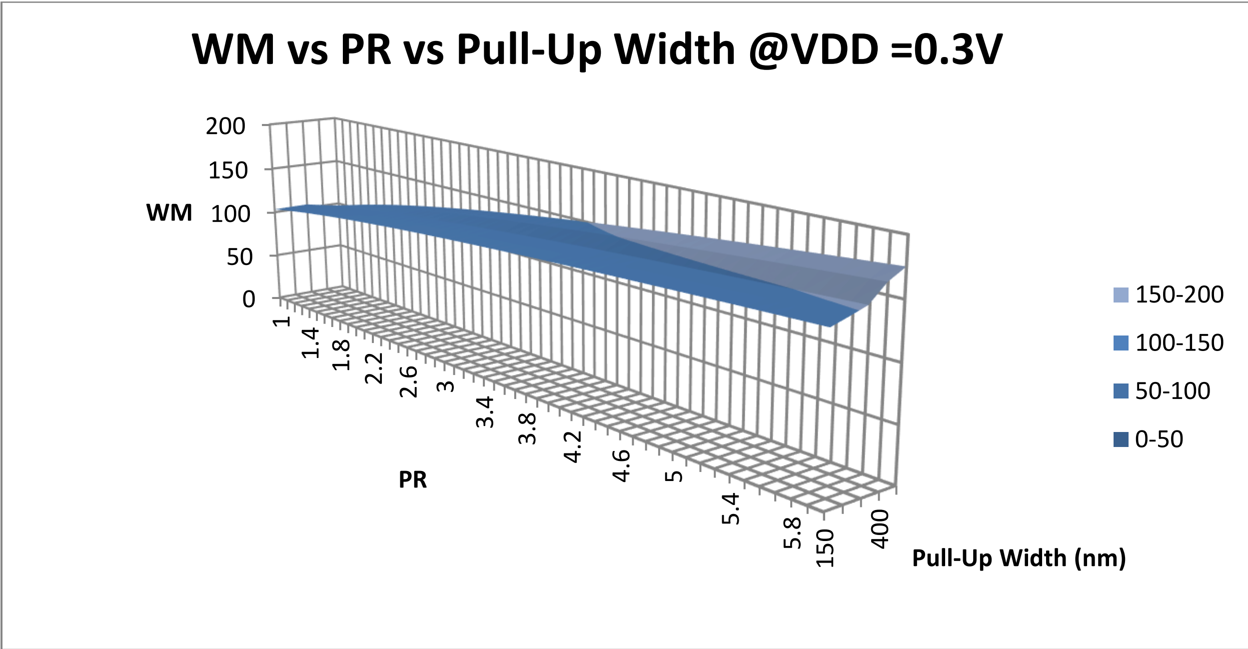

Figure 60: A 3-dimentional illustration of WM vs Pull-Up Ratio vs Pull- up Transistor Width for a 6T cell at VDD=0.3V.

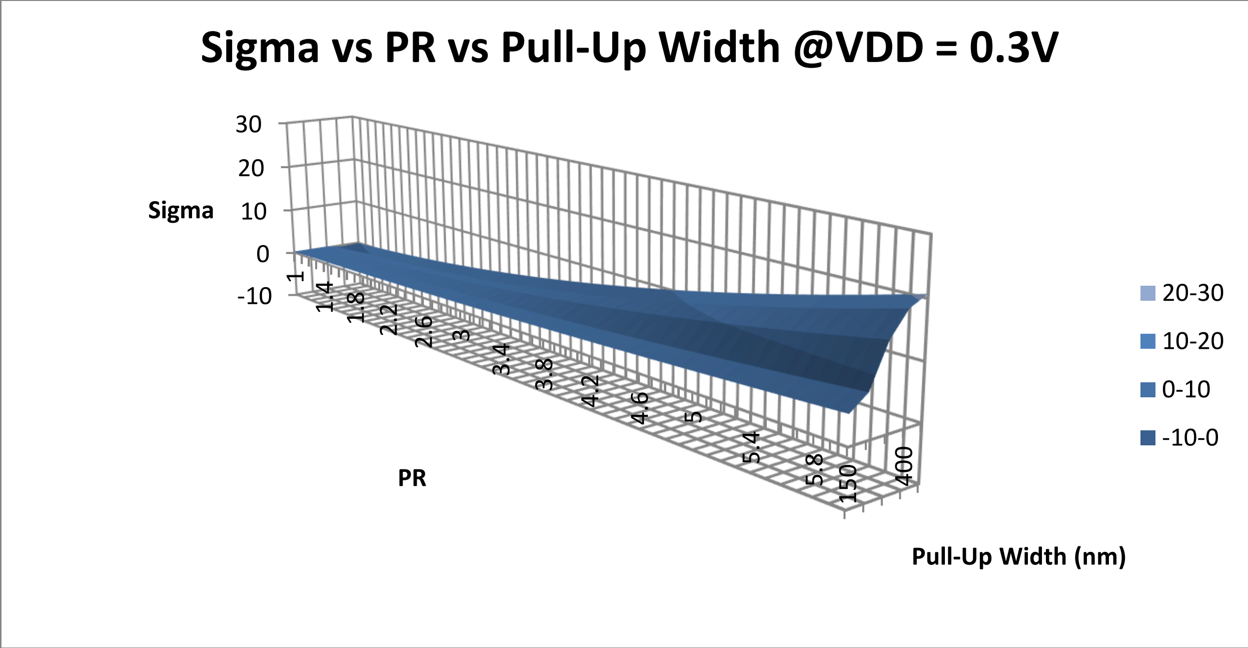

Figure 61: A 3-dimentional illustration of Sigma vs Pull-Up Ratio vs Pull- up Transistor Width for a 6T cell at VDD=0.3V.

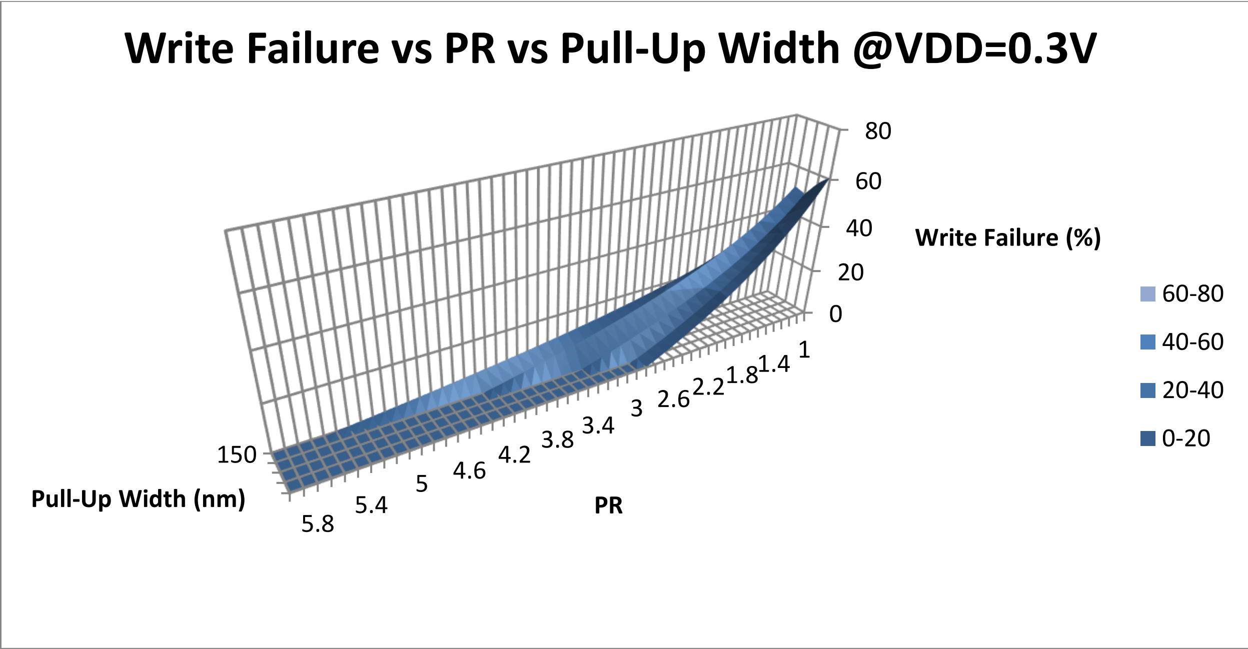

Figure 62: A 3-dimentional illustration of Write Failure vs Pull-Up Ratio vs Pull- up Transistor Width for a 6T cell at VDD=0.3V.

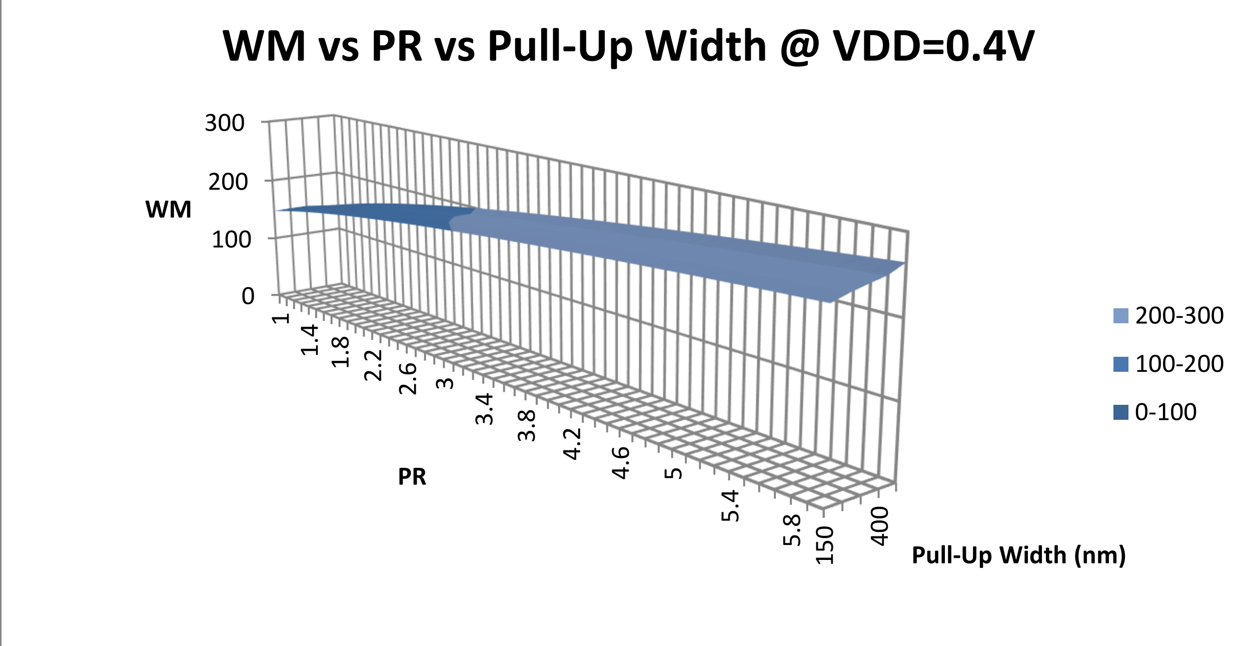

Figure 63: A 3-dimentional illustration of WM vs Pull-Up Ratio vs Pull- up Transistor Width for a 6T cell at VDD=0.4V.

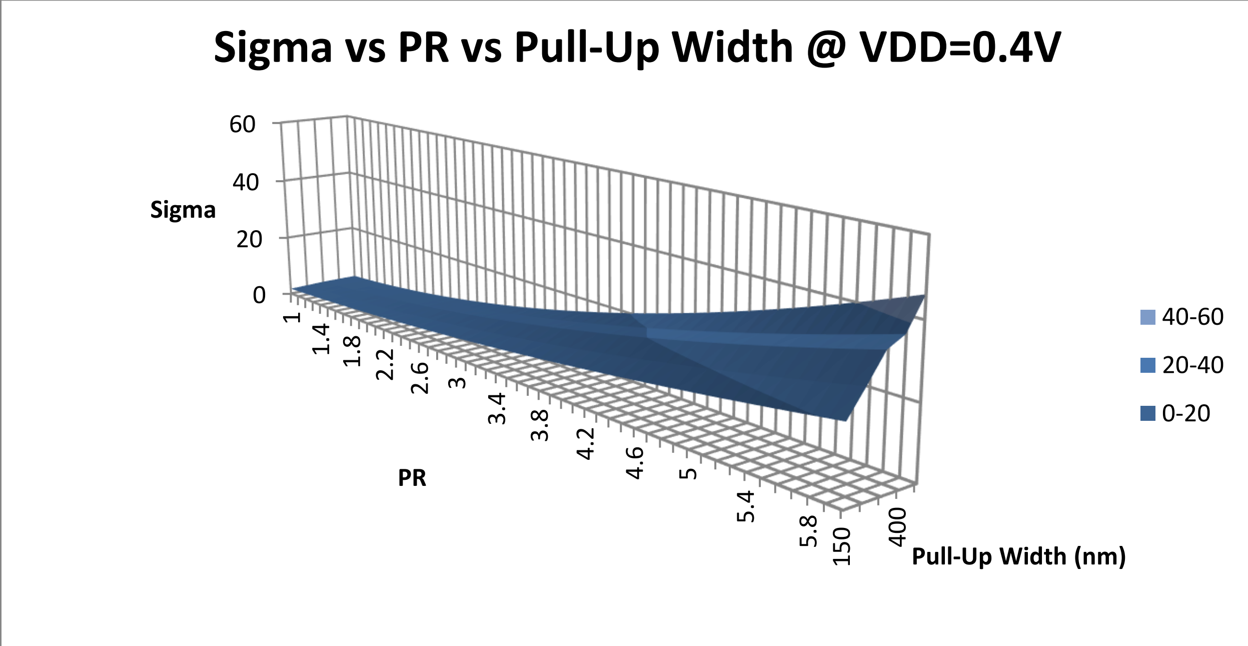

Figure 64: A 3-dimentional illustration of Sigma vs Pull-Up Ratio vs Pull- up Transistor Width for a 6T cell at VDD=0.4V.

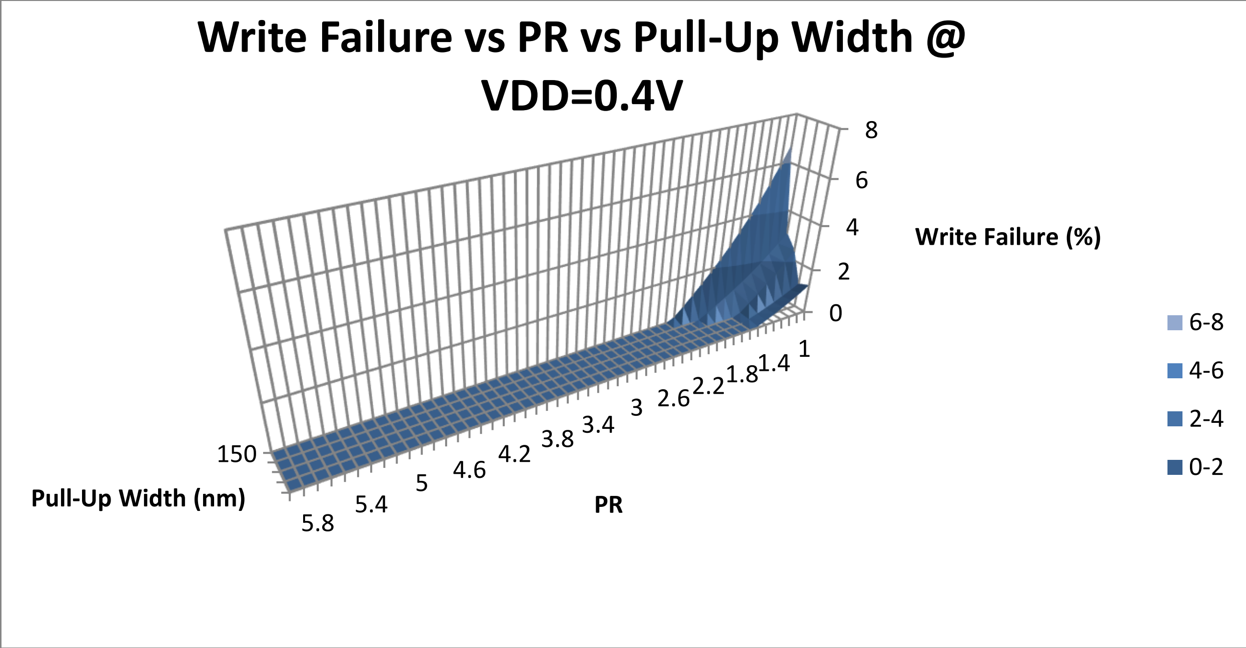

Figure 65: A 3-dimentional illustration of Write Failure vs Pull-Up Ratio vs Pull- up Transistor Width for a 6T cell at VDD=0.4V.

6.3.3 10T Cell Read Failure Simulation

To investigate the 10 transistor write failure, the 10 transistor SRAM cell is evaluated at different applied voltages (VDD). The supplied voltage is varied from 0.3 volts to 0.4 volts. These voltages are chosen to be at the extremes of the subthreshold domain, as the subthreshold behavior of the device is desired. The selection of this range of voltages creates results that are more comparable to the 6T simulation results. In each round of simulation for each supplied voltage, a fixed PMOS transistor width is chosen and the pull-up ratio will be varied by changing the pass transistor width each time by a set ratio "a". Also the sink NMOS widths are chosen to be "2a" to satisfy the read stability criteria. For each setup the WM is calculated, Figure 66 illustrates the WMs of the 10T cell under supplied voltage of 0.3 volts and with the use of minimum width devices (150nm) while PR is varied.

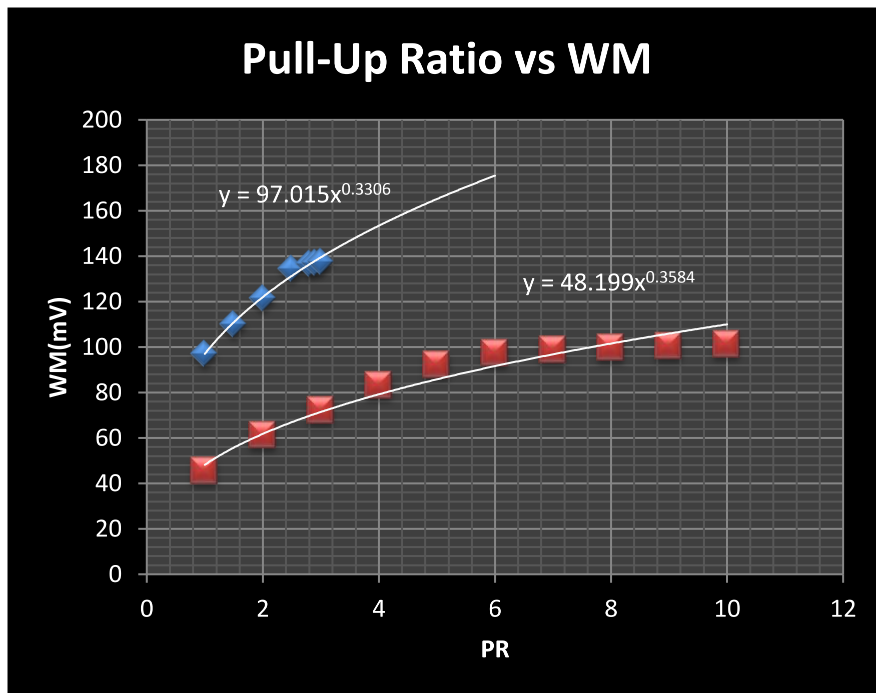

Figure 66: WMs of the 6T SRAM cell (Blue) and 10T SRAM cell (Red) under supplied voltage of 0.3 volts and with the use of minimum width devices (150nm) while PR is varied.

As it is illustrated in the figure, it is clear that there is a significant difference between the Write Margin of the 6T and 10T cells. The 10 transistor architecture shows a significantly lower Write Margins compared to the standard 6 transistor cell which is undesirable. To increase the Write Noise Margin of the device designers usually boost the voltage applied the wordlines of the 10T cells to a higher voltage than VDD. In this paper to create more energy efficient device a new method of voltage boost is introduced. Instead of boosting both word lines to voltages higher than VDD, only one of the wordlines is given a boost and only by 0.1 volts. In this write method, WWL is set to be kept at VDD while WL is gets a voltage boost a value 0.1V higher than VDD. This action is thought to be enough to reduce the write interruption by sink transistor M8 and improve the noise margin by making the M10 stronger. , Figure 67 illustrate the WMs of the 10T cell under supplied voltage of 0.3 volts (with 0.1 voltage boost on WL) and with the use of minimum width devices (150nm) while PR is varied.

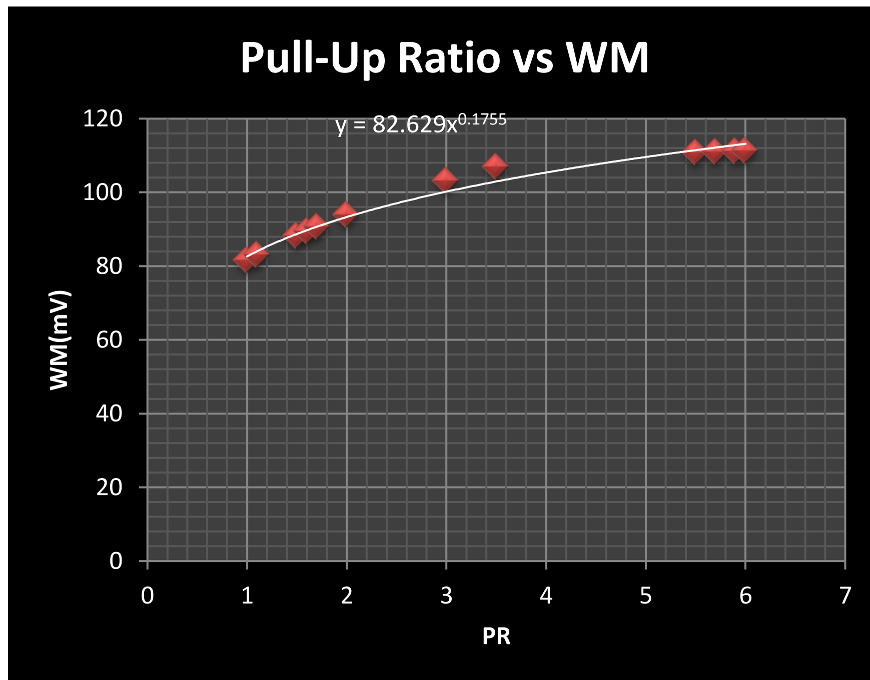

Figure 67: WM of the 10T SRAM cell (after a 0.1V boost) under supplied voltage of 0.3 volts and with the use of minimum width devices (150nm) while PR is varied.

From the analysis, the approximate function that relates the WM and PR can be driven.

(19) $$WM = -a\,x^{b}$$

Where a and b are some constants dependent on the transistors width and x is the pull-up ratio.

With analysing the generated graphs, it can be concluded that for a fixed device voltage, the WM and PR have a power relationship in 10T SRAM cell in 65nm technology which is similar to the result concluded for the 6T SRAM cell.

Considering the write margins calculated for each setup, a Monte Carlo analysis is performed to analyse the effect of process variation and mismatch of the devices and their associated parameters. The Monte Carlo analysis is set to have 5000 samples. The Monte Carlo gives us a mean value for WM of the samples, and also a standard deviation of these WMs. With the use of this information, the 6Sigma analysis is performed on the data with a lower bond set to be 100mV. Figure 68 illustrates the 6Sigma analysis result for the 10T SRAM cell under supply voltage of 0.3V (with a 0.1 WL voltage boost) and with the use of minimum sized devices (150nm).

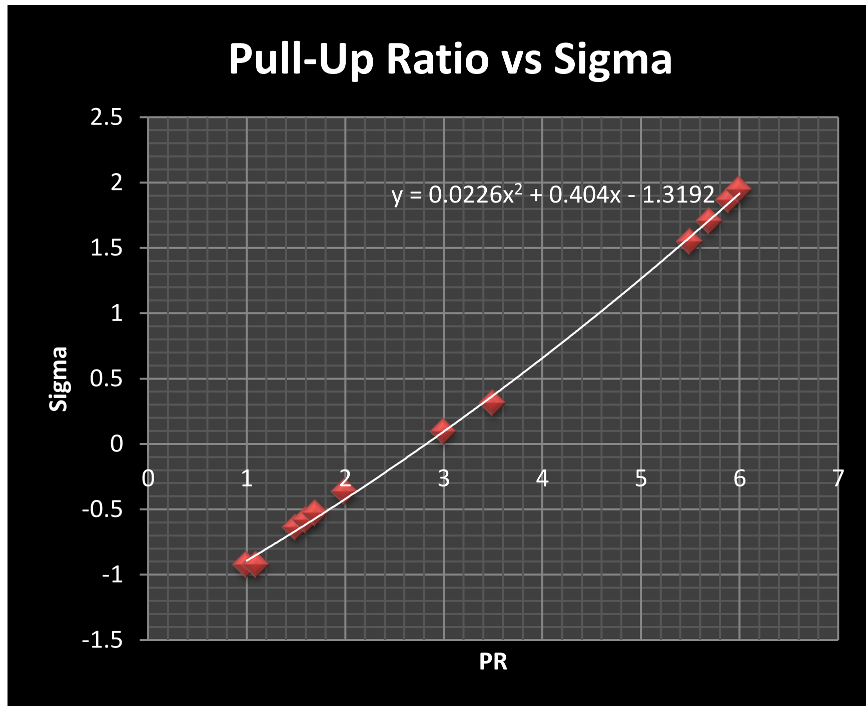

Figure 68: Sigma of the 10T SRAM cell (after a 0.1V boost) under supplied voltage of 0.3 volts and with the use of minimum width devices (150nm) while PR is varied.

From the analysis, the approximate function that relates the Sigma and PR can be driven.

(20) $$WM = a\,x^2 + bx + c$$

Where a and b are some constants dependent on the transistors width and x is the pull-up ratio.

With analysing the generated graphs, it can be concluded that for a fixed device voltage, the Sigma and PR have a quadratic relationship in 10T SRAM cell in 65nm technology.

If the result of similar simulations for different widths of the PMOS transistors (from 150nm to 500nm) are combined, 3-dimentional graphs similar to the ones generated for 6T SRAM cell can be generated that shows the change in WM, Sigma values for different simulation setups. Figure

69 and Figure 70 show these 3-dimentional graphs @ VDD=0.3V. Figure 71 Figure 72 show these 3-dimentional graphs @ VDD=0.4V.

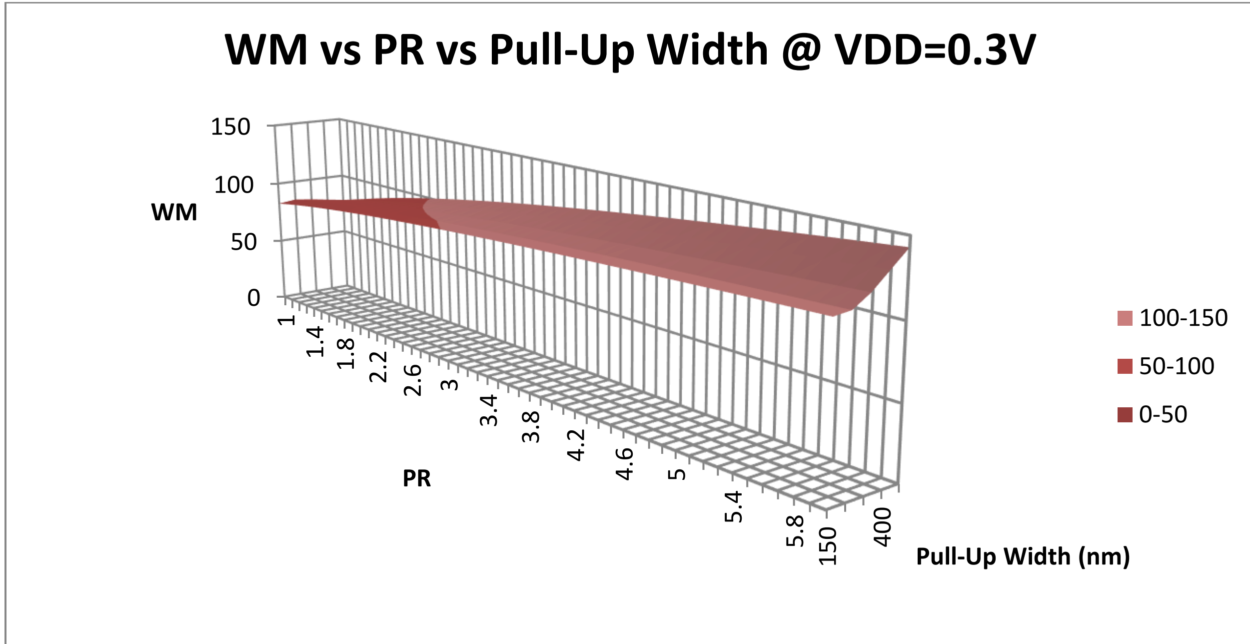

Figure 69: A 3-dimentional illustration of WM vs Pull-Up Ratio vs Pull- up Transistor Width for a 10T cell at VDD=0.3V.

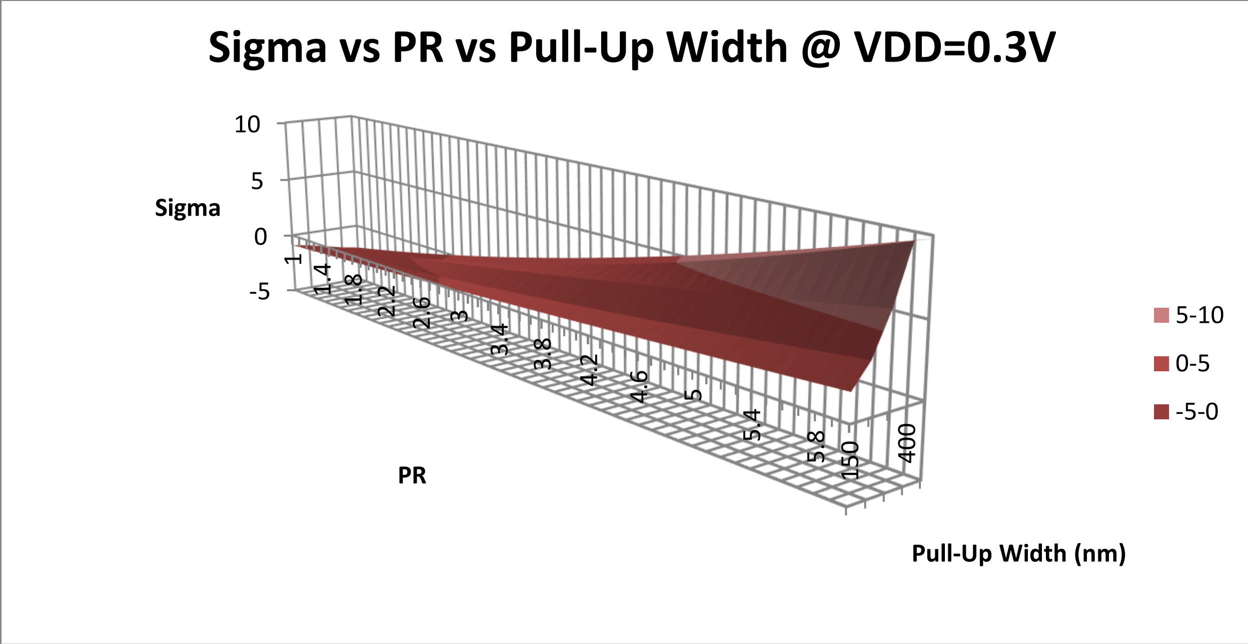

Figure 70: A 3-dimentional illustration of Sigma vs Pull-Up Ratio vs Pull- up Transistor Width for a 10T cell at VDD=0.3V.

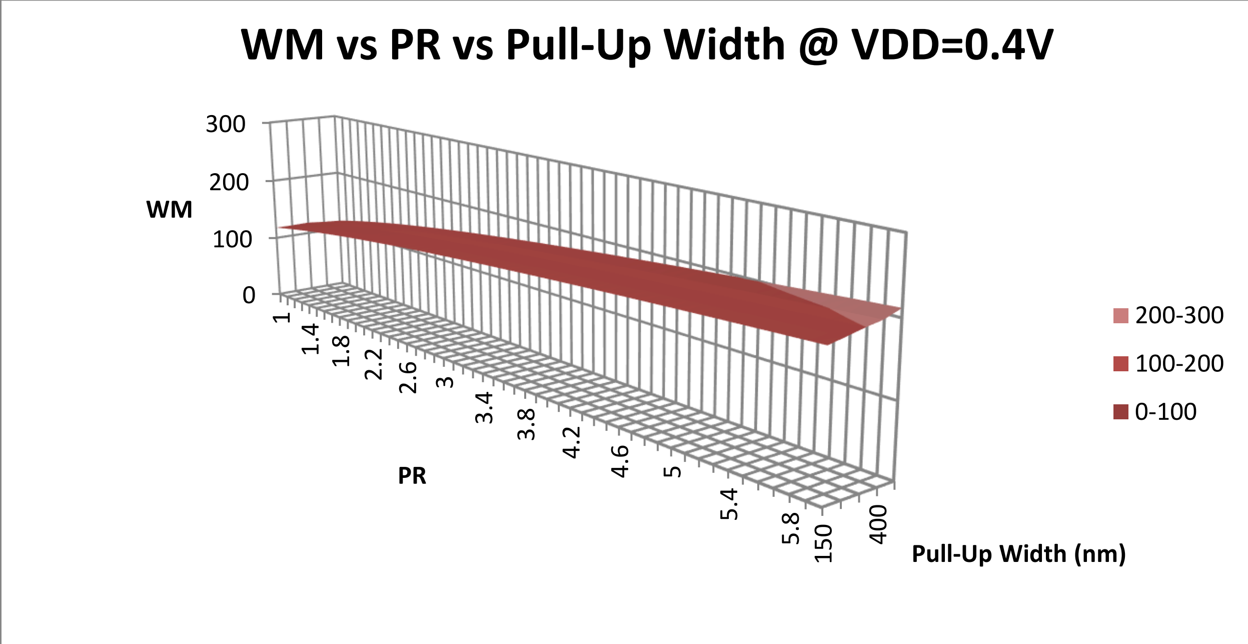

Figure 71:A 3-dimentional illustration of WM vs Pull-Up Ratio vs Pull- up Transistor Width for a 10T cell at VDD=0.4V.

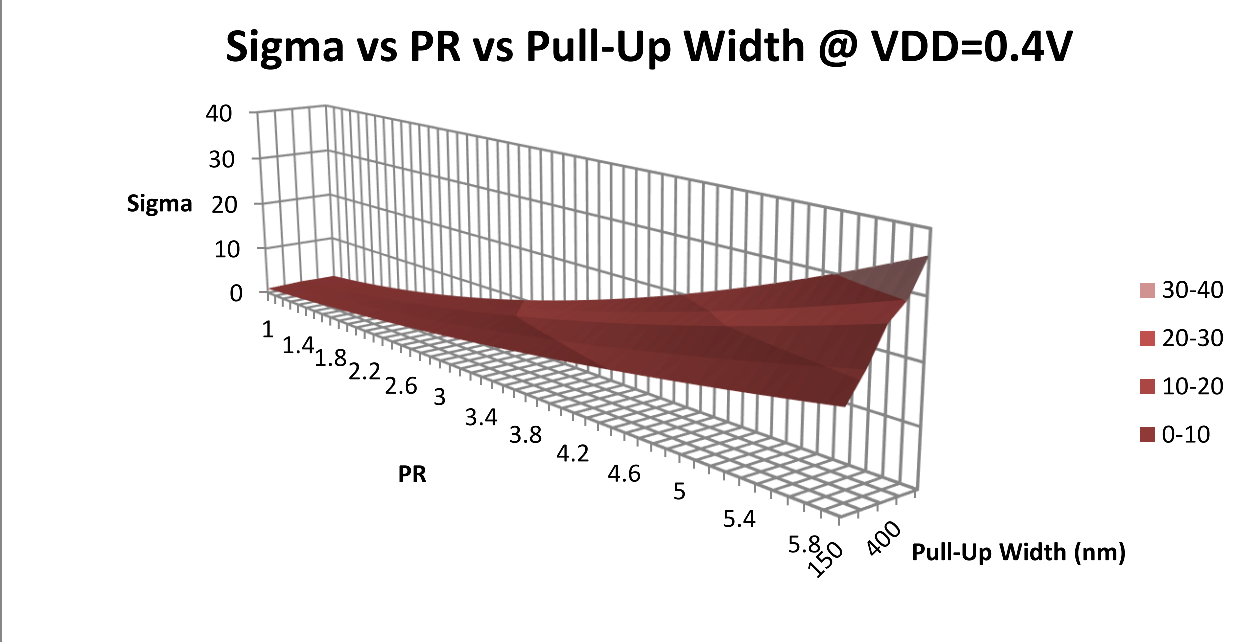

Figure 72: A 3-dimentional illustration of Sigma vs Pull-Up Ratio vs Pull- up Transistor Width for a 10T cell at VDD=0.3V.

6.4 Write Margin Comparisons

After analysing 6T and 10T cells, it is revealed that a minimal voltage boost of WL in 10 transistor cell will boost its Write Noise Margin significantly. With a 0.1 voltage boost the Write Noise Margin of the 10T SRAM cell will reach the values 2 times the regular 10T SRAM cell which reach values up to 80 percent of Write Margins of the 6T cell. This increase also decreases the cell's susceptibility to process variation and mismatch significantly. Figure 73 and Figure 74 illustrate the comparison of WM and Sigma values of 6T and 10T cells for a wide range of simulations.

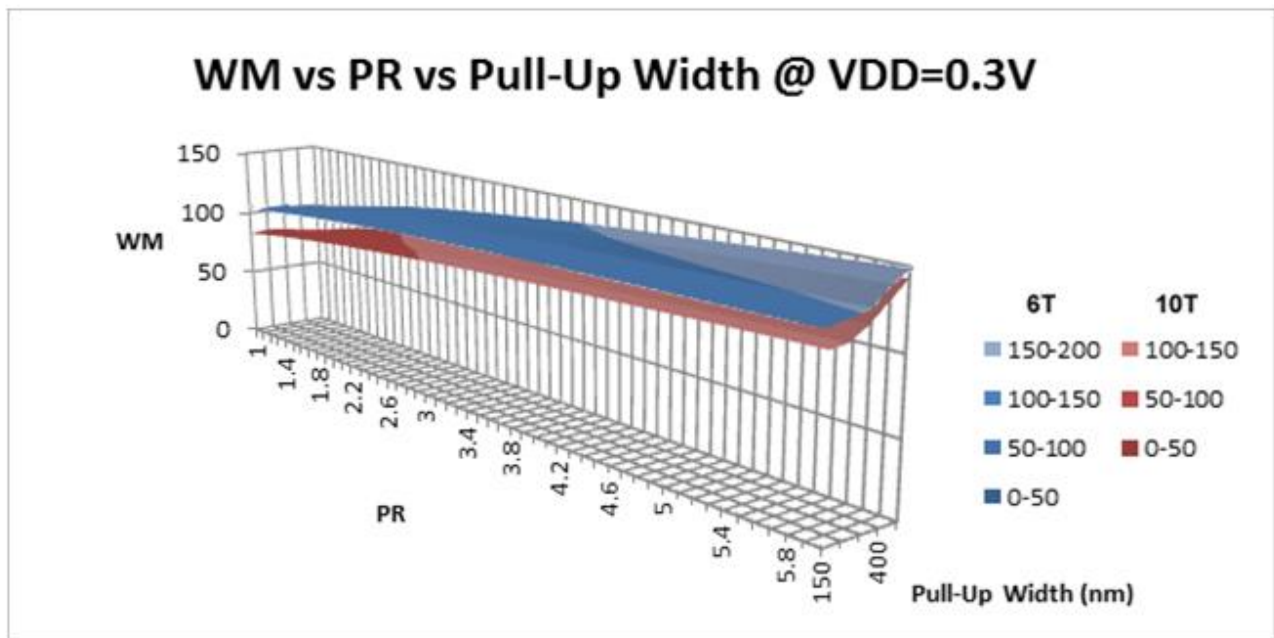

Figure 73: A 3-dimentional comparison of Write Margin vs Pull-Up Ratio vs Pull- up Transistor Width of the 6T and 10T cells at VDD=0.3V.

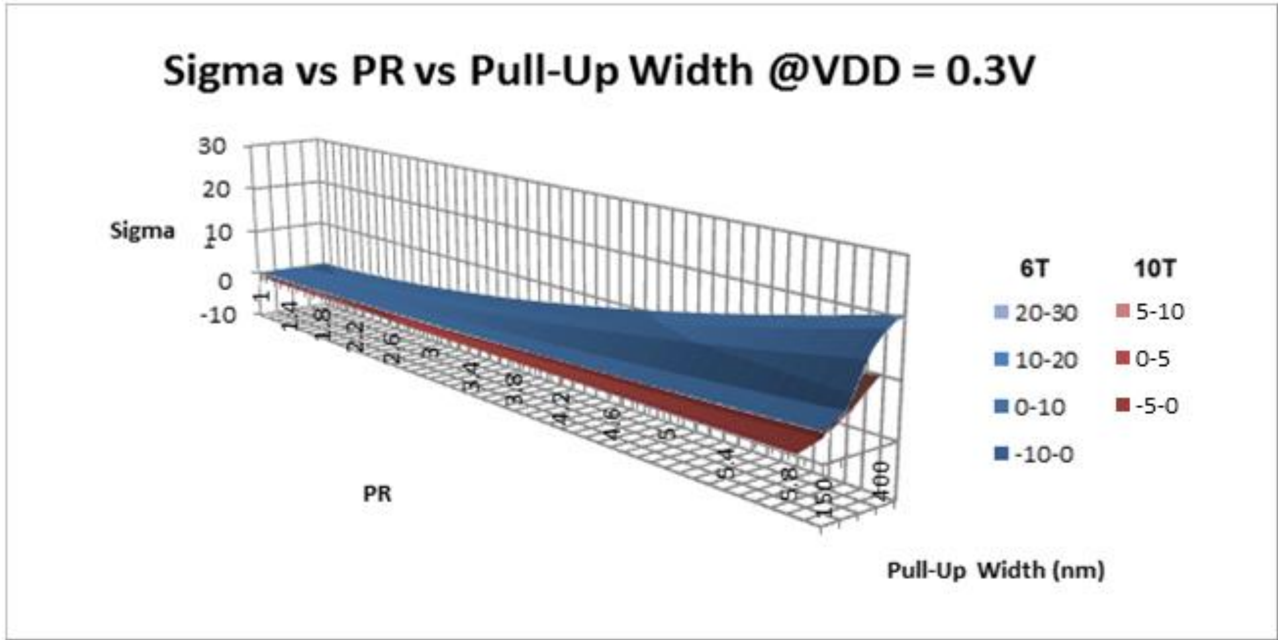

Figure 74: A 3-dimentional comparison of Sigma vs Pull-Up Ratio vs Pull- up Transistor Width of the 6T and 10T cells at VDD=0.3V.

Chapter 7

Conclusion

In this thesis, the 10 transistor Static Random Access Memory proposed by Chang et al. was compared to a 6 transistor Static Random Access Memory in the lower spectrum of the subthreshold region of operation of a 65nm technology node. The compression was more focused on the stability of the devices in performing read and write operations. Three-dimensional graphs were to better compare the difference between these SRAM cells. These figures may suggest design possibilities to designers. Moreover, a low power Write Margin improvement method is proposed for the 10 transistor cell, to raise its stability to a level comparable to that of its 6 transistor counterpart.

7.1 SNM Simulations

In this paper, the Static Noise Margin of the conventional 6T SRAM cell was compared to tha of a 10T SRAM cell. In this comparison, the effect of process variation and device mismatch was considered. It is been proven through simulation that the 10T cell is far more stable in terms of read operations than the 6T cell, and shows lower read failures.

7.2 Read and Leakage Current Simulations

In this thesis, the read and leakage currents of the conventional 6T SRAM cell was compared to that of the 10T SRAM cell, considering the effect of process variation and device mismatch. It has been proven through simulation that the 10T has more leakage than the 6T cell, due to the introduction of more leakage paths. . The 6T cell was also shown to have a a slightly higher read current than the 10T cell.

7.3 WM simulations

The Write Margins of the conventional 6T SRAM cell were compared to those of the 10T SRAM cell., Additionally, a voltage boost method was proposed that increased the write margin of the 10T cell by 50% and brought it up to 80% of the 6T write Margin with only a small boost of 0.2V.

Overall, the 10T cell with an area of 2.5 times that of its 6T counterpart and a 0.1V wordline voltage boost during write operations will possess around the same write margin as the 6T cell while benefiting from a far larger static noise margin during read operations.

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