Fabrication and Characterization of Microcrystalline Silicon Near Infrared Photodiode Detector Pixel on Glass Substrate for Large Area Electronics

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

This thesis is focused on development of near infrared (NIR) photodetectors on glass substrate at low temperatures for large area electronics applications. In the first part of this thesis we study the optical properties of plasma enhanced chemical vapor deposition (PECVD) prepared hydrogenated microcrystalline silicon (μc-Si:H) material. We demonstrate that μc-Si:H film has absorption coefficient of 10^3 cm^{-1} at wavelength of 850 nm, which is more than three orders of magnitude higher than the absorption coefficient in conventionally used hydrogenated amorphous silicon (a-Si:H) material in large area electronics. However, in spite of its high absorption coefficient in NIR region, we demonstrate that metal-semiconductor-metal (MSM) detectors based on μc-Si:H have a weak dynamic range (DR) of operation of about 50 at wavelength of 850 nm per 1 mW/cm^2 of incident optical power density. Furthermore, we demonstrate that NIR DR for μc-Si:H MSM detectors is very close to the one for a-Si:H MSM device and hence μc-Si:H detector is not efficient for NIR light detection. As a result, we focused on photodiodes instead of MSM detectors as an alternative device structure with high DR capability. For this purpose we developed and characterized doped μc-Si:H layers and fabricated an n type-intrinsic-p type (n-i-p) μc-Si:H photodiode with intrinsic layer thickness of 343 nm. This device shows an external quantum efficiency (EQE) of 2 % at 850 nm with a DR of almost 500 for 1 mW/cm^2 of incident optical intensity which is an order of magnitude higher than the one for μc-Si:H MSM detector. By increasing the intrinsic layer thickness to about 2 μm we observed that the EQE was increased to 8 % without a notable change in DR due to proportional increase in dark current level as compared to the photocurrent level. By incorporation of 1 μm thick textured AZO back reflector to the photodiode structure, however, we were able to reach EQE of 19.2 % with DR of more than 1000 at 850 nm per mW/cm^2 of incident optical density, which is 20 times higher than the one for μc-Si:H MSM device. Furthermore, we developed HSpice circuit model parameter extraction method for our photodiode demonstrating a non ideality factor of 1.54, reverse saturation current of 4.94×10^{-11} A, shunt resistance of 1.35 $G\Omega$, series resistance of 191.3 $k\Omega$, and parallel capacitance of 40 pF for area of 500×500 μm^2. In the second part of this thesis, we focused on development of a-Si:H thin film transistor (TFT) in order to fabricate pixel circuits based on our developed photodiode to test its feasibility for implementation of 2D imaging arrays. During the design of our TFT fabrication process, integration of our μc-Si:H photodiode had been taken into consideration and hence a bottom gate structure was adopted compared to the top gate one. In order to design a hybrid TFT/photodiode pixel circuit we needed to obtain accurate HSpice model representation for our TFT. As a result we adopted the HSpice Level 61 transistor model and presented an step by step parameter extraction procedure for our TFT obtaining the 29 TFT parameters in this

model. The HSpice simulation results accurately modeled the behaviour of the TFT in both above threshold and subthreshold regimes in comparison to the experimental TFT data. The fabricated TFT showed a very low threshold voltage of 3.6 V with an on/off ratio of 10^6, and field-effect mobility of 0.64 cm^2/Vs, which is suitable for μc-Si:H photodiode pixel circuit design. In the third part of this thesis we focused on integration of the developed photodiode and TFT for realization of a hybrid photodiode/TFT pixel circuit for imaging arrays where we presented three different pixel designs and their fabrication processes based on the developed μc-Si:H photodiode and a-Si:H TFTs. We discussed the design, simulation, analysis, fabrication, and experimental measurements of conventional pixel with one TFT and one photodiode. We demonstrated that the conventional pixel suffers from saturation problem and signal drift due to high dark current flow of the μc-Si:H photodiode (compared to a-Si:H photodiode) during pixel wait time. In order to solve the saturation problem we presented a novel design with integrated capacitance underneath the photodiode to enhance pixel capacitance. However, the enhanced pixel capacitance comes at the cost of slower response and the pixel still suffers from signal drift during wait time. As a result, we proposed a new pixel design with two TFTs, one capacitor, and one photodiode which proved to reduce the signal drift of the pixel during the wait time. As a result the proposed pixel shows promising characteristics for large area NIR imaging on glass substrate which can be used in smart displays and wearable sensor applications.

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Finally I would like to express my deepest gratitude and appreciation to my beloved parents and my sister for their endless support during this period.

Dedication

This thesis is dedicated to my parents and my sister.

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Chapter 1

Introduction

Near infrared (NIR) radiation is commonly defined as electromagnetic radiation with the wavelength ranging from $0.7\ \mu m$ (upper bound of visible region) up to $1.4\ \mu m$. NIR has important applications in circumstances where it is not possible to use visible light source or visible light source is not available such as in night vision and security surveillance applications [1]. On the other hand NIR is the preferred wavelength for fiber optics communications due to the low attenuation losses of the SiO_2 glass medium in this region [2]. NIR can also be used for imaging in obscured environments due to presence of gas and haze as longer (red/infrared) wavelengths are scattered less in those environments [3]. There is another class of applications for NIR in biological spectroscopy in the wavelength region of 650 to 1350 nm. In this wavelength region (also known as biological or therapeutic window) light has maximum depth of penetration in tissue facilitating the deep tissue imaging and treatment [4].

Nowadays the state of art semiconductor technology provides a variety of semiconductor device solutions for NIR light detection required by the aforementioned applications. These

semiconductor photodetector devices are commercially available in the form of discrete devices or integrated arrays. Discrete detectors are used for signal acquisition applications (e.g. fiber optics communication) and are usually available in both photodiode and photoconductor configurations. On the other side, integrated array detectors are used for imaging applications and are commercially available in the form of charge coupled device (CCD) or complementary metal oxide semiconductor (CMOS) arrays. These NIR detectors are commonly fabricated using either of the following four semiconductor materials (Silicon, Si, Germanium, Ge, Gallium Arsenide, GaAs, and Indium Gallium Arsenide, InGaAs) depending on the NIR wavelength required by that application [5]. However none of the existing technologies are compatible with fabrication over large area because of their dependence on expensive, size limited crystalline substrates.

By domination of the display market with flat panel displays in recent years, and increased demand for smart displays with enhanced capabilities and features, a new generation of innovative ideas emerged which utilize invisible NIR light for hover mode touch sensing and fingerprint detection. Han et al. are the pioneers in introduction of NIR sensors into large area electronics world by demonstration of the first flat panel display using in-pixel NIR touch sensing elements based on hydrogenated amorphous silicon germanium (a-SiGe:H) thin film transistors [6, 7, 8]. Since then a lot of research has been carried out to implement NIR sensors on large area substrates using hydrogenated amorphous silicon ([9]) and organic semiconductors ([10, 11, 12, 13]). Either of the existing solutions for large area NIR photodetection have their own disadvantages. As an example, a-SiGe:H semiconductor is prone to light induced degradation and shows 200 times lower carrier mobility compared to amorphous silicon (a-SiGe:H electron mobility of 0.005 cm^2/Vs vs mobility of 1 cm^2/Vs in a-Si:H) resulting in very slow response (1/60 s) for the detectors fabricated based on this material ([6]). In addition the doping of a-SiGe:H film is

very difficult and fabrication of a-SiGe:H NIR photodiodes which can have faster response (due to their short vertical distance) is very challenging. On the other hand even though the organic NIR photodiodes show fast response (response times in the order of 100 ns [10]), there are still technical challenges associated with instability of organic materials in air and aqueous ambient which makes micro-scale patterning and integration of these materials with existing standard thin film transistor technologies nearly impossible. In order to overcome the three aforementioned challenges associated with existing thin film NIR sensors in the literature (e.g. light induced degradation, slow response, and stability in air and aqueous ambient) and based on our research we selected hydrogenated micro-crystalline Silicon (μc-Si:h) as our candidate material for realization of a NIR detector on glass substrate which can be fast, stable and can be integrated with the existing standard a-Si:H thin film transistor technology.

The goals of this work were:

- To develop hydrogenated microcrystalline silicon photosensor with parameters suitable for pixelated array applications;
- To integrate the photosensor with pixel switches (TFTs) and to develop display industry compatible fabrication process;
- To develop pixel circuits for flat panel display applications with integrated touch sensors;
- To develop simulation tool for developed pixel circuits.

This thesis is structured as follows,

- Chapter 2 presents the literature review on large area NIR photodetector technologies and NIR properties of hydrogenated amorphous silicon (a-Si:H), a-SiGe:H, μc-Si:H, and organic thin films and devices.

- Chapter 3 describes experimental details of our research. We discuss device structure, performance figures of merit, the fabrication sequence, and performance measurements for our thin film photodiodes and TFTs.

- Chapter 4 presents our study on optoelectronic properties of μc-Si:H material. We discuss μc-Si:H photodiode detector and present the effect of intrinsic layer thickness and textured back reflector on photodiode performance. Finally, we present the circuit model for our best performance photodiode alongside with the procedure for parameter extraction from the photodiode model.

- In chapter 5, we consider the use of a-Si:H TFT switches and μc-Si:H photodiodes for implementation in 2D imaging arrays. Here, we discuss HSpice circuit model for our in-house fabricated a-Si:H TFT in order to be able to simulate and analyze the behaviour of photodiode/TFT pixel circuits. Furthermore, we show the analysis, simulation, design, fabrication for three different types of hybrid photodiode /TFT pixel circuits alongside with experimental measurement of the pixel circuits.

- Finally, in chapter 6, the summary and conclusions of this PhD research are presented. Possible future work is also suggested to further advance the research in this field.

Chapter 2

Thin Film NIR Photodetectors for Large Area Electronics Applications

2.1 Amorphous Silicon NIR Detector

a-Si:H is the most widely used semiconductor material for large area imaging applications. Several visible light photodetector structures such as p-i-n photodiodes [14, 15], metal-semiconductor-metal photoconductors [16, 17], metal-semiconductor Schottky barrier diodes, and thin film phototransistors [18, 19] have been successfully implemented based on a-Si:H semiconductor technology in the past, all relying on high absorption coefficient of a-Si:H in the visible wavelength region. For photon energies higher than the optical gap of a-Si:H (E_{ph} >1.78 eV), the absorption coefficient is higher than that of crystalline silicon (c-Si) [20]. The high absorption coefficient of a-Si:H in the visible region is commonly associated with direct absorption of photons due to loss of momentum conservation in its disordered atomic structure as opposed to the indirect photon absorption

phenomena in indirect bandgap silicon crystal [21]. However, the absorption coefficient for NIR region ($700 - 1400\ nm$) in a-Si:H semiconductor is lower than that of its crystalline counterpart. As an example, the absorption coefficient for c-Si material at 850 nm (photons with energy of 1.45 eV) is around $10^3\ cm^{-1}$ as opposed to the absorption coefficient of $10^0\ cm^{-1}$ in a-Si:H semiconductor. The low absorption coefficient of a-Si:H material very well explains the low dynamic range (DR) of 10 achieved in a-Si:H NIR photo-transistor under 852 nm illumination with intensity of 0.51 mW/cm^2 (normalized DR of 20 per mW/cm^2 of incident 850 nm NIR light) [9].

2.2 Hydrogenated Amorphous Silicon-Germanium NIR Detectors

It was demonstrated that the bandgap of a-Si:H prepared by chemical vapor deposition (CVD) method can be modified by introduction of carbon based (e.g. CH_4) or germanium based (e.g. GeH_4) precursor gases alongside with the silane gas (SiH_4) to create hydrogenated amorphous silicon carbon (a-Si_xC_{1-x}:H) or hydrogenated amorphous silicon germanium (a-Si_xGe_{1-x}:H) alloys [22, 23]. As a result, the bandgap can be reduced from 1.76 eV in a-Si:H down to 1 eV by incorporating Ge atoms, or it can be increased to 3 eV by introducing C atoms [22, 23]. Therefore, it is possible to develop large area deposition compatible thin film semiconductors with sensitivity extended to NIR or ultraviolet (UV) wavelength regions by controlling Ge atom concentration in a-SiGe:H semiconductor or C atom concentration in a-SiC:H semiconductor. It is reported that a-SiGe:H is more disordered compared to its a-Si:H predecessor as compositional disorder is added to the already existing structural disorder. As a result of this disorder, the alloy shows lower

carrier mobility caused by an increase in deep defect densities which act as trapping and recombination centres [24]. These defects are attributed to the preferential attachment of hydrogen atoms to the silicon rather than germanium atoms thus creating high density of germanium dangling bonds. Since GeH_4 is less stable in the glow discharge compared to SiH_4, Ge is preferentially deposited from SiH_4/GeH_4 mixtures, therefore, even low GeH_4 fraction in the gas already results in a high Ge fraction in the solid, and, consequently in high density of deep defects [25]. Palinginis et al. studied the defect structure in various a-SiGe:H samples deposited using standard PECVD method by varying Ge percentage in the film [26]. They observed that the defect density increases from 8.5×10^{14} cm^{-3} to 4.5×10^{15} cm^{-3} as Ge concentration is increased from 2% to 20% in the film. They also reported the presence of defect energy bands in a-SiGe:H films located at 0.68 eV and 0.79 eV below the conduction band, which was attributed to silicon and germanium dangling bonds, respectively. Incorporated H atoms and their bonding configurations are also believed to play an important role in the quality of a-SiGe:H alloys. In Ref [27, 28] authors report significant presence of dihydride Si-H_2 bonding in a-SiGe:H films and that hydrogen is preferentially attached to Si sites rather than Ge atoms due to the smaller binding energy of Ge-H bond compared to the Si-H bond, which results in deterioration of photo conductivity, defect density, and photostability of a-SiGe:H alloy [29]. Chou et. al. [30] demonstrated that the dark conductivity of a-SiGe:H film starts to decrease by increasing Ge content by a small amount (up to 10%) [30]. After that point dark conductivity starts to increase due to decreased bandgap, which favors thermal generation of free carriers. It was observed that the photo-sensitivity was reduced from 10^5 to 10^1 for high germanium concentration, which is attributed to enhanced dark current. In a-SiGe:H films, the photoconductivity does not necessarily improve compared to a-Si:H. This is due to the presence of high density of deep defects in the film, which increases carrier trapping and recombina-

tion resulting in suppressed electron drift mobilitiy. However, high hydrogen dilution has been proposed as an efficient way of improving the material quality and a-SiGe:H material with bandgap of 1.47 eV and photosensitivity of 2×10^5 has been reported [31]. Alternating thin film deposition and H_2 annealing [32], and He dilution instead of hydrogen dilution [33] are reported as other methods for improvement of photosensitivity in low bandgap a-SiGe:H films. Samples with the bandgap of 1.4 eV and photosensitivity of 10^4 deposited using hot wire CVD technique are also reported in the literature [34] whereas other reports suggest that increasing deposition temperature from 190 °C to 310 °C results in increased film photosensitivity from 3×10^2 to 10^4 [35].

In terms of devices, a-SiGe:H n-i-p diode has received extensive amount of attention in the past for fabrication of high efficiency tandem solar cells where low bandgap a-SiGe:H layer is used for absorption of NIR wavelengths of solar spectrum. It has been demonstrated that a-SiGe:H n-i-p single junction solar cells can achieve external quantum efficiency (EQE) values up to 6% at 850 nm whereas for a-Si:H material, the EQE at this wavelength is around 0.01% [36]. Agarwal et al. studied EQE and absorption coefficient values of different single junction a-SiGe:H solar cells with various densities of Ge in the intrinsic layer [36]. It was reported that for photon energies equal to 1.45 eV (equivalent to the wavelength of 850 nm), the absorption coefficient can reach 10^3 cm^{-1} for a sample with bandgap of $E_g = 1.48$ eV. This is three orders of magnitude higher than the absorption coefficient of a-Si:H material. Similar results have been reported in Ref. [37] where graded i-layer a-SiGe:H film deposited by hot wire chemical deposition method showed EQE values of about 2% for 850 nm [37]. EQE values around 15% have also been reported in the literature for $\lambda = 850$ nm in low defect density a-SiGe:H films deposited using very high frequency plasma enhanced chemical vapor deposition (VHF PECVD) system [38]. In Ref. [39] authors demonstrated higher EQE value (of about 50%) at $\lambda = 850$ nm for their

hydrogenated microcrystalline silicon germanium (μc-SiGe:H) single junction solar cells [39]. However, unfortunately the aforementioned EQE reports for a-SiGe:H solar cells are not paired up with reports on dark current and therefore dynamic ranges for the reported a-SiGe:H photodiodes are unknown and suitability of these devices for NIR light detection is under the shadow of uncertainty.

a-SiGe:H phototransistor detectors have been proposed recently as a promising solution for NIR light detection in touch sensing applications thanks to their sensitivity to NIR light and compatibility with TFT fabrication process [6]. The highest sensitivity for the a-SiGe:H phototransistor was reported to occur for a-SiGe:H film with the bandgap of 1.6 eV. One would expect the maximum sensitivity for 850 nm illumination to occur when material bandgap is less than the photon energy (1.45 eV), however, for a-SiGe:H, the sensitivity is at maximum when the bandgap is around 1.6 eV. This is another evidence that the sensitivity is higher due to better electronic properties of wide bandgap film which stems from the low concentration of germanium dangling bonds as reported by other researchers [40, 41]. The photo-to-dark current ratio of 900 was reported for 600 nm thick a-SiGe:H phototransistor with drain-source voltage (V_{ds}) of 5 V and gate-source voltage (V_{gs}) of -10 V under NIR illumination with power density of 13.75 mW/cm^2 and wavelength of 850 nm. This is equivalent to normalized DR of 65 per mW/cm^2 of radiation intensity. It is observed that the dynamic range of a-SiGe:H TFT is almost 3.25 times higher than its a-Si:H counterpart (discussed in section 2.1) and as a result a-SiGe:H TFT is more suitable for NIR light detection compared to its a-Si:H TFT counterpar.

2.3 Microcrystalline Silicon NIR Detectors

Hydrogenated microcrystalline silicon (μc-Si:H) is another promising material for NIR photodetectors due to its lower bandgap and higher NIR photon absorption compared to a-Si:H. Very important property of μc-Si:H is its suppressed light induced degradation effect compared to a-Si:H alloys. It was reported that μc-Si:H shows no degradation after 640 hours of exposure by air mass 1.5 (AM1.5) light as opposed to 40 % reduction of photocurrent in a-Si:H due to staebler wronski effect [42]. As a result, the devices based on μc-Si:H material are more stable under prolonged light exposure in large area imaging systems. In addition, μc-Si:H demonstrates reported electron mobility values as high as 50 cm^2/Vs [43] as opposed to the electron mobility of 1 cm^2/Vs in a-Si:H. Furthermore, since μc-Si:H film is consisting of crystalline silicon grains embedded in an amorphous silicon network, it shows lower optical bandgap compared to pure amorphous film. As a result, higher absorption coefficient in NIR region was achieved in μc-Si:H film. It was shown that the absorption coefficient for μc-Si:H is three orders of magnitude higher than that of a-Si:H for photon energy of 1.45 eV (wavelength of 850 nm) [44, 45]. μc-Si:H thin films are conventionally deposited using standard PECVD system with excitation frequency of 13.56 MHz from a mixture of Silane and Hydrogen gasses. It is well known that high Hydrogen dilution of Silane gas can favor crytsalline grain formation during the film growth process [46, 47]. However, very low growth rate of the film in standard capacitively coupled PECVD systems sets a major challenge for preparation of thick μc-Si:H film, which is necessary for efficient NIR photon absorption. It has been demonstrated that μc-Si:H film growth rate can be improved by increasing the plasma excitation frequency from 13.56 MHz up to 70 MHz [48]. Another high rate deposition technique using hot wire chemical vapor deposition [49] has been reported in the literature for preparation of thick μc-Si:H films. In typical

PECVD deposition reactors, the resulting thin film is amorphous if pure Silane is used in the deposition chamber. By introducing hydrogen to the plasma, the layer quality can be improved, but it still remains amorphous until hydrogen dilution is increased beyond a threshold percentage. If the hydrogen dilution is further enhanced, crystallites start to form, and crystalline volume fraction rapidly increases until we obtain layers that are predominantly microcrystalline. For high values of hydrogen dilution, columnar growth of microcrystalline grains prevails [50].

In terms of devices, it was demonstrated that the undoped μc-Si:H n-i-p solar cells show EQE value of 20% at 850 nm and the small micro-compensation of the undoped layer results in EQE of 30% at 850 nm [42]. Other studies show that μc-Si:H single junction solar cell with textured zinc oxide (ZnO) electrodes can provide EQE values as high as 50% for NIR wavelength of 850 nm [51]. However, unfortunately the dark current and photo sensitivity values of these μc-Si:H solar cells are not reported and assessment of feasibility of these devices as NIR photodetectors requires further study and research which is the goal of this thesis.

2.4 Organic NIR Detectors

In the past decade, discoveries in the field of organic chemistry led to the development of new generation of materials that had extended sensitivity in NIR region and could be deposited over large area using solution processing techniques. As a result, organic photodetectors were fabricated using low band gap polymers (PTT:PCBM blend) that have peak EQEs of about 45% at 750 nm [10]. Even though these photodiodes show extremely high EQE values compared to their inorganic counterparts, they suffer from very high values of reverse bias dark current density ($2 \times 10^{-5}\ A/cm^2$) resulting in a very

poor DR of around 7.8 per mW/cm^2 of incident 850 nm NIR light. Further research on organic NIR photodiodes led to development of higher DR NIR polymer photodetectors based on PDDTT:PCBM blend with peak EQE of 30 % at 850 nm but with an order of magnitude lower dark current compared to the previous polymer photodetectors (2×10^{-6} A/cm^2) [11]. These photodiodes show DR of 101 per mW/cm^2 of incident 850 nm NIR light. Similar results have been observed for small molecule organic photodiodes based on DHTBTEZP:PCBM blend demonstrating peak EQE of 25 % at 850 nm and dark current density of 2×10^{-5} A/cm^2 which results in DR of 84 per mW/cm^2 of incident 850 nm NIR light [12]. However, very recent publications on organic photodiodes based on cyanine (Cy7-T) small molecules present peak EQE of 17 % at wavelength of 850 nm but with much lower dark current density of 3×10^{-8} A/cm^2. The highest DR among all reported organic photodiodes is this cyanine based photodetector with a DR of 450 per mW/cm^2 of incident 850 nm NIR light hence making it very suitable for NIR light detection [13].

2.5 Chapter Summary

In summary, literature review on optoelectronic properties of large area a-SiGe:H and μc-Si:H inorganic materials reveals an almost three orders of magnitude superiority in absorption coefficient at wavelength of 850 nm for both of these semiconductor materials compared to their a-Si:H counterpart. In addition, research publications on single junction solar cells fabricated from optimized a-SiGe:H and μc-Si:H semiconductor recipes suggest maximum achievable EQE of 15% and 50% at wavelength of 850 nm for each of these semiconductors, respectively. However, lack of existing reports on dark current density for either of these devices makes it very difficult to judge on their suitability as photodetectors. On the other hand, research on a-SiGe:H phototransistors demonstrates NIR/Dark current

ratio of 65 per mW/cm^2 of 850 nm incident light and very poor response speed of 1/60 s which stems from poor electrical properties due to high defect density in a-SiGe:H. On the other hand, even though multiple reports show suitability of organic photodiodes for NIR photodetection due to selective sensitivity to NIR light, there are technological challenges associated with patterning and integration of organic semiconductors with standard thin film transistor electronics due to rapid degradation of organic material in air or water ambient.

Chapter 3

Experiment

3.1 Material Characterization

3.1.1 Undoped Microcrystalline Silicon Layer

3.1.1.1 Optical Properties

Prior to fabrication of any photodetector it is necessary to estimate the absorption coefficient of its absorber layers. Ultraviolet/Visible/Near-Infrared transmission-reflection spectroscopy was used to calculate the absorption coefficient of our undoped μc-Si:H thin film layers using the following procedure based on the equations developed in Ref. [52]. The transmitted photon intensity (T) and reflected photon intensity (R) in thin film material with complex refractive index of $N_1 = n_1 + ik_1$ deposited on a glass substrate with refractive index of $N_2 = n_2$ and exposed to incident light through air (Figure 3.1) with

refractive index of $N_0 = 1$ is described by Equations 3.1 and 3.2, respectively [52],

$$T = \frac{T_{02}T_{23}}{1 - R_{20}R_{23}} \tag{3.1}$$

$$R = \frac{{T_{20}}^2 R_{23}}{1 - R_{20}R_{23}} + R_{02} \tag{3.2}$$

The symbols used in Equation 3.1 and 3.2 are described in Equation 3.3 as follows,

$$\begin{aligned}
T_{02} &= T_{20} = \frac{n_2}{n_0}\left|\frac{e_1 t_{01} t_{12}}{1 - {e_1}^2 r_{10} r_{12}}\right|^2 \\
R_{02} &= \left|r_{01} + \frac{e_1^2 t_{01} t_{10} r_{12}}{1 - {e_1}^2 r_{12} r_{10}}\right|^2 \\
R_{20} &= \left|r_{21} + \frac{e_1^2 t_{21} t_{12} r_{10}}{1 - {e_1}^2 r_{12} r_{10}}\right|^2 \\
T_{23} &= |t_{23}|^2 \times \frac{n_2}{n_3} \\
e_1 &= exp\left(\frac{2\pi i N_1 d}{\lambda}\right) \\
t_{pq} &= \frac{2N_p}{N_p + N_q} \\
r_{pq} &= \frac{N_p - N_q}{N_p + N_q}
\end{aligned} \tag{3.3}$$

T_{02} is transmitted light intensity from layer 0 to layer 2 and T_{20} is the transmitted light intensity from layer 2 to layer 0. R_{02} is the reflected light intensity from layer 2 to layer 0 and R_{20} is reflected light from layer 0 to layer 2. T_{23} is the transmitted light intensity from layer 2 to layer 3. t_{pq} and r_{pq} are fresnel transmission and reflection coefficients at the interface of two adjacent media (p and q). In the above expressions, d is the thin film thickness, $N_m = n_m + ik_m$ is the complex refractive index of the m_{th} layer, and λ is the incident light wavelength.

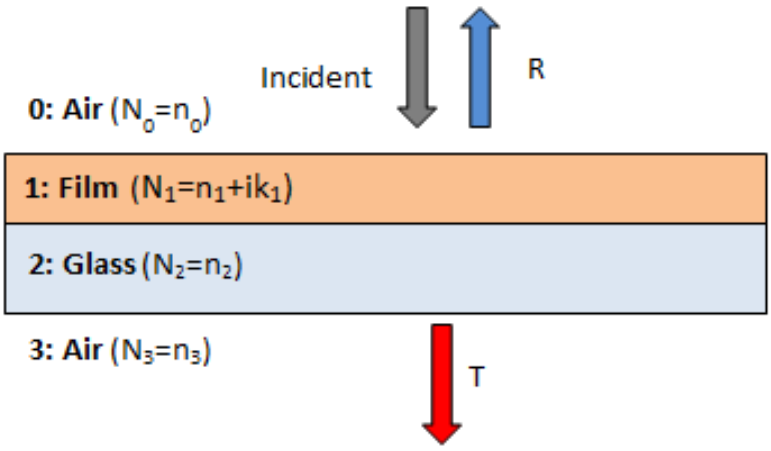


Figure 3.1: Schematic cross section of a thin film material on glass. UV-VIS-NIR transmission reflection Spectroscopy is used to find refractive index of the thin film (N_1).

Considering that the refractive index of air (N_0 and N_3) is equal to 1 and refractive index of Eagle 2000 glass substrate is equal to 1.51 [53] (Note that the imaginary part of refractive index for glass substrate is zero in the wavelength region of interest), it is possible to calculate the complex refractive index of the sample at each wavelength by solving the system of two nonlinear equations consisting of Equations 3.1 and 3.2 as functions of unknowns n_1 and k_1. For short wavelengths, where the absorption in the film is high and there is no or minimal interference present in the spectra, transmission and reflection equations can be approximated by Equations 3.4 and 3.5 respectively [54],

$$T \approx (1-R)^2 exp\left(\frac{-4\pi k_1 d}{\lambda}\right) \tag{3.4}$$

$$R \approx \left(\frac{n_1 - 1}{n_1 + 1}\right)^2 \tag{3.5}$$

which can be used to find approximate analytical solutions for n_1 and k_1 as follows,

$$n_1 \approx \frac{1 + R + \sqrt{R}}{1 - R} \tag{3.6}$$

$$k_1 \approx \frac{\lambda}{4\pi d} ln \left(\frac{(1 - R)^2}{T} \right) \tag{3.7}$$

The approximate solutions for n_1 and k_1 from Equations 3.6 and 3.7 can be used as an initial solution for the system of nonlinear equations to find more accurate values for real and imaginary parts of refractive index at that wavelength. As a result, values of n_1 and k_1 get updated and can be used as an initial guess for estimation of n_1 and k_1 at the next wavelength step. Finally, the absorption coefficient spectrum can be calculated from the imaginary part of refractive index (k_1) using Equation 3.8,

$$\alpha = \frac{4\pi k_1}{\lambda} \tag{3.8}$$

3.1.1.2 Crystallinity

The crystalline volume fraction (X_c) for the μc-Si:H films is estimated via Raman spectroscopy using Equation 3.10 (Ref. [55, 56]),

$$X_c = \frac{I_c}{I_c + \eta I_a} \tag{3.9}$$

In this formula, I_a and I_c are the integrated area of amorphous and crystalline peaks, respectively, and η is the back-scattering coefficient, which is approximately equal to 0.8.

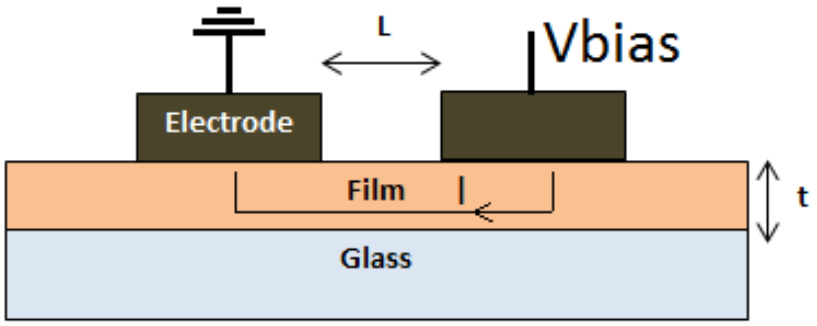


Figure 3.2: Schematic of a coplanar metal-semiconductor-metal (MSM) thin film photodetector.

3.1.1.3 Conductivity

In order to measure the dark conductivity, the thin film is deposited on glass substrate and coplanar electrodes are formed on top of the thin film using DC sputtering of aluminum through a shadow mask forming the structure shown in Figure 3.2. The resistance (R) of the coplanar device is calculated based on the current-voltage measurements of this device under bias voltage in probe station using Agilent 4155C semiconductor parameter analyzer. The conductivity of the thin film is estimated based on its resistance using the following formula,

$$\sigma = \frac{RtW}{L} \tag{3.10}$$

where t is thickness of the thin film measured using Dektak profilometer and W and L are width and spacing of the coplanar aluminum electrodes respectively.

3.1.2 Doped Microcrystalline Silicon Layers

For doped thin films the efficiency of doping is monitored through the increase in conductivity of the film using the procedure explained in section 3.1.1.3. the crystallinity of the doped thin films are also estimated based on Raman spectroscopy measurements using the method presented in section 3.1.1.2.

3.1.3 Aluminum Doped Zinc Oxide

3.1.3.1 Refractive Index

For aluminum doped zinc oxide (AZO) transparent conductive anti-reflective coating layer, the refractive index is calculated based on transmission-reflection spectroscopy and the method developed in section 3.1.1.1.

3.1.3.2 Sheet Resistance

The sheet resistance of the AZO layer prepared on glass substrate is measured using custom designed 4 point probe system connected to Keithly 2400 source-meter as schematically illustrated in Figure 3.3. Sheet resistance ($\rho_{\square}$) is calculated based on the applied current and measured voltage using the following formula [57],

$$\rho_{\square}\left(\frac{\Omega}{\square}\right) = \frac{\pi V}{ln(2)I} \tag{3.11}$$

Where I is the current source value and V is the measured voltage.

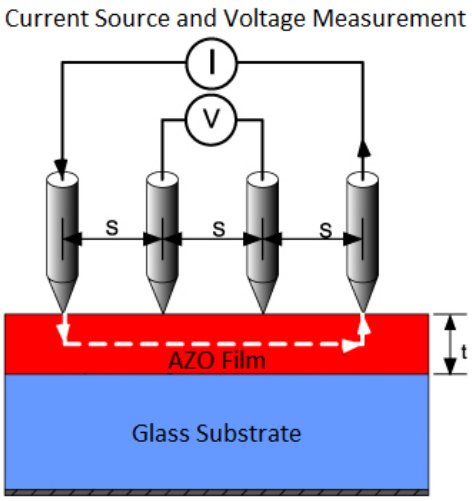


Figure 3.3: Schematic illustration of 4 point probe sheet resistance measurement system.

3.1.3.3 Haze Measurements of Textured AZO

The haze measurement for textured AZO is carried out using Shimadzu ISR-2200 dual beam integrating sphere system as illustrated in Figure 3.4. The measurement sample is divided into two pieces and set on both sample and reference sides. The barium sulfate white plate is removed from the sample side and the transmission measurement is carried out. In this way, the entire transmitted light (I_{total}) of the sample is received as the reference signal and only the diffusely transmitted light ($I_{diffuse}$) is received as the sample signal and the transmission measurement result will directly give the haze value ($Haze = I_{diffuse}/I_{total}$).

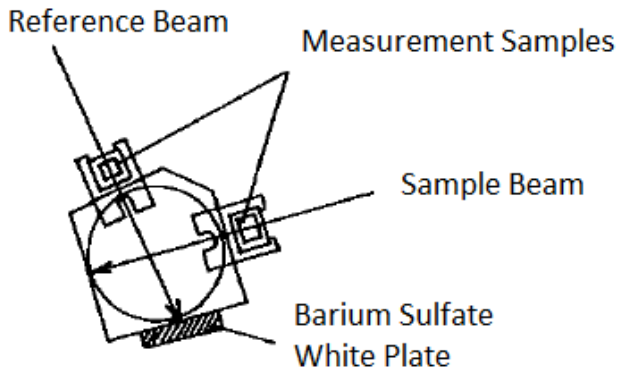


Figure 3.4: Schematic illustration of haze measurement.

3.2 Photodiode Structure and Performance Parameters

Figure 3.5 shows the basic structure of a thin film n-i-p photodiode. In n-i-p photodiodes an electric field is formed accross the intrinsic layer due to offset in fermi levels of n-type and p-type regions. This built in electric field over a controllable thickness (thickness of intrinsic layer) makes this device very suitable for extraction of photogenerated carriers in its intrinsic region. As a result of this built in electric field the photogenerated electrons drift towards the n-type region and the photogenerated holes drift towards the p-type region and create a photocurrent signal. As opposed to the conventional p-n junction diodes which are diffusion devices and rely on diffusion of minority carriers for efficient extraction of photogenerated charge, the n-i-p photodiodes are drift devices and their performance mainly relies on drift of photogenerated carriers in its intrinsic layer. The performance figures of merit for a photodiode are explained as follows [58],

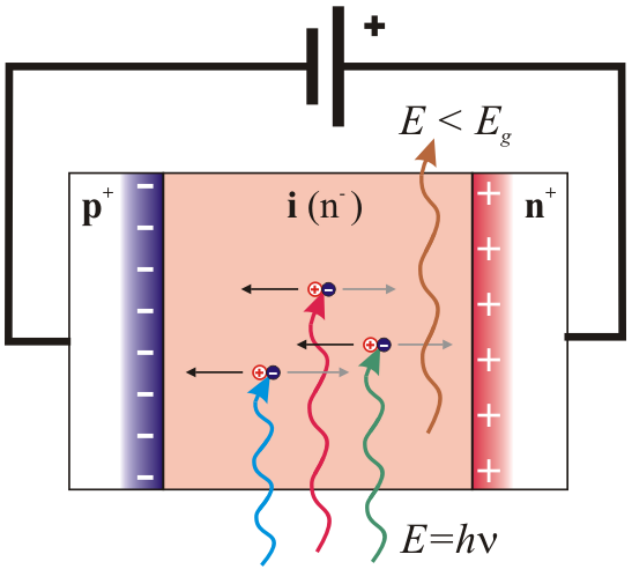


Figure 3.5: Schematic illustration of a n-i-p photodiode.

3.2.1 EQE

The most important property of a photodetector is its capability to convert optical signal to electrical signal. If a semiconductor with the bandgap of E_g is exposed to photons with the wavelength of λ and the photon energy ($E_{ph} = hc/\lambda$, h is planck constant and c is speed of light in vacuum) is higher than the bandgap, an electron-hole pair gets generated for every photon that is absorbed. In presence of an electric field, the electron-hole pair can drift to the external circuitry and create an electrical current. The ratio of number of extracted charges to the number of incident photons on the device is called external quantum efficiency (EQE) and is a measure of device capability to convert light

to electricity which is defined as follows,

$$EQE = \frac{I_{ph}/e}{P_{opt}/h\nu} \tag{3.12}$$

Here I_{ph} is the photocurrent extracted to external circuitry, e is the electron charge, P_{opt} is the optical power density incident on the device, and $h\nu$ is the photon energy.

3.2.2 Spectral Responsivity

Spectral responsivity (R_λ) is defined as the ratio of the photocurrent to incident optical power on the device. It is similar to EQE and can be calculated based on EQE of the device and on the wavelength (λ) of incident photons as shown in Equation 3.13.

$$R_\lambda = \frac{I_{ph}}{P_{opt}} = EQE \times \frac{e}{h\nu} = EQE \times \lambda \times \frac{e}{hc} \tag{3.13}$$

3.2.3 Dark Current and Minimum Detectivity

In photodiodes, the current flowing in the absence of light is called the dark current of the photodetector which is due to thermal generation of carriers at room temperature. As a result, the minimum detectable optical signal is limited by the level of dark current. Figure 3.6 (a) illustrates the typical relationship between photocurrent and incident optical power on the photodetectors. Figure 3.6 (b) is the magnified version of Figure 3.6 (a) at low optical power levels. As it is shown in Figure 3.6 (b) the optical power that generates the photo current equal to the dark current is the minimum detectable optical power of the photodiode which is called detectivity of the photodiode. This figure of merit describes how sensitive the photodetector is when exposed to low levels of light.

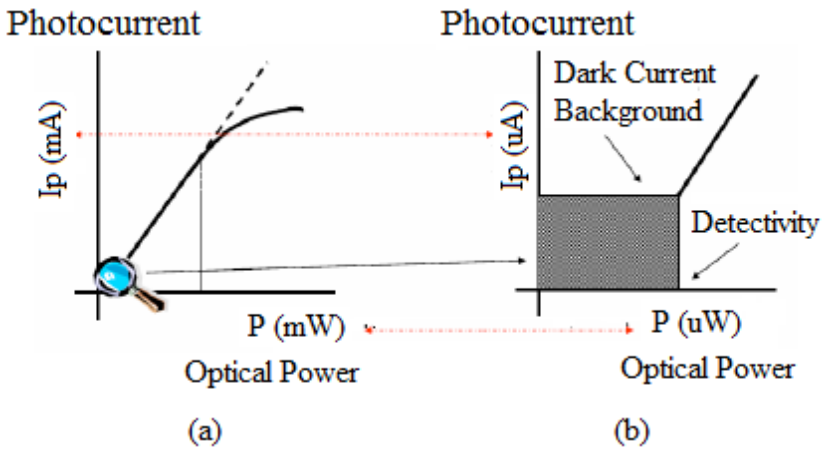


Figure 3.6: Schematic illustration of photodiode sensitivity relationship with dark current.

3.2.4 Dynamic Range of Operation

The ratio of the photo current over the dark current in a photodetector is called the dynamic range of operation, which is the figure of merit for signal to noise ratio in steady state operation. The dynamic range is of particular importance for imaging applications since the number of digitization bits for the image depends on the dynamic range. As an example, for 8 bit digitization, the dynamic range over 2^8 is required.

$$Dynamic\_Range = \frac{I_{photo}}{I_{dark}} \tag{3.14}$$

3.2.5 Response Time

The response time of a photodiode is defined as the time for the signal to rise (fall) from 10% to 90% (90% to 10%) of its final value. Three factors determine the response time of a photodiode detector:

- The drift time of generated electron-hole pairs in the depletion region of the photodiode.
- The diffusion time of the electron-hole pairs in the neutral regions of the photodiode.
- The RC time constant of the device, $\tau = RC$, where R is the sum of series resistance and the load resistance ($R_S + R_L$), and C, is the sum of the photodiode junction capacitance, C_j, and the stray capacitances, C_s ($C_j + C_S$).

The junction capacitance (C_j) is dependent on the area of the photodiode and on the applied reverse bias voltage, hence shorter response times are obtained in smaller area photodiodes, under high reverse biases. The total response time is determined by Equation 3.15, where all three factors contribute to the response time.

$$\tau_{total} = \sqrt{\tau_{drift}^2 + \tau_{diffusion}^2 + \tau_{RC}^2} \tag{3.15}$$

3.3 TFT Structure and Performance Parameters

Figure 3.7 shows the schematic cross sections of an a-Si:H TFT. This structures in which gate metal is below the active layer and source/drain contacts are on the top is known as the bottom-gate inverted-staggered TFT [59]. The main performance figure of merits for a TFT are summarized as follows [60],

3.3.1 Field-Effect Mobility

Higher field effect mobilities result in higher drain current and faster response of the TFT. Field effect mobility can be evaluated from the transfer characteristics of the TFT in

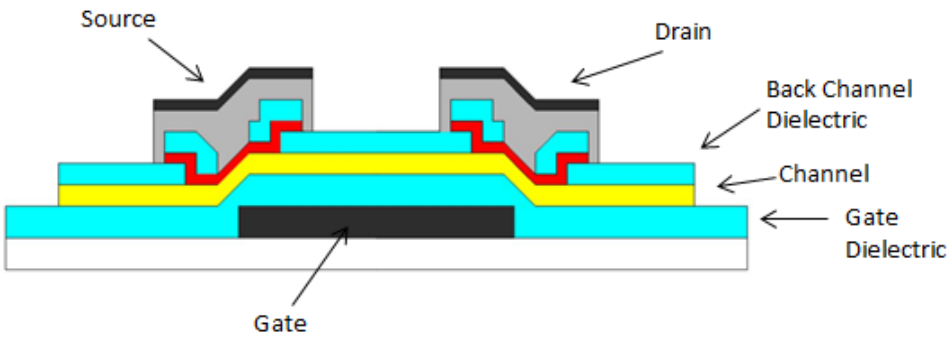


Figure 3.7: Cross section of inverted staggered TFT.

saturation regime using the following equation,

$$\mu = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_d}}{\partial V_{gs}}\right)^2 \tag{3.16}$$

where I_d is the drain current, V_{gs} is gate-source bias voltage, L and W are channel length and channel width respectively, and C_i is capacitance per unit area of gate insulator.

3.3.2 On/Off Current Ratio

I_{on}/I_{off} is the ratio of TFT drain current above the threshold voltage to the drain current below the threshold voltage. I_{on}/I_{off} can be evaluated from the transfer characteristics of the TFT. I_{on}/I_{off} ratio of more than 10^6 is usually required in a-Si:H TFTs used in liquid crystal displays and thin film imagers.

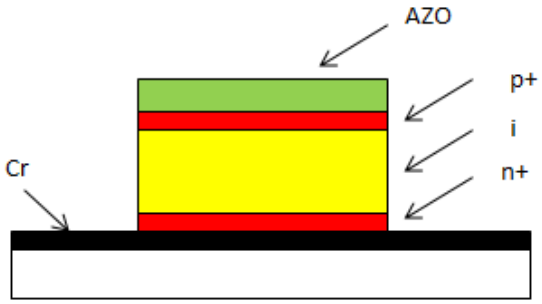


Figure 3.8: Schematic cross section of a thin film μc-Si:H photodiode on glass substrate.

3.3.3 Threshold voltage

It is the minimum gate voltage at which the TFT begins to conduct due to accumulation of electrons near the interface between semiconductor channel and gate insulator. Lower threshold voltage is usually more favorable as it increases TFT drain current.

3.3.4 Subthreshold slope

It is defined as the gate voltage required to change the drain current by one decade in the sub threshold region. Subthreshold slope is the figure of merit that shows how good can the TFT be switched on and off. A TFT with higher subthreshold slope exhibits a faster transition between off (low current) and on (high current) states.

3.4 Photodiode Fabrication Sequence

Figure 3.8 shows the cross section of thin film silicon photodiode. The photodiode fab-

rication process begins with sputtering of chromium cathode contact on Eagle 2000 glass substrate at room temperature using DC sputtering. Then deposition of n+, i, and p+ μc-Si:H layers takes place in a 13.56 MHz multi-chamber capacitive plasma enhanced chemical vapor deposition (PECVD) system without breaking the vacuum. Finally, the sample is removed and placed in RF sputtering system for sputtering of aluminum doped zinc oxide (AZO) transparent conductive oxide (TCO) layer on top of the n-i-p stack. Square shape anode (AZO) contacts are then defined using photolithography followed by etching of AZO in hydrochloric acid (HCL) aquatic solution and dry etching of silicon thin film layers using (SF_6 and O_2 mixture) to reach bottom Cr cathode contact. Photodiodes with various areas (ranging from 1 cm^2 down to 2500 μm^2) were fabricated. Fabrication process was carried out using University of Waterloo G2N lab facilities. Further details of deposition conditions and device fab are given in Chapter 4.

3.5 TFT Fabrication Sequence

Figure 3.9 shows the schematic cross section of the bottom gate a-Si:H TFT fabricated for our photodiode pixel circuit. The fabrication process of our TFT is summarized as follows,

- The fabrication process begins with cleaning of Eagle 2000 glass substrate in RCA1 solution. Thin Cr layer is then sputtered on the substrate in DC sputtering system. Mask 1 is then used to photolithographically pattern the gate metal to form the structure shown in image A on Figure 3.10.

- The photoresist is then stripped in strip remover and the wafer is placed in O_2 reactive ion etching (RIE) system to completely remove residual photoresist on top

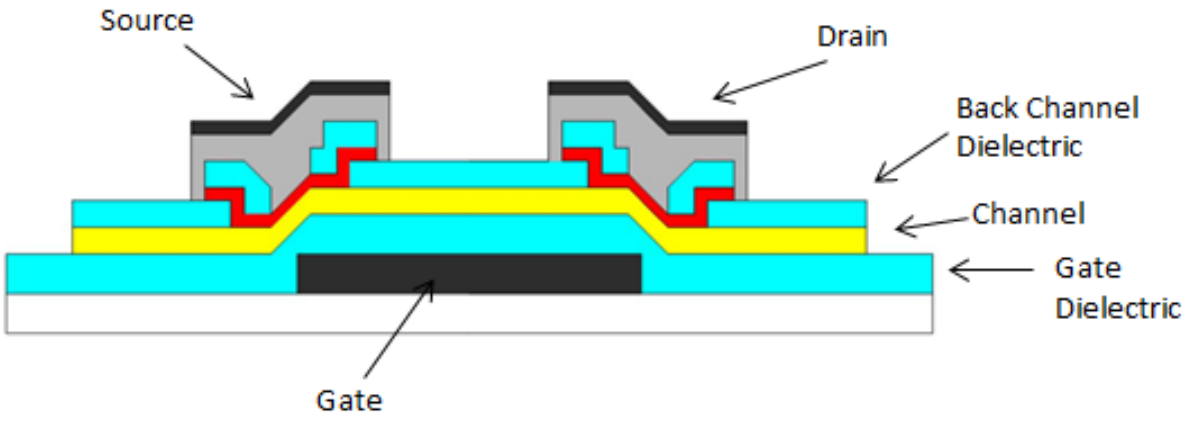


Figure 3.9: Cross section of the bottom gate a-Si:H TFT.

of Cr layer. The substrate is subsequently placed in an acetone beaker in ultrasound bath to clean the substrate thoroughly of any residual photoresists.

- In the next step the substrate is placed in PECVD system for deposition of SiN_x/a-Si:H/SiN_x tri-layer stack. Mask 2 is then used to define source and drain openings as well as transistor islands as shown in image B on Figure 3.10. The substrate is then placed in buffered HF solution for removal of the second nitride layer to form source/drain openings and transistor islands. The photoresist is again stripped and the substrate is washed thoroughly in acetone filled ultrasound bath.

- In the subsequent step, the substrate is placed in PECVD system for deposition of n+ nc-Si:H source/drain contact layer and third nitride SiN_x layer without breaking the vacuum. Mask 3 is applied to define the pattern for keeping third SiN_x and n+ on top of source/drain region. The sample is placed in buffered HF to etch third SiN_x, and without removing the photoresist the sample is placed in SF_6 RIE to etch n+ layer on TFT island as well as n+/i layer around TFT island region. This results

in the structure shown in image C of Figure 3.10. Photoresist is then stripped and the sample is washed in acetone filled ultrasound bath.

- At this point mask 4 is used to open vias in SiN_x to reach n+ layer over source and drain regions as well as the Cr layer bottom gate contact. The substrate is subsequently placed in HF to etch SiN_x to access source/drain n+ layer. Photoresist is again stripped and the wafer is washed in Acetone ultrasound bath. Figure 3.10 (image C) represents the TFT at this stage.

- The TFT is then placed in DC sputtering system to sputter source/drain metal contacts composed of Al layer capped with thin Cr layer. The choice of Al is due to its low mechanical stress permitting filling vias and steps without peeling off, and thin Cr capping layer serves as a barrier against Al oxidation and pinhole formation. Mask 5 is then used to pattern source, drain, and gate contacts, and the substrate is placed in Cr etchant and PAN etchant solutions to remove Cr and Al metal layers outside contact areas. Figure 3.10 (image D) shows the finished TFT.

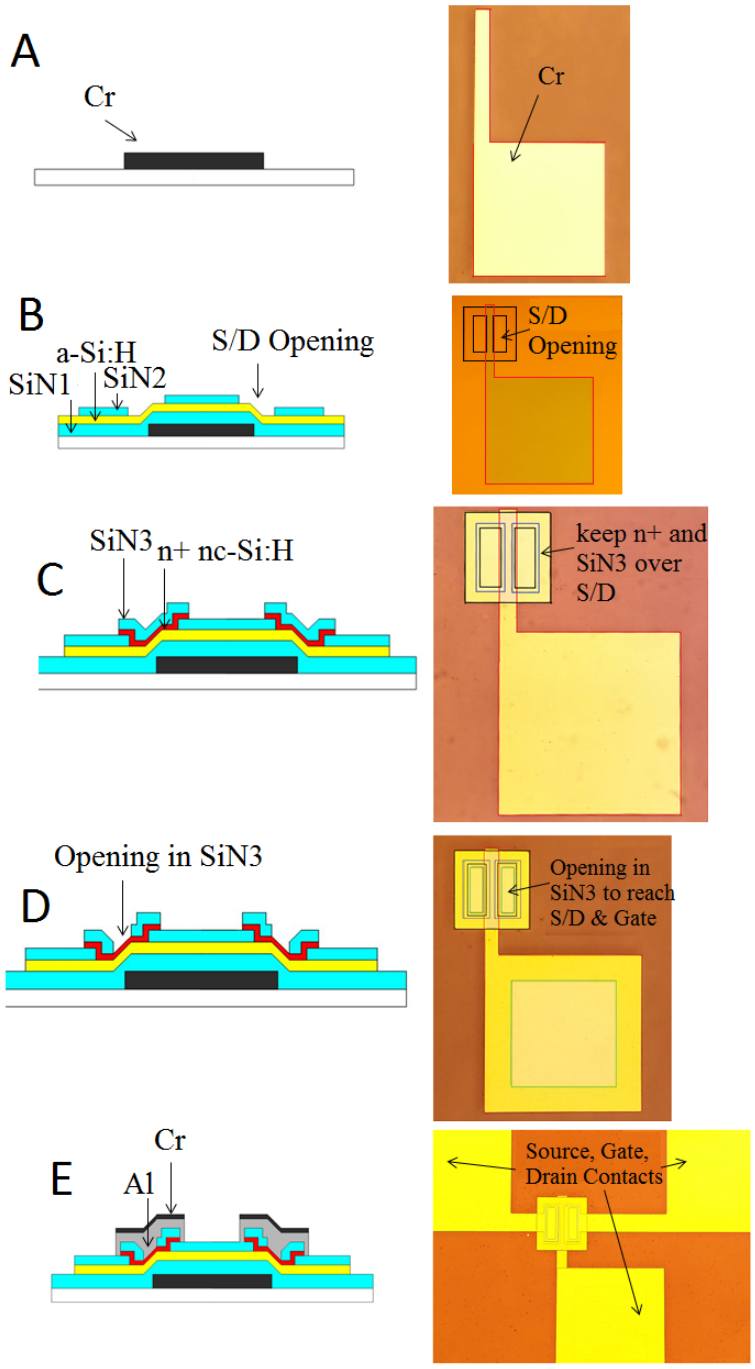


Figure 3.10: Top view and schematic cross section of TFT fabrication process.

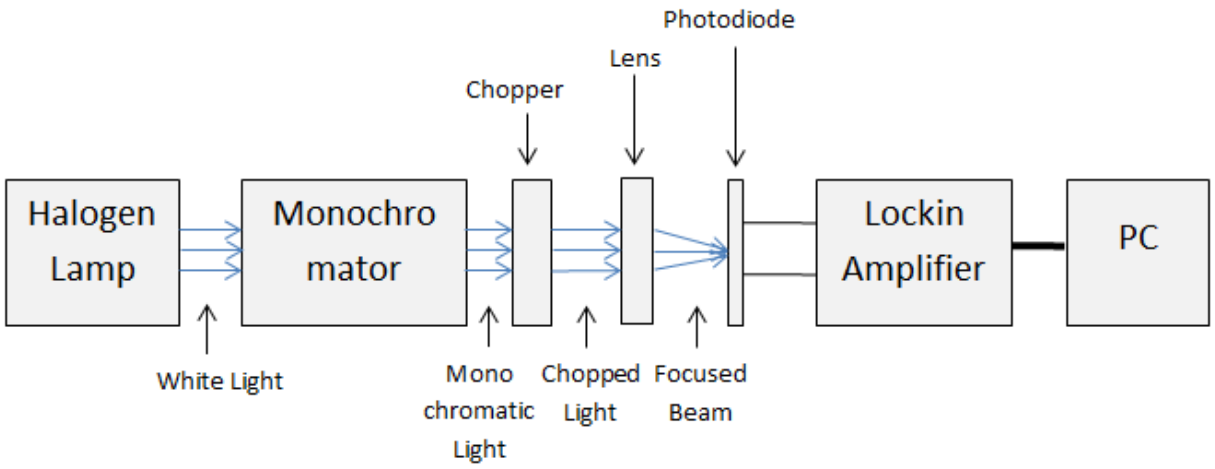


Figure 3.11: Schematic of EQE measurement setup.

3.6 Photodiode Measurement Setup and Performance Measurement

3.6.1 EQE Measurements

EQE measurements of the photodiodes were carried out using custom made EQE measurement system shown in Figure 3.11. The system comprises of a visible light source, a monochromator, a chopper rotating at frequency of 400 Hz and a lock-in amplifier to convert the photodiode current to the voltage while eliminating the background noise. The analog signal from the amplifier is connected to an analog/digital (A/D) converter to transmit digital signal to a computer for recording and monitoring. Prior to EQE measurement for each sample, EQE setup was calibrated using standard silicon photodiode detector.

3.6.2 Steady State Photo and Dark Current Measurements

The steady state dark and photocurrent measurements of the photodiodes were carried out using Agilent 4155C semiconductor parameter analyzer connected to the probe station covered with a dark blanket to minimize interference noise from the ambient light. For NIR photocurrent measurements, we used wide viewing angle (140 degrees) LED at the wavelength of 850 nm [61]. LED was mounted on a flat surface to be placed on top of the probe station at a distance of 2 cm from the sample surface. LED was connected to a Keithly 2400 source meter to control LED bias voltage and thus the emitted optical power. The optical power density emitted from the photodiode was measured by an optical power density meter prior to device photocurrent measurements.

3.6.3 Transient Photocurrent Measurements

Transient photocurrent measurements for the photodiode were carried out in the probe station using the Agilent semicondoctor parameter analyzer in the sampling mode. NIR LED was pulsed using costum designed LED pulsing circuit shown in Fig. 3.12. Our accuracy for response time measurements were limited by the sampling interval for Agilent semiconductor analyzer which was 80 μs.

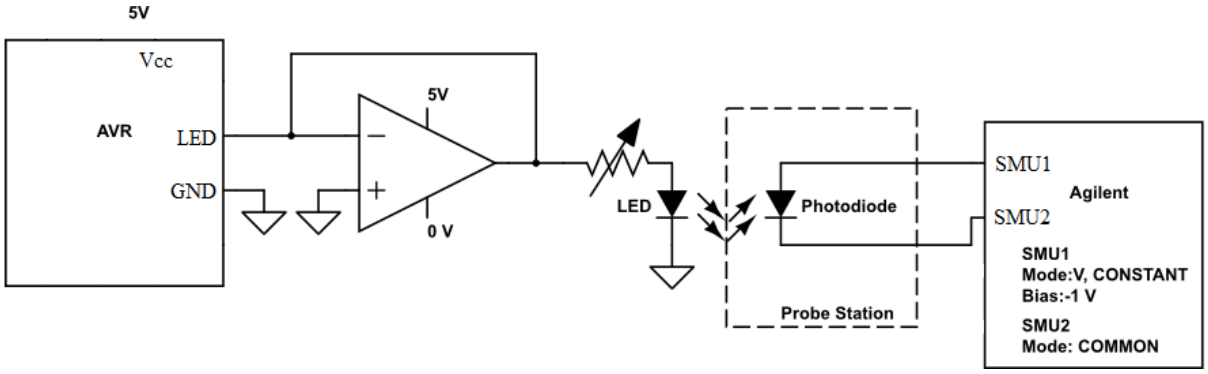


Figure 3.12: Schematic of transient photodiode measurement setup.

3.7 TFT Measurement Setup and Performance Measurements

The transfer (Id-Vgs) and output (Id-Vds) characteristics measurements of the TFT were carried out using probe station connected to the Agilent semiconductor parameter analyzer. These measurements are carried at voltage sweep steps of 0.01 V and time delay of 0.1 s. These measurements will be used in chapter 5 for extraction of TFT parameters which will be used for pixel circuit design and fabrication.

3.8 Chapter Summary

In this chapter first we summarized the material characterization experiments used for development of our μc-Si:H thin film photodiode. Subsequently, we discussed the device structure and performance figure of merits for the two components of our NIR pixel circuit e.g. the μc-Si:H photodiode and the a-Si:H TFT. In addition we presented the fabrication

sequences used to fabricate each of these devices. Finally, experimental measurement setups used for characterization of the photodiode and the TFT were shown. In conclusion, this chapter serves as a reference for all experimental procedures used in this thesis which will be refered to in subsequent chapters.

Chapter 4

Hydrogenated Microcrystalline Silicon Photodiode for NIR Detection

4.1 Undoped Microcrystalline Silicon Optimization

It was demonstrated in chapter 1 that the presence of crystalline silicon grains in μc-Si:H material is the enabling attribute for its efficient near infrared (NIR) photon absorption. In order to measure the absorption coefficient spectrum of μc-Si:H thin film, Ultraviolet/Visible/Near-Infrared transmission-reflection spectroscopy was carried out for a 0.343 μm thick μc-Si:H sample in comparison to a reference a-Si:H sample with thickness of 0.332 μm, both deposited with a standard (13.56 MHz) PECVD system using the deposition conditions summarized in Table 4.1. Figure 4.1 shows the results of transmission-reflection spectroscopy for the two samples.

Figure 4.2 compares the absorption coefficient spectra of the a-Si:H and μc-Si:H thin films of Table 4.1 calculated using the method presented in section 3.1.1.1. Notable dif-

Table 4.1: Amorphous and microcrystalline silicon deposition conditions for absorption coefficient measurements.

	Gases	Flows sccm	Press. mTorr	Power W	Temp °C	Thick nm	Time s
a-Si:H	SiH_4/H_2	40/200	900	2	180	332	3430
μc-Si:H	SiH_4/H_2	8/400	1500	10	180	343	4800

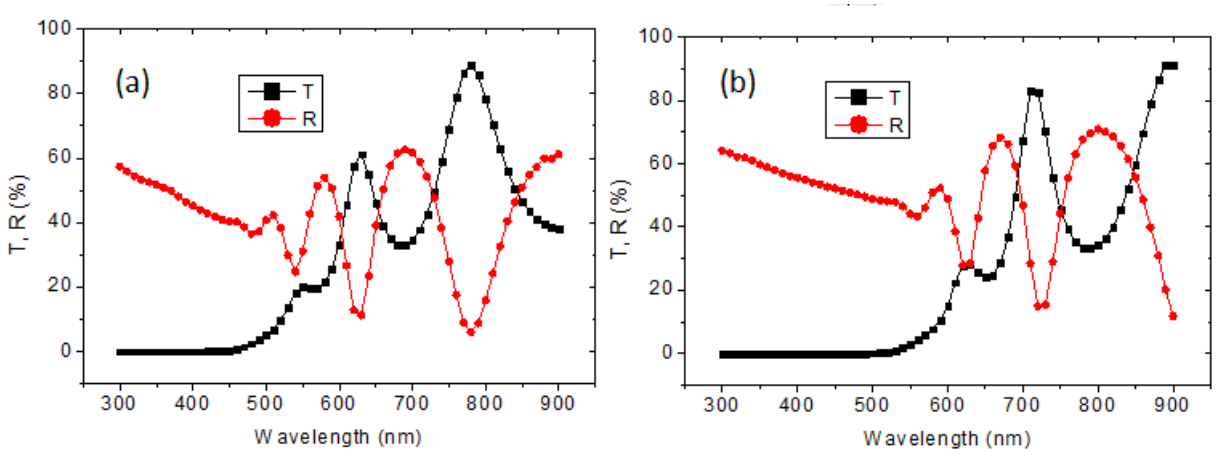


Figure 4.1: Transmission and Reflection spectra from (a) 0.332 μm a-Si:H and (b) 0.343 μm μc-Si:H films.

ference in near infrared photon absorption coefficient is observed between μc-Si:H film and its a-Si:H counterpart. For example, at 850 nm the absorption coefficient of μc-Si:H film is three orders of magnitude higher than that of a-Si:H material. This can be associated with the presence of low bandgap crystalline silicon grains. In fact, Raman spectroscopy measurements confirm the presence of crystalline silicon grains in our μc-Si:H samples as shown in Figure 4.3. Crystalline volume fraction (X_c) for μc-Si:H films is estimated to be approximately equal to 40% using the method discussed in section 3.1.1.2.

Thus μc-Si:H is more efficient NIR light absorbing material compared to its a-Si:H counterpart. However, simple μc-Si:H planar metal-semiconductor-metal (MSM) structure

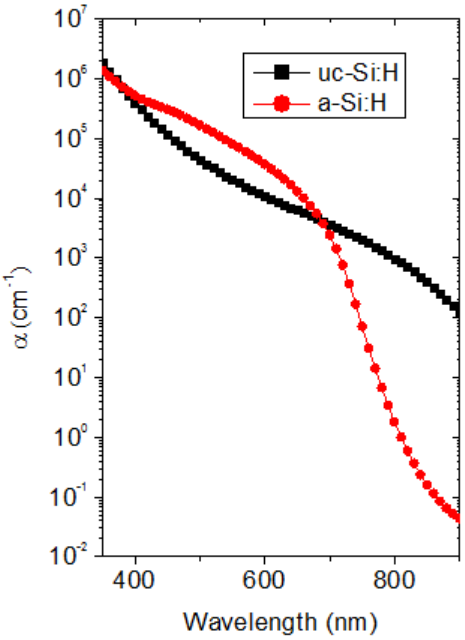


Figure 4.2: Comparison of absorption coefficient in undoped a-Si:H (0.332 μm) and μc-Si:H (0.343 μm) thin films.

(shown in Figure 3.2) is not capable to create high dynamic ratio.

Figure 4.4 compares the voltage dependent dark current and photo current flow in μc-Si:H and a-Si:H MSM structures. As it can be seen devices show nonideal behaviour at zero bias due to difficulty of ohmic contact formation in intrinsic amorphous films which is observed in other reports as well [16]. As a result intrinsic amorphous and micro-crystalline silicon MSM devices are operated at voltages above 1 V to avoid this nonideal behaviour. It is seen that the dark current in μc-Si:H film is 10^3 times higher than that for a-Si:H material which agrees with measured absorption coefficient values. As a result of such a high dark current, small photo/dark current ratio was obtained in μc-Si:H MSM detector, which is very close to the values obtained for a-Si:H MSM device (see Figure

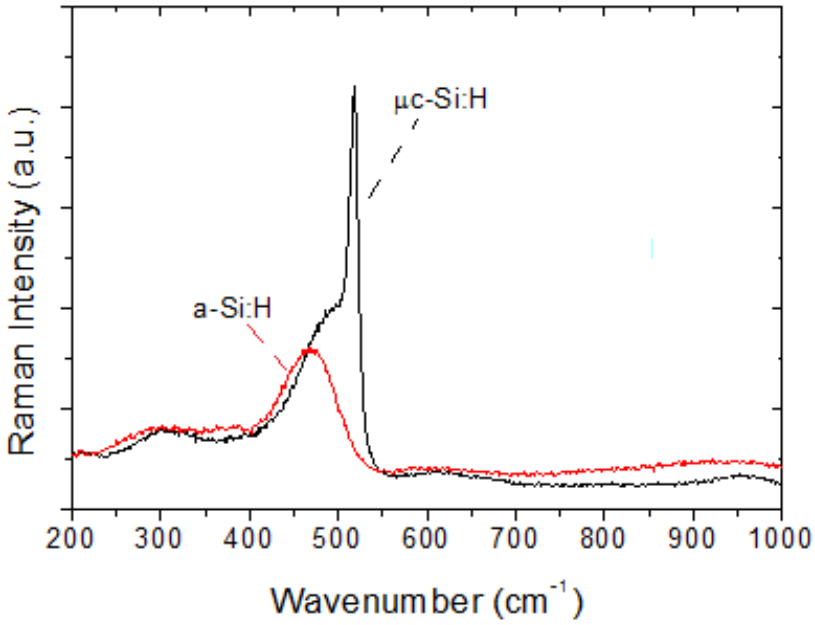


Figure 4.3: Comparison of the Raman spectra for a-Si:H (0.332 µm) and µc-Si:H (0.343 µm) samples.

4.4). Considering the I-V equations in MSM semiconductor photodetector (Ref. [5]), one can realize that changing applied bias voltage or device geomety (W/L ratio) does not affect the photo/dark current ratio. Therefore, in order to be able to take advantage of high NIR photon absorption coefficient in our µc-Si:H film, it is necessary to adopt different device structure which would have high level of photocurrent while maintaining a lower level of dark current. Hence, we focused our effort on fabrication of microcrystalline silicon photodiode to get both high photocurrent and low dark current under reverse bias condition. For this purpose, development and characterization of doped microcrystalline thin films will be necessary.

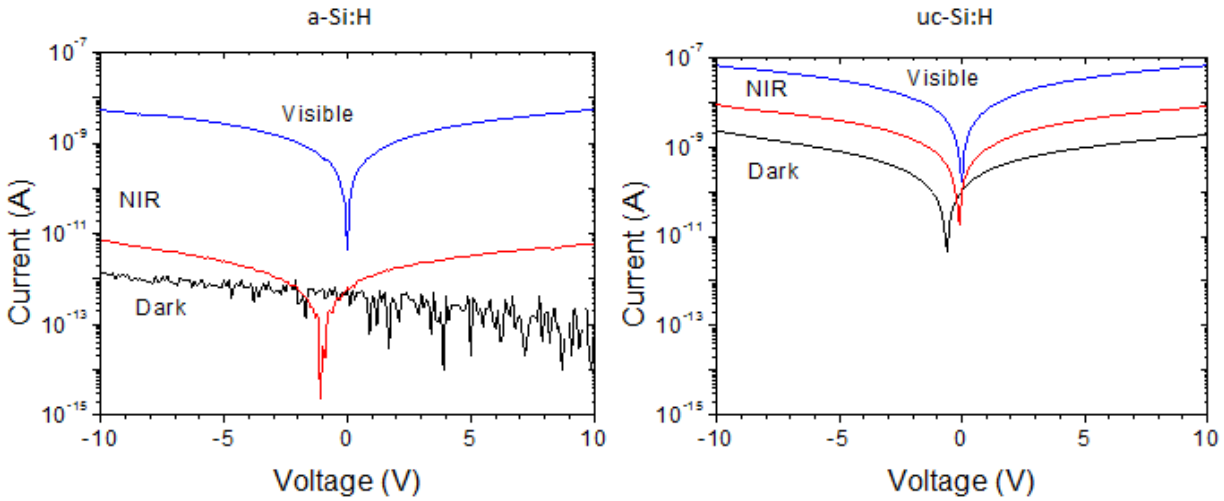


Figure 4.4: Comparison of dark current, NIR current (850 nm, 0.2 mW/cm^2), and visible current (noncalibrated) for a-Si:H (0.332 μm) and μc-Si:H (0.332 μm) MSM detectors. The coplanar contacts have a separation of L=2 mm and length of W=20 mm.

4.2 Heavily Doped n+ and p+ Microcrystalline Silicon Optimization

Doped μc-Si:H layers are required for successful fabrication of μc-Si:H photodiode detector. It is experimentally observed that using amorphous doped layers with intrinsic μc-Si:H absorber layer does not yield working photodiodes due to band-gap mismatch between amorphous and microcrystalline layers and subsequent barrier formation at microcrystalline/amorphous heterojunction interface. Table 4.2 summarizes the deposition conditions for optimized n+ and p+ μc-Si:H layers with maximum achievable dark conductivity. The optimum amorphous silicon doped layer recipes are also included in Table 4.2 for comparison. Figure 4.5 demonstrates dark I-V characteristics of doped μc-Si:H and a-Si:H thin films with identical thickness of 30 nm and coplanar contact structure. It is seen that

Table 4.2: Optimum recipes for doped μc-Si:H and a-Si:H thin films.

	Gases	Flows sccm	Press. mTorr	Power W	Temp °C	Thick nm	Crystal %	Conduct. Ωcm^{-1}
μc-Si:H								
n+	$SiH_4/H_2/PH_3$	8/400/7	1500	10	180	30	40	7.63
p+	$SiH_4/H_2/TMB$	2/200/1	900	2	180	30	20	0.02
a-Si:H								
n+	$SiH_4/H_2/PH_3$	40/80/40	900	2	180	30	N/A	4.6×10^{-3}
p+	$SiH_4/H_2/B_2H_6$	40/80/40	900	2	180	30	N/A	7.7×10^{-5}

the conductivity of μc-Si:H n-type layer is 1600 times higher than that of its amorphous counterpart, and conductivity of μc-Si:H p-type layer is 260 times higher than that of its amorphous counterpart. Crystallinity in microcrystalline doped layers was estimated using Raman spectroscopy where distinctive peaks at 520 cm^{-1} are observed corresponding to crystalline silicon phase within the film. Trimethylborane gas was used for p-type μc-Si:H film deposition whereas conventional diborane gas was used for p-type a-Si:H film. In addition, the crystallinity of p type μc-Si:H is 20%, which is lower than 40% crystalline volume fraction in n type μc-Si:H layer. The reason is that the presence of boron atoms supresses crystalline growth due to catalytic reaction with hydrogen resulting in the loss of surface hydrogen coverage [62].

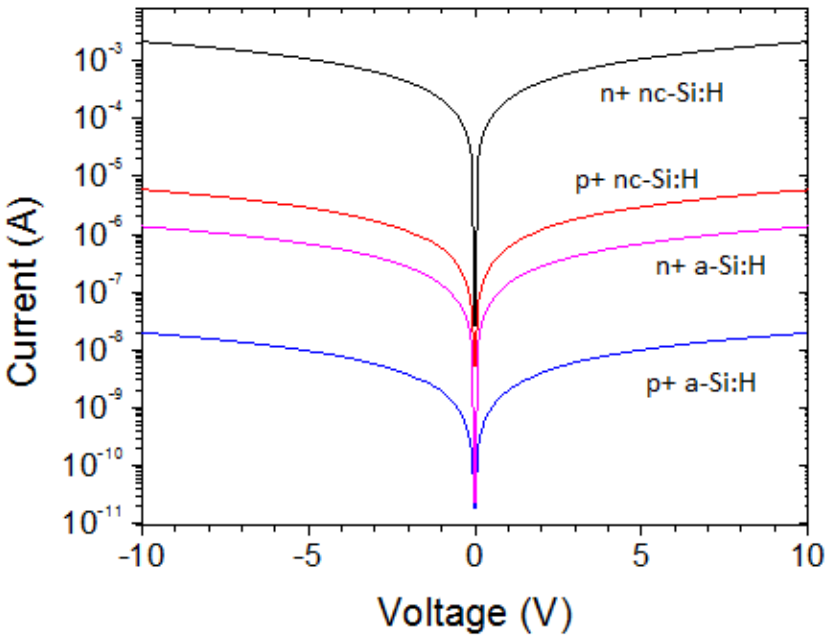


Figure 4.5: Dark IV measurements of doped amorphous and nanocrystalline silicon thin films of Table 4.2. All films have a thickness of 30 nm with a coplanar device structure with electrode separation of L=2 mm and electrode width of W=20 mm.

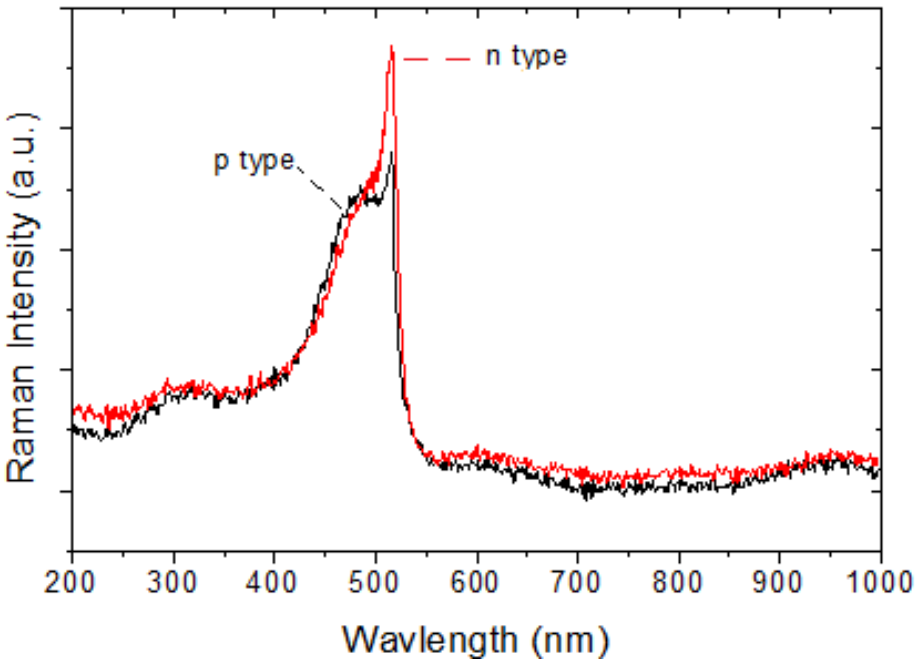


Figure 4.6: Comparison of Raman spectra for n type and p type doped μc-Si:H films of Table 4.2.

4.3 AZO Optimization

Aluminum doped zinc oxide (AZO) transparent conductive oxide (TCO) is used as front contact in our photodiodes. The thickness of the AZO layer (d) must be tuned to minimize reflected wave at 850 nm wavelength (wavelength of interest in our application) based on the following quarter wavelength antireflective coating design criteria [63],

$$d = \frac{(2m+1)\,\lambda}{4n} \tag{4.1}$$

Here λ is the wavelength of light in vacuum, n is the refractive index of AZO at that wavelength, and $2m+1$ is an odd number. In order to be able to calculate d using Equation 4.1, we need to calculate refractive index (n) of AZO layer first. Transmission and reflection spectroscopy of 272 nm thick AZO layer (sputtering conditions are summarized in Table 4.3) was used for calculation of AZO refractive index using the method discussed earlier in section 3.1.3.1 and assuming that the absorption coefficient of AZO is equal to zero in visible and NIR region.

As it can be seen from Figure 4.7 (b), for λ=850 nm, the refractive index is n=1.66. By plugging the values of λ and n back into Equation 4.1 and choosing m to be 1, the antireflection coating thickness at 850 nm is calculated to be 384 nm. The sheet resistance for 384 nm AZO layer was measured to be 58.3 Ω/□. For the case of m=0, the calculated antireflection coating thickness from Equation 4.1 is 128 nm, which results in the sheet

Table 4.3: Summary of sputtering conditions of AZO layer.

	Gases	Flows sccm	Press. mTorr	Power W	Temp °C	Thick nm	Sheet Resistance Ω/□
AZO	Ar	15	5	80	150	272	97.6

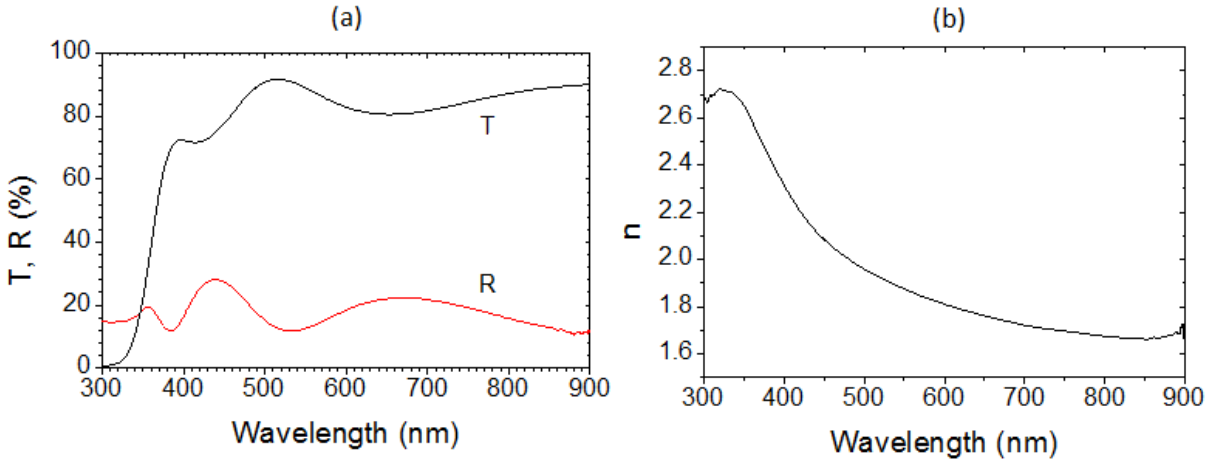


Figure 4.7: (a) UV-VIS-NIR transmission-reflection spectroscopy of AZO thin film on glass and (b) calculated refractive index of the AZO film.

resistance of 332.3 Ω/□.

4.4 Photodiode Characterization

Photodiode fabrication process is the same as the one discussed in section 3.4. Microcrystalline silicon photodiode was fabricated on glass substrate using intrinsic and doped μc-Si:H thin film recipes presented earlier in section 4.1 and 4.2, which are summarized in Table 4.4.

The thickness of Cr layer is 200 nm resulting in the sheet resistance of 4.46 Ω/□. Aluminum doped zinc oxide (AZO) transparent conductive oxide (TCO) was sputtered at substrate temperature of 150 °C with thickness of 384 nm and sheet resistance of 58.3 Ω/□. Photodiodes with various areas ranging from 1 cm^2 down to 2500 μm^2 were fabricated. Devices with the area of 1 cm^2 were used for EQE measurement since the spot size of EQE system beam is larger than 1 mm^2. Smaller devices were used for I-V measurements.

Figure 4.8 shows the EQE of the microcrystalline silicon photodiode shown in Figure 3.8 with AZO antireflective coating layer thickness of 384 nm (3/4 wavelength antireflective coating). EQE for an a-Si:H photodiode fabricated using conditions shown in Table 4.4 is included for comparison. The dark and photo I-V characteristics for both μc-Si:H and a-Si:H photodiodes are presented in Figure 4.9 for device with the area of 0.25 mm^2. The logarithmic scale on y-axis are used here for better visual comparison of the current in the devices. Photo I-V characteristics was measured at 850 nm and incident power density of 0.2 mW/cm^2 for both photodiodes. It can be seen from Figure 4.8 and 4.9 that EQE and photocurrent for microcrystalline sample is two orders of magnitude higher than the one for its a-Si:H counterpart with similar intrinsic layer thickness. Figure 4.10 compares photo-to-dark current ratio in microcrystalline and amorphous photodiodes as a function of applied bias voltage. It is seen that the ratio is higher for negative bias values and reaches its maximum at zero bias condition where dark current is equal to zero. Unfortunately, in

Table 4.4: Summary of the deposition conditions of n-i-p μc-Si:H photodiode and n-i-p a-Si:H photodiode.

	Gases	Flows sccm	Press. mTorr	Power W	Temp °C	Thick nm	Crystal %	Conduct. Ωcm^{-1}
μc-Si:H								
n+	$SiH_4/H_2/PH_3$	8/400/7	1500	10	180	30	40	7.63
i	SiH_4/H_2	8/400	1500	10	180	343	40	5.8×10^{-7}
p+	SiH_4/H_2/TMB	2/200/1	900	2	180	30	20	0.02
a-Si:H								
n+	$SiH_4/H_2/PH_3$	40/80/40	900	2	180	30	N/A	4.6×10^{-3}
i	SiH_4/H_2	8/400	1500	10	180	332	N/A	$<5\times10^{-10}$
p+	$SiH_4/H_2/B_2H_6$	40/80/40	900	2	180	30	N/A	7.7×10^{-5}

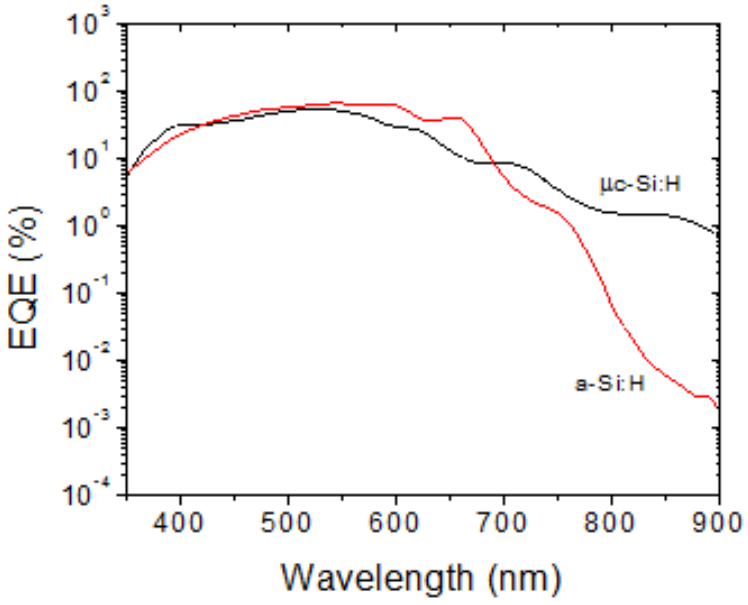


Figure 4.8: EQE of μc-Si:H photodiode (with intrinsic layer thickness of 343 nm) and a-Si:H photodiode (with intrinsic layer thickness of 332 nm).

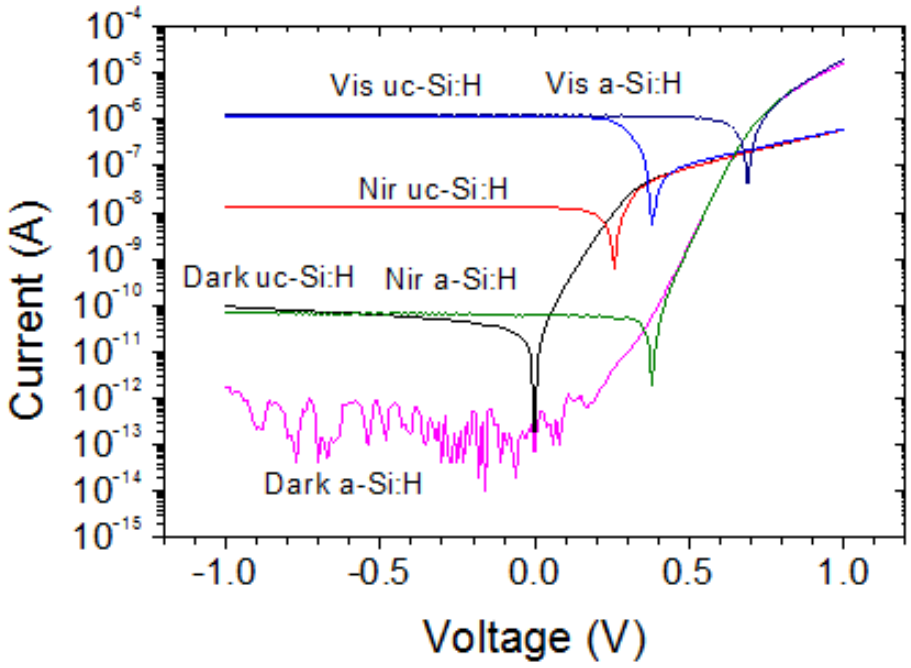


Figure 4.9: Comparison of dark, NIR (850 nm, 0.2 mW/cm^2), and visible (noncalibrated) photocurrent flow in μc-Si:H and a-Si:H photodiodes.

practical applications, where 2D array of photodiodes is needed, it is not feasible to bias each diode at its short circuit condition due to practical complications arising from the number of required readout amplifiers and complex wire routing [64, 65, 66]. Therefore, photodiodes are usually configured in such a way that their anode (p contact) is biased at a negative voltage and the cathode (n contact) is connected to a capacitor, which can store the photo generated charge for subsequent readout cycles. As a result, the bias for the photodiode can swing from negative bias to short circuit and to open circuit condition in 2D imaging array systems. Hence the photo-to-dark ratio must be investigated at negative bias voltages because short circuit operation is inevitably impossible in 2D arrays.

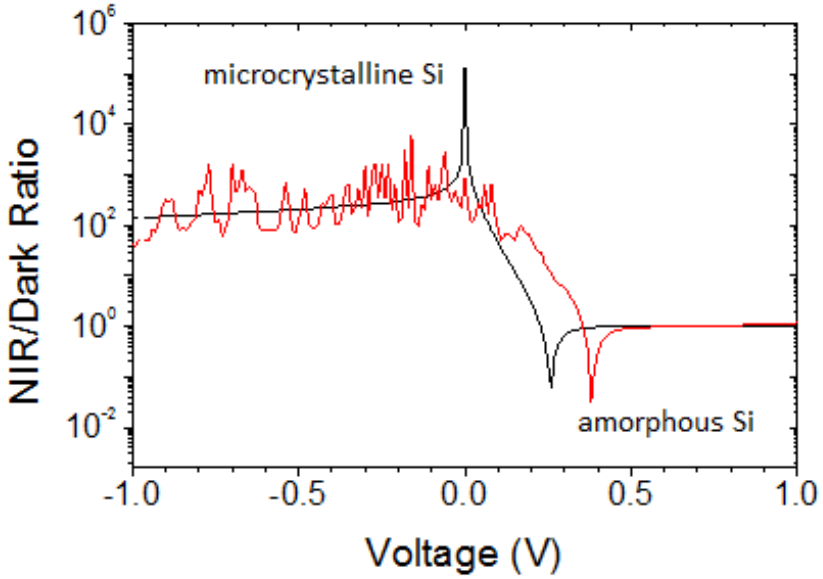


Figure 4.10: Comparison of NIR photo/dark ratio in a-Si:H and μc-Si:H photodiodes of Table 4.4.

4.5 Undoped Layer Thickness Effect

In the previous section, we saw that EQE for microcrystalline silicon diode with i layer thickness of 343 nm is about 2 %. Even though this value is more than two orders of magnitude higher than that for its amorphous counterpart, it is still considered to be low compared to maximum EQE of this device (50 %) achieved in visible wavelength region. Therefore operation of these microcrystalline photodiodes under ambient light requires visible light to be filtered out with very strong attenuation in the visible region. In order to make μc-Si:H photodiodes more practical for operation under ambient light conditions, it is necessary to increase EQE in NIR region. One possible solution for enhancement of EQE at NIR wavelengths is to increase the intrinsic layer thickness. For this purpose

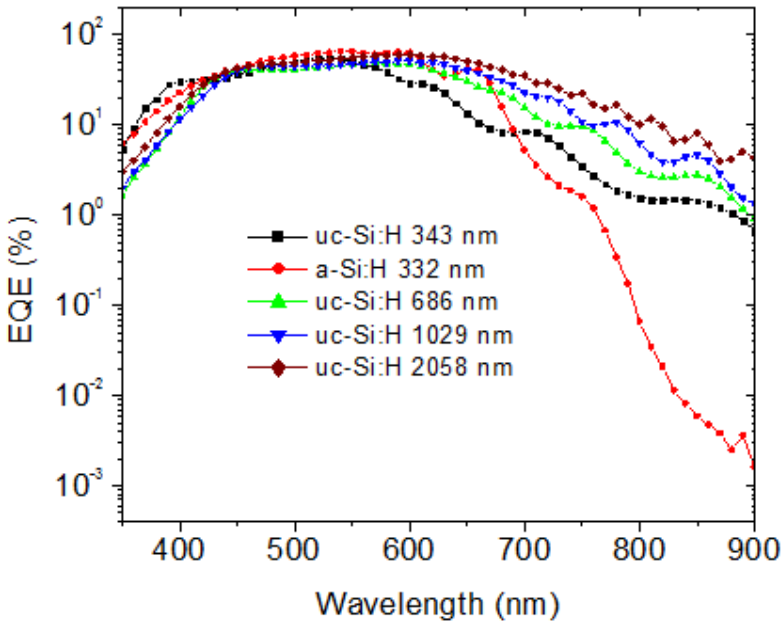


Figure 4.11: Comparison of EQE for μc-Si:H photodiodes with various thicknesses.

i-layers with several different thicknesses; e.g. 343nm, 686 nm, 1029 nm, and 2058 nm were prepared. EQE spectra for these microcrystalline silicon photodiodes are shown in Figure 4.11. As it can be seen in Figure 4.11, EQE in NIR region increases by increasing the intrinsic layer thickness. Figure 4.12 shows I-V characteristics of these photodiodes under dark condition and under incident light with the wavelength of 850 nm and power density of 0.2 mW/cm^2. The NIR photocurrent level was improved by a factor of 3.6 at i-layer thickness of 2085 nm compared to i-layer thickness of 343 nm. However, it is observed that the dark current also increased by similar ratio of 3.5. In p-i-n photodiode, the electric field is built across the entire i-layer and the thermally generated carriers are being swept to contacts. In microcrystalline silicon, the mobility-lifetime product was reported to be in the range of 10^{-6} cm^2/Vs [67], hence the increase in absorption layer thickness up to tens

of micrometers increases dark current proportionally in agreement with the results shown in Figure 4.12.

Therefore, it might seem that increasing i layer thickness does not have any advantage. However, a closer inspection of I-V characteristics reveals that the enhancement factor for the current in the visible range is 2.157, which is less than the one at 850 nm (3.5). Therefore, even though the dynamic range at 850 nm remains the same, the dynamic range for visible light is reduced and hence the devices becomes less prone to the interference from ambient light.

In Figure 4.12, the minimum in logarithmic representation of absolute value of the current corresponds to open circuit voltage condition. For dark current, the open circuit voltage is zero. Under 850 nm illumination, even though the photocurrent increases with thickness, the dark current also increases proportionally, hence the photo-to-dark current ratio stays the same. As the result, the open circuit voltage is similar for the photodiodes with different undoped layer thickness. In contrast, under visible light illumination, the photocurrent in thicker samples does not increase as much as the dark current, hence the open circuit voltage is reduced.

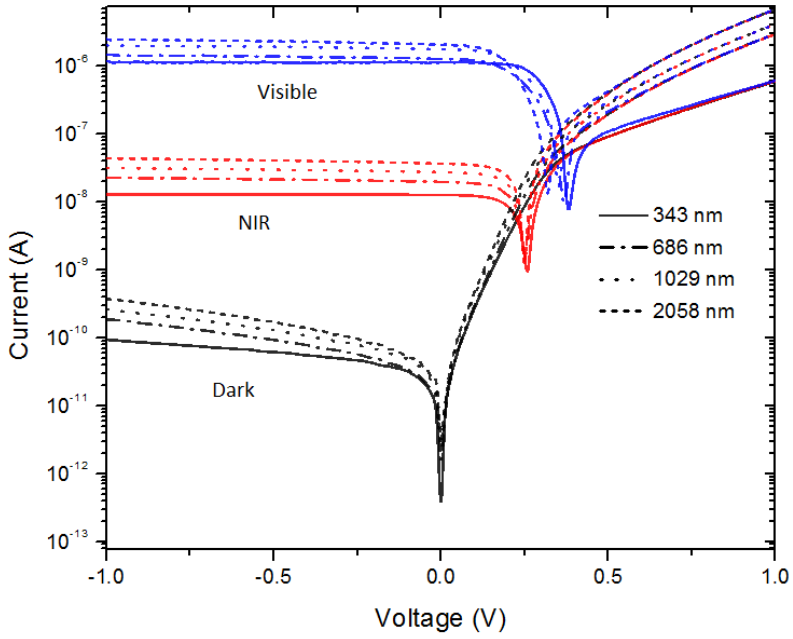


Figure 4.12: Comparison of dark, NIR (850 nm, 0.2 mW/cm^2), and visible light (noncalibrated) photocurrent in μc-Si:H photodiodes with various intrinsic layer thicknesses.

4.6 EQE Enhancement By Using Textured Back Reflector

4.6.1 Fabrication and Performance Evaluation

In the previous section we saw that one way to enhance EQE for NIR wavelengths is to increase intrinsic layer thickness in order to increase possibility of photon absorption in the intrinsic layer. Another way to enhance traveling path of photons inside the intrinsic layer is to scatter photons using textured back reflector so that the photons which do not get absorbed on the first pass and reach the bottom surface of the photodiode get scattered in

all directions rather than being vertically reflected.

In order to enhance diffuse reflection, it is required to have textured surface which can scatter light in all directions. Aluminum doped zinc oxide (AZO) is a well-known material to yield rough surface when etched in HCL solution [68, 69, 70]. We prepared four samples of AZO films on glass substrate in order to study haze properties of textured AZO surfaces. The deposition conditions of these four AZO samples were the same as the one in Table 4.3 except for the thickness, which was 3 μm. Three of these four samples were immersed in 0.5 % HCL solution in water for 2 min, 4 min, and 6 min, respectively, which gave rough AZO films with thickness of 2.5 μm, 2 μm, and 1 μm, respectively. Figure 4.13 shows haze measurements of these samples using an integrating sphere. It is seen that the surface texturing increases film haze value due to enhanced scattering of light with rougher surfaces (sample 4) resulting in higher haze percentage.

The textured AZO sample 4 shows the highest haze of 10% among the samples at the wavelength of 850 nm. This textured AZO (sample 4) was used on top of 200 nm thick Cr layer and nip μc-Si:H photodiode stack with intrinsic layer of 2058 nm to create a photodiode with textured back reflector. Figure 4.14 compares the EQE for the photodiode with textured back reflector to the one without it. The measurements show that EQE is increased in NIR region when the textured back reflector is used and interference fringes in EQE spectrum disappeared due to random scattering of light in all directions. Figure 4.15 compares the bias dependent dark and photo current characteristics of the photodiode with textured back reflector compared to the one without it. It is seen that the photocurrent level is increased from 4.2×10^{-8} A to 10^{-7} A as previously predicted by EQE curves. However, the dark current remains at the same level. As a result, the dynamic range of the device is increased by a factor of 2.4.

Indeed, in devices with textured reflector, the photocurrent shows higher increase at

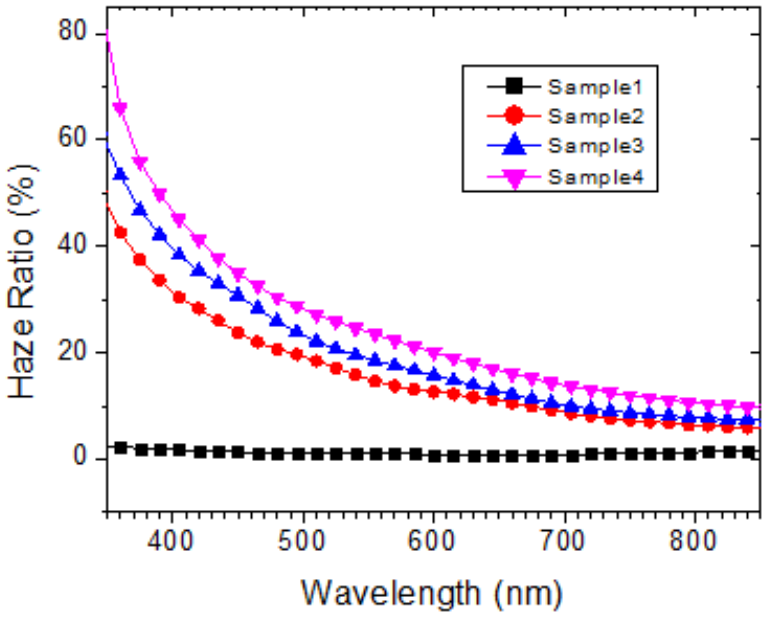


Figure 4.13: Comparison of haze ratio in four AZO samples with initial thickness of 3 μm etched in 0.5 % HCL solution for 0 min (sample1), 2 min (sample2), 4 min (sample3), and 6 min (sample4).

NIR than at visible light. The reason is that the visible light must be largely absorbed before reaching the back reflector due to shorter absorption depth (e.g. microcrystalline silicon absorption coefficient is about $10^5\ cm^{-1}$ at 500 nm but about $10^3\ cm^{-1}$ at 850 nm). Hence NIR light is not well absorbed after one pass through the absorber and thats why the scattering of light has strong effect on EQE at NIR.

4.6.2 Modeling and Parameter Extraction

In order to be able to design pixel circuit based on our photodiode, we need to come up with the circuit model for the photodiode. Single diode circuit model for the n-i-p photodiode

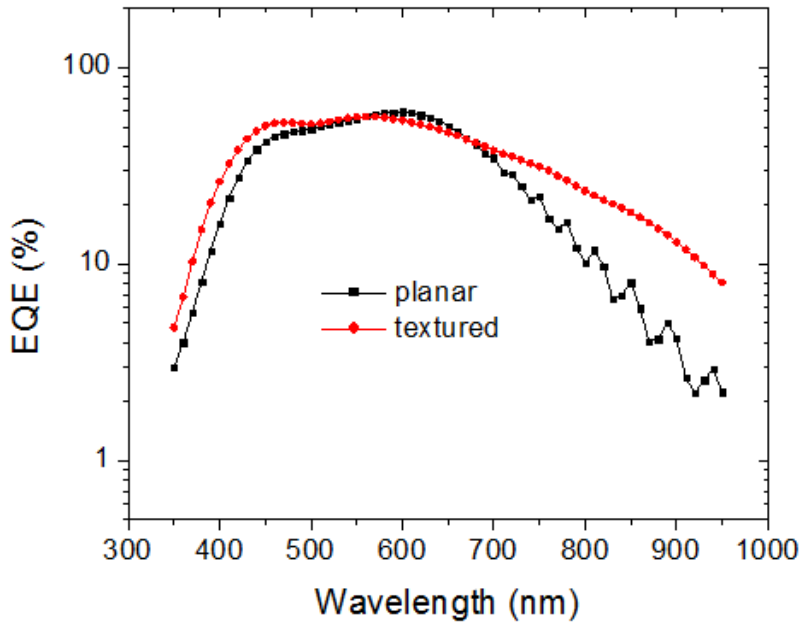


Figure 4.14: Effect of applying a 1 μm thick textured back reflector on enhancement of EQE in NIR region.

is shown in Figure 4.16 [71]. The model consists of a diode in parallel with a photocurrent source (I_{ph}), a shunt resistor (R_{sh}), a capacitor (C) and a series resistor (R_s). For the photodiode we use the non-ideal diode I-V characteristics:

$$I_d = I_s \left(e^{\frac{q(V_d - I_d \times R_S)}{nkT}} - 1 \right) - \frac{V_d - I_d \times R_s}{R_{sh}} \tag{4.2}$$

Here I_d is the photodiode current, I_s is the saturation current, V_d is the photodiode voltage, k is the Boltzmann constant, T is the measurement temperature, q is the electron charge and n is the ideality factor. In the region where $\frac{qI_d \times R_s}{nkT} \ll \frac{qV_d}{nkT}$, Equation 4.2 can be approximated as follows,

$$I_d = I_s \left(e^{\frac{qV_d}{nkT}} - 1 \right) \tag{4.3}$$

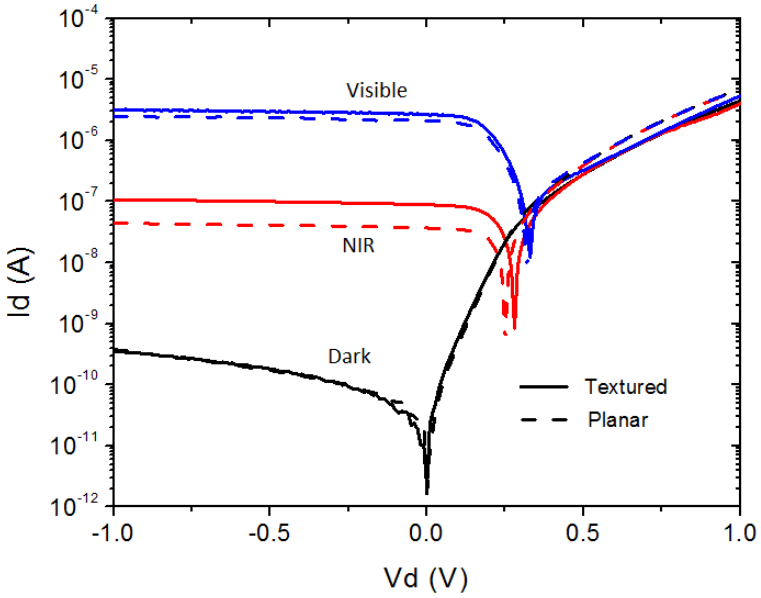


Figure 4.15: Bias dependent photo and dark current levels for a photodiode with intrinsic layer thickness of 2058 nm with and without 1 μm thick AZO textured back reflector.

The slope (S) of the natural logarithm of I_d versus V_d in this region can be used to estimate the diode non-ideality factor, n, as follows.

$$n = \frac{q}{SkT} \tag{4.4}$$

The slope of $S = 24.84$ and nonideality factor of $n = 1.54$ was obtained for our textured photodiode. Diode reverse saturation current value equal to $I_s = e^{-23.73} = 4.94 \times 10^{-11}$ was obtained from the vertical axis intersection of the linear fit with $\ln(I_d)$-V_d curve. In reverse bias region the exponential term in Equation 4.2 can be ignored and the following equation can be used to model the behaviour of the photodiode in reverse bias region:

$$I_d = -I_s - \frac{V_d - I_d \times R_s}{R_{sh}} \tag{4.5}$$

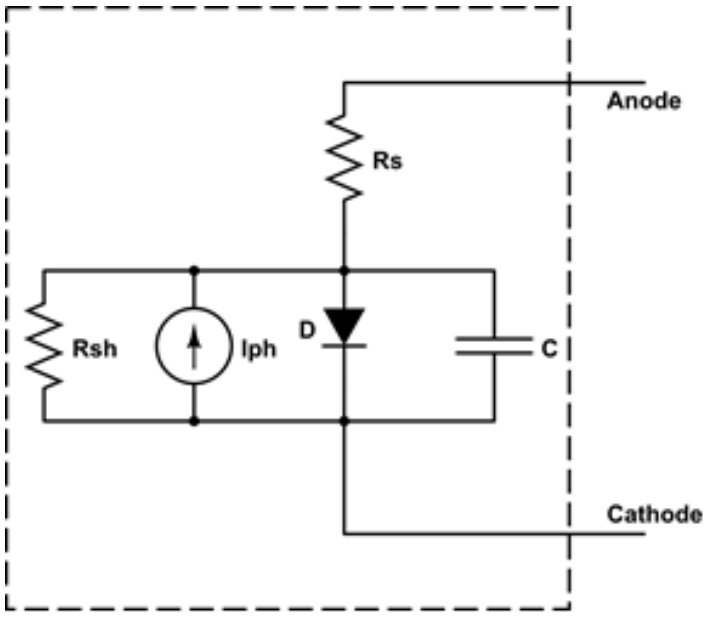


Figure 4.16: Equivalent circuit model for the μc-Si:H photodiode.

Equation 4.5 can be rearranged as follows,

$$I_d = \frac{-I_s - \frac{V_d}{R_{sh}}}{1 - \frac{R_s}{R_{sh}}} \tag{4.6}$$

Assuming that the series resistance R_s is much less than the shunt resistance R_{sh}, Equation 4.7 can be simplified as follows,

$$I_d = -I_s - \frac{V_d}{R_{sh}} \tag{4.7}$$

The shunt resistance can then be obtained from the inverse of the slope of the I-V characteristics in reverse bias region as shown in Figure 4.18. For this photodiode the slope is 7.37×10^{-10} and the shunt resistance is therefore 1.35 GΩ. After all the previous parameters such as n, I_{sh}, and I_s are extracted, the parameter R_s can be estimated with help of

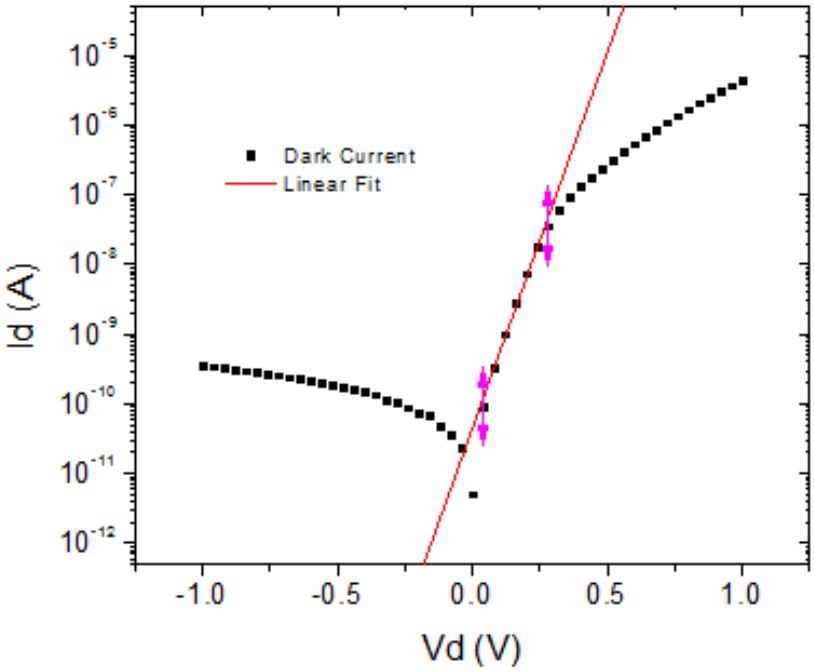


Figure 4.17: Linear fit to ln(I_d)-V_d curve for extraction of n and I_s parameters.

HSpice circuit simulator as follows.

Matlab function named Diode_Fit_Error is written, which accepts the parameter R_s as input (Note that the other parameters such as n, I_s, and R_{sh} are known at this point). This Matlab function then builds an HSpice netlist description for the circuit shown in Figure 4.16 using the value of input variable R_s and the values extracted for n, I_s, and I_{sh} calculated previously. Then HSpice is invoked to read the netlist in order to solve for I_d by sweeping the photodiode bias voltage from -1 V to 1 V. Finally, a minimum least square error value, which indicates the deviation of simulated I_d vector from the actual measured I_d vector, is returned by this Matlab function as the function output. The Diode_Fit_Error function is used with the Matlab fminbnd (which finds minimum

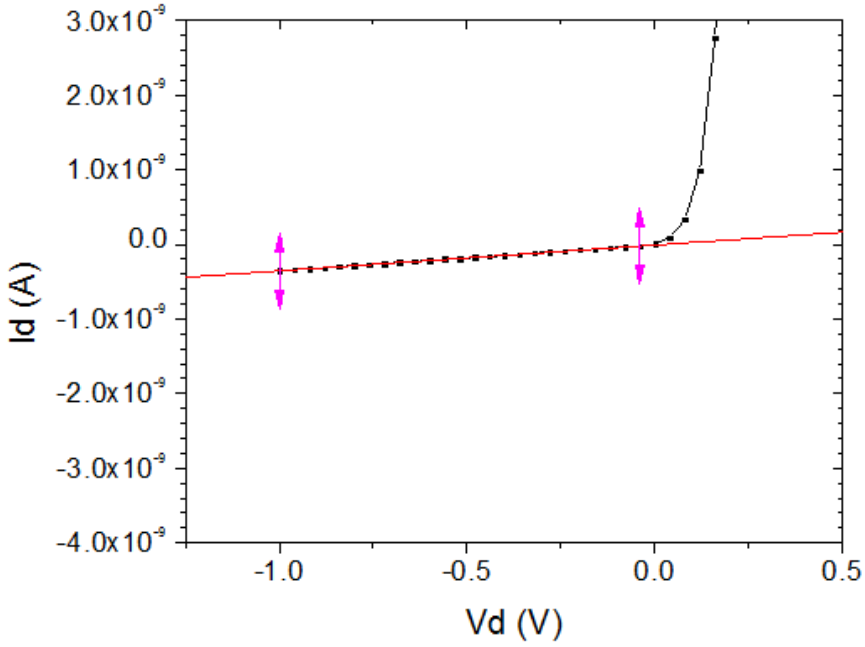


Figure 4.18: Extraction of diode shunt resistance from the slope of linear fit to photodiode I-V characteristic in reverse bias region.

of a single variable function in a bounded region) to calculate the optimum value of R_s that minimizes the least square fitting error between HSpice simulation and measurement results. Figure 4.19 shows the optimum solution for the curve fitting problem finding R_s value of 191.3 KΩ.

The capacitance of the diode was measured using an RLC meter under dark condition with sweeping voltage in the range of -1 V to 1 V using a sinusoidal signal with amplitude of 10 mV and frequency of 2 MHz. One can see that the capacitance is 40 pF at -1 V and increases to 180pF at 1 V. This is due the fact that the depletion region is wider under reverse bias conditions. Table 4.5 summarizes the results of photodiode parameter extraction for the square diode with area of $500 \times 500\ \mu m^2$. These model parameters were

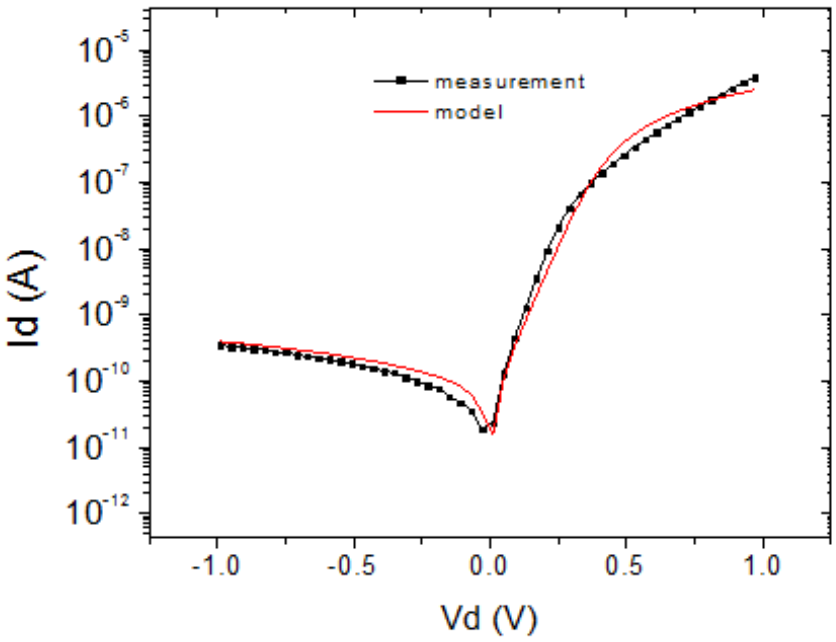


Figure 4.19: The optimum model simulation fit to measured data.

Table 4.5: Summary of μc-Si:H photodiode equivalent circuit model parameters for the circuit shown in Figure 4.16.

Parameter	n	I_s	R_{sh}	R_s	C_s
Value	1.54	4.94×10^{-11} A	1.35 GΩ	191.3 kΩ	40 pF

later used for simulation of NIR photodetector pixel circuit.

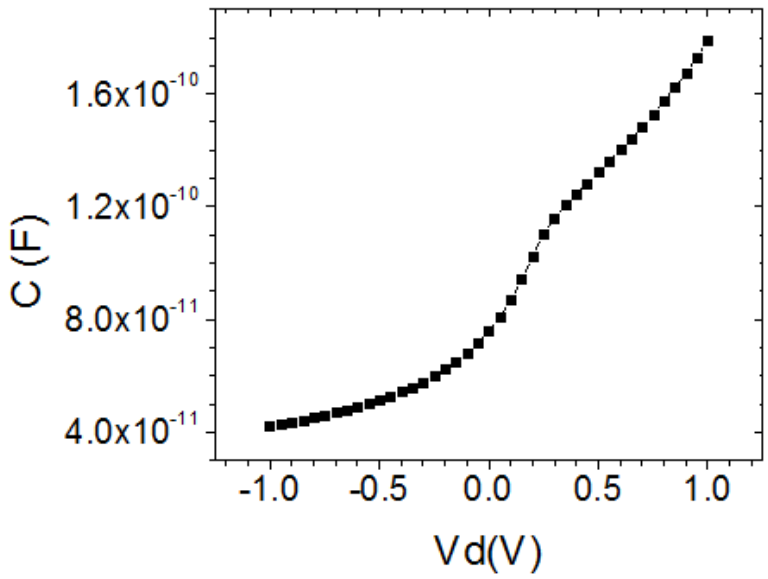


Figure 4.20: Capacitance of the μc-Si:H photodiode with the area of 500×500 μm^2 measured with sinusiodal voltage with amplitude of 10 mV and frequency of 2 MHz.

4.7 Chapter Summary

In this chapter, first we measured the absorption coefficient in μc-Si:H thin film and demonstrated that its absorption coefficient is 3 orders of magnitude higher than its amorphous silicon counterpart. We concluded that microcrystalline silicon is very suitable for large area NIR photodetector applications. However, measurements on fabricated coplanar MSM photodetector based on μc-Si:H revealed a very poor dynamic range of operation for the MSM detector due to the high levels of dark current in the device. The dynamic range of operation of the device was 10 when exposed to 850 nm light with intensity of 0.2 mW/cm^2. In order to be able to take advantage of the high absorption coefficient in the μc-Si:H we decided to consider a different device configuration which can result in a higher dynamic

range of operation. As a result, we developed doped n-type and p-type μc-Si:H thin films for fabrication of μc-Si:H photodiode. We demonstrated that n-i-p μc-Si:H photodiode with optimized anti-reflection coating layer can result in EQE values as high as 2 % and dynamic range of operation of more than two orders of magnitude compared to dynamic range of one order of magnitude in MSM device with similar thickness. We experimented the fabrication of same photodiode by increasing its i layer thickness up to 2085 nm. The EQE was increased from 2 % up to 8 %, however the dynamic range didn't change due to similar amount of increase in dark current. By using a 1 μm thick AZO textured back reflector we were able to increase the EQE at 850 nm up to 19.2 % achieving a dynamic range of 200 at incident light intensity of 0.2 mW/cm^2. The dynamic range achieved in our work is almost 13 times higher than the best reported inorganic large area NIR detector which belonged to a-SiGe:H phototransistor, and twice better than the best organic NIR detector based on cyanine small molecule photodiode. In order to be able to design a pixel circuit based on our developed photodiode we needed to extract a circuit model of our photodiode. We modeled the photodiode with a nonideal diode in parallel with a current source. We used a parallel resistor to model the shunt behaviour and a series resistor to model the series resistance of the diode. A method for extraction of this circuit model parameters was developed for the thin film photodiode using HSpice simulator and parameters were extracted for a device with area of 500×500 μm^2. The photodiode circuit model is used in chapter 5 for design and analysis of hybrid photodiode/TFT pixel circuits.

Chapter 5

Pixel For NIR Imaging

5.1 Operation of a Conventional 1 Photodiode 1 TFT Pixel Circuit

In the previous chapter we discussed the fabrication, characterization, and modeling of μc-Si:H photodiode detector and developed a circuit model for its optoelectrical behavior. As we mentioned earlier in chapter 2, when it comes to fabrication of a large two dimensional (2D) array of photodiodes, it becomes practically impossible to connect each photodiode in the array to an individual readout amplifier due to arising complications in wire routing and increased cost of readout circuitry. To solve this issue, a row based readout scheme has been adopted in which TFTs are integrated with the photodiodes in a configuration that allows for in-pixel storage of photo-generated charge. The charge stored in the pixels of each row are then read out simultaneously and the process continues until the entire data stored in the rows are retrieved. Schematic illustration of such a system is shown in Figure 5.1 [72]. In this architecture, the gates of all TFTs of one row are tied together

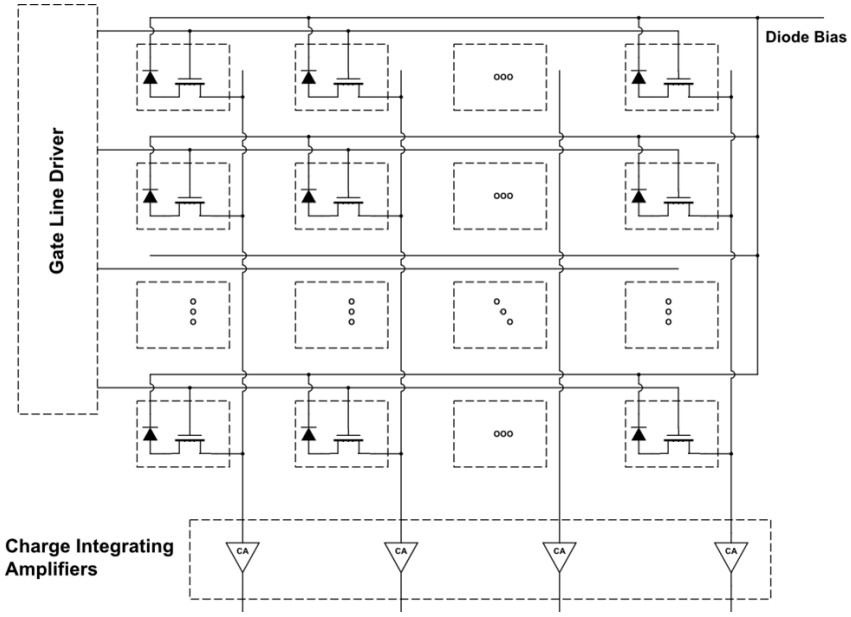


Figure 5.1: Architecture of a conventional 2D photodiode imaging system.

and connected to their corresponding gate-line driver circuitry. The drains of all TFTs of each column are also tied together and connected to the input of corresponding column charge integrating amplifier. The cathode of each photodiode is connected to the source of its corresponding TFT, and the anode contacts of all photodiodes are connected to a common diode bias voltage. The operation of the 2D imaging system can be divided into four different phases as follows:

Reset Phase

In reset phase, all photodiodes are discharged by activating all gate lines (turning on all TFT switches) simultaneously.

Capture Phase

Immediately after the reset phase, all TFTs are turned off, and the array is exposed

to light. Each photodiode generates charge proportional to the amount of incident light on that photodiode. This charge is stored in pixel capacitor.

Wait Phase

The wait phase is a period of time between the capture phase and the readout phase. This period differs from one row to another in a row-by-row readout scheme. As a result, the wait time for the first row can be zero whereas the wait time for the last row is $(N-1) \times t_{readout}$, where N is the number of rows and $t_{readout}$ is the readout time required for each row.

Readout Phase

During the readout phase, gate lines are activated on a row-by-row basis. As a result, all TFTs in one row are turned on while the TFTs in the other rows remain off. In this way all photodiodes in a specific row get connected to the external charge amplifiers, which discharge pixel capacitors in that row and convert the charge into the output voltage. This process is repeated until all rows are discharged and the amount of charge stored in each pixel is measured.

5.2 Development of TFT Model

5.2.1 TFT Fabrication and Characterization

As demonstrated in Figure 5.1, fabrication of large area imaging pixel requires development of thin film transistor switches to be integrated with the photodiodes. For this purpose, we decided to adopt bottom gate a-Si:H TFTs as our pixel TFTs. Our choice of a-Si:H as the channel layer material for pixel TFTs based on several advantages of this material. The

Table 5.1: Tri-layer stack deposition conditions.

Layer	Gases	Flow ($sccm$)	Pressure ($mTorr$)	Power (W)	Temp ($^{\circ}C$)	Time (s)	Thickness (nm)
SiN_x	$SiH_4/N_2/NH_3$	5/50/100	400	2	260	2460	300
a-Si:H	SiH_4/H_2	40/200	900	2	260	500	50
SiN_x	$SiH_4/N_2/NH_3$	5/50/100	400	2	260	1230	150

Table 5.2: Source/drain n+ and third SiN_x deposition conditions.

Layer	Gases	Flow ($sccm$)	Pressure ($mTorr$)	Power (W)	Temp ($^{\circ}C$)	Time (s)	Thickness (nm)
n+ nc-Si:H	$SiH_4/PH_3/H_2$	4/3/400	1500	2	260	600	27
SiN_x	$SiH_4/N_2/NH_3$	5/50/100	400	2	260	1230	150

first advantage is that the low off-current in a-Si:H TFTs (Ref. [73]) results in minimal interference with photodiode operation in the capture phase. The second advantage is the mobility of a-Si:H TFTs ($\mu_n \sim 1\ cm^2/Vs$ [73]), which is sufficient for the readout speed requirements during the pixel operation in the readout phase. The third advantage is the compatibility of a-Si:H TFT fabrication process with that of μc-Si:H photodiode fabrication process we developed. Among the two existing a-Si:H TFT structures (top gate, and bottom gate), bottom gate structure was preferred over the top gate configuration due to its lower threshold voltage and better dielectric-channel interface properties compared to the top gate structure [74]. Figure 3.7 shows the schematic cross section of the bottom gate a-Si:H TFT fabricated for our photodiode pixel circuit.

Fabrication process of our bottom gate a-Si:H TFT is discussed in details in section 3.5. The thickness of Cr gate is 50 nm. The tri-layer SiN_x/a-Si:H/SiN_x stack was deposited using the conditions summarized in Table 5.1. n+ nc-Si:H source/drain contact layer and third nitride SiN_x layer were deposited using the conditions summarized in Table 5.2. The source/drain metal contacts consist of 200 nm thick Al layer capped with 20 nm of Cr

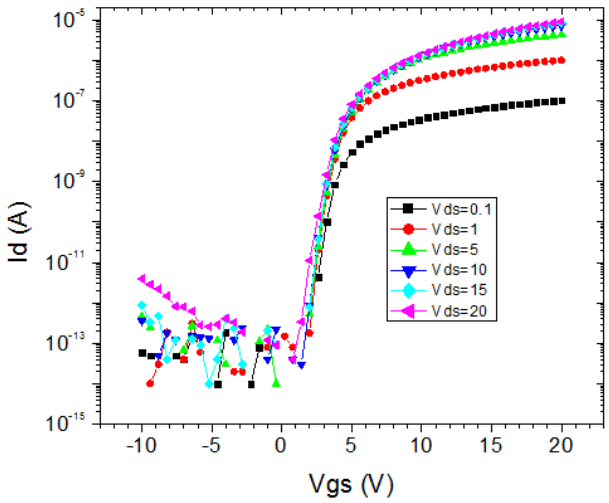


Figure 5.2: I_d-V_{gs} characteristics of our a-Si:H bottom gate TFT with L=40 μm, W=200 μm, and OL=4 μm.

layer.

A series of TFTs with the channel length of $L = 40\ \mu m$ and the channel width of $W = 200\ \mu m$ and $W = 400\ \mu m$ were fabricated using the same set of masks. Each series has three different source/gate and drain/gate overlap lengths of $OL = 4\ \mu m$, $OL = 8\ \mu m$, and $OL = 12\ \mu m$. Figure 5.2 shows the I_d-V_{gs} curves of our TFT at different V_{ds} bias voltages (0.1 V, 1 V, 5 V, 10 V, 15 V, 20 V). The drain-source bias in our pixel TFTs will never exceed 1.3 V (1 V for bias voltage and 0.3 V for open circuit voltage of the photodiode), as a result, low V_{ds} bias voltage is of high importance in our pixel circuit. Figure 5.3 shows I_d-V_{ds} output characteristic of the same TFT at various V_{gs} bias voltages (0 V, 1 V, 5 V, 10 V, 15 V, 20 V).

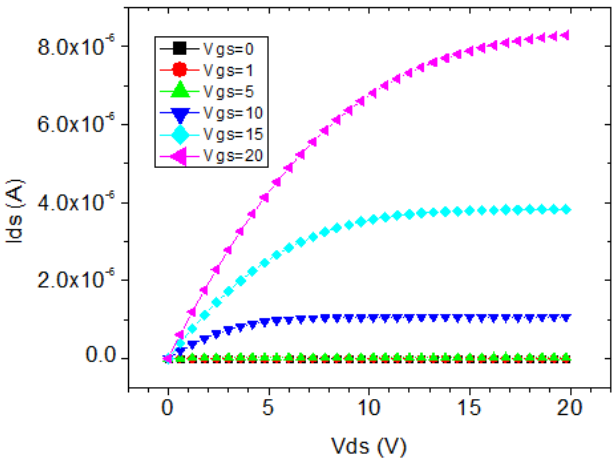


Figure 5.3: I_d-V_{ds} characteristics of our a-Si:H bottom gate TFT with L=40 μm, W=200 μm, and OL=4 μm.

5.2.2 Level 61 TFT Spice Model

In chapter 4, we developed circuit model for our μc-Si:H photodiode. Suitable circuit model for our a-Si:H TFTs is also required in order to be able to simulate and predict the photodiode pixel circuit performance prior to expensive and time consuming fabrication process. Level 61 spice model in HSpice circuit simulator is a universal model for a-Si:H TFTs which is used for modeling our TFTs in this study [75]. The model is fairly complex and consists of 29 parameters, which are all listed in Table 5.3.

These parameters are categorized into seven different groups. The first group contains those parameters that are related to geometrical and technological factors, or other parameters which can be directly measured in the lab. These parameters are (CGSO, CGDO, TOX, EPSI, EPS, TNOM, IOL). The second group contains parameters, which are related to a-Si:H semiconductor properties such as (MUBAND, DEF0, EMU). They can be obtained from semiconductor physics reports in the literature, and in this work, their default

Table 5.3: Level 61 Hspice TFT model parameters.

Group	Parameter	Unit	Description
1	CGDO	F/m	Gate-drain overlap capacitance per meter channel width
	CGSO	F/m	Gate-source overlap capacitance per meter channel width
	TOX	m	Thin dielectric thickness
	EPSI	-	Relative dielectric constant of gate insulator
	EPS	-	Relative dielectric constant of channel layer
	TNOM	C	Parameter measurement temperature
	IOL	A	Zero bias leakage current parameter
2	MUBAND	m2/Vs	Conduction band mobility
	DEF0	eV	Dark fermi level position
	EMU	eV	Field effect mobility activation energy
3	ALPHASAT	-	Saturation modulation parameter
	GAMMA	-	Power law mobility parameter
	VAA	V	Characteristic voltage for field effect mobility
	LAMBDA	1/V	Output conductance parameter
	M	-	Knee shape parameter
	VTO	V	Zero-bias threshold voltage
	RD	Ω	Drain resistance
	RS	Ω	Source resistance
4	GMIN	m-3eV-1	Minimum density of deep states
	V0	V	Characteristic voltage for deep states
	VFB	V	Flat band voltage
5	KASAT	1/X	Temperature coefficient of ALPHASAT
	KVT	V/X	Threshold voltage temperature coefficient
6	EL	eV	Activation energy of the hole leakage current
	SIGMA0	A	Minimum leakage current parameter
	VDSL	V	Hole leakage current drain voltage parameter
	VGSL	V	Hole leakage current gate voltage parameter
7	VMIN	V	Convergence parameter
	DELTA	-	Transition width parameter

values from level 61 model were used. The third group contains parameters that mostly affect the above threshold behavior of the TFT such as (ALPHASAT, GAMMA, VAA, LAMBDA, M, VTO, RD, RS), which can be extracted based on the above threshold characteristics of the TFT in linear and saturation region. The fourth group contains those parameters that define the subthreshold behavior of the TFT such as (GMIN, V0, VFB) that can be estimated based on the subthreshold I-V characteristics of the TFT. The fifth group contains the temperature coefficient parameters. For these parameters, the default values were used as all our measurements were carried out at room temperature and hence the values of these parameters are redundant in our study. The sixth group contains the leakage current parameters. We used default values for these parameters in our study as we were unable to extract them since the leakage current level was below the detection limit of our semiconductor parameter analyzer equipment. However, this does not impact our pixel performance since our pixel TFTs are not going to be biased in negative V_{gs} region. The last group contains two convergence parameters, for which we use the default values from level 61 model.

The first group of parameters are the directly measurable parameters. Figure 5.4 shows the gate-drain capacitance measurements for a TFT with channel length of 40 μm and channel width of 200 μm, and various gate-drain and gate-source overlaps of 4 μm, 8 μm, and 12 μm, respectively. The capacitance is 0.7 pF for the device with overlap of 4 μm, which is the focus of our study in this chapter. As a result, the capacitance per meter of channel width is equal to 3.5×10^{-9} F/m for CGDO and CGSO parameters. Our TFT dielectric thickness (TOX) is measured to be 300 nm using Dektak profilometer. The room temperature parameter TNOM during the device characterization was 25 °C. Relative dielectric constant of our gate dielectric material (silicon nitride) was measured to be 7.1. The relative dielectric constant of our a-Si:H material was 11.4. The zero bias

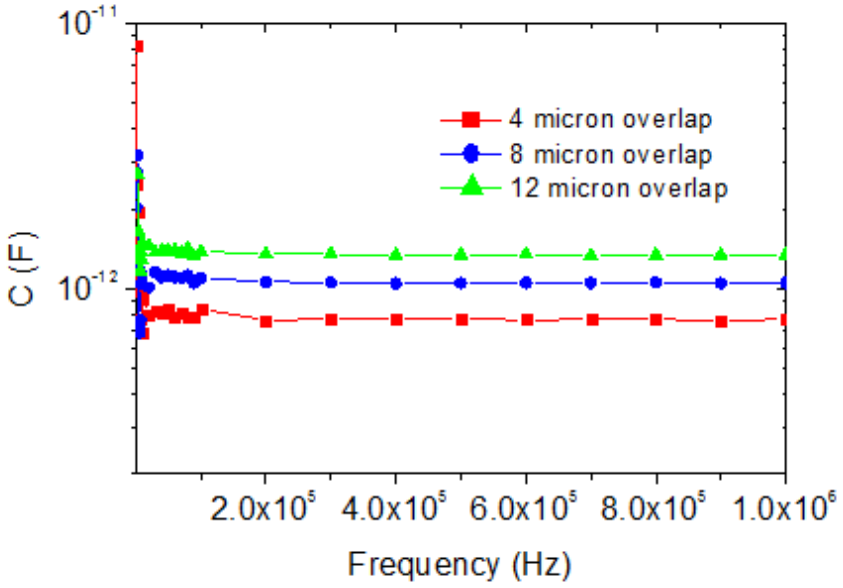


Figure 5.4: Gate-drain capacitance measurement in a TFT with channel length of 40 μm and channel width of 200 μm and gate-drain and gate-source overlap of 4 μm.

leakage current parameter IOL of our TFT was measured to be 2×10^{-14} A. For parameters in group 2, which are related to physical properties of amorphous silicon, the default values from Hspice were used. MUBAND was set to 0.001 $cm^2/V.s$. DEF0 was set to 0.6 eV and EMU was set to 0.06 eV. For parameters in group 5, 6, and 7, the default values from Hspice were used as well.

In order to obtain the above threshold and subthreshold parameters for our TFTs we adopt a procedure known as integral function method [76, 77, 78], which extracts TFT model parameters based on its measured I-V characteristics. Figure 5.5 shows the level 61 Hspice model for a-Si:H TFTs. The drain-source current for level 61 TFT model is defined as:

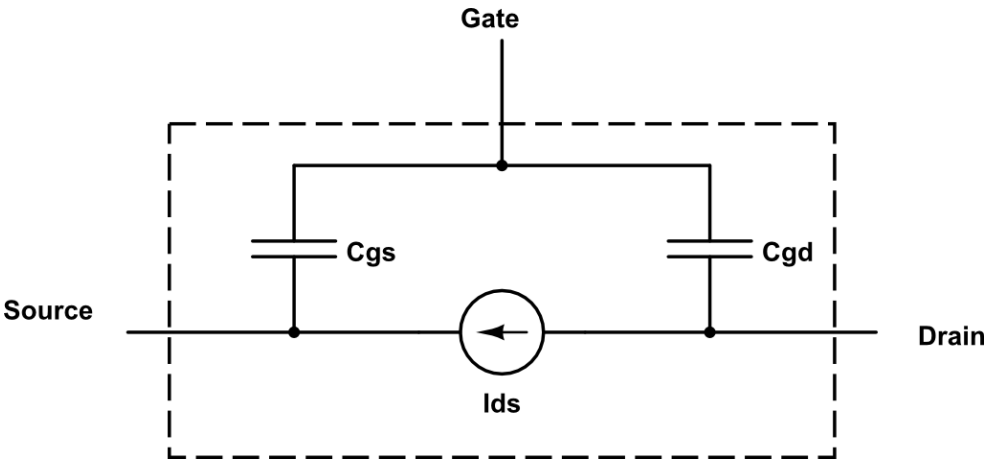


Figure 5.5: Level 61 model of a-Si:H TFT.

$$I_{ds} = I_{leakage} + I_{ab} \tag{5.1}$$

By ignoring the leakage current, which has little contribution in above threshold region, the drain-source current can be approximately described by Equation 5.2:

$$\begin{aligned} I_{ds} \approx I_{ab} &= g_{ch} \frac{V_{ds}}{\left[1 + (V_{ds}/V_{sate})^{M}\right]^{1/M}} (1 + LAMBDA.V_{ds}) \\ V_{sate} &= \alpha_{sat} V_{gte} \\ V_{gte} &= \frac{VMIN}{2} \left[1 + \frac{V_{gs} - V_T}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gs} - V_T}{VMIN} - 1\right)^2}\right] \end{aligned} \tag{5.2}$$

In level 61 TFT model, VMIN is a convergence parameter with default value of 0.3 V. As a result, for $V_{gs} - V_T \gg VMIN$ and $DELTA^2 \ll \left(\frac{V_{gs}-V_T}{VMIN} - 1\right)^2$, V_{gte} can be approximated

as $V_{gte} \approx V_{gs} - V_T$. Thus, I_{ds} in Equation 5.2 can be approximated as follows:

$$\begin{aligned} I_{ds} &\approx g_{ch} \frac{V_{ds}}{\left[1 + (V_{ds}/V_{sate})^M\right]^{1/M}} (1 + LAMBDA.V_{ds}) \\ V_{sate} &= \alpha_{sat} (V_{gs} - V_T) \end{aligned} \tag{5.3}$$

In this model, α_{sat} and V_T are defined as follows:

$$\begin{aligned} \alpha_{sat} &= ALPHASAT + KASAT (TEMP - TNOM) \\ V_T &= VTO + KVT (TEMP - TNOM) \end{aligned} \tag{5.4}$$

Assuming that all measurements are carried out at room temperature, $TEMP = TNOM$, and hence I_{ds} in equation 5.3 can be simplified to:

$$I_{ds} \approx g_{ch} \frac{V_{ds}}{\left[1 + (V_{ds}/ALPHASAT (V_{gs} - VTO))^M\right]^{1/M}} (1 + LAMBDA.V_{ds}) \tag{5.5}$$

The channel conductance value (g_{ch}) used in Equation 5.5 is defined as follows:

$$\begin{aligned} g_{ch} &= \frac{g_{chi}}{1 + g_{chi} (RS + RD)} \\ g_{chi} &= q n_s \frac{W}{L} MUBAND \\ n_s &= \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}} \end{aligned} \tag{5.6}$$

Here n_{sa}, is described by the following equation:

$$n_{sa} = \frac{EPSI.V_{gte}}{q.TOX} \left(\frac{V_{gte}}{V_{aat}}\right)^{GAMMA} \tag{5.7}$$

An approximate equation for n_{sa} can be obtained by using the approximate value for V_{gte}

($V_{gte} \approx V_{gs} - V_T$) and using the following approximation for V_{aat} at room temperature ($TEMP \approx TNOM$) from level 61 model:

$$V_{aat} = VAA.exp\left[\frac{EMU}{q.GAMMA}\left(\frac{q}{k_B TNOM} - \frac{q}{k_B TEMP}\right)\right] \approx VAA \tag{5.8}$$

By replacing the approximate values for V_{gte} and V_{aat} into Equation 5.7, n_{sa} can be approximately estimated by Equation 5.9:

$$n_{sa} \approx \frac{EPSI.(V_{gs} - VTO)}{q.TOX}\left(\frac{V_{gs} - VTO}{VAA}\right)^{GAMMA} = \frac{EPSI}{q.TOX}.\frac{(V_{gs} - VTO)^{1+GAMMA}}{VAA^{GAMMA}} \tag{5.9}$$

On the other hand, in level 61 model, n_{sb} is defined as follows:

$$\begin{aligned} n_{sb} &= n_{s0}\left(\frac{t_m}{TOX}\frac{V_{gfbe}}{V0}\frac{EPSI}{EPS}\right)^{\frac{2V0}{V_e}} \\ n_{s0} &= N_c t_m \frac{V_e}{V0} exp\left(-\frac{DEF0}{V_{th}}\right) \quad , \; N_c = 3 \times 10^{25}\ m^{-3} \end{aligned} \tag{5.10}$$

In the above threshold region, $n_{sb} \gg n_{sa}$. As a result, $n_s \approx n_{sa}$. By replacing n_s with n_{sa} in Equation 5.7, we get the following approximate equation for g_{chi} and g_{ch}:

$$\begin{aligned} g_{chi} &\approx q n_{sa}\frac{W}{L}MUBAND = \frac{EPSI}{TOX} \times \frac{(V_{gs} - VTO)^{1+GAMMA}}{VAA^{GAMMA}}\frac{W}{L}MUBAND \\ g_{ch} &\approx \frac{\frac{EPSI}{TOX} \times \frac{(V_{gs} - VTO)^{1+GAMMA}}{VAA^{GAMMA}}\frac{W}{L}MUBAND}{1 + \left(\frac{EPSI}{TOX} \times \frac{(V_{gs} - VTO)^{1+GAMMA}}{VAA^{GAMMA}}\frac{W}{L}MUBAND\right)(RS + RD)} \end{aligned} \tag{5.11}$$

By inserting the approximate g_{ch} identity from Equation 5.11 back into Equation 5.5, one

can get the following approximate solution for drain current in the above threshold region:

$$I_{ds} \approx \frac{\frac{EPSI}{TOX} \times \frac{(V_{gs}-VTO)^{1+GAMMA}}{VAA^{GAMMA}} \frac{W}{L} MUBAND}{1+\left(\frac{EPSI}{TOX} \times \frac{(V_{gs}-VTO)^{1+GAMMA}}{VAA^{GAMMA}} \frac{W}{L} MUBAND\right)(RS+RD)} \times \frac{V_{ds}}{\left[1+\left(V_{ds}/ALPHASAT\,(V_{gs}-VTO)\right)^{M}\right]^{1/M}} (1+LAMBDA.V_{ds}) \tag{5.12}$$

At very small V_{ds} voltage the above equation for I_{ds} is simplified to:

$$I_{ds} \approx \frac{\frac{EPSI}{TOX} \times \frac{(V_{gs}-VTO)^{1+GAMMA}}{VAA^{GAMMA}} \frac{W}{L} MUBAND}{1+\left(\frac{EPSI}{TOX} \times \frac{(V_{gs}-VTO)^{1+GAMMA}}{VAA^{GAMMA}} \frac{W}{L} MUBAND\right)(RS+RD)} \times V_{ds} \tag{5.13}$$

5.2.3 Above Threshold Region

Equations 5.12 and 5.13 are the closed form approximations for I_{ds} in the above threshold region, which are the basis for the extraction of all the above threshold parameters in level 61 model as categorized in group 3 of Table 5.3.

5.2.3.1 Extraction of GAMMA and VT0

Equation 5.13 can be further simplified by ignoring the effect of series resistance at low V_{gs} values. We know that the series resistance shows its effect at very high V_{gs}, where the channel resistance is not the bottleneck for the current flow and it is the contact series resistance that limits the current flow. Therefore, for small V_{gs} values, Equation 5.13 can be safely approximated by the following equation ignoring the effect of series resistance for

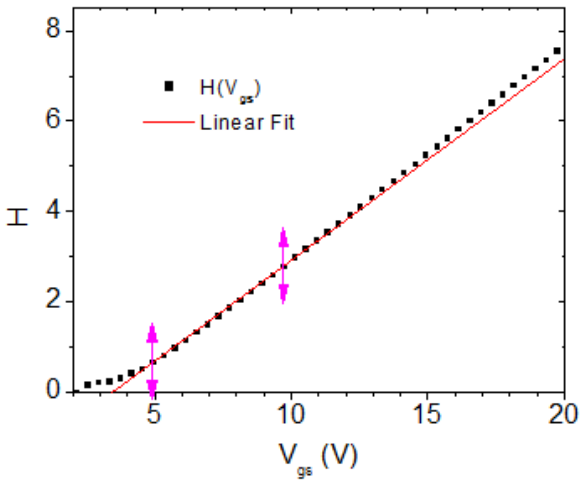


Figure 5.6: Linear fit to H(Vgs) function used for calculation of VT0 and GAMMA.

small V_{gs} values:

$$I_{ds} = \frac{EPSI}{TOX} \times \frac{(V_{gs} - VTO)^{1+GAMMA}}{VAA^{GAMMA}} \frac{W}{L} MUBAND \times V_{ds} \tag{5.14}$$

By integrating I_{ds} with respect to V_{gs} and dividing it by I_{ds}, the expression $H\,(VGS)$ is obtained, which can be used for extraction of $GAMMA$ and $VT0$ parameters:

$$H\,(V_{gs}) = \frac{\int_0^{V_{gs}} I_{ds}(v)dv}{I_{ds}} = \frac{1}{2 + GAMMA}\,(V_{gs} - VTO) \tag{5.15}$$

$VT0$ and $GAMMA$ are estimated from horizontal axis intersection and the slope of linear fit to $H\,(V_{gs})$ function in the above threshold region, respectively, as shown in Figure 5.6. The values extracted for $VT0$ and $GAMMA$ in our TFTs are 3.46 V and 0.23 respectively.

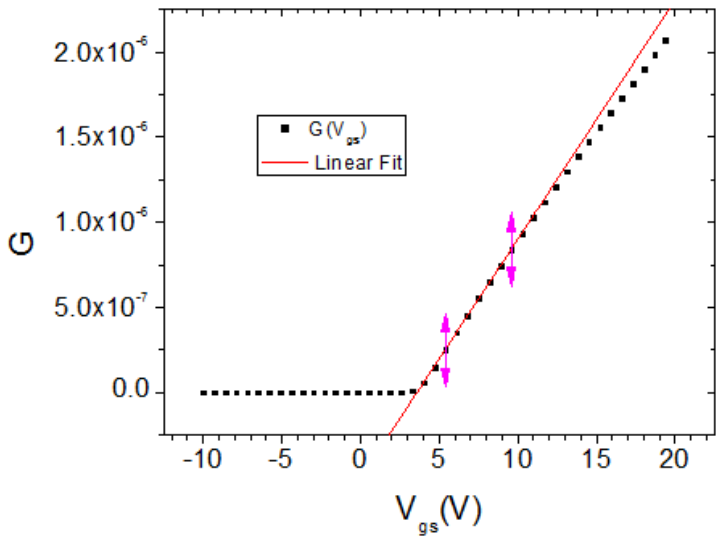


Figure 5.7: Linear fit to G(Vgs) function used for calculation of VAA.

5.2.3.2 Extraction of VAA

After extracting GAMMA, one can find VAA by taking the 1+GAMMA root of I_{ds} in Equation 5.14. The 1+GAMMA root of I_{ds} is named $G(V_{gs})$ and is presented in Equation 5.16. The advantage of $G(V_{gs})$ is that it is a linear function of V_{gs}, whose slope depends on only one unknown parameter, which is VAA. Therefore VAA can be easily extracted from the slope of linear fit to $G(V_{gs})$ using Equation 5.17.

$$G\left(V_{gs}\right) = \sqrt[1+GAMMA]{I_{ab}} = \sqrt[1+GAMMA]{\frac{EPSI}{TOX} \times \frac{\frac{W}{L} MUBAND \times V_{ds}}{VAA^{GAMMA}}} \times \left(V_{gs} - VTO\right) \tag{5.16}$$

$$VAA = \sqrt[GAMMA]{\frac{EPSI}{TOX} \times \frac{\frac{W}{L} MUBAND \times V_{ds}}{slope^{1+GAMMA}}} \tag{5.17}$$

The calculated value for VAA in our TFT is 2.4×10^6 V.

5.2.3.3 Extraction of RS+RD

RS+RD can be calculated from equation 5.13 at the maximum V_{gs} value using the parameters calculated from the previous steps. In our TFT, $RS + RD$ value is equal to 92.6 KΩ. Considering measured I_{ds} value of 8 μA at $V_{gs} = 20\ V$ and $V_{ds} = 20\ V$ one can see that the total channel and contact resistance is 2.5 $M\Omega$. This sets a limit on how much the channel length of the device can be reduced before the contact resistance becomes a bottleneck. In this device the current in TFTs with channel length below 1.5 μm will be limited by contact properties.

5.2.3.4 Extraction of ALPHASAT

In saturation region ($V_{ds} \gg V_{gs} - VT0$) and for small $V_{gs} - VT0$ values, Equation 5.12 can be approximated as follows:

$$I_{ds} \approx \frac{EPSI}{TOX} \times \frac{(V_{gs} - VTO)^{2+GAMMA}}{VAA^{GAMMA}} \frac{W}{L} MUBAND \times ALPHASAT \tag{5.18}$$

The function $U\left(V_{gs}\right) = I_{ds}^{1/2+GAMMA}$ is linear function whose slope depends on ALPHASAT parameter value, hence ALPHASAT can be calculated from the slope using Equation 5.19:

$$ALPHASAT = \frac{S^{2+GAMMA} VAA^{GAMMA}}{\frac{EPSI}{TOX} \times \frac{W}{L} MUBAND} \tag{5.19}$$

ALPHASAT was calculated and had the value of 0.501 in our TFT.

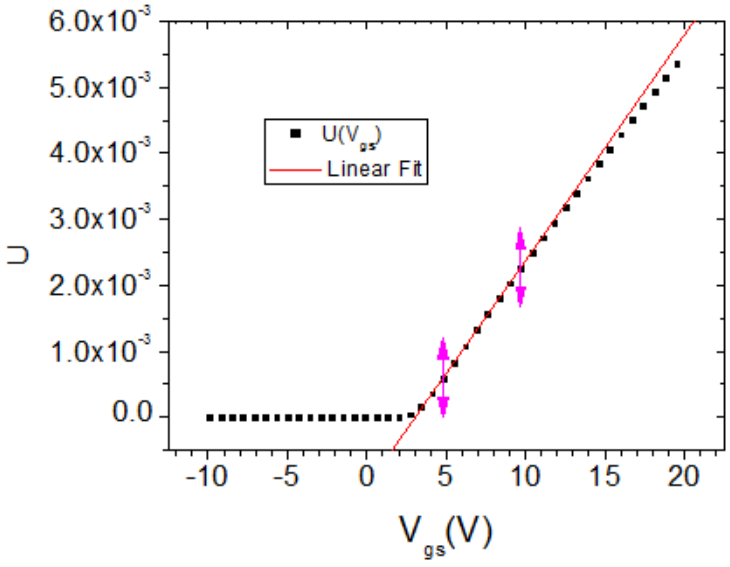


Figure 5.8: Linear fit to U(Vgs) function used for calculation of ALPHASAT.

5.2.3.5 Extraction of M and LAMBDA

These parameters are obtained from output characteristics at V_{gs} value of 10 V and by using Equation 5.12 and replacing V_{ds} by $ALPHASAT\,(V_{gs} - VTO)$, and assuming $LAMBDA.V_{ds}$ value to be small, which results in:

$$I_{ds} \approx \frac{EPSI}{TOX} \times \frac{(V_{gs} - VTO)^{2+GAMMA}}{VAA^{GAMMA}} \frac{W}{L} MUBAND \times \frac{ALPHASAT}{2^{1/M}} \tag{5.20}$$

From the previous equation, M can be calculated as follows:

$$M \approx \frac{log2}{log\left[\frac{EPSI \times (V_{gs} - VTO)^{2+GAMMA} W \times MUBAND \times ALPHASAT}{TOX \times VAA^{GAMMA} \times L \times I_{ds}}\right]} \tag{5.21}$$

In our TFT, the extracted value for M is equal to 1.59. After calculating all above threshold parameters, LAMBDA can be easily obtained from the following equation by using measured current value at maximum V_{ds} bias voltages of 20 V from the $I_d - V_{ds}$ curves at maximum V_{gs} value of 20 V.

$$\begin{aligned} I_{ds} \approx & \frac{\frac{EPSI}{TOX} \times \frac{(V_{gs}-VTO)^{1+GAMMA}}{VAA^{GAMMA}} \frac{W}{L} MUBAND}{1 + \left(\frac{EPSI}{TOX} \times \frac{(V_{gs}-VTO)^{1+GAMMA}}{VAA^{GAMMA}} \frac{W}{L} MUBAND \right) (RS + RD)} \\ & \times \frac{V_{ds}}{\left[1 + \left(V_{ds} / ALPHASAT \left(V_{gs} - VTO \right) \right)^{M} \right]^{1/M}} \left(1 + LAMBDA.V_{ds} \right) \end{aligned} \tag{5.22}$$

The calculated value for LAMBDA for our TFT is 0.0049.

5.2.4 Subthreshold Region

For extraction of subthreshold parameters, different equation for current voltage characteristics is used in level 61 model:

$$\begin{aligned} & I_{ds} \approx K. \left(V_{gs} - VFB \right)^{\left(\frac{2V0}{kT/q} - 1 \right)} \times V_{ds} \\ & K = q \frac{W}{L} MUBAND.N_c. \sqrt{\frac{EPS}{2qGMIN}}. \frac{2kT/q}{2V0 - kT/q} \times \\ & exp \left(- \frac{DEF0}{kT/q} \right). \left(\frac{\sqrt{\frac{EPS}{2qGMIN}}.EPSI}{TOX.V0.EPS} \right)^{\left(\frac{2V0}{kT/q} - 1 \right)} \end{aligned} \tag{5.23}$$

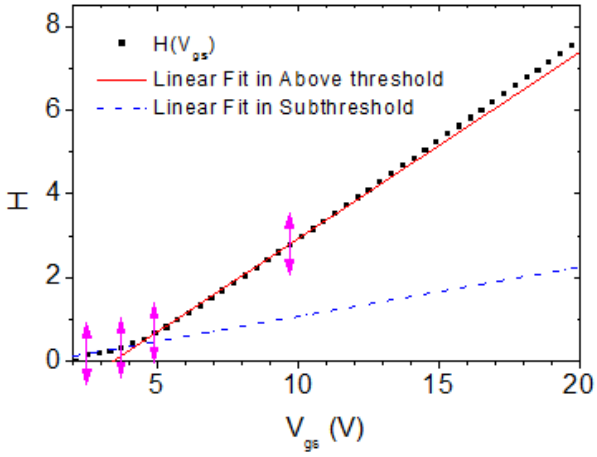


Figure 5.9: Linear fit to H(Vgs) function in subthreshold region used for calculation of V0 and VFB parameters.

5.2.4.1 Extraction of VFB and V0

VFB and V0 can be calculated from the slope and the intersection of linear fit to the function $H\left(V_{gs}\right)$ defined in Equation 5.24 in subthreshold regime:

$$H\left(V_{gs}\right)=\frac{\int_{0}^{V_{gs}} I_{ds}(x)dx}{I_{ds}}=\frac{1}{\frac{2V0}{kT/q}}\times\left(V_{gs}-VFB\right) \tag{5.24}$$

Figure 5.9 shows two linear fits to the function $H\left(V_{gs}\right)$ in above threshold and sub-threshold regions. The slope of linear fit in subthreshold region is used to find V0 using Equation 5.25, where the parameter V0 is caculated to be 0.13 in our TFT.

$$V0=\frac{kT/q}{2\times slope} \tag{5.25}$$

The intersection of linear fit with horizontal axis determines VFB, which is equal to 0.9 V in our TFT.

5.2.4.2 Extraction of GMIN

Finally, after extracting all previous parameters, GMIN can be obtained from the slope of the function $Z\left(V_{gs}\right) = I_b^{\frac{1}{\left(\frac{2V0}{kT/q}-1\right)}}$ as follows:

$$\begin{aligned} Z\left(V_{gs}\right) &= I_b^{\frac{1}{\frac{2V0}{kT/q}-1}} \approx K^{\frac{1}{\frac{2V0}{kT/q}-1}} \times V_{ds}^{\frac{1}{\frac{2V0}{kT/q}-1}} \times \left(V_{gs} - VFB\right) \\ K &= \frac{slope^{\left(\frac{2V0}{kT/q}-1\right)}}{V_{ds}} \end{aligned} \tag{5.26}$$

Figure 5.10 shows the function $Z\left(V_{gs}\right)$ alongside with its linear fit in subthreshold region for our TFT. The slope of the line can be used for calculation of K using Equation 5.27. After calculation of parameter K, GMIN can be calculated from Equation 5.28, which has the value of 9.1×10^{22} in our TFT.

$$\begin{aligned} K = q\frac{W}{L} MUBAND.N_c . \frac{2kT/q}{2V0 - kT/q} . exp\left(-\frac{DEF0}{kT/q}\right) \times \\ . \left(\frac{EPSI}{TOX.V0.EPS}\right)^{\left(\frac{2V0}{kT/q}-1\right)} . \left(\frac{EPS}{2qGMIN}\right)^{\frac{V0}{kT/q}} \end{aligned} \tag{5.27}$$

$$GMIN = \frac{EPS}{2q}\left[\frac{K}{q\frac{W}{L}.MUBAND.N_c.\frac{2kT/q}{2V0-kT/q}.exp\left(-\frac{DEF0}{kT/q}\right).\left(\frac{EPSI}{TOX.V0.EPS}\right)^{\left(\frac{2V0}{kT/q}-1\right)}}\right]^{\frac{-kT/q}{V0}} \tag{5.28}$$

The parameter GMIN is calculated to have the value of 9.1×10^{22} in our TFTs.

Table 5.4 summarizes the values obtained for level 61 model of our TFT with the

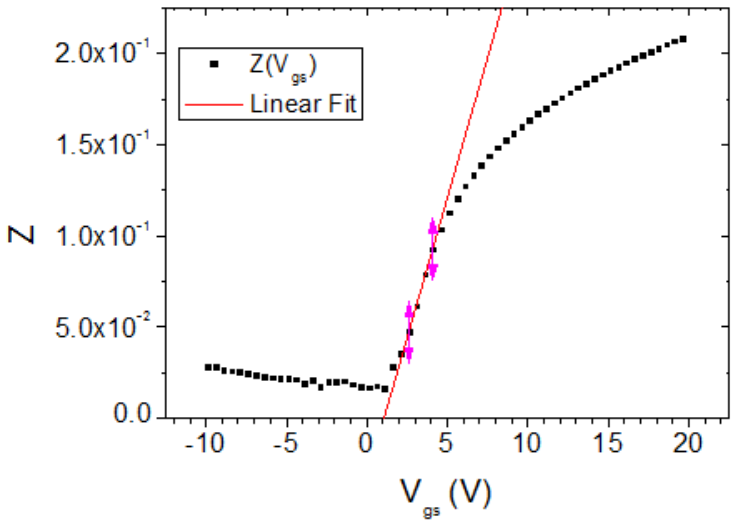


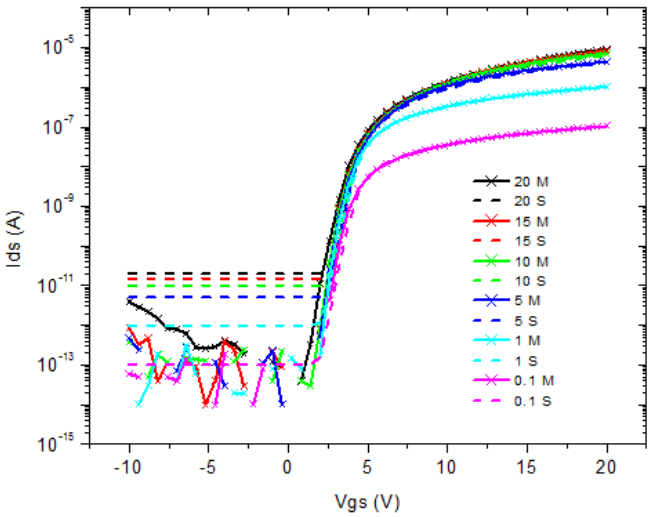
Figure 5.10: Linear fit to Z(Vgs) function in subthreshold regime used for calculation of GMIN.

channel length of 40 μm, the channel width of 200 μm, and the gate-drain and gate-source overlap of 4 μm.

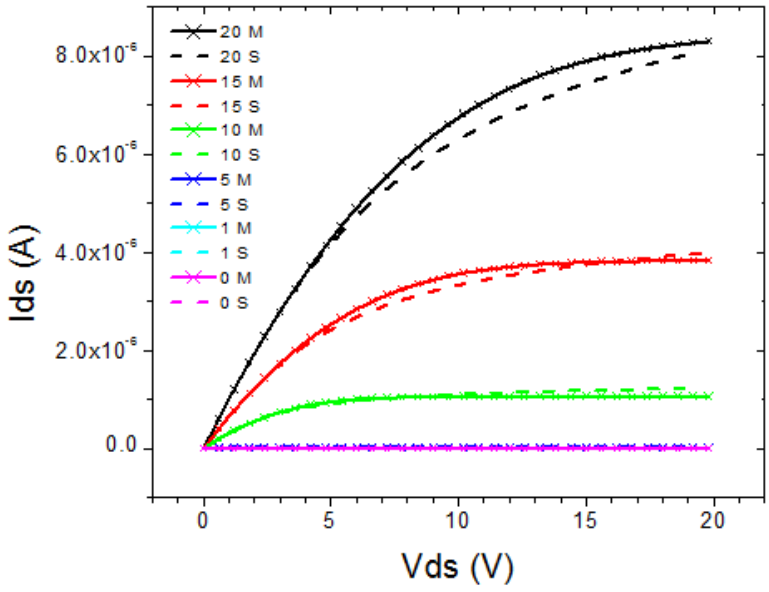
After extracting all the parameters of the TFT using the explained procedure, HSpice simulations were carried out to verify the accuracy of extracted model parameters. Figure 5.11 compares the measurement and HSpice simulation results for the TFT with (L=40 μm, W=200 μm, and OL=4 μm). It can be seen from the curves that level 61 model fits the measurement results in above threshold as well as sub-threshold region on both Id-Vgs and Id-Vds curves in saturation and linear region. As a result, HSpice proves to be a powerful tool for analysis, simulation, design, and prediction of NIR pixel circuit performance as we have accurate models in hand to describe the behavior of our TFTs and photodiodes.

Table 5.4: Level 61 Hspice model parameters values obtained for our TFT with the channel length of 40 μm, the channel width of 200 μm, and the gate-drain and gate-source overlap of 4 μm.

Group	Parameter	Unit	Value
1	CGDO	F/m	3.5×10^{-9}
	CGSO	F/m	3.5×10^{-9}
	TOX	m	300×10^{-9}
	EPSI	-	7.1
	EPS	-	11.4
	TNOM	C	25
	IOL	A	2×10^{-14}
2	MUBAND	m2/Vs	0.001
	DEF0	eV	0.6
	EMU	eV	0.06
3	ALPHASAT	-	0.501
	GAMMA	-	0.23
	VAA	V	2.4×10^{6}
	LAMBDA	1/V	0.0049
	M	-	1.59
	VTO	V	3.46
	RD	Ω	46.3×10^{3}
	RS	Ω	46.3×10^{3}
4	GMIN	m-3eV-1	9.1×10^{22}
	V0	V	0.13
	VFB	V	0.9
5	KASAT	1/X	0.006
	KVT	V/X	-0.036
6	EL	eV	0.35
	SIGMA0	A	1×10^{-14}
	VDSL	V	7
	VGSL	V	7
7	VMIN	V	0.3
	DELTA	-	5



(a) $I_d - V_{gs}$ at $V_{ds} = 0.1\ V, 1\ V, 5\ V, 10\ V, 15\ V, 20\ V$



(b) $I_d - V_{ds}$ at $V_{gs} = 0\ V, 1\ V, 5\ V, 10\ V, 15\ V, 20\ V$

Figure 5.11: Comparison of measurement (denoted by M in the figures) and Hspice level 61 simulation (denoted by S in the figures) results for the transfer characteristic (a) and output characteristics (b) for a TFT with L=40 μm, W=200 μm, and OL=4 μm.

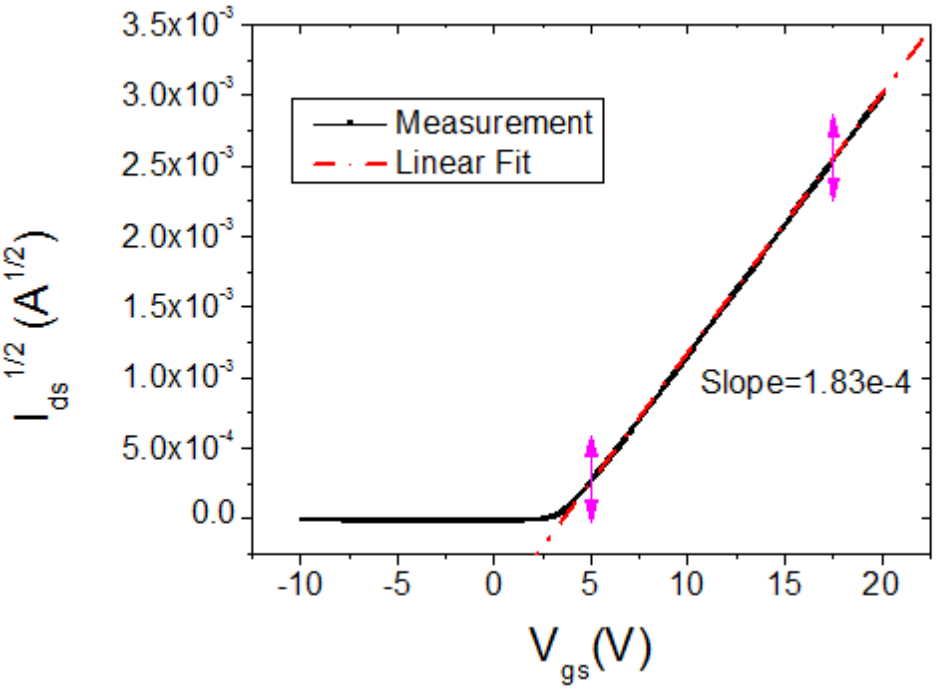


Figure 5.12

5.2.4.3 Extraction of Field-Effect Mobility

Extraction of field effect mobility is often used for evaluation and comparison of the TFT fabrication processes. The method in section 3.3.1 is used for extraction of this parameter based on the slope of $I_{ds}^{1/2} - V_{gs}$ curve in saturation region (shown in Figure 5.12) and using equation 3.16. The value of 0.64 cm^2/Vs is calculated for the field effect mobility of our TFTs which is very close to the value of ≈ 1 cm^2/Vs reported for a-Si:H TFTs [73].

5.3 Pixel Analysis & Simulation

In the previous chapters we discussed the fabrication and characterization of μc-Si:H photodiode and a-Si:H TFT, and obtained circuit models which enable us to simulate and design pixel circuits for 2D imaging array system based on developed technology without the need for costly and time consuming trial and error fabrication experiments in the clean room. In this section, we will discuss different design concepts for NIR pixel circuits. For each pixel circuit, first, we analysed the circuit operation to understand the effect of each design parameter on pixel performance metrics, then we simulated the circuit using our extracted HSpice circuit models for our devices. We finally fabricated each pixel circuit and presented experimental measurement results for that pixel. The schematic circuit model of conventional pixel circuit composed of one photodiode, one TFT, and charge integrating amplifier is shown in Figure 5.13 [79]. Performance figures of merit during reset, capture, wait, and readout phases of the pixel operation are explained as follows.

Reset Phase: In reset phase, the important figure of merit is the amount of time required to discharge the photodiode. Just before the reset phase begins, the TFT is in its off state ($V_{gs} = 0$) and some random amount of charge is stored in C_d depending on the light exposure prior to reset phase. In order to reset the pixel, the TFT is turned on and as a result, the node N_y gets connected to the virtual ground of the amplifier through R_s and R_{on} (on-resistance of the TFT). Therefore, the voltage V_y approaches the steady state voltage of Equation 5.29 with time constant presented in Equation 5.30:

$$V \approx \frac{R_{on} + R_s}{R_{on} + R_s + R_{sh}} \times V_{anode} + I_s \times \left[(R_{on} + R_s) \,||R_{sh}\right] \tag{5.29}$$

$$\tau \approx C_d \times \left[(R_{on} + R_s) \,||R_{sh}\right] \tag{5.30}$$

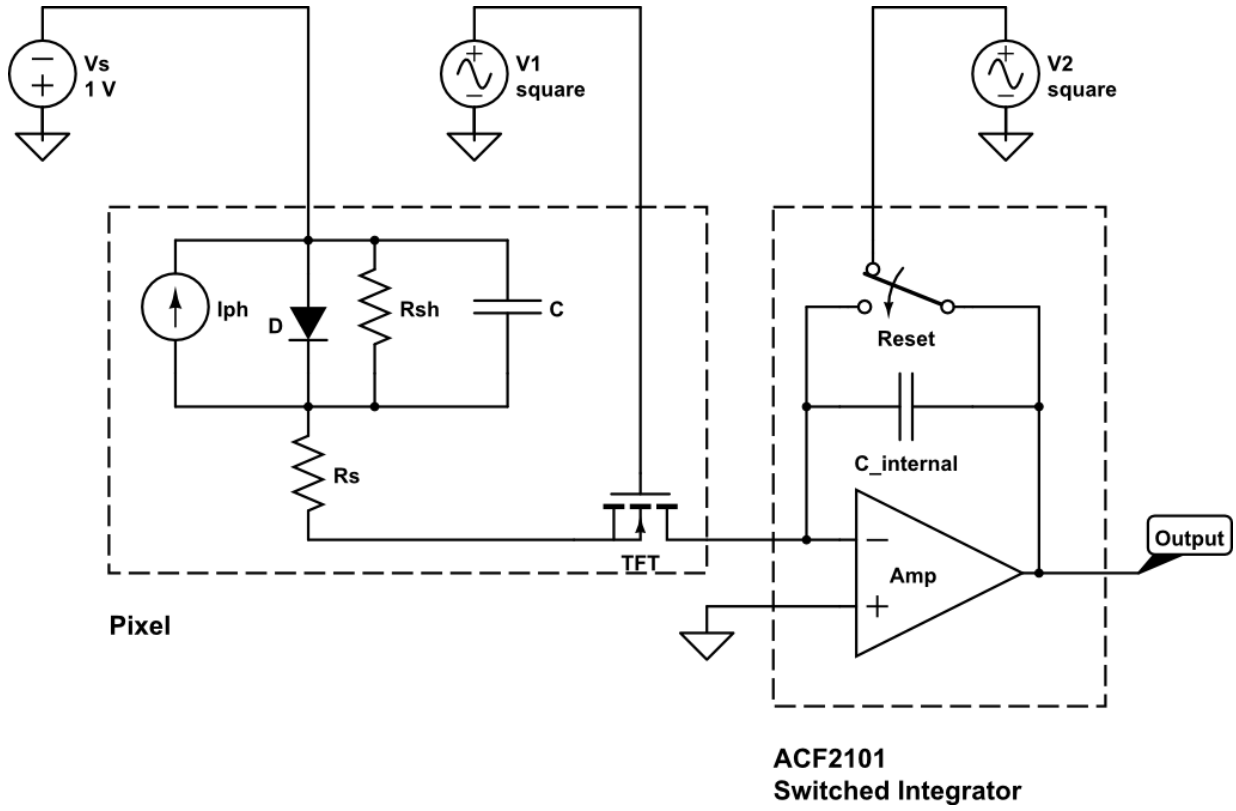


Figure 5.13: Schematic circuit model for a pixel circuit with one TFT and one photodiode connected to a charge integrating amplifier.

Since $R_s \ll R_{on} \ll R_{sh}$, the steady state voltage is very close to zero and the time constant is determined by $\tau \approx C_d \times R_{on}$. As a result the reset time of the pixel is mainly determined by diode capacitance and TFT on resistance both of which need to be reduced as much as possible to minimze the reset time.

Capture Phase: During capture phase all TFTs are turned off and light is exposed on photodiodes. Under exposure the photodiodes generate a photocurrent flowing from cathode to anode which is modeled by a photocurrent source (I_{ph}) demonstrated in Figure 5.13. This current flow tends to reduce the voltage V_y from its steady state value (approximately

zero) reached during the reset phase. The minimum negative voltage that V_y can reach during exposure phase is equal to:

$$V_{y,min} = V_s - V_{oc} \tag{5.31}$$

This means that the voltage on the node Y will be clamped at open circuit voltage value below V_s. When V_y goes below V_s, the diode becomes forward biased, and in forward bias condition, the diode can still maintain the current from the cathode to the anode under light exposure. This will continue until the diode reaches its open circuit voltage condition where $V_y = V_s - V_{oc}$. In practical applications, the light intensity or exposure time must be deliberately chosen according to the following constraint in Equation 5.32 in order to prevent saturation of V_y voltage:

$$I_{ph,max} \times t < |V_s - V_{oc}| \times C_d \tag{5.32}$$

Wait Phase: During the wait phase, both the light source and the TFT are off. As a result, the voltage on node Y will be prone to change due to photo-diode dark current and TFT leakage current. However, considering the subpicoamp leakage current flow in our TFTs compared to the few hundreds of picoamps of dark current in the photodiode, we can safely assume that the voltage on node Y is affected by the photodiode leakage during the wait period. With this assumption, the kirchhoff current law (KCL) equation for node Y during the wait time is as follows:

$$I_s \left(e^{(\frac{V_s - V_y}{nKT/q})} - 1 \right) + \frac{V_s - V_y}{R_{sh}} - C\frac{dV_y}{dt} = 0 \tag{5.33}$$

In reverse bias region, the diode current can be approximated by $-I_s$, and Equation 5.34 can be written as follows:

$$-I_s + \frac{V_s - V_y}{R_{sh}} - C\frac{dV_y}{dt} = 0 \tag{5.34}$$

The solution for V_y from Equation 5.34 is as follows:

$$v_y(t) = (v_y(0) + I_s R_{sh} - V_s)\, e^{-\frac{t}{CR_{sh}}} + (V_s - I_s R_{sh}) \tag{5.35}$$

Considering typical values for C and R_{sh} ($C = 40\ pF$ and $R_{sh} = 1.35\ G\Omega$), one can see that the time scale of wait period is much less than the time constant for node Y during discharge period ($t << CR_{sh}$). As a result, the exponential term in equation 5.36 can be safely approximated with linear term:

$$v_y(t) \approx\ (v_y(0) + I_s R_{sh} - V_s)\,.\left[1 - \frac{t}{CR_{sh}}\right] + (V_s - I_s R_{sh}) \tag{5.36}$$

Readout Phase: During the readout phase, the light source is turned off and the TFT is turned on by applying gate-source voltage greater than its threshold voltage. The gate-source voltage must be high enough to operate the TFT in its linear region ($V_{ds} < V_{gs} - V_{th}$). In other words:

$$V_{ds} + V_{th} < V_{gs} \tag{5.37}$$

Since V_{ds} can reach $|V_s| + V_{oc}$, in order to assure the operation of TFT in its linear region, the following condition must hold:

$$|V_s|\ + V_{oc}\ + V_{th} < V_{gs} \tag{5.38}$$

In linear region, the on-resistance of the TFT can be estimated as follows:

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{gs} - V_{th})} \tag{5.39}$$

As a result, the time constant for the voltage on node Y (V_y) to reach zero during the readout period can be estimated using the following Equation:

$$\tau \approx C_d \times R_{on} = \frac{C_d}{\mu C_{ox} \frac{W}{L} (V_{gs} - V_{th})} \tag{5.40}$$

Consider the following identities for diode capacitance (C_d) and TFT gate capacitance per unit area (C_{ox}),

$$\begin{aligned} C_d &= \epsilon_0 \epsilon_{r_{Diode}} \frac{A_{diode}}{t_{diode}} \\ C_{ox} &= \epsilon_0 \epsilon_{r_{Gate-Dielectric}} \times \frac{1}{t_{TFT-Gate-Dielectric}} \end{aligned} \tag{5.41}$$

In this case, the readout time constant can be described by Equation 5.42:

$$\tau = \frac{\epsilon_{r_{Diode}}}{\epsilon_{r_{Gate-Dielectric}}} \times \frac{A_{diode}}{\mu \frac{W}{L} (V_{gs} - V_{th})} \times \frac{t_{TFT-Gate-Dielectric}}{t_{diode}} \tag{5.42}$$

Equations 5.42 can be used to maximize readout (as well as reset) speed, considering the saturation constraint described by Equation 5.32. The design parameters are the TFT channel width W and length L and the diode area A_{diode}. A_{diode} does not have any impact on the signal amplitude V_y as both the photocurrent and the diode capacitance are proportional to A_{diode}. However, A_{diode} can be reduced to increase the readout speed. In a similar fashion, the TFT parameter $\frac{W}{L}$ can be increased to increase the readout speed. Other parameters such as TFT gate dielectric thickness, gate dielectric permittivity, and field effect mobility as well as the diode thickness and the diode permittivity are not variable

enough to be used as design parameters.

Prior to the fabrication of the passive pixel circuit, Hspice circuit simulation was carried out to predict the behaviour of NIR detector pixel circuit demonstrated in Figure 5.13. The photodiode model parameters used in these simulations were the ones extracted for our photodiode presented in Table 4.5. The TFT model parameters are given in Table 5.3. The PSpice model for external charge integrating amplifier was obtained from Texas Instrument website, and the netlist naming for some elements were modified to comply with HSpice circuit simulator element naming conventions. Figure 5.14 shows the results of HSpice simulation of the photodiode pixel circuit with the area of 1 mm^2 and TFT channel length and width of 200 μm and 40 μm with gate-drain and gate-source overlap of 4 μm illuminated by 850 nm light pulses with intensity of 1 mW/cm^2.

As it is shown in Figure 5.14, the voltage on node Y is initially equal to -1 V in its steady state condition. By application of the first gate pulse for 10 ms (which serves as a reset signal), the voltage on node Y increases to zero with time constant proportional to $(R_{on} \times C_{diode})$. After application of the gate pulse for 10 ms, we have the wait period in which both the gate pulse and the light pulse are absent for 10 ms. As it can be seen in the circuit simulation in Figure 5.14, the voltage on node Y is linearly decreasing over time as predicted in our theoretical analysis in Equation 5.36. In Figure 5.14, right after the wait period, the light is shined on the device for 10 ms (capture phase). The photo-generated current reduces the voltage on node Y linearly over time. Simulations confirm our previous circuit analysis prediction that the voltage on node Y will be saturated at one open circuit voltage below the photodiode anode voltage when the intensity of light is high. After the capture phase, again, we have another wait phase for 10 ms in our simulation. There are two phenomena during this wait phase, which were not predicted in our theoretical analysis. It is seen that if the pixel gets saturated, the voltage on node Y starts to increase

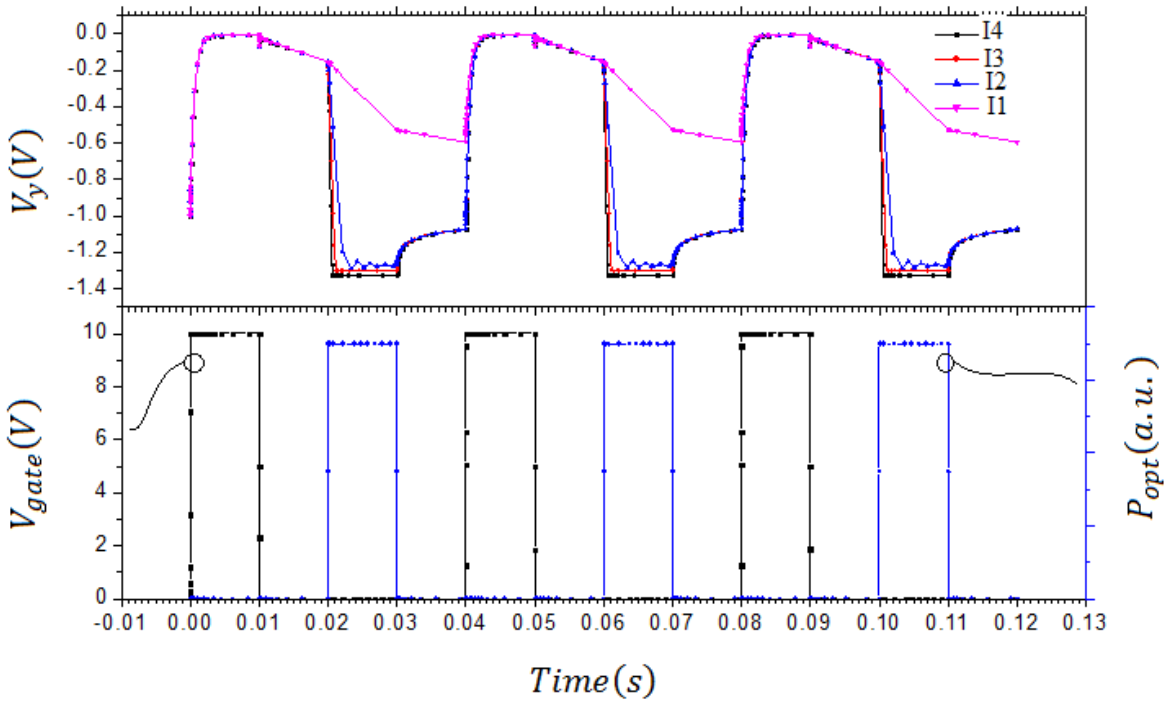


Figure 5.14: Hspice transient simulation for a conventional pixel circuit with a photodiode area of 1 mm^2 and and TFT channel length and width of 200 μm and 40 μm with gate-drain and gate-source overlap of 4 μm under variable light densities: $I_1 = 5\ \mu W/cm^2$, $I_2 = 50\ \mu W/cm^2$, $I_3 = 150\ \mu W/cm^2$, and $I_4 = 500\ \mu W/cm^2$.

during the wait phase. This is due to the fact that the photodiode is under forward bias and as soon as the light pulse is turned off, the current flows from the anode to the cathode, which starts to increase the voltage on node Y until the photodiode reaches its short circuit condition where the voltages on the anode and the cathode become equal. That is why we see exponential nonlinear voltage increase for node Y in the saturated waveforms in Figure 5.14 (Waveforms 2, 3, and 4). At the end of the wait phase, the gate pulse is applied for another 10 ms to readout the signal. Similar to what we had during the reset phase, the voltage on node Y starts to increase to zero during the reset phase with time constant in

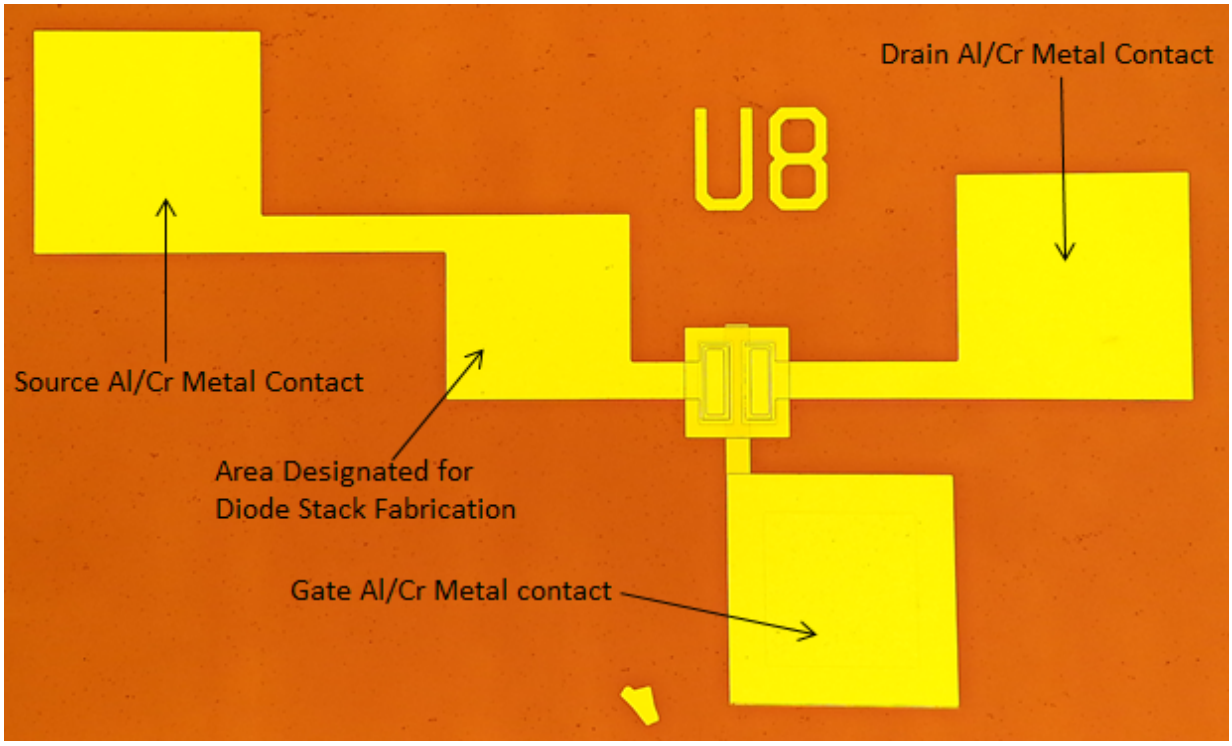


Figure 5.15: Top view micrograph of pixel circuit after TFT fabrication.

the order of 1 ms for the pixel specifications in Figure 5.14.

5.4 Pixel Fabrication

The fabrication process begins with fabrication of the bottom gate TFT. he fabrication steps are exactly the same as those discussed in chapter 3 for the bottom gate TFT. The only difference is the designation of an area for the photodiode next to TFT source contact as shown in Figure 5.15. After TFT fabrication as shown in Figure 5.15, the bottom AZO electrode of the photodiode was sputtered all over the wafer and etched to form textured back reflector structure. The nip stack was then deposited all over the wafer followed by

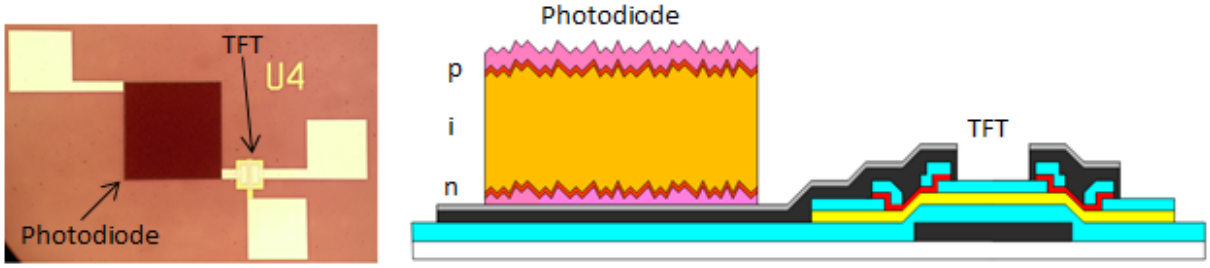


Figure 5.16: Top view and schematic cross section of the conventional pixel circuit after using mask 6.

deposition of top AZO. The 6^{th} mask was used to pattern the photodiode region. After that, the device was placed into RIE system to etch microcrystalline silicon nip stack using SF_6 gas. The bottom AZO layer plays very significant role during SF_6 RIE step. As a matter of fact, bottom AZO layer is acting as protection barrier that prevents TFT from unintentional damages in SF_6 RIE process since AZO does not get etched in SF_6 RIE. Finally, when RIE is done (without removing the photoresist), the sample was placed in HCL solution to etch the AZO layer over unwanted areas. As we are going to etch the back reflector AZO layer in the regions outside photodiode island, HCL solution can damage Al contacts in those regions and the Cr capping layer prevents these damages as Cr is very resistive to HCL solution unlike Al. It is notable to mention that the surfaces exposed to HCL solution at this step are either SiN_x or Cr, non of which react with HCL.

5.5 Pixel Characterization

Figure 5.17 shows schematic representation of the measurement setup for the passive pixel circuit. AVR microcontroller is used to generate the pulses for NIR LED light source and

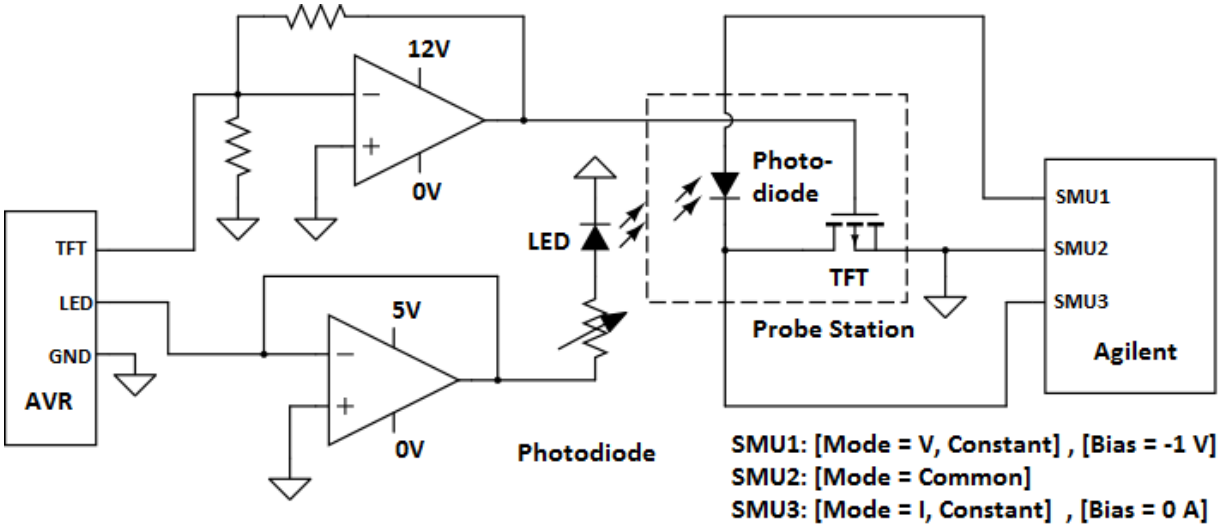


Figure 5.17: Schematic representation of transient measurement setup for conventional pixel circuit.

for TFT gate voltage. Proper operational amplifiers (OP-AMPs) are used to amplify the output voltage of AVR microcontroller to generate the pulses with amplitude of 10V for the TFT and the pulses with adjustable amplitude for LED source. LED amplifier is a high output current amplifier which can provide current up to 1 A to the LED. Figure 5.18 shows transient current measurements for the pixel comprising of the photodiode with the area of 1 mm^2, and of TFT with W=200 μm and L= μm and OV=4 μm. Figure 5.18 shows that by increasing NIR light intensity, generated voltage signal increases until the voltage of node Y saturates at approximately 1.3 V, which is the sum of the anode bias voltage and the open circuit voltage of the photodiode. It can be seen in the figure that the behaviour of the pixel circuit does not depend on the input light intensity during the reset, wait, and readout phases, and that they are identical for all of our four different light intensity experiments. Figure 5.19 shows the effect of the photodiode area on the transient response. Transient responses for three pixels with TFTs of the same size (W=200 μm,

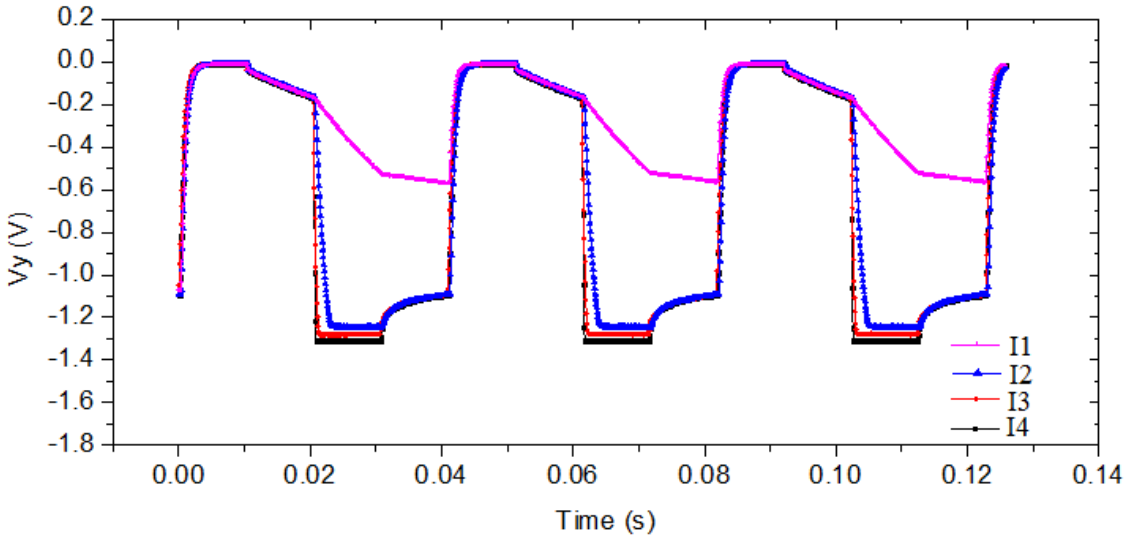


Figure 5.18: Transient measurements for conventional pixel circuit with photodiode with area of 1 mm^2 and TFT with channel length and width of 200 μm and 40 μm, and gate-drain and gate-source overlap of 4 μm under variable light densities: $I_1 = 5\ \mu W/cm^2$, $I_2 = 50\ \mu W/cm^2$, $I_3 = 150\ \mu W/cm^2$, and $I_4 = 500\ \mu W/cm^2$.

L=40 μm) and photodiodes with variable areas of 1 mm^2, 0.25 mm^2 and 0.01 mm^2 are shown in Figure 5.19. The measurements show that reducing photodiode area results in faster reset and readout time due to reduced capacitance. However, the voltage drop on V_y at rise time and fall time of gate pulse is more pronounced for smaller diode areas.

As a result, there is a trade off between the amount of increase in readout speed and unwanted voltage drop during TFT gate pulse transients. We initially had two different assumptions for voltage drop observed during gate voltage transients. The first culprit is the capacitive coupling between the gate and the photodiode cathode due to the presence of gate-source capacitance. The second possibility is the charge injection from (to) source and drain contacts when TFT is turned on (off). In order to find out which phenomenom was dominant, we designed pixels with the same TFT and photodiode size but with differ-

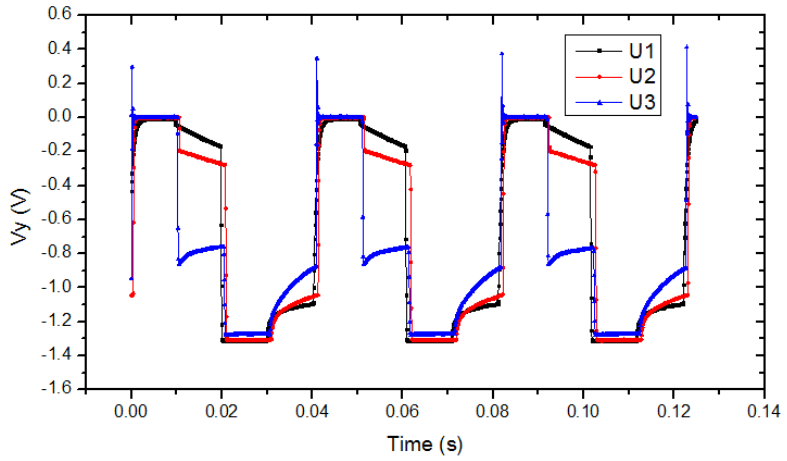


Figure 5.19: Transient measurement results for a pixel with TFT with L=40 μm and W=200 μm and OV=4 μm for various photodiode areas of 1 mm^2 (U1), 0.25 mm^2 (U2), and 0.01 mm^2 (U3) under incident power density of 500 $\mu W/cm^2$.

ent gate-source and gate-drain overlap, which results in different gate-source (gate-drain) capacitance values. Figure 5.20 shows the timing measurement results for the pixel with photodiode area of 1 mm^2 and TFT with W=400 μm and L=40 μm with three different gate-source (gate-drain) overlaps of OV=4 μm, OV=8 μm, and OV=12 μm. As it can be seen in Figure 5.20, the transient voltage on node Y is identical for all three pixels, which shows that the gate-source capacitive coupling is not the dominant factor when it comes to the voltage drop at node Y. In order to verify whether it is TFT charge injection effect which causes the voltage drop, we designed two identical pixels with the same diode area of 1 mm^2 and TFT channel length of L=40 μm and overlap length of OV=4 μm but with different TFT width of W=200 μm and W=400 μm. It is seen that the wider TFT shows higher voltage drop as a result of higher charge accumulation (depletion) in the channel during turn on (turn off) transients.

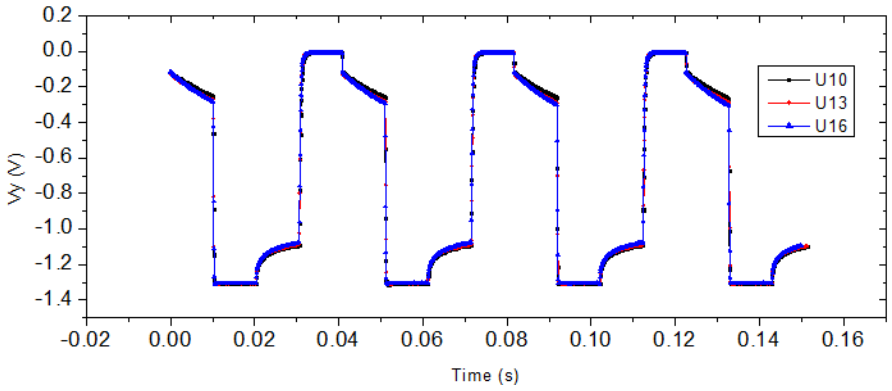


Figure 5.20: Transient measurement results for a pixel with a photodiode area of 1 mm^2 and TFTs with L=40 μm and W=400 μm but different overlap lengths of OV=4 μm (U10), OV=8 μm (U13), and OV=12 μm (U16) under incident power density of 500 $\mu W/cm^2$.

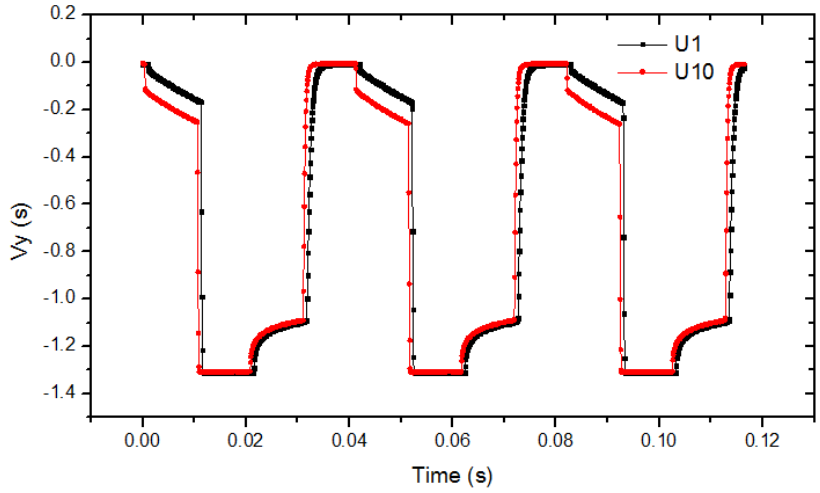


Figure 5.21: Transient measurement results for a pixel with similar photodiode areas of 1 mm^2 and TFTs with L=40 μm and OV=4 μm but different widths of W=200 μm (U1), and W=400 μm (U10) under incident power density of 500 $\mu W/cm^2$.

5.6 Integrated Capacitance for Charge Storage Enhancement

In the previous section, we presented the characteristics of a conventional pixel circuit comprised of one photodiode and one TFT. We observed three problems with the operation of conventional pixel circuit: (1) Saturation of stored charge in the pixel; (2) Voltage drop during gate switching transients; (3) Voltage change during wait period. We already demonstrated that the voltage drop problem can be mitigated by reducing size of TFT to minimize the charge injection effect. However, measures must be taken to resolve the remaining problems with pixel saturation and signal change during wait period. In order to resolve the saturation problem, one must increase the stored charge capacity in the pixel by either increasing the bias voltage to push the clamp voltage further down, or by increasing the pixel capacitance to store more charge prior to saturation. Changing the bias voltage turns out to be disadvantageous as the minimum sensitivity of the detector would be affected by increasing reverse bias due to dark current increase. Therefore, in order to increase the stored charge capacity, one has to increase the pixel capacitance. Figure 5.23 shows a possible solution to increase the pixel capacitance [80]. This pixel circuit can be fabricated without any additional cost compared to the conventional pixel circuit in terms of the area or the number of required photo masks, or the number of fabrication steps. Here, the capacitor C_y can be placed underneath the photodiode as shown in Figure 5.23. The bottom electrode of the capacitor C_y can be fabricated during the fabrication of TFT bottom gate contact. The first SiN_x gate dielectric layer can act as the capacitor dielectric, and the rest of fabrication steps for this pixel are exactly similar to the ones of the conventional pixel. Figure 5.24 shows the schematic of the measurement setup

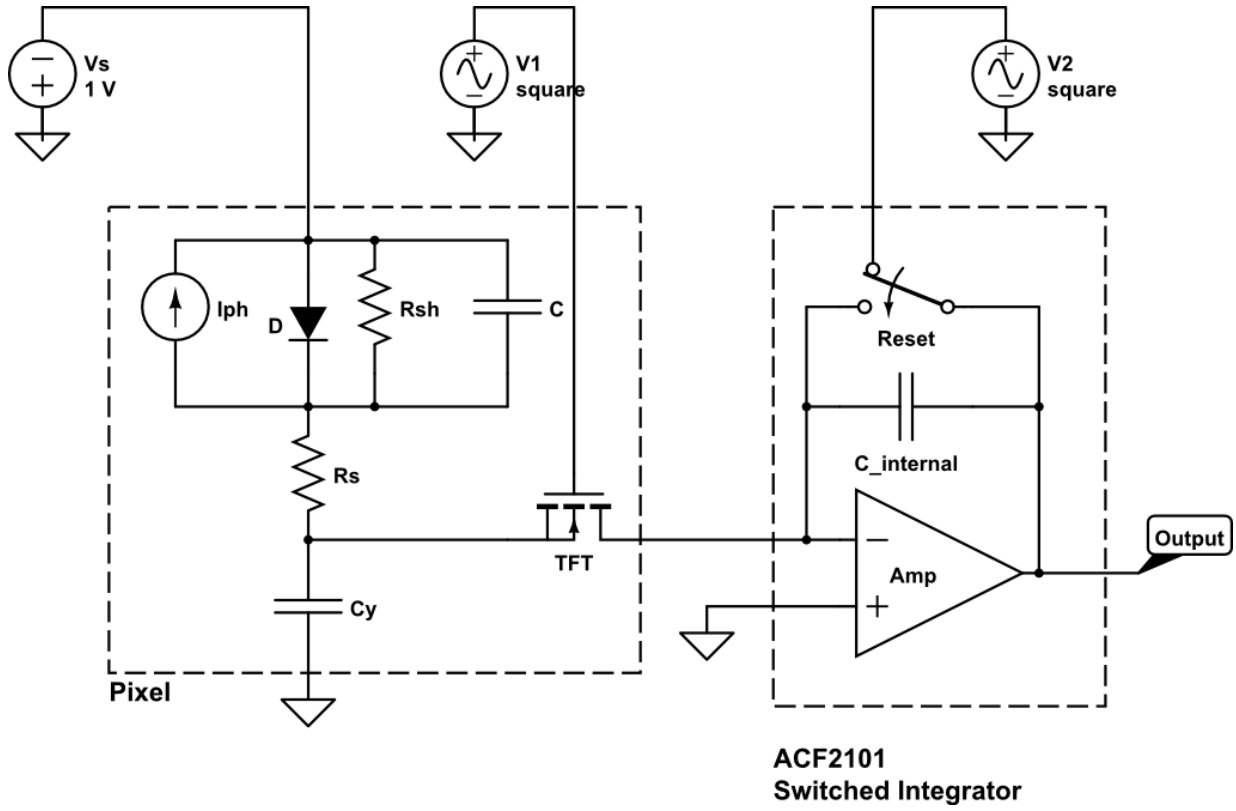


Figure 5.22: Schematic circuit model for a pixel circuit with one TFT and one photodiode and an integrated capacitance for enhanced charge storage capacity.

used for measurement of the pixel with integrated capacitance. Figure 5.25 compares the transient response for the pixel with integrated capacitor to the conventional pixel circuit without integrated capacitor. The photodiode area is 1 mm^2 and TFT dimensions are W=400 μm, L=40 μm, and OV=4 μm for both cases. Here, transient voltage V_y(t) shows two important changes. First, the slope of $V_y(t)$ during exposure time is decreased due to increased capacitance. This results in lower voltage being created at node Y for the pixel with integrated capacitance. This means that longer exposure time or more intense light would be required to saturate the pixel with integrated capacitance. The second

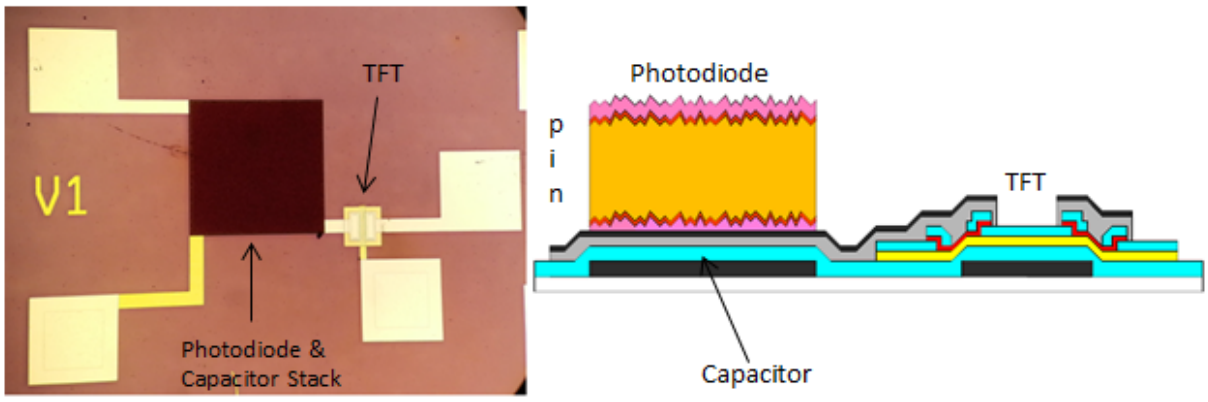


Figure 5.23: Top view and schematic cross section of the pixel circuit with integrated capacitance.

important difference is the reset (readout) time of the pixel. The response time increases linearly with the capacitance making the pixel with integrated capacitance slower than conventional pixel.

The operation of pixel circuit with integrated capacitor is very similar to that of the conventional pixel circuit discussed earlier, which is explained as follows:

Reset Phase: During the reset phase, the voltage on node Y approaches the steady state voltage given by Equation 5.43 with time constant given by Equation 5.44. It should be noted that the readout time constant for this circuit is higher due to increased capacitance connected to node Y.

$$V \approx \frac{R_{on}}{R_{on}+R_s+R_{sh}} \times V_{anode} + I_s \times \left(\frac{R_{on}}{R_{on}+R_s}\right)[(R_{on}+R_s)\,||R_{sh}] \tag{5.43}$$

$$\tau \approx (C_d + C_y) \times [(R_{on}+R_s)\,||R_{sh}] \tag{5.44}$$

Capture Phase: During the capture phase, the light is incident on the photodiode while

TFT is off. As a result, the voltage on node Y linearly decreases from its steady state value reached at the end of reset phase. Time dependence of the voltage drop in the capture mode is determined by Equation 5.45. The voltage gets clamped at one open circuit voltage of the photodiode below the bias voltage (V_s-V_{oc}). However, compared to the conventional pixel circuit, this pixel can store more charge prior to saturation:

$$\Delta V = \frac{I_{ph}}{C_d + C_y} \times \Delta t \tag{5.45}$$

Readout Phase: During the readout phase, TFT is turned on while the photodiode is still off. Stored charge discharges through the TFT and is stored in the internal capacitance of the charge integrating amplifier. The readout time constant is therefore determined by RC time constant described by Equation 5.46.

$$\tau = (C_d + C_y) \times R_{on} = \frac{C_d + C_y}{\mu C_{ox} \frac{W}{L} (V_{gs} - V_{th})} \tag{5.46}$$

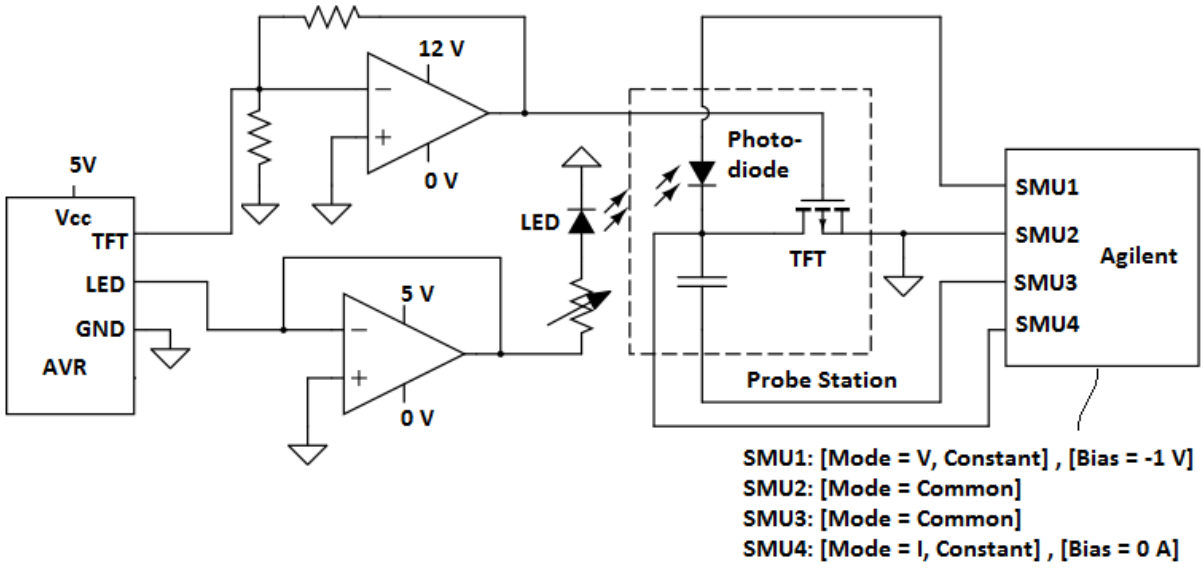


Figure 5.24: Schematic representation of transient measurement setup for pixel circuit with integrated capacitance.

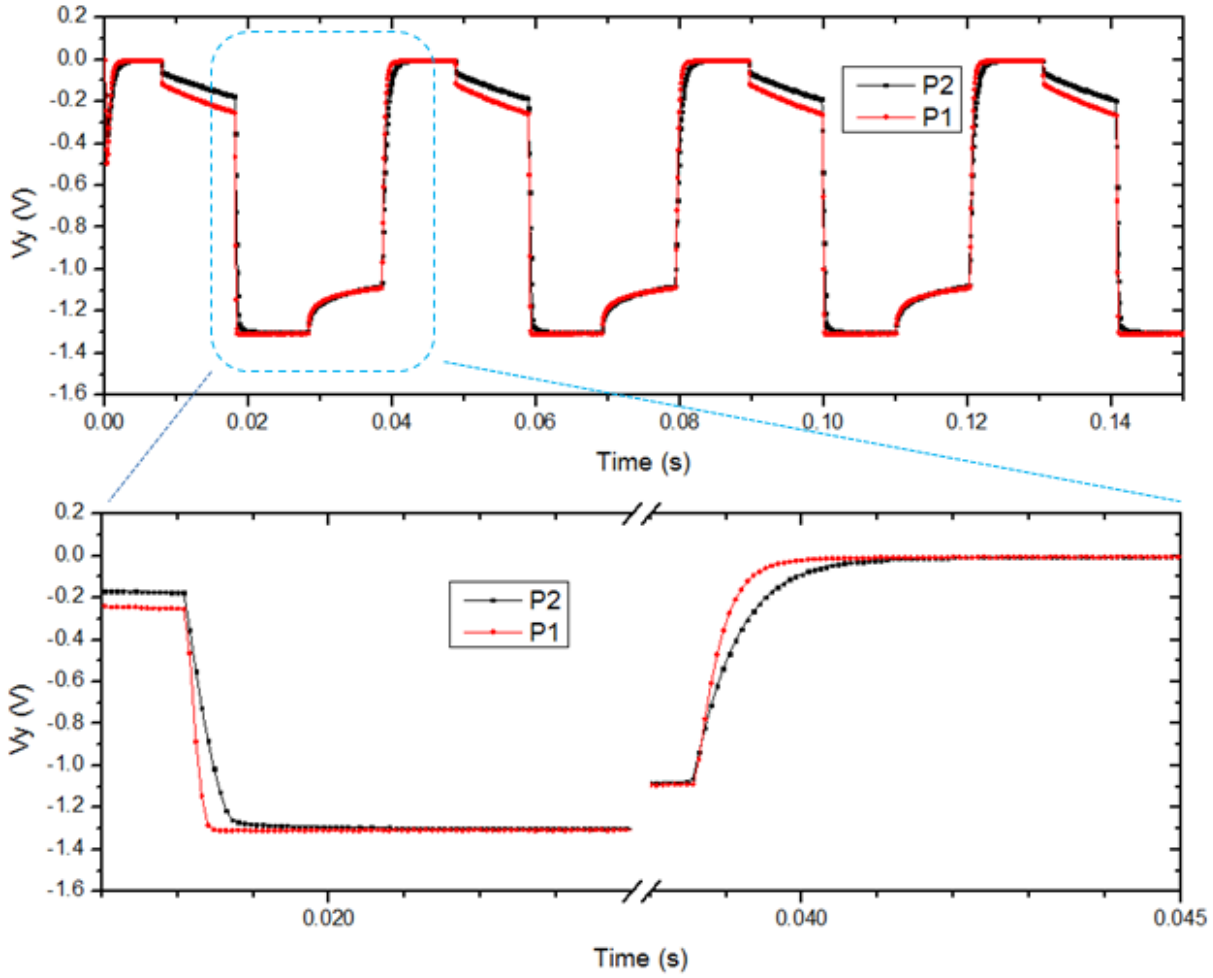


Figure 5.25: Comparison of transient measurement results for conventional pixel and pixel with integrated capacitance. Both pixels have a photodiode area of 1 mm^2 and TFTs with $W = 200\ \mu m$, $L = 40\ \mu m$, and $OV = 4\ \mu m$. For the pixel with integrated capacitance the capacitor dimensions is exactly the same as the photodiode dimensions with area of 1 mm^2. The incident power density during on-time of the light pulse is 500 $\mu W/cm^2$.

5.7 Dual TFT Pixel for Voltage Drift Elimination During Wait Period

One of the major drawbacks of the two pixel circuits discussed earlier in Section 5.3 and 5.6 is the stored charge change in the pixel during the wait time due to photodiode dark current. This problem is very critical since the pixels of different rows in a 2D imager have different wait times. As an example, it is shown in Figure 5.18 that for conventional pixel the voltage drift rate is 6.7 mV/ms, which is significant compared to the maximum bias voltage of 1 V in our pixels. In order to prevent the stored charge from being affected by the photodiode dark current during the wait time, we came up with the idea of the pixel circuit shown in Figure 5.26, where an a-Si:H TFT is inserted between the photodiode cathode and the charge storage node. The advantage of this new pixel design is that it does not require more masks compared to previous two pixels, and yet it can eliminate the signal drift during the wait period. Figure 5.27 shows the schematic cross section and top view micrograph of fabricated dual TFT pixel. Fabrication process begins with fabrication of the two bottom gate TFTs using the first five photomasks as discussed earlier in Chapter 3. The charge storage capacitor is also fabricated in parallel with TFTs by using the TFT gate dielectric as capacitor dielectric. Then the photodiode stack is deposited and the sixth mask is used to pattern the photodiodes on designated areas (drain of TFT1). The operation of the pixel circuit is as follows,

Reset Phase: During the reset phase, TFT2 is turned on while TFT1 is off, and there is no light incident on the photodiode. As a result, the capacitor C_y is discharged through TFT2, and the voltage on node Y (V_y) approaches zero.

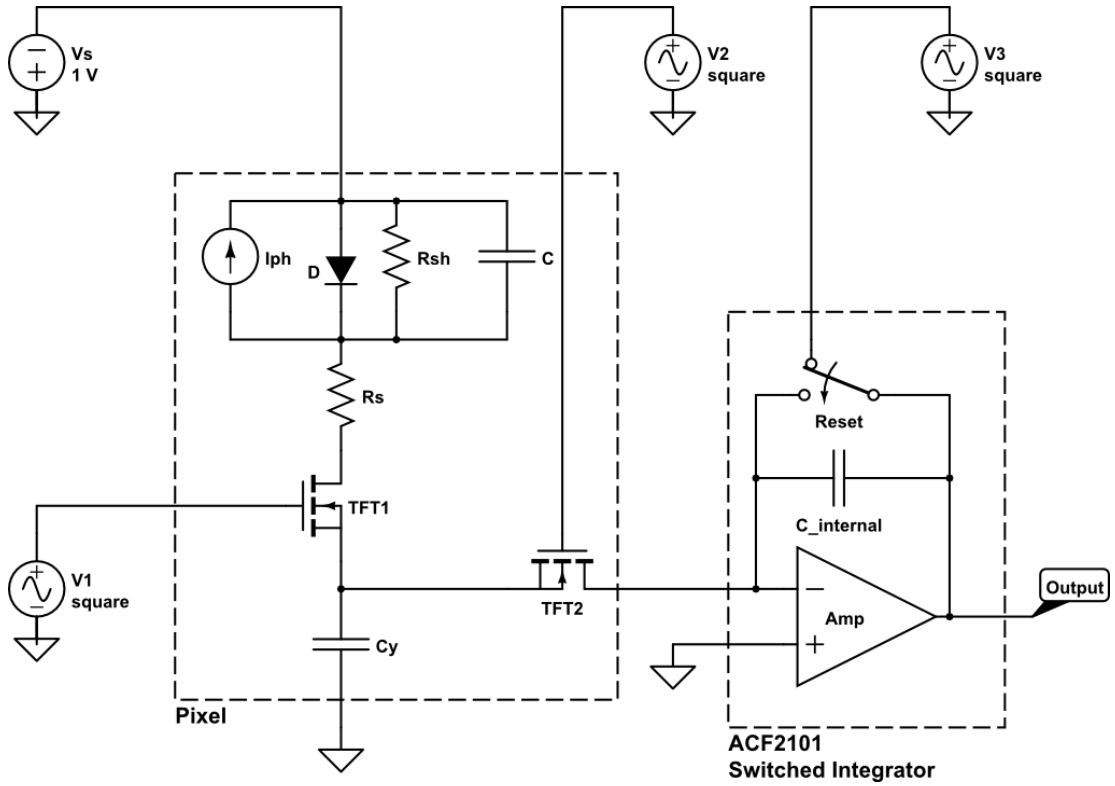


Figure 5.26: Schematic circuit model for a dual TFT pixel circuit designed to eliminate photodiode dark current induced signal offset during wait time.

Capture Phase: During the capture phase, TFT2 is turned off and TFT1 and the light source are turned on simultaneously. In this mode, the on-resistance of TFT1 is in series with the photodiode. As long as the photodiode remains under reverse bias, constant photo current flows from the charge storage capacitor, which reduces the voltage at C_y linearly over time.

Wait Phase: At the end of capture phase, both TFT1 and the light source are turned off. Right after this point, the pixels experience wait period until their charge is read out to the external charge integrating amplifier. The wait time for the first row is zero, and for

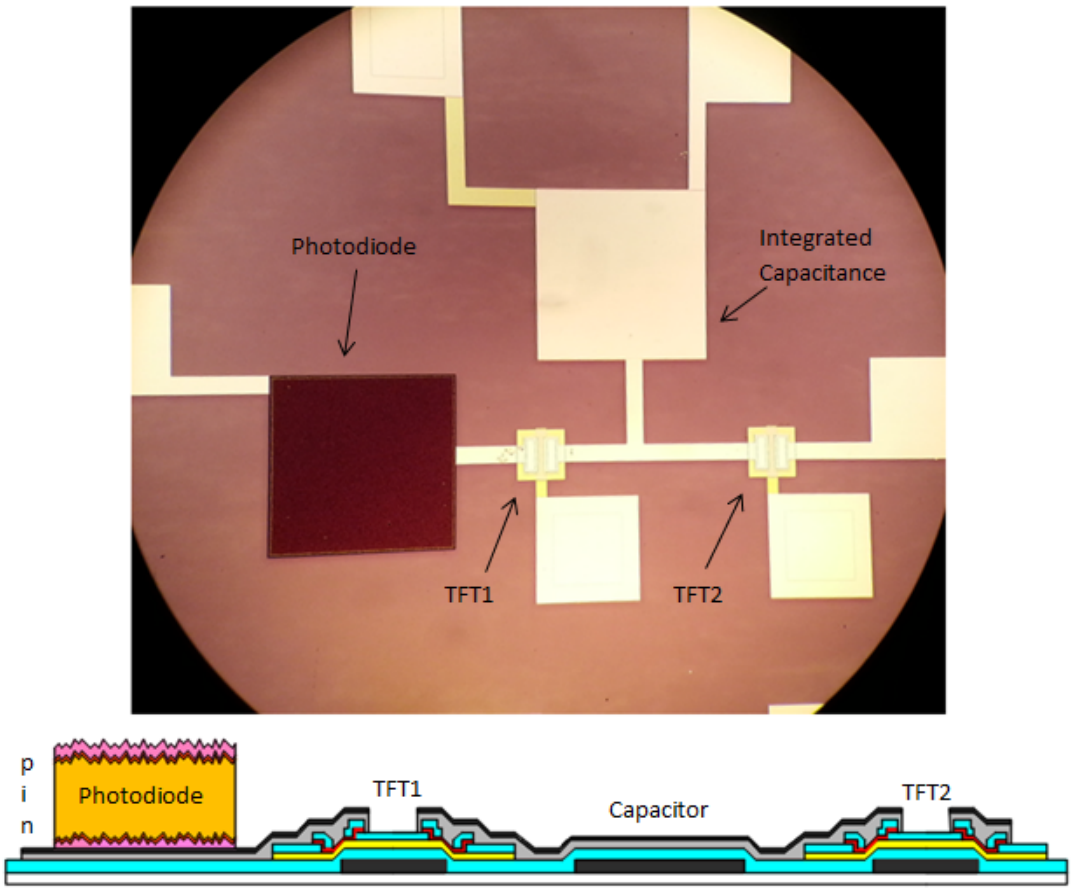


Figure 5.27: Top view micrograph and schematic cross section of the dual TFT pixel circuit.

the Nth row, it is (N-1)×$t_{readout}$. The novelty of this circuit is that the maximum current through the photodiode is limited by TFT1, which is in its off state acting as very high resistance in series with the photodiode.

Readout Phase: At the beginning of the readout phase, TFT2 is turned on by a gate pulse, and the charge stored in C_y is discharged through the TFT2 to the external charge amplifier. Once again, the readout time is determined by RC time constant composed of

TFT on-resistance and capacitance C_y.

Figure 5.28 shows the transient measurements for the pixel consisting of two TFTs with dimensions of (W=40 μm, L=200 μm, OV=4 μm), the photodiode with the area of 500×500 μm^2, and the capacitor with the area of 1 mm^2. As predicted earlier, the drift of the voltage V_y due to photodiode dark current is limited by TFT1. The voltage drift during the wait time for this dual TFT pixel is near zero whereas the voltage drift for conventional pixel was 6.7 mV/ms.

As seen in Figure 5.28 the dual pixel TFT still suffers from voltage jumps during TFT gate pulse rise time and fall time due to charge injection from TFTs. As stated before this problem can be resolved by TFT scaling. Figure 5.29 compares the HSpice simulation results for dual TFT pixels for a pixel with TFT size of ($L = 40$ μm, $W = 200$ μm) and a pixel with scaled TFTs with dimensions of ($L = 4$ μm, $W = 20$ μm). The simulation results show that the dual TFT pixel with small TFTs is immune to signal jump during gate pulse transients, signal drift during wait time and saturation. As a result dual TFT pixel with scaled TFTs can be used for realization of two dimensional microcrystalline silicon photodiode NIR detector arrays.

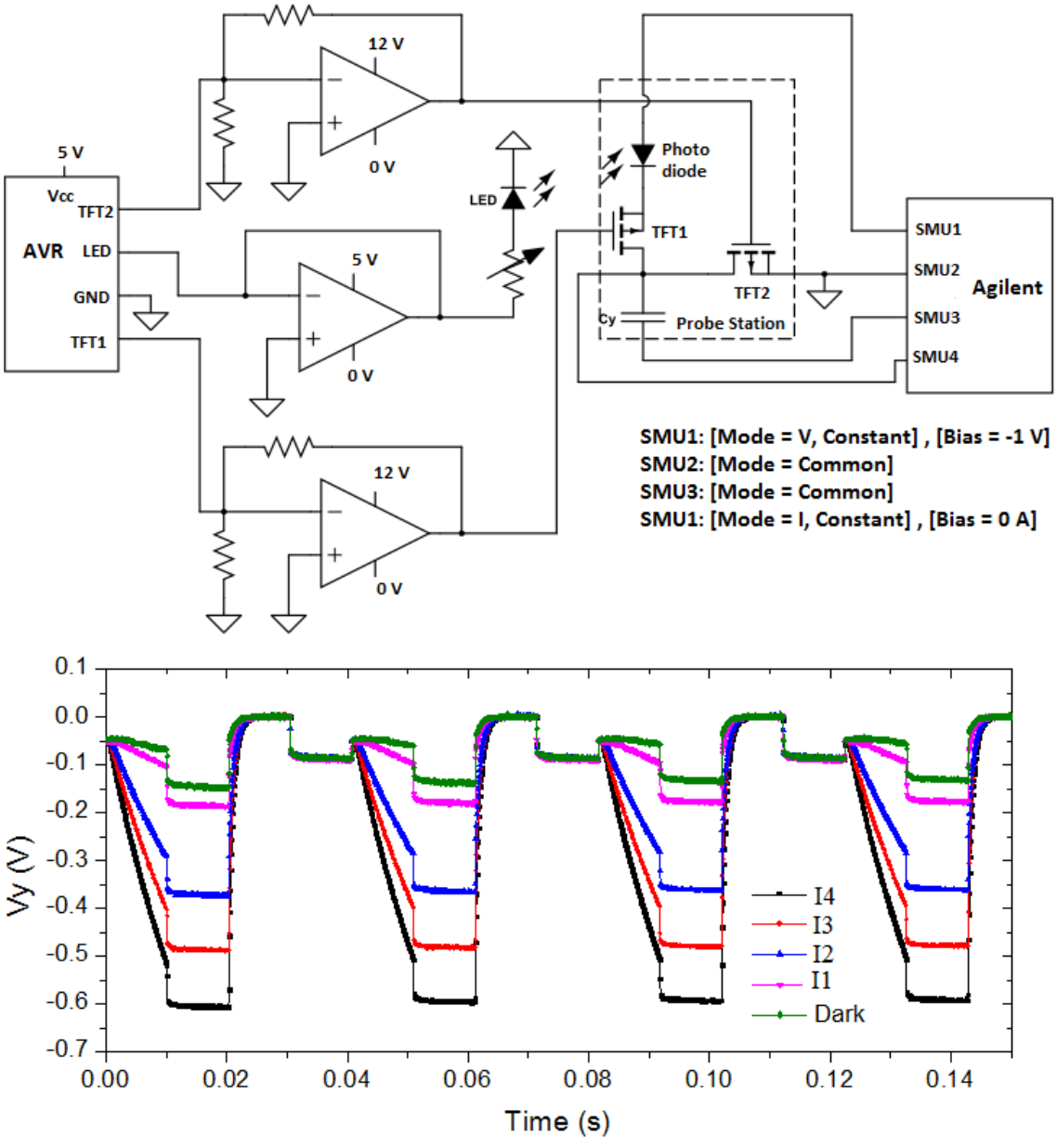


Figure 5.28: (a) Schematic representation of transient measurement setup for dual TFT pixel circuit. (b) Transient measurement results for dual TFT pixel with photodiode area of 0.25 mm^2 and two TFTs with $L = 40\ \mu m$, $W = 200\ \mu m$, and $OV = 4\ \mu m$ and pixel capacitor with the area of 1 mm^2 under variable light densities: $I_1 = 2.5\ \mu W/cm^2$, $I_2 = 12.5\ \mu W/cm^2$, $I_3 = 17\ \mu W/cm^2$, and $I_4 = 24.5\ \mu W/cm^2$.

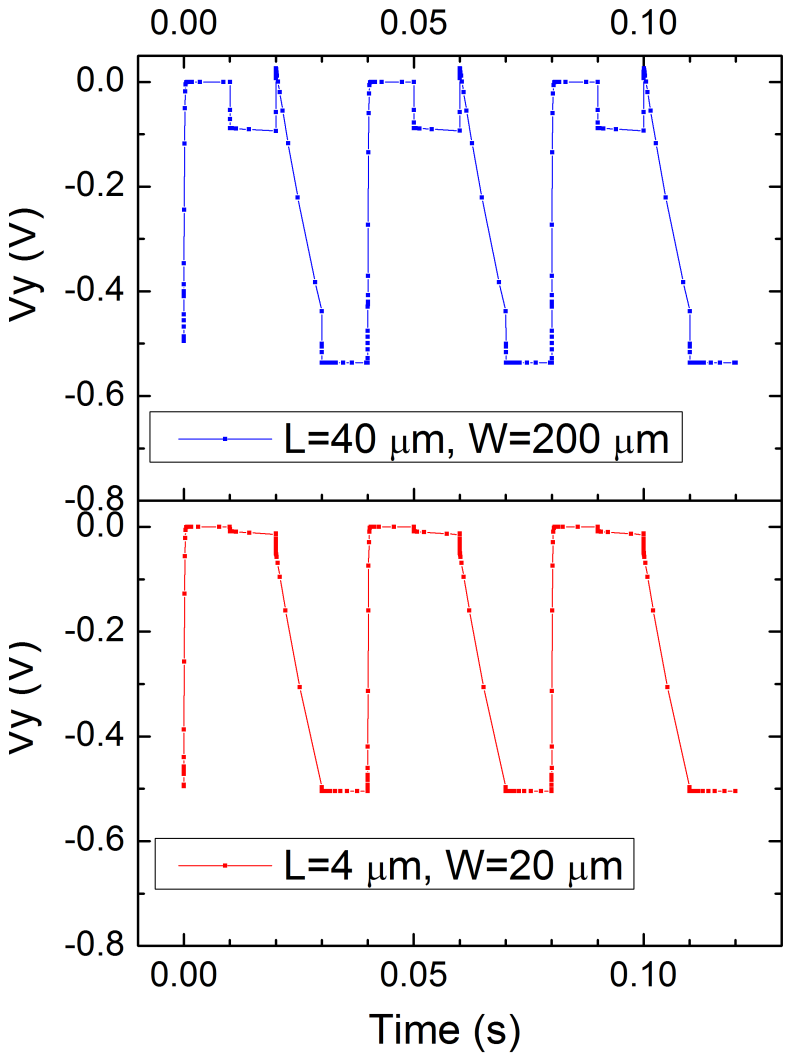


Figure 5.29: Comparison of transient simulation in dual TFT pixel with (a)$L = 40\ \mu m$, $W = 200\ \mu m$ and (b)$L = 4\ \mu m$, $W = 20\ \mu m$.

5.8 Chapter Summary

In this chapter, first we presented our results on fabrication of a bottom gate a-Si:H TFT which was used for integration with our μc-Si:H NIR photodiode to make NIR pixel circuits for 2D large area imaging applications. As opposed to previous works which tried to model the behaviour of the TFT using simple quadratic model of a transistor with two parameters (threshold voltage, and field effect mobility), we decided to model our TFTs using a more accurate HSpice level 61 model of the TFTs which contains 29 parameters for accurate modeling of the TFT in above threshold, subtreshold, and leakage regimes. We categorized these 29 model parameters into seven groups. The parameters in three groups out of the seven groups could be directly estimated using the existing facilities in G2N lab. For the rest of the parameters we used the default values for a-Si:H from the Hspice model. We also argued that the choice of the default values for those parameters doesn't introduce any discrepancy in our model. As a matter of fact the results of Hspice simulation are in very good agreement with the measurement results of our in house fabricated TFTs. This proves the accuracy of the extracted TFT model and provides a powerful tool for analysis of hybrid photodiode/TFT pixel circuits as we have accurate HSpice models for both devices. As a result, we were able to design and analyse the behaviour of hybrid pixel circuits using the HSpice simulation tool without requiring costly and time consuming trial and error fabrication and measurement steps in clean-room facility.

In the next part of this chapter we have discussed three different pixel designs using hybrid a-Si:H TFTs and μc-Si:H photodiode. Through theoretical analysis and by the use of Hspice simulator we were able to analyse and design a new type of photodiode pixel circuit. First of all we demonstrated that the conventional photodiode pixel circuit which works very well for a-Si:H photodiodes is not in fact suitable for μc-Si:H photodiodes due to

problems with pixel saturation and pixel signal drift during wait time. In order to address the pixel saturation problem we investigated the pixel with integrated capacitance. This circuit improves the early saturation problem but does not resolve the signal drift issue. Hence we proposed the new dual TFT circuit with integrated capacitance in order to resolve saturation problem and get rid of pixel signal drift.

In summary our final hybrid pixel circuit with two TFTs with $W = 200\ \mu m$, and $L = 40\ \mu m$, and $OV = 4\ \mu m$, one capacitor with area of 1 mm^2, and one photodiode with area of $500 \times 500\ \mu m^2$ shows a response time of 1.5 ms and almost no signal drift as opposed to drift of 6.7 mV/ms in conventional circuit. As a result, for the first time we demonstrate the possibility of microcrystalline silicon for implementation of fast, high dynamic range, and large area electronic compatible NIR photodetector pixel.

Chapter 6

Conclusion and Future Work

6.1 Summaries and Conclusions

In this work, we developed and characterized thin film microcrystalline silicon based photodiode NIR detector for large area contactless touch sensing application with high dynamic range of operation. Our photodetector gives dynamic range of 13 times higher than the state of the art large area inorganic near infrared detector reported to date. Furthermore, we extracted an accurate HSpice circuit model for our photodiode for further simulation, design and fabrication of pixel circuits for 2D arrays.

For this purpose, we designed and developed bottom gate a-Si:H TFT process for integration with the photodiode to create a NIR imaging pixel with switching capabilities. Our bottom gate TFT yeilds threshold voltage of 3.6 V with field effect mobility of 0.64 cm^2/Vs which is comparable to the state of the art a-Si:H TFT characteristics. Furthermore, we used HSpice level 61 model parameter extraction method for our a-Si:H TFTs, which is shown to accurately model TFT behaviour in above threshold and subthreshold region.

This TFT model alongside with the circuit model of our photodiode provided us with a tool to simulate and analyse the behaviour of pixel circuits fabricated based on the TFT/Photodiode hybrid.

Finally, we developed fabrication process for integration of TFTs with the photodiode to create pixel circuits for 2D imaging arrays. We analysed, designed and fabricated conventional pixel, which was proposed for a-Si:H indirect X-ray imaging systems and showed that it suffers from 2 major problems when microcrystalline silicon photodiode is used instead of a-Si:H photodiode. The first problem was the saturation of pixel and the second problem was significant pixel signal drift during the wait time due to high leakage current in μc-Si:H photodiode as opposed to a-Si:H photodiode. In order to prevent early saturation of the pixel, we proposed pixel with integrated capacitor with no additional cost compared to the conventional pixel circuit. We also demonstrated that there is a trade off between pixel speed and pixel capacitance in the pixel with integrated capacitor. We demonstrated that both conventional pixel and pixel with integrated capacitance suffer from signal drift during the wait time. In order to cope with the signal drift problem, we proposed novel pixel circuit design with 2 TFTs, one photodiode and an integrated capacitance. This pixel has orders of magnitude less signal drift during wait time compared to the two aforementioned circuits. As a result it is suitable for large area NIR imaging arrays.

The results of this work were published in the following journal papers ([17],[45]) and were reported at the following international conference ([81]).

6.2 Future Work

Although we proposed simple and feasible way to implement large area NIR detector pixel circuit based on a-Si:H TFTs and μc-Si:H photodiodes, we were still suffering from the charge injection phenomena from our TFTs as the size of TFTs were very large ($L = 40\ \mu m$ and $W = 200\ \mu m$). This was mainly stemming from our limited budget for design of 6 photomasks with fine pattern. micron sized patterns. If we could have been able to scale our channel length by a factor of 10 down to 4 μm we could have been able to reduce the charge injection effect by two orders of magnitude and the steps during the transients of the gate pulse could have been suppressed by a factor of 100. As a result in our future work we will invest on fabrication of our pixel circuit with small TFT channel length. The other advantage of small TFT dimensions is that our pixel fill factor can increase if we use small TFTs in our pixel layout.

Currently, we are experiencing pixel response time of about 1.5 ms in our hybrid pixel circuit. This means that if we have a resolution of 1080p the amount of time to capture one frame would be in the order of 2 s, which is very slow. As a result in order to be able to operate our pixel at higher speed, we need to use TFTs with much lower on-resistance. new technologies such as Gallium Indium doped Zinc Oxide have been demonstrated to have field effect mobilities which are two orders of magnitude higher than our current a-Si:H TFT. If those materials as TFT channel layer are used, our pixel circuit can be two orders of magnitude faster. As a result, replacement of a-Si:H TFT with new technologies such as GIZO will be another topic of future work.

Lastly, in order to increase the fill factor of our detector, we need to implement the integrated large area capacitor underneath the photodiode. This will only be possible if we come up with a design with more than 6 photomasks which will be implemented in our

future work.

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