Low-Leakage ESD Power Supply Clamps in General Purpose $65\ nm$ CMOS Technology

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Electrostatic discharge (ESD) is a well-known contributor that reduces the reliability and yield of the integrated circuits (ICs). As ICs become more complex, they are increasingly susceptible to such failures due to the scaling of physical dimensions of devices and interconnect on a chip [1]. These failures are caused by excessive electric field and/or excessive current densities and result in dielectric breakdown, electro-migration of metal lines and contacts. ESD can affect the IC in its different life stages, from wafer-fabrication process to failure in the field. Furthermore, ESD events can damage the integrated circuit permanently (hard failure), or cause a latent damage (soft failure) [2]. ESD protection circuits consisting of I/O protection and ESD power supply clamps are routinely used in ICs to protect them against ESD damage. The main objective of the ESD protection circuit is to provide a low-resistive discharge path between any two pins of the chip to harmlessly discharge ESD energy without damaging the sensitive circuits.

The main target of this thesis is to design ESD power supply clamps that have the lowest possible leakage current without degrading the ESD protection ability in general purpose TSMC 65 nm CMOS technology. ESD clamps should have a very low-leakage current and should be stable and immune to the power supply noise under the normal operating conditions of the circuit core. Also, the ESD clamps must be able to handle high currents under an ESD event. All designs published in the general purpose 65 nm CMOS technology have used the SCR as the clamping element since the SCR has a higher current carrying capability compared to an MOS transistor of the same area [3]. The ESD power supply clamp should provide a low-resistive path in both directions to be able to deal with both PSD and NDS zapping modes.

The SCR based design does not provide the best ESD protection for the NDS zapping mode (positive ESD stress at V_{SS} with grounded V_{DD} node) since it has two parasitic resistances (R_{Nwell} and R_{Psub}) and one parasitic diode (the collector to base junction diode of the PNP transistor) in the path from the V_{SS} to V_{DD}. Furthermore, SCR based designs are not suitable for application that exposed to hot switching or ionizing radiation [2]. In GP process, the gate oxide thickness of core transistors is reduced compared with LP process counterpart to achieve higher performance designs for high-frequency applications

using 1 V core transistors and 2.5 V I/O option. The thinner gate oxide layer results in higher leakage current due to gate tunneling [4]. Therefore, using large thin oxide MOS transistors as clamping elements will result in a huge leakage.

In this thesis, four power supply ESD clamps are proposed in which thick oxide MOS transistors are used as the main clamping element. Therefore, the low-leakage current feature is achieved without significantly degrading the ESD performance. In addition, the parasitic diode of the MOS transistors provides the protection against NSD-mode. In this thesis, two different ESD power supply clamp architectures are proposed: standalone ESD power supply clamps and hybrid ESD power supply clamps. Two standalone clamps are proposed: a transient PMOS based ESD clamp with thyristor delay element (PTC), and a static diode triggered power supply (DTC). The standalone clamps were designed to protect the circuit core against ± 125 V CDM stress by limiting the voltage between the two power rails to less than the oxide breakdown voltage of the core transistors, $BVOX_{ESD} = 5$ V. The large area of this architecture was the price for maintaining the low-leakage current and adequate ESD protection. The hybrid clamp architecture was proposed to provide a higher ESD protection, against ± 300 V CDM stress, while reducing the layout area and maintaining the low-leakage feature. In the hybrid clamp structure, two clamps are connected in parallel between the two power supply rails, a static clamp, and a transient clamp. The static clamp triggers first and start to sink the ESD energy and then an RC network triggers the primary transient clamp to sink most of the ESD stress. Two hybrid designs were proposed: PMOS ESD power supply clamp with thyristor delay element and diodes ($PTDC$), and NMOS ESD power supply clamp with level shifter delay element and diode ($NLDC$).

Simulation results show that the proposed clamps are capable of protecting the circuit core against ± 1.5 kV HBM and at least against ± 125 V CDM stresses. The measurement results show that all of the proposed clamps are immune against false triggering, and transient induced latch-up. Furthermore, all four designs have responded favorably to the 4 V ESD-like pulse voltage under both chip powered and not powered conditions and after the stress ends the designs turned off. Finally, TLP measurement results show that all four proposed designs meet the minimum design requirement of the ESD protection circuit in the 65 nm CMOS technology (i.e. HBM protection level of ± 1.5 kV).

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Dedication

To
my family
for their support and encouragement.

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List of Abbreviations

C

CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor

D

DSCR	Darlington-based SCR
DTC	Diode Triggered ESD power supply Clamp with thyristor delay element
DTSCR	Diode Triggered SCR
DUT	Device Under Test

E

EOS	Electrical Over Stress
ESD	Electrostatic Discharge

G

GGNMOS	Grounded-Gate NMOS
GP	General Purpose

H

HBM	Human Body Model

I

IC	Integrated Circuit
I/O	Input/Output

J

JEDEC	Joint Electron Device Engineering Council

L

LVTSCR	Low Voltage Triggered SCR

M

MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor

N

NLDC	NMOS ESD power supply Clamp with Level shifter delay element and Diodes

P

PTC	PMOS ESD power supply Clamp with Thyristor delay element
PTDC	PMOS ESD power supply Clamp with Thyristor delay element and Diodes

S

SCR	Silicon Controlled Rectifier
SoC	System on Chip
SPT	Square Pulse Testing

T

TC	Traditional Clamp
TLP	Transmission Line Pulse
TLU	Transient-Induced Latch-up
TSMC	Taiwan Semiconductor Manufacturing Company
TSC	Traditional Static Clamp

V

VLSI	Very Large Scale Integration

Chapter 1

Introduction

Since the development of Integrated Circuits (ICs) in the 1960's, fabrication technology of ICs has improved from being able to integrate just a few transistors in Small Scale Integration (SSI) to several billions of transistors in Very Large Scale Integration (VLSI). According to Moore's law [15], the physical dimensions of a transistor are shrinking every eighteen months, and the complexity of the integrated circuits will continue to increase dramatically. Consequently, the fabrication process of future VLSI circuits will continue to be an increasingly challenging issue, and many problems will arise within the VLSI design process. One of the problems is designing and implementing Electrostatic Discharge (ESD) protection circuits in advanced CMOS technologies. ESD is a well-known contributor to poor IC reliability and yield, and as ICs become more complex, they are increasingly susceptible to such failures due to the scaling of physical dimensions on a chip. This chapter introduces the basics of the ESD event, the design window of the ESD circuits, the modeling of the ESD event along with the ESD zapping modes and ESD protection method.

1.1 Nature of ESD phenomena

One of the well-known ESD events is the electric shock that happens to the human body by touching any metal, such as a doorknob, after walking on carpet. An electrostatic

charge is created in the human body by rubbing the shoes on the carpet; the charge is then discharged by touching the doorknob. This usually results in the discharge of a potential in a range of 0.1 to 35 kV [1]. The ESD event in the IC industry has four stages: charge generation, charge transfer, device response and device failure. The first stage, generation of a charge leads to an imbalance of electrons between two bodies that leads to the production of an electrical field. When two materials with two different potential charges come into contact, the second stage of an ESD event occurs in which a charge transfers from the higher potential object to the lower potential object until the voltages are equal between the two objects. The three models of the charge transfer are: Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM). The last two stages are checking the IC's response to the event and see if the IC is damaged or not [2].

The IC materials can be charged in different ways: triboelectric charging, contact with another charged material, and induction. Triboelectric is the most common way, and it occurs when two materials come in contact and are then separated. When two materials come into contact with each other, electrons transfer from one to the other depending on the electrical characteristics of each object. When the two materials are separated, if they are conductors the electrons redistribute and balance. However, if one or both materials are insulators, the insulator becomes charged. Many factors that affect the amount of triboelectric charge, such as the area of contact, the speed of separation, the relative humidity, the chemistry of the materials, and other factors [16]. In the case of a walking person, the charge transfers from the carpet to the body.

Conductive charging is the case when a charged object comes into contact with an isolated object of lower potential. While the two objects are in contact, a charge transfers to the lower potential object until the voltage is balanced between the two objects. After the separation, both objects will have a charge with the same polarity, but the amount of the charge will be proportional to the capacitance of each object [2]. Inductive charging, on the contrary, does not require a physical contact between the two objects rather it happens when a charged object "A" gets close enough to a conductive object "B". The electric field produced by object "A" leads to an internal separation of charges in object "B". Grounding object "B" while object "A" is still close removes the polarized charge.

When object "A" is removed, object "B" will have a charge that is opposite in polarity to the charge in object "A". This type of charging can lead to two ESD events for object "B", one while object "A" is present and the other after the charged object is removed [2].

1.2 ESD design window

There are many different aspects that should be considered when ESD protection circuits in nano-metric CMOS technology are being developed. It begins with choosing the appropriate protection circuit and ends with optimizing the ESD circuit. All ESD devices must be operated within the ESD design window that is shown in Fig. 1.1. In this figure, the vertical axis represents the maximum ESD current, which can be reflected as the HBM failure threshold level. The horizontal axis represents the voltage trends for both the core voltage (V_{DD}) and gate oxide breakdown voltage ($BVOX_{ESD}$) [7]. The figure also illustrates the two important regions of any IC: the IC operating area and the IC reliability area. For an ideal ESD design, the ESD protection circuit must turn on once the voltage across the power rails is higher than the I/O application voltage with some noise margin. Moreover, the ESD specification current must be reached before either the oxide breakdown voltage, or the transistor junction breakdown voltage for input, or output pad is reached. Generally, the ESD protection for an IC is limited by the oxide breakdown ($BVOX_{ESD}$). The figure also shows the interconnect metal threshold current density (JM_{ESD}), for the ESD regime which is governed by the metal thickness [7]. In addition, the figure shows the target HBM protection level, which is 1.5 kV in the case of 65 nm CMOS technology.

Fig. 1.2 presents the oxide breakdown voltage as a function of the gate oxide thickness under the ESD regime [8]. This reference was used as the guideline for designing the ESD devices in this thesis. The gate oxide thickness of the core transistor is about 2 nm in the used GP 65 nm CMOS technology. As a result, the gate oxide can sustain 5 V. Therefore, in this research, the design criterion was to design power supply clamps those can keep the voltage below 5 V under a 125 V CDM ESD stress and stays on for the entire 1.5 kV HBM ESD stress.

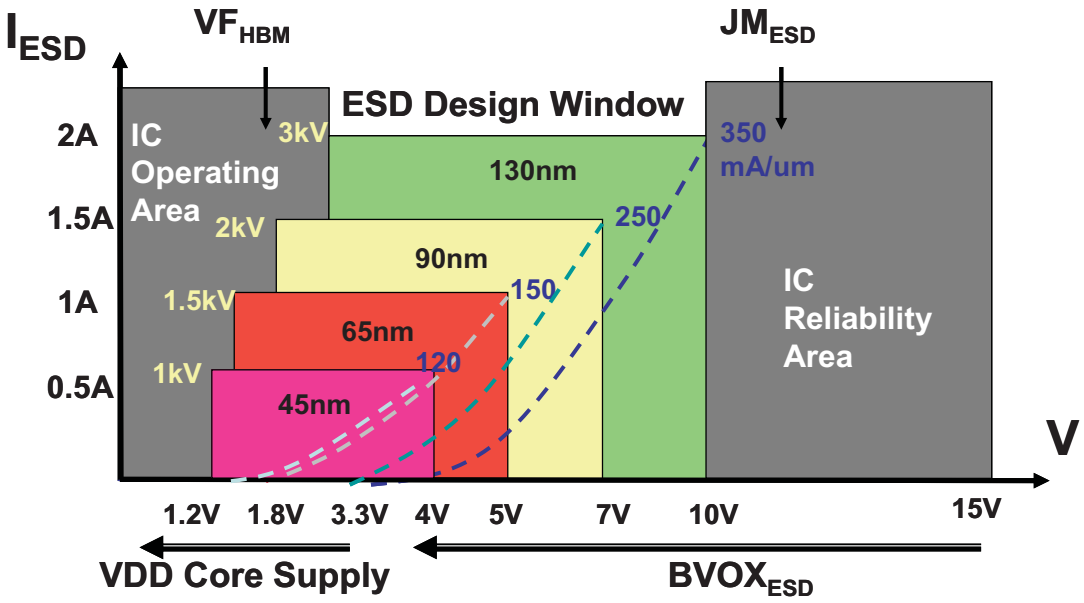


Figure 1.1: ESD design widow from 130 nm to 45 nm CMOS technologies [7].

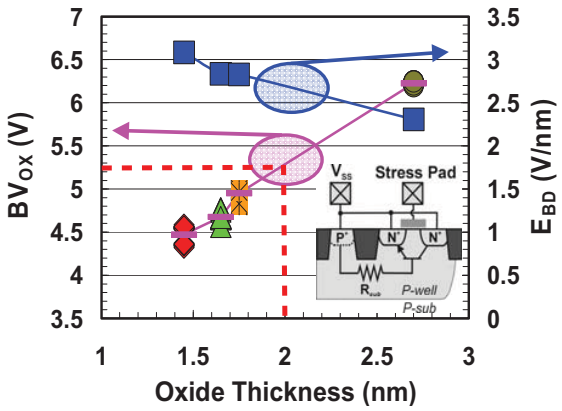


Figure 1.2: Gate oxide breakdown voltage trend [8].

1.3 Motivation

As the ESD event happens, it balances the charge between two objects and it is discharged in a very short time, it leads to high currents. As the current passes through an object, a voltage is developed across it and results in creating an electric field. The semiconductor devices can be damaged by both the high current density and the high electric field [2]. The high current density damages the semiconductor devices through thin-film fusing, filamentation, and junction spiking [17]. Thin-film fusing happens because high current density creates joule heating that can melt a region of a structure. Also, the high current density can cause high junction leakage because of filamentation damage. The junction spiking is the extreme case of filamentation [17]. The high electric field, on the other hand, can cause failure through dielectric breakdown or charge injection. In integrated circuits, silicon dioxide (SiO_2) is usually used as the dielectric material with high impedance, which can be broken down if the electric field is greater than the dielectric strength of the material. As a result, the oxide is damaged, and a conducting path is created between the gate and the substrate/drain of the MOS transistor. Charge injection does not result in a complete loss of functionality; rather it degrades the performance of the circuit. One effect of charge injection is a shift in the threshold voltage of an MOS device and more leaky devices because of the traps created in the oxide [17].

Based on the discussion above, a semiconductor device can fail if it becomes the discharge path of an ESD event. In the semiconductor industry, ESD is considered as a type of failure that is known as an electrical overstress (EOS), which includes conditions outside of the design operating environment such as voltage, current, and temperature. Also, the ESD can affect the integrated circuits (ICs) at different life stages from wafer-fabrication process (the first step of IC fabrication process) to the failure in the field. Furthermore, the ESD event can damage the integrated circuit immediately and permanently (hard failure), or cause a partial damage (soft failure) [1]. It has been reported that the ESD and EOS have caused up to 72 percent of the failures in IC technology [14]. Therefore, it is important to understand the ESD phenomenon and design ESD protection circuits that are capable of preventing those failures. The main target of the ESD protection circuits is to minimize the charge generation by draining any charge that builds up [1].

To achieve high switching speed in the current semiconductor processing technologies, the gate oxide thickness has been reduced to tens of angstrom that makes the chip more susceptible to ESD damages. Moreover, the increase of the chip sizes leads to increasing parasitic and package capacitances that can store a higher charge and makes the design more susceptible to ESD damages due to charged device discharge (CDM). Furthermore, leakage current has become a big issue in advanced CMOS technologies, and as the ESD protection circuits are off during normal operating conditions of the circuit core, it is essential to design low-leakage ESD protection circuits without significantly degrading the ESD performance. As a result, the ESD protection design becomes more challenging and increasingly important.

To show the importance of reducing the leakage of an ESD power supply clamp, the 8 Transistor 32 kbit SRAM shown in Fig. 1.3 proposed by J. Shah *et. al.* [18] is considered as an example. The design was fabricated in TSMC 65 nm CMOS technology, and it was tested in the CDR group's lab at the University of Waterloo. The total measured leakage current of this SRAM design was 172 μA that includes the core leakage as well as the leakage of Input/output periphery circuit. The ESD clamps are usually part of the I/O periphery circuit and let us assume that four ESD clamps were used with a thin transistor as a clamping element that has $L = 100$ nm and $W = 2000$ μm. The total simulated leakage current of these four clamps is 22 μA, which is about 12.8 % of the total leakage current of the entire design. This example gives an idea of the importance of reducing the leakage of the ESD clamps.

In this thesis, different ESD protection circuits (power supply clamps) are proposed and tested in 65 nm technology in which a low-leakage current with an excellent ESD performance are achieved.

1.4 Modeling the ESD event

Most ICs contain ESD protection circuits; these protection circuits are tested using the ESD event models to ensure correct functionality and to meet the desired reliability for a given application in the real world. The three most important sources of the ESD events

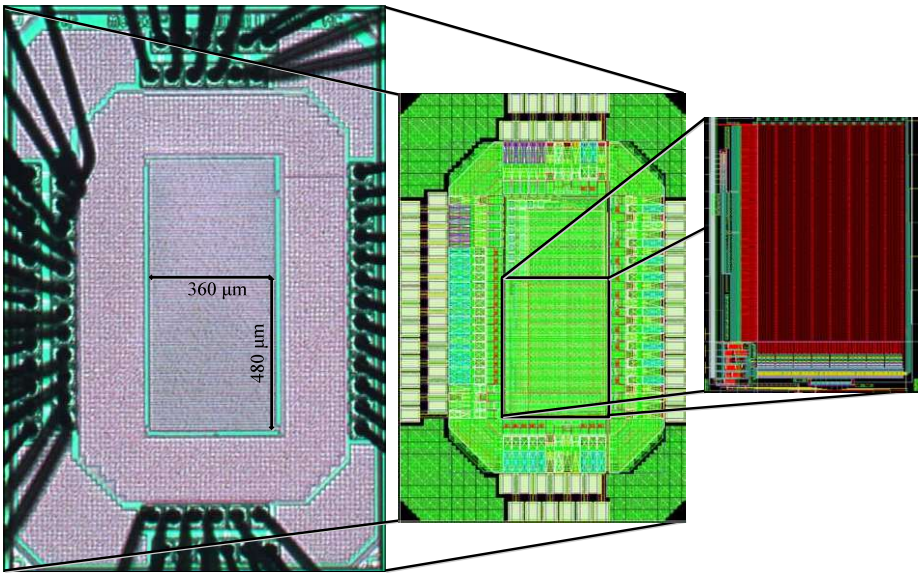


Figure 1.3: Die photo, chip-level layout, and the array layout of 8 T 32 kb SRAM [9].

are modeled: Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM).

1.4.1 Human Body Model (HBM)

HBM models a charged human body that dissipates the ESD event current through a grounded IC. The charge can transfer to the chip during assembly and handling. Fig. 1.4 shows the HBM ESD equivalent circuit, according to the Military Standard (Method 3015.8) [19], and JEDEC standard [20], where C_b represents the human body capacitance and the resistance R_b represents the human arm resistance, while DUT represents the device under test. The peak current through the DUT can be approximately calculated by [21]:

$$I_{PEAK}(A) \approx \frac{V_{ESD}}{(R_{DUT} + 1500\Omega)} \tag{1.1}$$

As a result, the peak current for each kilovolt can be approximately given by [21]:

$$I_{PEAK}(A) \approx 0.67 * V_{ESD} \pm 0.1 * V_{ESD}(A/kV) \tag{1.2}$$

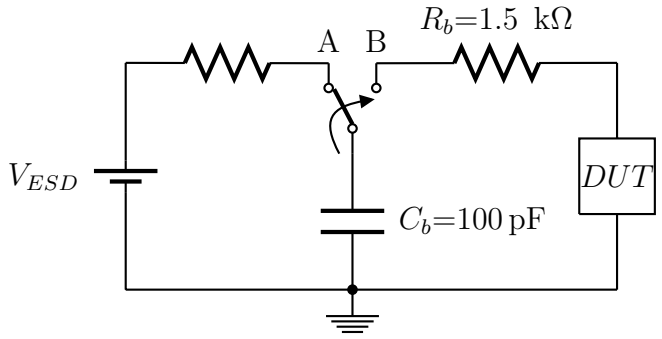


Figure 1.4: The Human Body Model (HBM).

The classification of the HBM stress based on their level of ESD protection is summarized in Table 1.1.

Class	V_{ESD} (V)
Class 0	< 250
Class 1A	$250 - 500$
Class 1B	$500 - 1,000$
Class 1C	$1,000 - 2,000$
Class 2	$2,000 - 4,000$
Class 3A	$4,000 - 8,000$
Class 3B	$> 8,000$

Table 1.1: Human Body Model Classes [5].

1.4.2 The Machine Model (MM)

MM represents a charged machine that is being discharged through a grounded IC (DUT). Fig. 1.5 shows the machine model in which the impedance of the charged machine (L_m) replaces the resistance in the HBM, while C_m represents the capacitance of the charged machine.

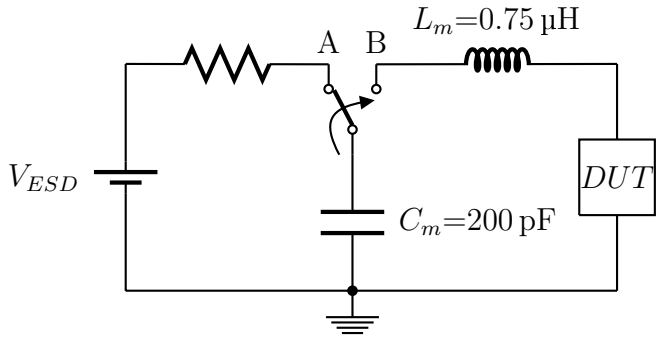


Figure 1.5: The Machine Model (MM).

Similar to the HBM, the MM is classified according to their ESD protection level. Table 1.2 summarizes the machine model classes.

Class	V_{ESD} (V)
Class M1	< 100
Class M2	$100 - 200$
Class M3	$200 - 400$
Class M4	> 400

Table 1.2: Machine Model Classes [6].

1.4.3 The Charged Device Model (CDM)

CDM models the case where the IC itself is charged and being discharged when it touches a grounded element. Fig. 1.6 shows the CDM ESD equivalent circuit according to JEDEC standard [22], where the capacitance C_{device} represents the packaging capacitance while the inductance L_p and the resistance R_p represents the discharging path from the chip to the ground. According to JEDEC Roadmap [10], in the modern assembly lines, an ESD-controlled environment is being used; as a result, the ESD protection level requirement

becomes lower. In this research work, a peak voltage of 125 V is chosen as a minimum requirement for the designs.

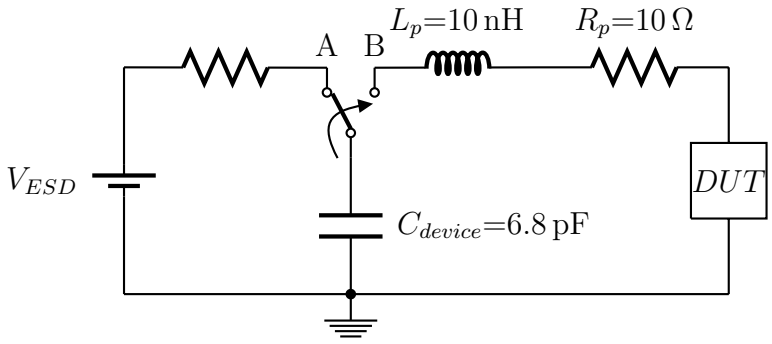


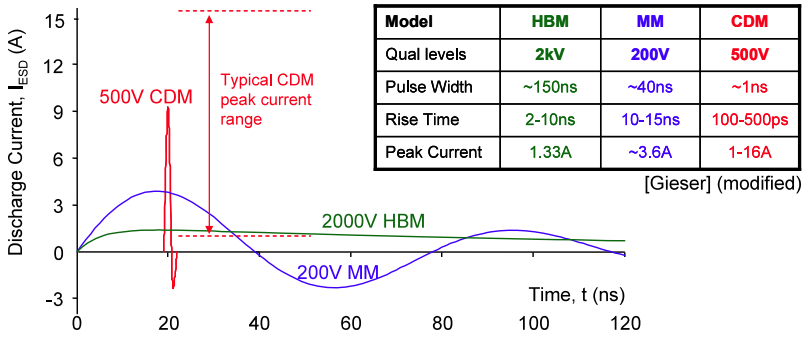
Figure 1.6: The Charged Device Model (CDM).

Similar to HBM and MM, Table 1.3 categorizes the charged device model into classes based on their ESD protection levels.

Class	V_{ESD} (V)
Class C1	< 125
Class C2	$125 - 250$
Class C3	$250 - 500$
Class C4	$500 - 1,000$
Class C5	$1,000 - 1,500$
Class C6	$1,500 - 2,000$
Class C7	$> 2,000$

Table 1.3: Charged Device Model Classes [1].

Fig. 1.7 shows the current waveforms for the different ESD models. The typical HBM discharge 2 kV has a peak current of 1.33 A, rise time of $2 - 10$ ns and decay time (pulse width) of $130 - 170$ ns and the entire duration is approximately $600 - 750$ ns; while the typical CDM has a peak current of $1 - 16$ A, and rise time of $100 - 500$ ps [10].



Model	HBM	MM	CDM
Qual levels	2kV	200V	500V
Pulse Width	~150ns	~40ns	~1ns
Rise Time	2-10ns	10-15ns	100-500ps
Peak Current	1.33A	~3.6A	1-16A

Figure 1.7: The current waveform for the different ESD models [10].

1.5 ESD testers

To test the robustness of ESD protection circuits, HBM, MM, CDM, and TLP tests are used as evaluation methods. The ESD tests can be done on the full circuit, on the sub-circuit such as input/output buffers or ESD power supply clamps, or on individual circuit components like transistors and resistors [23]. The main three testers in the industry are HBM/MM testers, CDM testers, and TLP testers.

1.5.1 HBM/MM testers

This class of testers is used to check the device under test (DUT) for both HBM and MM models. The voltage of the HBM/MM is gradually increased, and the result is given as the DUT passes or fails the applied voltage. The DUT is normally destroyed and cannot be reused [1].

1.5.2 CDM testers

This class of testers is similar to the previous category, but the difference is that the DUT is tested for CDM model. The voltage of the CDM is gradually increased, and the result is given as the DUT passes or fails the applied voltage. The DUT is normally destroyed and cannot be reused [1].

1.5.3 Transmission Line Plus (TLP) testers

The TLP tester is used to obtain the I-V characteristic of ESD protection circuits. TLP testing is one of the most popular methods to test the effectiveness of ESD protection devices and circuits. Maloney and Khurana [24] introduced the TLP technique for testing the ESD protection circuits in the 1980s, and since then it is widely used as it offers a reliable, and repeatable means for ESD testing. In the TLP testing, the HBM is modeled using the rectangular-pulse testing (RPT) or square-pulse testing (SPT). TLP with rectangular pulse widths of $75 - 200$ ns is correlated with HBM with 150 ns exponential pulse width [25]. The ESD industry has set the de facto standard of the TLP testing as: TLP pulse width set to 100 ns, and TLP rise time set to $2 - 10$ ns [11]. Fig. 1.8 shows the typical TLP and the HBM current waveforms.

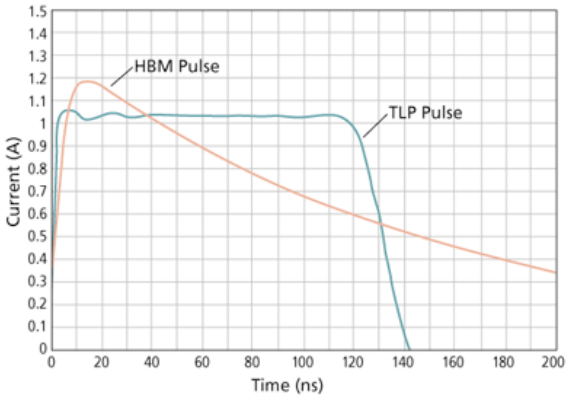


Figure 1.8: HBM pulse vs. TLP pulse [11].

It can be seen in Fig. 1.8 that the TLP current waveform does not represent any type of the real ESD event. However, it has been used to test the robustness of the ESD protection circuit since the experimental results showed that a TLP with a pulse width of 100 ns causes the same damage at the same peak current as the HBM ESD event [26]. The TLP testing is carried out using the TLP tester shown in Fig. 1.9. In Fig. 1.9, the high voltage DC source charges the transmission line, which creates a pulse while discharging. The amplitude of the pulses is gradually increased starting from 1 V until the Device Under Test (DUT) fails, the DUT is considered failed when its leakage current under the nominal

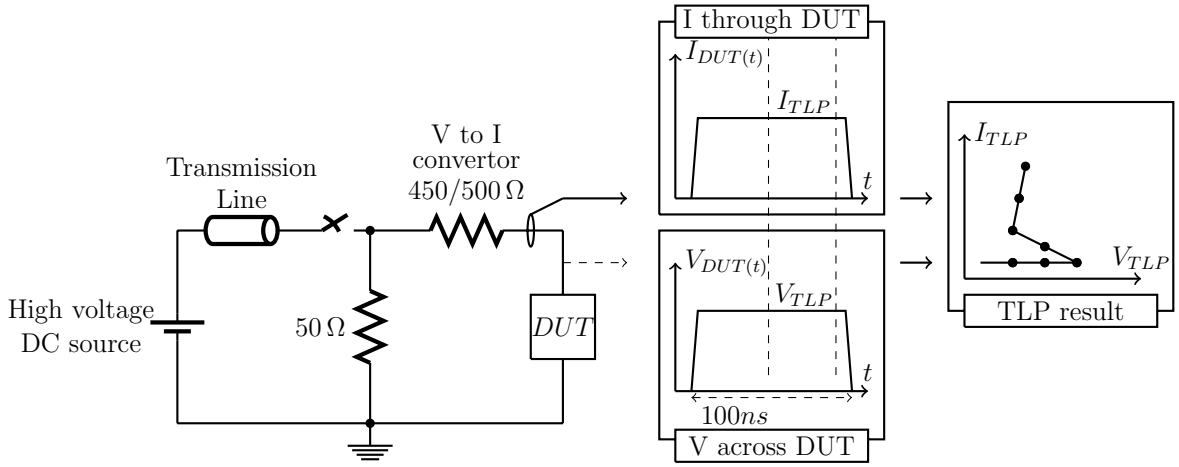


Figure 1.9: The schematic of the constant current TLP tester.

power supply significantly increases [21]. When the DUT fails, the second breakdown current (I_{t2}) happens, and the leakage current suddenly increases. I_{t2} is multiplied by the human body resistance (1.5 $K\Omega$) to estimate the maximum protection capability of a DUT under HBM stress [21].

In the TLP tester, the 50 Ω resistance is used as a controlled load for the transmission line, while the other resistance $450 - 500$ Ω is used to convert the voltage generated by the transmission line to a constant current to inject it into the DUT. This tester is known as a constant current TLP tester and can provide up to 4 A; however, a higher current is needed in many IC designs. To provide a higher current, another TLP tester named a constant impedance TLP tester is used. This TLP tester provides up to 10 A with a rise time range of $0.2 - 10$ ns [1]. As a result of the TLP testing, an I-V curve that represents the accurate values of the current (I_{TLP}) and the voltage (V_{TLP}) of the DUT is obtained. The accurate values are produced by averaging the digitized data for a certain period of time close to the end of the pulse (pick-off points range from 50% to 90% of the pulse width). The TLP tester generates the TLP pulse at each point in the curve to the DUT while it is not powered [27], as shown in Fig. 1.9. The slope of the generated curve is the inverse of the on-resistance (R_{ON}) of the DUT.

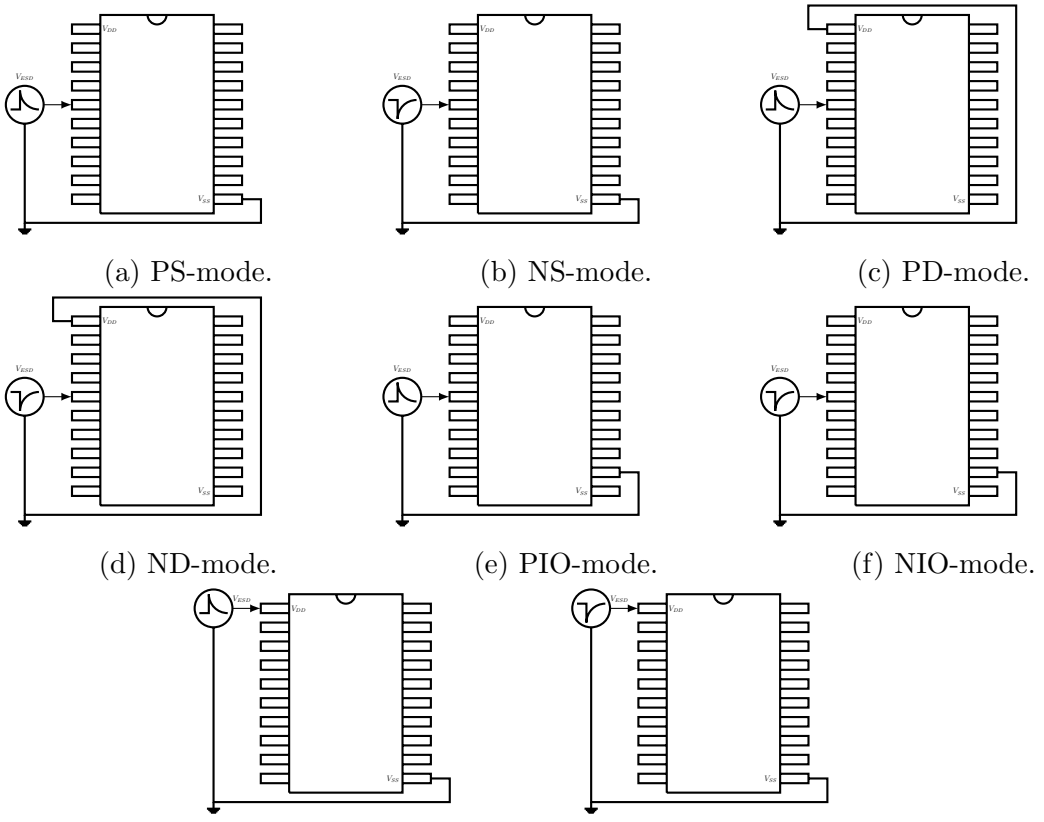
1.6 ESD zapping modes

Typically, there are three different pin types in a packaged IC: V_{DD}, V_{SS} and I/O. When ESD events happen associated with an I/O pad, there are six possible zapping modes for an ESD event depending on the polarity of electrostatic charge and the discharge path. These modes are a positive ESD voltage at the I/O pad with grounded V_{SS} (PS-mode) as shown in Fig. 1.10 (a), a negative ESD voltage at the I/O pad with grounded V_{SS} (NS-mode) as shown in Fig. 1.10 (b), a positive ESD voltage at the I/O pad with grounded V_{DD} (PD-mode) as shown in Fig. 1.10 (c), a negative ESD voltage at the I/O pad with grounded V_{DD} (ND-mode) as shown in Fig. 1.10 (d), a positive ESD voltage at one I/O pad with respect to another I/O pad (PIO-mode) as shown in Fig. 1.10 (e), and a negative ESD voltage at one I/O pad with respect to another I/O pad (NIO-mode) as shown in Fig. 1.10 (f). In addition to these six zapping modes, there are two other possible zapping modes associated with the power supply rails, which are: a positive ESD voltage at V_{DD} pad with grounded V_{SS} pad (PDS-mode) as shown in Fig. 1.10 (g) and a negative ESD voltage at V_{DD} pad with grounded V_{SS} pad (NDS-mode) as shown in Fig. 1.10 (h).

1.7 ESD protection method

As mentioned in the previous section, ESD stress can be in one of eight forms: PS, NS, PD, ND, PIO, NIO, PDS, and NDS modes. Therefore, ESD protection circuit should be able to deal with all zapping modes. Fig. 1.11 shows a whole-chip ESD protection scheme against all zapping modes using ESD power supply clamps. The importance of the whole-chip ESD protection has increased and now plays an important role in the reliability of the integrated circuits. The circuit core is susceptible to damage if there are only ESD protection circuits at the input and the output pads. As a result, it is important to have an effective ESD power supply clamp across the power supply rails so that the ESD event would be discharged through it and protects the circuit core [28].

To illustrate the whole-chip ESD protection scheme, consider the realization of the PS-mode (a positive charge at an $I/O\ PAD_1$ with grounded V_{SS}) protection is activated



(a) PS-mode. (b) NS-mode. (c) PD-mode.

(d) ND-mode. (e) PIO-mode. (f) NIO-mode.

(g) PDS-mode. (h) NDS-mode.

Figure 1.10: Zapping modes.

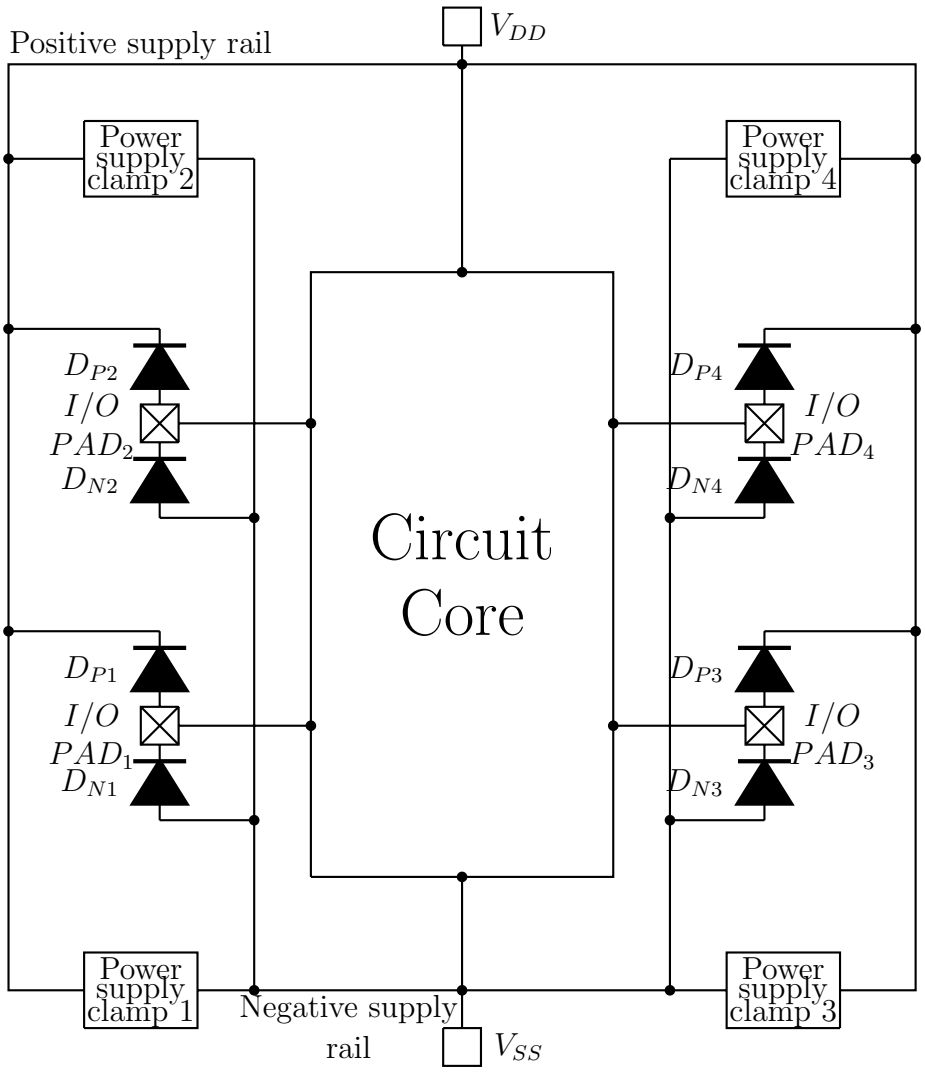


Figure 1.11: A typical whole-chip ESD protection scheme.

by transferring the ESD charge to the positive supply rail using the forward-biased D_{P1}. Subsequently, ESD power supply clamp 1 transfers the charge to V_{SS} and protects the circuit core. Fig. 1.11 shows diodes are used as the protection component attached to the input/output pads; however, the avalanche junction such as MOSFET and Silicon Controlled Rectifier (SCR) are also used to design the protection circuit. When the ESD stress happens, these devices operate in their breakdown region, which has a snapback characteristic. Therefore, these devices are classified as snapback protection devices [1]. A single power supply clamp or multiple power supply clamps can be distributed across the IC between the two power rails. Using multiple distributed clamps reduce the parasitic resistance between the power supply clamp and the pin clamps [17]. The ESD power supply clamps usually operate in the normal operating region and classified as non-snapback protection devices. Also, the ESD clamps should provide a low-resistive path for both directions to deal with both PSD and NDS zapping modes. The usage of an efficient ESD power supply clamp can result in smaller dimensional ESD protection components at I/O pads to fulfill high ESD robustness [29].

1.8 Summary and thesis outline

In this chapter, electrostatic discharge (ESD), as one problem in modern semiconductor technologies was briefly presented. Moreover, ESD failures in nano-metric technologies and the ESD design window were briefly introduced. The three main models of the ESD event were introduced along with different zapping modes. Finally, the typical whole-chip ESD protection scheme was introduced. The remainder of the thesis is organized as follows: Chapter 2 introduces an overview of previous efforts in developing ESD protection circuits especially for ESD power supply clamps. Chapter 3 presents the proposed standalone ESD power supply clamps and shows the results obtained. Chapter 4 presents the proposed hybrid ESD power supply clamps and shows the obtained results. Finally, Chapter 5 concludes the thesis.

Chapter 2

Literature Review

This thesis is concerned with the investigation of Electrostatic Discharge (ESD) protection circuits in GP 65 nm CMOS technology, especially ESD power supply clamps. This chapter presents previous work that has been carried out to design ESD power supply clamps and figures of merit that are used to compare the different ESD clamps. As mentioned in the previous chapter, it is important to have an effective ESD power supply clamp across the power supply rails to provide a low-ohmic discharge path for the ESD event that results in protecting the circuit core [1]. This ESD power supply clamp should have the following characteristics:

- Very low on-resistance.
- Very low-leakage current.
- Its triggering / turn-on voltage should be greater than the supply voltage (V_{DD}).
- Turns on immediately when the ESD event happens.
- Be capable of handling high currents.
- Consumes a small layout area.
- Immune against false triggering as well as power supply noise.

To achieve adequate characteristics of the above list, different ESD power supply clamps have been designed. These designs can be classified under one of the following two categories:

1. Static power supply ESD clamps.
2. Transient power supply ESD clamps.

The selection of what type of clamp to use in a design depends on many criteria. The first criterion is what circuit elements are available in a process. The second one is related to the environment where the design will be used. For instance, SCR is not suitable for application that exposed to hot switching or ionizing radiation. The last criterion is the current carrying capability and the turn on time for the clamping element [17].

2.1 Static power-rail ESD clamps

The static ESD clamp turns on once the voltage across the power supply rails exceeds the triggering voltage then the clamp starts discharging the ESD event. Based on the clamping element, the static clamps can be classified into three categories: diode based, MOSFET based and SCR based.

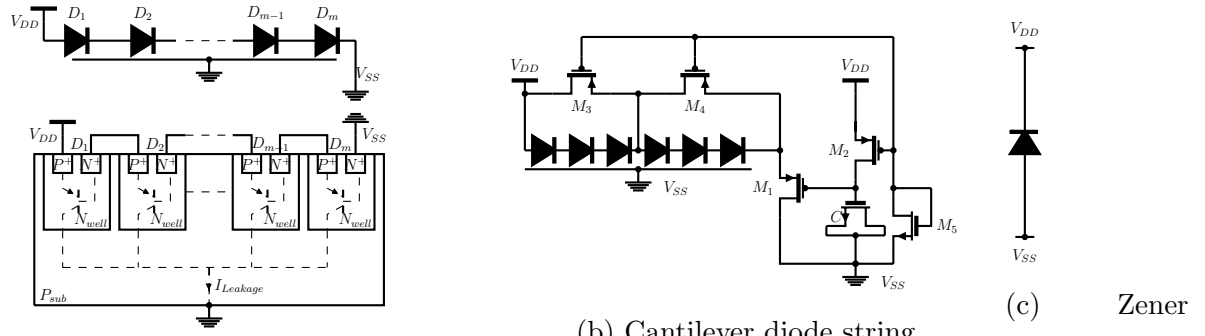
2.1.1 Diode based static ESD clamps

Since the diode can sustain a very high current when it operates in the forward-biased condition, Voltman *et. al.* [30] proposed the diode string as shown in Fig. 2.1 (a).

The triggering voltage of the design can be adjusted by increasing the number of the diodes using the following equation:

$$V_{trigg}(I) = m * V_D(I) - n * V_T * \frac{m(m-1)}{2} * ln(\beta + 1) \tag{2.1}$$

Where m is the number of diodes, V_D is the triggering voltage of the diode, n is an ideality factor, and β is the current gain of the PNP transistors, which are used to shunt the ESD



(a) Diode string and its sectional view.

(b) Cantilever diode string.

(c) Zener diode

Figure 2.1: Diode based power-rail ESD clamp.

current. The main disadvantages of this design are: (i) the leakage current increases when the number of diodes increases, (ii) stacking more diodes does not increase the triggering voltage linearly; also, the triggering voltage reduces and the leakage current increases with increase in temperature.

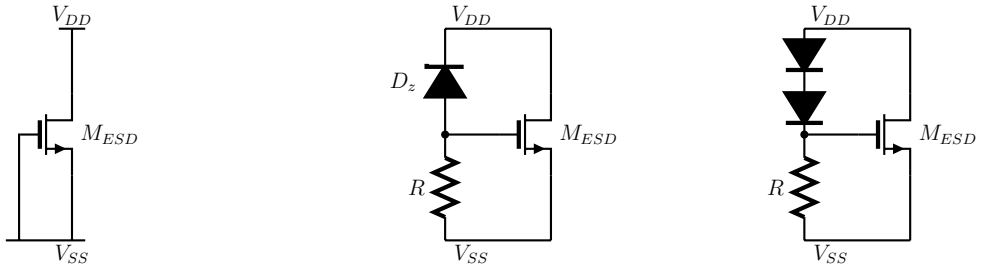
To overcome the leakage problem, Maloney *et. al.* [31], [32] proposed the cantilever diode string shown in Fig. 2.1 (b). The transistor M_1 is used to block the diode string from V_{SS} when the circuit is operated under the normal operating conditions; as a consequence, the leakage current is reduced. When the ESD event happens M_1 is turned on, and a conducting path between the power supply buses exists. Transistors M_2 and M_5 with the capacitor C are used to detect the ESD event and turn the transistor M_1 on, while M_3 and M_4 are used to distribute the current among the diode string; thus, the reduction in the blocking voltage is reduced. The cantilever diode string was developed to reduce the leakage current in the diode based ESD clamps operating in a high-temperature environment. However, the area of the cantilever design is large compared with the diode string since the transistor M_1 has to be large to sink a substantial amount of current during the ESD event.

In addition, the ESD static clamps can be developed using different kinds of diodes such as Zener diode as shown in Fig. 2.1 (c). When the ESD event occurs, the Zener diode operates in avalanche breakdown region. Therefore, the breakdown voltage of the Zener diode has to be greater than the supply voltage; also, the Zener diode is not available in

many technologies (i.e. requires additional processing steps) [1].

2.1.2 MOSFET based static ESD clamps

Grounded gate NMOS (GGNMOS) was one of the first proposed MOS based clamps as shown in Fig. 2.2 (a) in which the width of the transistor is typically $800\mu m$ [33]. The advantage of this design is it does not require large silicon area; however, it usually has a large drain to gate spacing. As a result, the clamp has a slow response to the ESD event and some transistors in the circuit core might have smaller spacing so that they can turn on before the GGNMOS and get destroyed.



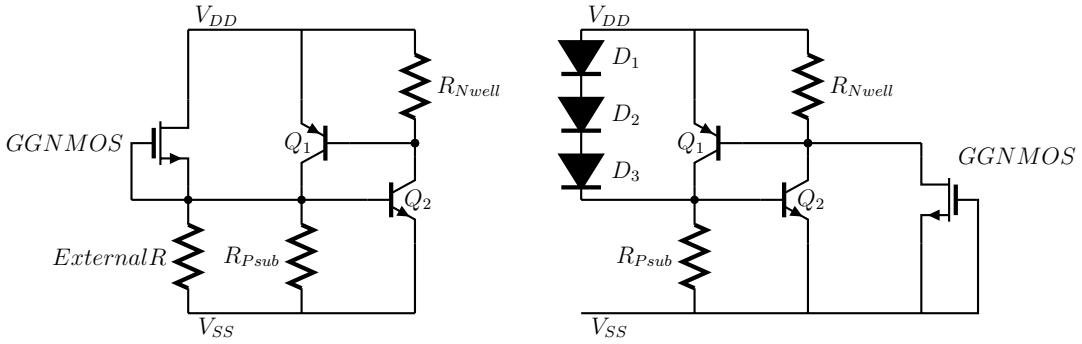
(a) GGNMOS. (b) Zener diode. (c) Diode string.

Figure 2.2: MOSFET based static power-rail ESD clamp.

To speed up the response of the GGNMOS, the Zener diode coupled design was proposed [34] as shown in Fig. 2.2 (b). Consequently, the triggering time is reduced compared with the GGNMOS, but this design has similar disadvantages as the Zener diode based clamp. Another design was proposed in [35] to overcome the slow response as shown in Fig. 2.2 (c). The design consists of a poly silicon diode string that has leakage in order of μA, which is three order of magnitude lower compared with the silicon diodes under the 5 V supply voltage bias. To reduce the leakage current, the number of the diodes should be 6 to 9 diodes.

2.1.3 SCR based static ESD clamps

Silicon Controlled Rectifier (SCR) devices can sustain high ESD stresses with a small layout area as compared with other traditional ESD protection elements [36]. However, they usually have a low triggering and holding current/voltage that causes them to be triggered by an external noise while the circuit is operated in the normal operating conditions [1]. To overcome this problem, modifications were done to the normal SCR; several SCR-based ESD static clamps were proposed. In [37], a high holding current Low Voltage Triggered SCR (LVTSCR) was proposed. As shown in Fig. 2.3 (a) the design consists of SCR, Grounded-Gate NMOS transistor (GGNMOS) and external poly resistance.



(a) HHI-SCR. (b) DTSCR.

Figure 2.3: SCR based static power-rail ESD clamp.

The values of the n-well and the p-substrate resistances can be reduced through adjusting the external poly resistance; as a result, a higher base current is required to trigger the SCR, which leads to a higher holding and triggering currents. The holding current of this design is three times greater than the conventional LVTSCR. In [38], a string of diodes was used to increase the triggering voltage of the LVTSCR as shown in Fig. 2.3 (b). In this architecture, as the number of the diodes increases the triggering voltage increases, typically $2-3$ diodes are used; however, the holding voltage must be increased above the supply voltage (V_{DD}) to ensure immunity against latch-up. In [39], a diode string is used along with resistance to trigger the SCR as shown in Fig. 2.4. Under ESD event, the diode string is on that leads to a voltage drop across the resistance R; thus, M_P is on, and

it triggers the SCR. During normal operating conditions, the diode string is off, and the voltage at node A is the same as V_{DD}, which makes M_P off and the SCR off.

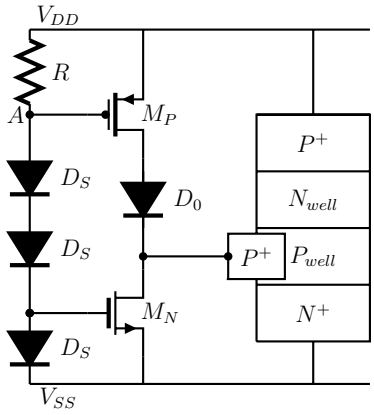


Figure 2.4: SCR based static power-rail ESD clamp with diode-string ESD detection.

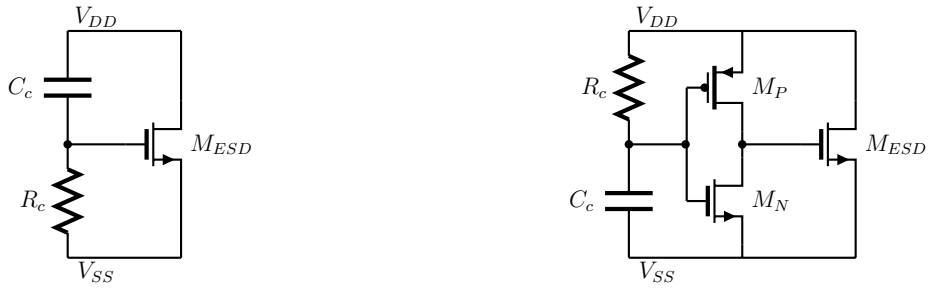
2.2 Transient power-rail ESD clamps

Since the ESD event has a rising time in microsecond range, which is three orders of magnitude greater than the normal rising time of the power supply, the transient ESD power supply clamps are designed so that they are turned on when the rising time of the voltage at the power supply rails exceeds a certain rising time. During design stages, some key parameters should be taken into account which are: triggering voltage, delay in turning on and on-time duration of the clamp [1].

The transient ESD clamps have the following advantages: they turn on very fast and turn off very slowly, stay on to discharge the ESD event for a fixed period of time, which is determined by RC network and the delay circuit, provide an ESD protection at a low triggering voltage, do not need any extra process steps, have a relaxed layout constraints, and can be designed and simulated using circuit simulators such as Cadence [40]. However, the transient clamp may trigger while the main circuit is in the normal operating mode, which will result in shorting the power supply to ground. The transient clamps can be classified as either MOSFET based or SCR based.

2.2.1 MOSFET based transient ESD clamps

Fig. 2.5 shows the traditional MOSFET based transient clamps in which the NMOS transistor is designed to be large so that it will be able to handle the ESD event. Under the normal operating conditions, the voltage at the gate of the transistor is low; therefore, the transistor is off. However, when the ESD event occurs, the detection circuit that consists of capacitor and resistor as in Fig. 2.5 (a) or capacitor, resistor, and inverter as in Fig. 2.5 (b) triggers the NMOS transistor to discharge the event.



(a) Gate coupled NMOS. (b) Traditional transient clamp.

Figure 2.5: MOSFET based transient power-rail ESD clamp.

The time constant of the RC circuit should be designed to ensure keeping the clamp conducting for a time of 500 ns to 1 μs [41]. A time constant of 1 μs can be obtained using a 50 $k\Omega$ poly silicon or n-well resistance and a 20 pF poly-gate or metal-to-metal (MOM) capacitance, which requires a large area [1]. In addition, the traditional transient ESD clamps suffer from the false triggering due to the noise of the power supply. Therefore, the three stage transient clamp [42] was proposed to overcome the disadvantages of the traditional MOSFET based transient clamps as shown in Fig. 2.6. In the three stage transient clamp, the triggering circuit is divided into a rise time detector and a delay element. The rise time detector consists of an RC network, and its time constant is typically set to 40 ns to distinguish between the normal power supply ramp up and the ESD event [41]. The delay element keeps the main transistor (M_{ESD}) on for enough time to sink the ESD event. This design has an improved noise immunity compared with the RC control ESD clamp; however, the experimental results show that clamps with several

inverters are susceptible to oscillation during the ESD event and/or power-on condition [43]. The oscillation is the case when the clamp oscillates between the on and the off states and might damage the circuit core. The oscillation can be ignored as long as its magnitude is less than the oxide breakdown voltage, and it has a limited duration. The power-on oscillation might result in severe damage during normal operating mode [1].

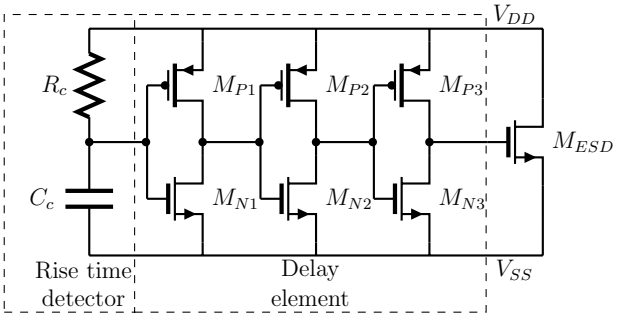
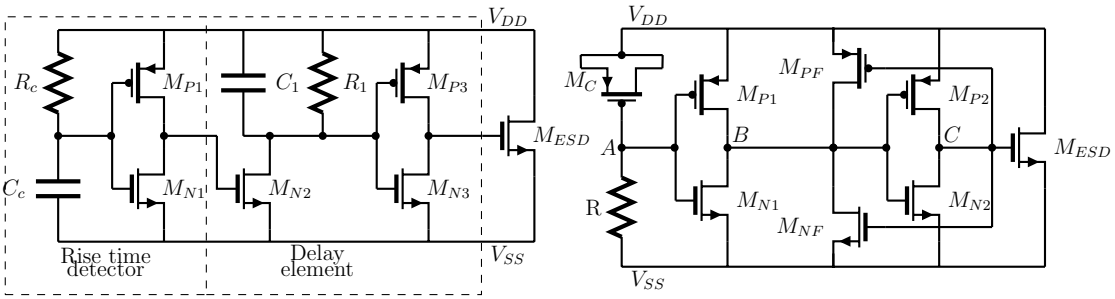


Figure 2.6: Three stage transient power-rail ESD clamp to avoid false triggering.

In [41], Stockinger *et. al.* proposed a clamp using this concept as shown in Fig. 2.7 (a). In this design, the triggering circuit is divided into a rise detector circuit consists of R_c, C_c with a time constant of 40 ns, inverter, and a delay element that is based on a mono-stable circuit. The delay element has a time constant (R_1, C_1) of 600 ns to ensure discharging the ESD event. In addition, the total area of the clamp was optimized by increasing the gate voltage of the large transistor M_{ESD} using a boosted supply bus; as a result, the total area of the main transistor M_{ESD} was reduced by 54%.

In [42], Merrill and Issaq proposed a SRAM based clamp shown in Fig. 2.7 (b). In this design, a SRAM was used as a delay element that keeps the main transistor M_{ESD} on for 700 ns. Under the normal operating conditions, the voltage at node A is low; as a consequence, the voltage at node B is high which pulls the voltage at node C to the ground; thus, the main transistor M_{ESD} is off. Under the ESD event, the voltage at node A is high; therefore, the voltage at node B is low, while the voltage of node C is high. As a result, the clamp transistor M_{ESD} is on to discharge the ESD event. The simulation and experimental results showed that this design is immune against false triggering and power supply noise; however, it is susceptible to oscillation.



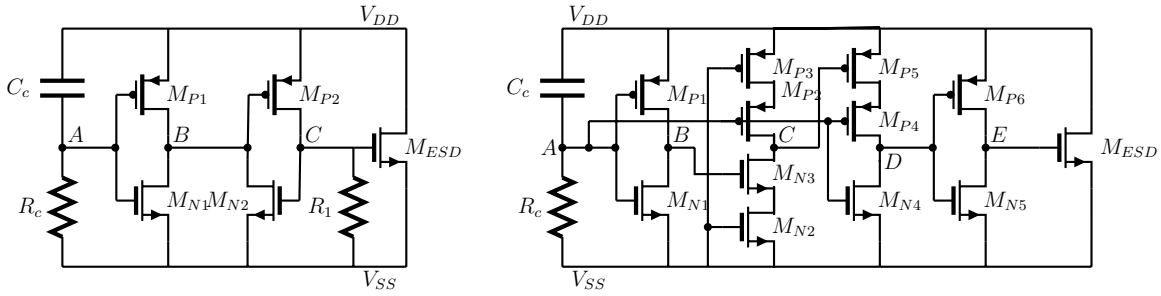
(a) Dual time constant triggering circuit.

(b) SRAM based.

Figure 2.7: Transient power-rail ESD clamp.

Sarbishaei *et. al.* [44] proposed a transient ESD clamp that uses CMOS thyristor as a delay element as shown in Fig. 2.8 (a). In this clamp, the time constant of the RC network was set to 40 ns. Under the ESD event, the voltage at node A is going towards V_{DD} very fast; as a result, the voltage at node B is going towards V_{SS} that turns the transistor M_{P2} on, which results in turning the main transistor M_{ESD} on. Besides, the CMOS thyristor keeps the main transistor M_{ESD} on for more than 1 μs, which is more than enough time to discharge the ESD event. Under the normal operating conditions, the voltage at node A is low, at node B is high; thus, M_{P2} is off, and the voltage at node C is floating. The resistance R_1 was added to pull down the voltage at node C under normal operating conditions. Simulation and experimental results showed that the design is immune against false triggering, power supply noise, and oscillation.

Serbishasi *et. al.* [45] proposed a D flip-flop based transient clamp that is shown in Fig. 2.8 (b). The data input of the flip-flop is connected to ground, while the rising edge is connected to the clock input. Under the normal operating conditions, the gate of transistor M_{P4} is connected to the clock signal (clk); thus, as the capacitor C_C is fully charged, the transistor M_{P4} is on and the clamping transistor M_{ESD} is off. The case is reversed under the ESD event, where the transistor M_{P4} is off, while the transistor M_{N4} and the clamping transistor M_{ESD} are on for more than 1 μs. Simulation and practical results showed that this design has immunity against false triggering, power supply noise, and oscillation.



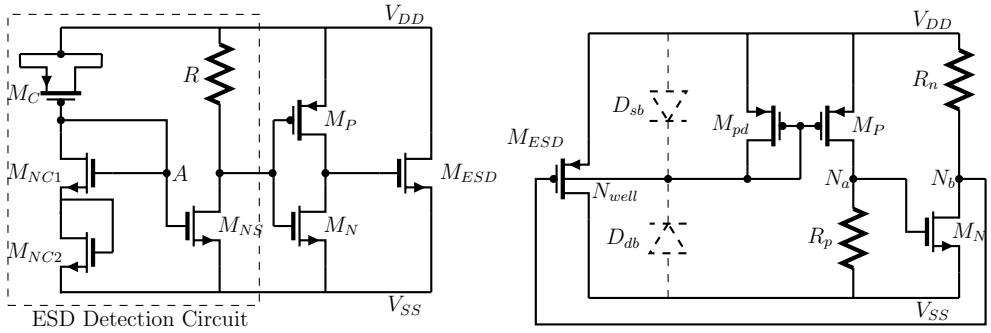
(a) Thyristor based. (b) Flip-flop based.

Figure 2.8: Transient power-rail ESD clamp.

2.2.1.1 Small capacitor and capacitor less transient ESD clamps

This section reviews designs that attempt to reduce the layout area of the transient ESD clamps. As the RC network consumes some area, optimizing the design to reduce the RC network or using different techniques to act as the rise time detector element will lead to reducing the overall area of the clamp. Chen and Ker in [46] proposed a design that is shown in Fig. 2.9 (a), in which the triggering circuit consists of the cascade transistors (M_{NC1} and M_{NC2}) and the capacitance M_C. Under the ESD stress, the voltage at node A is high which turns both M_{NS} and M_P transistors are on that leads to trigger the main transistor M_{ESD} on. By using this technique, overall area of the clamp was reduced by 13% compared with the traditional transient clamp shown in Fig. 2.5 (b). In [47], shown in Fig. 2.9 (b), the design utilizes the two parasitic diodes of the main transistor (M_{ESD}) as the equivalent capacitance, while the diode-connected PMOS transistor M_{pd} is used as a large resistance. During the ESD event, the equivalent RC turns M_P on; thus, M_N is on, and that turns on the main transistor M_{ESD}. The layout area of this clamp is reduced by 46% compared with the traditional transient ESD clamp.

In [48], [49], Yeh *et. al.* took advantage of the large size of the main transistor M_{ESD} and they used its parasitic capacitors as the capacitor of the trigger detection circuit as shown in Fig. 2.10 (a). The main transistor M_{ESD} was implemented in BigFet style without silicide blocking; as a consequence, large parasitic capacitances were obtained. The parasitic capacitors along with the resistance R_p build the capacitance-coupling mechanism.

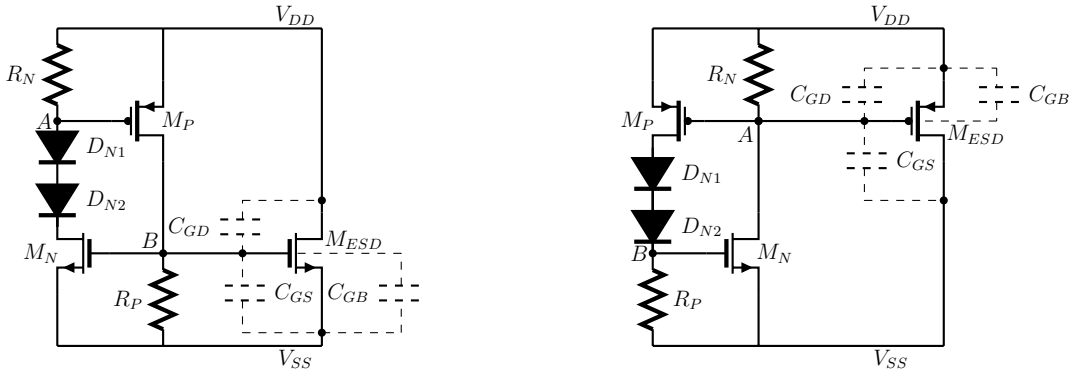


(a) With smaller capacitance in ESD transient detection circuit.

(b) With equivalent detection mechanism.

Figure 2.9: Power-rail ESD clamp.

As a result of using the parasitic capacitors, the layout area of this design was reduced by 54% compared with the traditional RC-based power-rail ESD clamp.



(a) With NMOS ESD element

(b) With PMOS ESD element

Figure 2.10: capacitor-less power-rail ESD clamp.

The triggering circuit of this clamp consists of two transistors (M_n and M_p) and two resistances (R_n and R_p). The gate of M_{ESD} is connected to the output of the triggering circuit. To avoid latch-up, the holding voltage of the clamp should be designed to be higher than the power supply voltage with some noise margin. Thus, a diode string was added to

adjust the holding voltage of the clamp. The holding voltage of the clamp is given by:

$$V_h = n * V_{(ON)Diode} + V_{THP} \tag{2.2}$$

Where n is the number of diodes, V_{THP} is the threshold voltage of the PMOS transistor. Under the ESD stress, the voltage at node A is going towards V_{DD}; as a result, the NMOS transistor M_n is turned on that leads to turning on the PMOS transistor M_p. Thus, the positive feedback keeps the clamp turned on for a period of time that is enough to dissipate the ESD stress. The experimental results show that the proposed clamp has larger turn on duration under the ESD stress condition compared with the traditional clamp. In addition, the design has better immunity against mis-trigger or transient-induced latch on event under the fast power-on and transient noise conditions.

In [50], Yeh *et. al.* designed a PMOS capacitor-less based transient ESD clamp that is complimentary to the designs proposed in [48], as PMOS transistor has lower leakage current compared with the NMOS transistor [51]. Fig. 2.10 (b) shows the schematic of the proposed design in which the triggering circuit of this clamp consists of two transistors (M_n and M_p) and two resistances (R_n and R_p), which is similar to the design presented in [48]. However, in this design the PMOS transistor M_{ESD} is used as the main transistor. In addition, the parasitic capacitors of the main transistor along with the resistance R_n are used to realize the RC network of the triggering circuit.

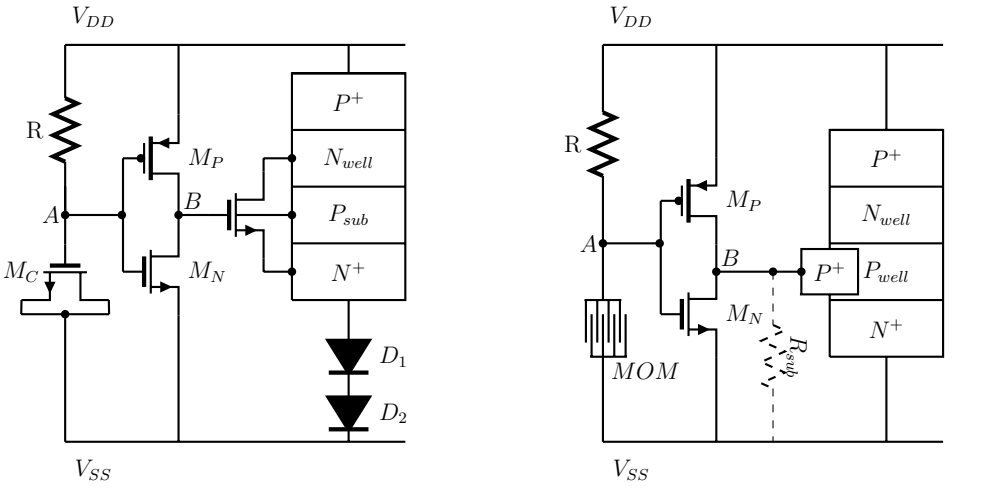
Under the ESD stress, the voltage at node A is going towards V_{SS}; as a result, M_p is on that leads to turning on M_n. Thus, the positive feedback keeps the clump turned on for a period of time that is enough to dissipate the ESD stress. The experimental results show that the proposed clamp has larger turn on duration under the ESD stress condition compared with the traditional clamp. In addition, the design has better immunity against mis-trigger or transient-induced latch up event under the fast power on and transient noise conditions. Furthermore, the experimental results show that the design has lower leakage current compared with the traditional transient clamp and the designs proposed in [48].

2.2.2 SCR based transient ESD clamps

All of the previous work presented in the previous sections has been proposed in older CMOS technologies or in low-power 65 nm CMOS technology. Low-power (LP) and general-purpose (GP) processes are the two commonly used processes in advanced nanoscale CMOS technologies. As LP process is for low-power applications using 1.2 V for core transistors and 2.5 V I/O option, gate leakage current is not a serious issue. Therefore, large MOS transistors are usually used as the clamping element of the ESD clamp. In GP process, on the other hand, the gate oxide thickness of core transistors is reduced compared with LP process counterpart to achieve higher performance designs for high-frequency applications using 1 V core transistors and 2.5 V I/O option. The thinner gate oxide layer results in higher leakage current due to gate tunneling; also, it leads to lower gate oxide breakdown voltage [4]. Therefore, SCR has been used as the clamping element in the implementation of ESD clamps in scaled technologies owing to its superior current carrying capabilities, low leakage, and compact size. The main disadvantage of the SCR is the slower response to an ESD event [52]. Therefore, a triggering circuit is added to speed up the ESD response and different structures have been proposed based on this concept.

In [53], Ker and Lo proposed an SCR based transient clamp as shown in Fig. 2.11 (a). The idea was to reduce the leakage current of the diode based static clamp through adding an NMOS-controlled lateral SCR (NCLSCR) that is triggered by ESD-detection circuit. When an ESD event happens, the ESD-detection circuit, which consists of a capacitor (M_C), resistance (R) and an inverter, triggers the NCLSCR through the NMOS transistor. As a result, there is a path between V_{DD} and V_{SS} and the ESD event is discharged using the NCLSCR and the diode string. On the other hand, when the circuit is operated under normal operating conditions, the NCLSCR is off, and the leakage current of the diode string is reduced. Another SCR based transient clamp was proposed by Chiu and Ker [54] as shown in Fig. 2.11 (b). When an ESD event occurs, the ESD detection circuit triggers the STSCR to discharge the ESD event. However, under normal operating conditions, the MOM capacitor is charged and the voltage at node A is high; as a result, M_N is on, and STSCR is off (no path exists between the two power supply rails).

The simulation shows that reducing the voltage across the MOS capacitor will reduce



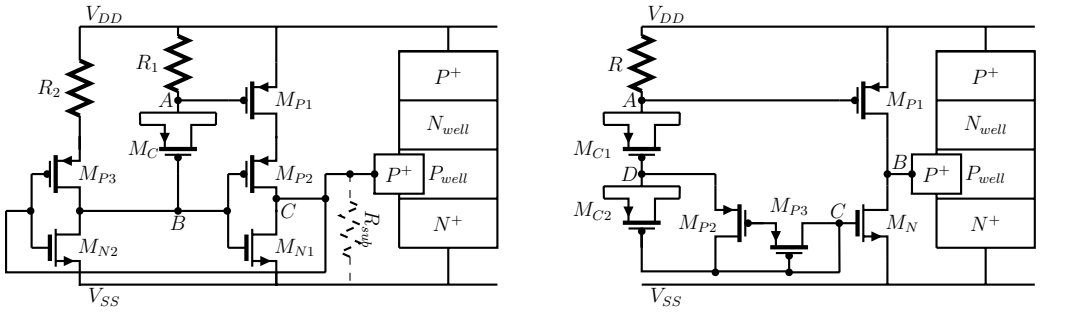
(a) With diode string. (b) With MOM capacitor.

Figure 2.11: SCR based power-rail ESD clamp.

its leakage current. As a consequence, the leakage of the triggering circuit is reduced as capacitances are used as part of the ESD detector circuit [4]. Ker and Chiu [55] proposed the clamp shown in Fig. 2.12 (a) in which there is no leakage due to the MOS capacitor as there is no direct path between the two power rails under normal operating conditions. Under normal operating conditions, the voltage at node A is high leads to turning M_{P1} off and the parasitic resistance R_{sub} pulls node C to ground. Thus, M_{P3} is on and drives node B to V_{DD} that makes M_{P2} completely off and M_{N1} is fully on that helps in keeping the voltage at node C low. Ensuring both nodes A and B are high results in eliminating the leakage caused by the MOS capacitance M_C. During the ESD event, as there is no voltage drop across the MOS capacitor M_C before the event, both M_{P1} and M_{P2} can turn on. Also, the RC network composed of M_C and R_1 reacts to the ESD event and pulls both node A and B low to help to turn M_{P1} and M_{P2} on. Therefore, the SCR is triggered and sinks the ESD current.

In [56], Fig. 2.12 (b), the design utilizes the gate current to bias the triggering circuit and to reduce the voltage across the MOS capacitor. M_N keeps the voltage at node B low, which leads to keeping the SCR off during the normal operating conditions. M_{P1}, on the other hand, is used to trigger the SCR on during the ESD stress, while it is fully off under

normal operating conditions. R, M_{C1} and M_{C2} compose the RC network of the clamp and M_{P2} and M_{P3} are used as a start-up circuit to conduct some gate current through M_{C1}; thus, nodes C and D are high and M_N is on. As a result, the voltage across the MOS capacitance is almost zero and the leakage due to M_{C1} is eliminated during normal operating conditions.

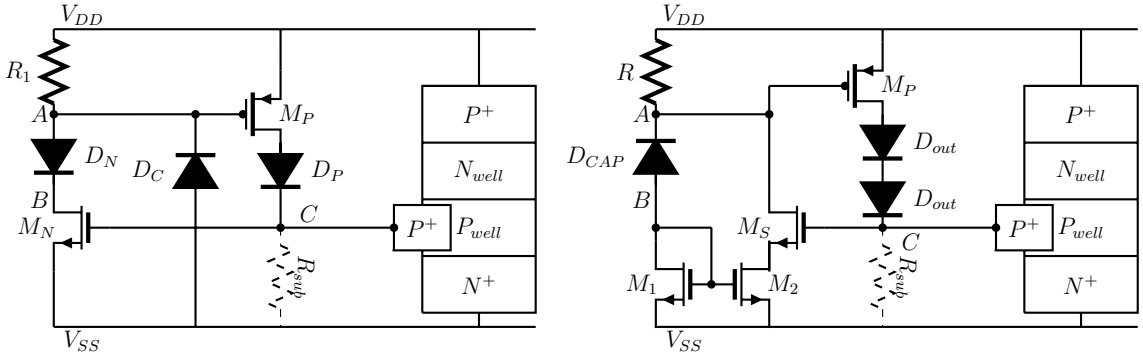


(a) With feedback control inverter 1. (b) With utilization of gate current.

Figure 2.12: SCR based power-rail ESD clamp.

Yeh [50] proposed an ESD clamp using SCR as a clamping element as shown in Fig. 2.13 (a); the triggering was also optimized to reduce the leakage current during normal operating conditions. The RC ESD detector circuit is realized through R_1 resistance and D_C diode as the capacitance. D_N and D_P are used to minimize the voltage at the gate of M_P transistor, which results in reducing the leakage current of the design. Under normal operating conditions, M_P is off, and the parasitic resistance of the SCR R_{sub} keeps the SCR off. When the ESD event happens, the RC network turns M_P on, which triggers the SCR to sink the ESD current. Altoaguirre [52] proposed an ESD clamp shown in Fig. 2.13 (b); the area of this design was optimized using a mathematical analysis and capacitor boosting technique. The RC ESD detector circuit is realized through the resistance R, D_{CAP} diode and the current mirror as the capacitance. The current mirror that is composed of M_1 and M_2 transistor amplifies the total capacitance of the clamp; thus, the total layout area is minimized. During the ESD event, M_P is on due to the voltage drop across the resistance R that triggers the SCR to conduct the ESD current. Under normal operating conditions,

M_P is off, and the SCR is kept off via its parasitic resistance R_{sub}. The diode string and M_S were added to reduce the leakage current.

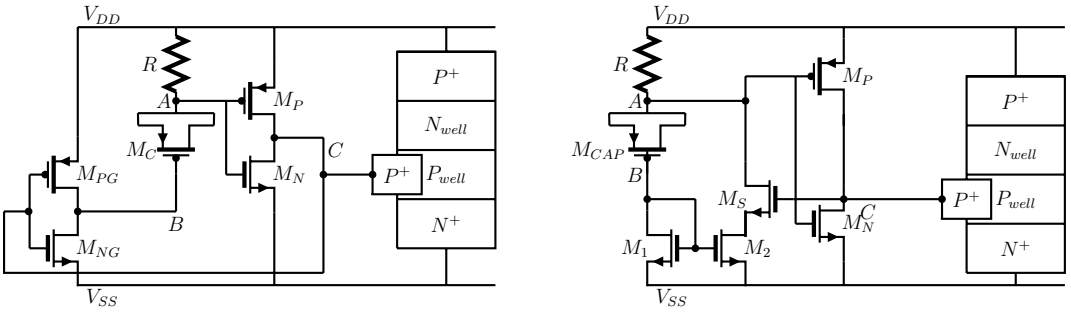


(a) With positive feedback. (b) Using capacitor boosting 1.

Figure 2.13: SCR based power-rail ESD clamp.

Fig. 2.14 (a) presents the design proposed by Altolaguirre [57] in which the voltage across the capacitor M_C is controlled by M_{GP} to minimize the leakage current of the design. Under ESD stress, the voltage drop across R turns M_P on, which triggers the SCR to conduct the ESD current. Under normal operating conditions, the voltage at node A is high, and that make M_P off, and M_N on; thus, the voltage at node C is pulled to ground to keep the SCR off. In [58], an ESD clamp shown in Fig. 2.14 (b) in which a capacitor boosting technique is used as well. During the ESD event, M_P turns on due to the voltage drop across the resistance R that triggers the SCR to conduct the ESD current. Under normal operating conditions, M_P is off, while M_N is on and keeps the SCR off.

Fig. 2.15 shows the design proposed by Yeh [59] in which the low leakage was the primary design criterion. The RC network is realized by the gate to source parasitic resistance of M_P transistor and the junction capacitance of D_C diode. Under the ESD stress, the voltage at node A goes to ground, which turns on M_P transistor and that triggers the SCR. The substrate resistance R_{sub} keeps the clamp off during normal operating conditions. The two diodes D_{P1} and D_{P1} are to reduce the voltage difference across the gate of M_P transistor; as a result, the leakage of the design is reduced.



(a) With feedback control inverter 2.

(b) Using capacitor boosting 2.

Figure 2.14: SCR based power-rail ESD clamp.

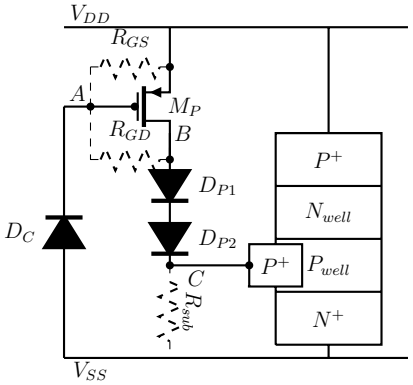


Figure 2.15: SCR based power-rail ESD clamp with resistor-less design with diode string ESD detection.

2.3 Figures of Merit

To evaluate different ESD power supply clamps, some figures of merit are considered and compared. Those figures include:

1. Current carrying capability: The ability to sink current under ESD stress. In this benchmark, the capability of conducting high currents is measured since during the ESD event a large amount of current is being discharged through the ESD circuit in a short period. Therefore, the larger the current that a protection circuit can sink becomes a priority. The current when the voltage across the ESD clamp is 5 V ($I_{@V=5V}$) in TLP testing is chosen as this figure for the purpose of comparison, where a higher value of $I_{@V=5V}$ means better current sinking ability of an ESD power supply clamp.

2. Peak voltage overshoot: The overshoot voltage is highly undesirable since a large voltage overstress can damage the gate oxide. Therefore, the ESD protection against voltage overshoot is better when a low value of this figure is indicated. The peak voltage overshoot should be less than the oxide breakdown ($BVOX_{ESD} = 5\ V$) of the core transistor to ensure robustness against ESD failures. The triggering voltage (V_t) of the ESD clamp under TLP testing is chosen as this figure where a lower value is desired.

3. Leakage current under normal operating conditions: This is an important evaluation of different ESD circuits as most of the time the ESD protection circuits are off and operate under normal operating conditions of the circuit core; as a result, they have some leakage current. Thus, a low value of this figure at different temperatures gives a better leakage performance.

4. Immunity to false triggering: In this test, the immunity to the false triggering is tested through applying a ramp from 0 to V_{DD} with 100 ns rise times. Then, to ensure correct functionality, the ESD power supply clamp should not be triggered by the first power-on case.

5. Immunity to transient-induced latch-up (TLU): In this benchmark, the immunity to TLU is tested by adding $\pm 210\ V$ pulse noise to the power supply V_{DD} under normal operating conditions. Thus, the clamp that does not trigger due to TLU is better. The immunity of the latch-up due to power supply noise can also be considered by ensuring that the holding voltage (V_h) and the triggering voltage (V_t) of an ESD clamp are higher than the supply voltage ($> V_{DD} + 10\%$).

6. On-resistance: The on-resistance (R_{on}) represents the resistance of the ESD clamp while it is on. A small value of R_{on} is desired as the ideal clamp should have a zero R_{on} under the ESD stress.

7. Area consideration: The area of ESD devices varies with the requirement of the protection level as well as the design. To have a fair comparison, the design that has higher ESD protection characteristics along with low-leakage current among all of the proposed ESD power supply clamps with the same area is the best.

In this thesis, these seven criteria are used to compare the proposed designs with each other and with the state-of-the-art designs in 65 nm CMOS technology. Table 2.1 presents figures of merit of the state-of-the-art clamps in general purpose 65 nm CMOS technology. All of the designs published in the general purpose 65 nm CMOS technology have used the SCR as the clamping element since the SCR has a higher current carrying capability compared to an MOS transistor of the same area [3]. The ESD power supply clamp should provide a low-resistive path in both directions to be able to deal with both PSD and NDS zapping modes. The SCR-based design does not provide the best ESD protection for the NDS zapping mode (positive ESD stress at V_{SS} with grounded V_{DD} node) since it has two parasitic resistances (R_{Nwell} and R_{Psub}) and one parasitic diode (the collector to base junction diode of the PNP transistor) in the path from the V_{SS} to V_{DD} rails. Besides, none of the work published in the general purpose 65 nm CMOS technology provided measurement or simulation results for NSD zapping mode. Furthermore, SCR-based designs are not suitable for application that exposed to hot switching or ionizing radiation [2].

As mentioned earlier in this chapter, in GP process, the gate oxide thickness of core transistors is reduced compared with LP process counterpart to achieve higher performance

Design	area (μm^2)	Leakage current (nA)			I_{t2} (A)	$I_{@V=5V}$ (A)	V_t (V)	V_h (A)	R_{on} (Ω)
		25^oC	75^oC	125^oC					
[52]	765	80	200	1080	2.25	1.75	4	2	2.66
[54]	3375	358	500	1810	2.5	1.5	3	2.5	2.86
[55]	-	116	350	1080	5	2.25	5	2	2.44
[58]	2025	165	-	1110	2.3	0.6	3	2.5	6.29
[59]	1051	1.43	-	-	2.74	2.1	3.86	2	1.77
[60]	1530	16.2	-	680	2.64	1.8	3.79	2	2

Table 2.1: Figures of Merit of the state-of-the-art clamps in 65 nm CMOS technology.

designs for high-frequency applications using 1 V core transistors and 2.5 V I/O option. The thinner gate oxide layer results in higher leakage current due to gate tunneling; also, it leads to lower gate oxide breakdown voltage [4]. Therefore, using large thin oxide MOS transistors as clamping elements will results in a huge leakage current; recall the example provided in section 1.3, where the leakage of the ESD clamps is about 12.8 % of the total leakage current of the entire design.

In the next two chapters, four power supply ESD clamps are proposed in which thick oxide MOS transistors are used as the main clamping element. Therefore, low-leakage current feature is achieved without significantly degrading the ESD performance. In addition, the parasitic diode of the MOS transistors provides the protection against NSD-mode.

Chapter 3

Standalone ESD Power Supply Clamps

This Chapter presents both PMOS ESD power supply clamp with thyristor delay element (PTC), and diode triggered power supply (DTC). In all of the proposed designs, the main target was to optimize the designs for having the lowest possible leakage current without degrading the ESD protection ability.

3.1 Design specifications and decisions

To ensure that the proposed designs have adequate characteristics those described in Chapter 2, Table 3.1 presents the specifications those should be met for the proposed designs. Under normal operating conditions, the ESD clamp should have a very low-leakage current as the clamp most of the time operates under normal operating conditions of the circuit core. In addition, the ESD clamp should be immune against latch-up due to noise at the power supply rails or due to ESD event. The latch-up presents the case where the clamp turns on due to noise at the power supply rail or stays on after the ESD stress ends.

Under the ESD stress, it is required that the ESD clamp reacts fast to the ESD event and stays on the entire ESD event. As shown in Chapter 1 Fig. 1.7, the CDM has the

fastest rising time of $100 - 500\ ps$, it is essential for the clamp to effectively react fast to the CDM stress so that the voltage across the clamp is limited to be below the breakdown voltage of the circuit core ($BVOX_{ESD} = 5\ V$). On the other hand, the entire duration of the HBM stress is approximately $600 - 750\ ns$; thus, the clamps should be on for more than $600\ ns$. Lastly, to ensure that the clamps do not falsely trigger and to protect the circuit core, the triggering voltage should be within the ESD design window ($1.2\ V < V_t < 5\ V$).

Design specifications		Criterion	Reason
Under normal operating conditions	Leakage	Minimum	To minimize the impact of of ESD clamp on circuit core
	Latch-up	Immune	
Under ESD stress	V_P (CDM)	$< 5\ V$	To protect the circuit core
	On-time	$> 500\ ns$	To stay on for the entire HBM
	Triggering voltage (V_t)	$1.2V < V_t < 5V$	To protect the circuit core and to avoid latch-up

Table 3.1: The specifications to be met for the proposed designs.

The first step in the design procedure was to investigate the leakage current and the current carrying capability of all transistors available in the TSMC 65 nm CMOS technology. As the MOS transistors are used as the clamping element of the proposed designs, and as large MOS transistors are needed to be able to carry the high current of an ESD event, the leakage current of different gate oxide transistors was investigated in general purpose TSMC 65 nm CMOS technology. Fig. 3.1 shows the leakage current for both thin oxide and thick oxide transistors as a function of the transistor width. These simulations were carried out with $V_{GS} = 0\ V$, and $V_{DS} = V_{DD}$, and the channel length for the four investigated transistors was $L = 350\ nm$. It is clear from this figure that thick oxide gate NMOS transistor has the lowest leakage among the investigated transistors. The thick oxide transistors have a gate oxide that is almost three times the thickness of the oxide of the thin oxide transistor. Thus, their leakage current is about nine thousand times lower than the leakage of the thin gate oxide transistor, while its current carrying capability is three times less compared to thin oxide counterpart. As a result, the overall gain of using

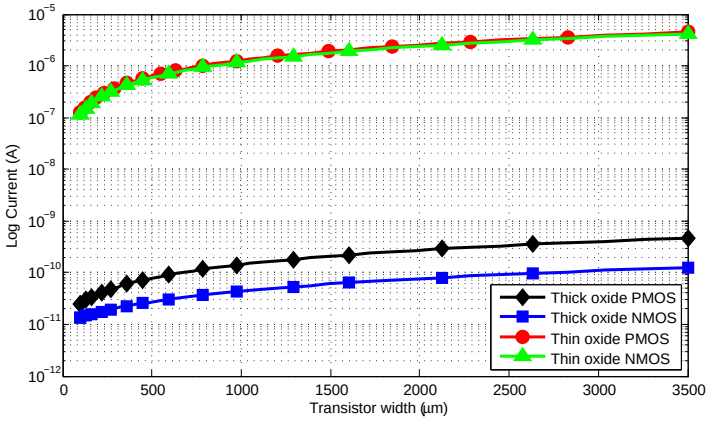
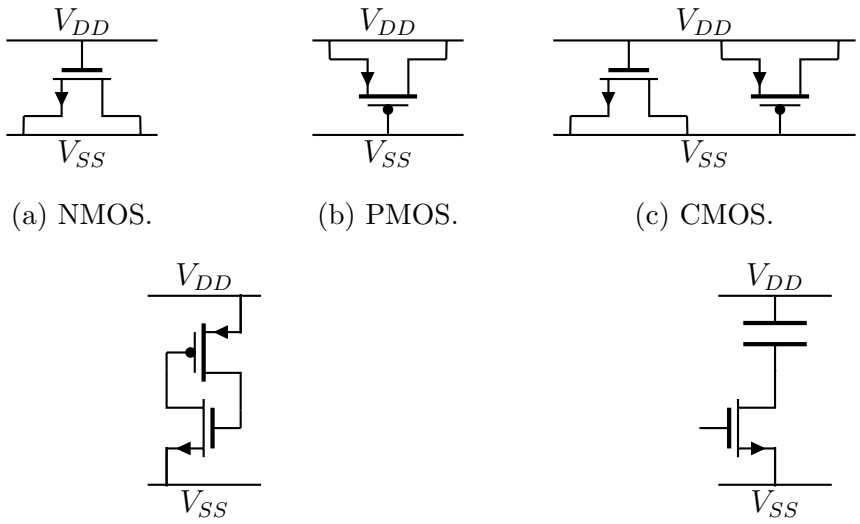


Figure 3.1: The simulated leakage of transistors in 65 nm CMOS technology.

thick oxide transistors is about 3000 x. Therefore, the thick gate oxide transistors were used as the clamping element for all of the proposed designs.

Once the thick oxide transistor has been selected to be used as the clamping transistor, the next step is to optimize the other components of the clamps in order to reduce the leakage. As mentioned in Chapter 2, capacitances and resistances are used to form the RC triggering circuit of the transient clamp and their time constant is usually set to 40 ns to distinguish between the first power-on condition and the ESD event. With this value of the time constant, the RC network can be a potential source of the leakage current and optimizing it to minimize the leakage is the next step of the design procedure. There are many ways to realize a capacitor in CMOS technology such as MOS-based capacitors, metal-oxide-metal (MOM) capacitors, and metal-insulator-metal (MIM) capacitors as shown in Fig. 3.2. The MOM are usually fabricated using oxide to separate two metal traces in the same metal layer, whereas MIM is usually fabricated using insulator to separate two metal traces in two different metal layers [12]. T. Charania *et. al.* [61] investigated different methods of implementing on-chip capacitors in in GP TSMC 65 nm CMOS technology. Different capacitances with the same capacitance value of 500 fF were fabricated and compared. Fig. 3.3 shows the leakage current of the fabricated capacitors as well as the effective capacitance per unit area at 10 GHz, while Fig. 3.4 presents the effective capacitance per unit area as a function of the operating frequency.



(a) NMOS. (b) PMOS. (c) CMOS.

(d) Back to Back (B2B). (e) Gated NMOS (Gated).

Figure 3.2: Capacitor realization in CMOS technology.

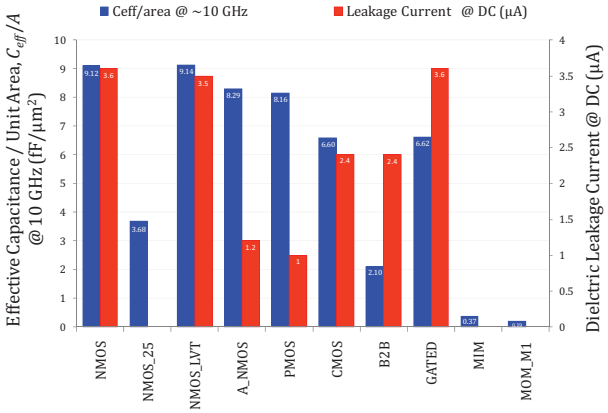


Figure 3.3: Effective capacitance per unit area (at 10 GHz) and leakage current (at DC) for different capacitors in GP 65 nm CMOS technology [12].

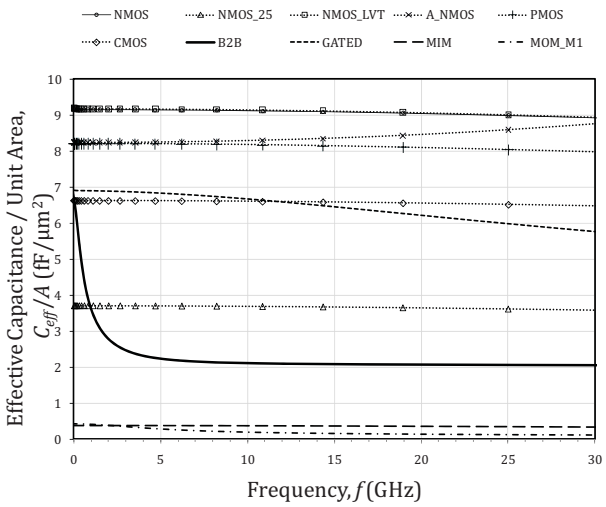


Figure 3.4: Effective capacitance as a function of operating frequency in GP 65 nm CMOS technology [12].

Based on the results presented in Fig. 3.3, the MOS-based capacitors with thin gate oxide (in Fig 3.3: NMOS, $NMOS\_LVT$, A_NMOS, PMOS, CMOS, and gated) have the highest capacitance per unit area; however, they have significantly high leakage current. On the other hand, MIM capacitors, MOM capacitors and thick oxide NMOS capacitors ($NMOS\_25$) have negligible leakage current. The thick oxide NMOS capacitor has the highest capacitance per unit area among the three low-leakage capacitors [61]. Fig. 3.4 clearly shows that the thick oxide NMOS capacitor ($NMOS\_25$) has a constant effective capacitance in the frequency range from DC up to 30 GHz [61]. Therefore, the thick oxide NMOS implementation was used to realize the capacitance of the RC network for all of the presented designs in this work as it has the lowest leakage current and the best capacitance per area among the low-leakage capacitances in the GP TSMC 65 nm CMOS technology. The capacitance was set to 500 fF for all proposed transient clamps.

As a resistor is needed to form the RC triggering circuit of the transient clamp, all available resistors in the GP TSMC 65 nm CMOS technology have been investigated to get the smallest layout possible for the resistance. The P^+ poly without salicide ($rppolywo$) offers the highest sheet resistance (sheet resistance of 756.206 Ω per square) in the GP TSMC 65 nm CMOS technology. Even though, the diffusion resistance implementation

provides more stable resistivity with lower sheet resistance. The RC time constant was set to 40 ns, while the slowest ESD event, MM stress, has a rise time of 15 ns. The P^+ poly without salicide has been selected to realize the resistor in all of the proposed designs as the time constant of the RC network can tolerate the variation of the resistivity. The resistance was set to 80 $k\Omega$ for all proposed transient clamps.

3.2 PMOS based ESD power clamp with thyristor delay element (PTC)

One of the challenges in the design of transient clamps is to implement an optimum delay element that keeps the main transistor on during the entire ESD event. Thus, a novel ESD clamp circuit is proposed in which a CMOS thyristor circuit is used as the delay element. It has been reported that a delay in the range of a few nanoseconds to millisecond range can be obtained by the CMOS thyristor with low sensitivity to environmental conditions and low static power consumption [62]. The proposed PMOS based ESD power supply clamp with thyristor delay element (PTC) is shown in Fig. 3.5, and table 3.2 summarizes the sizes of the elements. PMOS thick oxide transistor was selected as the main clamping element despite having slightly higher leakage current compared with NMOS counterpart. However, PMOS transistor has $10-15$ % lower triggering voltage compared with an NMOS transistor of equal dimensions; as a result, PMOS transistor turns on faster than NMOS transistor.

Under normal operating conditions, the capacitor M_C is fully charged and the voltage at node A is low. Thus, the transistor M_3 is on, and the voltage of node B is high, which keeps the main transistor M_{ESD} off. Under the ESD event, the voltage of node A becomes high; and as a consequence, both transistors of the CMOS thyristor are on, pulling the voltage of node B to V_{SS} and turning on the main transistor M_{ESD}. Even though, the time constant of R and M_C is low, the CMOS thyristor works as a delay element and keeps the main transistor M_{ESD} on for a period of time more than 1 μs. The main transistor (M_{ESD}) was sized to ensure that the peak voltage is below 5 V under the ± 125 V CDM ESD stress. All transistors used in the proposed design are thick oxide transistors. M_1

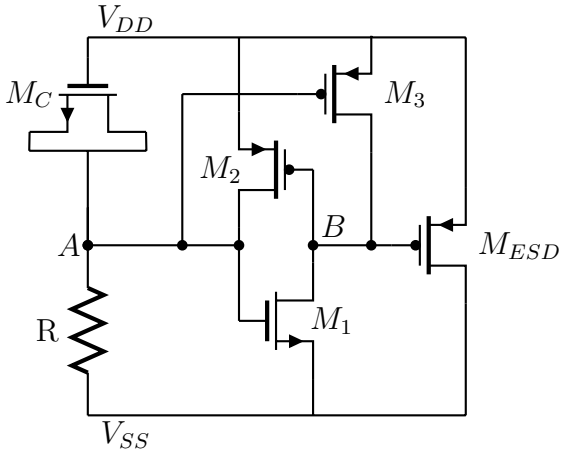


Figure 3.5: PMOS ESD clamp with thyristor delay element (PTC).

was designed large to be able to pull node B to V_{SS} as fast as possible, which leads to a faster response to the ESD stress.

Element	Type	Length (μm)	Total width (μm)	number of fingers
M_{ESD}	PMOS	0.28	2400	60
M_1	NMOS	0.28	7	1
M_2	PMOS	0.28	2	1
M_3	PMOS	0.28	0.4	1
M_C	NMOS	1	82.44	6
R	rppolywo	25	7.7	5

Table 3.2: The size of the elements used in the PTC design.

3.2.1 ESD simulation results

3.2.1.1 HBM ESD stress simulation setup and results

The proposed clamps were simulated under $\pm 1.5\ kV$ HBM stress using the HBM test defined in the Military standard (Method 3015.8) [19]. Fig. 3.6 shows the HBM test setup that was used to simulate the proposed clamps. A transient simulation was carried out and the switches shown in Fig. 3.6 are controlled by pulse signal. The switches have a very low resistance while they are on ($1\ m\Omega$) and a very large resistance while they are off ($1\ T\Omega$). All designs were simulated at the schematic level as the designs composed of large devices; as a result, the impact of the interconnects on the performance is negligible. In addition, the proposed designs were tested at the lab under both ESD stress and normal operating conditions; therefore, post layout simulations were not carried out for all designs. The proposed clamps were simulated in both directions, i.e. the HBM stress was applied to the V_{DD} node of the clamp with grounded V_{SS} node (positive HBM stress) and to V_{SS} node of the clamp with grounded V_{DD} node (negative HBM stress). The ESD stress was applied in both directions to ensure that the proposed clamps are capable of protecting the circuit core in both directions through limiting the voltage across it to less than $5\ V$.

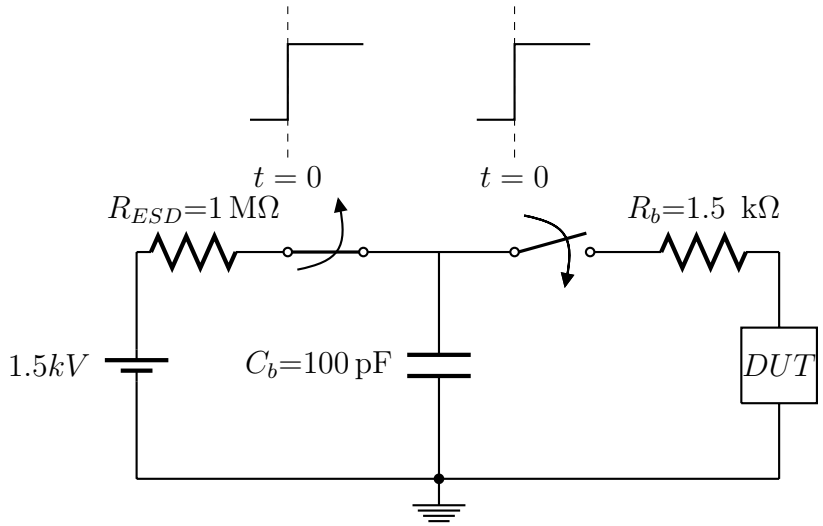
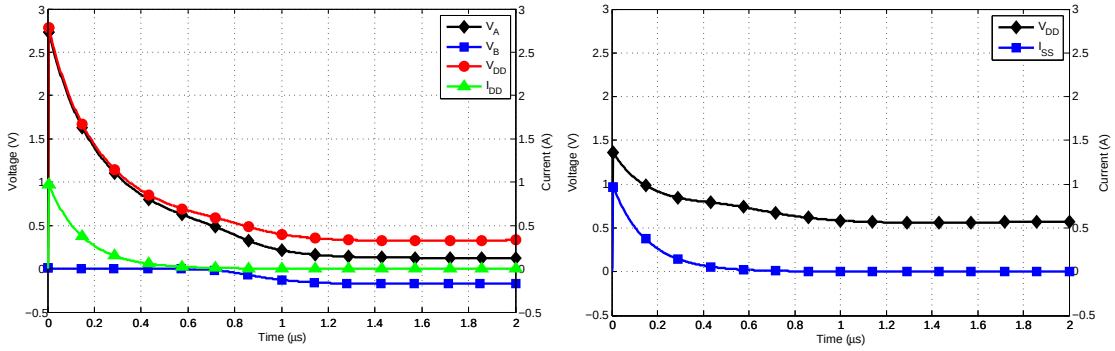


Figure 3.6: The HBM simulation setup based on Military standard (Method 3015.8).

Fig. 3.7 (a) presents the PTC design under the positive HBM stress, while Fig. 3.7 (b) presents the PTC design under the negative HBM stress. It can be seen in Fig. 3.7 (a), the thyristor delay element keeps the voltage of node B low to keep the main transistor M_{ESD} on for long enough time to safely discharge the complete ESD stress. Based on the HBM response presented in Fig. 3.7, it can be concluded that the clamp is capable of protecting the circuit core against $\pm 1.5\ kV$ HBM stress as the peak voltage was limited to 2.78 V in the positive HBM stress and 1.37 V in the negative HBM stress.



(a) HBM stress = 1.5 kV. (b) HBM stress = -1.5 kV.

Figure 3.7: Simulating the PTC design under $\pm 1.5\ kV$ HBM stress.

3.2.1.2 CDM ESD stress simulation setup and results

The proposed clamps were also simulated under $\pm 125\ V$ CDM stress using the CDM Class A test specified by the JEDEC standard [10]. Fig. 3.8 shows the CDM test setup that was used to simulate the proposed clamps. As in HBM simulation, the proposed clamps in this Chapter were simulated in both directions under the $\pm 125\ V$ CDM stress to ensure that the proposed clamps can protect the circuit core against positive and negative CDM stresses. Fig. 3.9 (a) shows the PTC design under the positive CDM stress, while Fig. 3.9 (b) shows the PTC design under the negative CDM stress.

It can be concluded from Fig. 3.9 that the PTC clamp is able to protect the circuit core against a $\pm 125\ V$ CDM stress as the peak voltage was limited to 4.9 V in the positive CDM stress and to 1.3 V in the negative CDM stress.

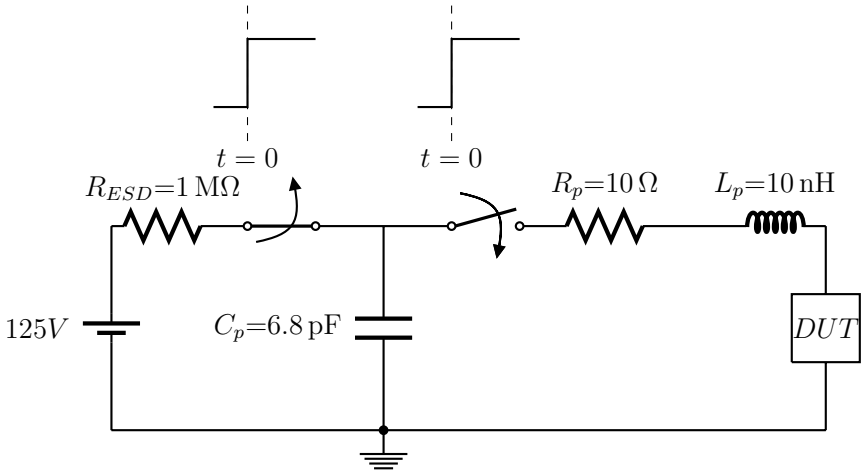
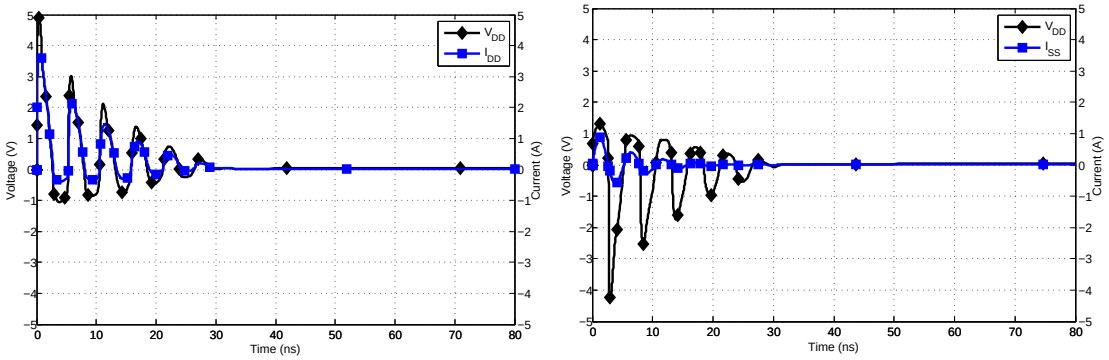


Figure 3.8: The CDM simulation setup based on JEDEC standard.



(a) CDM stress = 125 V.

(b) CDM stress = - 125 V.

Figure 3.9: Simulating the PTC design under ±125 V CDM stress.

3.2.2 Normal operating conditions simulations

3.2.2.1 Immunity to false triggering

The proposed clamps were simulated under normal operating conditions as well. The first power-on condition was simulated by applying a 1 V voltage with a 100 ns rise time to V_{DD} node with grounded V_{SS} node. The voltage of different nodes for the first power-on of the PTC clamp as well as the current flowing in the PTC clamp (I_{DD}) are shown in Fig. 3.10. It can be seen in Fig. 3.10 that the voltage of node A rises to 200 mV only, while the voltage of node B follows the power supply voltage most of the time. In addition, I_{DD} goes to only 7 μA then it goes back to the leakage current range. Thus, the PTC clamp does not trigger after a very fast power-on (100 ns rises time) and this design is robust against false triggering.

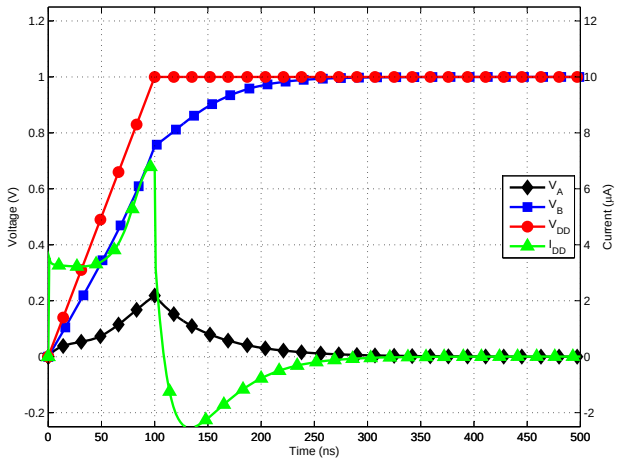


Figure 3.10: Simulating the PTC design under 100 ns power-on condition.

3.2.2.2 Immunity to power supply noise

The immunity to power supply noise was studied by adding a sinusoidal signal with a wide frequency range starting with near DC up to 3 GHz and amplitude of 200 mV to the power supply node with grounded V_{SS} node. A typical power supply noise of $5-10\%$ is

considered for such analysis [63]. However, in this analysis, we simulated a higher power supply noise of up to 20%. An example of a noise signal with a frequency of 1 GHz is shown in Fig. 3.11. The figure illustrates simulations results showing the voltage at node B of the clamp and the V_{DD} node. It is apparent that the voltage of node B stays higher than 850 mV, which is high enough to keep the main transistor off. As a result, the clamp is robust against the power supply noise.

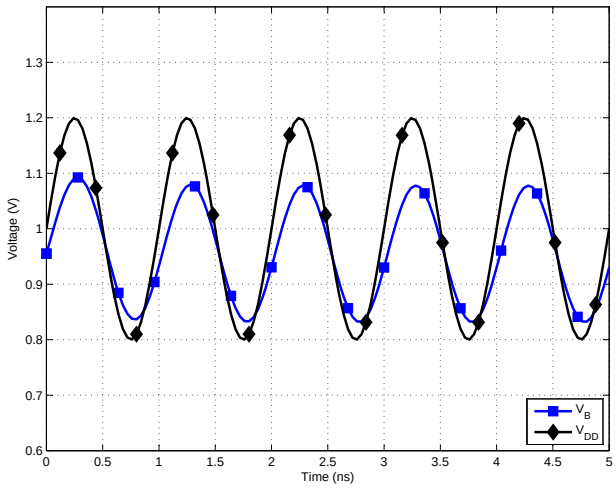


Figure 3.11: Simulating the PTC design under 20% power supply noise.

3.2.3 Measurement results

Fig. 3.12 shows the layout of the PTC clamp. The total layout area of the PTC clamp is 75 μm x 47.36 μm. This section provides the measurements that were carried out to verify the PTC clamp under both ESD condition and normal operating conditions.

3.2.3.1 ESD performance

3.2.3.1.1 Turn on verification: The turn-on mechanism of the proposed clamps was verified under both the chip not powered and chip powered conditions. The chip not powered condition was carried out to observe the turn-on efficiency of the proposed clamps.

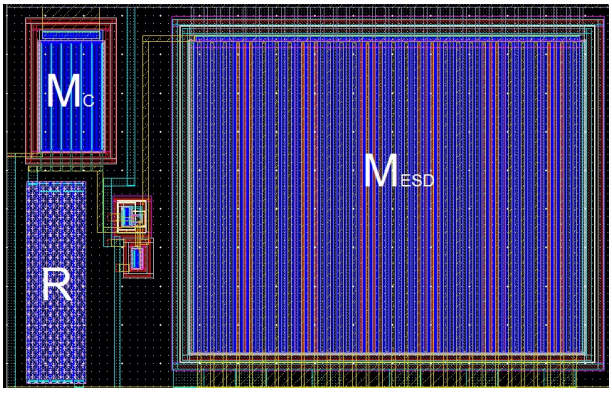


Figure 3.12: The layout of the *PTC* design.

The chip powered condition, on contrary, was carried out to check latch-up issues [49]. In both cases, a 4 V ESD-like pulse voltage with 20 ns rise time and a width of T_W was applied to V_{DD} node with grounded V_{SS}. Fig. 3.13 shows the measurement setup of the test. In this figure, the voltage before and after applying the pulse (V_A) was 1 V under the chip powered condition and 0 V under the chip not powered condition. The Agilent 33210A function generator [64] was used to generate the pulse and then the voltage across the clamp and the current flowing in it were monitored.

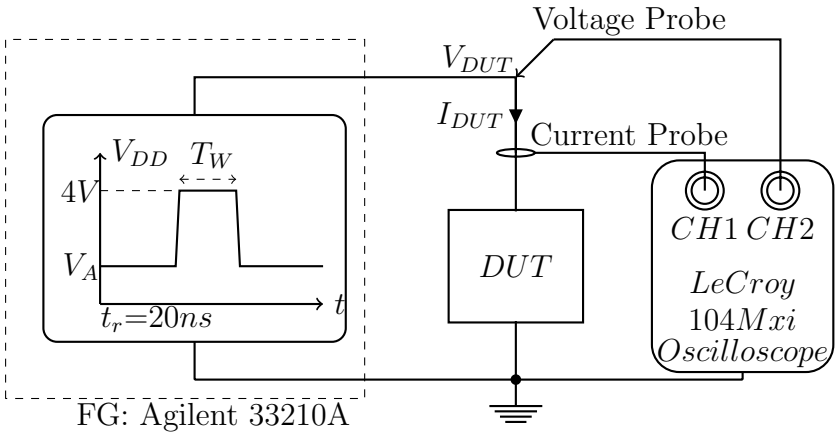


Figure 3.13: The setup for turn-on verification measurement.

- Chip not powered: The main purpose of this test is to ensure that the proposed clamps stays on for the entire HBM stress; thus, the pulse width was set to $T_W = 500$ ns. Fig 3.14 presents measurement results of the chip not powered case. Fig. 3.14

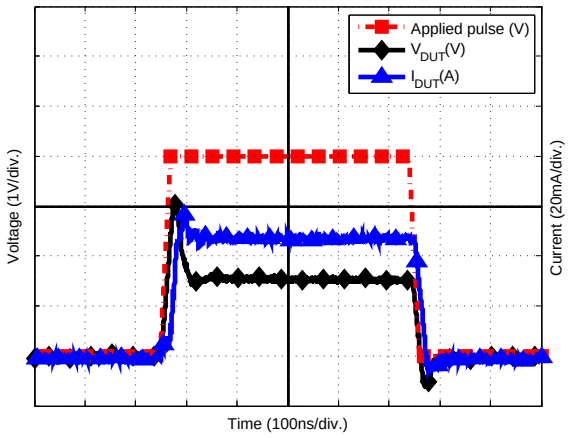


Figure 3.14: Turn-on verification of PTC clamp under not powered condition.

shows that the PTC design stays on for the entire pulse duration. After the pulse ends the current I_{DUT} flowing through the clamp returns to zero. The PTC clamp conducts about 50 mA and the voltage at V_{DD} node is limited to only 1.5 V under the 4 V ESD-like pulse voltage.

- Chip powered: A pulse width of 100 ns was used in this case as the goal of this test is to ensure that the proposed clamps do not stay on after an ESD event. As shown in Fig. 3.15, the PTC clamps was triggered by the voltage stress and the average current going through the clamp I_{DUT} is about 50 mA. However, the PTC clamp is turned off after the stress ends, and the I_{DUT} goes back to the leakage current level. The powered condition confirms that the PTC clamp does not latch-up due to an ESD-like event as it turns off once the ESD-like event ends.

  The PTC clamp reacts to the ESD-like event under both chip not powered and chip powered and after the stress ends the clamp turns off and under both cases the average current going through the PTC clamp I_{DUT} is about 50 mA.

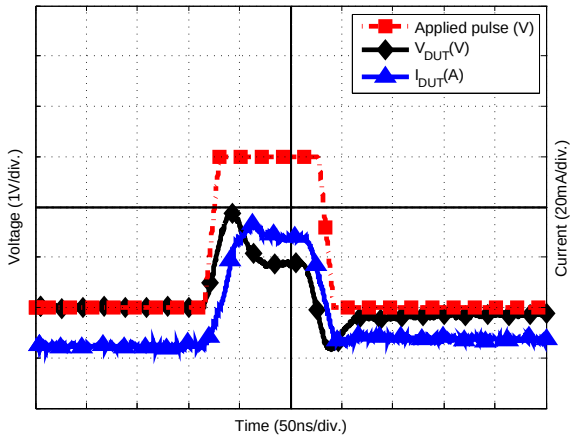


Figure 3.15: Turn-on verification of *PTC* design under powered condition.

3.2.3.1.2 TLP measurement: As mentioned in section 1.5.3, TLP measurement is widely used in the industry to characterize the ESD protection circuits as it offers a reliable, repeatable and nondestructive means for ESD circuits. Also, TLP with a pulse width of 100 ns initiates the same junction damage at the same peak current as the HBM stress [1]. A TLP system generates a pulse that has 10 ns rise time and a width of 100 ns. The amplitude of the pulses is gradually increased till the clamp fails. After each pulse, the leakage current of the clamp is measured to check if the design has failed or not. A clamp is considered failed when its leakage current significantly increases [21]. The Pulsar 900 TLP system from SQP products [65] was used to carry out the TLP measurements for all proposed designs. Fig. 3.16 shows the setup for TLP measurement, and Fig. 3.17 presents the TLP results of the *PTC* clamp. The *PTC* design is capable of handling 3.82 A of current, while its leakage is only 494 pA under 1 V supply at room temperature. As the five volts oxide breakdown ($BVOX_{ESD}$) of the circuit core transistors sets the limit of the ESD protection for an IC in the GP 65 nm technology, the current at 5 V ($I_{@V=5V}$) becomes an important figure of merit to compare the proposed designs against the-state-of-art ESD power supply clamps. $I_{@V=5V}$ shows the actual current carrying capability as long as the device failure happens when the voltage is higher than 5 V. From Fig. 3.17, $I_{@V=5V}$ of the *PTC* clamp is 1.6 A, which can result in HBM failure threshold level of 2.4 kV. The *PTC* clamp has an on-resistance (R_{ON}) of 2.63 Ω.

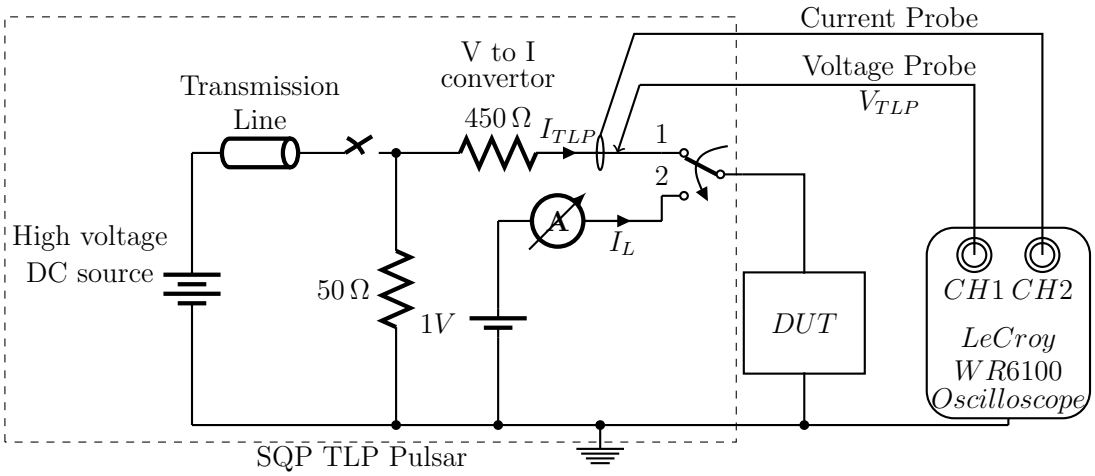


Figure 3.16: The setup for TLP measurement.

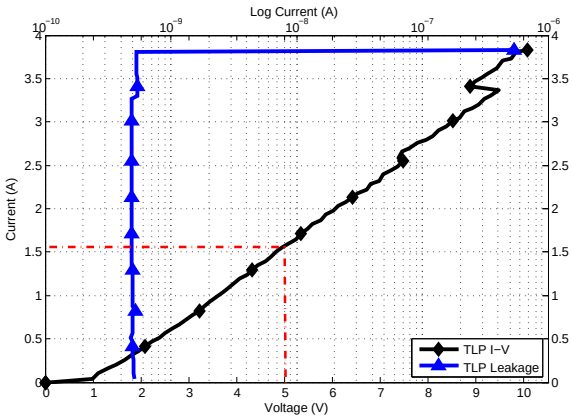


Figure 3.17: TLP measurement results of the *PTC* clamp.

3.2.3.1.3 HBM and CDM measurements: Subsequently, the proposed clamps were also subjected to HBM and CDM testing. These measurements were carried out by Evans Analytical Group (EAG) labs [66] using $JEDECJS-001$ standard [5] for HBM measurements and the $JESD22-C101F$ [22] for the CDM measurements. For both measurements, the leakage current was traced before and after each zapping and the clamp is considered failed if the leakage current significantly increases after the zapping. Positive as well as negative HBM stresses with 250 V step sizes were applied to the V_{DD} of the proposed clamps while the V_{SS} node is grounded. The PTC clamp passes both $+3.25$ kV and -1.75 kV HBM stresses, but fails to pass $+3.5$ kV and -2 kV HBM stresses.

For CDM measurement, the packed chip with the proposed clamps was charged to both positive and negative voltages with 50 V step sizes. Subsequently, for the positive CDM stress, the V_{SS} node is grounded to zap the CDM event. Similarly, for the negative CDM stress the V_{DD} node is grounded to zap the CDM event. The PTC clamp passes $+800$ V and -550 V CDM stresses, but it fails to pass $+850$ V and -600 V CDM stresses.

3.2.3.2 Normal operating conditions

3.2.3.2.1 Immunity to false triggering: Fig. 3.18 shows the setup used to check the immunity against false triggering of the proposed clamps. The proposed clamps were also tested using the Agilent $33210A$ function generator [64] by mimicking the fast power-on with a rise time of 100 ns and a voltage peak of 1 V. Both the voltage across the proposed clamps and the current flowing in them were monitored.

Fig. 3.19 presents the first power-on condition of the PTC clamp in which it can be seen that the PTC design does not falsely trigger due to the fast power-on condition. The PTC clamp does not trigger on as the current (I_{DUT}) increases to 600 μA then it goes back to the leakage current level. Thus, the PTC clamp is robust against the false triggering due to the first power-on condition.

3.2.3.2.2 Leakage vs. temperature: As the clamp most of the time is operated at different temperatures not only at the room temperature, the leakage of the proposed clamps was measured at various temperatures. Fig. 3.20 shows the setup that has been

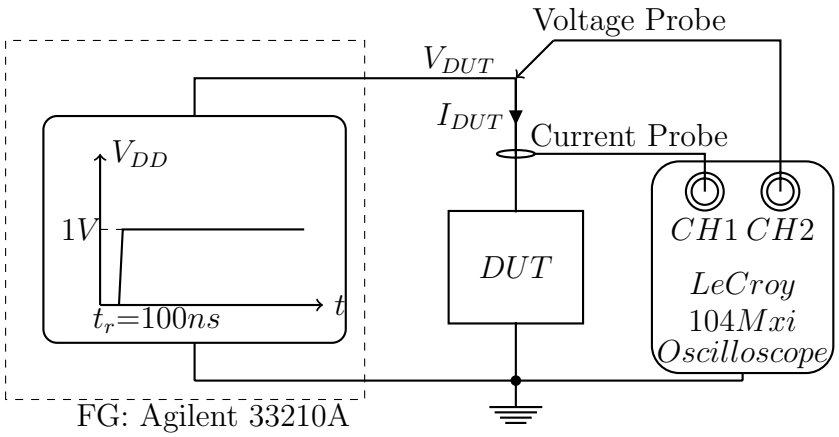


Figure 3.18: The setup for false triggering measurement.

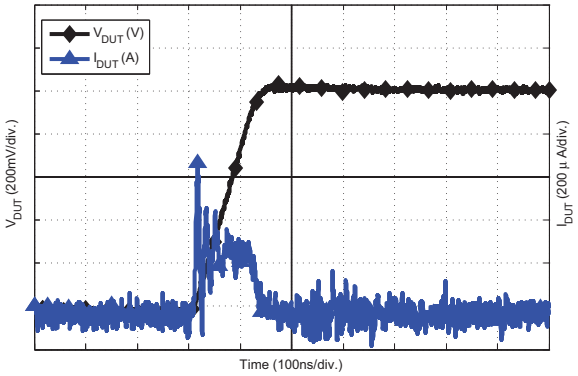


Figure 3.19: The proposed under a first power-on condition.

used to obtain the leakage current of the proposed clamps at different temperatures. The Pulsar 900 TLP system [65] was used to measure the leakage current, while the ESPEC temperature chamber [67] was used to control the ambient temperature. The ESPEC temperature chamber can control the ambient temperature from -40^oC to 80^oC. Fig. 3.21 shows the leakage current of the PTC design as a function of the temperature. As ESPEC chamber limits the measurement to the maximum temperature of 80^oC, the simulated leakage current of the PTC design is shown up to 125^oC in the figure. Since the measured and simulated values are very close in the 25^oC to 80^oC range, it is expected the simulated values outside this range to be similar to the actual leakage currents. Based on the measurement results, the PTC clamp has a leakage current of 494 pA, and 13.4 nA at 25^oC and 75^oC, respectively.

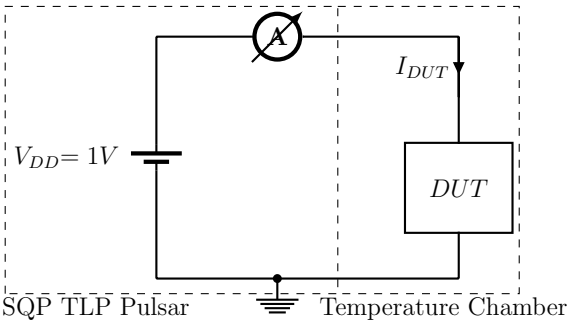


Figure 3.20: The leakage vs. temperature measurement setup.

3.2.3.2.3 Immunity to transient induced latch-up: Transient-induced latch-up (TLU) test is the technique to investigate the vulnerability of an ESD protection device to the transient noise in the power rails under normal operating conditions. The TLU measurement setup at the component-level can precisely simulate the ESD-induced noise on the power rails under system-level ESD test [68]. Fig. 3.22 shows the measurement setup for TLU test. Two different polarities are usually used for the charging voltage: positive charging voltage ($V_{charge} > 0$) and negative charging voltage ($V_{charge} < 0$). The positive (negative) can cause the ESD device to be triggered through positive-going (negative-going) bipolar trigger noises on the V_{DD} node of device [13]. The proposed clamp was

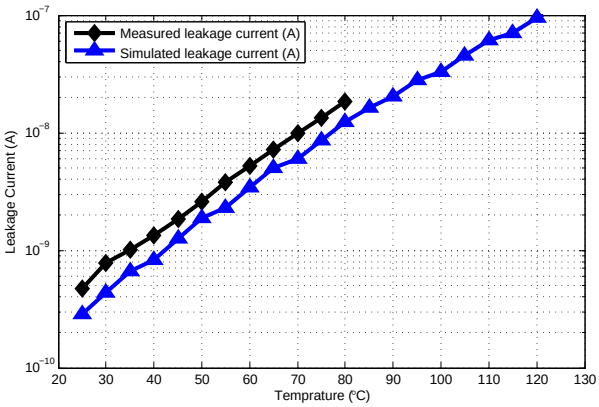


Figure 3.21: The measurement result of leakage vs. temperature for PTC clamp.

biased to ensure that the voltage at V_{DD} node is 1 V. The noise trigger source was directly connected to the proposed designs as shown in Fig. 3.22. The current-limiting circuit was added to protect the proposed clamps against the electrical-over-stress (EOS) damage under a high-current latch-up state and to limit the current going to the DC power supply [13]. The TLP system was used to generate the charging voltage. The TLP system limits the charging voltage only to ± 210 V. Thus, the measurements were limited to ± 210 V.

Fig. 3.23 (a) presents the PTC design under a positive transient-induced latch-up with V_{charge} of $+210$ V, while Fig. 3.23 (b) presents the PTC design under a negative transient-induced latch-up with V_{charge} of -210 V. Fig. 3.23 clearly shows that the PTC design is robust against latch-up due to transient-induced noise with V_{charge} ± 210 V as the current (I_{DUT}) goes back to the leakage current level once the transient-induced noise ends.

3.3 Diode triggered static power supply clamp with delay element (DTC)

Fig. 3.24 illustrates the proposed static power supply clamp with a delay element. In order to keep leakage currents low, thick gate oxide transistors were used for all transistors. The

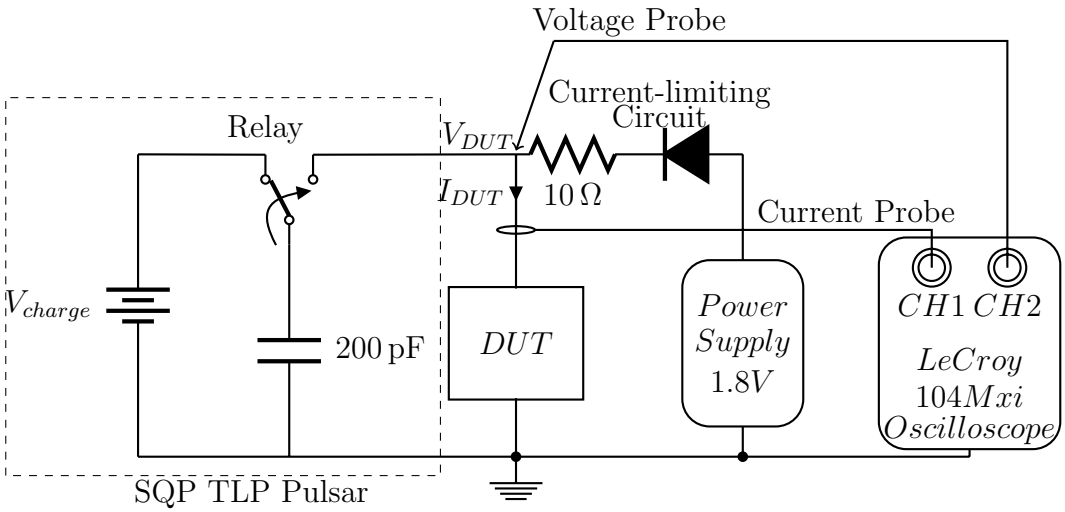
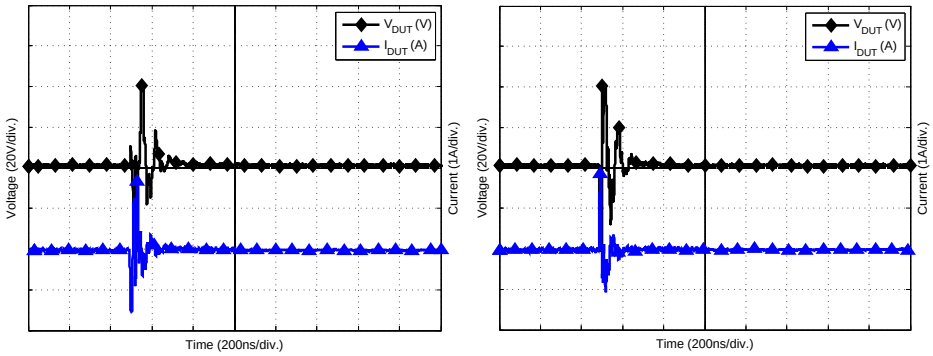


Figure 3.22: The setup for TLU measurement [13].



(a) V_{charge} = 210 V. (b) V_{charge} = - 210 V.

Figure 3.23: The PTC design under TLU with different V_{charge}.

thick oxide transistor has a gate oxide that is almost three times the thickness of the normal transistor. As a result, the thick gate oxide transistor has lower leakage current compared with their counterparts; however, it results in slow ESD response. To speed up the ESD response, the design takes advantage of the fast rise time of the voltage at the V_{DD} node during the ESD event to quickly turn on the main transistor M_{ESD} through the two diodes (D_1 and D_2). As a result, the clamp exhibits desirable features such as low-leakage and fast response time. Under normal operating conditions, the voltage at the V_{DD} node is 1 V; therefore, the two diodes are off. Also, M_4 is on; thus, the voltage at node A is high, which makes M_3 on to keep M_{ESD} off. The transistor M_4 was added to make sure that the voltage at node A is high so that the thyristor that consists of M_1 and M_2 does not turn on.

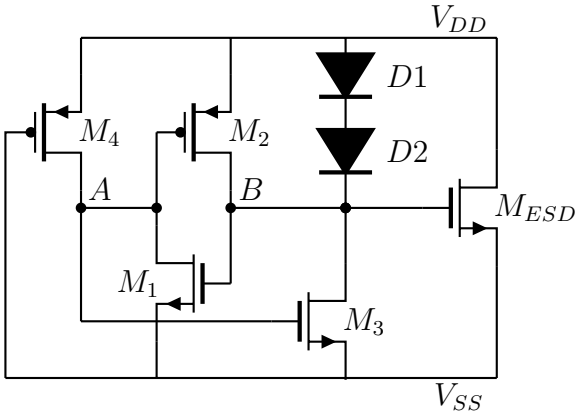


Figure 3.24: Diode triggered Clamp (DTC).

Under the ESD event, the voltage at the V_{DD} node is higher than the triggering voltage of the diode string (1.4 V); thus, the voltage at node B becomes high and turns the main transistor M_{ESD} on. In addition, as the voltage at node B is high, the thyristor is on and keeps the voltage at node B high for enough time to sink the ESD event. On the other hand, M_4 is on and is trying to turn off the main transistor through turning M_3 on also by pulling up the voltage at node A. This case was addressed by designing both M_1 and M_2 to be larger, stronger, than M_3 and M_4 to ensure that the voltage at node B is kept high for enough time to safely dissipate the ESD stress. Simulation results in Fig. 3.26

further illustrate the transient response of the clamp under a +1.5 kV HBM stress. The main transistor (M_{ESD}) was sized to ensure that the peak voltage is below 5 V under the ±125 V CDM ESD stress. Table 3.3 summarizes the sizes of the transistors.

Element	Type	Length (nm)	Total width (μm)	number of fingers
M_{ESD}	NMOS	300	2000	50
M_1	NMOS	280	4	1
M_2	PMOS	280	24	3
M_3	NMOS	280	0.4	1
M_4	PMOS	280	0.6	1
D_1, D_2	pdio	240	0.24	–

Table 3.3: The size of the transistors used in the DTC design.

3.3.1 ESD simulation results

3.3.1.1 HBM ESD stress simulation results

In the traditional static clamp (TSC) shown in Fig. 2.2 (c) , the value of resistor R is critical and should be chosen carefully. A small value of R will lead to improved robustness against false triggering. However, it will also lead to slower reaction time, and shorter on-time. On the other hand, a high value of R will lead to improved reaction time, and longer on-time at the expense of increased chances of false triggering. Both TSC and the proposed clamp were simulated under a positive 1.5 kV HBM stress using the HBM test defined in the Military standard (Method 3015.8) [19]. The +1.5 kV stress was applied to the V_{DD} node of both clamps. Fig. 3.25 shows the voltage at the power supply node (V_{DD}) and the voltage at the gate of the main transistor (V_g) of the TSC under +1.5 kV HBM stress with different resistance values from $R = 1$ $k\Omega$ to $R = 100$ $k\Omega$.

When the resistance value is small, $R = 1$ $k\Omega$, the voltage at the gate of the main transistor ($V_g@R = 1$ $k\Omega$) is not high enough to keep the main transistor strongly on; as a result, the voltage at the power supply node ($V_{DD}@R = 1$ $k\Omega$) has a high peak voltage

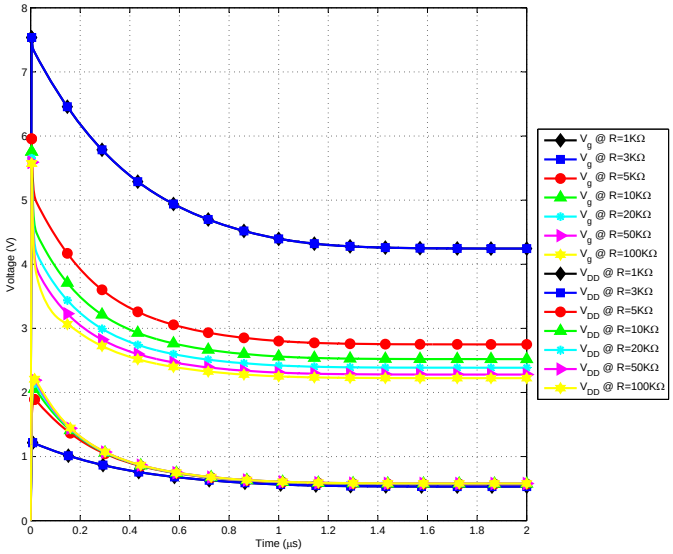
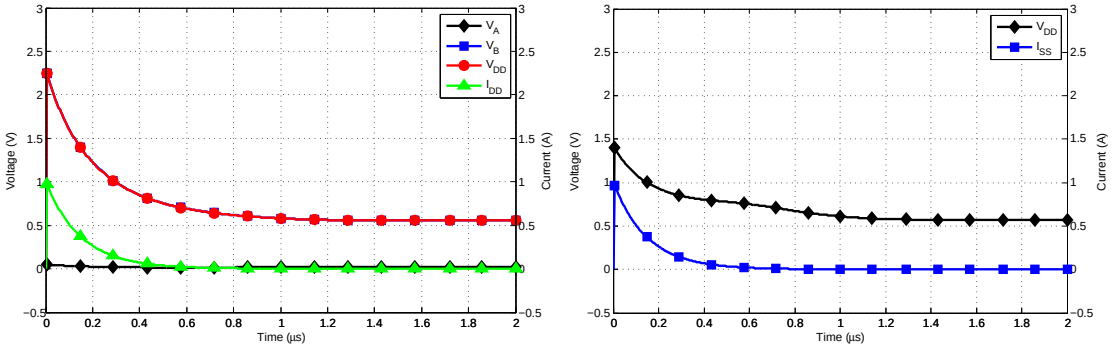


Figure 3.25: The traditional static clamp under 1.5 kV HBM stress.

($V_P = 7.5\ V$) and the voltage at $t = 2\ \mu s$ is 4.24 V. When the resistance value is large, $R = 100\ k\Omega$, the voltage at the gate of the main transistor ($V_g@R = 100\ k\Omega$) is increased due to the higher voltage drop across the resistance and leads to a reduction in the peak ($V_P = 5.57\ V$) ($V_{DD}@R = 100\ k\Omega$) and the voltage at $t = 2\ \mu s$ to 2.22 V. Even though, the large resistance has improved the HBM response of the TSC, the voltage at $t = 2\ \mu s$ is still high, which means the HBM ESD stress is not completely discharged.

Fig. 3.26 (a) shows the voltage of different nodes under positive 1.5 kV HBM stress of the DTC clamp. It can be concluded from Fig. 3.26 (a) that adding the delay element has improved the ESD HBM performance by lowering the peak voltage of the V_{DD} node to only 2.24 V thanks to higher voltage at node B. The main reason for improvement is as follows: At the onset of the ESD event, the node B goes high turning M_{ESD} on. The thyristor provides a sufficient delay so that M_{ESD} is kept on for sufficiently long time. Therefore, the HBM stress is discharged to 0.55 V at $t = 2\ \mu s$. The relative sizes of M_2 and M_4 is an important consideration in the design. Transistor M_4 is significantly weaker as compared to M_2, so that node B can follow the ESD stress voltage. Fig. 3.26 (b) shows the voltage at V_{DD} node is limited to 1.4 V under negative 1.5 kV HBM stress, which means that the

DTC clamp provides the protection for the circuit core against ±1.5 *kV* HBM stress.

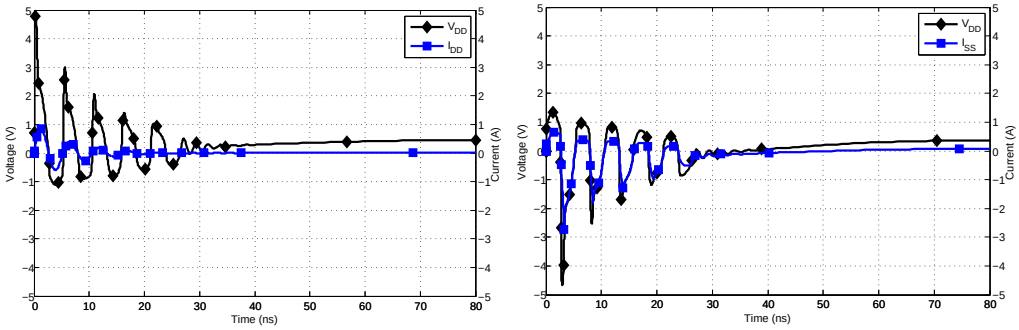


(a) HBM stress = 1.5 *kV*. (b) HBM stress = -1.5 *kV*.

Figure 3.26: Simulating the *DTC* design under ±1.5 *kV* HBM stress.

3.3.1.2 CDM ESD stress simulation results

The *DTC* design was also simulated under ±125 *V* CDM stress. Fig. 3.27 (a) shows the *DTC* design under the positive CDM stress, while Fig. 3.27 (b) shows the *DTC* design under the negative CDM stress. The *DTC* design is able to protect the circuit core against a ±125 *V* CDM stress as the peak voltage is limited to 4.78 *V* in the positive CDM stress and to 1.34 *V* in the negative CDM stress.



(a) CDM stress= 125 *V*. (b) CDM stress= - 125 *V*.

Figure 3.27: Simulating the *DTC* design under ±125 *V* CDM stress.

3.3.2 Normal operating conditions simulations

3.3.2.1 Immunity to false triggering

The proposed clamp was simulated under normal operating conditions as well. The first power-on condition was simulated by applying a 1 V voltage with a 100 ns rise time to V_{DD} node with grounded V_{SS} node. The voltage of different nodes for the first power-on of the DTC clamp as well as the current flows in the DTC clamp (I_{DD}) is shown in Fig. 3.28. As shown in Fig. 3.28, the voltage at node A follows the power supply voltage, while the voltage of node B briefly rises to 200 mV and then falls back to zero. In addition, I_{DD} goes to only 14 μA then it goes back to the leakage current range. Thus, the DTC clamp is not triggered even after a very fast power-on (100 ns) and this design is robust against false triggering.

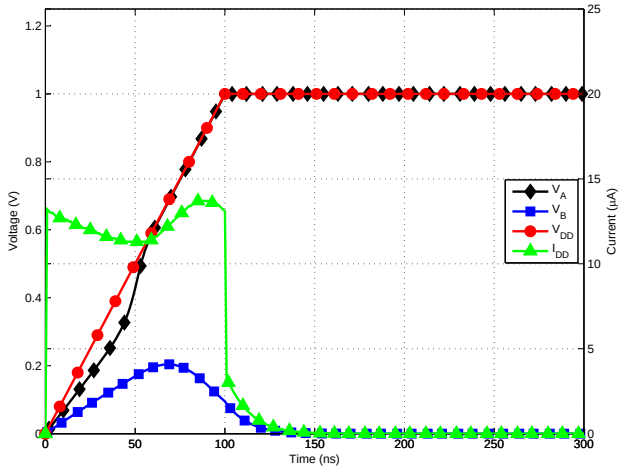


Figure 3.28: Simulating the DTC design under 100 ns power-on condition.

3.3.2.2 Immunity to power supply noise

The immunity to power supply noise was studied by adding a sinusoidal signal with a wide frequency range starting with near DC up to 3 GHz and amplitude of 200 mV (20% of normal voltage) to the power supply node with grounded V_{SS} node. An example of a noise

signal with a frequency of 1 GHz is shown in Fig. 3.29; the figure illustrates simulations results indicating the voltage at node B of the clamp and the V_{DD} node. It is apparent that the voltage of node B stays below 50 mV, which is not high enough to turn the main transistor on. As a result, the clamp is robust against the power supply noise.

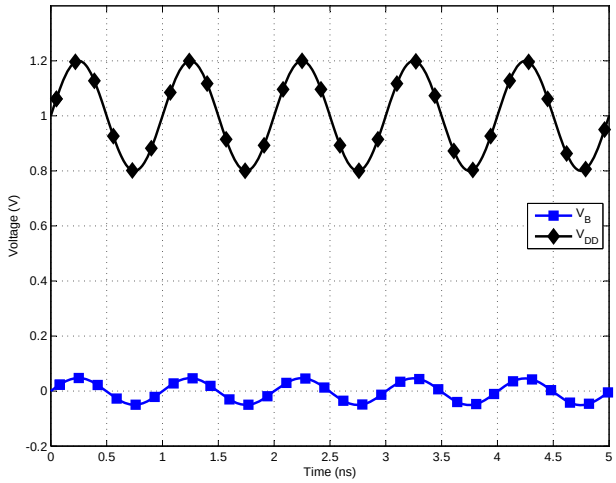


Figure 3.29: Simulating the DTC design under 20% power supply noise.

3.3.3 Measurement results

Fig. 3.30 shows the layout of the DTC clamp. The total layout area of the DTC clamp is 70 μm x 46 μm. The carried out measurements to verify the DTC clamp under both ESD condition and normal operating conditions are presented in this section.

3.3.3.1 ESD performance

3.3.3.1.1 Turn-on verification: The setup of the turn-on verification measurement of the PTC clamp was provided in section 3.2.3.1.1, the same setup was used for the DTC clamp.

- Chip not powered: Fig. 3.31 shows the voltage at the V_{DD} node (V_{DUT}), as well as the current flowing in the DTC clamp (I_{DUT}). It can be seen in Fig. 3.31 that the

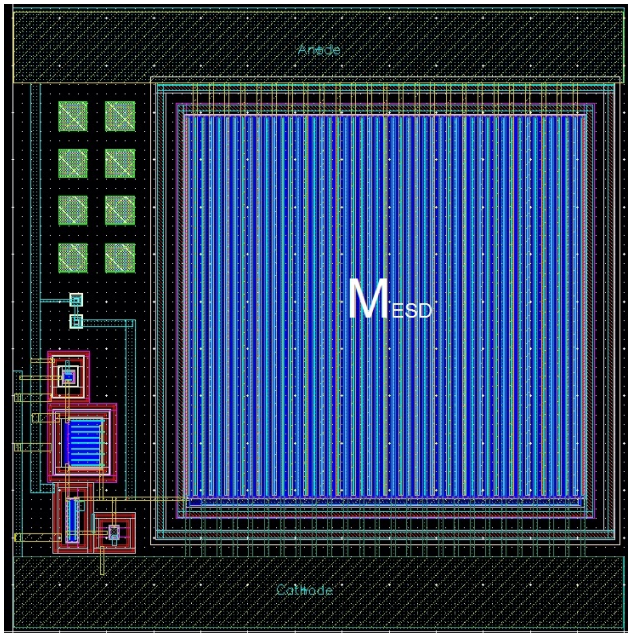


Figure 3.30: The layout of the *DTC* clamp.

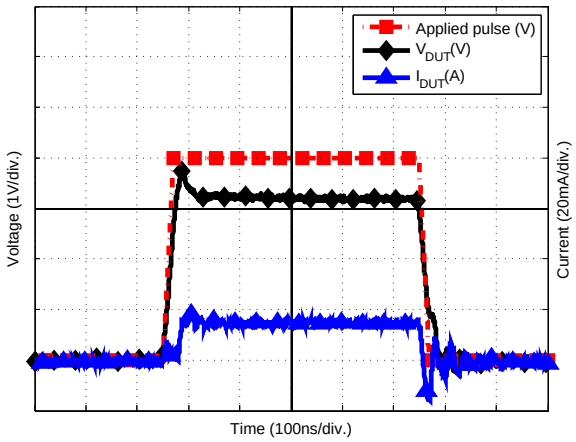


Figure 3.31: Turn-on verification of *DTC* clamp under not powered condition.

proposed design stays on for the entire pulse and after the pulse finishes the clamp is turn off, and the current flowing in it goes back to zero. Also, it is evident from the figure that the clamp is conducting about 20 mA and the voltage at V_{DD} node is limited to only 3.3 V under 4 V ESD-like pulse voltage.

- Chip powered: As shown in Fig. 3.32, the voltage stress triggers the DTC and the average current going through the clamp (I_{DUT}) is about 20 mA. However, the DTC clamp is turned off after the stress is gone, and the I_{DUT} goes back to the leakage current level. Thus, the clamp is immune to the latch-on issue due to an ESD-like event.

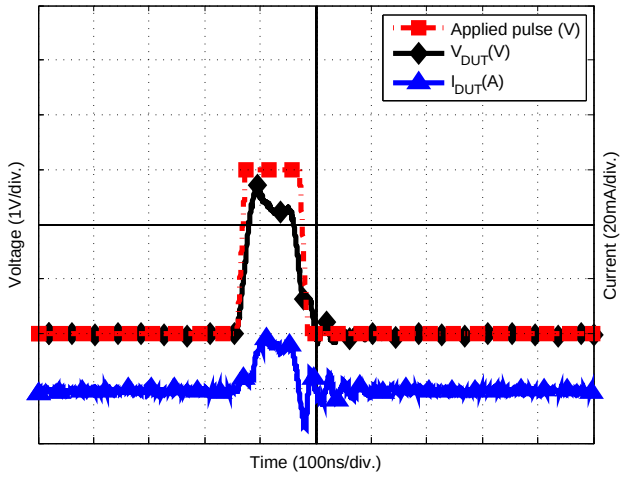


Figure 3.32: Turn-on verification of DTC clamp under powered condition.

3.3.3.1.2 TLP testing: The same configuration described in section 3.2.3.1.2 was used to obtain I-V TLP curve of the DTC clamp. Fig. 3.33 presents the TLP results of the DTC clamp. From Fig. 3.33, it can be seen that the proposed design is capable of handling 3.21A of current, while its leakage is only 180 pA at 1 V supply. Also, the figure shows that the proposed clamp has a holding voltage of 1.5 V and a triggering voltage of 3.3 V. From Fig. 3.33, $I_{@V=5V}$ of the DTC clamp is 1.82 A, which can result in HBM failure threshold level of 2.7 kV. Also, the DTC clamp has an on-resistance (R_{ON}) of 2.334Ω. Based on

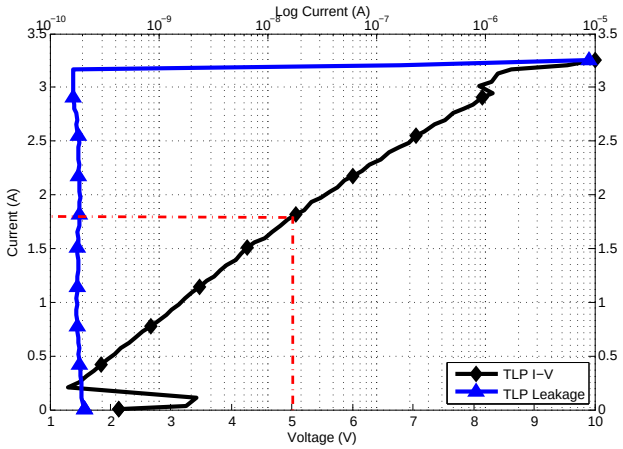


Figure 3.33: TLP measurement results of the proposed DTC clamp.

the data from the TLP measurements, it can be seen that the design has met the design requirement of the 65 nm CMOS technology (i.e. HBM protection level of 1.5 kV).

3.3.3.1.3 HBM and CDM measurements: This clamp passes both +3.5 kV and −4.5 kV stresses, but the clamp fails to pass +3.75 kV and −4.75 kV stresses. In CDM measurement, the chip that includes the clamp is charged by both positive and negative voltages with 50 V step sizes. Then, in the positive CDM stress, the V_{SS} node is grounded to zap the CDM event, while in the negative CDM stress the V_{DD} node is grounded to zap the CDM event. The DTC clamp passes both +700 V and −450 V stresses, but it fails to pass +750 V and −500 V stresses.

3.3.3.2 Normal operating conditions

3.3.3.2.1 Immunity to false triggering: The measurement setup described in section 3.2.3.2.1 was used for this design. Fig. 3.34 presents the first power-on condition; it can be seen that the proposed design does not falsely trigger due to the first power-on condition. It clear from the figure that the clamp does not trigger on as the current (I_{DUT}) goes high to 600 μA and then it goes back to the leakage current level.

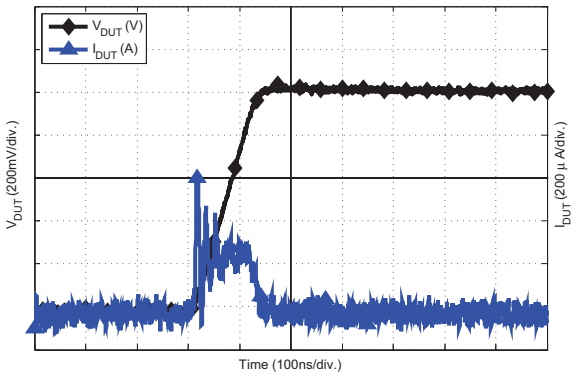


Figure 3.34: The DTC under a first power-on condition with 1 V voltage pulse and 100 ns rise-time.

3.3.3.2.2 Leakage vs. temperature: The same configuration described in section 3.2.3.2.2 was used to measure the leakage current as a function of temperature. Fig. 3.35 shows the measured leakage current of the DTC design up to 80^oC and the simulated leakage current of the DTC design up to 125^oC as a function of the temperature. The data presented in Fig. 3.35 clearly shows that the fabricated design has almost the same leakage current as the simulated structure in the temperature range from 25^oC to 80^oC. Therefore, it is expected that the leakage current of the fabricated design will follow the same trend as the simulated leakage current when the temperature is higher than 80^oC. Based on the measurement results, the DTC clamp has a leakage current of 180 pA, and 5.77 nA at 25^oC and 75^oC, respectively.

3.3.3.2.3 Immunity to transient induced latch-up: The same configuration described in section 3.2.3.2.3 was used to evaluate the stability of the DTC design against the transient induced latch-up. Fig. 3.36 (a) presents the DTC design under a positive transient-induced latch-up with V_{charge} of +210 V, while Fig. 3.36 (b) presents the DTC design under a negative transient-induced latch-up with V_{charge} of −210 V. Fig. 3.36 clearly shows that the DTC design is immune against latch-up due to transient-induced noise with V_{charge} ±210 V as the current (I_{DUT}) goes back to the leakage current level once the transient-induced noise ends.

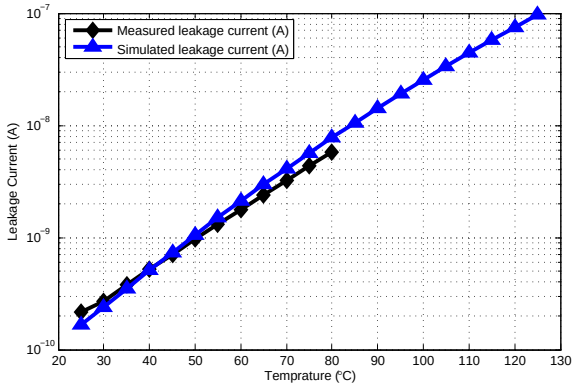
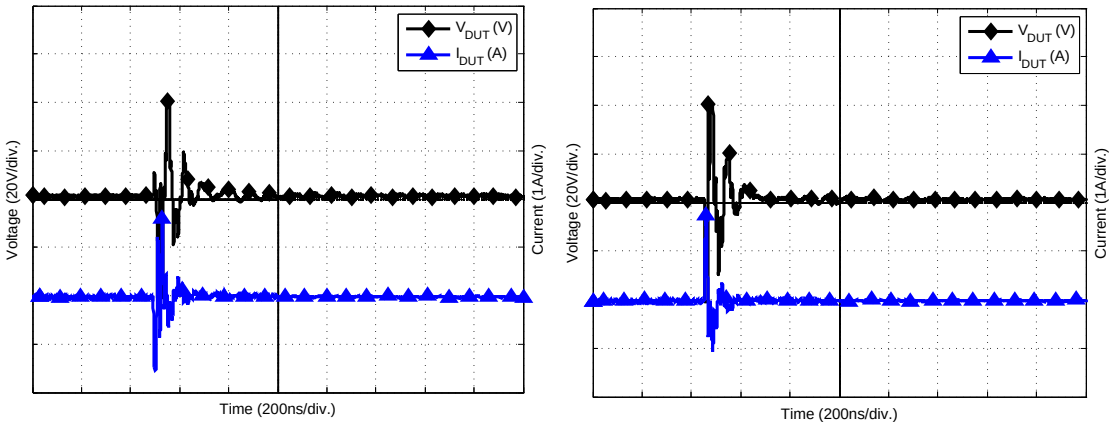


Figure 3.35: The simulated and measurement result of leakage vs. temperature for *DTC* clamp.



(a) V_{charge} = 210 V. (b) V_{charge} = - 210 V.

Figure 3.36: The *DTC* design under TLU with different V_{charge}.

Chapter 4

Hybrid ESD Power Supply Clamps

In this Chapter, two new ESD power supply clamps in 65 nm GP CMOS technology are proposed, which are: PMOS based ESD power clamp with thyristor delay element and diodes ($PTDC$) and NMOS based ESD power clamp with level converter delay element and diodes ($NLDC$). The main target of these two designs is to improve the CDM performance to be able to protect the circuit core against CDM stress with 300 V level while maintaining the low-leakage current as in the designs proposed in Chapter 3. Therefore, the two designs proposed in this Chapter have been designed based on the pi-network ESD protection circuit, shown in Fig. 4.1, with some changes. The original pi-network ESD protection consists of two static clamps, a primary clamp and a secondary clamps such as a diode string and/or an SCR. The secondary clamp triggers first and due to the voltage build up through the resistance (R) the primary clamp is triggered and conducts most of the ESD energy [14]. In my designs, a transient clamp is used as the primary clamp, which is triggered through its own triggering circuit, while a diode configuration that consists of two diodes is used as the secondary clamp. The reason for using two diodes is to ensure that the clamp does not trigger under normal operating conditions. The proposed designs were named hybrid clamps as they consist of both static and transient clamps.

Two diodes in series were used in the path from V_{DD} to V_{SS}, while one diode was used in the path from V_{SS} to V_{DD}. The two diode configuration leads to a triggering voltage of 1.4 V, which is higher than the power supply voltage. As a consequence, the static

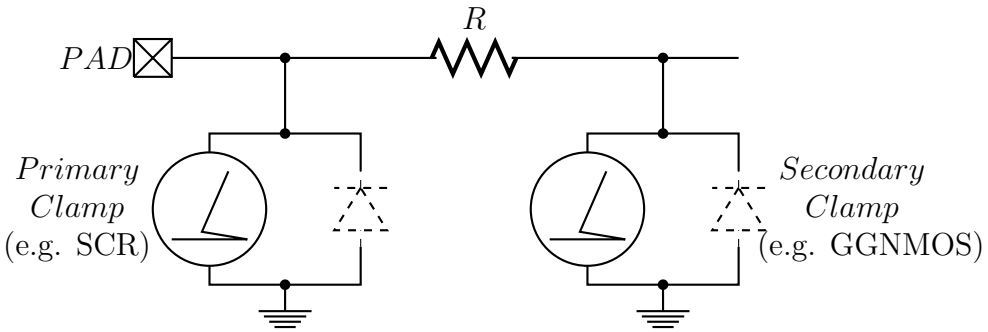


Figure 4.1: The pi ESD protection network [14].

clamp is stable and has a fast response to an ESD event. The leakage current of diodes as a function of the diodes' area was investigated, and the simulation results are presented in Fig 4.2, where 1 V DC voltage was applied to the V_{DD} node with grounded V_{SS} node. Based on the results presented in Fig 4.2, the diode string has a leakage that less than 6 nA for an area about 100 μm^2.

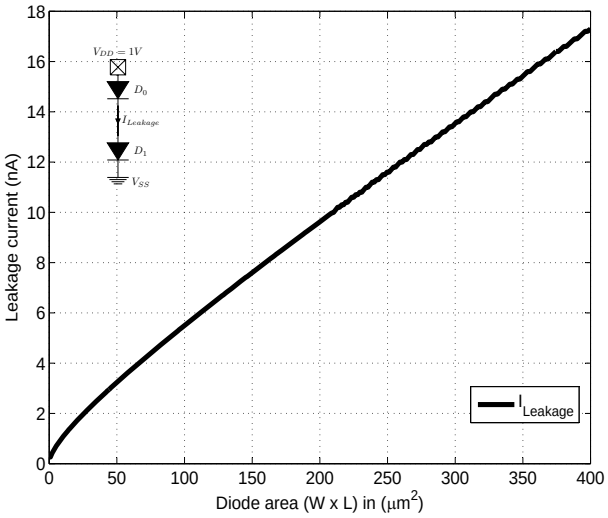


Figure 4.2: The simulated leakage of a diode string in 65 nm technology.

4.1 PMOS based ESD power clamp with thyristor delay element and diodes (*PTDC*)

The first design step was to simultaneously optimize the width of the clamping transistor and the diodes' area, for the leakage current and a peak voltage of a positive 300 V CDM stress. Fig. 4.3 provides a summary of simulation results. On the X-axis, moving from left to right, the width of the M_{ESD} transistor is increasing, and the area of the diodes is decreasing while the total area is kept constant. The left Y-axis gives the simulated peak CDM voltage, while the right Y-axis gives the total leakage current of the proposed design. The target is to ensure that the peak voltage of the positive 300 V CDM stress is less than $5V$. Based on the results presented in Fig. 4.3, the diodes' size of 11.35 x 8.8 μm^2 and M_{ESD} size of 600 μ $m/350$ nm were selected as they meet the specified criteria of having the peak voltage of the positive 300 V CDM stress is less than 5 V voltage ($V_P = 4.74$ V) with minimized leakage current ($I_{Leakage} = 31.37$ nA). Fig. 4.4 shows the structure of the $PTDC$ design, while Table 4.1 summarizes the sizes of the elements.

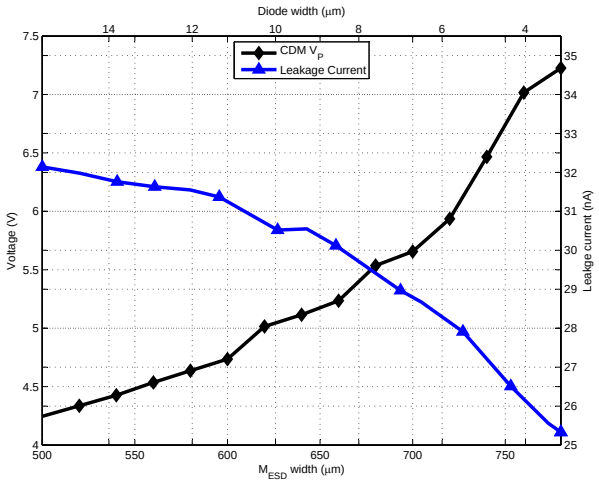


Figure 4.3: Design exploration of the clamping components with constant area.

The body of M_{ESD} is connected to the anode of D_1, which has two advantages: reduction of the threshold voltage of M_{ESD} to speed up its triggering mechanism and to provide

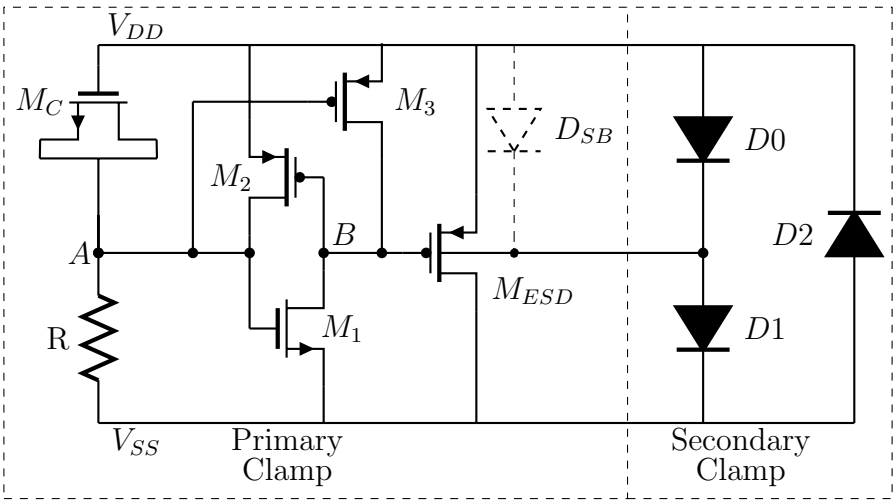


Figure 4.4: PMOS ESD clamp with thyristor delay element and diodes ($PTDC$).

Element	Type	Length (μm)	Total width (μm)	number of fingers
M_{ESD}	PMOS	0.35	600	30
M_1	NMOS	0.280	2	1
M_2	PMOS	0.280	2	1
M_3	PMOS	0.280	0.4	1
M_C	NMOS	1	82.44	6
R	rppolywo	25	7.7	5
D_0, D_1	pdio	8.8	11.35	3
D_2	pdio	18.25	3.5	–

Table 4.1: Element sizes in the $PTDC$ design.

another path for the ESD current through the parasitic source-body diode (D_{SB}) and D_1 diode. Under the normal operating conditions, the secondary clamp is off as the voltage at V_{DD} node is 1 V. The capacitor M_C is fully charged and the voltage of node A is low, which turns M_3 on and that keep the main transistor M_{ESD} off by pulling node B high. Under the ESD event, the secondary ESD clamp (diodes) is triggered first and starts to sink the ESD energy. Then, the primary clamp (M_{ESD}) starts to conduct and sinks most of the ESD energy through the following sequence: the voltage at node A becomes high, and that turns the CMOS thyristor on. As a result, the voltage of node B goes low and turns on the main transistor M_{ESD}.

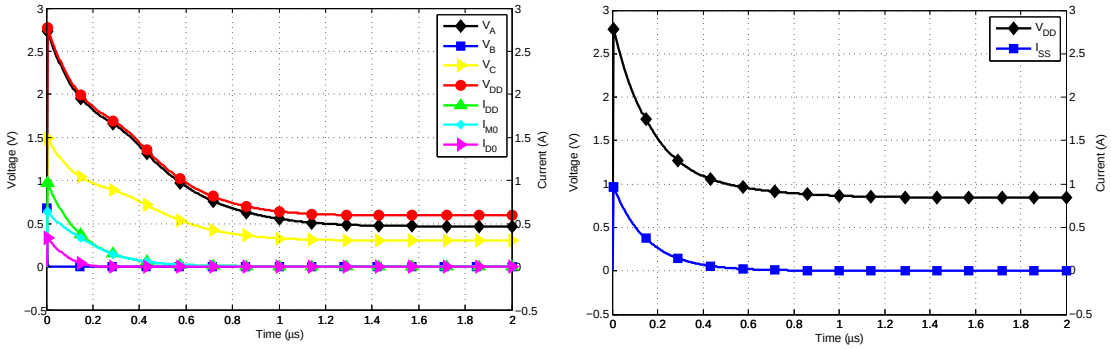
4.1.1 ESD simulation results

4.1.1.1 HBM ESD stress simulation results

Fig. 4.5 (a) shows the voltage of different nodes under the positive 1.5 kV HBM stress that was applied to V_{DD} node of the $PTDC$ with grounded V_{SS} node. It can be seen in Fig. 4.5 (a) the peak voltage of the V_{DD} node is 2.76 V; also, the main transistor M_{ESD} sinks most of the ESD current (I_{M0}). Fig. 4.5 (b) shows the response of the $PTDC$ design to the negative 1.5 kV HBM stress that was applied to V_{SS} node of the $PTDC$ with grounded V_{DD} node. It can be seen in Fig. 4.5 (b) that the voltage across the clamp is limited to $2.78V$, which means that the $PTDC$ clamp provides the protection for the circuit core against ± 1.5 kV HBM stress.

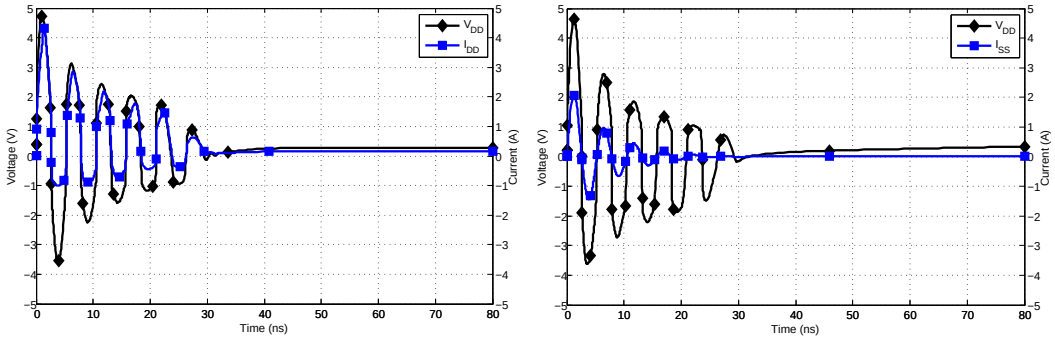
4.1.1.2 CDM ESD stress simulation results

The $PTDC$ design was also simulated for ± 300 V CDM stress using the same setup described in section 3.2.1.2. Fig. 4.6 (a) shows the design under the positive CDM stress that was applied to V_{DD} node with grounded V_{SS} node, while Fig. 4.6 (b) shows the design under negative CDM stress that was applied to V_{SS} node with grounded V_{DD} node.



(a) HBM stress = 1.5 kV. (b) HBM stress = - 1.5 kV.

Figure 4.5: Simulating the $PTDC$ design under ± 1.5 kV HBM stress.



(a) CDM stress = 300 V. (b) CDM stress = - 300 V.

Figure 4.6: Simulating the $PTDC$ design under ± 300 V CDM stress.

The $PTDC$ design can protect the circuit core against a $\pm 300\ V$ CDM stress as the peak voltage is limited to $4.73\ V$ in the positive CDM stress and to $4.3\ V$ in the negative CDM stress.

4.1.2 Normal operating conditions simulations

4.1.2.1 Immunity to false triggering

To test the $PTDC$ clamp under first power-on condition, a $1\ V$ voltage with a $100\ ns$ rise time was applied to V_{DD} node with grounded V_{SS} node; Fig. 4.7 presents the simulation results. It can be seen in Fig. 4.7 that the voltage of node A rises up to only $200\ mV$, while the voltage of B follows the power supply voltage. In addition, I_{DD} goes to only $6\ \mu A$ then it goes back to the leakage current range. Thus, the $PTDC$ clamp is robust against false triggering due to $100\ ns$ rise-time first power-on condition.

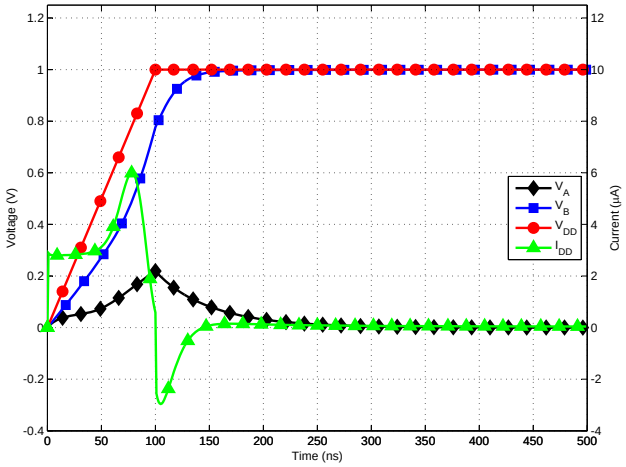


Figure 4.7: Simulating the $PTDC$ design under $100\ ns$ power-on condition.

4.1.2.2 Immunity to power supply noise

Immunity to power supply noise was studied by adding a sinusoidal signal with a wide frequency range starting with near DC up to $3\ GHz$ and amplitude of $200\ mV$ (representing

20% supply noise) to the power supply node with grounded V_{SS} node. An example of a noise signal with a frequency of 1 GHz is shown in Fig. 4.8. It is apparent in the figure that the voltage of node B stays higher than 850 mV, which is high enough to keep the main transistor off. As a result, the clamp is robust against the power supply noise.

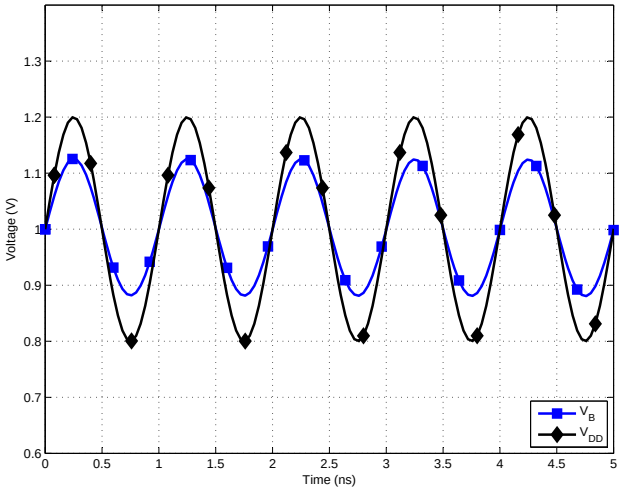


Figure 4.8: Simulating the *PTDC* design under 20% power supply noise.

4.1.3 Measurement results

The layout of the *PTDC* clamp is shown in Fig. 4.9. The total layout area of the *PTDC* clamp is 79.1 μm x 25.8 μm. This section provides the measurement verifications that were carried out for the *PTDC* clamp under both ESD and normal operating conditions.

4.1.3.1 ESD performance

4.1.3.1.1 Turn-on verification: The setup of the turn-on verification measurement of the *PTDC* clamp was given in section 3.2.3.1.1.

- Chip not powered: Fig. 4.10 shows the voltage at the V_{DD} node (V_{DUT}) as well as the current flowing in the *PTDC* clamp (I_{DUT}). It can be seen in Fig. 4.10 that the

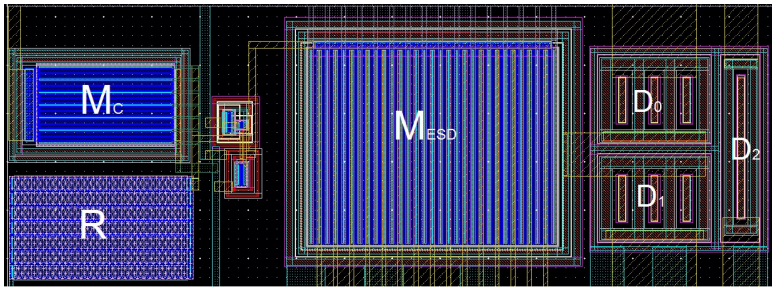


Figure 4.9: The layout of the *PTDC* clamp.

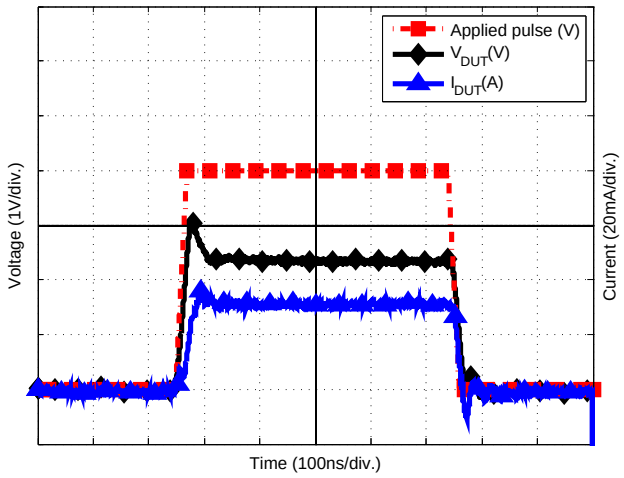


Figure 4.10: Turn-on verification of *PTDC* clamp under not powered condition.

PTDC design stays on for the entire pulse and after the pulse ends, the clamp turns off, and the current flowing in it goes back to zero. Also, the figure shows that the clamp is conducting about 30 mA and the voltage at V_{DD} node is limited to only 2.3 V under the 4 V ESD-like pulse voltage.

- Chip powered: As shown in Fig. 4.11, the voltage stress triggers the *PTDC* and the average current going through the clamp (I_{DUT}) is about 30 mA. However, the *PTDC* clamp turns off after the stress is gone, and the I_{DUT} goes back to the leakage current level. Thus, the clamp is immune to the latch-on issue due to an ESD-like event when the clamp is powered.

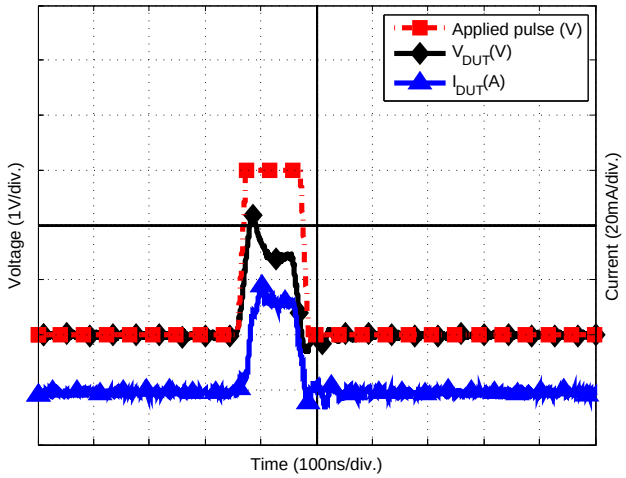


Figure 4.11: Turn-on verification of *PTDC* clamp under powered condition.

4.1.3.1.2 TLP testing: The same configuration described in section 3.2.3.1.2 was used to obtain I-V TLP curve of the *PTDC* clamp. Fig. 4.12 presents the TLP results of the *PTDC* clamp. From Fig. 4.12, it can be said that the design has a leakage of 124 nA at 1 V supply. The high leakage compared with the designs presented in chapter 3 is due to the diode string as well as the parasitic D_{SB} diode. Also, the figure shows that $I_{@V=5V}$ of the *PTDC* clamp is 1.24 A, which will result in HBM failure threshold level of 1.85 kV. The on-resistance (R_{ON}) of *PTDC* is 3.76 Ω. Based on the data from the TLP

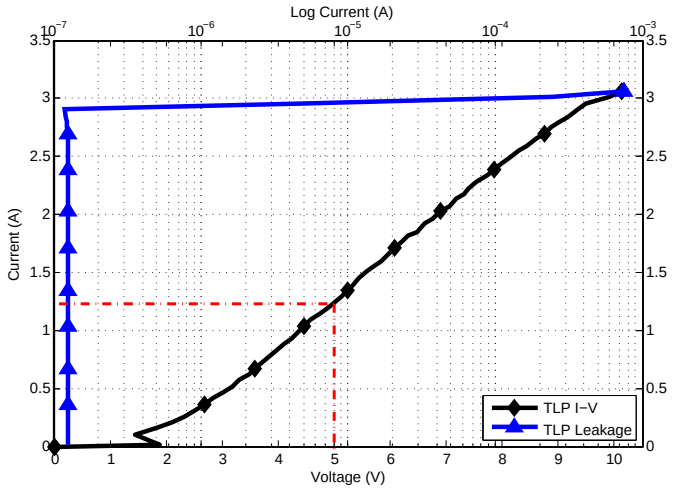


Figure 4.12: TLP measurement results of the proposed *PTDC* clamp.

measurements, the design has met the design requirement of 65 nm CMOS technology (i.e. HBM protection level of 1.5 kV).

4.1.3.1.3 HBM and CDM measurements: This clamp passes both +4.5 kV and −2.25 kV stresses, but the clamp fails to pass +4.75 kV and −2.5 kV stresses. In CDM measurement, the clamp is stressed by both positive and negative voltages in 50 V step sizes. In the positive CDM stress, the V_{SS} node is grounded to zap the device, while in the negative CDM stress the V_{DD} node is grounded to zap the device. The *PTDC* clamp passes both +800 V and −450 V stresses, but fails to pass +850 V and −500 V stresses.

4.1.3.2 Normal operating conditions

4.1.3.2.1 Immunity to false triggering: The measurement setup was described in section 3.2.3.2.1. Fig. 4.13 presents the fast power-on condition in which it is seen that the *PTDC* design does not falsely trigger even with a fast power-on condition. It is clear from the figure that the clamp does not trigger on as the current flows (I_{DD}) increases to 600 μA and then it goes back to the leakage current level.

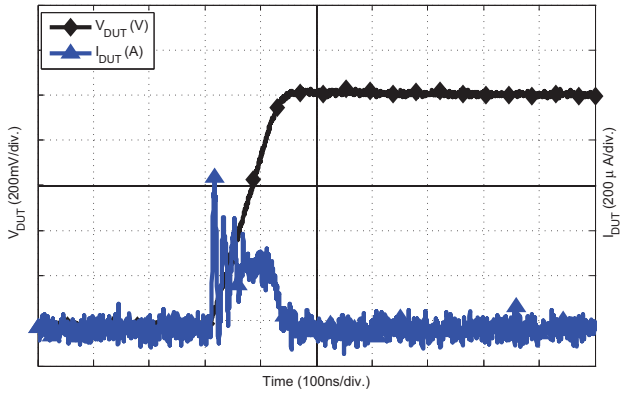


Figure 4.13: The *PTDC* under a first power-on condition with 1 V voltage pulse and 100 ns rise-time.

4.1.3.2.2 Leakage vs. temperature: The same configuration described in section 3.2.3.2.2 was used to measure the leakage current as a function of temperature. Fig. 4.14 shows the leakage current of the design up to 80^oC and the simulated leakage current up to 125^oC as a function of the temperature.

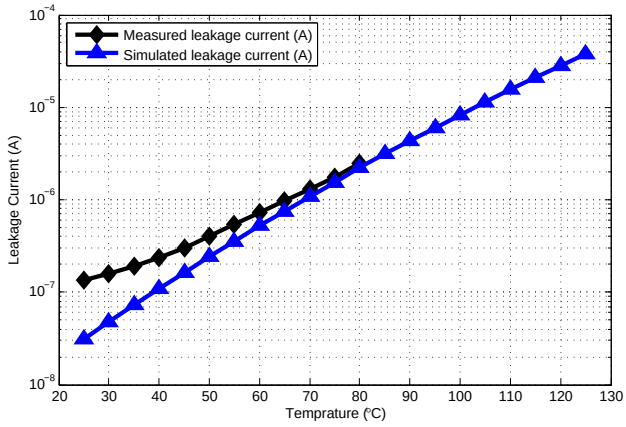
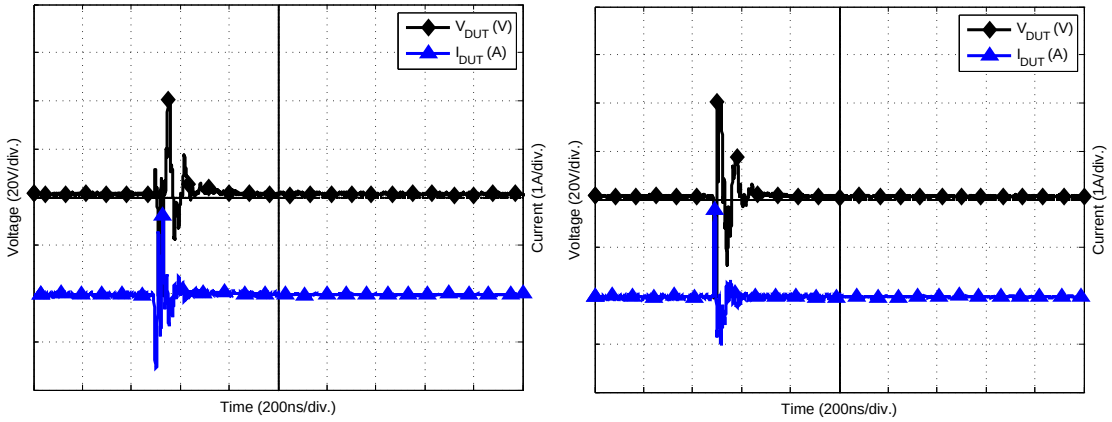


Figure 4.14: The measurement and simulation results of leakage vs. temperature for *PTDC* clamp.

The data presented in Fig. 4.14 shows that the measured and simulated results flow the same trend in the temperature range from 25^oC to 80^oC. Therefore, it is expected that

the leakage current of the fabricated design will follow the same trend as the simulated leakage current when the temperature is higher than 80^oC. Based on the measurement results, the $PTDC$ clamp has a leakage current of 124 nA, and 1.76 μA at 25^oC and 75^oC, respectively.

4.1.3.2.3 Immunity to transient induced latch-up: The same configuration described in section 3.2.3.2.3 was used to evaluate the stability of the proposed design against the transient induced latch-up. Fig. 4.15 (a) presents the $PTDC$ design under a positive transient-induced latch-up with V_{charge} of +210 V, while Fig. 4.15 (b) presents the $PTDC$ design under a negative transient-induced latch-up with V_{charge} of −210 V. Fig. 4.15 clearly shows that the $PTDC$ design is immune against latch-up due to transient-induced noise with V_{charge} ±210 V as the current (I_{DUT}) goes back to the leakage current level after the transient-induced noise is gone.



(a) V_{charge} = 210 V. (b) V_{charge} = - 210 V.

Figure 4.15: The $PTDC$ design under TLU with different V_{charge}.

4.2 NMOS based ESD power clamp with level shifter delay element and diodes (*NDLC*)

The *NLDC* structure was designed based on the same concept that was used to design *PTDC* structure (i.e. the pi-network ESD protection circuit). The width of the clamping transistor and the diodes' area were optimized for the leakage current and a peak voltage of a positive 300 V CDM stress. Fig. 4.16 provides a summary of simulation results. On the X-axis, moving from left to right, the width of M_{ESD} transistor is increasing, and the area of the diode is reducing while the total area is kept constant. The left Y-axis gives the simulated peak CDM voltage, while the right Y-axis gives the total leakage of the proposed design. The design objective was to ensure that the peak voltage of the positive 300 V CDM stress does not exceed 5 V. Based on the results presented in Fig. 4.3, the diodes size of 10.4 x 8.6 μm^2 and M_{ESD} size of 680 $\mu m/350$ nm were selected as they meet the specified criteria, CDM V_P = 4.89 V with minimized leakage current ($I_{Leakage}$ = 13.12 nA). Fig. 4.17 shows the structure of the *NLDC* design, while Table 4.2 summarizes the sizes of the components.

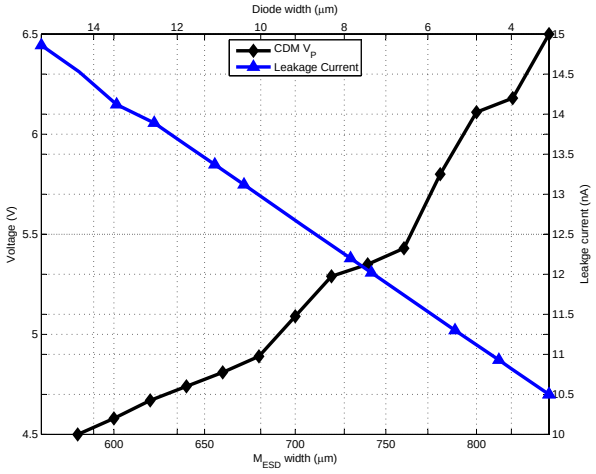


Figure 4.16: Design exploration of the clamping components with constant area.

Under normal operating conditions, the capacitor M_C is fully charged, and the voltage

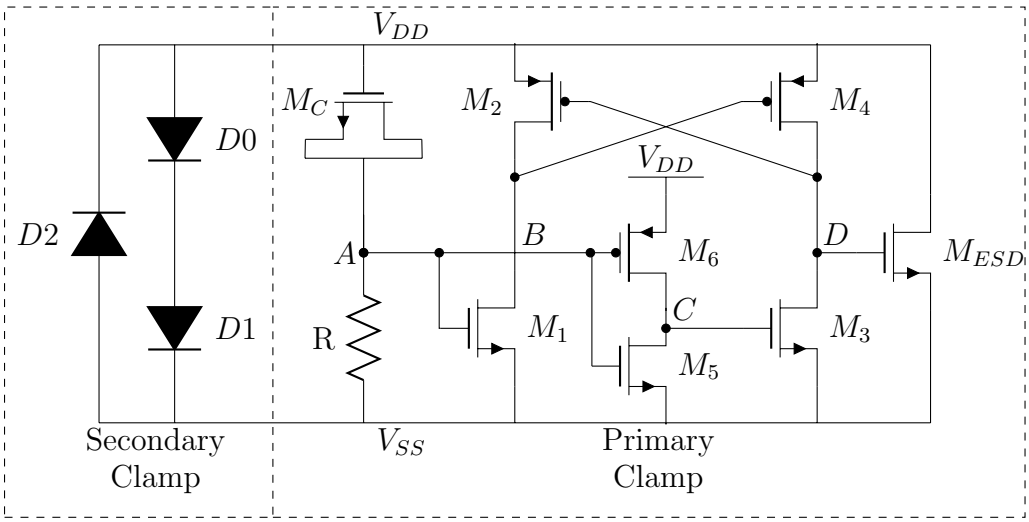


Figure 4.17: NMOS ESD clamp with level shifter delay element and diodes (NLDC).

Element	Type	Length (μm)	Total width (μm)	number of fingers
M_{ESD}	NMOS	0.35	680	34
M_1	NMOS	0.1	0.4	1
M_2	PMOS	0.26	24	8
M_3	NMOS	0.06	0.2	1
M_4	PMOS	0.1	0.4	1
M_5	NMOS	0.1	0.4	1
M_6	PMOS	0.1	0.8	1
M_C	NMOS	1	82.44	6
R	rppolywo	25	7.7	5
D_0, D_1	pdio	8.6	10.4	3
D_2	pdio	18.6	3.5	–

Table 4.2: Element sizes in the *NLDC* design.

at node A is low. Thus, the voltage at node C is high; therefore, M_3 is on and the voltage at node D is low, which keeps M_{ESD} off. Under an ESD event, the secondary ESD clamp (diodes) is turned on as the voltage at V_{DD} node exceeds its triggering voltage and starts to sink the ESD energy, first. Then, the primary clamp (M_{ESD}) is triggered to sink most of the ESD event through the following sequence: The voltage at node A becomes high for a short time; as a consequence, M_1 is on and pulls down the voltage at node B that turns M_4 on. As a result, the main transistor M_{ESD} is on and starts to sink the ESD energy. Since the time constant of the R M_C is small, the voltage at node A starts to decrease rapidly. Therefore, the voltage at node C is increasing and trying to pull down the voltage at node D down through turning on M_3; at the same time M_4 is trying to pull up the voltage at node D. M_4 was designed to be larger, and slower, keeps the M_{ESD} on for enough time to sink the ESD event.

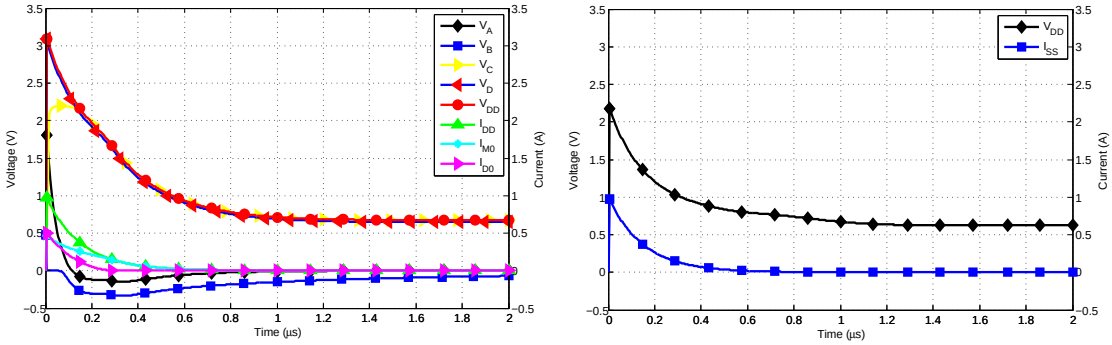
4.2.1 ESD simulation results

4.2.1.1 HBM ESD stress simulation results

Fig. 4.18 (a) shows the response of the *NLDC* design to the positive 1.5 kV HBM stress that was applied to V_{DD} node with grounded V_{SS} node. It can be concluded from Fig. 4.18 (a) the peak voltage of the V_{DD} node is 3.09 V; also, the main transistor M_{ESD} sinks most of the ESD current, (I_{M0}) in the figure. Fig. 4.18 (b) shows the response of the *NLDC* design to the negative 1.5 kV HBM stress that was applied to V_{SS} node of the *NLDC* with grounded V_{DD} node. Fig. 4.18 (b) shows the voltage across the clamp is limited to 2.18 V, which means that the *NLDC* clamp provides the protection for the circuit core against ± 1.5 kV HBM stress.

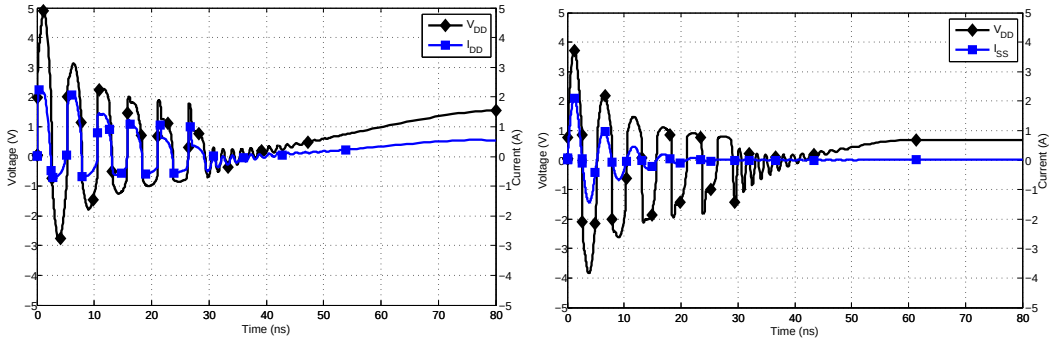
4.2.1.2 CDM ESD stress simulation results

The *NLDC* design was also simulated for ± 300 V CDM stress using the same setup described in section 3.2.1.2. Fig. 4.19 (a) shows the design under the positive CDM stress, while Fig. 4.19 (b) shows the design under the negative CDM stress.



(a) HBM stress = 1.5 kV. (b) HBM stress = - 1.5 kV.

Figure 4.18: Simulating the *NLDC* design under ±1.5 kV HBM stress.



(a) CDM stress = 300 V. (b) CDM stress = - 300 V.

Figure 4.19: Simulating the *NLDC* design under ±300 kV CDM stress.

The *NLDC* design can protect the circuit core against a ±300 V CDM stress as the peak voltage is limited to 4.89 V in the positive CDM stress and to 3.7 V in the negative CDM stress.

4.2.2 Normal operating conditions simulations

4.2.2.1 Immunity to false triggering

The proposed clamp was simulated under normal operating conditions as well. A 1 V voltage pulse with 100 ns rise time was used in simulation to test the *NLDC* clamp under the first power-on condition. The voltage pulse was applied to V_{DD} node with grounded V_{SS} node. The voltage of different nodes for the first power-on of the *NLDC* clamp as well as the current flowing through it (I_{DD}) is shown in Fig. 4.20.

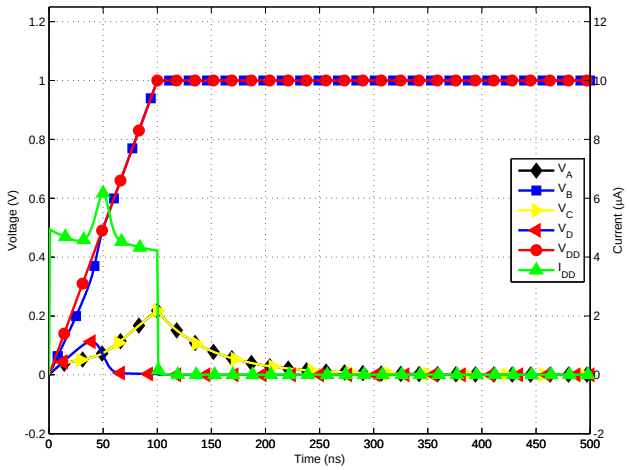


Figure 4.20: Simulating the *NLDC* design under 100 ns power-on conditions.

It can be seen in Fig. 4.20 that the voltage of node D rises to only 100 mV, which is not high enough to trigger the main transistor (M_{ESD}). In addition, I_{DD} goes to only 6 μA then it goes back to the leakage current range. Thus, the *NLDC* clamp is robust against false triggering under a 100 ns rise-time first power-on condition.

4.2.2.2 Immunity to power supply noise

The immunity to power supply noise was studied by adding a sinusoidal signal with a wide frequency range starting with near DC up to 3 GHz and amplitude of 200 mV to the power supply node with grounded V_{SS} node. An example of a noise signal with a frequency of 1 GHz is shown in Fig. 4.21; the figure illustrates simulations results showing the voltage at node D of the clamp and the V_{DD} node. It is apparent that the voltage of node D stays below 50 mV, which is substantially smaller than the threshold voltage of the main transistor (435 mV). The secondary clamp; with two diodes being a static one, is robust against false triggering. As a result, the clamp is robust against the power supply noise.

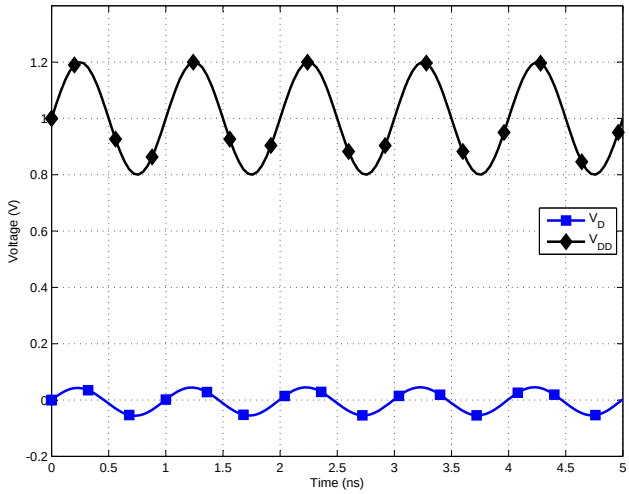


Figure 4.21: Simulating the *NLDC* design under 20% power supply noise.

4.2.3 Measurement results

The layout of the *NLDC* clamp is shown in Fig. 4.22. The total layout area of the *NLDC* clamp is 82.5 μm x 27 μm.

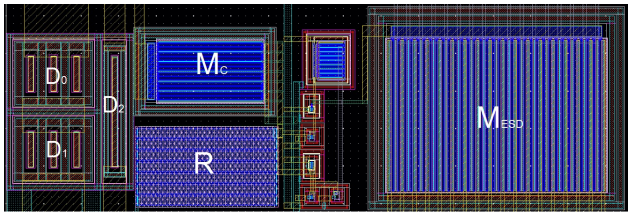


Figure 4.22: The layout of the *NLDC* clamp.

4.2.3.1 ESD performance

4.2.3.1.1 Turn-on verification: The setup of the turn-on verification measurement of the *NLDC* clamp was given in section 3.2.3.1.1.

- Chip not powered: Fig. 4.23 shows the voltage at the V_{DD} node (V_{DUT}) as well as the current flowing in the *NLDC* clamp (I_{DUT}). It can be seen in Fig. 4.23 that the

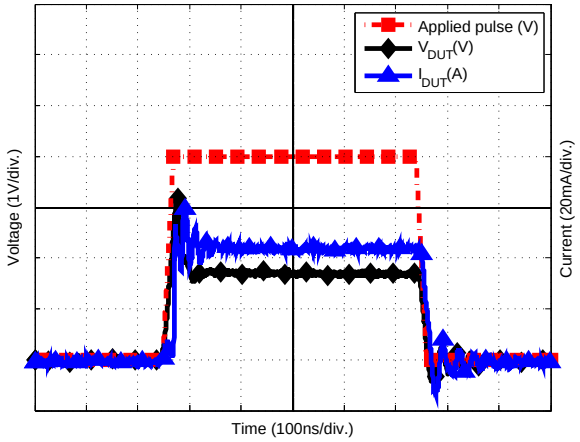


Figure 4.23: Turn-on verification of *NLDC* clamp under not powered condition.

NLDC design stays on for the entire pulse and after the pulse finishes the *NLDC* clamp turns off and the current flowing in it goes back to zero. The clamp is carrying about 45 mA of current and the voltage across the *NLDC* design is only 2.2 V under the 4 V ESD-like pulse voltage.

- Chip powered: As shown in Fig. 4.24, the voltage stress triggers the *NLDC* and the average current going through the clamp (I_{DUT}) is about 35 mA. However, the *NLDC* clamp turns off after the stress is gone, and the I_{DUT} goes back to the leakage current level. Thus, the clamp is robust against the latch-on issue due to an ESD-like event when the clamp is powered.

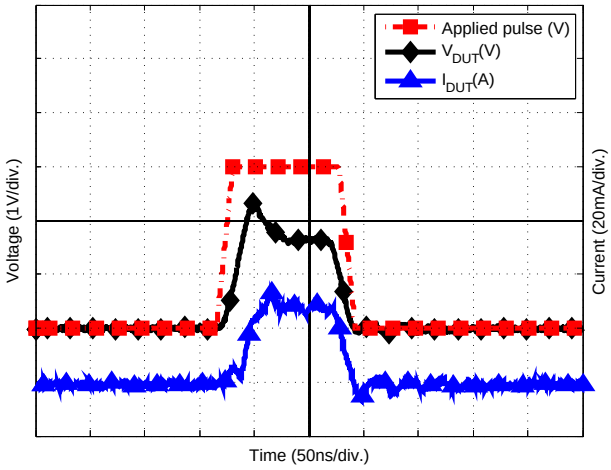


Figure 4.24: Turn-on verification of *NLDC* clamp under powered condition.

4.2.3.1.2 TLP testing: The same configuration described in section 3.2.3.1.2 was used to obtain I-V TLP characteristics of the *NLDC* clamp. Fig. 4.25 presents the TLP results of the *NLDC* clamp. Based on the I-V TLP curve presented in Fig. 4.25, the *NLDC* design has a leakage of 14.3 nA at 1 V supply at room temperature and the $I_{@V=5V}$ of the *NLDC* clamp is 1.29 A, which can result in HBM failure threshold level of 1.93 kV. The on-resistance (R_{ON}) of *NLDC* is 2.97 Ω. The design meets the design requirement of the 65nm CMOS technology (i.e. HBM protection level of $\pm$1.5 kV).

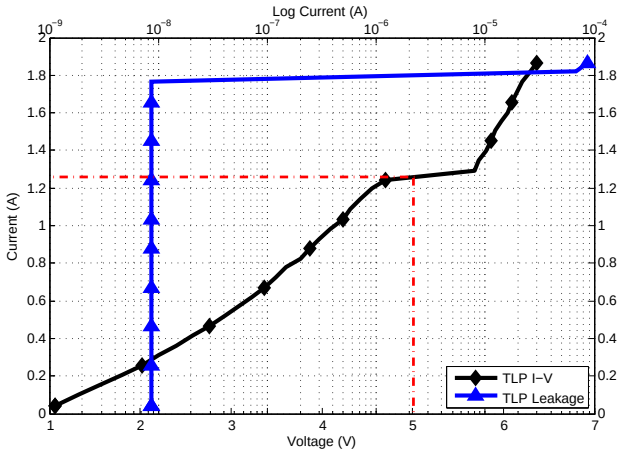


Figure 4.25: TLP measurement results of the proposed *NLDC* clamp.

4.2.3.1.3 HBM and CDM measurements: This clamp passes both +1.5 kV and −5 kV stresses, but fails to pass +1.75 kV and −5.25 kV stresses. In CDM measurement, the chip that includes the clamp is stressed by both positive and negative voltages in 50 V step sizes. In the positive CDM stress, the V_{SS} node is grounded to zap the device, while in the negative CDM stress the V_{DD} node is grounded. The *NLDC* clamp passes both +850 V and −400 V stresses, but fails to pass +900 V and −450 V stresses.

4.2.3.2 Normal operating conditions

4.2.3.2.1 Immunity to false triggering: The measurement setup described in section 3.2.3.2.1 was used for this design. Fig. 4.26 presents the fast power-on condition in which it can be seen that the *NLDC* design does not falsely trigger with the fast power-on condition. It is clear from the figure that the clamp does not trigger as the current flows (I_{DUT}) goes high to 600 μA then it goes back to the leakage current level.

4.2.3.2.2 Leakage vs. temperature: The same configuration described in section 3.2.3.2.2 was used to measure the leakage current as a function of temperature. Fig. 4.27 shows the measured leakage current of the *NLDC* design up to 80^oC and the simulated leakage current of the *NLDC* design up to 125^oC as a function of temperature. As shown

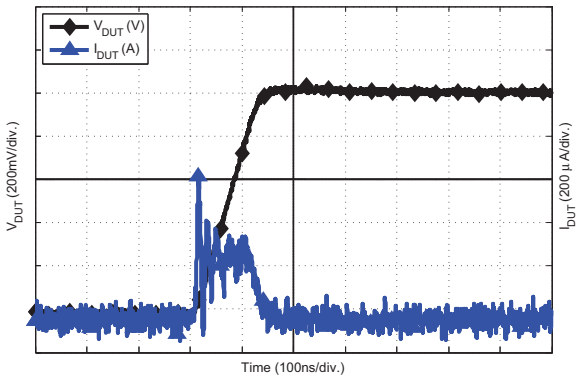


Figure 4.26: The *NLDC* under a fast power-on condition with 1 V voltage pulse and 100 ns rise-time.

in Fig. 4.27, the trend of both the fabricated design and the simulated structure is similar in the temperature range from 25^oC to 80^oC and that is expected to continue when the temperature is above 80^oC. Based on the measurement results, the *NLDC* clamp has a leakage current of 14.3 nA, and 75.1 nA at 25^oC and 75^oC, respectively.

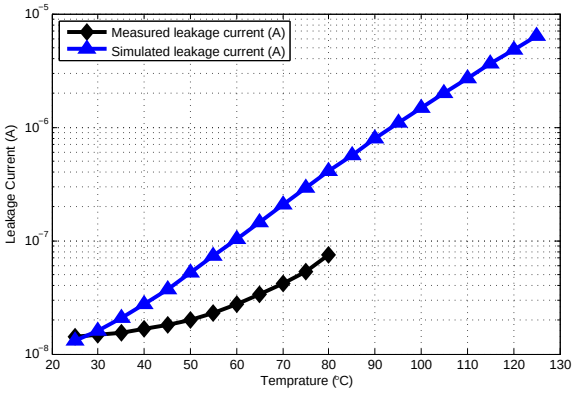
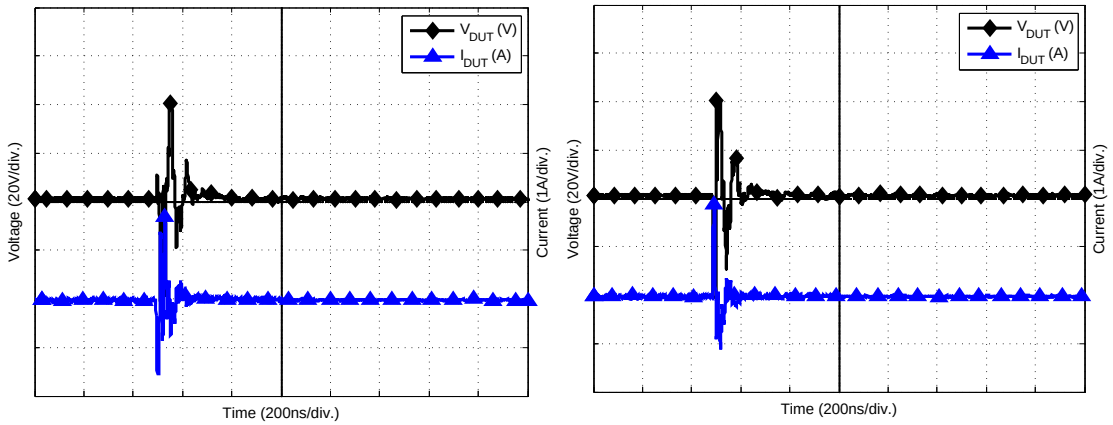


Figure 4.27: The measurement and simulation results of leakage vs. temperature for *NLDC* clamp.

4.2.3.2.3 Immunity to transient induced latch-up: The same configuration described in section 3.2.3.2.3 was used to evaluate the stability of the proposed design against

the transient induced latch-up. Fig. 4.28 (a) presents the *NLDC* design under a positive transient-induced latch-up with V_{charge} of $+210\ V$, while Fig. 4.28 (b) presents the *NLDC* design under a negative transient-induced latch-up with V_{charge} of $-210\ V$. Fig. 4.28 clearly shows that the *NLDC* design is immune against latch-up due to transient-induced noise with V_{charge} $\pm 210\ V$ as the current (I_{DUT}) goes back to the leakage current level after the transient-induced noise is gone.



(a) $V_{charge} = 210\ V$. (b) $V_{charge} =$ - $210\ V$.

Figure 4.28: The *NLDC* design under TLU with different V_{charge}.

4.3 Comparison between the proposed clamps

In this section, the four proposed designs in this thesis, the standalone clamps (PTC and DTC) and the hybrid clamps (PTDC and NLDC), are compared with each other. Both of *DTC* and *PTC* were designed to provide a protection to the circuit core against ± 125 V CDM stress through limiting the voltage between the two power rails to less than the oxide breakdown voltage of the core transistors, $BVOX_{ESD} = 5\ V$. On the other hand, the hybrid clamps were designed to be able to provide higher protection level, protection against $\pm 300\ V$ CDM stress. The protection against $300\ V$ CDM stress was achieved using the pi-network in which two clamps are connected in parallel, the primary and secondary

clamp. As a result, the total area of the hybrid designs is less than the area of the standalone clamps, but the standalone clamps offer a lower leakage current. Table 4.3 presents layout area of the four designs and the measured leakage current of the different designs under two different temperatures.

Design	PTC	DTC	$PTDC$	$NLDC$
$I_{leakage}$(nA)@25^oC	0.473	0.18	124	14.3
$I_{leakage}$(nA)@75^oC	13.4	5.77	1760	75.1
Area (μm^2)	3552	3221	2041	2227

Table 4.3: Area and measured leakage current of the proposed designs.

It was expected that the hybrid clamps to have a higher leakage current especially at higher temperature as diode string was used as the secondary clamp. The $PTDC$ has the highest leakage among the proposed clamps because the diode string as well as the parasitic D_{SB} diode. As the hybrid clamps have a higher leakage when the temperature is more than 50^oC, they can be used in applications where the area is the concern not the leakage current. The standalone clamps consume almost $1.5x$ the area of the hybrid clamps because large thick oxide transistors are used as the clamping element, whereas the area of the clamping element is reduced in the hybrid clamps where diodes and MOS transistors compose the clamping element.

The measurement results showed that all of the proposed clamps are immune against false triggering, and transient induced latch-up. Also, all of the four designs have reacted to the 4 V ESD-like pulse voltage under both chip not powered and powered conditions and after the stress ends the designs turned on. Thus, the proposed designs are robust against latch-up due to ESD-like stress under chip powered. The TLP result of the four designs is summarized in Table 4.4. As shown in Table 4.4, standalone clamps offer the higher current capability since large MOS transistors have been used as the clamping element; as a result, they have a smaller on-resistance compared with the hybrid clamps. Also, it is clear from Table 4.4 that all of the four proposed designs meet the minimum design requirement of the ESD protection circuit in the 65 nm CMOS technology (i.e. HBM protection level of 1.5 kV).

	PTC	*DTC*	*PTDC*	*NLDC*
$I_{FAILURE}$ (A)	3.82	3.21	2.95	1.82
$I_{@V=5V}$ (A)	1.60	1.82	1.24	1.29
R_{ON} (Ω)	2.63	2.33	3.76	2.97
Expected HBM protection Level (kV)	2.4	2.7	1.85	1.93

Table 4.4: Figures of merit for TLP measurement results.

4.4 Comparison with state-of-the-art ESD power supply clamps in 65 nm technology

Table 4.5 presents the comparison results of the proposed clamps with the state-of-the-art clamps in GP 65 nm CMOS technology. Both standalone clamps offer lower leakage current compared with the state-of-the-art ESD power supply clamps in 65 nm technology, while the hybrid clamps have a leakage current in the same order of magnitude as the state-of-the-art ESD power supply clamps in GP 65 nm technology. In addition, all of the proposed clamps have a comparable layout area, ESD protection level, and on-resistance compared with the state-of-the-art ESD power supply clamps in GP 65 nm technology.

Design	area (μm^2)	Leakage current (nA)			I_{t2} (A)	$I_{@V=5V}$ (A)	V_t (V)	V_h (A)	R_{on} (Ω)	ESD level			
		25^oC	75^oC	125^oC						+ HBM (kV)	- HBM (kV)	+ CDM (V)	- CDM (V)
PTC	3552	0.494	13.4	-	3.82	1.6	-	-	2.63	3.25	1.75	800	550
DTC	3221	0.18	5.77	–	3.21	1.82	3.3	1.5	2.33	3.5	4.5	700	450
PTDC	2041	124	1760	-	2.95	1.24	1.9	1.5	3.76	4.5	2.25	800	450
NLDC	2227	14.3	75.1	-	1.81	1.29	-	-	2.97	1.5	5	850	300
[52]	765	80	200	1080	2.25	1.75	4	2	2.66	4	-	-	-
[54]	3375	358	500	1810	2.5	1.5	3	2.5	2.86	4	-	-	-
[55]	-	116	350	1080	5	2.25	5	2	2.44	> 8	-	-	-
[58]	2025	165	-	1110	2.3	0.6	3	2.5	6.29	3	-	-	-
[59]	1051	1.43	-	-	2.74	2.1	3.86	2	1.77	5	-	-	-
[60]	1530	16.2	-	680	2.64	1.8	3.79	2	2	5	-	-	-

Table 4.5: Comparison of the proposed clamps with other published clamps in 65 nm technology.

Chapter 5

Conclusions and Future work

As the ESD event happens, it balances the charge between two objects and leads to a high current in a very short time. As the current passes through an object, a voltage is developed across it and results in creating an electric field. Semiconductor devices are damaged by both the high current density and the high electric field [2]. The high current density damages the semiconductor devices through thin-file fusing, filamentation, and junction spiking [17]. The high electric field, on the other hand, can cause failure through a dielectric breakdown or a charge injection [17]. ESD protection for an IC is limited by the oxide breakdown (B_{VOXESD}), which is 5 V for 65 nm CMOS technology [7]. Therefore, it is important to design ESD protection circuits that are capable of preventing these failures. The target HBM protection level is 1.5 kV for 65 nm CMOS technology [7].

A whole-chip ESD protection scheme that consists of I/O protection and ESD power supply clamps are routinely used in ICs to protect them against ESD damage. The main goal of ESD protection circuits is to provide a low-resistive discharge path from any two pins in the chip. The circuit core is susceptible to ESD damage if there are only an ESD protection circuits at the I/O pads. The ESD clamp provides the discharge path for an ESD event that happens between the two power rails (PSD-mode, NDS-mode). The power supply clamp is also part of the discharge path for both PS-mode and ND-mode. As a result, it is important to have an effective ESD power supply clamp across the power supply rails [1].

All designs published in the general purpose 65 nm CMOS technology have used the SCR as the clamping element since the SCR has a higher current carrying capability compared to an MOS transistor of the same area [3]. The ESD power supply clamp should provide a low-resistive path in both directions to be able to deal with both PSD and NDS zapping modes. The SCR-based design does not provide the best ESD protection for the NDS zapping mode (positive ESD stress at V_{SS} with grounded V_{DD} node) since it has two parasitic resistances (R_{Nwell} and R_{Psub}) and one parasitic diode (the collector to base junction diode of the PNP transistor) in the path from the V_{SS} to V_{DD} rails. Furthermore, SCR-based designs are not suitable for application that exposed to hot switching or ionizing radiation [2]. In GP process, the gate oxide thickness of core transistors is reduced compared with LP process counterpart to achieve higher performance designs for high-frequency applications using 1 V core transistors and 2.5 V I/O option. The thinner gate oxide layer results in higher leakage current due to gate tunneling [4]. Therefore, using large thin oxide MOS transistors as clamping elements will result in a huge leakage current.

In this thesis, four power supply ESD clamps are proposed in which thick oxide MOS transistors are used as the main clamping element. Therefore, the low-leakage current feature is achieved without significantly degrading the ESD performance. Two different ESD power supply clamp architectures are proposed: standalone ESD power supply clamps and hybrid ESD power supply clamps. Two standalone clamps are proposed: a transient PMOS based ESD clamp with thyristor delay element (PTC), and a static diode triggered power supply (DTC). The standalone clamps were designed to provide protection to the circuit core against ± 125 V CDM stress by limiting the voltage between the two power rails to less than the oxide breakdown voltage of the core transistors, $BVOX_{ESD} = 5$ V. The large area of this architecture was the price for maintaining the low-leakage current and the adequate ESD protection. The hybrid clamp architecture was proposed to provide a higher ESD protection, against ± 300 V CDM stress, while reducing the layout area and maintaining the low-leakage feature. Two hybrid designs were proposed: PMOS ESD power supply clamp with thyristor delay element and diodes ($PTDC$), and NMOS ESD power supply clamp with level shifter delay element and diode ($NLDC$). In the hybrid clamp structure, two clamps are connected in parallel between the two power supply rails,

a static clamp, and a transient clamp. The static clamp triggers first and start to sink the ESD energy and then an RC network triggers the primary transient clamp to sink most of the ESD stress.

The simulation results showed that the proposed clamps are capable of protecting the circuit core against $\pm 1.5kV$ HBM and at least staging $\pm 125\ V$ CDM response. The measurement results showed that all of the proposed clamps are immune against false triggering, and transient induced latch-up. Also, all of the four designs have reacted to the $4\ V$ ESD-like pulse voltage under both chip not powered and powered conditions and after the stress ends the designs turn on. Thus, the proposed designs are robust against latch-up due to ESD-like stress under chip powered. Finally, TLP measurement results showed that the proposed designs meet the minimum design requirement of the ESD protection circuit in the 65 nm CMOS technology (i.e. HBM protection level of 1.5 kV).

It was expected that the hybrid clamps to have higher leakage current, especially at a higher temperature as diode string was used as the secondary clamp. The $PTDC$ has the highest leakage among the proposed designs is caused by the diode string as well as the parasitic D_{SB} diode. As the hybrid clamps have high leakage when the temperature is more than 50 ^oC, they can be used in applications where the area is the concern, not the leakage current. The standalone clamps consume almost $1.5x$ the area of the hybrid clamps because large thick oxide transistors are used as the clamping element, whereas the area of the clamping element is reduced in the hybrid clamps where diodes and MOS transistors compose the clamping element. Even though the hybrid architecture has a higher leakage current compared with the standalone counterpart, the leakage current of the $PTDC$ at room temperature is 124 nA that still orders of magnitude smaller than the leakage current of thin oxide transistor based clamp. Recall the example provided in section 1.3 in which a thin oxide transistor based transient clamp was used to protect an SRAM. The total simulated leakage current of these four clamps is 22 μA, which is about 12.8 % of the total leakage current of the entire design. Using four $PTDC$ clamps will results in a total leakage current of 496 nA, which will lead to reducing the total leakage of the circuit by 12.5 %.

5.1 Future work

As Darlington-based SCR (DSCR) provides high ESD protection level for the ESD protection circuit [1], DSCR can be used as the main component of a transient clamp. Also, as the ESD power supply clamps should provide a low-resistive path for both directions to be able to deal with both PSD and NDS zapping modes, dual SCR, and all direction SCR are an excellent candidate to be used as a clamping element in the ESD clamps. In System on Chip (SoC), analog and digital blocks with multiple supplies and ground pins are being integrated into the same chip. Therefore, designing an ESD protection circuit to protect all pins is becoming a big challenge. The ESD protection circuits should be able to provide the required ESD protection level along with keeping the analog blocks isolated from the digital ones.

With the evolving of the biomedical and wearable electronics, ESD protection design will face a different and more complicated challenge. The biomedical and wearable electronics have different semiconductor materials and different substrate materials. In addition, as these devices are in a direct contact with the human body, they are more susceptible to CDM caused failures. Another possible area of research is designing ESD protection circuits for thin-film transistor (TFT) based and flexible electronics applications. More aspects will impact the reliability of these applications, and one of these is the ESD-related failures.

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APPENDICES

Appendix A

Details of Test-Chip 1

- **Technology:** GP TSMC 65 nm CMOS
- **Design name:** ISCWTME1
- **Die size:** 1099 * 1110 μm^2
- **Package:** CQFP80A
- **CMC Run:** 1302CS

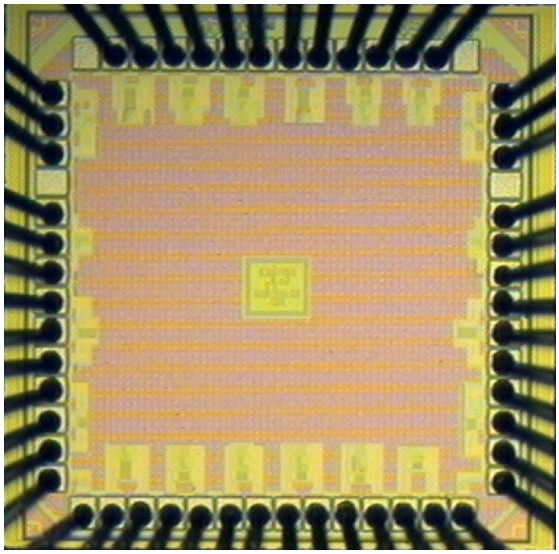


Figure A.1: Micrograph of test-chip 1.

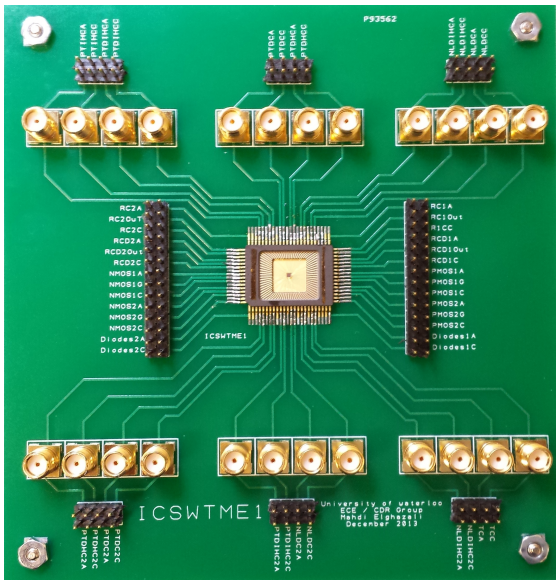


Figure A.2: PCB used to evaluate test-chip 1.

A.1 Implemented designs

A.1.1 Transient ESD clamps

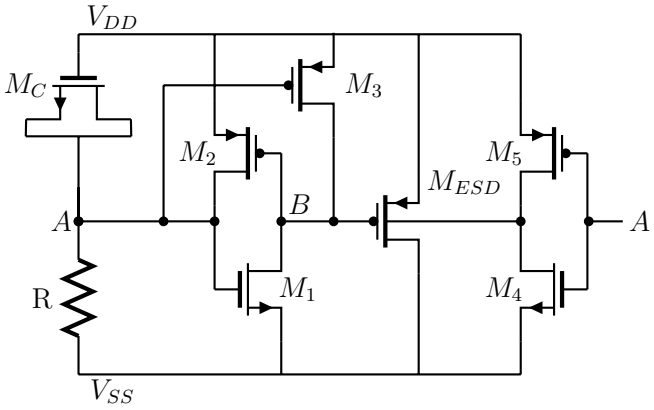


Figure A.3: Proposed: PMOS ESD clamp with thyristor delay element and inverter helper (PTIHC).

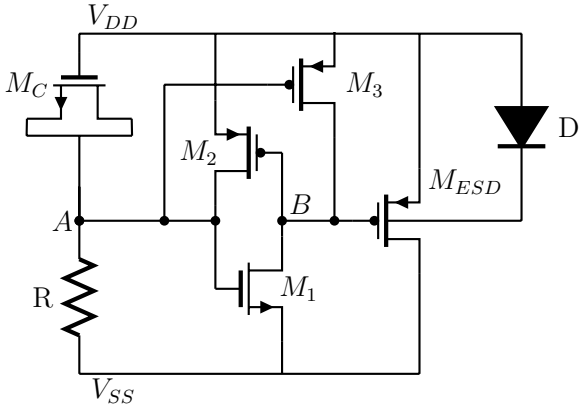


Figure A.4: Proposed: PMOS ESD clamp with thyristor delay element and diode helper (PTDHC).

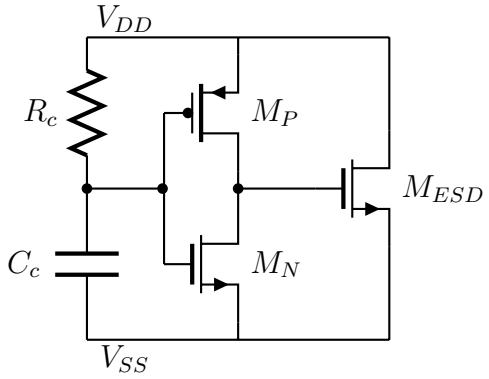


Figure A.5: Reference: Traditional transient clamp (TC)

A.1.2 Hybrid ESD clamps

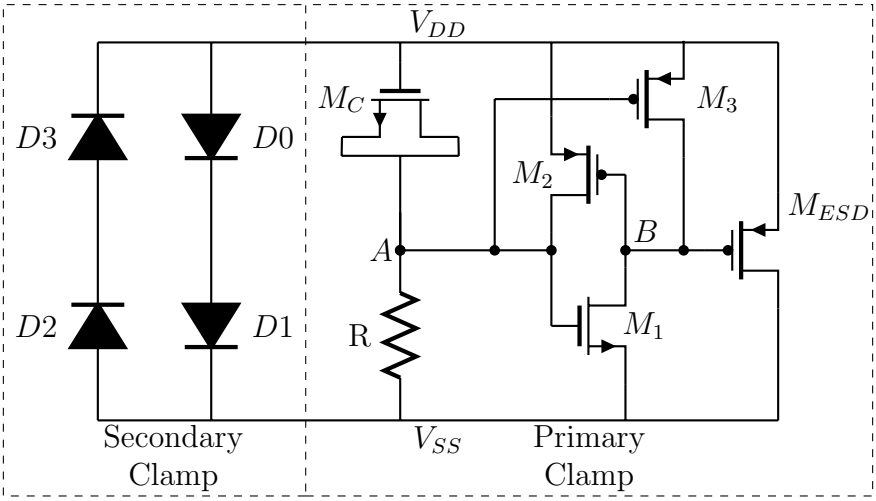


Figure A.6: Proposed: PMOS ESD clamp with thyristor delay element and diodes (PTDC).

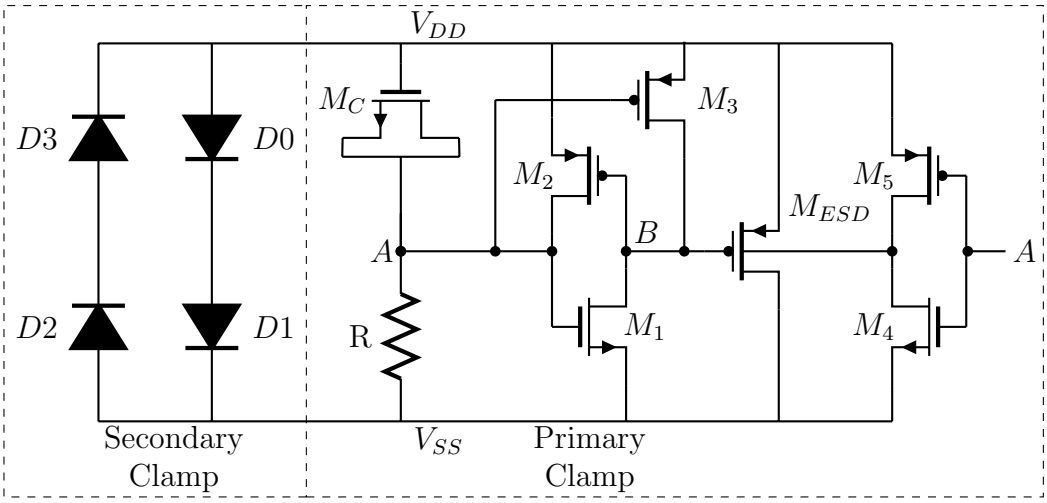


Figure A.7: Proposed: PMOS ESD clamp with thyristor delay element, inverter helper, and diodes (PTDIHC).

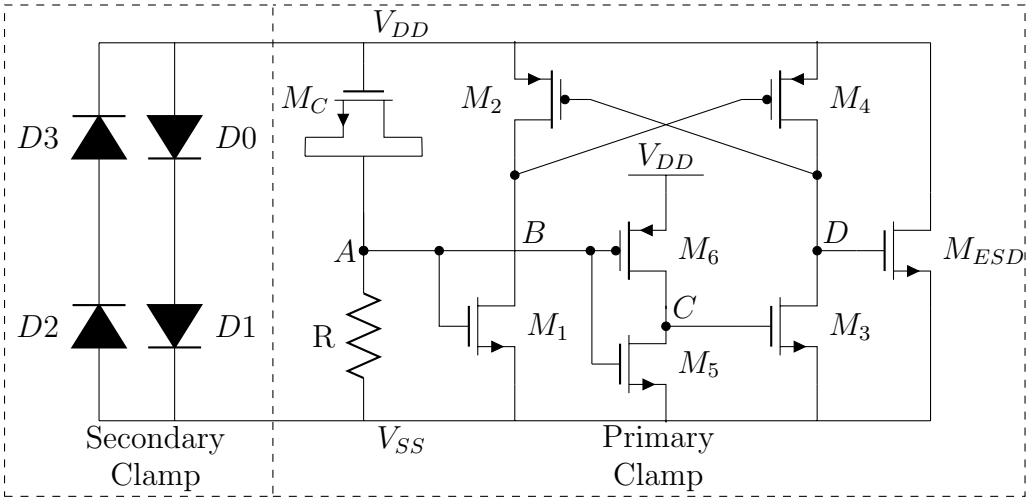


Figure A.8: Proposed: NMOS ESD clamp with level shifter delay element and diodes (NLDC).

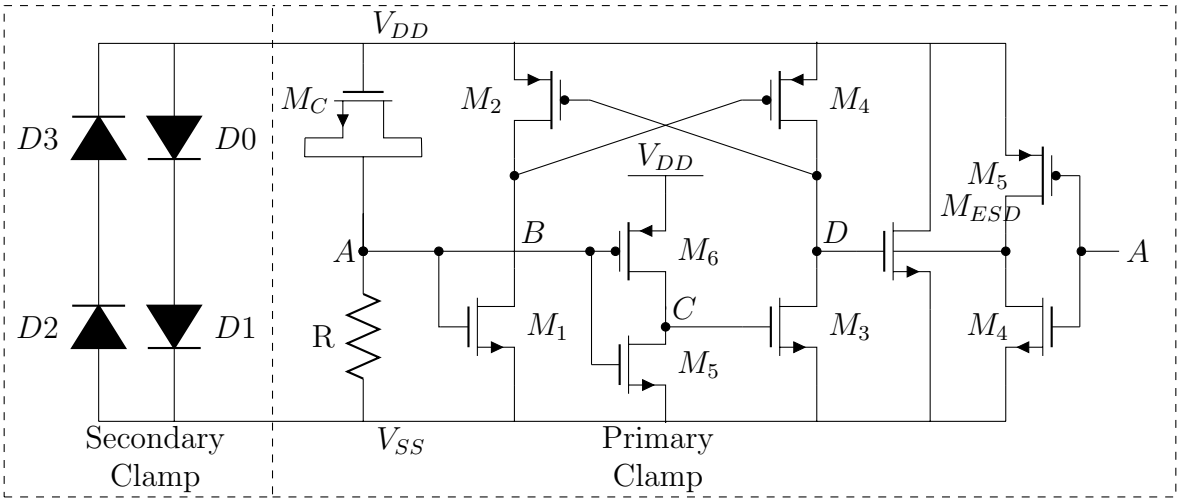


Figure A.9: Proposed: NMOS ESD clamp with level shifter delay element, inverter helper and diodes (NLDIHC).

A.2 TLP measurement results

Thick transistors are used in the designs end with two in Table A.1, while the other designs use thick transistor for the clamping element and thin transistor for the triggering circuit. Thin transistors are used in the traditional clamp (TC).

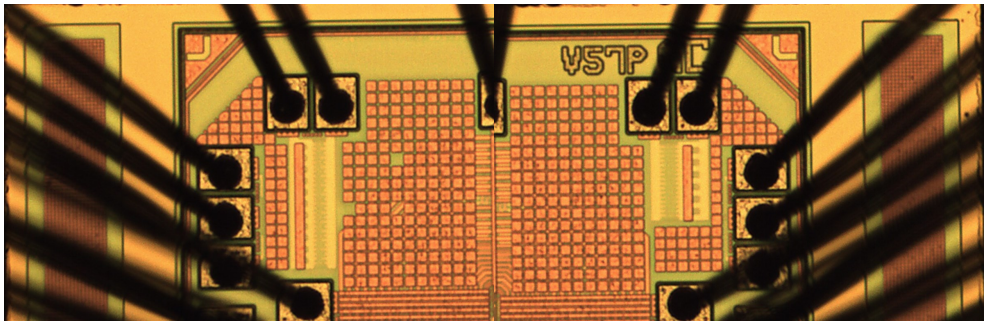
	Design	Layout Area (μm^2)	$I_{FAILURE}$ (A)	$I_{LEAKAGE}$ (μA)	R_{ON} (Ω)	$I_{@V=5V}$ (A)
1	PTIHC	1854	1.34	220000	7.78	0.49
2	PTDHC	1979	0.651	0.158	7.66	0.51
3	PTDHC2	2500	1.79	0.108	8.14	0.49
4	TC	1000	N/A	116000	–	–
5	PTDC	1932	1.09	0.125	4.52	0.66
6	PTDIHC	1932	1.25	0.0795	4.44	0.7
7	NLDC	1000	1.77	0.0129	4.56	0.7
8	NLDIHC	1000	2.15	0.238	2.34	0.68
9	PTDC2	2400	1.53	0.0659	7.78	0.49
10	PTDIHC2	2500	1.545	0.0329	4.12	0.72
11	NLDC2	2500	1.73	0.03	2.85	0.8
12	NLDIHC2	2500	2.1	0.106	2.72	0.83

Table A.1: TLP measurement results of test-chip 1.

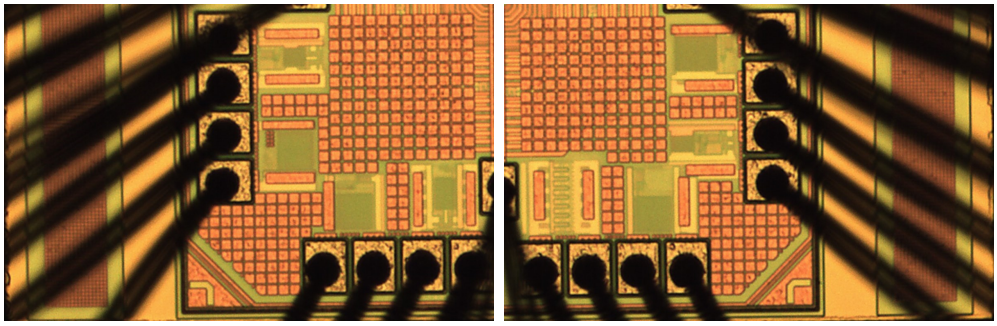
Appendix B

Details of Test-Chip 2

- **Technology:** GP TSMC 65 nm CMOS
- **Design name:** ISCWTMMT
- **Die size:** 1628 * 1744 μm^2
- **Assigned area (four corners):** 720 * 620 μm^2
- **Package:** CPG20809
- **CMC Run:** 1502CS



(a) NW corner. (b) NE corner.



(c) SW corner. (d) SE corner.

Figure B.1: Micrograph of test-chip 2.

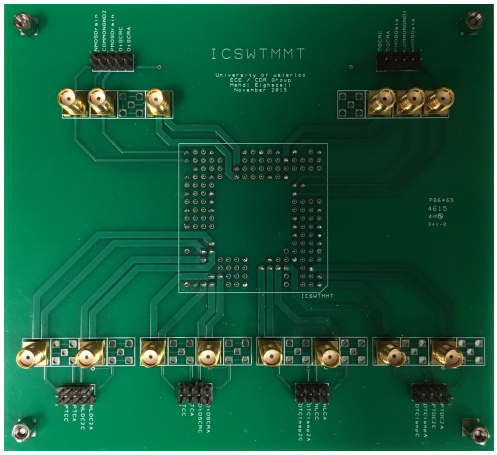


Figure B.2: PCB used to evaluate test-chip 2.

B.1 Implemented designs

B.1.1 Transient ESD clamps

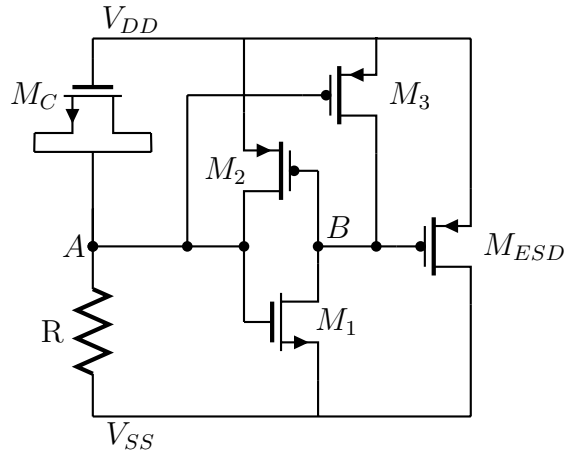


Figure B.3: Proposed: PMOS ESD clamp with thyristor delay element (PTC).

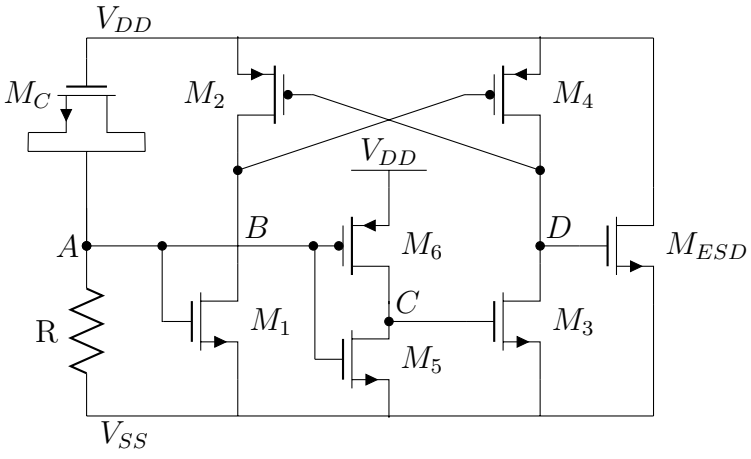


Figure B.4: Proposed: NMOS ESD clamp with level shifter delay element (NLC).

B.1.2 Static ESD clamps

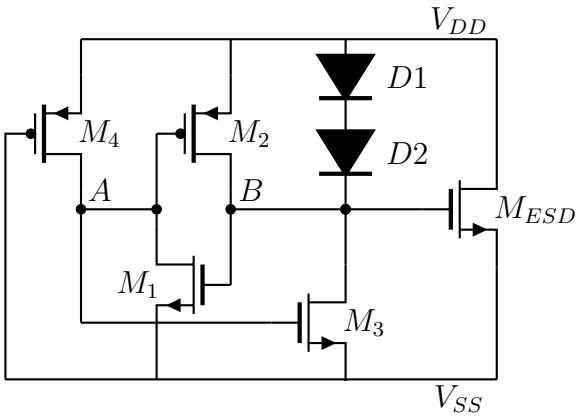


Figure B.5: Proposed: Diode triggered clamp (DTC).

B.1.3 Hybrid ESD clamps

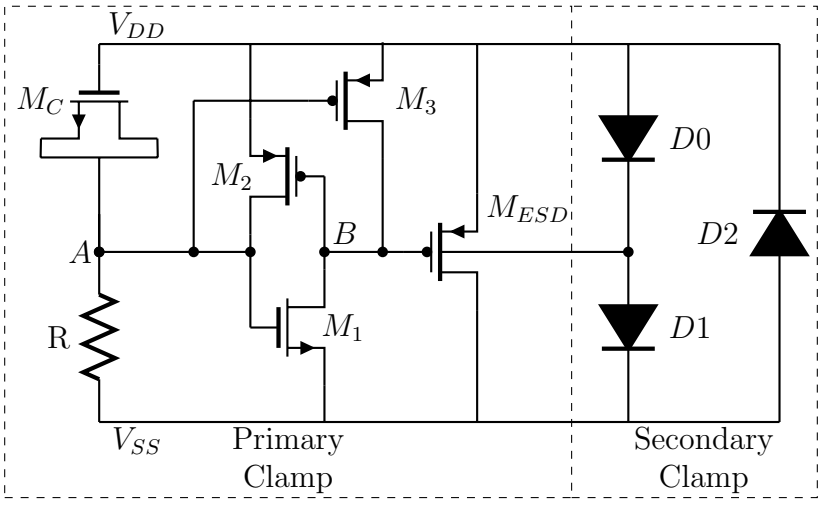


Figure B.6: Revised: PMOS ESD clamp with thyristor delay element and diodes (PTDC2).

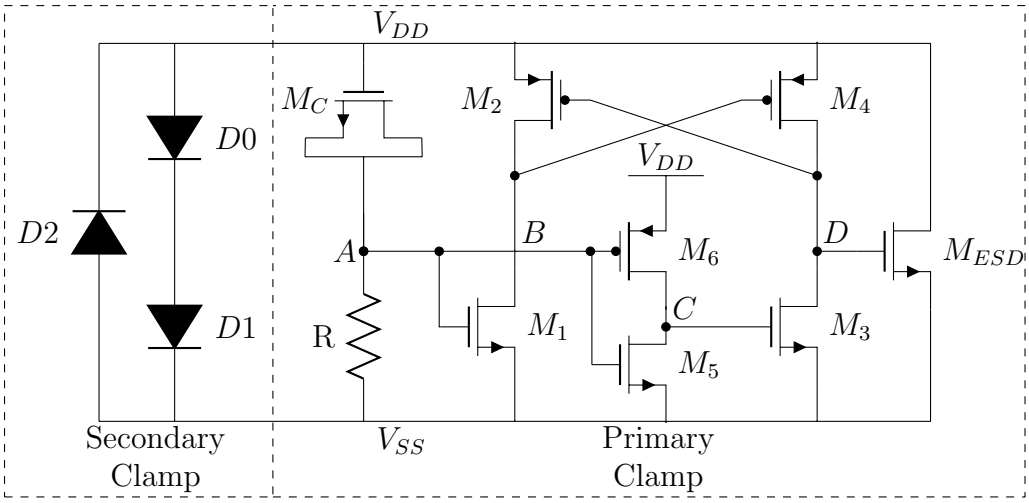


Figure B.7: Revised: NMOS ESD clamp with level shifter delay element and diodes (NLDC2).

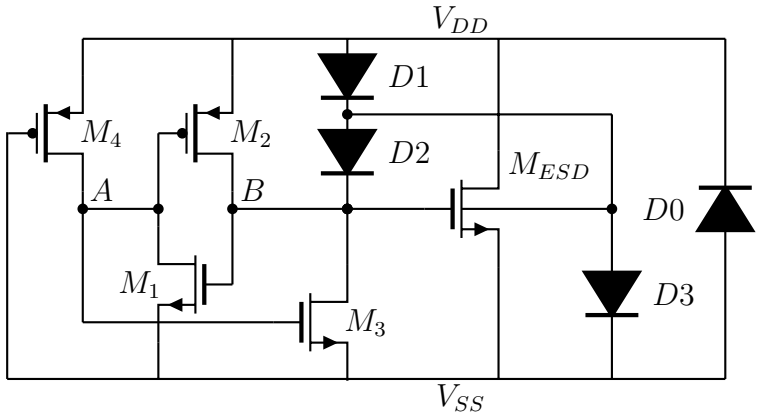


Figure B.8: Proposed: Diode triggered clamp (DTC2).

B.1.4 I/O ESD protection devices

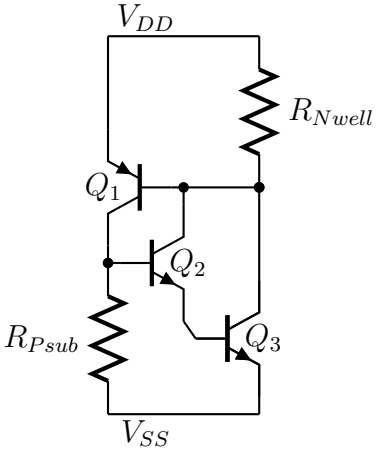


Figure B.9: Reference 1: Darlingington-based silicon controlled rectifier (DSCR).

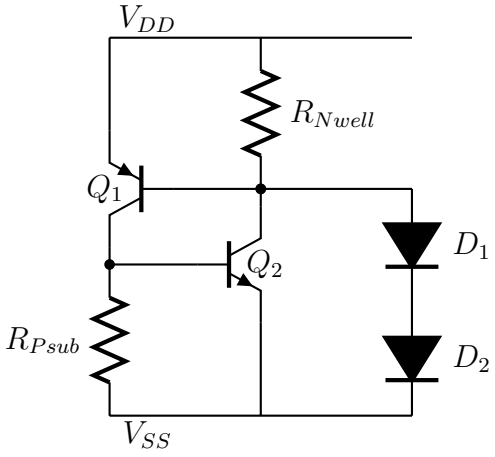


Figure B.10: Reference 2: Diode triggered silicon controlled rectifier (DtSCR).

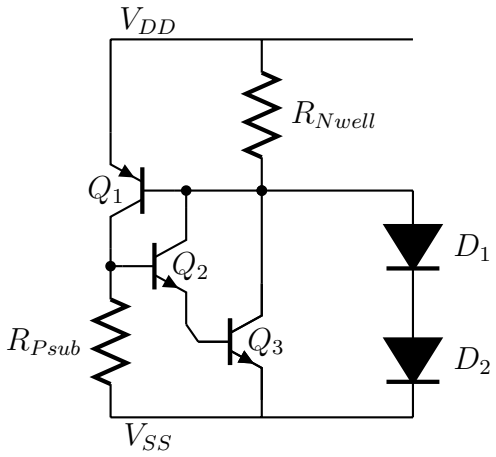


Figure B.11: Proposed: Diode triggered darlington-based silicon controlled rectifier (DtD-SCR).

B.2 TLP measurement results

	Design	Corner	Layout Area (μm^2)	$I_{FAILURE}$ (A)	$I_{LEAKAGE}$ (μA)	R_{ON} (Ω)	$I_{@V=5V}$ (A)
1	PTC	SE	3552	3.82	0.000502	2.63	1.6
2	NLC	SW	3479	0.37	0.01	1.85	2.14
3	PTDC2	SW	2040	2.95	0.124	3.76	1.24
4	NLDC2	SE	2227	1.81	0.00858	2.97	1.82
5	DTC2	SW	2560	3	38800	2.25	1.86
6	DTC	SW	3221	3.21	0.00018	2.33	1.82
7	DSCR	NW	1700	2.35	0.000035	2.34	–
8	DtSCR	SE	1700	3.4	20900	3.65	0.41
9	DtDSCR	NE	1700	3.3	16000	2.32	–

Table B.1: TLP measurement results of test-chip 2.