Physics Based Virtual Source Compact Model of Gallium-Nitride High Electron Mobility Transistors

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Gallium Nitride (GaN) based high electron mobility transistors (HEMTs) outperform Gallium Arsenide (GaAs) and silicon based transistors for radio frequency (RF) applications in terms of output power and efficiency due to its large bandgap (~3.4 eV@300 K) and high carrier mobility property (1500 – 2300 $cm^2/(V \cdot s)$). These advantages have made GaN technology a promising candidate for future high-power microwave and potential millimeter-wave applications.

Current GaN HEMT models used by the industry, such as Angelov Model, EEHEMT Model and DynaFET (Dynamic FET) model, are empirical or semi-empirical. Lacking the physical description of the device operations, these empirical models are not directly scalable. Circuit design that uses the models requires multiple iterations between the device and circuit levels, becoming a lengthy and expensive process. Conversely existing physics based models, such as surface potential model, are computationally intensive and thus impractical for full scale circuit simulation and optimization. To enable efficient GaN-based RF circuit design, computationally efficient physics based compact models are required.

In this thesis, a physics based Virtual Source (VS) compact model is developed for GaN HEMTs targeting RF applications. While the intrinsic current and charge model are developed based on the Virtual Source model originally proposed by MIT researchers, the gate current model and parasitic element network are proposed based on our applications with a new efficient parameter extraction flow. Both direct current (DC) of drain and gate currents and RF measurements are conducted for model parameter extractions. The new flow first extracts device parasitic resistive values based on the DC measurement of gate current. Then parameters related with the intrinsic region are determined based on the transport characteristics in the subthreshold and above threshold regimes. Finally, the parasitic resistance, capacitance and inductance values are optimized based on the S-parameter measurement. This new extraction flow provides reliable and accurate extraction for parasitic element values while achieving reasonable resolutions holistically with both DC and RF characteristics. The model is validated against measurement data in terms of drain current, gate current and scattering parameter (S-parameter).

This model provides simple yet clear physical description for GaN HEMTs with only a short list of model parameters compared with other empirical or physics based models. It can be easily integrated in circuit simulators for RF circuit design.

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List of Abbreviations

2DEG	2-Dimentional Electron Gas
ANN	Artificial Neural Networks
CAD	Computer Added Design
CPFC	Canadian Photonics Fabrication Center
CW	Continuous Wave
DC	Direct Current
DIBL	Drain Induced Barrier Lowering
DMM	Digital Multimeter
DUT	Device Under Test
EM	Electromagnetic
EVM	Error Vector Magnitude
FEM	Finite Element Method
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GCA	Gradual Channel Approximation
GSG	Ground-Signal-Ground
HEMT	High Electron Mobility Transistors
IC	Integrated Circuit
IMD3	Third-Order Intermodulation Distortion
ISS	Impedance Standard Substrates
I-V	Current-Voltage
LDMOS	Laterally Diffused MOSFET
LNA	Low Noise Amplifier
LTE	Long Term Evolution
LUT	Look-Up-Table
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PA	Power Amplifiers
PAE	Power Added Efficiency
PDK	Process Design Kit
QAM	Quadrature Amplitude Modulation

RF	Radio Frequency
SiC	Silicon Carbide
S-parameter	Scattering Parameter
SSM	Small Signal Model
TLM	Transmission Line Method
VNA	Vector Network Analyzer
VSM	Virtual Source Model

Chapter 1
Introduction

1.1 Background

Wireless communication systems have greatly changed our daily lives over the past several decades. With technology advancement, personal wireless communication has moved from low-data-rate voice-based communication in the 2nd Generation (2G) standard to high-speed data-based communication in the 4th Generation (4G) Long Term Evolution (LTE) standard, and towards even higher-data-rate in the next 5th Generation (5G) mobile network standard [1].

In the old days, high frequency and high power output were not of priority in personal wireless communications, and therefore the performance requirements for radio frequency (RF) circuits, especially the power amplifiers (PAs), were not stringent in terms of either device performance or circuit design techniques. Silicon based devices, such as Si-laterally diffused metal-oxide-semiconductor field-effect transistors (Si-LDMOS), were able to provide sufficient power output in base stations [2], while Gallium Arsenide (GaAs) high electron mobility transistors (HEMTs) were used to meet the low-power and small-size requirements in hand held devices [3, 4].

On the other hand, in modern wireless communication systems, frequency bands have moved from L and S-band to higher frequency bands (*e.g.,* X-band, K-band or even V-band) meanwhile high order modulation schemes (*e.g.,* 64QAM) have been widely used [5 - 8]. These changes have greatly improved the throughput of wireless communication systems, but they have also posed demanding performance requirements in RF circuits and systems in terms of power, efficiency, linearity, advanced circuit topologies and system architectures. To handle these increasingly strict design requirements, not only high-performance device technologies are needed, but also carefully constructed device models which are suitable for modern computer added design (CAD) tools are required.

The emerging GaN technology is promising for high power and high frequency power amplifiers design due to its competitive material properties, such as high bandgap, superior electron mobility and carrier velocity. The wide bandgap ($3.5\ \text{eV@300 K}$) allows for up to 100 V drain to source voltage without device breakdown, which enables GaN HEMTs having more than an order of power density than Si-based power devices and GaAs HEMTs [9]. The superior electron mobility (2300 $\text{cm}^2/(\text{Vs})$ @ 300 K) and carrier velocity ($2.1\times10^7\text{cm/s}$) makes it capable to operate even in W-band

(75 – 110 GHz) while delivering watt level power without significant power-combining circuitry [10].

In addition to process technologies, device models play a significant role in high-performance RF circuit design [11, 12]. Currently, due to the sustainable development of electromagnetic (EM) CAD software, general passive devices used in RF circuits are well modeled with simple and precise descriptions [13, 14]. However, the models for active devices, such as diodes and transistors, are modeled with less satisfaction for circuit design in terms of both accuracy and computation efficiency due to the nature of multi-physics-dependent device nonlinear behavior. Therefore, the limitations and trade-offs of the existing models are discussed.

Compact models refer to device models used for integrated circuit design in circuit simulation [15]. Based on the model formation, the existing compact models for RF transistors can be divided into two categories, the empirical models and the physics based models. The empirical models for GaN HEMTs, such as Angelov model, EEHEMT model and DynaFET (Dynamic FET) model, use analytical functions with fitting parameters or artificial neural networks (ANNs) [16 - 18] to empirically describe the current and charge behaviors at each terminal. These empirical models usually have simple parameter extraction routine and are easy to implement in circuit simulators. Furthermore, due to the close-form property of empirical functions and ANNs, these models are computational efficient, making them widely used in commercial CAD software for circuit design [17]. However, the equations in empirical models do not represent the operating principles of the device and do not allow direct linkage between device parameters and circuit level performance. Moreover, the empirical models are usually fitted to measurement data with non-physical fitting parameters, which are not scalable with geometry, biasing and/or temperature. This often means only very limited device dimensions are available with each technology library with reasonable accuracy for circuit design. To adopt other device dimensions beyond the default dimensions requires lengthy recalibration. Furthermore, different characteristics in the empirical models are usually modeled using independent equations and different sets of parameters which are fitted through different sets of measurement data, leading to inconsistency of model behaviors.

Another category is the physics based models, which is the counterpart of the empirical models in modeling ideology. These models solve equations from basic semiconductor laws, such as Schrodinger equations and Poisson's equation, to describe the behavior of the transistors. The most widely adopted semiconductor physics based model is the surface potential model. It solves the

Poisson's equation and Schrodinger equations iteratively to determine the potential and electric field of the channel and thereafter calculate the drain current by the carrier drift-diffusion theory [18, 19]. The equations in the model are semiconductor physics based, which have two major advantages. First, it provides a more consistent and sometimes more accurate global fittings than the empirical models not only in static behaviour but also its derivatives, such as tranconductance and third-order intermodulation distortion (IMD3) [20], due to the universal applicability of physics laws. Second, after the physics parameters are extracted, the model is inherently scalable with geometry, biasing and other physical dimensions [21], which makes the device optimization for circuit performance improvement much easier and straightforward. However, the physics based model are not without shortcomings. The semiconductor equations are usually open-form, which need iterations for solving the equations [18 - 21]. Therefore, one major issue with physics based models is that they are generally computationally intensive. They are time consuming in simulation and usually not simple to implement in circuit simulators.

1.2 Motivation

With the stringent performance requirements of the frequency, power and linearity in modern communication systems, the designing complexity of RF circuits is escalating, which requires more advanced models. This model advancement has three aspects in motivating our research.

First, the high frequency and high power application scenarios require the transistor model to be accurate under both conditions, while the high order modulation schemes pose linearity requirements that some significant nonlinear behaviors, such as gate leakage, triode region drain current and sub-threshold drain current, should be considered carefully in the modern model.

Second, the goal for modern transistor modeling is not only to accurately model the behavior of the transistor, but also enable the best performance of the entire system. Achieving this goal requires physics based compact models. Physics based models provide designers circuit-level element representation of the device, which enables device optimization, such as layout parasitic optimization for the optimum device performance. Furthermore, physics based models potentially support device-circuit interactive design, which optimizes the RF circuit and device as a holistic system. Therefore, it is important and necessary to implement physics-based description of transistor behaviour in modern transistor modeling techniques.

Third, the design procedure for modern RF circuit is usually an iterative and optimization based procedure, in which the computational complexity of the model significantly affects the time and labor cost of RF circuit design. Semiconductor-level physics based models, such as surface potential based models, are usually computationally expensive and not suitable for circuit design. Circuit-level element based models usually implement equivalent circuits and close-form current sources to describe the electrical behavior of the model, which is computational efficient without sacrificing accuracy significantly. Therefore, circuit-level element based models are more preferable for RF circuit design.

Based on the discussion in background and motivation section, the research objective is stated below.

1.3 Research Objective

This thesis has two major research objectives. First, to propose a physics based GaN HEMT compact model that meets the requirements for computational efficiency and simulation accuracy in RF circuit design. Second, to develop a complete model parameter extraction workflow and validate the model accuracy against measurement data.

1.4 Thesis Organization

The organization of the thesis is as follows. In chapter 2, a literature review of existing empirical compact models and physics based compact models is presented. In addition, the limitations and trade-offs of empirical compact models and physics based compact models are discussed.

In chapter 3, a physics based device model partition scheme is proposed which consists of several models according to their physical origins, including the probing pad model, parasitic model and intrinsic model. Base on the model partition scheme, detailed modeling scheme for each module is discussed in details.

In chapter 4, the full model parameter extraction flow for each module is demonstrated with measurement data of two GaN HEMT samples. The modeled drain current, gate current and small signal S-parameters of the transistor are validated by comparing them to the measured data. The normalized error of the model is presented and discussed.

Finally, in chapter 5, summary and conclusions of the thesis are presented. Future work is also discussed.

Chapter 2
GaN HEMTs Compact Models: An Overview

Device models play a significant role in high-performance RF circuit design. As GaN technology matures in terms of process and fabrication, an increasing number of GaN compact models are developed and adopted. The main focus of this chapter is the literature review of the existing GaN HEMT compact models. Several important empirical and physics based GaN compact models are introduced in this chapter and the limitations and trade-offs of the compact models are discussed.

2.1 Empirical Compact Models

Empirical compact models focus on the selection and combination of mathematical functions to numerically fit the behavior of the model to measurement data. In many cases, such mathematical functions do not carry any physical explanation for the device behavior. Historically, III-V empirical models were originally formulated to cater to GaAs-based technologies for RF-applications. As GaN technology matures in terms of process and fabrication, these empirical models are adopted to GaN devices. The Angelov, EEHEMT and DynaFET models are well-known empirical models and widely used in industry. An overview of these models is given in the following section, highlighting the modeling approaches and the limitations.

2.1.1 Angelov Model

The Angelov model was an empirical model first proposed by Prof. Iltcho Angelov in 1992 for GaAs MESFETS and HEMTs [22] and later extended for GaN HEMTs as Angelov-GaN model [23, 24]. The model was developed with an emphasis on nonlinear fitting of drain current and its derivatives. The equivalent GaN circuit of Angelov-GaN model is shown in Figure 2.1.

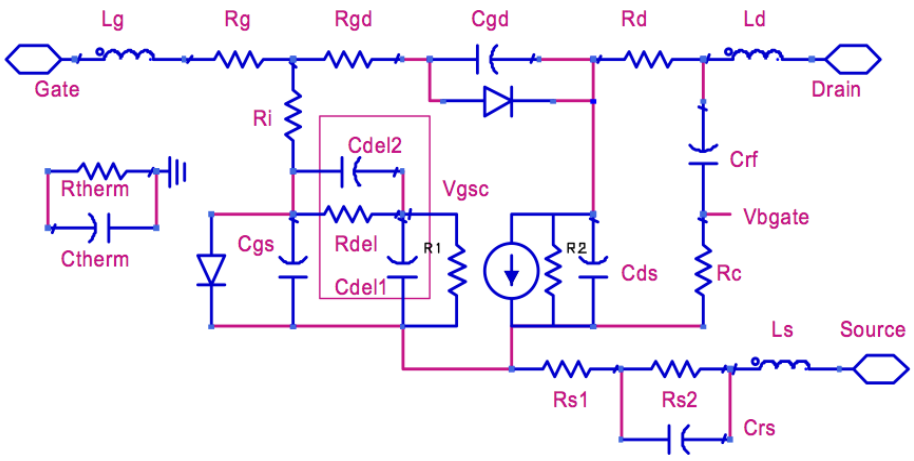

Figure 2.1 Equivalent circuit of Angelov-GaN model [24]

The core equations of Angelov-GaN model include those describing drain current (I_{DS}), gate current (I_{GS}, I_{GD}) and nonlinear capacitors (C_{gs}, C_{gd}, C_{ds}). Observation of drain current, gate current and nonlinear capacitance have shown that they usually exhibit a hyperbolic tangent shape with respect to gate voltage while their tranconductance exhibit a bell shape, and therefore $tanh(x)$ function is selected as the core empirical fitting function. Figure 2.2 gives an example of the shapes of drain current (I_{ds} in the figure) and transconductance (G_m) published for the Angelov-GaN model [25].

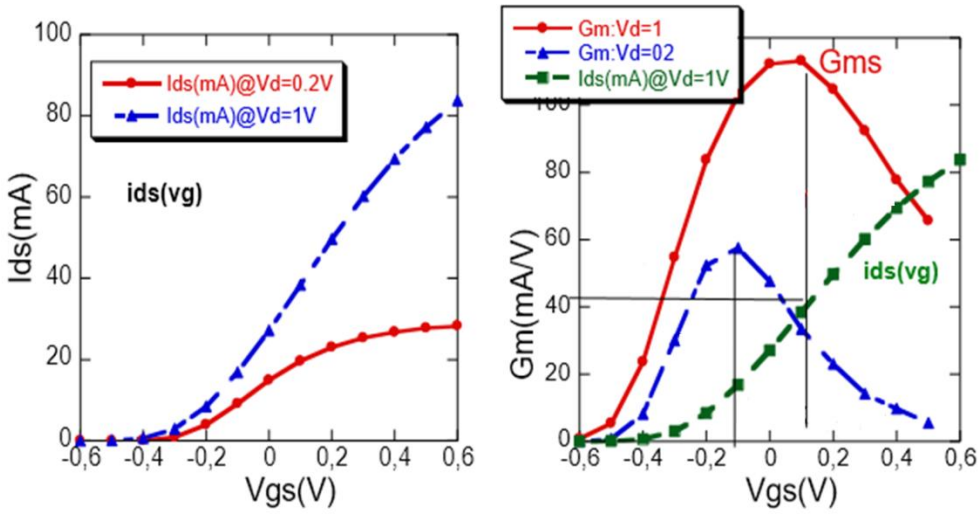

Figure 2.2 Shapes of drain current (I_{ds}) and its derivative (G_m) as an example in Angelov-GaN model extraction [25]

The drain current is modeled by the product of V_{GS} dependent term and V_{DS} dependent term, which is as follows [22, 25]

$$I_{ds} = I_{pk}(1 + \tanh(\psi))(1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \tag{2.1}$$

I_{pk} is the drain current at the bias corresponding to the maximum transconductance g_{mpk}. λ is the coefficient for modeling drain induced barrier lowering (DIBL). ψ is modeled as a power series at peak g_m point as shown below [22, 25].

$$\psi = P_1(V_{gs} - V_{pk}) + P_2(V_{gs} - V_{pk})^2 + P_3(V_{gs} - V_{pk})^3 \cdots \tag{2.2}$$

V_{pk} is the gate voltage for maximum g_{mpk}. Here more empirical fitting parameters (P_1, P_2, P_3 ...) are added for fitting gate-source voltage dependence.

The terminal charge is modeled by empirically fitting the nonlinear capacitance to the measured capacitance by the following equations [22, 25]

$$C_{gs} = C_{gso}[1 + \tanh(\psi_1)][1 + \tanh(\psi_2)] \tag{2.3}$$

$$C_{gd} = C_{gdo}[1 + \tanh(\psi_3)][1 - \tanh(\psi_4)] \tag{2.4}$$

More fitting parameters ($\psi_1, \psi_2, \psi_3, \psi_4$) are introduced here to fit the capacitance model. According to [12], about 90 parameters in total are used for Angelov-GaN model. Based on the large number of fitting parameters, the model is capable to capture the nonlinear current and charge, trapping effect and self-heating effect. However, large number parameter extraction is time and effort consuming. The independency of fitting parameters (such as the set of P and ψ shown above) in I-V equations could cause model inconsistency. Furthermore, the model is non-speculative since it is not physics based. The model construction cannot provide any physical insights to the device engineers or circuit designers. Any process or geometry change made to the device needs re-fitting of the model.

2.1.2 EEHEMT Model

The EEHMET model is developed by Keysight Technologies for GaAs and GaN HEMT for RF applications. EEHEMT model divides the drain current into three portions – DC current (I_{DC}), displacement current (I_{AC}), and dispersion current (I_{dbp}) and calculates the sum of the three portions as drain current [26, 27]. The equivalent circuit of EEHMET model is shown in Figure 2.3.

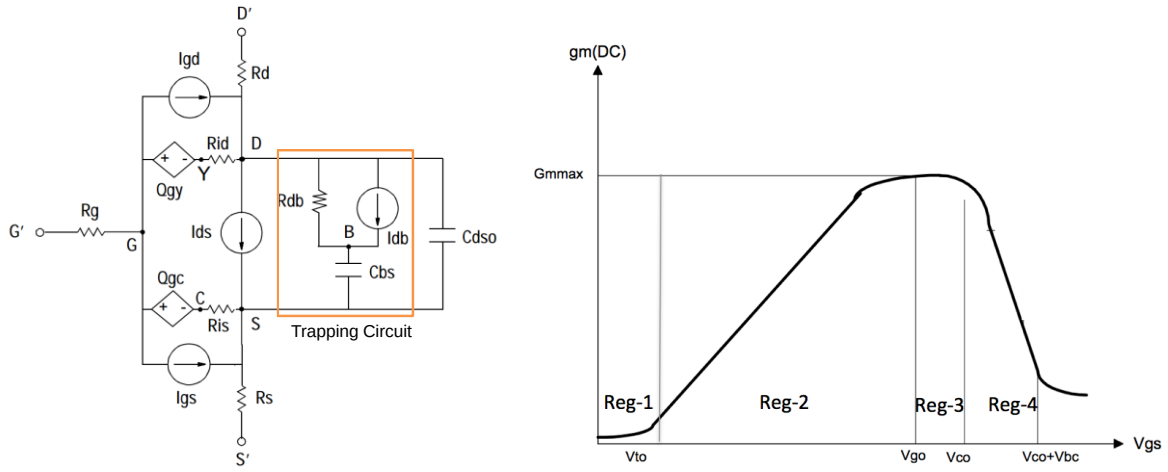

Figure 2.3 Equivalent circuit of EEHMET model (left) and piecewise regions of transconductance (right) [27]

The DC drain current is modeled in a similar way as Aneglov model, which uses $tanh(x)$ function to fit the $I_{DS} - V_{DS}$ dependence as follows [26, 27]

$$I_{DC} = I_1(V_{gs}) \cdot I_2(V_{ds}) \cdot \tanh(\alpha V_{ds}) \tag{2.5}$$

$I_1(V_{gs})$ and $I_2(V_{ds})$ are sophisticated piecewise empirical functions based on the piecewise regions of transconductance (Figure 2.3) without physical explanations.

The displacement current (I_{AC}) is modeled by the charging and discharging current of charge source Q_{gy} and Q_{gc} as follows:

$$I_{AC} = \frac{dQ_{gy}}{dt} + \frac{dQ_{gc}}{dt} \tag{2.6}$$

$$Q_{gy} = \left(q_g(V_{gc}, V_{gc} - V_{gy}) - \gamma V_{gc}\right) \cdot f_2 + \gamma V_{gy} \cdot f_1 \tag{2.7}$$

$$Q_{gc} = \left(q_g(V_{gc}, V_{gc} - V_{gy}) - \gamma V_{gy}\right) \cdot f_1 + \gamma V_{gc} \cdot f_2 \tag{2.8}$$

In these equation, q_g is the gate effective capacitance. V_{gc} and V_{gy} are voltage between internal nodes. More fitting parameters (f_1, f_2, γ) are introduced in the above equations, where detailed explanations can be found in the EEHMET model user manual [27].

The gate current (I_{gs}, I_{gd}) is modeled by the standard 2-parameter diode model, in which the non-ideality effects of the diode are not considered. The trapping effect is modeled by an RC network and a current source between drain and source terminal to mimic the measured trapping behaviour.

Dispersion current (I_{dbp}) is modeled by excluding the DC and displacement current portion from the measured current and piecewisely fit the residue by $\tanh^{-1}(V_{ds})$ function after the parameters for DC and displacement current are determined.

EEHMET model has become an industry standard and been integrated in Agilent's (now Keysight) Advanced Design System (ADS). EEHEMT model achieves better modeling accuracy than Angelov model due to its piecewise region strategy, but still a large number (71 instead of 90 for Angelov-GaN model) of parameters are adopted in the model. Although Keysight provides automatic parameter extraction software to save time and effort for model construction, its inherent empirical nature makes it not scalable with geometry and process.

2.1.3 DynaFET Model

The DynaFET ("Dynamic FET") model is proposed by Keysight technologies in 2014 for GaAs/GaN HEMTs. It uses large-signal waveform data of a GaAs/GaN HEMT together with I-V and S-parameter measurement data to extract a time-domain model that can be used for various circuit analyses, such as transient and harmonic-balance simulations [28].

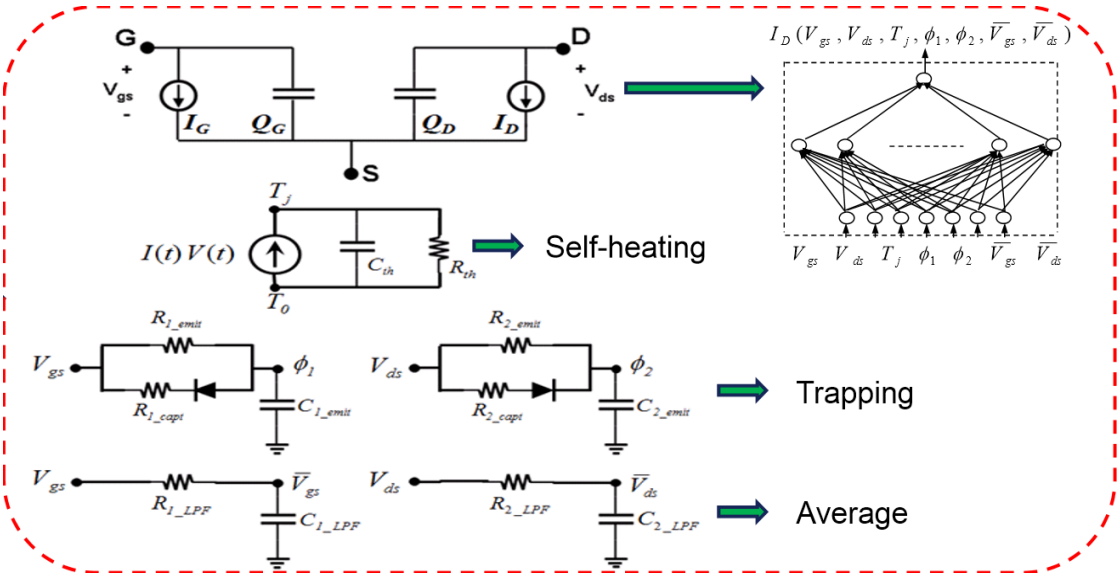

Figure 2.4 DynaFET model formation including sub-circuit (left) and artificial neural networks (right) [28, 29]

The formation of DynaFET model is shown in Figure 2.4. The DynaFET model exploits artificial neural networks (ANNs) and sub-circuits to model the behaviour of the device. The ANNs are used to formulate gate charge, gate current, drain charge and drain current while sub-circuits model specific behaviours of GaN HEMTs such as self-heating effect and trapping effect [28, 29].

The DynaFET model captures dynamic trapping/de-trapping processes in GaN HEMT by introducing two effective voltages, ϕ_1 and ϕ_2, representing gate trapping state and drain trapping state respectively through dedicated asymmetric RC networks [28]. The RC networks including an ideal diode are used to mimic the trapping behaviour that an increasing drain (decreasing gate) voltage propagates almost instantaneously to ϕ_2 (ϕ_1), whereas a decreasing drain (increasing gate) voltage hardly affects ϕ_2 (ϕ_1).

The self-heating effect is modeled using conventional first order RC thermal network. The thermal source is the total electric power generated inside the transistor. The thermal resistance and capacitance are related to material properties which can be determined by finite-element-method (FEM) simulation or from measurement.

The ANNs take the nodal voltage of the sub-circuits ($V_{gs}, V_{ds}, T_j, \phi_1, \phi_2, \overline{V_{gs}}, \overline{V_{ds}}$) as input to the neuron networks and use the measured large signal waveform to train the weight of each neuron in the network. Weights of all neurons in the ANNs are iteratively adjusted during the training process until ANNs' output (such as terminal current) agrees with measurement data within an acceptable tolerance.

DynaFET model has achieved good results in DC, S-parameter, harmonic, intermodulation distortion, and loadpull simulation over a very wide range of bias conditions, complex loads, powers, and frequencies [29]. Besides, using $tanh(x)$ as the transition function, DynaFET model is infinitely differentiable and computationally efficient, which is critical for harmonic balance simulation.

DynaFET model is not without its drawbacks. Although DynaFET model is computational efficient in simulation, large-signal waveform measurement and the model training take a large amount of time and effort. Besides, although trapping and self-heating equivalent circuit are included for modeling the trapping and self-heating effect, the relation between terminal voltages, currents and charges are still modeled by empirical ANNs without physical explanations, which inherits all the limitations empirical models have.

2.2 Physics Based Compact Models

Another approach of device modeling is the physics based compact models. This approach analyzes the cause of the behavior in the devices based on semiconductor physics such as material characteristics and carrier transport. The equations in physics based compact models are physical, often with a much smaller number of parameters than empirical models. These physical parameters can not only be extracted from one's measurement, but also be taken from other independent sources, which saves time and effort in model construction. The Tsinghua-HKUST model and ASM-HEMT are well-known models based on the surface potential while NCSU model is based on the simple gate charge control and drift-diffusion theory. These models are introduced in the following as representatives of physics based models.

2.2.1 Tsinghua-HKUST Model

The Tsinghua-HKUST model is a surface potential based model for GaN HEMTs. Its current-voltage model is proposed by X. Cheng and Y. Wang at Tsinghua University in 2011 [30]. The charge model is extended later by A. Zhang and K. Chen at HKUST in 2014 [31].

The idea of Tsinghua-HKUST surface potential model is directly inspired from the band diagram of AlGaN/GaN HEMT, which is shown in Figure 2.5. High-density 2DEG forms at the heterointerface of AlGaN/GaN due to the discontinuity of the conduction band and polarization-induced charge at the interface. The sheet carrier density n_s, Fermi-potential E_F and surface potential φ_s are obtained by iteratively solving the Poisson's and Schrodinger equations along the channel [30].

Applying gradual channel approximation (GCA) and drift-diffusion theory, simple and clear current-voltage relationship can be obtained for the model [30]. The current-voltage equation is verified to be valid over a wide bias and temperature range. By self-consistently solving for E_F and n_s in the potential well, modeling accuracy is improved compared to the threshold voltage based model even in moderate-accumulation regimes [30]. Besides, the model equations are source–drain symmetric without derivative singularities up to second order, which improves the computational robustness in harmonic balance simulations. Detailed formation explanation of the model can be found in [30].

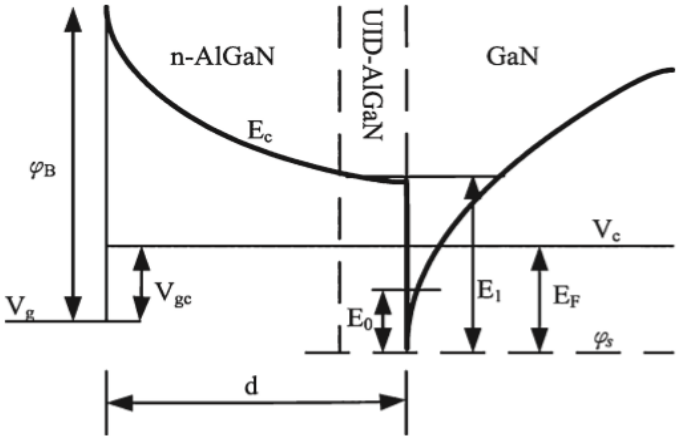

Figure 2.5 Energy band diagram of AlGaN/GaN HEMT for nonzero gate bias [30].

The intrinsic charge and capacitance are derived consistently with the current model. By integrating the sheet charge density model along the channel, the gate charge is obtained. Ward–Dutton charge partition method is used to divide total gate charge into gate-source charge and gate-drain charge [31].

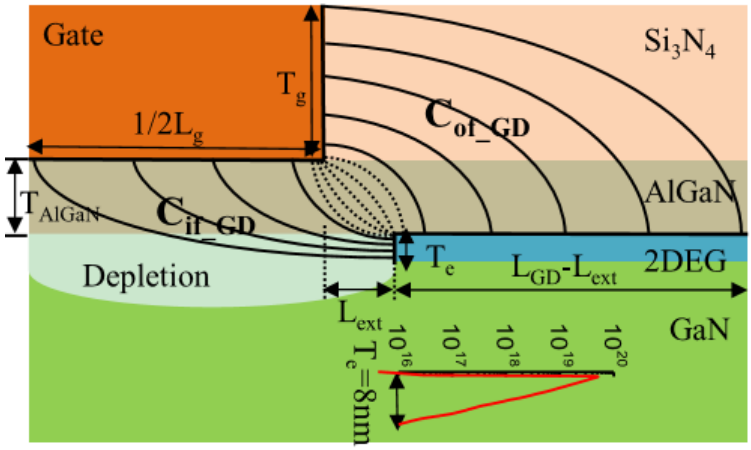

Figure 2.6 Cross-sectional schematic view for the inner and outer fringing capacitances modeling of the drain side [31]

The inner and outer fringing capacitance are modeled as parasitic capacitance using conformal method and verified by using Technology-CAD simulation. Detailed formation explanation and verification of the model can be found in [30].

The surface potential model clearly describes the behavior of the device based on semiconductor physics with only a small amount of physical parameters. The model is scalable with geometry, biasing and temperature. However, the model equations are open-form, which need a number of iterations to solve the equations depending on the solution accuracy. This makes the surface potential model computational intensive and difficult to implement in circuit simulators. Besides, the physics of access regions are not provided in surface potential model, which has a significant impact on the accuracy of the physics-based model.

2.2.2 ASM-HEMT Model

The ASM-HEMT (Advanced SPICE Model for GaN HEMTs) model is also a surface-potential model proposed by S. Khandelwal [32, 33]. This surface potential model is based on the same semiconductor physics (*i.e.*, band diagram, Poisson and Schrodinger's equation) as the Tsinghua-HKUST model. Khandelwal proposed a new algorithm to obtain the open-form Poisson and Schrodinger's equations that can be implemented in SPICE simulator. The model construction workflow for this model is shown in Figure 2.7.

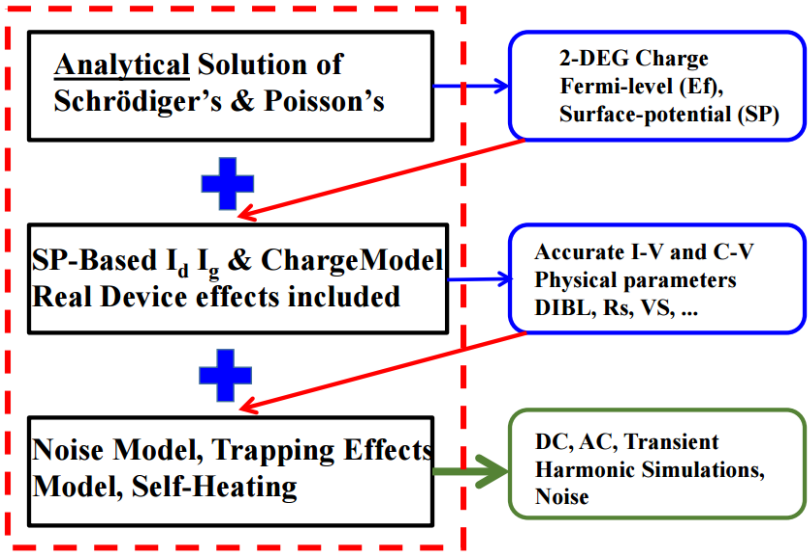

Figure 2.7 Construction workflow for ASM-HEMT model [34]

Apart from current model and charge model, the ASM-HEMT model captures most of the device characteristics required by circuit simulation, such as gate leakage, self-heating, trapping and noise. This model is aimed at achieving industrial model quality and has passed into the Phase-II for

standardization at the Compact Model Coalition. The theory and validation results of the model will not be reproduced here and detailed model explanation and validation can be found in [32, 33, 34].

Although in ASM-HEMT model, a new algorithm is proposed to solve the open-form Poisson and Schrodinger's equations, this model is still computational intensive and not easy to implement in circuit simulators.

2.2.3 NCSU Model

The NCSU model is a drift-diffusion-based compact model proposed by D. Hou and R. Trew at North Carolina State University in 2012 [35] and later extended the charge model for displacement current [36]. The model is developed by separating the conducting channel of the GaN HEMT into a series of zones, based upon physical behavior and the validity of gradual channel approximation (GCA). Drift-diffusion equations are used to model the carrier transport of each zone and all the equations are consistently solved applying the boundary conditions of each zone.

The model operates in two modes, triode and saturation. The zone separation of each mode is shown in Figure 2.8.

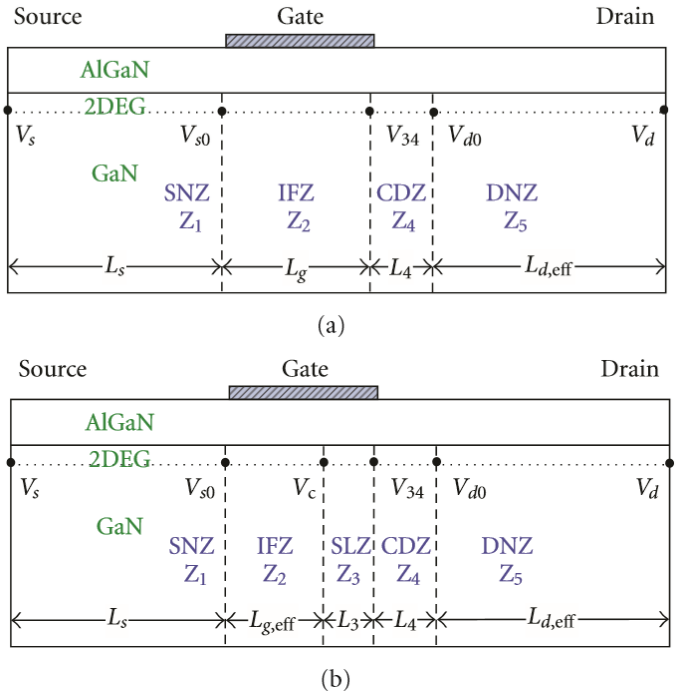

Figure 2.8 Cross-section of NCSU model (a) triode mode with its four physical zones (b) Saturation mode with its five physical zones [35].

Source and drain access region are modeled as SNZ and DNZ (source neutral zone and drain neutral zone) respectively, applying steady-state carrier drifting equations. The gated transistor is modeled as IFZ (intrinsic FET zone). In IFZ, GCA holds, and therefore current expression can be immediately setup. Poisson equation are constructed for describing the current and voltage relationship in charge deficit zone (CDZ) and space-charge-limited Zone (SLZ). Detailed equation formations can be found in [35].

Assuming quasi-static operation, the charge is modeled by integrating the gate controlled charge density along the channel [36]. By solving the derivative of gate-source and gate-drain charge, the displacement current is obtained.

About 20 parameters are required to characterize the model, which compared to empirical models, is a significant reduction. Although the model employs approximations in solving equations and the determining zone boundaries, measurements of single transistor and a Class-AB power amplifier have approved that the NCSU current–voltage model and charge–voltage model are able to accurately model the DC and RF behavior (both small signal and large signal) of a GaN HEMT [35, 36].

This model is not without its limitations. Due to the assumption of GCA, the approximations in solving equations and determining zone boundaries, more error will be introduced in this model when the gate length is further scale down to cater higher frequency applications.

2.3 Limitations and Trade-offs of Compact Models

The empirical models use a large number of fitting parameter to fit the device for various geometry or operating spaces (such as biasing and temperature) to measurement data. The equations are close-form, which are computational efficient and simple to implement in circuit simulators. The parameter extraction for empirical model usually not require any prior process knowledge of the device, which allows it for quick performance evaluation of new device at circuit and system level. However, the limitations of the empirical models are as follows.

First, the empirical model usually has no physical insight into the device. Device and circuit designer use the model as a black box and cannot provide any information for the inside characteristic of the device. It is impossible to improve the circuit performance from a device perspective or provide any feedback for the technology tuning. Without the interaction between device and circuit, the design job often becomes a blind tuning, which could take many iterations to reach the design target.

Second, extraction of large number parameters is time and effort consuming, in which experienced modelers are required. The parameters extracted for one device are not valid for another device. Any process or geometry change made to the device needs re-fitting of the model.

Third, the current, charge and capacitance behaviors are usually modeled separately based on different sets of fitting equations. Therefore, inconsistencies such as violations of charge conservation and incontinuities at fitting boundaries are often unavoidable, which significantly affects the computational robustness in circuit simulation.

Physics based models employ semiconductor physics to model the behavior of the device and can compensate the limitations of empirical models. First, the physics based models generally provide simple and clear explanations to device behaviors from the very basic quantum physics, device physics level such as carrier transport to physical-element-based equivalent circuit level depending on the applications of the model. Physics based models are able to provide designers insights of circuit-level physics, which allows for device-circuit interactive design and optimization for better circuit performance.

Second, the parameters in physics based models often have a clear physical meaning. The modeler could adopt the parameter value from other independent sources. The sharing of parameters between models and modeling groups will greatly reduce the repetitive time and labor cost in model construction. It also provides a way to validate the values of extracted parameter.

Third, the current, charge and capacitance behaviors in physics based models are usually results from the same physics origins, and therefore sophisticated physics based model can guarantee that the behavior of each sub-model is consistent with other sub-models.

The major limitation of physics based model is that the model equations are usually open-form, which need special numerical algorithms to iteratively solve the equations depending on the solution accuracy. These algorithms are usually computational intensive and not easy to implement in circuit simulators. Some approximations can be made in solving the equations to make the solution close-form, but the solution accuracy and consistency will be affected. Besides, physics based model usually required detailed process information of the device, for which most commercial devices are not available.

Chapter 3
Physics Based Virtual Source Compact Model of GaN HEMTs

Since a GaN HEMT is such a complex system, in order to clearly organize and represent the physics concepts behind it, it is necessary to divide the device model into separate modules and model each module by its corresponding physics. This chapter discusses the partition of the model, the physics of each partition and its modeling strategy.

In this chapter, the model partition scheme is proposed based on the physical construction of the device first. After that, the equivalent circuits to model the probing pads and parasitics are discussed. At the end, the theory of Schottky diode model and Virtual Source model for the intrinsic transistor are introduced, which forms the core of the model.

3.1 Model Partition

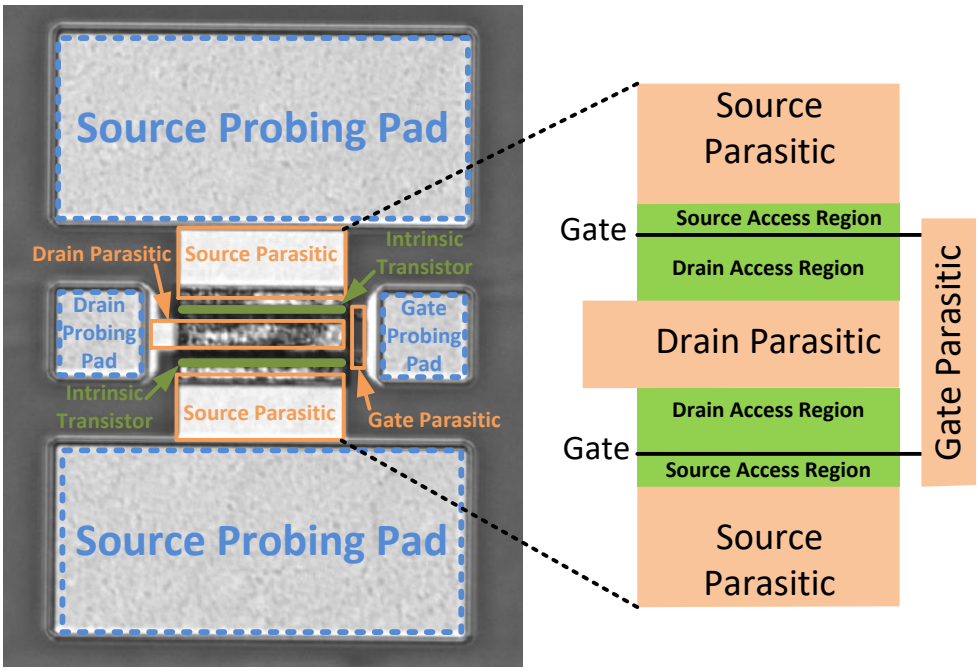

Figure 3.1 Top view of an on-wafer GaN HEMT and corresponding layout partition (left) and zoomed in illustration of intrinsic transistor (right)

A compact device model used in circuit simulator is usually partitioned into sub-models based on the physical construction of the device [22, 27, 42 - 44, 47]. Figure 3.1 shows a microscopic photo of a 2-finger GaN HEMT embedded into a pair of ground-signal-ground (GSG) probing pads for on-wafer

characterization. The gate and drain terminal of the transistor are connected to the signal pads on both sides and the two source terminals are merged into the ground pads.

Based on the physical layout, the typical GaN model can be divided into three layers, as is shown in Figure 3.2 in which the colored regions are corresponding to those regions in Figure 3.1. In this case, the GSG probing pads model serves as the outmost layer. This layer represents the behavior of connection from the probing tips to the boundary of the metal connection of intrinsic transistor. To adapt the proposed model to generalized cases, the outmost layer needs to be adjusted accordingly. For example, in integrated circuit (IC) design, the outmost layer is transmission lines which connect the transistor to the front or back stage while in a discrete power transistor, the outmost layer is the wire bonding pads or the device package. In general, the outmost layer should include the metallization which connects the intrinsic transistor and associated parasitics to the fixture or other part of the circuit.

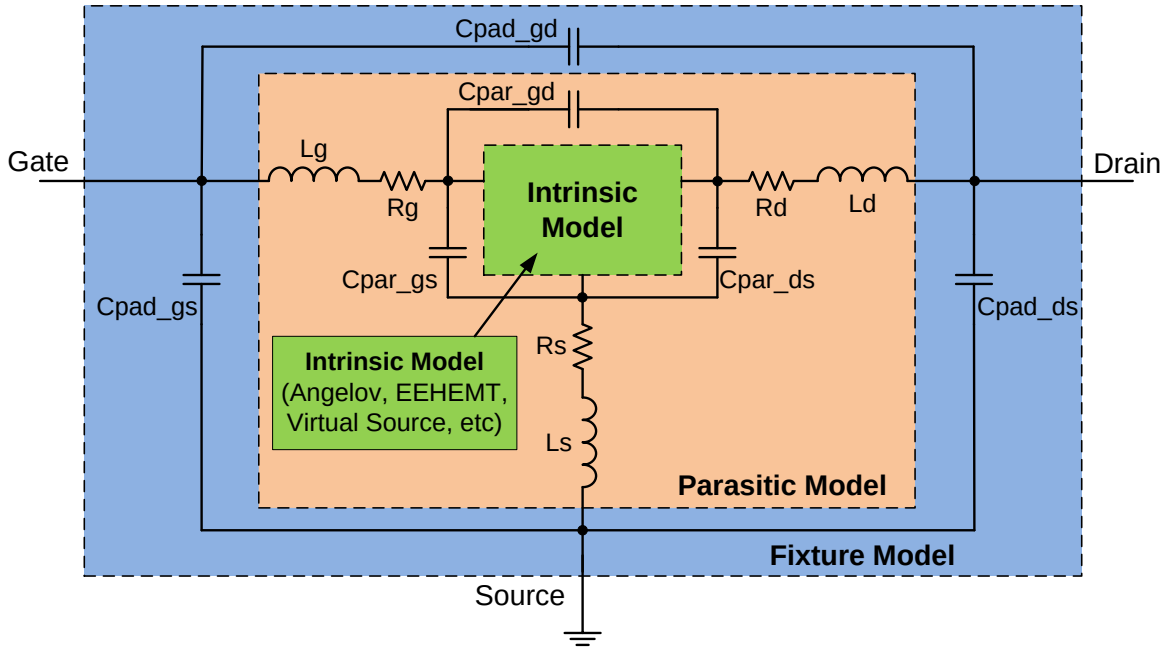

Figure 3.2 Device model partition: GSG pads model, parasitic model and intrinsic model

The middle layer that is enclosed by the GSG pads model is the parasitic EM model. This model describes the non-negligible resistive, capacitive and inductive behavior between the GSG pads and the intrinsic transistor. These resistive and inductive behaviors usually results from the metal extension or vias at the source terminal and the manifold or air-bridge at the gate and drain terminal while the capacitive behavior is due to the spatial coupling between them.

The innermost layer is the core of the transistor – the intrinsic model. The intrinsic model describes the electrical behavior of the active region of the transistor, which includes the nonlinear gate and drain current and terminal charge. Different types of intrinsic models, such as look-up-table (LUT) model, small signal model (SSM) and all the compact models described in Chapter 2 can be substituted into the innermost layer to form a complete model.

The circuit elements in GSG pads model and parasitic model are always passive while the intrinsic model has nonlinear active elements in it. In advanced intrinsic models, thermal effect and trapping effect are also considered for GaN HMETs [37 -40].

The modeling schemes of GSG pads, device parasitics and intrinsic model of gate current and drain current are introduced in the following sections.

3.2 GSG Pad Model

Modeling probing pads is relatively straightforward compared to modeling other parts of the transistor. Although complicated GSG pad model applicable up to 200 GHz is proposed [41], using a simple capacitive network to model pads is still reasonably accurate below tens of gigahertz [42 - 44], because that pads are spatially separated metals without conductive connections between them.

Figure 3.3 shows the microscopic photo of a pair of dummy GSG pads measured for this thesis and its equivalent circuit. The structure is vertically symmetrical, and therefore three capacitors are used in the equivalent circuit to model the pads.

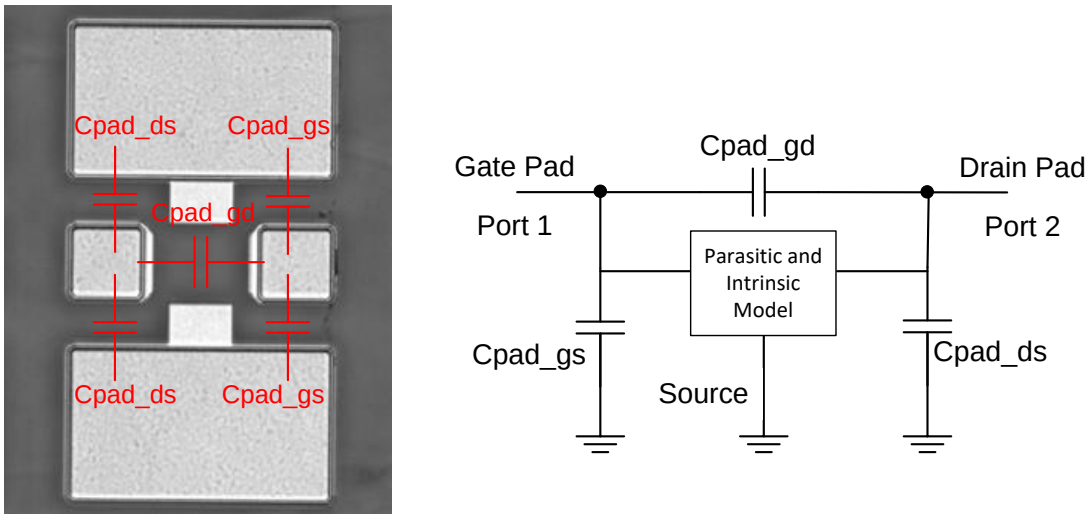

Figure 3.3 Photo of a pair of dummy GSG pads (left) and model equivalent circuit (right)

C_{pad_gs},C_{pad_ds} and C_{pad_gd} represent the capacitance between gate-source, drain-source and gate-drain, respectively. The device is mounted on copper carrier, which serves as circuit ground connected with source pads. The pitch of the GSG pads in our measurement is 150 μm, which is in the same order of the wafer thickness. C_{pad_gs} and C_{pad_ds} not only include the pad spatial capacitance on top of the structure, but also include the capacitance between the pad and the bottom copper carrier. These two partial capacitors can be merged into one capacitor (C_{pad_gs} or C_{pad_ds}) without losing the generality of the model.

3.3 Parasitic and Intrinsic Model

Figure 3.4 shows the cross section structure of the GaN HEMT measured for this thesis work copied from the PDK user manual [45]. The thickness of each layer is not drawn to scale. There are two major structural differences of this device from many conventional GaN HEMTs. First, a "GaN Cap" layer is grown between the AlGaN layer and the gate metallization, in order to reduce gate current [12] and intrinsic strain at the surface for improved device reliability [46]. Second, an ultra-thin AlN spacer (usually several to tens angstroms) is grown between the AlGaN layer and GaN buffer layer to boost the electron mobility by removing alloy scattering [56].

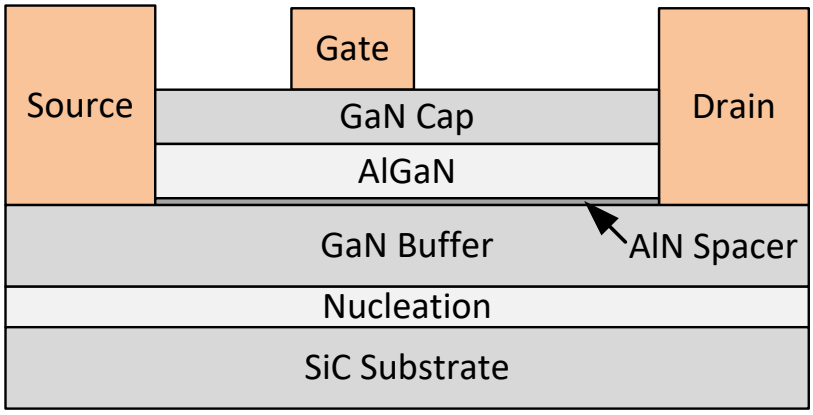

Figure 3.4 Cross section structure of GaN HEMT modeled in this thesis [45]

The gate metal (Ni/Au alloy) forms Schottky contact with the "GaN Cap" layer due to the work function difference, and therefore two Schottky diodes will be used to model the gate-source and gate-drain diode behavior at the gate/GaN Cap interface.

Due to the band gap difference at the AlGaN/GaN interface, a triangular potential well confines the free electrons in GaN buffer and forms the 2-dimentional electron gas (2DEG). The carrier transport

in 2DEG is modeled by three transistors in series, describing the behavior of source access region, gated region and drain access region, respectively.

The AlN spacer forms a potential peak at the interface of AlGaN and GaN buffer where the carriers are tunneled through and the AlGaN and GaN buffer creates a potential barrier, which significantly reduces the gate current at high V_G when the Schottky diodes at the gate/GaN Cap interface is forward biased. In [57], the authors proposed to use a weak reverse diode to model the transport through the AlGaN/AlN/GaN buffer layers. In our work, we choose to use a simple effective series resistor R_{series} instead of a reverse diode to model the tunneling behavior as well as any additional series resistance due to the GaN Cap layer, GaN buffer layer and/or AlGaN layer. This is to simplify the model to avoid potential convergence issues in the parameter extraction flow. As seen in Chapter 4, our gate current model is able to achieve reasonable accuracy.

The equivalent circuit of the parasitic and intrinsic model can be mapped on to the cross section, which is shown in Figure 3.5 below. D_{gs} and D_{gd} are symmetrical, and therefore R_{series} is equally split to two branches (each branch has resistance of $2\times R_{series}$) for clearer equivalent circuit illustration.

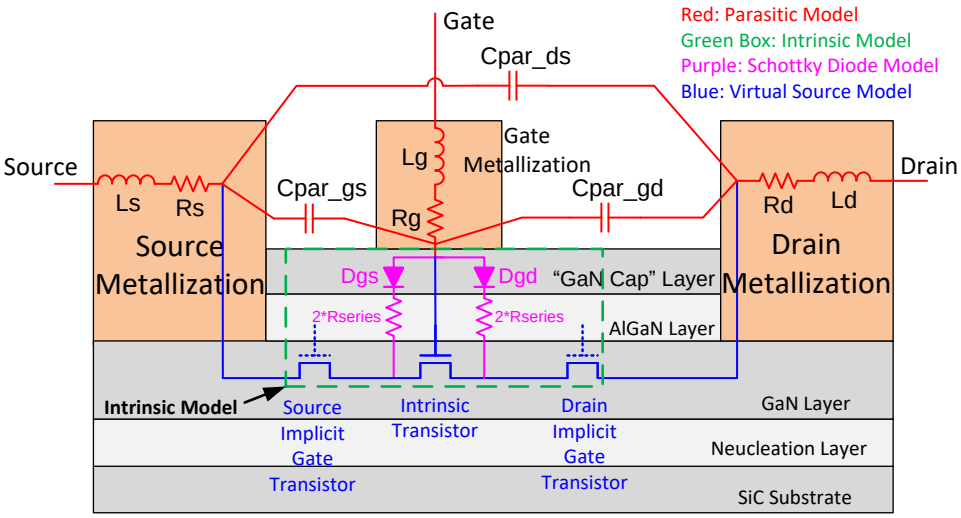

Figure 3.5 Mapping of the parasitic and intrinsic equivalent circuit on the cross section structure

The parasitic model of power transistors is usually demonstrated by proposing a transistor small signal equivalent circuits [42 - 44, 47]. In [42], a 22-element small signal model with parasitic inter-

electrode capacitance is proposed for large size GaN HEMTs. In [47], parasitic network with substrate leakage is introduced for GaN HEMTs on sapphire due to the substrate's non-negligible electrical conductivity. In [43, 44], series resistance and inductance are used for conventional GaN HEMTs on SiC substrate.

Considering the small size transistor (2×50 μm) measured in this work, the interconnect pattern and the substrate material, a pair of resistor and inductor is used for modeling the resistive and inductive behaviour of the metallization for each terminal (L_g, R_g for gate, L_d, R_d for drain, L_s, R_s for source). The spatial coupling is modeled by capacitance between the gate, drain and source as C_{par_gd}, C_{par_gs} and C_{par_ds}.

The intrinsic model can be divided into two part: the gate Schottky diode model and the Virtual Source model. The gate Schottky diode model employs two effective series resistor ($2\times R_{series}$) and two Schottky diodes (D_{gs} and D_{gd}) to model the joint resistive behaviour of the stacked layers from gate/GaN Cap interface down to AlN/GaN interface and the gate leakage from gate to source and gate to drain, respectively. The Virtual Source model theory is used to model both the gated and ungated channel regions, which forms the current path between drain and source current together in series connection.

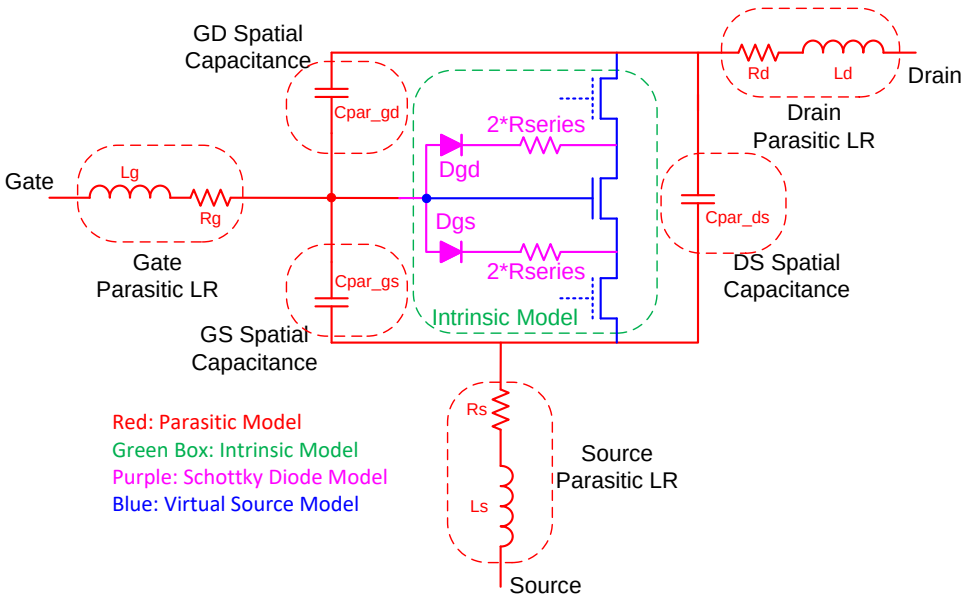

Figure 3.6 Flattened equivalent circuit for the parasitic and intrinsic model

The flattened equivalent circuit for the parasitic and intrinsic model is shown in Figure 3.6. This equivalent circuit can be used as schematic input for circuit simulators. The detailed modeling theory of the Schottky gate diode and the Virtual Source model is described in the following sections.

3.4 Intrinsic Gate Current: Schottky Gate Diode Model

The gate metal (Ni/Au alloy) forms Schottky diode with the "GaN Cap" layer due to the work function difference of the two material, and therefore it is preferable to use the Schottky diode theory to model gate current. The Schottky diode leakage affects the power added efficiency (PAE), especially in power amplifier design because of its significant gate over-drive voltage and non-negligible gate current. In addition, the drain to gate leakage limits the off-state current, which affects the transistor behaviour in switching mode [15]. Therefore, accurate modeling of gate current is required for power GaN HEMTs. The I-V characteristic of a Schottky diode with series resistance is shown in Figure 3.7.

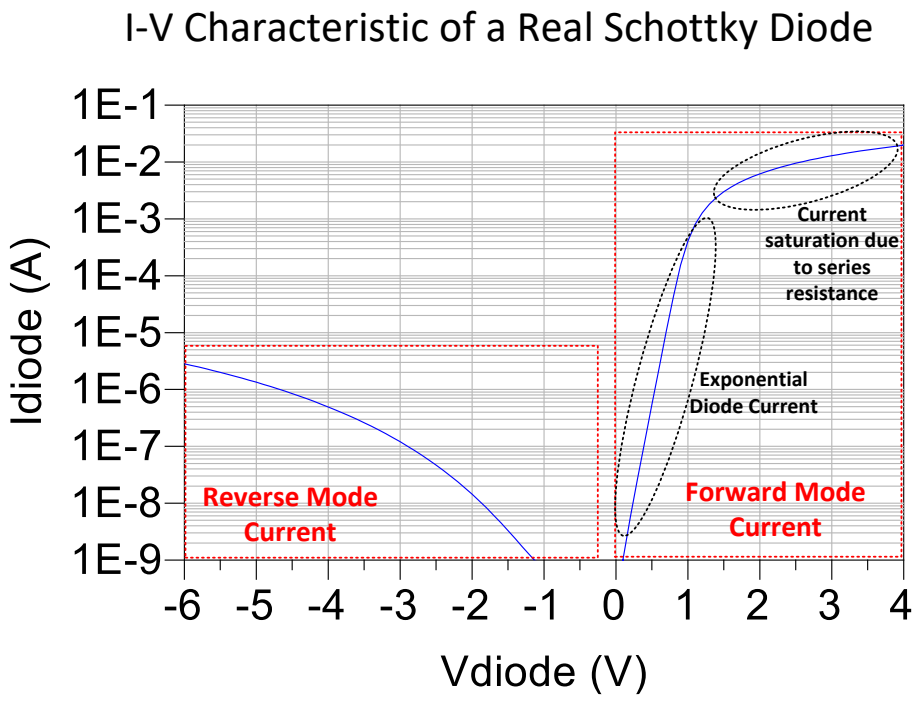

Figure 3.7 I-V characteristic of a Schottky diode with series resistance

The forward mode current is modeled with Schottky diode equations and effective series resistances ($2\times R_{series}$). At low forward voltage ($Vdiode < 1$ V), the forward current is low enough to neglect the voltage drop on the series resistor result from the forward current. At high forward voltage

($Vdiode > 1$ V), the voltage drop on the series resistor saturates the diode current and eventually makes it increase with $Vdiode$ almost linearly. The forward mode current equations are as follows [15]:

$$I_{Dgs,forward} = W \cdot I_j \cdot e^{-\frac{\phi_B}{\eta\phi_T}} \cdot \left(e^{\frac{V_{gsi}}{\eta\phi_T}} - 1\right) \tag{3.1}$$

$$I_{Dgd,forward} = W \cdot I_j \cdot e^{-\frac{\phi_B}{\eta\phi_T}} \cdot \left(e^{\frac{V_{gdi}}{\eta\phi_T}} - 1\right) \tag{3.2}$$

Here V_{gsi} (> 0 V) and V_{gdi} (> 0 V) is the intrinsic voltage applied on the gate-source and gate-drain diode, respectively. W is the total transistor width. I_j is the reverse saturation current density. ϕ_T is the thermal voltage. ϕ_B is the Schottky barrier height, which is typically 1 V for GaN HEMT. η is the ideality factor for the forward diode. The process variation in one device is assumed to be low, and therefore the gate-source diode and gate-drain diode is identically modeled with the same set of model parameters.

Reverse mode current of the Schottky diode is described by using the following empirical equations [15]:

$$I_{Dgs,rec} = -W \cdot I_{rec} \cdot \left(e^{\frac{F_{sat,gsi}}{\eta_{rec}\phi_T}} - 1\right) \tag{3.3}$$

$$I_{Dgd,rec} = -W \cdot I_{rec} \cdot \left(e^{\frac{F_{sat,gdi}}{\eta_{rec}\phi_T}} - 1\right) \tag{3.4}$$

$$F_{sat,gsi} = -\frac{V_{gsi}}{1+|V_{gsi}|/V_{gsats}} \tag{3.5}$$

$$F_{sat,gdi} = -\frac{V_{gdi}}{1+|V_{gdi}|/V_{gsatd}} \tag{3.6}$$

In these equations, I_{rec} is the reverse current density. η_{rec} is the ideality factor for the reverse diode. V_{gsats} and V_{gsatd} are empirical reverse saturation voltage for gate-source and gate-drain diode, respectively. $F_{sat,gsi}$ and $F_{sat,gdi}$ are empirical equations modeling the saturation of reverse current with gate voltage. The total gate current between gate-source (I_{Dgs}) and gate-drain (I_{Dgd}) is the sum

of the forward mode current ($I_{Dgs,forward}$ and $I_{Dgd,forward}$) and reverse mode current ($I_{Dgs,rec}$ and $I_{Dgd,rec}$).

Here only the modeling theory is introduced. The parameter extraction procedure will be demonstrated and the gate current modeling will be validated in Chapter 4.

3.5 Intrinsic Drain Current: Virtual Source Model

The Virtual Source model is first proposed at MIT for highly scaled silicon based FETs with quasi-ballistic mode of transport [48] and later extended to drift-diffusive transport for GaN HEMTs [15，49]. The Virtual Source model calculates the density of carriers, which flow in the channel to form the transistor current model, and integrates the carrier distribution along the channel to form the transistor charge model. The model is physical based on the drift-diffusive transport theory, and employs only a small number of fitting parameters to form the model. A brief description of the Virtual Source modeling theory is given below to introduce the basic idea.

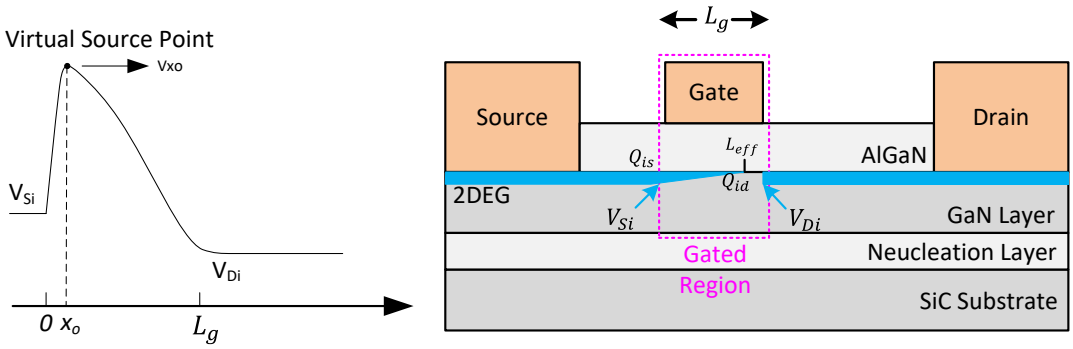

Figure 3.8 Band diagram under the gate (left) and charge density (right)

Virtual Source Model: Current Formation

The gated region in conventional GaN HEMTs has gate length ranging from tens of nanometers to a few hundred of nanometers, and therefore the mean-free-path of a few angstroms [15] for electrons in the 2DEG in GaN HEMTs results in scattering-dominated drift-diffusive transport. Assuming gradual channel approximation (GCA), the drain current is the product of the charge and carrier velocity at the same location and is related to the potential along the channel as follows [15]:

$$I_{DS} = W \cdot Q_i(x) \cdot v(x) = W \cdot Q_i(x) \cdot \mu \frac{d\varphi(x)}{dx} \tag{3.7}$$

Here $Q_i(x)$ is the charge density and $\varphi(x)$ is the channel potential at location x. μ is the carrier mobility.

To account for carrier velocity-saturation effect, Equation 3.7 is written in the following form [15]:

$$I_{DS} = W \cdot Q_i(x) \cdot \mu \cdot \frac{\frac{d\varphi(x)}{dx}}{\left(1+\left(\frac{\frac{d\varphi(x)}{dx}}{\frac{v_{sat}}{\mu}}\right)^{\beta}\right)^{\frac{1}{\beta}}} \tag{3.8}$$

In Equation 3.8, v_{sat} is carrier saturation velocity and β is the transition coefficient that controls the transition sharpness at saturation voltage. Equation 3.8 is valid at all x provided GCA holds, which is reasonable for a major portion of the channel except in the pinch-off or velocity-saturated region at the drain-end of the gate.

Charge density $Q_i(x)$ is related to channel potential $\varphi(x)$ by the gate capacitance in strong inversion (C_{inv}). Substituting $dQ_i(x) = C_{inv} \cdot d\varphi(x)$ into Equation 3.8 and integrating from $x = 0$ to the effective gate length $x = L_{eff}$, which equals to L_g in triode region and smaller than L_g in saturation region (up to the position of pinch-off point), I_{DS} is obtained as follows after the simplification.

$$I_{DS} = W \cdot \frac{\mu}{2C_{inv}L_g} \cdot \frac{\left(Q_{is}^2 - Q_{id}^2\right)^2}{\left(1+\left(\frac{Q_{is}-Q_{id}}{\frac{C_{inv}\cdot v \cdot L_{eff}}{\mu}}\right)^{\beta}\right)^{\frac{1}{\beta}}} \tag{3.9}$$

In Equation 3.9, $Q_{is} = Q_i(0)$ is the charge density at intrinsic source (V_{Si}) and $Q_{id} = Q_i(L_{eff})$ is the charge density at intrinsic drain (V_{Di}). L_{eff} is not necessarily equal to the physical-gate-length (L_g), since it has to be corrected for short-channel-effects described in [15]. v is the carrier velocity combing strong and weak accumulation regimes by the Fermi function (F_f) as below.

$$v = v_{sat}\left(1 - F_f\right) + 2\phi_T \frac{\mu}{L_g} F_f \tag{3.10}$$

$$F_f = \frac{1}{1+\exp\left(\frac{\max(V_{GSi}, V_{GDi}) - (V_T - \alpha\phi_T/2)}{\alpha\phi_T}\right)} \tag{3.11}$$

$$V_T = V_{T0} - \delta V_{DSi} \tag{3.12}$$

In Equation 3.10, v_{sat} is the carrier saturation velocity and ϕ_T is the thermal voltage. For the fermi function (F_f), α is the fitting parameter for the transition at threshold voltage and V_T is the threshold

voltage, which is defined by Equation 3.12. V_{T0} is the threshold voltage at $V_{DS} = 0$. δ is the drain induced barrier lowering (DIBL) coefficient.

When the source is grounded and drain is ramped to positive voltage, the charge density at intrinsic source (Q_{is}) and drain (Q_{id}) are obtained as [15]:

$$Q_{is} = C_{inv} 2n\phi_T \ln\left(1 + \exp\left(\frac{V_{GSi} - (V_T - \alpha\phi_T F_{fs})}{2n\phi_T}\right)\right) \tag{3.13}$$

$$Q_{id} = \begin{cases} C_{inv} 2n\phi_T \ln\left(1 + \exp\left(\frac{V_{GDi} - (V_T - \alpha\phi_T F_{fd})}{2n\phi_T}\right)\right) \\ C_{inv} 2n\phi_T \ln\left(1 + \exp\left(\frac{V_{GSi} - V_{DSAT1} - (V_T - \alpha\phi_T F_{fd})}{2n\phi_T}\right)\right) \end{cases} \tag{3.14}$$

In Equation 3.13 and Equation 3.14, F_{fs} and F_{fd} are the fermi function for source and drain, respectively. V_{DSAT1} is the refined saturation voltage for compensating the smaller L_{eff} when the transistor is in saturation region. n is the subthreshold factor which combines the subthreshold slope (SS) and punch through factor as follows (n_d):

$$n = \frac{SS}{\phi_T \ln(10)} + n_d V_{DSi} \tag{3.15}$$

Complete explanation and derivation for the Virtual Source current model can be found in [15, 44].

Virtual Source Model: Charge Formation

The channel charge in GaN HEMTs exhibits nonlinearity which significantly affects the large signal RF behaviour of the device. In order to enable a charge based rather than capacitor based model, the non-uniform channel charge should be partitioned to generate gate-source and gate-drain charges at source and drain terminals. The Virtual Source model accomplishes this in a self-consistent manner by using the current-continuity and linear Ward-Dutton charge partition scheme [15, 50]. The expressions for charge partitioning along with the total gate charge are given below:

$$Q_S = WL \int_{x=0}^{x=L} \left(1 - \frac{x}{L}\right) Q_i(x) dx \tag{3.16}$$

$$Q_D = WL \int_{x=0}^{x=L} \left(\frac{x}{L}\right) Q_i(x) dx \tag{3.17}$$

$$Q_G = WL \int_{x=0}^{x=L} Q_i(x) dx \tag{3.18}$$

Plugging in the drain current expression (Equation 3.8 and 3.9) and integrating along the channel, the close-form charge expressions are as follows [15]:

$$Q_S = \frac{2WL}{\left(Q_{is}^2 - Q_{id}^2\right)^2}\left[\frac{Q_{is}^5 - Q_{id}^5}{5} - Q_{id}^2\frac{Q_{is}^3 - Q_{id}^3}{3}\right] \tag{3.19}$$

$$Q_D = \frac{2WL}{\left(Q_{is}^2 - Q_{id}^2\right)^2}\left[Q_{is}^2\frac{Q_{is}^3 - Q_{id}^3}{3} - \frac{Q_{is}^5 - Q_{id}^5}{5}\right] \tag{3.20}$$

$$Q_G = \frac{2WL}{Q_{is}^2 - Q_{id}^2}\left[\frac{Q_{is}^3 - Q_{id}^3}{3}\right] \tag{3.21}$$

Complete explanation and derivation for the Virtual Source charge model can be found in [15, 49].

Access Regions: Implicit Gate Transistor Model

The access regions in GaN HEMTs are ungated two-terminal structures that exhibits nonlinear resistive behaviour same as transmission line method (TLM) structures. When low voltage ($< 1V$) is applied across a TLM structure, the TLM structure behaves as a linear resistor, whose resistance is determined by the active region sheet resistance and its geometry. When high voltage is applied, the resistance is increased with the applied voltage, due to the carrier velocity saturation in the active region. This nonlinear resistive behaviour is well captured by using a transistor model which is biased with a constant gate to source voltage [15]. This constant V_{GS} is determined by making the on-resistance (resistance at a certain V_{GS} and $V_{DS} = 0$) of the model equal to the resistance of TLM at low voltage, which is :

$$I_{access} = \frac{V_{access}}{R_{sh}\times\frac{L}{W}} = \frac{W}{L}\mu C_{inv}(V_{GS} - V_T)V_{access} \tag{3.22}$$

Solving Equation 3.22, the gate over drive voltage ($V_{GS} - V_T$) can be calculated from carrier mobility μ, sheet resistance R_{sh} and implicit gate capacitance C_{Ig} as [15]:

$$V_{GS} - V_T = \frac{1}{R_{sh}\mu C_{Ig}} \tag{3.23}$$

Since it is difficult to determine a location for the implicit gate, the implicit gate capacitance is treated as a fitting parameter. The implicit gate capacitance C_{Ig} is the only additional fitting parameter needed for the access regions in the Virtual Source model.

3.6 Model Parameters Summary

The proposed physics based compact model has the simplicity of using small numbers of parameters to model the device. The key parameters needed for the complete model are listed in Table 3.1.

Table 3.1 Model parameter summary

Model Partition		Parameters	No. of Parameters
Fixture Model		$C_{pad\_gs}, C_{pad\_ds}, C_{pad\_gd}$	3
Parasitic Model		$L_g,\ L_d, L_s, R_g, R_d, R_s, C_{par\_gs}, C_{par\_gd}, C_{par\_ds}$	9
Intrinsic Model	Diode Model	$R_{series},\ I_j,\ \eta, I_{rec},\ \eta_{rec}, V_{gsats}, V_{gsatd}$	7
	Gated Transistor	$v_{xo}, \mu_0, \beta, V_{t0}, DIBL_1, DIBL_2, SS, nd, DIBL_{sat}$ R_{th}, C_{th}	11
	Source Access Region Model	$C_g^{SAR}, v_{xo}^{SAR}, \mu_0^{SAR}, \beta^{SAR}$	4
	Drain Access Region Model	$C_g^{DAR}, v_{xo}^{DAR}, \mu_0^{DAR}, \beta^{DAR}$	4

Chapter 4
Model Parameter Extraction and Validation

Model parameter extraction and validation are among the most important procedures in device modeling procedure. In this chapter, the complete model parameter extraction flow is demonstrated with the measurement data of two GaN HEMTs first. Since the key contribution of this thesis is the physics based Virtual Source compact model that is suitable for RF circuit simulation, the complete model formation and parameter extraction described in this chapter form the heart of the thesis. After all the parameters have been extracted, the GaN HEMT model constructed is validated against independent device measurement in terms of drain current, gate current and the S-parameter with respect to its associated sweeps (biasing and/or frequency). With the proposed extraction flow, the model is able to achieve reasonable accuracy for both DC and RF characteristics with a single set of parameter values.

4.1 Physics Based Virtual Source Compact Model Extraction

Based on the model partition proposed above, the complete model extraction flow is introduced in this section. Starting form device measurement results, the algorithm and technique of extracting each parameter are demonstrated step by step until the complete model is established for model validation.

4.1.1 Overview of Model Extraction Procedure

Since the wide adoption of GaAs HEMTs more than 20 years ago, the pinch-off cold-FET technique was appeared most frequently in literature for HEMT parasitic extraction [42, 47, 52- 54]. However, as pointed out by A. Landa in [55], the classical cold-FET method cannot be used in the parasitic extraction of GaN HEMTs, due to the reason that in GaN HEMTs the capacitive behavior of the Schottky diode, which affects the determination of parasitic resistance and inductance in classical cold-FET method, cannot be suppressed even by using large forward gate-source current.

In order to overcome the inaccuracy due to the interference of parasitic resistances, capacitances and inductances during the extraction flow, a new gate current based resistive parameter extraction method is proposed for extracting the parasitic resistance and sheet resistance of the device. This method determines the resistive elements by using DC gate current first, which eliminates the affection of the gate capacitance in S-parameters. After the DC current of the transistor has been

correctly modeled, the parasitic inductance and capacitance are determined by fitting the S-parameter characteristics of the complete model to measurement data.

The flowchart of the complete parameter extraction is shown in Figure 4.1. First, the dummy GSG pads structure is measured (step 1) to extract the pad capacitance (step 2). After that the DC-IV and DC S-parameter of the transistor are measured to extract the parasitic and intrinsic model parameters (step 3).

During the parasitic and intrinsic model parameter extraction, the parameters for forward diode are extracted from gate current (step 4). After that the source and drain contact resistance, active region sheet resistance and the parameters for forward diode are extracted from the gate current measurement (step 5). Then a few Virtual Source model parameters, such as the subthreshold slope and punch through factor, are directly extracted from measurement as initial values for VSM optimization (step 6). After that the VSM parameters are optimized to fit the drain current of both above-threshold region and subthreshold region (step 7). The parameters for reverse gate-drain diode current are optimized to fit the gate to drain leakage floor and the overall gate current (step 8). At the end, the parasitic inductance and capacitance are optimized to fit the modelled S-parameter to measurement data (step 9).

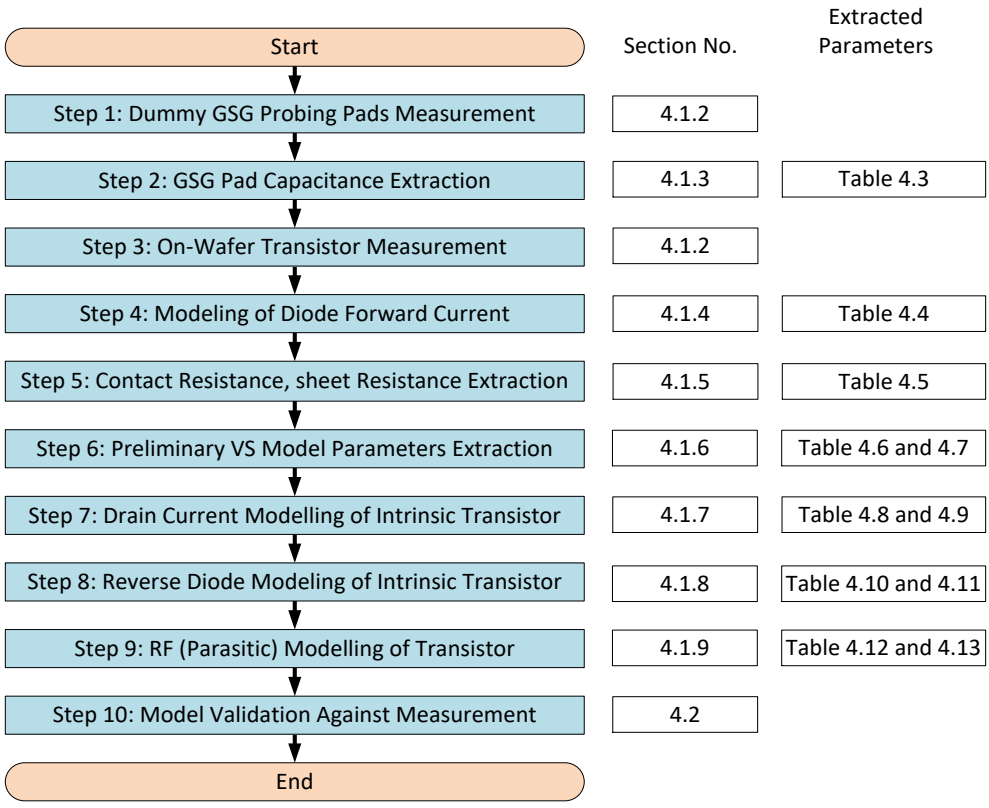

Figure 4.1 Flowchart of the complete parameter extraction procedure

After all the model parameters have been extracted, the complete model is validated against measurement data, which will be demonstrated in next section (step 10).

4.1.2 On-Wafer Device Characterization Setup

Device characterization is the initial and one of the most important steps in device modeling procedure. The model developed in this thesis is fitted to measurement data, and therefore the reliability and accuracy of the device model depend largely on the choice of measurement method and the measurement accuracy. Considering the relatively lower measurement accuracy of pulsed measurement and the capability of thermal modeling in the intrinsic Virtual Source model as well as the relatively good thermal conductivity of the GaN samples on SiC substrate, DC-IV and DC S-parameter measurement are performed. The on-wafer device characterization setup is shown in Figure 4.2.

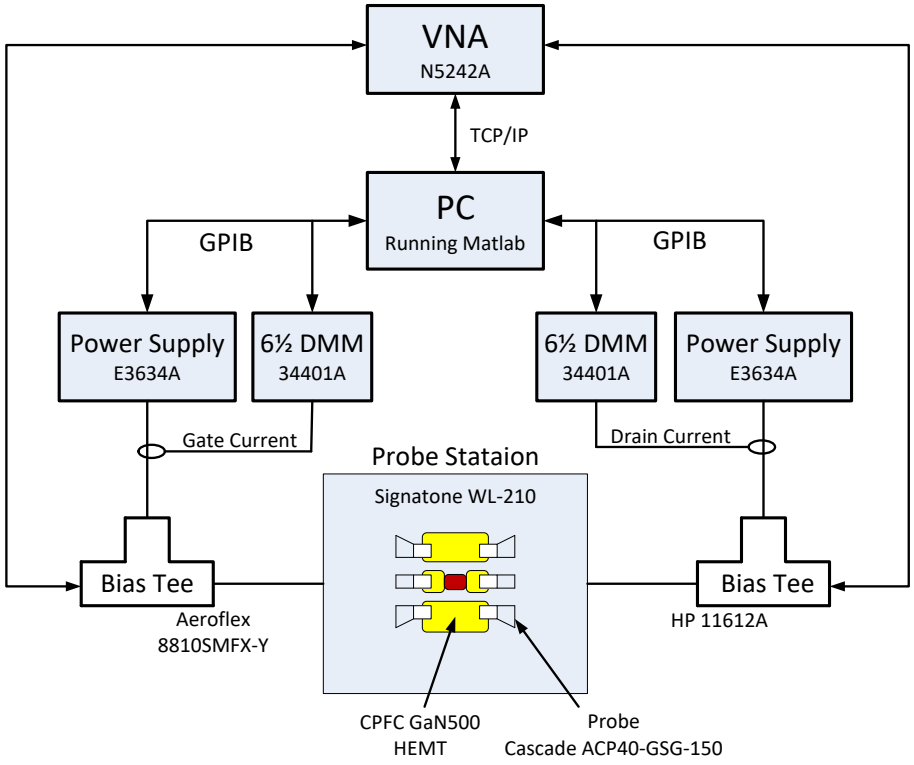

Figure 4.2 On-wafer device characterization setup

The DC-IV and DC S-parameter of device under test (DUT) are measured on the probe station with gate and drain connected to bias tees for DC biasing. The gate and drain voltage is supplied and measured by two power supplies while the gate and drain current are measured by a 6½ digital

multimeter (DMM) instead of directly read from power supply for improved accuracy. The S-parameter is measured using a vector network analyzer (VNA) from 45 MHz to 18 GHz. All the equipment are controlled by customized Matlab program running on a personal computer. The full measurement is conducted automatically using Matlab programs without the experimenter's intervene.

The on-wafer GaN device characterized in this study are fabricated by Canadian Photonics Fabrication Center (CPFC) using its GaN500 process. Figure 4.3 shows a microscopic photo of a die measured in this study. Each device on the die includes the GSG pads for probing and the embedded transistor. Three different gate widths of transistor are fabricated on the die with its width of 50 µm, 100 µm and 200 µm. All the transistors have a gate length of 500 nm and 2 fingers.

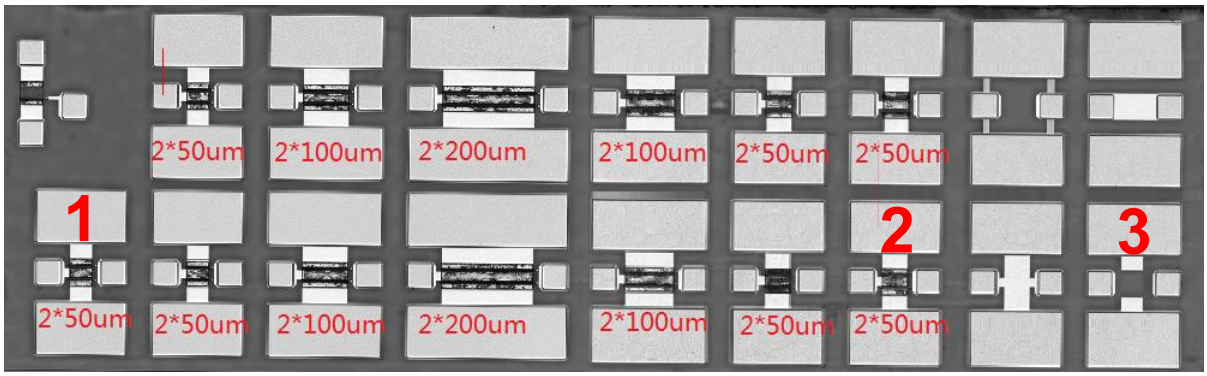

Figure 4.3 Microscopic photo of a die with different sized transistors

In order to achieve higher breakdown voltage, drain access region length is designed two times larger than the source access region length, which gives the transistor a breakdown voltage of more than 100 V [45]. Limited by the bias-tee operating voltage limitation, the transistors are only measured up to drain voltage of 45V. The devices are fabricated on SiC substrate, which allows for good thermal dissipation, therefor during measurement, the DC power of the transistor is limited to 10 W/mm.

The devices measured in our study are device No. 1 and 2, both of which have a gate width of 50 µm. Geometrical parameters of the 2×50 µm transistor are listed in Table 4.1 below.

Table 4.1 Geometrical parameters of the 2*50um transistors

Parameters	Value	Unit
Gate Length	500	nm
Gate Width per Finger	50	µm

Number of Fingers	2	
Source Access Region Length	1.1	μm
Drain Access Region Length	2.4	μm

In addition to the transistors, a short, open, line and Thru (SOLT) structure is fabricated on the die as well for probing calibration. The open structure is dummy GSG pad structure (device No. 3 in Figure 4.3), whose S-parameter is measured for pad capacitance extraction in step 1 in our study.

The parameter extraction for drain current model and gate current model requires different ranges of biasing sweeping. For drain current model parameter extraction, positive V_{GS} is not required due to the negative threshold voltage, but V_{DS} should be swept to tens of volts in order to accurately characterize the current saturation and thermal effect. Biasing sweep for gate current model parameter extraction is just the opposite. Positive V_{GS} is applied to generate large enough gate current for forward diode model extraction while V_{DS} is swept only up to several volts, which is sufficient enough to supress the gate current. Furthermore, sweeping step for measuring gate current is much finer than that for measuring drain current, due to the higher biasing sensitivity for gate current.

The biasing sweeps for model parameter extraction and validation is listed in Table 4.2.

Table 4.2 Biasing sweeping for model parameter extraction and validation

Measurement	**Parameter Sweep**	**Dataset for Fitting**			**Dataset for validation**		
		Start	Stop	Step	Start	Stop	Step
Drain Current and S-parameter	V_{DS}(V)	0	45	1	0.5	44.5	1
	V_{GS}(V)	-6	0	0.2	-5.9	0.1	0.2
	Frequency (Hz)	45M	18G	25.9M	45M	18G	25.9M
Gate Current	V_{DS}(V)	0	1.8	0.2	0.1	1.7	0.2
	V_{GS}(V)	-6	1.6	0.2	-5.9	1.5	0.2

During all the measurements, the DC power is limited to 10 W/mm, in order to avoid the burndown of the device.

4.1.3 GSG Pad Capacitances Extraction

The GSG pad modeling theory is already introduced in Section 3.2. The two-port S-parameter of GSG pads is measured for pad capacitance extraction. GSG pad model is a pure capacitive network

(shown in Figure 3.3), and therefore the measured S-parameter is converted to Y-parameter for a direct capacitance representation as follows.

$$C_{pad\_gd} = -\frac{imag(Y_{12})}{2\pi \cdot Freq} \tag{4.1}$$

$$C_{pad\_gs} = \frac{imag(Y_{11})}{2\pi \cdot Freq} + \frac{imag(Y_{12})}{2\pi \cdot Freq} \tag{4.2}$$

$$C_{pad\_ds} = \frac{imag(Y_{22})}{2\pi \cdot Freq} + \frac{imag(Y_{12})}{2\pi \cdot Freq} \tag{4.3}$$

The extracted pad capacitance vs. frequency is shown in Figure 4.4. The pads exhibit behaviour as constant capacitors for a wide range of frequency (except low frequency reaching the VNA's measurement limitation) due to the reason that there is no physical conductive connection between each pad.

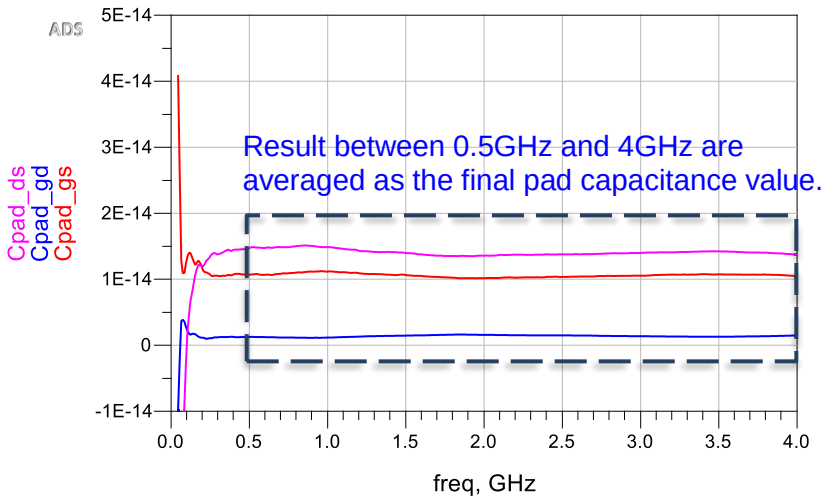

Figure 4.4 Extracted pad capacitance vs. frequency

The extracted results of C_{pad_gs}, C_{pad_ds} and C_{pad_ds} between 500 MHz and 4 GHz are averaged as the final pad capacitance, which is listed in Table 4.3.

Table 4.3 Final pad capacitance results

Parameter	Value	Unit
C_{pad_gs}	1.06×10^{-2}	pF
C_{pad_ds}	1.41×10^{-2}	pF
C_{pad_gd}	1.39×10^{-3}	pF

As is shown in Figure 3.3, the GSG pads are symmetrical, and therefore the gate pad capacitance (C_{pad_gs}) and drain pad capacitance (C_{pad_ds}) should have the same value. However, C_{pad_gs} and C_{pad_ds} extracted in our study are not exactly the same. Possible reasons could be the position of gate probe and drain probe placement from the center are not ideally the same, which introduce unsymmetrical spatial capacitance to C_{pad_gs} and C_{pad_ds}.

4.1.4 Forward Diode Parameters Extraction

The forward diode parameters are extracted from the forward gate current under the biasing condition of $V_{DS} = 0$ and $V_{GS} \geq 0$ assuming gate-source diode (D_{gs}) and gate-drain diode (D_{gd}) are symmetrical. When the drain and source are both tied to ground, the DC equivalent circuit of the Schottky diode, the channel and the access regions are shown in Figure 4.5. The channel and the access regions are linear resistors, whose resistance is proportional to its horizontal length. The access region resistance ($R_{s\_access}, R_{d\_access}$) is represented in terms of channel resistance (R_{ch}), which is labeled in Figure 4.5.

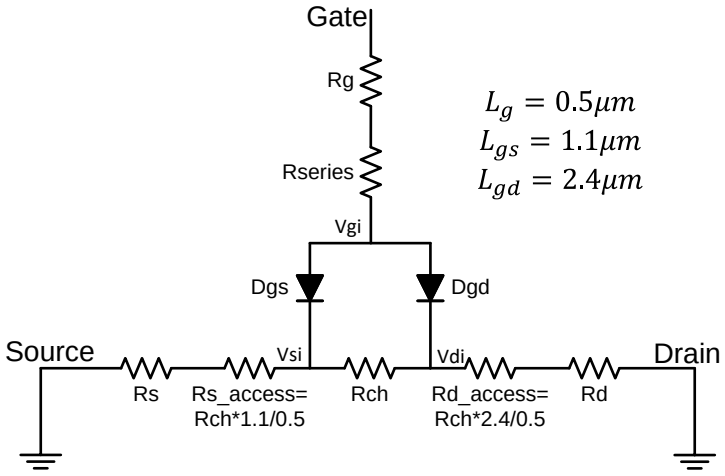

Figure 4.5 DC equivalent circuit of the transistor under biasing condition of $V_{DS} = 0$ and $V_{GS} \geq 0$

The forward Schottky diode parameters ($R_g + R_{series}$, I_j, η as introduced in Section 3.4) are extracted by fitting the linear forward gate current to the measured I_g of $V_{DS} = 0$ V and $V_{GS} > 0$ V. R_s, $R_d, R_{ch}, R_{s\_access}$ and R_{d_access} are ohms level while the gate leakage is small (< 4 mA). Therefore, the voltage drop on R_s, $R_d, R_{ch}, R_{s\_access}, R_{d\_access}$ due to gate leakage can be neglected,

and the two gate diode resistors ($2\times R_{series}$) in parallel can be converted to one series resistor (R_{series}). In this circuit simulation and parameter optimization, R_s, R_d, R_{ch}, R_{s_access}, R_{d_access} are all set to 0 and $R_g + R_{series}$, I_j, η are optimized to fit the linear I_G($V_{ds} = 0$ V, $V_{gs} > 0$ V) curve from measurement. The fitting result of linear scale and log scale gate current is shown in Figure 4.6 and Figure 4.7, respectively.

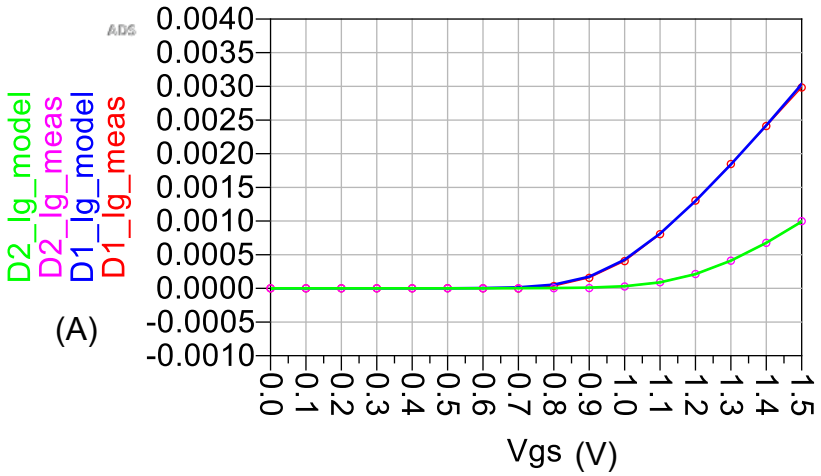

Figure 4.6 Fitting result of linear scale forward gate current of device 1 and 2

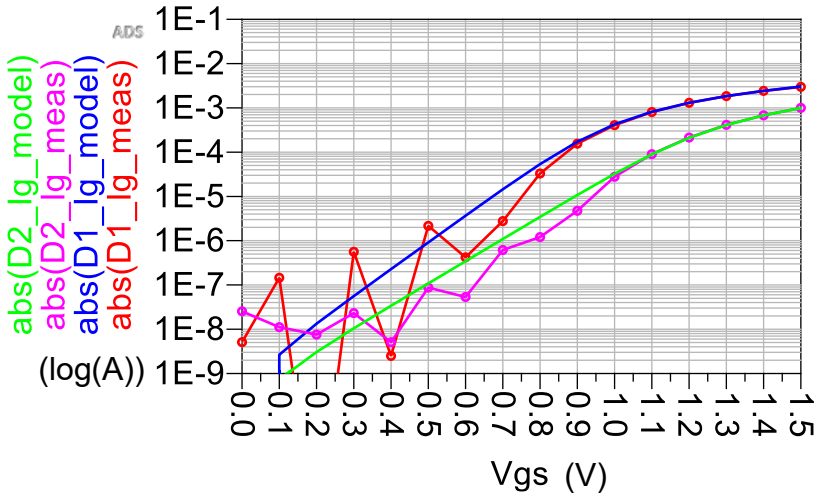

Figure 4.7 Fitting result of log scale forward gate current of device 1 and 2

The extracted forward diode parameters for device 1 and 2 are listed in Table 4.4.

Table 4.4 Extracted forward diode parameters for device 1 and 2

Parameter	Device 1	Device 2
$R_g + R_{series}$ (Ω)	131	205
I_j (mA/mm)	4.80	1.75
η	2.80	3.37

The parasitic gate resistance (R_g) and effective series resistance (R_{series}) are in series, which cannot be distinguished in this section, and therefore the sum of the two resistance is extracted here. R_{series} constitutes most part of $R_g + R_{series}$ because R_{series} models not only the series layer resistance but also the equivalent resistance due to the tunneling through the AlGaN/AlN/GaN structure. The value of R_g and R_{series} will be determined by S-parameter fitting in the section of 4.1.9.

As is demonstrated in Figure 4.6 and Figure 4.7, the Schottky forward diode model accurately describes the gate current vs. gate voltage. The process variation causes the large difference in gate current difference in device 1 and 2. This difference is accurately reflected in terms of the parameter difference shown in Table 4.4.

4.1.5 Gate Current Based Resistive Parameters Extraction

After the forward diode model has been established, the method of how to determine the source and drain contact resistance, active region sheet resistance is demonstrated in this section.

Before extracting the contact resistance and sheet resistance based on the gate current, the on-resistance of the transistor is extracted first. The on-resistance (R_{on}) is defined as the total series resistance between the drain and source terminal when the channel is turned on at $V_{DS} = 0$, which is equal to $R_s + R_{s\_access} + R_{ch} + R_{d\_access} + R_d$ in Figure 4.5. The on-resistance serves as constrain of the total series resistance in the optimization to be discussed later in this section and the value of each resistive part is determined based on the V_{DS} dependence of the gate current.

The on-resistance is extracted from the S-parameter measurement at $V_{GS} = 0$ and $V_{DS} = 0$. If the gate terminal is defined as port 1 and drain terminal is determined as port 2 in Figure 4.5, R_{on} can be easily represented from the Z-parameter converted from S-parameter as follows.

$$R_{on} = re(Z_{22}) = R_d + R_s + R_{s\_access} + R_{d\_access} + R_{ch} \tag{4.4}$$

The Z-parameter used here is not converted from the raw S-parameter of the measurement but the S-parameter in which the pad capacitance has already been de-embedded. The pad capacitance usually includes errors, and therefore incomplete or over de-embedding of the pad capacitance introduce nonlinear frequency dependence in the real part of de-embedded Z-parameters [42]. To reduce the errors, the de-embedded Z-parameter is first multiplied by ω^2, which is:

$$\omega^2 \cdot R_{on} = \omega^2 \cdot re(Z_{22}) = \omega^2 \cdot (R_d + R_s + R_{s\_access} + R_{d\_access} + R_{ch}) \tag{4.5}$$

By linear regression of $\omega^2 \cdot re(Z_{22})$ vs. ω^2, R_{on} is extracted from the slope. The linear regression of device 1 and 2 with frequency range from 45 MHz to 18 GHz and the corresponding R_{on} is shown in Figure 4.8.

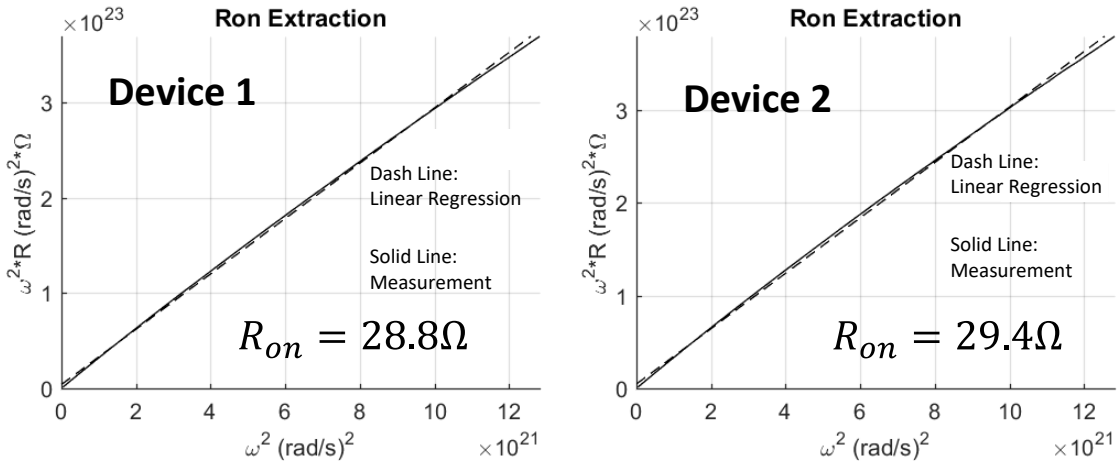

Figure 4.8 R_{on} extraction of device 1 and 2

After R_{on} is extracted, the total series resistance constrain is established. Considering the proportional property of access regions and channel resistance in Figure 4.5, the resistance constrain is written as follows:

$$R_{on} = R_s + R_d + 8 \times R_{ch} \tag{4.6}$$

The free variables in Equation 4.6 are R_s, R_d and R_{ch}. Any two of these three free variables can be selected as independent variables while the other one as dependent variable for optimization to fit the model I_G to the linear I_G curves measured vs. positive V_{GS} and V_{DS} sweeps.

The fitting result of linear scale and log scale gate current vs. positive V_{GS} and V_{DS} sweeps is shown in Figure 4.9 and Figure 4.10, respectively.

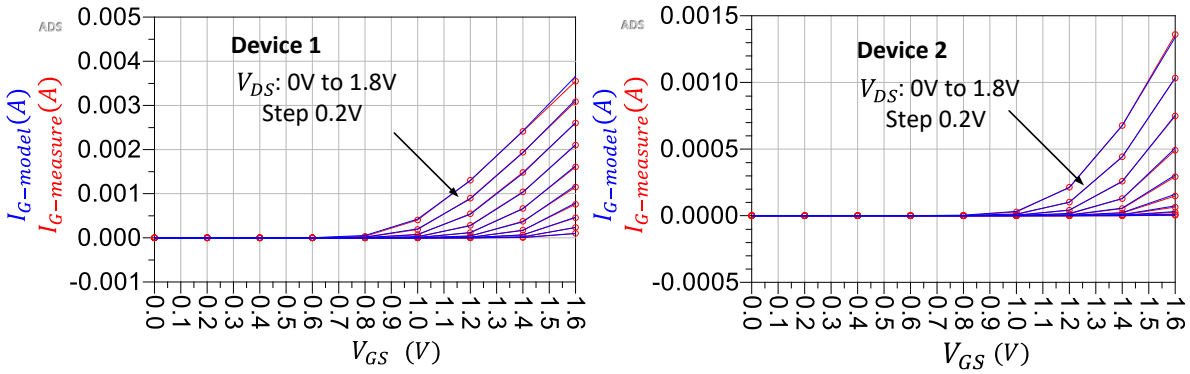

Figure 4.9 Fitting result of linear scale forward gate current vs. V_{GS} and V_{DS} sweeps of device 1 (left) and 2 (right)

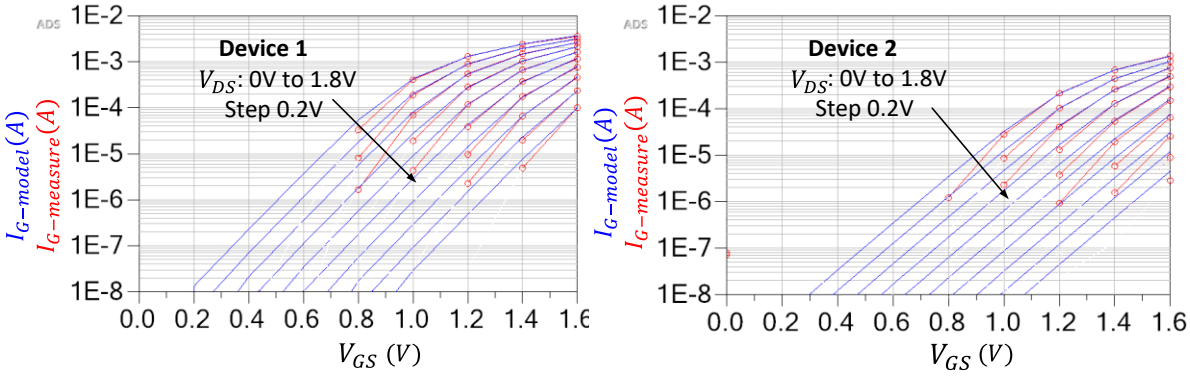

Figure 4.10 Fitting result of log scale forward gate current vs. V_{GS} and V_{DS} sweeps of device 1 (left) and 2 (right)

The contact resistance and sheet resistance are calculated using the following equations, in which W is the total width of the transistor.

$$R_{cs} = R_s \times W \tag{4.7}$$

$$R_{cd} = R_d \times W \tag{4.8}$$

$$R_{sh} = (R_{on} - R_s - R_d) \cdot \frac{W}{L_{gs}+L_{gd}+L_g} \tag{4.9}$$

The complete extraction result for parasitic resistance, contact resistance and sheet resistance is shown in Table 4.5.

Table 4.5 Extraction result for parasitic resistance, contact resistance and sheet resistance

Parameter	Device 1	Device 2
R_s (Ω)	8.392	9.724
R_d (Ω)	9.288	10.60
R_{cs} (Ω · m)	8.392E-4	9.724E-4
R_{cd} (Ω · m)	9.288E-4	10.60E-4
R_{sh} (Ω · sq)	278	226

4.1.6 Preliminary Virtual Source Model Parameters Extraction

Most of the parameters in the Virtual Source model are determined by optimizing the model output to the measurement data. However, before the optimization, a few parameters need to be extracted or estimated from the measurement as constant or initial values for optimization. The gate-to-channel capacitance is extracted as a constant while the subthreshold slope and punch through factor are extracted as initial values for optimization.

Gate Capacitance Extraction and Threshold Voltage Estimation

The gate-to-channel capacitance (C_{inv}) is defined as the capacitance between the gate and channel when the channel is fully turned on. It is an important parameter which directly impacts the current of the channel. The gate-to-channel capacitance is extracted from the value difference of the total gate capacitance before and after the channel is turned on.

The gate capacitance distribution of a GaN HEMT when the channel is turned off ($V_{GS} \ll V_{th}$) is illustrated in Figure 4.11. C_{par_gs} and C_{par_gd} are the gate parasitic capacitance and C_{ofs} and C_{ofd} are the fringing capacitance of the gate metallization. The capacitance under the gate is controlled by V_{GS} and can be written as $C_{ug}(V_{GS})$. $C_{ug}(V_{GS})$ only includes the fringing capacitance when the V_{GS} is lower than the threshold voltage but increases dramatically as V_{GS} increases higher than the threshold voltage due to the formation of the channel.

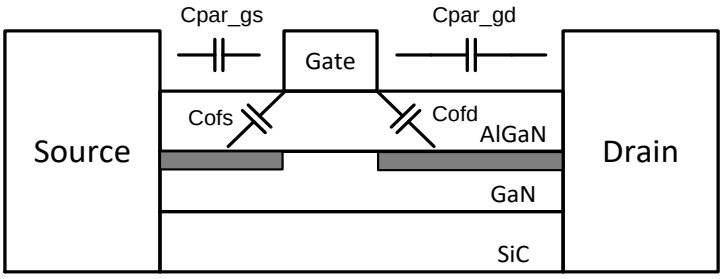

Figure 4.11 Gate capacitance distribution when the channel is turned off ($V_{GS} \ll V_{th}$)

The gate capacitance distribution of a GaN HEMT when the channel is fully turned on ($V_{GS} = 0$) is illustrated in Figure 4.12. When $V_{GS} = 0$, the channel is completely formed, and therefore the gate-to-channel capacitance (C_{inv}) remains almost constant with even higher V_{GS} and $C_{ug}(V_{GS})$ can be written as $C_{ug}(V_{GS} = 0) = C_{ofs} + C_{ofd} + C_{inv}$.

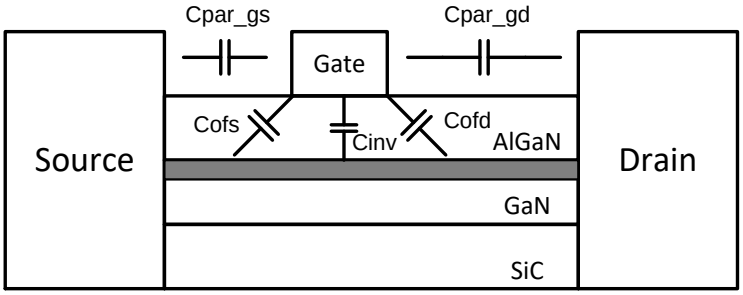

Figure 4.12 Gate capacitance distribution when the channel is fully turned off ($V_{GS} \gg V_{th}$)

The total gate capacitance is express as Equation 4.10 and the total capacitance can be calculated from low frequency (hundreds of MHz) Y-parameter converted from measured S-parameter.

$$C_{total}(V_{GS}) = C_{pad\_gs} + C_{pad\_gd} + C_{par\_gs} + C_{par\_gd} + C_{ug}(V_{GS}) \tag{4.10}$$

If the gate and drain are define as port 1 and port 2 and the transistor is biased with $V_{DS} = 0$, the total gate capacitance is defined by the Y-parameter as:

$$C_{total}(V_{GS}) = \frac{imag(Y_{11})}{j\omega} \tag{4.11}$$

Therefore, the gate-to-channel capacitance can be calculated as

$$C_{inv} = C_{ug}(V_{GS} = 0) - C_{ug}(V_{GS} \ll V_{th}) = C_{total}(V_{GS} = 0) - C_{total}(V_{GS} \ll V_{th})$$

$$= \frac{imag(Y_{11}(V_{GS}=0)) - imag(Y_{11}(V_{GS} \ll V_{th}))}{j\omega} \tag{4.12}$$

Frequency range from 200 MHz to 1 GHz is used for the total gate capacitance (C_{total}) extraction. The extracted values in the frequency range are averaged as the final value. C_{total} vs. V_{GS} sweep is shown in Figure 4.13.

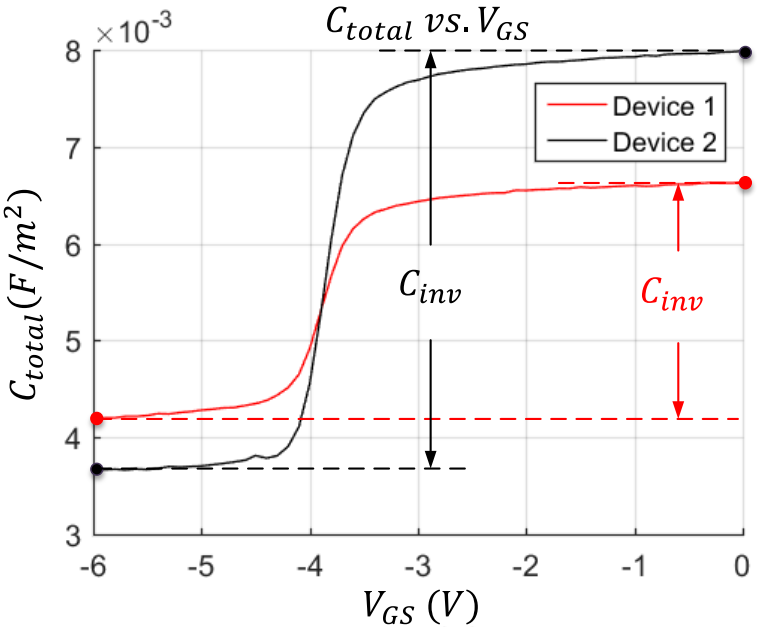

Figure 4.13 Total gate capacitance vs. V_{GS} sweep at $V_{DS} = 0$

The total gate capacitance of $V_{GS} = -6$ V and 0 V are selected as the turned-off capacitance and turned-on capacitance, as is marked in Figure 4.13. The difference between the on an off capacitance is calculated as the gate-to-channel capacitance, which is listed in Table 4.6. The threshold voltage (V_{th}) is estimated by looking for the V_{GS} value that gives the maximum slope on the C_{total} vs. V_{GS} curve. The estimated V_{th} is listed in Table 4.6. These V_{th} are initial values and will be optimized in the DC intrinsic parameter optimization section.

Table 4.6 Gate-to-channel capacitance and threshold voltage.

Parameter	Device 1	Device 2
C_{inv} (mF/m^2)	2.453	4.327
V_{th} (V)	-3.90	-3.85

The extracted gate-to-channel capacitance of device 1 and 2 diverges with each other significantly due to the process variation, which is partly because the devices were fabricated with immature process.

Subthreshold Slope and Punch Through Factor Estimation

One of the important advantages of the Virtual Source model is that the subthreshold behaviour of the transistor is correctly modeled. The subthreshold behaviour depends on the subthreshold slope and the punch through factor by the following equation.

$$SS(V_{DS}) = SS_0 + n_d \phi_t \ln(10) \cdot V_{DS} \tag{4.13}$$

In Equation 4.13, $SS(V_{DS})$ is the drain current depended subthreshold slope appeared in the Virtual Source drain current model. SS_0 is the constant subthreshold slope extracted at $V_{DS} = 0$. n_d is the punch through factor, which captures the V_{DS} dependence of SS.

The purpose of this section is to introduce a method of extracting SS_0 and n_d as initial values for the Virtual Source DC intrinsic parameter optimization. Both SS_0 and n_d affect the drain current depended subthreshold slope (SS) and in a sense they compensate each other. Therefore, extracting SS_0 and n_d initial values helps the optimizer avoid being trapped in local minima and save optimization time as well.

Log scale of drain current vs. V_{GS} is shown in Figure 4.14 and the subthreshold region used to extract subthreshold slope is highlighted in the blue quadrilateral. The subthreshold slope is defined as the maximum slope on the curve of each V_{DS} in the subthreshold region.

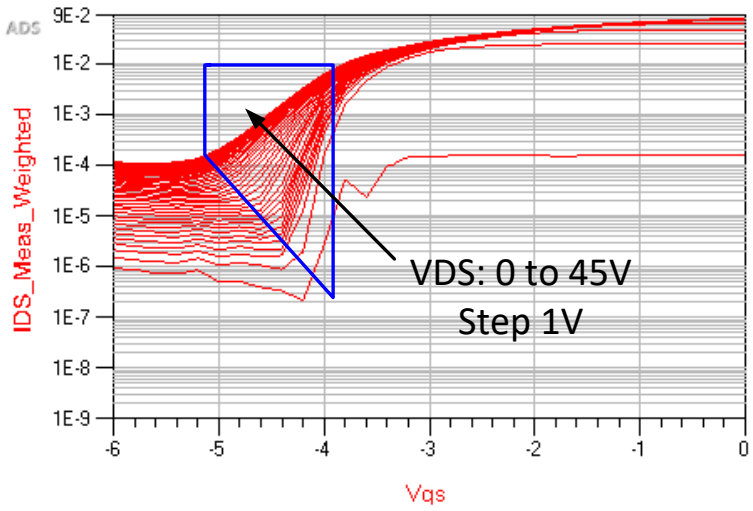

Figure 4.14 Log scale of drain current showing the subthreshold slope

The maximum slope of device 1 and 2 is searched in the quadrilateral and plotted with respect to V_{DS}, which is shown in Figure 4.15.

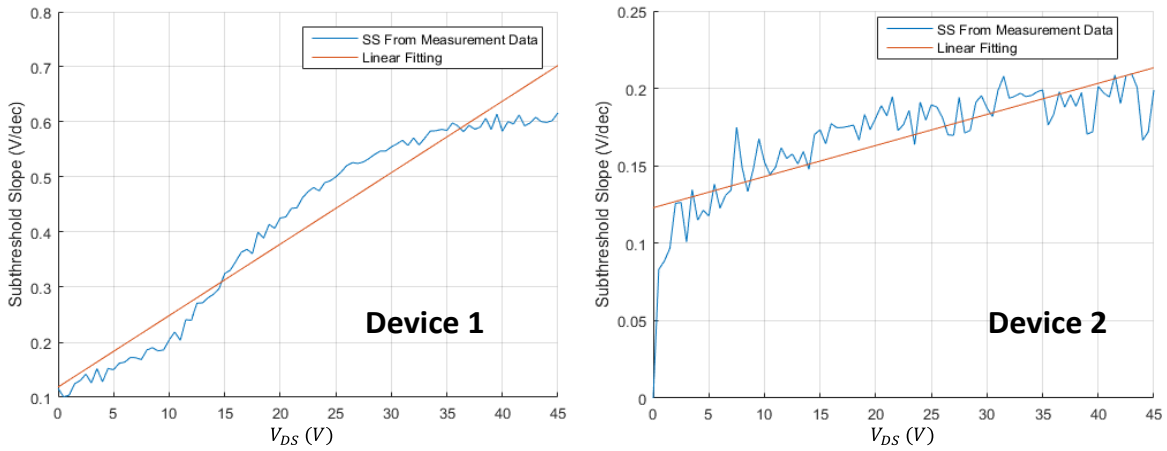

Figure 4.15 Subthreshold slope vs. V_{DS} of device 1 and 2

The zigzag shape on the extracted curves is mainly due to the fact that the maximum slope does not happen exactly at the V_{GS} point where is swept, in which case the average of two adjacent second-largest values is used. Nevertheless, the overall trend is well captured by fitting the threshold curve to the linear subthreshold slope Equation 4.13. The fitted straight line is plotted red in Figure 4.15. Punch through factor (n_d) can be calculated from the slope of the straight line and SS_0 is the interception of the straight line with V_{DS} equal to zero. The extracted result is listed in Table 4.7.

Table 4.7 Extracted result of subthreshold slope (SS_0) and punch through factor (n_d)

Parameter	Device 1	Device 2
SS_0 (V/dec)	0.11858	0.12294
n_d	0.216783	0.03354

The process variation is mainly responsible for the significant parameter difference of device 1 and 2.

4.1.7 Drain Current Modeling of Intrinsic Transistor

The DC intrinsic parameters of the Virtual Source model are obtained from optimizing the output of the model to fit the measurement data. Different error function is chosen for the optimization for above-threshold and subthreshold current due to different magnitude and span of the current. Besides, parameter sets controlling the above-threshold and subthreshold current are optimized separately, in

order to reduce optimization dimensions and avoid the difficulty of combining two separate optimization goals.

Above-threshold Drain Current Fitting

Drain current curves measured with $V_{GS} > -4$ V, which is roughly the threshold voltage, are regarded as above-threshold current. The modeling theory was introduced in section 3.5. Here the focus is the explanation of optimization procedure for parameter extraction.

A linear form rather than log form error function is used for the above-threshold optimization. This is mainly due to that the above-threshold current accuracy dominates the accuracy of the performance prediction of a power transistor. Little error in log scale could result in large difference in linear scale while linear scale error function could give a better description of the overall fitting. Therefore, a linear form error function, which normalizes the fitting error to measurement data, is used for the optimization as shown below. This is mainly due to the fact that current and voltage follows a roughly linear relationship in above-threshold region.

$$ERR_{IV-above-threshold} = \frac{1}{N_{above}} \sum_{i=1}^{N_{above}} \frac{|I_D^{model}(i) - I_D^{measure}(i)|}{|I_D^{measure}(i)|} \quad (4.14)$$

In Equation 4.14, $I_{DS}^{model}(i)$ and $I_{DS}^{measure}(i)$ are the drain current of model output and measurement data, respectively, and i is the index of all the (V_{GS}, V_{DS}) sweeping combination. N_{above} is the total number of the (V_{GS}, V_{DS}) biasing points swept for above-threshold current. The sweep range of V_{DS} starts from 1 V instead of 0 for the reason that the drain current of the model at $V_{DS} = 0$ is theoretically zero, which will always give a normalized error equal to one without any benefit to the optimization.

Apart from the initial values extracted in Section 4.1.6, the initial values of other parameters, such as saturation velocity and carrier mobility, are set to values within the common range reported by literature. Gradient optimization algorithm is chosen to optimize the model parameters to minimize the error function.

The key parameters optimized for fitting the above-threshold drain current and the optimum values are listed in Table 4.8.

Table 4.8 Key parameters optimized for fitting the above-threshold drain current

Region	Parameter		Device 1 Initial Value	Device 2 Initial Value	Device 1 Optimum Value	Device 2 Optimum Value	Unit
Gated Transistor	Saturation Velocity	v_{xo}	1.5×10^5	1.5×10^5	1.99×10^5	1.71×10^5	m/s
	Carrier Mobility	μ_0	0.2	0.2	0.23	0.22	m^2/Vs
	Transition Fitting Parameter	β	1	1	1.8	0.89	
	Threshold Voltage	V_{to}	-3.90	-3.85	-3.93	-3.90	V
	1st Order DIBL	δ_1	0	0	0.031	0.011	
	Punch Through Factor	n_d	0.217	0.034	0.22	0.034	
Source Access Region Transistor	Source Implicit Gate Capacitance	C_g^{SAR}	1×10^{-3}	1×10^{-3}	5.0×10^{-4}	5.8×10^{-4}	F/m^2
	Source Access Region Saturation Velocity	v_{xo}^{SAR}	1.5×10^5	1.5×10^5	1.55×10^5	1.33×10^5	m/s
	Source Access Region Carrier Mobility	μ_0^{SAR}	0.2	0.2	0.19	0.19	m^2/Vs
	Source Access Region Transition Fitting Parameter	β^{SAR}	1	1	0.63	0.61	
Drain Access Region Transistor	Drain Implicit Gate Capacitance	C_g^{DAR}	1×10^{-3}	1×10^{-3}	5.0×10^{-4}	5.29×10^{-4}	F/m^2
	Drain Access Region Saturation Velocity	v_{xo}^{DAR}	1.5×10^5	1.5×10^5	1.90×10^5	1.36×10^{-5}	m/s
	Drain Access Region Carrier Mobility	μ_0^{DAR}	0.2	0.2	0.15	0.15	m^2/Vs
	Drain Access Region Transition Fitting Parameter	β^{SAR}	1	1	0.81	4.71	
Thermal Coefficients	Thermal Resistance	R_{th}	10	10	8.58	18.3	K/W

The optimized saturation velocity and carrier mobility of device 1 and 2 are close to each other, and all of them represent the high carrier velocity and carrier mobility advantage of GaN HEMTs. The optimization gives an overall fitting error of 3.4% and 1.9% for device 1 and device 2, respectively. The measured and fitted above-threshold drain current curves are shown in Figure 4.16 and Figure 4.17.

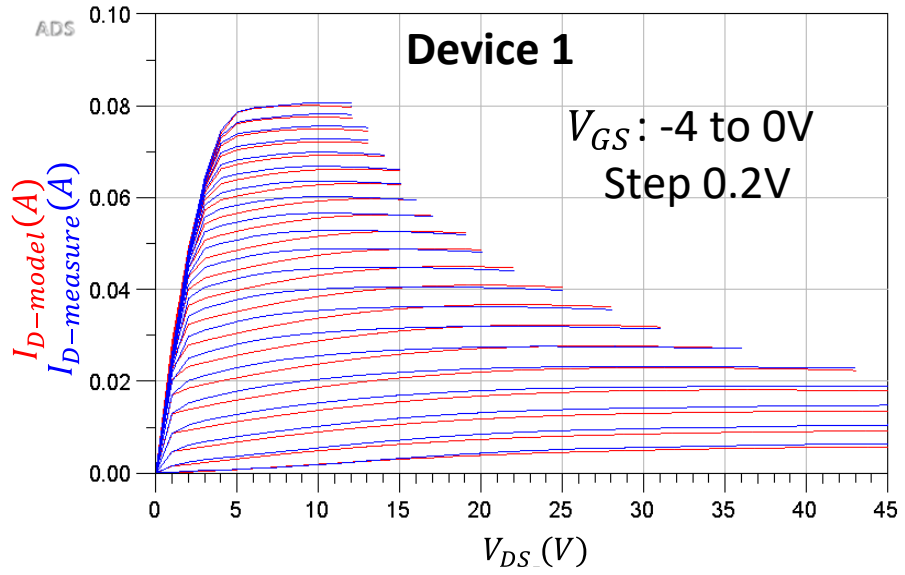

Figure 4.16 Above-threshold drain current fitting of device 1

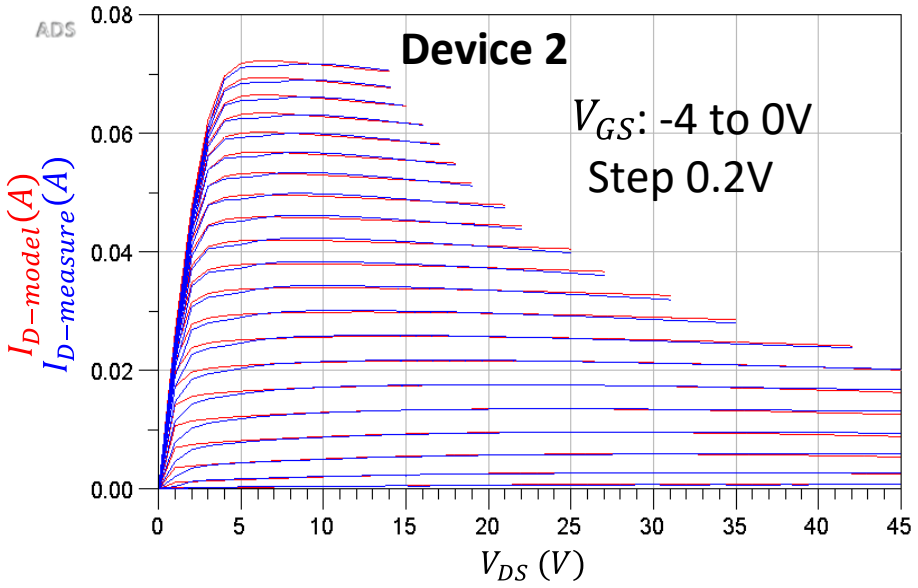

Figure 4.17 Above-threshold drain current fitting of device 2

Except that some low V_{DS} regions have relatively larger fitting error, the model accurately captures the drain current profile of the transistor. The problem of fitting error in the low V_{DS} region (triode regions) needs further investigation. One way to improve the accuracy in triode region is to make the transition fitting parameter β dependent on V_{DS}. However, doing so with ADS simulator causes

convergence issues. Therefore, this method is not used to improve triode region fitting accuracy at the moment. Besides, device 2 has more significant thermal effect than device 1, which is correctly modeled by the thermal resistance.

Subthreshold Drain Current Fitting

Drain current with $-6\ \text{V} \le V_{GS} \le -4\ \text{V}$ is regarded as subthreshold current. A log form error function is selected to calculate the subthreshold drain current error due to the reason that the subthreshold current is much lower than above-threshold current and it spans to decades of values. The log for error function directly calculates the exponent difference of the model output and measurement data without normalization, which is as follows:

$$ERR_{IV-subthreshold} = \frac{1}{N_{sub}} \sum_{i=1}^{N_{sub}} \left| \log\left(I_D^{model}(i)\right) - \log\left(I_D^{measure}(i)\right) \right| \tag{4.15}$$

$I_{DS}^{model}(i)$, $I_{DS}^{measure}(i)$ and i are defined the same as in Equation 4.14. N_{sub} is the total number of the (V_{GS}, V_{DS}) biasing points swept for subthreshold current.

In subthreshold model optimization, both subthreshold slope at $V_{DS} = 0$ (SS_0) and punch through factor (n_d) affect the actual subthreshold slope. n_d is already determined in above-threshold model optimization. Only SS_0 of the gated transistor is optimized in subthreshold optimization. The initial value is the SS_0 estimated in Section 4.1.6.

To eliminate the misguiding of gate-drain diode leakage floor in the subthreshold model optimization, I_D points higher than two times of corresponding gate leakage floor and with V_{GS} lower than -4 V (points inside the blue quadrilateral in Figure 4.14 or the upper quadrilateral in Figure 4.18 and Figure 4.19) are selected for the optimization. The optimization algorithm is Gradient. The initial value the optimum value of SS_0 is list in Table 4.9.

Table 4.9 Initial value and the optimum value of SS_0

Region	Parameter	Device 1 Initial Value	Device 2 Initial Value	Device 1 Optimum Value	Device 2 Optimum Value	Unit
Gated Transistor	SS_0 (Subthreshold Slope at $V_{DS} = 0$)	0.12	0.12	0.08	0.151	V/dec

The measured and fitted subthreshold drain current curves of device 1 and device 2 are shown in Figure 4.18 and Figure 4.19.

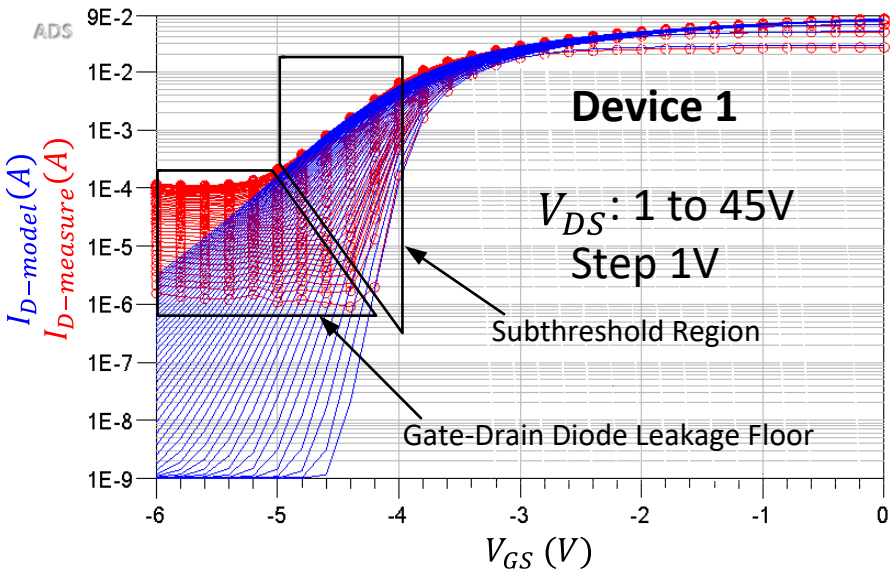

Figure 4.18 Subthreshold region fitting of device 1

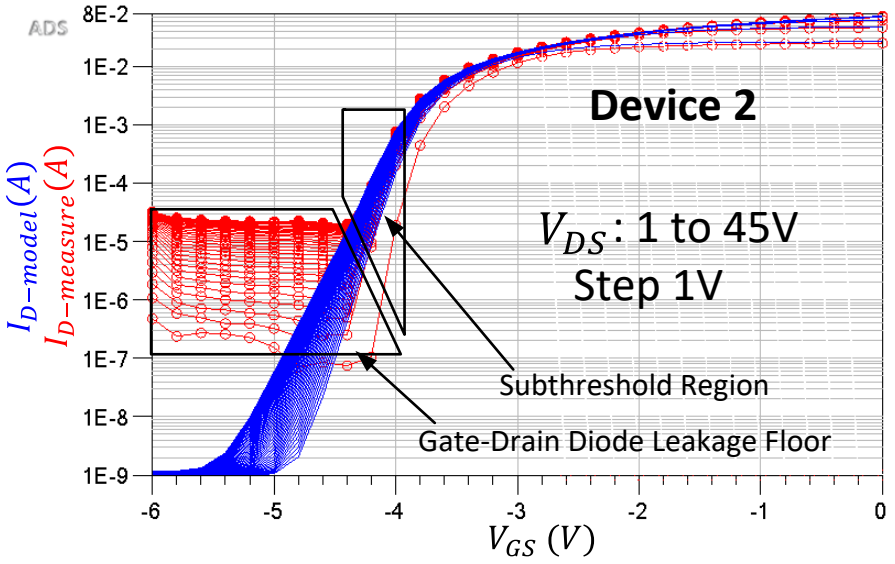

Figure 4.19 Subthreshold region fitting of device 2

Due to process variation, the subthreshold regions of device 1 and device 2 show different slopes and V_{DS} dependence, which are accurately captured and modeled by SS_0 and n_d. The drain current leakage floor is due to the reverse leakage from drain to gate at high V_{DS}, which will be modeled in the next section.

4.1.8 Reverse Diode Parameter Extraction

Gate-Drain Reverse Diode Parameter Extraction

The equations to model gate reverse current is introduced in Section 3.4. The gate reverse current consists of two parts – the gate-drain reverse current and gate-source reverse current. Gate-drain reverse current determines the I_D floor at low V_{GS} shown in $I_D(V_{DS}, V_{GS})$ plot while the sum of the two parts determines the overall leakage at low V_{GS} shown in $I_G(V_{DS}, V_{GS})$ plot. Therefore, parameters of gate-drain reverse diode are extracted first from the drain current leakage floor and after that parameters of gate-source reverse diode are extracted from the rest of gate leakage current to form a complete reverse diode model.

The reverse current density I_{rec}, the ideality factor for the reverse diode η_{rec} and the empirical reverse saturation voltage for gate-drain V_{gsatd} are optimized to fit the I_D of the model to the measured I_D leakage floor. Log form error function (Equation 4.15) is used for the gate-drain reverse current optimization. Two times of $I_D(V_{DS}, V_{GS} = -6V)$ of each V_{DS} is regarded as the floor current threshold and all the $I_D(V_{DS}, V_{GS})$ points less than the floor current threshold (the lower quadrilateral in Figure 4.18 and Figure 4.19) are selected as data set for the optimization.

The optimum parameters for the gate-drain reverse diode are listed in Table 4.10.

Table 4.10 Optimum parameters for the gate-drain reverse diode

Parameter	Device 1	Device 2
η_{rec}	3.37	3.36
I_{jrec} (mA/mm)	1×10^{-9}	3×10^{-10}
V_{gsatd} (V)	1.87	1.84

The measured and fitted gate-drain reverse leakage floor are shown in Figure 4.20 and Figure 4.21, respectively.

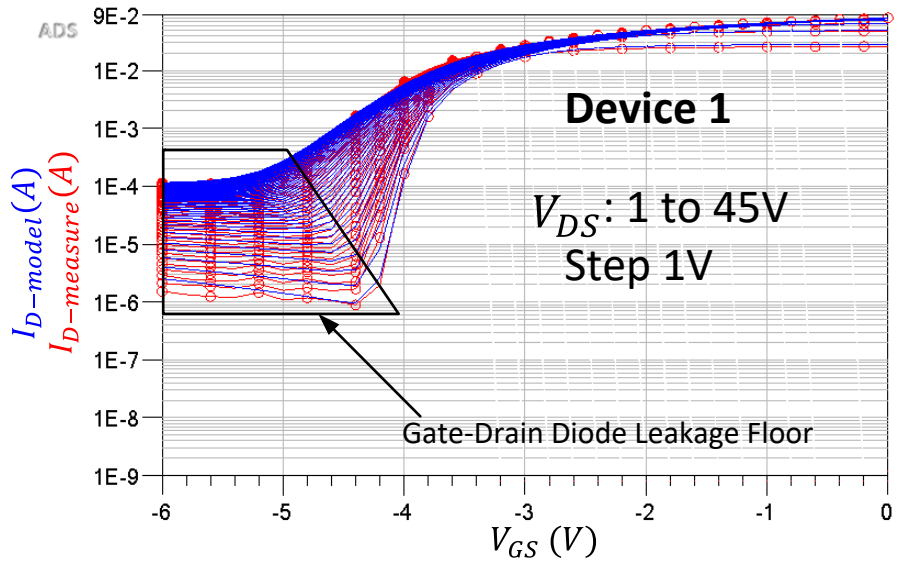

Figure 4.20 Fitting of gate-drain reverse leakage floor of device 1

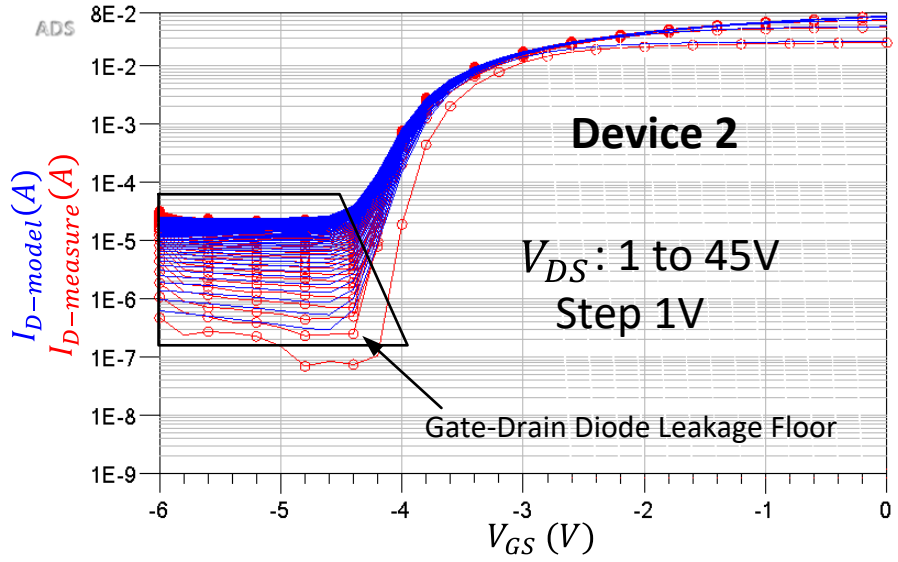

Figure 4.21 Fitting of gate-drain reverse leakage floor of device 2

Gate-Source Reverse Diode Parameter Extraction

After the parameters of gate-drain reverse diode are determined, the reverse current density I_{rec} and the ideality factor η_{rec} for gate-source reverse diode are determined as well. The only variable to be optimized for gate-source reverse diode is the reverse saturation voltage V_{gsats}. V_{gsats} is optimized to

fit the gate current I_G to measurement data. Log form error function (Equation 4.15) and gradient algorithm are selected in the optimization. In order to avoid the impact of measurement noise, only the measured I_G with V_{GS} lower than -4 V is used in the optimization.

The optimum parameter for the gate-drain reverse diode is listed in Table 4.11.

Table 4.11 Optimum parameters for the gate-source reverse diode

Parameter	Device 1	Device 2
V_{gsats} (V)	1.87	2.15

The measured and fitted gate reverse current with the full range V_{GS} sweep are shown in Figure 4.22 and Figure 4.23, respectively.

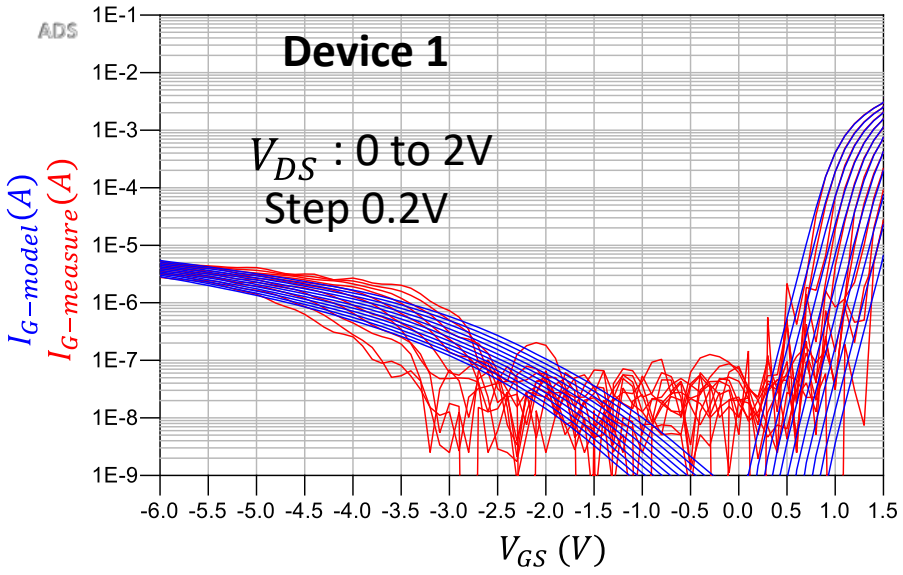

Figure 4.22 Gate current with both forward and reverse current of device 1

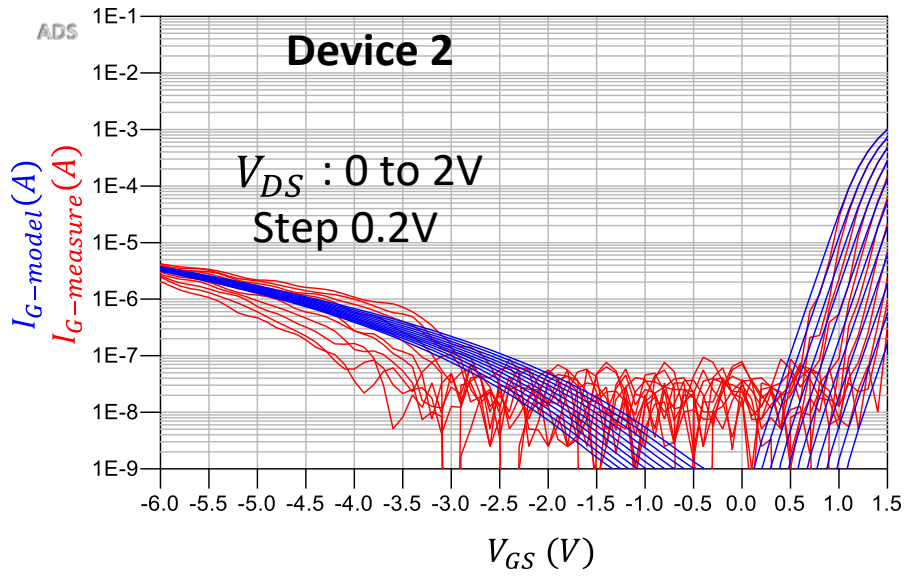

Figure 4.23 Gate current with both forward and reverse current of device 2

From Figure 4.20 to Figure 4.23, it is clear that the proposed Schottky gate diode model not only models the reverse and forward gate current for a large range of V_{GS} sweep, but also captures the drain current leakage floor at low V_{DS}. The parameters extracted are physics based, which clearly describes the device behaviour, and are able to facilitate future device design and optimization.

4.1.9 RF (Parasitic) Parameter Extraction

Because of Virtual Source model's physics based characteristic, the charge model is determined as well when the parameters are extracted from DC-IV measurement. The intrinsic model constructed from DC-IV measurement has the capability of describing the RF behavior of the intrinsic transistor, but the parasitic model cannot be extracted from pure DC measurement. Therefore, the measured S-parameter is used to extract the parasitic gate resistance (which cannot be separated form GaN Cap layer resistance introduced in Section 4.1.5), inductance and capacitance in the equivalent circuit shown in Figure 3.5 and Figure 3.6.

The behavior of parasitic gate resistance (R_g) is mainly represented by S_{11}. R_g has much less impact on the other S-parameters (ie. S_{12},$S_{21}$and S_{22}). Besides, optimizing R_g with other parasitic parameters results in a higher dimensional optimization space (RCL space instead of only R space), in which the optimization will be easily trapped in local minima. Therefore, in our methodology, R_g is extracted from S_{11} optimization first. After that parasitic inductance (L_g, L_d, L_s) and capacitance

($C_{par\_gs}, C_{par\_gd}, C_{par\_ds}$) are optimized to fit the overall S-parameter of the complete model (with GSG pad model) to the S-parameter from the measurement.

S-parameter Dataset for Parasitic Optimization

The parasitic elements optimization is based on the constructed DC Virtual Source model. The DC fitting accuracy significantly affects the parasitic element values when they are optimized to fit model S-parameter to the measured S-parameter. For example, the DC transcondutance (g_m), which is the origin of transistor gain, determines S_{21} together with the input and output RCL network. If the DC transconductance is not correctly modeled, the error will propagate to the RCL values during the optimization. Besides, S-parameter simulation is computationally intensive. It takes a huge amount of time to optimize the model with respect to all the biasing points. Considering the two issues above, only the V_{DS} point that gives the best I_D fitting (thus, the best g_m fitting as well because g_m is the derivative of I_D vs. V_{GS}) is selected and the corresponding S-parameters are used in the parasitic optimization.

Simulation shows that $V_{DS} = 12$ V for device 1 and $V_{DS} = 10$ V for device 2 give the most accurate I_D and g_m fitting with the full V_{GS} sweep from the threshold voltage to zero, which is highlighted in Figure 4.24 and Figure 4.25. The I_D points of the model and measurement on the dashed line fit each other with the least error (3.3% of device 1and 1.8% of device 2).

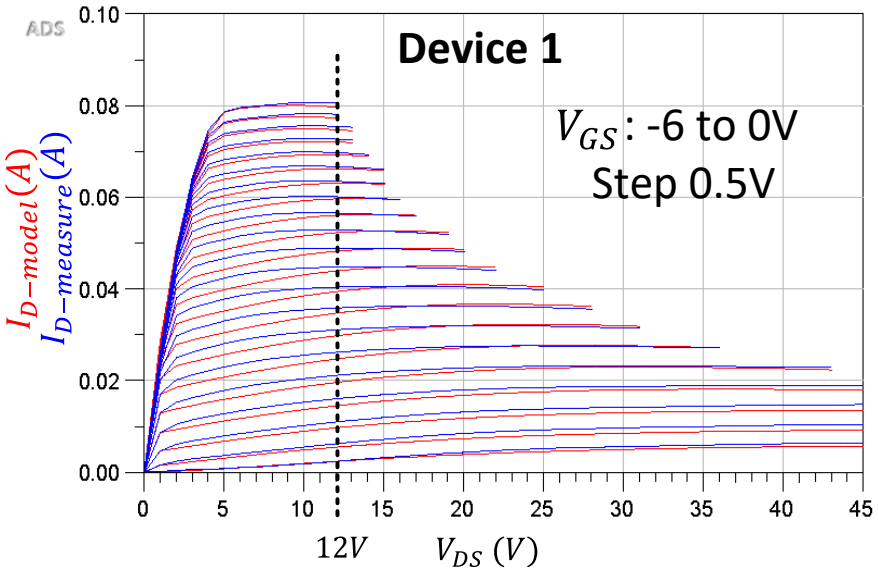

Figure 4.24 $V_{DS} = 12$ V gives the best I_D and g_m fitting of device 1

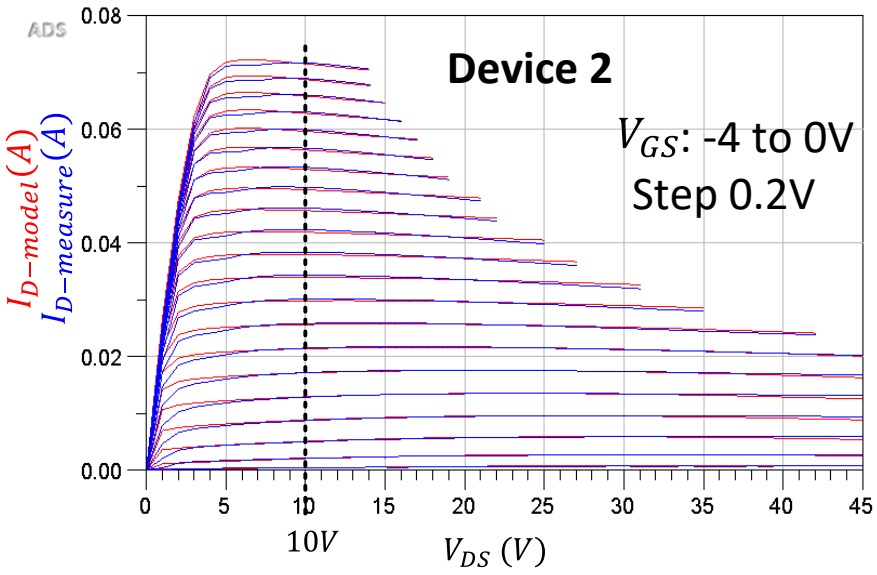

Figure 4.25 $V_{DS} = 10$ V gives the best I_D and g_m fitting of device 2

The S-parameter with $V_{DS} = 12$ V from device 1 measurement and $V_{DS} = 10$ V from device 2 measurement are used in the following optimization.

There are two rounds of optimization in this step. In the first round, R_g is optimized with parasitic inductance and capacitance set to 0. R_{series} is then decided by using the optimum value of R_g. In the second round, R_g and R_{series} are fixed to the final value for last round of optimization, in which the parasitic inductance and capacitance are determined.

Round 1: Parasitic Gate Resistance Optimization

Parasitic gate resistance (R_g) is optimized to fit S_{11} of the model to the $S_{11}$of the measurement. At this time, the parasitic inductance and capacitance are not determined yet. Setting them to 0 is a reasonable choice without affecting the result of R_g.

S-parameter data include a set of vectors, and an error vector magnitude (EVM) form error function is used for the S-parameter fitting error calculation, which is shown as follows.

$$E_{11}^{i} = \frac{\sqrt{\left|real(S_{11-model}^{i} - S_{11-meas}^{i})\right|^2 + \left|imag(S_{11-model}^{i} - S_{11-meas}^{i})\right|^2}}{|S_{11-meas}^{i}|} \tag{4.16}$$

$$E_{12}^{i} = \frac{\sqrt{\left|real(S_{12-model}^{i} - S_{12-meas}^{i})\right|^2 + \left|imag(S_{12-model}^{i} - S_{12-meas}^{i})\right|^2}}{|S_{12-meas}^{i}|} \tag{4.17}$$

$$E_{21}^{i} = \frac{\sqrt{\left|real\left(S_{21-model}^{i} - S_{21-meas}^{i}\right)\right|^{2} + \left|imag\left(S_{21-model}^{i} - S_{21-meas}^{i}\right)\right|^{2}}}{\left|S_{21-meas}^{i}\right|} \tag{4.18}$$

$$E_{22}^{i} = \frac{\sqrt{\left|real\left(S_{22-model}^{i} - S_{22-meas}^{i}\right)\right|^{2} + \left|imag\left(S_{22-model}^{i} - S_{22-meas}^{i}\right)\right|^{2}}}{\left|S_{22-meas}^{i}\right|} \tag{4.19}$$

$$ERR_{SP} = \frac{1}{N_{SP}} \sum_{i=1}^{N_{SP}} \frac{1}{4} \times \left(E_{11}^{i} + E_{21}^{i} + E_{12}^{i} + E_{22}^{i}\right) \tag{4.20}$$

Gradient algorithm is used in R_g optimization. The S_{11} before and after R_g optimization of device 1 and device 2 are shown in Figure 4.26 and Figure 4.27 respectively.

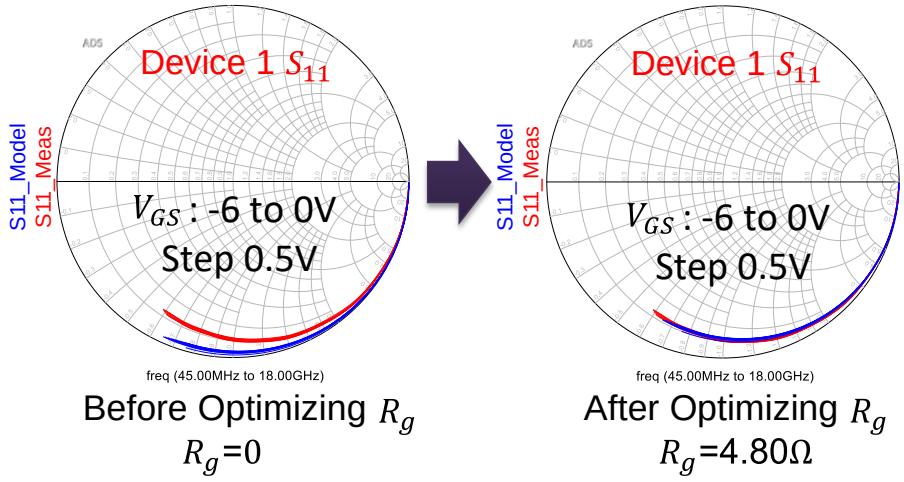

Figure 4.26 S_{11} before and after R_g optimization of device 1

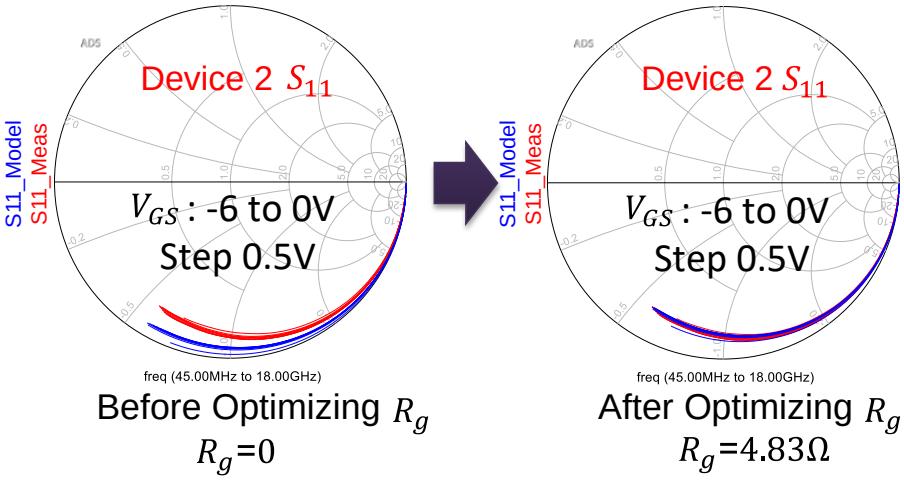

Figure 4.27 S_{11} before and after R_g optimization of device 2

Optimization of R_g converges the modeled S_{11} curves to the measured S_{11} curves. The model accurately captures the S_{11} behavior of the device. In the section of forward diode parameter extraction (Section 4.1.4), R_g and the effective series resistance R_{series} cannot be separated. Therefore, the sum of R_g and R_{series} were extracted. Now the values of both R_g and R_{series} are determined, which are listed in Table 4.12.

Table 4.12 Result of parasitic gate resistance (R_g) and effective series resistance (R_{series})

Parameter	Device 1	Device 2
R_g (Ω)	4.80	4.83
R_{series} (Ω)	126	200

Round 2: Parasitic Inductance and Capacitance Optimization

Parasitic inductance (L_g, L_d, L_s) and capacitance ($C_{par\_gs}, C_{par\_ds}, C_{par\_gd}$) are optimized to fit the overall S-parameter ($S_{11}, S_{12}, S_{21}, S_{22}$) of the model to the S-parameter of the measurement. Here the same S-parameter error function and optimization algorithm are used as introduced in last section.

The model S-parameters after optimization of device 1 and 2 are shown in Figure 4.28 and Figure 4.29. The total S-parameter EVM fitting error for device 1 and device 2 are 7.4% and 6.8% respectively. The model accurately captures the voltage gain S_{21} and reflection coefficient S_{11} of the device, which is of great importance for power amplifier design. The EVM fitting error for isolation S_{12} is relative large, but since the absolute value of S_{12} is always very small (< 0.1) compared to other S-parameters, the error in S_{12} has very little affection on performance prediction, and therefore the S_{12} fitting error can be accepted. The modeled S_{22} correctly captures the trend of measured S_{22}, but there is certain discrepancy in the amplitude of the modeled and measured S_{22} data. The amplitude difference represents the difference in output resistance of the model and the measurement, which needs further investigation. Detailed EVM error with respect V_{DS} is listed in Table 4.14.

Device 1

V_{GS} : -6 to 0V
Step 0.5V

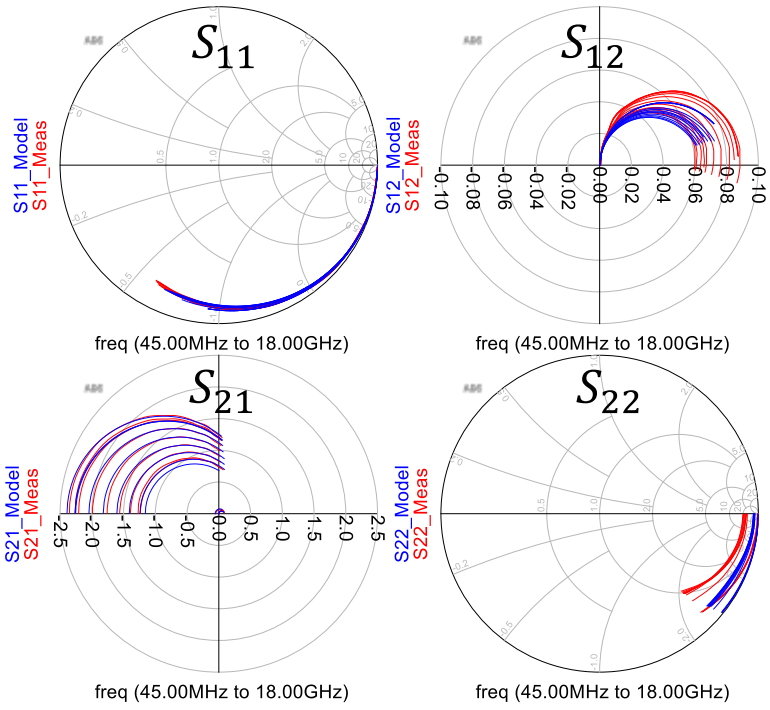

Figure 4.28 S-parameter fitting of device 1

Device 2

V_{GS} : -6 to 0V
Step 0.5V

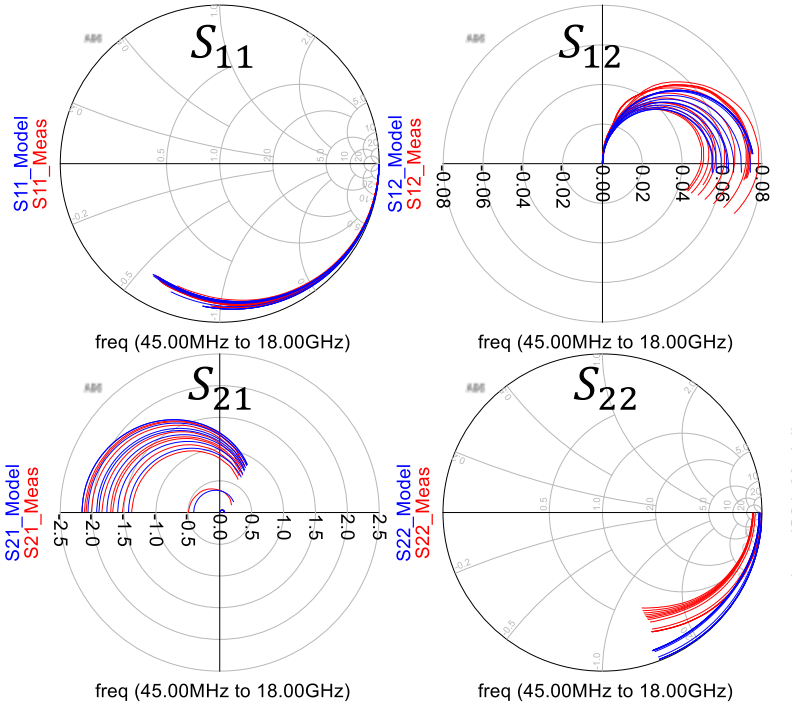

Figure 4.29 S-parameter fitting of device 2

Since S_{21} is the most critical for power amplifier design, the magnitude and phase of S_{21} of device 1 and device 2 are plotted separately in rectangular plots, which are shown Figure 4.30. Both the magnitude and phase of S_{21} are reasonably well described by the proposed model.

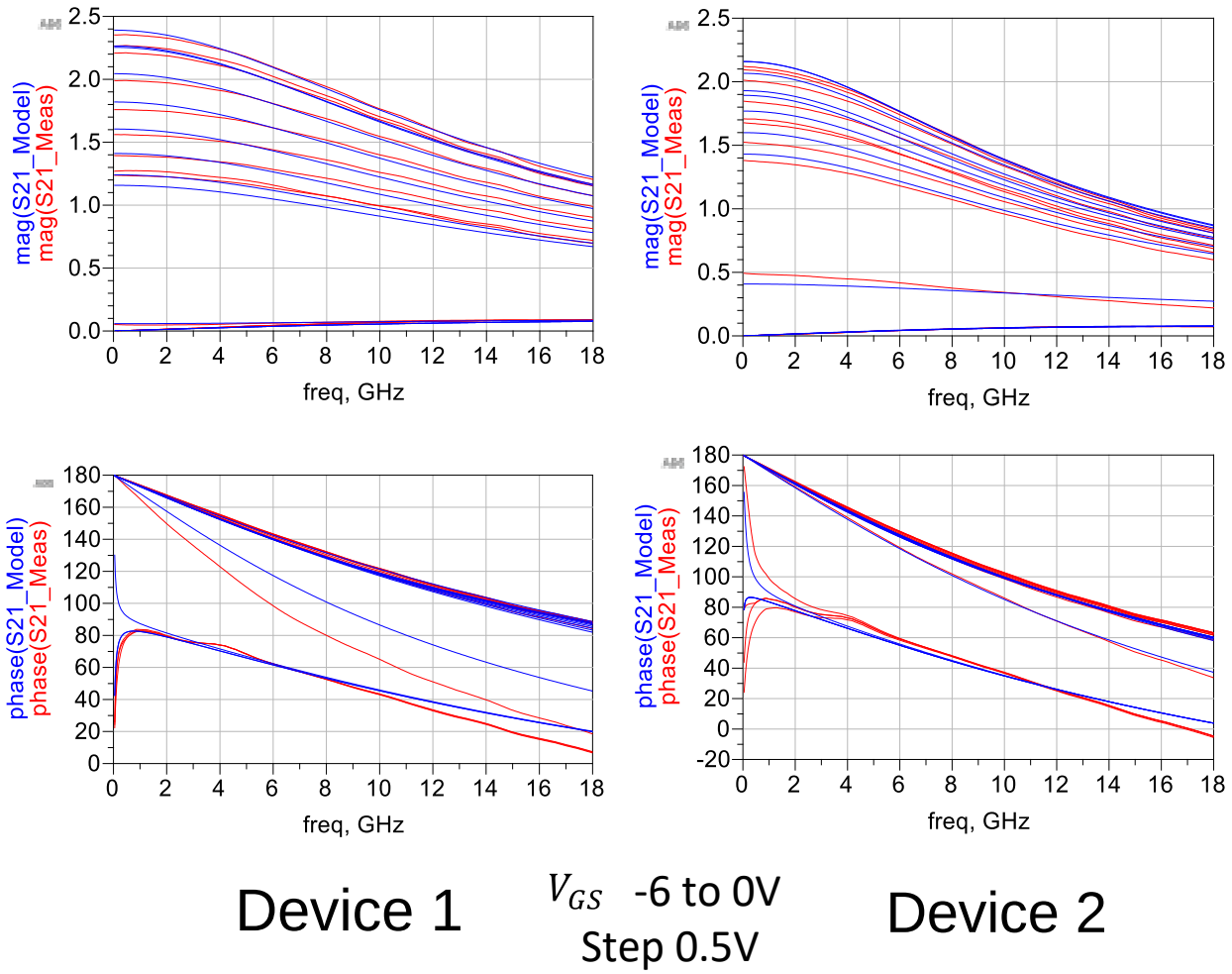

Figure 4.30 Magnitude and phase of S_{21} of device 1 (left two plots) and device 2 (right two plots)

The optimum values of the parasitic inductance and capacitance from the optimization are list in Table 4.13. The optimum parameters of device 1 are reasonably close to those of device 2 (within the same decade), due to the reason that parasitics are passive elements and the process variation of passive elements is much less severe than process variation in active regions.

Table 4.13 Optimum values of the parasitic inductance and capacitance

Parameter	Device 1	Device 2
L_g (pH)	10.75	8.16
L_d (pH)	25.3	15.75
L_s (pH)	9.16×10^{-3}	7.26×10^{-3}
C_{par_gs} (pF)	0.162	0.168
C_{par_gd} (pF)	1.08×10^{-3}	3.01×10^{-3}
C_{par_ds} (pF)	0.029	0.084

S-parameter EVM Fitting Error Summary

The overall EVM error and the EVM error of each S-parameter with respect to V_{DS} are listed in Table 4.14. Generally, S_{11}, S_{21} and S_{22} are better modeled than S_{12} due to the large absolute values of S_{11}, S_{21} and S_{22} which give dominant affection in not only guiding the optimization but also predicting the transistor performance. A significant degradation of S_{22} happens in the saturation regime (high V_{DS}) for both device 1 and 2, which indicates that output impedance significantly changes in saturation region. This issue needs further investigation.

Table 4.14 S-parameter EVM fitting error of different V_{DS}

V_{DS}	Device 1					Device 2				
	S11	**S12**	**S21**	**S22**	**Overall**	**S11**	**S12**	**S21**	**S22**	**Overall**
5V	9.8%	25.4%	13.9%	19.4%	17.1%	3.2%	9.6%	8.9%	14.1%	9.0%
10V	8.4%	14.9%	8.1%	13.0%	11.1%	3.4%	5.7%	5.4%	12.8%	6.8%
20V	5.1%	4.9%	4.0%	9.0%	5.7%	2.8%	9.1%	5.0%	13.1%	7.5%
30V	4.3%	6.2%	5.0%	12.8%	7.1%	2.6%	10.6%	7.0%	19.7%	10.0%
40V	3.3%	6.2%	4.8%	14.7%	7.3%	2.7%	11.9%	9.50%	31.1%	13.8%

The proposed model with its optimum parameters is validated in the next section.

4.2 Model Validation

4.2.1 Drain Current Model Validation

The measurement dataset for device validation should be completed independently from the dataset used for model parameter extraction to avoid the error dependence inheritance. Base on this dependence requirement, the dataset for model validation is obtained by shifting both the V_{GS} and V_{DS} by a constant value from the V_{GS} and V_{DS} points swept in the dataset for model parameter extraction.

Due to the wide span (from μA to a hundred of mA), drain current is validated in two parts – above-threshold current validation in linear scale and subthreshold current validation in log scale.

Above-Threshold Drain Current

As shown in Table 4.2, V_{GS} and V_{DS} sweepings for drain current validation are shifted by 0.1 V and 0.5 V from the sweepings for model parameter extraction, respectively. Drain current points with $V_{GS} \geq -3.9$ V (shifted threshold voltage from -3.8 V to -3.9 V) are regarded as above-threshold current. The above-threshold drain current points of device 1 and device 2 vs. V_{DS} are plotted in Figure 4.31.

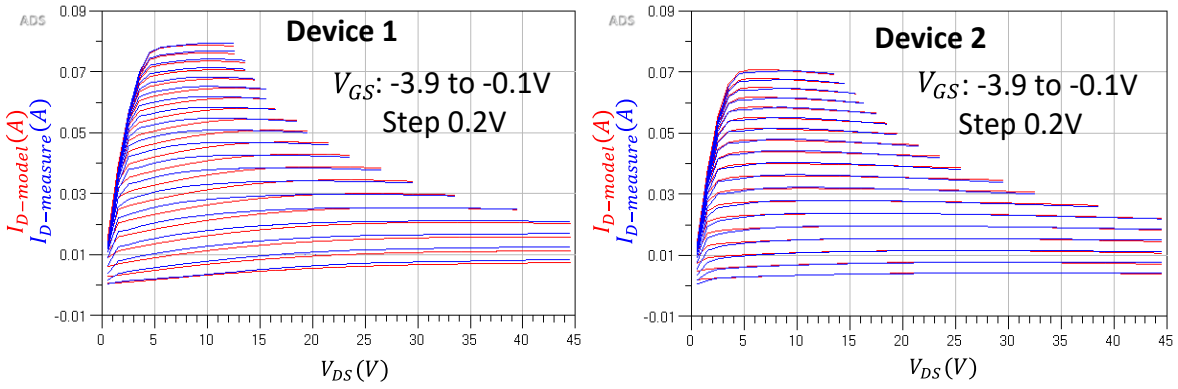

Figure 4.31 Above-threshold drain current with shifted biasing of device 1 (left) and device 2 (right)

Figure 4.31 shows that except some low V_{DS} regions (triode region) have relatively larger fitting error, the model accurately predicts the drain current profile compared measurement data. The overall fitting error of device 1 and device 2 with the shifted biasing are 4.4% and 2.4%, respectively.

Subthreshold Drain Current and Gate-Drain Reverse Leakage

The subthreshold drain current and the gate-drain reverse leakage are plotted in log scale in Figure 4.32. The subthreshold slope and its dependence on V_{DS} is correctly modeled and validated by the constructed model.

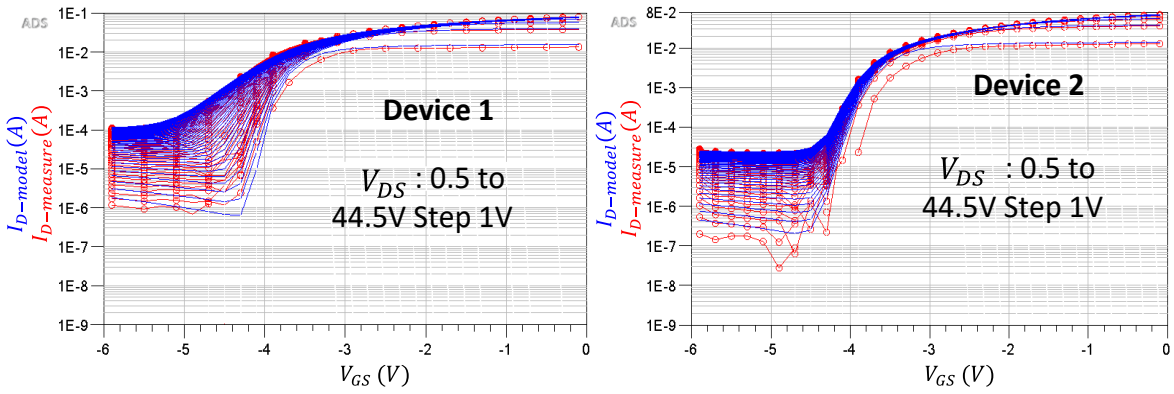

Figure 4.32 Subthreshold drain current and gate-drain reverse leakage of device 1 (left) and device 2 (right)

The gate-drain leakage that caused the drain current floor is modeled and validated as well. Leakage current above 1×10^{-6}A is well captured by the gate-drain diode. Leakage current below 1×10^{-6}A is reaching the instrument's limitation. Therefore, the current deviation between the model and measurement data below 1×10^{-6}A in the right figure is reasonable to be neglected, due to the unreliable measurement.

4.2.2 Gate Current Model Validation

Similar to the drain current validation, both V_{GS} and V_{DS} sweepings for gate current validation are shifted by 0.1 V from the sweepings for model parameter extraction (Table 4.2). The forward mode current is validated in linear scale due to its relatively large value. The total gate current with both forward and reverse current is validated in log scale with full V_{GS} range from -5.9 V to 1.5 V.

Forward Mode Current in Linear Scale

Forward gate current with shifted biasing sweepings of device 1 and device 2 is plotted in Figure 4.33. The gate forward diode model accurately predicted the gate current with respect to both V_{GS} and V_{DS}. Upper limit up to $V_{GS} = 1.5$ V is high enough for validation purpose since the device is reaching

its operating limitation at this voltage. In common power amplifier designs, the gate voltage seldom reaches such a high value.

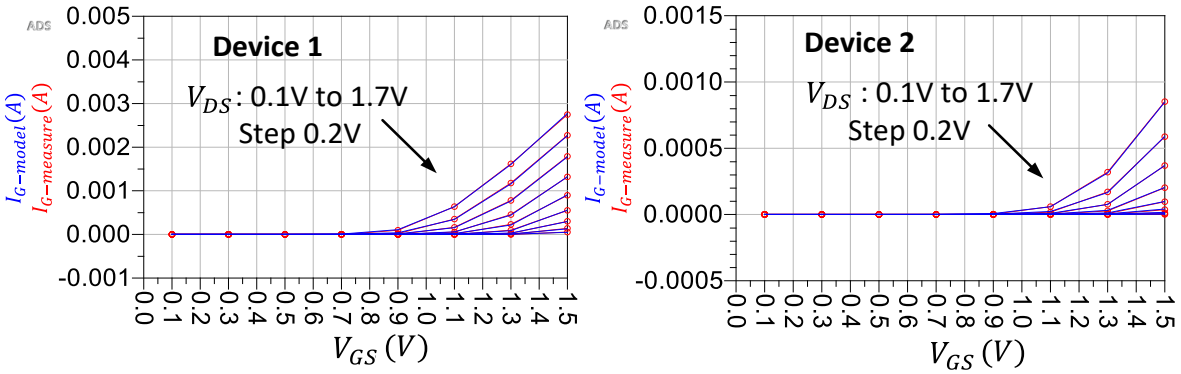

Figure 4.33 Linear scale forward gate current vs. shifted V_{GS} and V_{DS} sweeps of device 1 (left) and 2 (right)

Forward and Reverse Mode Current in Log Scale

The gate current in log scale with full range of V_{GS} sweep of device 1 and device 2 is plotted in Figure 4.34. Gate current measured below 1×10^{-6}A is discarded due to the unreliable measurement error due to the equipment limitation.

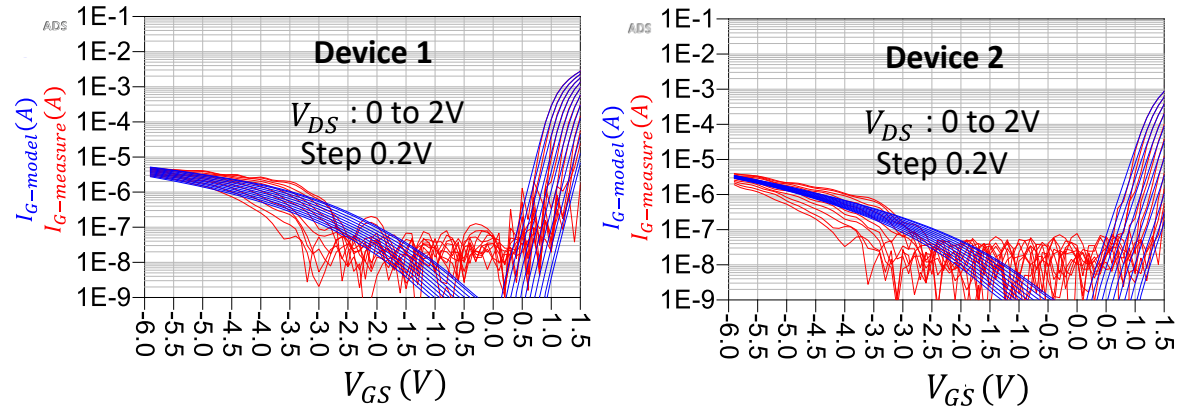

Figure 4.34 Log scale gate current with both forward and reverse current of device 1 (left) and device 2 (right)

The proposed Schottky gate diode model is validated with the full range V_{GS} sweep. The model accurately describes the forward gate current above 1×10^{-5}A. For the forward and reverse current

between 1×10^{-5}A and 1×10^{-6}A, the modelling accuracy is not as accurate as gate current above $1\times10^{-5}A$, but still accurate for circuit simulation.

4.2.3 S-parameters Model Validation

In Section 4.1.9, the S-parameters of the V_{DS} that achieve the most accurate I_{DS} fitting vs. V_{GS} are selected for optimizing the parasitic elements. The optimum V_{DS} found for device 1 and device 2 is 12 V and 10 V, respectively. Here the optimum V_{DS} is shifted upwards by 0.5 V to validate the vector S-parameters and the magnitude and phase of S_{21}. The shifted optimum V_{DS} of device 1 and device 2 for validation are 12.5 V and 10.5 V respectively.

S-parameters on Smith Chart

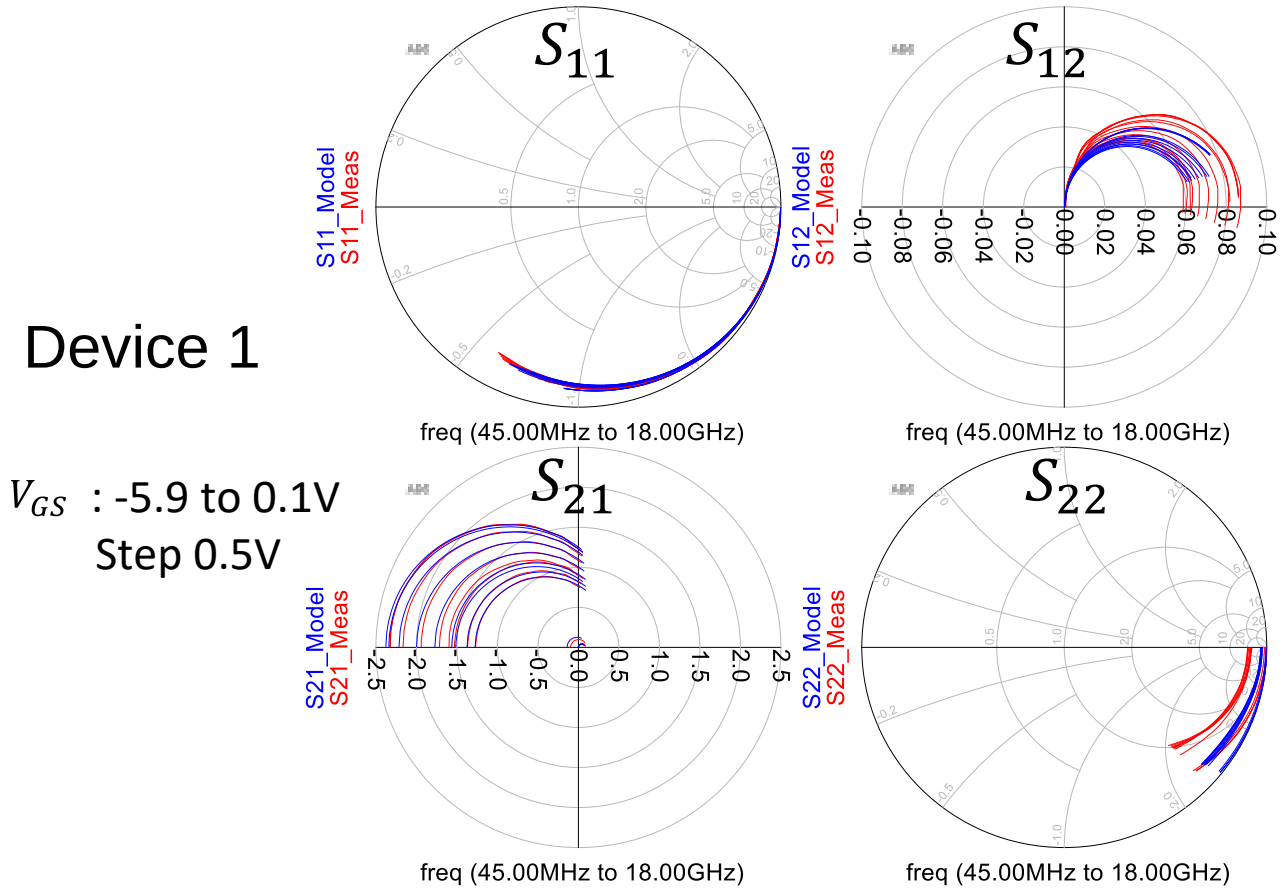

Figure 4.35 S-parameter validation of device 1

The S-parameters of device 1 and device 2 on the shifted optimum V_{DS} are shown in Figure 4.35 and Figure 4.36. Using the validation dataset, the total S-parameter EVM fitting errors for device 1 and device 2 are 7.7% and 6.9%, respectively, which are close to that error in the previous chapter. The model accurately captures the voltage gain S_{21} and reflection coefficient S_{11} of the device. Using the parameter extraction dataset, the relative large error in S_{12} and S_{22} has the same pattern of those appeared in the corresponding smith chart of the previous chapter, which needs further investigation.

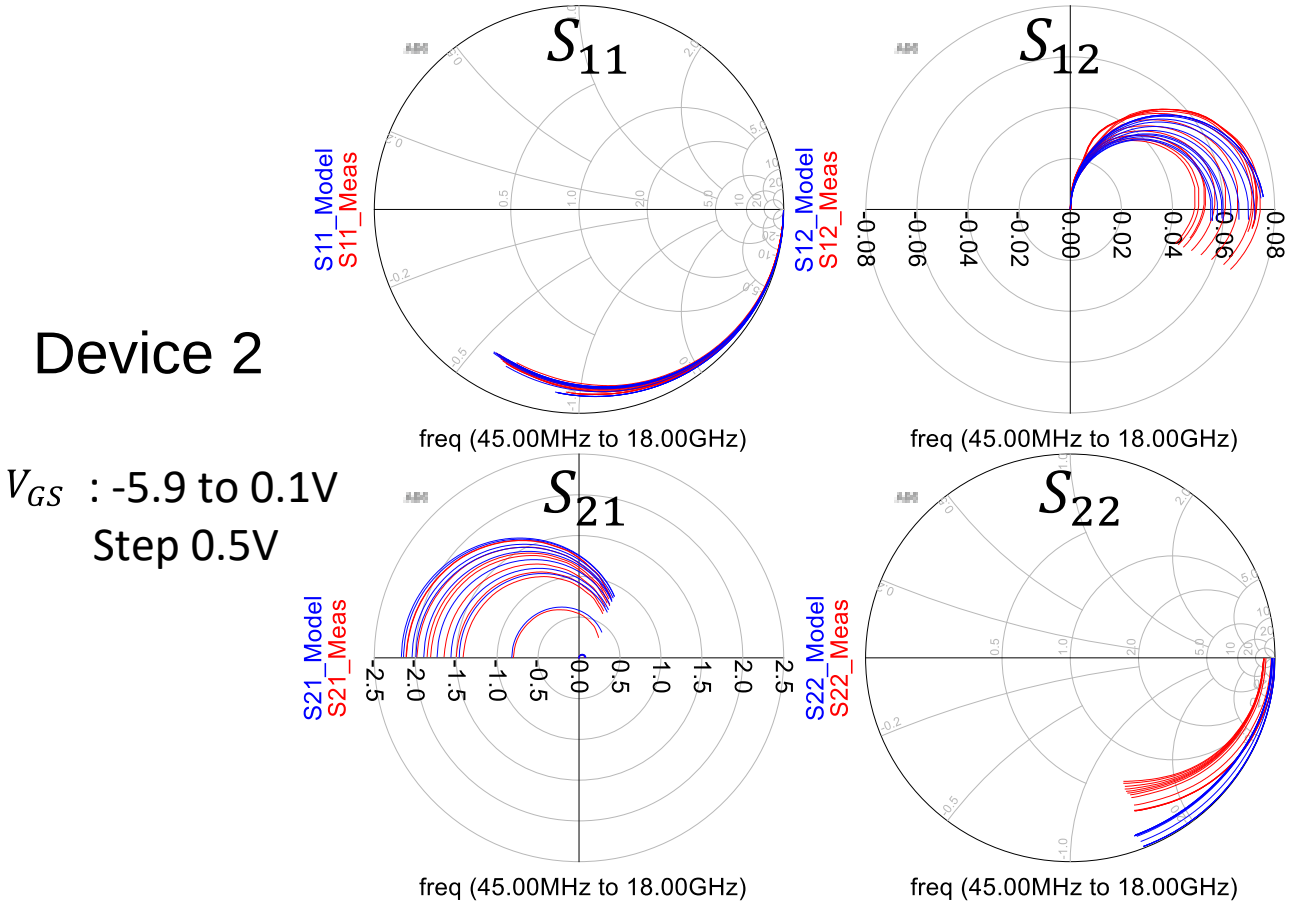

Figure 4.36 S-parameter validation of device 2

Magnitude and Phase of S_{21}

The magnitude and phase of S_{21} for the two device are shown in Figure 4.37. The magnitude and phase of S_{21} are separately validated by dataset from independent measurement.

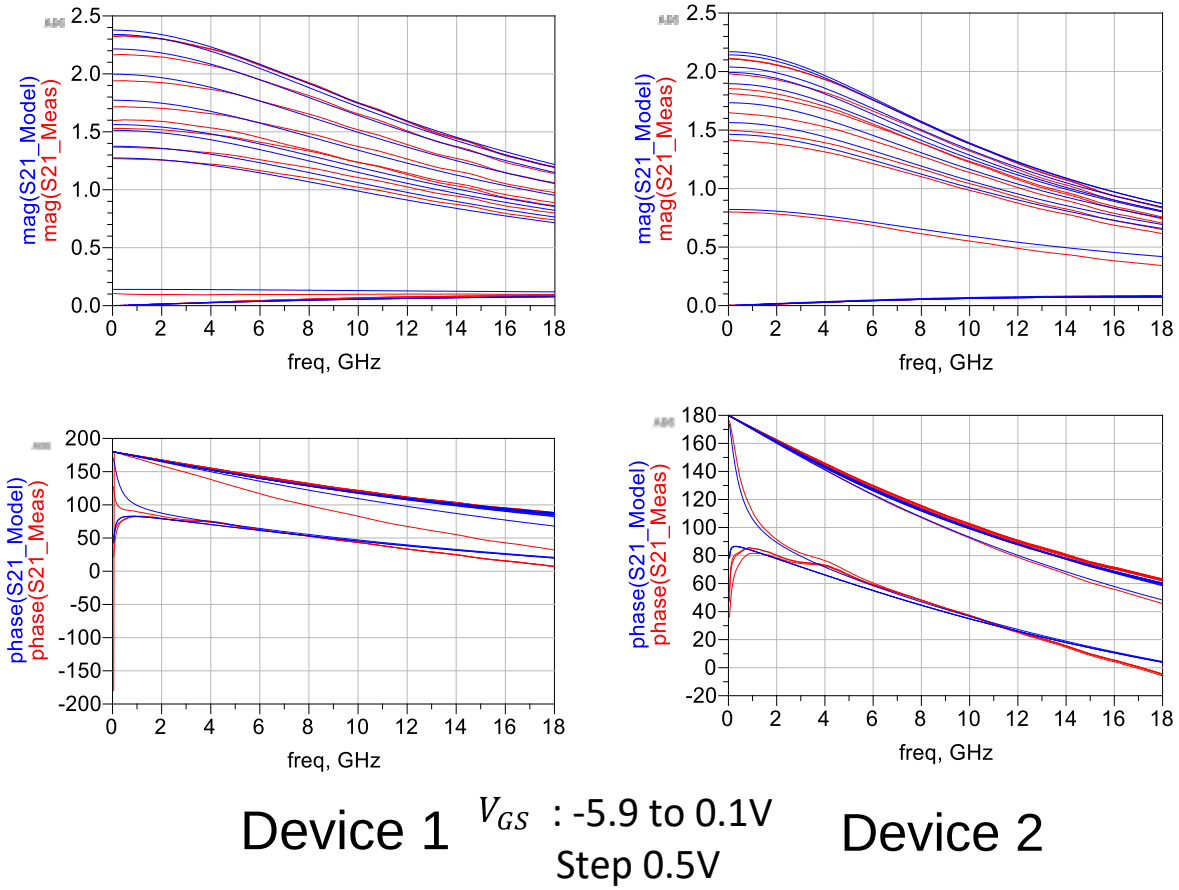

Figure 4.37 Magnitude and phase of S_{21} of device 1 (left two plots) and device 2 (right two plots)

The proposed model accurately captures both the amplitude and phase of S_{21}, which provides a solid evidence for the model's capability of power amplifier simulation.

S-parameter EVM Validation Error Summary

The overall EVM error and the EVM error of each S-parameter with the dataset under original biasing for extraction (last chapter) and the dataset under shifted biasing for validation (this chapter)

are listed in Table 4.15. The fitting error before and after the biasing shift are close to each other, which proves the model's validity for the full biasing range.

Table 4.15 S-parameter EVM error comparison of parameter extraction and validation

V_{DS}		Device 1					Device 2				
		S11	S12	S21	S22	Overall	S11	S12	S21	S22	Overall
Fitting	5V	9.8%	25.4%	13.9%	19.4%	17.1%	3.2%	9.6%	8.9%	14.1%	9.0%
Val	5.5V	10.1%	26.4%	13.5%	19.9%	17.5%	3.5%	10.2%	7.7%	15.0%	9.1%
Fitting	10V	8.4%	14.9%	8.1%	13.0%	11.1%	3.4%	5.7%	5.4%	12.8%	6.8%
Val	10.5	8.3%	14.2%	10.0%	13.9%	11.3%	3.5%	5.8%	5.3%	13.0%	6.9%
Fitting	20V	5.1%	4.9%	4.0%	9.0%	5.7%	2.8%	9.1%	5.0%	13.1%	7.5%
Val	20.5	4.8%	4.6%	3.9%	9.3%	5.7%	3.0%	9.5%	5.7%	13.6%	7.9%
Fitting	30V	4.3%	6.2%	5.0%	12.8%	7.1%	2.6%	10.6%	7.0%	19.7%	10.0%
Val	30.5	3.6%	6.5%	5.0%	13.4%	7.1%	2.8%	11.0%	7.9%	20.9%	10.6%
Fitting	40V	3.3%	6.2%	4.8%	14.7%	7.3%	2.7%	11.9%	9.5%	31.1%	13.8%
Val	40.5	3.6%	6.4%	4.7%	15.1%	7.4%	2.7%	11.3%	9.4%	31.6%	13.7%

In summary, the GaN HEMT model constructed in the last chapter is validated against device measurement in this section. Validation with independent measurements proves that the drain current, gate current and S-parameter with respected to biasing are accurately modelled by the proposed physics based Virtual Source compact model.

Chapter 5
Conclusions and Future Work

5.1 Conclusions

A physics based Virtual Source compact model for GaN HEMTs has been proposed to accurately model the DC and RF behaviors. The proposed GaN HEMT model is partitioned into three modules based on the physical layout of the device – the GSG pad model, the parasitic model and the intrinsic model. This physics based partition scheme is valid and efficient for modeling the device behavior on the top-most level.

The GSG pads are modeled by a pure capacitive network due to their layout while the transistor parasitics are modeled by a pair of serial resistor and inductor for each terminal and a spatial coupling capacitor between each terminal. Separate measurement for GSG pads and pad capacitor extraction have shown that the proposed pads model is able to model the behavior of the pads. The parasitic elements are extracted by S-parameter fitting after the DC model of the device has been constructed. The extracted elements correctly represent the physical behaviors of the parasitics.

The intrinsic drain current is physically modeled based on the Virtual Source model theory proposed at MIT. Virtual Source model parameters are determined by optimizing model output to measurement data. The proposed optimization method that optimizes above-threshold current parameters and subthreshold current parameters separately is demonstrated to be efficient to reduce optimization space and obtain reliable parameters. The intrinsic gate current is modeled by a Schottky diode with forward and reverse current. Fitting results show that the both drain and gate current with dependence on V_{GS} and V_{DS} are accurately predicted by the proposed model.

Besides, a complete model parameter extraction workflow is demonstrated by constructing actual models for two GaN HEMTs from device measurement. A novel gate current based resistive parameter estimation technique is proposed for extracting the parasitic source and drain resistance and channel resistance. This technique uses only DC gate current to determine the resistive elements, which avoids the inaccuracy and uncertainties due to the interference of different types of parasitic elements as happened in conventional methods such as the cold-FET method. This method also eliminates the effort of fabricating the TRL structure for measuring active region sheet resistance, which is used in MIT Virtual Source model parameter extraction.

At the end, the constructed model is validated with independent measurement dataset in terms of drain current, gate current and S-parameter targeting future RF circuit design. Reasonable accuracy is reported for both DC (gate current and drain current) and S-parameter characteristics using the same set of extracted parameters.

Compared to the empirical compact models, such as Angelov model, EEHEMT model and DynaFET model, the proposed physics-based Virtual Source compact model clearly describes the behavior of the device based on the drift-diffusive transport theory with a significant smaller amount of physical parameters. It is computational efficient and easy to implement in circuit simulator. The model is scalable with dimension, biasing and temperature. However, due to the device process limitation and measurement set up, the scalability of the model cannot be validated with all the dimensions. This serves as part of the future work described in next section.

5.2 Future Work

Several works are worth further investigation at the conclusion of this project. These works can be divided into three aspects – improving the accuracy of the model, validating model's capability and adding new features to the model.

A. Improving the Accuracy of the Model

The model introduced in this thesis didn't use pulse-IV measurement to avoid the thermal effect in drain current due to the large measurement error of pulsed measurement and the capability of thermal modeling in the intrinsic Virtual Source model. However, with the development of instrumentation, future high resolution pulse-IV measurement is more valuable and preferred for GaN HEMT modeling. Pulse-IV measurement is able to isolate thermal effect, and therefore the current model and thermal model can be characterized separately to avoid error propagation. Furthermore, by separating thermal effect, more complicated (such as layout dependent) thermal networks can be implemented and calibrated to model the dynamic thermal behavior of the transistor.

Although the overall I-V fitting of the transistor is satisfactory, there is still noticeable divergence between the fitted curves and measurement data in triode region. This issue is neglected at the moment due to the reason that for power amplifier design, the load line seldom goes into the triode region. To provide a more accurate model not just for power amplifier design, the specific device operating principles and corresponding modeling method need investigation in the future.

For the S-parameter, model S_{22} correctly captures the trend of S_{22} from measurement, but the amplitude does not exactly matches each other. The amplitude difference represents the difference in output resistance of the model and the measurement. To provide a more accurate prediction of the output characteristics, this issue needs further investigation.

B. Validating Model's Capability

The model is inherently scalable with geometry, biasing and other physical dimensions. These scalabilities have not been validated in our work so far due to the limitation of device samples, process and measurement setup. For the future, devices with different gate length and access region length should be fabricated and measured for validating the scalability on device geometry. Moreover, high voltage (> 40 V) measurement setup and thermal chuck can be utilized for validating the scalability on biasing and temperature.

C. Adding New Features to the Model

With the advancement of GaN process technology, the trapping effect exhibited in modern GaN devices is much less serious than in devices several years ago. In the DC-IV measurement performed for this study, only trivial trapping effect is observed. Apart from trapping effect, the noise and breakdown in the device weren't considered in our model either. However, it is reasonable to integrate trapping modeling, noise modeling and breakdown modeling in the future, in order to provide a complete model framework that is suitable for modeling devices of different generations and manufactures, of different applications (such as power amplifier design or low noise amplifier (LNA) design) and of different operating conditions (under normal condition or operate beyond breakdown limitation).

Although the proposed compact model is able to be constructed from DC-IV and small signal S-parameter measurement, advanced large signal measurements, such as load-pull and intermodulation measurement, are worth to be performed to validate the large signal accuracy of the model in the future. Moreover, using I-V characteristics measured from RF excitation (RF-IV) to characterize device model is an emerging trend for the future.

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