# Design of Low Voltage Unsaturated Ring Oscillator for a Sigma Delta Time to Digital Converter

by

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**Abstract**

This thesis investigates the phase noise of two different 2-stage cross-coupled pair unsaturated ring oscillators with no tail current source. One oscillator consists of top cross-coupled pair delay cells, and the other consists of top cross-coupled pair and bottom cross-coupled pair delay cells. Under a low supply voltage restriction, a phase noise model is developed and applied to both ring oscillators. Both top cross-coupled pair and top and bottom cross-coupled pair oscillators are fabricated with 0.13 $\mu m$ CMOS technology. Phase noise measurements of -92 dBc/Hz and -89 dBc/Hz ,respectively, at 1 MHz offset is obtained from the chip, which agree with theory and simulations. Top cross-coupled ring oscillator, with phase noise of -92 dBc/Hz at 1 MHz offset, is implemented in a second order sigma-delta time to digital converter. System level and transistor level functional simulation and timing jitter simulation are obtained.

## Acknowledgements

First, I would like to express my gratitude to my supervisor Professor Bosco Leung. Without his guidance, dedication, patience, and knowledge, this would not be possible. I would like to thank Yon Chiet Ng, for his help and support over the last couple of terms. Many thanks to Phil Regier for his help on computer problems and CMC support.

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# Chapter 1

# Introduction

## 1.1 Research Objective

With the large growth of mobile communications, sensors, there is an increasing need for cost reduction, power reduction and efficiency improvement of these systems. Since, analog to digital converter (ADC) is an essential block used in any mixed analog/digital system, it is necessary to improve its performance. However as technology scales, supply voltages reduces, ADCs becomes increasingly difficult to design due to lower voltage swings [2]. Time to digital converters (TDCs) do not suffer from such voltage supply reduction problems.

This thesis covers the design of a voltage controlled (ring) oscillator, VCO, based sigma delta TDC. A fundamental performance limiting factor in such TDC is the accumulative clock jitter from the VCO [3]. Ring oscillators suffers from poor phase noise performance and hence limits the overall performance of the TDC. This short coming can be reduced by utilizing efficient VCO architecture and optimizing its design parameters.

The aim of this research is to improve the performance of a ring oscillator based TDC by improving the performance of the ring oscillator in terms of speed, frequency of operation, and phase noise.

## 1.2   Thesis Organization

The thesis is organized as follows.

Chapter 2 presents the basic background information on ring oscillators. Different ring oscillators are compared with the ring oscillators covered in this thesis.

Chapter 3 provides background information on phase noise. It will also examine some known phase noise models and proceeds to provide a phase noise model on the oscillator covered in this thesis.

Chapter 4 provides numerical calculation using phase model developed in chapter 3. Comparison is made between numerical calculations, simulations and chip measurements of phase noise.

In chapter 5, time to digital converter (TDC) is introduced. This section includes a detailed implementation of TDC using top cross-coupled pair ring oscillator covered in previous sections. System level and transistor level simulations of TDC are performed.

Conclusion is provided in chapter 6 with future work also presented in this section.

# Chapter 2

# Oscillator

## 2.1  Introduction

With the large growth of mobile communications, ring oscillators are useful RF components in frequency synthesizers. They are also frequently used as building blocks in phase-locked loops and time to digital converters, for its ease of implementation and wide tuning range. This chapter will discuss the design methodology to enhance the phase noise of two differential cross coupled pair oscillator. First, this chapter will begin with comparison between the differences between these two oscillator topology and various other topologies covered by other papers and journals. The next section will focus on the operation and design of these oscillators.

## 2.2 Ring Oscillator Basics

A ring oscillator consists of a series of delay cells stages with a simple feedback circuit. In general there are two types of ring oscillator: single ended and differential. Since a ring oscillator is essentially a circuit with a feedback loop, in order to oscillate, the Barkhausen criteria is to be met. The two criteria for oscillation include:

1) the magnitude of loop gain is equal to unity

2) the phase shift of the feedback loop must be zero or an integer multiple of $2\pi$.
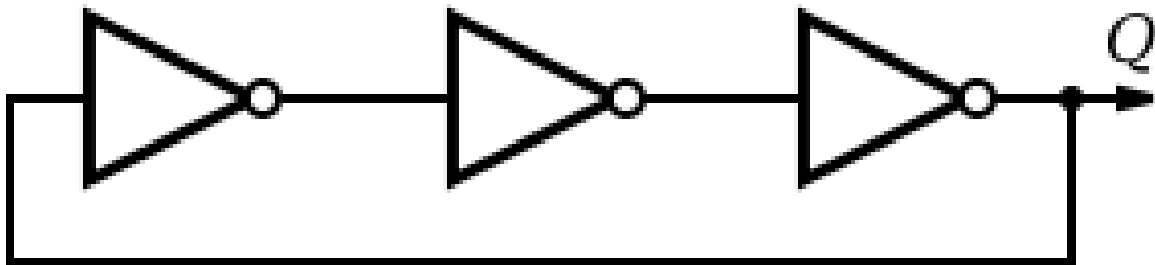


Figure 2.1: 3 stage ring oscillator

Figure 2.1 is an example of a 3-stage single ended ring oscillator, each stage provides a gain greater or equal to one and offers a phase shift of 180°. Hence, in order to satisfy the second Barkhansen criteria, an odd number of stages is required for single ended ring oscillators. However, in the case of differential ring oscillator, we can 'criss-cross' the output such that an odd number of stages is not required to meet the second criteria as illustrated in Figure 2.2b.
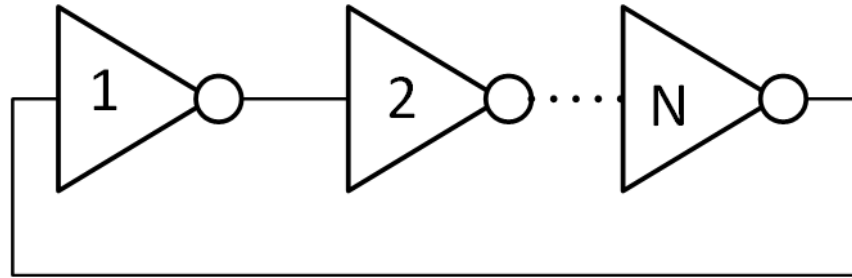
(a) Single Ended N-stages Ring Oscillator where N is odd
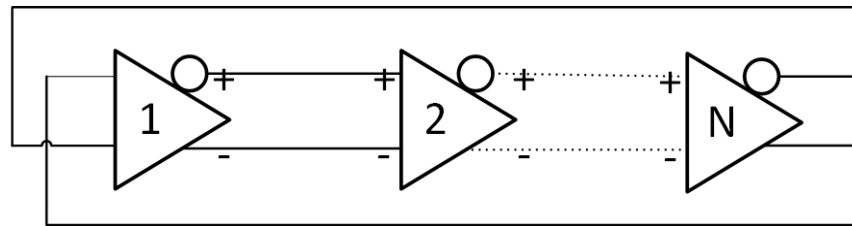


(b) Differential ended N-stages ring oscillator

Figure 2.2: Single ended and differential ended ring oscillators

The oscillation frequency of a ring oscillator is defined by the number of delay stages. Each delay stage, which also refers to as delay cells, generates a certain delay. Using this delay cell we can calculate the frequency of oscillation ($f_{osc}$), which is defined in equation 2.1.

$$f_{osc} = \frac{1}{2Nt_d} \tag{2.1}$$

where $N$ is the number of stages and $t_d$ is the delay generated by each stage of the oscillator.

The delay of each stage, $t_d$, can be approximated by its $RC$ time-constant. This is approximated by equation 2.2

$$t_d = RCln(2) \tag{2.2}$$

This equation is based on the assumption that, $(i)$, each delay cell is identical to one another and $(ii)$, the following stage switches once the previous stage crosses the midpoint shown in Figure 2.3.
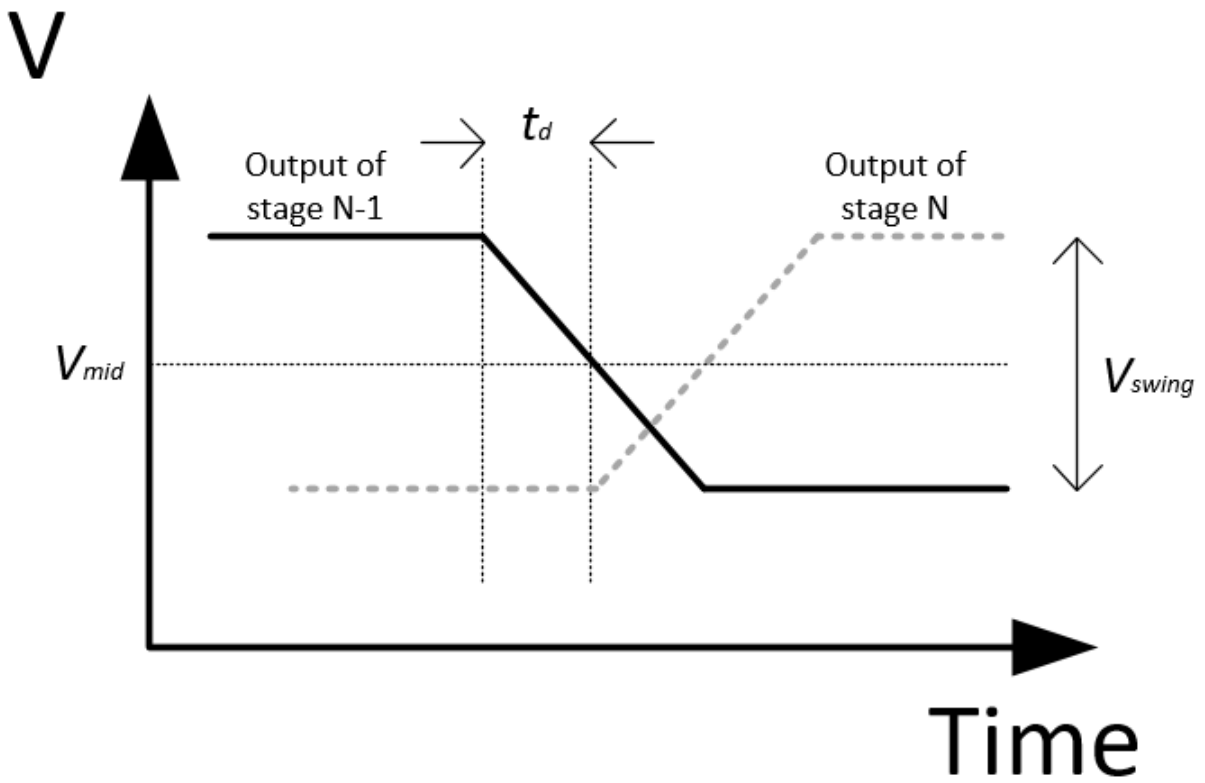


Figure 2.3: Approximated $t_d$ of single ended ring oscillator

## 2.3   Other Delay Cell Designs

In this section ring oscillators with different delay cell topologies are analyzed. Differential oscillators, such as ones in [4], [5] (Figure 2.4a) use designs involving source coupled pair. These designs require tail current source. Due to stacking of the transistors, these oscillators require higher power supply voltage than those without a tail current source. As technology scales down, supply voltage reduces, making ring oscillator design such as [6, 7, 8] an attractive alternative (Figure 2.4b).

Delay cell of [6] avoids the implementation of source coupled pair and uses two CMOS inverters in a feed-forward manner for differential operation (Figure 2.4b left). This avoids tail current source and can operate at lower supply voltage. [7] uses PMOS-controlled current-starved CMOS inverters in a direct path and four basic CMOS inverters in a feedforward path (Figure 2.4b right). [8] uses a pseudo-differential inverter to achieve differential operation without tail current source. In addition, [5] differs from [6, 7, 8], in that it has only 2-stage (requiring less hardware), whereas [6, 7, 8], use 4 or more stages. Compared to [6, 7, 8], this reduction of stages cause [5] to perform as an unsaturated ring oscillator, meaning the output of the oscillator never reach the supply voltage $V_{DD}$. From equation 2.1, reduction in stages offers higher frequency of oscillation. Moreover, lowering the number of delay cells also reduce the size of the oscillator, saving hardware and area. We can further improve the design by removing the tail current source, allowing for lower supply operations( i.e. [9] is an example of a cross-couple pair without tail current source operating at 0.9-1V supply). These improvements are implemented in the two stage cross-coupled pair ring oscillators covered in this thesis (Figure 2.5).
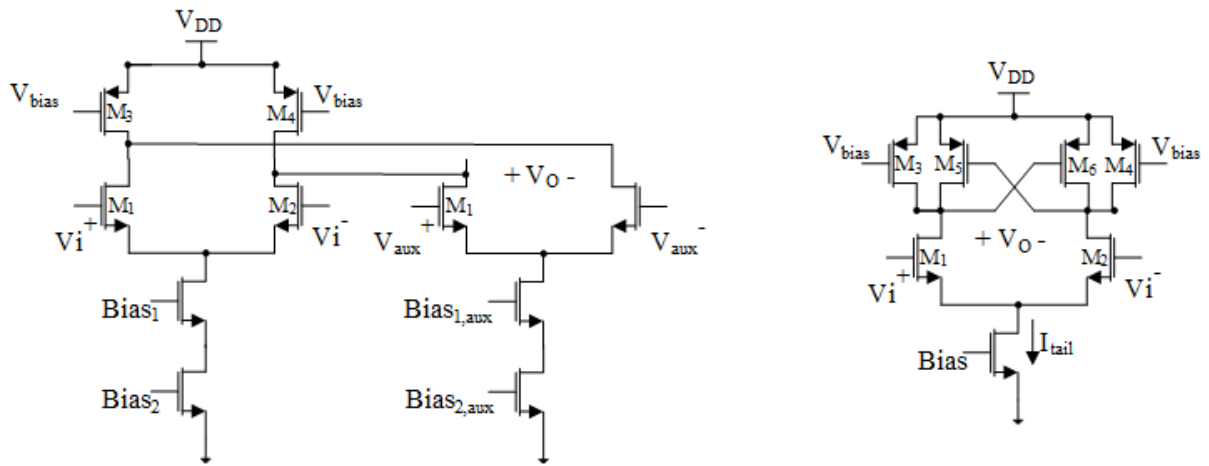
(a) Source coupled delay cells with tail current source from [4] and [5] respectively
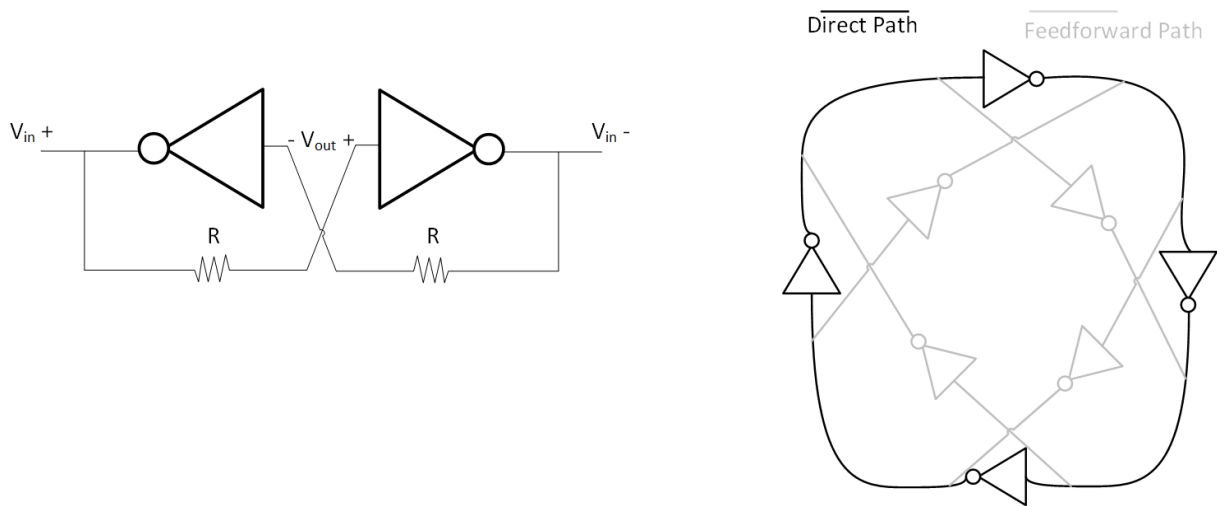


(b) Delay cells and ring oscillator architecture without use of current source from [6] and [7] respectively

Figure 2.4: Various other delay cell and ring oscillator architecture

## 2.4 Cross-Coupled Pair Differential 2-Stage Ring Oscillator Without Tail Current Source
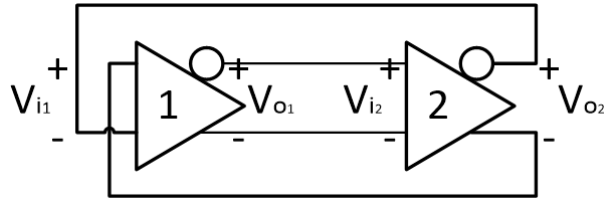


(a) 2 Stage Ring oscillator
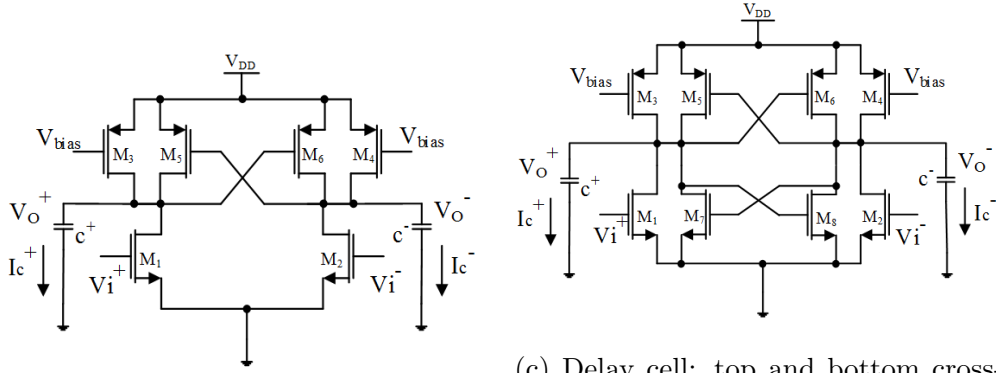


(b) Delay cell: top cross-coupled pair



(c) Delay cell: top and bottom cross-coupled pair

Figure 2.5: 2-stage oscillator design, and delay cell topologies

Figure 2.5a shows the block diagram of a two-stage ring oscillator. Two oscillators are implemented, using delay cells with topologies in Figure 2.5b and Figure 2.5c. Both delay cells consist of the same driver (M1-M2), and the same resistive (M3-M4 biased in triode) part of the load. Meanwhile, in the load, Figure 2.5b has, in addition, a top cross-coupled pair i.e. transistor M5/M6 (hence denoted as top cross-coupled pair oscillator), while Figure 2.5c, has both a top and a bottom cross-coupled pair i.e. transistors M5/M6 and M7/M8 (hence denoted as top and bottom cross-coupled pair oscillator)[8]. Similar

to [5], due to its low number of stages (2 stage), the oscillator is unsaturated.

We focus the analysis on the more complicated delay cell in Figure 2.5c, as it carries over to Figure 2.5b. The load capacitance $C+$ of Figure 2.5c, which comes from the gate and other parasitics of the following stage, determines the delay and the oscillation frequency of the cell. M3, M4 are the load. M5, M6 and M7, M8 are the cross-coupled pairs that enhance charging and discharging. During charging, M1 is off and M2 is on, M3 provides the charging current to $C+$. M5, M6 provides extra charging current via positive feedback action and enhances the slew rate of $C+$ ramping up. Unlike [6], with the extra cross coupled pair M7-8, it provides extra current during discharge and enhances the negative slew rate. Thus during discharging of $C+$, M1 is on and M2 is off so that M1 overcomes M3 and provides discharging current to $C+$. M7, M8 provides extra discharging current via positive feedback action and enhances the slew rate of $C+$ ramping down. This help symmetrizes the slew rate in both directions.

In summary, the cross-coupled pair presents a negative resistance (basically $-1/g_m$) that tends to cancel out the positive resistance from the resistive (triode; basically $g_{ds}$) load. This affects the phase shift of the delay cell. The 2-stage oscillator, in a manner akin to that in [5], is designed so that this phase shift is enough to sustain oscillation. Then $V_{bias}$, which controls $g_{ds}$, is used to change oscillation frequency and can be considered as tuning the voltage controlled oscillator VCO [8].

Compared to previous ring oscillator designs, the two cross-coupled pair oscillator designs in this thesis offer two advantages.

1) By reducing the number of stages, we allow for faster speed (frequency of oscillation) and less hardware, making it more cost efficient.

2) ring oscillator with delay cell without tail current source allows for a larger output

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range, since there is more headroom. This allows for low supply design.

However the disadvantage of unsaturated oscillator is that if has more phase noise due to cycle to cycle correlation [5].

# Chapter 3

# Oscillator Phase noise

## 3.1  Introduction

An important metric for oscillators is phase noise. It is very difficult to design a simple, intuitive and accurate phase model for ring oscillators. In this section, some phase noise models are introduced. A phase noise model for the cross-coupled pair oscillators without tail current source is presented.

## 3.2  Phase Noise Basics

Phase noise is the frequency domain measurement of noise in an oscillator. It is defined as the ratio of the side-band power at an offset frequency across a 1 Hz span over the total power of the carrier signal. A typical frequency domain plot of an ideal and actual oscillator is shown in Figure 3.1. The effect of frequency instability creates a 'skirt' around the carrier frequency, $f_{osc}$.
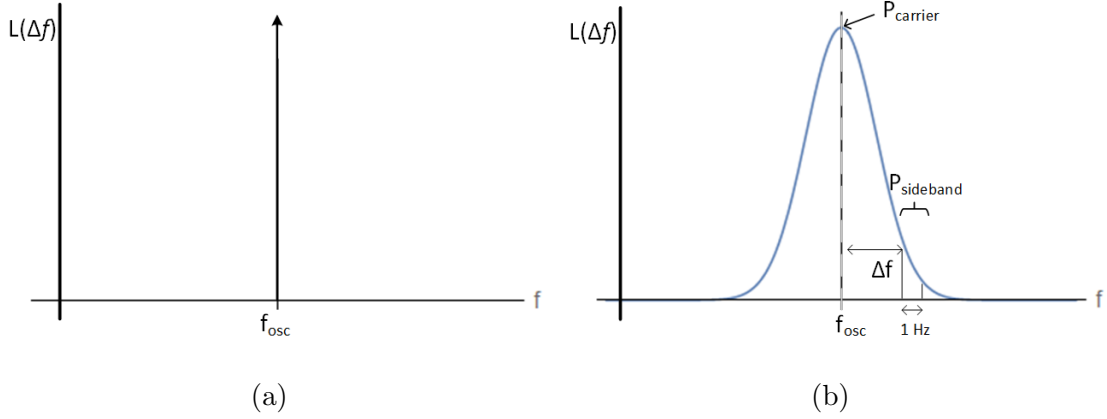
Figure 3.1: Frequency spectrum of a) ideal oscillator b) actual oscillator

In general, phase noise (measured in $dBc/Hz$) has been shown to have Lorentzian spectrum as describe in equation 3.1 [10].

$$L(\Delta f) = 10log(\frac{1}{\pi}\frac{\pi f_{osc}^2 c}{(\pi f_{osc}^2 c)^2 + \Delta f^2}) \qquad (3.1)$$

where $f_{osc}$ is the oscillation frequency and c is a scalar constant that describes the phase noise in an oscillator. For $\Delta f \gg \pi f_{osc}^2 c$, equation 3.1 can be simplified as equation 3.2.

$$L(\Delta f) = 10log(\frac{1}{\pi}\frac{\pi f_{osc}^2 c}{\Delta f^2}) \qquad (3.2)$$

In relation to cycle-to-cycle jitter, time domain measurement of noise in an oscillator, $\sigma_c^2$ phase noise is defined by equation 3.3

$$L(\Delta f) = 10log(\frac{1}{\pi}\frac{\sigma_c^2 f_{osc}^3}{\Delta f^2}) \qquad (3.3)$$

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## 3.3   Phase Noise Model

Three phase noise models are discussed in this section starting with Razavi's phase noise model [11], followed by phase noise model proposed by Hajimiri [12] and finally phase noise model proposed by Leung [5].

### 3.3.1   Razavi's Phase Noise Model

Razavi's phase noise model introduces an equivalent open loop Q factor for ring oscillator which measures how much the closed loop system oppose the variation in frequency[11]. This Q factor is defined in equation 3.4.

$$Q = \frac{f_{osc}}{2}\sqrt{(\frac{dA}{df})^2 + (\frac{d\phi}{df})^2} \tag{3.4}$$

where $A(\omega)$ and $\phi(\omega)$ is the amplitude and phase of the open loop transfer function.

The phase noise from Razavi's model is defined as 3.6.

$$L(\Delta f) = 10(\frac{2NFkT}{P_s}\frac{1}{4Q}(\frac{f_{osc}}{\Delta f})^2) \tag{3.5}$$

where $N$ is the number of stages in ring oscillation, $F$ is the excess noise factor, $k$ is the Boltzmann's constant, and $P_s$ is the average power dissipation within one cycle. Razavi's model is applicable to both LC oscillator and single-ended ring oscillator. However, issues occurred when applying this model to differential ring oscillators, as it does not account for transistors that turns off during part of the period[11]. Furthermore, Razavi also briefly discuss additive, high frequency multiplicative and low frequency multiplicative noise. These account for non-linear effects not considered in the model.

### 3.3.2 Hajimiri's Phase Noise Model

The phase noise model proposed by Hajimiri introduces the impulse sensitive function (ISF), $\Gamma(f_{osc}\tau)$ to characterize the time varying effects in ring oscillator [12]. As illustrated in Figure 3.2, the amount of phase fluctuation depends on the time that the impulse current noise is injected. This impulse noise source is captured by the ISF over one period. Phase noise in Hajimir's model is defined as:

$$L(\Delta f) = 10\Big(\frac{\Gamma_{rms}^2}{q_{max}^2}\frac{\overline{i_n^2}/\Delta f}{2(2\pi)^2}\Big) \tag{3.6}$$

given the periodic nature of ISF, 3.6 is expanded to:

$$L(\Delta f) = 10\Big(\frac{C_o^2}{q_{max}^2}\frac{\overline{i_n^2}/\Delta f}{2(2\pi)^2}\Big(\frac{f_{1/f}}{\Delta f}\Big)\Big) \tag{3.7}$$

where $\overline{i_n^2}/\Delta f$ is the current noise power spectral density, $f_{1/f}$ is the corner frequency of the device $1/f$ noise,. $c_o$ is the DC component of the ISF, and $q_{max}$ is the maximum amount of charge at the output node defined by equation 3.8.

$$q_{max} = C_{node}\cdot V_{swing} \tag{3.8}$$

Hajimiri's model shows that we can minimize the 1/f noise by reducing $c_o$ or equivalently by designing an oscillator with symmetrical rise and fall waveform. In conclusion, the model shows good agreement between simulated and measured results. However, the drawback with this model is the lack of design insight regarding trade-offs between circuit parameters and phase noise.
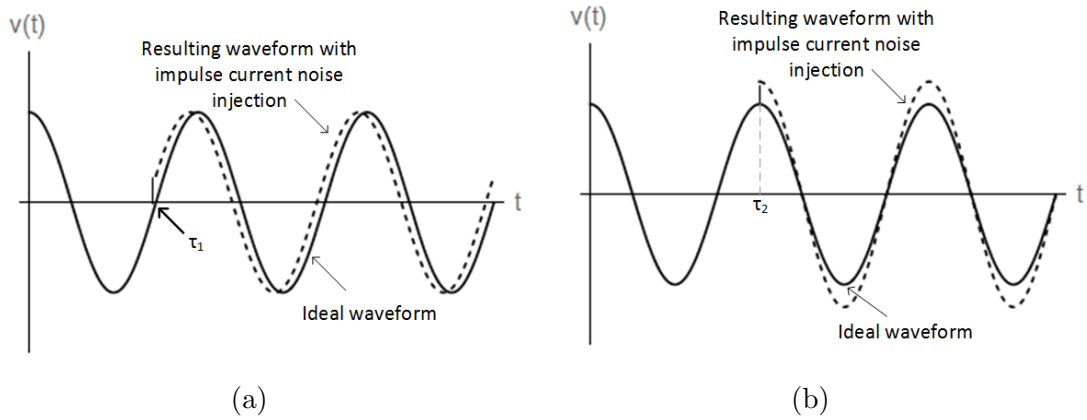
Figure 3.2: Effects of impulse current noise on oscillator waveform injected at $\tau_1$ and $\tau_2$

### 3.3.3 Leung's Phase Noise Model

Unlike Razavi, Leung's model focuses on differential ring oscillators with cross coupled pairs. The phase noise model proposed by Leung characterizes the effect of circuit parameter on phase noise. The analysis of this model is based on the dominant thermal noise and its cycle-to-cycle correlation [5], in unsaturated ring oscillators. The mathematical model, based on cross-coupled paired ring oscillator with current source offers valuable design insights on trade-offs between circuit parameters and phase noise. This model can be applied to cross-coupled pair ring oscillator without a current source for low supply application. Due to low supply, approximations can be made to further simplify and offer clearer design insight which are summarized in the next section. This model and its simplification is explained in the next section.

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## 3.4 Differential 2-Stage Cross-coupled Low Voltage (Supply) Unsaturated Ring Oscillator Phase Noise Model

As stated, Leung's phase noise models is based on cycle-to-cycle correlation of an unsaturated oscillator. This correlation is largely dependant on the circuit characteristics, which is dependent on circuit parameters (e.g. $W/L$) and operating conditions (e.g. $V_{bias}$).

Figure 3.4 is the output of a cross-coupled pair oscillator with no tail current source. As it is unsaturated and similar to [5], cycle to cycle correlation dominates the phase noise. Like [5], to derive an accurate phase model we must

1) investigate the circuit parameter and operating conditions on the delay cell circuit's characteristics.

2) obtain a phase model dependant on cycle to cycle correlation based on the delay cell circuit characteristics.

Since frequency of VCO is tuned by changing the circuit parameter $V_{bias}$, which incidentally also affects the delay cell characteristics and hence phase noise. The dependency of $V_{bias}$ will receive particular attention.

### 3.4.1 Investigation of Circuit Parameter and Operating Conditions on Delay Cell Circuit's Characteristics

We begin by looking at the first stage of a top only cross coupled ring oscillator with its delay cell once again shown in Figure 3.3a. The output $V_o^+$ and input $V_i^+$ of the first

stage is simulated in Figure 3.4. Since there are only 2 stages, there are 4 quadrants in 1 period as shown by Q1, Q2, Q3, and Q4 in Figure 3.4[5]. We perform analysis on the first quadrant Q1 as shown in Figure 3.4.



(a)                                                                 (b)
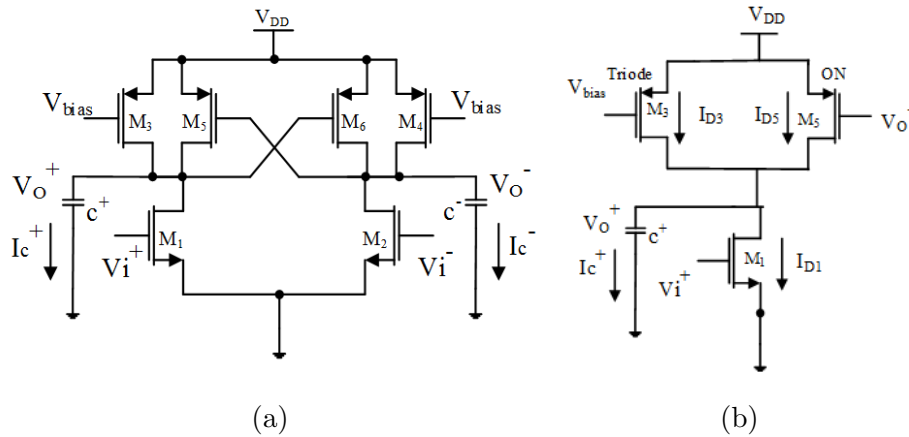
Figure 3.3: a) Top only cross couple pair delay cell. b) Half circuit of top only cross couple pair delay cell
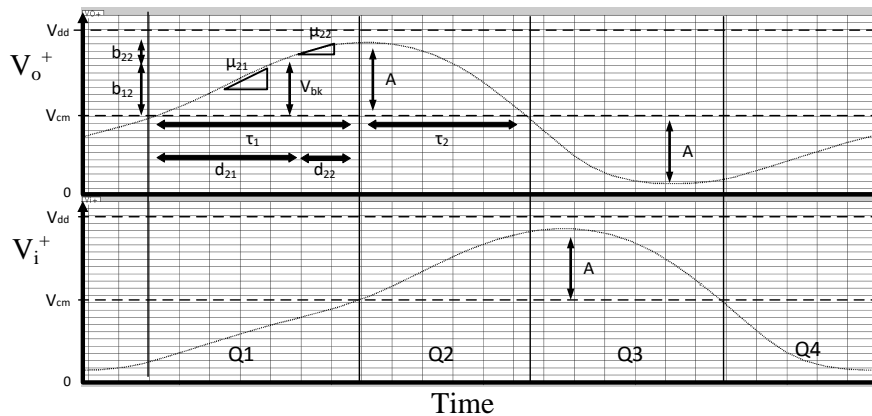


Figure 3.4: Transient output of $1st$ stage top cross-coupled pair oscillator.

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## Half Circuit

We start with the left-hand half circuit (M1, M3, and M5) of the delay cell Figure 3.3b and look at the current $I_c^+$. Initially, $V_i+$ rises but is below the threshold[1]. M1 conducts no current ($I_{D1} = 0$). When $V_i+$ reaches the threshold $V_{cm}$ (the common mode voltage) (moving into Q2), M1 is on. If we look at drain of M1 of Figure 3.3b, we have

$$C\frac{dV_o^+}{dt} = I_c^+ = \overbrace{(I_{D3} + I_{D5})}^{I_{load}} - \overbrace{(I_{D1})}^{I_{driver}} \tag{3.9}$$

Where $I_{D3} + I_{D5}$ $I_{load}$ and $I_{D1}$ is $I_{driver}$.

Using long channel approximation for simplicity, and assuming $V_{gs1}$ stays constant at $V_{cm}$:

$$I_{driver} = I_{D1} = \frac{1}{2}k_n\left(\frac{W_1}{L_1}\right)(V_{gs1} - V_{tn})^2 = \frac{1}{2}k_n\left(\frac{W_1}{L_1}\right)(V_{cm} - V_{tn})^2 = I_{D_{ON}} \tag{3.10}$$

i.e. $I_{driver}$ is the constant current $I_{D_{ON}}$

Turning to the load, since it is independent of whether the tail current source is present or not, we can follow [5] and the impedance (given in Table II of [5]) is repeated here for Q1 of Figure 3.4 at the drain of M1. Depending on whether M5 is ON this quadrant 1 has two durations $d_{21}$ and $d_{22}$ as summarized below:

---

[1]To be precise threshold is $V_t$. To simplify the discussion, we adopt the common mode voltage ($V_{cm}$) as the threshold

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Table 3.1: Impedance at node 2 when delay cell is in quadrant 1

|  | M1 | M2 | M6 | M5 | Impedance at Drain of M1 |
|---|---|---|---|---|---|
| at $d_{21}$ | off | Triode | on | Sat | $-1/(g_{m_5} - g_{ds_3})$ |
| at $d_{22}$ | off | Triode | on | Off | $1/g_{ds_3}$ |

Here $g_{ds3}$ is the conductance of M3 (in triode), $g_{m5}$ is the transconductance of M5 (in saturation).

Using the load impedance expression in Table 3.1 we express small signal variation of load current $I_{load}$: $I_{D3}$, $I_{D5}$ from their bias or common mode value (i.e. $I_{D3_{cm}}$, $I_{D5_{cm}}$) in terms of small signal variation of output voltage $V_o^+$:

$$(I_{D3} - I_{D3_{cm}}) + (I_{D5} - I_{D5_{cm}}) = (V_o^+ - V_{cm})(g_{m5} - g_{ds3}) \quad V_{cm} \le V_o^+ \le V_{cm} + V_{bk}$$

$$(I_{D3} - I_{D3_{cm}}) + (I_{D5} - I_{D5_{cm}}) = (V_o^+ - V_{cm})(-g_{ds3}) \qquad V_{cm} + V_{bk} \le V_o^+ \le A \quad (3.11)$$

A is the amplitude of oscillation. $V_{bk}$ (or more precisely $V_{bk} + V_{cm}$) is the breakpoint voltage, where M5-M6 turns on. This is also shown in Figure 3.4. Other symbols in Figure 3.4 ($\tau_1, \tau_2, b_{21}, b_{22}, \mu_{21}, \mu_{22}$) are explained in the next section, section 3.4.2, and appendix A. To complete our determination of the circuit characteristics dependency on circuit parameters, we now derive the explicit dependency of $V_{cm}$, $V_{bk}$ on circuit parameters, followed by I-V characteristic of the load. The expression for $A$ will be presented at the end of section 3.4.2 using derived load characteristics.

### $V_{cm}$, common mode voltage:

Because $V_{o2}$ is fedback to $V_{i1}$ in Figure 2.5, the common mode for input and output of delay cell are the same, and both are denoted as $V_{cm}$. Common mode voltage is obtained

when $V_o^+ = V_o^-(= V_{cm})$. To determine $V_{cm}$, let us go back to equation 3.9 and set $I_c^+ = 0$, and have $I_{D3}$, $I_{D5}$, $I_{D1}$ replaced by their common mode values: $I_{D1_{cm}} = I_{D3_{cm}} + I_{D5_{cm}}$. Again, like equation 3.10 we use long channel approximation and we have

$$
\begin{aligned}
\frac{1}{2}k_n\frac{W_1}{L_1}(V_{cm} - V_{tn})^2 &= \frac{1}{2}k_p\frac{W_3}{L_3}(V_{DD} - V_{cm})(2(V_{DD} - V_{bias} - |V_{tp}|) \\
&\quad - (V_{DD} - V_{cm})) + \frac{1}{2}k_p\frac{W_5}{L_5}(V_{DD} - V_{cm} - |V_{tp}|)^2
\end{aligned}
\tag{3.12}
$$

Assuming the delay cell is designed such that $k_n(\frac{W}{L})_1 = k_p(\frac{W}{L})_5 = k(\frac{W}{L})$, equation 3.12 is simplified[2] and $V_{cm}$ is:

$$
V_{cm} = \frac{V_{DD}}{2}\left(1 + \frac{(V_{DD} - V_{bias} - V_t)k_p(\frac{W_3}{L_3})}{(V_{DD} - 2V_t)k(\frac{W}{L}) + (V_{DD} - V_{bias} - V_t)k_p(\frac{W_3}{L_3})}\right)
\tag{3.13}
$$

This is simpler than solving $V_{cm}$ in [5], where the tail current complicates matter and involves solving a full quadratic equation ([5]'s model is shown in its long Table IV). Thus it can be seen an increase in $V_{bias}$ or $(W/L)$ causes a decrease of $V_{cm}$, while increasing $(W/L)_3$ increase $V_{cm}$.

### $V_{bk}$, breakpoint:

$V_{bk}$ is the breakpoint in the output voltage, which physically defines when M5 (in Figure 3.3b) turns on. This occurs when $V_o^+$ is at $V_{DD} - |V_{tp}|$. In differential form, $V_{bk} = 2(V_{DD} - |V_{tp}| - V_{cm})$ and substituting equation 3.13, $V_{bk}$ is:

---

[2]we assume there is symmetry between the cross-coupled pair part of the load and the driver i.e. PMOS device (M5) have equal strength as the NMOS (M1). Also we assume that $(V_{DD} - V_{cm})$ is small and its squared term even smaller, so that the square term in equation 3.12 can be neglected

$$V_{bk} = 2\left((V_{DD} - |V_{tp}|) - \left(\frac{V_{DD}}{2}\left(1 + \frac{(V_{DD} - V_{bias} - V_t)k_p(\frac{W_3}{L_3})}{(V_{DD} - 2V_t)k(\frac{W}{L}) + (V_{DD} - V_{bias} - V_t)k_p(\frac{W_3}{L_3})}\right)\right)\right)$$

(3.14)

This is again simpler than the $V_{bk}$ equation derived in [5]. With equation 3.14, it can be seen, increase in $V_{bias}$ (i.e. a decrease of $V_{cm}$, shown above), leads to increase in $V_{bk}$. Furthermore, when $(W/L)$ increases, $V_{cm}$ decreases and $V_{bk}$ increases. $A$ is the amplitude of oscillation. [3]

## Full Circuit

Next, let us analyze the total circuit (both side of half circuit)

**I-V characteristics of driver:**

The differential driver current is determined by applying equation 3.10. It becomes $I_{D1} - I_{D2} = I_{D_{ON}}sgn(V_i)$ and upon normalization i.e. by dividing $I_{D_{ON}}$,

$$I_{D1_{norm}} - I_{D2_{norm}} = sgn(V_i)$$

(3.15)

$I_{D1_{norm}}$ and $I_{D2_{norm}}$ are the normalized currents of $I_{D1}$ and $I_{D2}$. $sgn$ is the sign function and so the differential $I_{driver}$ is a piecewise constant function of $V_i$, the differential input voltage.

---

[3] $A$ can be found through simulation. Typically, $A$ is found to be 1.2 to 2 times of $V_{bk}$

**I-V characteristics of load:** $S_s$ **(side slope), and** $S_c$ **(center slope)**

The differential load current $I_{D3} + I_{D5} - (I_{D4} + I_{D2})$ can similarily be calculated by applying equation 3.11 and then normalized. The right hand side (RHS) is in terms of differential output voltage $V_o = V_o^+ - V_o^-$. The current can then be written as piecewise linear function ($pwl$) of $V_o$ (i.e $I_{D3} - I_{D4} + I_{D5} - I_{D6} = pwl(V_o^+ - V_o^-) = pwl(V_o)$) as shown in Figure 3.5.
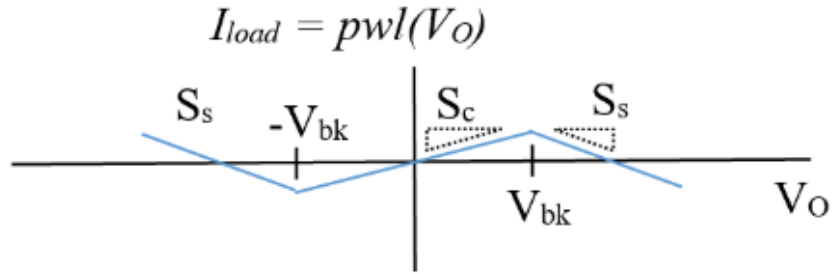


Figure 3.5: Differential output current shown as a piecewise linear function ($pwl$) of $V_o$ where $V_{bk}$, defined as the voltage when M5-M6 turn on/off, is the break point between $S_s$ and $S_c$.

In Figure 3.5, side slope ($S_s$) and center slope ($S_c$) are normalized slopes of the $pwl$ function and are:

$$S_s = -g_{ds3}/I_{D_{ON}} \tag{3.16}$$

$$S_C = (g_{m5} - g_{ds3})/I_{D_{ON}} \tag{3.17}$$

Notice in Figure 3.5 $S_c$ is positive so that the load gives sufficient phase shift to sustain oscillation in the 2-stage low voltage ring oscillator.

Combining the *pwl* expression of differential load current with the previous *sgn* expression of the differential driver current (shown in equation 3.15, equation 3.9 can be written in differential form. We then normalize by dividing C:

$$\left(\frac{1}{I_{D_{ON}}/C}\right)\frac{dV_o}{dt} = sgn(V_i) + pwl(V_o) \tag{3.18}$$

RHS is the delay cell characteristic for Figure 2.5b.

Repeating for circuit in Figure 2.5c, similar symmetry consideration in footnote 2 is adopted in the design, and delay cell characteristics remains the same except $S_c$ is:

$$S_C = (g_{m5} + g_{m7} - g_{ds3})/I_{D_{ON}} \tag{3.19}$$

With $S_s$ and $S_c$ derived for delay cell in this paper, they can be used in the generic amplitude expression, for unsaturated ring oscillator, presented in [5], to obtain oscillation amplitude, $A$:

$$A = V_{bk} - \frac{ScV_{bk}}{2S_c} - \frac{\sqrt{(2S_cV_{bk})^2 - 4((2S_cV_{bk})^2 - 1 + (1 - (S_cV_{bk})^2)^{(1-\frac{S_s}{S_c})})}}{2S_s} \tag{3.20}$$

Now that we defined the delay cell circuit characteristics in terms of $S_c$ and $S_s$, we can now derive the phase noise model.

## 3.4.2  Phase Noise Model Based on $S_s$ and $S_c$

Now we add noise component to our model. Since the output is unsaturated, there is cycle to cycle correlation. This can be demonstrated by adding noise in Figure 3.4 shown again as Figure 3.6 below:
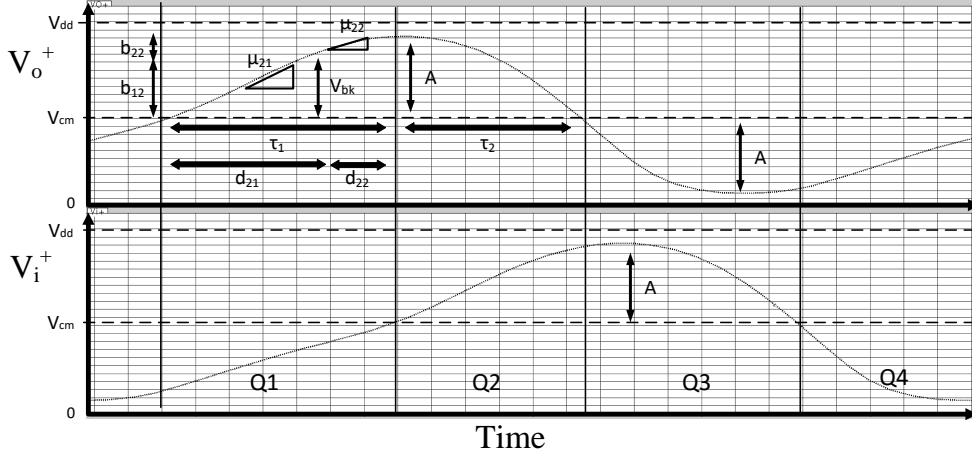
Figure 3.6: Transient output of $1st$ stage top cross-coupled pair oscillator.

Without noise, when $V_i^+$ ramps up and crosses $V_{cm}$ (between Q1 and Q2), $V_o^+$ switches around from ramping up to ramping down at $V_{cm} + A$, and when $V_o^+$ crosses $V_{cm}$ (between Q2 and Q3) $V_i^+$ changes from ramping up to ramping down at $V_{cm} + A$. However due to noise, between Q1 and Q2, $V_i^+$ ramps up and crosses $V_{cm}$ at a random time ($\tau_1$). This random crossing causes the switch around of $V_o^+$ not to be exactly at $V_{cm} + A$, but slightly above or below. This deviation in turn causes $V_o^+$ (now ramping down) to cross $V_{cm}$ at a random time ($\tau_1 + \tau_2$), with correlation to the original random crossing of $V_i^+$ across $V_{cm}$ (between Q1 and Q2) at $\tau_1$(it should be remembered that there is also noise injected on $V_o^+$, during ramping down, which is also responsible for this random crossing). Eventually the effect of this random crossing will propagate through the remaining quadrants and causes random crossing in the next cycle, resulting in cycle-to-cycle correlation. This is captured in correlation coefficient $\theta$, and noise $\sigma_\epsilon$ [5]. With linear approximation, $\sigma_\epsilon$ is simplified from [5] and approximation made in the derivation of $\theta$ is also made more accurate (see

appendix A):

$$\theta = \frac{-(S_s(\frac{A-V_bk}{2} - V_bk) + 1 + S_cV_bk)}{S_cV_bk - 1 + S_s(A - V_bk)} \tag{3.21}$$

$$\sigma_\epsilon^2 = \left( \frac{V_{bk}\sigma^2}{\left(S_s\left(\frac{A+V_{bk}}{2}\right) + S_cV_{bk} - 1\right)\frac{I_{D_{ON}}}{2C}\right)^3} + \frac{(A - V_{bk})\sigma^2}{\left((S_c\left(\frac{V_{bk}}{2}\right) - 1)\frac{I_{D_{ON}}}{2C}\right)^3} \right) \tag{3.22}$$

$\sigma$ is the noise component of $I_{load}$, $I_{driver}$ i.e. $\sigma = \sqrt{4kT[(2/3)(g_{m_1} + g_{m_5}) + g_{ds_3}]}/C$. $V_{bk}$ is given in equation 3.14. Similar calculation can be repeated for Figure 2.5c, where $\sigma$ has extra noise contribution from the lower cross-coupled pair:

$$\sigma = \frac{\sqrt{4kT[\frac{2}{3}(g_{m_1} + g_{m_5}) + g_{ds_3}]}}{C} \tag{3.23}$$

The $\theta$ and $\sigma_\epsilon$ expression is simpler than in Table IV of [5]. With $\theta$ and $\sigma_\epsilon$ , we can then determine the power spectral density function $psd$, where $f_o$ is the oscillation frequency:

$$psd\left(\frac{\omega_{offset}}{\omega_o}\right) = 10 \log \left( \frac{1 - r^2}{f_o(1 + r^2 - 2r \cos\left(\frac{\omega_{offset}}{\omega_o}\right))} \right) dBc/Hz \tag{3.24}$$

$$r = \exp\left( - \frac{4\sigma_\epsilon^2 f_o^2}{2(1 - \theta)^2} \right) \tag{3.25}$$

# Chapter 4

# Numerical Calculation, Simulations, and Measurement

In order to validate the accuracy of our phase model, phase noise calculation using our phase noise model and phase noise simulation are obtained. Design insights obtain from the phase noise model is then confirmed. Finally, on chip phase noise measurement is taken and is compared to simulation and calculated phase noise results.

## 4.1   Example Calculation and Simulation of Phase Noise

The new phase noise model is applied to an example using the design in Figure 2.5. For Figure 2.5b design parameters are: $V_{DD} = 1.2V$, $I_{D_{ON}} = 100uA$, $C = 20fF$, $V_{bias} = 0.5V$, $(W/L)_{1-2} = 1\mu m/0.12\mu m$, $(W/L)_{3-4}) = 2.5\mu m/0.12\mu m, (W/L)_{5-6} = 1\mu m/0.12\mu m$. Using these, $g_{ds}$, $g_m$ are obtained and substituting in equation 3.16 and 3.17:

$$S_s = -0.8 \qquad S_c = 0.1$$

From equation 3.13 and equation 3.14, $V_{cm}$ is calculated to be 0.7V and $V_{bk}$ to be 0.26V. Together with $S_s$ and $S_c$, $\theta$ is calculated to be 0.87 from equation 3.21. Meanwhile from $g_{ds}$, $g_m$, $\sigma$ is calculated as 143 $V/s \cdot \sqrt{Hz}$. Upon substituting in equation 3.22 this gives $\sigma_\epsilon$ of 0.12ps. Substituting into equation 3.24 with equation 3.25 evaluated at an offset frequency of 1 MHz, we have phase noise of -92 $dBc/Hz$ at 1 MHz offset.

For example using design in Figure 2.5c design parameters are same as that for Figure 2.5b, with the additional $(W/L)_{7-8} = 0.25\mu m/0.12\mu m$. Phase noise is calculated to be -91dBc/Hz. The $\sigma$ would be larger due to extra M7-8 (see equation 3.23) and this results in more phase noise.

To generalize this, we work out different cases, and we summarize qualitatively this trend of phase noise vs parameter variations in Table 4.1 below. This allows us to capture design insights on effect of $V_{bias}$ and load ($(W/L)_{3-4}$ and $(W/L)_{5-6}$) on phase noise.

Table 4.1: Effect of circuit parameters on phase noise*

| | $V_{bias} \uparrow$ | $(W/L)_{3-4} \uparrow$ | $(W/L)_{5-6} \uparrow$ |
|---|---|---|---|
| $S_c$ | $g_{ds3} \downarrow \rightarrow S_s \uparrow$ | $g_{ds3} \uparrow \rightarrow S_s \downarrow$ | $g_{ds3} \downarrow \rightarrow S_s \uparrow$ |
| $S_c$ | $g_{ds3} \downarrow \rightarrow S_c \uparrow$ | $g_{ds3} \uparrow \rightarrow S_c \downarrow$ | $g_{m5} \uparrow, g_{ds3} \downarrow \rightarrow S_s \uparrow$ |
| $\theta^{**}$ | $\uparrow$ | $\downarrow$ | $\downarrow$ |
| phase noise $(PN)$ | $\uparrow$ | $\downarrow$ | $\downarrow$ |

*It should be noted that the impact on phase noise due to parameter variations (such as $g_m$, $g_{ds}$ and $V_{cm}/V_{bk}$) is primarily due to cycle to cycle correlation via $\theta$, as witnessed in the factor $1/(1-\theta^2)$ dependency in equation 3.24 and 3.25. The impact from $\sigma_\epsilon$, the noise factor, via the factor $\sigma_\epsilon^2$, by comparison is much smaller, as evidenced by the square root dependency of $\sigma$ (and subsequent $\sigma_\epsilon$ dependency) on $g_{ds3}, g_{m1,5,7}$ in equation 3.23. Hence it is neglected.

** For parameter variations considered in Figure 4.1, $S_s$ dominates $S_c$ in the 2nd, 3rd columns and vice versa in the 4th column, resulting in the subsequent trend in $\theta$ as shown.

To elaborate on where the trend in Table 4.1 comes from quantitatively:

$$V_{bias} \uparrow \xrightarrow{[5]:\text{Table IV}} g_{ds3} \downarrow \xrightarrow{\text{Eq. 3.16-3.17}} S_s, S_c \uparrow \xrightarrow{\text{Eq. 3.21}} \theta \uparrow \xrightarrow{\text{Eq. 3.24}-3.25} PN \uparrow$$

$$\left.\begin{array}{l} (W/L)_{3-4} \uparrow \\ (W/L)_{3-4} \uparrow \xrightarrow{\text{Eq. 3.14}} V_{cm} \uparrow \end{array}\right\} \xrightarrow{[5]:\text{Table IV}} g_{ds3} \uparrow \xrightarrow{\text{Eq. 3.16-3.17}} S_s, S_c \downarrow \xrightarrow{\text{Eq. 3.21}} \theta \downarrow \xrightarrow{\text{Eq. 3.24}-3.25} PN \downarrow$$

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$$(W/L)_{5-6} \uparrow \xrightarrow{\text{[5]:Table IV}} g_{m5} \uparrow \xrightarrow{\text{Eq. 3.17}} S_c \uparrow$$
$$(W/L)_{5-6} \uparrow \xrightarrow{\text{Eq. 3.14}} V_{cm} \downarrow \xrightarrow{\text{[5]:Table IV}} g_{ds3} \downarrow \xrightarrow{\text{Eq. 3.16}} S_s \uparrow \Bigg\} \xrightarrow{\text{Eq. 3.21}} \theta \downarrow \xrightarrow{\text{Eq. 3.24}-3.25} PN \downarrow$$

Next Eldo (Mentor Graphics) phase noise simulation *(.sstnoise)* is performed [13][1]. The resulting simulated phase noise is shown in row 1 and 3 of Table 4.2, where theory is seen to agree rather well with simulation.

The theoretical derivation and simulation are repeated, first with varying $V_{bias}$. We start by increasing the $V_{bias}$ used in design example (0.5V). Since $V_{bias}$ is used to tune VCO (see [8]), a typical tuning range of around 100mV is adopted here[8] i.e. from 0.5V to 0.6V. From theory, the phase noise worsens as bias voltage increases. As discussed previously, this is related to the decrease of $g_{ds}$ from equation 3.16 when bias is increased, which causes $|S_s|$ to decrease. Furthermore, as $V_{bias}$ increases, $V_{cm}$ decreases, causing an increase in $V_{bk}$. This decreases the magnitude of the denominator of equation 3.21, while only slightly decreases the numerator (for the $V_{bias}$ range adopted). This results in an overall increase of $\theta$, hence more cycle-to-cycle correlation, or worse phase noise. Meanwhile, with an increasing $V_{bias}$, $S_c$ would also increase, which would decrease $\theta$. However, again for the $V_{bias}$ range adopted, $\theta$ is dominated more by the change in $|S_s|$ and $V_{bk}$. The overall trend is shown in Figure 4.1 as "triangles" for top cross-coupled pair oscillator and as "diamonds" for top and bottom cross-coupled pair oscillator. Simulations were performed and results shown as "dots" for top cross-coupled pair oscillator (labelled as top, sizing: design example) and as "dots-and-dashes" for top and bottom cross-coupled pair oscillator.

---

[1]Eldo Platform delivers the required SPICE accuracy and performance for design and verification. Both SPECTRE and Eldo were used and have provided similar results, however most of the results are obtained using ELDO due to easier automation and faster run-time during simulation.

Finally, to see some of the impact of transistors sizing on phase noise, the above $V_{bias}$ sweep is repeated, with the sizing of the load halved. The *phase noise vs $V_{bias}$* is shown in Figure 4.1 as "circles" for top cross-coupled pair oscillator and as "asterisks" for top and bottom cross-coupled pair oscillator. Simulations were performed and results are shown as "dashes" for top cross-coupled pair oscillator and as "solid line" for top and bottom cross-coupled pair oscillator. As for the impact, with sizing of the load halved, the phase noise is worse since the decrease of sizing of the load decreases $V_{cm}$ and causes $|S_s|$ to decrease, resulting in higher correlation ($\theta$ becomes larger), and hence worse phase noise.
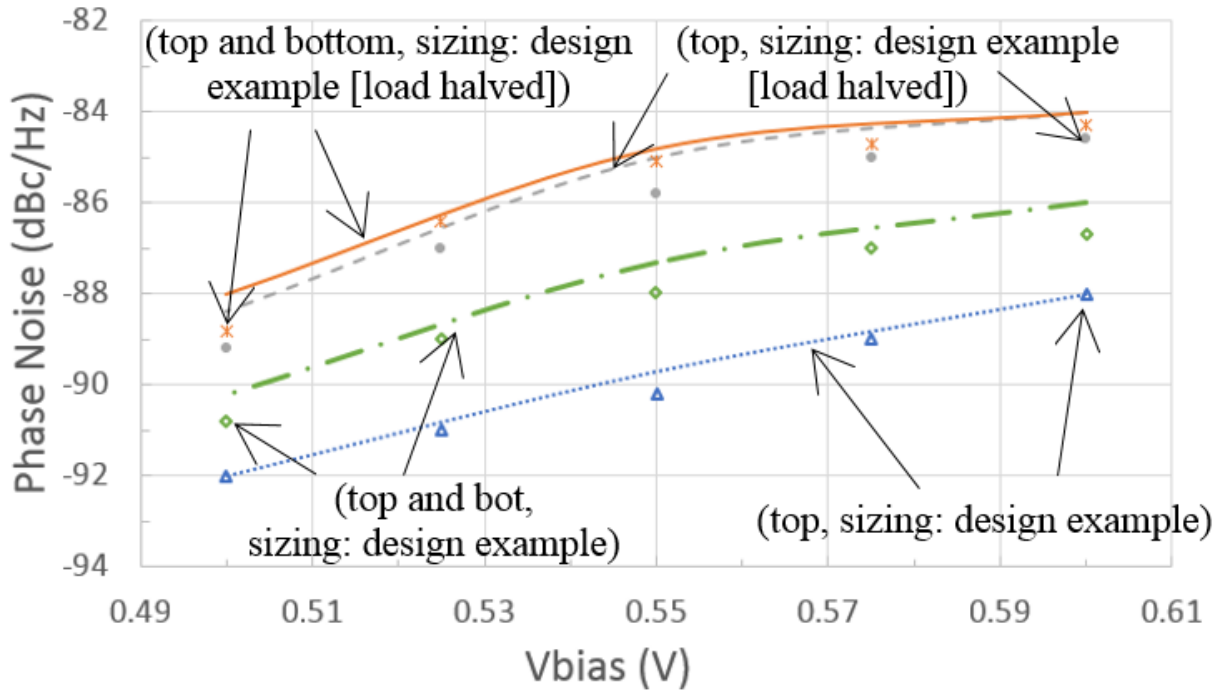


Figure 4.1: Simulated *phase noise vs. $V_{bias}$* at 1 MHz frequency offset for 4 cases: top/top and bottom (with design example sizing); top/top and bottom with sizing of the load halved. Numerical values calculated from derived phase model is shown as "triangles", "diamonds", "circles", and "asterisks".
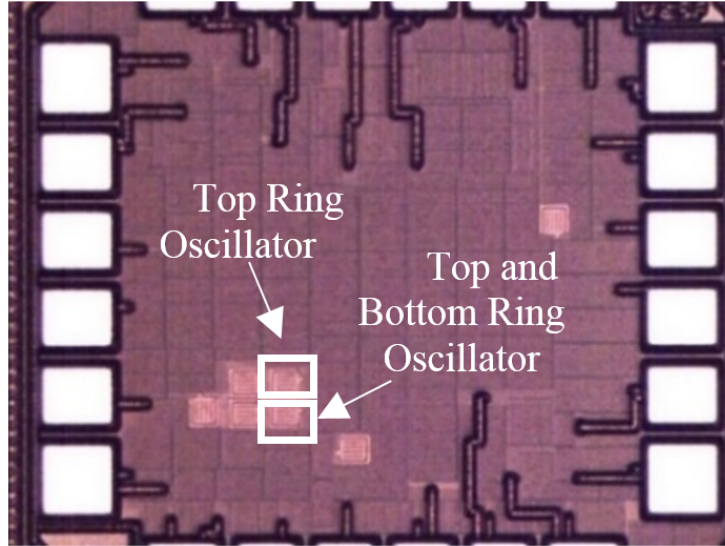
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## 4.2    Phase Noise Measurement Results



Figure 4.2: Ring oscillator chip microphotograph.

The design of two-stage oscillators using delay cells shown in Figure 2.5b and Figure 2.5c are implemented using 0.13um CMOS technology, $V_{DD}$ of 1.2V, with the transistor sizing employed in design example of section 4. Figure 4.2 shows the chip microphotograph. In measurements, $V_{bias}$ corresponding to the boundary of tuning range i.e. 0.5/0.6V is used. Figure 4.3-4.6 show the measured phase noise (PN) plots. Measured phase noise at 1 MHz offsets are shown in Table 4.2. The measured phase noise of Figure 2.5b is -92dBc/Hz at $V_{bias}$=0.5V and increases to -86dBc/Hz at $V_{bias}$=0.6V. For Figure 2.5c phase noise is -89dBc/Hz at $V_{bias}$=0.5V and increases to -85dBc/Hz at $V_{bias}$=0.6V. This agrees well with theory/simulation, as shown in Table 4.2. Note the slope at the 1 MHz offset frequency of Figure 4.3-4.6 is larger than -20dB/dec, this is due to the extra noise from cycle to cycle correlation.

Table 4.2: Numerical calculations, simulation, and measurement phase noise results at 1 MHz frequency offset for $V_{bias}$ of 0.5 V and 0.6 V

| Design | $V_{bias}$ (V) | Theory (dBc/Hz) | Simulation (Eldo) (dBc/Hz) | Measurement (dBc/Hz) |
|---|---|---|---|---|
| Top cross-coupled pair | 0.5 | -92 | -92 | -92 |
| | 0.6 | -88 | -88 | -86 |
| Top and bottom cross-coupled pair | 0.5 | -91 | -89 | -89 |
| | 0.6 | 87 | -85 | -85 |

We have presented a new model for calculating the phase noise of a 2-stage unsaturated ring oscillator in low voltage implementation. Two different delay cell topologies are investigated. Compared to previous phase noise model for unsaturated differential ring oscillator, it can handle topologies with no tail current source. Using a $0.13\mu m$ CMOS technology in 1.2 V supply, theory compares well with simulation under different circuit parameters and operating conditions. Measured results on fabricated chip show the effect of changing bias voltage (for tuning the VCO) on phase noise and it agrees with theory and simulation.

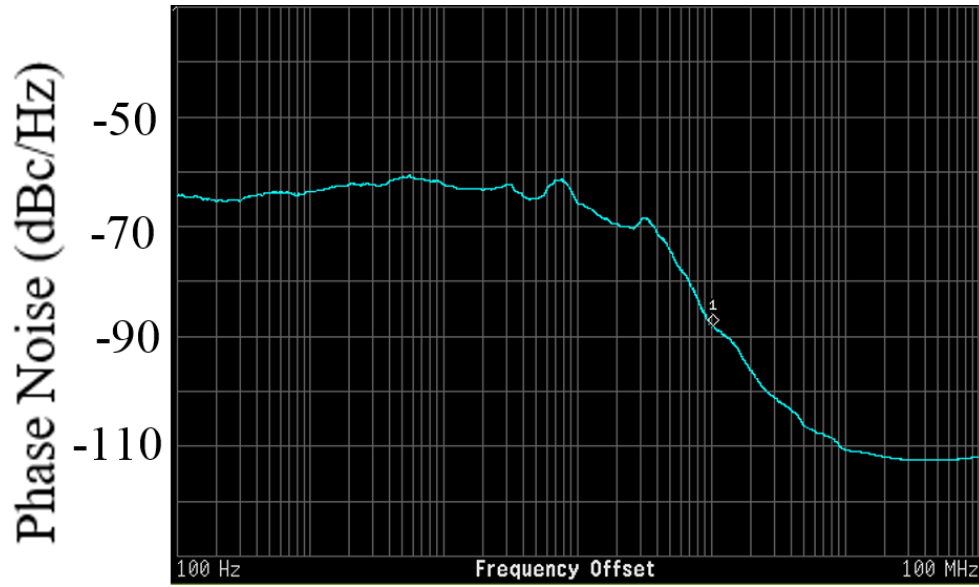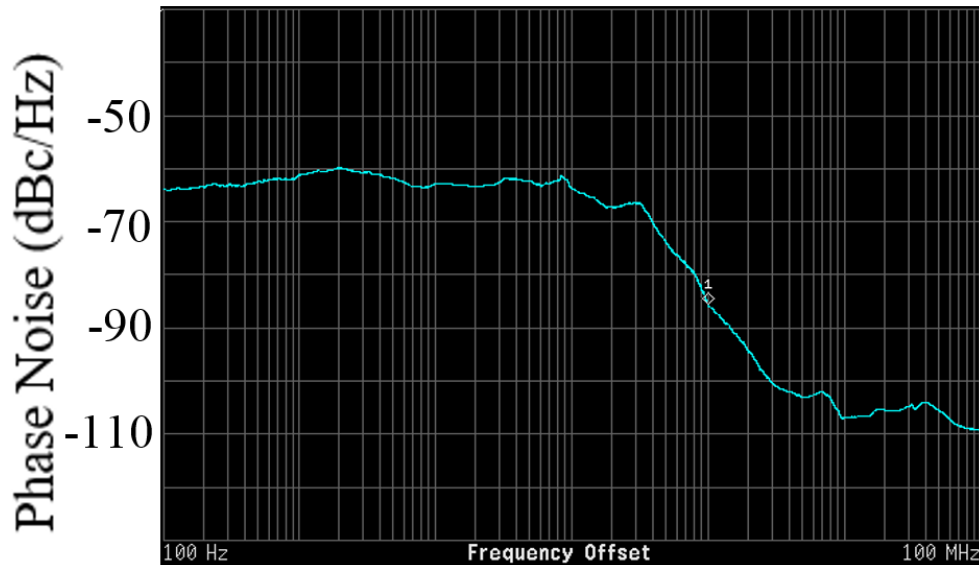Figure 4.3: Phase noise plot of top and bottom oscillator: -89dBc/Hz at 1 MHz offset, $V_{bias}$=0.5V.



Figure 4.4: Phase noise plot of top and bottom oscillator: -85dBc/Hz at 1 MHz offset, $V_{bias}$=0.6V.
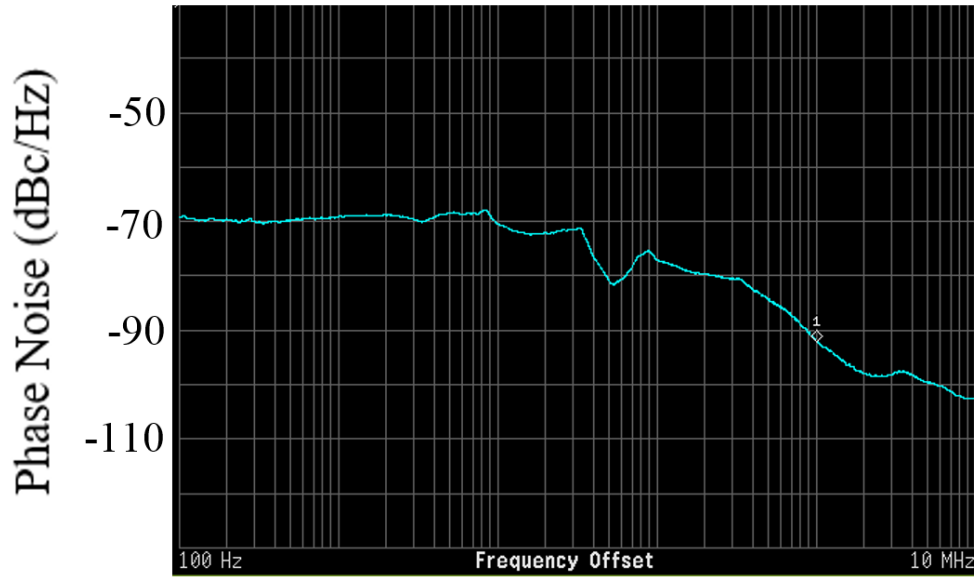
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Figure 4.5: Phase noise plot of top oscillator: -92dBc/Hz at 1 MHz offset, $V_{bias}$=0.5V.
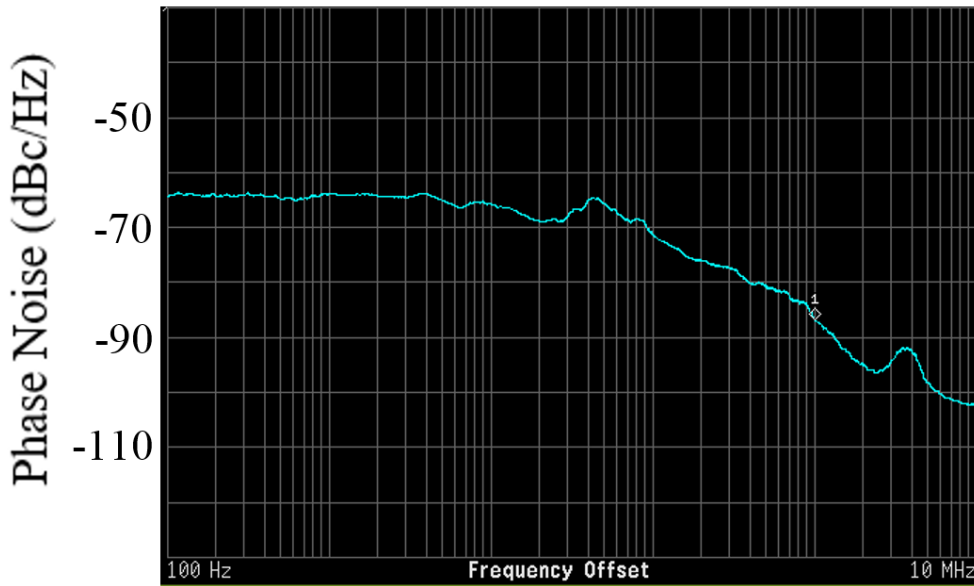


Figure 4.6: Phase noise plot of top oscillator: -85dBc/Hz at 1 MHz offset, $V_{bias}$=0.6V.

# Chapter 5

# Application of Proposed Oscillator: Time to Digital Converter

## 5.1 Introduction

As technology scales down, so does the supply voltage. The reduction in supply voltage results in lower voltage swing. This causes low signal to noise ratio (SNR) in analog to digital converters (ADCs). Furthermore, the threshold voltage of the transistor does not decrease at the same rate as the supply voltage. Hence, operational amplifiers in ADCs becomes more and more difficult to design. Time based digital converters, on the other hand, do not suffer from the lowering of voltage swings, nor is it necessary for them to require the use of operational amplifiers making them very advantageous in this regard.

The function of the time to digital converter (TDC) is to quantize the time representation of the input into a digital code. TDC may be implemented as a count and dump converter, as shown in Figure 5.1. To implement this, the TDC counts and quantizes the

number of rising edges of the period modulated signal $F_{in}$ during the sampling interval period of $F_{ref}$ as shown in Figure 5.2.
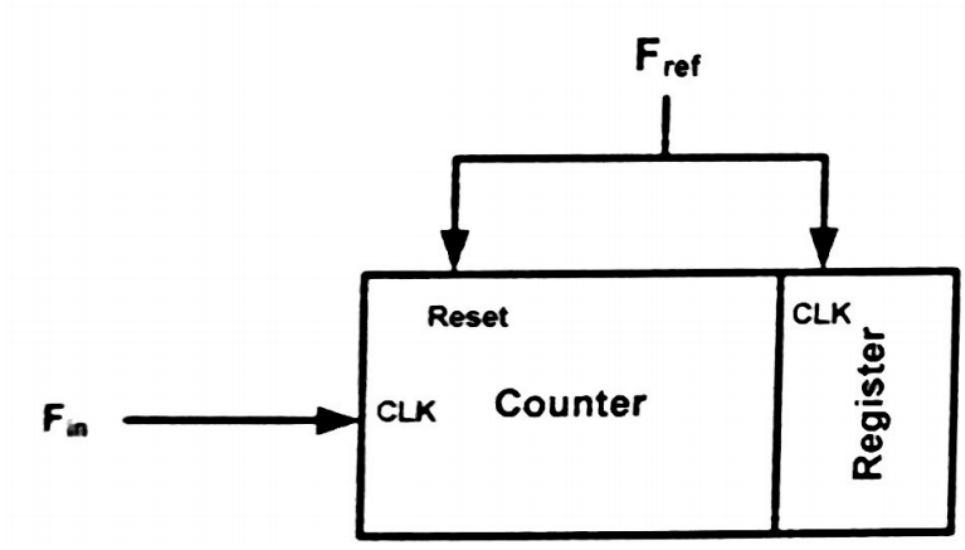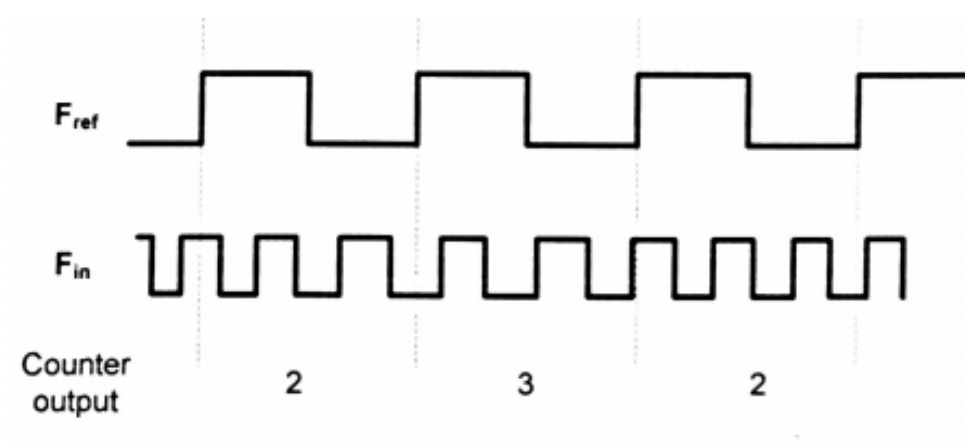


Figure 5.1: Counter TDC



Figure 5.2: Counter TDC waveforms

This TDC is simple and cost efficient, however, the drawback of this type of TDC

is the counter resetting operation, which is a limiting factor for high-speed operation. Furthermore, there may be aliasing effect if the next input is sampled before completion of the previous operation.

### 5.1.1   First Order Sigma-Delta Based TDC

To deal with the resetting of the counter, the aforementioned TDC can be implemented as a first order oversampling Sigma-Delta TDC. [1] implements a first order TDC through use of a D flip-flop as a phase detector and a dual modulus frequency divider (DMD), Figure 5.3.

Figure 5.4 is a simplified waveform representation of Figure 5.3. The input signal, $f_{in}$, is assumed to be a carrier with some form of angle modulation. The DMD divides the input frequency either by N or by N + 1, according to the digital output.

D flip-flop acts as a quantizer, it compares the rising edge of the reference frequency $f_{ref}$ with the output of the DMD $f_{out}$ and gives a one-bit approximation of the phase difference. DMD operates at a frequency, phase locked with the reference between $N f_{ref}$ and $(N+1)f_{ref}$. When the digital output is '1', DMD has an output frequency, $f_{out}$, with an average input period $(N + 1)T_{in}$, where $T_{in}$ is average period of $f_{in}$. When the digital output is '0', DMD has an output frequency, $f_{out}$, with an average input period $(N)T_{in}$.

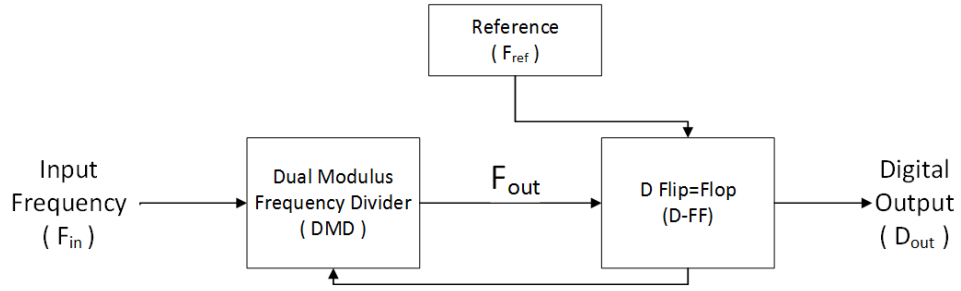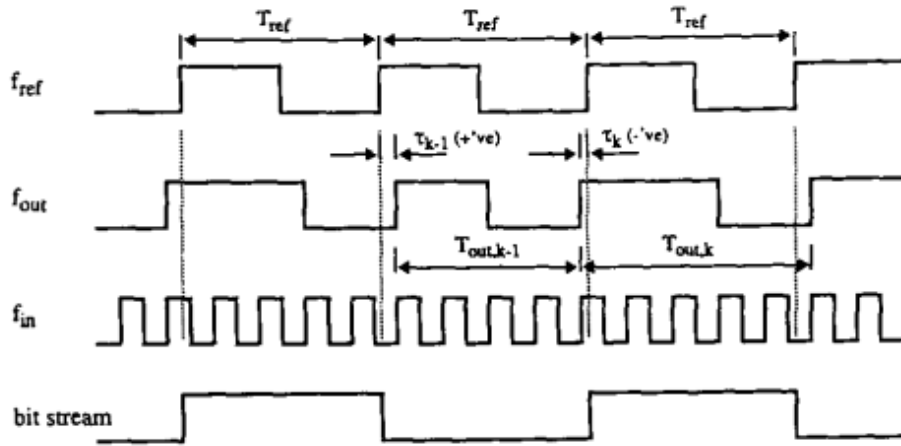Figure 5.3: First order sigma delta TDC



Figure 5.4: Example output of first order TDC

Figure 5.4 is an example output of the TDC obtained in [1], where N is 4. From Figure 5.4, the first order difference equation describing the system can be written as

$$\tau_k = \tau_{k-1} + [(N+0.5)T_{in,k} - T_{ref}] - sgn(\tau_{k-1})T_{in,k-1}/2 \tag{5.1}$$

where

$$T_{in,k} = [(N+0.5)T_{in,k} - T_{ref}] \tag{5.2}$$

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which corresponds to the simplified 1st order system level block diagram in Figure 5.5.
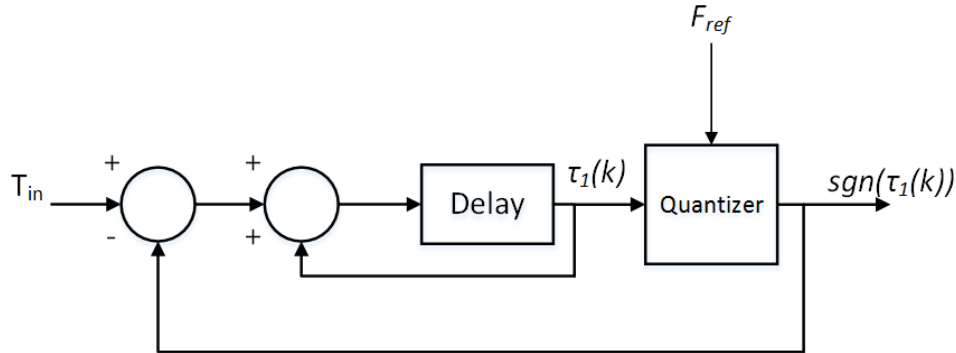


Figure 5.5: Block diagram of first order TDC

## 5.2 Second Order Sigma-Delta Based TDC

Oversampling delta-sigma modulation techniques have become very popular as a mean of achieving high-resolution data conversion with low-cost technologies.

The underlying characteristic of delta-sigma modulation which allows for the realization of high-resolution data converters is the high pass transfer function of quantization noise to the output imposed by the loop. Higher-order loops impose higher-order transfer functions resulting in even greater suppression of baseband quantization noise. As well, the use of higher-order loops significantly reduces the correlation of quantization noise with input level, helping to minimize the problem of noise spikes and hence to further reduce baseband quantization noise. Because of these reasons, higher-order delta-sigma loops are generally used to realize practical high-resolution converters [1].
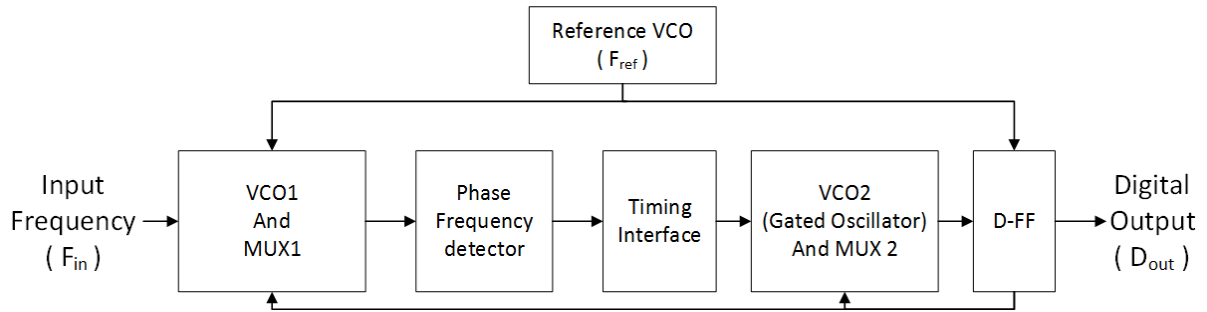
Figure 5.6: Block diagram of a system level second order Sigma Delta TDC.

## 5.3  TDC Implementation

The block diagram of Figure 5.6 represents a second order time to digital converter in time domain. The system takes in a angular modulated signal and is compared to the output of a merged voltage controlled oscillator and multiplexer, $VCO1$ and $MUX1$. The phase difference or timing difference between the input signal and output of merged $VCO1$ and $MUX1$ is collected by the phase frequency detector. This difference is used to control the period of the second VCO, $VCO2$, which is a gated ring oscillator (GRO). Like $VCO1$ and $MUX1$, $VCO2$ is also merged with the second multiplexer $MUX2$. Finally the output of $VCO2/MUX2$ is passed into a D flip-flop, which access as the quantizer and a digital (binary) output is produced. This digital signal is then fedback to control $MUX1$ and $MUX2$.

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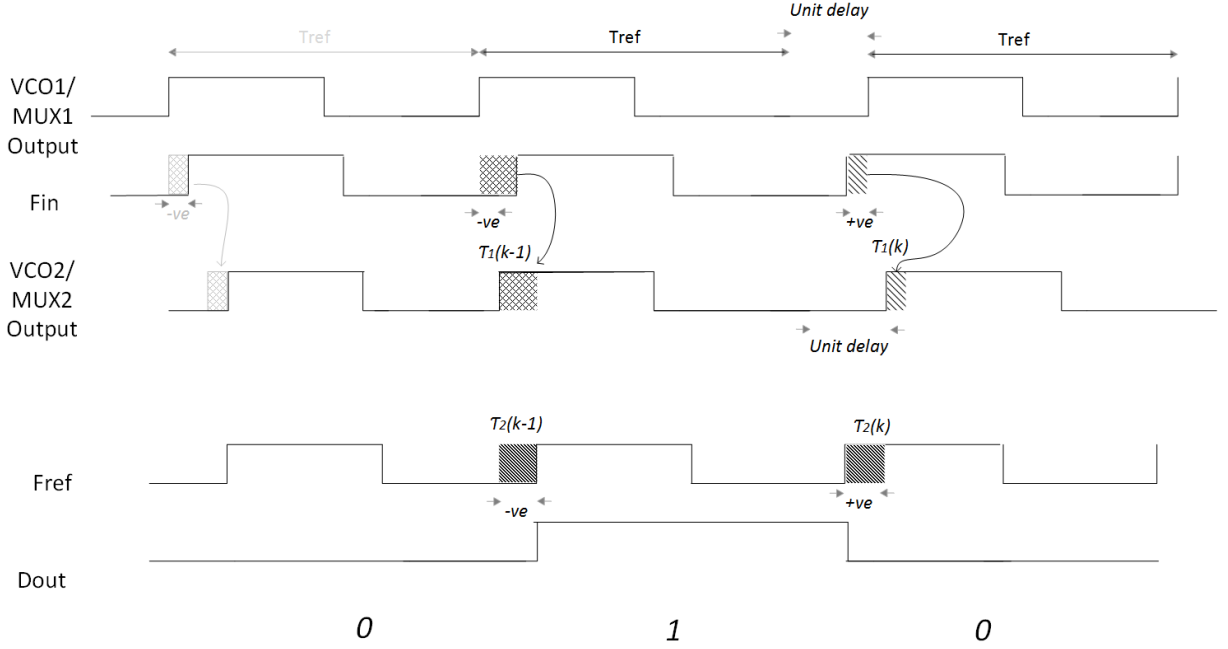
Figure 5.7: Representative waveforms of system shown in Figure 5.6

Figure 5.7 illustrates a set of representative waveforms for system shown in Figure 5.6. From 5.7 we can obtain the second order difference equation describing the system, which will be further elaborated in this section.

$$\tau_1(k) = \tau_1(k-1) + T_{in} - sgn(\tau_2(k-1)) \cdot t_{unitdelay} \tag{5.3}$$

$$\tau_2(k) = \tau_2(k-1) + \tau_1(k) - sgn(\tau_2(k-1)) \cdot t_{unitdelay} \tag{5.4}$$

where $T_{in}$ is the time representation of the input signal obtain from subtracting the reference period from period of $Fin$ .

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Figure 5.8 shows a block diagram representing of equation 5.3 and equation 5.4. As we can see Figure 5.8 is clearly a second order $\Delta\Sigma$ in time domain.



Figure 5.8: The equivalent block diagram of 2nd Order TDC

## 5.3.1 Voltage Control Oscillator 1 and Multiplexor 1 Based on Proposed Cross-Coupled Oscillator Design



Figure 5.9: Block diagram of VCO1 and MUX1

A more in-depth block diagram of $VCO1$ and $MUX1$ is displayed in Figure 5.9. 5.9 illustrates two top cross-coupled delay cell, Figure 2.5c, where the output of second delay cell is fed into the $MUX1$ i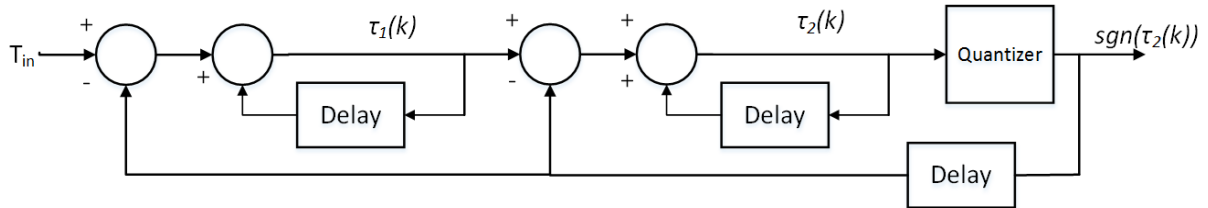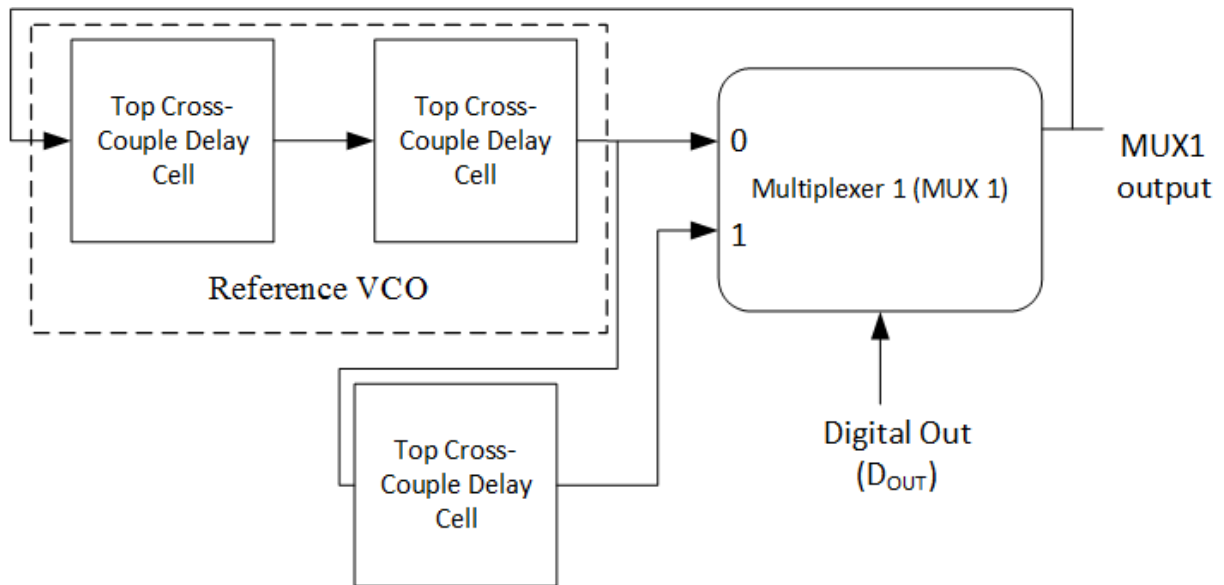nput '0', and also to another top cross-coupled delay cell which is then feed into $MUX1$ input '1'. The output of the multiplexer is fedback into the input of the first delay cell, forming a merged VCO. $MUX1$ is controlled by the digital signal fedback by the output of the TDC. If the digital output is '0' the output of the multiplexer is the output of a 2-stage VCO, which is designed to have the same frequency as the reference VCO, and if the digital output is '1', the output of the multiplexer is the output of a 3-stage VCO. We can express in terms of period

$$
T_{VCO1} = \begin{cases} T_{ref}, & \text{if } Dout = 0 \\ T_{ref} + T_{unit\_delay}, & \text{if } Dout = 1 \end{cases} \tag{5.5}
$$

where $T_{VCO1}$ is the period of the merged $VCO1$ and $MUX1$. $T_{ref}$ is the period of the reference VCO, and $T_{unit\_delay}$ is the delay caused by the third top cross-coupled pair delay cell. We can then express the output of $MUX1$ as:

$$
T_{MUX}(k) = T_{MUX}(k-1) + T_{VCO1} \tag{5.6}
$$

Substituting 5.5 into 5.6:

$$
T_{MUX}(k) = T_{MUX}(k-1) + T_{ref} + sgn(D_{out}(k-1)) \cdot T_{unit\_delay} \tag{5.7}
$$

where in terms of time, $T_{MUX}(k)$ is the current output of $MUX1$ and $T_{MUX}(k-1)$ is the previous output of $MUX1$ and $D_{out}(k-1)$ is the previous digital output.

## 5.3.2  Phase Frequency Detector and Timing Interface

The phase frequency detector is a simple comparator that compares the output of $MUX1$ to the phase of the input signal. The difference between the rising edge of the two signals in time, is used to control the period of the second VCO ($VCO2$).

First, we can express the the period of the input signal as the summation between the period of the carrier, $T_{carrier}$, and $T_{in}$ the varying phase input. The carrier period, $T_{carrier}$, is also equivalent period of the reference signal $T_{ref}$. The complete input signal can be written as:

$$T_{input}(k) = T_{input}(k-1) + T_{ref} + T_{in} \tag{5.8}$$

Subtracting output of $MUX1$ from the input signal (i.e. $T_{input}(k) - T_{MUX}(k)$) results in the phase frequency detector output, $\tau_1$ shown below:

$$\tau_1(k) = T_{input}(k-1) + T_{in} - T_{MUX}(k-1) - sgn(D_{out}(k-1)) \cdot T_{unit\_delay} \tag{5.9}$$

and is further simplified to

$$\tau_1(k) = \tau_1(k-1) + T_{in} - sgn(D_{out}(k-1)) \cdot T_{unit\_delay} \tag{5.10}$$

where $\tau_1(k-1) = T_{input}(k-1) - T_{MUX}(k-1)$. This is the same as equation 5.3. Note $\tau_1(k)$ is recursive, and represents the first integrator of Figure 5.8. When $\tau_1$ is positive, $T_{input}$ lags $T_{MUX}$. $\tau_1$ is negative when $T_{input}$ leads $T_{MUX}$.

As stated earlier $\tau_1$ is used to controlled the period of $VCO2$. If $\tau_1$ positive we add a delay of length $\tau_1$ to period of $VCO2$. However, if $t_1$ is negative, we must add a *negative*

*delay* to period of $VCO2$. Physically, it is impossible to add a *negative delay.* A solution to this problem is to make sure that the period of $VCO2$ is always smaller than period of reference period by a value of $T_d$. We can then add $T_d$ back to the period of $VCO2$ by means of the timing circuity shown in Figure 5.10 and Figure 5.11.

Figure 5.10 shows a timing waveform example when the period of input signal period lags behind the output of VCO (i.e. $\tau_1$ is positive). The timing difference between a shifted $MUX1$ output and input signal $F_{in}$ gives an enable signal of length $T_d + \tau_1(k)$. By adding this enable signal to the period of $VCO2$ we obtain:

$$T_{gro} + T_d + \tau_1(k) = T_{ref} - T_d + T_d + \tau_1(k) = T_{ref} + \tau_1(k) \tag{5.11}$$

where $T_{(}gro)$ which is the period of $VCO2$. The period of $VCO2$ has period of $T_{ref} + \tau_1(k)$.

Similarly, Figure 5.11 shows a timing waveform example when the period of input signal period leads the output of VCO, (i.e. $\tau_1$ is negative ). The timing difference between the shifted $MUX1$ output and $F_{in}$ gives an enable signal of $T_d + \tau_1(k)$. In this case $\tau_1(k)$ is negative. By adding this enable signal to the period of $VCO2$ we once again obtain:

$$T_{gro} + T_d + \tau_1(k) = T_{ref} - T_d + T_d + \tau_1(k) = Tref + \tau_1(k) \tag{5.12}$$

The period of $VCO2$ has period of $T_{ref} + \tau_1(k)$, with a negative $\tau_1(k)$.

For proper operation of the phase detector and timing circuitry the rising edge of the shifted $MUX1$ output must always lead the rising edge of input signal. The shifting of $MUX1$ output can be easily implemented by adding a delay cells to the output of $MUX1$.

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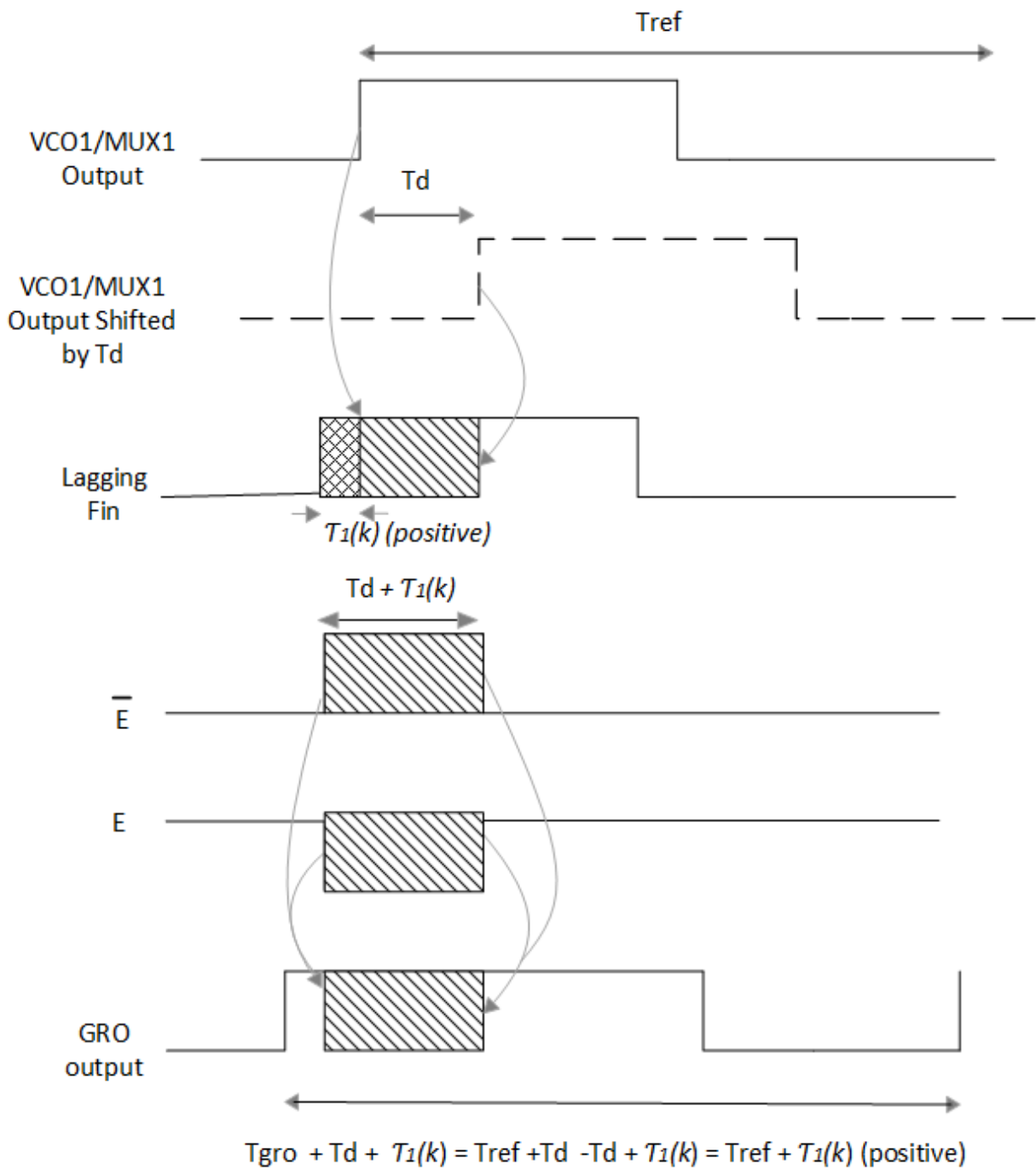
Figure 5.10: When input lags behind VCO ouput 1
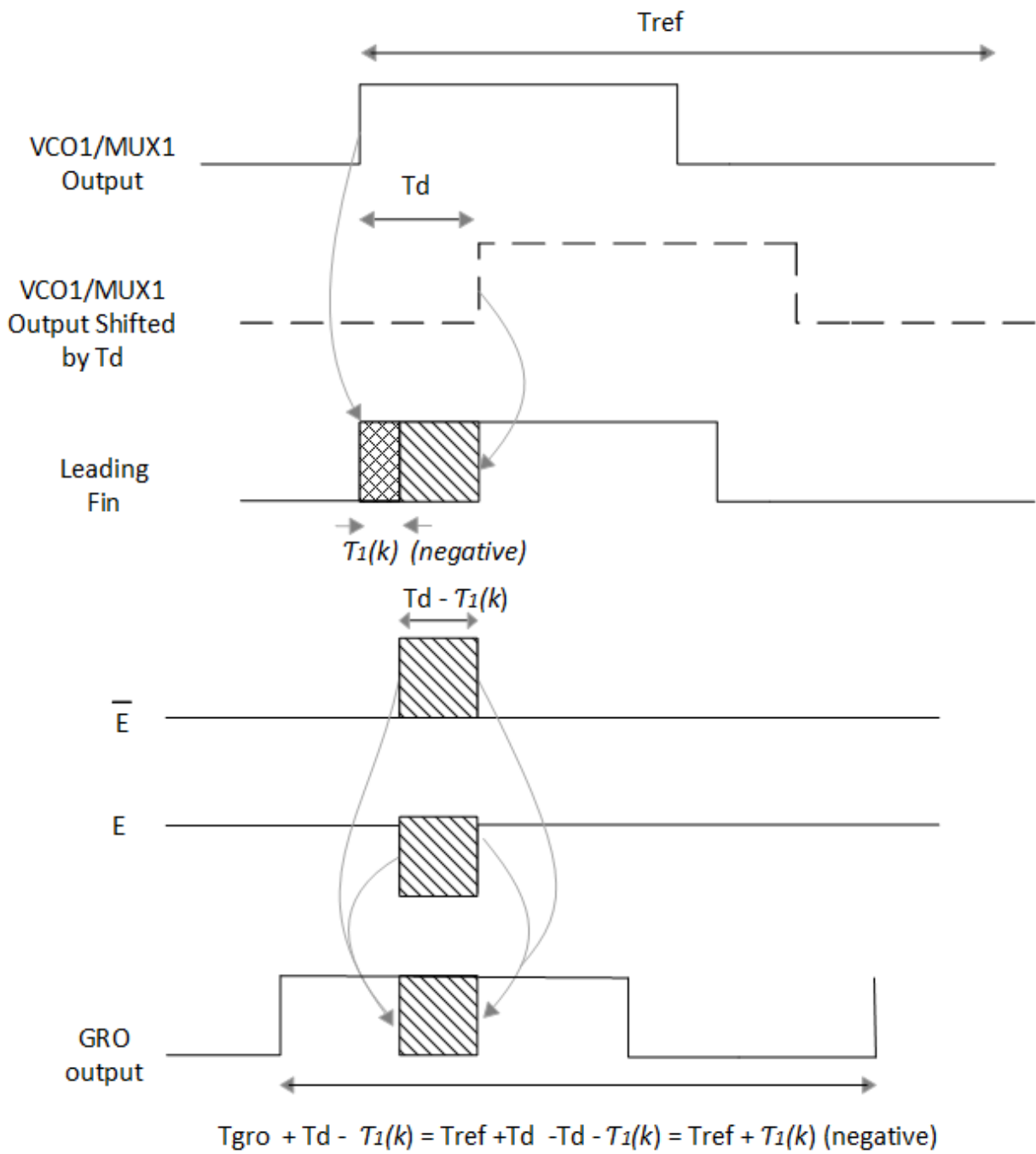
Figure 5.11: When input leads VCO ouput 1

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The addition of $\tau_1$ to the period of $VCO2$ is accomplished by means of transmission gates shown in Figure 5.12. The two inverter at the output of the phase detector transmission gate is used to generate the enable and disable signal, $E$, which is adds $\tau_1$ to the period of $VCO2$ through use of the GRO.

The truth table for $E$ is shown in Table 5.1. Since input $F_{in}$ always lag behind the shifted output of $MUX1$. $E$ is low only when $F_{in}$ is high and when shifted $MUX1$ is low.
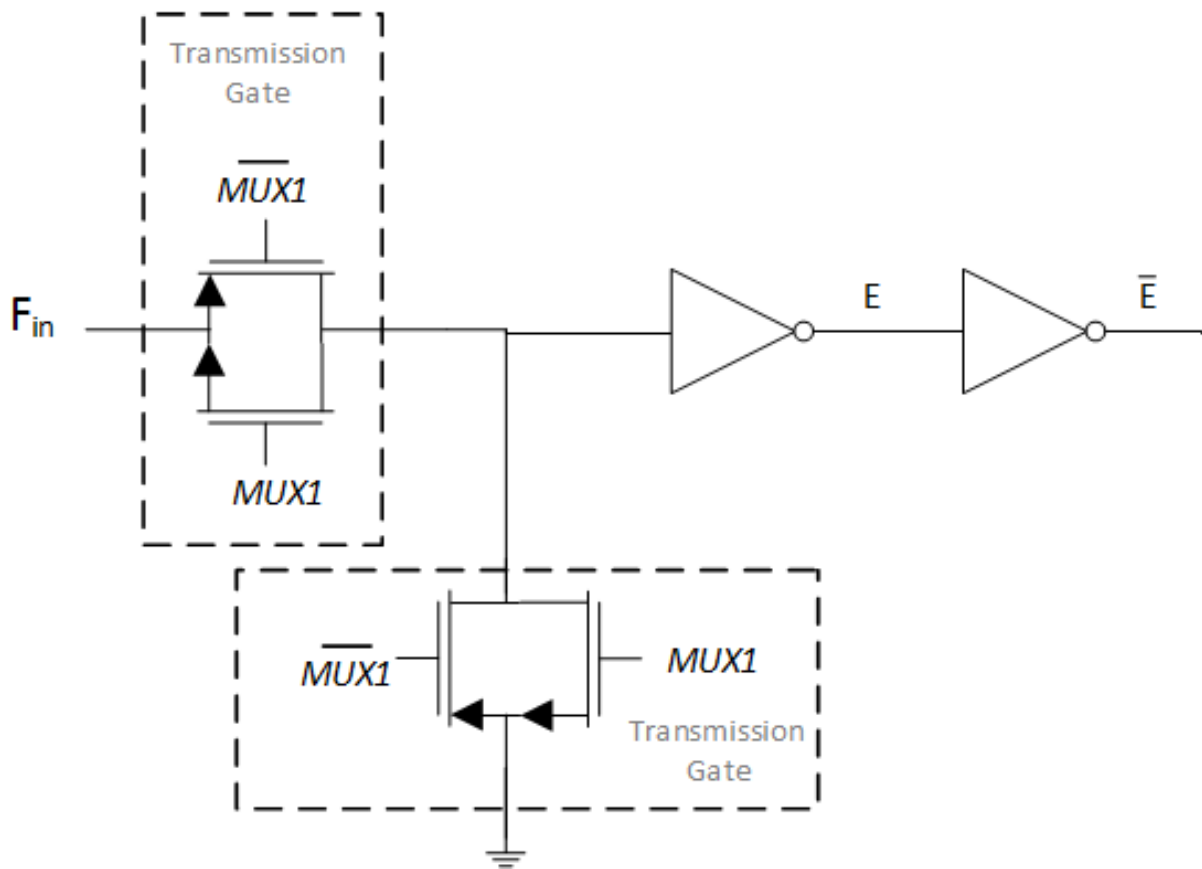


Figure 5.12: Phase Detector and timing circuit output $E$ and $\overline{E}$

Table 5.1: Phase detector output

| $F_{in}$ | Shifted $MUX1$ | $E$ |
|:---:|:---:|:---:|
| 0 | X | 1 |
| 1 | 1 | 0 |
| 1 | 0 | 1 |

### 5.3.3 VCO2 with MUX2 Based on Proposed Cross-Coupled Oscillator Design

Similar to $VCO1$ and $MUX1$, $VCO2$ is merged with $MUX2$ with the added input of $E$, which adds as $\tau_1$ to the period of $VCO2$ shown in Figure 5.13. We can express the output of $MUX2$ as:

$$T_{MUX2}(k) = T_{MUX2}(k-1) + T_{ref} + \tau_1(k) + sgn(D_{out}(k-1)) \cdot T_{unit\_delay} \qquad (5.13)$$

where in terms of time, $T_{MUX2}(k)$ is the current value of $MUX2$. $T_{MUX2}(k-1)$ is the previous value of $MUX2$. $D_{out}(k-1)$ is the previous digital output and $\tau_1(k)$ is delay caused by the enable signal $E$.
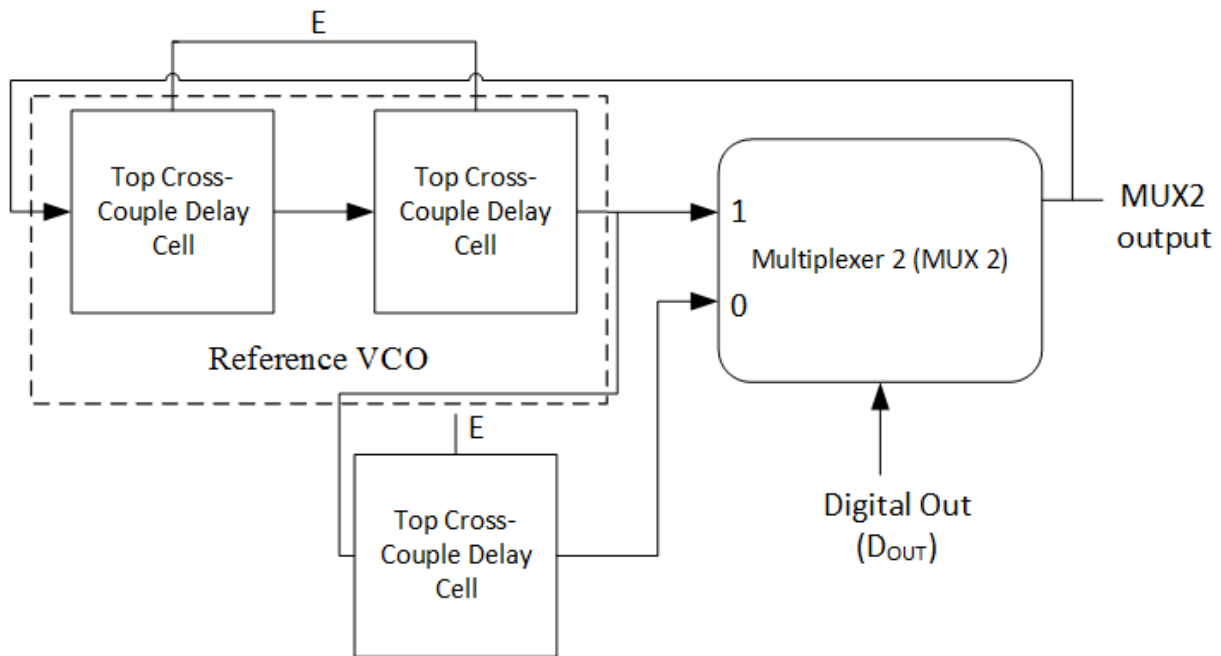
Figure 5.13: MUX2 merged with VCO2 block diagram

Now the only problem remaining is how to add the $\tau_1$ to period of $VCO2$. This is accomplished through the use of GRO.

### 5.3.4 Gated Ring Oscillator

Figure 5.14 illustrates an inverter based gated ring oscillator (GRO) used in [2]. In Figure 5.14, two transistor switches are added to each inverter of the conventional ring oscillator. The NMOS switch and the PMOS switch are controlled by the enables signals $E$ and $\overline{E}$ respectively.
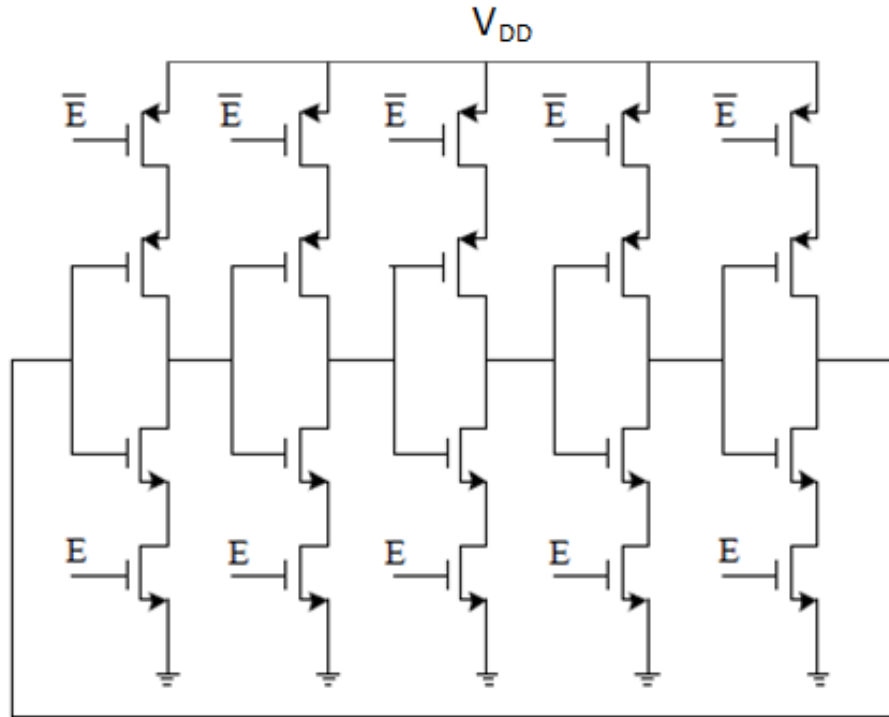
Figure 5.14: Cadence transistor design of phase detector using transmission gates

If the switches are closed, E is '1', as shown in Figure 5.14(a), the supply will be connected to the inverters and the ring starts oscillation. On the other hand, if the switches are open, E is '0', as shown in Figure 5.14(b), the paths to $V_{DD}$ and $gnd$ will be disconnected and there is no path for the parasitic capacitance, at the output of each inverter, to charge or discharge . This means that when the GRO is not enabled. It will retain the state of the ring just before the enable signal switches from '1' to '0'. When the GRO is enabled again the ring will start oscillating from the last saved state [1].

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[1]The effect caused by the deterioration of state with time is negligible as the GRO is only enable during a very small interval of time

We can replace the inverter delay cell based GRO in Figure 5.14 with cross-coupled pair delay cell proposed in section 2.4. Furthermore we can reduce the number of stages of the GRO to two as illustrated in Figure 5.16.

However the problem with the GRO in Figure 5.14 and Figure 5.16, is that the GRO is stacked with 4 transistors, leaving high overhead and not ideal for low supply voltage applications. Hence a modification of the GRO is made and shown as 5.16.
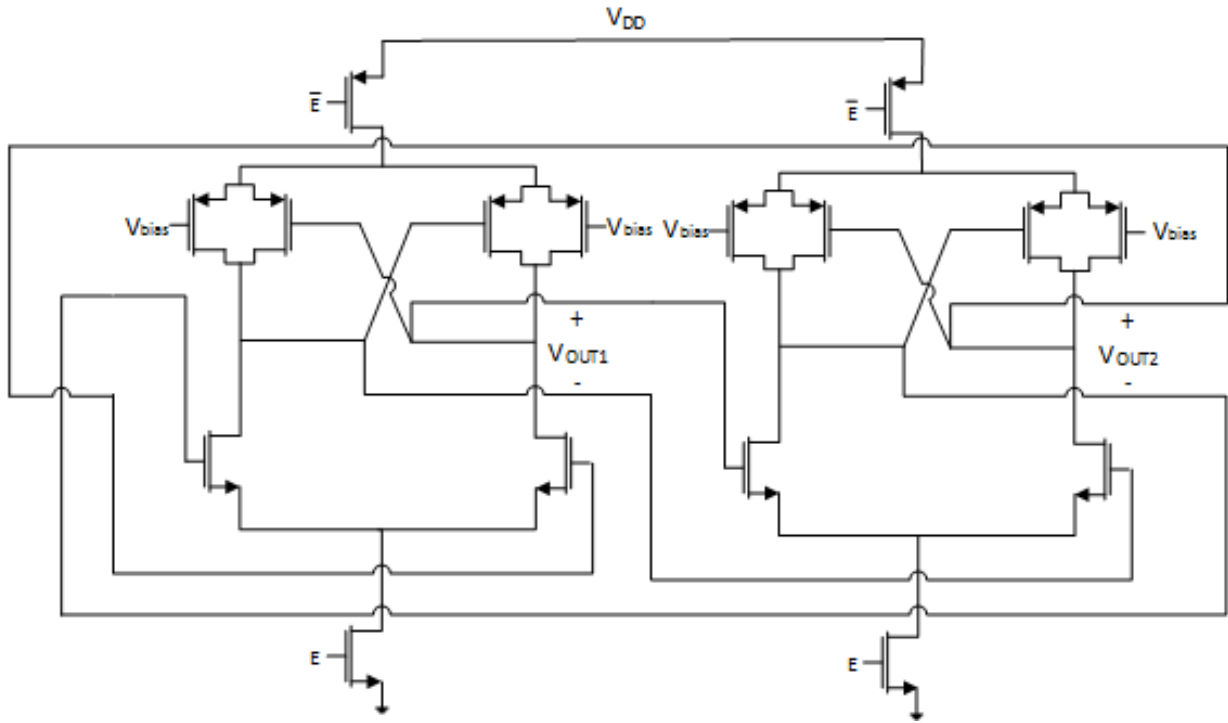


Figure 5.15: Cadence transistor design of gated cross coupled pair ring oscillator using transmission gates
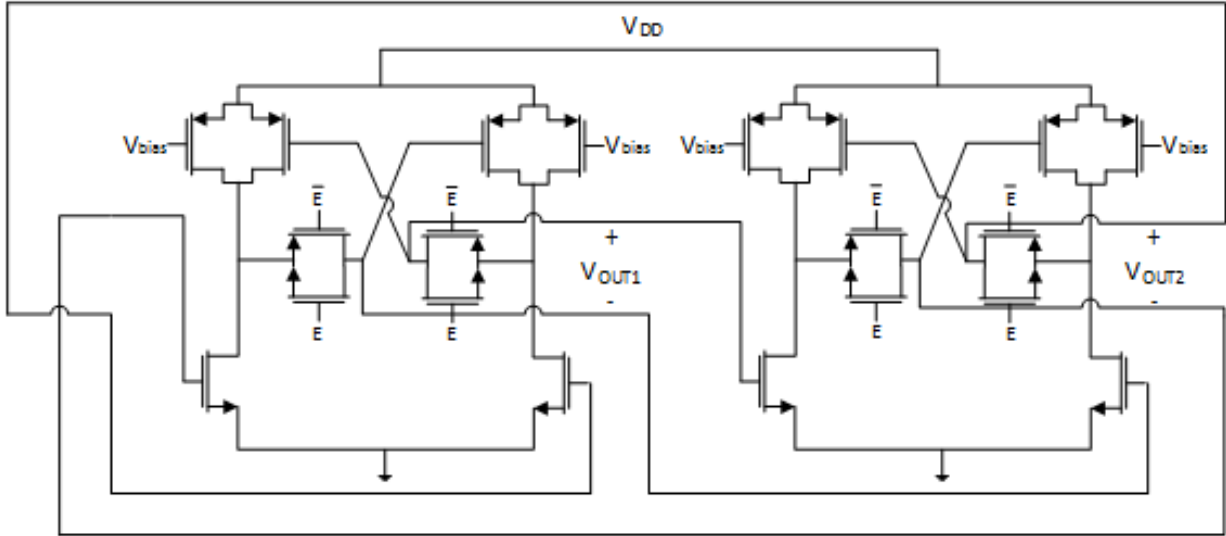
Figure 5.16: Cadence transistor design of gated cross coupled pair ring oscillator using transmission gates located at output of each delay cell

When $E$ is '1', the output of the delay cell charges and discharges using the load and driver transistors, and the ring oscillators oscillates. On the other hand, when $E$ is '0', There is no path for the output of the parasitic capacitance, at the output of the delay cell to charge or discharge. This disables the GRO and oscillation stops. The state of the output voltage is retained, until $E$ once more becomes '1'.

### 5.3.5   Quantizer: Digital Output

Finally, the digital output is obtain by comparing the rising edge of $MUX2$ with the rising edge of the reference $VCO$. We can express the difference between the two edges as:

$$\tau_2(k) = T_{MUX2}(k-1) + T_{ref} + \tau_1(k) + sgn(D_{out}(k-1)) \cdot T_{unit\_delay} - T_{ref\_out}(k-1) - T_{ref} \quad (5.14)$$

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and is further simplified to

$$\tau_2(k) = \tau_2(k-1) + \tau_1(k) - sgn(D_{out}(k-1)) \cdot T_{unit\_delay} \tag{5.15}$$

where $T_{ref\_out}(k-1)$ is the previous output of reference VCO and $\tau_2(k-1) = T_{MUX2}(k-1) - T_{ref\_out}(k-1)$. This is the same as equation 5.4.

If $\tau_2$ is greater than 0 (i.e. $MUX2k$ lags behind the falling edge of the reference VCO), a digital output of '1' is given. If $\tau_2$ is less than 0 (i.e. $VCO2_{out}$ leads the falling edge of the reference VCO), a digital output of '0' is given. This is comparator is implemented via a simple digital flip-flop.

## 5.4   TDC Simulation

This section illustrates the functionality of the second order sigma delta modulator, first from a system level, then from transistor level.

## 5.5   System Level Simulation

Figure 5.17 is the system level Matlab simulation of the second order $\Sigma\Delta$ modulator operating at 1 GHz, with a sinusoidal input signal of 3.14 Mhz. Figure 5.17 convey the correct digital ouput. Furthermore Figure 5.18 is the FFT output, it shows a 2nd order noise shaping showing that the system is indeed a second order $\Sigma\Delta$ TDC. Figure 5.19 shows the SNR of the system as function of signal amplitude. 5.20 shows the SNR of the TDC with varying jitter injected in the oscillator. 5.20 shows that the SNR drops approximately 15dB when a jitter of 4ps is injected.
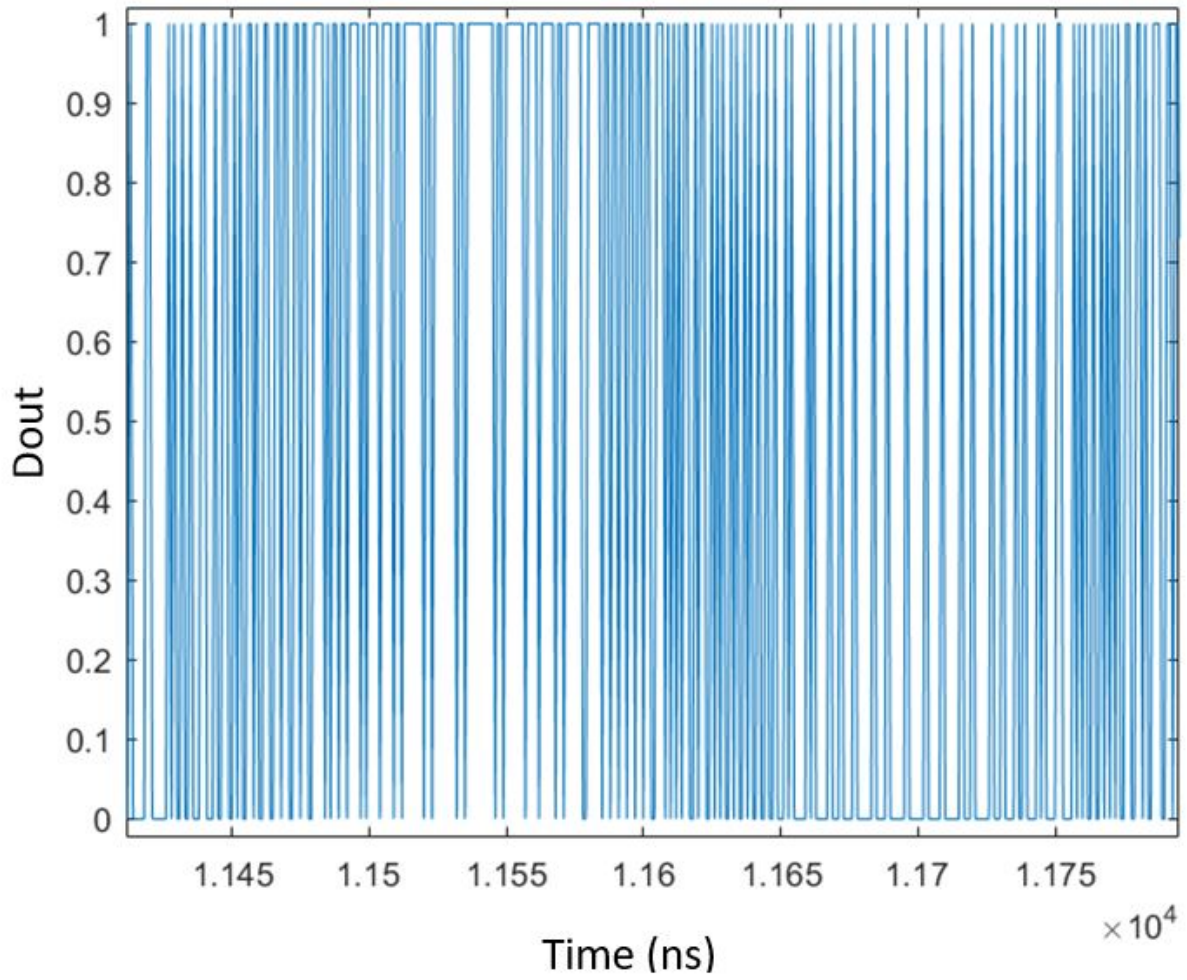
Figure 5.17: Sinusoidal pulse density modulation output of system level Matlab simulation of 2nd order $\Sigma\Delta$ TDC
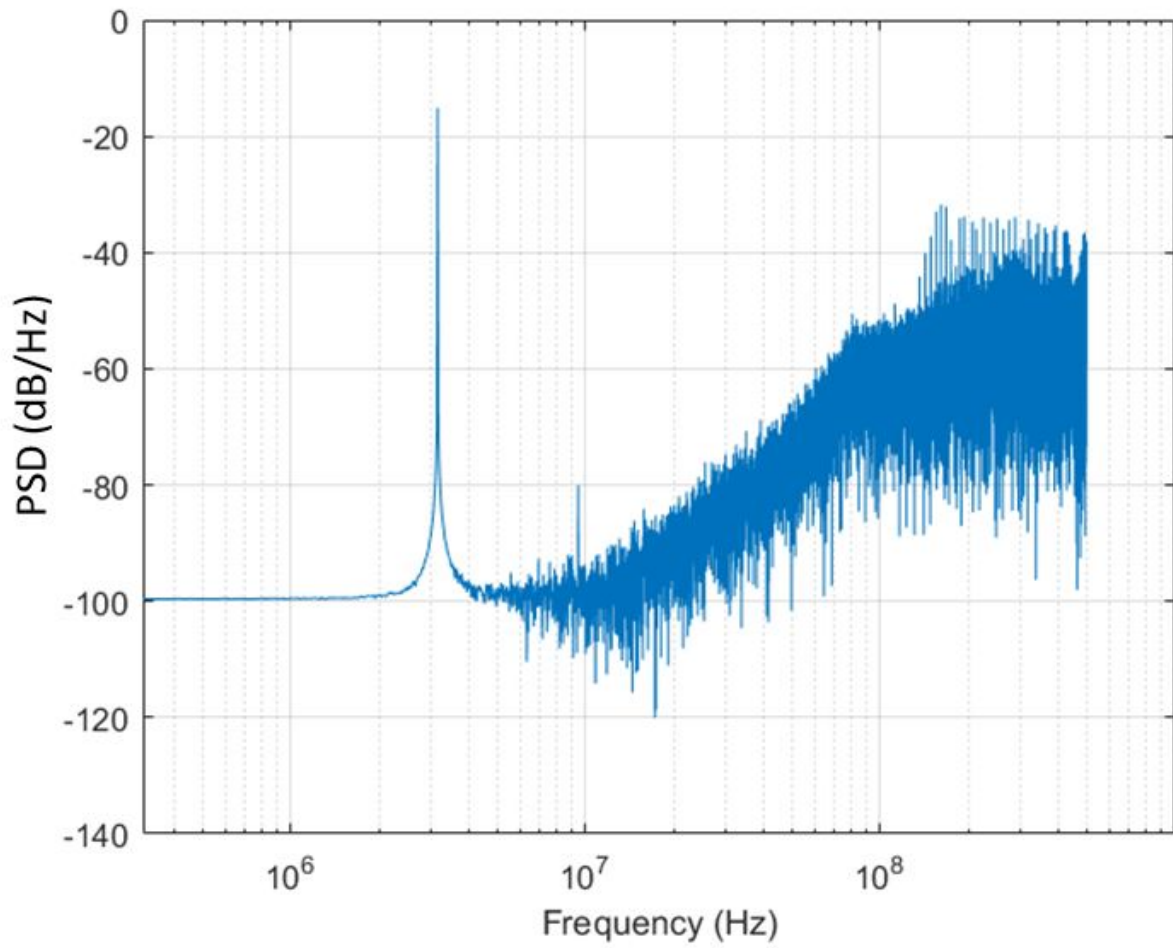
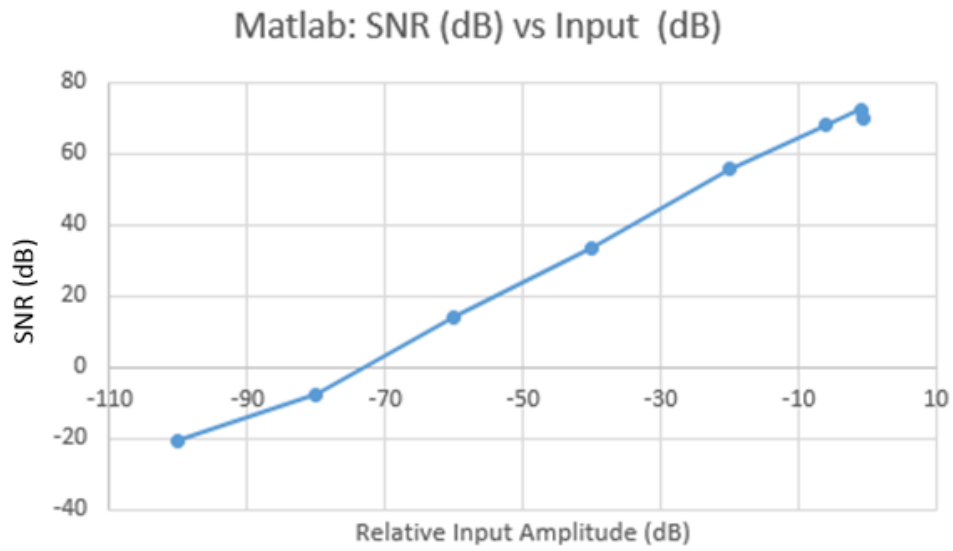Figure 5.18: System level FFT output of TDC showing 2nd order noise shaping

Figure 5.19: SNR vs input signal amplitude
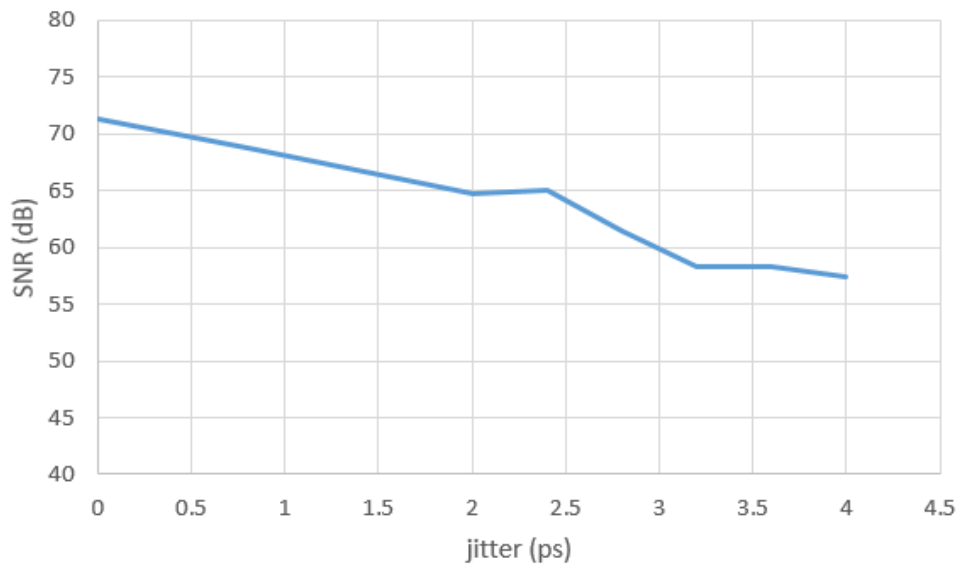


Figure 5.20: SNR vs jitter injected into the oscillator

## 5.6 Transistor Level Simulation

Using design insights obtain from Section 3, a TDC using cross-coupled ring oscillator is implemented using Cadence with 0.13 $\mu m$ technology. To start a TDC with a sampling frequency of 450 MHz is implemented. Figure 5.21 shows the timing waveform and output of the 450 MHz sampling frequency TDC with an equivalent analog input value of 0.5V. The first waveform shows the digital output (an average of 0.5), the second is the enable/disable output of the timing circuitry; third waveform is the output of the GRO; fourth waveform is the output of the delayed VCO1; finally the last waveform is the reference frequency.

The sample frequency of the TDC is then increased to 1 GHz. An 3.14 MHz input is passed through and the timing output is shown in Figure 5.22. The last waveform of Figure 5.22 is the pulse modulated output of the 3.14 MHz input sampled at 1 GHz. An FFT of the output is shown in Figure 5.23, which also shows a 2nd order noise shaping of 40db per dec.



Figure 5.21: Cadence timing waveform simulation showing digital output of 2nd order Sigma Delta TDC with a sampling frequency of 450 MHz
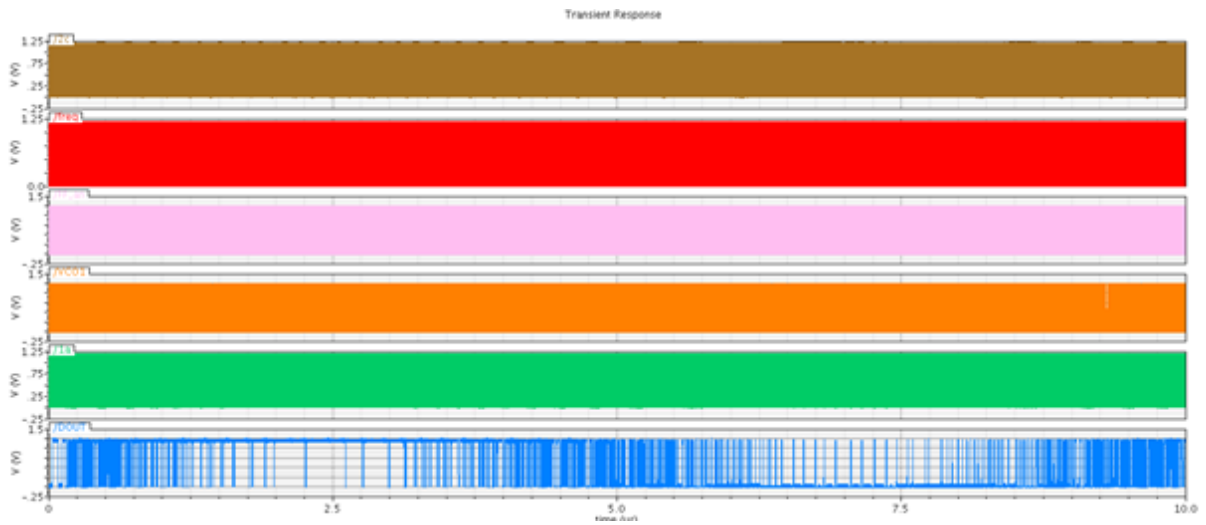
Figure 5.22: Cadence simulation of a 3.14 MHz sinusoidal signal at a sampling frequency of 1 GHz
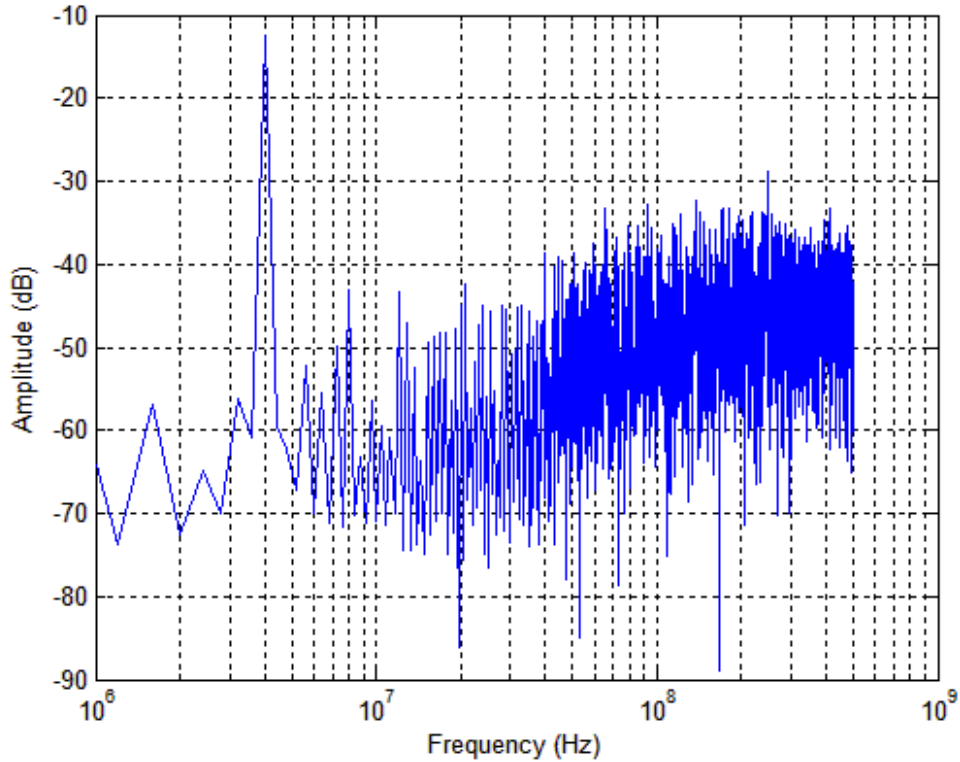
Figure 5.23: FFT output of TDC (with sampling frequency of 1 GHz) of an input signal at 3.14 MHz

Transient noise analysis on multiple runs of the TDC is performed. The outputs are shown in Figure 5.24, demonstrating a maximum deviation of 10 *ps*. Most of this jitter comes from the oscillator (see Appendix B). With a bandwidth of 3.14 MHz and OSR of 320, the jitter arriving from the oscillator, using equation B.9 is calculated to be around 18 *ps* [2] which is of the same magnitude as the simulated results. With the assumption that jitter is dominant noise in TDC we can used equation C.2 and calculated the SNR to be

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[2]This value is obtain from approximating the area under the phase noise plot of Figure 4.6

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approximately 55 dB[3].
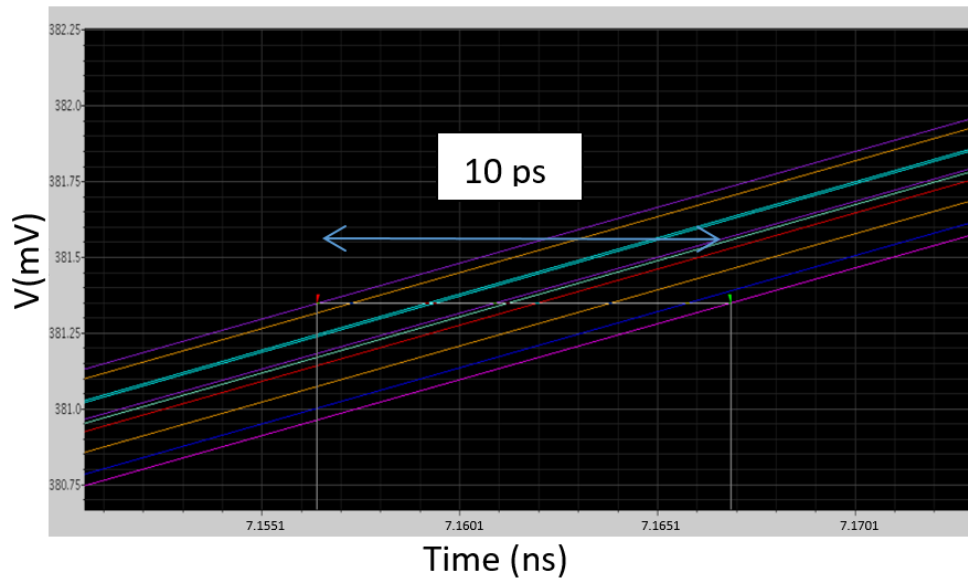


Figure 5.24: Multiple runs of digital outputs of TDC with jitter

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[3]using phase noise and offset values obtained from simulation

# Chapter 6

# Conclusion

The importance of ADC is becoming more crucial in telecommunication and sensor applications. ADC is starting to become the system bottleneck in performance due to reduction of supply voltage. One way to overcome the challenge of low-voltage design, due to technology scaling, is to process the signal in the time-domain. In ring oscillator based TDCs, the fundamental performance limiting factor is the accumulation of clock jitter from the VCO. The design on improvement of ring oscillator phase noise in a ring oscillator based TDC have been addressed in this thesis.

The key contributions of this thesis can be summarized as

- A phase noise model of low supply cross-coupled pair ring oscillator is presented.

- A 2-stage cross-coupled pair ring oscillators was fabricated. Phase noise measurements are performed with results that matches simulation and numerical values calculated using presented phase model.

- A second order $\Sigma\Delta$ TDC based on proposed cross-coupled pair ring oscillator is presented.

Experimental verification of 2nd order $\Sigma\Delta$ should be obtained in the future.

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# Appendix A

# Derivation of $\theta$, $\sigma_\epsilon$, power spectral density of phase noise

Referring to Figure 3.4, there are 4 quadrants in each cycle. Correlation coefficient $\theta$ captures the quadrant to quadrant correlation. Cycle to cycle correlation is then $\theta^4$. $\theta$ is [14]:

$$\theta = \frac{E((\tau_2 - E(\tau_1))|\tau_1)}{\tau_1 - E(\tau_1)} \tag{A.1}$$

$\tau_1$, $\tau_2$ are the two-quarter periods for Q1, Q2, the first two quadrants. $E(\tau_1)$ is the expectation or mean of $tau_1$ [14] and $E((\tau_2 - E(\tau_1))|\tau_1)$ is the conditional expectation of $\tau_2 - E(\tau_1)$, conditioning on $\tau_1$ [14]. Unlike [5], since we operate in low voltage supply where, with the range reduced, non-linear waveforms like $V_o^+$ in $\tau_1$, $\tau_2$ (see Figure 3.4) can be linearised and averaged. For example, in A.1, the term $E(\tau_1)$ (equal $d_{21} + d_{22}$, the sum of 2 durations in Q1) can be approximated as $b_{21}/\mu_{21} + b_{22}/\mu_{22}$ . To calculate this expression from Figure 2, $b_{21} = V_{bk}$, $\mu_{21} = average\ slewrate$ (SR). From equation

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3.9 SR is $I_c^+/C$ (part comes $I_{load}$, part from $I_{driver}$). From Figure 3.5, $I_{load}$ is averaged as $V_o$ sweeps from 0 to $V_{bk}$, and when normalized, is $S_c V_{bk}$. $I_{driver}$, when normalized, is 1. Similarly, $b_{22} = A - V_{bk}$, and $\mu_{22}$, the average SR, is calculated from $I_{load} = (A - V_{bk})S_s$, and $I_{driver} = -1$.

Repeating the approximation and calculation for rest of the terms in A.1:

$$\theta = \frac{-(S_s(\frac{A-V_bk}{2} - V_bk) + 1 + S_cV_bk)}{S_cV_bk - 1 + S_s(A - V_bk)} \tag{A.2}$$

Similarly $\sigma_\epsilon$:

$$\sigma_\epsilon^2 = \left( \frac{V_{bk}\sigma^2}{\left(S_s\left(\frac{A+V_{bk}}{2}\right) + S_cV_{bk} - 1\right)\frac{I_{D_{ON}}}{2C}\right)^3} + \frac{(A - V_{bk})\sigma^2}{\left((S_c\left(\frac{V_{bk}}{2}\right) - 1)\frac{I_{D_{ON}}}{2C}\right)^3} \right) \tag{A.3}$$

$\sigma$ is the root mean square of the noise from $I_{load}$, $I_{driver}$.

Next, we sum quarter periods $\tau_1, \tau_2, ... \tau_n$ as $S_n$, where due to correlation and noise, $\tau_n = \tau_{mean} + \theta\tau_{n-1} + \epsilon_n$. Here $\epsilon_n$ is random noise, modelled as a stochastic process with a Gaussian distribution, having standard deviation $\sigma_\epsilon$, as given in equation A.3). $\theta$ is given in equation A.2. $\tau_1, \tau_2, ... \tau_n$ are quarter periods in Figure 3.4. They are random (due to noise) with mean $\tau_{mean}$. Substituting $\tau_n$ expression from above, we have $S_n$:

$$S_n = \theta\tau_n\left(\frac{1 - \theta^k}{1 - \theta}\right) + \epsilon_{n+1}\left(\frac{1 - \theta^k}{1 - \theta}\right) + ...\epsilon_{n+k} \tag{A.4}$$

The covariance [14] of exponentiated $S_n$, defined as $R_k = cov[exp(jS_n), exp(jS_{n+k})]$, upon substitution of equation A.4, and subsequent fourier transformation, yields power spectral density ($psd$), with $f_o$ being the oscillation frequency:

$$psd\left(\frac{\omega_{offset}}{\omega_o}\right) = 10\log\left(\frac{1 - r^2}{f_o(1 + r^2 - 2r\cos\left(\frac{\omega_{offset}}{\omega_o}\right))}\right) dBc/Hz \qquad \text{(A.5)}$$

$$r = \exp\left(-\frac{4\sigma_\epsilon^2 f_o^2}{2(1 - \theta)^2}\right) \qquad \text{(A.6)}$$

# Appendix B

# 2nd Order TDC Noise and Noise Transfer Functions

Equation B.1 represent the sinusoidal output of an oscillator where $\omega_c$ is the oscillator frequency.

$$S_{osc}(t) = cos(\omega_c + \Delta\theta(t)) \tag{B.1}$$

$\Delta\theta(t)$ is the random phase fluctuation from the noise of the oscillator. The spectral density of $\Delta\theta(t)$ is denoted as $\Delta\theta(f)$. By assuming the phase fluctuation is small, $\Delta\theta(f)$ is then a narrowband modulation, which can be approximated by amplitude modulation [15].

An example is shown in B.1, Figure B.1a is the phase representation of the oscillator phase noise spectral density where the spectral density of the oscillator phase noise is represented as pairs of individual input frequencies with amplitudes $A_1(f_{m1})$, $A_2(f_{m2})$,

and $A_3(f_{m3})$ at $\pm f_{m1}, \pm f_{m2}$, and $\pm f_{m3}$ respectively. Looking at the pair of impulses with amplitude of $A_1(f_{m1})$ at $\pm f_{m1}$, substituting into B.1, and in time domain they become:

$$S_{osc}(t) = cos(\omega_c + A_1(f_{m1})cos(\omega_{m1}t)) \tag{B.2}$$

Under narrowband assumption B.2 becomes:

$$S_{osc}(t) = cos(\omega_c) - A_1(f_{m1})sin(\omega_{m1}t)sin(\omega_c t) \tag{B.3}$$

which consists of of the carrier at $f_c$ and two frequency impulses at $f_c \pm f_{m1}$. Similarly with impulse pairs $A_2(f_{m2})$ and $A_3(f_{m3})$ at their respective frequencies, under narrowband, we also obtain frequency impulses at $f_c \pm f_{m2}$ and $f_c \pm f_{m3}$. This is shown in Figure B.1b. Notice from Figure B.1a to Figure B.1b, phase variable $\Delta\theta(f)$ is transformed to amplitude variable $S_{osc}(f)$. Also, the envelope shown as dotted line in B.1b formed by the impulses at $\pm f_{m1}, \pm f_{m2}$, and $\pm f_{m3}$ has the same shape with the spectral density B.1a. This means we can, therefore, also use B.1b, amplitude, to indirectly represent the spectral density of the phase noise as well[15].
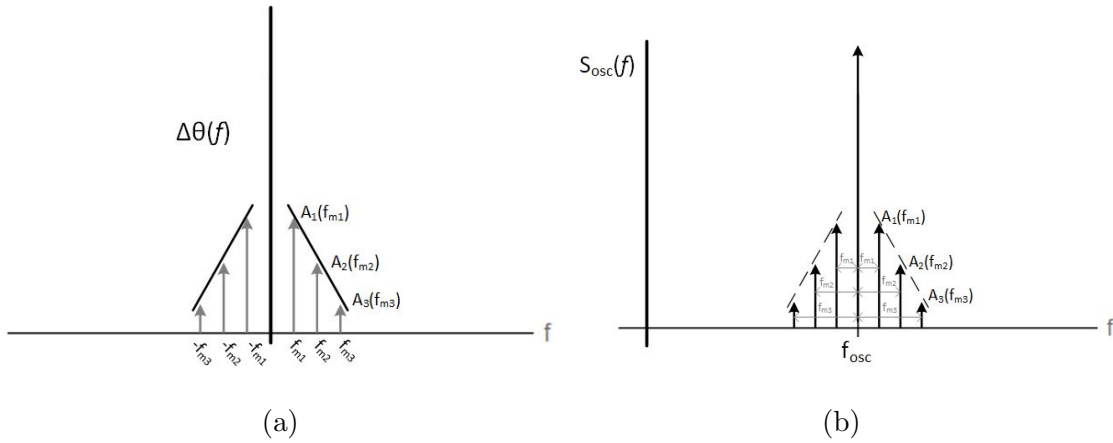
(a)            (b)

Figure B.1: a) Phase representation of oscillator phase noise spectral density, using frequency impulses b) amplitude representation of oscillator phase noise spectral density, shown by the envelope formed formed frequency impulse peaks

Now that we have express the relationship between of the phase noise spectral density in terms of phase and amplitude. We can add noise components and also modify the block diagram of the 2nd order sigma delta modulator in terms of phase to:
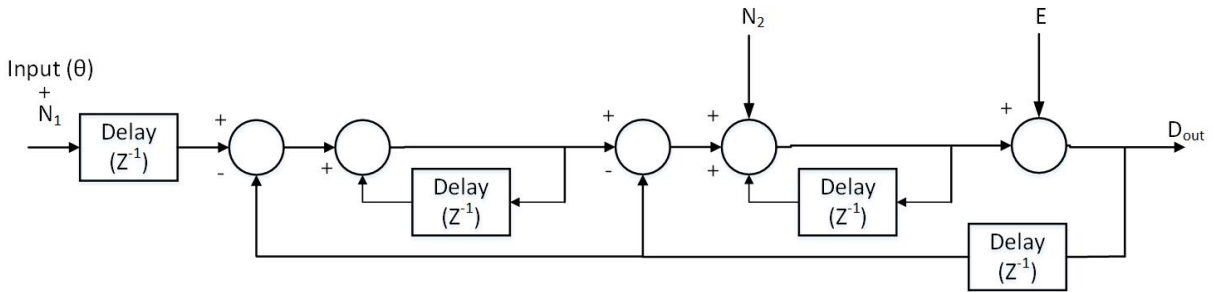


Figure B.2: The equivalent block diagram of 2nd Order TDC[1] with noise

$Input(\theta)$ is the phase representation of the input signal; $D_{out}$ is the output; $N_1$ is the noise of $VCO1$; $N_2$ is the noise of $VCO2/GRO$; and $E$ is the quantization error. In

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$z$-transform we get following noise transfer functions:

$$\frac{D_{out}}{N_2} = \frac{1/(1-z^{-1})}{1 + \frac{z^{-1}}{1-z^{-1}} + \frac{z^{-1}}{(1-z^{-1})^2}} = 1 - z^{-1} \tag{B.4}$$

$$\frac{D_{out}}{N_1} = \frac{z^{-1}/(1-z^{-1})^2}{1 + \frac{z^{-1}}{1-z^{-1}} + \frac{z^{-1}}{(1-z^{-1})^2}} = z^{-1} \tag{B.5}$$

From noise transfer function of the oscillators B.4 and B.5, substituting $z = e^{j\omega T}$, transfer function B.4 and B.5 respectively becomes:

$$|H_{N2}(f)| = |1 - z^{-1}| = 2sin(\frac{\omega T}{2}) \tag{B.6}$$

$$|H_{N1}(f)| = |e^{-j\omega T}| \tag{B.7}$$

where $\omega$ is the frequency of the input in $rad/s$; $T$ is period of the sampling clock. A visual presentation of $|H_{N1}|$ and $|H_{N2}|$ is shown below:
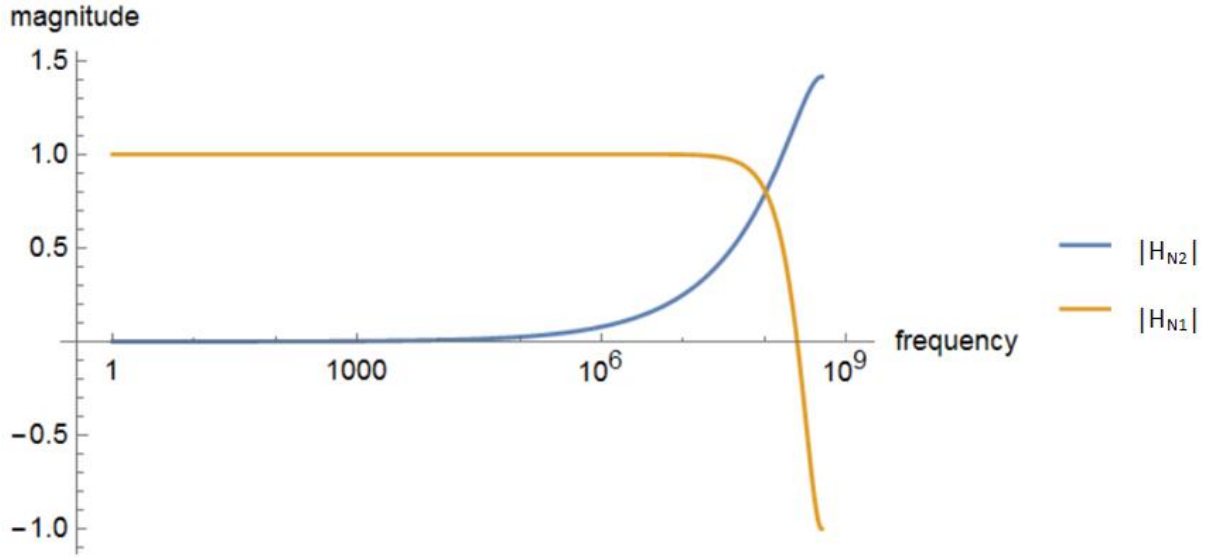
Figure B.3: Noise transfer function $|H_{N1}|$ and $|H_{N2}|$

From Figure B.3, we see that $|H_{N1}|$ acts like a low pass filter, while $|H_{N2}|$ has a first order noise shaping and acts as a high pass filter. This means at lower frequencies, phase noise from $VCO1$ dominates and at high frequencies $VCO2$ dominates.

Given an example bandwidth frequency of 3.14 MHz, low frequency noise coming from $VCO2$ is mostly cut off by $|H_{N2}|$ and is negligible. Meanwhile noise from $VCO1$ is passed through. Hence the calculated power spectral density of the TDC's noise due to VCO phase noise at a 3.14 MHz bandwidth, denoted as $S_{sys}(f)$, is approximated to

$$S_{sys}(f) = S_{osc}(f)|H_{N1}|^2 = S_{osc}(f) \tag{B.8}$$

where $S_{osc}(f)$ is the power spectral density of the oscillator phase noise[1]. We are interested

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[1] we can obtain the power sectral density $S_{osc}(f)$ by either integrating PSD function A.5 or find the area under a phase noise plot i.e. Figure 4.3-4.6

in the jitter arriving from the power spectral density of the oscillator, we can used the power spectral density referenced using offset equation A.5 and obtain the RMS period jitter of the oscillator using [16]

$$Jitter_{RMS} = \frac{\sqrt{2 * 10^{A/10}}}{\omega_o}(seconds) \tag{B.9}$$

A is obtained from integrating the phase noise power (dBc) over the frequency range of a phase noise plot (which can be obtained from A.5) and $\omega_o$ is the ideal oscillator frequency in $rad/s$.

# Appendix C

# 2nd Order TDC SNR for Dominant Timing Jitter

Assuming the timing jitter is the dominant noise in the TDC, the SNR of the TDC can then be described as [19]:

$$SNR = 10log(\frac{0.5 * T_{fs}^2}{\sigma_{jitter}^2 * OSR^{-1}})$$  (C.1)

where $T_{fs}$ is the full scale input, and $\sigma_{jitter}$ is the RMS jitter. Alternatively, in terms of phase noise, from [19], we have

$$SNR = 10log(\frac{f_{osc}^3}{8 * PN(f_{offset}) * f_{offset}^4 * OSR})$$  (C.2)

where $PN(f_{offset})$ is the phase noise, $f_{offset}$ is the carrier offset frequency, and $f_{osc}$ is the oscillating frequency.