Realization of Non-Volatile Memory in Amorphous Silicon Thin-Film Transistors

by

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A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Master of Applied Science
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2017

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

The integration of memory circuits in thin-film transistors (TFTs) is essential to extend the functionalities of large-area applications such as flat-panel displays, imagers etc. Intensive research is being conducted with the goal of producing high-performance memory devices for active-matrix backplane electronics. For example, a memory in a pixel circuit has the potential to reduce the refresh rate for display applications. This eventually leads to reduced power consumption which is vital for producing low-power displays. In addition, memory in pixel circuits can improve the fill factor of the display by its ability to hold the data without the need for a storage capacitor. Prior work has reported various TFT structures justifying the performance of the devices especially on their behavior under floating conditions. This work investigates the effect of continuous read cycles on the stability of low-temperature hydrogenated amorphous silicon (a-Si:H) memory TFTs prepared using the industrial standard back-channel etched (BCE) TFT process, as the topic yet to be explored systematically.

An engineered charge-trapping interface between the gate dielectric and the channel layer is fabricated to realize non-volatile memory. The performance of the devices was initially measured by comparing the transfer characteristics of the memory TFTs with conventional a-Si:H TFTs. The stability of the memory devices was measured under different stress conditions by varying the gate voltage and stress time. An emphasis was placed on the stability of the memory devices under floating and persistent read cycles as followed in display applications. The drain current was measured over various intervals of time for $\sim$60 days to track the degradation of the devices. The reliability of the memory devices was also measured.

From the analysis of the results, the charge-trapping memory TFTs demonstrated good

stability, large memory window, and better endurance. The charge retention of the devices under floating conditions was extrapolated and it showed a lifetime of ∼10 years. However, the charge retention of the memory TFTs exhibited a 50% decrease in lifetime under realistic persistent read bias conditions (∼5 years). This is possibly due to the instability of a-Si:H devices. This lifetime is subjected to change under different read voltage. Hence, the lifetime under continuous read cycles is extremely important to provide boundaries for expected memory lifetimes under normal display operating conditions.

Acknowledgements

The happiest task of my research is to thank my supervisor, Professor Manoj Sachdev who has made this happen in the first place by the opportunity for research and steering my research journey on the right track and guarding against drifting. He provided valuable inputs to build on and without his willingness to give his time and share his knowledge there would not have been any chance of my research work coming to fruition. Professor William Wong was instrumental in helping me understand device concepts better and his guidance and encouragement all through this work benefitted me immensely. It has truly been an honor knowing him as a mentor and unmatched privilege learning from him.

Next I would like to thank Dr. Czang-Ho Lee for spending his quality time to fabricate the device and circuit samples. Many thanks for his valuable time for discussion on my research work. Besides I owe a lot of thanks to Qing Li for his guidance and support. My interaction with him has kept my curiosity alive and kicking. I also acknowledge with thanks CMOS Design and Reliability (CDR) and Advanced Flexible Electronics (AFET) group members for their great contributions. I also appreciate greatly Govindakrishnan Radhakrishnan, Morteza Nabavi, Mellissa Chow, and Anthony Ho for clearing my sundry doubts. I would like to thank Phil Regier in the Department of Electrical and Computer Engineering, University of Waterloo for his technical support.

And, finally and immensely, I thank my parents and my family for their love and support.

Dedication

To my brother, Keshav!

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Chapter 1

Introduction

1.1 Memories

Semiconductor memory has always been a vital component and backbone of modern electronic systems from hand held devices to large supercomputers since its introduction in early 1970's. The data stored can be information that is processed in real-time or software programs or information that can be accessed by the machine at any point during the operation. During the early days, data were made up of huge magnetic cores. As the development of microelectronics continued, data were stored in tiny blocks of semiconductor arrays represented in bits. Today, the current estimation of digital data storage is 8 billion terabytes and its increasing rapidly for every two years. By 2020, data is expected to reach 44 zettabytes mainly driven by the internet of things and cloud based services (source:Crossbar Inc). From low-power microcontrollers, to connect devices, to large data centers, memory is everywhere.

1.2 Memory and its applications

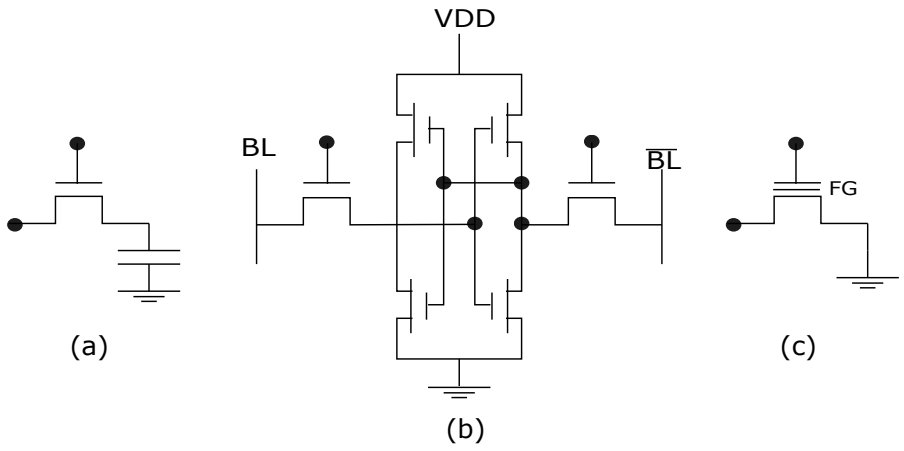


Figure 1.1: Memory circuit structures (a) DRAM (b) 6T-SRAM (c) Non-volatile flash

Semiconductor memories are classified as volatile or non-volatile. Volatile memories like DRAM (Dynamic random access memory) and SRAM (Static random access memory) need constant power supply to hold the data. On the other hand, non-volatile flash memories can retain information even when the power is off. The basic circuit structures of DRAM, SRAM, and flash based devices are shown in Figure 1. Compared to DRAM and SRAM, flash memories can scale to high capacity, be relatively cheap, and consume less power [1]. However, flash memories operate slowly compared to SRAM and DRAM. Nevertheless, its non-volatility has made flash based memory market vibrant and almost expected to be used in all mordern electronic equipments from consumer and automotive to computer and communications compared to it's volatile counterparts.

The semiconductor industry has had significant improvements since the introduction of flash devices. Non-volatile memory market is expected to garner $82 billion by 2022 [2]. Non-volatile memories are widely used in consumer applications, automotive, trans-

portation, enterprise storage, industrial etc. Flexibility is another developing area to bring affordable wearable electronics using thin-film technology. Thin film market has been a growing demand for applications such as solar cells, thin-film transitors (TFTs), light-emitting diodes, displays etc. With various emerging non-volatile memory technologies such as FERAM, RRAM, and PCRAM non-volatile memory market looks promising.

1.3 Amorphous silicon for large-area electronics

Although research works have developed various reliable materials for large-area electronic systems, the most common material of choice is hydrogenated amorphous silicon (a-Si:H) because of its unique properties and advantages. a-Si:H TFTs have been widely used as pixel switching devices in large-area flat-panel displays for several decades. The research documented in this thesis focusses on a-Si:H material as they offer the following advantages.

1. Si is a most abundant material in the earth. This allows the production-cost to be very less compared to poly-crystalline counterparts.

2. a-Si:H gives the feasibility of depositing uniformly across large-substrates. This property is vital for displays where pixel brightness needs to be uniform for wide flat-panel displays. Large-substrates can also be cut to produce efficient large-volume of small substrates.

3. a-Si:H can be deposited at very low-temperature (120°C) allowing the material to be used for flexible substrates like plastic.

4. Although organic materials are simple and easy to fabricate, the electron mobility($\sim 1 cm^2$/V.s) of a-Si:H TFT is one order greater than organic materials (Fig. 1.2). Inspite of this

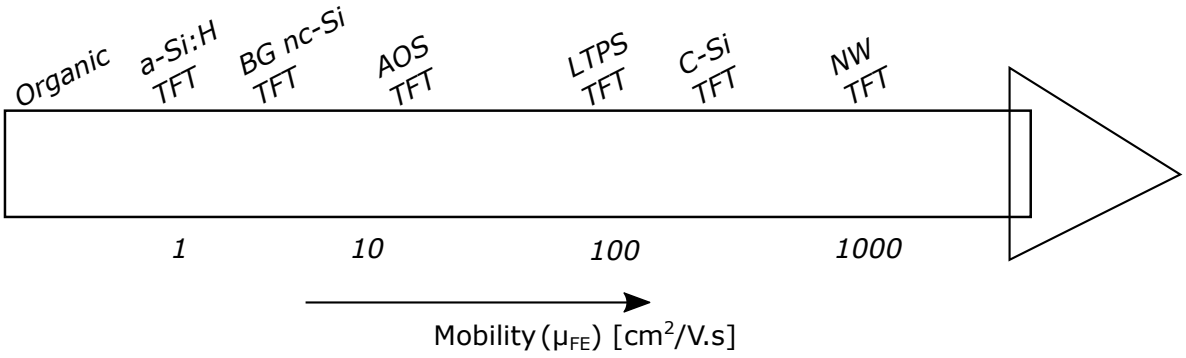


Figure 1.2: Comparison of mobility for various TFT materials

being smaller compared to polycrystalline and crystalline materials, this mobility is sufficient for a-Si:H TFTs to drive Organic Light-Emitting Diode (OLED) [3, 4] which is superior to the traditional Active Matrix Liquid Crystal Display (AMLCD) in terms of view angle, response speed, power consumption and cost.

5. a-Si:H TFTs also have a low leakage current of the order of $< 10^{-12}$ A due to the high resistivity of a-Si:H film. This prevents charge in the pixel capacitor to leak during the frame period. In addition, having a large ON/OFF ratio allows for larger grey scale making it attractive for display applications.

1.4 Motivation

Non-volatile memory using a-Si:H thin-film technology has been a subject of great interest for large-area electronics which could expand the functionalities of these systems. A memory device in each pixel circuit could lower the display refresh rate by storing the

information in the memory device. This could lead to reduced power consumption which is vital for display applications ranging from small flexible wearable devices to flat-panel display systems. In addition, integrating memory devices within the panel could allow the possibilities of demonstrating system on a panel (SOP). Hence, there is a vast demand for reliable non-volatile memory devices.

One of the basic requirements for flash based non-volatile memory devices is the stability and charge-retention (CR) of the memory devices. Research works have been carried out to implement non-volatile memories in large-area electronic systems using a-Si:H technology. However, one of the challenges of using a-Si:H TFT is the metastability effects. The threshold voltage (V_T) of a-Si:H TFTs shifts over time on applying gate bias. This disturbs the electrical characteristics of the devices leading to degradation of the device. For example, in a simple two-transistor (2-T) pixel circuit, the meatastability effects leads to the decrease in the OLED current over time requiring compensation circuits to maintain uniform OLED current.

In order to develop reliable non-volatile devices using a-Si:H technology, the effects of metastability have to be considered. This requires more precise characterization of memory devices depending upon their applications. However, such type of measurements are ignored. Hence, the goal of the research presented in this thesis is to demonstrate a reliable non-volatile device by an industrial standard process using a-Si:H and to investigate its impact under realistic operational conditions followed in large-area electronic systems. Such knowledge can be used to predict boundaries for expected memory lifetimes under normal display operating conditions.

Chapter 2

Amorphous Silicon Thin-Film Transistor

a-Si:H TFTs have been widely used as the switching elements in large-area electronics such as flat-panel displays and imagers since their demonstration in 1976 [5]. This chapter briefly discusses an overview on the a-Si:H materials property, TFT structure, and a-Si:H TFT operation and metastability.

2.1 Properties of a-Si:H

a-Si:H is generally termed as hydrogenated amorphous silicon. The introduction of hydrogen suppresses the defects present in an un-hydrogenated a-Si, which enables a-Si:H possible to be used in semiconductor devices.

a-Si:H is a disordered material having the short-range order as crystalline Si (c-Si) but lacks the long-range order (Fig. 2.1) [4]. The bond length (0.23 nm) and bond angle (109°) have a ∼10% spread and ∼1% spread, respectively, in the a-Si:H compared to crystalline counterparts, leading to weak bonds. In a-Si:H, abrupt band edges in c-Si extend into the

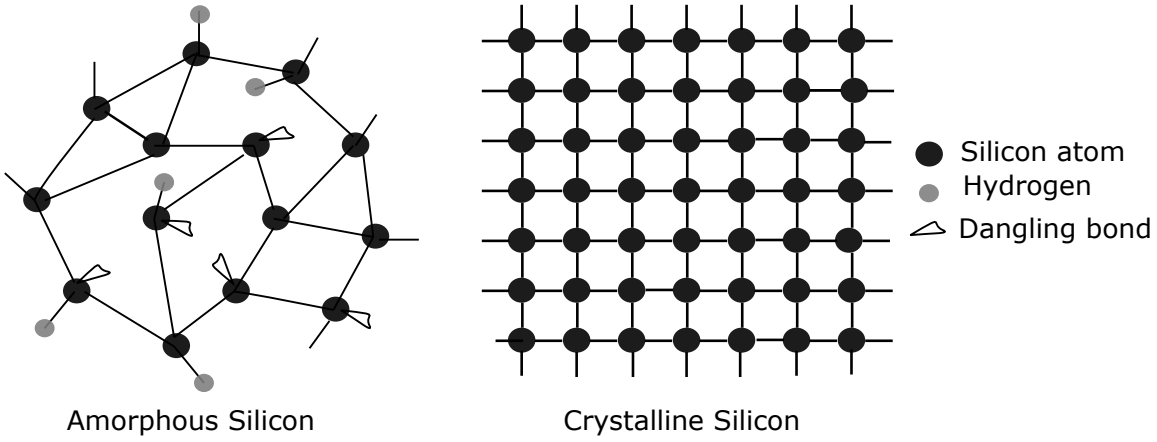


Figure 2.1: a-Si:H vs c-Si

bandgap (E_g) due to the changes in bond angle and bond length. Such changes create coordination defects (dangling bonds) which can lead to electronic states deep into the E_g (Fig. 2.2). About 10% of these dangling bonds are passivated by hydrogen and $10^{15}\sim10^{16}$ cm^{-3} bonds are not passivated leading to defects [6]. These defects affect the electronic properties such as conductivity and mobility of the material by controlling trapping and recombination.

2.2 Density of states in a-Si:H

The electronic properties of a-Si:H change depending on the distribution of the density of states (DOS). The DOS can be represented as shown in Fig. 2.2. The E_g, which is the separation between the valence band and the conduction band, is a main property of semiconductors. Within the E_g, the presence of states is due to the disorder of the material. These are localized states. As discussed above, the formation of weak bonds is due to the change in bond length and bond angle. This leads to band tails. The structural defects

form dangling bonds leading to deep states. The valence and conduction band extended states are similar to c-Si.

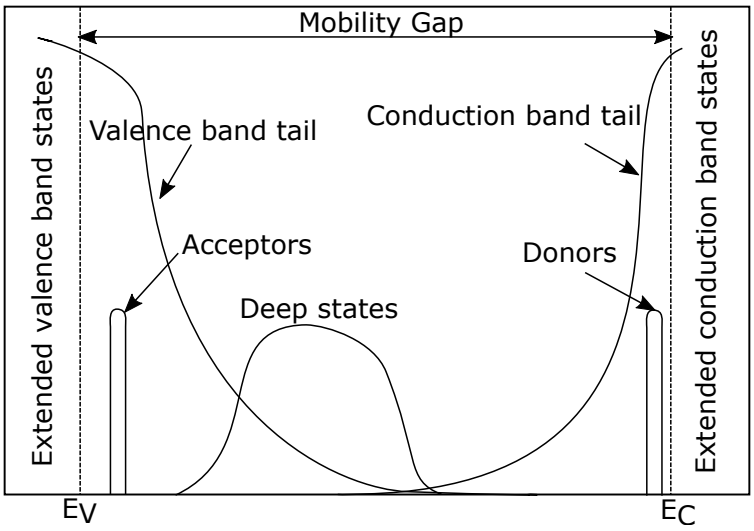


Figure 2.2: Schematic representation of DOS of a-Si:H

Band tails: The valence and conduction band tails have an exponential distribution extending 0.1-0.5 eV from their corresponding band edge [4]. Here, the slope of the band tails is determined by their characteristic temperatures T_v and T_c, for the valence and conduction band, respectively. The valence $N_v(E)$ and conduction $N_c(E)$ band tail density can be expressed as follows:

$$N_v(E) = N_{v0} exp(-E/KT_v) \tag{2.1}$$

$$N_c(E) = N_{c0} exp(-E/KT_c) \tag{2.2}$$

Deep states: The dangling bond defect can exist as three charge states,D^+, D^- and D^0 depending upon the Fermi level [4]. A dangling bong containing a single electron is

neutral (D^0). If the electron is removed or a hole is trapped it leads to positively charged dangling bond (D^+). A dangling bond with two electrons is negatively charged (D^-). From the widely accepted defect-pool model [7] [8], the dangling bonds minimize the formation energy. Thus the Fermi energy affects the distribution and DOS. The deep defects in a-Si:H change under different conditions. Many models have been reported for DOS following either gaussian or exponential distribution.

2.3 TFT device structure

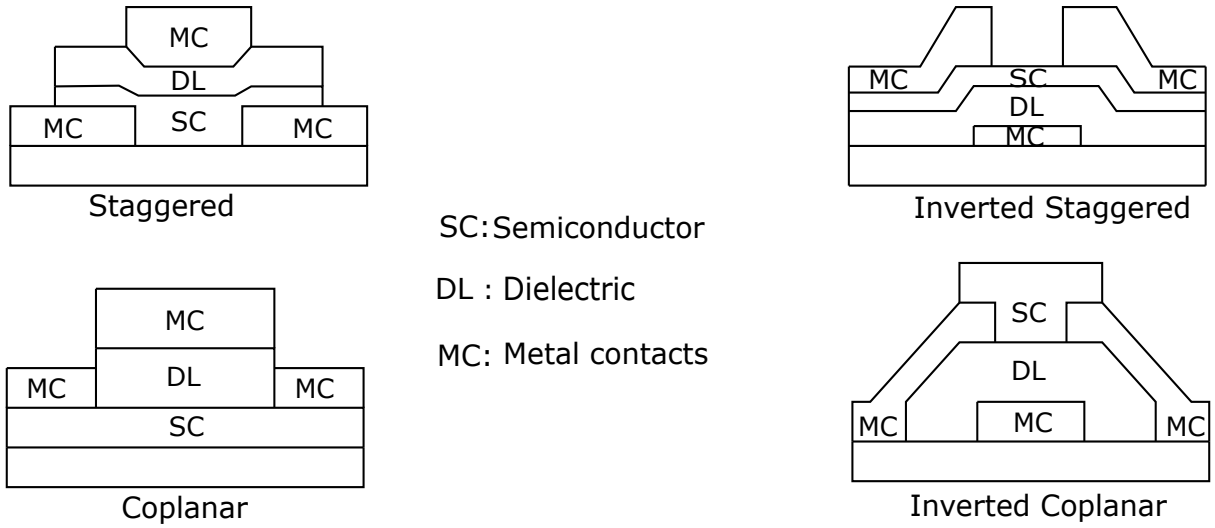


Figure 2.3: Various TFT structures

a-Si:H TFTs can be fabricated into a variety of structures namely staggered, coplanar, inverted-staggered, and inverted-coplanar as shown in Fig. 2.3. Each structure consists of a gate metal, gate dielectric, active layer, ohmic contact/metal contacts for source and drain. Among those structures, the inverted-staggered structure is the most commonly

used structure for research and in industry for manufacturing large-area electronics [9].

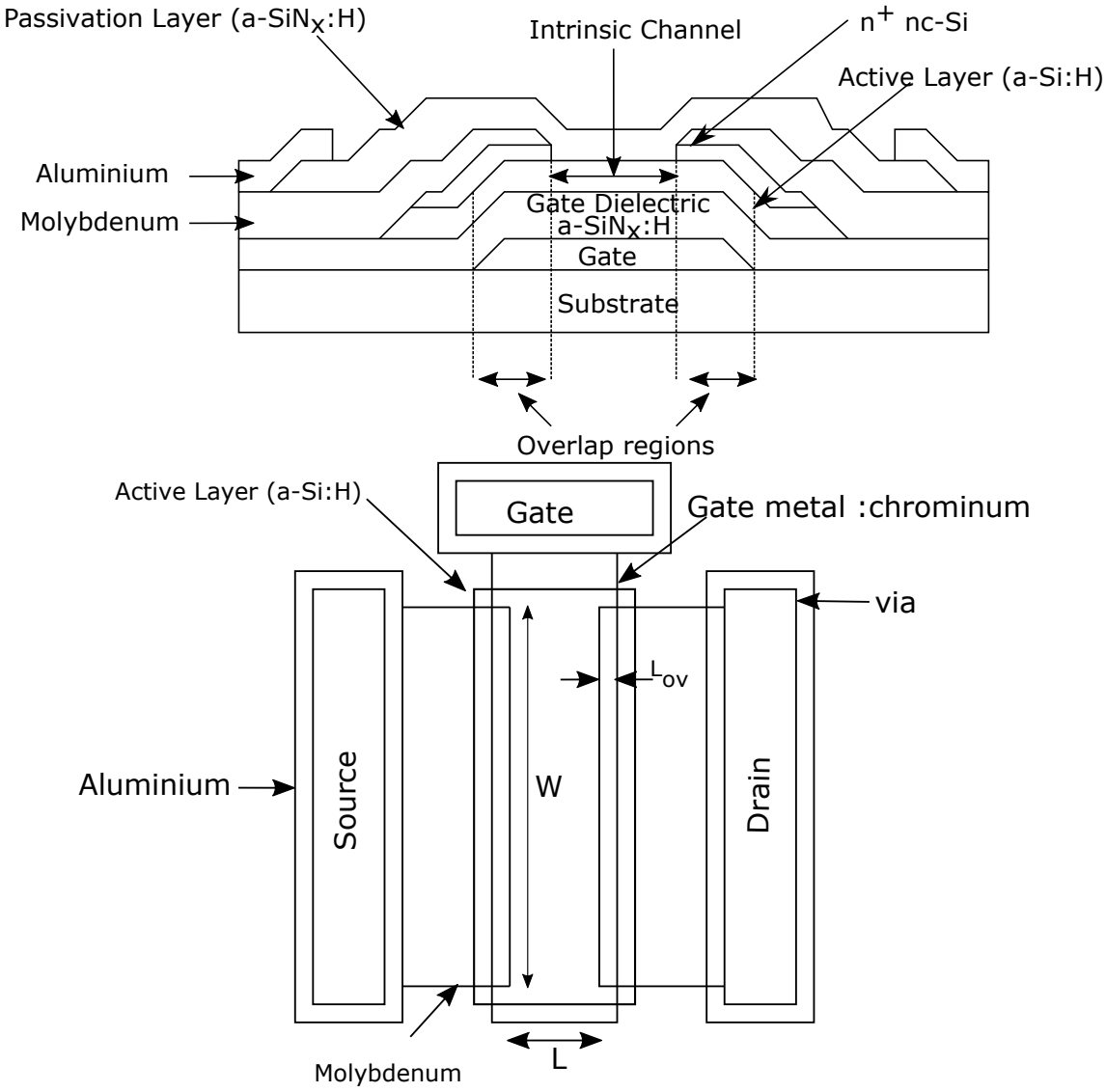


Figure 2.4: Inverted staggered BCE a-Si:H TFT a)cross-section b)layout

In the staggered structure, the gate and source/drain contact metals are placed on the opposite sides of the active layer whereas in the coplanar structure all the three contact

electrodes are in the same side of the active layer. Therefore, in coplanar structure, channel is formed very close to the ideal structure as assumed in most TFT models [10]. However, inverted coplanar structure leads to high series resistances because of the offsets between gate and source/drain terminals. This problem is avoided in staggered structure since there is an overlap between the gate and source/drain contacts and also giving the possibility of having larger contact areas. The dielectric and the active layers are deposited sequentially by plasma-enhanced chemical vapor deposition (PECVD) technique by controlling the flow of deposition precursor gases over the substrate with a pressure of a few millitorr. The main differences between non-inverted and inverted structure is that the active layer is first deposited followed by the gate dielectric and finally the gate metal. Here, the plasma used to deposit gate dielectric layer may affect the semiconductor interface leading to poor device characteristics. Hence, inverted staggered structure is highly preferred among the other TFT structures.

The inverted-staggered TFTs can be further divided into back-channel etched (BCE) and etch-stop (ES) TFT structures. In the ES TFT, we have a passivation layer on the top of the active-layer before depositing the source/drain contacts. This allows to have a thin active-layer. In BCE process, there is a possibility for the active layer to be affected. However, BCE is the most commonly used industrial standard process since it requires less mask process steps compared to its ES counterpart. All the TFTs used in this research are inverted-staggered structure using BCE process (Fig. 2.4).

2.4 Operation of a-Si:H TFTs

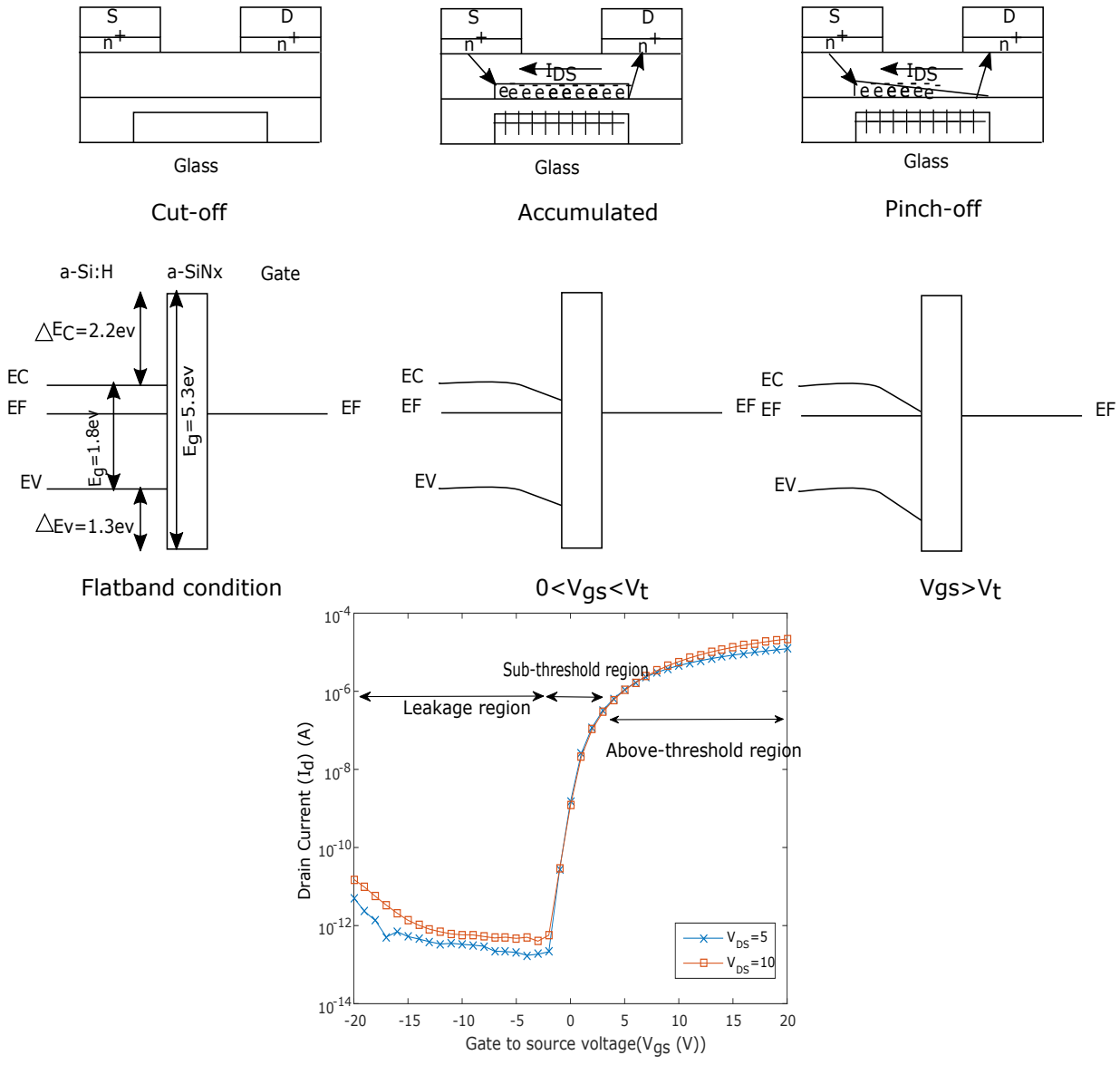
a-Si:H TFTs are n-type accumulation devices. a-Si:H TFTs have three different regions of operations; above-threshold region, subthreshold region, and leakage region as shown in

Fig. 2.5. The above threshold region is divided into linear region and saturation region. When gate to source voltage (V_{GS})=0, the channel is not formed and the transistor is off. The bands of the semiconductor do not bend and remain flat. When V_{GS} is applied, the electrons are accumulated at the a-SiH:/SiN_x interface and channel is formed. The bands of the semiconductor bends down showing the accumulation of electrons. When a small drain to source voltage (V_{DS}) is applied, drain to source current (I_{DS}) is generated. The TFT enters the subthreshold region. Due to the defects of a-Si:H devices, a major portion of the accumulated charges are trapped at the localized states, so the current conduction in a-Si:H is much weaker compared to MOSFETs. Beyond the above-threshold region, TFT acts like a ideal resistor with I_{DS} increasing for increase in V_{DS}. On increasing V_{DS} to large values, the channel is pinched off near the drain terminal and TFT enters the saturation region.

2.4.1 Above threshold

When a-Si:H TFT operates in the above threshold region, some part of the induced charges in the channel gets trapped at the localized traps. This leads to reduced mobility since only a part of the induced charge contributes to current conduction. Hence, the I-V equations for c-Si MOSFETS cannot be replicated for a-Si:H devices and are modified using RPI model [11]. Here, the impact of localized states is taken into account by modeling mobility in terms of gate voltage [12].

$$\mu_{FET} = \mu_n\left(\frac{n_{sa}}{n_{ind}}\right) \tag{2.3}$$



Transfer Characterisctics of a fabricated a-Si:H TFT

Figure 2.5: TFT operating regions

where n_{sa} is the sheet density of free charge and n_{ind} is the sheet density of the trapped charges in the localized states.

$$\mu_{FET} = \mu_n \Big(\frac{V_{GS} - V_T}{V_{AA}} \Big)^{\gamma} \tag{2.4}$$

where γ and V_{AA} are empirical parameters [11]. Hence, I_{DS} in the linear region of a a-Si:H TFT is given by

$$\boxed{I_{DS} = C_i \frac{W}{L} \mu_n \Big(\frac{V_{GS} - V_T}{V_{AA}} \Big)^{\gamma} (V_{GS} - V_t) V_{DS}} \tag{2.5}$$

I_{DS} in the saturation region is given by

$$\boxed{I_{DS} = C_i \frac{W}{L} \mu_n \Big(\frac{V_{GS} - V_T}{V_{AA}} \Big)^{\gamma} (V_{GS} - V_t)^2 \alpha_{sat} (1 + \lambda(V_{DS}))} \tag{2.6}$$

where $(1 + \lambda(V_{DS}))$ is used to model the channel length modulation (CLM) effect , since the effective channel length decreases in saturation region.

2.4.2 Subthreshold

In the subthreshold region, I_{DS} increases exponentially with increasing V_{GS}. The subthreshold current is given by

$$\boxed{I_{DS_{sub}} = I_{sub} \frac{W}{L} exp \Big(\frac{V_{GS} - V_{ST}}{SS} \Big)} \tag{2.7}$$

where V_{ST} is the onset of subthreshold region from the cut-off region. The subthreshold slope (SS) can be found by the change in I_{DS} by V_{GS}. This value represents how much is the change in current per decade. This value depends upon the defects states. For large defect states, the slope will be as steep as possible.

2.4.3 Leakage region

The leakage regime (I_l) of TFT operation is shown in Fig. 2.5. The TFT exhibited low leakage current in the order of 10^{-12} A. The leakage current is due to three components [11]; hole-injection-limited current, hole-conduction current, and electron-limited current. Since it is difficult to exactly build a precise model, an empirical model for I_l is given as

$$\boxed{I_l = I_{oL}\Big[exp\Big(\frac{V_{DS}}{V_{DSL}}\Big) - 1\Big]exp\Big(\frac{-V_{GS}}{V_{GL}}\Big) + \sigma_0 V_{DS}} \tag{2.8}$$

where I_{oL} is the zero bias leakage current, V_{DSL} and V_{GL} describe the dependence of V_{DS} and V_{GS} respectively. σ_0 considers the minimum resolution of measuring instrument [11].

2.5 Instability of a-Si:H TFTs

The V_T shift of a-Si:H TFTs is reported due to two reasons [13], [14]. One is due to the slow creation of defect states in a-Si:H [13]. Another mechanism is the charge trapping at the a-Si:H/Si:N interface or in the bulk of SiN gate insulator [14]. The principle difference between the two mechanisms is that the defect creation is a slow process of creation of extra states, which are in good communication with the a-Si:H conduction band. There is a slow increase in the density of defect states. On the other hand, charge trapping occurs when charges get trapped in the already existing states [14] in the gate insulator bulk or at the interface. These states are in poor communication with the a-Si:H conduction band.

2.5.1 Defect state creation

In defect creation mechanism, the electrons in the channel break the weak Si-Si bonds forming dangling bonds at relatively low gate voltage. These dangling bonds then trap

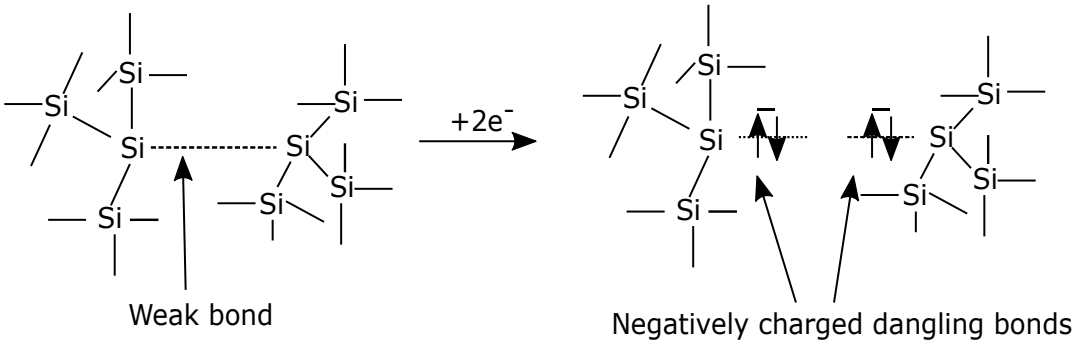


Figure 2.6: Defect creation in a-Si:H TFT under relatively low bias condition

electrons and become negatively charged defects as shown in Fig. 2.6 [15]. In this process, whenever the Fermi level changes in a-Si:H, the equilibrium density of dangling bonds changes. The Fermi level remains initially near midgap of intrinsic a-Si:H. A shift in Fermi level either higher or lower causes a positive shift in the V_T as these defect states need to be occupied to turn the transistor ON (Fig. 2.7).

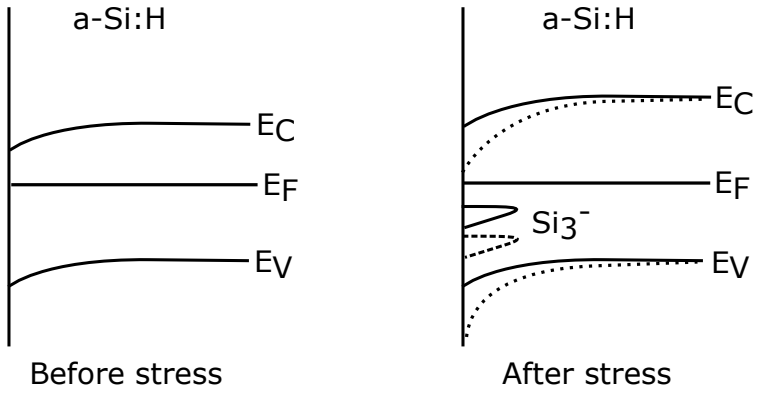


Figure 2.7: Mechanism of defect creation [16]

2.5.2 Charge trapping

Charge Trapping is another instability mechanism in a-Si:H TFTs due to the application of relatively high gate voltage. This trapping mechanism can be due to various processes as reported by Powell (Fig. 2.8) [17]. Fowler-Nordheim (F-N) tunneling ([2] in Fig. 2.8), the most common mechanism used to program/write charge-trapping memory devices can be eliminated since it needs high electric fields. Charge transfer can happen due to direct tunneling ([1] in Fig. 2.8) and trap-assisted tunneling ([3] in Fig. 2.8) at low electric fields, but requires high electric fields initially to reach the tunneling range. The main process responsible is the tunneling of electrons from conduction band to states at Fermi level and then subsequent redistribution of charges in SiN by hopping mechanism. The charges first tunnel to states in SiN and after certain time, the charges at the occupied shallow traps hop to the deep traps in SiN ([6] in Fig. 2.8).

The energy band-diagram of a-Si:H TFTs when the gate voltage during unbiased (V_{GS}=0) and biased (V_{GS} >0) conditions is discussed (Fig. 2.9). When the gate voltage is zero, band bending do not occur and the potential across the a-Si:H is zero. At this condition, if some of the electrons from the channel get trapped in the SiN, those electrons can get back to the a-Si:H channel due to the presence of empty states above the Fermi level. On the other hand, when a positive gate voltage is applied, the charge accumulates in the semiconductor to form a conductive channel. The electrons in the channel get trapped to the defect sites in the SiN. These electrons will have lower probability to be released from the trap state at a bias condition since there are no empty states below the Fermi level. Hence, this leads to a shift in the V_T. The ΔV_t through this mechanism has a logarithmic time dependence as given by [18]: $\Delta V_t = r_d \log(1+t/t0)$ where r_d is the density of traps [Nt] and t0 is a time-dependent supply function.

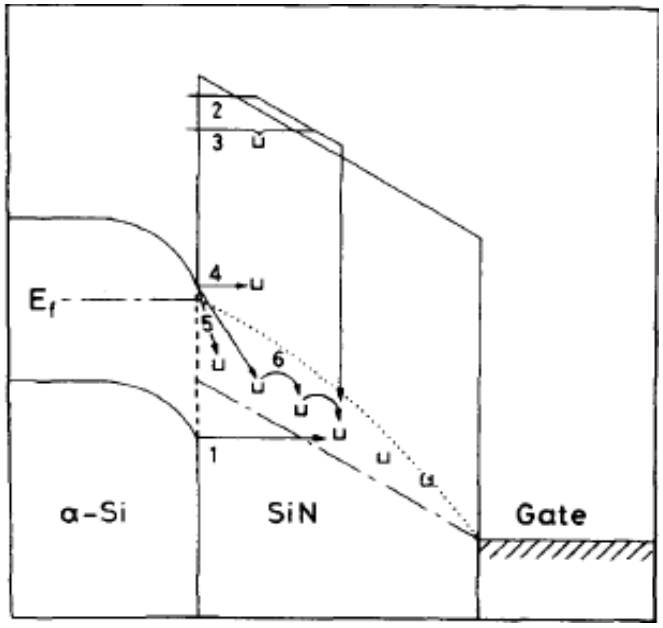


Figure 2.8: Charge trapping mechanisms [17]

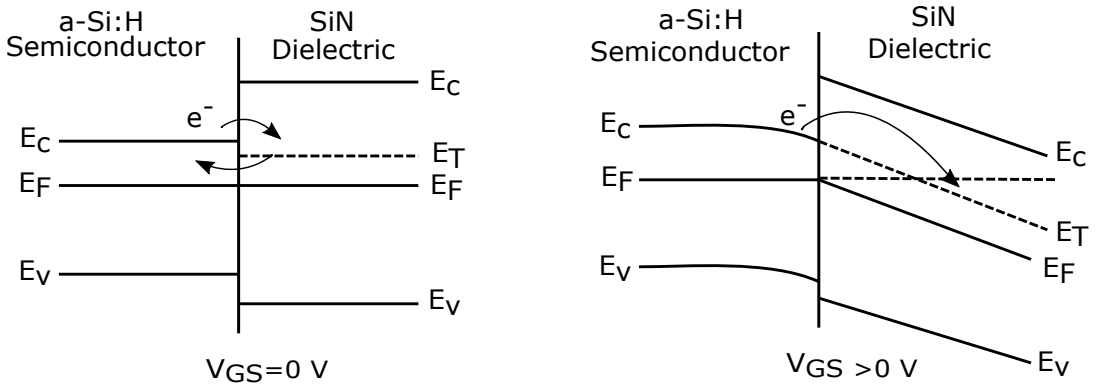


Figure 2.9: Energy band diagram of charge trapping mechansim

Chapter 3

Non-Volatile Memory Types and Prior Work

Non-volatile memories can be classified into the following types depending upon their functional properties based on the mechanism of operation:

1. Charge Storage
    - Floating-gate (FG)
    - Charge-trapping memory (CTM)
    - Nano-particles (NP)
2. Ferroelectric memory (FERAM)
3. Magnetic random access memory (MRAM)
4. Phase change memory (PCM)

5. Resistive random access memory (RRAM)

The charge storage type memory is the popular choice for implementation in a TFT process owing to its compatibility and simple fabrication process. We have implemented charge storage type non-volatile devices using a-Si:H thin-film technology in this thesis. Other memory types are being researched and have niche applications [1]. In this section, we will describe various charge storage memories in detail.

3.1 Charge storage non-volatile memory types

3.1.1 Floating-gate non-volatile memory

The FG non-volatile memory is the basic building block of flash memory proposed by Kahng and Sze in 1967 [19]. The FG device consists a conventional MOSFET configuration with a conductive polycrystalline silicon (poly-Si) between the tunnel and the control dielectric. This poly-Si has no contact and has the ability to alter the potential of the transistor by applying voltage at the control gate (V_{GS}).

The Fig.3.1 (a) shows the structure of a conventional FG memory device. The gate dielectric consists of a trilayer stack of control oxide/FG/tunnel oxide layers. The mechanism of operation is based on charge stored on the FG. Positive charges on the FG creates a negative shift in the V_T of the device and negative charges creates a positive V_T shift. Hence, by altering the charges from/into the FG, two different states of operation can be obtained. Since the FG is insulated on all the sides by dielectrics, the stored charges remain even when the power is off and hence its non-volatile. When a positive voltage is applied to the gate, the electrons from the channel tunnel through the thin tunnel oxide

(∼10 nm) and get trapped in the FG. These electrons act as a shield to the applied gate voltage, preventing current flow in the transistor making it "OFF". On applying a negative voltage, the stored charges on the FG are removed and they tunnel back to the channel making the transistor "ON".

3.1.2 Capacitance model of the FG

The capacitance model [20][21] of the FG device is shown in Fig. 3.1(b). In a conventional MOSFET, the voltage on the V_{GS} produces an electric field which is directly proportional to the thickness of the dielectric (E=V/D) where "D" is the thickness of the control oxide. However, in a FG device, this is not the case. This reason is due to the capacitance associated between the drain and the FG (C_{FD}). The potential of the floating gate (V_F) defines a coupling coefficient denoted by, α_{FG}. Considering source and substrate terminals as grounded, the potential at the FG is defined by

$$V_F = \frac{C_{FD}V_{DS} + C_{FG}V_{GS}}{C_{Total}} \tag{3.1}$$

where,

$$C_{Total} = C_{FD} + C_{FG} + C_{FC} + C_{FS} \tag{3.2}$$

$$V_F = C_{FG}(\frac{C_{FD}V_{DS}}{C_{Total}C_{FG}} + \frac{V_{GS}}{C_{Total}}) \tag{3.3}$$

$$V_F = \frac{C_{FG}}{C_{Total}}(\frac{C_{FD}V_{DS}}{C_{FG}} + V_{GS}) \tag{3.4}$$

where,

$$\boxed{\alpha_{FG} = \frac{C_{FD}}{C_{FG}}} \tag{3.5}$$

Thus the I-V equations of a floating gate device can be written modifying the conventional MOSFET I-V equations as:

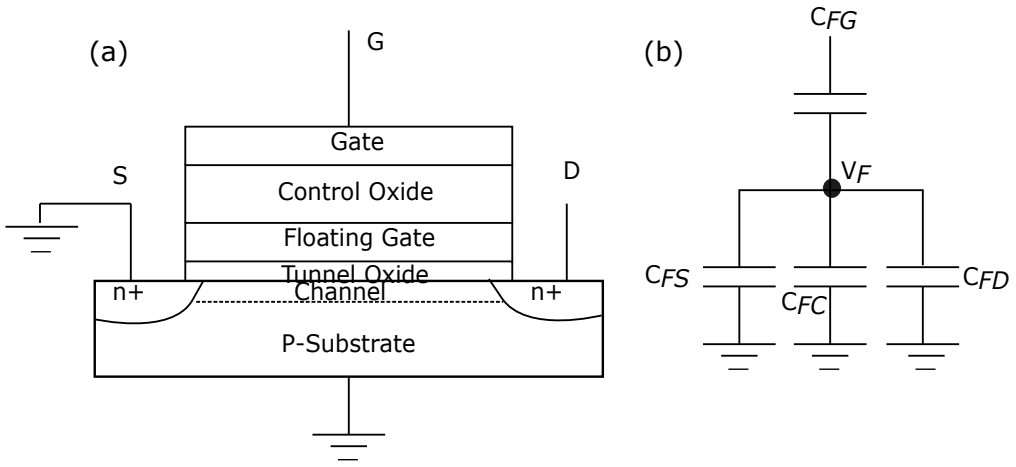


Figure 3.1: (a) The structure of a conventional FG memory device (b) Capacitance model of FG device

Linear region :

$$\boxed{I_{DS} = \beta[(V_{GS} + \alpha_{FG}V_{DS} - V_T)V_{DS} - \frac{1}{2}\frac{C_T}{C_{FG}}V_{DS}^2]} \tag{3.6}$$

Saturation region:

$$\boxed{I_{DS} = \frac{\beta}{2}\frac{C_{FG}}{C_T}(V_{GS} + \alpha_{FG}V_{DS} - V_T)^2} \tag{3.7}$$

where β and V_T are with respect to the control gate and not FG.

Some important observations can be obtained from Eq.(3.6) and (3.7)

1. The I_{DS} of a FG transistor is dependent on the drain voltage (Eq. 3.7). Hence, I_{DS} increases with increase in drain voltage and saturation will not occur.

2. Secondly, the FG transistor can conduct current even when $V_{GS}<V_T$ through the $\alpha_{FG}V_{DS}$ term in Eq. 3.6. Hence, can act as depletion device.

3. The capacitive coupling term strongly depends upon C_{FD} and C_{FG} terms only.

3.2 Charge-trapping memory

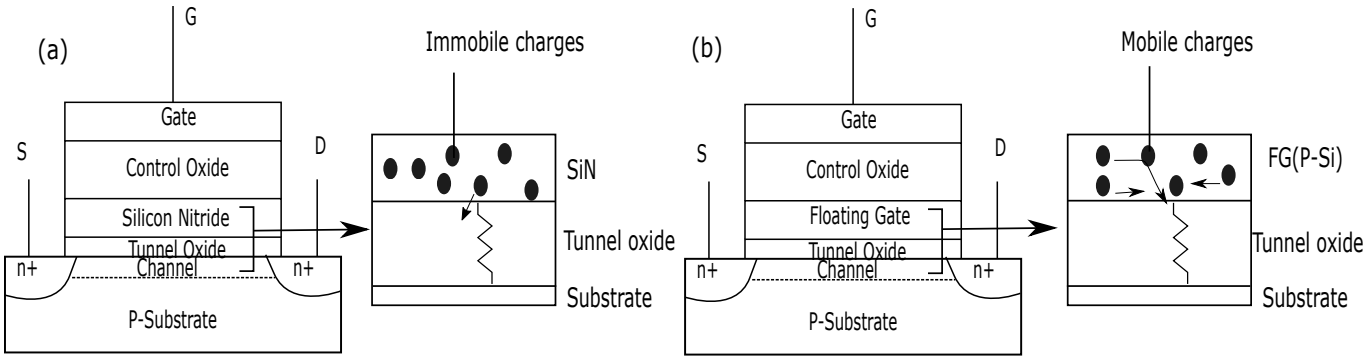


Figure 3.2: (a) SONOS device with immobile charges in the silicon nitride trap layer and (b) FG device with mobile charges in the poly-Si FG leading to charge loss

The CTM device is almost similar to that of FG device except in the CTM the charges are stored in the intrinsic traps of the charge-trapping nitride layer. The first CTM device was presented by Wegener et al. [22] in the form of metal-nitride-oxide-silicon (MNOS) structure. Here, the charges are stored in the isolated trap sites in the nitride layer by tunneling through the thin oxide layer. However, the charges stored at SiN_4 traps often suffered from charge loss and reliability issues. Hence a modified structure termed MONOS containing an additional silicon oxide layer as the blocking layer was introduced to prevent the leakage of defects through the gate. Later the metal was replaced a poly-Si and SONOS was developed as shown in Fig. 3.2(a).

SONOS devices offer better CR over FG devices. In FG memory devices, the trapped

charges are stored in conductive poly-Si layer and hence the charges are mobile. Here, in the presence of a single low resistance defect path in the tunnel oxide, the stored charges can easily leak out of the trap layer as shown in Fig. 3.2(b). This can be avoided when using CTM memories where the charges are stored in discrete trap sites and hence defects in the tunneling layer will not cause complete loss of stored charges from the trap layer [1][20].

3.3 Nano-particle based non-volatile memory

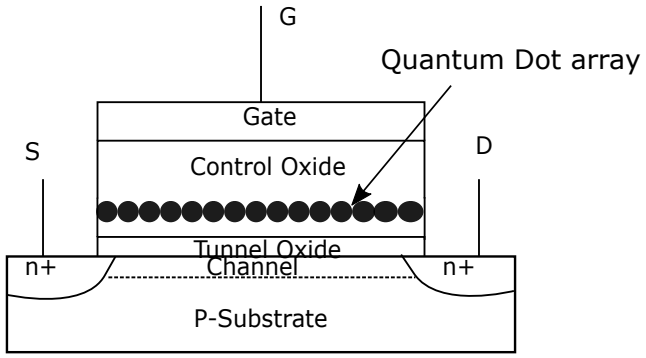


Figure 3.3: The nanoparticle based charge-trapping non-volatile memory device

As the dimensions of the devices are scaling down, there has been an interest in using quantum dots (QDT's) as a trapping media in non-volatile memory devices. The scaling down of transistors has brought some serious limitations in FG devices due to the leakage of trapped charges as we discussed above. The first non-volatile device employing nanoparticle was presented by IBM and is shown in Fig. 3.3. The quantum dots are generally made of group III-V semiconductors namely Si or Ge. They act as discrete FG trap sites that store

charges. The device operation is similar to that of FG devices with the trap sites being the nanoparticles instead of FG.

Although, the quantum dots improved on the scaling issues, it has some challenges. The interface between the nanoparticles and the surrounding dielectric plays an important role due to the stress between two dissimilar materials [23]. Poor fabrication can lead to charges getting trapped at interface which affects the non-volatility of the device. Secondly, as most of the nano-particles are semiconducting materials, they have bigger band-gap compared to insulators. This effectively reduces the band offsets which can affect the charge retention of the device.

3.4 Operations of charge-storage non-volatile devices

The operations of charge-storage non-volatile memory devices can be classified into programming/writing, reading and erasing. This section discusses each of them in detail.

3.4.1 Programming / Writing

Programming/Writing is a operation through which the state of the memory device is altered. This operation can be performed by either HOT carrier injection [24] or F-N tunneling [25] mechanism. Each mechanism has a different way of operation.

Channel hot electron injection (CHE) is a method in which the electrons get high energy to overcome the energy barrier and gets trapped in the charge-trapping layer. In this mechanism, a large voltage is applied to the drain and gate electrodes keeping the source and substrate grounded. This leads to impact ionization at the drain region leading to the generation of both majority and minority carriers. The majority carriers which

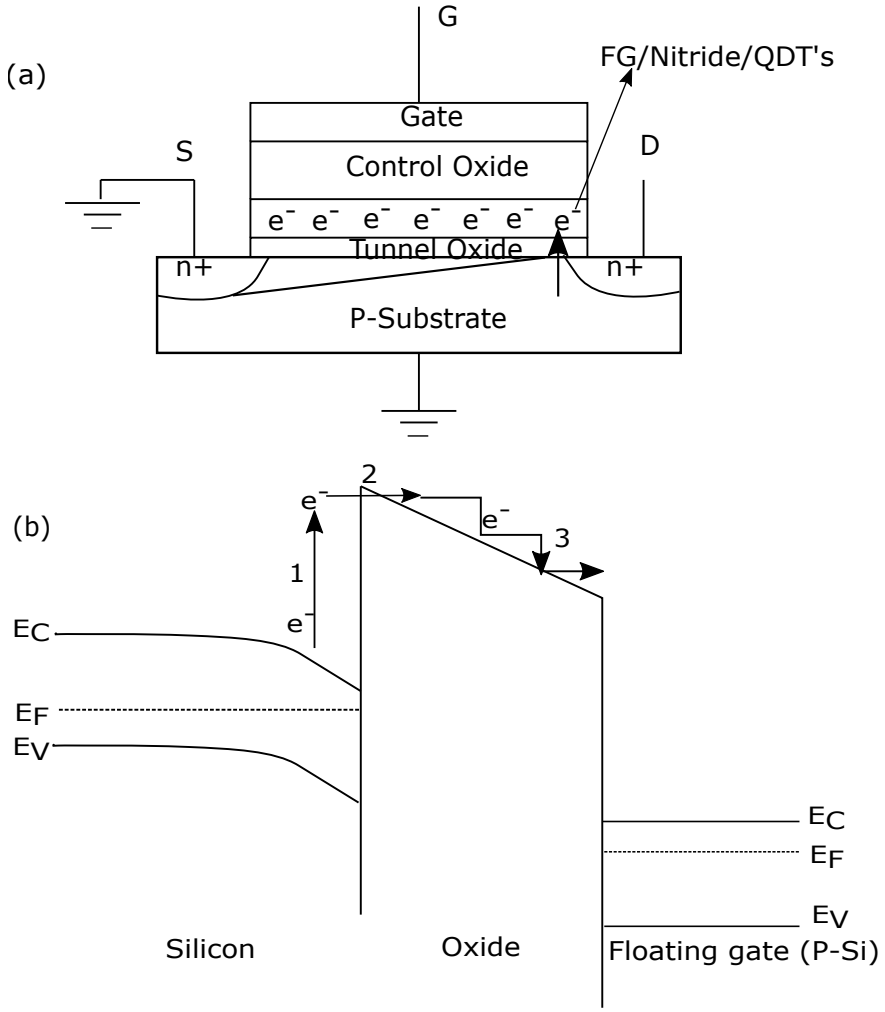


Figure 3.4: (a) CHE programming conditions and (b) Band diagram of CHE operation: (1) The electrons are excited to overcome the energy barrier by kinetic energy, (2) Only the electrons escaping from collision reach gate dielectric/channel interface, and (3) Injected electrons are collected by the FG

are highly energetic are collected at the substrate contact and form the substrate current. The minority carriers are collected at the drain. The large drain voltage induces a lateral electrical field between the source and drain. This electric field increases the energy of electrons making them hot. The high energy gained electrons overcomes the energy barrier and gets trapped in the charge-trapping medium by the vertical electric field from the gate and hence the name hot electron injection. This mechanism is shown in Fig. 3.4.

The high energy gained electrons will have the problem of collision. The electrons that overcome the collision retaining the high energy will only be injected to the charge-trapping media. Hence the charges injected using CHE mechanism is quite less. In addition, due to large drain-source currents the power consumption is high.

The most widely used mechanism for programming is F-N tunneling mechanism, which has been followed to program the memory devices in the thesis. This is based on field-assisted electron-tunneling mechanism [26].

F-N tunneling is based on quantum-mechanical tunneling through a thin potential barrier, by the application of an electric field at the gate under keeping the source, drain, and substrate grounded. The operation of F-N tunneling is shown in Fig. 3.5. When an electric field is applied at the gate, the thin oxide barrier bends and presents a triangular-shaped barrier. Due to the high electric field, the electrons from the conduction band tunnels through the thin tunneling layer. Here, the width tunneling barrier decreases with the applied electric field and the tunneling current increases with the electric field as more charge carriers tunnels through the barrier. Lenzlinger et al. [26] have reported the tunneling current density (J_{FN}) as

$$\boxed{J_{FN} = \alpha {E_{app}}^2 exp \frac{-\gamma}{E_{app}}} \tag{3.8}$$

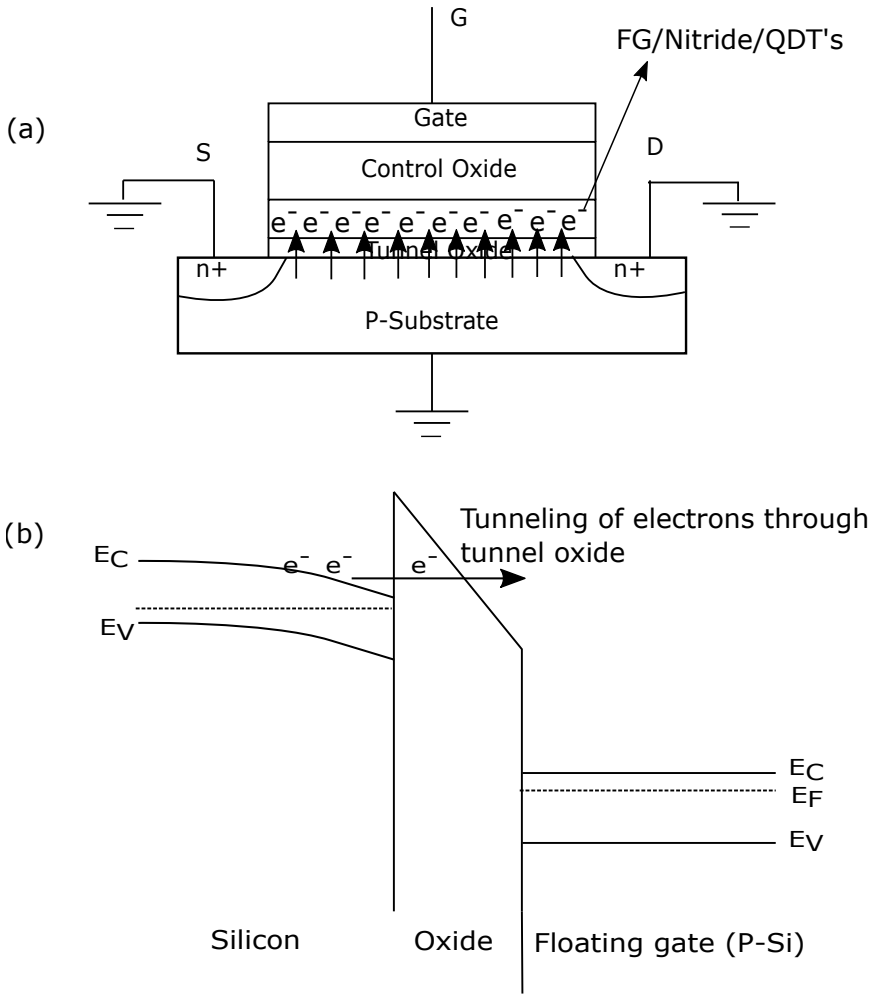


Figure 3.5: The mechanism of F-N tunneling

with

$$\alpha = \frac{q^3}{8\pi h \phi_b} \frac{m}{m^*} \tag{3.9}$$

$$\gamma = \frac{4sqrt(2m^*){\phi_b}^{\frac{3}{2}}}{3\eta q} \tag{3.10}$$

$$E_{app} = \frac{V_{app} - V_{fb}}{t_{oxide}} \tag{3.11}$$

where, h-planck's constant ϕ_b-barrier offset between Si/SiO_2 interface

E_{app}-applied electric field at the gate m-free electron mass(9.1×10^{-31} Kg)

m^*-effective mass of an electron η-$\frac{h}{2\pi}$

q-Charge of an electron(1.602×10^{-19}C) V_{app}-electric field across the oxide

V_{fb}-flat band voltage t_{oxide}-thickness of the insulator(oxide)

Equation 3.8 can be used as the tunneling current density for non-volatile memory devices. It should be noted that the influence of temperature has been ignored to calculate J_{FN}.

F-N method is simpler and more reliable compared to CHE mechanism. However, F-N tunneling have some drawbacks. Since the tunneling current depends upon the barrier thickness, this mechanism needs same thickness across various devices. But, due to process variations there can be slight change in electrical characteristics across devices, which might lead to different tunneling current. However, this is effect is negligible making this mechanism an effective way for programming.

3.4.2 Reading

Once programming is done, the next operation is to read the state of the device for memory cells. The devices that are programmed, exhibits a parallel shift in the V_T. This is because

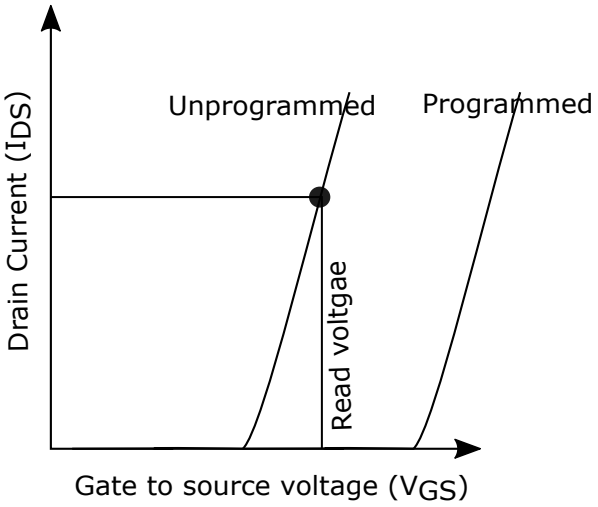


Figure 3.6: Read opeartion

the trapped electrons in the charge-trap layer (FG/Nitride/QDT's) act as a shield to the applied electric field. This causes an increase in the V_T to the right. Hence, when a V_{GS} less than the V_T of the programmed cell is applied, the programmed cells are "OFF" and conducts no current, whereas the V_T of the unprogrammed cells are "ON" and delivers high current (Fig. 3.6).

3.4.3 Erasing

Erasing is done in order to bring the programmed device back to its initial value. Erasing a non-volatile device can be done using either CHE mechanism, ultra violet (UV) radiation or F-N tunneling mechanism. The limitations faced by CHE mechanism for programming applies for erasing as well. Hence, CHE mechanism is ignored.

UV radiation imparts high energy to the electrons stored in the trap layer to overcome

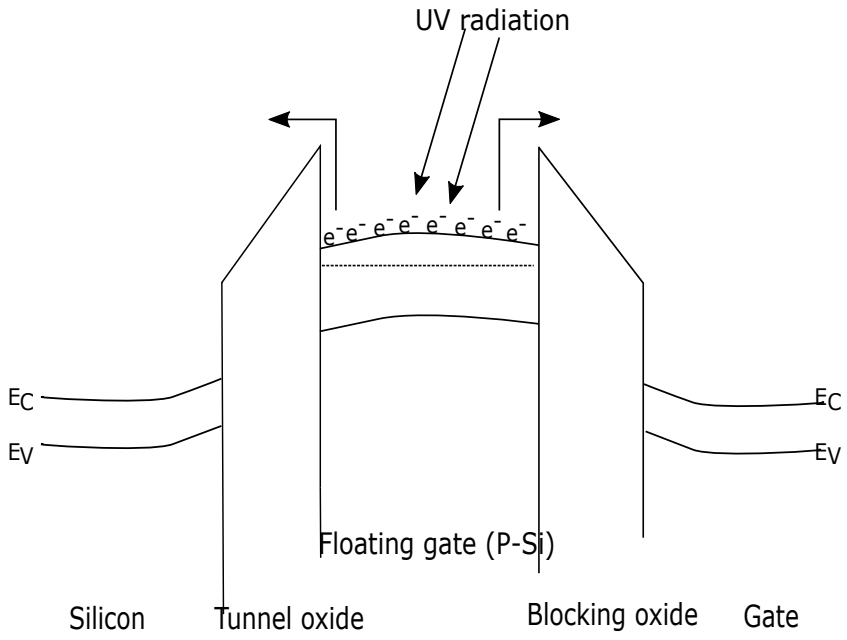


Figure 3.7: UV erasing mechansim

the energy barrier of the surrounding dielectrics as shown in Figure. 3.7. The removal of electrons from the trap layer, reduces the V_T of the device to its initial value. However, UV faces few drawbacks. Erasing cells using UV radiation is a slow process and can take minutes to erase the devices [27]. Secondly, upon erasing, the electrons from the trap layer overcomes the energy barrier to reach the control gate. At the same time, an undesirable stream of electrons coming from the substrate to the trap layer can neutralize the erasing mechanism making it inefficient [27]. This mechanism also faces selectivity problems. Erasing a single cell in an array is not possible while keeping the other cells unaffected. Finally, the need for a UV source makes it impossible to do in a laboratory environment.

Erasing using F-N tunneling works in the same manner as programming, expect the magnitude of the gate voltage is reversed (Fig. 3.8). When a high negative voltage is

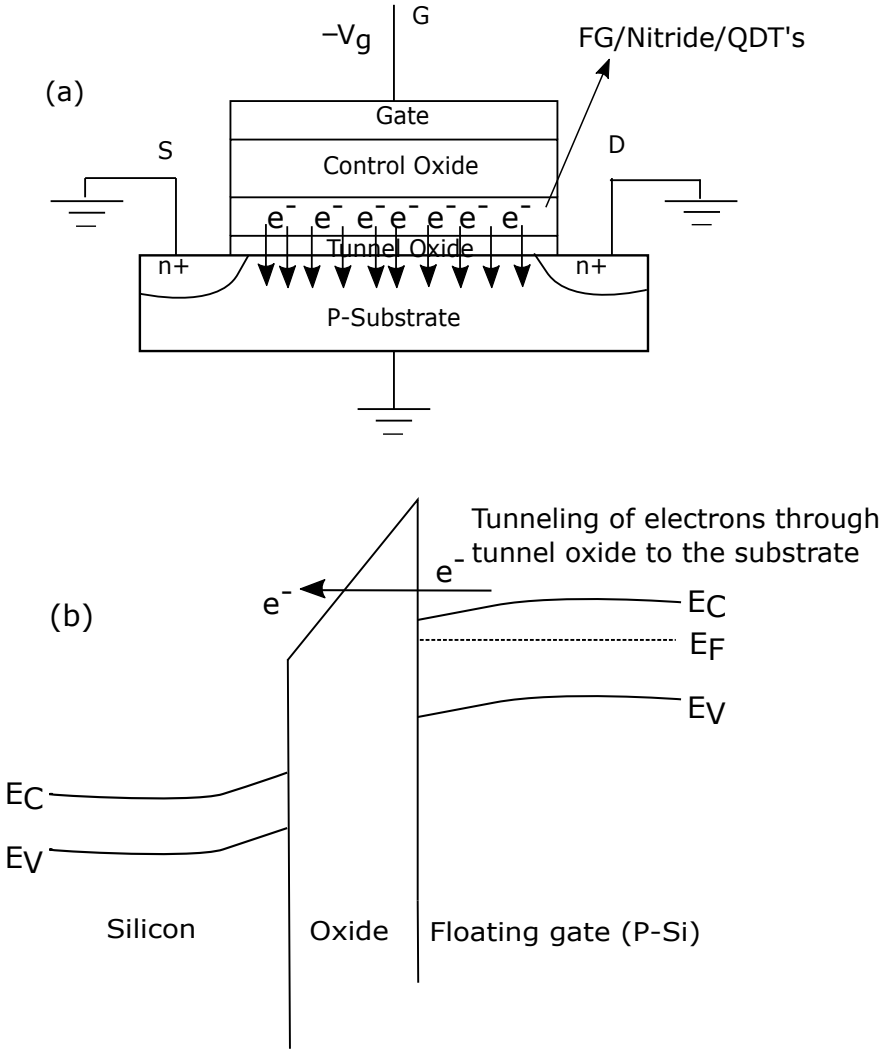


Figure 3.8: FN erasing mechanism

applied at the gate, the electrons from the trap layer tunnels through the thin tunneling layer to reach the channel region. This brings the V_T of the device back to its initial value. The mechanism is faster than UV radiation and also allows to reliably erase individual cells in a memory array.

3.5 Prior work

There have been reported charge-trapping non-volatile memory devices using a-Si:H TFT technology. Kuo et al. have presented a floating-gate a-Si:H TFT using an etch-stop process with a thin a-Si:H layer (7 nm) as the charge-trapping medium. In their implementation, CR characteristics under floating conditions were achieved for over 3,600 seconds [28]. However, the floating-gate memory TFT often suffers from the impact of drain-gate overlap capacitance (C_{ov}) [Eq.3.7]. The influence of C_{ov} leads to a ΔV_t dependence on the drain voltage. This effect has greater impact on emissive displays where the brightness of the pixel depends on the I_{DS}. This C_{ov} effect was explained by Huang et al. [29] where an engineered defect layer was introduced between the silicon nitride gate dielectric and the a-Si:H channel layer. They reported the memory behavior of the TFT with a CR of over 10 years under floating conditions. Choi et al. also demonstrated a hydrogenated-amorphous-silicon germanium (a-SiGe:H) non-volatile memory TFT using a trilayer oxide stack (OO_XO_N) charge-trap layer [30]. They showed that with a 20 % germanium content, 58% of the initial trapped charge remained even after 10 years compared to a device without germanium.

The previous research characterized the CR of the memory TFT based on floating conditions with an estimated lifetime of ∼10 years. However, in many applications such as flat-panel displays, when memory is integrated as a driver in a pixel circuit as proposed in [31], to reduce excess refresh cycles, the memory device is read periodically to display certain information. The driving scheme utilized to read can influence the stability of the memory device and thereby affect the CR and lifetime of the pixel under practical conditions compared to floating conditions. Hence, persistent read bias (PRB) is essential to determine the realistic lifetime of a memory device.

Chapter 4

Memory Behavior of Charge-Trapping Amorphous Silicon Thin-Film Transistor

This chapter discusses about the fabrication process and the characterization of the charge-trapping a-Si:H non-volatile memory TFTs. The fabricated memory devices posses good endurance, large memory window (M_W) and longer lifetime. The CR of the memory devices were measured under floating conditions and also under reading conditions. The details of the results are discussed.

4.1 Fabrication experiment

Bottom-gated a-Si:H memory TFTs with a charge-trapping layer were fabricated based on a standard back-channel etched (BCE) process. The fabrication flow of the memory TFT is shown in Fig.4.1. In our approach, the TFT is a back-channel etched structure, employing a 200 nm thick a-SiN_x gate dielectric. The TFT process started with sputtering of a 80 nm

Cr to pattern the bottom-gate metal. Next, a 200 nm a-SiN_x gate dielectric was deposited and followed by deposition of a thin 10 nm a-Si:H layer using 13.56 MHz plasma-enhanced chemical vapor deposition at 260° C. The thin a-Si:H layer was then completely dry-etched, to create a defective interface on top of the gate dielectric surface. A tri-layer of 20 nm a-SiN_x tunnel gate dielectric, 200 nm a-Si:H channel and 40 nm n^+ a-Si:H ohmic contact layers were deposited consecutively at 260° C. After patterning the TFT active area by dry etching, a 200 nm Al/Cr bilayer source/drain metals were sputtered and patterned. The n^+ a-Si:H was then dry etched using the source/drain metal as a mask to define the effective channel region followed by a gate contact opening. Here, 20-30 nm a-Si:H was intentionally over-etched to confirm complete n^+ a-Si:H etching. A reference TFT was also fabricated with a 220 nm single SiN_x gate dielectric layer (NH3/SiH4=20) for comparison (Fig. 4.2). The fabricated TFTs were annealed in vaccum at 180° C for 2 hours before electrical characterization.

4.2 Characterization of a-Si:H memory TFTs

4.2.1 Memory vs Reference TFT

Reference TFTs without any charge-trapping layer were prepared and compared with memory TFT. Fig. 4.3 shows the transfer (I_d vs. V_{gs}) characteristics of the memory and the reference TFTs. Both the TFTs are programmed and erased, with the source and drain nodes grounded, by applying a gate voltage (V_G) of +30 V and -30 V for 10 seconds, respectively. In the memory TFT, a +30 V bias was applied to the gate, to create a positive V_T shift. A -30 V bias was applied to negatively shift V_T resulting in a M_W of 3 V. The reference TFT shows a ΔV_t of 0.7 V upon programming due to the electrical instability

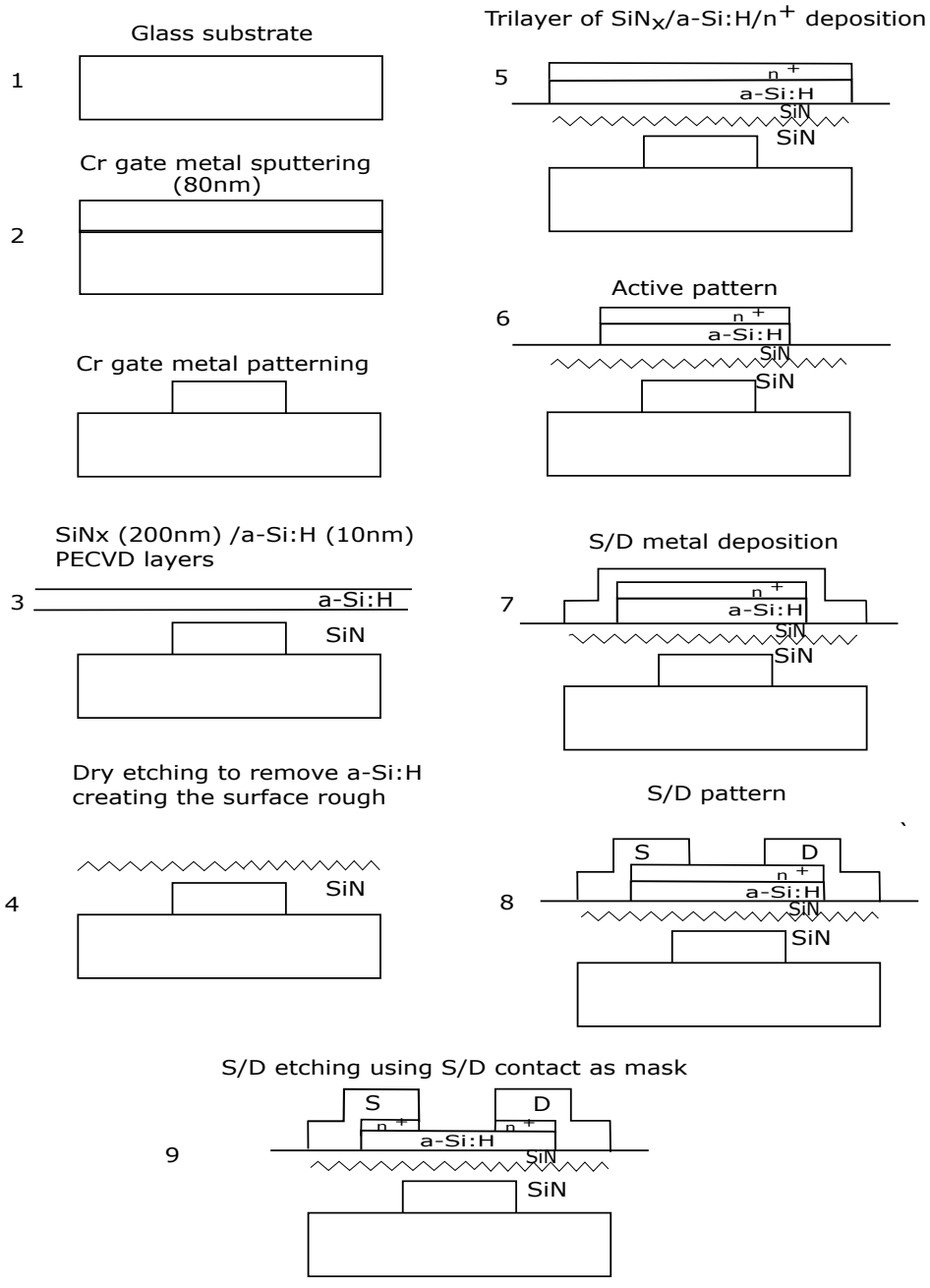


Figure 4.1: Fabrication flow of a-Si:H memory TFT

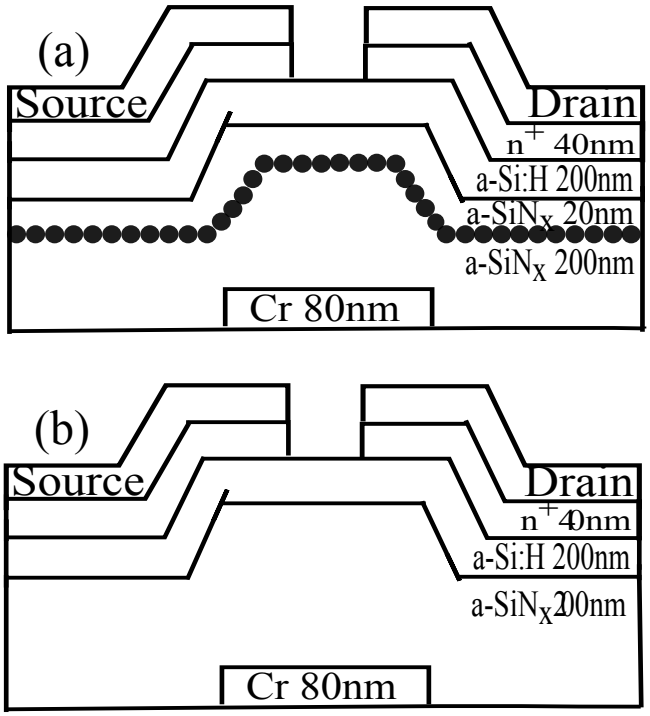


Figure 4.2: Schematic cross section of (a) charge-trapping TFT (not drawn to scale) , and (b) reference TFT (not drawn to scale)

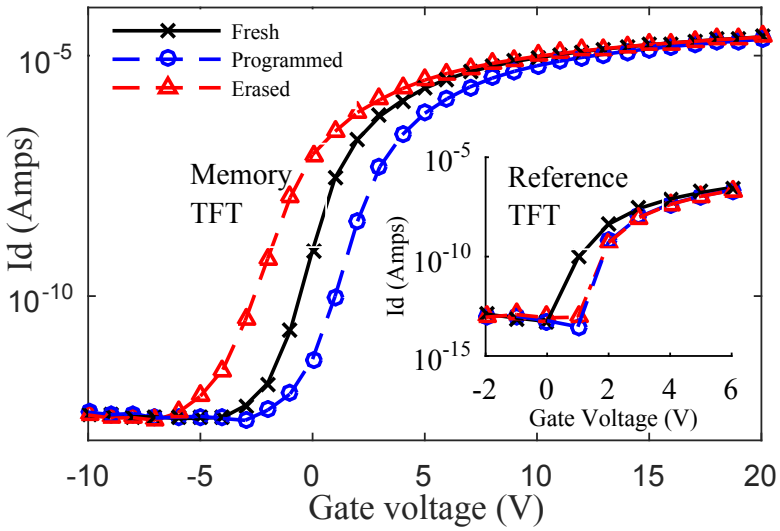


Figure 4.3: Transfer characteristics of the memory and reference TFT showing fresh, programmed and erased state. The program voltage =+30 V and erase voltage=-30 V for 10 s.

of a-Si:H TFT under constant gate bias [13]. However, on erasing, the V_T stays constant, negating the memory behavior. This behavior demonstrates the memory operation due to trapping and de-trapping within the engineered defect layer. The memory device shows good electrical properties with an I_{on}/I_{off} ratio of 10^8 and a SS of 500 mV/dec. The SS after programming as well as after erasing was found to be 700 mV/decade. This observation may be either due to the contribution of defect creation at the a-Si:H/a-SiN_x channel interface during the programming (erase) condition as well as the charge-trapping (detrapping) into (from) the medium. However, the SS did not change for both the conditions, suggesting the dominant mechanism to be charge-trapping compared to defect creation in the memory devices.

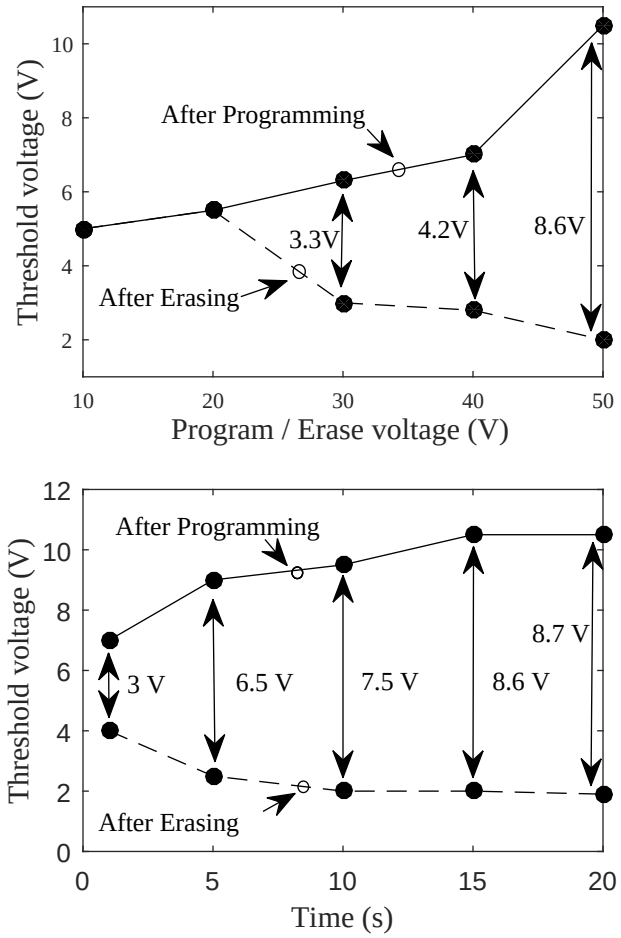


Figure 4.4: (a)The V_T shift variousfor programming and erasing voltage at a set time of 15sec. The M_W was observed for V_G greater than 20 V. (b) The time dependent ΔV_t for programming and erasing voltage at +50 V and -50 V, respectively. The M_W varied between 3 to 8.7 V

4.2.2 Programming/Erasing characteristics

Impact of different programming and erase voltages were measured on the memory devices. The programming and erasing mechanism were carried using F-N method as discussed in the previous chapter by grounding both the source and drain nodes and applying high voltage to the gate. Fig.4.4 (a) shows the V_T of the memory device as a function of programming and erasing gate voltages for a set time of 15 sec. The M_W was achieved starting from over +/- 20 V which allows the device to be able to program (positive gate bias) and erase (negative gate bias) at a suitable voltage. Here, the maximum M_W of 8.6 V was achieved at +/- 50 V. Hence +50 V for program and -50 V for erase were chosen as the default gate voltage in all our subsequent measurements to have a clear differentiation between the two states.

The M_W for various bias times under the programming and erasing voltages of +/- 50 V was also analyzed to find the influence of time on the M_W as shown in Fig. 4.4 (b). The M_W was observed to increase between 1 sec and 15 sec. The V_T shift after 15 sec began to saturate, suggesting the complete filling of traps within the defect medium.

4.2.3 Charge retention of memory TFTs

Data/Charge retention is one of a crucial factor which estimates the efficiency of a charge-trapping memory device. Here, the CR of the memory TFT was estimated based on floating and persistent read bias conditions.

Floating Conditions

The room-temperature charge retention characteristics of the memory TFT are shown in Fig. 4.6. While the device was kept floating, V_T was measured periodically for ∼60 days. The initial M_W after programming and erasing was 8.6 V and started to decrease with time due to the charge loss from the release of trapped charge. Memory lifetimes were determined through extrapolation [32] of the M_W and was calculated to be 4 V after 10 years with a charge loss rate of about ∼54%.

Persistent read bias conditions

The impact of PRB conditions on the memory device was subsequently analyzed by reading one bit of information, represented by state '0' and state '1'. The overall lifetime of the non-volatile memory device was calculated based on the driving scheme used in display applications [33]. A voltage less than the V_T after programming represented the state '0' and a voltage greater than V_T after erasing was state '1'. The measurements were carried out with the gate input signal (Inset of Fig. 4.6) produced using a Tektronix AFG3052C function generator. The maximum (ON) and minimum (OFF) amplitude of the signal was +5 V and 0 V, respectively. The period of the signal was set to 16 ms to simulate a 60 Hz refresh rate in a display. Considering a 64 × 64 pixel array, the programming phase was 'ON' for 250 µs and 'OFF' during the remainder of the period for the driving phase. The TFT was connected using a probe station to the measuring equipment and the entire test was carried out in the dark. The I_{DS} was converted to a voltage signal using a two-stage operational amplifier configuration (Fig. 4.5) and a DSA91304A digital signal analyzer oscilloscope was used to measure. At first, the TFT was programmed at + 50 V for 15 sec resulting in a ΔV_t = 6.6 V. The state '0' was read in saturation mode for 24 hours by

applying a V_{GS} of +5 V and a V_{DS} of +5 V. The TFT was erased by applying -50 V for 15 sec and state '1' was read in the same way for 24 hours.

The CR characteristics of the memory TFT under PRB conditions is also shown in Fig. 4.6. The results show that the V_T when reading state '1' increased more compared to the measurements under floating conditions (Fig. 4). On reading state '1', the gate is biased for every 16 ms at a voltage greater than the V_T of the device (inset of Fig. 4.6), due to erasing. It leads to the bias dependence instability issues of a-Si:H TFT [17],[13] thereby causing an increase in V_T . This eventually leads to a decrease in the M_W. Extrapolating shows that V_T crosses +5 V in about 5 years (Point A). Beyond this point the stored memory is lost as the V_T becomes comparable to the V_{GS}. This results in almost 50 % decrease in lifetime from measurements taken under floating conditions. The results demonstrate the negative impact of continuous read cycles on the device lifetime. The impact could be more severe with a device having a narrow initial M_W and the device lifetime is subjected to change with respect to the applied reading voltage. Table 4.1 provides a summary of our measurement results along with the recently published papers [28],[29],[30].

The M_W of a device is a function of various parameters such as dielectric thickness, applied electric field, and stress time. As apparent from the table, there is a wide ranging spread amongst these parameters reported by different groups. However, for a given dielectric thickness, the M_W is proportional to the applied electric field and stress time. For example, in [29], the stress time is in msec, but the thick dielectric induces small initial M_W despite high applied electric field. Similarly, [28] has stress time in seconds, but the thick dielectric and low applied electric field lead to very small initial M_W. The researchers in [30] achieve excellent initial M_W with msec stress time under very thin dielectric and high electric field.

Additionally, as illustrated in Fig. 4.4(b), we could achieve an initial M_W of 3 V for the

stress time of 1 second. Moreover, we believe that the stress time can further be optimized given application requirements. However, in our study we highlighted that high initial M_W is important for a memory device operating under realistic reading circumstances. For example, the lifetime of a memory device changes significantly from floating to PRB conditions.

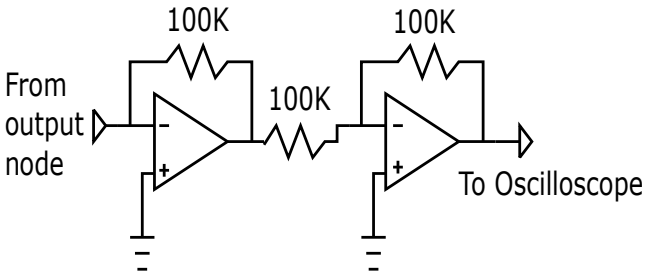


Figure 4.5: Two stage OPAMP configuration

4.2.4 Endurance/Reliability

Figure 4.7 shows the endurance characteristics of the memory TFT where the device was programmed and erased continuously for 50 cycles. Both the V_T for programming and erasing cycles was observed to increase while the M_W slightly decreased. This observation may result from residual charge that are trapped in the deep states of the control nitride. The erase voltage applied might not be sufficient to remove the residual charges that results in the small increase in V_T [14]. However, the M_W after 50 cycles was reduced by only 0.7 V without affecting the reading voltage. This result implies that the memory device is reliable for multi-time programmable applications.

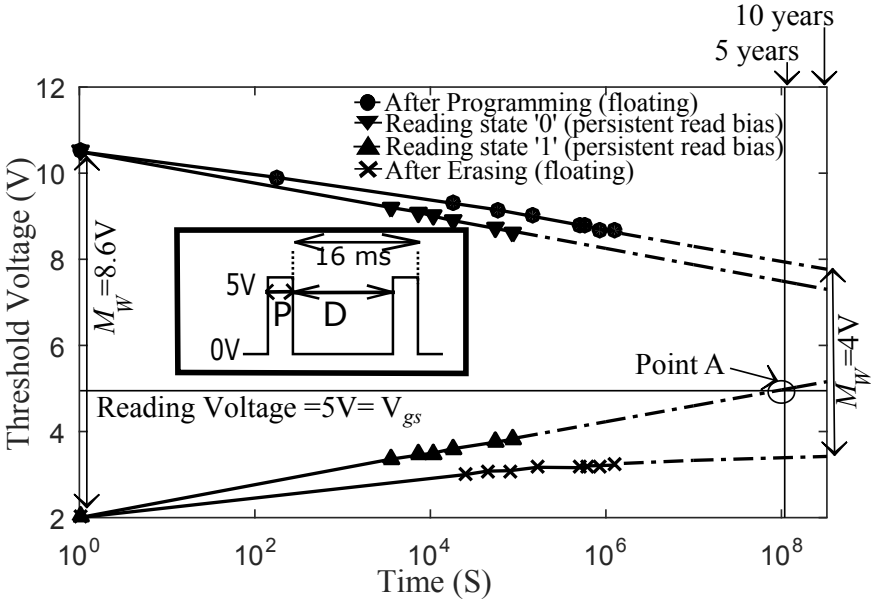


Figure 4.6: Charge retention characteristics of the memory device on the glass substrate at room temperature (27° C) measured during floating conditions and PRB conditions. The dotted lines are extrapolated from measured data points. The inset shows the timing waveform of the gate input signal followed for reading state '1' and state '0'. P represents the programming phase which is 'ON' for 250 µs and D represents the driving phase which is 'OFF' for the remaining period (16 ms). The memory is lost when $V_T = V_{gs}$ (at Point A)

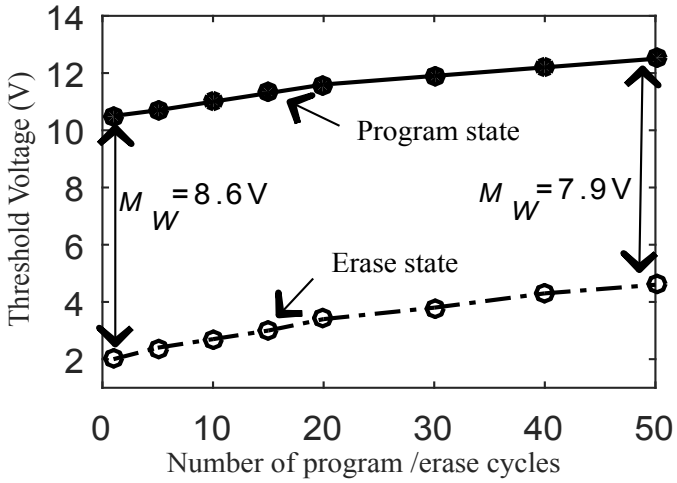
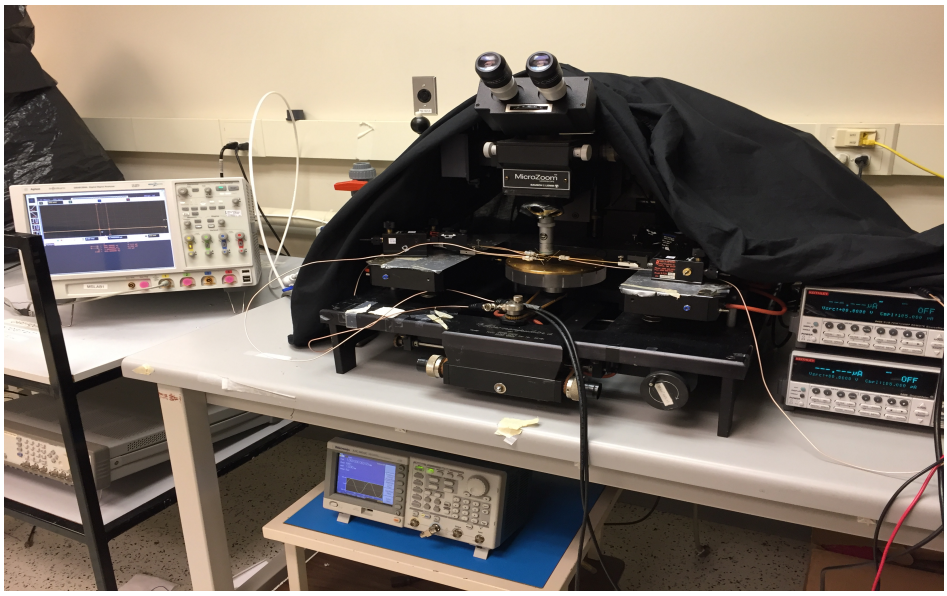


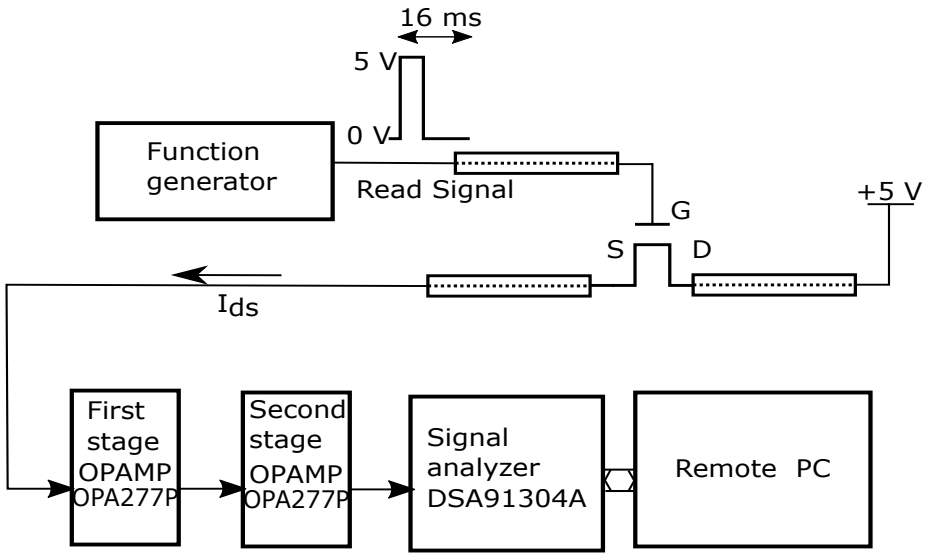
Figure 4.7: Endurance behavior of the memory TFT. The TFT was programmed and erased by applying V_G =+50 V and V_G=-50 V for 15 s, respectively

Table 4.1: Summary of results

Reference	Dielectric thickness (nm)	Applied electric field (V/m) P:Program, E:Erase	Stress time	Initial M_W (V)	CR	
					Floating	PRB
Present Work	220	P: 22.7×10^7 & E: -22.7×10^7	15 s	8.6	∼10 years	∼5 years
[28]	∼300	P: 3.3×10^7 & E: -3.3×10^7	1 s	0.7	∼3600 sec	-
[29]	110	P: 31.8×10^7 & E: -25.9×10^7	10 ms	2.5	∼10 years	-
[30]	37.5	P: -18.6×10^7 & E: 40×10^7	1 ms	6.75	∼10 years	-



(a)



(b)

Figure 4.8: The setup of the reading test on the memory TFT using a cascade summit 1200 probe station: (a) Photograph (b) Schematic

Chapter 5

Conclusion & Future Work

5.1 Conclusion

In this thesis, a non-volatile charge-trapping memory using a-Si:H TFT has been realized. The rapid increase in digital data has created a huge demand for storage devices in many applications such as industrial and transportation, enterprise storage, consumer electronics etc. In particular, the need for non-volatile devices are attractive due to its low-standby power compared to volatile counterparts. Although, non-volatile memories like flash face scaling challenges in CMOS technology, it is not a major limitation for large-area electronics such as displays and imagers. For example, integrating memories will benefit displays by reducing power consumption, improving fill factor and also expands the opportunities for system on a panel.

Here, a-Si:H was chosen to realize the memory devices because of its key advantages such as uniformity, low-cost, low thermal budget etc. compared to polycrystalline counterparts. The properties, different TFT structures and instabilities of a-Si:H material were discussed.

The various non-volatile memory devices were discussed along with the prior works. The limitations of conventional FG transistors for display systems due to the capacitance effects were also discussed.

Finally, an etched non-volatile memory structure has been demonstrated using an industrial standard back-channel etch process at low-temperature. The fabrication process is simple without any extra masks. The memory device exhibits large M_W ($\sim$8.6 V), good endurance and a long retention time ($\sim$10 years). The TFTs performance has been demonstrated under continuous read cycles as followed in display applications. The result exhibits the impact of read signal on the charge-trapping memory device which shows a 50% decrease in the lifetime of the device. This type of reading tests is vital for integrating memory devies in pixel circuits. The results would help predict accurate boundaries of expected lifetime of the memory devices compared to floating conditions.

5.2 Future work

The benefits of memory in TFTs has created a huge demand for developing efficient memory circuits and devices. Inspite of the developments, they still face challenges by needing extra process steps, poor device uniformity etc. The future work is to explore creating memory devices using standard process steps as used in a conventional TFT fabrication process with better reliability. The back gate in TFTs are an area to explore in creating memory circuits which coud expand the applications and functionalities of thin-film technology.

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