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Design strategy of two-dimensional material field-effect transistors: Engineering the number of layers in phosphorene FETs

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Thickness or the number of layers in 2D semiconductors is a key parameter to determine the material's electronic properties and the overall device performance of 2D material electronics. Here, we discuss the engineering practice of optimizing material and device parameters of phosphorene field-effect transistors (FETs) by means of self-consistent atomistic quantum transport simulations, where the impacts of different numbers of phosphorene layers on various device characteristics are explored in particular, considering two specific target applications of high-performance and low-power devices. Our results suggest that, for high-performance applications, monolayer phosphorene should be utilized in a conventional FET structure since it can provide the equally large on current as other multilayer phosphorenes ($I_{on} > 1\,\mathrm{mA}/\mu\mathrm{m}$) without showing a penalty of relatively lower density of states, along with favorableness for steep switching and large immunity to gate-induced drain leakage. On the other hand, more comprehensive approach is required for low-power applications, where operating voltage, doping concentration, and channel length should be carefully engineered along with the thickness of phosphorene in tunnel FET (TFET) structure to achieve ultra-low leakage current without sacrificing on current significantly. Our extensive simulation results revealed that either bilayer or trilayer phosphorene can provide the best performance in TFET with the maximum I_{on}/I_{off} of $\sim 2 \times 10^{11}$ and the subthreshold swing as low as 13 mV/dec. In addition, our comparative study of phosphorene-based conventional FET and TFET clearly shows the feasibility and the limitation of each device for different target applications, providing irreplaceable insights into the design strategy of phosphorene FETs that can be also extended to other similar layered material electronic devices. *Published by AIP Publishing.*
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I. INTRODUCTION

Silicon-based complementary metal-oxide-semiconductor (CMOS) technology has been standard in modern semiconductor industry for the past decades without significant contenders to compete. However, as consumer electronics are separated from power cords and become more diversified for various applications such as wearable sensors and health care services, demands for new materials in electronics have been dramatically increased. Two-dimensional (2D) layered semiconductors are a class of novel materials that can provide new functionalities in electronics such as flexibility and transparency due to their inherent thinness along with high carrier mobility.[1] Recently, 2D semiconductors such as molybdenum disulfide (MoS_2) or black phosphorus have been explored for future electronic device applications,[2–5] and they exhibited promising device characteristics such as high field-effect mobility ($\mu_{eff} > 1000\,\mathrm{cm}^2/\mathrm{V\ s}$),[6] large on current ($I_{on} \sim 240\,\mu\mathrm{A}/\mu\mathrm{m}$),[4] and large on-off current ratio ($I_{on}/I_{off} > 10^8$).[2] However, most 2D-material electronic devices were studied individually without discussing the significance of the number of layers, and therefore, comprehensive design strategies for different target applications are currently absent, although the number of layers in 2D materials is strongly correlated to bandgap, density of states, and gate efficiency, which are key parameters determining the overall device performance. Thus, in this study, we will mainly discuss the engineering practice to optimize the number of layers in 2D-material electronic devices for different target applications.

Here, we use the layer of black phosphorus or phosphorene for active material of field-effect transistors (FETs). The device characteristics are investigated by means of self-consistent, atomistic quantum transport simulations using tight-binding approximation. We have carefully chosen tight-binding parameters that can rigorously describe the band structure of multilayer phosphorene as well as monolayer,[7] in contrast to other previous studies where the electronic states were approximated with effective mass,[8] $k{\cdot}p$,[9,10] or limited tight-binding parameters tailored exclusively for mono- or bilayer phosphorene.[11–15] First, we focus on high-performance applications using a conventional field-effect transistor (FET) structure based on phosphorene, where we investigate the impact of channel thickness on various device performance such as on current, subthreshold behavior, and minimum leakage current. In general, for fast switching speed, large density-of-states (DOS) materials are favorable for the channel and multiple layers could satisfy such a requirement. However, at the

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same time, thicker channel can result in a poor gate electrostatic control, increasing the leakage current significantly. Therefore, both on and off states should be simultaneously investigated in designing high-performance 2D-material FETs to maximize the device performance.

Engineering tunnel FETs (TFETs) by varying the number of layers could be more complicated because trade-off exists between the thickness and the bandgap of 2D materials.[16] In principle, monolayer can provide the best switching behavior, but its on current can be significantly limited by the large bandgap, rendering it impractical. On the other hand, multilayer phosphorene can suffer from large leakage current and poor electrostatic control, resulting in small on-off current ratio (I_{on}/I_{off}), which is not desirable for low-power switching devices. Therefore, we carry out comprehensive engineering practices to optimize the performance of phosphorene TFETs by varying material and device parameters such as number of layers, power supply voltage, doping concentration, and channel length. Finally, we compare the best performance of each device structure to clearly identify the target applications of each device and also to provide valuable insights into the design strategy of 2D material transistors.

II. SIMULATION APPROACH

Electronic states of few-layer phosphorene are described with a tight-binding approximation using ten intralayer hopping parameters ($t_1^{\parallel} = -1.486$ eV, $t_2^{\parallel} = 3.729$ eV, $t_3^{\parallel} = -0.252$ eV, $t_4^{\parallel} = -0.071$ eV, $t_5^{\parallel} = -0.019$ eV, $t_6^{\parallel} = 0.186$ eV, $t_7^{\parallel} = -0.063$ eV, $t_8^{\parallel} = 0.101$ eV, $t_9^{\parallel} = -0.042$ eV, $t_{10}^{\parallel} = 0.073$ eV) and four additional parameters ($t_1^{\perp} = 0.524$ eV, $t_2^{\perp} = 0.180$ eV, $t_3^{\perp} = -0.123$ eV, $t_4^{\perp} = -0.168$ eV) for interlayer coupling, which can provide accurate band structure for multilayers as well as mono- and bilayer phosphorene.[7] We have used the recursive Green's function algorithm,[17] where tri-diagonal block matrix is required to find the numerical solution of the non-equilibrium Green's function (NEGF) simulation efficiently. For this, we have constructed a supercell, including two unit cells in y direction, to take into account the long-range interactions through $t_8^{\parallel}$ as shown in Fig. 1(a), which cannot be included if only the nearest unit cells are considered. By taking the supercell, the first Brillouin zone is reduced as shown in Fig. 1(b) due to zone folding, where Γ point is overlapped with the Y point of the unit cell (denoted as Y_0) and X point with the S point of the unit cell (S_0). The consequent band structures of mono-, bi-, and tetralayer phosphorene are shown in Figs. 1(c)–1(e) and the density of states (DOS) of the same materials are numerically calculated in Fig. 1(f). In this study, we have explored mono- to pentalayer phosphorene for the transistor applications, and their bandgaps and effective masses are shown in Table I.

Transport characteristics of mono- to pentalayer phosphorene FETs are simulated based on non-equilibrium Green's function (NEGF) formalism,[18] where the Hamiltonian matrix is constructed using the supercell as described above. The ballistic transport equation is solved iteratively with Poisson's equation until self-consistency between the charge and the

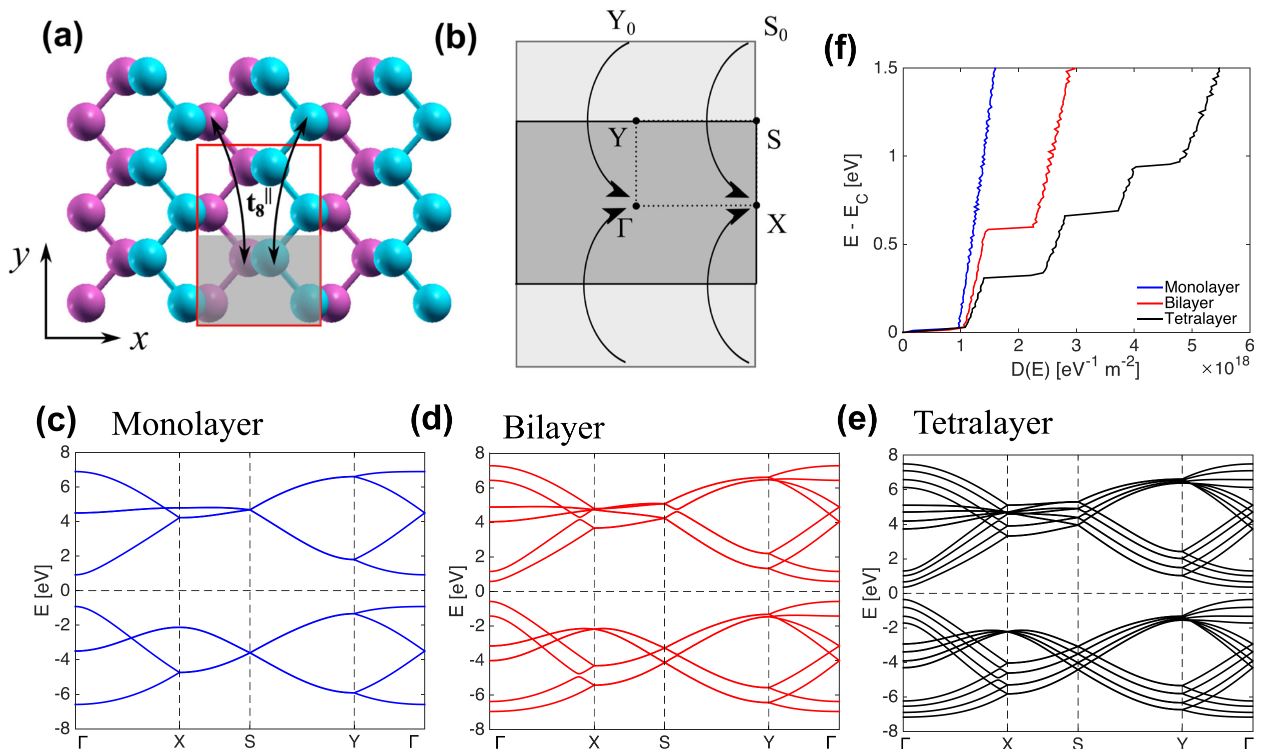

FIG. 1. (a) Atomistic configuration of phosphorene (top view). Different colors are used for top (cyan) and bottom (dark pink) layers for visualization. The red rectangle shows the supercell that we have used in our simulation, which consists of two unit cells of phosphorene. A unit cell is shown by the shaded region. (b) The first Brillouin zone of phosphorene using the supercell (dark region) and the original unit cell (bright region), where arrows show zone folding. Band structure of (d) monolayer (e) bilayer, and (f) tetralayer phosphorene plotted using the supercell. (f) Density of states (DOS) of monolayer, bilayer, and tetralayer phosphorene near the conduction band edge.

TABLE I. Bandgap and effective mass of mono- to pentalayer phosphorene in $\Gamma \rightarrow X$ transport direction.

Number of layers	1	2	3	4	5
E_g (eV)	1.84	1.16	0.87	0.72	0.63
m_e^* (m_0)[a]	0.19	0.18	0.17	0.16	0.15
m_h^* (m_0)[a]	0.2	0.17	0.16	0.15	0.14

[a] m_0 is free electron mass.

electrostatic potential is satisfied. We considered $\Gamma \rightarrow X$ to be the direction of transport, which is also referred to as the armchair direction in literature.[12,19] Charge density and current are calculated by the numerical summation of transverse modes. Two different device structures are considered: conventional FET structure for high-performance applications and tunnel FET structure for low-power applications. The nominal device has 15-nm channel length (L_{ch}) and 20-nm source/drain extensions. The source and drain are n-doped in conventional FETs, and p-doped source and n-doped drain are used for the TFETs. The doping concentration at source and drain ($N_{S/D}$) is $1.6 \times 10^{13}\,\mathrm{cm}^{-2}$. We use a single gate (SG) for conventional FETs (Fig. 2(a)) following the recent experimental demonstrations,[6,20] whereas a double-gate (DG) device geometry (Fig. 2(b)) is assumed for TFETs because the electrostatic control is critical for abrupt switching in low-power devices.[21,22] In both devices, 3.14-nm ZrO_2 ($\kappa \approx 23$) or an equivalent oxide thickness (EOT) of $\sim$0.5 nm is used and the dielectric constant of phosphorene is 10.[23] Scattering is ignored since it is expected that our devices will be operated in ballistic or quasi-ballistic regime due to short channel lengths considered in this study. For long-channel devices, scattering mechanism can reduce the drain current and also limit the minimum leakage current and subthreshold swing (SS), but its impact would be minimal for the size of devices considered here. It is assumed that the devices are operated at room temperature (300 K).

III. RESULTS AND DISCUSSION

A. Phosphorene-based conventional FETs for high-performance applications

First, we investigated the device characteristics of conventional FETs using various numbers of phosphorene layers

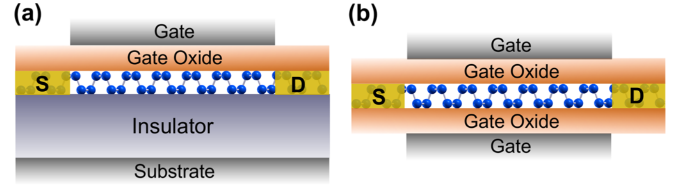

FIG. 2. Device structure of phosphorene field-effect transistors (FETs) with (a) single-gate (SG) and (b) double-gate (DG) geometry. We have used mono- to pentalayer phosphorene for the channel material (monolayer is shown here).

for the channel material. Figures 3(a) and 3(b) are transfer characteristics of mono-, bi-, and tetralayer conventional FETs in linear and log scale, respectively. In terms of on-state characteristics, no remarkable difference is observed among the devices where $I_{on} > 1$ mA/μm and $g_m \sim 15$ mS/μm. This is because few-layer phosphorenes have almost identical electron effective masses (Table I) and DOS near the conduction band edge (at $E - E_c < 0.3$ eV in Fig. 1(f)) where the majority of carrier flows. Although multilayer phosphorene has larger DOS than monolayer phosphorene at higher energy levels, its impact on the I_{on} is minimal since the relevant energy states are too far from the conduction band minima.

On the other hand, we can observe dissimilar off-state characteristics with different numbers of phosphorene layers. In particular, the minimum leakage current can be significantly increased if thicker phosphorene is used due to the smaller bandgap. Figure 3(b) shows that, as the gate voltage is lowered, the off current of tetralayer phosphorene FET monotonically decreases to $\sim 10^{-6}$ μA/μm, but I_{off} increases significantly beyond this point if the gate voltage is decreased further at $V_G < -0.05$ V. This is gate-induced drain leakage (GIDL) that is caused by band-to-band tunneling in small-bandgap materials.[10,24] We have plotted conduction and valence bands on top of the local density of states (LDOS) of the tetralayer phosphorene FET at $V_G = -0.5$ V in the left panel of Fig. 4(a), and the corresponding energy-resolved current spectrum is shown on the right. It is clearly shown that the tunneling current is significantly larger than thermionic current (which cannot be even observed in the current spectrum due to its negligible contribution to the total current). In comparison, FETs based on larger-bandgap materials like mono- or bilayer phosphorene have more immunity to GIDL and the minimum leakage

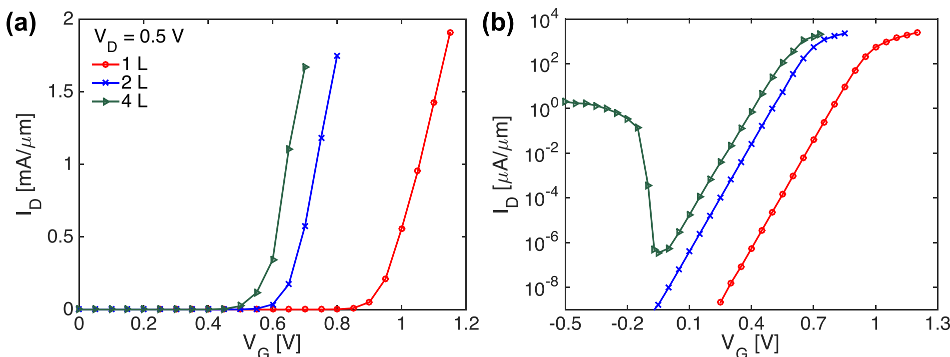

FIG. 3. I_D–V_G plots of conventional FETs based on monolayer (1L; line with circles), bilayer (2L; line with crosses), and tetralayer phosphorene (4L; line with triangles) shown in (a) linear and (b) logarithmic scale.

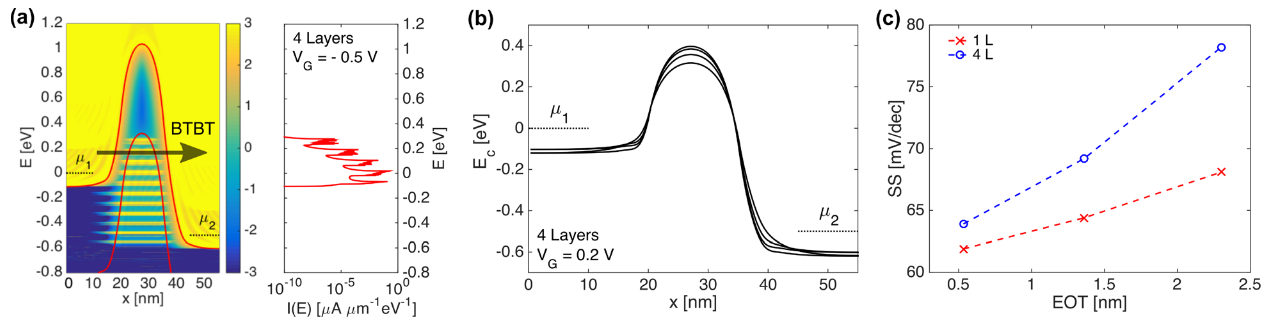

FIG. 4. (a) (Left) Conduction (E_c) and valence band (E_v) of tetralayer phosphorene FET plotted on local density of states (LDOS; in log scale) at $V_G = -0.5$ V and $V_D = 0.5$ V, where E_c and E_v are the average potential of four layers. $\mu_{1,2}$ are chemical potentials at source and drain, respectively. The arrow indicates band-to-band tunneling (BTBT). (Right) The corresponding energy-resolved current spectrum. (b) Conduction band profile of each layer (without taking the average) along the device in the tetralayer phosphorene FET at $V_G = 0.2$ V and $V_D = 0.5$ V. (c) Subthreshold swing (SS) of monolayer and tetralayer phosphorene FETs at various equivalent oxide thicknesses (EOTs).

current can be significantly smaller than that of the multilayer phosphorene FETs.

Subthreshold swing (SS) is one of the most important device characteristics at off state. Thicker phosphorene shows larger subthreshold swing, although the difference is insignificant with EOT of 0.5 nm: SS = 61.9, 62.3, and 63.9 mV/dec for mono-, bi-, and tetralayer phosphorene, respectively. This lower efficiency of the electrostatic control by the gate in tetralayer phosphorene FETs can be observed in Fig. 4(b), which clearly depicts that the electrostatic potential of each layer is controlled non-uniformly by the gate, unlike the monolayer FET. Even with very thin EOT, the potential barrier heights show ~0.1 eV difference between the top and the bottom layers. As the EOT becomes thicker, the performance degradation of gate electrostatic control in the tetralayer phosphorene becomes more conspicuous, which can be seen in Fig. 4(c), where SS of tetralayer phosphorene FET at 2.3-nm EOT is 22% larger than that at EOT = 0.5 nm, while monolayer shows only 10% increase for the same change.

In view of the above results, we can conclude that monolayer can provide the best device characteristics in phosphorene-based conventional FETs toward high-performance applications due to the following reasons: (i) Monolayer guarantees the best electrostatic control by the gate, resulting in the abrupt switching characteristics near the classical limit. (ii) Multilayer phosphorene suffers from GIDL or band-to-band tunneling due to its small bandgap, which is not observed in the monolayer phosphorene FET. (iii) In addition, monolayer phosphorene does not show any drawback in on current and transconductance despite its relatively lower DOS, as compared to the multilayer phosphorene. From this perspective, engineering the number of layers in phosphorene-based conventional FETs can be straightforward. However, things are getting more complicated if tunnel FETs are taken into account, which will be discussed next in detail.

B. Phosphorene tunnel FETs for low-power applications

In this section, we compare device performance of mono- to pentalayer phosphorene TFETs. For this, we first use a common power supply voltage (V_{DD}) of 0.4 V, which is the maximum drain voltage (V_D) that can be used for the pentalayer phosphorene (the smallest bandgap material considered in this study) TFET to avoid significant leakage at off state. This limitation is clearly shown in Fig. 5(a), which is the band profile of a pentalayer phosphorene TFET at the off state with the minimum leakage current, where significant leakage current would be inevitable if a larger V_D was applied. The transfer characteristics of mono- to pentalayer phosphorene TFETs are plotted in Fig. 5(b), where pentalayer shows the largest on current and also the largest leakage current due to the smallest bandgap. On the other hand, the large bandgap of monolayer phosphorene (1.84 eV) imposes a huge tunnel barrier even at high gate voltages, rendering it impractical for electronic devices under the given condition. Thus, we have plotted the subthreshold swing only for the remaining four devices in Fig. 5(c), where bi- to pentalayer phosphorene TFETs show SS in the range of 30–43 mV/dec. Although thicker channel gradually loses electrostatic control, even the pentalayer device exhibited a reasonably good switching characteristic. In general, thinner phosphorene TFETs can provide larger maximum achievable I_{on}/I_{off}, but its on current can be significantly limited compared to thicker phosphorene devices as shown in Fig. 5(d), which indicates that I_{on} can be improved with more number of layers by sacrificing the on-off current ratio.

In the above discussion, for a comparison of phosphorene TFETs with different number of layers, we used a common V_D, which limited the achievable range in I_{on}/I_{off}, particularly for large bandgap materials. In principle, for the same on current, larger I_{on}/I_{off} can be achieved by using a larger V_D, since the device can be operated within a larger voltage window. Figure 6(a) is I_D–V_G characteristics of the trilayer phosphorene TFET at two different drain voltages of 0.4 V (solid line) and 0.6 V (dashed line), which clearly shows that I_{on}/I_{off} can be significantly increased with $V_D = 0.6$ V for the common I_{on} of 1.6 μA/μm (at $V_{on} = 0.9$ V). Moreover, a larger I_{on} can also be achieved at $V_D = 0.6$ V, as compared with $V_D = 0.4$ V, due to the larger energy window for current flow at higher gate voltages as shown in Fig. 6(b). Therefore, to take the advantages of large V_D, we have used different drain voltages for different numbers of phosphorene layers: $V_D = 0.7$ V for mono- and bilayer, 0.6 V for trilayer, 0.5 V for tetralayer, and 0.4 V for pentalayer phosphorene TFETs. The corresponding I_{on} vs.

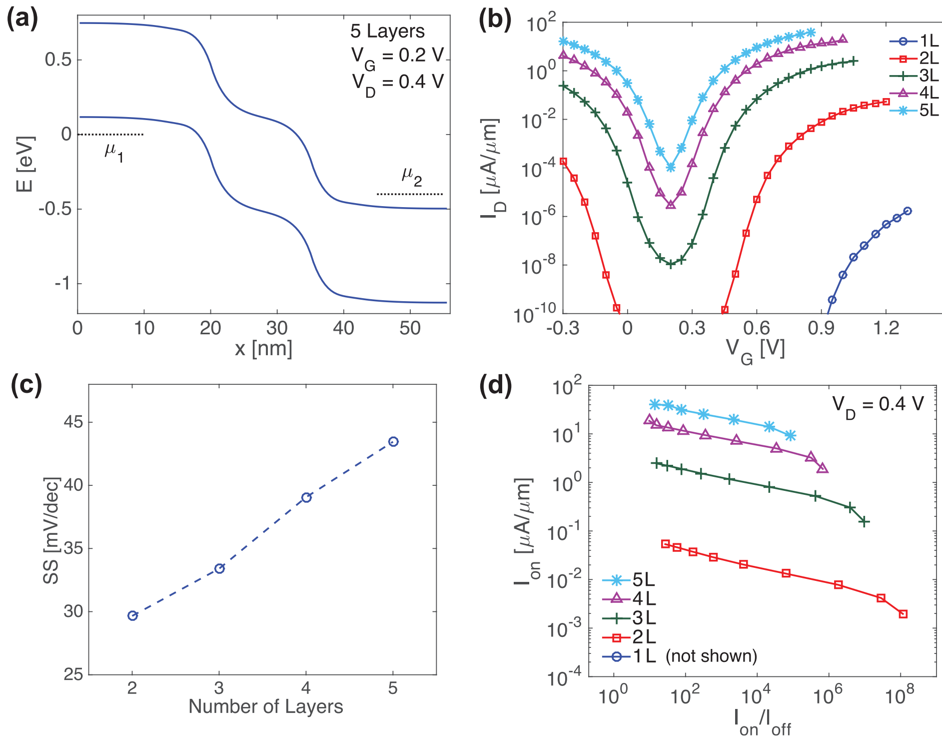

FIG. 5. (a) The conduction and the valence band profile for pentalayer phosphorene TFET at $V_G = 0.2$ V and $V_D = 0.4$ V. (b) I_D–V_G characteristics for mono- to pentalayer phosphorene TFETs at $V_D = 0.4$ V. (c) The subthreshold swing of bi- to pentalayer phosphorene TFETs. (d) I_{on} vs. I_{on}/I_{off} of phosphorene TFETs at $V_D = 0.4$ V. Monolayer is out of range in this plot due to its extremely small I_{on}.

I_{on}/I_{off} is shown in Fig. 6(c). We have observed that, for bilayer phosphorene TFET, the maximum achievable I_{on}/I_{off} is significantly increased by more than one order of magnitude and I_{on} is also increased by a factor of 40 for the same $I_{on}/I_{off} = 10^8$ using a larger V_D. However, such a dramatic improvement of maximum achievable I_{on}/I_{off} was not observed in tri- and tetralayer phosphorene TFETs with the increased drain voltages. This is due to the larger minimum leakage current (I_{min}) at larger V_D, as can be seen in Fig. 6(a), which is attributed to the larger energy window for the direct tunneling from source to drain. In Fig. 6(c), we classified phosphorene TFETs into two groups: Three or more numbers of phosphorene layers TFETs (Group A) show reasonably high on current but relatively low I_{on}/I_{off}; bilayer phosphorene TFET is another group (Group B) that can provide a large I_{on}/I_{off} but a limited I_{on}. In the subsequent discussion, we will employ different strategies for these two groups to enhance the device performance of phosphorene TFETs.

In principle, the leakage current of a ballistic TFET can be suppressed by increasing the channel length without degrading the on-state characteristics, and therefore, we have varied L_{ch} from 15 to 25 nm for tri- to pentalayer phosphorene TFETs (Group A) using the same drain voltages as shown in Fig. 6(c). The I_D–V_G characteristics are shown for trilayer phosphorene TFETs with different channel lengths in Fig. 7(a), where the minimum leakage current decreases exponentially as L_{ch} increases. We have repeated the same also for tetra- and pentalayer phosphorene TFETs and plotted I_{on} vs. I_{on}/I_{off} in Fig. 7(b). It is shown that, while I_{on} remains intact, the maximum achievable I_{on}/I_{off} is significantly increased for all three devices with 25-nm channel, up to 4 orders of magnitude for the trilayer phosphorene. In addition, subthreshold swing is also decreased significantly from 35 to 15 mV/dec by increasing the channel length from 15 to 25 nm for trilayer phosphorene TFETs (Fig. 7(c)).

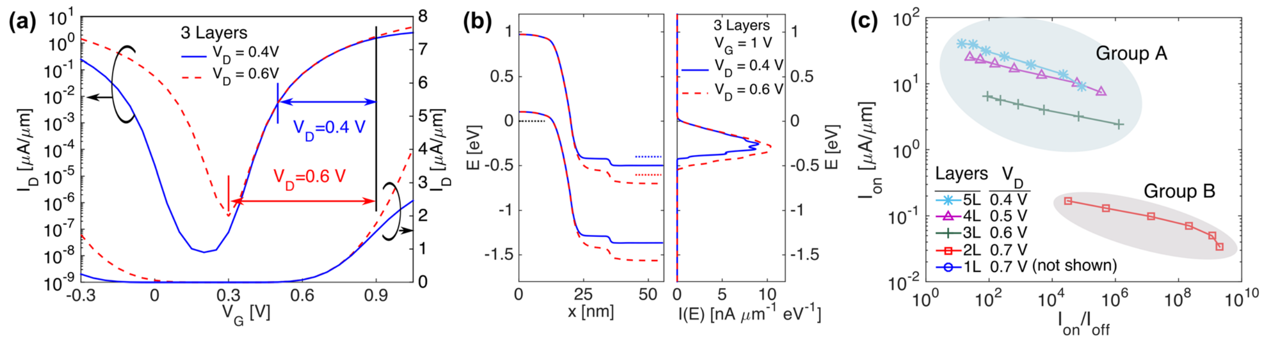

FIG. 6. (a) I_D–V_G characteristics of trilayer phosphorene TFETs at $V_D = 0.4$ V (solid line) and $V_D = 0.6$ V (dashed line), shown in logarithmic scale (left axis) and linear scale (right axis). (b) Energy-resolved current spectrum (right panel) shown with the E_c and E_v profiles along the device (left panel) for the trilayer phosphorene TFET for $V_D = 0.4$ V (solid line) and 0.6 V (dashed line) at $V_G = 1$ V. (c) I_{on} vs. I_{on}/I_{off} of phosphorene TFETs with various drain voltages carefully chosen for different numbers of layers: $V_D = 0.7$ V for mono- and bi-layer, 0.6 V for trilayer, 0.5 V for tetralayer, and 0.4 V for pentalayer, respectively. Monolayer is out of range in this plot due to the extremely small I_{on}.

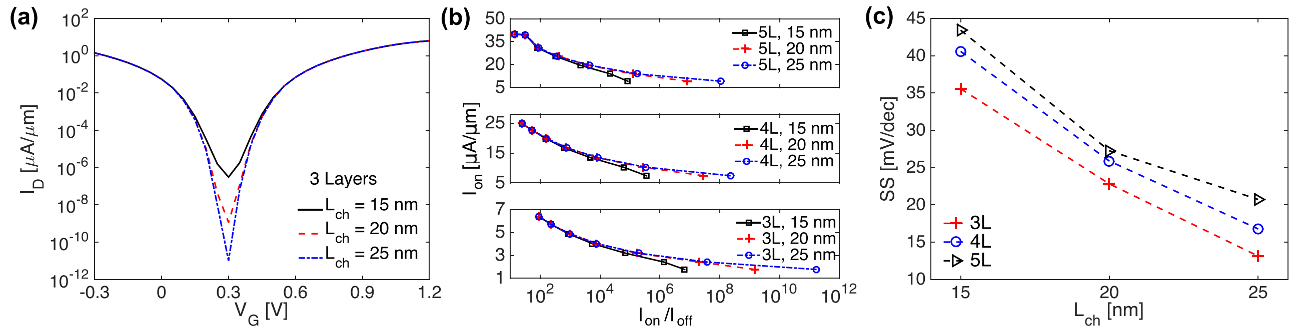

FIG. 7. (a) I_D–V_G characteristics of trilayer phosphorene TFETs for $L_{ch} = 15$ nm (solid line), 20 nm (dashed line), and 25 nm (dashed-dotted line) at $V_D = 0.6$ V. (b) I_{on} vs. I_{on}/I_{off} for trilayer (lower panel), tetralayer (middle panel), and pentalayer (upper panel) phosphorene TFETs with $L_{ch} = 15$–25 nm at V_D shown in Fig. 6(c). (c) Subthreshold swing as a function of channel length for the devices shown in (b).

One of the common issues in TFETs is relatively small on current due to the large tunnel barrier even at large gate voltages, which is exactly what we have observed particularly with the bilayer phosphorene TFET (Group B). In order to overcome such a limitation, barrier-free tunneling based on carbon heterostructure has been proposed earlier.[25] However, the same approach cannot be applicable to phosphorene TFETs, and therefore, here the similar effects will be achieved by increasing doping concentration at source and drain to enhance the I_{on} of bilayer phosphorene TFETs. A 15-nm channel and the same drain voltage are used as shown in Fig. 6(c). Figure 8(a) shows the significant upward shift of I_D–V_G curve for bilayer phosphorene TFETs (dashed line and solid line with squares are for $N_{S/D}$ of $1.6 \times 10^{13}\,\text{cm}^{-2}$ and $3.2 \times 10^{13}\,\text{cm}^{-2}$, respectively). Figure 8(b) shows that the increase of $N_{S/D}$ enormously enhanced the I_{on} of bilayer phosphorene TFET by two orders of magnitude with the cost of I_{on}/I_{off} by one order of magnitude. Figure 8(c) shows the enhancement of current spectrum at the on state ($V_G = 1$ V), the origin of which is barrier thinning at the source-channel junction as shown in Fig. 8(d), whereas the larger leakage current is attributed to the larger energy window for carrier injection opened by the larger $N_{S/D}$.

It would be worth investigating mono- and trilayer phosphorene TFETs based on high $N_{S/D}$ in addition to the bilayer phosphorene TFET. Both devices exhibited significant improvement in on-state characteristics as shown in Figs. 8(a) and 8(b), but the I_{on} of monolayer phosphorene TFET still remained very low. We further engineered bi- and trilayer phosphorene TFETs with longer channel lengths to suppress the minimum leakage current. For trilayer phosphorene TFET, the channel length engineering for smaller

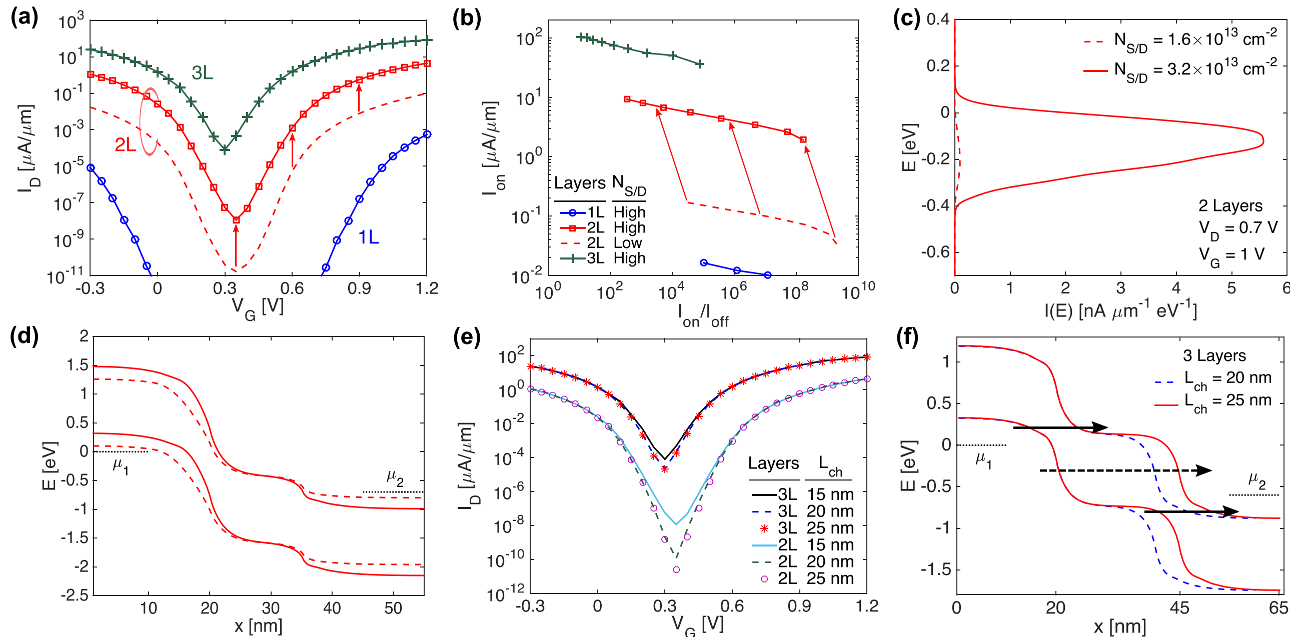

FIG. 8. (a) I_D–V_G characteristics for monolayer (solid line with circles), bilayer (solid line with squares), and trilayer (solid line with crosses) phosphorene TFETs with $N_{S/D} = 3.2 \times 10^{13}\,\text{cm}^{-2}$. Bilayer phosphorene TFET with $N_{S/D} = 1.6 \times 10^{13}\,\text{cm}^{-2}$ (dashed line) is also shown for a reference. L_{ch} is 15 nm and V_D is as shown in Fig. 6(c). (b) I_{on} vs. I_{on}/I_{off} for the devices shown in (a). (c) Energy-resolved current spectrum of bilayer phosphorene TFETs for different $N_{S/D}$. (d) Potential profile for the device shown in (c). (e) I_D–V_G characteristics of bi- and trilayer phosphorene TFETs for the channel lengths of 15, 20, and 25 nm with $N_{S/D} = 3.2 \times 10^{13}\,\text{cm}^{-2}$. (f) Potential profile along the device for trilayer phosphorene TFETs at the off state for the channel lengths of 20 nm (dashed line) and 25 nm (solid line). Dashed arrow illustrates direct leakage through the entire channel, and solid arrows indicate the additional leakage paths through the junction between the source/drain and the channel.

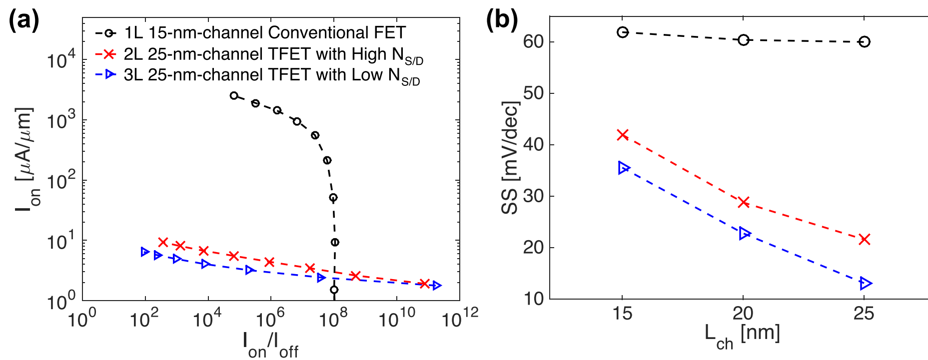

FIG. 9. (a) I_{on} vs. I_{on}/I_{off} for 15-nm-channel monolayer phosphorene conventional FET (dashed line with circles), 25-nm-channel bilayer phosphorene TFET with $N_{S/D} = 3.2 \times 10^{13}\,\text{cm}^{-2}$ (dashed line with crosses), and 25-nm-channel trilayer phosphorene TFET with $N_{S/D} = 1.6 \times 10^{13}\,\text{cm}^{-2}$ (dashed line with triangles). (b) Subthreshold swing of the devices shown in (a) at various channel lengths.

I_{min} becomes less efficient with an increased doping concentration (Fig. 8(e)), as compared to low $N_{S/D}$ case (Fig. 7(a)), and there is almost no gain in I_{min}, particularly for the channel longer than 20 nm. This is due to the presence of additional leakage paths as shown by the solid arrows in Fig. 8(f), making the channel length engineering ineffective. For bilayer phosphorene TFETs, however, we can see larger gains in suppressing I_{min} in Fig. 8(e), due to the larger bandgap and hence less amount of tunneling through the addition leakage paths. With the increased doping density, the bilayer phosphorene TFET exhibits similar device performance as that of the trilayer phosphorene TFET based on low doping concentration with the maximum I_{on}/I_{off} of $\sim 10^{11}$ at $L_{ch} = 25$ nm.

C. Comparison of phosphorene-based conventional FETs and TFETs

Finally, we compare the device performance of phosphorene-based conventional FET and TFET. For a conventional FET, monolayer phosphorene is taken since it can provide the best device performance as we have shown earlier, and we choose bilayer and trilayer phosphorene for TFETs due to the same reason. Figure 9(a) shows I_{on} vs. I_{on}/I_{off} of those three devices that we simulated in Sections III A and III B. It turns out that the conventional FET can have significantly larger I_{on} than TFETs, making it more appropriate for high-performance applications where fast switching speed is critical. On the other hand, bilayer and trilayer phosphorene TFETs exhibited significantly larger I_{on}/I_{off} compared to the conventional FET, indicating that they can be suitable for low-power applications where speed is less important but power consumption is the main concern. In addition, the subthreshold swing of TFETs can be significantly smaller than the best conventional FET, especially for longer channel lengths, as shown in Fig. 9(b). At $L_{ch} = 25$ nm, bilayer and trilayer phosphorene TFETs exhibit 64% and 78% smaller SS than the conventional FETs. This comparison of the best devices from different configurations clearly identifies the target applications of each device and also provides useful insights into various parameters including the number of channel layers to maximize the performance of phosphorene FETs.

IV. CONCLUSIONS

We explored mono- to pentalayer phosphorene FETs using self-consistent atomistic quantum transport simulations. We first examined the conventional FET structure and concluded that monolayer phosphorene can provide the best performance in every aspect. We showed that monolayer phosphorene FET can be switched near the classical limit of SS = 60 mV/dec with the large immunity to GIDL. Moreover, it exhibited equally large on current ($I_{on} > 1$ mA/μm) as multilayer phosphorene FETs, without any penalty of relatively lower DOS. On the other hand, the device performance of phosphorene TFETs is very susceptible to various material and device parameters such as number of layers, power supply voltage, channel length, and doping concentrations. Our comprehensive simulation results revealed that either bilayer or trilayer phosphorene can provide the best performance in TFET with the maximum I_{on}/I_{off} of 2×10^{11} and the SS as low as 13 mV/dec by engineering channel length, doping concentration and power supply voltage properly. Finally, we compared the performance of conventional FET and TFETs based on phosphorene, showing feasibility of each device for different target applications where different requirements are needed. Here, we have provided irreplaceable insights into phosphorene-based FETs through comprehensive optimization processes, which may also be extended to the engineering practice of other similar 2D semiconductor FETs.

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