

High Aspect Ratio Polystyrene Structure and Nano-gap Electrode Fabrication Using Electron Beam Lithography

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of the thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

This thesis discusses the techniques of nanostructure fabrication using electron beam lithography (EBL). This technique has become the most widely employed among other nanofabrication techniques. Additionally, EBL is used in research and development and for the prototyping/production of photo-masks and imprint molds. However, the focus here is on the study of a novel resist and development process, as well as a pattern transfer procedure after lithography.

There are several chapters in this thesis that discuss various aspects of nanofabrication. In part I (Chapters 1-3), a brief introduction of nanotechnology is presented in the first chapter. The second chapter introduces two major nanofabrication techniques that are essential in the manufacturing of nanostructures. These are film deposition and wet/dry etching. The basic concepts, working mechanisms and important parameters of these two techniques are briefly discussed. The third chapter outlines a relatively new nanofabrication technique, using electron beam lithography (EBL). This chapter presents more details about EBL, such as the limitations, proximity effect, and EBL resists.

The second part (II) consists of two chapters. Chapter 4 presents the process of fabricating high aspect ratio polystyrene structures using electron beam lithography which do not collapse. The fabrication of high aspect-ratio nanostructures would open several new possibilities in the MEMS/NEMS field, especially in BioMEMS. It is easy to obtain these kinds of structures on silicon substrate; however, there are some challenges for keeping the tall pillars (with a pitch of 2 μm and a diameter of sub- 200 nm) stable,

particularly when organic EBL resist, such as polystyrene (PS), is used. Nonetheless, it is preferable to use PS as it is of low cost and is a simple process to control. This chapter, therefore, focuses on method pattern collapse by using PS-EBL. The resist is first exposed at 20keV, then at 4keV to cross-link the top layer as a bridge to hold the tall pillars together during rinsing and drying. After development, there will be a house-like structure of pillars supporting a “roof”, and the “roof” prevents the pillars from falling down. This top layer can then be etched by O₂ plasma RIE (reactive ion etching), leaving behind tall PS pillars without collapse.

Finally, chapter 5 introduces the fabrication of nano-gap electrodes for nano-devices. The process involves creating a nano-gap using an optimized two-step exposure technique. First, high energy (20 keV) exposure is used to define a nanogap between two thin lines. Then the large pad structure, which could be used as an electrode, is defined using low energy exposure (2.5 keV). The proximity effect will be very significant for large microscale features, but the lateral backscattering range is small (100-200 nm) for the low energy used, and thus the proximity exposure at the middle of the gap would be low if the two pads are separated by >100-200 nm. Therefore, with accurate alignment between the two exposures, a nano-gap between the two large pads can be obtained when the wide gap region is filled with a pair of thin lines having a nano-gap in between them.

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Dedication

To My Great Family

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CHAPTER 1

Introduction to Nanotechnology and Nanofabrication

1.1 Overview of Nanotechnology:

Scientific exploration has grown after scientists discovered new manifold ways of perceiving the theories of atoms and molecules, and their subdivisions became established and interfaced. This revolution has led to our world being changed forever. Nano is a Greek word that means dwarf. Technology based on this very tiny scale is currently known as nanotechnology. This technology was revealed after the physicist Richard Feynman mentioned it in his speech titled, “There is plenty of room at the bottom” in 1965 at the annual meeting of the American Physical Society at the California Institute of Technology (Caltech). It is a unique statement that has brought on a new concept in technology, which was later called “nanotechnology” by Professor Norio Taniguchi in 1974.¹ Indeed, there are four main generations of nanotechnology that have existed. The first generation consisted of nanoparticles and continued up to the year 2000. The second generation continued up to 2005 and included advancements such as bio-devices and targeted drug delivery. The third one is the revolution in 2010 encompassing 3D networking and bio-design. The last generation will be from 2015 to 2020. An example of this is atomic or molecular devices.⁹

Nanotechnology is defined as the fabrication of technology on a nanometer scale (1 billionth of a meter) with dimensions down to sub-100 nm. To understand just how small that is, the length of a typical bacterium is 200 nanometers, and the diameter of a strand of DNA, a mere two nanometers. However, submicron (1000–100 nm), nano

(100–1 nm), and atomic (or angstrom, less than 1 nm) are the three categories of microfabrication systems as shown in Figure 1-1.^{4,5} It has been used and combined across various scientific fields, for instance, chemistry, biology, physics, material science, computer science, and engineering. One example of nanotechnology is nanotubes. This technology has rapidly spread and quickly received widespread attention across the world after the invention of the scanning tunneling microscopy (STM).¹ In addition, nanoelectronics⁶, nanomaterials, nanorobotics, nanomagnetics, nanophotonics, nanobiology, nanomedicine⁷, etc. are all parts of the various subject areas that utilize nanotechnology. Moreover, the development of nanofabrication techniques has opened new possibilities in numerous applications, such as micro and nano-electromechanical systems (MEMS, NEMS), and especially bioMEMS. An example in this field is a miniature robot capable of self-propulsion inside a viscous liquid. These micro-robots can be used to swim in blood or other fluids found in the body with the aim of monitoring the cancerous cells.² Therefore, nanostructures can be produced by using a wide variety of nanofabrication techniques.

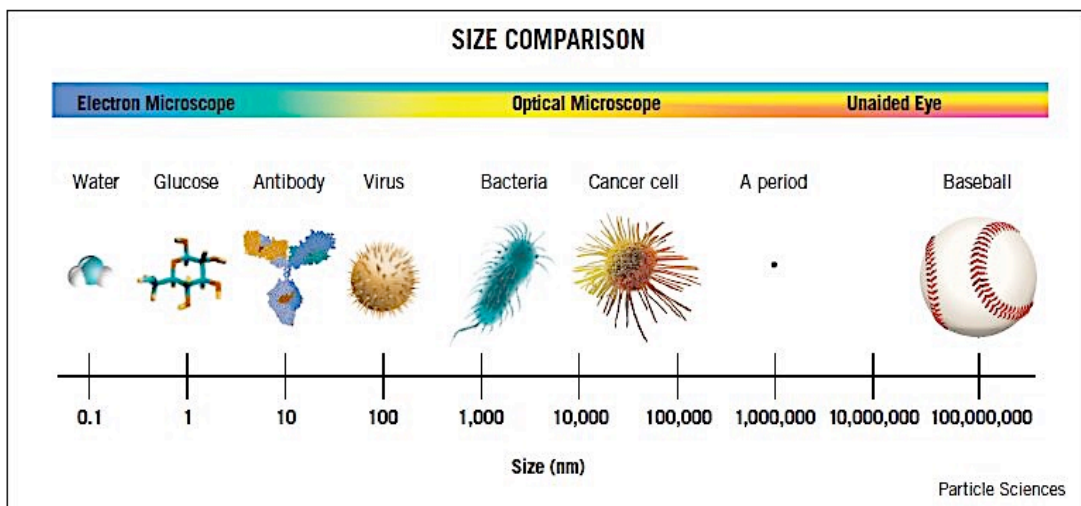


Figure 1-1: The sizes of different objects in nanometers.⁴

1.2 Overview of Nanofabrication:

Nanofabrication is a technology that has the ability to produce the desired nanoscale structures. In particular, nanofabrication techniques are the key to achieving a structure with feature sizes below 100 nm. In the 21st century, the techniques of nanofabrication have been developing in various ways to fulfill the claims of nanotechnology and nanofabrication. Broadly, there have been two different ways of obtaining control over matter at the nanoscale: “top-down” and “bottom-up”. The top-down method has not generally given atomically precise control but it is moving down toward a scale that is similar. This method starts with bulk material and through various methods the size is brought down to the nanoscale, whereas the bottom-up procedure begins with individual

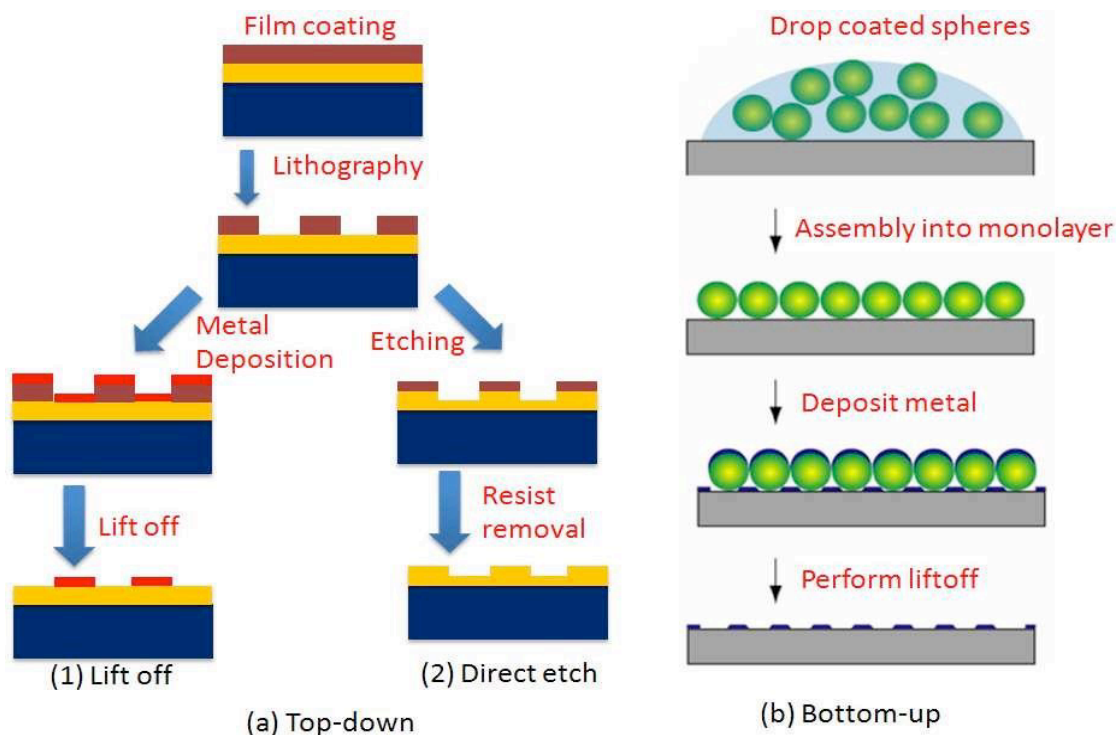


Figure 1.2 The schematic of the (a) top-down and the (b) bottom-up approach. In the top-down approach, the resist is first patterned by lithography, and then (1) the pattern is transferred by deposition followed by liftoff, or (2) the pattern is transferred by direct etching. In the bottom

up approach, the pattern is usually acquired by self-assembly and then transferred onto substrates by liftoff¹⁰.

atoms and builds upwards to create the required shapes and characteristics of the nanostructures and functional devices.⁸ Figure 1-2 below shows the schematic of both approaches of nanofabrication. These nanofabrication techniques become beneficial to the researchers who seek to fabricate advanced practical devices. The top-down approach uses various methods of lithography including electron beam lithography, scanning probe lithography, nanoimprint lithography and block co-polymer lithography, etc. In general, thin-film deposition, etching, and lithography are usually the three common techniques associated with nanofabrication.

Development in the field of nanotechnology has been driven by the prediction of Moore's Law, which states that the number of transistors on integrated circuits (ICs) will double approximately every 18 months due to their reduced size.^{2,11} The first lithography technique used for ICs in the 1970s was optical lithography, also known as photolithography. The concept of this method is simple. The patterns in a mask are transferred onto a thin layer of a light sensitive photoresist. The sample is then developed after photoresist exposure using a shining light through a mask leaving behind the fabrication pattern. The required photoresist contains two types of organic light-sensitive material that form positive and negative photoresist. In positive photoresist, illumination leads to the exposed areas becoming soluble in the developing solutions and then patterns can be easily isolated. In contrast, the exposed areas in a negative photoresist will not be dissolved in developing solutions while the residual areas will be soluble in the solvent. Therefore, the remaining areas will become the desirable structures with a resolution of around 1 μm . Even though this concept is simple, accomplishing this method costs a

significant amount of money and is quite complex. Also, there are several challenges, such as placement accuracy, high throughput, and defect density, etc¹². For these reasons, photolithography has progressed to developing resolution enhancement techniques (RET) and can achieve dimensions down to 10 nm, which makes it the most popular technique in the modern semiconductor industry.⁸ In contrast to photolithography, EBL is the most convenient system that can be used for direct writing. In short, lithographic systems can be classified into two main categories: parallel or serial. EBL is a serial lithography method since the pattern must undergo exposed step-by-step. Consequently, it takes more time and is technique appropriate only for R&D purposes or mask/mold fabrication. Besides EBL, there are other serial lithographic methods, including scanning probe lithography (SPL) and ion beam lithography (IBL)¹³. Unlike the serial methods, parallel systems can achieve the structures in one step. Examples of parallel lithographic systems include: extreme ultraviolet lithography (EUVL), photolithography, deep ultra-violet lithography (DUVL), x-ray lithography (XRL), and nanoimprint lithography (NIL).

These methods are essential tools for nanofabrication, yet there are some layers of materials that need to be added or removed during the process, such as dielectrics, semiconductors, and metals. For this case, an integrated circuit (IC) process typically uses many techniques for material layer deposition and etching. A thin-film deposition is used as an additive technique, which can be divided into two main classifications: physical vapor deposition (PVD), and chemical vapor deposition (CVD).^{10,12} In the PVD process, the material is usually released from a source and deposited onto substrates. The physical deposition has been classified into two types, which are evaporation and sputtering. More details of PVD will be discussed in the next chapter. In

the case of CVD, however, a deposition chamber is prepared for reactant gases and then a chemical reaction occurs between the reactant gas and the surface of the samples, leaving behind a desirable thin film. There are currently numerous sorts of chemical vapor deposition (CVD) techniques, including low-pressure CVD, plasma-enhanced CVD, metal-organic CVD, etc.^{8,14}

The unwanted materials that are deposited on the wafer surface can be removed from the substrates by various etching mechanisms. To obtain the required patterns, the process can be done either through dry or wet etching. Dry etching includes the usage of gas phase etchants in plasma. As the plasma is a part of the process, dry etching is also described as plasma etching, whereas wet etching often involves liquid etchants in order to etch away the deposited materials. This method is cheap and simple but difficult to control. More details on both dry and wet etching techniques can be found in the next chapter as well.

CHAPTER 2

The Techniques and Systems for Nanofabrication: Etching and Thin Film Deposition

2.1 Thin Film Deposition:

In the previous chapter, physical vapor deposition (PVD) was discussed as one of the two categories of layer deposition. Unlike PVD, CVD is an alternate method for depositing thin films that involves chemical reactions. However, there are several issues that should be considered when analyzing the precipitated film growth of thin films and choosing a deposition technique. The initial issue is the quality of the materials that need to be deposited on a wafer surface. Hence, important factors that indicate the film depositions' quality are contamination grades, mechanical and electrical properties, defect density, and synthesis procedures. Above all, the adhesion to the substrate is critical for underlying films. A second problem is that the deposition materials must have a uniform thickness. This uniformity is known as step coverage. Finally, the filling of spaces between or within micro-nanostructures is the third problem which also needs to be addressed. In filling these spaces, researchers can achieve a smooth and flat surface at the top of the sample.^{12, 15}

2.1.1 Physical Vapor Deposition (PVD):

The physical vapor deposition (PVD) techniques are fundamentally physical methods that do not involve chemical reactions. Broadly speaking, PVD is a versatile method because most materials can be used in this process. Using this technique, scientists can simply obtain a desirable thin film of these metallic materials with a nano-

scale thickness. Besides these advantages, PVD is considered a relatively inexpensive and fast method.¹⁶

As mentioned in the previous section, evaporation and sputtering are the most popular operations for PVD that can be used for coating a metallic thin film on the objective substrate. These two operations rely on a source of energy that releases single atoms or molecules, and the experiment can be either in a vacuum or a very low-pressure gas stage.¹⁷ However, both PVD methods have advantages and drawbacks. The advantages of utilizing PVD methods, such as the evaporation method, include minimal damage to the wafer, very pure deposited films, and limited step coverage, whereas the advantages of sputtering are the adjustability of the deposition time, easily controllable operating to obtain specific film thicknesses, and sputter-cleaning of the substrate under vacuum prior to film deposition.¹⁷ However, all of the previously mentioned methods (PVD techniques) suffer from some serious limitations. For instance, the evaporation method has difficulty with materials that have low vapor pressures, and the film adhesion can be problematic, whereas the sputtering method is not suitable for some materials because their components are easily degraded by ionic bombardment, and there is a greater probability of introducing impurities into the substrate.

2.1.1.1 Sputtering:

Sputter deposition is the most commonly used thin film deposition technique. The basic concept of this system is that the atoms of the bulk materials are released from the target (source) by applying a voltage at low-pressure to both the source and substrate with the assistance of plasma (see Figure 2.1). Then, the ionized gas is accelerated to collide

with the target. The ejected atoms will transfer and condense onto the sample that is located at a suitable position to collect the emitted materials. Consequently, the condensed materials will form the desired thin film. However, this system suffers from significant contamination. Therefore, the sputter system is more suitable in some applications rather than others, such as thin antireflection coatings on glass for optical applications and the production of computer hard disks. The sputtering event can be described by using an essential metric, which is the sputtering yield (Y), and it is given by the equation: ¹⁴

$$Y = \text{Number of sputtered atoms ejected} / \text{Number of ions incident}$$

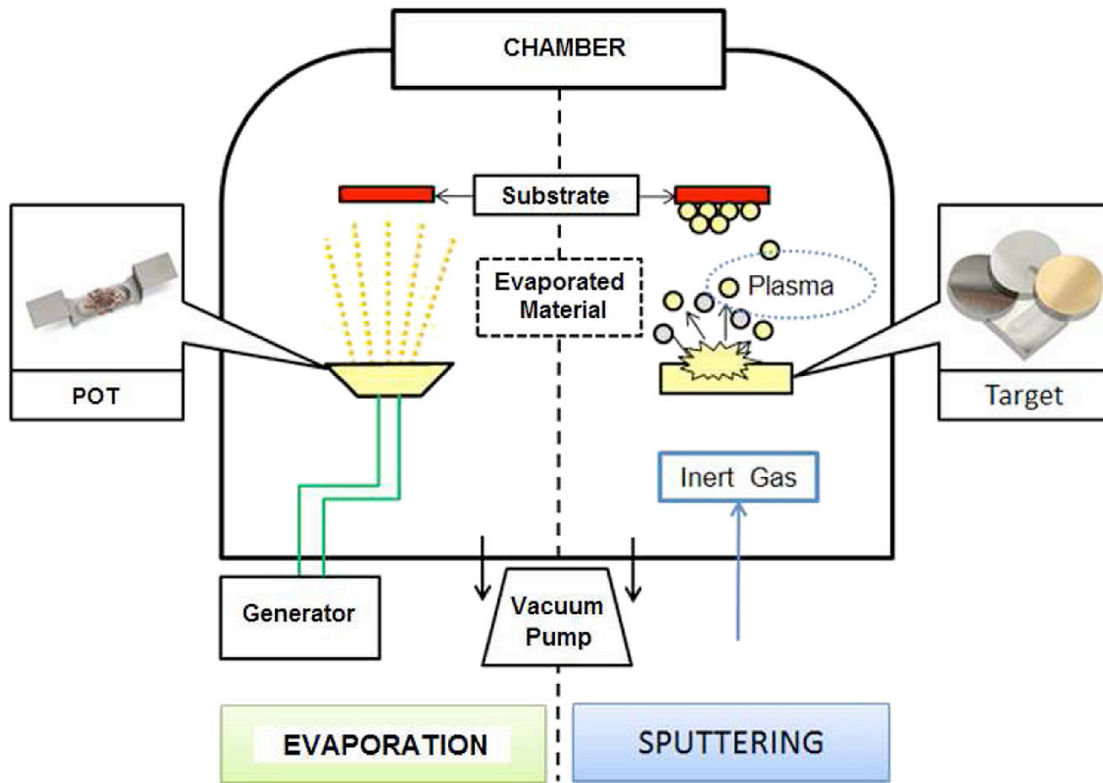


Figure 2.1: Schema of two difference types of PVD process. ¹⁷

2.1.1.2 Evaporation:

Evaporation is the second option for depositing materials, such as Aluminum (Al), Chromium (Cr), Titanium (Ti), Copper, Titanium Nitride, and SiO₂, etc. The evaporating system is considered the first technique that was widely utilized in the IC industry.¹⁸ This process is similar to that of the sputtering system, and both of them are illustrated in Figure 2.1. An evaporating system can be classified into two major categories based on the method of generating high-temperature: thermal evaporation and electron-beam evaporation.

As mentioned, heating of the material is required in both types for melting the source materials. The different types of evaporation are dependent on the method of generating the heat. In thermal evaporation, there will be a filament or RF coils around the graphite crucible which contains the source material. Then, the source material is heated by passing an electrical current over the filament or RF coils. After the source material is heated, the evaporated atoms condense onto the substrate. All these steps are initially done in a vacuum chamber. Figure 2.2 shows the schematic diagram of thermal evaporation. However, this method has limitations that make thermal evaporation exclusive to specific materials. Organic materials are an appropriate choice for this technique since they have a temperature of 1600°C or below, where 1600°C the highest temperature that can be reached in thermal evaporation. Furthermore, another vital issue is that the crucible is heated as well as the source material, which leads to a high contamination in the deposited layer from crucible evaporation and condensation.¹⁹

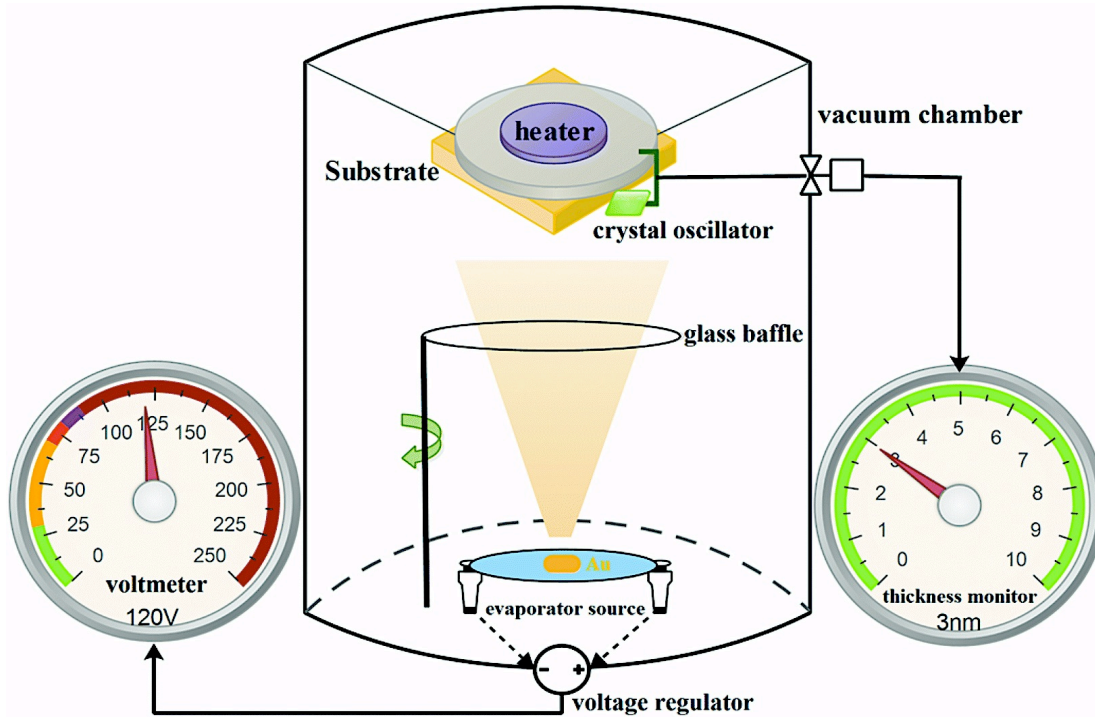


Figure 2.2: The schematic diagram of one of thermal evaporation technique.²⁰

In electron-beam (e-beam) evaporation, the source material can be heated to high temperatures when a focused high-energy electron beam is applied in a high vacuum chamber (less than 10^{-5} torr). In addition, the temperature that an e-beam heater can reach is from 3000°C to 10000°C ; therefore, an assortment of materials can be evaporated. This high energy is obtained by using magnetic fields to focus the beam onto a crucible that contains the source material. To achieve a focused beam, the electron gun (e-source) generates the electron beam, and the released electrons accelerate when a high electrical potential (10 kilovolts) is applied. Then, the evaporated atoms are emitted and irradiated through the vacuum. For e-beam systems, unlike the thermal approach, only the top of the source material is often melted so there will be no impurities from the crucible. Moreover, the target metal (source) is directly located above the electron gun. As a result,

a pure film of desirable metal can be deposited onto the surface of the wafer. The following Figure 2.3 illustrates the schematic of the e-beam evaporation device.

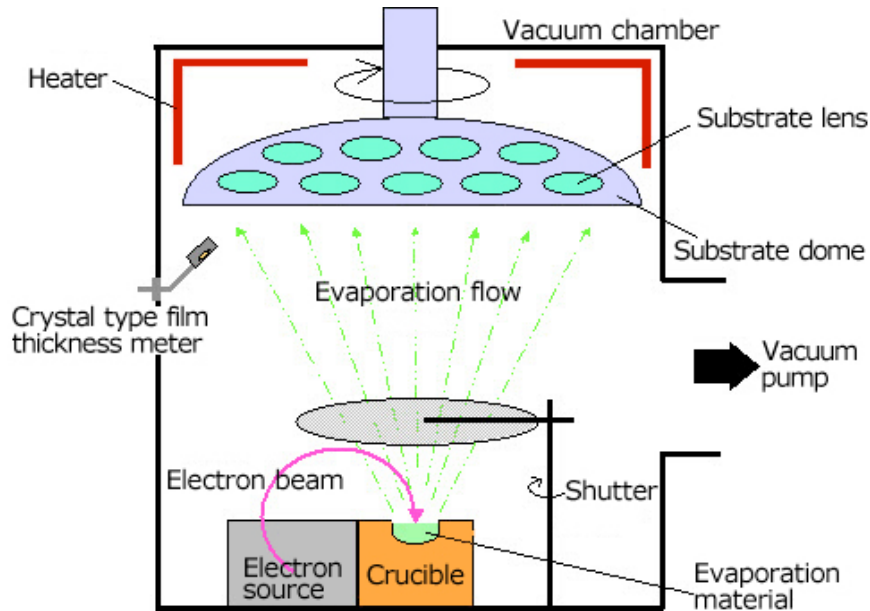


Figure 2.3: The schematic of e-beam evaporation system.²¹

Despite the fact that e-beam and thermal deposition are typically simple methods, there are some significant parameters that should be considered in evaporation systems.²² Initially, as described previously, a high vacuum must be utilized in both systems. The purpose of significantly low pressures in the reaction chamber is that this pressure defines the mean free path of the atoms and molecules. The mean free path is the average distance of a gas molecule that travels without striking other molecules. This parameter is critical for a film deposition since the evaporated atoms must travel a very long trajectory. Also, the atoms that are emitted must travel in essentially straight lines with few collisions from the source to the wafer substrate surface.¹⁹ The mean free path (λ) is given by the equation:

$$\lambda = \frac{kT}{\sqrt{2\pi} p d} \quad (2.1)$$

where k is the Boltzmann constant, d is the diameter of the gas molecule, T is the temperature in the chamber, and p is the pressure in the chamber.²³

2.2 Etching:

A desirable film pattern on a wafer substrate can be achieved by etching the selectively unwanted region of the deposited film. Etching can be also defined as the process by which material is removed from a surface. The process can occur in either a wet or dry environment and is a major technique used in the semiconductor industry. Dry etching can be done by utilizing gas-phase etchants in a plasma. Thus, this process is overwhelmingly also called plasma etching. For wet etching, liquid etchants are a requirement and the wafer is usually dipped in the etchant solution to etch and remove the exposed material through a chemical reaction. Figure 2.5 below shows the general process of etching.

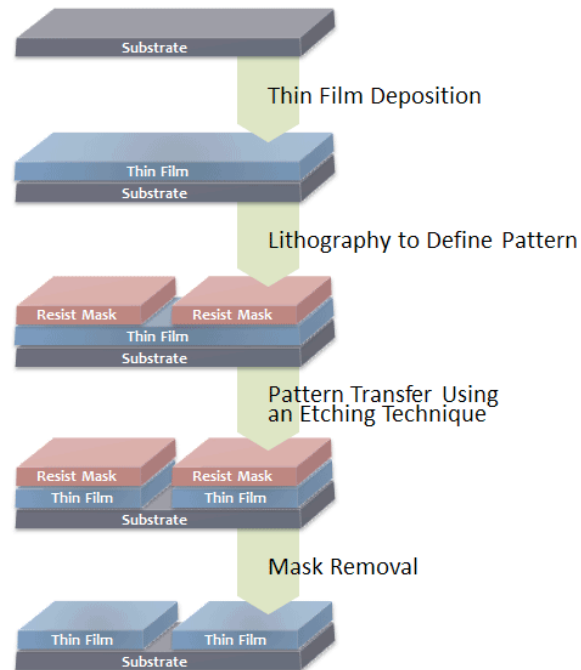


Figure 2.5: The general process of an etching technique. ²⁴

In the etching process, there are several significant parameters that should be considered. The initial parameter is the etching rate. The etching rate is known as the depth of cavities or number of entire layers that are etched out per unit time (A/minute) if the etching is meant to create cavities or eliminates one entire layer of the multilayer system. The second substantial parameter is the selectivity, **S**. The ratio of the etching rate between various materials describes the selectivity, which preferentially removes a particular area during etching without affecting other regions or layers. Therefore, a high selectivity is necessary during etching. Additionally, this parameter is useful in achieving an ideal etch profile that has rather straight sidewalls. Figure 2.6 describes the variation between a poor and a high selectivity of etching terms.

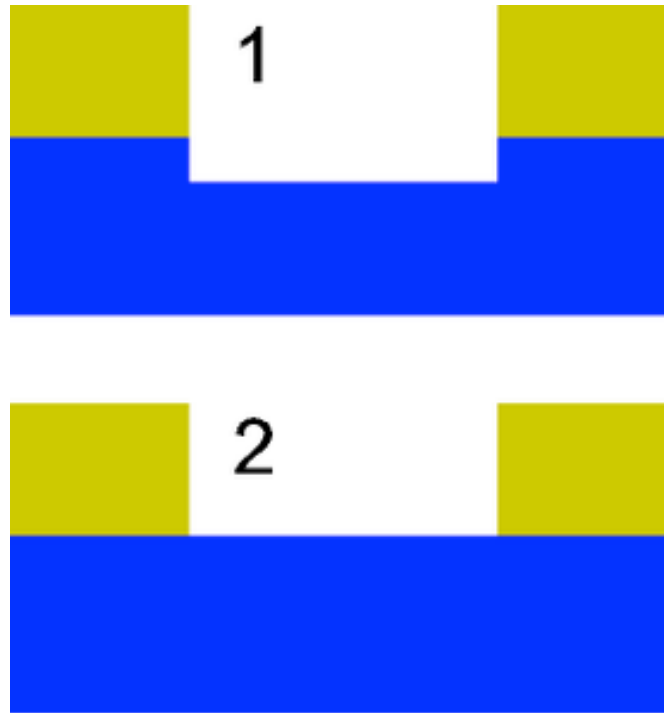


Figure 2.6: A schematic representation of (a) a poor selectivity causes the etchant to attack the bottom layer material while removing the top layer, (b) a high selectivity causes the etch-out of the top layer without affecting the underlying layer.²⁵ (Courtesy of Smack.)

Finally, the third most important parameter is etching directionality. Etch directionality can be divided into three categories: isotropic, anisotropic, and completely anisotropic etching. Figure 2.7 illustrates the difference between three various types of etching directions. Anisotropic etching occurs laterally with less etching.^{12,27} This process almost etches in one particular direction. Anisotropic etchants, which can be used, include KOH, TMAH, and hydrazine, etc.²⁶ Figure 2.7(a) shows the schematic of anisotropic etching. In comparison, isotropic etching is a process that can etch in all directions of the silicon wafer which can occur when the etch rates are nearly the same. Isotropic etching can be done by using very strong acids, such as mixtures of hydrofluoric acid (HF) and nitric acid (HNO₃). The resulting profile is a rounded groove on the substrate. This is shown in Figure 2.7(b).²⁷

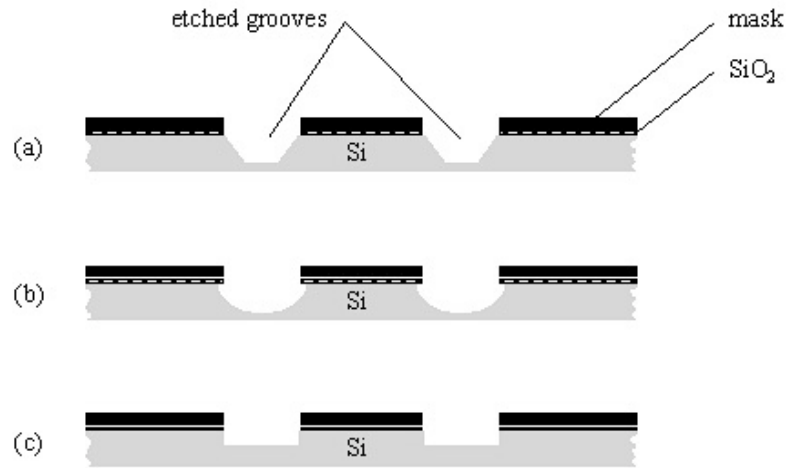


Figure 2.7: Etched grooves for different degrees of etching: (a) anisotropic etching, (b) isotropic etching, (c) completely anisotropic etching.²⁷

However, there is also a completely anisotropic etching. In this case, the etching will be in one direction, and this means no etching at all in the lateral direction as illustrated in Figure 2.7(c). This result is often desirable in some applications in the semiconductor industry. There are several techniques, which can achieve completely anisotropic etching, such as reactive ion etching (RIE) and ion milling. In fact, physical effects play a significant role in etching directionality.

2.2.1 Dry Etching:

In the past years, plasma etching was not as commonly utilized as wet etching. This is because wet etching was cheap and simple leaving almost no damage due to its purely chemical nature, while also being highly selective. However, there was a need for smaller features (line-widths) and vertical structures. Thus, wet etching was not suitable for these requirements. Besides, it also has significant drawbacks, such as poor

anisotropy, poor process control (temperature sensitivity), and poor particle control. Therefore, dry (or plasma) etching techniques were developed for IC manufacturers in order to match the need for fabricating vertical structures. To know just how the mechanism of plasma etching operates, plasmas must first be understood. A plasma is a gas that is fully or partially ionized and consists of almost equal numbers of negative and positive charges and a portion of neutral molecules. This occurs when an electric field of a sufficient magnitude is applied to separate the gas molecules in order to ionize them. For an ideal environment, there are specific gas molecules that can be normally employed in a plasma such as noble gases that include argon and halogens. In addition, the electric field can be supplied in two ways. One method, direct current (DC) plasma, is provided by a DC power input. The alternate method is radiofrequency plasma (RF), which exists when no direct current is provided. The DC plasma mechanism is explained in Figure 2.8. Once the molecules become ionized, the positive ions move towards the cathode after they accelerate. There is also ion bombardment that assists in removing contamination, which occurs during etching, from the traveling ions. The positive ions reach the wafer surface that is located on the cathode. Hence, the secondary electrons are ejected from the cathode. Subsequently, the number of ejected electrons will increase close to the cathode causing the disability of mobile positive ions.²⁹

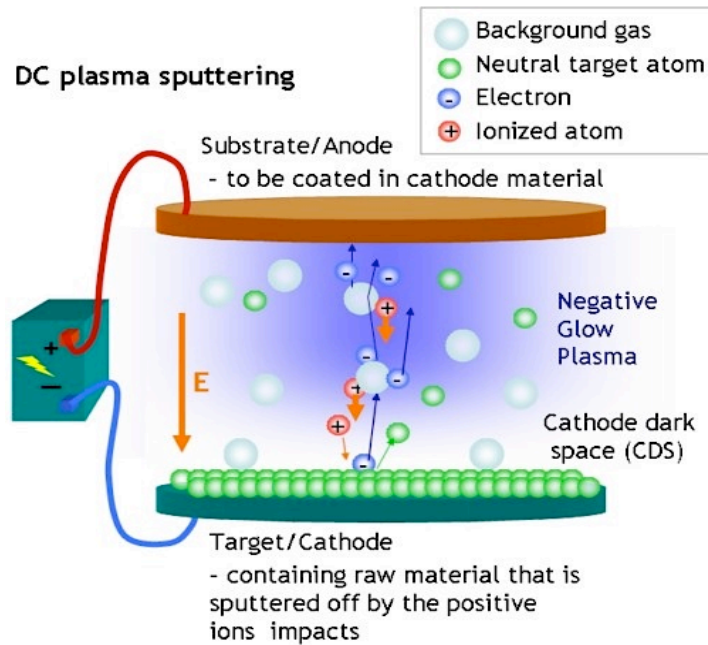


Figure 2.8: The schematic of a DC plasma system.²⁸

There are various types of plasma etch systems that have been developed to fulfill the demand of etching films in semiconductor patterns. Reactive ion etching (RIE) is one of these techniques. RIE is considered a parallel plate etch system that is commonly utilized for the plasma etching of films.³⁰ In addition, RIE is an etching process that involves chemical reactants in the plasma to improve the selectivity while also supporting physical ion bombardment. High directionality is produced by the ionic species, while a high etch selectivity is created by chemical reactive species (free radicals). Figure 2.9 illustrates the diagram of reactive ion etching of oxygen plasma mode. RIE operates by initially producing neutral radicals and ions in the plasma. The reactive species travel towards the objective substrate and then adsorb onto the surface of the wafer to be etched. In order to allow for fewer ion collisions during transport across the sheath, the operating

chamber operates at a low pressure. As a result, the directed ion flux mostly moves toward the wafer.

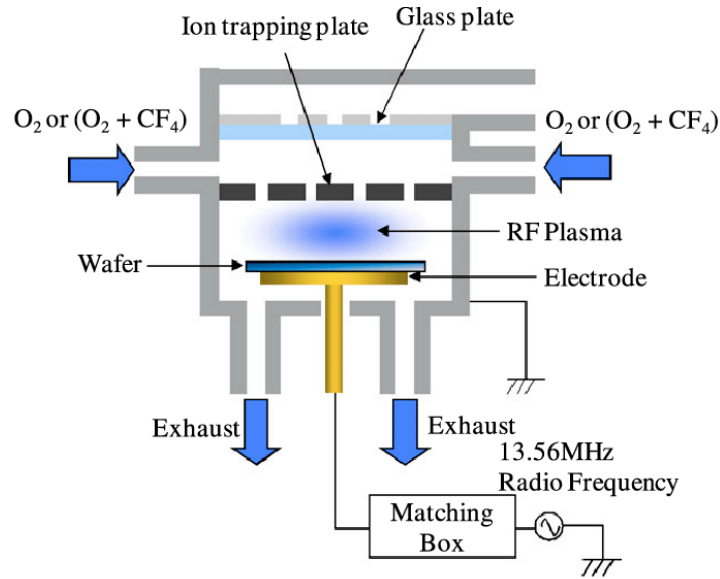


Figure 2.9: Schematic diagram for reactive ion etching (RIE) plasma system. ³²

A chemical reaction occurs to etch the material on the wafer surface. Therefore, the by-products are then desorbed and removed from the substrate leaving behind the desired, etched structures. Figure 2.10 describes one example of RIE for the case of Si etching by using CF_4 . ³¹

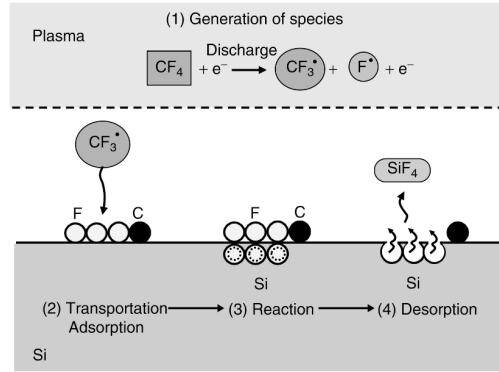


Figure 2.10: Si etching using CF_4 in RIE system. ³

CHAPTER 3

Electron Beam Lithography

3.1 Introduction:

Electron beam lithography (EBL) is the most popular direct writing nanofabrication technique for fabricating high-resolution nanostructures. Also, EBL is classified as a top-down nanofabrication method to produce nanostructures and nano-devices. Compared to conventional photolithography, EBL is much better. The advantage of EBL lies in the capability to create nano-scale features by eliminating the diffraction limit of light. Additionally, EBL is able to obtain very high resolutions due to the very short wavelength of an electron. There is also the flexibility to work with an assortment of materials. However, EBL also has drawbacks including expense, speed, and complexities. In EBL, a pattern is created on a sensitive resist by applying a focused e-beam at desired locations on the resist in order to change the local chemical properties, and the desired pattern on the resist is etched in order to transfer structures to the substrate.³³ In this work, EBL is the main technique that was used. Thus, the focus of this third chapter will be on the working principle of EBL that leads to high-resolution features.

Electron beam lithography has been developed and evolved over the years. For example, electron projection lithography is an advanced EBL system.^{33,34} However, there are two types of e-beam systems: scanning lithography and projection lithography. Figure 3.1 and Figure 3.2 are schematics of electron projection lithography and electron beam lithography and illustrate the differences between them. The difference lies in the focused

beam of electrons. In scanning electron beam lithography, the pattern can be written on the resist by a concentrated beam of electrons. But for projection electron-beam lithography, there is no focused beam of electrons. Here, the whole image can be achieved during one exposure of a vast unfocused flux of electrons (see Figure 3.1). Therefore, projection EBL is easier than scanning electronic microscopy, and projection EBL has higher throughput. The next section will discuss the EBL system.

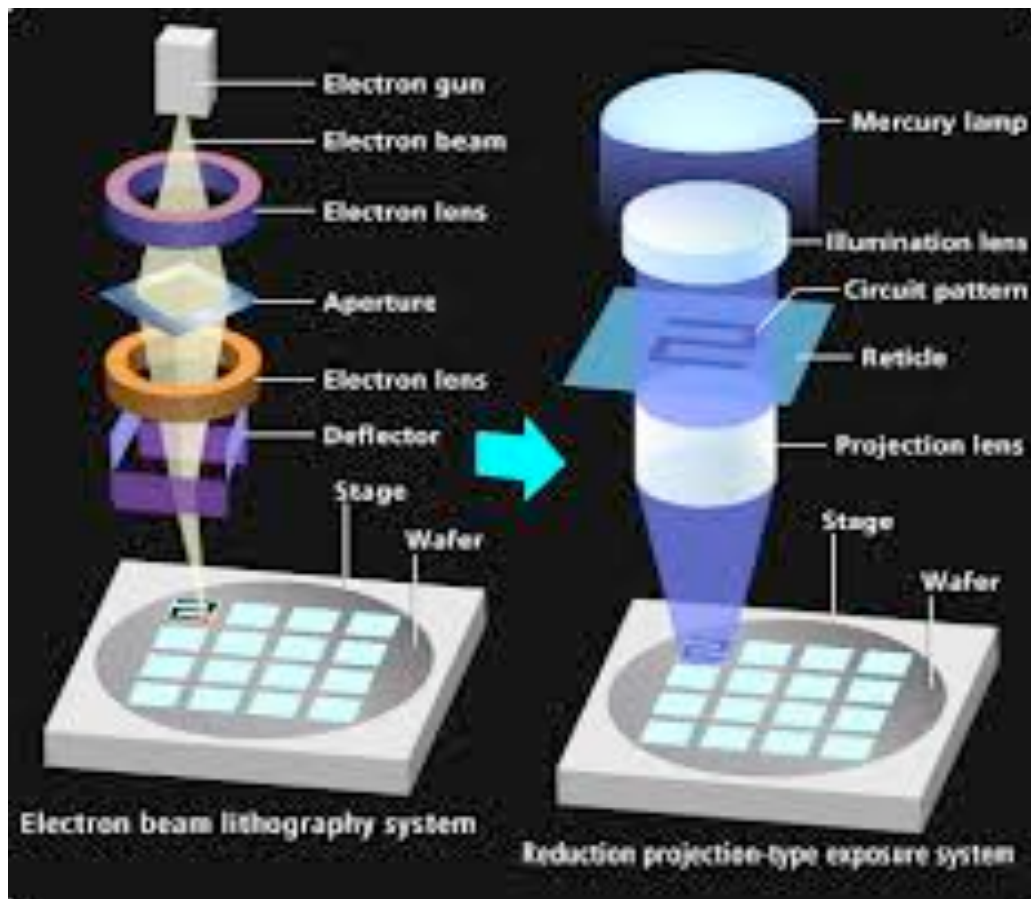


Figure 3.1: Advanced electron projection lithography compared with e-beam lithography system.³⁵

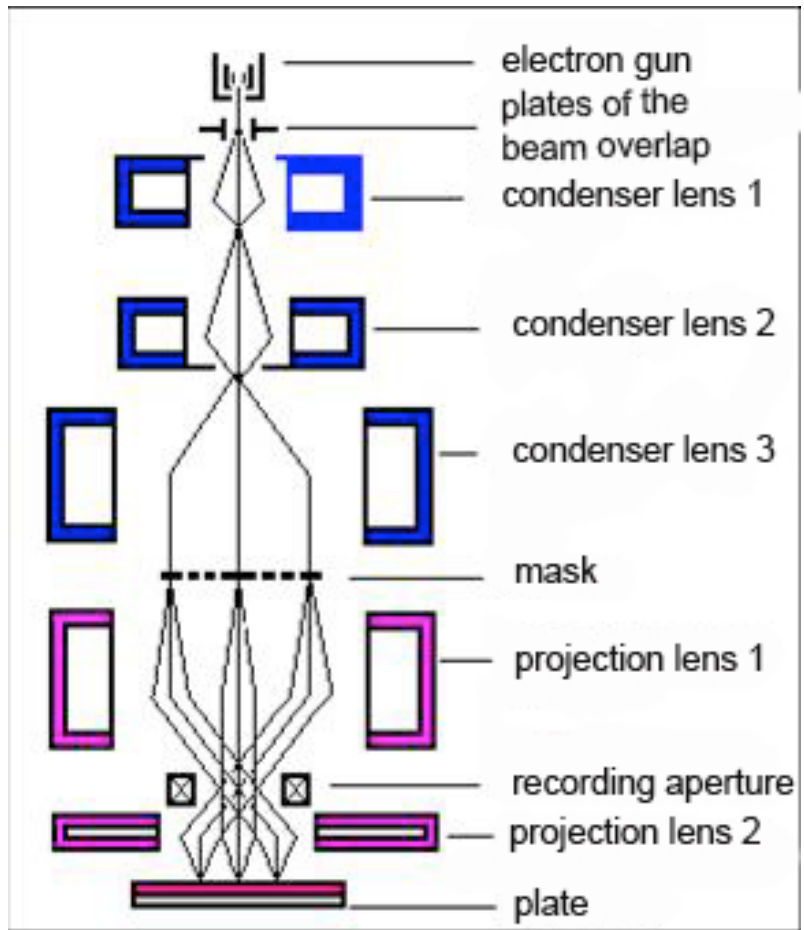


Figure 3.2: Schematic of electron projection lithography system. ³⁶

3.2 Instrumentation:

As illustrated in Figure 3.3, the electron beam lithography system is comprised of three major components including the chamber, column, and lithography control system (control electronics). ³⁸ The essential part of the EBL technique is the column that forms and controls the electron beam. The EBL column typically consists of various parts, such as an electron source, a series of electromagnetic lenses, a mechanism for deflecting the beam, a beam blander, apertures, a stigmator, and an electron detector.

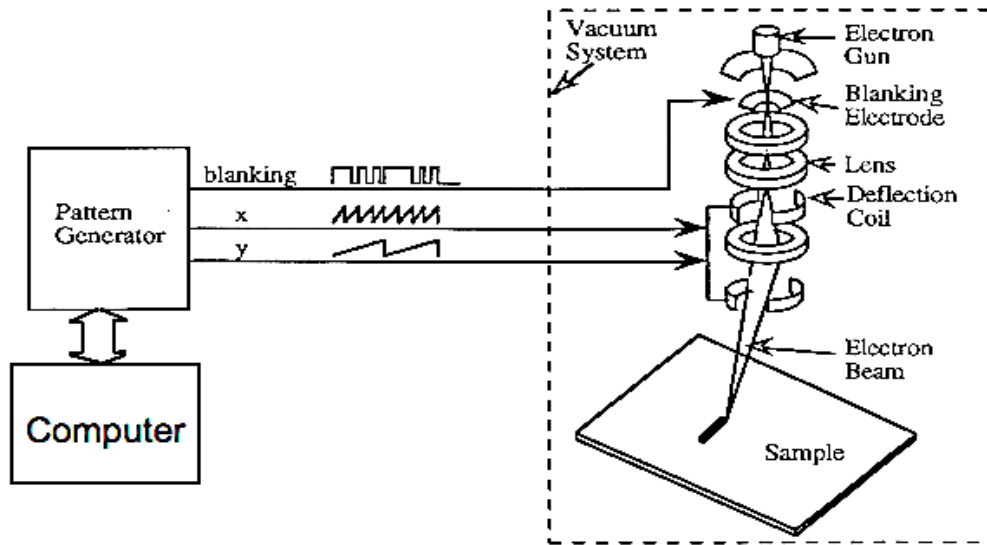


Figure 3.3: Schematic of e-beam lithography system and scanning electron microscopy.³

Initially, the electron gun generates an e-beam, which is accelerated and condensed to a fine probe or spot to expose the resist at its surface. The acceleration voltage for emitting the electron beam ranges from 1- 100 kV, which occurs between the cathode and the anode. The e-beam can be controlled by the blunker that can turn the beam on or off to prevent the resist from being exposed during the beam movement. The aperture aims to determining the spot size of electron beam. The beam flux then goes through an electromagnetic lens to form and deflect the passing e-beam. The electromagnetic lenses contain a condenser lens and one objective lens. Regarding the function of these lenses, the condenser lens reduces the electron beam diameter, while the objective lens focuses the electron beam on a nanometer scale. Also, there are stigmator and alignment systems, which help correct astigmatism and focus the beam. Moreover, these processes happen in a high vacuum in order to assist the electron's trajectory to follow and travel in a straight path without any collision with gas molecules.³⁹ There is

also a chamber that is located underneath the column and connected to the vacuum system. The chamber consists of a sample stage that allows for the loading and moving of the sample. Finally, there is a computer that controls the system to do all these procedures. The computer also performs other functions, such as sending the pattern data to the pattern generator, and aligning and focusing the electron beam. Figure 3.4 shows a picture of a typical commercial EBL system.³⁷



Figure 3.4: Electron beam lithography system.³⁷

3.3 Limitations of Electron Beam Lithography (Spot Size):

Despite the fact that EBL is the most appealing technique among the others, it suffers from several limitations. A small spot size is one of the major EBL limitations. The spot size issue occurs due to the expansion and deformation of the beam spot as a result of various deflections of electron optics. The two critical aberrations of electron

beam lithography and microscopy are spherical and chromatic deflections.⁴⁰ The ideal definitive electron spot size is given by:⁴¹

$$d_o = \frac{d_v}{M} \quad (3.1)$$

Where: d_v is the virtual source diameter, and $M (>1)$ is demagnification by the lenses. However, the final minimum beam diameter size limited by the chromatic aberration is given by:

$$d_c = C_c \frac{\delta V}{V} \alpha \quad (3.2)$$

Where: V is the accelerating potential, and C_c is the coefficient of chromatic aberration. The diffuse energy of the electron (eV) causes chromatic aberration. This leads to complications in focusing because the electron lens cannot focus the electrons with higher energy and cannot reach their focal points.³

In contrast, there are electrons that cross the external regions of an electron lens. These electrons possess a shorter focal length. As a result, spherical aberrations appear. The final minimum beam diameter size limited by spherical aberrations is given by:

$$d_s = 0.5 C_s \alpha^3 \quad (3.3)$$

Where: C_s is the spherical aberration coefficient.

If the spherical aberration coefficient is nearly equal to the lens focal length f , a well-designed magnetic lens can be obtained.⁴²

Therefore, by adding the previous factors in one equation to present the final beam spot size (d_i), the following equation is obtained:

$$d_i^2 = d_o^2 + d_c^2 + d_s^2 \quad (3.4)$$

The beam current, accelerating voltage, and lens-to-sample spacing are three keys for controlling the diameter of the beam. As a consequence, a high-resolution pattern of electron beam lithography is achieved with high voltage, low beam current, and small working distance.⁴³ Also, there is another factor that should be considered which is the wavelength of the electron. When the wavelength and the spherical aberration decrease, the probe size also decreases, leading to a small current. However, at low accelerating voltages, the contribution of chromatic aberrations cannot be ignored in the range of 2 kV or below.⁴⁴

3.4 Electron Scattering and Proximity Effect:

Other issues of EBL include electron scattering and the proximity effect. When the electron beam hits the surface of the resist and substrate, the high-energy electrons will lose energy and get scattered. Thus, there are two main types of electron scattering: forward scattering and backscattered electrons. The forward scattering of electrons is inelastic (electron-electron interactions) with angles less than 90° . In this type of scattering, high energy of electrons generates secondary electrons with low energy during the penetration of the resist. The second type of scattering is backscattering which is elastic scattering with angles greater than 90° . The backscattering of electrons happens

primarily in the substrate and the scattered electrons are emitted into and through the resist.⁴⁵ Figure 3.5 shows the two types of scatterings and electromagnetic radiations.

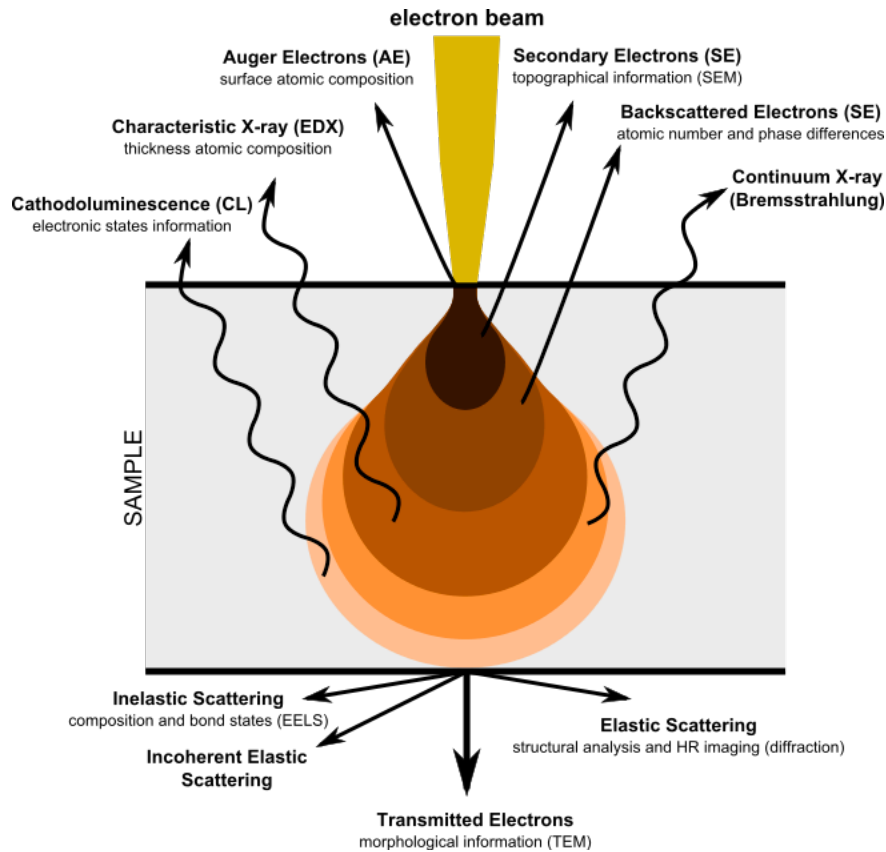


Figure 3.5: Interaction of electrons including BSE and SE with coating sample.⁴⁶

Therefore, the primary beam electrons lose their energy due to the implementation and interaction with the resist and substrate. However, backscattered electrons have a major impact on the exposure of the resist pattern because the deflected electrons can generate an additional exposure underneath the resist surface. At a high voltage, the backscattering range becomes large and detrimentally affects the pattern features. This phenomenon is called proximity effect. For instance, various energies of 1-20 keV were incident in a 500

nm thick polystyrene resist that was coated on a bulk silicon substrate to illustrate the electron trajectories as shown in Figure 3.6.⁴³

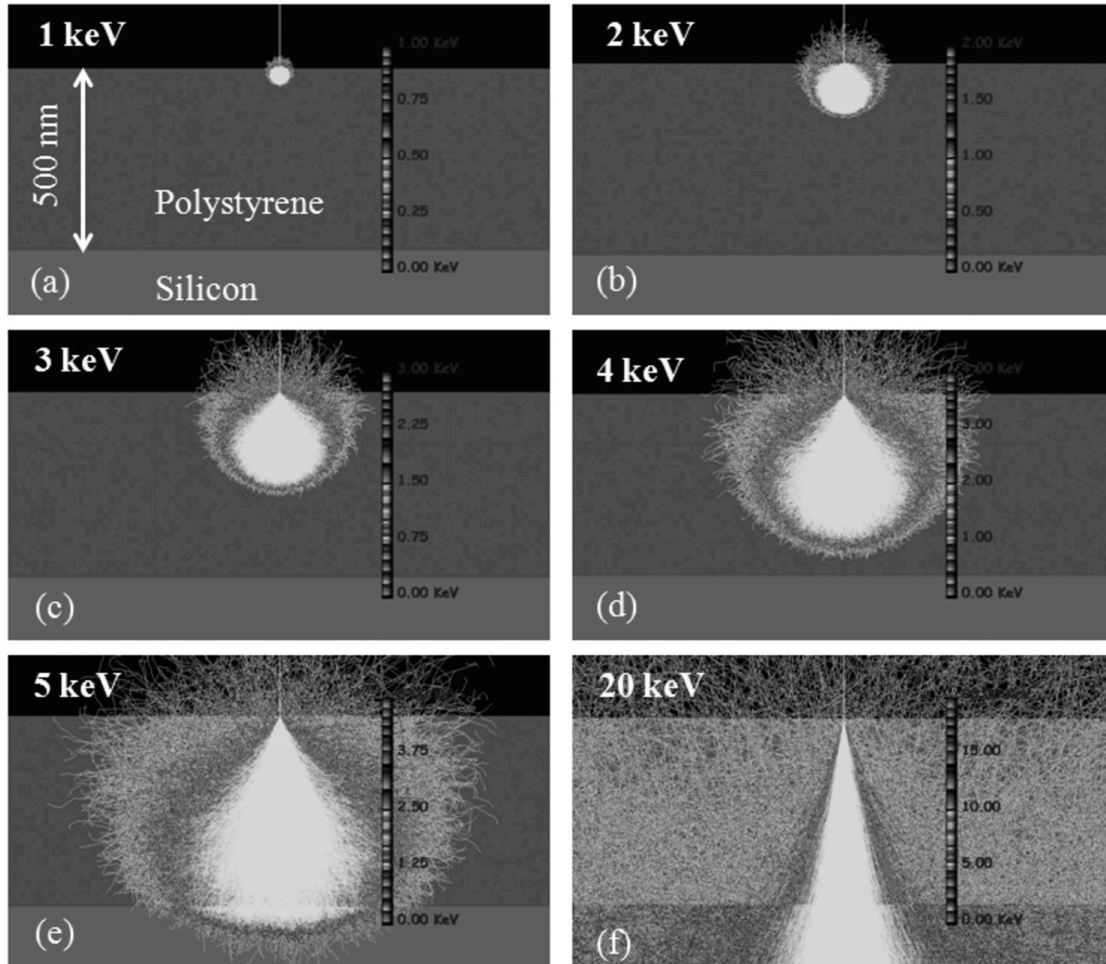


Figure 3.6: The electron trajectories in polystyrene resist with different energies.⁴³

There are several methods to minimizing or eliminating the proximity effect. For instance, the design pattern can be modified by removing or adding the appropriate pixels (see Figure 3.7). In addition, knowing the target exposure dose before performing the exposure assists in eliminating the proximity effect. The aim exposure dose can be known by using some software programs, such as a numerical simulation.

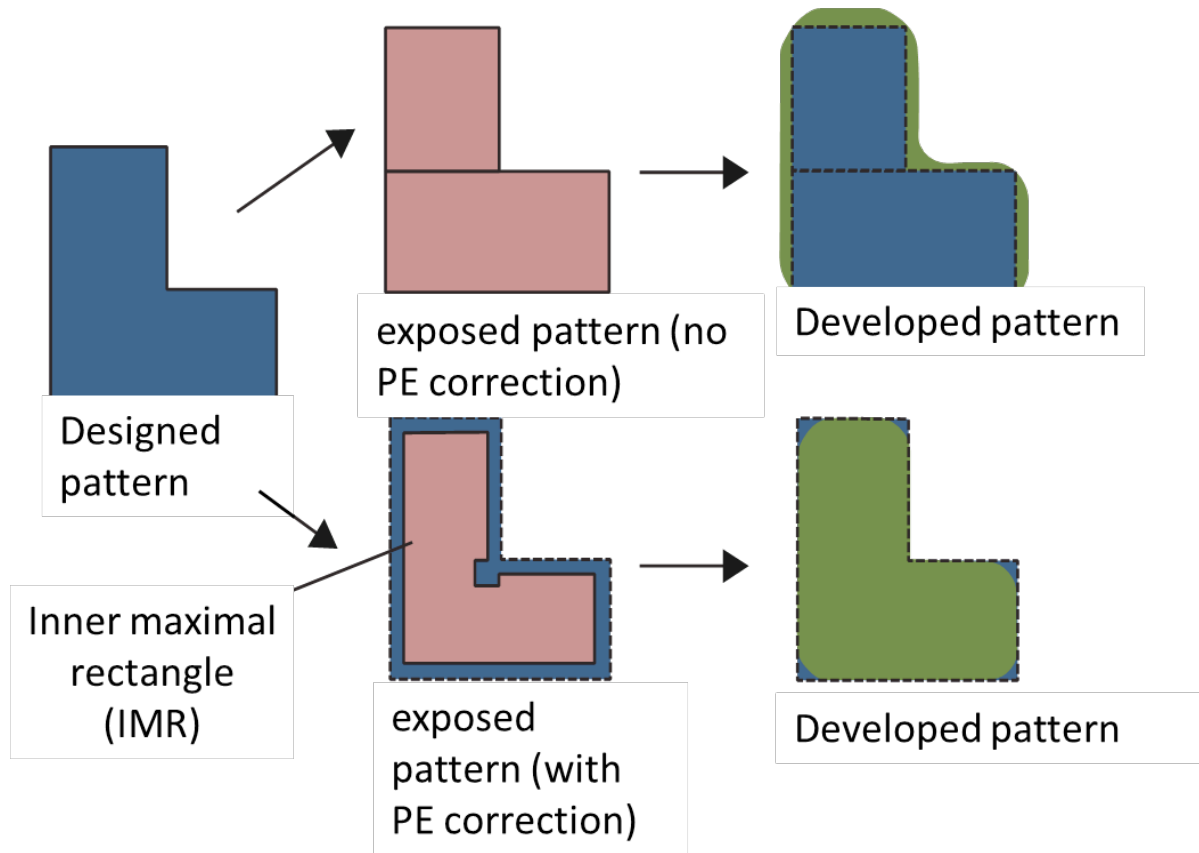


Figure 3.7: Proximity effect (PE) correction by shape modification at critical points.²

3.5 Electron Beam Lithography Resists:

In this section, various types of resists that can be employed with EBL will be discussed. Fundamentally, the resists that can be utilized in EBL are electron-sensitive materials. EBL resists can be divided into two groups: positive and negative tone resists.

Table 3.1 presents the list of EBL resists and their characteristics.⁴⁷

Common EBL resists with their properties and uses

Resist	Supplier	Tone	Sensitivity ($\mu\text{C}/\text{cm}^2$) at 100kV	Developer(s)	Characteristics
PMMA (high molecular weight)	Microchem	Positive	900	Cellosolve Methanol 3:7 or MIBK:IPA1:3 or IPA:Water (conc. varies)	High resolution, single layer or top of Hi/Lo bilayer, liftoff
PMMA (low molecular weight)	Microchem	Positive	800	Cellosolve Methanol 3:7 or MIBK:IPA1:3 or IPA:Water (conc. varies)	High resolution, bottom of Hi/Lo bilayer, liftoff
Copolymer (MMA/MAA)	Microchem	Positive	300	Same as above	Large undercut profile for liftoff when used as bottom layer with PMMA on top
Zep520	Zeon Chemicals	Positive	300	Hexyl Acetate, n-Amyl Acetate, or Xylenes	High resolution, good etch resistance
Zep7000	Zeon Chemicals	Positive	80	3-Pentanone Diethyl Malonate	Fast, good for making masks
NEB31	Sumika Materials	Negative	80	0.26N TMAH	Fast, chemically amplified resist
H5Q	Dow Corning	Negative	1000	0.26N TMAH	High resolution, good etch resistance, flowable oxide
Calixarene	Synthesized	Negative	10 000 or higher	Xylenes, IPA, MIBK	High resolution, good etch resistance

Table 3.1: Popular e-beam resists and their characteristics.⁴⁷

The e-beam first exposes a desirable pattern on the resist. Then, the pattern on the sample is developed in a solvent. The difference between positive and negative resist can be seen in Figure 3.8. In positive e-beam resist, the exposed areas will be easily removed after development in the developer solution due to the weak-resist polymer chain scission. On the other hand, the unexposed regions will remain. The most widespread positive tone e-beam resist is polymethyl methacrylate (PMMA) and ZEP-520. Unlike positive e-beam resist, the exposed areas of negative resist are not soluble in its solvent. The exposure causes cross-linking in the resist and thus the unexposed areas of the resist will be dissolved, leaving behind the desired pattern. Polystyrene (PS) is an example of negative e-beam tone resist. Figure 3.9 illustrates the chemical component of PS resist.

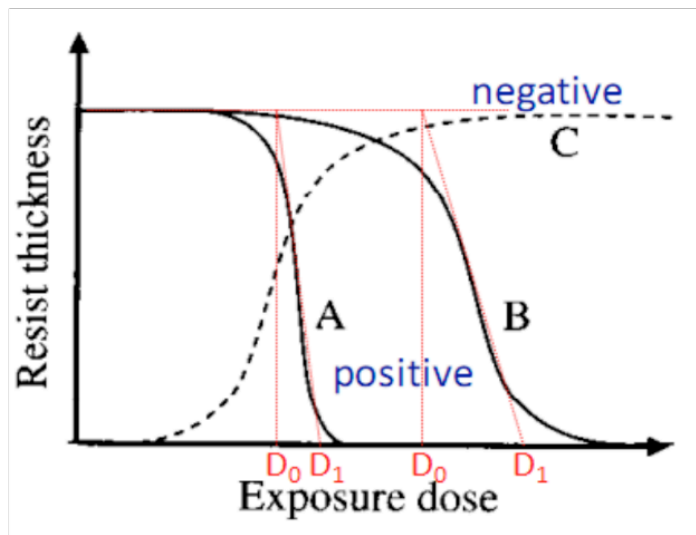
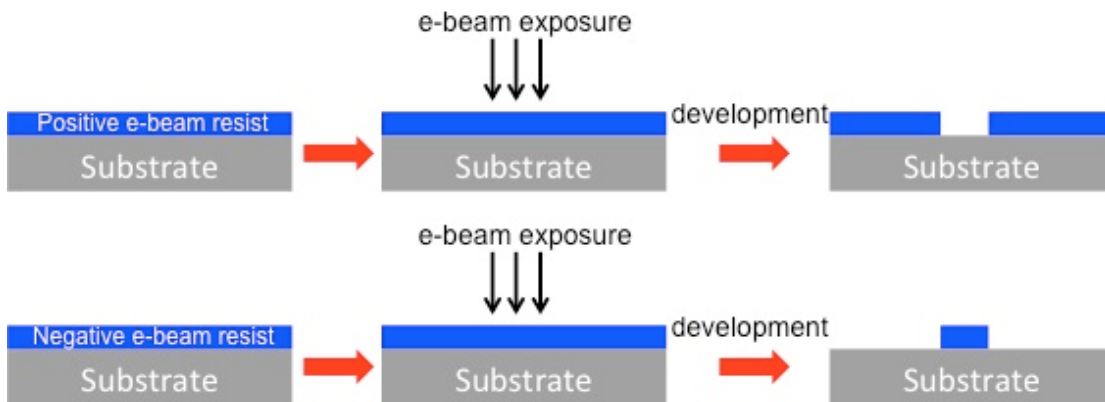


Figure 3.8: The schematic diagram and contrast curves for positive and negative resist.⁴⁸

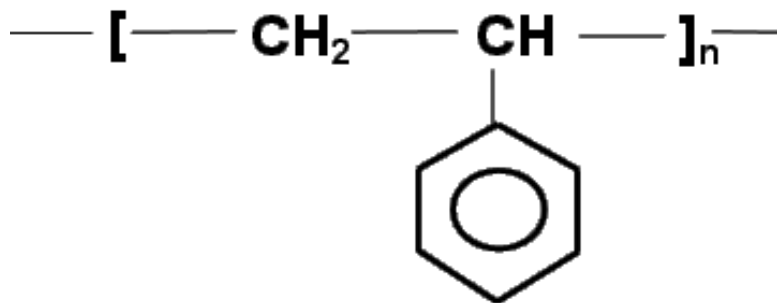


Figure 3.9: the chemical structure of polystyrene.⁴⁹

CHAPTER 4

High Aspect Ratio Polystyrene Structure Fabrication Using Electron Beam Lithography

Introduction:

The fabrication of stabilized high aspect ratio (HAR) nano-structures^{1,2} plays a very important role in various applications, such as MEMS/NEMS and especially BioMEMS. These applications demand nano-pillars with sub-micrometer feature sizes. To etch HAR structures require a thick resist as the etching mask. However, the tall resist pattern is often unstable, suffering from collapse and detachment right after the development due to the strong capillary forces. Deformation of the patterns is caused by lopsided capillary forces among HAR nano-pillars during the drying process.

The capillary forces are those which allow liquids to flow in confined areas even when there are no external forces to support them. The reason for liquid flow is the integration and combination of adhesion (intermolecular forces) between the liquid and surrounding solid surface, and the surface tension (cohesion within the liquid) as shown in Figure 4.1. Jurin's Law illustrates this by the equation:³

$$h = \frac{2\gamma \cos \theta}{\rho g r} \quad (4.1)$$

Where γ is the liquid-air surface tension (force/unit length),

θ is the contact angle,

ρ is the density of the liquid (mass/volume),

g is the local acceleration due to gravity (length/square of time),

h is The height of a liquid column, and r is the radius of the tube.

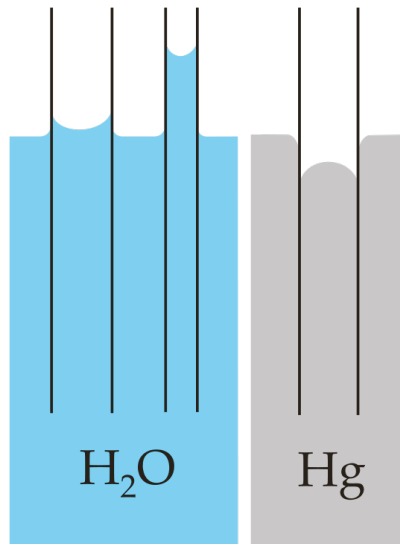


Figure 4.1: The capillary force action.³

The surface tension γ is one of the reasons for deformation in resist nanostructures. It presents a difference of pressure at the liquid-air interfaces. This phenomenon is defined as Laplace pressure and is given by the equation:⁴

$$\Delta P = \frac{2\gamma \cos \theta}{S} \quad (4.2)$$

where θ is the contact angle between the rinse liquid and the resist sidewall and S is the trench width. This is shown on the left side of Figure 4.2.

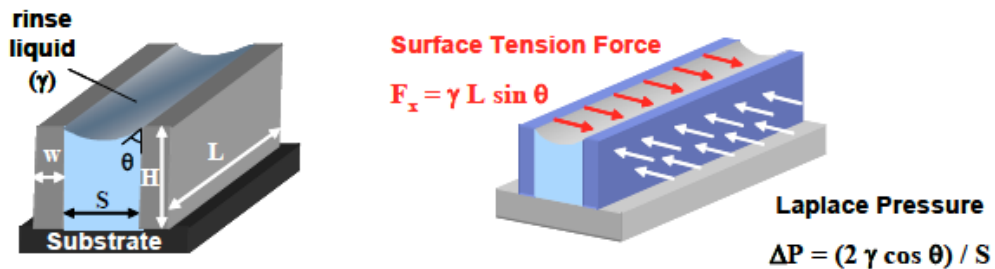


Figure 4.2: A three-dimensional diagram of surface tension.⁴

The diagram shows the parameter of the surface tension on two parallel resist patterns, width W , length L , height H , separated by a narrow space of width S . The gap between the two patterns S is completely filled with the rinse liquid. The surface tension force (STF), F_x , acts on the resist sidewall. This is given by the equation:

$$F_x = \gamma_{LV} L \sin \theta \quad (4.3)$$

where L is the length of the resist line. It is worth noting that the differential pressure ΔP is applied to the entire pattern sidewall, whereas F_x is exerted only at the contact line between the rinse liquid and the resist feature (see Figure 4.2 left side).⁴

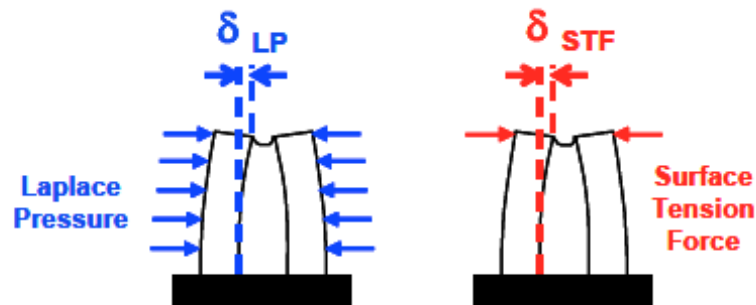


Figure 4.3: Schematic of the pillars displacement generated by Laplace pressure and STF.⁴

Throughout the developing process, the developing liquid remains between the nanostructures. Since the adhesion force of the liquid on the resist pattern is stronger than the surface tension of the developer, the curve of the surface liquid is affected by both the Laplace pressure and surface tension force. This leads to the pattern displacement (δ) that is caused by (δ_{LP}) and (δ_{STF})⁵ as demonstrated in Figure 4.3.

For micro-nanoelectronics applications, this becomes a critical issue for maintaining the tall pillars (high aspect ratio) and the fine-pitch of resist patterns. It is a

challenge to keep high aspect ratio nanostructures standing without collapse. Theoretical analysis and technical processes are the two general ways which attempt to avoid pattern collapse.⁷ There are three different strategies to solve this matter including increasing the resist stiffness, eliminating surface tension during the drying phase, and utilizing supercritical fluids.⁸ Despite the fact that they are able to eliminate the surface tension during the developing process, there are still limitations. Alternatively, the capillary force can be reduced by adding a final rinse for modified development using a selective solvent that provides an adequate large contact angle θ .⁹ Lastly, there are numerous other techniques that have been reported to prevent the tall patterns from deformation and collapse, such as auxiliary drying.¹⁰

Nanoimprint lithography (NIL), focused ion beam (FIB) lithography, soft lithography, nanosphere lithography, and electron beam lithography (EBL) have presently been the most commonly utilized techniques for the fabrication of nanostructures.¹¹ EBL is a unique method among the other nanolithography techniques that is able to fabricate nanoscale structures, especially those with high aspect ratios (HAR).¹² In addition, the resist can be classified into two types: positive and negative. However, the EBL resist should have some required properties, such as high sensitivity, high contrast, and high dry etching selectivity.¹³ There are a variety of positive and negative resists for EBL. Of these, SML resist which is a novel polymer that has been specifically designed to answer the demands of the EBL community, hydrogen silsesquioxane (HSQ), and polystyrene (PS) have recently attracted more attention.

In this chapter, a new technique for reducing the distortion/deformation of high aspect ratio nanostructures to prevent tall pattern collapse is presented and described.

Such high aspect ratio structures can be patterned using conventional electron beam lithography followed by conventional etching of the substrate/sub-layer, ideally using a negative resist such as polystyrene.

Experimental Section:

Polystyrene resist was chosen because it is a very versatile and popular negative resist, offering an ultrahigh resolution with low molecular weights, and ultrahigh sensitivity for high molecular weight. A molecular weight of 700 Kg/mol of polystyrene (solid), dissolved in 130 ml anisole was required for a 15% polystyrene solution with a thickness of 2 μm . In order to obtain a homogeneous solution, the PS solution was put on a hotplate at low temperature 30-50° C for 2 hrs. Then it was left for 24 hours (overnight). After solvent cleaning with acetone and isopropanol alcohol (IPA), the silicon surface was activated by oxygen plasma reactive ion etching (RIE) with 20 Scm, 20 W RF power, and 20 mTorr pressure for 1 min. Directly coating PS onto the silicon substrate is not optimal due to its weak adhesion. In order to enhance the adhesion, a thin monolayer of the polystyrene (PS) brush layer (PS-COOH) was deposited because the -COOH group can enhance the grafting process.³ The PS-COOH brush was used with a molecular weight of 0.5 g/mol dissolved in 10 ml of Xylene. The coating of PS-COOH was achieved by spin-coating the sample at 4000 rpm for 40 seconds. When this was completed, the sample was baked for 24 hours at 160° C to induce a chemical bond between the polymer and the substrate surface (-Si-O-C- for silicon substrate). After that, the sample was dipped in xylene for 1 min to remove the unbound bulk polymer, leaving behind a very thin monolayer of approximately 10 nm in thickness.

Next, the silicon wafer was sequentially coated with thick PS by spin-coating at 2000 rpm for 40 seconds and then baked at 180° C for 10 min to give a final film thickness of 2 μm , as measured by a Dektak profilometer. Then, a Leo 1530 scanning electron microscope was used for electron beam lithography. A Raith beam blanker and nanometer pattern generation system (NPGS) are connected to the Leo 1530 SEM (Scanning Electron Microscopy).

As seen in Figure 4.5, our method to overcome the HAR resist structure collapse or detachment issue is by using a “ceiling” to hold the HAR structures. The ceiling is formed by low energy (e.g. 4 keV) electron beam exposure that will only cross-link the upper part of the PS. When the ceiling size and the gap between adjacent ceiling patches are well designed, the solvent developer can still enter through the gap underneath the ceiling to dissolve the uncrosslinked PS there. After development and drying of the rinsing liquid, the ceiling patches can be removed by oxygen plasma etching.

To start the process, EBL is used to write the nanopatterns at an acceleration voltage of 20 keV, and 4 keV cross-link only the superficial layer (top 200-300 nm) as a ceiling to hold the tall pillars. The first writing is the nanopillars with area doses of 600 $\mu\text{C}/\text{cm}^2$, and 40 $\mu\text{C}/\text{cm}^2$ for the ceiling with a beam spot size of 30 nm. The pattern consists of 4x4 arrays of pillars with line spaces of 1 μm as shown in figure (4.4). After exposure, the pattern was developed in xylene for 3 min at room temperature and rinsed with IPA before drying. Xylene is one of many solvent developers that can dissolve unexposed polystyrene. The final stage is removing the top layer (roof) through oxygen plasma RIE (20 Sccm, 20 mTorr pressure, and 20 W power) leaving behind tall PS pillars that do not collapse as schematically illustrated in Figure (4.5).

In order to obtain a specific electron penetration depth in the resist at low and high-energy exposure, we carried out a numerical simulation with Casino v3. The software is based on Monte Carlo modeling to obtain the electron trajectory in a solid, and it considers the interaction and generation of x-rays and backscattered and secondary electrons. In our simulation, the trajectories of 100,000 primary electrons were simulated, from which we deduced the electron penetration depth into the resist at an electron energy of 2–20 keV.

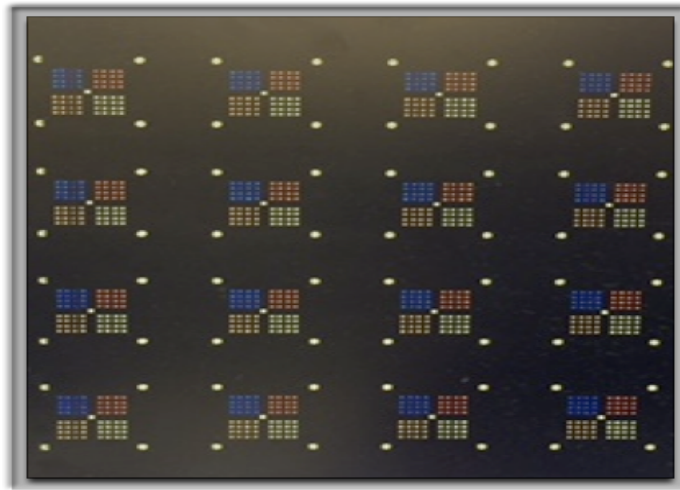


Figure 4.4: The nanostructures arrays.

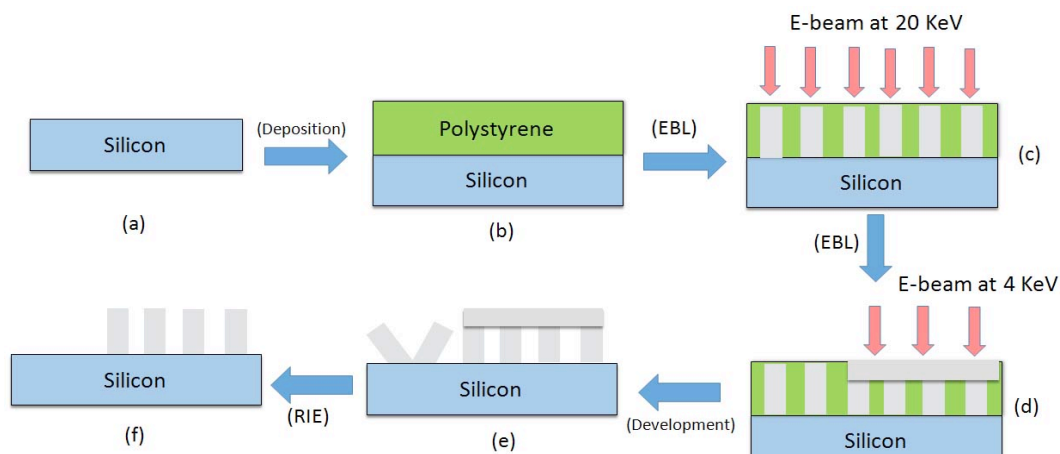
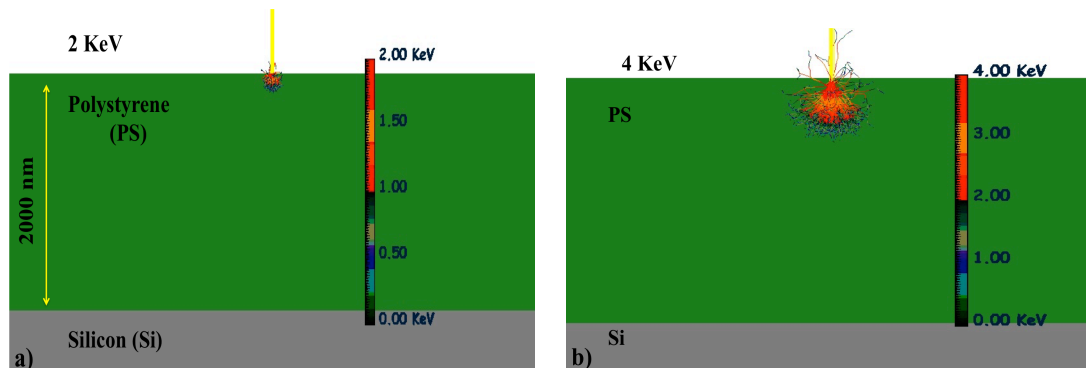


Figure 4.5: Process steps for patterning stabilized high aspect ratio polystyrene nanostructures followed by high and low energy electron beam lithography.

Results and discussion:

The objective of this project is to minimize the HAR resist pillar collapse caused by capillary force when drying the rinsing liquid. This technique prevents the tall pillars of $\sim 2 \mu\text{m}$ height from falling down or detaching from the substrate by creating a cross-linked “ceiling” above the pillars using low energy exposure to hold the HAR structures.

To understand the procedure of exposure, an electron trajectory or numerical simulation is used in order to acquire the distribution of electron trajectories. As a result, a scattering volume and the electron penetration range are estimated. Secondary electrons (with energies of tens of eV) are generated as primary electrons (several KeV) and penetrate the resist. The secondary electrons have energies closer to that required to induce a chemical reaction. Thus they are mainly responsible for resist exposure rather than the primary electrons. The electron trajectories in $2 \mu\text{m}$ thick polystyrene that was coated on bulk silicon substrate are illustrated at different energies of 2, 4, 20 KeV (see Figure 4.6 below).



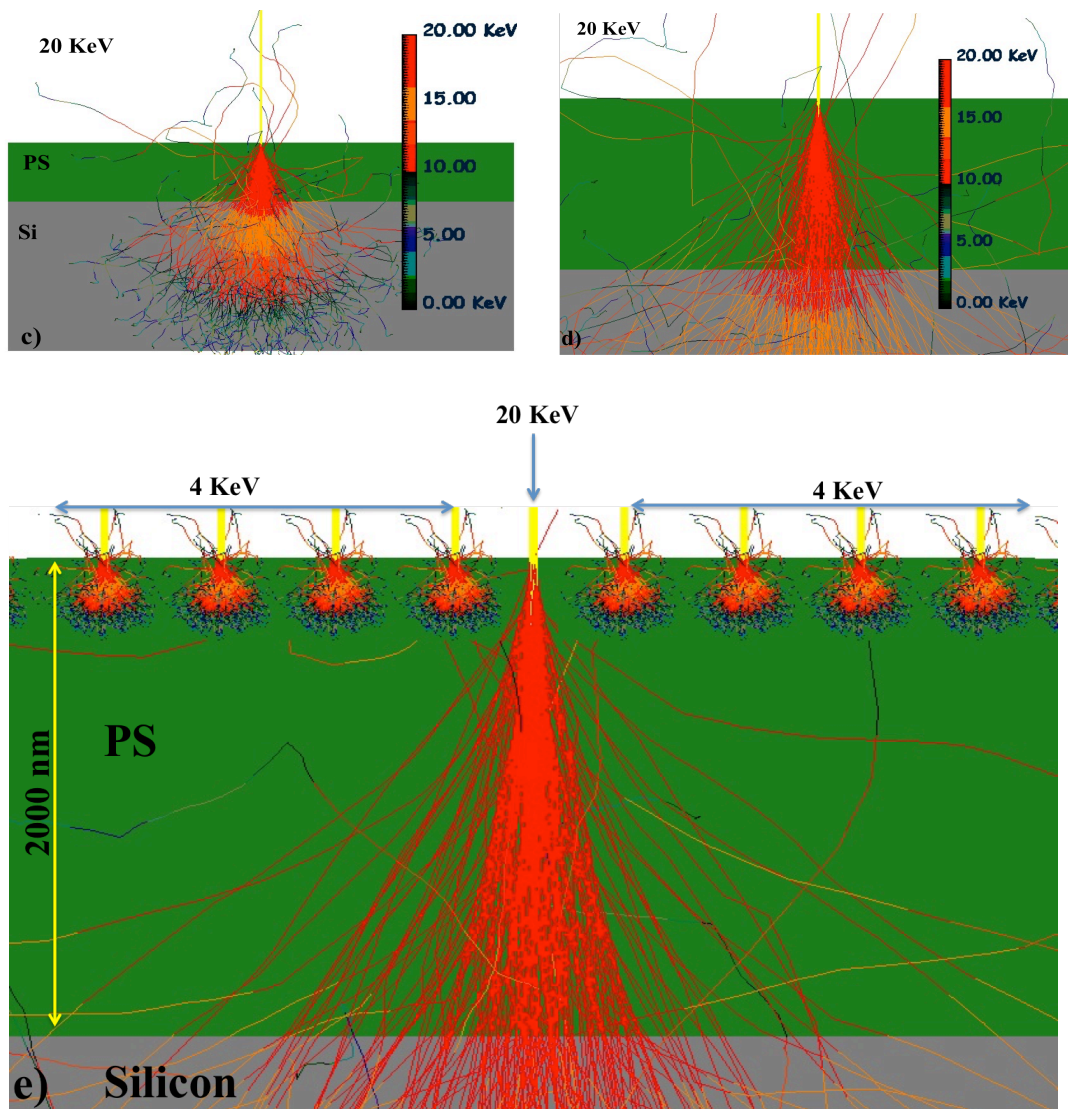


Figure 4.6: Monte Carlo simulation of 100,000 electron trajectories in 2000 nm thick polystyrene coated on silicon with electron energy of (a) 2 keV, (b) 4 keV, (c) 20 keV, (d) zoom of a tapered profile of 20 keV, (e) the ceiling with 4 KeV and pillar with 20 KeV.

At energies of 2 and 4 KeV, the electron trajectories over the polystyrene resist are shallow and forward scattering is significant. The electrons are also stopped before reaching the half thickness of the polystyrene resist. At 2 KeV, a depth of 220 nm in the

PS resist is roughly exposed and the electron penetration depth is much less than the resist thickness as shown in Figure 4.6 (a). Whereas in Figure 4.6 (b), a depth of 500 nm in the PS resist is exposed at 4 keV and this leads to the electron penetration depth of only a quarter of the PS thickness. Therefore, an undercut or underneath profile will be easy to obtain with the low energy exposure since the resist bottom (near the substrate) is not cross-linked at that energy. At 20 KeV; however, most electrons penetrate deep into the substrate as shown in Figure 4.6 (c). As the PS resist is a negative resist, a tapered profile (wider opening) is typically formed due to electron forward scattering as illustrated in Figure 4.6 (d). The low electron energy exposes the top shallow part of the resist which leads to the formation of a ceiling, which is a crucial part in the work as shown in Figure 4.6 (e).

As a proof of concept, Figure 4.7 (a), illustrates that the polystyrene pillars on the left, without a “ceiling”, were all detached whereas the pillars on the right side, with a “ceiling”, all remained with some deformations due to the rinsing process. Since the capillary force is very strong, the ceiling was deformed and displaced as shown in Figure 4.7 (b). Hence, it requires the fabricating of large pillars at the ceiling corners to hold it more strongly. We believe that the pillar array can remain intact and stable throughout this development process under optimal conditions (Figure 4c). Pillars in Figures 4.7(c), 4.8 (a) were stable without collapsing or detaching from the substrate. However, the opposite result is found in Figures 4.7(b), 4.8 (b) in which some of the pillars had fallen down or adhered to each other and detached from the substrate as shown. Additionally, there appears to be sections of a residual ceiling that had adhered to both the substrate and the pillars, which resulted in contamination. Process optimization is required to

reduce the amount of residual that remains on the substrate surface, as seen on Figure 4.8 (a), and the pillars, as seen in Figures 4.7(c), 4.8 (b).

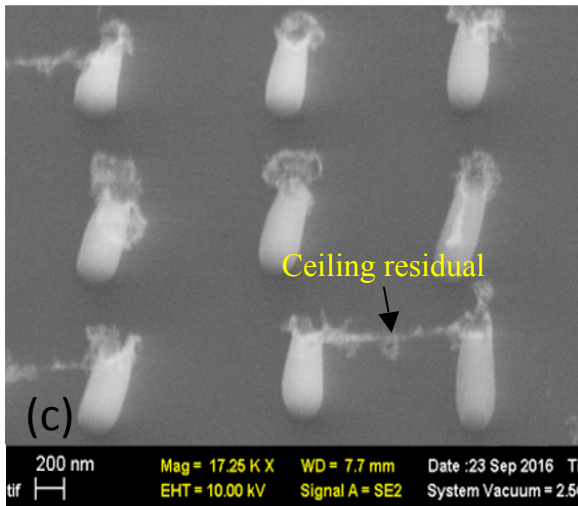
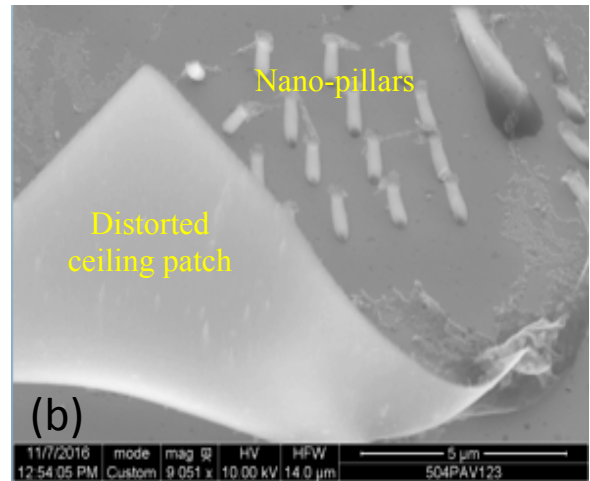
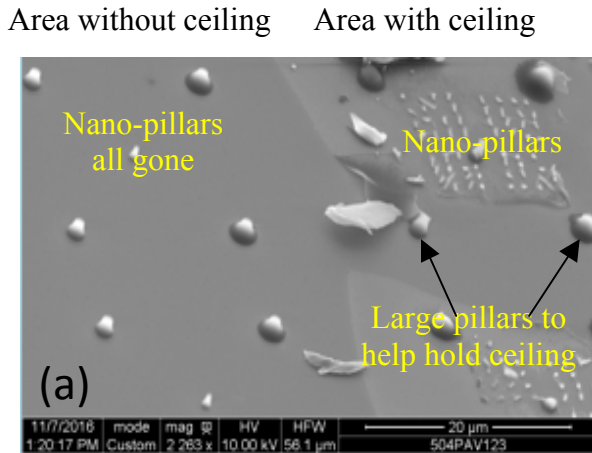


Figure 4.7: SEM images of polystyrene pillar array under the area originally without or with ceiling. (a) Low magnification view, showing all nano-pillars were gone if without ceiling, and remained if with ceiling; (b) In some area the ceiling is greatly distorted by the capillary force; (c) Array of 200 nm diameter pillars that survived the development process well.

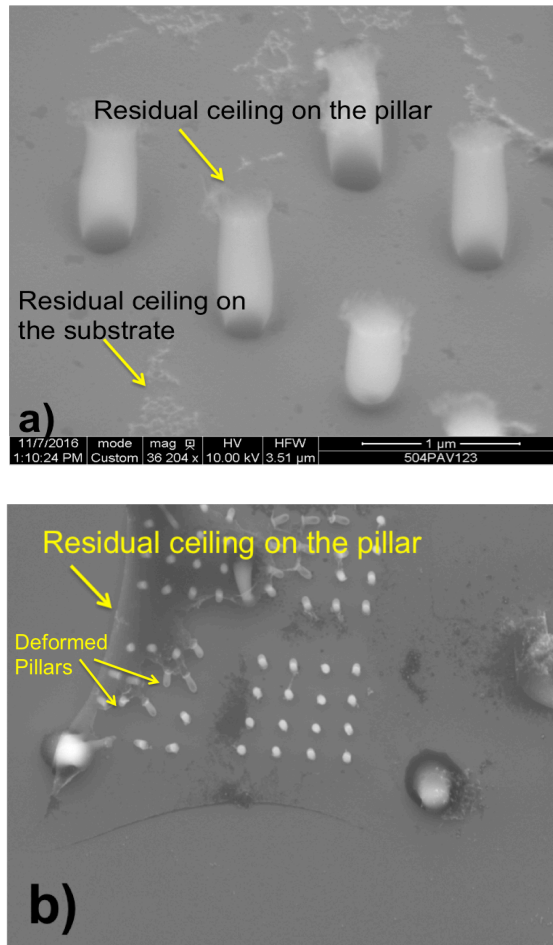


Figure 4.8: The remaining ceiling on the pillars and substrate surface.

Moreover, the ceiling was shifted and displaced from the original place, and this is clear in Figure 4.7 (b). However, the HAR nanostructures were also destroyed since some ceilings were greatly deformed and displaced and finally flowed over the nano-pillar areas. Clearly, Figure 4.8 (b) shows a 4-by-4 nano-pillar array that endured the fabrication process under the protection of the ceiling structure. The development of a structure to prevent the nano-pillars from collapsing as a result of capillary forces is underway and will be presented.

Conclusions:

We demonstrated that by using resist “ceilings” to hold the resist structures, tall nano-scale resist pillars can be obtained without collapse or detachment because of capillary forces. The ceilings were created by the low-energy exposure that penetrates into only the top part of the resist film. Ultimately, the possibility of fabricating upright high aspect ratio (HAR) nanostructures was proven by using this simple and very effective method. These stabilized high aspect ratio nanostructures have applications in various sectors, such as MEMS/NEMS and especially BioMEMS in particular.

Chapter 5

Nano-gap Electrodes

1-Introduction:

Narrow-gap structures have applications ranging from NEMS¹, Bio-MEMS², and SERS imaging³ to bio/molecular electronics⁴ etc. For a device to function properly, one needs to fabricate narrow-gap structures with a high degree of reproducibility.

In fact, the creation of bio/molecular electronics, which uses individual molecules as functional elements in electronic circuits, has been motivating researchers for a long time. The molecular-based devices are ideal choices for nano-electronics, as they have an assortment of specific electronic functions, and can be used for rectifiers, switches, and transistors. In addition, there are special advantages to these electronic applications including lower costs, higher efficiencies, flexibility, useful electronic properties and distinct optical properties, etc.¹³ However, these molecular devices are still far from commercialization, mainly due to the difficulty of fabricating nano-sized narrow-gap structures, which are necessary to connect molecular elements that bridge the gap with regards to the macroscopic elements of electronic circuits.

Fabricating narrow-gap structures is challenging and researchers have demonstrated a wide range of methods to produce structures with gaps in the nanometer range, which include electron beam lithography (EBL)⁵, electron-beam induced deposition⁶, focused ion beam (FIB) lithography^{4,7}, etc. Some other alternate methods, such as mechanical break junction⁸, electrochemical deposition⁹, electromigration methods¹⁰,

photolithography by post-annealing processes¹¹, etc. are also used to fabricate narrow-gap structures. Nevertheless, EBL is one of the more conventional techniques that is often connected to other machines part of the fabrication process for the nanostructures. EBL is employed in the first stage to achieve narrow gaps with widths of 10-20 nm in various methods of fabricating nanogap electrodes. For example, EBL technique was used in a mechanically controllable break (MCB) junction⁹, which is vastly utilized for single-molecule and single-atom devices. Additionally, electrochemical and chemical deposition is another method for fabricating nanogap electrodes.¹⁴ In this process, a special technique or system is not required and a gap with a distance ranging from several angstroms to 10 nm has conveniently been achieved¹⁵ and this is illustrated in Figure (5.1-b). Electromechanical deposition also has another feature, such as the ability to fabricate asymmetric nanogap electrodes with many fingers^{13,16} as shown in Figure (5.1-a). Electromigration and electrical breakdown procedures²⁰ are utilized to fabricate nano-sized gaps by using EBL. Electromigration is capable of creating gaps down to 1nm (Figure 5.1-c) that is especially used in preparing three-electrode devices. This method was recently used to create a new and simple technique for the simultaneous fabrication of nanogap electrodes called activation.¹⁹ Although it has these unique advantages, it has two main problems. Firstly, the excessive temperature generated during the formation of the nanogap must be controlled. Secondly, the metal debris in the process may interfere with the gap, which would block the demand signals.^{13, 12}

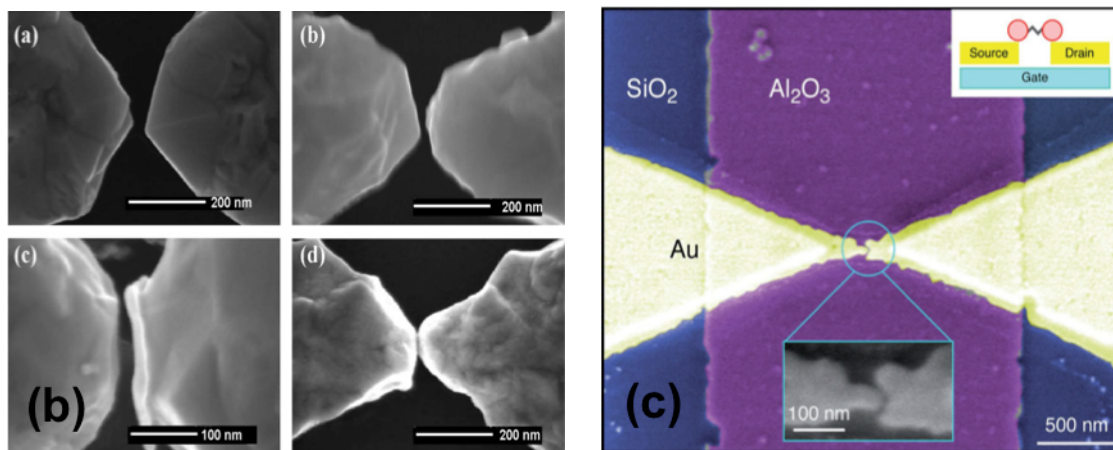
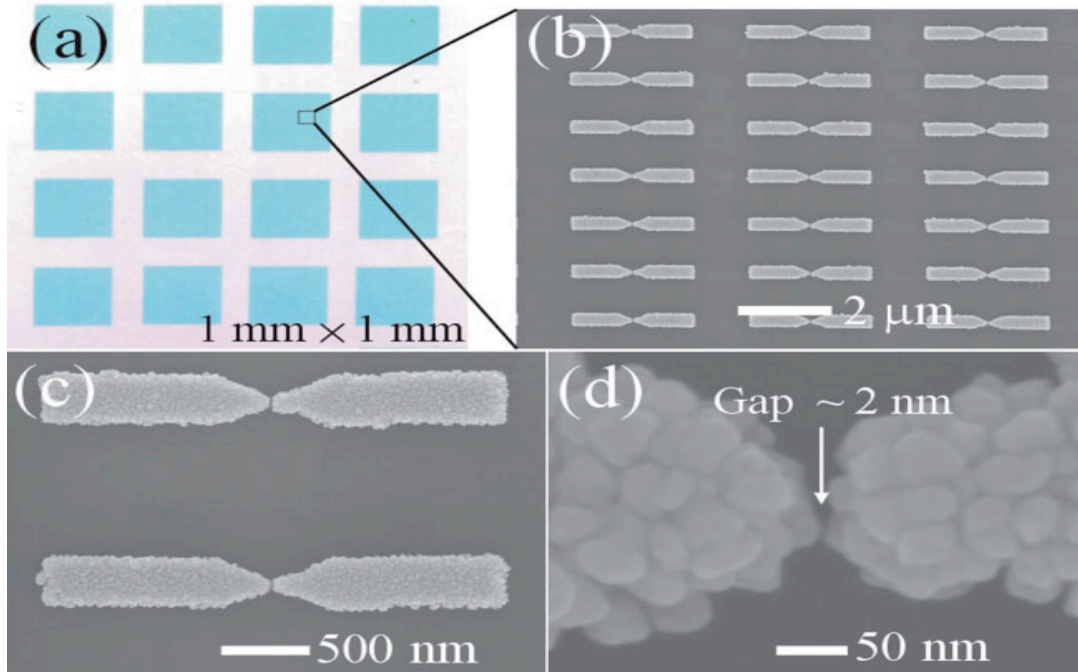


Figure 5.1: Various SEM images of fabricated nanogap electrodes. a) An array of nanogaps using chemical deposition technique. b) An image of the samples prepared using chemical deposition method. c) The two gold electrodes separated by ~ 1 nm using electron beam lithography and the electromigration-induced break-junction technique. Reproduced with permission from.¹³

Moreover, oblique angle shadow evaporation is another technique for nanogap fabrication that can locate the metal leads by combining shadow evaporation with electron beam lithography and optical lithography as shown in Figure 5.2.^{17,18}

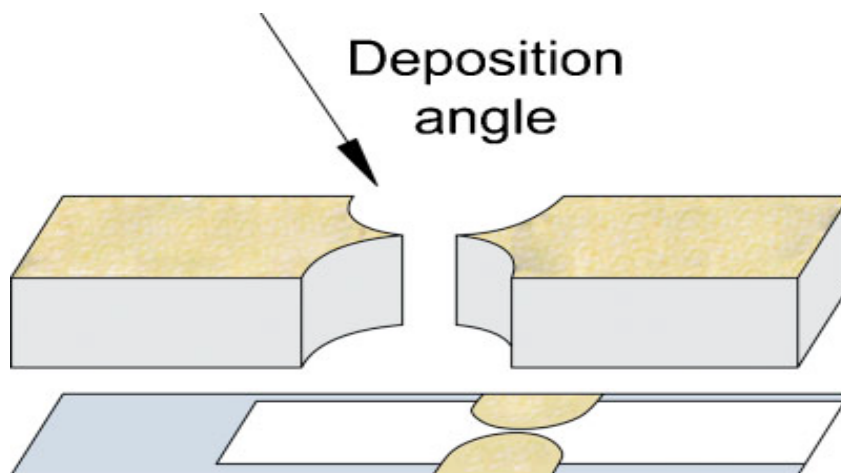


Figure 5.2: The schematic of oblique angle shadow evaporation technique with two masks to great space with a few nanometers.¹⁹

FIB lithography without dispute is a standard approach for the fabrication of nanostructures, such as nanogap electrodes.²¹ FIB lithography has several advantages that make it the most notable technique in this field. For instance, small beam size (roughly about 5-20 nm), high speed, good reproducibility and less proximity effect make FIB an appropriate and credible method for patterning nanogap electrodes.¹³ The spot size of the beam diameter seems to be very large compared to the desirable narrow gap below 10 nm. Therefore, a metal layer (i.e. Ti) can be used in some processes to shrink the nanogaps to narrower nano size of 3 nm.²² Various processes that have the ability to produce nanogap electrodes are also utilized in nano and single molecule devices.

However, all the previously mentioned methods suffer from some serious limitations. The drawbacks include complex procedures, high cost, and low throughput etc.^{23, 24} Electron beam lithography is one of these techniques that play a major role in different procedures of fabrication nanogap electrodes. Though EBL is a high resolution

and reproducible process, the proximity effect caused by backscattered electrons greatly limits the attainable gap size. One way to eliminate the proximity effect is to carry out EBL on thin electron-transparent silicon nitride membranes; this has achieved gaps in gold down to 3 nm⁽¹²⁾, yet the membrane is extremely fragile.

In this paper, we propose to fabricate nano-gaps using an optimized two-step exposure technique. As shown in Figure 5.3, we first used high energy (20 keV) exposure to define the nanogap between two thin lines, knowing that the proximity effect is negligible for isolated sparse patterns. Then we defined the large pad structure (which could be used as an electrode) using low energy (2.5 keV) exposure. Proximity effect will be very significant for such large microscale features, but the lateral backscattering range is small (100-200 nm) for this low energy, and thus the proximity exposure at the middle of the gap would be low if the two pads are separated by >100-200 nm. Therefore, with accurate alignment between the two exposures, a nano-gap between two large pads can be attained when the wide gap region is filled with a pair of thin lines having a nano-gap in-between.

2- Experiment:

In this experiment, a thin layer of PMMA resist (~ 30 nm) was spun on a Si wafer that was cleaned by acetone and IPA (isopropanol alcohol) followed by a brief etching (a few seconds) using O₂ plasma Reactive Ion Etching (RIE) with 20 Sccm, 20 W power, and 20 mTorr pressure. The coating was performed using spin coating. The sample was then baked at 180° C for a minimum of 10 min.

EBL was used to accomplish the exposures via two different energies. However, there are several steps that need to be considered while doing the e-beam exposure in order to obtain a fine nanostructure: high alignment accuracy, sample location, and high focus. In the proposed method, we exposed two different structures. In the first step, a square structure (order of 1 μm side length) was exposed with a low-energy beam (2.5 keV), and then, a long, thin rectangle (about 50 nm wide, many micrometers long) was exposed with a high-energy beam (20 keV).

After the exposures, the sample was developed in methyl isobutyl ketone (MIBK):IPA (1:3) for 20 seconds at room temperature. Alternatively, it can be developed at low temperature (-20°C) for 30 seconds. To obtain a high resolution and high contrast SEM image, a thin layer ($\sim 10\text{ nm}$) of Cr has been deposited.

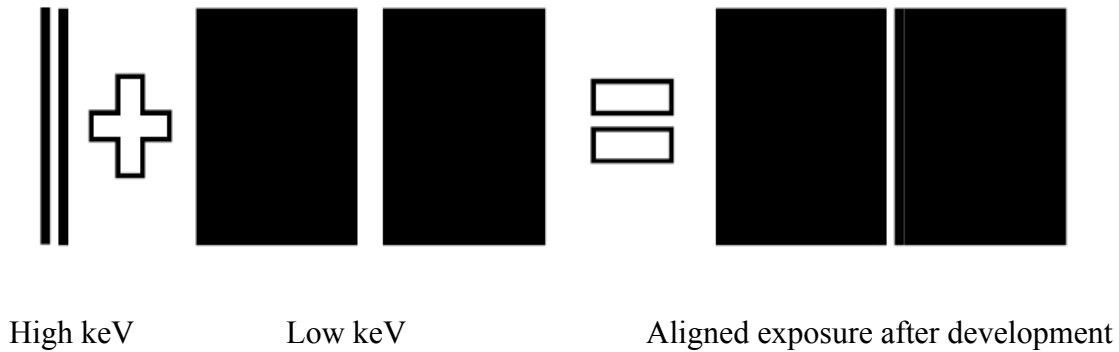
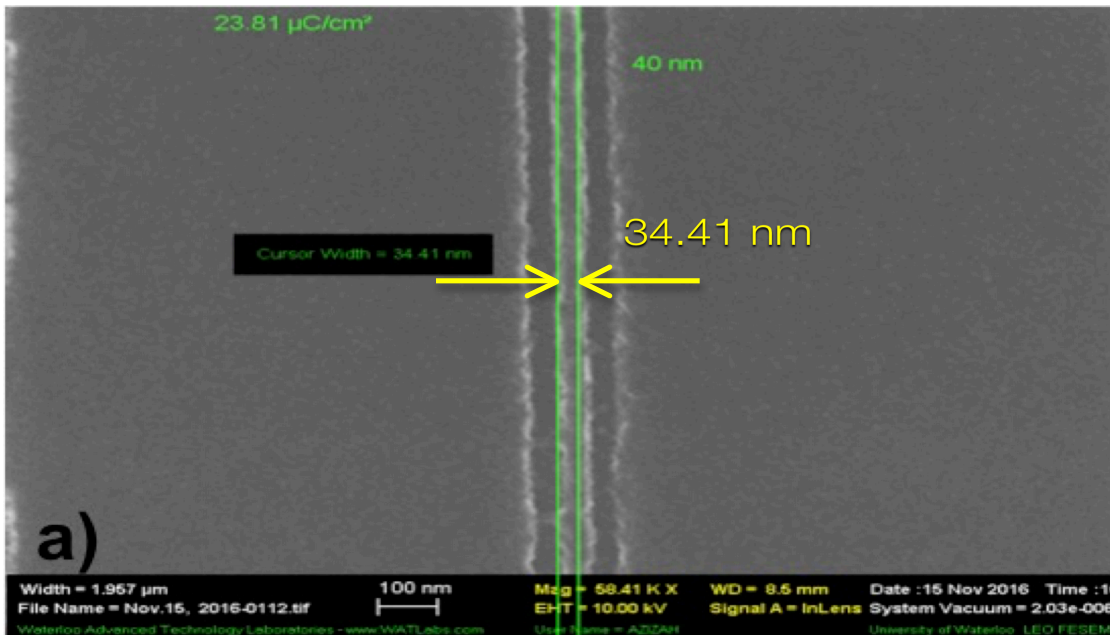


Figure 5.3: Schematic to show the working principal of high and low energy exposure for the fabrication of a nano-gap between two very large electrodes.

3- Results and Discussion:

EBL was selected because it has desirable features, such as reproducibility and the capability of fabricating nanogaps on a large surface. As a quick proof of concept,

Figure (4c) shows the gap fabricated between two thin lines and two large pads exposed at various electron energies (20 keV and 2.5 keV), indicating that a nano-gap of only 45 nm was achieved when exposed at two electron energies. Two large pads were exposed at 2.5 keV in order to obtain a nanogap of 20 nm in size within a one-step exposure. In Figure (5.4a), two rectangles of PMMA resist were exposed at 20 keV, and a resulting 34 nm gap was obtained. Compared to the pads that were exposed at 2.5 keV, a single energy of 20 keV was used to expose the two large pads to obtain a gap of approximately 20 nm. However, the acquired gap is down to 77 nm as shown in Figure (4d). Note that the pad here is much larger and leads to a much greater challenge for nano-gap fabrication.



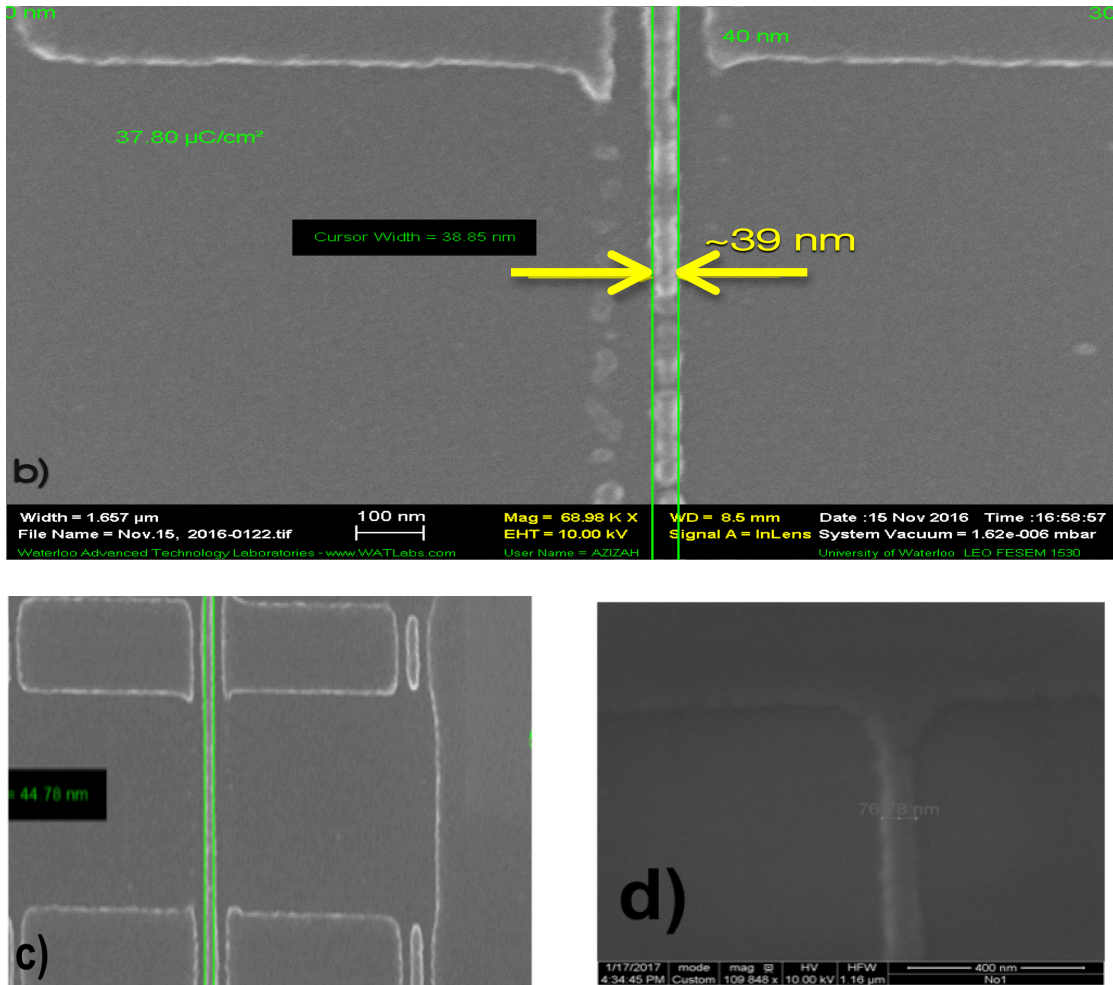


Figure 5.4: SEM images of (a) 34 nm gap between two lines exposed at 20 keV; (b) a nano-gap of 34,41 nm. (c) 45 nm gap between two large pads exposed at 20 and 2.5 keV following the step shown in Figure 3; (d) For comparison, a 77 nm gap was obtained when exposed at a single energy of 20 keV.

As mentioned in the previous section, the electron trajectory simulation is used to evaluate the electron penetration range and scattering volume. In this work, the PMMA resist thickness is very small (~30 nm). When a low electron energy (2.5 KeV) exposes 30 nm thick PMMA resist that is coated on silicon, the electron penetration depth is greater than the resist thickness. Although the forward scattering is not significant at low energies of electrons, most electrons continue until they reach the substrate. Figure 5 illustrates the exposure at low energy on thin film PMMA. As shown in the Figure, the

primary electrons (the beginning blue lines) penetrate the resist and substrate generating the secondary (wide blue lines) and backscattering electrons (red lines) along its path.

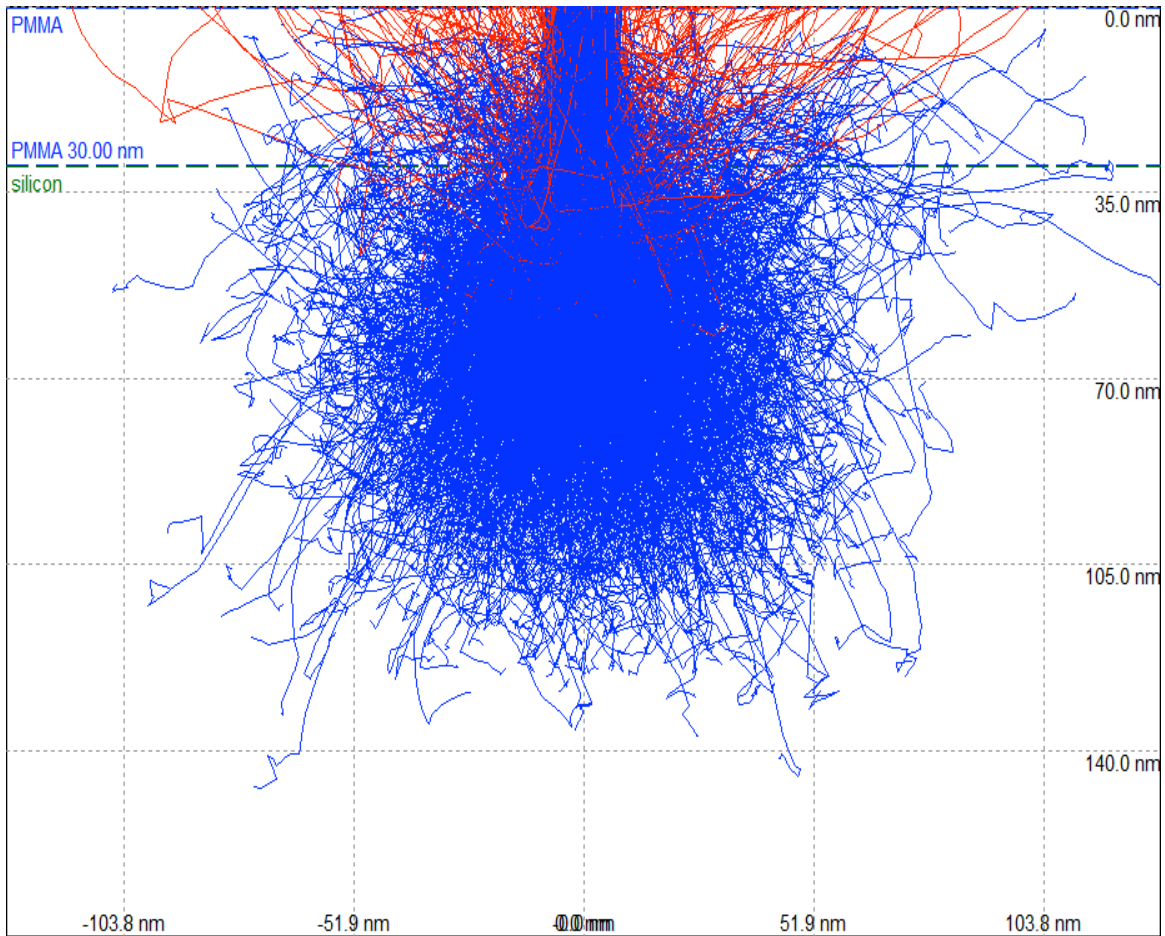


Figure 5.5: A numerical simulation of 100 000 electron trajectories in 30 nm thick PMMA coated on silicon with electron energy of 2.5 KeV.

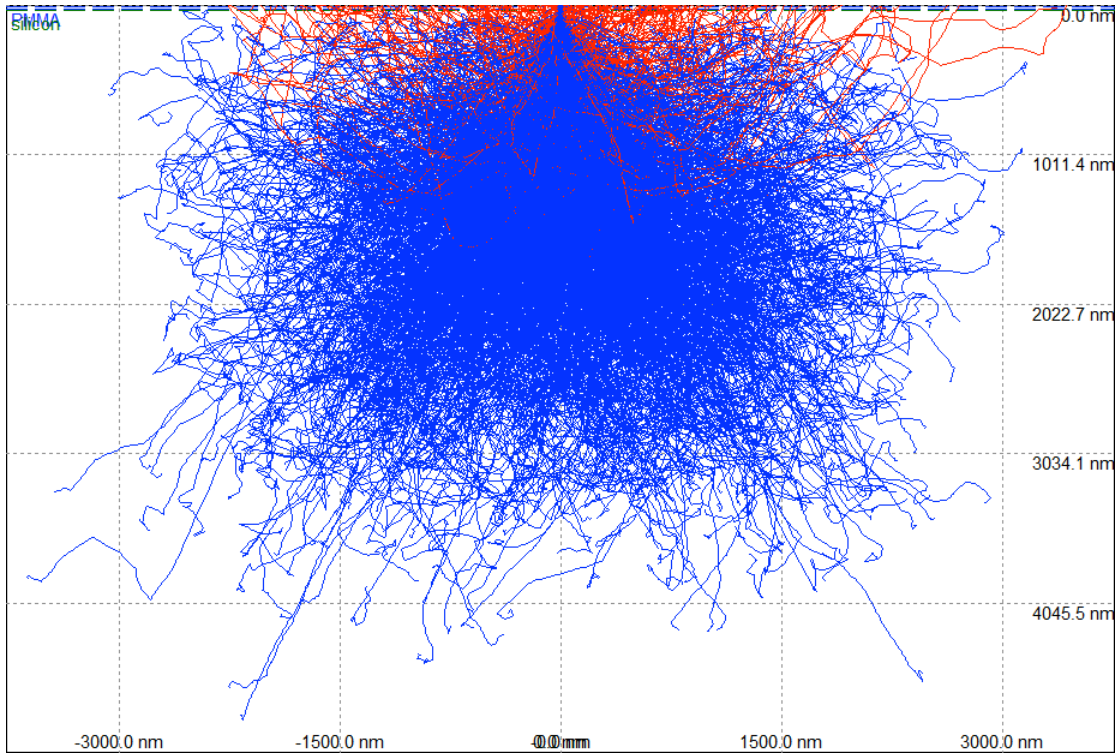


Figure 5.6: A numerical simulation of 100,000 electron trajectories in 30 nm thick PMMA coated on silicon with electron energy of 20 KeV.

At 20 KeV, the electrons penetrate significantly deeper into the silicon as in Figure 6. The primary beams directly penetrate the PMMA resist with less collision. As a result, a sharper line dose is obtained. However, there are interactions of the primary beam electrons with the resist and substrate. The interactions lead to forward scattering and backscattering electrons. Forward scattering electrons occur due to deflecting primary electrons by a typically small angle. Whereas, backscattering electrons exist when the electrons penetrate the substrate and collision with its heavy particles. This leads to a wide-angle scattering that contributes to PMMA resist exposure and causes subsequent inelastic or exposing processes. The backscattering electrons are concentrated on the PMMA resist as shown in Figure 6.

4- Conclusions:

Producing nano-gap electrodes using electron-beam lithography (EBL) is one of the numerous techniques that have been recently developed.²³ This experiment demonstrates that by utilizing EBL for fabricating nanogap electrodes some of the challenges to nano-devices can be reduced, such as control during manufacturing and obtaining reliable aspects in large numbers. In addition, narrow-gaps of 45 nm have been achieved by using an optimized procedure with two exposure steps. A nano-gap below 20 nm between two large pads is expected with considerable further process optimization. However, there are still some issues, which need to be addressed, such as the numerous molecules that go between the gap, and understanding the mechanism of charge transporting. These problems are still waiting to be solved in the years to come.

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Chapter 5

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