Silicon Based Heterojunction Solar Cells and Photodetectors

by

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ABSTRACT

Solar energy is one of the most important clean and renewable energy options for fossil fuel replacement. Efforts have been placed on high performance and low cost solar devices for decades. Although the targets of high performance and low cost have been achieved separately, finding the sweet point between the two is challenging.

Si based heterojunction device is one of the most promising technologies for achieving high performance and low cost at the same time. Currently, Heterojunction with Intrinsic Thin layer (HIT) solar cell is the most popular structure with intrinsic and highly doped a-Si:H thin films. It also holds the Si based single junction solar cell energy conversion efficiency record since 2014.

However, two main constraints exist for such type of solar cells: 1. device performance is highly sensitive to the properties of intrinsic thin layer; any high temperature process can change the heterojunction behavior easily; 2. high cost Transparent Conductive Oxide (TCO) is included in the structure which has low temperature tolerance and therefore standard industrial metallization methods are not applicable for such devices.

One possible solution to mitigate the disadvantages mentioned above is poly-Si/c-Si heterojunction structure. Poly-Si thin film is well-developed material which is much less sensitive to fabrication conditions. Poly-Si thin film fabricated by Low Pressure Chemical Vapor Deposition (LPCVD) has the advantages of relatively low thermal budget, high through put and high quality. Furthermore, the poly-Si thin film can be doped during deposition, which eliminates further high temperature diffusion or dopant activation processes. The conductivity of doped poly-Si thin film is reasonably high. Therefore, it is possible to eliminated the application of TCO layer. On one hand, bring down the material cost; on the other hand enable standard industrial metallization methods.

Challenges exist on achieving high current output and high fill factor (FF) for poly-Si/c-Si heterojunction solar cells. Because, high current output requires thin poly-Si

layer for better blue response, while high FF requires thick poly-Si layer for lower series resistance loss.

In this research, an interface passivation layer and rapid thermal annealing process are analyzed and applied to achieve high current output and high FF at the same time. With non-textured planar solar cell, J_{sc} and FF of 29.37 mA/cm^2 and 79.1% are achieved at the same time.

Different types of Si based heterojunctions exhibit very different device behaviors. With the knowledge of Si based heterojunction analysis, the properties of Al-ZnO/Si heterojunction are analyzed in details. The superior junction properties of Al-ZnO/(n)Si over Al-ZnO/(p)Si structure are identified and explained in a systematic comparative study. The photoresponse mechanisms for Al-ZnO/Si heterojunction are explained and verified with experimental results.

With the in depth understanding of Al-ZnO/(n)Si heterojunction structure, further modifications on the device are applied. Namely, thickness of Al-ZnO thin film is optimized and an interface passivation layer is applied. A high performance broadband photodetector is fabricated and presented with close to theoretical maximum responsivity for red color wavelength at self-powered mode.

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LIST OF ABBREVIATIONS

ARC	Anti-reflection coating
a-Si:H	Hydrogenated amorphous silicon
Al-ZnO	Aluminium doped zinc oxide
BSF	Back surface field
CCD	Charge coupled device
CMOS	Complemetry metal-oxide-semiconductor
Cz	Czochralski
DI	Deionized
EQE	External quantum efficiency
FF	Fill factor, ratio of maximum power output over the product of Isc and Voc
FSF	Front surface field
FZ	Float zone
HIT	Heterojunction with intrinsic thin layer
IBC	Interdigitated back contact
IPA	Isopropyl alcohol
IQE	Internal quantum efficiency
Isc	Short circuit current, current at short circuit (zero current) condition
ITO	Indium tin oxide
LPCVD	Low pressure chemical vapor deposition
MCL	Minority carrier lifetime
NAO	Nitric acid oxide
PECVD	Plasma enhanced chemical vapor deposition
PERL	Passivated emitter and rear locally diffused
PV	Photovoltaic
RTA	Rapid thermal annealing
SEM	Scanning electron microscope
TCO	Transparent conductive oxide
UNSW	University of New South Wales
UV	Ultraviolet
Voc	Open circuit voltage, voltage at open circuit (zero current) condition

CHAPTER 1

INTRODUCTION AND OBJECTIVES

1.1 Si Based Solar Cell Technology

Ever since the world experienced the first energy crisis in the 1970s, people have addressed more and more attention to energy consumption, fossil fuel storage and alternative energy sources. Unfortunately, with the population explosion and development of developing countries, 50% increase in energy consumption is expected by the year 2035. So analysis is carried out to estimate the timeline for expiration of fossil fuels. Although different organizations are giving different numbers, 50 to 70 years are agreed by most [1]. Of course, we can manage the fossil fuel usage within this time and discover new coal mines and fuel wells, to prolong the period. But no matter what it is, 50 years or 100 years, one thing we are sure about is that there is a date, when the world has to work without fossil fuels, and that it is not far away. In other words, alternative energy is necessary in the near future, and it must have a huge capacity to solve the energy problem we are facing. In this circumstance, it is solar power to the rescue. More solar energy is arriving at the earth in an hour than the total energy we need to power up the whole world for a year. Moreover, solar power is widely available, and it is clean, renewable with unlimited supply. Plants create energy out of sunshine to feed all living beings. Solar devices work exactly the same way except that they create power only for human beings. They agree on the function of nature and that is why they can solve another serious problem coming along with the violent usage of fossil fuels: global warming. As known to all, the major source of man-made carbon emission is burning of fossil fuels. That means every bit of energy replacement of fossil fuels by solar energy is a step of global warming mitigation.

In 2015, the photovoltaic industry production increased by almost 20% and reached a world-wide production capacity of about 60 GWp [2]. The compound annual growth rate (CAGR) over the last 15 years was over 40%, which makes photovoltaics one of the fastest growing industries at present [3].

Actually, photovoltaic industry has grown steadily over the last 40 years. Silicon-based solar cell is and has always been the dominant technology of PV market. Crystalline silicon solar cell has taken up 90% market share for decades. Fig.1.1 shows the solar cell production specification in 2010 [4].

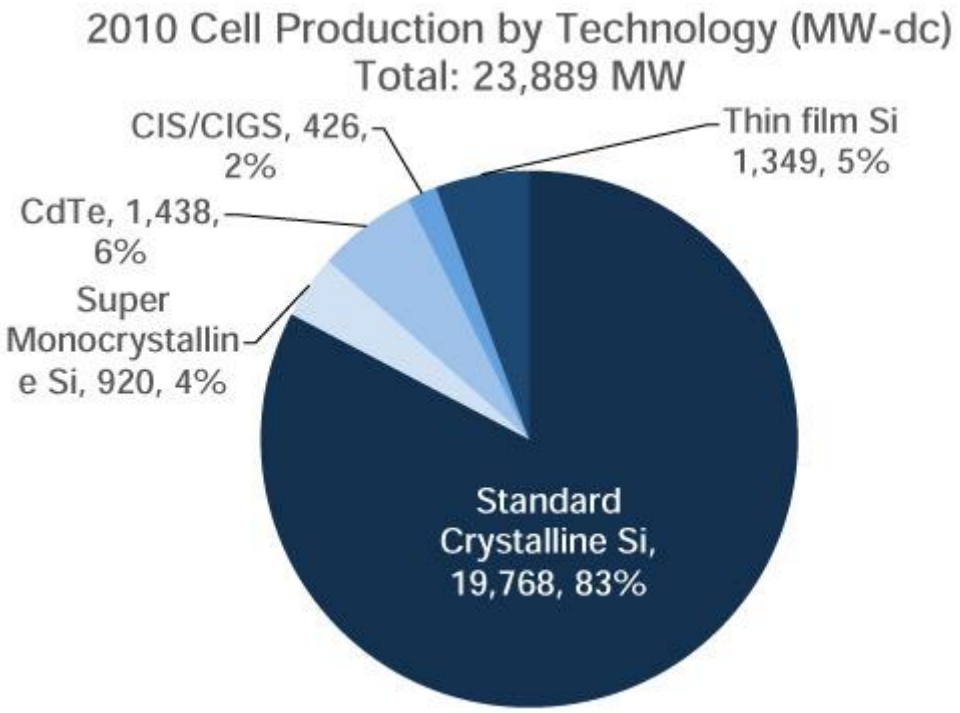


Figure 1.1 Cell production distribution in 2010

We can see from the diagram that even within the remaining 10% to 20% thin film market, silicon is also observed in form of a-Si:H and poly-Si. In other words, silicon is the chosen material for solar devices by both scientists and engineers. The most important reason why silicon is favored traces back to the 1950s. Si was first chosen by semiconductor industry, and after 20 years of development, Si was well known from material science and device physics to fabrication technology and production line design in 1970s. Therefore, solar industry took advantage of semiconductor industry at the very beginning and ever since. Although the paths of development for these two

industries are different, they still share technology innovation and production tools in some cases. Other than the advantage of manufacturing “know-how”, Si has another incomparable superiority to other materials, which is huge stock on earth. Solar devices have certain efficiency limit. Therefore, in order to achieve huge amount of power supply, corresponding massive usage of material is expected. The abundance of silicon makes it the perfect choice for large scale fabrication. Moreover, the non-toxic nature of Si also counts as a non-negligible factor for being widely used. Some other inorganic semiconductors, Cd for instance, have been proved to be capable for reasonable efficiency solar devices. However, these materials are not environmental friendly or even toxic. Some of these semiconductors are totally forbidden in some countries. Last but not least, Si has a reasonable band-gap for terrestrial solar devices, especially for single junction cells. With all these elegant advantages, Si has been the most popular material that dominates solar industry and will still be so in the near future.

1.2 Si Based Hetero-Junction Photodetectors

The excellent photovoltaic properties of Si material have many applications other than solar power harvesting. One of the most important application is photodetector. Si based photodetectors have very similar structures and basically the same operation principles.

In the recent years, the demand in high quality visible light photodetectors has been boosted by new types of applications, such as CMOS cameras, visible light communications systems, internet of things (IoT) applications, etc. However, very few types of Si based photodetectors can achieve mass production with reasonable performance. Still, Si based PN or PIN junction photodetectors are the main candidates. Although, Si based heterojunction photodetectors have been researched on, they are still having limited demonstrated performance or difficulties in mass productions. One of the reasons for this fact is that limited resources and efforts were invested in the Si based photodetector industry in the past. However, solar energy industry has been very well developed for decades. Efforts have been located on optimizing light confinement, enhancing junction properties, surface passivation approaches, and exploring and applying novel materials, etc. Much of the knowledge is readily transferable for photodetectors. The theoretical understanding and technical experiences on Si based

heterojunction structures are valuable resources and promising methods to help Si based photodetectors to achieve new development and finally provide series of new applications and new ways of living for the modern people. One of the promising candidates of Si based heterojunction photodetector is Al-ZnO/Si photodetector, which will be discussed in detail in Chapter 7.

1.3 Research Motivations

1.3.1 Poly-Si/c-Si Heterojunction Solar Cells

Although Si solar cells have been well developed in the last few decades, there is still huge space for further improvement for future devices. Mainly, technology develops towards two targets: higher conversion efficiency and lower fabrication cost. There are still mystery blocks along the path to these targets. Currently, the high-performance heterojunction solar cells include several essential components, which are not favored by low cost fabrication processes. For example, a TCO layer is applied to help lateral carrier transport and it is expensive. Moreover, the TCO layer has relatively low temperature tolerance and therefore is not compatible with typical metallization processes. Another example is, the highly deliciated interfacial passivation layer – ultra-thin intrinsic amorphous Si layer. It is extremely difficult to achieve the optimized layer and therefore devices with satisfactory performance. That means, performance variation and product yield are very hard to improve. Furthermore, only very few facilities can produce such devices and therefore limited product volume is available for the market.

One of the approaches that may solve the problem can be applying LPCVD poly-Si emitter instead of highly doped a-Si:H emitter. In the meantime, replace the a-Si:H interfacial passivation layer with other type of passivation layers.

LPCVD poly-Si is a well-developed material for semiconductor industry [5,6]. LPCVD poly-Si possesses the advantages of relatively simple process, high through put, high yield, high uniformity, high repeatability, high temperature tolerance, high stability and etc. Therefore, LPCVD poly-Si has always been popular for semiconductor industries. The main applications for LPCVD poly-Si are gate material for CMOS technologies

[7], TFTs [8], etc. LPCVD poly-Si/c-Si heterojunction solar cells were first developed in the 80s' [9]. However, due to Fill Factor (FF) and blue response limitations [10], this technology has not been the favorite for most researchers in the last several decades. In the recent years, poly-Si/c-Si heterojunction solar cells resurfaced in the PV community [11,12]. This is because the development in surface passivation and more importantly in the interfacial passivation layer technologies [12,13]. These passivation technologies mitigate the disadvantages associated with the relatively destructive poly-Si layer. Furthermore, Transparent Conductive Oxide (TCO) is boosting the FF of poly-Si/c-Si heterojunction solar cells without the requirement of a thick poly-Si layer [11,12]. Presently, the poly-Si layers in poly-Si/c-Si heterojunction solar cells are basically formed by recrystallization of a-Si:H thin film. An a-Si:H thin film is first deposited by PECVD or LPCVD, and then with the help of high temperature thermal annealing process, the film is re-crystallized to poly-Si [12,14]. The doping procedure can be done at a-Si:H deposition stage, through ion implantation with subsequent dopant activation or simply by diffusion after recrystallization. Several limitations still exist in these processes. First, high thermal budget from recrystallization, dopant activation and diffusion are involved; Second, the passivation from interfacial layer is sensitive to the thermal treatment, worst case scenario it will lose the passivating properties after long period of annealing; Third, to achieve high FF, TCO layer is applied. Therefore, the temperature tolerance of the devices is relatively low, and still not applicable for standard mass production metallization methods.

In this work, the author explores the possibilities of achieving in-situ doped LPCVD emitter solar cells with interface passivation layer. The target is to eliminate the long period of high temperature treatment, maintain high temperature tolerance for metallization, while retain satisfactory FF and blue response at the same time.

1.3.2 Al-ZnO/Si Heterojunction Photodetectors

Aluminum doped zinc oxide (ZnO:Al, AZO or Al-ZnO) thin films have been intensively studied in the recent years. Owing to its excellent optical and electrical properties, Al-ZnO films have been developed for various optoelectronic devices, such as UV photodetectors [15-17], broadband photodetectors [18-21], solar cells [22, 23], LEDs [24], etc. Al-ZnO can be applied as conductive window layer, or form

heterojunction with other semiconductor materials. Al-ZnO/Si heterojunction is one of the most studied device structures and has a potential for future optoelectronic applications.

Al-ZnO/Si heterojunction photodiodes have several fundamental advantages over typical silicon p-n or p-i-n photodiodes, namely: high switching speed, no "dead layer", low shading loss and simple and low temperature fabrication processes.

- High switching speed

  Switching speed is an important parameter for a diode and this is especially true for photodetectors. The Al-ZnO/Si broadband photodetector is a Schottky-like structure. When switching, Al-ZnO/Si is a majority carrier device. Hence, no minority carrier storage makes it possess the advantage of low reverse recovery time in nature, as shown in Fig. 1.2 [25].

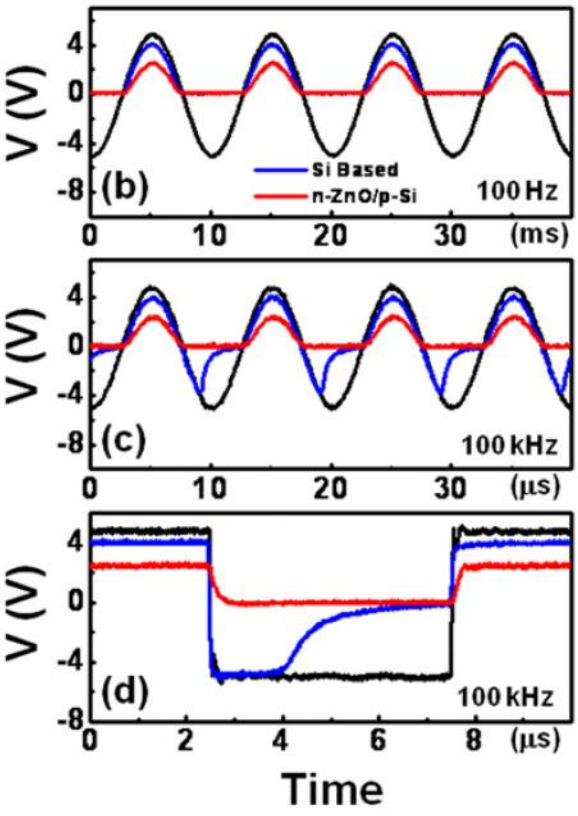


Figure 1.2 Switching comparison between Si p-n junction and Al-ZnO/Si heterojunction

- No "dead layer"

In a typical p-n or p-i-n junction photodiode, a heavily doped layer presents in the path way of incoming photons. These doped layers are usually highly destructive and suffer from very low minority carrier lifetime. Thus, most of the photons absorbed in these layers will be less likely to contribute to the final photocurrent, or in other words, compromise the device responsivity. The junction or the depletion region for photoresponse of Al-ZnO/Si heterojunction is formed by surface energy band-bending as will be discussed in more details below. That means no heavily doped layer is required at the front surface. The exemption of a heavily doped emitter (dead layer) provides possibility of achieving even higher responsivity than conventional p-n junction photodiodes.

- Low shading loss

The trade-off between low series resistance and low shading loss for typical photodiode has been troubling engineers since the beginning of photodiode development. This trade-off is especially important for large area photodetectors. The design should also take the "dead layer" effect into consideration. That is to say, basically less shading loss leads to higher series resistance and stronger "dead layer" effect. One of the options to solve the shading loss and "dead layer" effect is moving the junction to the rear side of the devices. However, rear junction devices typically have reduced internal quantum efficiency (IQE) because the region of high photogenerated carrier collection efficiency (close to and within depletion region) is no longer aligning with the region of high absorption (front surface). Furthermore, rear junction devices usually entail a much more complicated fabrication process. Al-ZnO is a wide bandgap material, and is transparent to most of visible light photons. In addition, Al-ZnO is highly conductive. Therefore, Al-ZnO/Si photodiodes can minimize or even eliminate shading loss from front metal connections without relocating the junction to the back side of the device.

- Simple and low temperature fabrication

As will be described below, the fabrication process for Al-ZnO/Si heterojunction is very simple. Moreover, there is no high temperature process involved during fabrication. Also, the fabrication of Al-ZnO/Si heterojunction is highly compatible

with standard semiconductor fabrication process and hence easy for mass production transaction. Besides, solution based Al-ZnO thin films have been studied for decades. With further optimization, low cost solution based process is possible for future Al-ZnO/Si heterojunction devices.

In this work, the author design and conduct systematic comparative study on Al-ZnO/(p)Si and Al-ZnO/(n)Si structures to fully understand the operation mechanisms of such heterojunction structures. Moreover, apply optimization approaches to push the device performance to be comparative to high quality Si PN junction photodetectors.

1.4 Objectives of Research

The objectives of this research are:

- **Design and perform software simulation to identify key parameters for Si based heterojunction solar cells, prepare for the analysis of Si based heterojunction solar cells;**
- **Develop and analyze standard Si solar cell fabrication technologies, prepare for the fabrication of Si based heterojunction solar cells and photodetectors;**
- **Design and fabricate LPCVD poly-Si/c-Si heterojunction solar cells, explore the possibility of eliminating TCO layer with acceptable device performance;**
- **Explore and develop performance enhancement methods for developed Si based heterojunction solar cells;**
- **Design and fabricate Al-ZnO/Si heterojunction photodetectors, understand and explain the operation mechanisms of Al-ZnO/Si heterojunction photodetectors;**
- **Explore and develop performance enhancement methods for developed Si based heterojunction photodetectors.**

- **Explore and demonstrate potential applications for Al-ZnO/Si heterojunction photodetectors.**

CHAPTER 2

BACKGROUND

2.1 High Efficiency Silicon Solar Cells

Considering difficulties in fabrication technologies, material stabilities, etc., multi-junction solar cells have been less attractive except for space applications. Therefore, main focus is located on single junction solar cells in this report. There are three leading solar cell architectures with associated technologies that provide guidelines for high efficiency silicon solar cell development, namely: Passivated Emitter with Rear Locally Diffused (PERL) solar cell, Interdigitated Back Contact (IBC) solar cell and Heterojunction with Intrinsic Thin-layer (HIT) solar cell. The reported best performances are listed in Table 2.1 [26-28].

Table 2. 1 High efficiency solar cell summary by 2013

Cell Structure	J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	Efficiency (%)
PERL [26]	42.7	0.706	82.8	25.0
HIT [27]	39.5	0.750	83.2	24.7
IBC [28]	40.5	0.721	82.9	24.2

PERL had been holding the record for single junction silicon solar cell since 1999, until the new record arrived in 2014. The basic structures for the three types of solar cells are quite different. A brief introduction to the device structures is given herein.

2.1.1 PERL Solar Cell

The PERL cell developed by UNSW (University of New South Wales) which holds the world record for single junction silicon solar cell. The reported efficiency is 24.7% and later to be 25% due to change of standard illumination data. Fig. 2.1 demonstrates the schematic of a PERL cell [26].

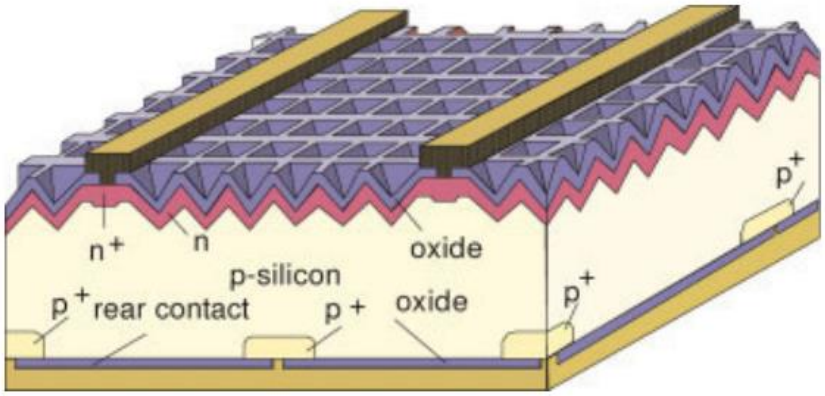


Figure 2.1 Schematic diagram of PERL cell

There are a few key features that minimize all kinds of losses and keep PERL the best for years. These key features listed below have been guidelines for different new types of solar cells:

- Reverse pyramid texturing to reduce front optical reflection;
- Double layer ARC (Anti-Reflection Coating) to reduce front optical loss;
- Narrow fingers to reduce metal finger reflection;
- Rear metal reflector to increase effective path length of light;
- High lifetime wafers to reduce bulk recombination;
- Front and back thermal oxide to minimize surface recombination;
- Locally diffused small rear point contact to reduce silicon-metal area and hence less recombination;
- Selective emitter to eliminate “dead layer” effect while keeping ohmic contact (improve blue response).

This technology achieved excellent conversion efficiencies. However, the draw backs are obvious. The fabrication process is too complicated and total cost is too expensive for industrial mass production.

2.1.2 IBC Solar Cells

SunPower’s A-300 cell is an outstanding rear contact cell. Amazingly, it is not only capable for lab research, but it is also demonstrated in production. The schematic

diagram of IBC solar cell is shown in Fig. 2.2 [28]. The key features for IBC solar cells are listed as follows:

- No front contact leads to any optical loss by metal shading;
- Standard texturing and ARC to reduce front surface reflection;
- High quality wafer to reduce bulk recombination;
- Front and rear oxide passivation to minimize surface recombination;
- Point contact at rear to reduce silicon-metal area;
- Both contacts at rear making it easier for module fabrication.

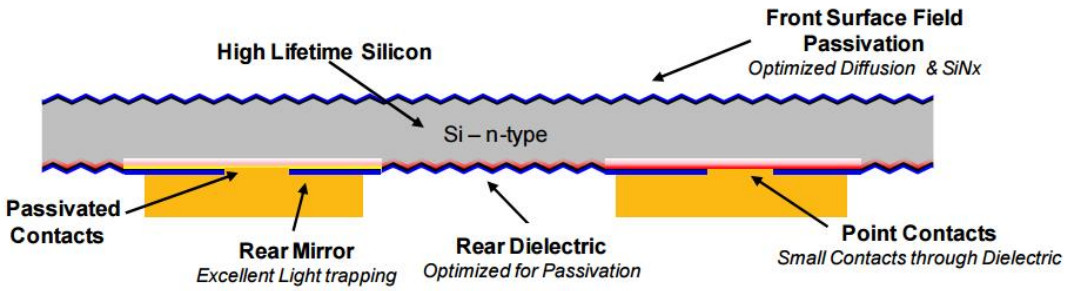


Figure 2.2 Schematic diagram of SunPower's back contact solar cell

Although its fabrication process is still complicated at rear surface, IBC solar cell is already more easier for production transfer. Another disadvantage is higher demand of wafer quality. Because the junction is at the back of the cell, e-h pairs have to be able to survive the whole way until they arrive there.

2.1.3 HIT Solar Cell

Sanyo's HIT cells have become more and more heated topic in the recent years. It has been demonstrated in industrial production and the temperature involved in the entire fabrication process is below 200ºC. The low process temperature also helps to realize the fact that no wafer bowing after whole fabrication process even with wafer as thin as 70um. Fig. 2.3 shows the schematic structure of HIT cell [27]. The key features of HIT cells are listed below:

- Hetero-junction to realise high V_{oc};
- Front and back intrinsic a-Si:H passivation achieving best passivation ever reported in device level;

- Application of TCO (Transparent Conductive Oxide) showing better long wavelength response;
- Front TCO is also served as ARC;
- High quality wafer and standard texturing as other high performance cells.

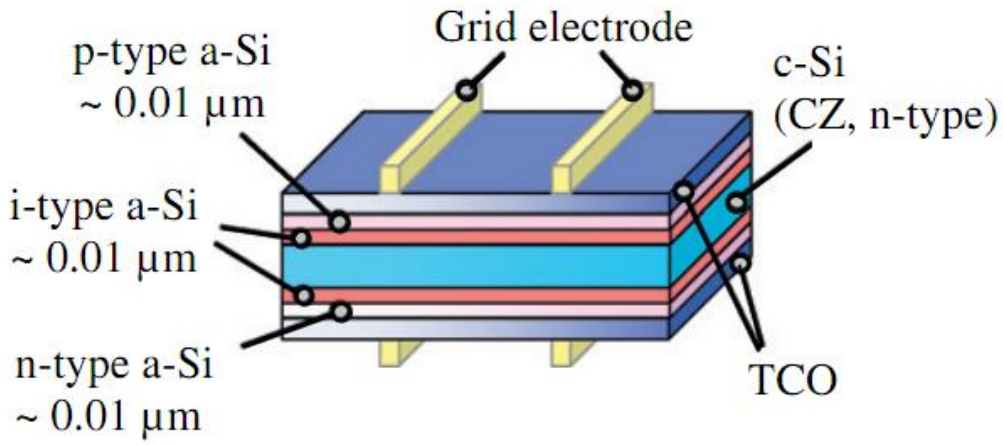


Figure 2.3 Schematic diagram of HIT solar cell

So far, the main draw backs for HIT cells are low blue response due to the front absorption by TCO/a-Si:H layer, highly sensitive to the thin film deposition conditions and more importantly, the low temperature tolerance, which limits the metallization methods.

2.2 Poly-Si/c-Si Heterojunction Solar Cells

Poly-Si emitter solar cells were first developed back in the 1980s [9]. The poly-Si layer may form by a-Si:H recrystallization, LPCVD deposition, metal induced crystallization, etc. This technology did not receive too much attention in the last few decades, the reported device performance is relatively low comparing to other types of c-Si based solar cells [10]. The main reason is that poly-Si is relatively defective and not conductive enough. Therefore, it absorbs most of blue light without contributing decent photo-generated current and it is tricky to minimize the series resistance so as to achieve high fill factor. In conventional poly-Si emitter solar cells, for a good blue response, thinner poly-Si layer is required. However, to have a high fill factor, thicker poly-Si layer is necessary. This dilemma makes it impossible for poly-Si emitter solar cell to

become the favorite child in the silicon solar cell family. A typical structure of poly-Si/c-Si heterojunction solar cell is presented in Fig. 2.4.

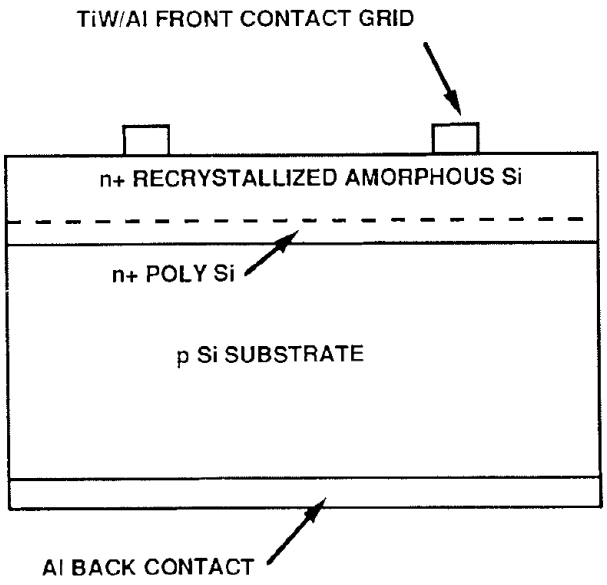


Figure 2.4 Recrystallized poly-Si/c-Si heterojunction solar cell

However, in the recent few years, poly-Si emitter has regained its attention. It is mainly because of the development in two aspects [11,12]: 1. with the help of a interfacial passivation layer, the recombination at poly-Si/c-Si interface due to the defective material structures is mitigated; 2. by applying a Transparent Conductive Oxide (TCO) layer, the problem of high series resistance, especially at very thin condition, for achieving high fill factor is solved.

Another reason for the interest in poly-Si emitter is that typical HIT solar cell structures are extremely sensitive to the properties of the intrinsic layer and the highly doped amorphous layer. Furthermore, the typical HIT structure does not have a high temperature tolerance for standard metallization process (i.e., screen printing followed by co-firing). Therefore, other materials are considered as substitutions for a-Si:H emitters.

However, the poly-Si passivated emitter solar cells reported so far are all based on the recrystallization of a very thin a-Si:H layer plus a TCO layer [11,12]. A typical structure of poly-Si/c-Si heterojunction solar cell with passivated heterojunction is presented in Fig. 2.5. That means, the problems of high cost TCO layer and low temperature tolerance for standard metallization process still exists in the structure. Therefore, a

poly-Si emitter without TCO that still presents decent blue response and fill factor at the same time is required and of great interest. Detailed device development and performance analysis are presented in Chapter 5.

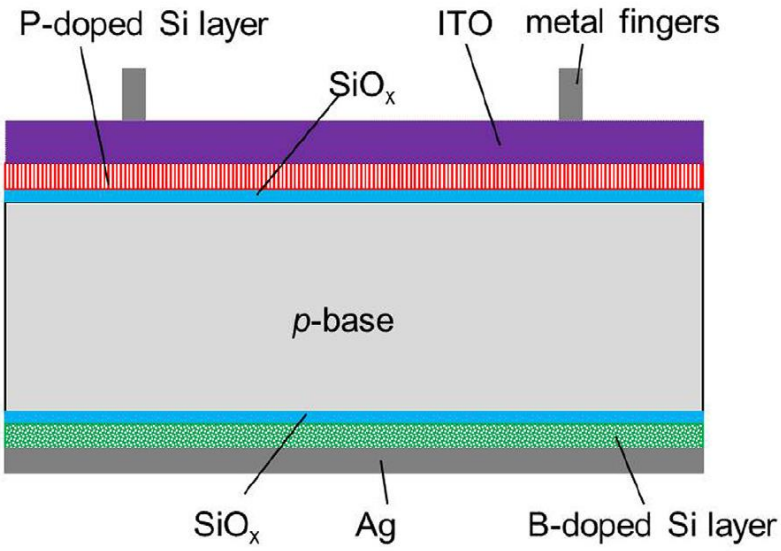


Figure 2.5 Recrystallized poly-Si/c-Si heterojunction solar cell with ITO and tunnel oxide BSF

2.3 Hydrogen Passivation for Si Solar Cells

Atomic hydrogen has been identified with passivation benefit for silicon based semiconductor devices, especially photovoltaic devices, for decades [29]. The most widely received mechanism is atomic hydrogen can passivate dangling bonds and crystal defects, therefore improve the structural and finally electrical properties of semiconductor devices. Based on the mechanism described, hydrogen passivation has been widely implemented for semiconductor devices with certain amount of grain boundaries and crystal defects, such as thin film poly-Si solar cells, thin film a-Si:H solar cells, multi-crystalline Si solar cells and etc. Satisfactory improvements on the device performances are reported [30,31].

There are mainly two approaches that are commonly used to achieve the atomic hydrogen passivation: 1) annealing with H_2 plasma [32]; 2) annealing with hydrogen rich thin films (i.e. SiN_x:H) [31]. Approach 1) involves additional plasma procedure which not only expensive but also enclose the potential of plasma damage. One method to mitigate the plasma damage is to implement remote-plasma system. However,

remote-plasma system is typically even more expensive. Approach 2) usually lead to one or in some cases several additional device fabrication processes. Moreover, the required annealing temperature and time are typically more crucial.

Additionally, the atomic hydrogen passivation introduced, to the author's best knowledge, are mostly applied in the middle of device fabrication processes. And the passivation effect and be reversed by the fabrication processes carried out later. Moreover, it may limit or have negative effect on the coming fabrication processes. Therefore, post-fabrication passivation would be the best option. However, post-fabrication hydrogen passivation effect is rarely reported. In this research, the author explores the possibility of introducing hydrogen passivation after device fabrication. Furthermore, efforts are located to eliminate the implementation of commonly used plasma environment. Therefore, the Post-fabrication Low Pressure Hydrogen Annealing (LPHA) process is discussed in Chapter 6.

2.4 Al-ZnO/Si Heterojunction Photodetectors

Although, Al-ZnO/Si heterojunction structures have been studied for more than a decade, the operation principles of such structure are still not fully understood. Given that Al-ZnO is an n-type material, Al-ZnO/(p)Si structure is assumed more suitable for photodiodes. Hence, most Al-ZnO/Si photodetectors are (p)Si based. Unfortunately, these devices suffer from high reverse bias current in the mA range, low rectification ratio and limited photoresponsivity, especially when operating under small bias as observed in [33-36]. One example is presented in Fig. 2.6(a). Interestingly, most Al-ZnO/Si heterojunction solar cells are (n)Si based. These devices and the minority (n)Si based photodetectors are reported with small reverse bias current in the dark and satisfactory rectification ratio [18, 37]. Moreover, some of the devices are presented with high quantum efficiency [38]. One example is presented in Fig. 2.6(b).

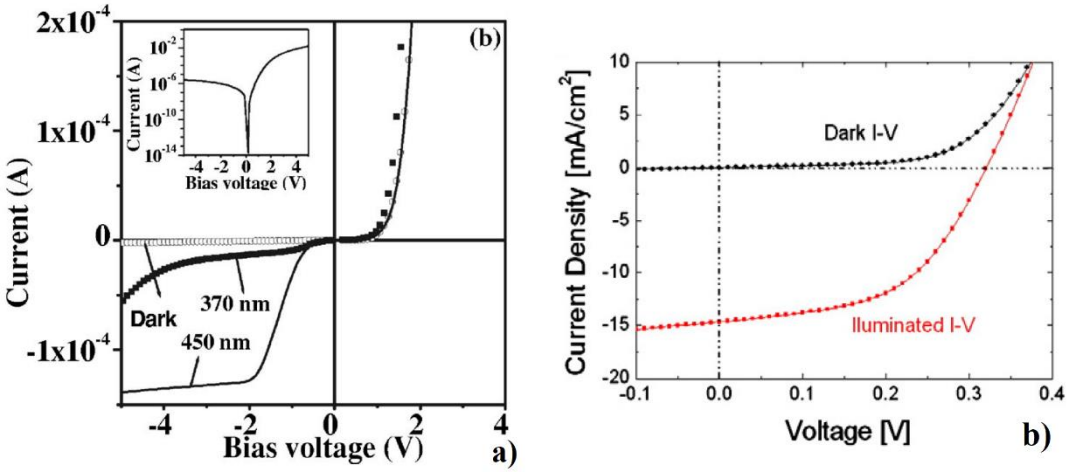


Figure 2.6 Photoresponse of Al-ZnO/(p)Si structure (a) and Al-ZnO/(n)Si structure (b)

Firstly, although the aforementioned and notable differences between Al-ZnO/(p)Si and Al-ZnO/(n)Si devices can be found from different articles, a comparative study into understanding the junction behaviors of the two structures is rarely reported. It is also difficult to identify whether the differences originate from the Al-ZnO thin film processing conditions or from the nature of the heterojunction structures.

Secondly, once the operation principles for Al-ZnO/Si heterojunction photodetectors are understood, improvements in device performance can be achieved through various approaches. With certain amount of efforts, Al-ZnO/Si heterojunction photodetectors may become the preferred substitutions for Si p-n or p-i-n photodetectors in certain types of applications.

Finally, some of the unique properties of Al-ZnO/Si heterojunction photodetectors may lead to novel optoelectronic devices, such as realizing UV and visible detection through two modes of a single device. Moreover, the nature of Al-ZnO/Si heterojunction makes it a possible for future optoelectronic devices with high switching speed.

Detailed structure analysis, device fabrication, and device characterization are presented in Chapter 7 and Chapter 8.

CHAPTER 3

SIMULATION AND ANALYSIS OF ADVANCED SOLAR CELL STRUCTURES

The performance of a solar cell device can be significantly affected by several parameters, such as Minority Carrier Lifetime (MCL), substrate thickness, emitter and Back Surface Field (BSF) doping, etc. Software simulation can be an effective tool to monitor and predict device performance without the complication of device fabrication. Most solar cell simulations are achieved with 1-D simulation software, such as PC1D, AMPS, etc. However, these 1-D simulations cannot include spatial effect (i.e. spatial electric field distribution and lateral current follow, etc.). Therefore, in this work, advanced 2-D simulation, Medici, is used for typical solar cell performance simulation. However, the limitation for Medici software is that it is difficult to define new type of materials and interfaces. Therefore, the specific software for heterojunction simulation, AFORS-HET, is used for heterojunction interface and emitter defect simulations.

3.1 Simulation of IBC Solar Cells

For standard solar cell parameter simulation, the solar cell structure of IBC solar cell is selected. The advantage of simulating such solar cell structure are two folds: first, because the incoming light is spatially dislocated with the semiconductor PN junction, the importance of the main parameters of a solar cell is amplified. Therefore, it is advantageous to qualitatively monitor key parameter effect with IBC solar cell simulations; second, after developing the advanced heterojunction solar cells, as will be introduced in Chapter 5, an interesting future work would be applying the heterojunction with an IBC solar cell structure. The knowledge acquired from the simulation herein will be of great assistance in the design of future devices.

The IBC solar cell is one of the most promising solar cell structures. Even after the announcement of latest record Si single junction solar cell efficiency [39], the author still believes IBC solar cell has space for further improvement. Therefore, a series of advanced 2-Dimentional simulation of IBC solar cells is performed to understand and provide guidance on the key parameters and research directions for such type of devices.

IBC solar cells are highly symmetrical. A simulation unit is defined to model the whole device performance. In this work, a periodic unit of cross section is taken as simulation unit. The defined unit includes half of an emitter area, half of a BSF (Back Surface Field) area and a gap area between emitter and BSF. A relatively small dimension has been chosen for efficient simulation. Fig. 3.1 depicts the method of defining a simulation unit. The defined simulation unit is periodically iterated. Therefore, left and right boundaries of simulation unit are using electrically symmetric configurations. Illumination is applied from the top of the structure.

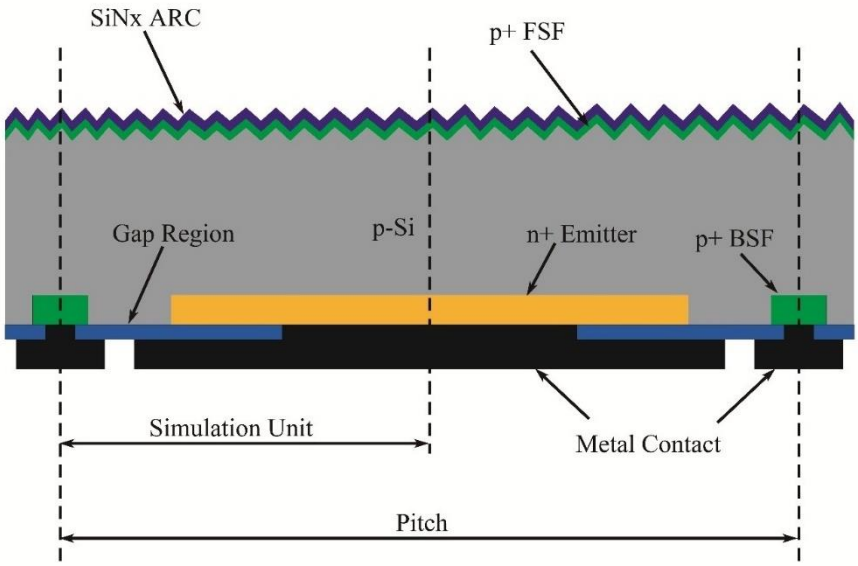


Figure 3.1 Schematic of IBC solar cell structure and simulation unit definition

Mesh generation is one of the most critical steps for 2-D simulations. The density of calculation unit has an important impact on the simulation accuracy. To make the best use of available amount of calculation units, the region in the simulation unit with junctions, close to junctions and especially at the edge of junctions are designed and assigned with more calculation units to maximize the simulation accuracy. An example

of the generated mesh (close to front and rear surfaces) for a simulation unit is presented in Fig. 3.2. Light is coming from the bottom of the structure.

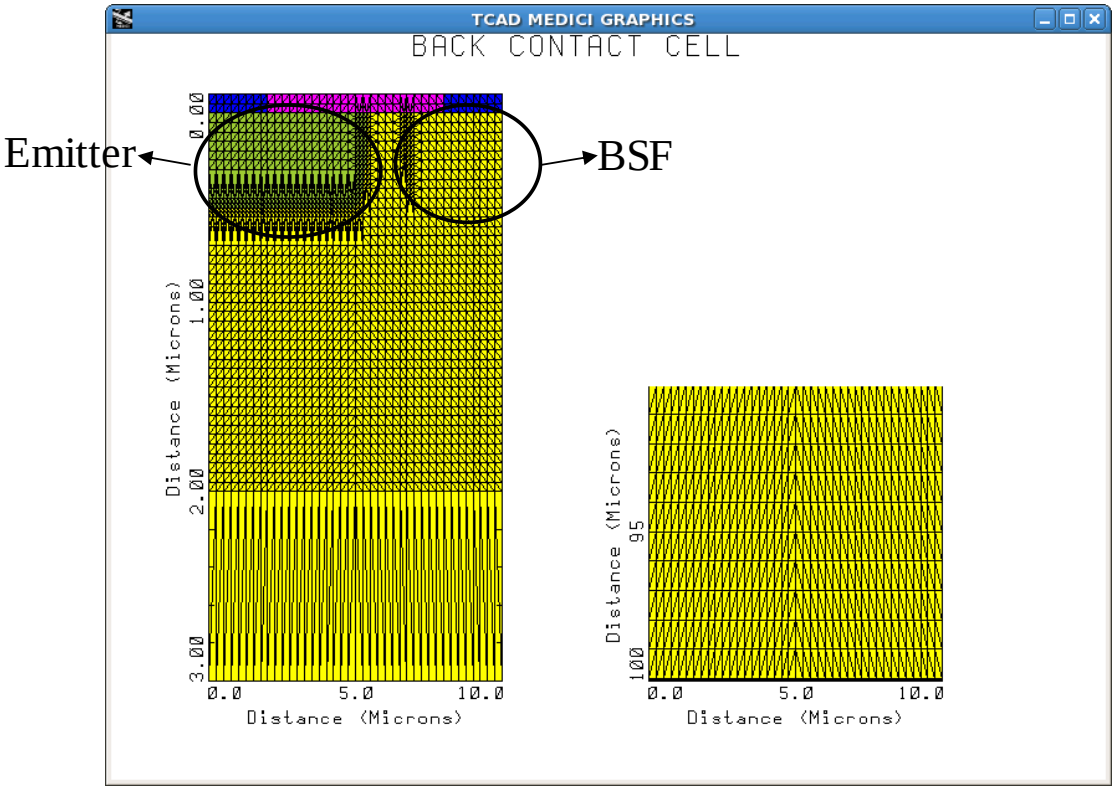


Figure 3.2 Schematic of IBC solar cell structure and simulation unit definition

From mesh density point of view, smaller simulation unit will generate more accurate results. Therefore, simulation on a 20 µm pitch size, which is 10 µm simulation unit size is performed. Details on key simulation parameters are presented in Table 3.1.

Emitter and BSF are competing space at the rear surface. A series simulation shows (not shown here) that making full use of surface area provides better device performance, which align with reported results in [40]. So, a technical limit of 2 µm aperture is used between emitter and BSF. Using similar mesh and model structure, different parameter analyses are performed.

Table 3. 1 Thickness and lifetime simulation result summarization

Parameter	Description
Cell Structure	IBC Solar Cell
Substrate MCL	30 - 1000 µs
Substrate Thickness	50 - 200 µm

Pitch Size	20 µm
Simulation Unit Size	10 µm
Emitter Coverage	7 µm
Back Surface Field Coverage	2 µm
Gap between n+ and p+	1 µm
Light Confinement	SiN_x ARC
Substrate Doping Level	5E15 cm^{-3}
Substrate Doping Profile	Uniform
Peak Doping in Emitter	1E20 cm^{-3}
Doping Profile in Emitter	Rotating Vertical Profile by Ratio of 0.75
Peak Doping in Back Surface Field	1E20 cm^{-3}
Doping Profile in Back Surface Field	Rotating Vertical Profile by Ratio of 0.75
Front Passivation	SiN_x Passivation
Front Surface Recombination Velocity	10 cm/s
Gap Passivation	SiN_x Passivation
Junction Edge Refinement	Re-grid at doping difference above factor of 10
Electrode Resistance	Neglected

3.1.1 Thickness and Lifetime Analysis

The Si substrate thickness and lifetime are very important parameters for device performance. However, these two parameters are mainly determined by material supplier and therefore cannot be controlled at experiment level. Because of that, these parameters are analyzed to predict and estimate the device performance and understand how the fabricated devices are limited by the original material. Moreover, it is believed that the substrate thickness and minority carrier lifetime are the two main parameters that can lead to a further improvement for IBC solar cell structures [41]. Therefore, these two parameters are simulated first.

The simulation of a solar cell performance is very complicated, the simplified and most basic analytical equations are introduced below for a comprehensive understanding:

As presented in Equation 3.1, the generation $G_{(x)}$ of electron and hole pairs at position x is the product of absorption coefficient α_{eh} (specific for the absorption that enables electron-hole pair generation) and the photon flux $N_{ph}(x)$ at the same position. It is worth mentioning that the $N_{ph}(x)$ decades exponentially based on the absorption coefficient from the front surface.

$$G_{(x)} = \alpha_{eh} N_{ph}(x) \text{----------} (3.1)$$

The competing process to generation is recombination U. The recombination rate is directly related to carrier lifetime. Take n type carrier as an example, the recombination U can be expressed as in Equation 3.2.

$$\mathrm{U} = \frac{\Delta n}{\tau_n} \text{----------} (3.2)$$

Within a defined space of semiconductor material, the number of carriers follows the continuity equation, as presented in Equation 3.3 (taking n-type carrier as an example). That means, at steady state, the sum of carrier generation and recombination directly reflects the amount of current flow.

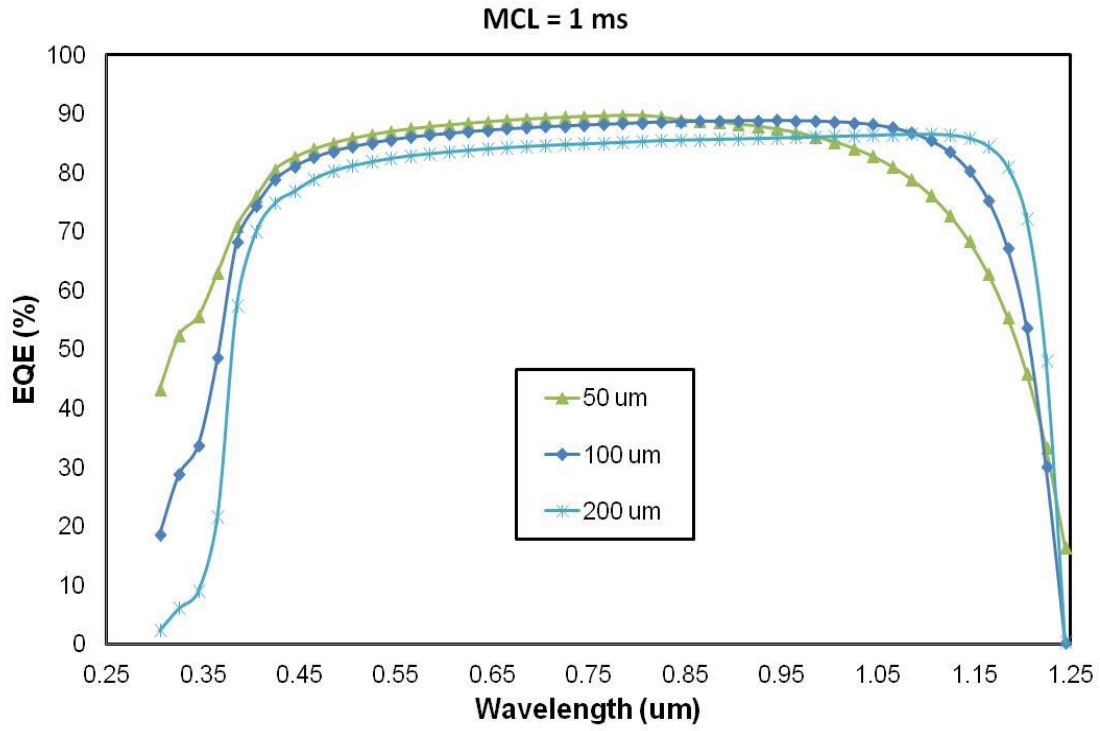
$$\frac{dn}{dt} = \frac{1}{q}\frac{dJ_n}{dx} + G_n - U_n \text{----------} (3.3)$$

The output illuminated current not only relates to the generation rate $G(x)$, but also governed by the carrier collection efficiency $f_c(x)$, which relates to the distance to the junction region (substrate thickness will affect the integration region) and also the carrier lifetime. A simplified equation is presented as Equation 3.4.

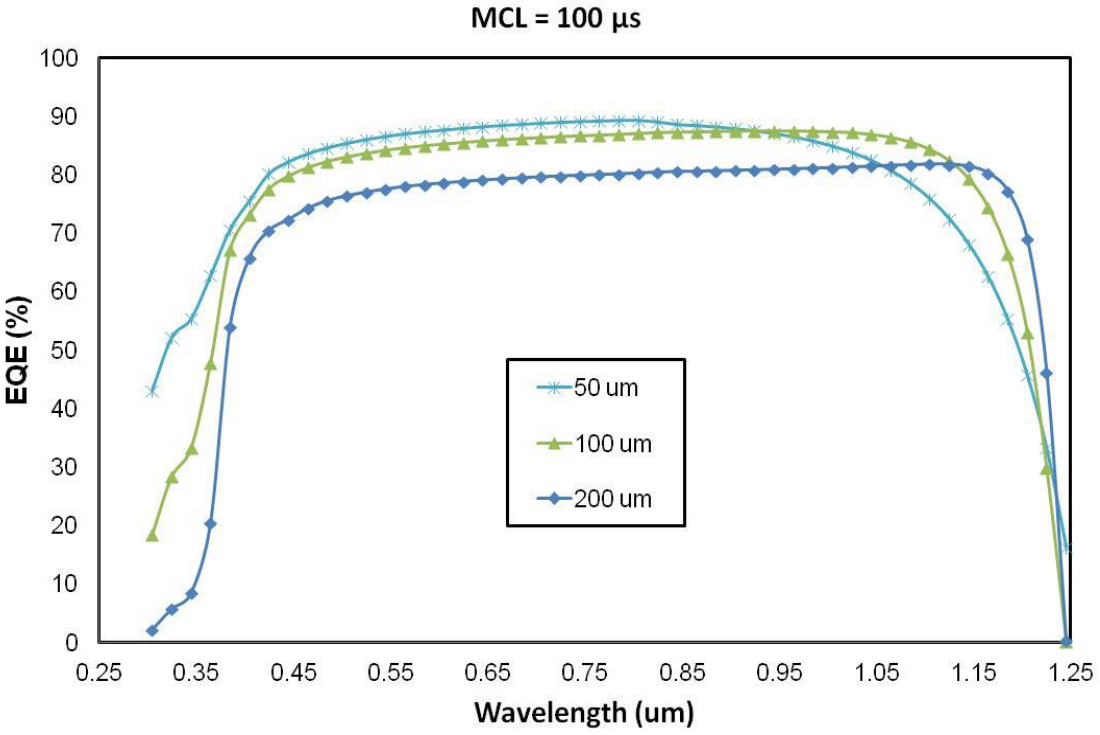
$$J_L = q \int_0^{\infty} G(x) f_c(x)\, dx \text{----------} (3.4)$$

Thickness effects vary according to different degree of wafer quality. Hence, simulation on 50 µm, 100 µm, 200 µm substrate thickness with minority carrier lifetime of 1 ms, 100 µs, 30 µs are performed.

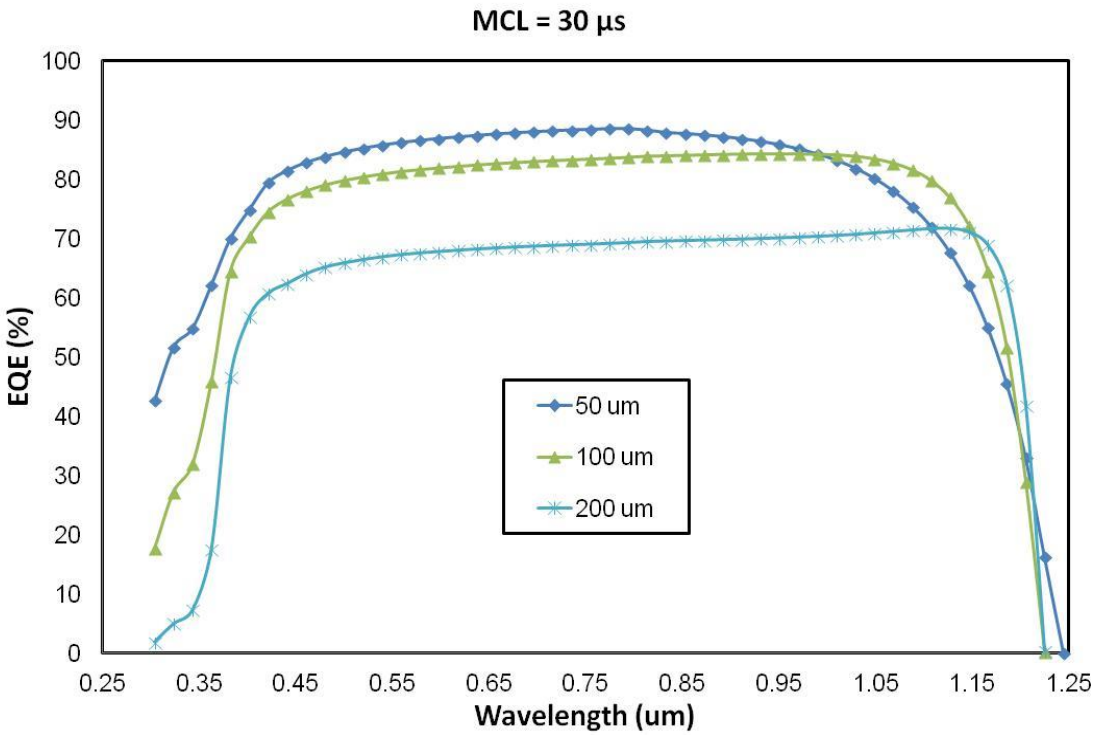
External Quantum Efficiency (EQE) comparison at each minority carrier lifetime (MCL) level is shown in Fig. 3.3.


MCL = 1 ms
EQE (%)
Wavelength (um)
50 um
100 um
200 um

(a)


MCL = 100 µs
EQE (%)
Wavelength (um)
50 um
100 um
200 um

(b)

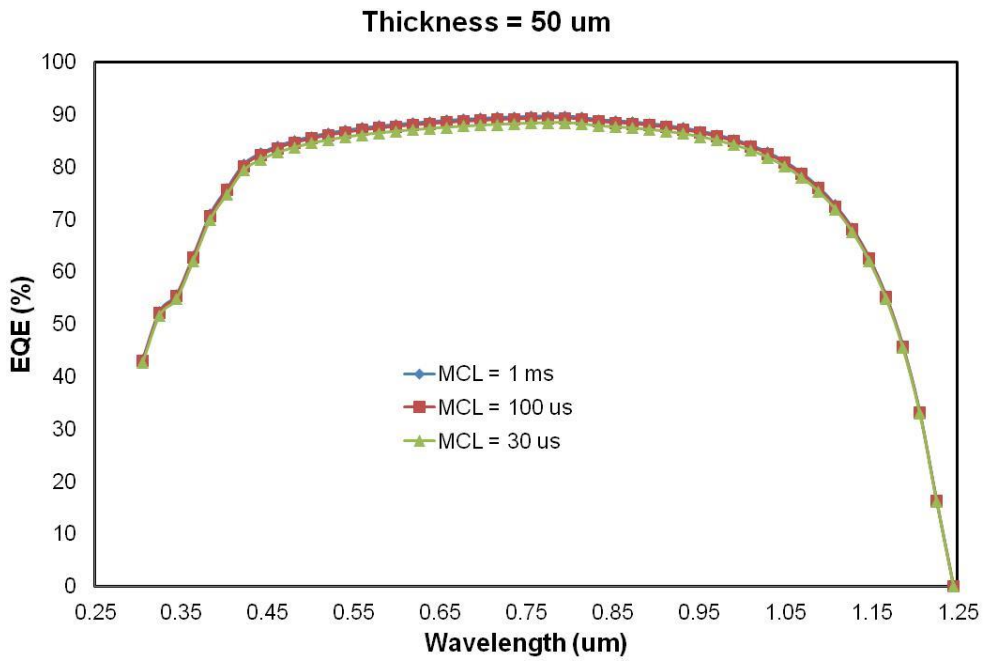


(c)

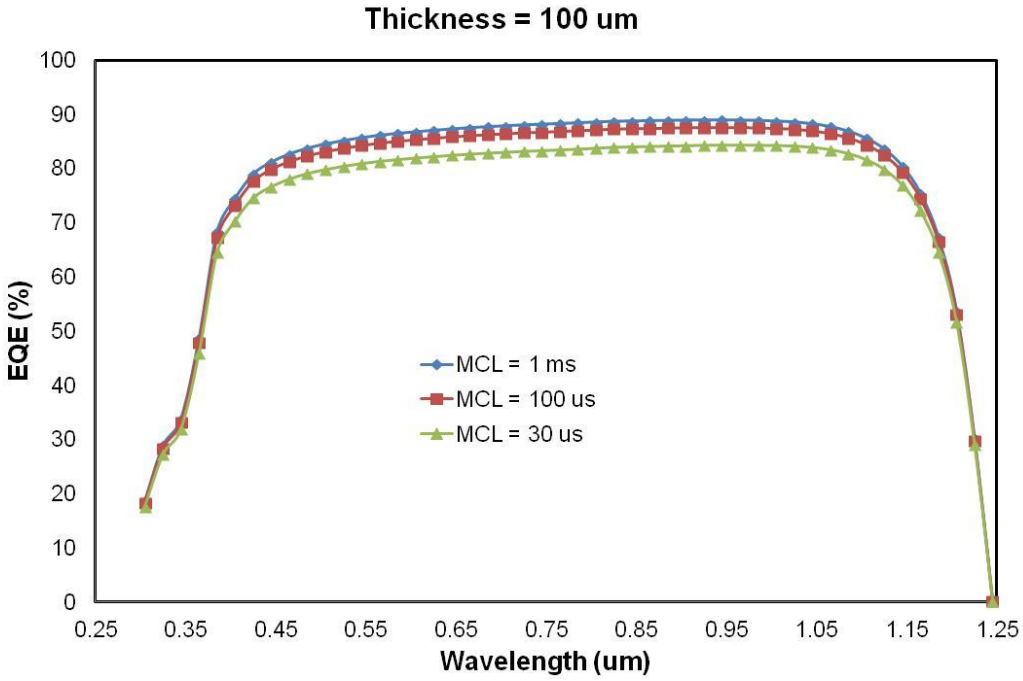
Figure 3.3 EQE simulation result comparison on substrate thickness at each MCL level

Apparently, at each lifetime level, thinner substrate cells are having better blue response. This is because most of the blue light is absorbed near front surface, and thinner substrate means shorter path for carriers to be collected by rear contact. However, thicker substrates are having better performance on red light region. This is because lower energy photons require thicker substrate to be fully absorbed. As substrate minority carrier lifetime decreases, advantage of blue response gets more obvious, becomes the dominative factor and makes thinner cells more favourable.

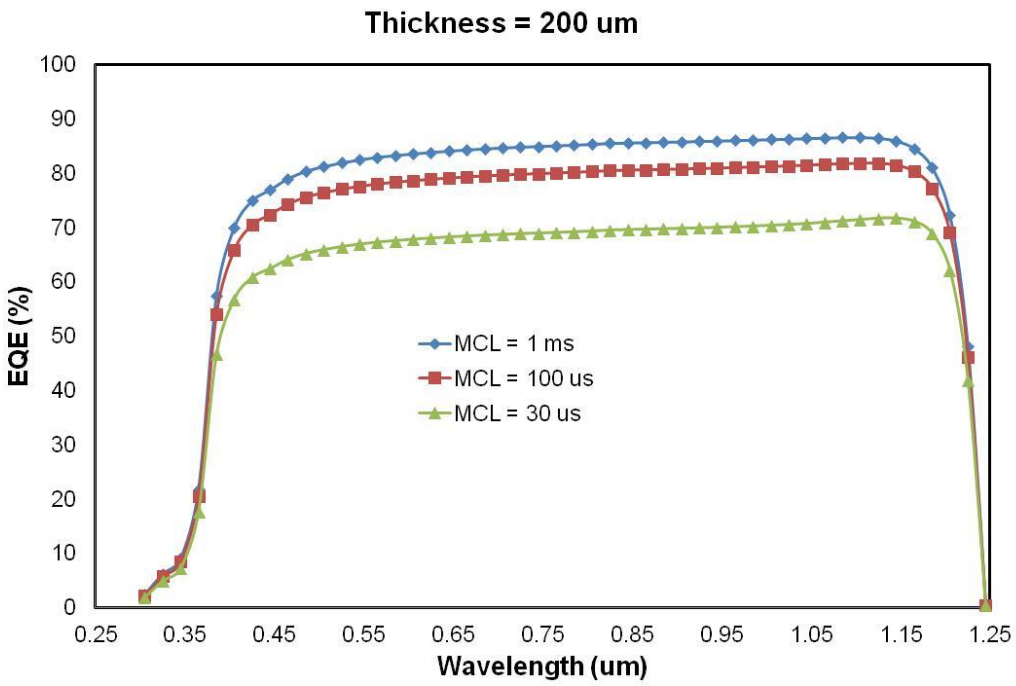
If the EQE results are plotted in groups of different minority carrier lifetime with the same substrate, another observation can be extracted, as shown in Fig. 3.4.


Thickness = 50 um
EQE (%)
Wavelength (um)
MCL = 1 ms
MCL = 100 us
MCL = 30 us

(a)


Thickness = 100 um
EQE (%)
Wavelength (um)
MCL = 1 ms
MCL = 100 us
MCL = 30 us

(b)



(c)

Figure 3.4 EQE simulation result comparison on different MCL at each substrate thickness

Obviously, the impact of MCL level on the EQE result differs at different substrate thickness. Almost no difference can be seen in thin substrate (50 μm), and huge EQE degradation is observed in thick substrate (200 μm). From this observation, one can conclude that to minimize the MCL requirement for IBC solar cells, scale down the substrate thickness is very effective. For IBC devices with thick substrate, high MCL is essential for acceptable device performance.

Another observation is the MCL of the substrate has a strong effect on V_{oc} output of the device, no matter what the substrate thickness is. This is rather important because in experiment processes, limited substrate quality may create a performance ceiling for the final device.

More details of the output results for the MCL and thickness simulation are shown in Table 3.2 and Fig. 3.5. 100 μm cells are slightly superior in high MCL device. However, 50 μm cells become the best at lower MCL levels. That means there is an optimum thickness around 100 μm at high MCL levels, as the lifetime goes down, the optimum thickness moves towards lower value. Also, as proposed previously, thinner substrate has higher tolerance on material MCL, especially for back contact solar cells.

Table 3. 2 Thickness and lifetime simulation result summarization

Thickness (μm)	Lifetime (s)	Isc (mA)	Voc (V)	FF (%)	Eff (%)
50	1.00E-03	39.02	0.6406	82.04%	20.51
	1.00E-04	38.88	0.6321	81.98%	20.15
	3.00E-05	38.50	0.6167	82.04%	19.48
100	1.00E-03	39.76	0.6405	82.04%	20.89
	1.00E-04	39.16	0.6255	82.02%	20.09
	3.00E-05	37.68	0.6037	82.05%	18.67
200	1.00E-03	38.80	0.6384	82.06%	20.33
	1.00E-04	36.57	0.6137	82.08%	18.42
	3.00E-05	31.68	0.5860	81.90%	15.20

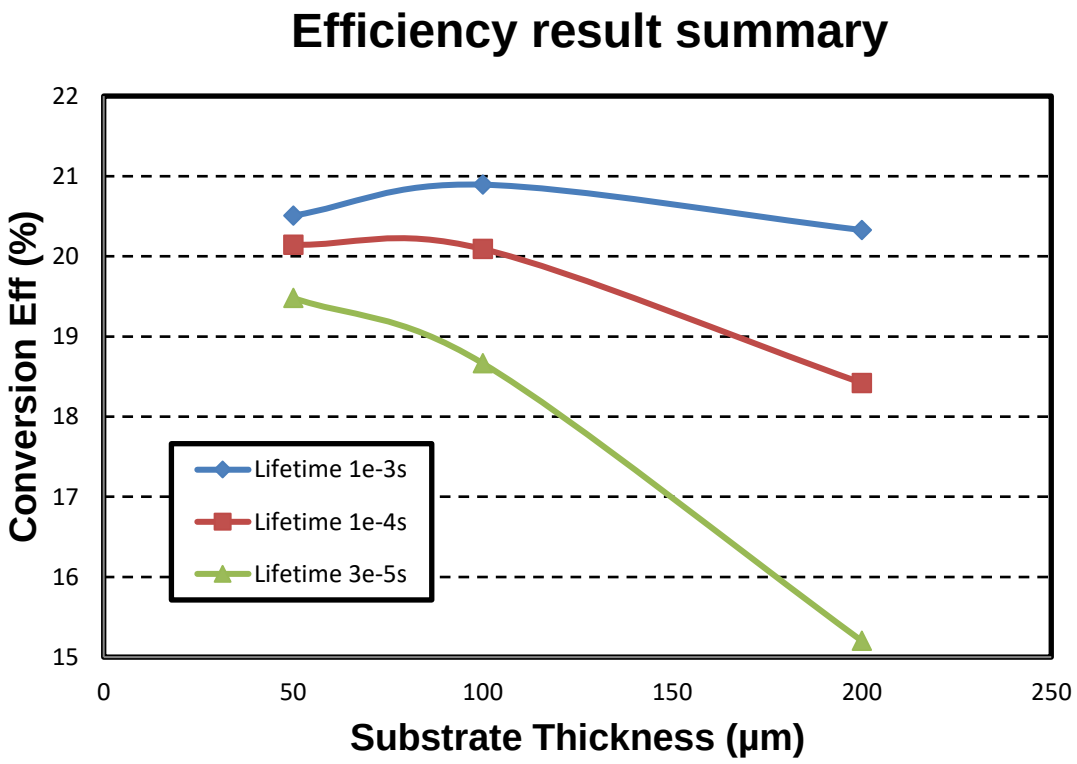


Figure 3.5 Thickness and lifetime simulation result summary

3.1.2 Back Surface Field Analysis

Comparison of three different doping concentrations (1E20, 1E19, 1E18) of BSF and one model without BSF is accomplished through EQE, J-V, and P-V outputs. Although QE results do not show obvious difference (except for the model without BSF), the J-

V and P-V results give a clear trend of performance change with different BSF doping concentrations. Therefore, J-V and P-V results are presented in Fig. 3.6, the EQE results are omitted. Because the simulation is done in 2-D mode, the direct output of current density is in the unit of A/μm. If every cross section of 3-D model is the same as simulated 2-D model, current density of 1E-8 A/μm is equivalent to 1 mA/cm^2 (with the simulation unit width of 10 μm). Hereafter, the simulation results of current density are presented in the form of more commonly used mA/cm^2.

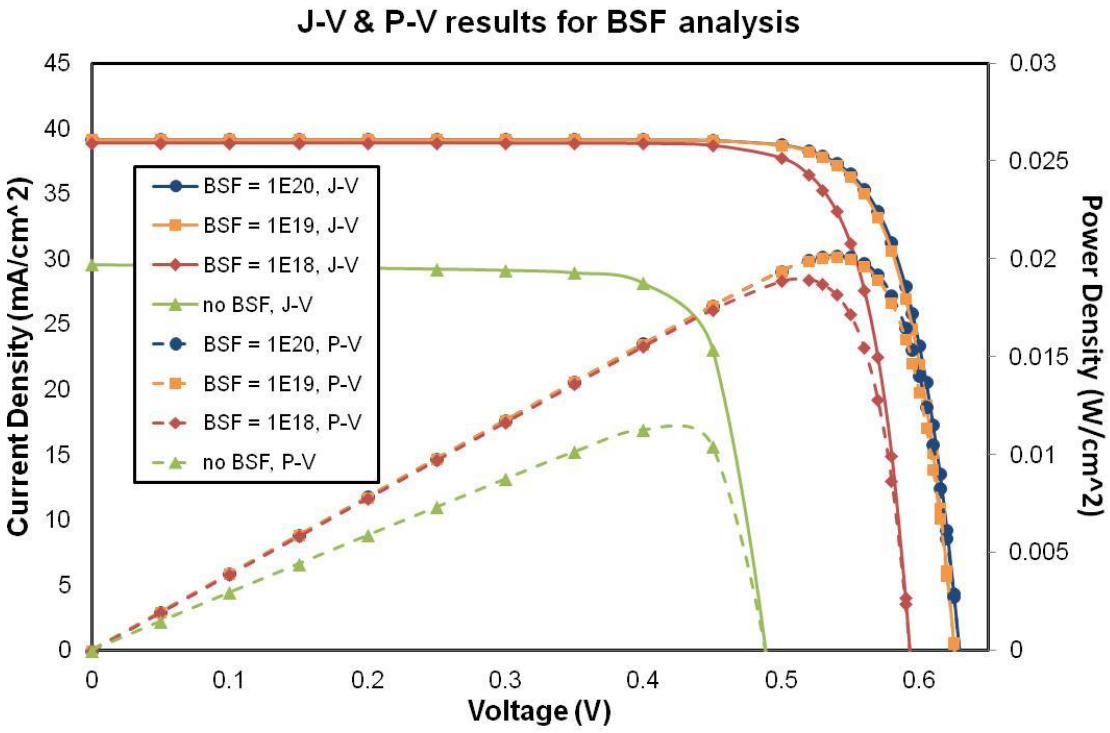


Figure 3.6 J-V and P-V result for different BSF doping concentrations

As shown in J-V and P-V plots, higher BSF doping concentration gives better cell performance. This is because higher BSF doping provides a better surface passivation. The improvement mainly comes from voltage output. The device without BSF presents much worse performance. Hence, BSF is essential and preferred to be heavily doped.

3.1.3 Emitter Analysis

IBC solar cell performance with different emitter doping concentration is analyzed. The wafer thickness and bulk lifetime are selected as 100 μm and 100 μs, respectively. Also, BSF are the same for this set of analysis with doping concentration of 1E20 cm^{-3}. The EQE results are quite similar with difference under 0.5%, so the graph is not shown

here. The reason for difference to be so small is that the emitter is located at the back of the device, the electric field is strong enough for most of photogenerated carrier collection. Moreover, most of absorptions are happening at the front surface, so the doping concentration of emitter does not vary the EQE much. However, voltage performance differences due to emitter doping concentration is observed and presented in the J-V and P-V plots in Fig. 3.7. Interesting observation is that the device with low BSF doping level (1E18 cm^{-3}), the Voc drops significantly. That means, at a low doping level of about 1E18 cm^{-3}, the effect of surface passivation is weakened, more surface recombination at the contact will result in lower Voc output.

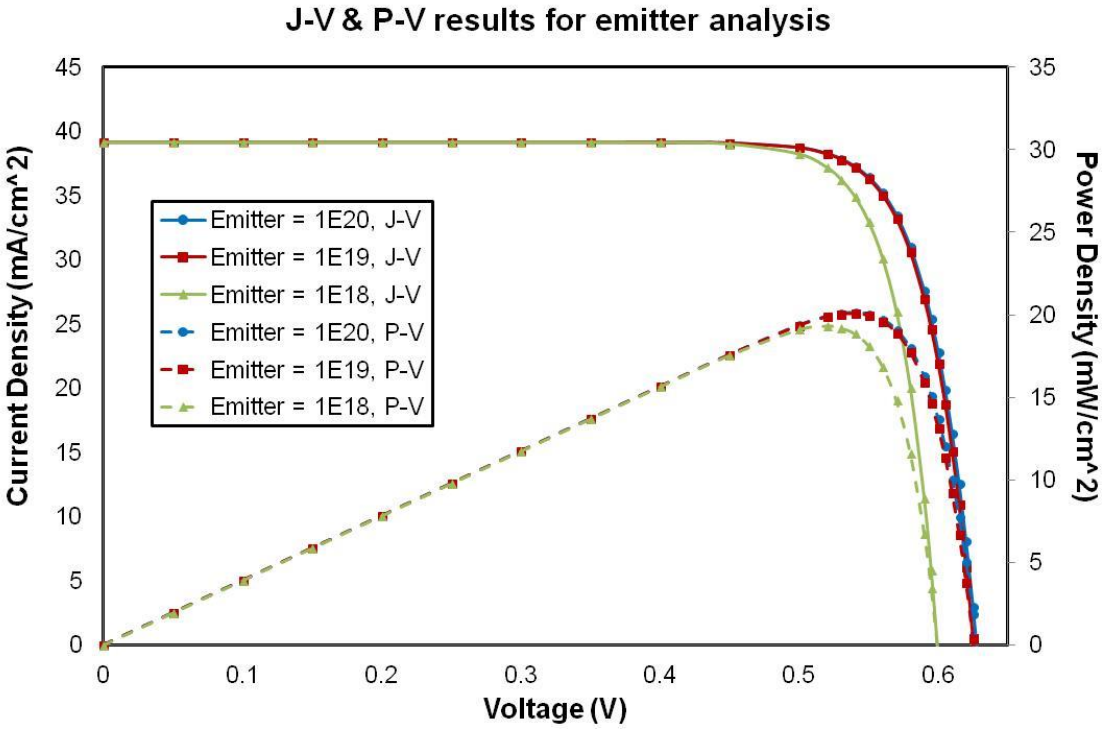


Figure 3.7 J-V and P-V result comparison for different emitter doping concentration

Parallel analysis on emitter width is carried out. Results are showing that wider emitter has slight gain in current output comparing to wider BSF. The short circuit current for emitter width of 5 µm, 4 µm, 3 µm are 39.2 mA/cm^2, 39.1 mA/cm^2, and 39.0 mA/cm^2, respectively. The plots are omitted because the difference is minor and difficult to tell from graphs.

3.1.4 Simulation on Different Pitch Size

Although theoretically smaller pitch size should generate more accurate simulation results (given certain amount of calculation capability), there is still possibilities that the pitch size may affect the device performance to a certain degree. Therefore, a series of simulation is performed using the same device structure and parameters with different pitch sizes, as shown in Table 3.3.

Table 3. 3 Key parameters for pitch size simulation on IBC solar cells

Cell Structure	IBC Solar Cell
Substrate MCL	1000 µs
Substrate Thickness	100 µm
Pitch Size	30.4 µm, 76 µm, 152 µm
Simulation Unit Size	15.2 µm, 38 µm, 76 µm
Emitter Coverage	10.4 µm, 26 µm, 52 µm
Back Surface Field Coverage	4.2 µm, 10.5 µm, 21 µm
Gap between n+ and p+	1.2 µm, 3 µm, 6 µm
Light Confinement	SiN_x ARC
Substrate Doping Level	5E15 cm^{-3}
Substrate Doping Profile	Uniform
Peak Doping in Emitter	1E20 cm^{-3}
Doping Profile in Emitter	Rotating Vertical Profile by Ratio of 0.75
Peak Doping in Back Surface Field	1E20 cm^{-3}
Doping Profile in Back Surface Field	Rotating Vertical Profile by Ratio of 0.75
Peak Doping in Front Surface Field	1E20 cm^{-3}
Doping Profile in Front Surface Field	Uniform
Front Passivation	Front Surface Field & SiN_x Passivation
Front Surface Recombination Velocity	10 cm/s
Front Surface Field Thickness	0.02 µm
Gap Passivation	SiN_x Passivation
Junction Edge Refinement	Re-grid at doping difference above a factor of 10
Electrode Resistance	Neglected

The simulation results show that even with 5 times difference in pitch sizes, the simulated device performance are still very similar. One expected change, that is the Fill Factor, is observed but again in a very small amount. Because the simulated EQE, J-V and P-V plots are almost identical, the graphs are omitted here. Detailed device performance results are presented in Table. 3.4.

Table 3. 4 Device performance summary for pitch size simulation on IBC solar cells

Pitch Size (μm)	Finger Width (μm)	Voc (mV)	Isc (mA/cm^2)	FF (%)	Eff (%)
30. 4	20	695	39. 17	82. 95	22. 58
76	50	696	39. 17	82. 88	22. 60
152	100	696	39. 16	82. 83	22. 58

3.1.5 Simulation on Front Surface Field (FSF)

Front Surface Field (FSF) is a critical component for IBC solar cells [42,43]. At the beginning of FSF development, it was mainly focused on achieving reasonable Fill Factor (FF) for the devices. Because IBC solar cells are usually fabricated on extremely lightly doped substrate to achieve high MCL, and the lightly doped substrate leads to high internal resistance. The FSF is applied as a bypass for lateral current flow. However, as the substrates for IBC solar cells getting thinner and thinner, the fabrication technologies for Si wafers getting better and better, MCL requirement is less critical (although still important) and extremely lightly doped material is no longer essential for achieving high MCL. Therefore, more detailed FSF analysis should be carried out to understand the impact on every aspect of device performance, especially for ultra-thin substrate devices.

A series of simulation is performed with different FSF schemes: no FSF, FSF of 1E19, 5E19, 1E20 cm^{-3} doping concentration, respectively. The EQE results of FSF doping concentration analysis is shown in Fig. 3.8.

The simulation parameters other than FSF properties are the same as those in section 3.2 with 100 μm finger width. So the parameter details are not repeated here.

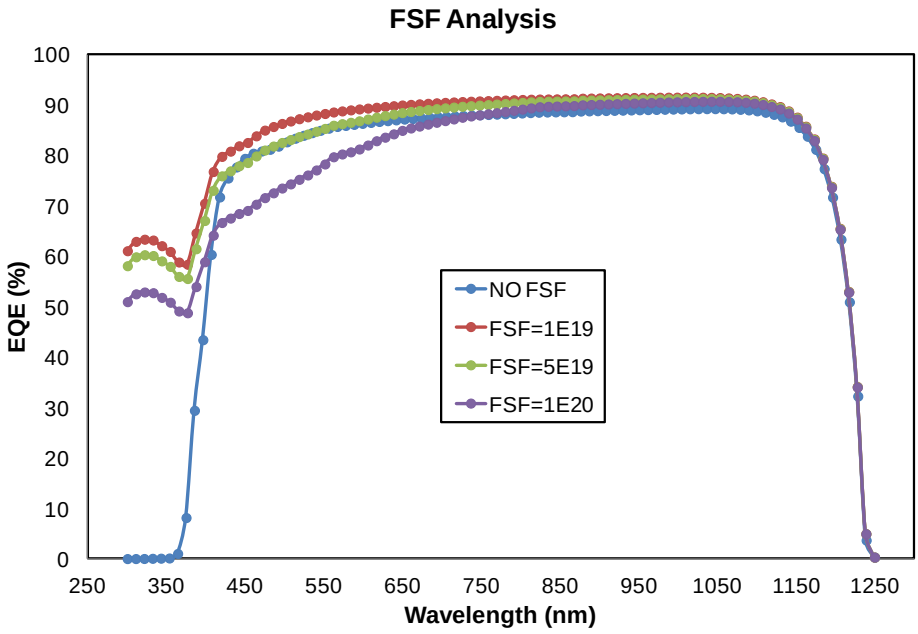


Figure 3.8 EQE result comparison for different FSF schemes

The EQE results show obvious benefit on blue response for all devices with FSF comparing to the one without. In addition, lightly doped FSF exhibits superior blue response than heavier doped ones. More detailed device performances including Voc, Isc, FF and Efficiency, are presented in Fig. 3.9.

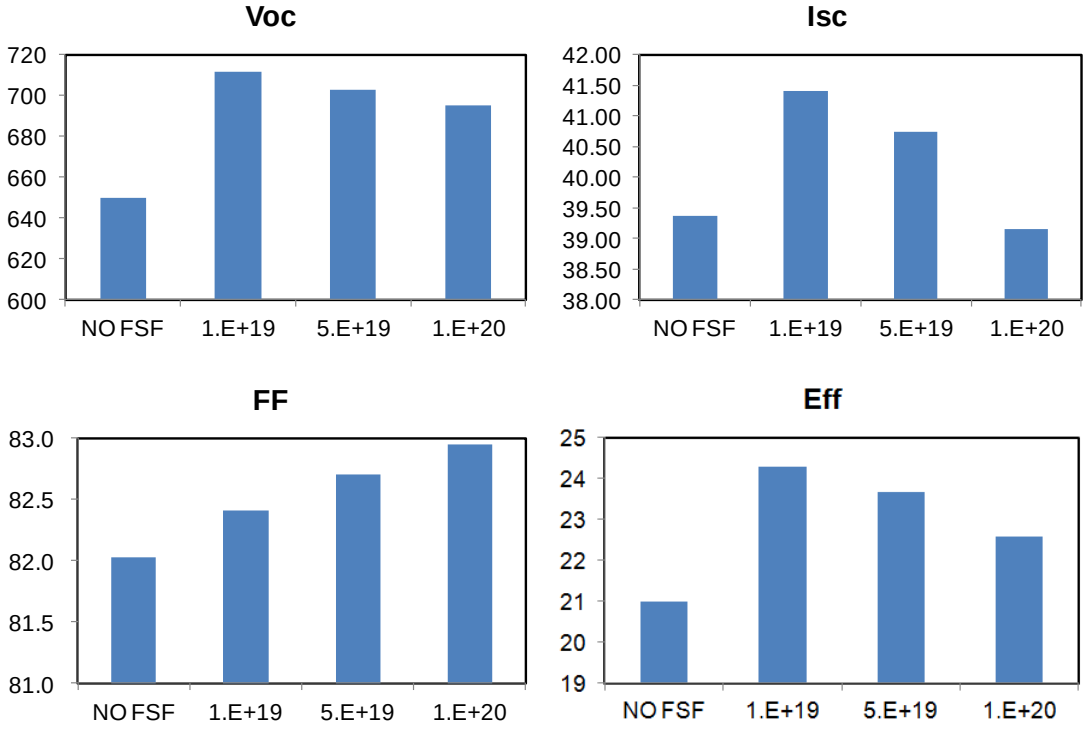


Figure 3.9 Device performance result comparison for different FSF schemes

From the simulation results, one important outcome is that, although heavily doped FSF gives a higher FF, the Voc and Isc output are both superior with lightly doped FSF. This is in agreement with the experiment results as reported in [44]. However, the analysis performed in [44] is more complicated and not focused on FSF doping levels. Therefore, further analysis is required to understand this behavior. Also, different thickness of FSF with the same doping level of 1E20 cm^{-3} is analyzed. From the simulation results, FSF thickness up to 50 nm has limited effect on cell performance. However, the undesired absorption of the FSF exhibit lower current output at 100 nm thickness. Detailed simulation data is listed in Table. 3.5.

Table 3. 5 Device performance summary for FSF simulation on IBC solar cells

	FSF conditions		Device Performance			
Sample ID	Thickness (nm)	Doping Level (cm^{-3})	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
FSF1	20	1.00E+20	695	39.16	82.95	22.58
FSF2	30	1.00E+20	695	39.19	82.95	22.59
FSF3	50	1.00E+20	695	39.18	82.93	22.58
FSF4	100	1.00E+20	695	39.06	82.88	22.50
FSF5	20	1.00E+19	712	41.41	82.42	24.30
FSF6	20	5.00E+19	703	40.74	82.71	23.69
FSF7	20	1.00E+20	695	39.16	82.95	22.58
woFSF	N/A	N/A	650	39.37	82.03	20.99

3.2 Impact of Substrate Thickness & MCL on IBC Solar Cells

--- Collaboration Project with Ubiquity Solar Inc.

The identification on the importance of substrate thickness and MCL aligns with the scope of a Canadian photovoltaic silicon material supplier start-up company, Ubiquity Solar Inc. As requested, a series of simulations based on the company's prototype silicon wafer properties is performed. Again, IBC solar cell structure is applied. To make the optical input more close to reality, the illumination spectrum is applied according to experimental results from real Si wafer samples with the combination of light confinement schemes of Random Pyramid Texturing and SiN_x ARC. Detailed simulation parameters are listed below in Table. 3.6. The simulation results were presented at IEEE 32nd EU-PVSEC in 2016 [45].

Table 3. 6 Key parameters for substrate thickness and MCL simulation on IBC solar cells

Cell Structure	IBC Solar Cell
Substrate MCL	100 - 3000 µs
Substrate Thickness	140 - 200 µm
Pitch Size	200 µm
Simulation Unit Size	100 µm
Emitter Coverage	70 µm
Back Surface Field Coverage	15 µm
Gap between n+ and p+	15 µm
Light Confinement	Random Pyramid Texturing + SiN_x ARC
Substrate Doping Level	5E15 cm^{-3}
Substrate Doping Profile	Uniform
Peak Doping in Emitter	1E20 cm^{-3}
Doping Profile in Emitter	Rotating Vertical Profile by Ratio of 0.75
Peak Doping in Back Surface Field	1E20 cm^{-3}
Doping Profile in Back Surface Field	Rotating Vertical Profile by Ratio of 0.75
Peak Doping in Front Surface Field	1E19 cm^{-3}
Doping Profile in Front Surface Field	Uniform
Front Passivation	Front Surface Field & SiN_x Passivation
Front Surface Recombination Velocity	10 cm/s
Front Surface Field Thickness	0.02 µm
Gap Passivation	SiN_x Passivation
Junction Edge Refinement	Re-grid at doping difference above a factor of 10
Electrode Resistance	Neglected

As marked above, in this set of simulation, the substrate thickness values are chosen from 140 µm to 200 µm, which is from the thickness of prototype Ubiquity Solar test wafer to the thickness of commercial “thin” wafer. The MCL values are chosen from 100 µs to 3000 µs, which is from typical value for Cz wafer to high quality FZ wafer. The energy conversion efficiency, open circuit voltage, short circuit current density output comparison between different MCL and thickness values are presented in Fig. 3.10.

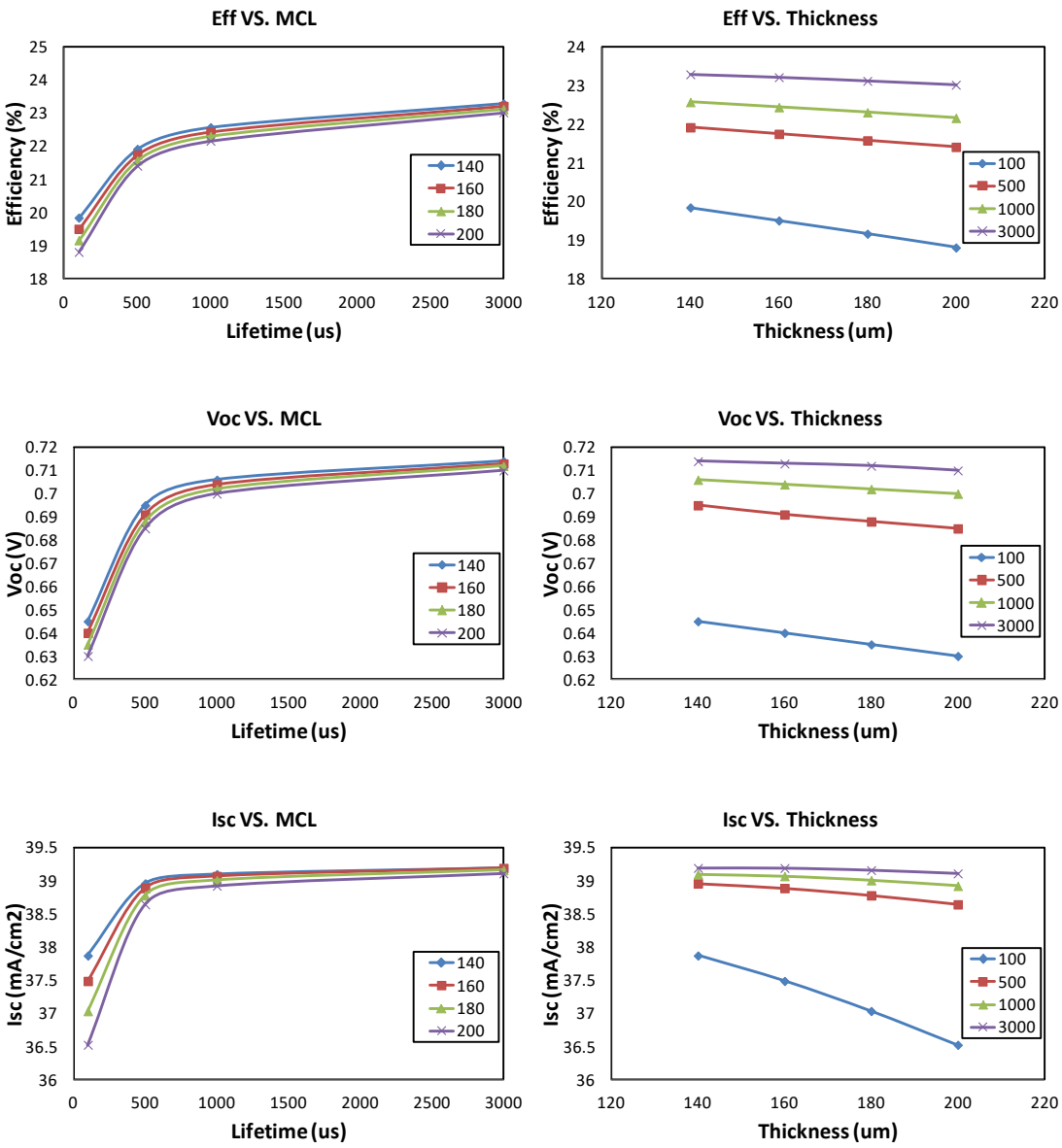


Figure 3.10 Substrate thickness and MCL simulation result comparison for IBC solar cells

The detailed simulation results, including I_{sc}, V_{oc}, FF and Efficiency, for each parameter set are listed in Table 3.7.

Table 3. 7 Key parameters for substrate thickness and MCL simulation on IBC solar cells

MCL (μs)	Thickness (μm)	Isc (mA/cm²)	Voc (V)	FF (%)	Efficiency (%)
100	140	37.8729	0.645	81.24	19.85
	160	37.489	0.640	81.30	19.51
	180	37.0353	0.635	81.50	19.17

500	200	36.5258	0.630	81.74	18.81
	140	38.9615	0.695	80.95	21.92
	160	38.8903	0.691	80.93	21.75
	180	38.7812	0.688	80.87	21.58
	200	38.6453	0.685	80.89	21.41
1000	140	39.1013	0.706	81.77	22.57
	160	39.0717	0.704	81.58	22.44
	180	39.0091	0.702	81.46	22.31
	200	38.9246	0.700	81.34	22.16
3000	140	39.195	0.714	83.22	23.29
	160	39.1934	0.713	83.07	23.21
	180	39.1623	0.712	82.92	23.12
	200	39.1127	0.710	82.90	23.02

Two observations can be concluded from this set of simulations: 1. the state-of-the-art Si wafer thickness for PV industry is still thicker than the optimized substrate thickness for IBC solar cells. Therefore, typical device output exhibits the tread of "the thinner the better"; 2. higher MCL values promise higher device performance as expected, the benefits from high MCL tend to saturate for even higher values. Device performance degradation due to low MCL values is less obvious for devices with thinner substrates, the same as previous simulation results.

3.3 Simulation of poly-Si/c-Si Heterojunction Solar Cells

AFORS-HET is a simulation software specifically designed for heterojunction solar cells. Many articles on typical HIT solar cell simulations are published with AFORS-HET [46-48]. However, poly-Si/c-Si heterojunction simulation is rarely reported. In this section, AFORS-HET is applied for poly-Si/c-Si heterojunction solar cells. Effects of defects in the poly-Si emitter and detects at the heterojunction interface on the final device performance are analyzed. Detailed simulation design and results are presented below.

3.3.1 Poly-Si/c-Si Heterojunction Solar Cell Structure

A simple poly-Si/c-Si heterojunction solar cell structure is applied in the simulation, as shown in Fig. 3. 11. Besides poly-Si emitter, c-Si substrate and electrodes, a defective interface layer is included to model the defective interface.

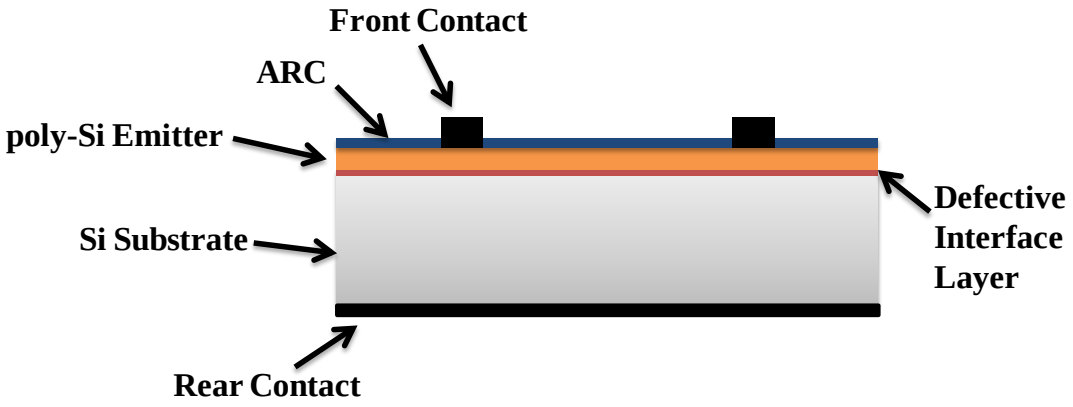


Figure 3.11 Poly-Si/c-Si heterojunction solar cell structure applied in AFORS-HET simulation

After the definition of the solar cell structure, the generated energy band diagram of the poly-Si/c-Si heterojunction is presented in Fig. 3.12. The electron affinity of poly-Si and c-Si substrate are the same (4.05 eV). However, the band gap of poly-Si (1.2 eV) is slightly higher than that of c-Si substrate (1.12 eV). Therefore, a small off-set at valence band is observed at heterojunction interface.

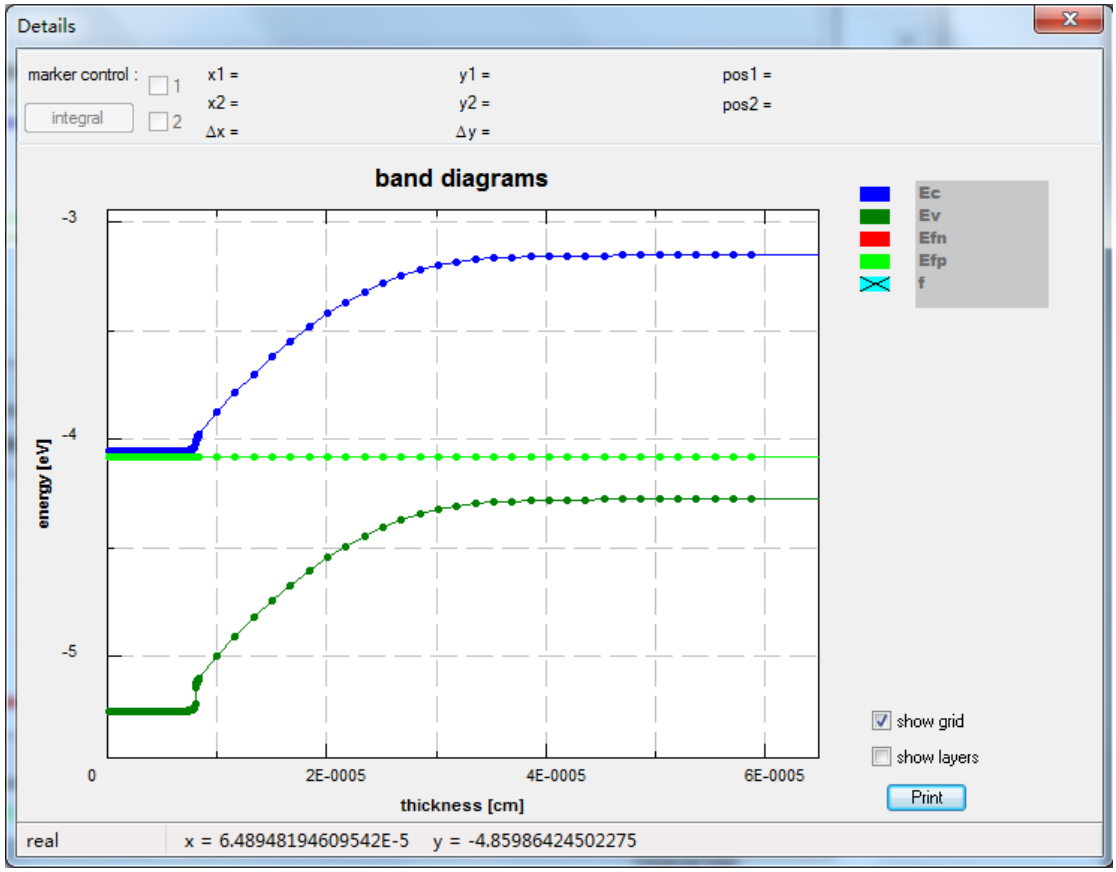


Figure 3.12 Energy band diagram of designed poly-Si/c-Si heterojunction structure

3.3.2 Simulation Parameters

In addition to the definition of emitter layer (n+ poly-Si) and substrate c-Si, a defective interface layer should be defined in between. The simulation on heterojunction interface is rather complicated and many assumptions are required. For example, the thickness of the defective interface layer is commonly considered to be in the nanometer range [49], the capture cross section of the donor and acceptor like defects are estimated as ~10^{-14} cm^{-3} [50]. Moreover, the defective layer is likely to present on both sides of the heterojunction. However, if both sides of the heterojunction are defined with defective layer, then the interface of the two defined defective layers will bring in further complication and uncertainties. Therefore, in this work, the defective interface layer is defined entirely on the crystalline Si side with a band gap of 1.12 eV. Additional parameters such as effective density of states, electron and hole mobility, band tail parameters (for poly-Si layer) are extracted from AFORS-HET material library and enriched by literatures [51,52].

The thickness of the poly-Si emitter, the defective interface layer and the c-Si substrate are 80 nm, 3 nm and 300 µm, respectively. Detailed layer properties of the poly-Si/c-Si heterojunction in the simulation are presented in Table 3.8.

Table 3. 8 Key parameters for substrate thickness and MCL simulation on IBC solar cells

Parameters and units (e and h for electrons and holes respectively)	poly-Si (n) (Poly-crystalline)	Defective interface layer
General electrical properties		
Dielectric constant [--]	11.9	11.9
Electron affinity [eV]	4.05	4.05
Band gap [eV]	1.2	1.12
Effective density of states in the CB [cm^{-3}]	$3x10^{19}$	$2.8x10^{19}$
Effective density of states in the VB [cm^{-3}]	$2x10^{19}$	$2.7x10^{19}$
Electron mobility [$cm^2V^{-1}s^{-1}$]	40	1041
Hole mobility [$cm^2V^{-1}s^{-1}$]	4	413
Ionized acceptor concentration [cm^{-3}]	0	$1.5x10^{16}$
Ionized donor concentration [cm^{-3}]	$9x10^{18}$	0
Thermal velocity of holes [cm/s]	$1x10^7$	$1x10^7$
Thermal velocity of electrons [cm/s]	$1x10^7$	$1x10^7$
Layer density [g cm^{-3}]	2.33	2.33
Effective minority carrier diffusion length [nm]	20	----
Band tail parameters		
Valence band tail donor-like states [$cm^{-3}eV^{-1}$]	$2x10^{20}$	----
Valence band tail capture cross section, e [cm^{-2}]	$1x10^{-15}$	----
Valence band tail capture cross section, h [cm^{-2}]	$1x10^{-17}$	----
Valence band tail Urbach energy [eV]	0.01	----
Conduction band tail acceptor-like states [$cm^{-3}eV^{-1}$]	$2x10^{20}$	----
Conduction band tail capture cross section, e, [cm^{-2}]	$1x10^{-17}$	----
Conduction band tail capture cross section, h, [cm^{-2}]	$1x10^{-15}$	----
Conduction band tail Urbach energy [eV]	0.01	----
Flat band distribution parameters		
Density of donor-like midgap states [$cm^{-3}eV^{-1}$]	$3x10^{16}$ – $5.6x10^{18}$	0 - $5.9\ x10^{18}$
Donor-like capture cross section, e [cm^{-2}]	$1x10^{-14}$	$1x10^{-14}$
Donor-like capture cross section, h [cm^{-2}]	$1x10^{-15}$	$1x10^{-14}$
Density of acceptor-like midgap states [$cm^{-3}eV^{-1}$]	$3x10^{16}$ – $5.6x10^{18}$	0 - $5.9\ x10^{18}$
Acceptor-like capture cross section, e, [cm^{-2}]	$1x10^{-15}$	$1x10^{-14}$
Acceptor-like capture cross section, h, [cm^{-2}]	$1x10^{-14}$	$1x10^{-14}$
Switch over energy [eV]	0.6	0.56

3.3.3 Effect of Emitter Defect Density

To identify the effect of emitter defect density on poly-Si/c-Si heterojunction solar cells, the density of flat-band mid-gap states are varied from the typical value of 1.8×10^{16} to 1×10^{19} cm^{-3} while exponential tail states are kept unchanged, as shown in Fig. 3.13.

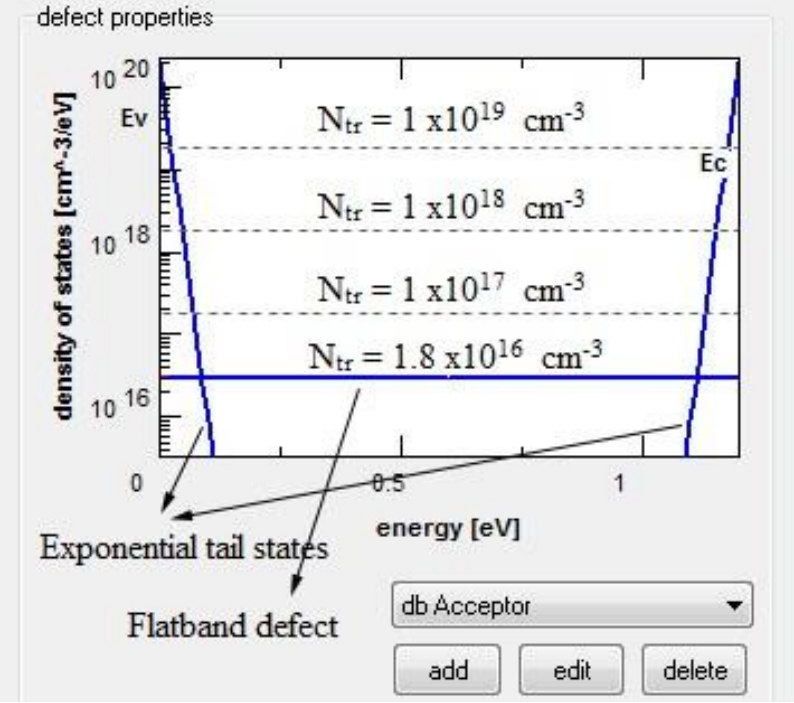


Figure 3.13 Density of states in poly-Si emitter layer

The defects in the emitter layer are the recombination centres for the photo-generated carriers. Therefore, the increase of emitter layer defect density has an obvious effect on current output. Specifically, the poly-Si/c-Si heterojunction structure has obvious different blue response with different defect density levels, as shown in the quantum efficiency results in Fig. 3.14. This is because short wavelength photons are absorbed within or closer to the emitter layer.

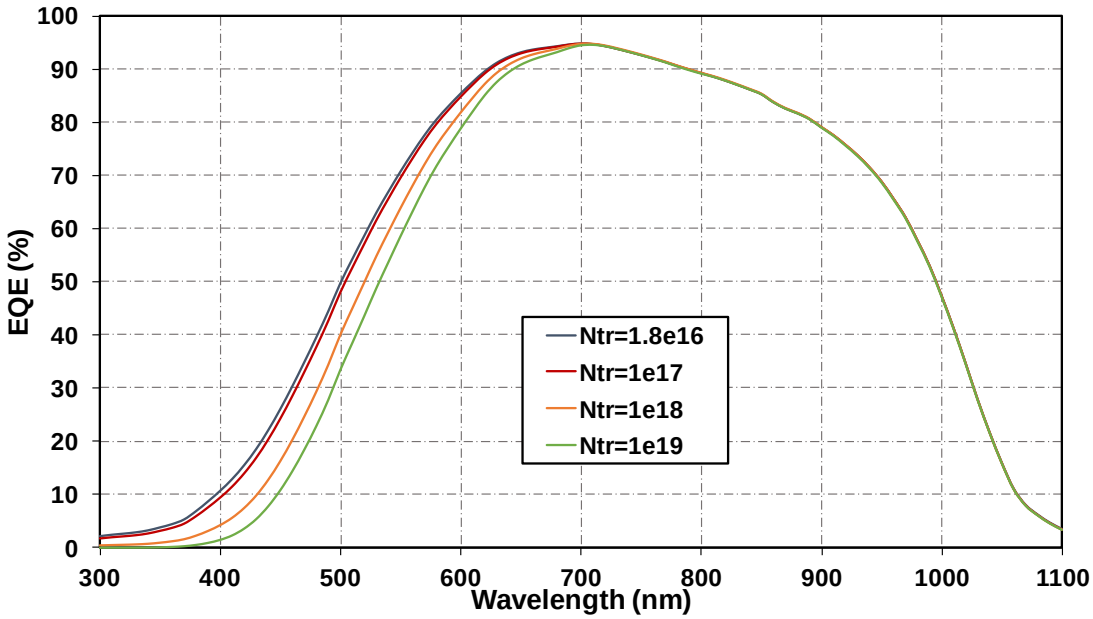


Figure 3.14 EQE results from poly-Si/c-Si heterojunction solar cells with different defect density levels in poly-Si emitter layer

Higher defect density levels result in lower blue response because more recombination occurs close to the front surface. That means better emitter properties will improve the final device blue response and therefore improve the overall energy conversion efficiency.

3.3.4 Effect of Interface Defect Density

Simulations on poly-Si/c-Si heterojunction solar cells are performed with different interface defect density (D_{it}) to analyze the effect of interface properties on final device performance. D_{it} values are changed from optimum to 1×10^{12} cm^{-2}, the corresponding device performances, J-V and P-V characteristics are presented in Fig. 3.15.

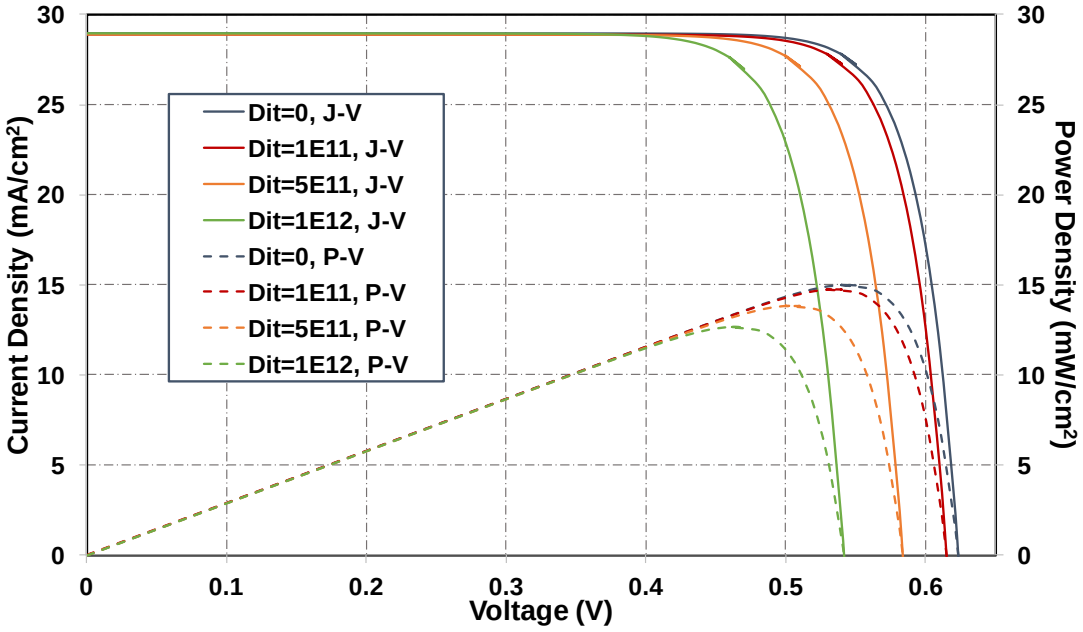


Figure 3.15 Illuminated I-V and P-V results from poly-Si/c-Si heterojunction solar cells with different level of defect density at interface

The quantum efficiency results of the simulation show that the difference in current output with different interface defects is limited. This is due to the limitation of the assumption made above, that the defective layer is entirely on the c-Si side. The interface defect density should also be the recombination centers for photo-generated carriers, especially for blue photons, as will be presented in Chapter 5. However, obvious degradation in voltage output is observed with increasing defects at the interface. This is because the defects will increase recombination and also weaken the junction, because the defects are in the middle of the junction.

3.4 Conclusions

IBC solar cells are simulated with advanced 2-D simulation software. The bulk MCL has a significate effect on Voc output. With the bulk MCL changing from 30 μs to 1 ms, the Voc output can benefit up to 50 mV for the simulated substrate thickness of 200 um. As will be discussed again in the following chapters, the substrate MCL can be a strong limiting factor for the fabricated devices. The Isc output is not only related to the substrate MCL, but also strongly affected by the substrate thickness. Device with thinner substrate has a higher tolerance on substrate MCL levels.

The BSF doping level initially only affect the voltage output. However, the absence of BSF can result in considerably amount of loss in current output due to recombination. The emitter doping level of the solar cell does not affect device performance much until it reaches a relatively low value, i.e. 1×10^{18} cm^{-3}. This is an important limiting factor for designing emitter profiles in fabrication processes such as etch-back process.

Poly-Si/c-Si heterojunction solar cells are simulated with AFORS-HET software. It is found that the emitter defect density has a strong effect on the quantum efficiency of short wavelength photons and therefore the output current. The interface defect density mainly affects the Voc output. The effect on quantum efficiency by the interface defect density is rather limited. However, it is believed that this is due to the limitations from the defective layer definition in the simulation process.

CHAPTER 4

BASE TECHNOLOGY DEVELOPMENT AND ANALYSIS FOR SI SOLAR CELLS

In this chapter, the main Si processing technologies are introduced in details. First, baseline technologies for Si high efficiency solar cells are presented. Second, parameters that affect the performance of each process are compared, analyzed and optimized to satisfactory level. Finally, standard Si mono-junction solar cells are fabricated. The processes are presented in categories as follows: Light Confinement, Junction Formation, Surface Passivation and Metallization.

For the experimental study on each parameter, multiple devices are studied. For reported results in this thesis, the results from multiple devices are rather similar. Therefore, for consistency considerations, the results from one device for each process are presented in this Chapter and the Chapters after.

4.1 Light Confinement

Surface reflection causes part of the incoming photons lost before even entering the PV devices for energy conversion. Therefore, surface reflection is one of the most important loss mechanisms for photovoltaic devices. Minimizing the surface reflection is essential and rather effective for PV device optimization. The most commonly used methods are surface texturing and Anti-Reflection Coating (ARC).

4.1.1 Random Pyramid Texturing

Random pyramid texturing is one of the most commonly used surface light confinement method. It is achieved by alkaline etching which is less expensive comparing to other texturing methods such as RIE texturing [53]. The basic mechanism is alkaline solution has different etching rate along different Si atom planes [54]. The challenges lie on achieving close to 100% pyramid coverage and reasonable pyramid size distribution, so that surface reflection is minimized.

4.1.1.1 Experiment Process

Polished wafers are usually used for research purposes. So saw damage (about 30 μm on both sides) is not a problem for texturing, but the smooth surface is difficult for pyramid to initialize. According to my experiment results, the samples without saw damage removal step usually have some spots that are still shinny after texturing, while the other parts are reasonably textured. As a result of that, the saw damage removal process is still carried out, but with shorter period of time. It is just used to evenly roughen the polished surface. With saw damage removal etching, the resulting surface normally has a satisfied uniformity of texturing.

Texturing is a very sensitive process which could change a lot with any obscure factors involved, such as surface cleanness (always better after RCA cleaning), purity of IPA or DI water, the position where the holder is touching wafers and even different supplier of KOH pills. Detailed process sequence is shown in Fig. 4.1.

Figure 4.1 Details of texturing process

After wafer cleaning, saw damage removal is carried out in 20% KOH solution. Solution temperature is preferred to be at 80 ºC and duration of 5 min is good enough for the surface roughening. The subsequent cleaning needs to be done right after etching.

Otherwise, if silicate forms at wafer surface, it would be difficult to remove and would affect the subsequent texturing result.

The solution used for texturing is made by 2% KOH (w/v) and 7% IPA (v/v). After the KOH solution is heated to 83ºC, IPA is poured into mixture. After about 1min agitation, make sure the temperature of final mixture is stable at 80ºC, and then put samples into solution and start timing. I have been using 40min for this process.

Post texturing cleaning is important because this is the very beginning of cell fabrication, the samples will experience high temperature process later on. Standard cleaning includes two steps: HF cleaning and HCl cleaning.

4.1.1.2 Results and Analysis

With the help of optical microscope, we can see the actual pyramids at wafer surface, but normally the resolution is a problem to check the shape and distribution clearly. Besides, it can only focus on one particular size of pyramid (or only the peak or base region) at a time. Therefore, SEM images are taken for texturing quality inspections. Fig. 4.2 shows the SEM images of my texturing results with different magnification and inspection angle.

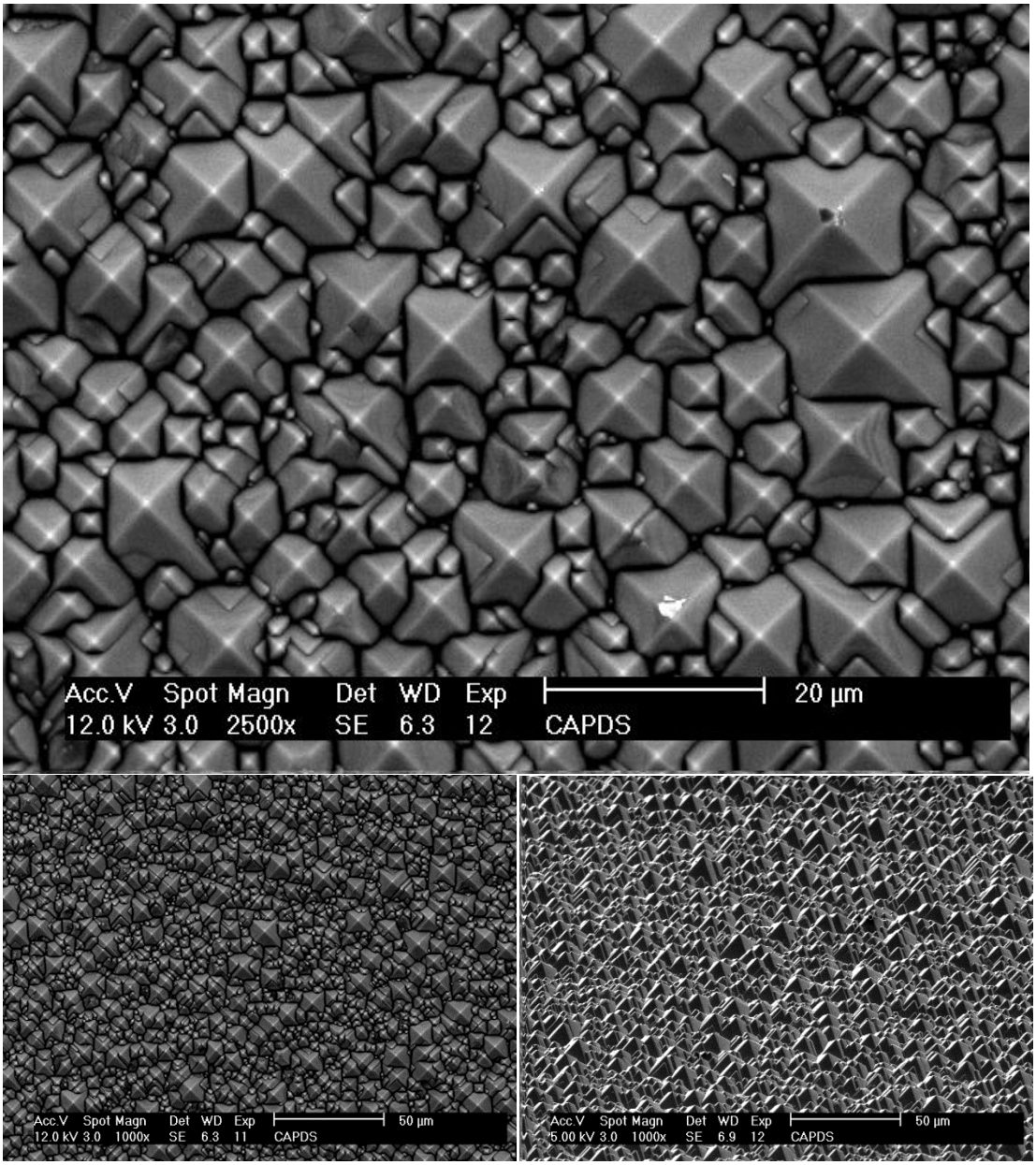


Figure 4.2 SEM images of textured silicon wafer surface

Successful texturing can bring down the reflection of silicon from 30% to about 10% at long wavelength region, and the number for short wavelength is expected to be 30% compared to 60% before texturing [55,56]. UV-Vis (Ultraviolet Visible spectroscopy) is usually used to characterize the reflection and transmission results. Fig. 4.3 demonstrates the reflection improvement from polished wafer to textured wafer. Reflection result from a textured wafer with a-SiN_x:H ARC is also presented for comparison.

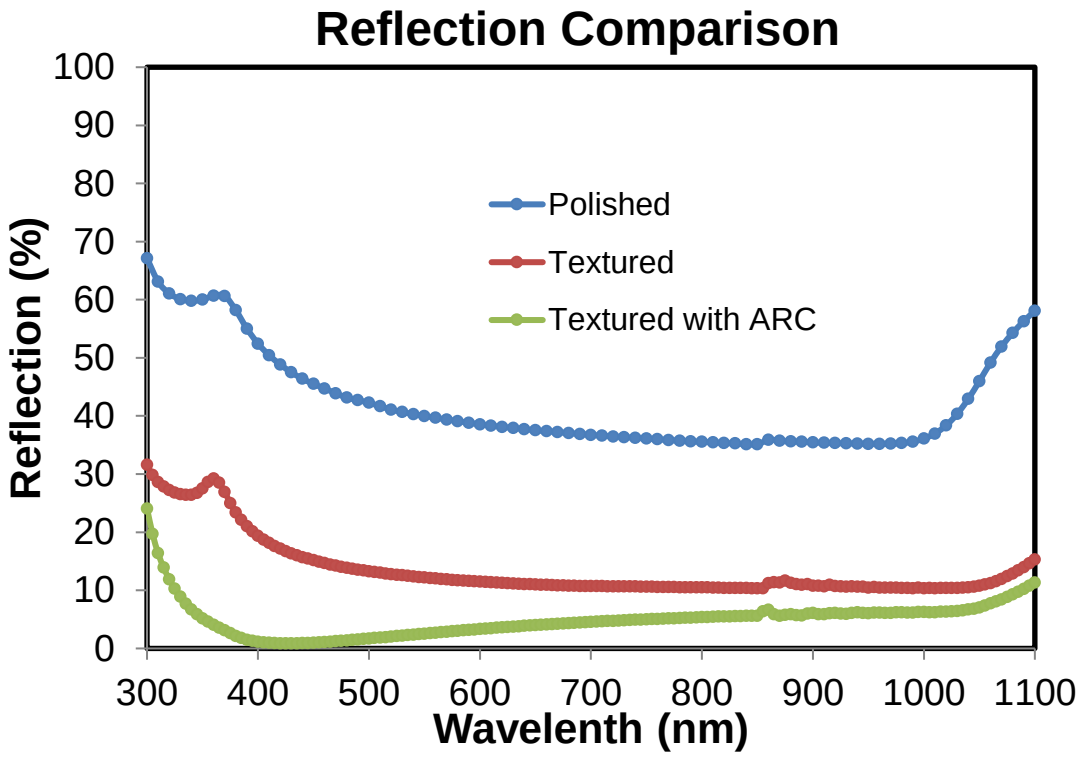


Figure 4.3 Reflection comparison of polished wafer, textured wafer and textured wafer with ARC

Reflection results above obviously proved the great reduction of optical loss from the front surface of a wafer. This process became a standard procedure for Si solar cell fabrication in CAPDS. With a proper ARC applied, the reflection in specific region could approach zero and well below 10% elsewhere. The reflection in the graph shows a thinner layer than expected. Otherwise the lowest reflection should happen at around 600 nm wavelength which is the wavelength of the strongest light component (green light) in solar spectrum. The ARC property will be discussed more in details in the section of "Passivating ARC".

As mentioned above, texturing is a very sensitive process to many controlling factors. Up to now, I have analyzed the effect of IPA concentration in a limited range. The result shows 7% of IPA is giving lowest reflection, while 10% of IPA presented smaller pyramid size and better uniformity, although reflection is a bit higher than the former recipe. Reused texturing solution could still achieve good texturing as in industry, but sometimes the result is not repeatable. Fig. 4.4 shows the comparison of texturing result with different IPA concentration in texturing solutions.

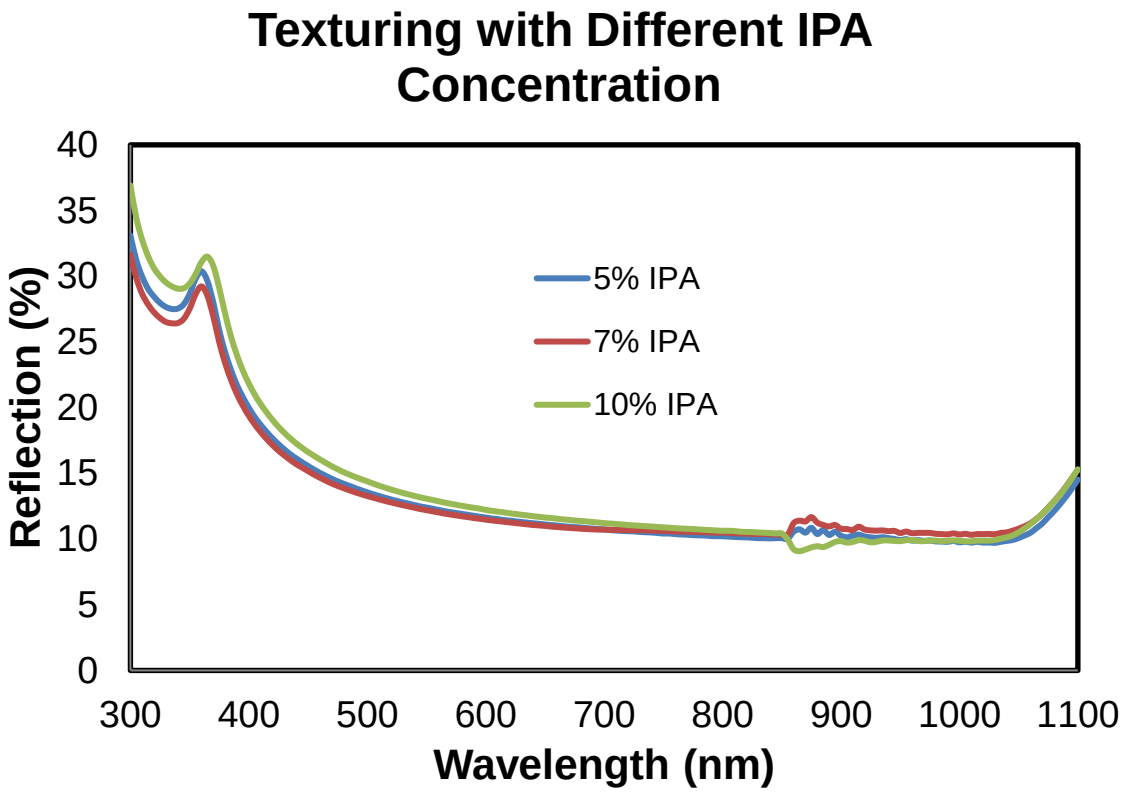


Figure 4.4 Reflection comparison of texturing with different IPA concentration

4.1.2 Anti-Reflection Coating (ARC)

There are different types of ARCs. Among all, a-SiN_x:H (or SiN_x, hereafter) is well studied and reported with good performance [57,58]. In my research, SiN_x film has been analyzed and fabricated for this layer.

4.1.2.1 Experiment Process

In CAPDS, we use direct rf-PECVD for SiN_x deposition. The schematic diagram of the system is shown in Fig. 4.5.

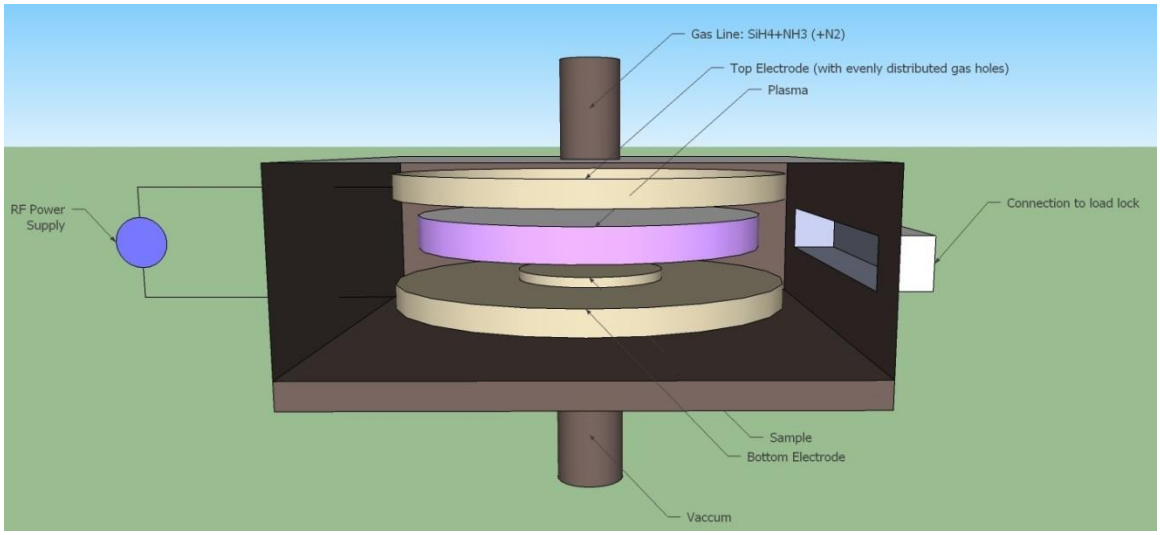


Figure 4.5 Schematic diagram of PECVD chamber in CAPDS

In the current recipe for SiN_x film deposition, substrate temperature is set to 350 ºC; pressure is 600 mTorr; power is 30 W initially to excite the plasma and lower down to 10 W for deposition. Gas flow rate for SiH_4 and NH_3 are 5 sccm and 100 sccm, respectively.

After standard RCA 1 cleaning and HF dip, samples are loaded to load lock directly. Although silicon is a great thermal conductor, 5 min of wafer pre-heating in the deposition chamber is performed to make sure of the film repeatability.

4.1.2.2 Results and Analysis

Different composition of the SiN_x films has different functions for resulted solar cells. High Si ratio usually leads to better passivation, while high N ratio often exhibits better optical properties [59,60]. The SiN_x film that is described and applied is targeting for better optical performance. By applying SiN_x as AR coating, reflection reduction is obvious from UV-Vis reflection results. Fig. 4.6 presents the reflection comparison of polished wafer surface, polished wafer with SiN_x coating and textured wafer with SiN_x coating.

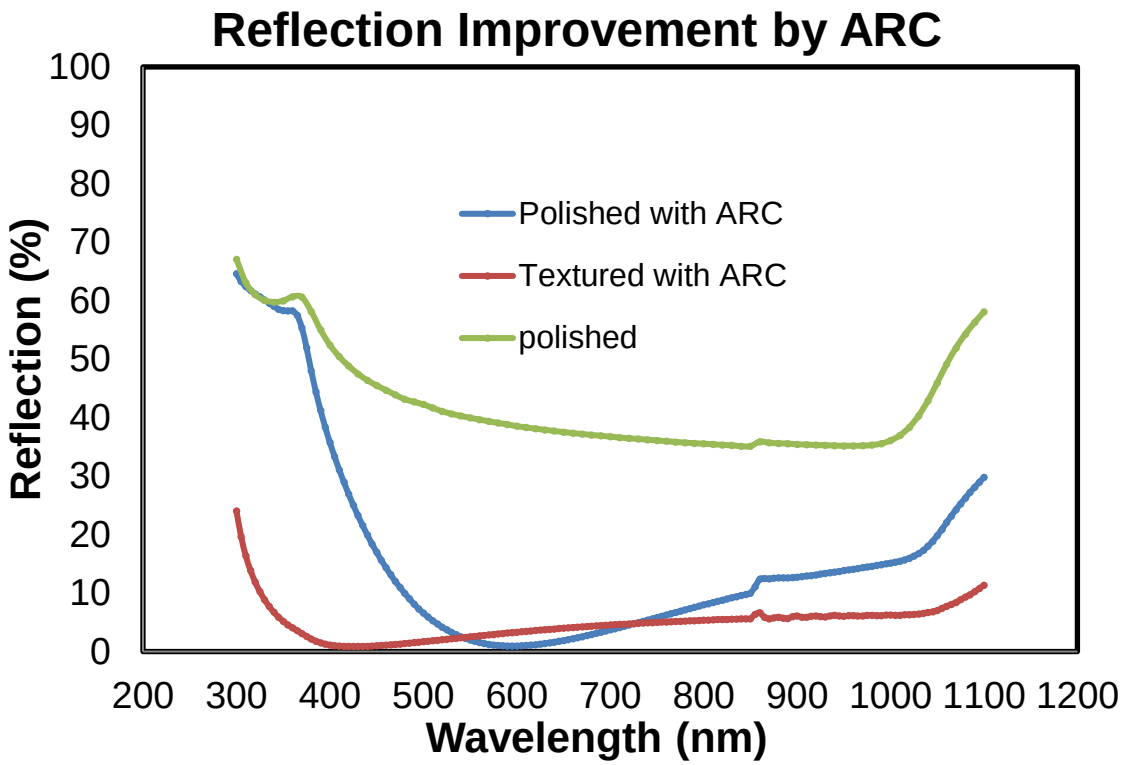


Figure 4.6 Reflection improvement of ARC

From the diagram above, it is obvious that ARC realizes dramatic reduction of optical loss. And together with texturing, wafer reflection could be well below 10% in most visible wavelength region. The refractive index is calculated to be 1.95 at 600 nm. Another thing we notice is the minimum reflection of the sample having both texturing and ARC is blue shifted. Actually, that is because the SiN_x film deposition exhibits slightly lower deposition rate on textured surface than on flat surface. And thinner ARC will lead to the blue shift of the reflection valley as will be presented in Fig. 4.7.

Optical properties of SiN_x film is closely related to film thickness. Using the deposition parameters above, deposition rate is confirmed to be approximately at 0.5 nm/s. Film thickness is designed to be 78 nm (according to reflective index at 600 nm), so the standard deposition duration for my experiment is 156 s. With different thickness, the reflection valley will shift accordingly, along with noticeable change in low and high wavelength regions. Fig. 4.7 shows the reflection result from Si wafers with different thickness of SiN_x films.

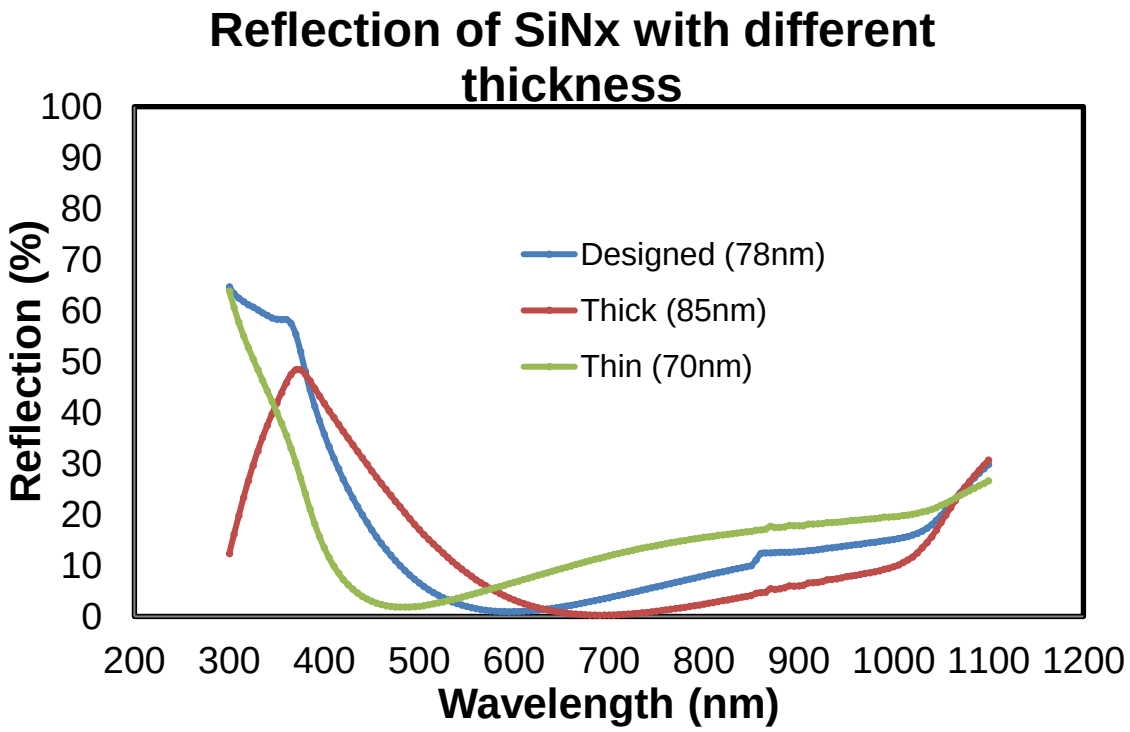


Figure 4.7 Reflection comparison of different ARC thickness

As shown in the diagram, by varying thickness, reflection can be optimized in different wavelength regions. There are several reasons why green light region (some uses 600 nm, others use 633 nm) is preferred for photovoltaic devices. First, solar spectrum has a greater photon flux in green region. That means by reducing same percentage of reflection in green region, it allows more photons entering photovoltaic device and therefore leads to more gain in energy conversion. Second, due to the mechanism of ARC layer, the closer the wavelength to the selected value is, the better the optical performance is. So the selected wavelength is preferred to be close to the middle of visible spectrum window, which is normally considered as from 300 nm to 1100 nm. Last but not least, generally speaking, the IQE (Internal Quantum Efficiency) in this region is normally higher. That means with the same increase of photon entering, more energy will benefit from this region. The physical reason laying behind this is in short wavelength region, although photons are easily absorbed, they could easily recombine due to front surface defects or "dead layer" (too heavily doped and result in low lifetime of minority carriers); in long wavelength region, photons are mostly absorbed far away from junction due to lower absorption coefficient, and this makes the usage of these low energy photons rely more on lifetime of the bulk material and the back surface

passivation (more so as the wavelength increases). Based on these facts, the 600 nm (or 633 nm) is selected as the favourable target wavelength for ARC design.

During my experiment work, it has been noticed that chamber condition has a great effect on the resulting film property. There are several users fabricating different films with the PECVD system. Typically, plasma cleaning with CF_4 gas is applied, but apparently, after certain amount of time, plasma cleaning is not sufficient for stable and well performance film deposition. Fig. 4.8 illustrates the huge difference in long wavelength reflection from two films deposited with the same recipe and thickness. The only thing different is that the film with better reflection was deposited after a thorough physical cleaning, while the other one was deposited in regular plasma cleaning with a long running history. According to the deposition history and result summarization, it is shown that the film performance is stable with several micrometer depositions on the side walls of PECVD chamber, given that there is a pre-deposition before actual film deposition. Therefore, we do not need to clean the chamber too frequently, but the chamber condition is a factor worth closely monitoring.

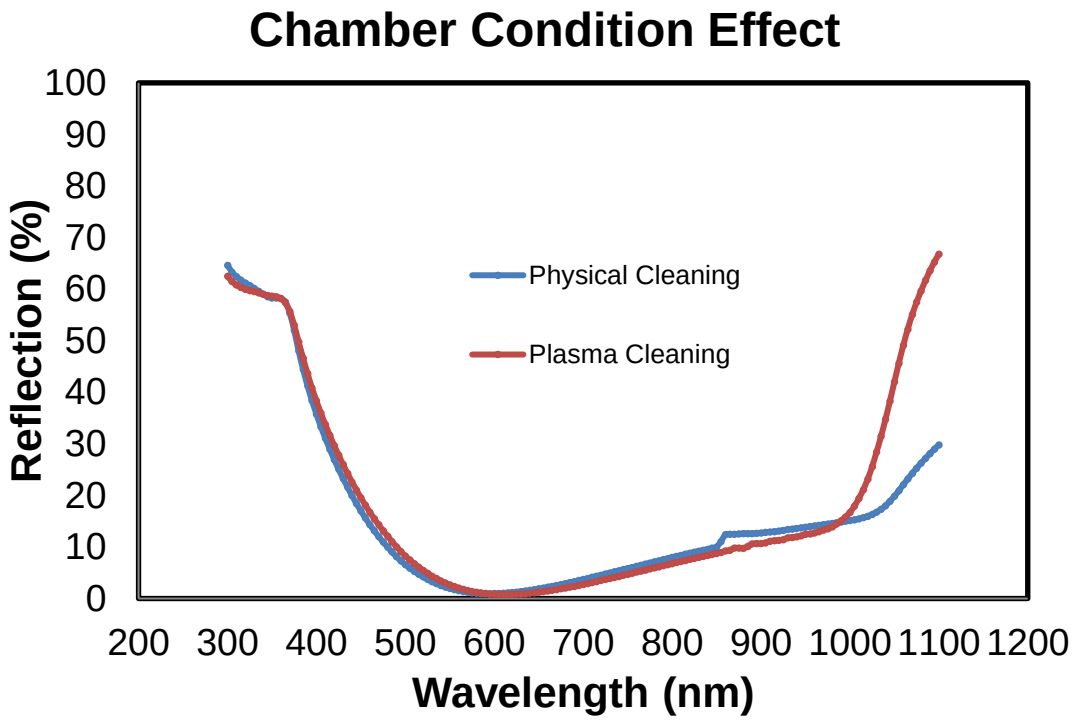


Figure 4.8 Chamber condition effect on ARC performance

All the results summarized above are the properties of SiN_x film alone. By applying the film in solar cells, we can actually see the improvement of performance in device level, and also have a better understanding to the function of this passivating ARC.

To analyze finished solar cell performance, EQE measurement is performed. EQE measurement is a typical characterization method for solar cells. It calculates the percentage of photons that produce usable carriers arriving at contacts against the incident photons on the cell surface. And the measurement takes readings from monochromatic light with different wavelength. The current density at standard illumination intensity can be extracted from the integral of all photons with respect to standard spectrum at each wavelength. Fig. 4.9 demonstrates the EQE results of simple solar cells with and without SiN_x film while other parameters are the same. For comparison proposes, the reflection results are also included in the diagram. All the other processes for fabrication are the same, including cleaning, diffusion, etch-back, contact deposition and dicing. The details about these processes will be addressed in the following sections.

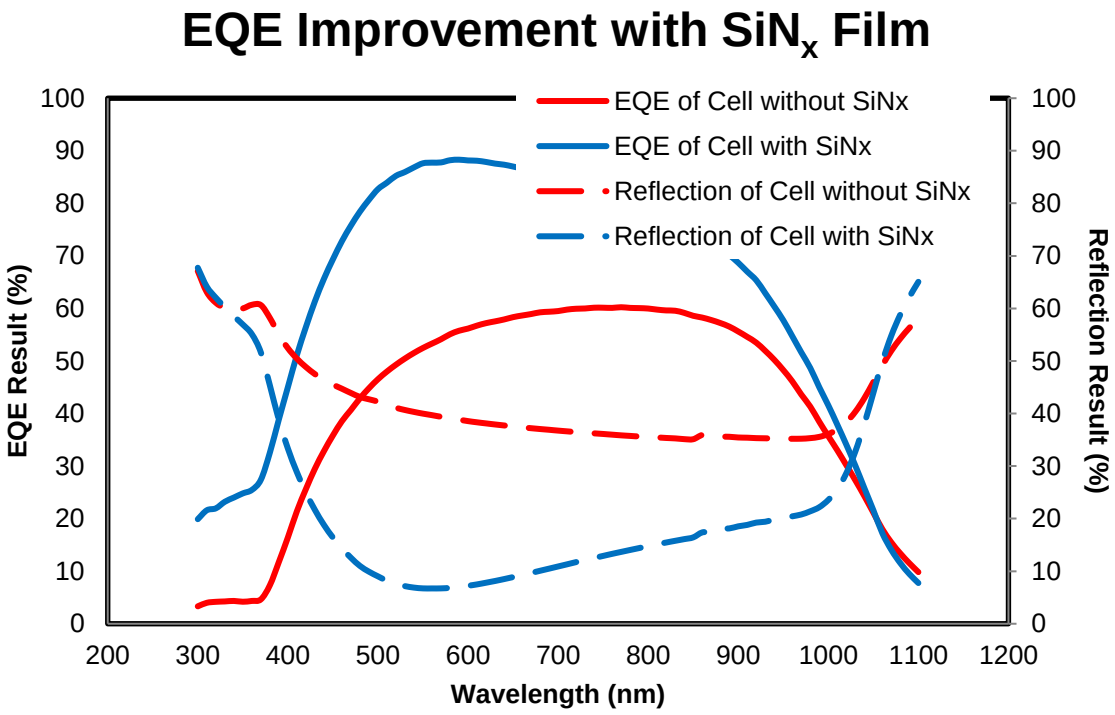


Figure 4.9 EQE improvement with SiN_x film

From the diagram, we can easily find that SiN_x film makes a huge improvement in EQE result and hence, in the cell performance. The predicted current density of the cell with

and without SiN_x film is 29.93 mA/cm^2 and 20.66 mA/cm^2, respectively. It can be concluded from the trend of EQE and reflection that the main gain of EQE in the cell with SiN_x film comes from the great reflection reduction. However, if the QE results are calculated carefully, it is found that in the short wavelength region, EQE improvement is more than the benefit from reflection. This part of improvement comes from the other effect of SiN_x film, front surface passivation. The passivation effect can be clearly seen from IQE (Internal Quantum Efficiency) result. The result will be shown and discussed in "Surface Passivation".

To demonstrate performance improvement of solar cells, illuminated I-V measurement is always the best way, because it can measure the actual output power that solar cells generate under standard illumination. Fig. 4.10 is the illuminated I-V measurement result at 100 mW/cm^2 (standard AM1.5 spectrum) from standard solar simulator for the solar cells with and without SiN_x film.

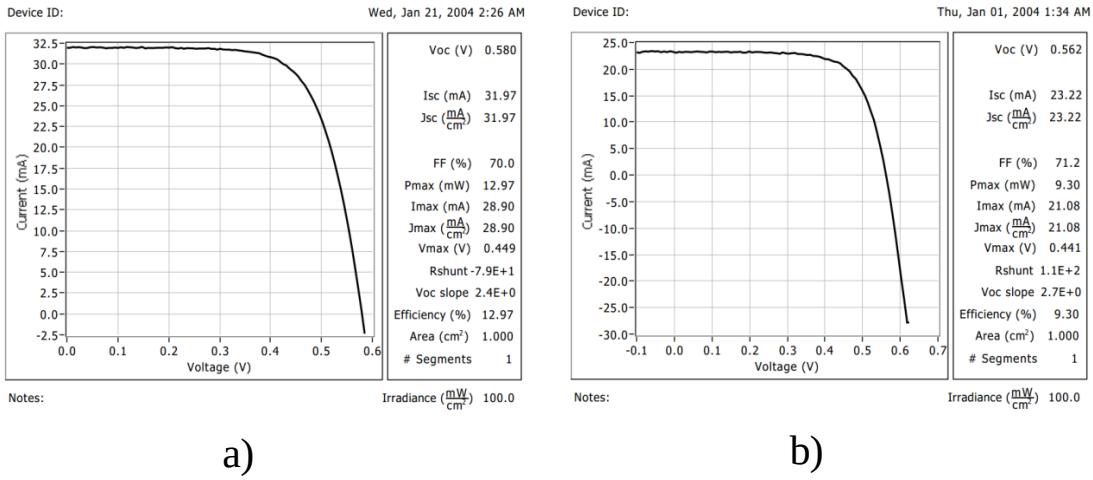


Figure 4.10 Illuminated I-V result improvement with SiN_x film a) with SiNx, b) without SiNx

V_{oc}, I_{sc} and FF (Fill Factor) are the most important parameters in illuminated I-V measurement and also for solar cell properties. First, the huge improvement in I_{sc} with SiN_x film is observed. The results are qualitatively consistent with EQE results. However, the final I_{sc} under standard illuminating is a bit higher than the predicted value from EQE for both cells. This is because solar cells normally exhibits slightly higher current output at high injection condition than at dark conditions. Second, V_{oc} results are slightly better in the cell with SiN_x film. This origins both from the surface passivation improvement and the increase in current density. Third, the FF shows a

moderate drop with SiN_x coated cell. The theoretical explanation is that increased current density makes series resistance more obvious in device performance. Also, this drop could come from any unexpected minor difference happened during contact deposition.

In sum, SiN_x has great properties as passivating AR coating. A highly repeatable thin film is developed and fabricated with satisfying quality, and the huge benefit is proved and demonstrated at device level with simple solar cell structures.

4.2 Junction Formation

4.2.1 Diffusion

Diffusion is a key step for solar cell fabrication. Typically, phosphorous is diffused in p-type wafer to form an n-type emitter or boron in n-type wafer for p-type emitter. Solid state diffusion is widely used both in industry and laboratory activities. In CAPDS, I use planar doping source for junction formation. Comparing with liquid phase diffusion, PDS (Planar Doping Source) products can promise a better uniformity and achieve more robust and repeatable junction.

The diffusion mechanism is rather straight forward both for phosphorous and boron diffusion. At diffusion temperature (normally 800 ºC to 1100 ºC for different doping sources), active component in the planner doping source decomposes to form dopant vapor, P_2O_5, for phosphorous diffusion. By products, in this case, SiO_2, are designed to stay at sample surface and removed with subsequent HF cleaning process.

4.2.1.1 System Set-ups

4.2.1.1.1 Quartz Tube

In CAPDS, systems are mostly designed for 4 inch wafers. The quartz tube for our furnace has a diameter of 120 mm. The length is approximately 2.5 m to make sure there is a uniform and steady gas flow in the center zone. There are temperature sensors in each zone of the furnace to monitor the temperature level and continuity across the tube. The tube opens are at the clean room side to eliminate any possible contaminations.

4.2.1.1.2 Doping Source

Our planar doping sources are purchased from Saint-Gobain Ceramic Materials. Specifications of these doping sources are listed in Table. 4.1.

Table 4.1 Planar doping source specifications

Dopant Type	Dopant Material	Dopant Vapor	Doping Source Series	Temperature Range (ºC)	Sheet Resistance Range(Ω/□)
N-type	Phosphorous	P_2O_5	PH-975	875-950	5-60
P-type	Boron	HBO_2	BN-950	775-1000	20-500

The doping sources are not ready for diffusion as arrived. They have to be activated at the beginning. Phosphorous doping source activation is straight forward by annealing with 100% N_2 for eight hours. Boron doping source need a more complex process with oxidation and stabilization.

4.2.1.2 Diffusion Process

When the furnace is not running diffusion process, the doping sources and dummy wafers are loaded in furnace tube in standby mode. That is 400 ºC with N_2 flowing at 2 slpm. For diffusion process, the N_2 flow rate is increased to 3 slpm. And temperature profile is designed precisely to maintain repeatable diffusion results. The diffusion temperature for phosphorous and boron are 900 ºC and 950 ºC, and the plateau time are 45 min and 60 min, respectively. For energy saving propose, the furnace is cooled naturally. So only the temperature ramping and plateau time are controlled. An example of temperature profile for phosphorous diffusion is shown in Fig. 4.11.

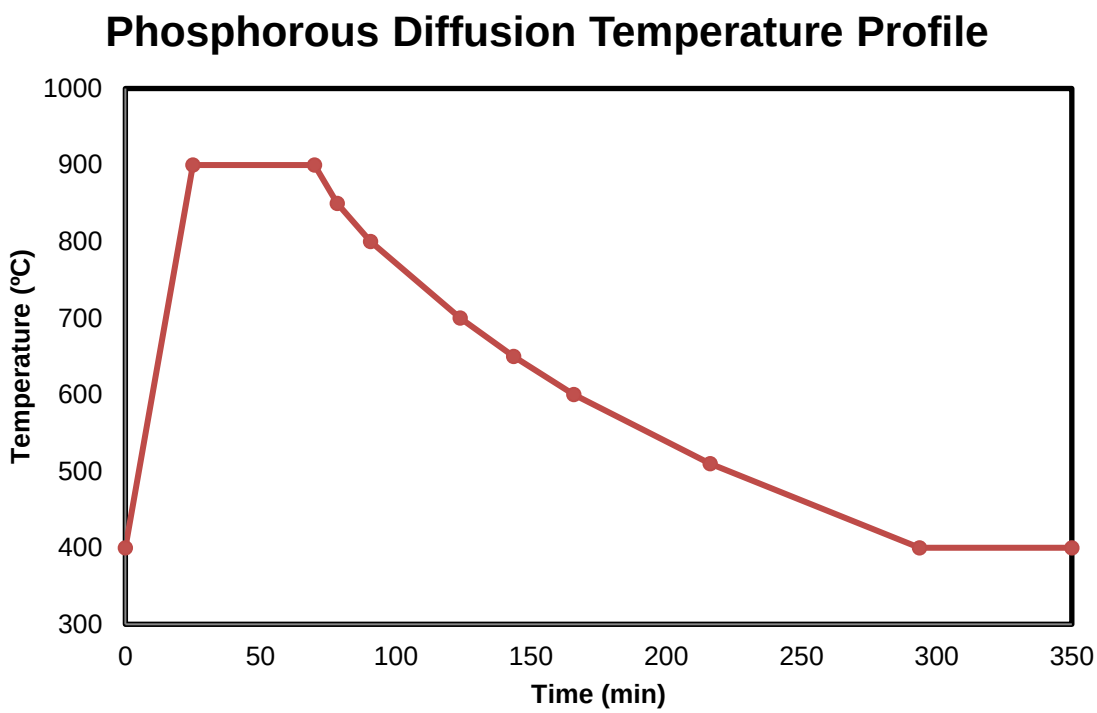


Figure 4.11 Temperature profile of phosphorous diffusion

After diffusion, there will be a layer of glass on the surface of silicon sample, also some native oxide on the other side. To remove this layer of glass and possible oxide, diffused wafers are put into 10% HF solution for 2 min after diffusion process.

4.2.1.3 Results

The planar doping source supplier has technical files for expected parameters such as sheet resistance, junction depth with different diffusion temperature and time. For phosphorous diffusion, medium temperature and time are selected to provide better stability and large enough window for etch back process which will be introduced in next section.

After diffusion, sheet resistance mapping was carried out for characterization. The sheet resistance mapping was done by Semi-lab tool. More often, when the processes are well known, sheet resistance is measured by four-point probe or Napson tools which are smaller and located inside clean room. Anyway, Semi-lab contactless sheet resistance mapping gives better view of diffusion uniformity. Fig. 4.12 shows the mapping result with 1 mm raster.

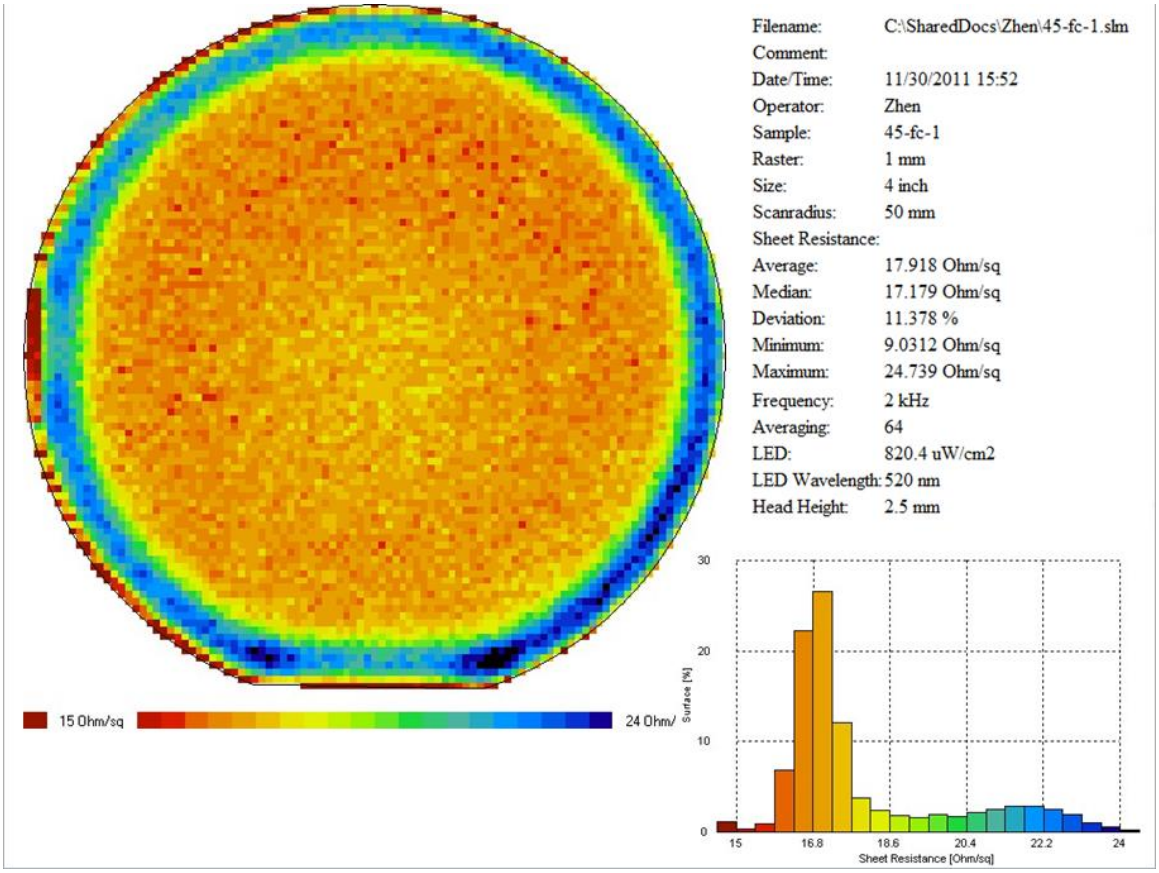


Figure 4.12 Sheet resistance mapping of phosphorous diffused p-type wafer

According to the sheet resistance mapping, except the typical edge effect for tube furnace diffusion, main part of the wafer has great diffusion uniformity.

Another important result for diffusion other than horizontal mapping is doping profile. The diffused samples are sent for SRP (Spreading Resistance Profiling) measurement to confirm the doping profile. Fig. 4.13 shows the profiling results. The parameters are in good agreement with diffused doping profiles as reported in literatures [61].

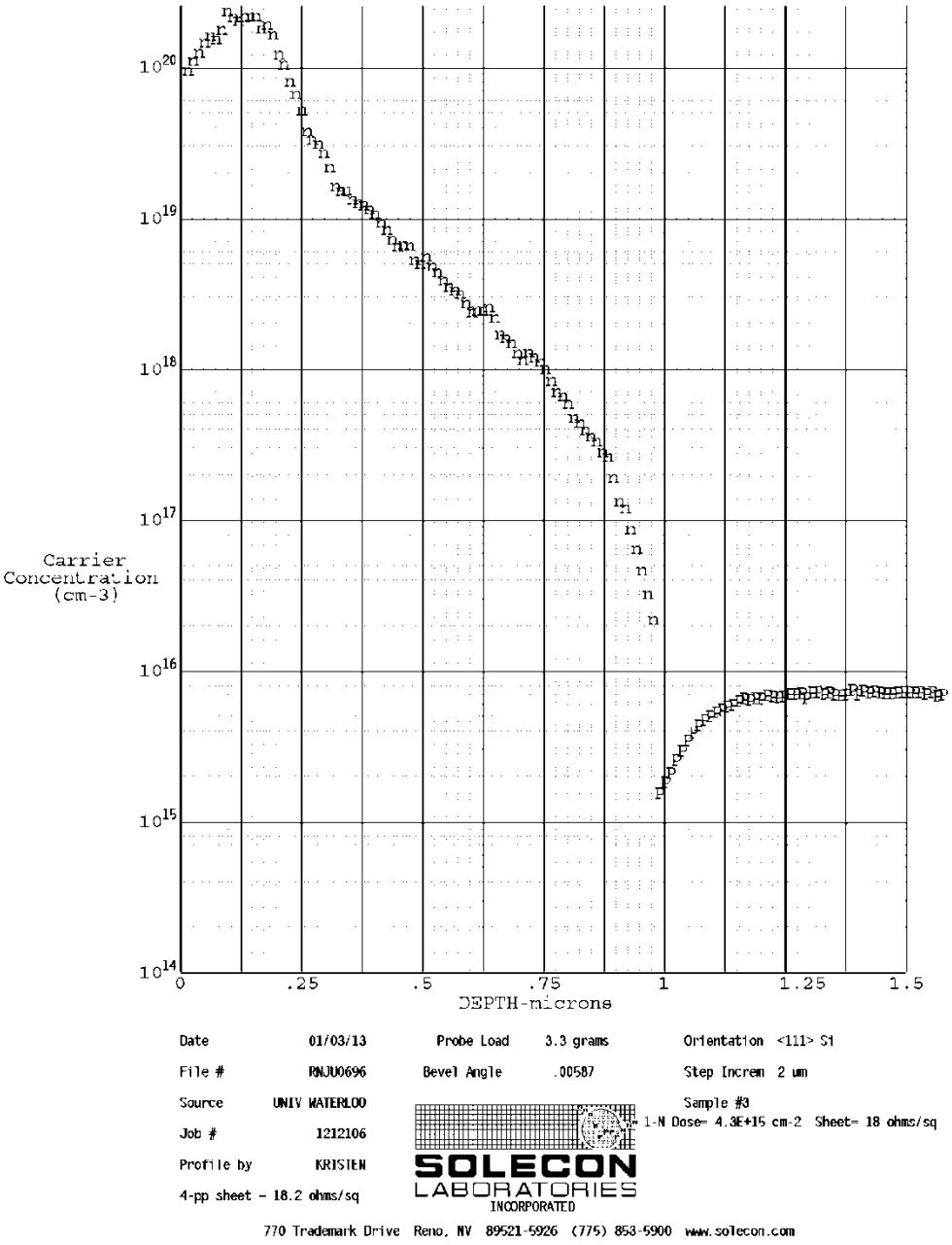


Figure 4.13 SRP result for phosphorous diffusion on p-type silicon wafer

Similarly, the SRP results for boron diffusion is shown in Fig. 4.14.

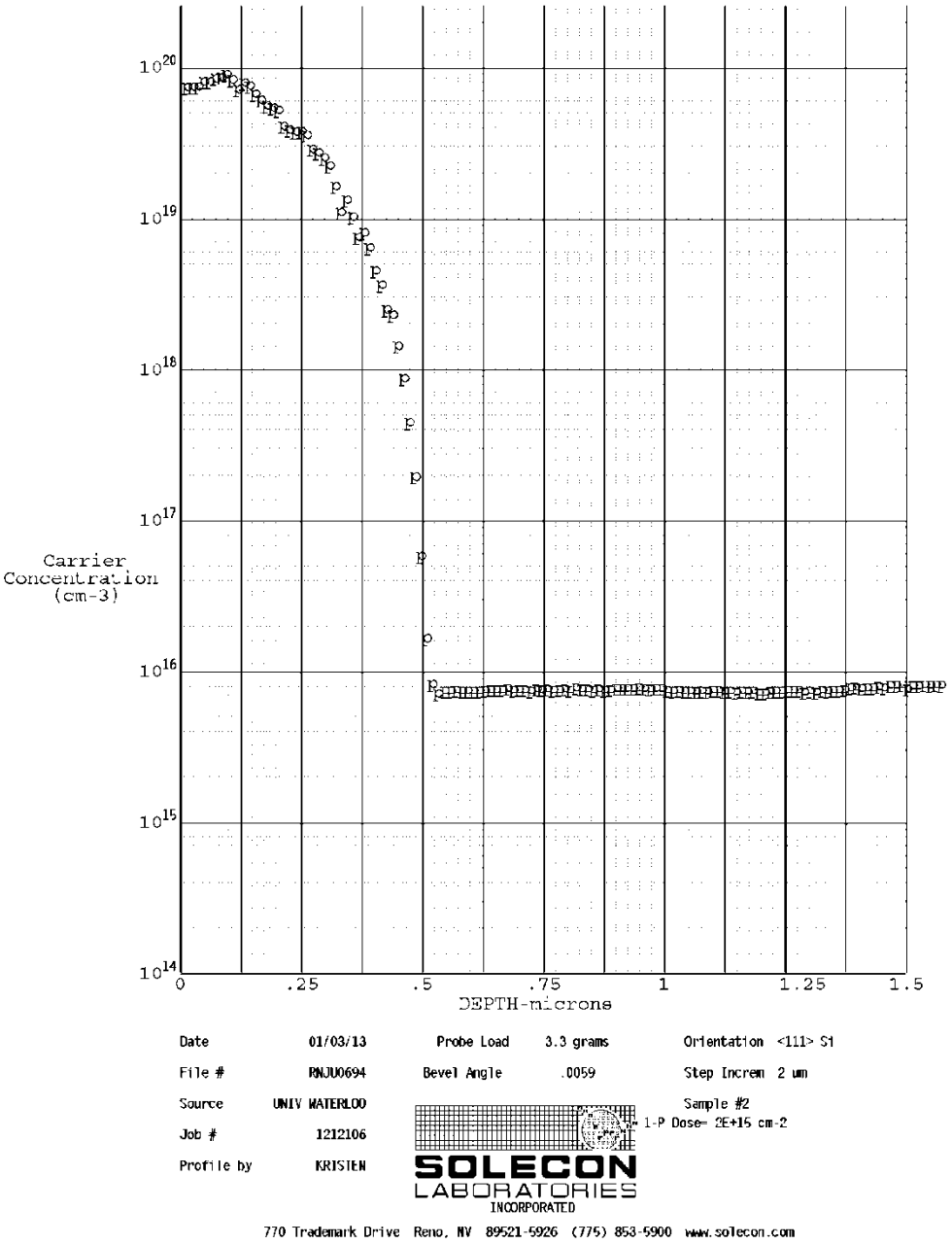


Figure 4.14 SRP result for boron diffused n-type silicon wafer

4.2.2 Etch Back

Etch back is basically an acid etching process to remove the very top layer after diffusion. As diffused samples have very high surface doping concentration (see Fig. 4.13), too many impurity atoms results in more recombination sites. Also, the extremely high concentration of majority carriers makes as generated minority carriers hard to survive until collection. This high recombination behavior is known as “dead layer”

effect. Furthermore, phosphorous doping process happens along with gettering effect. Hence, the very surface is the most defective layer. Solar cell performance will be pronouncedly improved by removing this layer through etch back process [62,63], experiment analysis is presented in the next section.

4.2.2.1 Etch Back Experiment Process

Etch back is usually completed by wet chemistry etching. Typically, the etching solution composes of HF, HNO_3 and Acetic Acid. Different composition results in different etching rate. The main etching mechanism is HNO_3 oxidize silicon surface and HF removes oxide to prepare the surface for further etching [64].

To make sure the etch back process is comparative with the specific diffused emitter as described in the previous section, two compositions for the etching solutions are developed. Since HF limited solution has better control of etching rate, 0.5% HF in 99.5% HNO_3 and 1% HF in 99% HNO_3 (by volume) have been selected and analyzed for etch back processes. The first recipe (0.5% HF) has better etching control, but the solution needs to be renewed more frequently. The second recipe is preferred and applied more commonly.

The etching happens in regular plastic beaker, but the holder is specially made single-sided etching tool, as shown in Fig. 4.15.

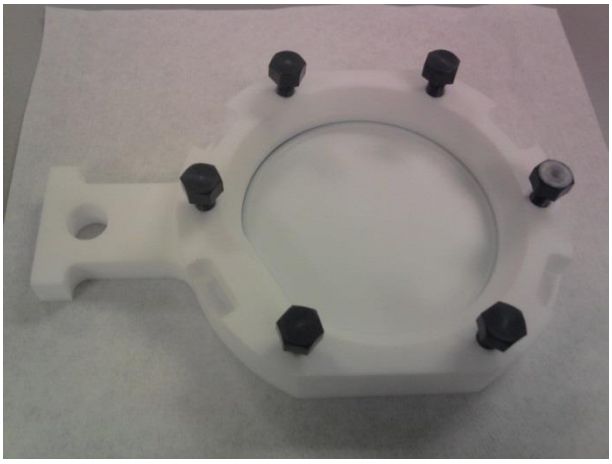


Figure 4.15 Picture of single-sided etching holder

After etching, 30 sec HF dip is performed to remove any oxide. And then, thorough cleaning is essential before next step not only to get rid of any solution residue but also prevent the formation of porous silicon [65].

5.2.2.2 Etch Back Results

Etch back process is typically targeting a specified sheet resistance or removed surface thickness. In order to make sure etching is done to the expected point, also to confirm the uniformity of etch back, sheet resistance is mapped by Semi-lab after different etching time. Mapping results are shown in Fig. 4.16. The solution used herein is with 0.5% HF.

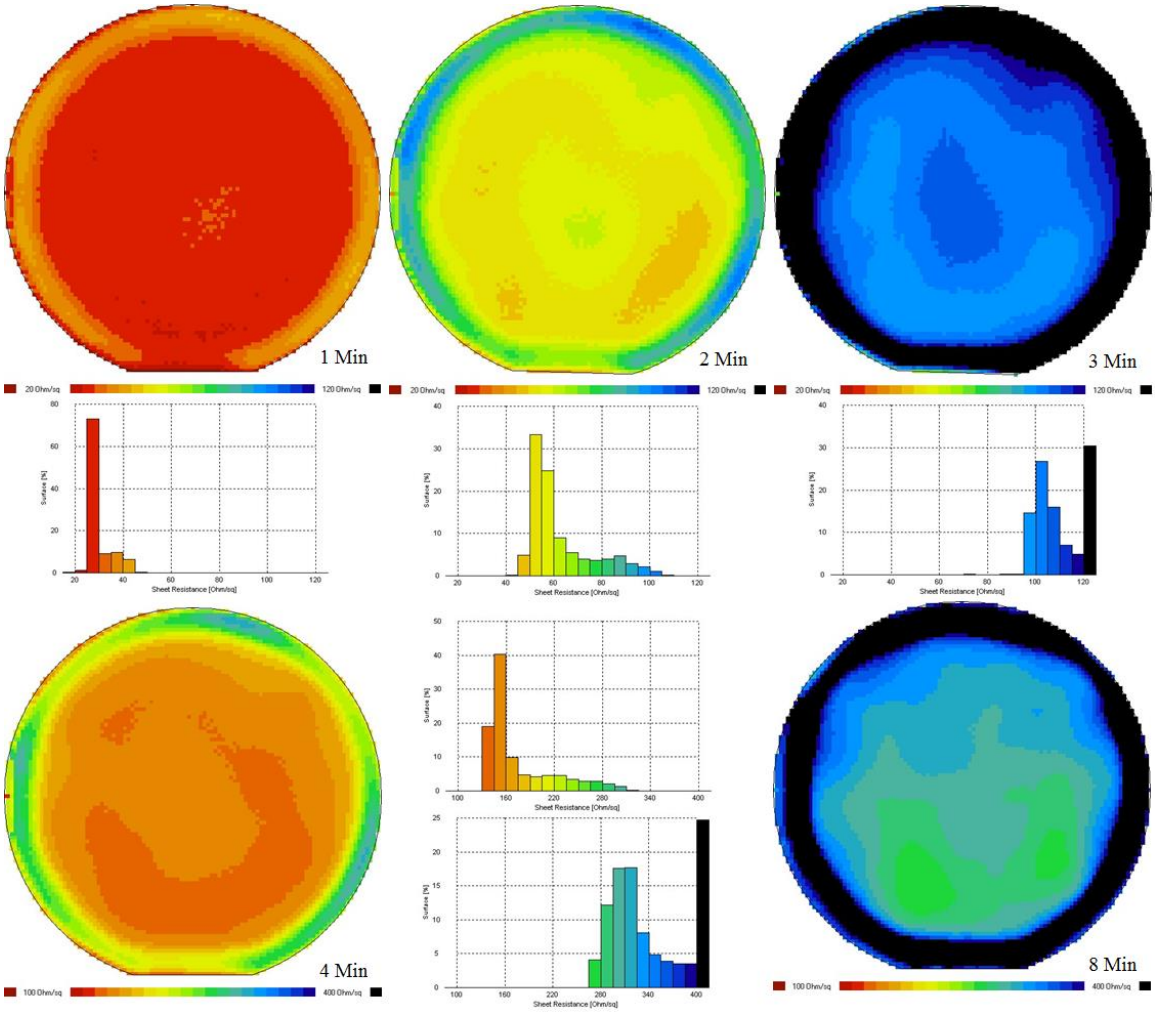


Figure 4.16 Sheet resistance mapping at different etching time

The same experiment was also performed for recipe with 1% HF. Etching is faster, and uniformity is also good. The most interested sheet resistance is around 90 Ω/□, so the

etching time is determined to be 40 s. About 250 nm silicon is removed from surface, and surface doping concentration is modified to 3×10^{19} (as shown in Fig. 4.17), the measured sheet resistance is 87 Ω/□. A sheet resistance of 85 to 120 is commonly preferred for both low "dead-layer" effect and satisfactory series resistance. In our device, current output is considerably high, therefore lower sheet resistance is preferred for mitigating more important fact of the two, which is series resistance.

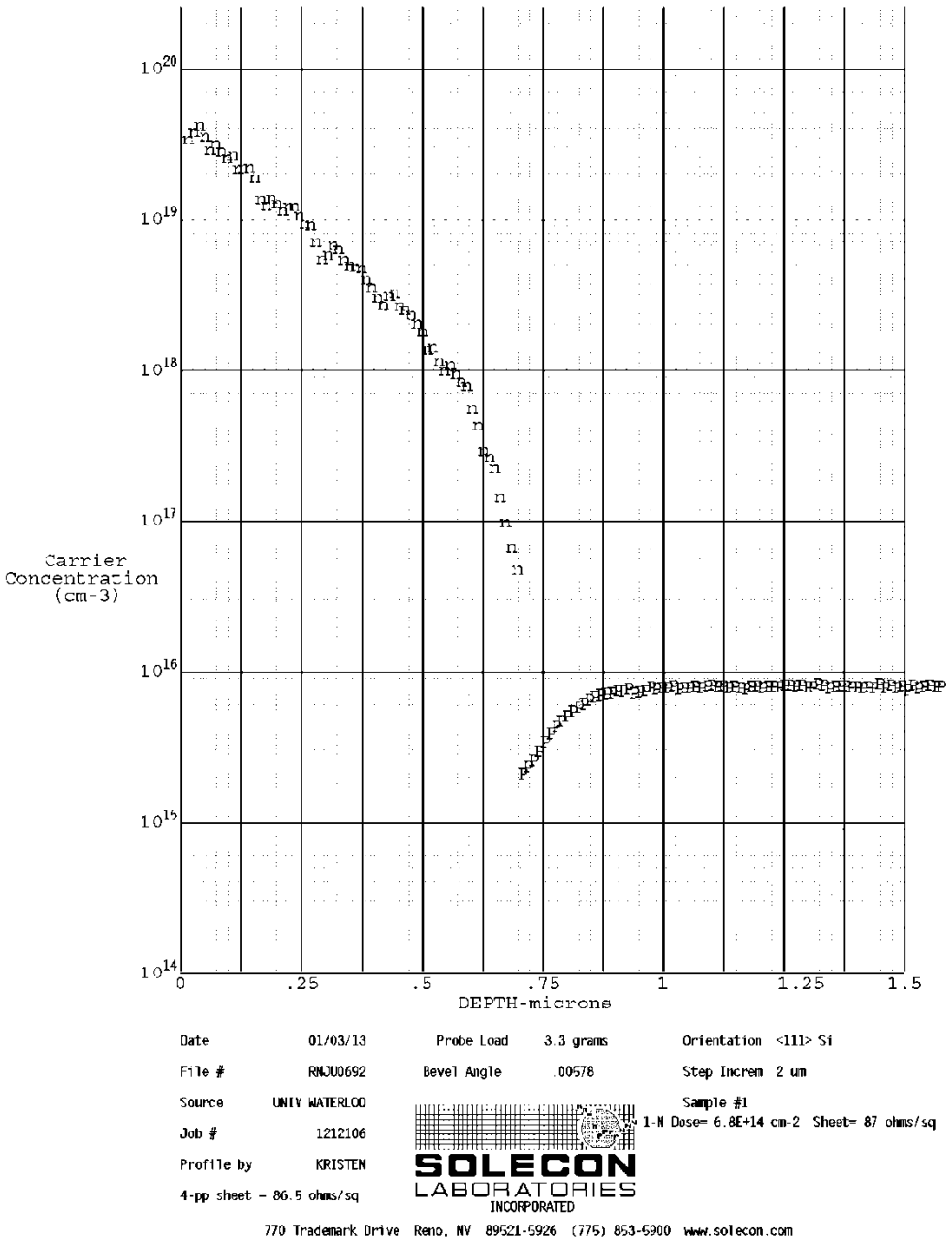


Figure 4.17 SRP result of etched back n-type emitter

This repeatable isotropic wet chemistry etch-back process is developed and applied as standard etch back process for diffused junction solar cell fabrication in CAPDS.

4.3 Surface Passivation

4.3.1 SiN_x Passivation

Lifetime measurement is a straight forward way to find out the surface passivation effect, if the wafer itself has decent bulk lifetime [66,67]. Fig. 4.18 shows the lifetime mapping of the wafer before passivation, after HF passivation and after SiN_x passivation.

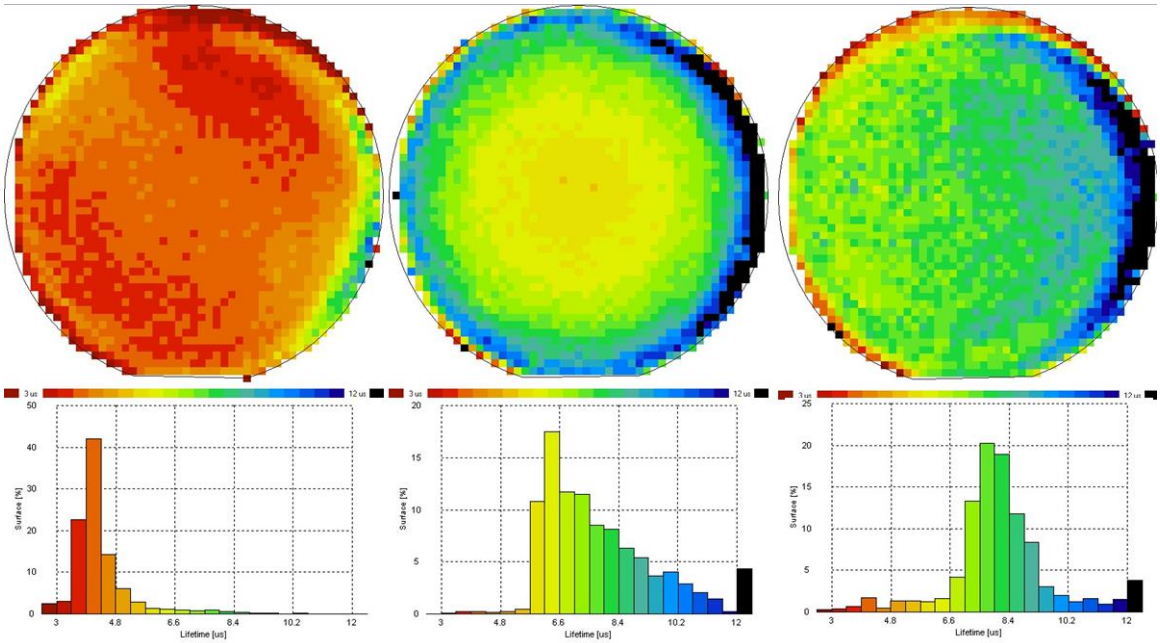


Figure 4.18 Lifetime mapping of bare wafer, HF passivated wafer and SiNx passivated wafer

From the lifetime mapping, it is obvious that before passivation the wafer lifetime is quite low at about 4 µs. After HF passivation, lifetime has increased to about 6 µs. After SiN_x passivation, lifetime is further improved to about 8 µs. The wafers we are getting from the supplier seem to have a lower lifetime than expected, but even with these thick and low lifetime wafers we can still see the passivation effect from lifetime measurement. Moreover, as mentioned above, the current recipe of SiN_x is actually focusing on optical property and is nitride rich film. Therefore, after fine tuning with

the gas ratios for SiN_x deposition, the passivation effect will achieve a higher level. Anyway, the effect of surface passivation will be more obvious in IQE comparison, which is presented below.

IQE is calculated from EQE and reflection results. It is the percentage of collected carriers against the number of photons that come in the photovoltaic device. That is to say, this characterization method eliminates the effect of reflection, and only monitors the photovoltaic efficiency inside solar cells. The calculation equation is shown below:

$$IQE_\lambda = \frac{EQE_\lambda}{1 - R_\lambda}$$

where IQE_λ, EQE_λ are the IQE and EQE result in certain wavelength, and R_λ is the reflection on that same wavelength. Fig. 4.19 shows the IQE results calculated from the EQE and reflection results in Fig. 4.9.

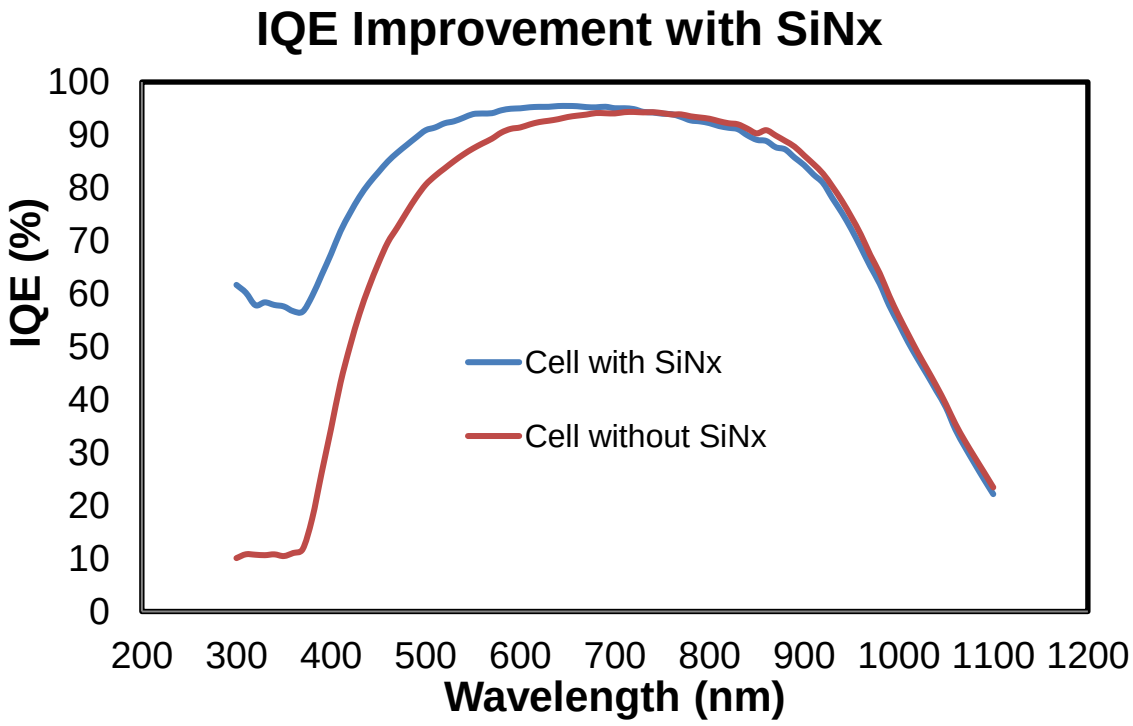


Figure 4.19 IQE improvement with SiN_x film

The diagram clearly shows that the cell with SiN_x film has better IQE below the wavelength of 700 nm. The better short wavelength response clearly indicates a better front surface passivation with SiN_x film. Moreover, the consistency of IQE in the wavelength larger than 700 nm illustrates the two cells have very similar back surface

condition and bulk minority carrier lifetime. This further enhanced the conclusion from the comparison in short wavelength range.

4.3.2 Back Surface Field Passivation

The minority carrier lifetime is directly related to the carrier concentration. Therefore, increasing the majority carrier concentration can reduce minority carrier concentration and hence improve minority carrier lifetime. That means, high-low junction is another way of surface passivation. Heavily doped layer (p+ on p substrate) could repel minority carrier and minimize the minority carrier concentration at highly defective surface. Therefore, minimize the recombination at the surface. Heavily doped layer is realized by boron diffusion, as introduced above. This type of passivation is usually used at back side, so it is called back surface field (BSF, hereafter) passivation. BSF is mainly helpful for long wavelength absorption, which happens close to rear surface. Fig. 4.20 shows the EQE and IQE improvement by applying BSF. The improvement at

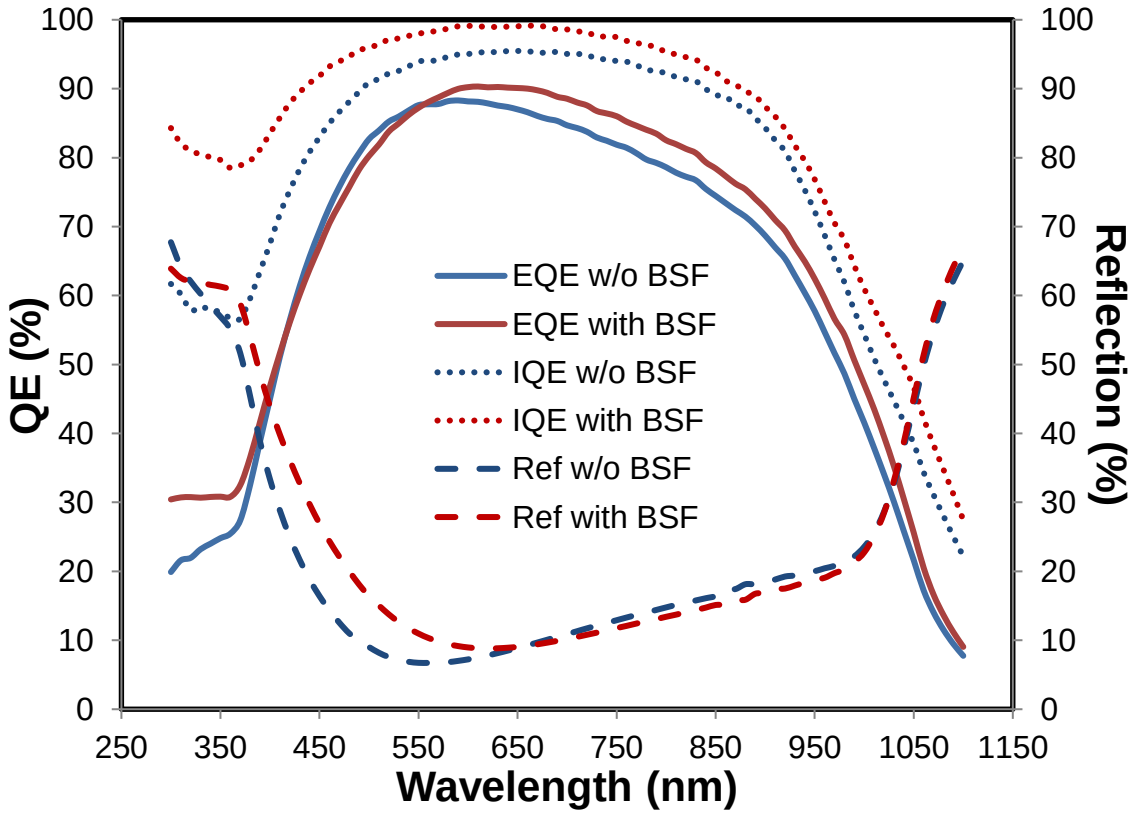


Figure 4.20 EQE and IQE results of cells with and without BSF

low wavelength region is due to optimization of etch back and ARC. The improvement with BSF is not as significate as observed in the software simulation. First, the substrate thickness (500 μm) is much thicker than the simulated device (200 μm). Second, the MCL of the substrate in the technology development is even lower than that of the lowest value in the simulation process.

4.4 Metallization

Typically, metal contacts for laboratory cells are finished by two steps: deposition and patterning. Deposition is basically done by all kinds of PVD (Physical Vapor Deposition) processes. In CAPDS, e-beam and sputtering tools are available for such process. To remove unwanted metal for patterning, two choices are metal etching and lift-off. In this section, the metal deposition is briefly introduced. Metal patterning process such as PAN (Phosphoric-Acetic-Nitric) solution etching, photolithography patterning and lift-off processes are omitted.

E-beam deposition is a well-known method. It has relatively high deposition rate, and capable for deposition of different kinds of metal, Ag, Al, Ti, etc. Although Ag has lower resistivity, it has higher atom number and kills much more sensors than Al. Also, Ag is less adhesive to silicon surface. So in the test stage, Al is preferred. Ti is used as adhesion layer and also diffusion barrier on the front side.

Front contact composes of two stacks, Ti and Ag with thickness of 50 nm and 1 μm respectively. In order to achieve steady deposition, the deposition power is carefully controlled especially at the beginning to heat up the whole target at the same time. First few nanometers of deposition affects the whole layer much more significantly. Hence, it is deposited much slower than the body part. The deposition rate is gradually increased from 0.1Å/s to 0.5Å/s during the first 10 nm deposition. The body deposition rate is around 5-10 Å/s. Back contact is made of 1 μm Al fully deposited over back surface. Deposition conditions are similar with from contact.

4.5 Standard Si Homo-Junction Solar Cell Fabrication

Standard Si homo-junction solar cells are fabricated on p-type Si substrate. These devices have only the most basic components of textured substrate, ARC, diffused emitter, diffused back surface field and metal contacts. Detailed fabrication process flow is presented in Fig. 4.21.

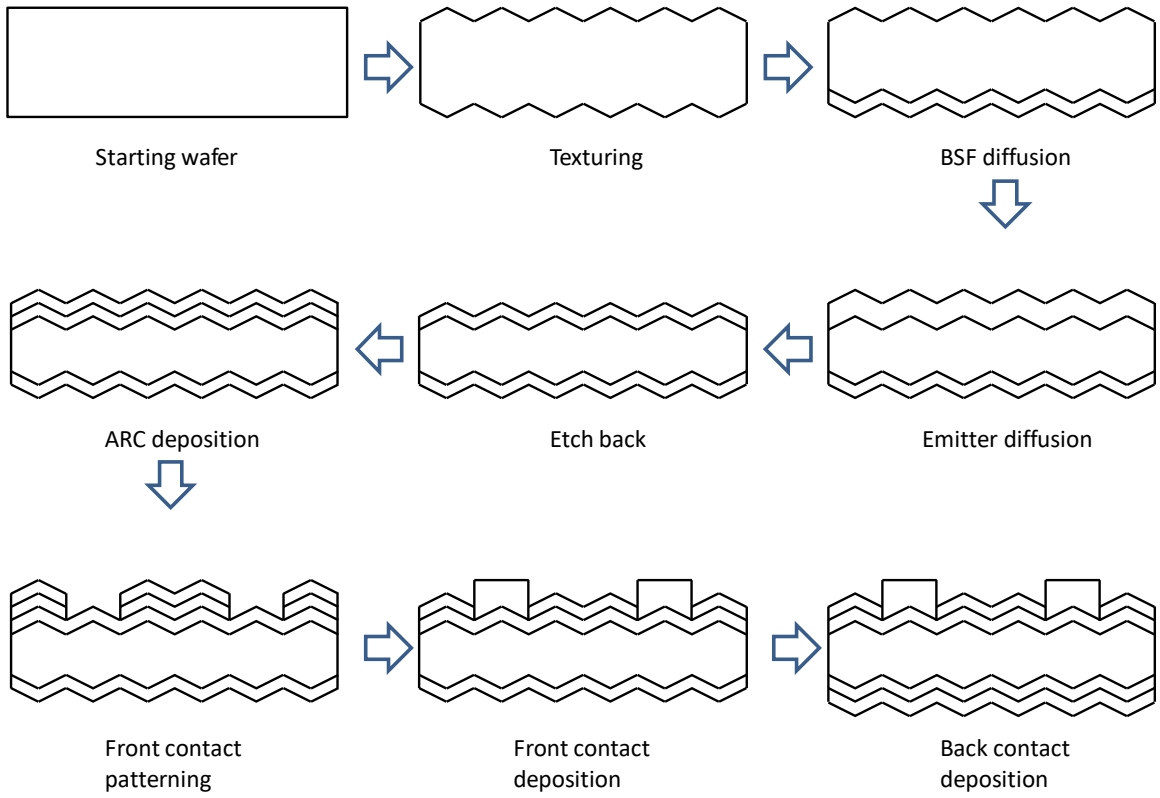


Figure 4.21 Schematic diagram of fabrication process flow for standard Si homo-junction solar cells

Typical energy conversion efficiency of 16.2% with average short circuit current above 39 mA/cm^2 is achieved. Dark I-V, Quantum Efficiency and Illuminated I-V characterization are performed. Results of different samples are rather similar. Therefore, the results and discussion on one example device is listed below for a clear presentation. **Additional hydrogen annealing process has boosted the efficiency up to 17.43% with short circuit current of 39.6 mA/cm^2.** The hydrogen annealing process and results will be discussed in more details in Chapter 6.

4.5.1 Dark I-V Analysis

Fig. 4.22 shows the dark I-V characteristics of the standard Si homojunction solar cells. In dark I-V analysis, the solar cells exhibit typical diode behavior. Rectification ratio is approximately 1.0×10^{3} at ±0.7 V. Reverse saturation current, I_o, is 1.0×10^{-6} A/cm^2. Using two-diode model, the ideality factors n_1 and n_2 of the standard solar cell are 1.98 and 3.89, respectively. The ideality factors are relatively high. From large number of repeated experiments, the high ideality factors are mainly due to quality of the wafer substrate. That means, with high quality wafers, the same fabrication process should generate even higher device performance.

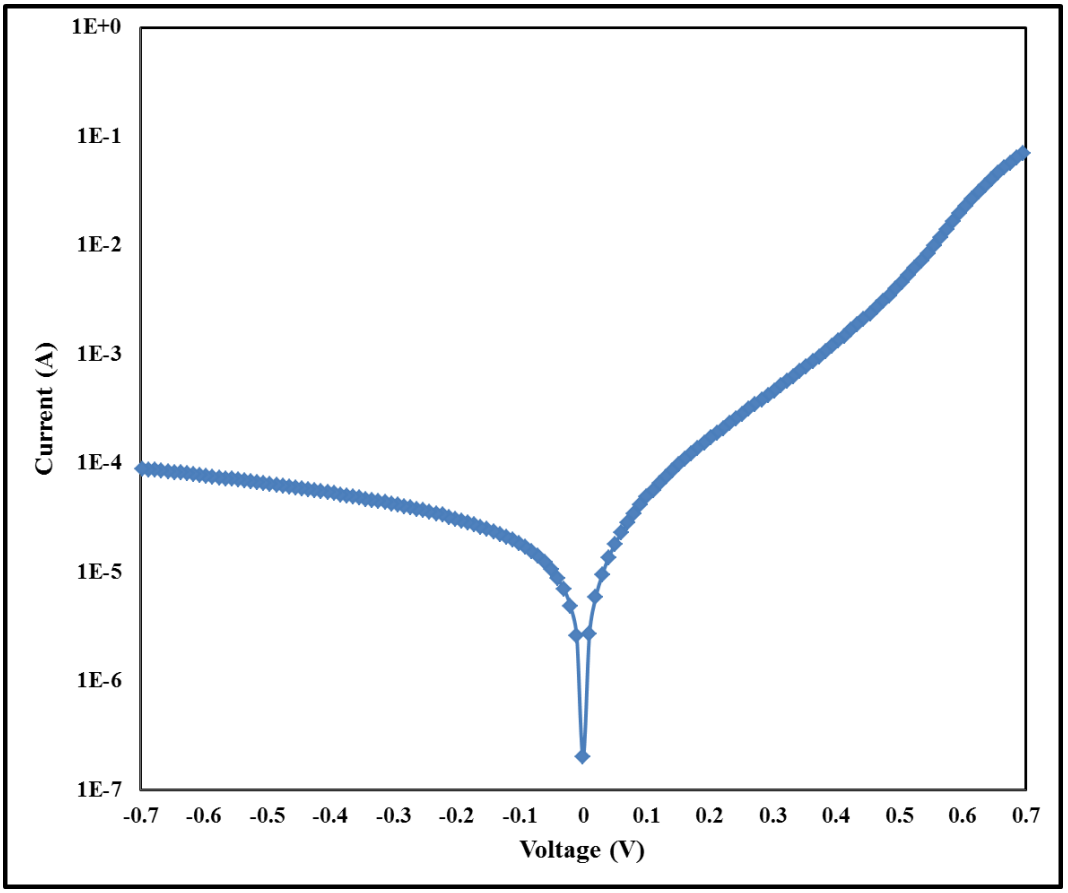


Figure 4.22 Dark I-V plot for standard Si homo-junction solar cell

4.5.2 Quantum Efficiency Analysis

Quantum efficiency is one of the most important properties for solar cells. EQE measurement is performed from 300 nm to 1100 nm, and the results are presented in Fig. 4.23. Reflection and IQE results are also plotted in the figure for device performance presentation.

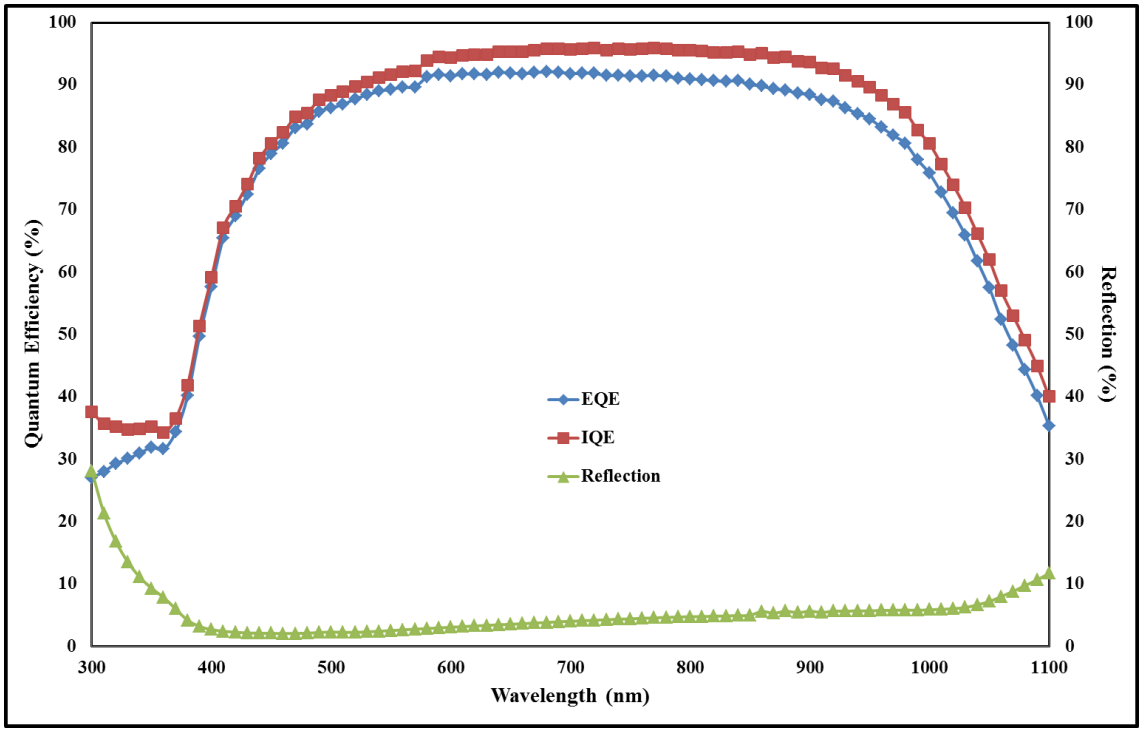


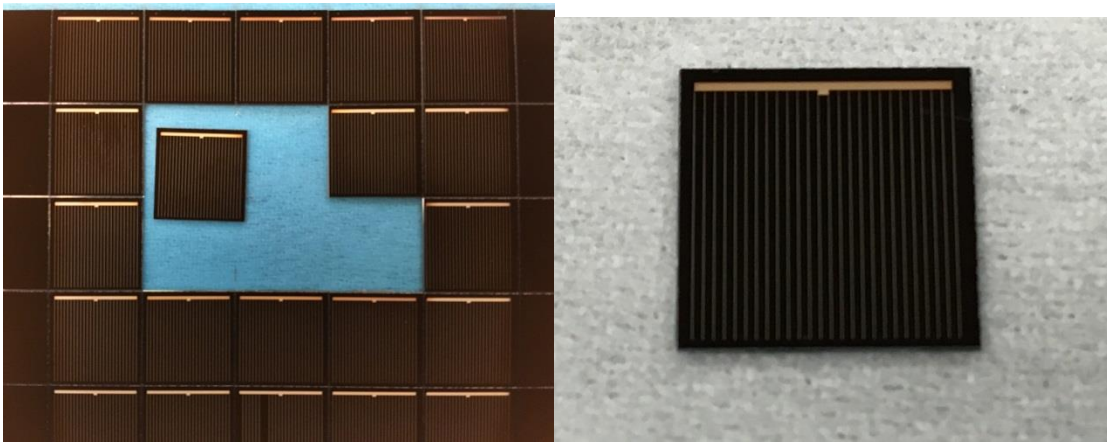
Figure 4.23 QE and reflection plots for standard Si homo-junction solar cell

4.5.3 Illuminated I-V Analysis

Illuminated I-V analysis is performed under 100mW/cm2 (AM1.5 standard spectrum) for standard Si homo-junction solar cells. The performance report is presented in Fig. 4.24.

Excellent short circuit current density is achieved at 39.2 mA/cm^2. It indicates that the light confinement approaches are very effective and the diffused junction is robust. Open circuit voltage is relatively low at 591 mV, which is the main constraint for the overall device performance. This low Voc is again believed to origin from the quality of the starting wafers as observed from the high ideality factors. The main purpose for

these experiments is to develop and analyze the processing technologies and also understand and compare the impact of each processes. Therefore, no high quality wafers like FZ wafers were applied. Moreover, as received 4-inch wafers are mostly suffering from low minority carrier lifetime. Almost all of the wafers have measured MCL of below 30 µs, some are even below 5 µs. Fill factor, 70%, is also a bit low,



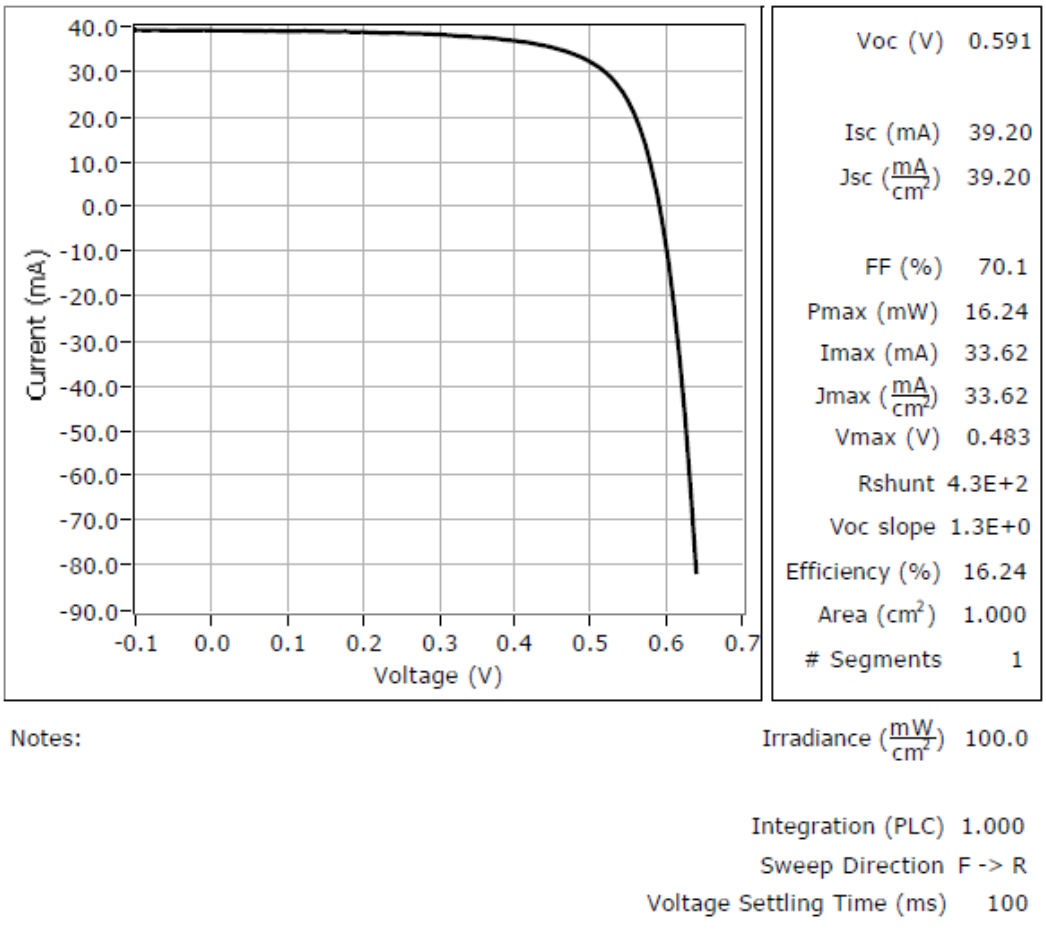


Figure 4.24 Photo of solar cell samples (top) and illuminated I-V result report for standard Si homo-junction solar cell (bot)

comparing to high efficiency solar cells. Because the metal fingers are relatively thin due to evaporation limitations, the high output current emphasizes this problem. For a standard technology baseline development, 16.2% energy conversion efficiency is a satisfactory achievement.

4.6 Conclusions

The technologies for standard Si homo-junction solar cell fabrication is developed and analyzed. Random pyramid texturing and SiNx ARC are developed to reduce surface reflection from around 30% to below 10% for most of visible spectrum. Junction of the solar cell is achieved by high temperature diffusion followed by etch-back process. Surface passivation methods of front surface SiNx and BSF are developed and analyzed. Standard homo-junction Si solar cell fabrication technology is established with the device energy conversion efficiency of more than 16%.

The capability of fabricating Si based solar cell independently is essential to start the research on novel solar cell and photodetector structures. It is the foundation to understand and explore novel solar cell and photodetector architectures and link the simulation results to the real devices. Moreover, the knowledge of optical and electrical optimization approaches presented herein are of great value for the fabrication and optimization of advanced devices, such as the high performance Al-ZnO/Si heterojunction photodetectors, which will be introduced in Chapter 8.

CHAPTER 5

DEVELOPMENT OF ADVANCED POLY-SI/C-SI HETEROJUNCTION SOLAR CELLS

5.1 LPCVD N+ Poly-Si Thin Film

In this research, the deposition occurs in a quartz tube furnace with a quartz boat for sample transport. Three thermal couples are located at front, middle and rear part of the tube to monitor and control the deposition conditions. SiH_4 is applied as main reactive gas and PH_3 is applied as dopant gas for in-situ n+ poly-Si thin film deposition. The PH_3 gas is diluted with H_2 to 2% concentration. The deposited thin films had obvious lower sheet resistance (Four Point Probe measurement) and higher crystallinity (Raman Spectrum measurement) with higher deposition temperature up to 650 °C for our system, which is in agreement with literatures [14,68]. Therefore, the deposition temperature is selected to be 650 °C for the analysis below.

5.1.1 Raman Spectrum

One of the most important properties for poly-Si thin film is the crystallinity. Raman spectrum can clearly present the crystallinity of a thin film. To eliminate Si substrate interference, poly-Si thin films are deposited on quartz wafers for Raman spectrum measurement. The shapes of Raman response for different deposition conditions (except for temperature) are rather similar. A strong peak is observed at around 520 nm, no broad blue shoulder presents at the spectrum like in a-Si:H [68]. That means the film

is fully crystallized. However, the peak positions of some samples are slightly different, which indicates different strain levels in the films. Fig. 5.1 shows the Raman spectrum measurement results of thin films deposited with three different gas flow rate (same gas ratio) together with a lightly doped c-Si wafer reference for comparison. The poly-Si thin film deposited with higher flow rate exhibits higher stress. The similar peak width from the three films indicates similar crystallinity.

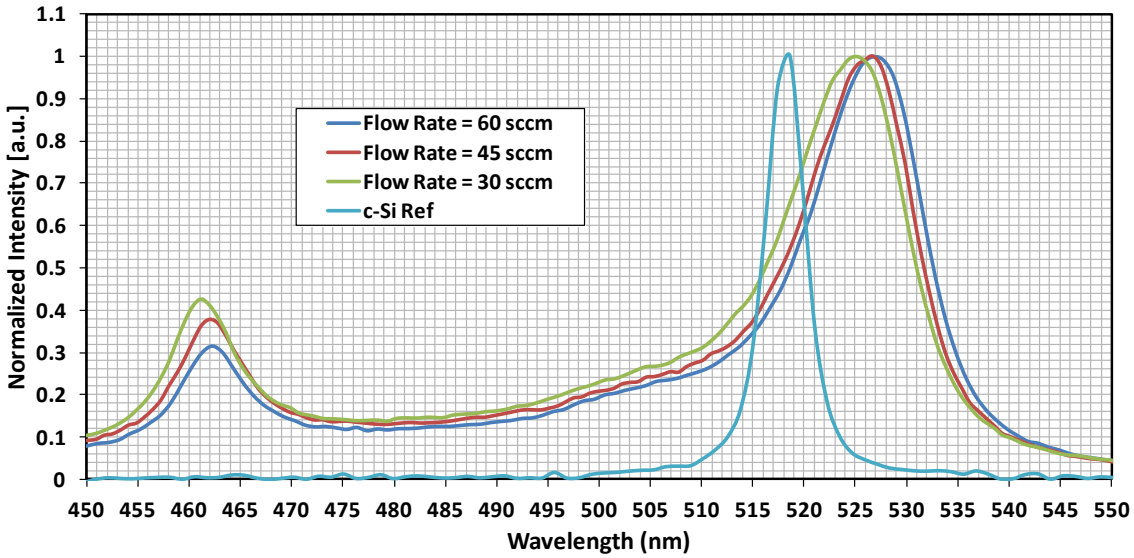


Figure 5.1 Raman spectrum of deposited poly-Si thin films and c-Si reference

5.1.2 Deposition Parameter Optimization

As demonstrated above, the Raman spectrums are rather similar for different thin films. Therefore, other characterization methods are required to monitor and optimize the deposition parameters. One of the best candidates is sheet resistance measurement. Sheet resistance provides direct indication for the film conductivity, therefore implies film quality and FF of finished device.

Gas flow rate, deposition pressure and gas flow ratio are three main parameters for LPCVD poly-Si thin film deposition. Sheet resistance result comparison for the three deposition conditions are presented below.

Fig. 5.2 shows the sheet resistance of poly-Si thin film deposited with different gas flow rate. The film quality dependency can vary from system to system. For the setup applied

in this research, at tested flow rate values, lower flow rate exhibits lower film sheet resistance, although the variation seems to be higher at lower flow rate.

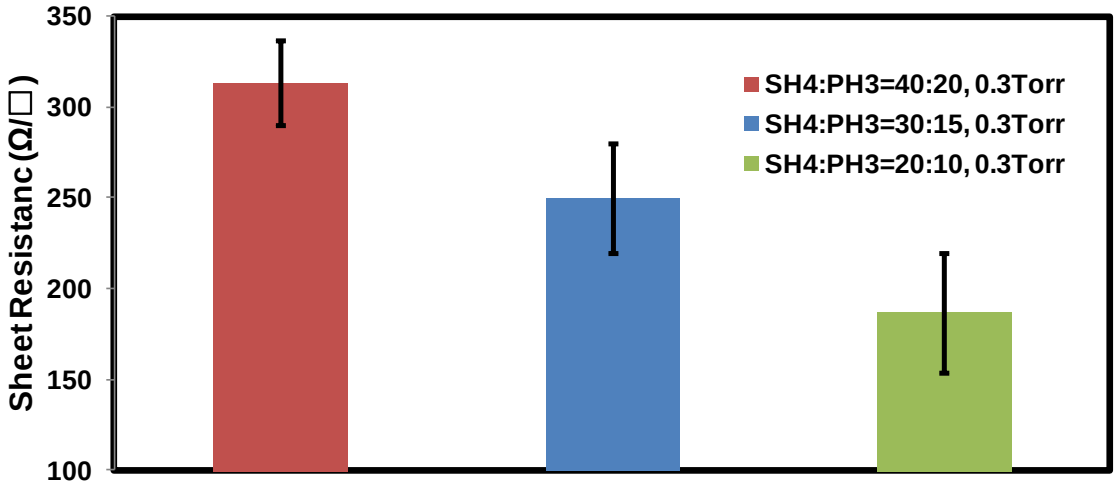


Figure 5.2 Sheet resistance comparison for different gas flow rate

Fig. 5.3 summarizes the sheet resistance results for the poly-Si thin films deposited with different gas flow rate and different pressure. Obviously, films deposited at lower pressure have superior performance: lower film sheet resistance and smaller variation are observed. Notably, the influence of gas flow rate on the finished film sheet resistance almost disappeared at lower deposition pressure. That means, at 0.2 Torr, the deposition entered "surface reaction" regime, which is preferred for LPCVD thin film deposition.

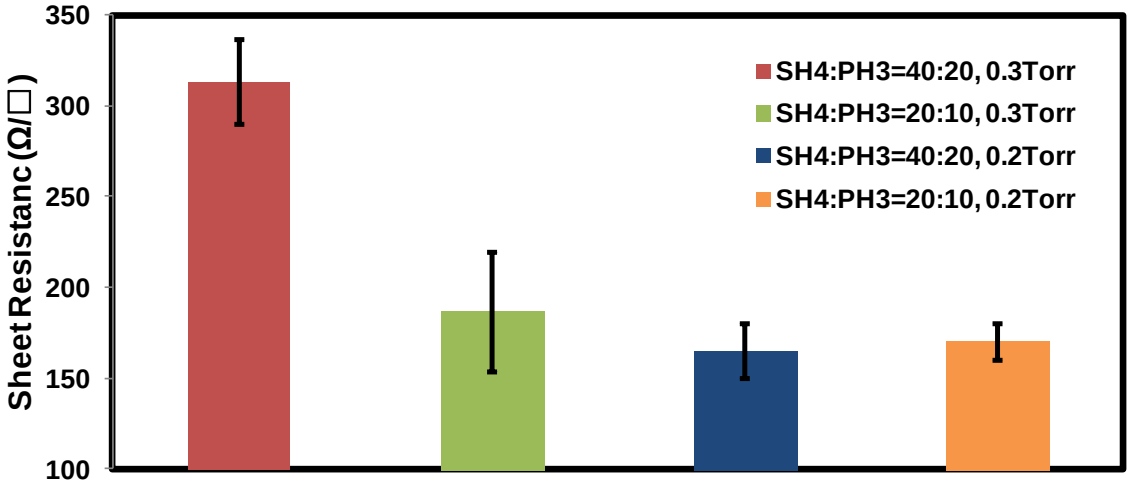


Figure 5.3 Sheet resistance comparison for different pressure

Fig. 5.4 demonstrates the gas ratio impact on LPCVD poly-Si thin film sheet resistance. A notable sheet resistance improvement is observed for SiH_4:PH_3 ratio of 1:1 comparing to that of 2:1.

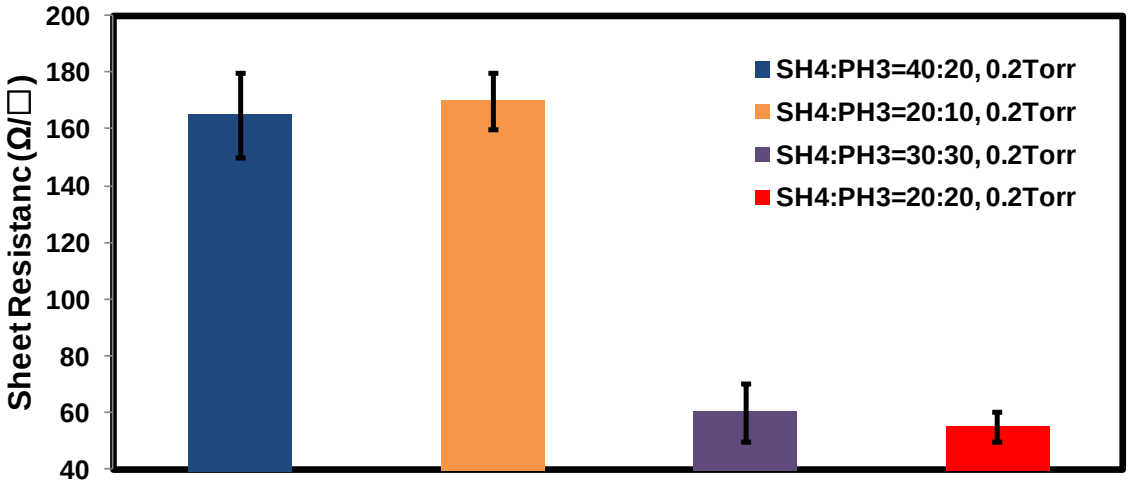


Figure 5.4 Sheet resistance comparison for different gas ratio

Since the poly-Si thin film with the best sheet resistance performance is found at deposition conditions of 650 °C, 0.2 Torr, SiH_4:PH_3 = 1:1, the poly-Si emitter solar cells are fabricated with the same type of poly-Si thin films.

5.2 LPCVD Poly-Si Emitter Solar Cell

With the LPCVD poly-Si thin film developed above, poly-Si emitter solar cells are fabricated and analyzed. The simplest cell structure, as shown in Fig. 5.5, is applied to demonstrate the baseline performance for the poly-Si/c-Si heterojunction structure.

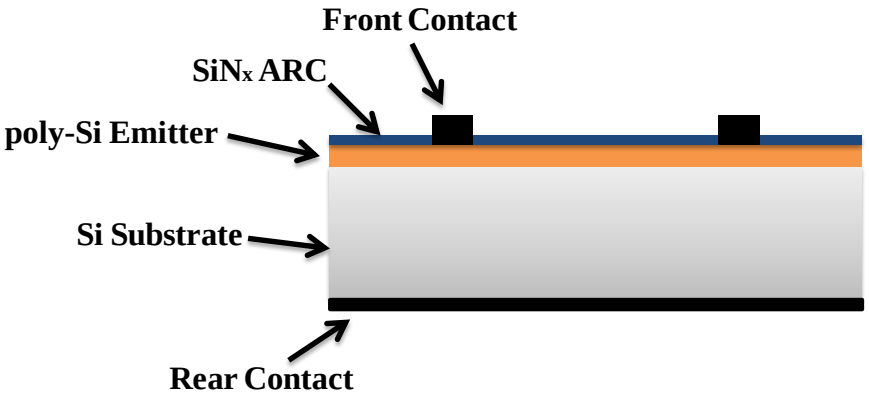


Figure 5.5 Schematic structure of standard poly-Si/c-Si heterojunction solar cell

In the recent years, multi-crystalline Si (multi-Si) weights more and more in the PV industry. Therefore, in parallel of poly-Si/c-Si heterojunction solar cell fabrication, poly-Si/multi-Si solar cells are fabricated with the same structure and processes. The dark IV characteristics for standard poly-Si/c-Si and poly-Si/multi-Si heterojunction solar cells are presented in Fig. 5.6.

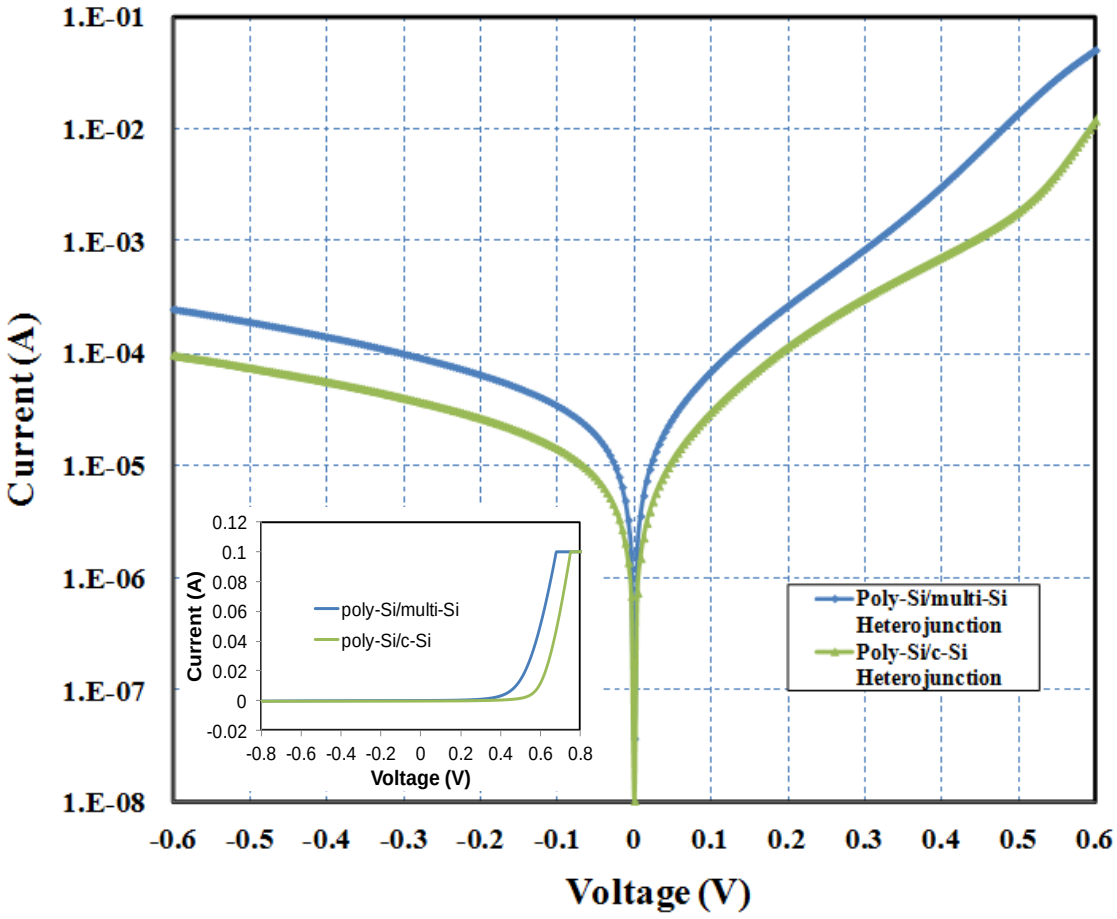


Figure 5.6 Dark IV characteristics of standard poly-Si/c-Si and poly-Si/multi-Si heterojunction solar cell (inset: linear scale characteristics)

As expected, poly-Si/c-Si heterojunction exhibits lower reverse saturation current than poly-Si/multi-Si heterojunction. Additionally, the multi-Si heterojunction shows lower turn-on voltage due to more defective junction interface. It can be observed more clearly in EQE results comparison, as shown in Fig. 5.7.

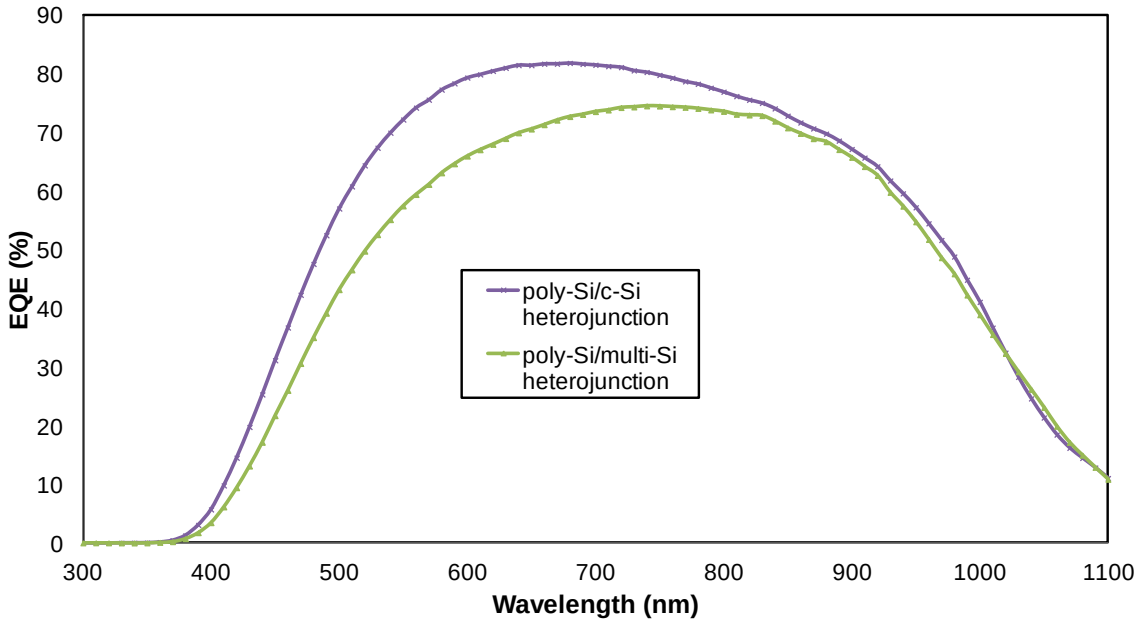


Figure 5.7 EQE results of standard poly-Si/c-Si and poly-Si/multi-Si heterojunction solar cells

Standard poly-Si/c-Si heterojunction shows reasonable quantum efficiency at green wavelength region. Relatively low blue response is observed as expected, since no junction refinement efforts have been addressed. There are several methods that may improve the blue response for poly-Si/c-Si heterojunction. The introduction of interfacial passivation layer, such as Nitric Acid Oxide (NAO) will be discussed in section 5.3; Rapid Thermal Annealing (RTA) process will be discussed in section 5.4; Low Pressure Hydrogenation (LPH) process will be discussed in Chapter 6.

Poly-Si/multi-Si heterojunction device shows lower blue and green response than poly-Si/c-Si heterojunction. That means, the destructive substrate makes the heterojunction less robust than poly-Si/c-Si heterojunction. However, relatively similar quantum efficiency at long wavelength region (above 800 nm) shows that the multi-Si substrate has less impact on photons absorbed further from the heterojunction interface. Therefore, interface treatment may benefit more for poly-Si/multi-Si than poly-Si/c-Si heterojunction devices.

The I-V characteristics of standard poly-Si/c-Si heterojunction solar cell under 100 mW/cm^2 illumination (AM1.5 standard spectrum distribution) is presented in Fig. 5.8.

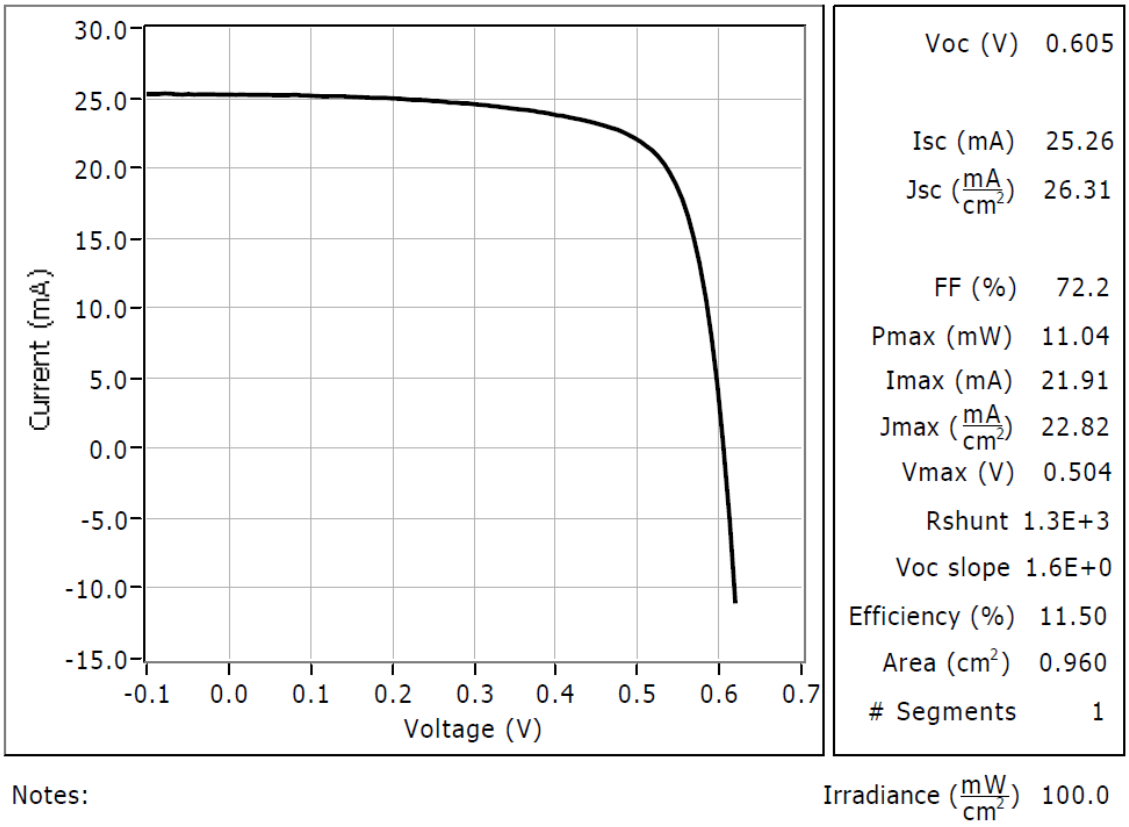


Figure 5.8 Illuminated IV characteristics of standard poly-Si/c-Si heterojunction solar cell

As shown in the solar simulator analysis report, the energy conversion efficiency for poly-Si/c-Si heterojunction solar cell is 11.5%. Slightly higher than expected V_{oc}, 605 mV is achieved for relatively low quality substrate. Theoretically, V_{oc} can be improved by better passivation and refined junction properties. However, these improvements may not always be observed at device level due to substrate property limitations, such as MCL of the substrate. Reasonable J_{sc} of 26.31 mA/cm^2 for non-textured substrate is achieved. Except for light confinement methods, improving blue response can also elevate J_{sc}. Satisfactory FF of 72.2% for poly-Si emitter solar cells has already accomplished. There is still space for improvement of FF to an excellent level of ~80% and therefore better energy conversion efficiency.

5.3 LPCVD Poly-Si Emitter Solar Cell with Interface Passivation Layer

As discussed above, poly-Si/c-Si heterojunction has a relatively defective junction interface. Defects inside the junction, which is also very close to front surface, result in low blue response. One of the most effective methods is to introduce interface passivation layer. Thermal oxide, chemically grown oxide, PECVD a-Si:H and PECVD SiN_x are all candidates for the passivation layer [69,70]. In this research, chemically grown Nitric Acid Oxide (NAO) layer is applied. The main advantages for NAO are listed as follows:

- Simple process, ready for industrial transfer;
- Self-limiting process, less sensitive to process parameters;
- Oxidation saturate at preferred thickness for tunnelling;
- No thermal budget;
- Stable;
- Repeatable;
- Satisfactory passivation performance.

The basic process is after standard RCA cleaning, and prior to loading sample to LPCVD for poly-Si thin film deposition, Si substrate is immersed in 68% nitric acid for 15 min to grow a nitric acid oxide (NAO) layer [71]. Schematic cell structure is presented in Fig. 5.9.

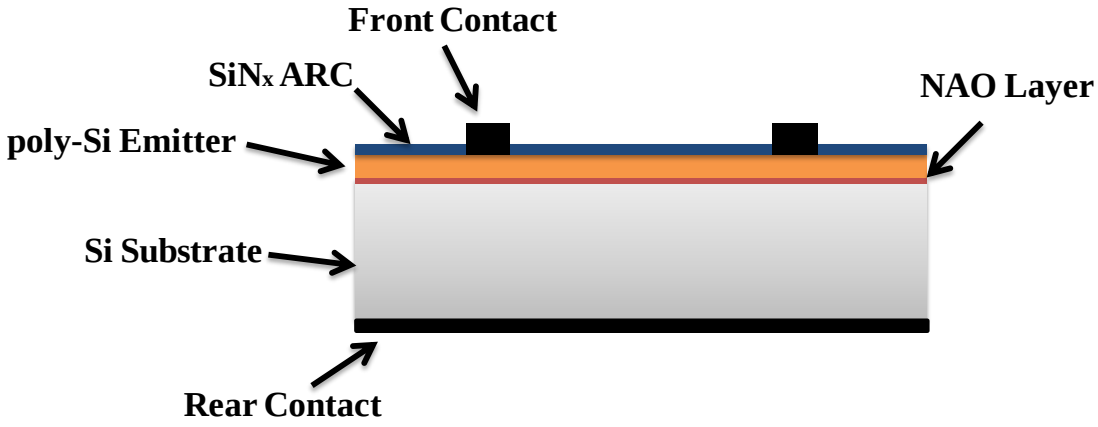


Figure 5.9 Schematic structure of poly-Si/c-Si heterojunction solar cell with interface NAO layer

One important function of interfacial passivation layer is to improve the junction properties and lower the leakage current. Typically, the main problem associated with the introduction of interfacial layer is huge increase in forward bias resistance [72].

Dark IV characteristics are performed on poly-Si/c-Si heterojunction solar cell with NAO passivation layer, as shown in Fig. 5.10. In comparison with standard poly-Si/c-Si heterojunction solar cell, device with NAO layer shows obvious lower reverse saturation current. Lower leakage current should contribute to a better shunt resistance and therefore better device performance. The benefit is more visible from illuminated IV characterization as will be discussed below. Notably, the series resistance at forward bias condition is almost not changed. That means, the introduction of the NAO layer does not compromise carrier flow at forward bias condition. Based on the ultra-thin thickness of NAO layer, tunneling is believed to be the main carrier transport mechanism. And the NAO layer herein is thin enough to maintain the satisfactory series resistance.

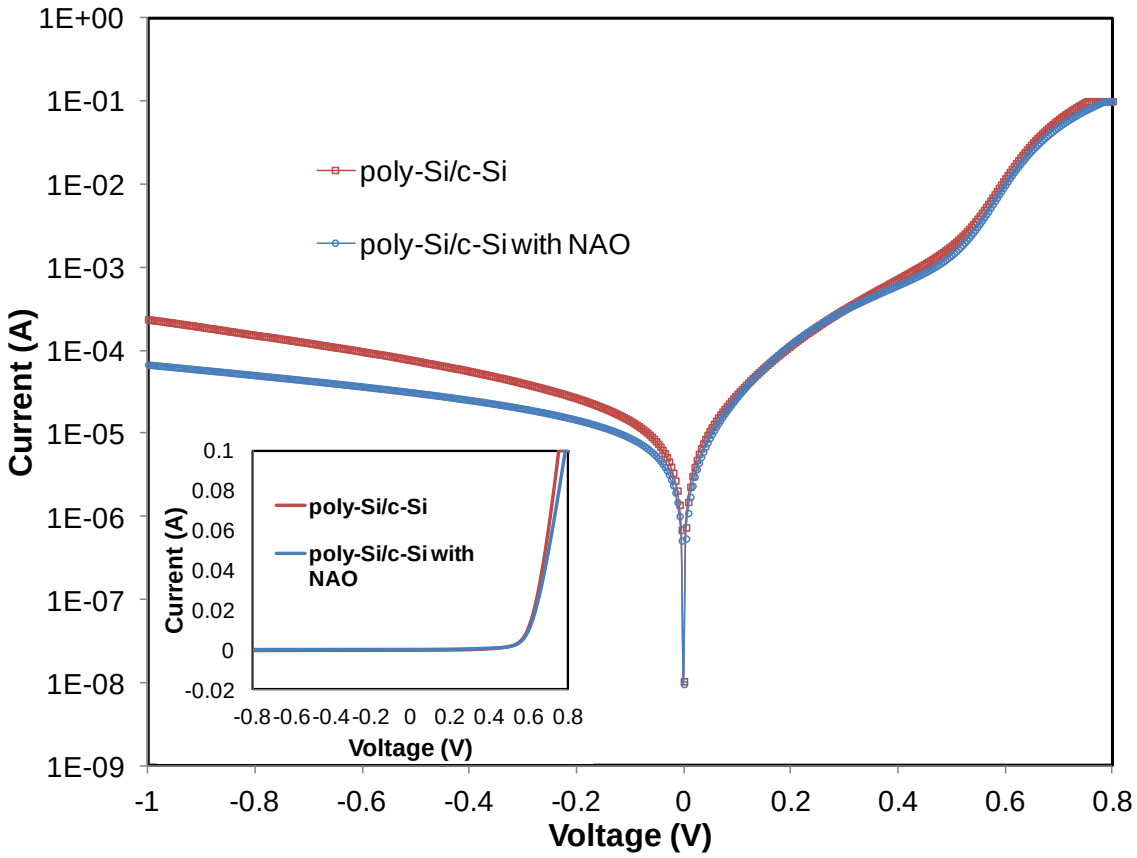


Figure 5.10 Dark IV characteristics comparison between poly-Si/c-Si heterojunction solar cells with and without interface NAO layer

Another important function of interfacial passivation layer is to passivate interface defects so that photogenerated carriers within and close to the junction will have less recombination therefore improve the quantum efficiency of the device. For front junction solar cells, the improvement is mainly on blue response.

Fig. 5.11 presents the EQE of standard poly-Si/c-Si heterojunction and poly-Si/c-Si heterojunction with NAO layer. Obviously, NAO layer helps the device benefit decent amount of blue response from 360 nm to 600 nm.

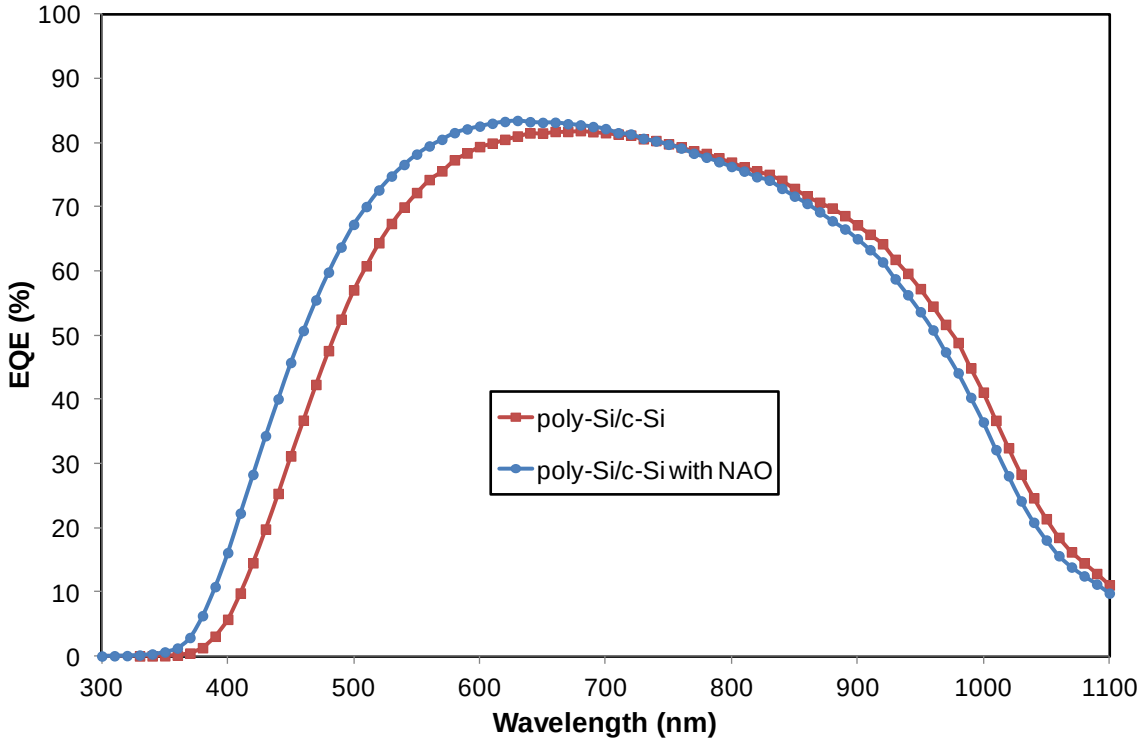


Figure 5.11 EQE results comparison between poly-Si/c-Si heterojunction solar cells with and without interface NAO layer

Illuminated IV characteristics are performed for poly-Si/c-Si heterojunction solar cells with and without interface NAO layer under 100 mA/cm^2 (AM1.5 standard spectrum). The results are presented and compared in Fig. 5.12.

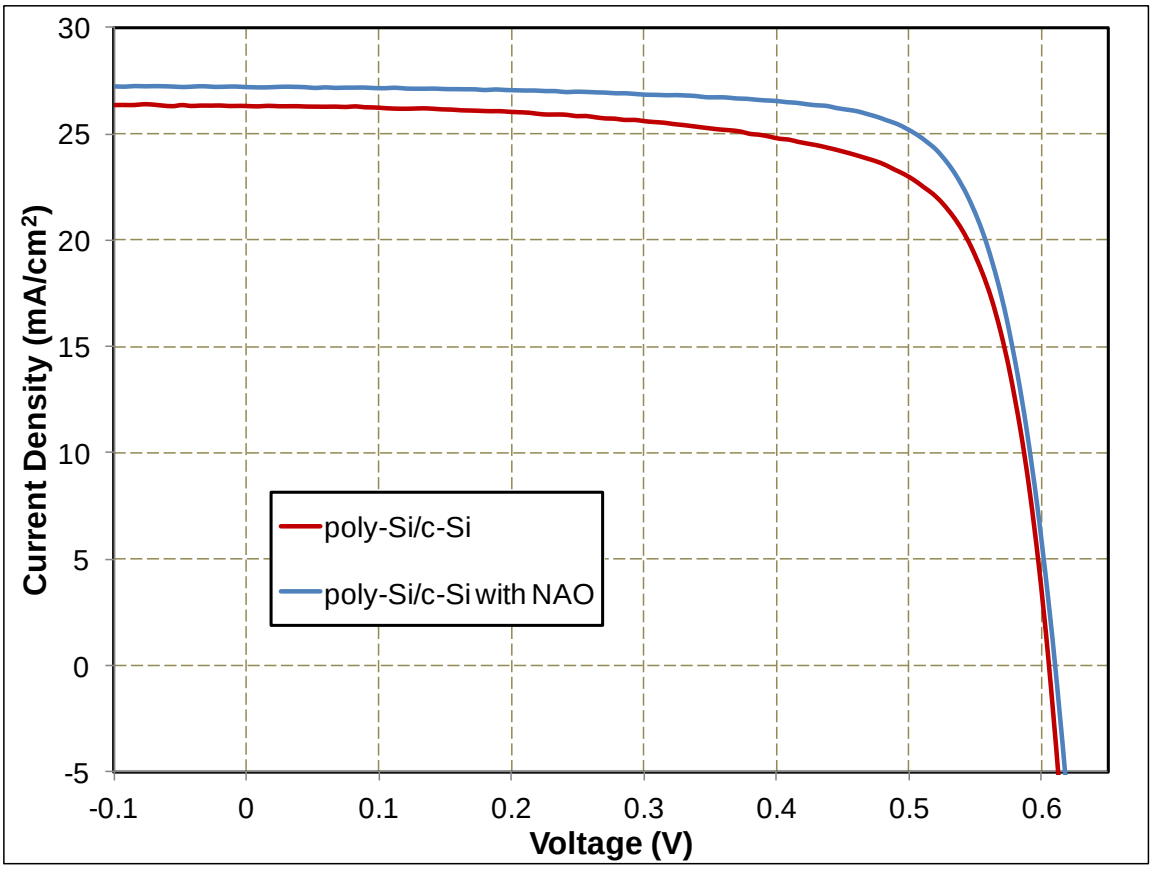


Figure 5.12 Illuminated IV characteristics comparison between poly-Si/c-Si heterojunction solar cells with and without interface NAO layer

Detailed illuminated IV results on the two types of devices are presented in Table. 5.1. From the illuminated characteristics, the promised current output improvement from better blue response is successfully delivered. J_{sc} of 27.2 mA/cm^2 is achieved for poly-Si/c-Si heterojunction device with NAO layer.

Notable amount of FF improvement is also observed. More importantly, from the illuminated IV curve, it is obvious that the FF improvement is mainly from improved shunt resistance as promised in dark IV characteristics. This is a strong indication that the junction properties have been improved.

Slight improvement in V_{oc} is also achieved. Theoretically, V_{oc} improvement is another major benefit for the introduction of interfacial passivation layer, as observed in Chapter 3. However, interface defect density is not the only factor that is governing the V_{oc}. V_{oc} is also highly dependent on substrate properties, such as MCL levels. Since the MCL level for the applied substrates is in the vicinity of 30 µs or worse, it is believed that the V_{oc} output is limited by substrate properties rather than heterojunction

properties. Therefore, the benefit on V_{oc} is not obvious at device level. However, as indicated by the simulation in Chapter 3, if the same fabrication process is applied on high quality substrate, the device is promising to achieve much higher V_{oc} output and therefore higher overall performance. According to the simulation results, a 5 mV Voc improvement is correlated to a defect density deduction of about 1E10 cm^{-3}.

Table 5.1 Illuminated IV result comparison for poly-Si/c-Si device with and without NAO layer

	QE Predict J_{sc} (mA/cm^2)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Efficiency (%)
poly-Si/c-Si	26.17	26. 31	605	72. 2	11. 50
poly-Si/c-Si with NAO	26.85	27. 20	610	76. 1	12. 65

5.4 RTA of LPCVD Poly-Si Emitter Solar Cell

Poly-Si is a relatively defective material. High temperature annealing is one of the most effective way to improve the film quality and therefore improve device performance. However, high temperature annealing with typical furnace normally involves a huge thermal budget. Not only the prolonged annealing will increase the power cost, but also it will introduce more complications into the fabrication process. For example, any contaminates and impurities will be activated and driven into the device and result in significate degradation in device performance.

Rapid Thermal Annealing (RTA) is an effective method to apply high temperature ambient while maintain a relatively low thermal budget. Also, RTA is possible for industrial level transfer. Therefore, RTA has been of great interest for thin film material property improvement [73].

Theoretically, high temperature process can benefit thin film properties by way of rearranging disordered atoms, scale down the amount of dangling bonds, activate dopant atoms, etc.

In this section, RTA is applied on poly-Si/c-Si heterojunction solar cells. Experimentally, RTA process is performed after the LPCVD deposition of poly-Si thin film and prior to the deposition of SiN_x ARC. The system, with sample loaded, rises

the temperature from room temperature to 850 °C, 900 °C or 950 °C within 5 min with N_2 ambient. The plateau time for the RTA in this research is selected as 120 s. The entire RTA process finishes within 15 min.

The research is focused on device level performance change rather than material level analysis. The heterojunction devices are characterized and compared with dark IV measurement, QE measurement and standard illuminated IV measurement. Detailed experiment results are presented below.

5.4.1 RTA Effect on poly-Si/c-Si Heterojunction Solar Cells

Poly-Si/c-Si heterojunction solar cells are fabricated with and without RTA process. Device structure is the same as presented in Fig. 5.5. Dark IV characteristics of the poly-Si/c-Si heterojunction devices with and without RTA process are presented and compared in Fig. 5.13.

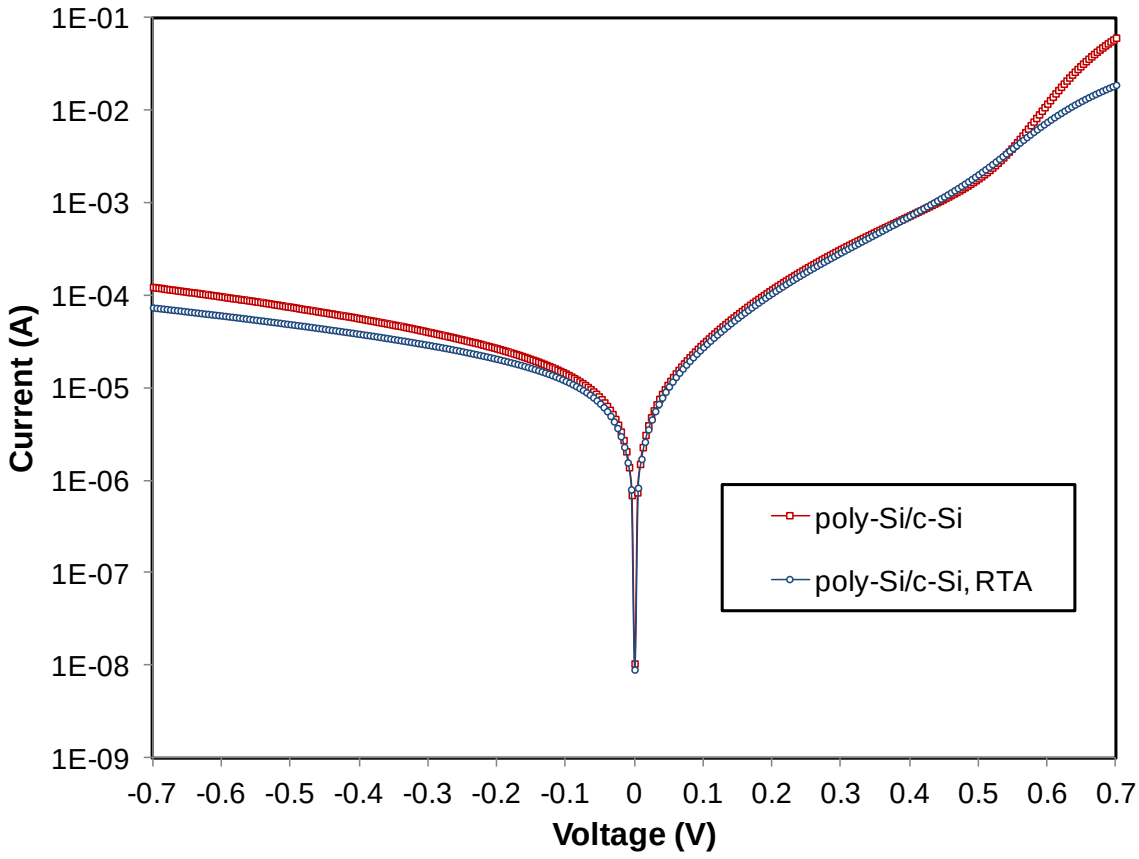


Figure 5.13 Dark IV characteristics comparison between poly-Si/c-Si heterojunction solar cells with and without RTA process

Lower reverse saturate current is observed for RTA processed poly-Si/c-Si heterojunction solar cell. The benefit most likely originates from structural improvement and reduced amount of dangling bonds of the thin film emitter.

Fig. 5.14 presents the EQE results of poly-Si/c-Si heterojunction solar cells with and without RTA process. Considerable amount of blue response boost is achieved with the help of RTA process. Because the improvement does not extend to long wavelength region, it elaborates the statement above that the benefit to RTA processed device originates from improvement on thin film emitter. Better emitter properties make carriers generated within and close to junction edge (and front surface) survive long enough for collection and therefore contribute to photogenerated current.

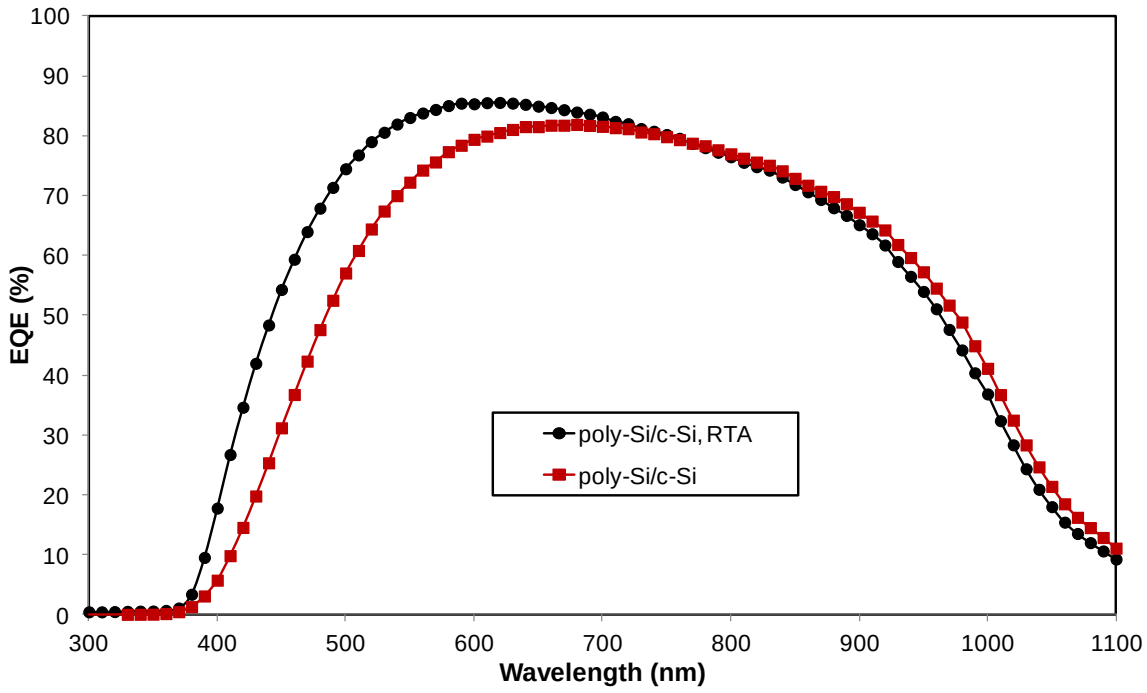


Figure 5.14 EQE results comparison between poly-Si/c-Si heterojunction solar cells with and without RTA process

Illuminated IV characteristics are performed under 100 mA/cm^2 (AM1.5 standard spectrum) for poly-Si/c-Si heterojunction solar cells with and without RTA process. The results are presented and compared in Fig. 5.15.

Detailed illuminated IV results on the two types of devices are presented in Table. 5.2. From the illuminated characteristics, the promised photocurrent output improvement from better blue response is successfully delivered. J_{sc} of 28.18 mA/cm^2 is achieved for

poly-Si/c-Si heterojunction device with RTA process. FF is also improved, despite the considerable amount of increase in output current. V_{oc} value stayed the same although it is expected to be slightly increased from the observation in QE properties. This shows the V_{oc} is most likely limited by the substrate properties. The energy conversion efficiency for the RTA processed poly-Si/c-Si heterojunction is boosted to 12.87%. More importantly, satisfactory J_{sc} and FF (28.18 mA/cm^2 and 75.4%, respectively) are achieved at the same time.

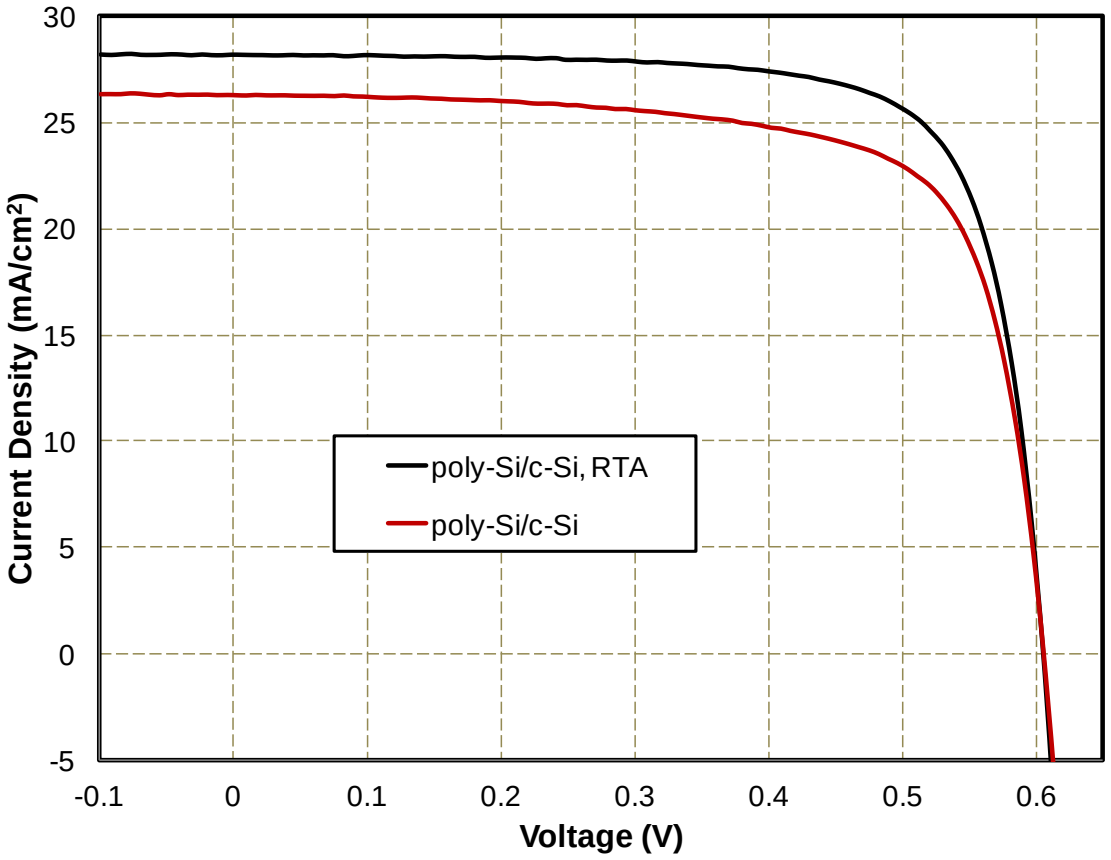


Figure 5.15 Illuminated IV characteristics comparison between poly-Si/c-Si heterojunction solar cells with and without interface NAO layer

Table 5.2 Illuminated IV result comparison for poly-Si/c-Si device with and without RTA process

	RTA Temp (°C)	RTA Time (s)	QE Predict J_{sc} (mA/cm^2)	J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	Eff (%)
Poly-Si/c-Si	N/A	N/A	26.11	26.31	0.605	72.2	11.50
Poly-Si/c-Si, with RTA	900	120	27.70	28.18	0.605	75.4	12.87

5.4.2 RTA Effect on poly-Si/c-Si Heterojunction Solar Cells with Interfacial Passivation Layer

After separate analysis on NAO layer and RTA process, the two optimization methods for poly-Si/c-Si heterojunction are applied together in hope of achieving even higher device performance.

Fig. 5.16 shows the dark IV characteristics for poly-Si/c-Si heterojunction solar cells with NAO layer, with RTA process and with both optimization methods. Regarding to reverse saturation current, NAO layer seems to be superior than RTA treatment. The combination of two optimization methods is obviously benefitting the final device more than one approach alone. That means, most likely the two treatments are improving the device through different mechanisms. Moreover, it is theoretically valid, and the reasons are as follows:

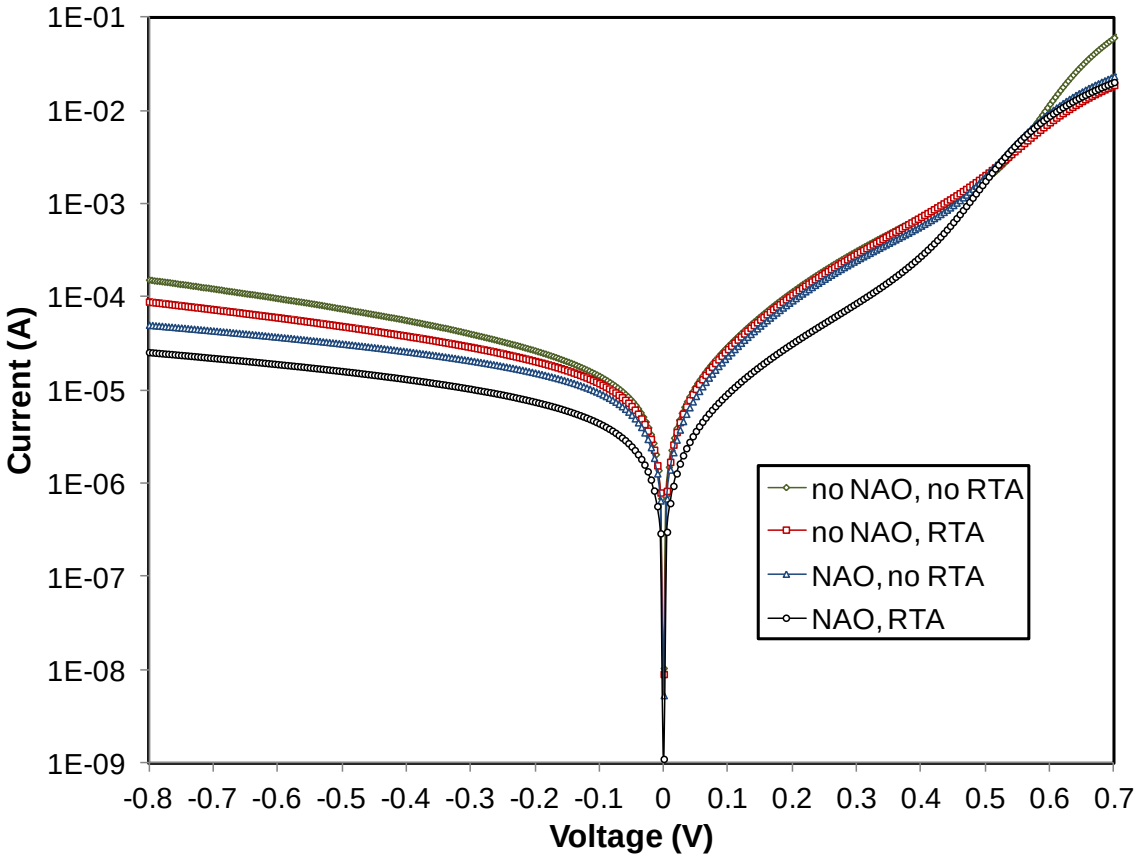


Figure 5.16 Dark IV characteristics comparison between poly-Si/c-Si heterojunction solar cells with and without NAO layer and RTA process

- the main function for NAO layer is to passivate the interface defects of poly-Si/c-Si heterojunction
- the main function of RTA process is to improve the properties of thin film emitter and reduce the defect densities within poly-Si thin film and at the interface of poly-Si/c-Si heterojunction

Another observation is that with both treatment methods, the forward bias current before the diode is turned on is much smaller than that for one treatment only, while the series resistance after the diode is turned on is almost the same. This demonstrates the combination of the two treatment is capable of limiting the shunt current and therefore higher V_{oc} is expected.

Fig. 5.17 presents the EQE result comparison of poly-Si/c-Si heterojunction solar cells with different junction treatment regimes. Again, the same as observed in dark IV characteristics, the implementation of two junction treatment approaches is superior to one approach alone. Further blue response improvement with close to 90% maximum value at about 580 nm is achieved.

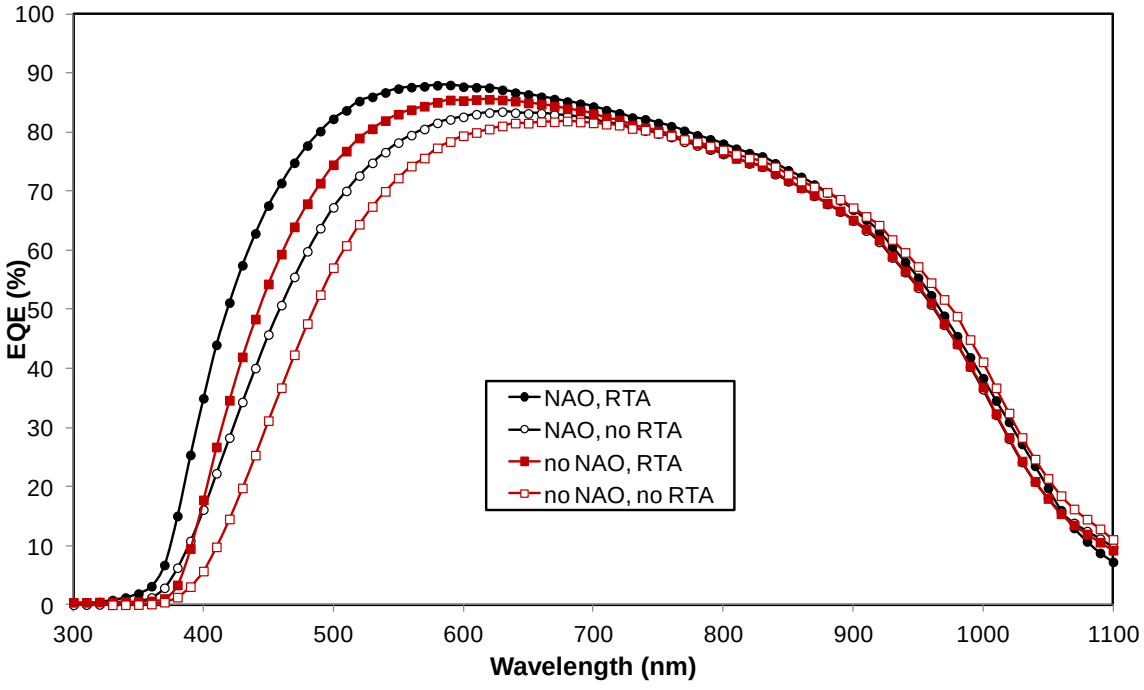


Figure 5.17 EQE results comparison between poly-Si/c-Si heterojunction solar cells with and without RTA process

It is worth mentioning that the devices fabricated herein does not have surface texturing for good optical confinement. Moreover, the thickness for the poly-Si thin film layer has not yet been optimized. Already, the preliminary devices possess close to 90% EQE at about 580 nm wavelength. With space for future improvement, these poly-Si/c-Si heterojunction solar cells are very promising for new types of products. Furthermore, applying the poly-Si/c-Si heterojunction structure to existing solar cell architectures such as IBC solar cells [74] will be interesting and promising research directions.

Fig. 5.18 shows the EQE results of poly-Si/c-Si heterojunction solar cells with different RTA process temperatures. EQE result shows higher RTA temperature resulted in lower red response while kept blue response unchanged. For consistency considerations, the three samples are from the same Si wafer substrate and fabricated with exactly the same rear side treatment. Therefore, the degradation on red response is related to the strength of poly-Si/c-Si heterojunction. That means, when the RTA temperature is too high, it can compromise the passivation properties which enhance the poly-Si/c-Si heterojunction. This is in agreement with the reported results in [13]. The reason is still

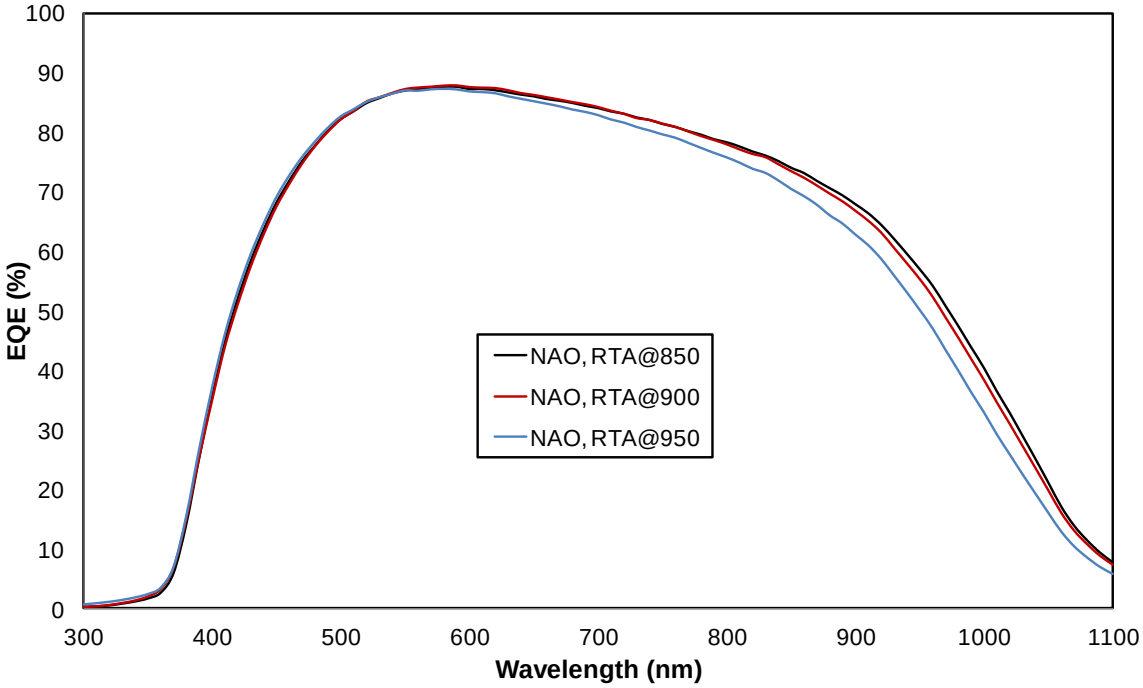


Figure 5.18 EQE results comparison between poly-Si/c-Si heterojunction solar cells with and with RTA process

not fully understood, the most commonly received reason is that micro- or even nano-pin-holes are forming within the NAO layer during high temperature processes, herein

RTA process. In other words, the RTA process applied in this research is over the optimum point. Less annealing time or a bit lower annealing temperature may lead to even better final device performance.

Illuminated IV characteristics are performed under 100 mA/cm^2 (AM1.5 standard spectrum) for poly-Si/c-Si heterojunction solar cells with different RTA process temperature. The results are presented and compared in Fig. 5.19.

Detailed illuminated IV results on poly-Si/c-Si heterojunction devices with different RTA process are presented in Table. 5.3. From the illuminated characteristics, the promised photocurrent output improvements from better blue response comparing to previous devices are again successfully delivered. J_{sc} of 29.68 mA/cm^2 is achieved for poly-Si/c-Si heterojunction device with RTA process at 850 °C. Excellent FF is achieved at 78.3%. The V_{oc} value is relatively low, which is believed to be limited by the substrate properties. The energy conversion efficiency for the RTA processed poly-Si/c-Si heterojunction is boosted to 13.77%. It is worth mentioning that these

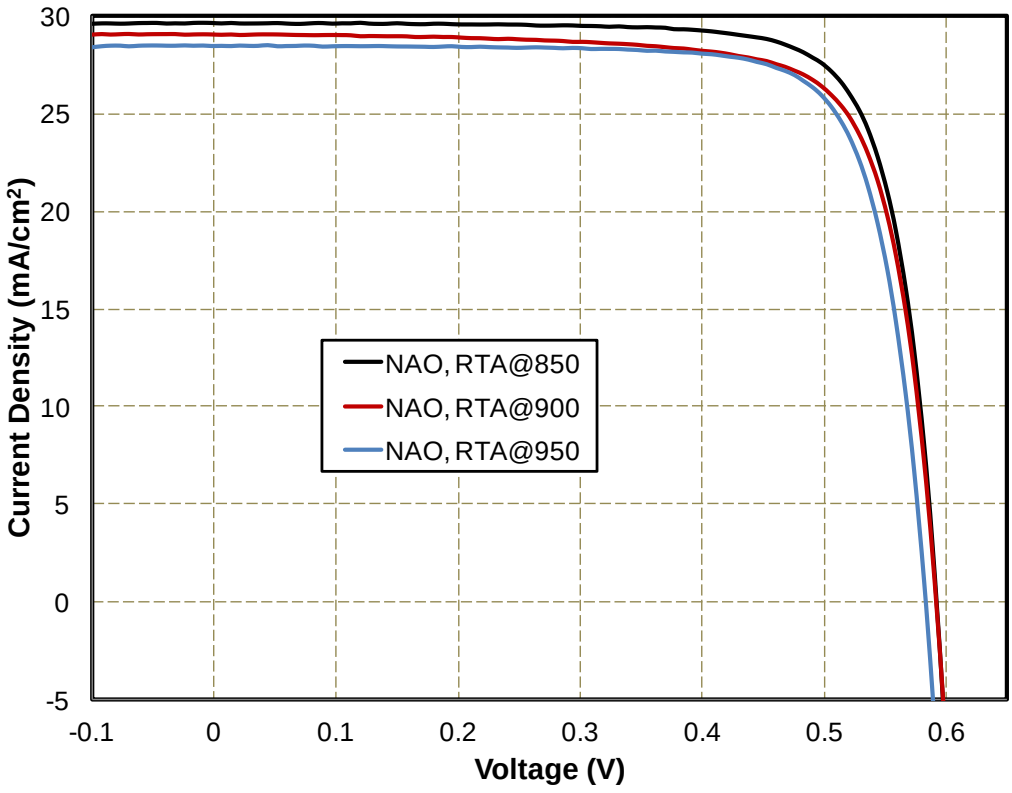


Figure 5.19 Illuminated IV characteristics comparison between poly-Si/c-Si heterojunction solar cells with and without interface NAO layer

preliminary poly-Si/c-Si heterojunction solar cells are fabricated for junction analysis purposes, and therefore have no surface texturing applied for light confinement, and also no rear side passivation applied for less surface recombination. Moreover, the Si substrate applied are low quality Cz wafers with less than 10 µs MCL. Worldwide best reported LPCVD poly-Si emitter solar cell on high quality FZ-wafer (without TCO for front contact) is 14% [14]. Best reported similarly structure poly-Si emitter solar cell on high quality Cz-wafer (MCL in ms range, with TCO for front contact and no rear side passivation) is 14.5% [11]. Best reported poly-Si emitter solar cell (with TCO for front contact and with rear side passivation) on high quality FZ-wafer is 17.9% [12], with average J_{sc} and FF of 31.6 mA/cm^2 and 79.4%, respectively. The goal of realizing good photocurrent while keeping decent FF without applying TCO for front contact is basically achieved. Furthermore, none of the emitter of "best reported" devices are from in-situ deposited n^+ poly-Si.

Table 5.3 Illuminated IV result comparison for poly-Si/c-Si device with different RTA process

Sample No.	Substrate MCL (µs)	NAO Layer	RTA Temp (°C)	RTA Time (s)	J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	Eff (%)
B7-1	<10	Yes	950	120	28.47	0.583	77.9	12.93
B7-2	<10	Yes	900	120	29.05	0.592	76.5	13.15
B7-3	<10	Yes	850	120	29.68	0.592	78.3	13.77
P5-6	>30	Yes	N/A	N/A	27.20	0.610	76.2	12.65
W3-3	20-30	No	900	120	28.18	0.605	75.4	12.87
[14]*	>1000	No	-	-	30.00	0.590	79.5	14.00
[11]**	>2500	Thermal	-	-	28.80	0.705	71.2	14.50
[12]***	>2500	Yes	-	-	31.80	0.694	81.1	17.90

* Poly-Si emitter is achieved by recrystallization of a-Si:H layer (deposited with LPCVD at 627°C) at 650°C for 1 hour.
**Poly-Si emitter is achieved by recrystallization of intrinsic a-Si:H, followed by high temperature diffusion. Passivation achieved by thermal oxide from 30 min annealing at 1050°C. poly-Si BSF was included in the device. ITO was included in both front and back contact for better FF and still relatively low FF.
***Poly-Si emitter is achieved by recrystallization of doped a-Si:H at 700 to 900°C. Poly-Si BSF is applied. NAO layer is applied on both emitter side and BSF side. ITO was included in both front and back contact for better FF. Hydrogen passivation is applied in the middle of the fabrication process.

5.5 Conclusions

LPCVD poly-Si thin film is deposited and analyzed for poly-Si/c-Si heterojunction solar cells.

After the poly-Si thin film is developed, first, standard poly-Si/c-Si heterojunction solar cells are fabricated. Relatively high reverse leakage current and low blue response are observed as expected.

Second, interface passivation layer and RTA process are applied separately to the standard poly-Si/c-Si heterojunction solar cells. Similar to the software simulation results in Chapter 3, the RTA process reduces the defects in the poly-Si emitter and therefore obvious improved blue response is achieved. The interface passivation layer mainly reduces the interface defect densities, as simulated in Chapter 3, a slight Voc improvement is achieved. It is believed that the Voc is still limited by the substrate quality. Otherwise, the Voc improvement with interface passivation layer should be even higher. Furthermore, blue response is also improved by the interface passivation layer, although the benefit is much smaller than that from RTA process.

Finally, poly-Si/c-Si heterojunction solar cells with RTA process and interface passivation layer are fabricated. Close to 30 mA/cm^2 of Isc and close to 80% of FF results are achieved at the same time.

The interface passivation layer is proven beneficial for reducing interface defects of heterojunction devices. This observation is of great importance for heterojunction device analysis and optimization. The application of the same interface passivation layer in Al-ZnO/Si heterojunction photodetector is presented in Chapter 8.

The research outcome indicates that poly-Si/c-Si heterojunction can provide decent device performance with LPCVD deposited n+ emitter and without the presence of TCO layer. It is promising for the low cost, low thermal budget high performance photovoltaic devices in the future. Due to limited time for the research program, the application of such advanced poly-Si/c-Si heterojunction in IBC solar cell structure is listed as future work, as described in Chapter 9.

CHAPTER 6

EFFECT OF POST FABRICATION TREATMENT FOR JUNCTION IMPROVEMENT

Hydrogen passivation is considered very helpful for poly-Si [75,76] and multi-Si devices [31]. The benefit for the bulk of diffused junction c-Si solar cells is also introduced in the recent years [77,78]. However, the hydrogen is usually introduced by expensive hydrogen plasma [31,79] or laser assisted processes [80]. Successful hydrogen passivation process without plasma and laser assistance has been demonstrated for multi-Si heterojunction solar cells [81]. However, to the author's best knowledge, it has not been demonstrated for c-Si solar cells or poly-Si/c-Si heterojunction solar cells. In this section, the author explores the possibility of introducing hydrogen passivation on diffused junction c-Si solar cells and poly-Si/c-Si heterojunction solar cells without plasma and laser conditions. The Low Pressure Hydrogen Annealing (LPHA) and Low Pressure Hydrogen Plasma (LPHP) are applied on standard diffused junction Si solar cells presented in Chapter 4, and LPHA is applied on poly-Si/c-Si heterojunction solar cells presented in Chapter 5.

6.1 Experiment

Standard diffused junction Si solar cells are cleaned with acetone, IPA and DI wafer. Samples fabricated from exactly the same processes are subjected to different hydrogenation processes: some with Low Pressure Hydrogen Annealing (LPHA) and others with Low Pressure Hydrogen Plasma (LPHP). To maintain exactly the same

condition for other parameters other than the plasma component, the LPHA and LPHP processes are implemented in the same equipment, Trion rf-PECVD chamber, as shown in Fig. 4.5. Gas flow rate for the H_2 is 100 sccm, no other gases are introduced. The process temperature and pressure are 350 °C and 200 mTorr, respectively, for both processes. For the LPHP process only, a RF power of 15 W is applied to maintain a purple glowing plasma. The duration of both processes are 15 min.

6.2 Post-fabrication LPHA for Standard Diffused Junction Si Solar Cell

The hydrogenation processes are applied at device level. Therefore, performances of the same devices before and after hydrogenation are compared.

Dark IV, EQE and standard Illuminated IV characteristics are performed for this analysis. Dark IV and standard Illuminated IV results have obvious improvement with the LPHA or LPHP process. Very small improvement on EQE results are observed and therefore omitted. However, the total current outputs are still slightly increased.

Fig. 6.1 shows the dark IV performance change for diffused junction Si solar cells before and after LPHP (top) and LPHA (bot) processes. Hydrogenation processes should passivate the junction and bulk defects (i.e. B-O defect), therefore reduce reverse saturation current. From the experiment results, obvious improvements on reverse saturation current are observed for both processes as expected. With the help of LPHP process, device rectification ratio changed from 5.6×10^2 to 5.1×10^3 at ±0.7 V. Similar benefit is observed for LPHA process, device rectification ratio improved from 5.6×10^2 to 2.8×10^3 at ±0.7 V. With the obvious improvement in dark IV characteristics, the device performance for illuminated IV should expect better shunt resistance and higher V_{oc} values.

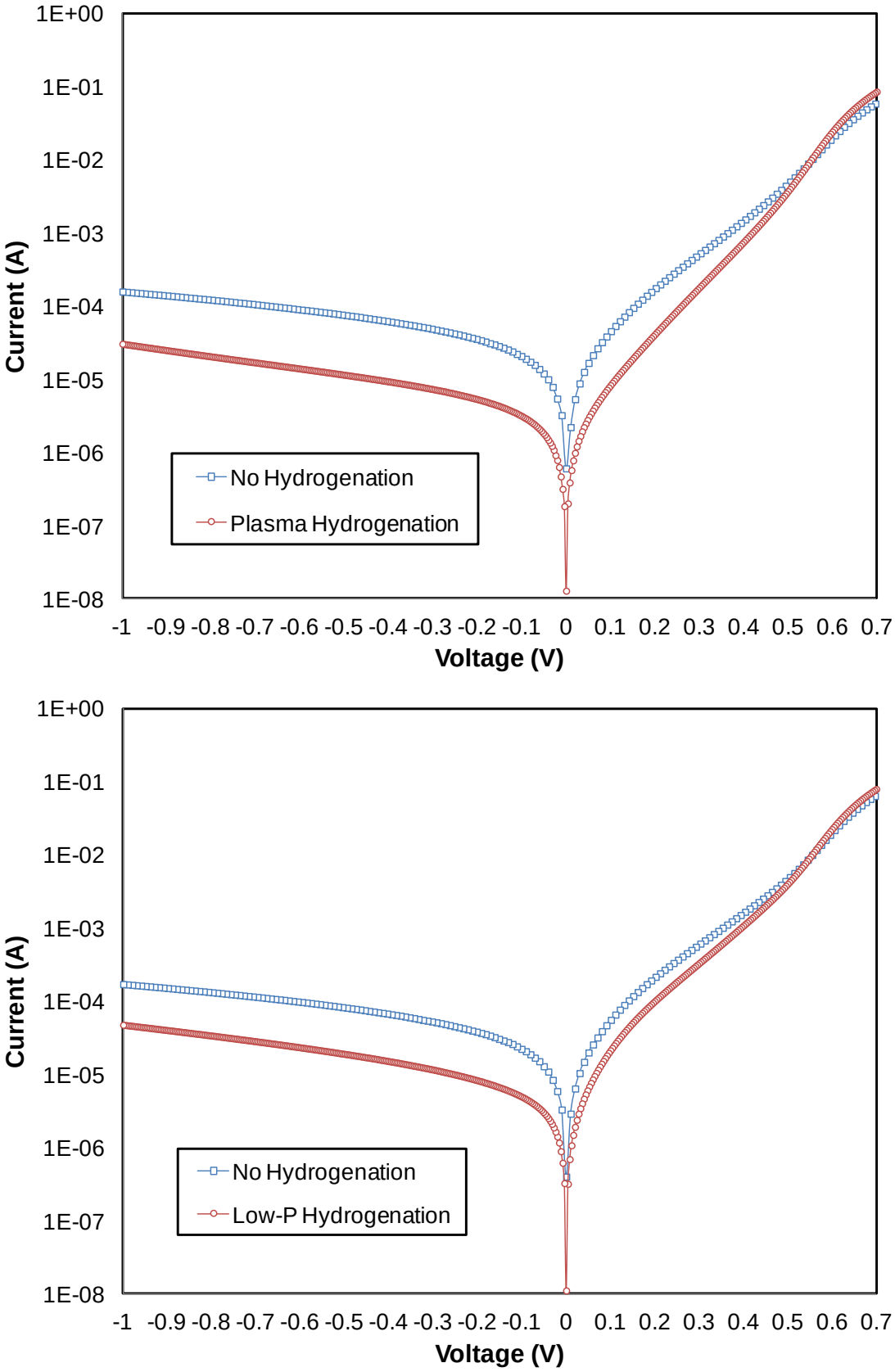


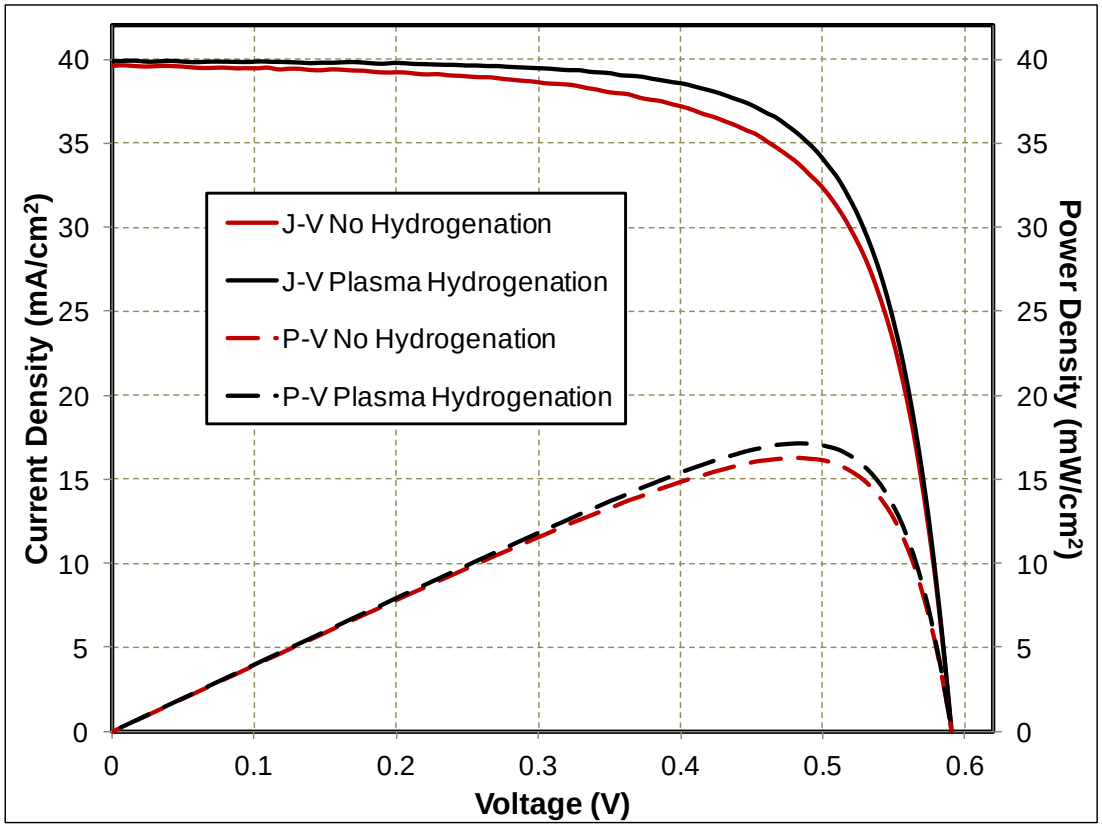
Figure 6.1 Dark IV characteristic comparison for standard Si solar cells before and after LPHP and LPHA hydrogenation

Fig. 6.2 presents the standard illuminated IV performance change before and after LPHP (top) and LPHA (bot) processes. Both hydrogenation processes exhibit considerable improvement on device FF. Moreover, the improvement is basically from higher shunt resistance. This observation aligns with the smaller reverse saturate current demonstrated in dark IV characteristics.

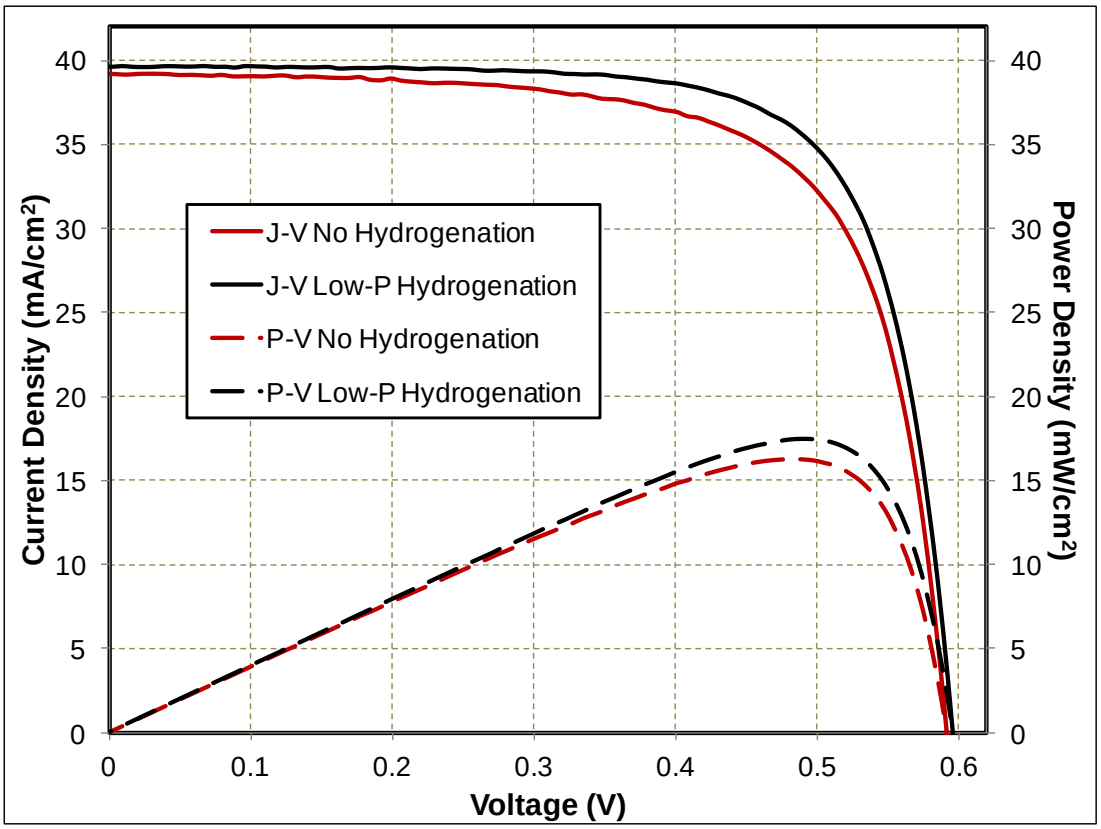
Slight increase in J_{sc} and V_{oc} is also observed as shown in Table 6.1. V_{oc} improvement is relatively smaller than expected. Again, it is believed that the substrate properties are limiting the final V_{oc} output of the devices.

The comparative study shows that hydrogen passivation can be achieved for finished devices. Furthermore, without the presence of plasma, H_2 annealing at low pressure can also provide reasonable hydrogen passivation.

At this point, the standard diffused junction Si solar cell baseline technology has been established. **Energy conversion efficiency for typical device is in the vicinity of 17.2%.**



(a)



(b)

Figure 6.2 Standard illuminated IV (100 mW/cm^2, AM1.5) characteristic comparison for standard Si solar cells before and after LPHP and LPHA hydrogenation

Table 6.1 Device performance before and after different hydrogenation process

Sample ID	Hydrogenation	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Eff (%)
W3-0207-C4	Before Hydrogenation	39.56	590	69.7	16.29
	After Plasma Hydrogenation	39.91	591	72.9	17.17
W3-0207-C2	Before Hydrogenation	39.20	591	70.1	16.24
	After Low-P Hydrogenation	39.64	596	73.8	17.43

6.3 Post-fabrication LPHA for poly-Si/c-Si Hetero-Junction Solar Cells

Post-fabrication LPHA is applied on poly-Si/c-Si heterojunction solar cells with different structures as presented in Chapter 5. The purpose of LPHA process is to passivate the defects within poly-Si emitter and at the poly-Si/c-Si heterojunction

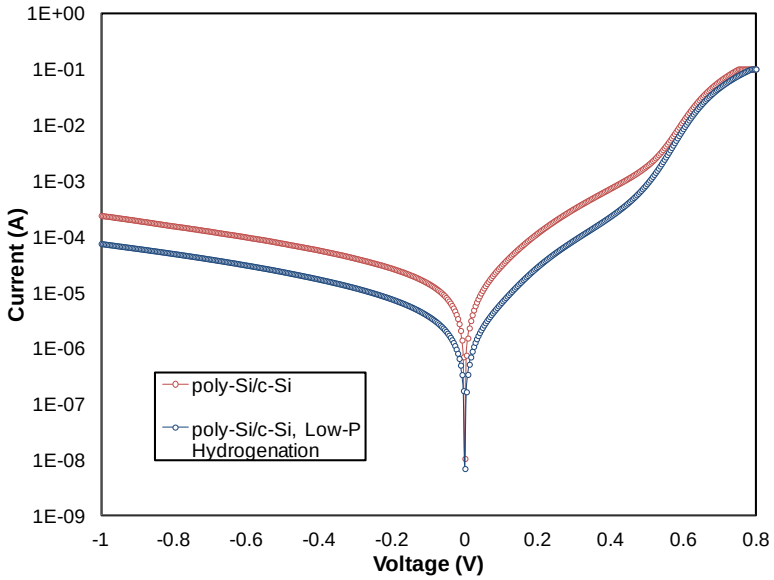
interface. Again, main improvement in the device performance is expected from better reverse saturation current and therefore better FF and V_{oc}.

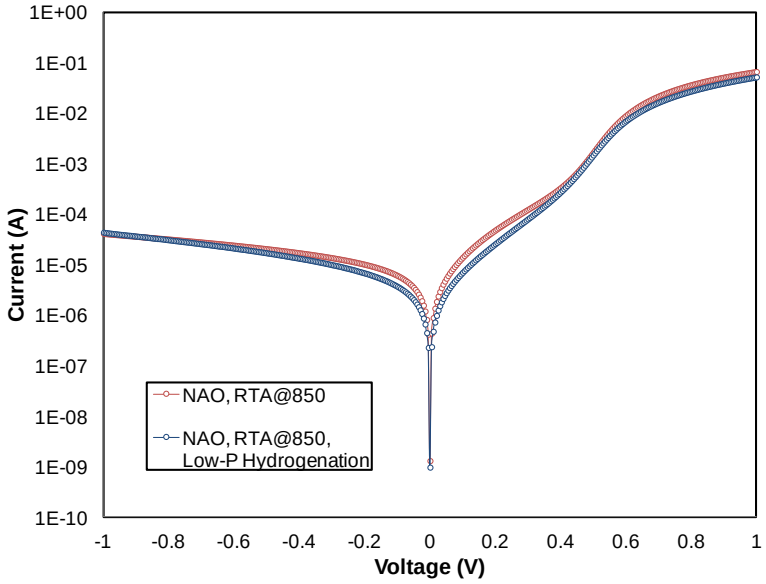
Fig. 6.3 shows the dark IV characteristics of different poly-Si/c-Si heterojunction solar cells before and after LPHA process. Improvement in leakage current is observed in all types of poly-Si/c-Si heterojunction devices. Improvement for devices with both NAO and RTA processes is less significant. That means, some defects that can be passivated by hydrogenation can also be eliminated by NAO interfacial passivation or RTA process.

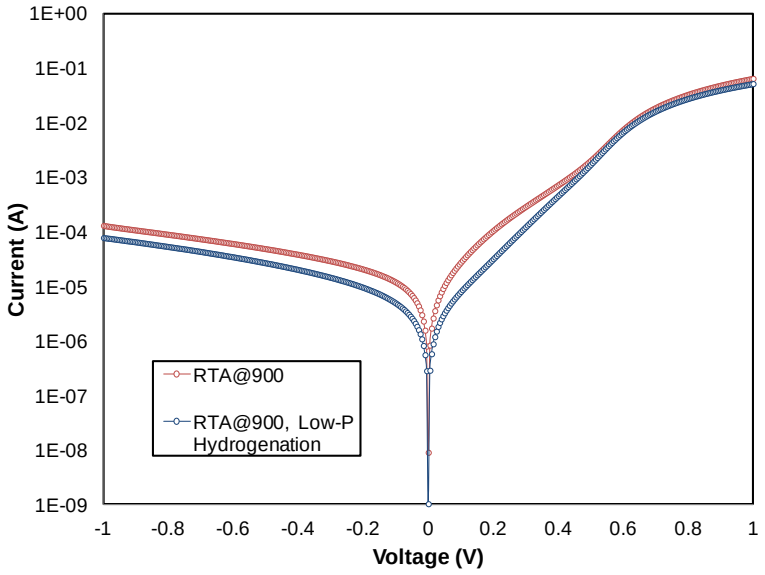
Table. 6.2 presents the poly-Si/c-Si heterojunction solar cell performance under standard illumination. Although not significant, almost every type of device has an improvement on device performance after LPHA. Interesting observation is, the dark saturation current and the ideality factor of the second diode (two-diode model) for each type of cell has been reduced. That means the LPHA process can passivate the crystal defect within the junction, improve shunt resistance and therefore reduce the dark leakage current.

Benefit from hydrogenation process is expected to be more obvious for poly-Si/c-Si heterojunction devices than diffused junction solar cells, because poly-Si/c-Si structure has much more crystal defects. However, the poly-Si emitter thin film is already a hydrogen rich layer. During LPHA, a competing process takes place at the same time, that is hydrogen emission from poly-Si thin film. Therefore, the benefit from LPHA is not as significant as expected.

The champion cell of poly-Si/c-Si heterojunction achieved 13.81% efficiency with FF and J_{sc} of 79.1% and 29.37 mA/cm^2, respectively.


1E+00
1E-01
1E-02
1E-03
1E-04
1E-05
1E-06
1E-07
1E-08
1E-09
Current (A)
-1
-0.8
-0.6
-0.4
-0.2
0
0.2
0.4
0.6
0.8
Voltage (V)
poly-Si/c-Si
poly-Si/c-Si, Low-P Hydrogenation


1E+00
1E-01
1E-02
1E-03
1E-04
1E-05
1E-06
1E-07
1E-08
1E-09
1E-10
Current (A)
-1
-0.8
-0.6
-0.4
-0.2
0
0.2
0.4
0.6
0.8
1
Voltage (V)
NAO, RTA@850
NAO, RTA@850, Low-P Hydrogenation


1E+00
1E-01
1E-02
1E-03
1E-04
1E-05
1E-06
1E-07
1E-08
1E-09
Current (A)
-1
-0.8
-0.6
-0.4
-0.2
0
0.2
0.4
0.6
0.8
1
Voltage (V)
RTA@900
RTA@900, Low-P Hydrogenation

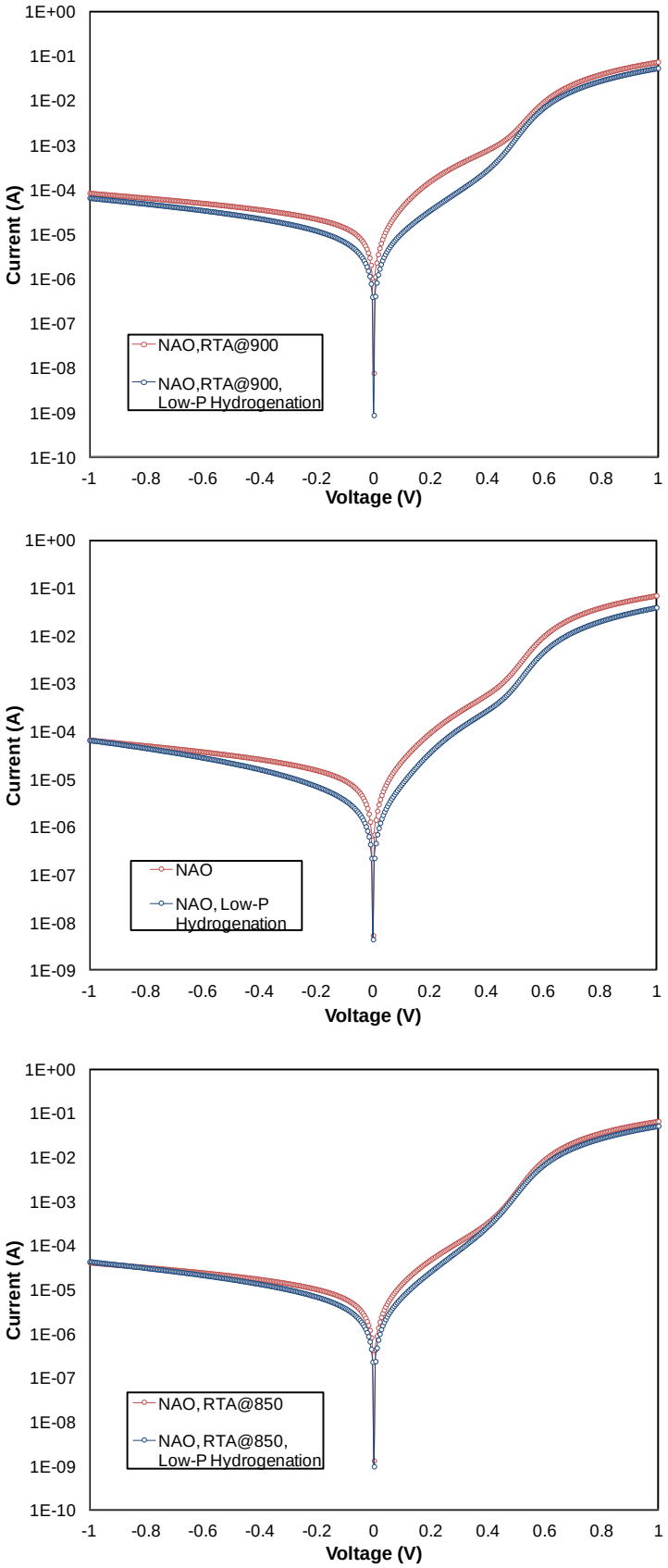


Figure 6.3 Dark IV characteristic comparison for poly-Si/c-Si heterojunction solar cells before and after LPHA hydrogenation

Table 6.2 LPHA effect on poly-Si/c-Si heterojunction solar cells

Sample ID	NAO Layer	RTA Temp (°C)	RTA Time (s)	Low-P Hydro-genation	Ideality Factors (n_1, n_2)	Dark Saturation Current I_{01}, I_{02} (A)	Jsc (mA/ cm^2)	Voc (V)	FF (%)	Eff (%)
W3-2	No	N/A	N/A	No	1.80, 3.04	3E-8, 3E-6	26.00	0.604	72.8	11.42
				Yes	1.59, 2.62	4E-9, 2E-6	26.69	0.618	77.1	12.73
W3-3	No	900	120	No	2.96, 2.92	3E-6, 8E-6	28.18	0.605	75.4	12.87
				Yes	3.61, 2.35	8E-6, 2E-6	28.18	0.605	75.9	12.94
P5-6	Yes	N/A	N/A	No	2.26, 2.87	4E-7, 6E-6	27.20	0.610	76.2	12.65
				Yes	2.21, 2.52	1E-7, 2E-6	27.64	0.612	76.1	12.86
B7-1	Yes	950	120	No	1.92, 3.14	7E-8, 5E-6	28.47	0.583	77.9	12.93
				Yes	2.05, 2.63	1E-7, 2E-6	28.35	0.585	77.3	12.82
B7-2	Yes	900	120	No	2.45, 2.96	8E-7, 1E-5	29.05	0.592	76.5	13.15
				Yes	2.15, 2.67	2E-7, 2E-6	28.87	0.594	78.0	13.38
B7-3	Yes	850	120	No	2.05, 3.15	1E-7, 4E-6	29.68	0.592	78.3	13.77
				Yes	2.21, 3.01	2E-7, 2E-6	29.37	0.594	79.1	13.81

6.4 Conclusions

Hydrogenation process is applied and analyzed on finished solar cells without the presence of plasma.

By applying LPHA, diffused homo-junction Si solar cells exhibit obvious improvement in both dark leakage current and rectification ratios. Moreover, the overall solar cell performance is boosted with 1% absolute increase achieving more than 17% final energy conversion efficiency.

Different types of poly-Si/c-Si heterojunction solar cells almost all benefited from the LPHA process. One common improvement is the dark saturation current for the second diode I_{02} (two-diode model). That means, defects within the junction have been passivated. Moreover, although limited, there have been slightly voltage output improvement for almost each type of heterojunction devices. Based on the simulations in Chapter 3, it indicates that the LPHA can realize heterojunction interface defect passivation.

Chapter 7

ADVANCDED AL-ZNO/SI HETERO-JUNCTIONS FOR PHOTODETECTOR APPLICATION

In this chapter, after a brief introduction of Al-ZnO thin film, a systematic analysis is conducted on both Al-ZnO/(n)Si and Al-ZnO/(p)Si structures to understand the operation of these heterojunctions as photodiodes. Quantum efficiency measurements performed under voltage bias and dark and illuminated I-V characterization allowed to explain the mechanisms of the photoresponse. The photocurrent dependence on the inversion and/or depletion layer as well as the way bias voltage influences the photocurrent are presented [82].

7.1 Al-ZnO thin film

A highly crystallized Al-ZnO thin film is important for excellent optical and electrical properties and hence is crucial for high performance Al-ZnO/Si heterojunction devices.

The Al-ZnO film deposition in this research was carried out in an RF magnetron sputtering system (Intlvac – nanochrome I). The sputtering targets were ceramic ZnO:Al_2O_3 disc targets with 99.9999% purity (Angstrom Sciences). The films were deposited at 250 °C with a chamber pressure of 0.5 mTorr and RF plasma power of 150 W. After a 2-minute pre-sputtering period in the chamber to stabilize plasma conditions, the Al-ZnO deposition was carried out to yield films with thickness of 780 nm,

measured by surface profiler (Dektac 150). Al-ZnO film properties can be slightly different with different thickness. The 780 nm film is the “standard” film for thin film characterizations.

Structural analysis was carried out by high resolution XRD at incident angle of 0.6° with CuKα (PANanalytical Xpert Pro MRD HR-XRD). Fig. 7.1 shows the XRD result of the standard Al-ZnO thin film. A strong dominate peak at 2 66° shows high crystallinity at (103) plane. A small peak at 34° is also observed at (002) plane.

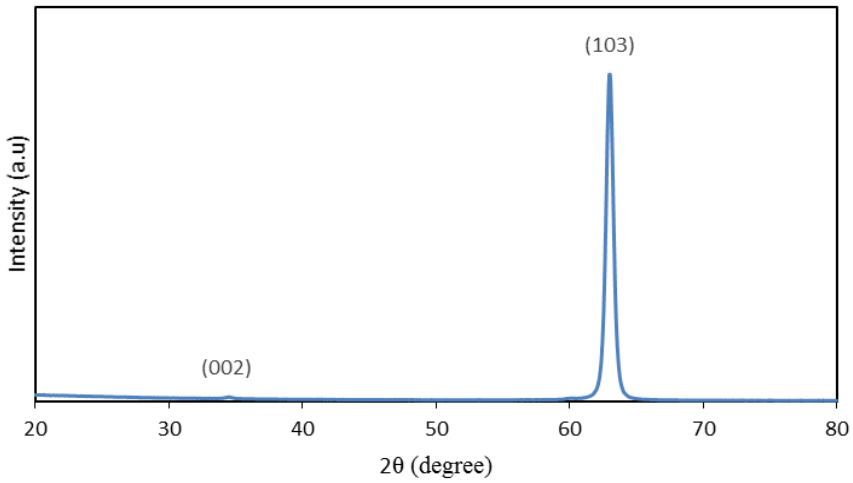


Figure 7.1 HR-XRD measurement result for standard Al-ZnO thin film

Fig. 7.2 presents the cross-section TEM micrograph and top surface HR-SEM image of the standard Al-ZnO thin film deposited on Si substrate, respectively. The TEM micrograph clearly shows the columnar structure of the sputtered Al-ZnO thin film. These columnar grains consist of several tilted crystallites. The HR-SEM image clearly shows the top morphology of Al-ZnO thin film. Also, the crystalline grain size can be roughly seen from the image.

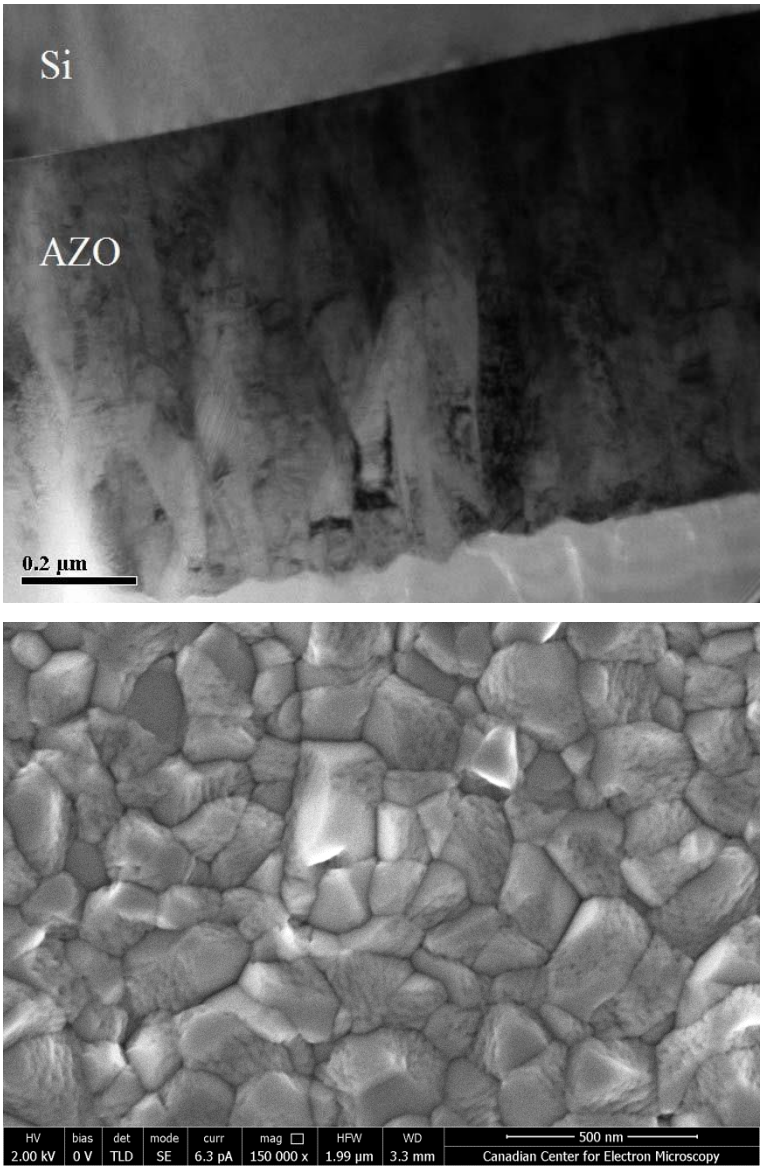


Figure 7.2 a) TEM image of Al-ZnO thin film on Si; b) HR-SEM image of top surface of Al-ZnO thin film

4" diameter glass substrates (Corning, Eagle XG) were used for standard Al-ZnO film deposition to carry out electrical and optical analysis. A picture of the sample with four contact points for Hall Effect measurement is shown as inset in Fig. 7.3. From Hall Effect measurement the carrier concentration was found to be 1.07×10^{21} cm^{-3} with the corresponding film resistivity of 2.94×10^{-4} Ω-cm, more detailed results are presented in Table 7.1. The high carrier concentration indicated that the Al-ZnO film is degenerate.

Table 7. 1 Hall Effect Measurement results of Al-ZnO thin film

Temp (^{0}C)	R_{Sh} (Ω/sq)	Resistivity ρ (Ω.cm)	Carrier Conc. N_e (cm^{-3})	Hall Mobility μ ($cm^{-2}V^{-1}s^{-1}$)	Thickness (nm)	Ref. Index (n) @ 550 nm
250	3.7	2.94E-04	1.07E+21	19.9	780	1.86

UV/VIS/near-infrared spectrophotometer (PerkinElmer Lamda 1050) was used to measure the optical transmission of the film. As shown in Fig. 7.3, a high average transmission, greater than 85% in the visible spectrum (390 - 700 nm), was observed even without eliminating the reflection and absorption caused by glass substrate. More details on the Al-ZnO film deposition and properties can be found in [83].

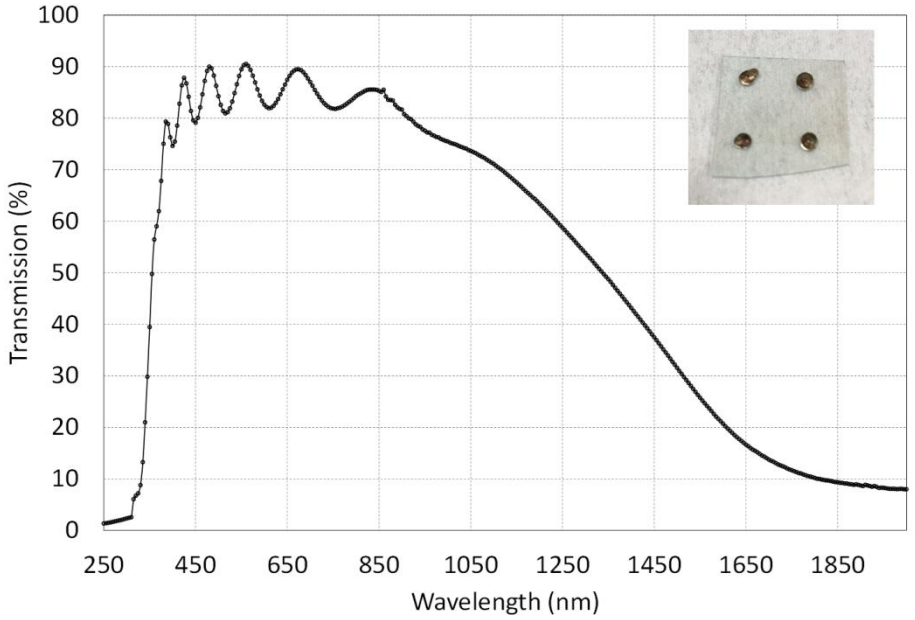


Figure 7.3 Transmission result of Al-ZnO thin film on glass. Inset: image of Al-ZnO sample for HEM

7.2 Device fabrication

7.2.1 Substrates

(100) oriented, 4" diameter n- and p- type Czochralski grown Si wafers were used as substrates for the deposition of the Al-ZnO films. The resistivity and carrier concentrations in the Si substrates determined by Hall Effect measurements were 1.5 Ω-cm and 4.03×10^{15} cm^{-3}, respectively for the n-type, and 0.6 Ω-cm and 1.32×10^{16} cm^{-3}, respectively for the p-type.

7.2.2 Al-ZnO Deposition

Prior to Al-ZnO deposition, Si substrates underwent standard RCA1 and RCA2 cleaning with a subsequent 30 s dip in 10% HF to remove the oxides. And then after DI water rinse and N_2 drying steps the wafers were quickly loaded into the sputtering chamber. The deposition conditions are the same as described above.

7.2.3 Device Structure

Diode structures with dimensions 22 mm × 22 mm were fabricated on samples with Al-ZnO films deposited on n- and p- type Si substrates. The rear ohmic contact was formed by blanket deposition of ≈ 1 μm thick Al by e-beam evaporation. The front Al contact pad was formed by evaporation through shadow mask covering 15 mm × 6 mm of the diode area. A schematic of the Al-ZnO/(n)Si diode is shown in Fig. 7.4 (a). Fig. 7.4 (b) and (c) are photos of standard Al-ZnO/Si device and optimized high performance Al-ZnO/(n)Si device, respectively.

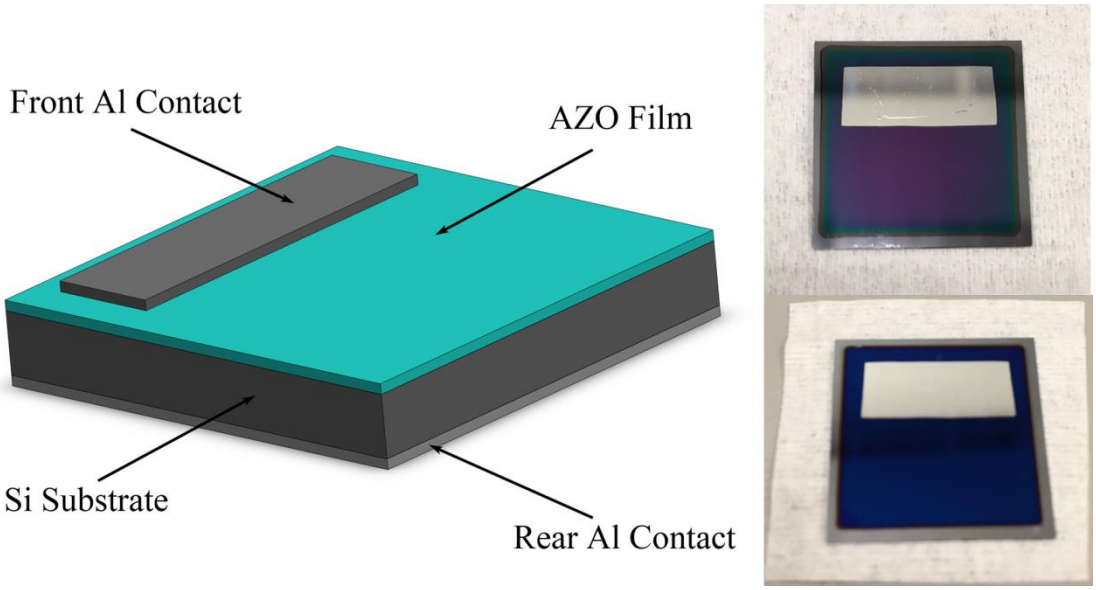


Figure 7.4 a) Schematic diagram of Al-ZnO/Si photodetector; b) Al-ZnO/Si photodetector with thick Al-ZnO layer; c) High performance optimized Al-ZnO/Si photodetector in Chapter 8.

Films deposited on Si substrates were used to study the Al-ZnO/Si interface using high resolution transmission electron microscopy (HRTEM, FEI Titan 80-300 HB, FEI Co). Fig. 7.5 shows an HRTEM image of the interface. The periodic atomic arrangement in the Si substrate and in the Al-ZnO film is clearly visible. The distinct interfacial region

between the Al-ZnO film and the Si substrate corresponds to a thin oxide (SiO_x) layer of about 2 nm thickness. Its presence is attributed to the existence of oxygen during deposition [84,85]. The formation of such thin oxide layer at the onset of sputtering process has been observed for similar structures of metal oxide film on Si [86,87].

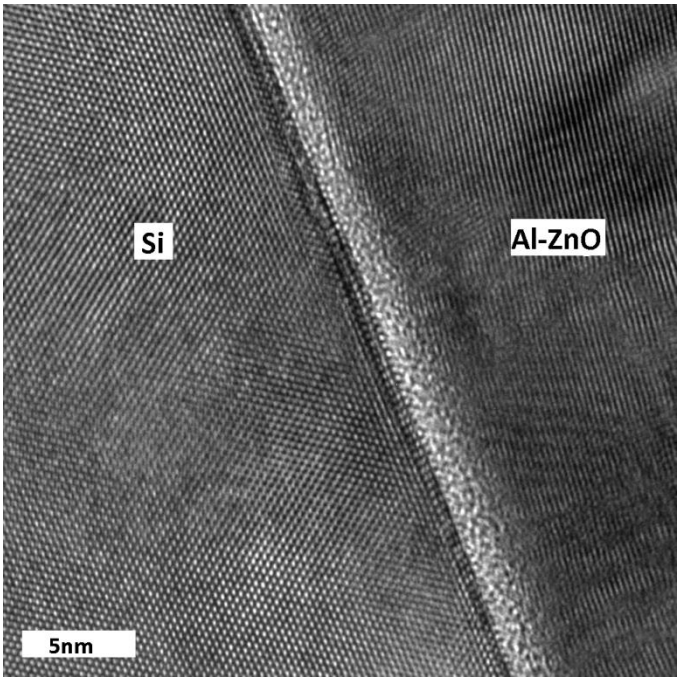


Figure 7.5 HRTEM image showing the Al-ZnO/Si interfacial region with a thin (≈2 nm) SiO_x region

7.3 Al-ZnO/Si heterojunction analysis

In research of Al-ZnO/Si heterojunction structures, the terms “forward bias” and “reverse bias” are defined according to the substrate. Therefore, forward bias of Al-ZnO/(n)Si heterojunction refers to the Al-ZnO being more positive compared to (n)Si. Meanwhile, “forward bias” of Al-ZnO/(p)Si corresponds to Al-ZnO kept at more negative than (p)Si.

7.3.1 Dark I-V Analysis

7.3.1.1 Dark I-V Analysis of the Al-ZnO/(n)Si Heterojunction

Fig. 7.6 shows the current-voltage characteristic of the Al-ZnO/(n)Si heterojunction in the dark at room temperature. The device shows diode-like behavior, with a

rectification ratio of 6.7×10^3 at ± 0.5 V. The reverse bias current in the μA range and the low turn-on voltage indicate the existence of a Schottky barrier. Assuming the main carrier transport mechanism is "thermionic emission" of majority carriers, the effective barrier height ϕB and ideality factor n can be calculated using the following equations [36,88,89]:

$$I_{dark} = I_0 \left[exp\left(\frac{qV}{nkT}\right) - 1 \right] \quad (1)$$

$$I_0 = AA^*T^2 exp\left(\frac{-q\phi_B}{kT}\right) \quad (2)$$

Where I_0, k, A, and A^* are the reverse saturation current, Boltzmann's constant, device area, and Richardson constant respectively. With the value for A^* of 3.2×10^5 $Am^{-2}K^{-2}$ (for $m_e^* = 0.27m_0$), the effective ϕB of the Schottky barrier is found to be ≈ 0.72 V. This value is in agreement with the ϕB of 0.78 V obtained by C-V measurements [90], and hence the assumption of "thermionic emission" dominating the carrier transport mechanism in the Al-ZnO/(n)Si heterojunction seems to hold.

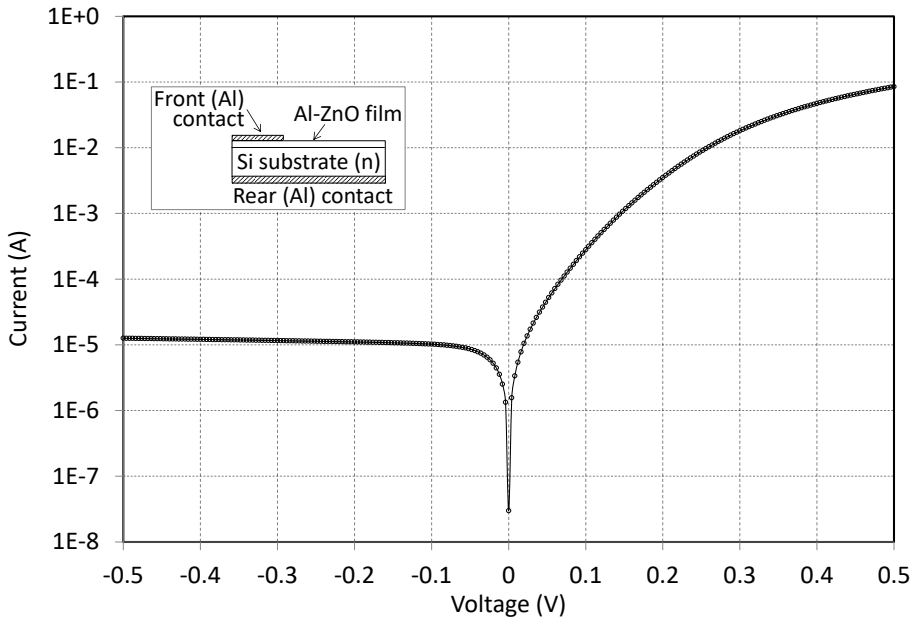


Figure 7.6 Dark IV characteristic of the Al-ZnO/n(Si) heterojunction device. (inset: device structure)

The calculated ideality factor n is 1.12 at the 0.1 V bias region, and it becomes larger at higher voltage bias (n=1.69 at 0.25 V). Since the work function of Al-ZnO is in the 4.1-4.7 eV range for low oxygen concentrations [91-93] and the crystalline surface electron affinity of (n)Si is 4.05 eV, a ϕB of 0.72 eV indicates that the barrier is not formed simply by Fermi level alignment. Fermi level pinning effect [94] is happening at Al-ZnO/Si interface, which is possible since our film is degenerated as shown by

Hall Effect measurements. Furthermore, 0.72 eV is very close to the general experience of Fermi level pinning effect for Si which is two thirds of Si bandgap (1.12 eV). The slightly smaller value could be the result of image-force effect [89]. The Fermi level position of (n)Si is calculated to be 0.24 eV below conduction band based on doping concentration and the valence band offset is calculated by the ϕB and bandgap of the two materials. From these data we are able to complete the energy band diagram under equilibrium condition which is schematically shown in Fig. 7.7. An important observation is the presence of an inversion layer (region c) at the Al-ZnO/(n)Si interface. Specifically, a (p^-)Si/(n)Si junction is naturally formed adjacent to the interface, meaning that, before the current density across the interface reaches the tunneling limit of the thin oxide layer [87], the Al-ZnO/(n)Si heterojunction is equivalent to a Al-ZnO/(p-)Si/(n)Si structure.

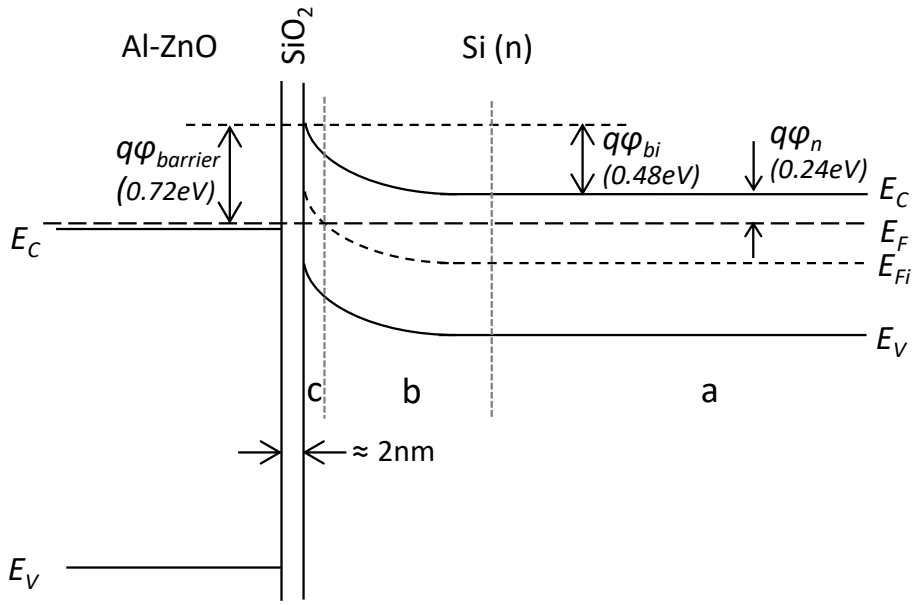


Figure 7.7 Energy band diagram of the Al-ZnO/(n)Si heterojunction under equilibrium. The three regions, a) quasi-neutral, b) depletion, and c) inversion are also indicated.

7.3.2 Dark I-V Analysis of the Al-ZnO/(p)Si Heterojunction

Fig. 7.8 shows the room temperature I-V characteristics of Al-ZnO/(p)Si heterojunction in the dark. No rectifying behavior is observed for +1 V to -1 V. The shape of the curve is similar to that of a low barrier height Schottky junction. The equivalent contact resistance is measured to be 135 Ω.

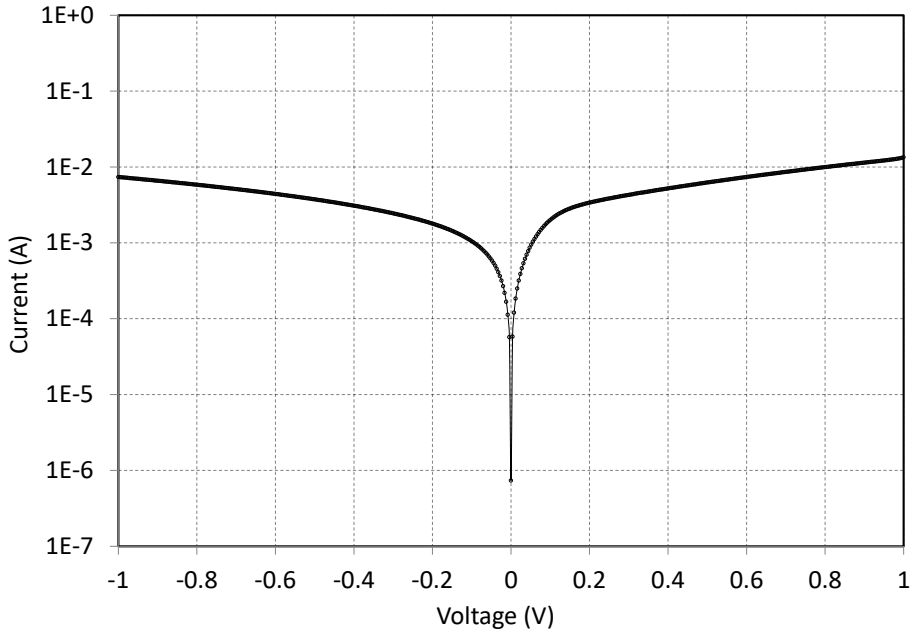


Figure 7.8 Dark IV characteristic of the Al-ZnO/p(Si) heterojunction device at room temperature.

Since the observed reverse bias current is high, there must be multiple carrier transport mechanisms other than thermionic emission alone. Therefore, the ϕB of Al-ZnO/(p)Si heterojunction cannot be calculated from the dark I-V plot. Considering that the sum of barrier heights between a given metal and semiconductor of n- and p- types is expected to be equal to the semiconductor bandgap [89], the ϕB of Al-ZnO/(p)Si heterojunction is expected to be around 0.4 eV (1.12 eV minus 0.72 eV). On the other hand, energy pinning effect considerations indicated the Schottky ϕB between ZnO and (p)Si to be approximately 0.37 eV [94]. Hence, a ϕB value in the vicinity of 0.37 to 0.4 eV can be assumed for the Al-ZnO/(p)Si heterojunction. With image-force effect, the effective ϕB can be even lower. While for energy pinning effect the actual ϕB is irrelevant to the Si doping level, the effective ϕB is lower for the substrate with higher doping. Therefore, to achieve reasonable rectifying behavior with the Al-ZnO/(p)Si structure, the Si substrate needs to be very lightly doped as reported in [95]. Considering all these facts, the energy band diagram for our Al-ZnO/(p)Si heterojunction is presented in Fig. 7.9.

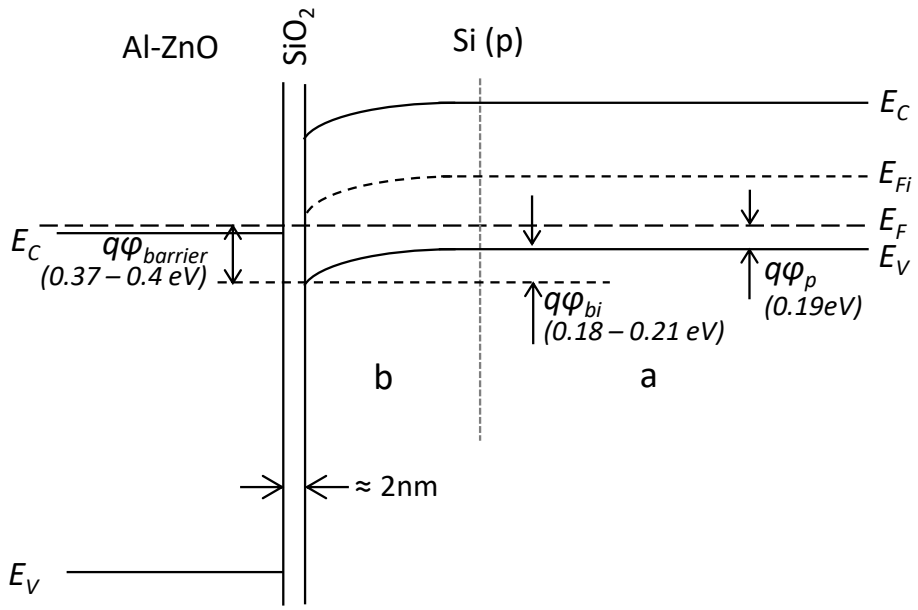


Figure 7.9 Energy band diagram of the Al-ZnO/(p)Si heterojunction under equilibrium. a) quasi-neutral region, b) depletion region.

In the next sections we further analyze and validate the energy band diagrams for both heterojunction structures by studying their I-V behavior under different intensities of full spectrum illumination.

7.3.2 Full Spectrum (White Light) Illuminated I-V Analysis

7.3.2.1 I-V Characteristics of Al-ZnO/(n)Si Heterojunction under Full Spectrum Illumination

To investigate the photo-response of the Al-ZnO/(n)Si structure, I-V measurements were performed under different intensities of illumination, up to 100 mW/cm^2 (AM1.5, standard spectrum distribution). The results for 4 different illumination levels are shown in Fig. 7.10 along with the dark I-V plot. All the curves meet at a forward bias point of ≈ 0.28 V indicating that the reverse photoresponse disappears at this bias voltage. For 100 mW/cm^2 illumination, the reverse photocurrent increases gradually from 0.28 V to -0.1 V, saturates at around -0.1 V, and stabilizes at stronger reverse biases. The lower the illumination intensity, the lower is the reverse bias required to reach the saturation photocurrent.

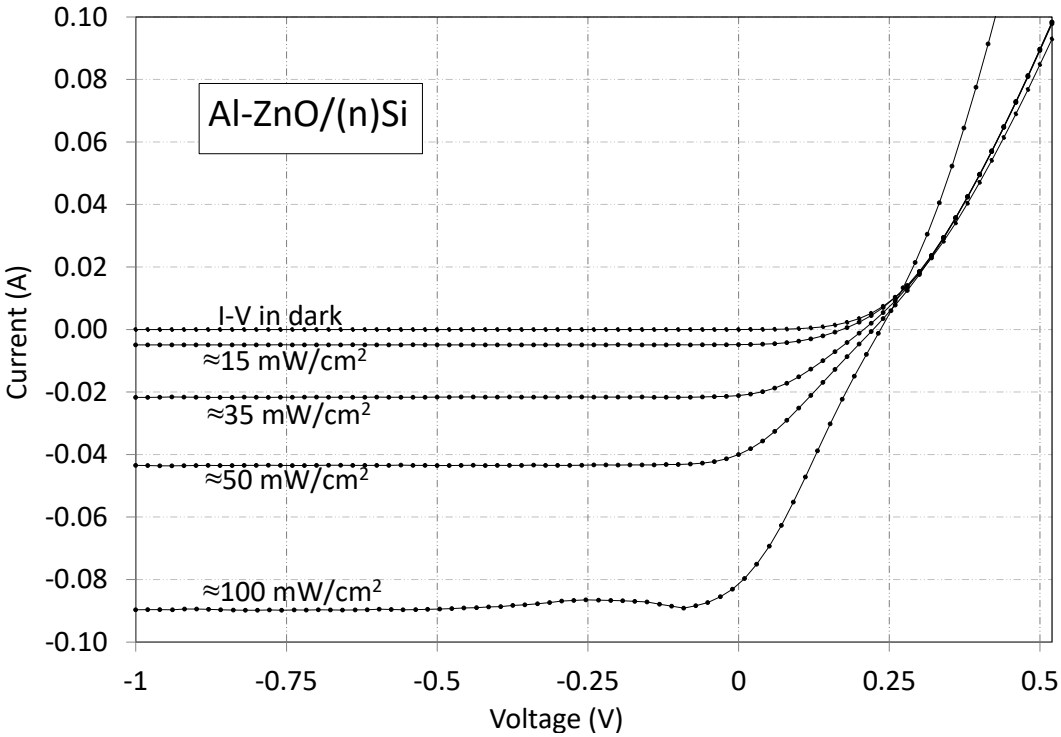


Figure 7.10 Measured I-V characteristics of the Al-ZnO/(n)Si heterojunction device in the dark and under different full-spectrum illumination intensities.

7.3.2.2 I-V Characteristics of Al-ZnO/(p)Si Heterojunction under Full Spectrum Illumination

Fig. 7.11 shows full spectrum illuminated I-V characterization for the Al-ZnO/(p)Si heterojunction. Again, all curves meet at a same forward bias point as the Al-ZnO/(n)Si case, but with a different bias of ≈ 0.15 V. For 100 mW/cm^2 illumination the reverse photocurrent (total current minus dark current) reaches saturation at around -0.5 V and almost no increases thereafter. As in the previous (n)Si case, smaller reverse voltages are required to reach maximum photocurrent with lower illumination intensities.

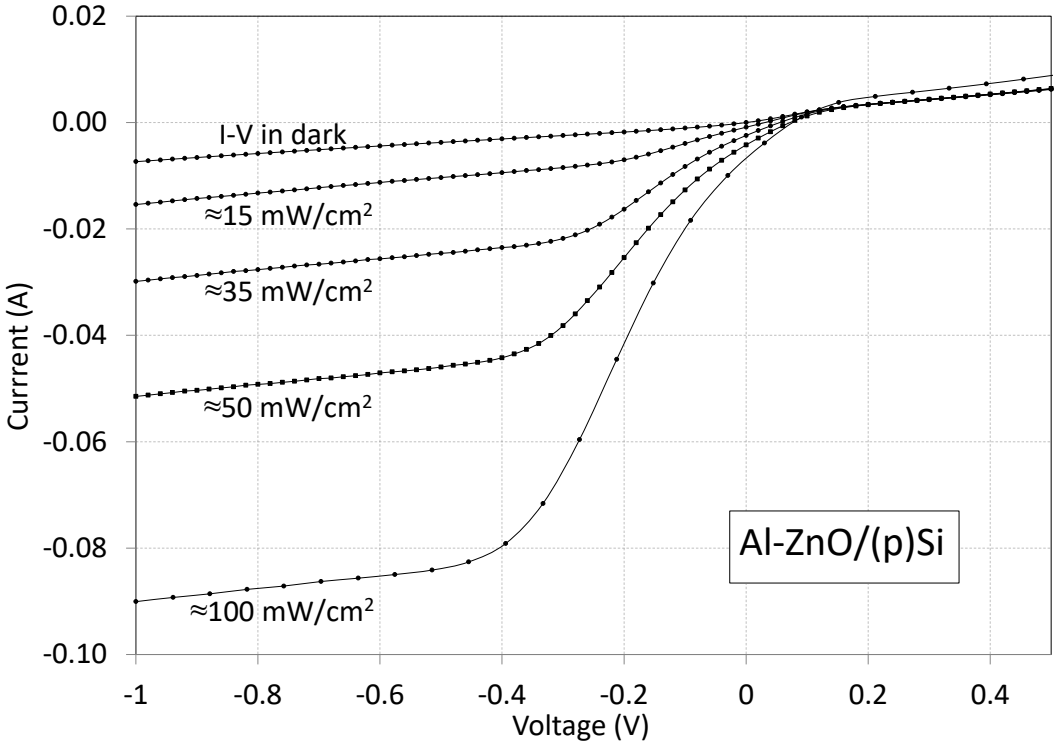


Figure 7.11 Measured I-V characteristics of the Al-Zn(O)/(p)Si heterojunction device in the dark and under different full-spectrum illumination intensities.

7.3.3 Discussion on Photoresponse Mechanism

The energy band diagrams of the heterojunctions and the full-spectrum I-V characteristics presented in the previous sections are used to establish the photoresponse mechanisms of the Al-ZnO/Si heterojunction structures.

Since the bandgap of the Al-ZnO film is large, photons in the visible range are primarily absorbed in the Si substrate and therefore, electron-hole pairs (EHPs) are mainly generated inside the Si substrate. Following the EHP generation, the competing mechanism for photocurrent is recombination. Recombination is governed by minority carrier lifetime. Therefore, unlike the dark current of the Schottky diode, photocurrent mainly depends on minority carriers.

In the example of Al-ZnO/(n)Si heterojunction, reverse photocurrent in illuminated I-V indicates minority holes flow from (n)Si to Al-ZnO. Under no-bias, the inversion and depletion layers (regions c and b in Fig. 7.7) are the only driving forces that maintain a current in this direction. As such, the existence of the inversion and/or depletion layer is essential for reverse photocurrent generation. From measurements taken across different bias voltage conditions, it is obvious that the magnitude of reverse

photocurrent is co-relative to the strength of the inversion and/or depletion layer. Additionally, as shown in the energy band diagram (Fig. 7.7), a large barrier exists between valence bands of Si and Al-ZnO. Therefore, the only possibility of collecting photo-generated holes on the Al-ZnO side requires a process in which the electrons in the Al-ZnO pass through the heterojunction, reach the valence band of Si and recombine with holes there. This mechanism is the same as a "metal-semiconductor (p-type)" interface.

Similar to Al-ZnO/(n)Si, the photoresponse of Al-ZnO/(p)Si heterojunction is attributed to the energy band bending at the hetero-interface and relies on the existence of a Si inversion and/or depletion layer. However, unlike the Al-ZnO/(n)Si, there is no naturally formed inversion layer at the Al-ZnO/(p)Si interface, only a shallow depletion layer exists in the energy band diagram (region b in Fig. 7.9). Therefore, the photocurrent at no-bias is rather small. However, as reverse bias voltage is increased, the photocurrent increases and saturates at a certain value as the depletion region is enhanced and stabilized.

7.3.4 Quantum Efficiency Analysis with Voltage Bias

While the full-spectrum illuminated I-V provides information on photoresponse characteristics, it does not directly link the underlying physics of photoresponse to the measurement results, because there are still some factors affecting the measurement, such as series and shunt resistances, carrier absorption, and Auger recombination in high injection, etc. Hence, external quantum efficiency (EQE) analysis with applied voltage bias is performed to further understand the photoresponse of the heterojunction. In the EQE analysis, monochromatic light at a specific wavelength is applied to the device, and measurements are done covering wavelengths ranging from 300 nm to 1100 nm. Each time the device is kept under different voltage bias to investigate the role of the inversion and/or depletion layer. A schematic of the measurement setup is shown in Fig. 7.12. Although EQE is typically presented as a positive percentage, since we included bias voltage in our experiments, in this work we denote EQE as "positive" and "negative" quantities to represent the direction of the photocurrent.

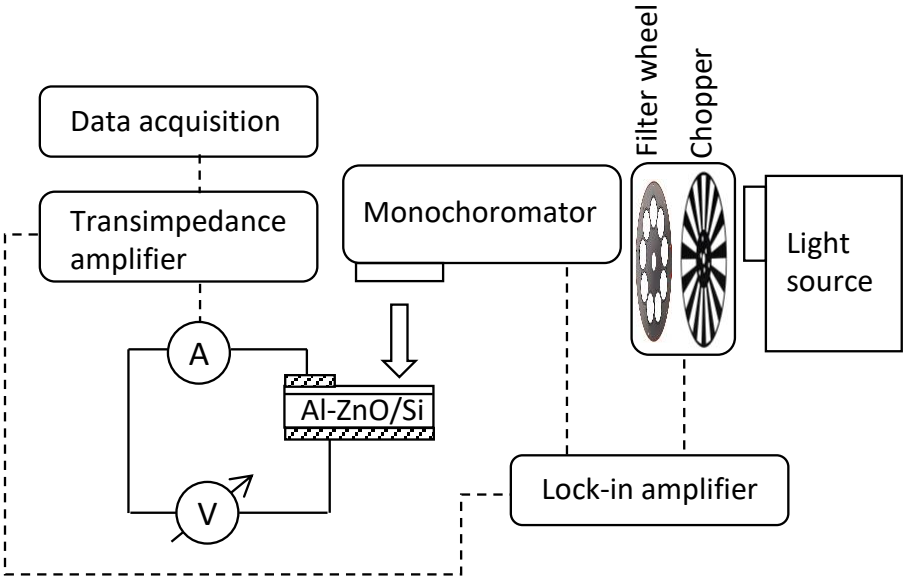
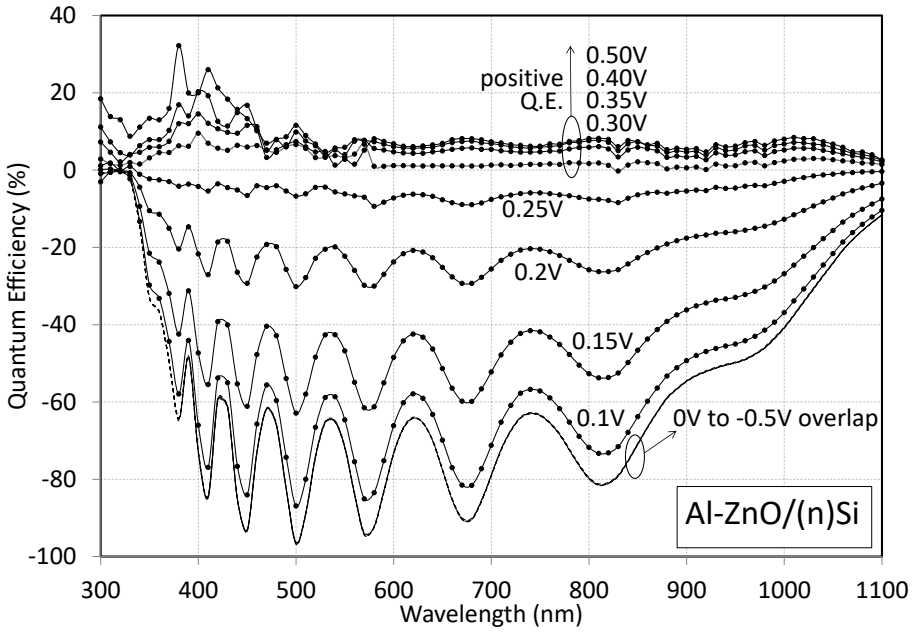


Figure 7.12 Schematic diagram of quantum efficiency measurement setup with applied voltage bias.

7.3.4.1 Quantum Efficiency Characterization of Al-ZnO/(n)Si Heterojunction with Applied Voltage Bias

Fig. 7.13 shows the EQE of Al-ZnO/(n)Si heterojunction at different voltage biases. Some of the lines are overlapped with each other, so a 3-D surface graph is also presented to illustrate the external quantum efficiency change with voltage bias.



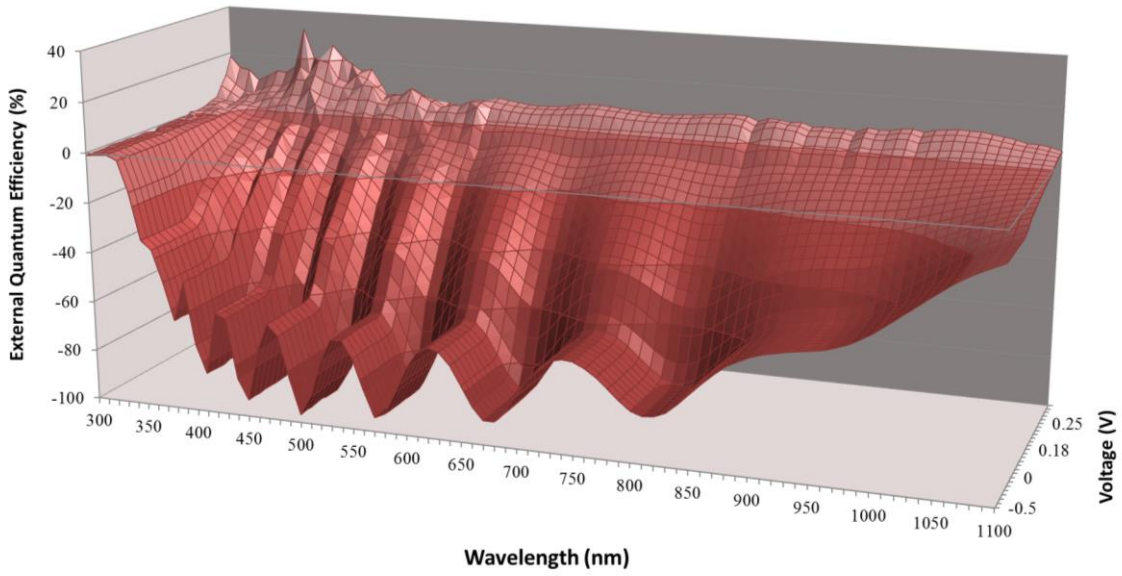


Figure 7.13 Measured EQE of the Al-ZnO/(n)Si heterojunction device under different bias voltages.

The wave-like pattern of the EQE curves is due to reflection (optical loss) at the front surface of the device. The shown QE behavior can be discussed in three different bias ranges:

(i) First, from 0 to -0.5 V reverse bias, the EQE curves stay unchanged. The EQE is fairly high under these bias conditions, comparable to Si solar cells. At 500nm the EQE is nearly 100%. The relatively low quantum yield below 350nm is due to absorption in the Al-ZnO film.

(ii) Second, from 0 to 0.25 V forward bias, the EQE drops drastically across all wavelengths. This indicates that the inversion layer becoming balanced by the forward bias and hence the photoresponse mechanism is weakened.

(iii) Third, 0.3 V forward bias and above, the EQE turns to the forward direction. Reverse photocurrent disappears because, under forward bias, after the disappearance of the inversion layer, the device structure is equivalent to Al-ZnO/(n+)Si/(n)Si. Thus, there is no inversion and/or depletion layer to assist the holes to reach the contact on the Al-ZnO side. In fact, holes are repelled from the hetero-interface resulting in the reverse photocurrent completely disappearing at high forward bias voltage. At the same time, forward photocurrent begins to rise.

Forward photocurrent can be generated via four mechanisms:

(i) the minority holes can travel through bulk Si and reach rear contact without recombining and therefore contributing to forward photocurrent. However, the occurrence of this minority-carrier-induced forward photocurrent is very limited due to the low lifetime of minority carriers. This mechanism is more visible in the long λ region (950 to 1100 nm), as the low energy photons are absorbed closer to the rear surface, providing the generated holes with a shorter path before being collected by the rear contact. A non-ohmic rear contact (e.g. a Schottky barrier) can further enhance this mechanism;

(ii) some majority electrons which originally do not have enough energy to cross the heterojunction can be stimulated by photons and become another source of forward photocurrent,

(iii) with the aid of high energy (short λ) photons, photogenerated electrons in the conduction band of (n)Si may acquire enough energy to cross the barrier at Al-ZnO/(n)Si interface to form forward photocurrent. The possibilities of the above 3 mechanisms are rather small and hence the forward photocurrent has a relatively low absolute value.

(iv) There is also a fourth mechanism where photons with energy higher than the bandgap of Al-ZnO are absorbed in the film and can generate free electrons which, under the forward bias, can contribute to forward photocurrent. This effect was observed in [96].

If the Al-ZnO/(n)Si heterojunction is used to function as a solar cell, the aforementioned forward photocurrent generation mechanisms will contribute as shunt current affecting fill-factor (FF) and open circuit voltage (V_{oc}). Minimizing these mechanisms is essential to improve the device performance. For instance, a proper tunneling interfacial layer can reduce the majority carrier thermionic-emission current (dark current and forward photocurrent through the second and third mechanisms), therefore reduce shunt current and improve V_{oc}.

7.3.4.2 Quantum Efficiency Characterization of Al-ZnO/(p)Si Heterojunction with Applied Voltage Bias

Fig. 7.14 shows the EQE of Al-ZnO/(p)Si heterojunction at different voltage biases.

In the same way as in the previous section, the EQE of Al-ZnO/(p)Si can also be discussed in three different bias ranges but with different values:

(i) First, -0.25 V reverse bias and below, the EQE curves stay unchanged, yielding reasonably high values. The EQE values are lower compared to the (n)Si case in the long λ region, and this is mainly due to the differences in doping concentrations and minority carrier lifetimes of the (n) and (p) Si materials.

(ii) Second, from -0.25V reverse bias to 0.1 V forward bias, the EQE drops significantly nearly reaching zero. This is because the depletion layer becomes weaker and eventually disappears due to external voltage bias.

(iii) Third, above 0.1 V forward bias, EQE changes to "forward" direction, and very low photoresponse is observed due to lack of driving force for carrier collection. The bump from 950 - 1100 nm shows a non-perfect rear contact as discussed in the first forward photocurrent mechanism.

In the Al-ZnO/(p)Si heterojunction structure, the electrons in Al-ZnO are the carriers that need to get through the hetero-interface to form forward current, not the majority holes in Si. So the second and third forward photocurrent mechanisms discussed in the previous section are not applicable for Al-ZnO/(p)Si. Therefore, the forward photocurrent measured for Al-ZnO/(p)Si is much lower than that of the (n)Si case.

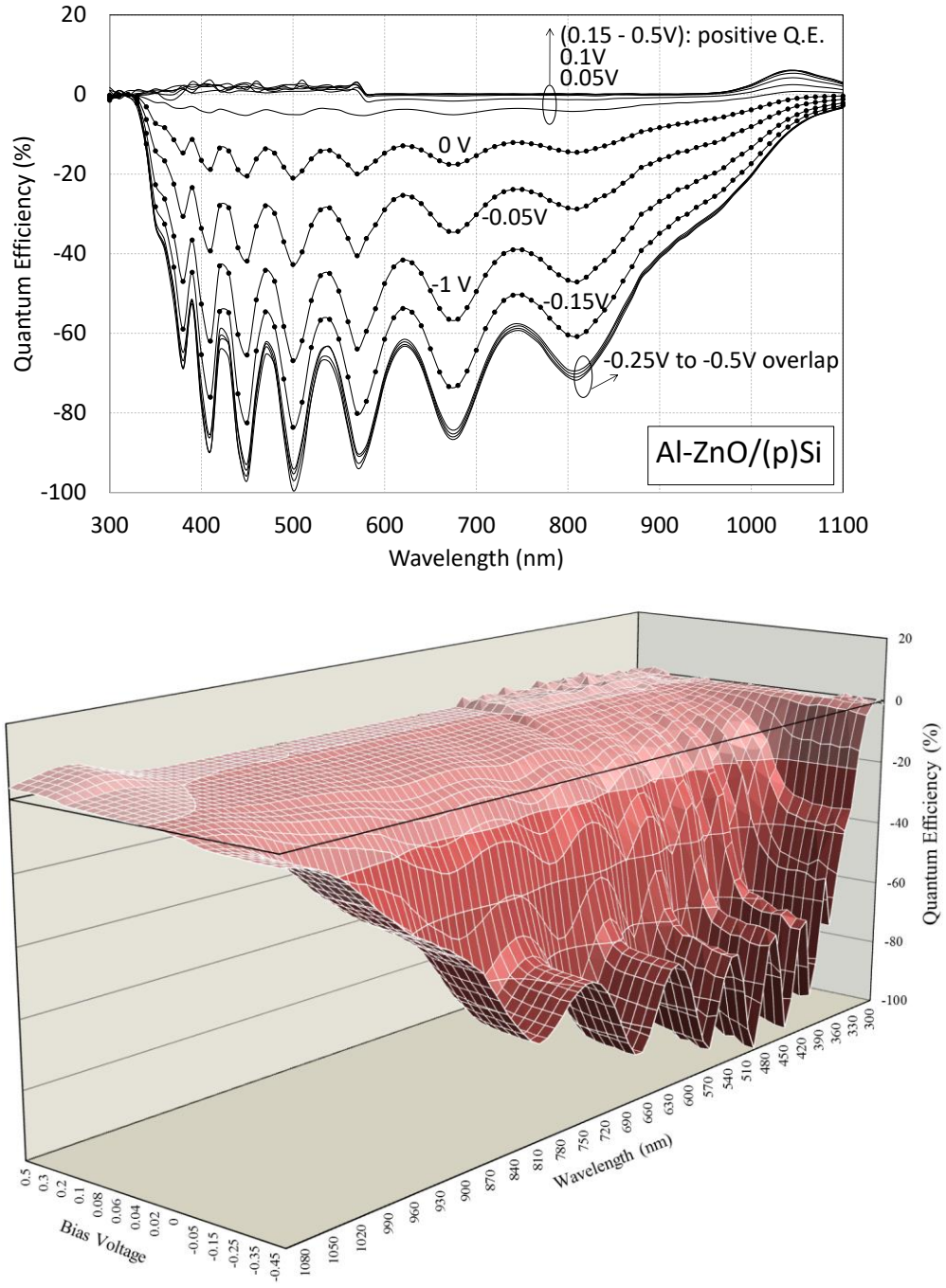


Figure 7.14 Measured EQE of the Al-ZnO/(p)Si heterojunction device under different bias voltages.

The boundaries of the three regions observed in biased QE measurements are similar to the results obtained from full spectrum illuminated I-V measurements. These three regions can be summarized as the inversion and/or depletion layer, **(1) being absent, (2) building-up, and (3) stabilized regions.** The transition points between region (1) and (2) are almost identical for the biased-QE measurement and full spectrum illuminated I-V measurements (0.28 V and 0.1 V for Al-ZnO/(n)Si and Al-ZnO/(p)Si,

respectively). However, transition between region (2) and (3) occurred at higher reverse bias values for the full spectrum I-V than for the biased QE measurement. This is because in the full-spectrum I-V measurements the devices operate under high injection conditions making factors such as free carrier absorption, shunt, and Auger recombination more profound. Accordingly, the heterojunction devices require a higher voltage bias to establish a stable inversion and/or depletion layer for collection of photogenerated carriers.

7.3.5 Photoresponse Analysis Summary for Al-ZnO/Si Devices

Different from that of most p/n or p/i/n junction photodetectors and solar cells, the photogenerated current of Al-ZnO/Si hetero-structures exhibits significant dependence on bias voltage, and a forward photocurrent is observed. Therefore, the unique feature of photogenerated current behavior in Al-ZnO/Si hetero-structures is worth studying for novel optoelectronics. For example, the forth forward photocurrent mechanism can enable the possibility of UV detection and visible wavelength detection with the same device by two different operation modes, as observed in [96].

Based on the photoresponse mechanism discussion, one can summarize that there are three regimes for the inversion and/or depletion layer at Al-ZnO and Si interface: (1) absent, (2) building-up, and (3) stabilized. These three regimes govern the photoresponse of Al-ZnO/Si devices. Qualitatively, below a certain bias voltage, in "stabilized" regime, photogenerated current should be close to constant; within certain bias voltage range, in "building-up" regime, photogenerated current should decrease and reach zero eventually; above the voltage of zero photocurrent, in "absent" regime, forward photocurrent should rise and stabilize eventually. Therefore, for the first time, a general model to describe the photogenerated current density behaviors of both Al-ZnO/(n)Si and Al-ZnO/(p)Si hetero-structures can be put forward for future Al-ZnO/Si device development. Moreover, the same model may also apply to similarly structured devices such as "pinned" MIS solar cells [97], ITO-Si heterojunction detectors [98], etc.

We first define two voltage points, V_{SAT} and V_{ABS} that separate the three intervals: V_{SAT} is the voltage bias below which the photocurrent becomes saturated at a certain value; at V_{ABS} the total photocurrent equals zero, i.e., depletion region is absent. And then we

define constants, J_{SAT} (>0) and J_{ABS} (<0), which are maximum photocurrents at given illumination intensity under reverse and forward bias respectively. Finally, consider there exists a strictly decreasing function *f(V)* such that $0 \leq f(V) \leq 1$ for $V_{SAT} \leq V \leq V_{ABS}$, and an increasing (not necessarily strict) function *g(V)* such that $0 < g(V) \leq 1$ for $V > V_{ABS}$. Therefore, the output current, J_{out}, and the photogenerated current, $J_L(V)$, for the Al-ZnO/Si heterojunction can now be expressed as follows:

$$J_{out} = J_{dark}(V) - J_L(V) \tag{3}$$

$$J_L(V) = \begin{cases} J_{SAT}\,, & V < V_{SAT}\,; \\ J_{SAT} \cdot f(V)\,, & V_{sat} \leq V \leq V_{ABS}\,; \\ J_{ABS} \cdot g(V)\,, & V > V_{ABS}\,. \end{cases} \tag{4}$$

Notably, because they are based on different mechanisms, reverse and forward photocurrents could co-exist at certain bias voltages (as shown in EQE of Al-ZnO/(n)Si at 0.28 V in Fig. 7.13). However, they are not formulated separately in this model. Equation (4) actually describes the sum of the two currents, which can be experimentally confirmed with device-level measurements. The function *f(V)* is determined by interface properties such as density of states, dielectric constant and surface recombination velocities, all of which can be subject to the carrier collection probability. As multiple components can affect forward photocurrent, the function *g(V)* will differ from device to device.

In this model, V_{SAT} represents the minimum bias voltage required for maximum photoresponse. Also, it is an indication of the strength of the inversion and/or depletion layer at the interface. V_{ABS} represents the bias voltage point where device photocurrent changes polarity. This is also where the device switches to a different operation mode. The absolute value, $|J_{SAT}|$ and $|J_{ABS}|$ indicate the photoresponse capabilities at reverse and forward bias conditions, respectively. *f(V)* expresses the sensitivity of the inversion and/or depletion layer to external bias. By analyzing the experimental results of future devices based on this model, these key parameters can be extracted and therefore represent the properties of the devices.

To further illustrate the function of the model, we integrate each curve in Fig. 7.13 and Fig. 7.14 with respect to the standard AM1.5 illumination (100 mW/cm^2) spectrum. Each of the integrations will generate a data point of photogenerated current density,

$J_L(V)$, at respective bias voltage. And then we plot all the generated data points in a graph of $J_L(V)$ vs. voltage, as shown in Fig. 7.15. The approximate voltage points of V_{SAT}-n, V_{ABS}-n and V_{SAT}-p, VABS-p are labelled in the plot for Al-ZnO/(n)Si and Al-ZnO/(p)Si devices, respectively. The $J_L(V)$ behaviors of both Al-ZnO/(n)Si and Al-ZnO/(p)Si devices fit very well with the proposed model.

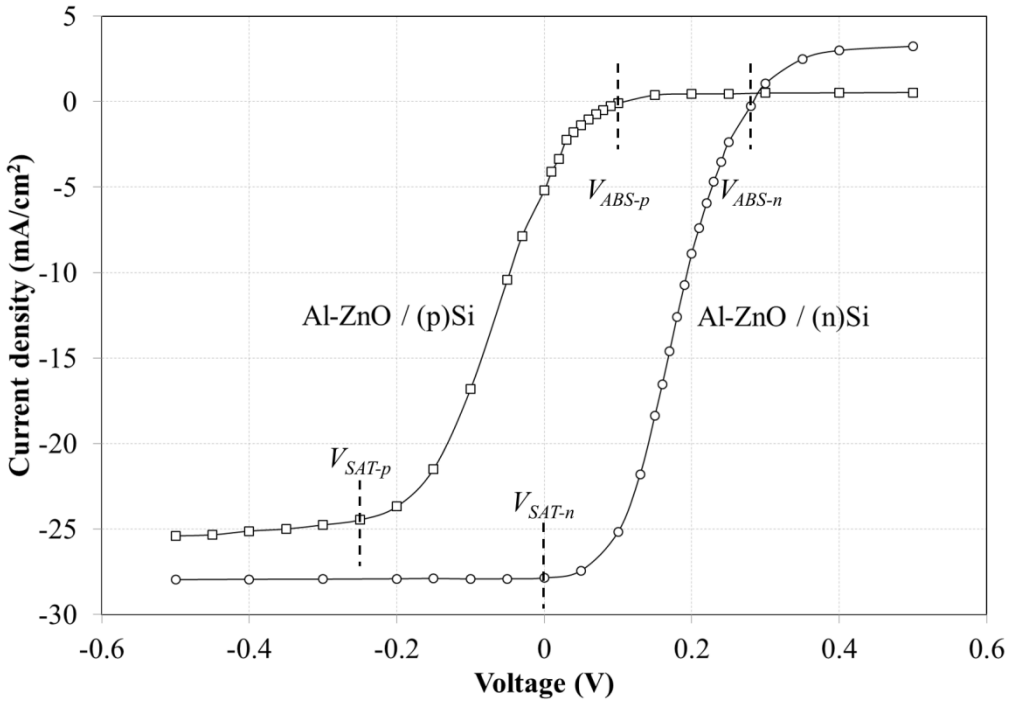


Figure 7.15 Integrated photogenerated current density of the Al-ZnO/(n)Si and the Al-ZnO/(p)Si heterojunction devices from biased EQE measurements.

7.4 Conclusions

Al-ZnO/Si heterojunction photodetectors are fabricated with both n-type and p-type substrate. Both types of devices are tested with dark I-V, illuminated I-V, biased QE measurement.

The Al-ZnO/(n)Si structure shows textbook Schottky diode behavior, while Al-ZnO/(p)Si structure does not show rectifying behavior up to 1 V. Both types of photodetectors exhibit decent photoresponse at reverse bias conditions. However, at zero bias, Al-ZnO/(n)Si maintains good photoresponse properties, while Al-ZnO/(p)Si only show very limited photoresponse capabilities.

Based on dark I-V characteristics, energy band diagrams and photoresponse properties of the devices, the photoresponse mechanisms for the Al-ZnO/Si heterojunction structures are summarized. It relies on the depletion region at the heterojunction interface.

The photoresponse mechanisms for the Al-ZnO/Si heterojunction structures are further confirmed with biased QE measurement on both types of devices. A descriptive model for the photocurrent of Al-ZnO/Si heterojunction structures is given.

CHAPTER 8

DEVELOPMENT OF ADVANCED PHOTODETECTOR BASED ON AL-ZNO/SI HETERO-JUNCTION

With the understanding of the photoresponse mechanisms of Al-ZnO/Si heterojunction structures, Al-ZnO/(n)Si heterojunction is chosen for high performance photodetector development. Two main modifications were made to "standard" Al-ZnO/(n)Si heterojunction detectors introduced above, namely:

- optimize Al-ZnO thin film thickness;
- introduce Nitric Acid Oxide layer at Al-ZnO/(n)Si heterojunction interface.

In the following discussions, example of "standard" Al-ZnO/(n)Si heterojunction detectors is labelled as Sample A, and example of the optimized high performance Al-ZnO/(n)Si heterojunction detectors is labelled as Sample B. Optical and electrical analysis results for Sample A and Sample B are demonstrated and compared.

8.1 Device Fabrication

Detailed fabrication process is described as follows: the two samples (Sample A and Sample B) were both fabricated on 500 μm thick, phosphorous doped n-type Czochralski (Cz) Si (100) wafers. The wafers were doped to roughly 4.0×10^{15} cm^{-3} with corresponding resistivity of 1.5 Ωcm. The wafers were first diced to 2.2 cm × 2.2 cm squares. After a standard RCA 1 and 2 cleaning, followed by a 30 sec HF dip,

Sample A was directly loaded into the rf-sputtering system. Meanwhile, Sample B was loaded to rf-sputtering system after immersion in 68% Nitric Acid for 15 min to obtain a thin (approximately 1.5 nm) Nitric Acid Oxide (NAO) layer [71]. Al-ZnO thin films were deposited onto both samples using the same deposition conditions with different deposition durations. Specifically, depositions occurred under a pressure of 0.5 mTorr with an RF power of 150 W at 250 °C. These conditions produced Al-ZnO films with thickness of 780 nm thickness and roughly 80 nm for Sample A and Sample B, respectively. The optical and electrical properties of the Al-ZnO films are described in detail in [83]. Briefly, this process produced highly transparent, highly conductive Al-ZnO films with carrier concentration of $1.07 \times 10^{21}\ \mathrm{cm}^{-3}$ and resistivity of $2.94 \times 10^{-4}\ \Omega\mathrm{cm}$ (at 780 nm thickness). Finally, ohmic contacts were formed on Sample A and Sample B via Al e-beam evaporation. Front contacts were formed by a shadow mask with finishing pads of 15 mm × 6 mm × 1 μm in dimension. Rear contacts were formed using blanket deposition of 1 μm Al.

8.2 Dark I-V Analysis

Fig. 8.1 shows the current-voltage characteristic of the Al-ZnO/(n)Si heterojunction in the dark. The Al-ZnO/(n)Si heterojunction shows excellent diode-like behavior, with rectification ratios of 6.7×10^3 and 2.7×10^3 at ± 0.5 V for Sample A and B respectively. The reverse current density of Sample A is 3.3×10^{-6} A/cm^{-2} at -0.5 V. Sample B exhibits a reverse current density almost one order of magnitude lower: 4.5×10^{-7} A/cm^{-2} at -0.5 V. This improvement is attributed to the implementation of NAO layer. Notably, the reverse currents were measured from rather large area devices (4.84 cm^2). Reverse dark current indicates the noise level of photodetector; therefore, scaled-down, smaller-sized devices, which would show even smaller reverse dark current values, are promising for low noise photodetectors. The higher resistance of Sample B under forward bias is attributed to its much thinner Al-ZnO layer and the tunneling process of majority carriers through NAO layer. However, photodetectors usually operate under reverse bias or photovoltaic mode, so the high resistance under forward bias is not a major concern for device performance. Furthermore, high bias resistance can be easily mitigated by optimizing the pattern of the front electrode and reducing device area.

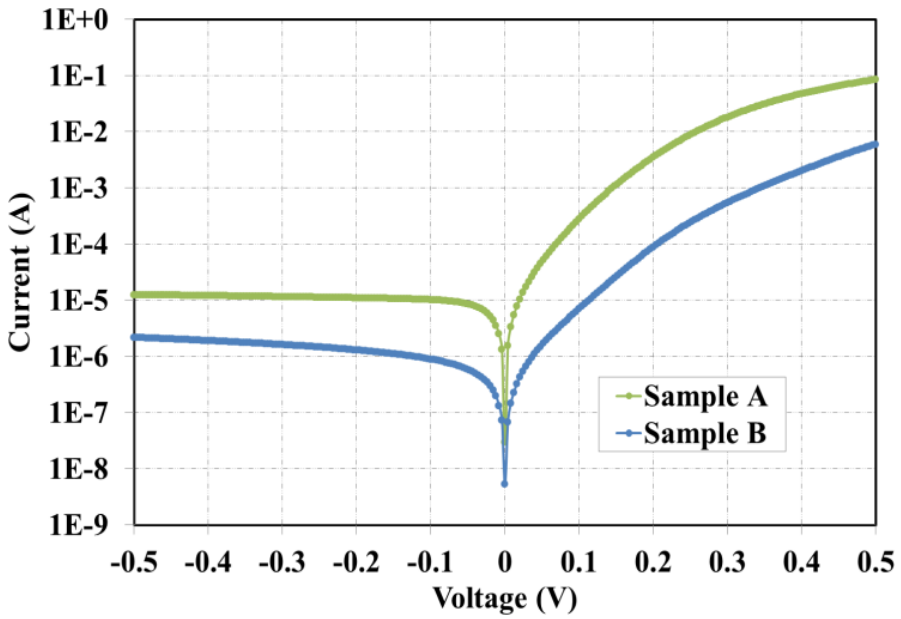


Figure 8.1 Dark IV characteristics of Sample A and Sample B

8.3 Reflection and Spectral Response Analysis

Surface reflection plays an important role in the EQE performance and responsivity of a photodetector. Fig. 8.2 presents the surface reflection results of Sample A and B, alongside the reflection results of a polished Si wafer (i.e. starting point of Sample A and B) for comparison. Due to thin film interference, the reflection of Sample A exhibits wave-like behavior between the 300 nm to 1100 nm wavelengths. By optimizing the thickness of the Al-ZnO film in Sample B, undesirable interference is disturbed. Moreover, the thickness of the Al-ZnO film is selected based on its refractive index (approximately 1.88 at 600 nm). Therefore, in this specific example, the Al-ZnO film in Sample B serves as an excellent ARC to minimize reflection at approximately 600 nm. Sample B achieved a reflection value below 5% between 540 nm and 750 nm. The reflection across most of the visible light wavelengths (490 nm to 960 nm) was below 15%. With proper substrate (Si) or thin film (Al-ZnO) texturing, the reflection of Al-ZnO/(n)Si heterojunction photodetector can be further improved [38, 55, 99].

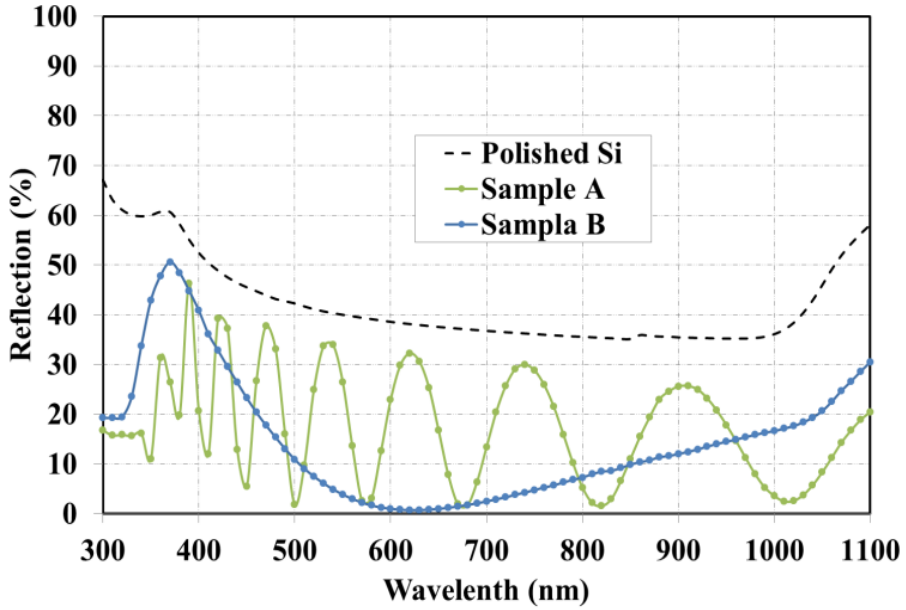


Figure 8.2 Reflection of polished Si, Sample A and Sample B

Fig. 8.3 presents the spectral response of Sample A and B without light bias or voltage bias at room temperature. The inset shows the corresponding responsivity of Sample A and B, together with the theoretical limit of responsivity (EQE=100%) for visible light broadband detectors.

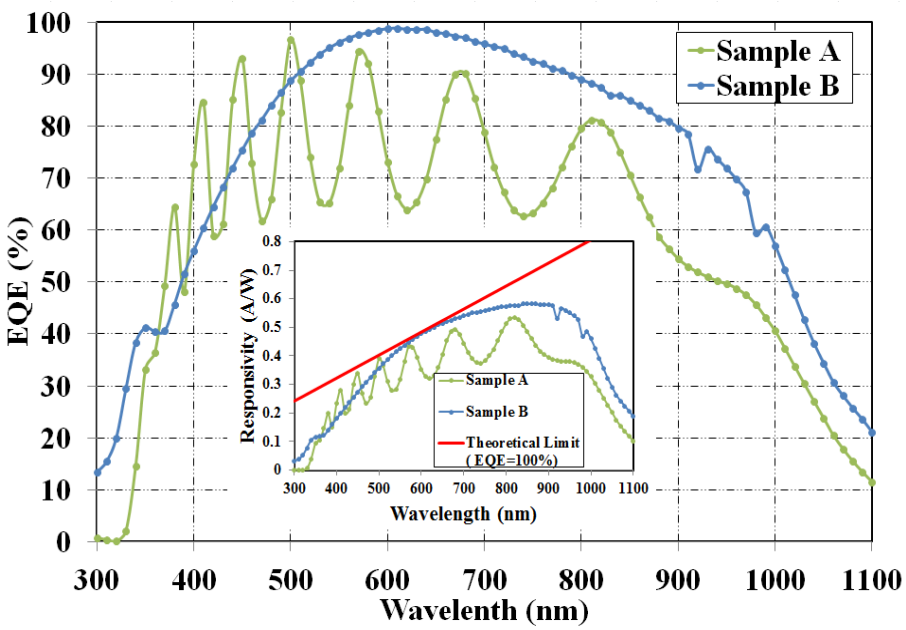


Figure 8.3 EQE and responsivity results of Sample A and Sample B

It is obvious that Sample B has a superior performance than Sample A for most of visible range wavelengths. Notably, the highest EQE of 98.8% is achieved at 600 nm and 610 nm; this is the record EQE reported so far among similarly structured devices.

The equivalent responsivity values are 0.478 A/W and 0.486 A/W for 600 nm and 610 nm, respectively. The EQE of Sample B is above 80% from 470 nm to 890 nm, which is comparable to high performance silicon p-n or p-i-n junction photodetectors. Considering the simple and low temperature fabrication processes of the Al-ZnO/(n)Si heterojunction photodetector presented here, it has great potential as a substitute for silicon p-n or p-i-n junction photodetectors for certain applications. Given the substrate thickness (500 µm) and untreated rear surface of the samples, EQE results of Sample B at infrared regions are also very impressive. Moreover, the infrared response can be further improved using simple processes such as the addition of an n+ surface field, nitride or oxide passivation [100-102]. It should be noted that the EQE of Sample B peaks at 600 nm because the Al-ZnO thickness is designed to minimize the reflection at this wavelength. Therefore, the maximum EQE can be tuned by adjusting the Al-ZnO film thickness.

As discussed above, the fringes and peaks of the EQE curves for Sample A and B result from surface reflection. To reveal the strength and capability of the internal field of Sample A and B for photo-generated carrier collection, Fig. 8.4 presents the IQE calculated by eliminating surface reflection (based on data of Fig. 8.2 and Fig. 8.3).

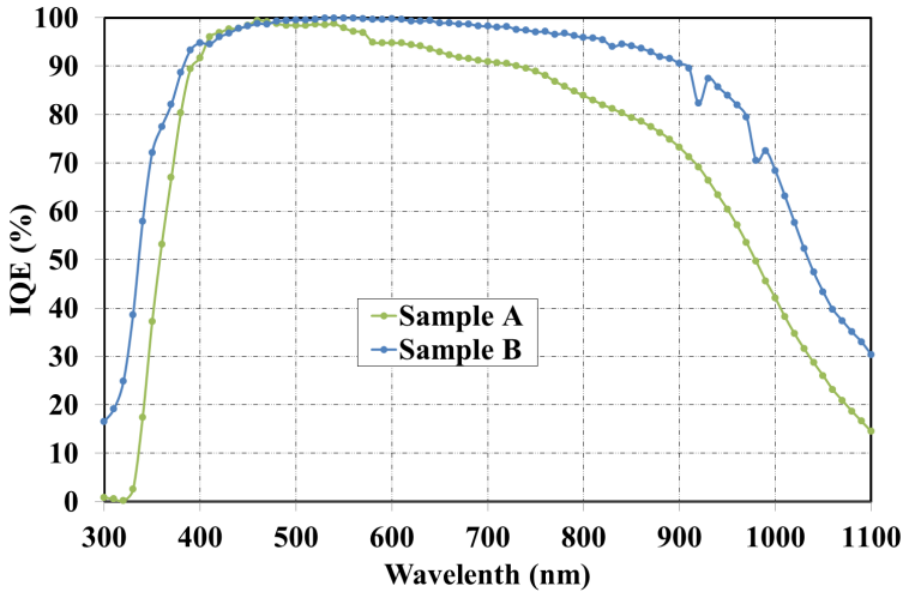


Figure 8.4 Internal quantum efficiency results of Sample A and B

The IQE of Sample B is above 90% from 390 nm to 900 nm; within the range of 420 nm to 820 nm the IQE is greater than 95%. This excellent IQE indicates a robust internal

depletion region at the Al-ZnO and (n)Si interface. Compared to Sample A, the IQE of Sample B shows improvement across almost the entire spectral region of 300 nm to 1100 nm. This clearly shows that the NAO layer is beneficial for strengthening the internal field and harvesting photo-generated carriers.

8.4 Modulated Signal Response of Al-ZnO/(n)Si Photodetector in Photovoltaic Mode

In order to demonstrate their capability for high speed detection, the Al-ZnO/(n)Si heterojunction detectors were examined under illumination of a 1 kHz optical signal in a breadboard-based simple circuit at room temperature. The schematic diagram of the experiment setup is shown in Fig. 8.5 Specifically, a 1 kHz square wave was generated with a waveform generator (Agilent 33120A); illumination was applied using a 650 nm red LED (L10881 from Hamamatsu Photonics), positioned 5 cm above the photodetector under test at normal incidence; voltage signals across the LED (Channel 1) and the load resistor (Channel 2) were collected by a dual channel oscilloscope (Analog Discovery portable analog circuit design kit); a 0.01 µF capacitor was placed in parallel with load resistor to cancel high frequency noise from the circuit.

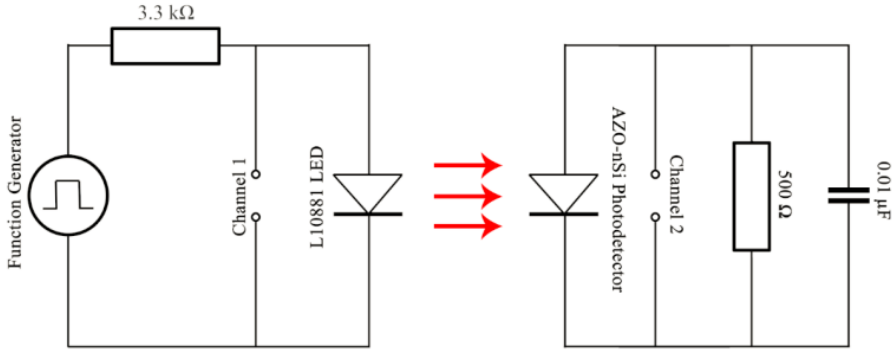


Figure 8.5 Schematic circuit diagram of modulated optical signal response analysis of Al-ZnO/(n)Si heterojunction photodetectors

Fig. 8.6 (a) and (b) show the signal response of photodetector A and B, respectively. Both photodetectors exhibited great synchronization with input optical signal at 1 kHz. The rise time (τ_r) and fall time (τ_f) are defined as time required to change from 10% to 90% and from 90% to 10% of peak output value, respectively. τ_r and τ_f of Sample A

were 100 µs and 140 µs, respectively. τ_r and τ_f of Sample B showed profound improvement to 75 µs and 75 µs (75% and 54% of Sample A), respectively.

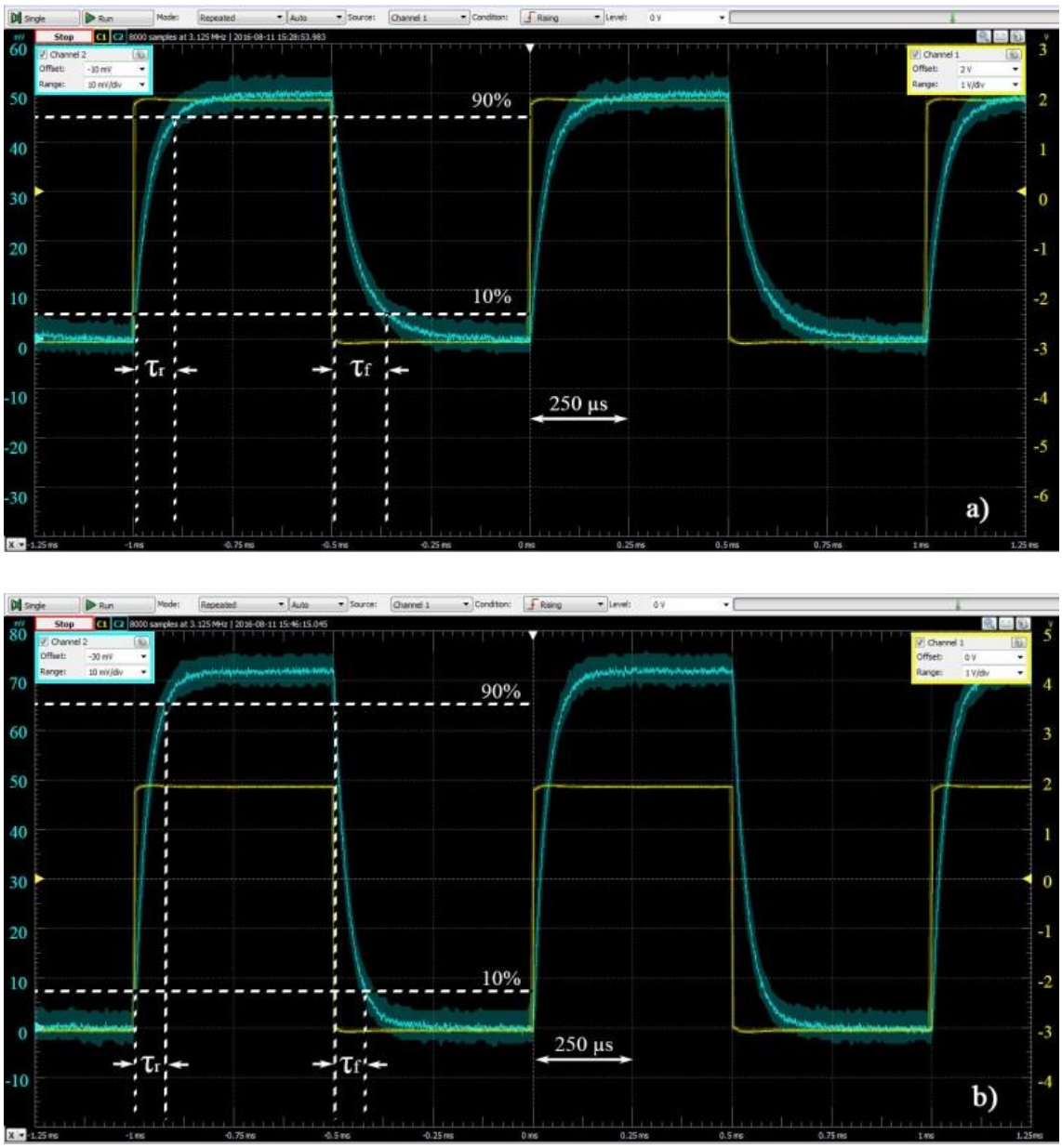


Figure 8.6 Modulated optical signal response of Sample A and Sample B

This is the first report of an Al-ZnO/(n)Si heterojunction photodetector operating with modulated optical signal. Moreover, it is believed that the present signal response is limited by the un-optimized proof-of-concept circuit. The operation of an Al-ZnO/(n)Si broadband photodetector in an optimized high frequency circuit is a promising future work.

8.5 Switching of Al-ZnO/(n)Si Heterojunction

As mentioned above, Al-ZnO/Si heterojunction is Schottky-like junction. Therefore, this structure possesses the advantage of high switching speed. Currently, the detectors fabricated are several orders of magnitude bigger than the size of typical high speed switching diodes [25]. Detector capacitance is directly related to the device area, therefore, the detectors fabricated so far are not suitable for high frequency operation. However, switching test for the over-sized devices can still provide meaningful observations for the device characteristics. Fig. 8.7 shows the schematic circuit diagram of the switching test. A load resistor as small as 1 Ω is implemented.

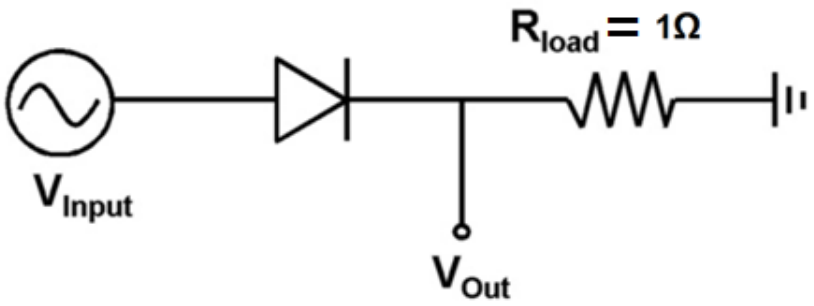


Figure 8.7 Modulated optical signal response of Sample A and Sample B

The switching test is performed with input sinusoidal waveform. Selected signal frequency are 1 kHz, 5 kHz and 10 kHz. The test results are presented in Fig. 8.8.

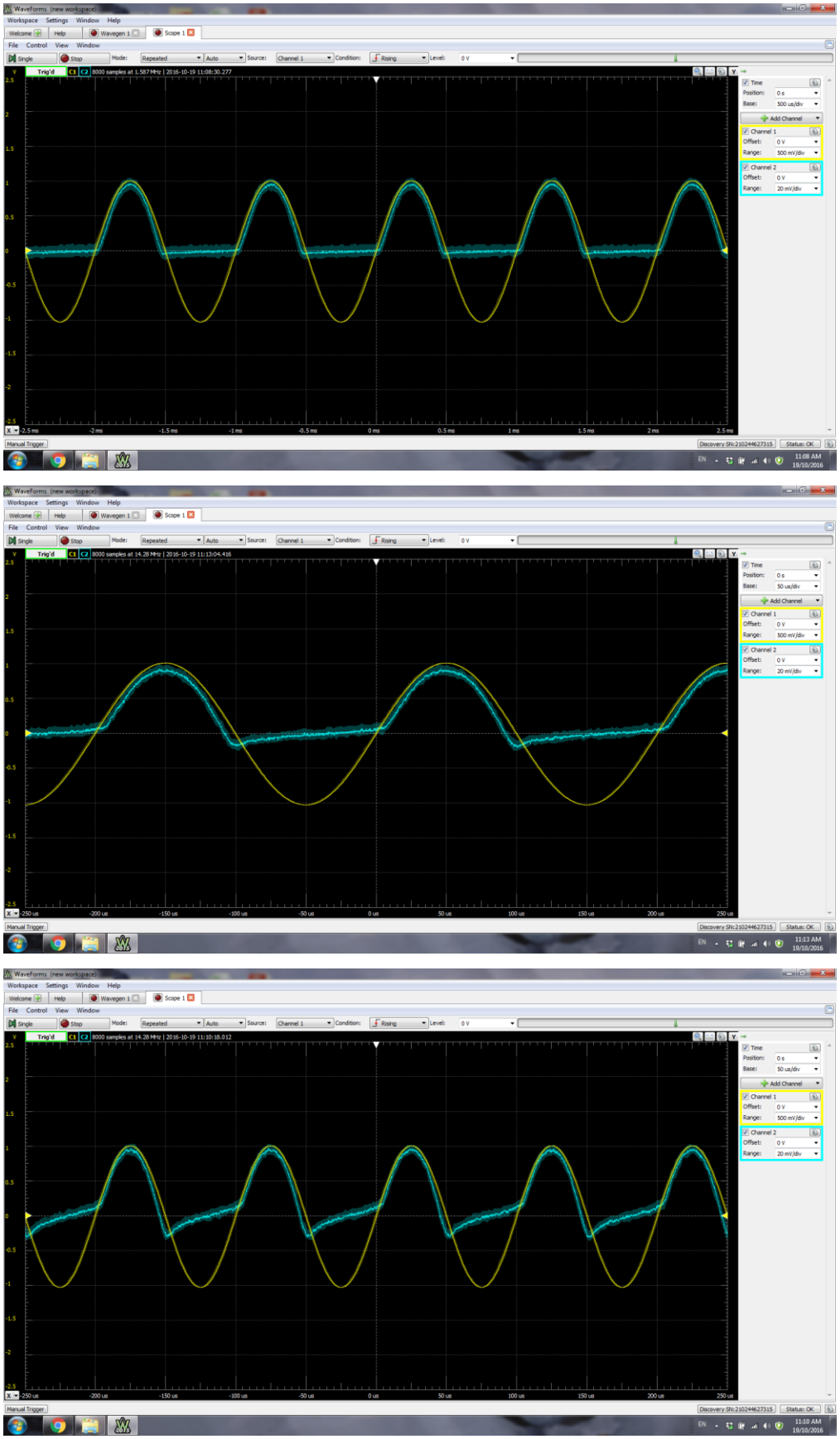


Figure 8.8 Switching test results on Al-ZnO/(n)Si photodiode at 1 kHz (top), 5 kHz (mid) and 10 kHz (bot).

At 1 kHz, the Al-ZnO/Si photodiode can almost perfectly rectify the input sinusoidal signal. The result demonstrates the Al-ZnO/Si heterojunction is capable of 1 kHz switching at the area of ~5 cm^2. Internal resistance and junction capacitance are two important parameters for diodes to operate in high frequency circuits. From the switching test results, the rectification can be observed even with a load resistor as small as 1 Ω. That means the internal resistance of the photodiode is rather small. If the capacitance value of the photodiode was brought lower by scaled-down devices, the total parasitic RC value of the photodiode would be small enough for high frequency operation. A small signal distortion can be observed at 5 kHz. At 10 kHz, a relatively large distortion presents in the output waveform.

8.6 Micro-Plasma Emission Spectrum Measurement with Al-ZnO/(n)Si Heterojunction Photodetector

--- Collaboration Project with Prof. Vassili Karanassios

Prof. Vassili Karanassios has been developing battery-operated micro-plasma for on-site use and for the "taking part of the lab to sample" types of chemical analysis applications [103,104]. In such systems, a micro-sample is introduced to the micro-plasma and the emission spectrum is measured to identify the composition of the micro-sample. Therefore, a self-powered high performance photodetector is desired for on-site systems. The main task in the collaboration is to evaluate the responsivity and capability of the Al-ZnO/(n)Si photodetector in respect to the micro-plasma emission spectrums. The schematic diagram of the micro-plasma system and responsivity measurement setup is presented in Fig. 8.9 [105].

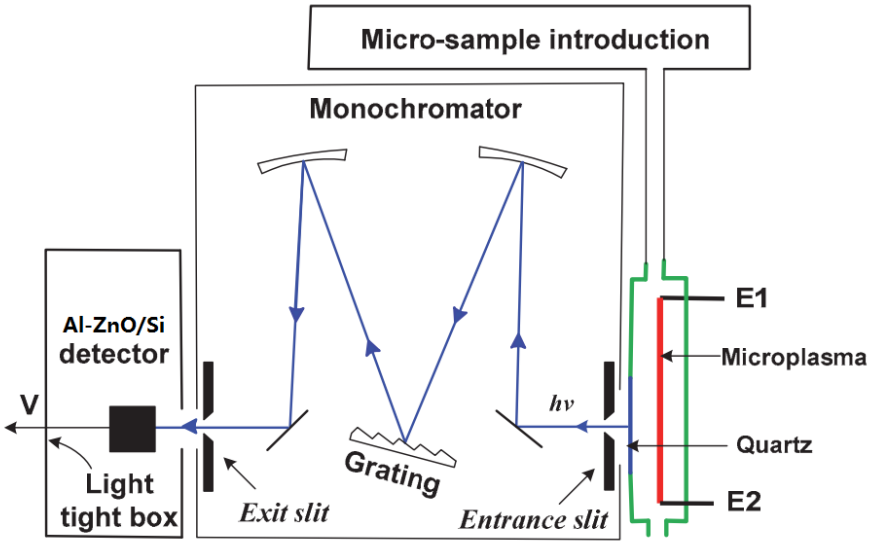


Figure 8.9 Schematic diagram of micro-plasma system and responsivity measurement setup

8.6.1 Neon Gas Micro-Plasma Emission Spectrum Measurement

Neon gas has peak clusters at visible wavelength range when introduced to micro-plasma systems. It is favoured to confirm the capability of a detector at visible wavelength range. Therefore, a series responsivity tests on micro-plasma with Ne gas is performed. Two sets of systems were used to measure the emission spectrum and the measurement results were compared.

On one hand, the emission spectrum is measured by optical fiber connected to commercial spectrometer system (EPP2000, StellarNet Inc.) with 2048 pixel UV enhanced CCD detector. The measurement result is presented in Fig. 8.10.

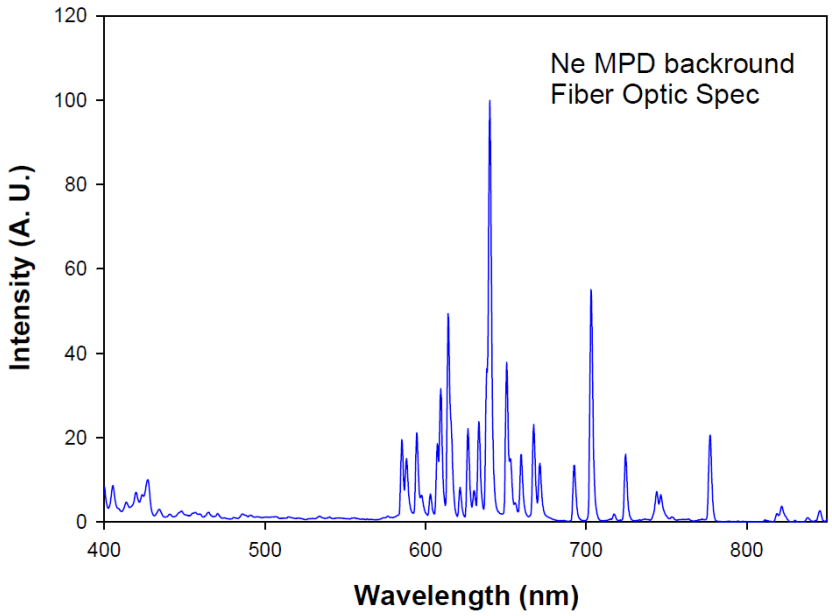


Figure 8.10 Ne micro-plasma emission spectrum measured by optical fibber connected commercial spectrometer system with CCD detector

On the other hand, the emission spectrum is measured by a scanning spectrometer (Heath 700, Benton Harbor, Michigan) with an Al-ZnO/Si photodetector. The measurement result is presented in Fig. 8.11.

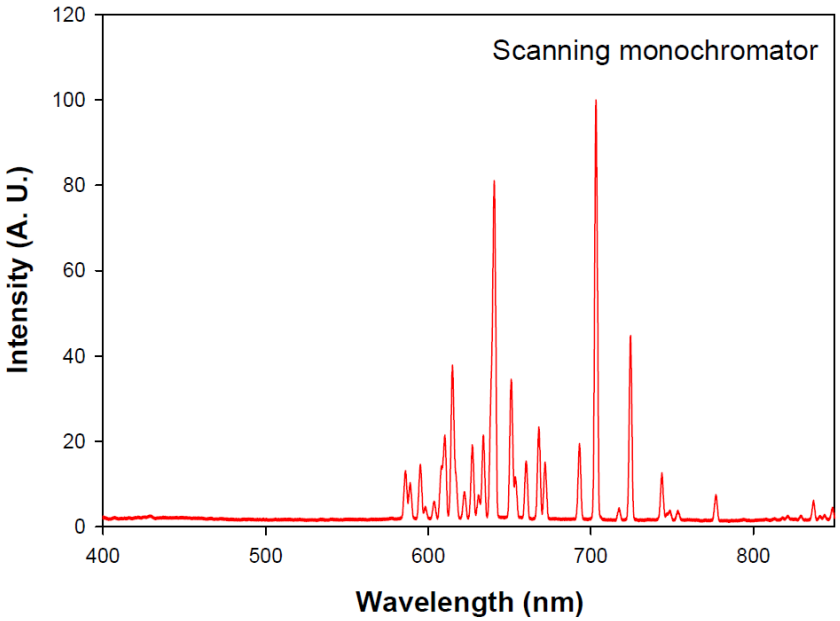


Figure 8.11 Ne micro-plasma emission spectrum measured by scanning spectrometer with Al-ZnO/Si detector

In Fig. 8.12, Ne micro-plasma spectrum measured by two sets of systems are presented together for comparison. Obviously, the two sets of systems are generating very similar output regarding to peak position and most of the peak magnitude at visible wavelength range (except for blue or UV region).

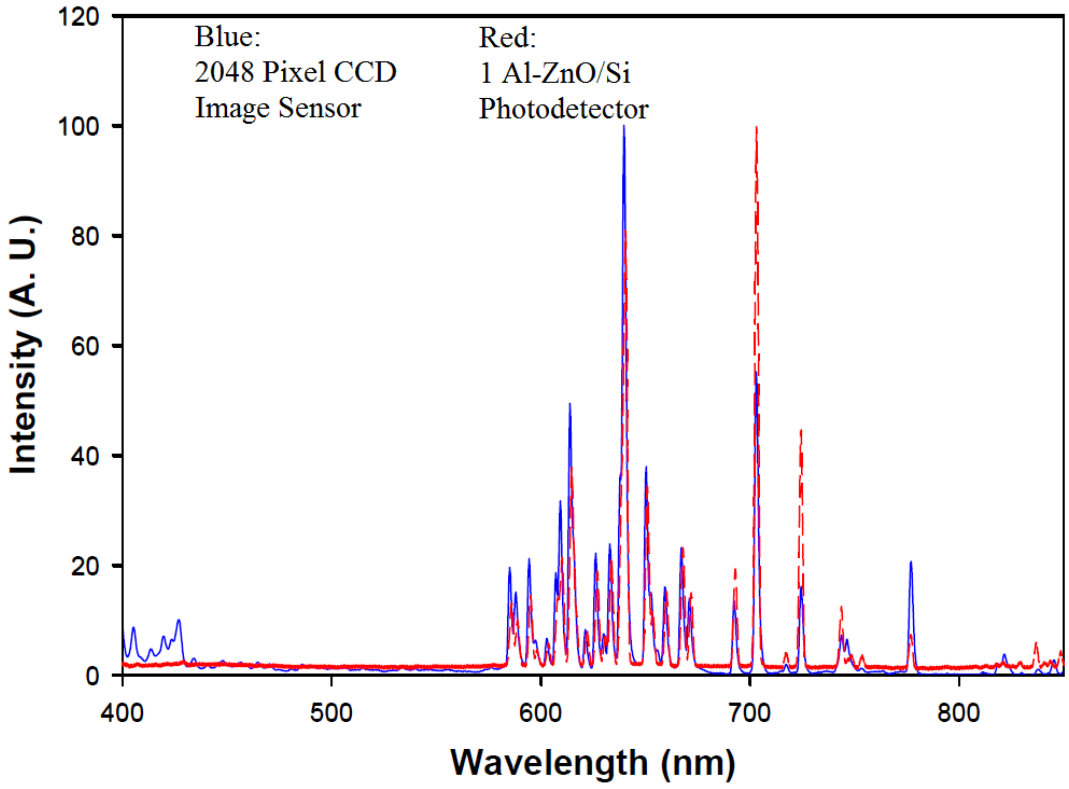


Figure 8.12 Ne micro-plasma emission spectrum measurement result comparison

8.6.2 Micro-Sample Introduction Test

As described above, in the final applications, micro-samples are introduced to the micro-plasma for material identification test. Here, standard Li and Na solutions are prepared. Scanning spectrometer is adjusted to known peak value, 670.8 nm and 589 nm for Li and Na, respectively. When the micro-samples are introduced to the micro-plasma, a flash is observed. Three consecutive runs are performed for each standard solution to test the response of Al-ZnO/Si heterojunction detector. Also, the test results are compared to confirm the repeatability of the experiments. Fig. 8.13 presents the photo response of Al-ZnO/Si detector when micro-samples (Li and Na standard solution) are introduced to micro-plasma system.

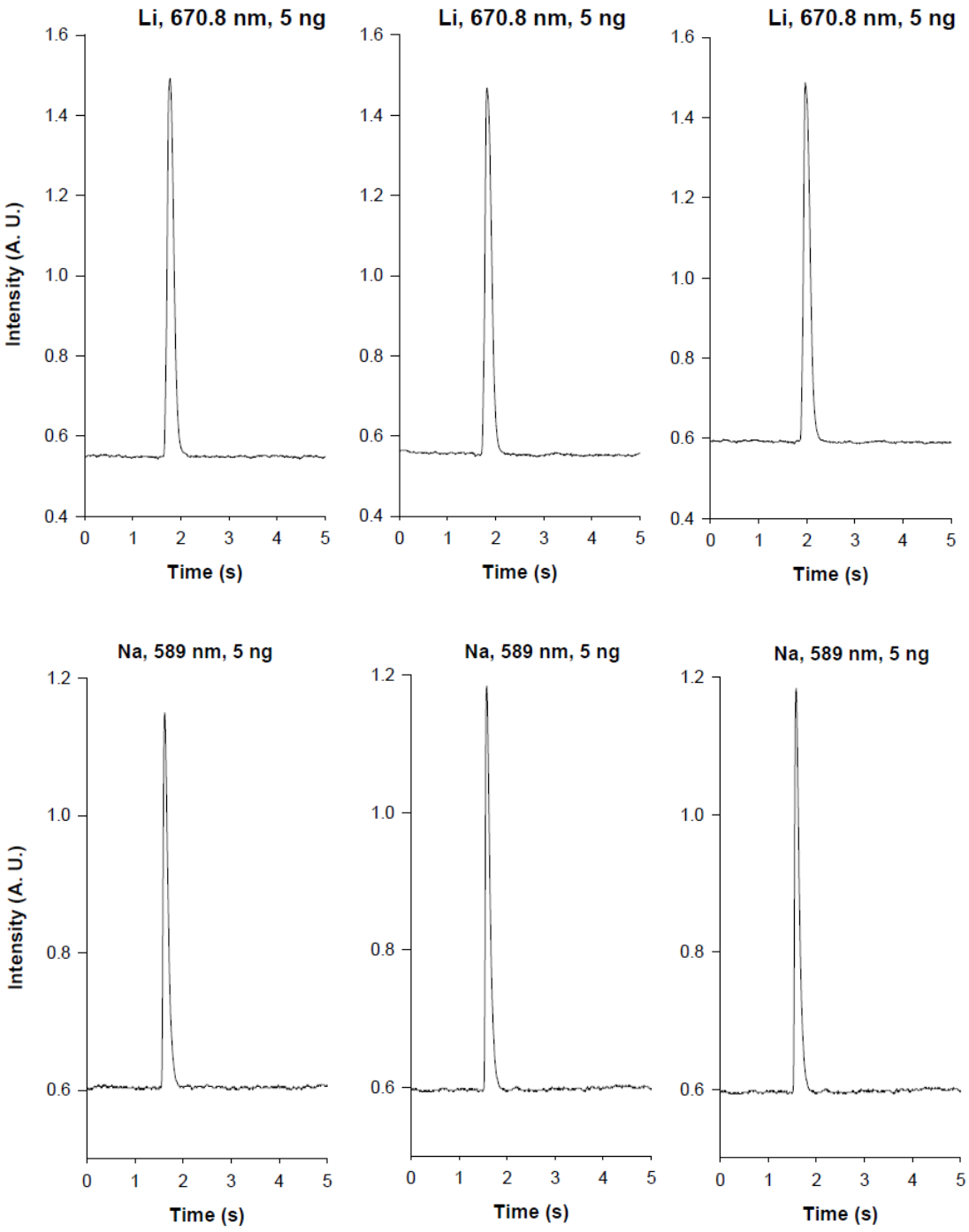


Figure 8.13 Three consecutive runs of Al-ZnO/Si detector photo response upon introduction of Li standard solution micro-sample (top) and of Na standard solution micro-sample (bot)

8.7 Conclusions

Based on the understanding of Al-ZnO/Si heterojunction structures, optimization approaches are applied to Al-ZnO/(n)Si heterojunction photodetectors. Optically, the

thickness of the Al-ZnO thin film is designed to serve as an ARC layer. Electrically, an NAO passivation layer is applied to passivate the interface defects and enhance the depletion region at the heterojunction interface. High performance large area self-powered Al-ZnO/(n)Si heterojunction photodetector is achieved with the optimization approaches.

The photoresponse of the Al-ZnO/(n)Si heterojunction photodetector with 1 kHz modulated optical signal is demonstrated with preliminary circuit design. The switching properties of the Al-ZnO/(n)Si heterojunction are presented up to 10 kHz. The photodetector is also presented in the micro-plasma system for micro-sample element identification. The performance of a single photodetector provided similar signal response to a commercial 2048 pixel CCD image sensor.

CHAPTER 9

CONCLUSION AND FUTURE WORK

9.1 Conclusion

In this thesis, advanced 2-D simulation of IBC solar cell is presented; one type of mono-junction device, standard diffused junction solar cell and two types of advanced heterojunction devices, poly-Si/c-Si heterojunction solar cell and Al-ZnO/Si heterojunction photodetector, are developed and analyzed.

9.1.1 Advanced 2-D Simulation of IBC Solar Cells

2-D simulation of IBC solar cells is performed with different device parameters and various dimension of simulation units. The simulation results provided valuable guidance for future high efficiency IBC solar cell development. The summarized conclusions from the simulation results are as follows:

1. Higher substrate MCL helps improve device performance in almost all aspects;
2. Thinner substrate lower the requirement of MCL levels for high efficiency devices;
3. Optimum substrate thickness for high MCL devices is way below that of current devices (i.e. 150 μm);
4. Thin and lightly doped FSF will further improve device performance.

9.1.2 Standard Diffused Junction Si Solar Cells

Technologies for standard diffused junction Si solar cells are developed and analyzed in category of light confinement, junction formation, surface passivation and metallization.

For light confinement methods, surface texturing and PECVD SiN_x ARC are developed and studied in house. An optimum alkaline texturing solution with 2% KOH and 7% IPA in DI water is presented. SEM imaging and UV/Vis reflection measurement are performance to inspect the performance of surface texturing. Close to 100% random pyramid coverage is achieved with reasonable size distribution. Textured surface exhibits close to 10% reflection comparing to about 30% reflection before texturing. PECVD SiN_x ARC is deposited on polished and textured Si wafer and Si solar cells. Surface reflection is measured. Less than 1% reflection is achieved at designed wavelength (i.e. 600 nm). The combination of surface texturing and SiN_x ARC demonstrated excellent light confinement with most visible wavelength reflection reduced to less than 10%. The reflection in green region is below 5%. The benefit from light confinement is also demonstrated at device level with significant increase in J_{sc}.

For junction formation, standard diffusion processes are developed for boron and phosphorous. Moreover, an etch back process is developed to achieve desired emitter thickness and sheet resistance (i.e. 120 Ω/□). The uniformity of the diffused junction is confirmed by sheet resistance mapping. The sheet resistance mapping is also applied at each step of etch back process to analyze and optimize the etch back parameters.

Surface passivation methods of PECVD SiN_x and BSF are developed and analyzed. With the knowledge from light confinement and junction formation, SiN_x and BSF methods are applied to diffused junction Si solar cells. Device performance improvement is demonstrated at device level. Moreover, IQE characteristics obviously showing the benefit brought by these passivation methods.

For metallization development and analysis, main efforts are located on optimizing photolithography and subsequent lift-off process. The parameters for photo-resist spin coating, pre-bake and post-bake processes, duration of UV exposure, etc. are optimized by way of optical microscopy visual inspection, especially for textured devices.

Standard diffused junction Si solar cells are fabricated with the above mentioned features. With the help of post-fabrication LPHA, **typical device efficiency achieved 17.2% with average short circuit current density more than 39 mA/cm^2.**

9.1.3 Advanced Poly-Si/c-Si Heterojunction Solar Cell

First, parameters for LPCVD n+ poly-Si thin films are optimized. Second, device property enhancement methods, interfacial passivation layer (NAO) and RTA at different temperature, are analyzed. Finally, advance poly-Si/c-Si heterojunction solar cells are fabricated and analyzed.

Optimized LPCVD n+ poly-Si thin film exhibits good sheet resistance with reasonable film thickness. It secured the possibility of achieving good FF and J_{sc} at the same time. A systematic comparative study is performed for poly-Si/c-Si heterojunction solar cells with, without and with different types of device enhancement methods (i.e. NAO layer and RTA process). Device performances are presented and compared at device level. The results show that the implementation of interfacial passivation layer (NAO) and RTA process further improved the device performance, especially on blue response as presented in QE characteristics and on reverse saturation current as presented in dark IV characteristics. **Champion device achieved J_{sc} of 29.68 mA/cm^2 and FF of 78.3% at the same time. Device efficiency reached 13.77% on a low MCL Si substrate. With the help of LPHA, device FF improved to 79.1% and efficiency increased slightly to 13.81%.**

The proposed device structure eliminated the commonly applied TCO layer. Therefore, high temperature tolerance allows the poly-Si/c-Si heterojunction solar cell to adapt typical industrial metallization processes. More importantly, the developed n+ poly-Si thin film, with the help of NAO layer and RTA process, maintained high FF while keeping reasonable blue response. The fabrication processes of the developed advanced poly-Si/c-Si heterojunction solar cells are transferable to industrial mass production. It is capable and promising for the next generation photovoltaic products.

9.1.4 Advanced Al-ZnO/Si Heterojunction Photodetector

First, high quality Al-ZnO thin film is deposited and analyzed. Second, Al-ZnO/Si heterojunction devices are fabricated. Moreover, comparative study of Al-ZnO/Si heterojunction is performed to reveal the photoresponse mechanisms of Al-ZnO/Si heterojunction devices. Third, based on the mechanism study, high performance Al-

ZnO/(n)Si heterojunction photodetector is developed and analyzed. Finally, Al-ZnO/Si photodetector switching test and its application on micro-plasma substance identification system are demonstrated.

Al-ZnO thin film is analyzed with HR-XRD, HR-SEM, TEM and Hall Effect Measurement, etc. Characterization results demonstrate highly crystallized thin film with excellent optical and electrical properties for opto-electronic devices.

Al-ZnO/Si heterojunction devices are fabricated with simple and low temperature processes. Dark IV, illuminated IV and biased QE characteristics revealed the photoresponse mechanism of the heterojunction structure. The surface induced depletion region is the driving force for the photoresponse of such devices. Therefore, different from common understanding, **Al-ZnO/Si heterojunction devices with (n)Si substrate have superior performance.**

High performance Al-ZnO/(n)Si heterojunction photodetectors are fabricated. Two approaches are applied to achieve high responsivity (QE): 1. Optimize Al-ZnO thin film thickness; 2. Apply interfacial passivation layer (NAO). **Excellent diode behavior with rectification ratio of 2.7×10^3 at ± 0.5 V is achieved. The reverse saturation current density is as low as 4.5×10^{-7} A/cm^{-2} at -0.5 V for a 4.84 cm^2 device. Maximum QE of 98.8% is achieved at designed wavelength (600 nm), which is the record for similarly structured devices. The operation of the detector under 1 kHz modulated signal is demonstrated.**

Switching test up to 10 kHz for the detector is presented. Moreover, the application of the detector on micro-plasma system is demonstrated in comparison with commercial 2048 pixel CCD image sensor. Excellent alignment for Neon gas micro-plasma spectrum and high repeatability for Na and Li micro-sample signal are achieved.

9.2 Future Work

9.2.1 Future Work for Poly-Si/c-Si Heterojunction Solar Cells

In this research, in-situ deposited LPCVD n+ poly-Si emitter solar cells are developed with the most basic solar cell structures. Multiple approaches can be applied to the current structure for further improved device performance.

Material upgrade:

- Implement high quality Si substrate;

Process optimization:

- Optimize RTA temperature and duration;
- Apply thermal oxide instead of NAO;
- Deposit thicker front metal contacts;

Structural improvement:

- Apply optical confinement method such as surface texturing;
- Apply back surface passivation such as BSF, localized rear contact, tunnel oxide passivated rear contact, etc;
- Apply the poly-Si/c-Si heterojunction in IBC solar cell structure with ultra-thin Si substrate.

With the refinement approaches stated above, high performance poly-Si/c-Si heterojunction devices are promising for future research.

9.2.2 Future Work for Al-ZnO/Si Heterojunction Photodetectors

The Al-ZnO/Si heterojunction photodetectors fabricated and analyzed in this research opened a brand new research direction. The work done in this research only explored very small part of the possibilities for such devices.

- Further improve the current high performance Al-ZnO/Si photodetector

  Features such as substrate texturing, nano-wire structure, different interfacial passivating layer, Quantum Dot (QD) down conversion layer, rear surface

passivation, etc. can be applied to the current structure to improve overall responsivities at entire visible spectrum.

- Application in high speed optoelectronic systems:

  Currently, devices are fabricated in the size of 4.84 cm^2. Smaller sized devices will have improvement in multiple aspects such as lower reverse saturation current, smaller built-in capacitance, etc. With the Schottky structure, Al-ZnO/Si heterojunction is promising for high speed optoelectronic systems.

- Advanced MSM photodetector

  One of the main problem for traditional MSM photodetectors is low active area ratio. Metal fingers are blocking large amount of incoming optical signal. Transparent Al-ZnO thin film eliminated this problem and hence promising for high performance MSM photodetectors.

- Application in advanced CMOS image sensor

  Because of its simple structure and low temperature fabrication process, Al-ZnO/Si heterojunction is capable of replacing and improving the state-of-the-art photodetectors applied in CMOS image sensor.

- Simple structure photodetectors on different semiconductor substrate

  After understanding the photoresponse mechanism of the Al-ZnO/Si heterojunction structure, similar structure may be able to transfer to other types of substrates such as Ge, Si_xGe_{1-x}, etc. With different bandgap of the active layer (i.e. substrate), photodetectors with different response wavelength can be achieved.

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Appendix: Example of Medici Coding

For the reference of possible future designs and analysis, the author is willing to share the original simulation design and coding for IBC solar cells. One of the Medici simulation coding example is given below:

```
TITLE Backcontact cell structure-

ASSIGN NAME=Tarc N.VAL=0.078
ASSIGN NAME=Tfsf N.VAL=0.02
ASSIGN NAME=Tbulk N.VAL=200
ASSIGN NAME=Tbackni N.VAL=0.1

ASSIGN NAME=Wemit N.VAL=70
ASSIGN NAME=Wbsf N.VAL=15
ASSIGN NAME=Wanode N.VAL=13
ASSIGN NAME=Wcathode N.VAL=68
ASSIGN NAME=Wunit   N.VAL=100

ASSIGN NAME=Xcathode N.VAL=@Wunit-@Wcathode
ASSIGN NAME=Ybody N.VAL=@Tarc+@Tbulk+@Tfsf

COMMENT Mesh Generation
MESH OUT.FILE=backcontact_mesh
X.MESH WIDTH=@Wunit H1=1
Y.MESH Y.MIN=-@Tbackni Y.MAX=0 H1=@Tbackni/2
Y.MESH Y.MIN=0 Y.MAX=2 H1=0.5
Y.MESH Y.MIN=2 Y.MAX=@Tbulk H1=@Tbulk/20
Y.MESH Y.MIN=@Tbulk Y.MAX=@Tbulk+@Tfsf H1=@Tfsf/2
Y.MESH Y.MIN=@Tbulk+@Tfsf Y.MAX=@Tbulk+@Tfsf+@Tarc H1=@Tarc/2

REGION NAME=backni Y.MIN=-@Tbackni Y.MAX=0 NITRIDE
REGION NAME=base Y.MIN=0 Y.MAX=@Tbulk+@Tfsf SILICON
REGION NAME=arc Y.MIN=@Tbulk+@Tfsf Y.MAX=@Tbulk+@Tfsf+@Tarc NITRIDE

COMMENT Electrodes
ELECTR NAME=1 X.MIN=0 X.MAX=@Wcathode Y.MIN=-@Tbackni Y.MAX=0
ELECTR NAME=2 X.MIN=@Wunit-@Wanode Y.MIN=-@Tbackni Y.MAX=0

COMMENT Doping
PROFILE P-TYPE Y.MIN=0 Y.MAX=@Tbulk N.PEAK=5E15 UNIFORM
OUT.FILE=backcontactstan

PROFILE P-TYPE Y.MIN=@Tbulk Y.MAX=@Tbulk+@Tfsf N.PEAK=1E19 UNIFORM

PROFILE N-TYPE N.PEAK=1E20 Y.JUNC=1 X.MIN=0 WIDTH=@Wemit XY.RAT=.75

PROFILE P-TYPE N.PEAK=1E20 Y.JUNC=1 X.MIN=@Wunit-@Wbsf WIDTH=@Wbsf
XY.RAT=.75

COMMENT surface recombination at the top surface
INTERFACE MATERIAL=(SILICON,NITRIDE) S.N=10 S.P=10
```

```
COMMENT Grid refinement based on doping.
REGRID DOPING LOG RATIO=1 SMOOTH=1 IN.FILE=backcontactstan

MODELS CONMOB CONSRH AUGER

COMMENT Specify Electrode Characteristics
CONTACT NAME=1 REFLECT=0.9
CONTACT NAME=2 REFLECT=0.9

MATERIAL REGION=base TAUN0=3E-3 TAUP0=3E-3

COMMENT Display the grid at the top and bottom on the same plot.
PLOT.2D TITLE="BACK CONTACT CELL"
+ ^MARKS ^LABELS X.LEN=15
PLOT.2D GRID FILL Y.MAX=3 TITLE=""
+ X.LEN=6 X.OFF=2 ^CLEAR
PLOT.2D GRID SCALE FILL Y.MIN=@Ybody-10 TITLE=""
+ X.LEN=6 X.OFF=11 ^CLEAR

ASSIGN NAME=wavenum N.VAL=90

COMMENT
PHOTOGEN
+ RAYTRACE SP.FILE=AM15.DAT
+ WAVE.ST=0.295 WAVE.EN=1.255 WAVE.NUM=@wavenum INT.SCAL=1
+ X.ORG=@Wunit/2 Y.ORG=@Tbulk+@Tfsf+1 ANGLE=270
+ RAY.WIDT=@Wunit RAY.NUM=1 INT.RATI=1E-3 N.INTEG=10 TRANSPAR PRINT.AB

SYMBOLIC NEWTON CARRIERS=2

COMMENT Solve for each wavelength of the spectral response
LOG OUT.FILE="backcontact_spec"

COMMENT solve for short circuit current for each wavelength
+ LOOP STEPS=@wavenum
+ SOLVE WAVE=1:1
+ L.END

SOLVE SPECTR

PLOT.1D X.AXIS=WA Y.AXIS=CE(2) POINTS COLOR=2 SYMB=2 ABS CLEAR PRINT
LABEL LABEL="backcontact cell " COLOR=2 SYMB=2
+ X=0.6 Y=30 C.SIZE=0.2

PLOT.1D X.AXIS=WA Y.AXIS=IT POINTS COLOR=2 SYMB=2 ABS CLEAR PRINT
LABEL LABEL="AM1.5" COLOR=2 SYMB=2
+ X=0.6 Y=30 C.SIZE=0.2

COMMENT solve for DC IV values for the whole spectrum

LOG OUT.FILE=backcontact_IV

SOLVE V(2)=0.00 ELEC=2 VSTEP=.05 NSTEP=10
SOLVE V(2)=0.52 ELEC=2 VSTEP=.01 NSTEP=6
SOLVE V(2)=0.59 ELEC=2 VSTEP=.005 NSTEP=16
SOLVE V(2)=0.675 ELEC=2 VSTEP=.001 NSTEP=60

PLOT.1D X.AXIS=V(2) Y.AXIS=I(2) POINTS COLOR=2 SYMB=2 CLEAR PRINT
```

```
LABEL LABEL="backcontact cell IV-AM1.5" COLOR=2 SYMB=2
COMMENT + X=0.2 Y=30 C.SIZE=0.2

COMMENT Calculate the power generated and load impedance.
EXTRACT NAME=Power EXP="-1e8*@I(2)*@V(2)/@Wunit" PRINT
+ UNITS=Watts/cm^2

COMMENT Plot the power-vs-load resistance curve.
PLOT.1D X.AXIS=V(2) Y.AXIS=Power POINTS COLOR=2 PRINT
+ TITLE="backcontact Cell Power vs. voltage"

PLOT.2D FILL BOUND
TITLE="CURRENT FLOW"
CONTOUR FLOW
```