

# Assessment of High-Frequency Performance Limit of Black Phosphorus Field-Effect Transistors

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**Abstract**—Recently gigahertz frequencies have been reported with black phosphorus (BP) field-effect transistors (FETs), yet the high-frequency performance limit has remained unexplored. Here we project the frequency limit of BP FETs based on rigorous atomistic quantum transport simulations and the small-signal circuit model. Our self-consistent non-equilibrium Green's function (NEGF) simulation results show that semiconducting BP FETs exhibit clear saturation behaviors with the drain voltage, unlike zero-bandgap graphene devices, leading to >10 THz frequencies for both intrinsic cutoff frequency ( $f_T$ ) and unity power gain frequency ( $f_{max}$ ). To develop keen insight into practical devices, we discuss the optimization of  $f_T$  and  $f_{max}$  by varying various device parameters such as channel length ( $L_{ch}$ ), oxide thickness, device width, gate resistance, contact resistance and parasitic capacitance. Although extrinsic  $f_T$  and  $f_{max}$  can be significantly affected by the contact resistance and parasitic capacitance, they can remain near THz frequency range ( $f_T = 900$  GHz;  $f_{max} = 1.2$  THz) through proper engineering, particularly with an aggressive channel length scaling ( $L_{ch} \approx 10$  nm). Our benchmark against the experimental data indicates that there still exists large room for optimization in fabrication, suggesting further advancement of high-frequency performance of state-of-the-art BP FETs for the future analogue and radio-frequency applications.

**Index Terms**—Black phosphorene, field-effect transistor, cutoff frequency, unity power gain frequency, non-equilibrium Green's function, small-signal circuit model

## I. INTRODUCTION

TWO-DIMENSIONAL (2D) materials are very intriguing for next-generation electronic devices due to their unique physical properties such as compelling electrical characteristics, large immunity to aggressive scaling, excellent optical and mechanical properties [1], [2]. For more than a decade, graphene has been explored extensively, and it turned out that graphene is promising for radio-frequency (RF) applications [3] rather than switching devices mainly due to its ultra-high carrier mobility ( $\sim 10,000$  cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup>) [4] and high saturation velocity ( $> 3 \times 10^7$  cm s<sup>-1</sup>) [5] yet inherently large leakage current. Graphene field-effect transistors (FETs) exhibit as comparably high cutoff frequency ( $f_T$ ) as state-of-the-art InAs high-electron-mobility transistors

(HEMTs) and GaAs metamorphic HEMTs [3], [6]–[8], although III-V semiconductors ( $\sim 1$  THz) [9] still outperform graphene FETs. The  $f_T$  of graphene FET (GFET) can reach a few hundred GHz when channel length scales down below 100 nm [10]. However, the unity power gain frequency ( $f_{max}$ ) of GFETs is significantly limited due to its poor saturation behavior of drain current. The highest reported  $f_{max}$  is  $\sim 50$  GHz, which is far less than  $f_T$  [11]. Moreover, its large output conductance ( $g_d$ ) also significantly limits the intrinsic voltage gain of GFETs. To overcome such limitations, a large band gap as well as high carrier mobility would be required, and black phosphorus (BP) can be an outstanding contender for high-frequency applications among many 2D materials.

Black phosphorus is a layered material with high hole mobility (10,000 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup>) and a thickness-dependent direct band gap ranging from 0.3 eV (bulk) to 2 eV (monolayer) [12], [13]. Even at its early stage, BP FETs have demonstrated high field-effect mobility ( $\sim 1,000$  cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup>) and a high on-off current ratio ( $> 10^5$ ) [14], [15], which are critically important not only for high-performance logic circuits but also for high-frequency applications. Recently, gigahertz frequencies ( $f_T = 17.5$  GHz;  $f_{max} = 14.5$  GHz) have been reported with BP FETs on a bendable substrate [16], [17]. However, the performance of BP FETs is currently limited by various factors. For example, the source/drain contact resistance ( $R_{SD}$ ) of BP FETs is relatively high ( $\sim 5$  k $\Omega \cdot \mu\text{m}$ ) [17] compared to that of GFETs, for which  $R_{SD} = 0.1$  k $\Omega \cdot \mu\text{m}$  was reported [18], [19]. Gate resistance ( $R_G$ ) can be another limiting factor for  $f_{max}$ , and parasitic resistance ( $C_p$ ) can also significantly affect the extrinsic performance of the device negatively [20]. As the high-frequency performance limit of BP FETs has remained unexplored yet, it would be worth investigating BP FETs based on rigorous models and numerical simulations before more extensive experimental efforts will be made.

In this study, we investigate the high-frequency performance limit of BP FETs using self-consistent quantum transport simulations and the small-signal circuit model. We thoroughly explore the effects of various device parameters on  $f_T$  and  $f_{max}$  by varying equivalent oxide thickness (EOT), channel length ( $L_{ch}$ ), device width ( $W$ ),  $R_G$ ,  $R_{SD}$  and  $C_p$ . Our simulation results reveal that BP FETs can exhibit as good  $f_T$  as GFETs. Furthermore,  $f_{max}$  of BP FETs is not limited, unlike that of GFETs, enabling near THz frequencies for both  $f_T$  and  $f_{max}$  with proper engineering. Our benchmark against experimental data indicates that there exists huge room for optimization, to boost the high-frequency performance of BP FETs, particularly with channel length scaling.

This work was supported in part by NSERC Discovery Grant (RGPIN-05920-2014) and in part by NSERC Strategic Project Grant (STPGP 478974-15). Computing resources were provided by SHARCNET through Compute Canada. The authors are with Department of Electrical and Computer Engineering & Waterloo Institute for Nanotechnology at the University of Waterloo, Waterloo, ON, Canada N2L 3G1 (Email: youngki.yoon@uwaterloo.ca).

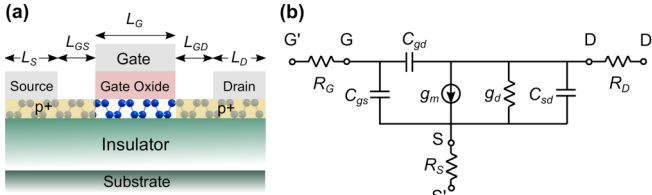


Fig. 1. (a) Device structure of a simulated black phosphorus (BP) field-effect transistor (FET). Monolayer BP is used for the channel, and the source/drain is p-doped forming an Ohmic contact. Single-gate geometry is used. (b) Small-signal equivalent circuit of the BP FET.  $g_m$  and  $g_d$  are the transconductance and the output conductance;  $R_G$ ,  $R_S$ , and  $R_D$  are the gate resistance, the source and the drain contact resistance, respectively;  $C_{gs}$ ,  $C_{gd}$ , and  $C_{sd}$  are the small-signal gate-to-source, the gate-to-drain, and the source-to-drain capacitance, respectively.

## II. APPROACH

### A. Device Structure

Figure 1 (a) shows a schematic device structure of a simulated BP FET. Monolayer BP is used for the channel as it can provide better performance than multilayer BP in the conventional FET structure [21]. A single-gate device structure is considered following the recent experimental demonstrations, and  $\text{Al}_2\text{O}_3$  ( $\kappa = 9$ ) is used for the gate oxide [17], [22]. For a nominal device, we set the following device parameters: 15-nm channel length and 3-nm-thick gate dielectric (equivalent oxide thickness of EOT = 1.3 nm). Source and drain extensions are p-doped, where Ohmic contact is achieved with a doping concentration of  $1.3 \times 10^{13} \text{ cm}^{-2}$ . We assume that metal electrodes are deposited as shown in Fig. 1(a). Device parameters such as channel length, contact resistance and parasitic capacitances will be varied to explore their impacts on the device performance.

### B. Numerical Simulations

Transport properties of BP FETs are simulated based on the non-equilibrium Green's function (NEGF) formalism within a tight-binding (TB) approximation, self-consistently with the Poisson's equation [23]. To accurately describe electronic states of monolayer black phosphorus, five TB parameters ( $t_1 = -1.220 \text{ eV}$ ,  $t_2 = 3.665 \text{ eV}$ ,  $t_3 = -0.205 \text{ eV}$ ,  $t_4 = -0.105 \text{ eV}$ ,  $t_5 = -0.055 \text{ eV}$ ) are used in the Hamiltonian matrix [24]. Considering the anisotropic nature of the band structure of black phosphorus, we took the armchair orientation for the transport direction due to its light hole effective mass ( $m_{hx} = 0.19m_0$ ) for the p-type conduction. Ballistic transport is assumed considering relatively short channel length with NEGF simulations, and the effect of scattering is treated separately based on the Landauer-Lundstrom-Datta model [25] in section F of the results. The large dimension of the device width is treated by a mode space approach with a periodic boundary condition. Charge density and current are calculated by using numerical summation of the transverse momentum. Therefore, device characteristics such as current and transconductance are given per unit width, with which different widths of devices (e.g., 1  $\mu\text{m}$  or 10  $\mu\text{m}$ ) are considered. Open boundary condition is treated by contact self-energies [26]. Power supply voltage of  $V_{DD} = 0.5 \text{ V}$  is used, and the room temperature is assumed.

### C. Equivalent Small-Signal Circuit Model

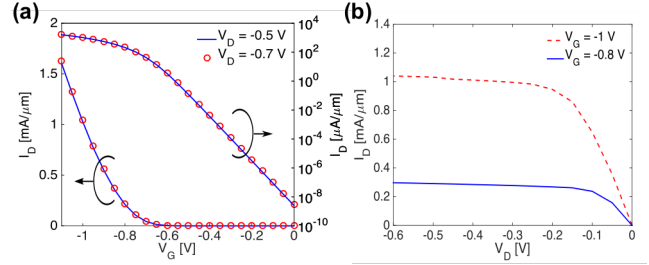


Fig. 2. (a)  $I_D$ - $V_G$  characteristics of a nominal BP FET at  $V_D = -0.5$  and  $-0.7 \text{ V}$ . (b)  $I_D$ - $V_D$  characteristics of the same device at  $V_G = -0.8$  and  $-1 \text{ V}$ .

Quasi-static treatment is used to assess high-frequency performance following standard procedures [27]. The steady-state channel charge ( $Q_{ch}$ ) and drain current ( $I_D$ ) are computed by performing self-consistent DC simulations. The intrinsic gate capacitance ( $C_{gg}$ ) and transconductance ( $g_m$ ) are extracted from the  $I_D$ - $V_G$  characteristics as

$$C_{gg} = \left. \frac{\partial Q_{ch}}{\partial V_G} \right|_{V_D}, \quad g_m = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_D}. \quad (1)$$

Similarly, intrinsic gate-to-drain capacitance ( $C_{gd}$ ) and the output conductance ( $g_d$ ) can be extracted from the  $I_D$ - $V_D$  characteristics as

$$C_{gd} = - \left. \frac{\partial Q_{ch}}{\partial V_D} \right|_{V_G}, \quad g_d = \left. \frac{\partial I_D}{\partial V_D} \right|_{V_G}. \quad (2)$$

Then, we can obtain gate-to-source capacitance as

$$C_{gs} = C_{gg} - C_{gd}. \quad (3)$$

In this study, the main interest lies in cutoff frequency (unity current gain frequency)  $f_T$  and unity power gain frequency  $f_{max}$  of BP FETs. The intrinsic  $f_T$  can be calculated as

$$f_T = \frac{g_m}{2\pi C_{gg}} \quad (4)$$

and intrinsic  $f_{max}$  is given by

$$f_{max} = \frac{f_T}{2\sqrt{g_d R_G + 2\pi f_T C_{gd} R_G}}, \quad (5)$$

where  $R_G$  is the gate resistance and it can be determined by

$$R_G = \alpha R_{SHG} \frac{W}{L} \times \frac{1}{N}. \quad (6)$$

$R_{SHG}$  is the gate sheet resistance of metal gate being related to the gate metal's resistivity ( $\rho_G$ ) and thickness ( $A_G$ ) as  $R_{SHG} = \frac{\rho_G}{A_G}$ .  $\alpha$  is 1/3 when the gate terminal is brought out from one side, and 1/12 when connected to both sides.  $W$  and  $L$  are the width and the length of gate metal per finger, respectively.  $N$  is the number of fingers. We assumed that the gate metal is connected from one end ( $\alpha = 1/3$ ) and a single finger structure is used ( $N = 1$ ) for the nominal device.

In practical devices,  $f_T$  and  $f_{max}$  can be significantly limited by other device parameters such as source/drain contact resistance and parasitic capacitances. The extrinsic  $f_T$  is calculated as

$$f_T = \frac{g_m}{2\pi \{C_{gg,t}[1 + g_d(R_S + R_D)] + C_{gd,t}g_m(R_S + R_D)\}}, \quad (7)$$

and the extrinsic  $f_{max}$  is given as

$$f_{max} = \frac{g_m}{4\pi\sqrt{\Psi_1 + \Psi_2 + \Psi_3}}, \quad (8)$$

where  $\Psi_1$ ,  $\Psi_2$  and  $\Psi_3$  are

$$\Psi_1 = R_G [(R_S + R_D)(C_{gg,t}g_d + C_{gd,t}g_m)^2 + C_{gg,t}(C_{gg,t}g_d + C_{gd,t}g_m)] \quad (9a)$$

$$\Psi_2 = R_D [R_S(C_{gg,t}g_d + C_{gd,t}g_m)^2 + C_{gd,t}(C_{gd,t}g_d + C_{ad,t}g_m)] \quad (9b)$$

$$\Psi_3 = R_S [g_m(C_{gg,t} - C_{gd,t})(C_{gd,t} - C_{ad,t}) + g_d(C_{gg,t} - C_{gd,t})(C_{gg,t} - C_{ad,t})] \quad (9c)$$

and the capacitance with subscript  $t$  is the total capacitance considering various parasitic components:

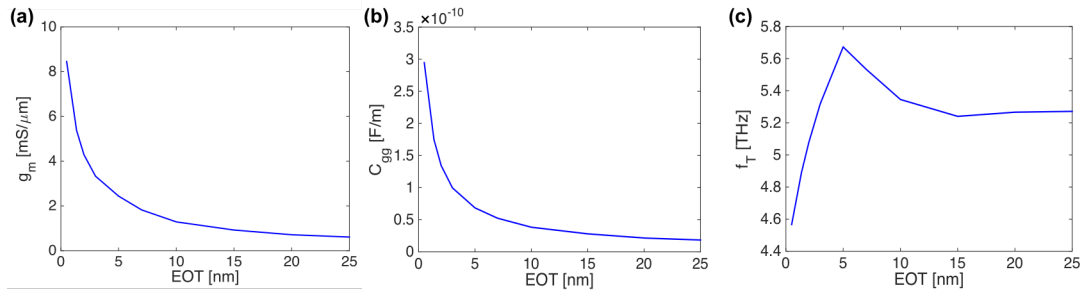


Fig. 3. (a)  $g_m$ , (b) small-signal intrinsic gate capacitance  $C_{gg}$ , and (c) intrinsic cutoff frequency  $f_T$  as a function of EOT varying from 0.5 to 25 nm. The  $g_m$  and  $C_{gg}$  are extracted at  $I_{on} = 1$  mA/μm from the simulation results.

$$C_{gg,t} = C_{gg} + C_{gd,p} + C_{gs,p} \quad (10a)$$

$$C_{gd,t} = C_{gd} + C_{gd,p} \quad (10b)$$

$$C_{dg,t} = C_{dg} + C_{dg,p} \quad (10c)$$

$$C_{dd,t} = C_{dd} + C_{dg,p} + C_{ds,p}. \quad (10d)$$

The intrinsic capacitances of  $C_{dg}$  and  $C_{dd}$  are determined by

$$C_{dg} = -\frac{\partial Q_D}{\partial V_{GS}}, \quad C_{dd} = \frac{\partial Q_D}{\partial V_{DS}}, \quad (11)$$

where we treat  $C_{dg}$  and  $C_{dd}$  being zero as the variation of charge inside the drain is negligible. Based on a planar MOSFET structure, we estimate  $C_p$  induced by the contacts as [27]:

$$C_{gs,p} = (\epsilon_S + \epsilon_0)W \times \frac{K(\sqrt{1-k_{gs}^2})}{K(k_{gs})}, \quad k_{gs} = \sqrt{\frac{L_{GS}}{L_{GS}+L_G}} \quad (12a)$$

$$C_{gd,p} = C_{dg,p} = (\epsilon_S + \epsilon_0)W \times \frac{K(\sqrt{1-k_{gd}^2})}{K(k_{gd})}, \quad k_{gd} = \sqrt{\frac{L_{GD}}{L_{GD}+L_G}} \quad (12b)$$

$$C_{ds,p} = (\epsilon_S + \epsilon_0)W \times \frac{K(\sqrt{1-k_{ds}^2})}{K(k_{ds})}, \quad k_{ds} = \sqrt{\frac{(2L_S+L_{DS})L_{DS}}{(L_S+L_{DS})^2}} \quad (12c)$$

where  $\epsilon_S$  and  $\epsilon_0$  are dielectric constant of semiconductor and air, respectively,  $L_G$  is the gate length, and  $K(k)$  is the complete elliptic integral of the first kind, defined as

$$K(k) = \int_0^1 \frac{dw}{(1-w^2)^{1/2}(1-k^2w^2)^{1/2}}. \quad (13)$$

The inductance of contact is ignored in the small-signal circuit as its impact is negligible compared to those of contact resistance and parasitic capacitance [27]–[30].

### III. RESULTS

#### A. Transfer and Output Characteristics of BP FETs

First, we have plotted the intrinsic transfer and output characteristics of the nominal device based on the self-consistent NEGF quantum transport simulations. Figure 2(a) shows the  $I_D$ – $V_G$  characteristics of the BP FET at  $V_D = -0.5$  and  $-0.7$  V in linear scale (left axis) and logarithmic scale (right axis). It exhibits large on current ( $I_{on} > 1.5$  mA/μm), large transconductance ( $g_m \sim 6.4$  mS/μm), large on/off current ratio ( $I_{on}/I_{off}$  reaches  $4.8 \times 10^7$  and  $1.8 \times 10^{10}$  at  $V_{DD} = -0.5$  V and  $-0.7$  V, respectively), and excellent switching characteristics with small subthreshold swing (SS = 64.8 mV/dec). One of the main advantages of monolayer BP over graphene is the presence of a large band gap, which enables a clear saturation behavior in  $I_D$ – $V_D$  characteristics as shown in Fig. 2(b). Output conductance of  $g_d = 147$  μS/μm and  $62$  μS/μm are achieved at  $V_G = -1$  V and  $-0.8$  V, respectively, even with a short channel length (15 nm).

#### B. Effect of EOT

In general, the efficiency of gate control is critical for the device performance of field-effect transistors [21]. Higher gate efficiency can be realized in various manners: by using double-gate geometry, high-κ dielectric, or thinner gate oxide. For switching devices, smaller EOT is generally preferred for steep subthreshold slope, large  $I_{on}/I_{off}$  and large  $g_m$ . However, it could be different for high-frequency applications, and therefore, we investigate the effect of EOT on the intrinsic  $f_T$  by varying it from 0.5 to 25 nm. Since the intrinsic  $f_T$  is a function of transconductance and gate capacitance,  $g_m$  and  $C_{gg}$  are plotted in Fig. 3(a) and 3(b), respectively, where both increase as EOT is scaled down. Figure 3(c) shows the intrinsic  $f_T$  as a function of EOT, and the peak value of 5.7 THz is achieved at EOT = 5 nm. Therefore, in the subsequent discussion, we will use EOT = 5 nm to evaluate high-frequency performance of BP FETs. It should be noted that the peak value of intrinsic  $f_T$  is not achieved with the thinnest EOT considered in our simulations, which is due to the fact that the increase of  $C_{gg}$  prevails over that of  $g_m$  as EOT scales down less than 5 nm.

#### C. Effect of Channel Length Scaling

We investigate the effect of channel length scaling on the intrinsic high-frequency performance of BP FETs by varying the channel length from 5 to 150 nm. Figures 4(a) and 4(b) show the  $g_m$  and  $C_{gg}$  as a function of  $L_{ch}$ , respectively, for a fixed EOT of 5 nm. While our ballistic transport simulation results show that  $g_m$  is nearly constant for the channel longer than 30 nm, it decreases as the channel length scales down less than 30 nm due to the short-channel effects. The intrinsic gate capacitance is extracted from our numerical simulation results at  $V_G = -1.3$  V, and the  $C_{gg}$  exhibits nearly linear dependence to the channel length. Then, we have plotted the intrinsic  $f_T$  vs.  $1/L_{ch}$ , which shows nice linearity for long-channel devices but it starts to deviate from  $1/L_{ch}$  dependence for  $L_{ch} < 30$  nm due to the degradation of  $g_m$ . The similar trend was also observed in graphene FETs [31]. To show the linearity of  $f_T$  to  $1/L_{ch}$  for the long-channel devices, we have plotted a guideline (dashed line) in Fig. 4(c) with  $f_T = 100$  GHz·μm/ $L_{ch}$ , which is, surprisingly, very similar to that of graphene FETs reported earlier [32]. Although semiconducting black phosphorus has relatively lower mobility than graphene, BP FETs can exhibit as comparable cutoff frequency as graphene FETs due to relatively smaller  $C_{gg}$ .

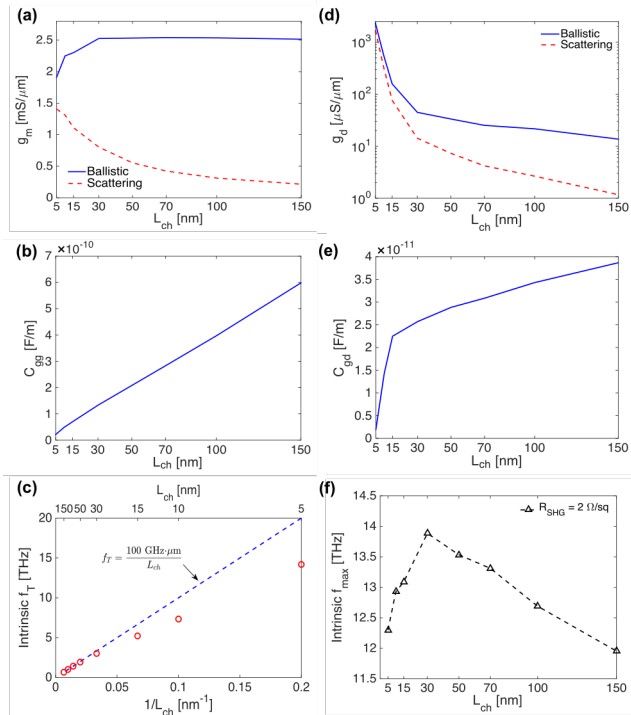


Fig. 4. Intrinsic  $f_T$  and unity power gain frequency  $f_{max}$  calculated for various  $L_{ch}$  with a fixed EOT of 5 nm at the on state ( $V_G = -1.3$  V;  $V_D = -0.5$  V). Channel length dependence of (a)  $g_m$ , (b)  $C_{gd}$ , (c) intrinsic  $f_T$ , (d)  $g_d$ , (e)  $C_{gd}$ , and (f) intrinsic  $f_{max}$  for gate sheet resistance of  $R_{SHG} = 2 \Omega/\square$  with a fixed device width of  $W = 1 \mu\text{m}$ . The dashed line in (c) shows the linear fitting for long-channel devices with  $f_T = 100 \text{ GHz}\cdot\mu\text{m}/L_{ch}$ .

One of the most significant drawbacks of graphene FETs for high-frequency applications is the limited unity power gain frequency. It has been observed from many experiments that  $f_{max}$  is significantly lower than  $f_T$  in graphene FETs [3], [7]. This is attributed to the fact that graphene is semi-metal and hence the current cannot be saturated with increasing the drain voltage. On the other hand, semiconducting BP-based FETs can offer significantly smaller  $g_d$  along with large  $f_T$ , which makes BP FETs attractive for high-frequency applications. Figure 4(d) shows the output conductance as a function of  $L_{ch}$ , which is extracted from the numerical simulations at  $V_D = -0.5$  V. We notice that  $g_d$  increases slowly as  $L_{ch}$  decreases from 150 nm to 30 nm, where the gate controls the electrostatic potential in the channel region well, and the  $g_d$  can be as low as 13  $\mu\text{S}/\mu\text{m}$  at 150-nm channel, which is smaller than that of graphene FETs by two orders of magnitude [28]. However, as the channel length further scales down below 30 nm,  $g_d$  increases significantly due to the short-channel effect, but the  $g_d$  of BP FETs still remain one order smaller than that of graphene FETs [28].

The gate-to-drain capacitance for various channel length is shown in Fig. 4(e), which is also extracted from the numerical simulation results at  $V_D = -0.5$  V. As the channel length scales down from 150 nm to 15 nm,  $C_{gd}$  is also linearly decreased, which can be explained by the strong correlation of the channel charge to the length of device, considering that  $C_{gd}$  is proportional to  $\Delta Q_{ch}$  for a given  $V_D$  variation as shown in Eq. (2). Notably, the channel length dependence of  $C_{gd}$  becomes even more significant (*i.e.*,  $C_{gd}$  vs.  $L_{ch}$  shows a steeper slope) at

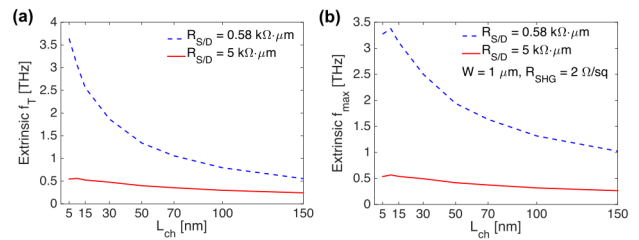


Fig. 5. Effect of contact resistance  $R_{SD}$  on extrinsic  $f_T$  and  $f_{max}$  ignoring parasitic capacitance. (a) Extrinsic  $f_T$  and (b)  $f_{max}$  for  $R_{SD} = 0.58$  and  $5 \text{ k}\Omega\cdot\mu\text{m}$  with  $W = 1 \mu\text{m}$  and  $R_{SHG} = 2 \Omega/\square$ .

$L_{ch} < 15$  nm, where the  $\Delta Q_{ch}$  for a given  $V_D$  variation becomes more susceptible to the change of channel length due to short-channel effect.

The intrinsic unity power gain frequency is plotted in Fig. 4(f) using the intrinsic  $f_T$ ,  $g_d$ , and  $C_{gd}$  evaluated above for a gate resistance. In general,  $R_G$  depends on the geometry of device and the actual fabrication process of the gate electrode (*e.g.*, the number and the width of gate fingers, and the materials of the gate). Here we use a single-finger metal gate reached out from one side, and the width of transistor is assumed to be  $W = 1 \mu\text{m}$ . Unlike the cutoff frequency,  $f_{max}$  is significantly affected by the device width, and the detailed investigation on its effect will be reserved for a later discussion. As can be seen from Eq. (6), distributed gate resistance is linearly proportional to  $W$  and  $R_{SHG}$ . Few decades ago,  $R_G$  was the most limiting factor for polysilicon gate. Nowadays, however, the use of metal gate has enabled a considerable reduction of  $R_{SHG}$ . The intrinsic  $f_{max}$  is investigated in Fig. 4(f) using  $R_{SHG} = 2 \Omega/\square$  [33], [34]. The peak value is observed to be 14 THz at  $\sim 30$  nm channel length, where two competing terms exist as shown in Eq. (5):  $f_{max}$  is mainly dictated by  $2\pi f_T C_{gd}$  for long-channel devices, whereas  $g_d$  becomes predominant for short-channel devices.

#### D. Effect of Contact Resistance

So far, we have investigated the intrinsic performance without considering contact resistances and parasitic capacitances. Now we will extend our discussion to the extrinsic  $f_T$  and  $f_{max}$ . First, we focus on the effect of contact resistance, and the impact of parasitic capacitance will be discussed separately in the following section.  $R_{SD}$  has been known as one of the limiting factors of device performance in 2D material electronics [30]. By carefully choosing source and drain metal and optimizing fabrication processes, low  $R_{SD}$  (0.1–0.78  $\text{k}\Omega\cdot\mu\text{m}$ ) has been realized for graphene and  $\text{MoS}_2$  devices [35], [36]. In case of BP FETs, 5  $\text{k}\Omega\cdot\mu\text{m}$  could be a typical value extracted from recent experiments [17], [37], [38]. First, we have taken this value along with  $W = 1 \mu\text{m}$  and  $R_{SHG} = 2 \Omega/\square$  to investigate the extrinsic  $f_T$  and  $f_{max}$ . Figure 5 shows that both  $f_T$  and  $f_{max}$  can be  $\sim 500$  GHz at  $L_{ch} = 10$  nm and reduces as the channel length increases, resulting in a half peak value when  $L_{ch} = 150$  nm. If the contact resistance is reduced significantly to 0.58  $\text{k}\Omega\cdot\mu\text{m}$ , which is the lowest value reported for BP FETs [39], the extrinsic  $f_T$  and  $f_{max}$  can be tremendously improved. By reducing the contact resistance from 5  $\text{k}\Omega\cdot\mu\text{m}$  to 0.58  $\text{k}\Omega\cdot\mu\text{m}$ , the peak values of  $f_T$  and  $f_{max}$  can be enhanced by 7 times, leading to  $\sim 3.5$  THz, if parasitic capacitance is ignored.

#### E. Effect of Parasitic Capacitance

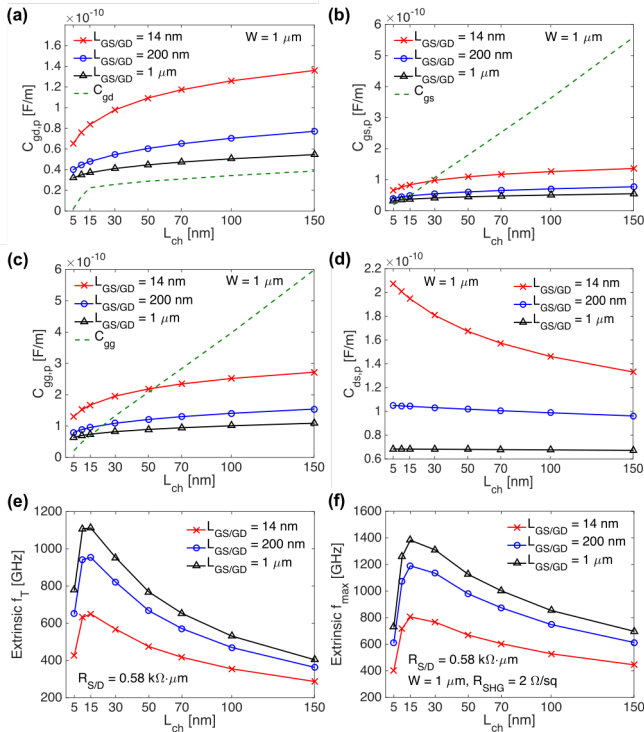


Fig. 6. Parasitic capacitances and their effects on extrinsic  $f_T$  and  $f_{max}$  with various  $L_{ch}$ . (a) parasitic small-signal gate-to-drain capacitance  $C_{gd,p}$ , (b) gate-to-source capacitance  $C_{gs,p}$ , (c) gate capacitance  $C_{gg,p}$ , and (d) drain-to-source capacitance  $C_{ds,p}$  as a function of  $L_{ch}$  for three different source/drain to gate metal distances  $L_{GS/GD}$  of 14 nm, 200 nm and 1  $\mu\text{m}$ , with a fixed  $W = 1 \mu\text{m}$ . In (a)–(c), dashed lines represent the intrinsic values for comparison. (e) Extrinsic  $f_T$  and (f)  $f_{max}$  as a function of  $L_{ch}$  with  $R_{SD} = 0.58 \text{ k}\Omega\cdot\mu\text{m}$ ,  $R_{SHG} = 2 \Omega/\text{sq}$  and  $W = 1 \mu\text{m}$ .

In practice, parasitic capacitance is one of the most important factors to consider when evaluating  $f_T$  and  $f_{max}$  as  $C_p$  is very sensitive to device size and geometry. Based on the planar device structure shown in Fig. 1(a), we calculate the parasitic capacitance using Eqs. (12a)–(12c), where metal line width ( $L_{SD}$ ), the spacing between the gate and the source/drain metal ( $L_{GS/GD}$ ), and the gate length ( $L_G = L_{ch}$ ) determine the parasitic capacitance. We used three different values of 14 nm, 200 nm and 1  $\mu\text{m}$  for  $L_{GS/GD}$  with  $L_{SD} = 200 \text{ nm}$ , and we have  $C_{gs,p} = C_{gd,p} = C_{dg,p}$  according to the conditions considered in this study. In Figs. 6(a)–(d), the parasitic capacitances are evaluated at various channel length for three different  $L_{GS/GD}$  and compared to their intrinsic values (dashed lines in Figs. 6(a)–(c)). As the metal lines are getting closer (with smaller  $L_{GS/GD}$ ), parasitic capacitances increase significantly at all channel lengths.

When a transistor is operated in the saturation region, the intrinsic  $C_{gd}$  is negligible, but its parasitic capacitance is not. For example, with  $L_{GS/GD} = 14 \text{ nm}$ ,  $C_{gd,p}$  is greater than  $C_{gd}$  by 3–4 times for the channel length from 15 to 150 nm as shown in Fig. 6(a). Therefore,  $C_{gd,p}$  plays an important role for the extrinsic  $f_T$  and  $f_{max}$ . On the other hand,  $C_{gs,p}$  and  $C_{gg,p}$  could be less critical since the intrinsic  $C_{gs}$  and  $C_{gg}$  are large in the saturation region, and impact of  $C_{gs,p}$  and  $C_{gg,p}$  would be relatively insignificant, especially for long channel devices, as shown in Figs. 6(b) and 6(c). However, our results reveal that  $C_{gs,p}$  and  $C_{gg,p}$  become comparable to or even larger than intrinsic capacitances for the short-channel devices. Moreover, as  $L_{GS/GD}$  decreases, the contribution by the parasitic components becomes more dominant in the total gate

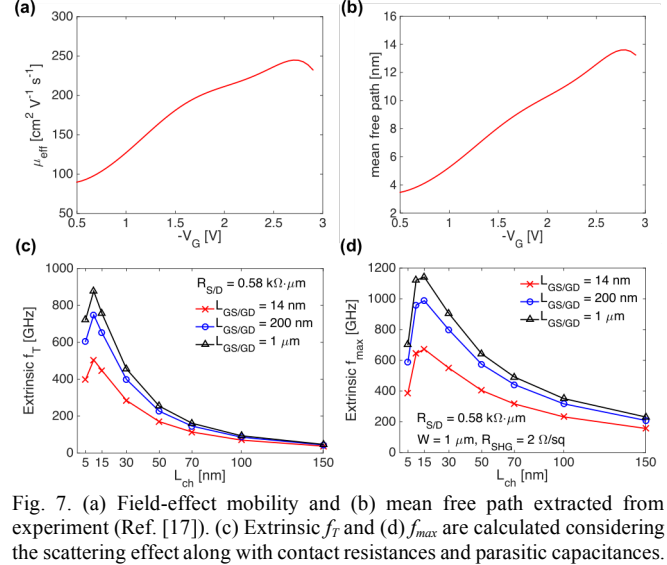


Fig. 7. (a) Field-effect mobility and (b) mean free path extracted from experiment (Ref. [17]). (c) Extrinsic  $f_T$  and (d)  $f_{max}$  are calculated considering the scattering effect along with contact resistances and parasitic capacitances.

capacitance  $C_{gd,p}$  for a given channel length, as can be seen in Fig. 6(c). Figure 6(d) shows  $C_{ds,p}$  for different  $L_{GS/GD}$  as a function of channel length, which exhibits that  $C_{ds,p}$  increases as the channel length scales down, unlike other parasitic capacitances discussed above, due to the strong interaction between source and drain metal lines.

Considering all parasitic capacitances and intrinsic ones along with contact resistance, we have plotted the extrinsic  $f_T$  and  $f_{max}$  in Figs. 6(e) and 6(f). When comparing these with the dashed lines in Figs. 5(a) and 5(b), we can clearly see the following distinctions. First, the values are significantly reduced. Second, the extrinsic  $f_T$  and  $f_{max}$  exhibit large degradation at extremely scaled channel lengths. The peak values are found at  $\sim 15 \text{ nm}$  channel: the maximum  $f_T$  varies from 600 GHz to 1.1 THz, the maximum  $f_{max}$  from 800 GHz to 1.4 THz under different parasitic capacitances.

### F. Effect of Scattering

So far, we have ignored the effect of scattering. Although we focus on relatively short channel lengths for the maximum  $f_T$  and  $f_{max}$  in this study, in order to minimize the gap between our assessment and the actual measurements, we take the effect of scattering into account using  $I_{proj} = \frac{\lambda_{max}}{L_{ch} + \lambda_{max}} I_{bal}$ , where  $\lambda_{max}$  is the peak mean free path of BP,  $I_{bal}$  is the ballistic current determined by the NEGF simulations, and  $I_{proj}$  is the projected current considering scattering [25]. To determine  $\lambda_{max}$ , we have taken the measurement data ( $I_D$ – $V_G$  plot) from Ref. [17] and followed the approach outlined in Ref. [40]. Figures 7(a) and 7(b) show the field-effect mobility and mean free path of black phosphorus. The extracted peak mobility is  $245 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ , which is in good agreement with Ref. [17] and the corresponding mean free path turns out to be 14 nm. The consequent  $g_m$  and  $g_d$  after considering the scattering effects are shown in Figs. 4(a) and (d) with dashed lines, respectively, where apparent degradation can be observed particularly for the long-channel devices. We assume that scattering has negligible impacts on intrinsic capacitance for the size of devices considered in this study [28], [41], and parasitic capacitance is determined solely by the device structure, not by scattering.

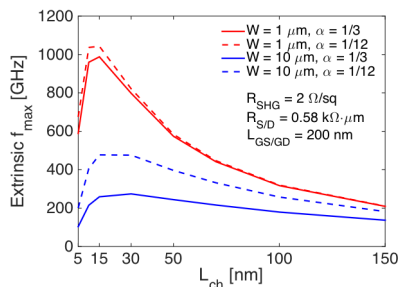


Fig. 8. The effects of device width and  $\alpha$  on extrinsic  $f_{max}$  at various  $L_{ch}$  with  $R_{S/D} = 0.58 \text{ k}\Omega\cdot\mu\text{m}$  and  $R_{SHG} = 2 \text{ }\Omega/\text{sq}$ , considering scattering and moderate parasitic capacitance ( $L_{GS/GD} = 200 \text{ nm}$ ).

The corresponding extrinsic  $f_T$  and  $f_{max}$  are plotted in Figs. 7(c) and 7(d) with  $R_{S/D} = 0.58 \text{ k}\Omega\cdot\mu\text{m}$ , moderate gate sheet resistance ( $R_{SHG} = 2 \text{ }\Omega/\square$ ) and  $W = 1 \text{ }\mu\text{m}$  for three different parasitic capacitances. The peak values can be found at  $L_{ch}$  of 10–15 nm. Although scattering affects the extrinsic  $f_T$  and  $f_{max}$  of long-channel devices significantly ( $f_T$  and  $f_{max}$  become only 50 GHz and 200 GHz, respectively, at  $L_{ch} = 150 \text{ nm}$ ), their impacts can be minimal for the short channel region where the peak frequencies are achieved. Even with scattering, the maximum  $f_T$  ranges from 500 to 900 GHz; the peak  $f_{max}$  from 650 GHz to 1.15 THz for different parasitic capacitances.

#### G. Effect of Device Width

In theory,  $f_T$  is not a function of device width since the units of both  $g_m$  in the numerator and capacitances in the denominator in Eq. (7) are given per unit width, and the width information is cancelled out. However, things will be different for  $f_{max}$  because the distributed gate resistance is proportional to the device width. We have studied the effect of  $W$  on the extrinsic  $f_{max}$  in Fig. 8 by considering  $W = 1$  and  $10 \text{ }\mu\text{m}$  under  $R_{S/D} = 0.58 \text{ k}\Omega\cdot\mu\text{m}$ ,  $R_{SHG} = 2 \text{ }\Omega/\square$ , and  $L_{GS/GD} = 200 \text{ nm}$ . In general, smaller device width is preferable for high  $f_{max}$ , and the peak  $f_{max}$  of  $W = 1 \text{ }\mu\text{m}$  is 5 times larger than that of  $W = 10 \text{ }\mu\text{m}$  with  $\alpha = 1/3$  (solid lines). Alternatively,  $f_{max}$  can be improved with a smaller gate resistance by using the gate terminal brought out from both sides, where  $\alpha$  becomes  $1/12$ . The blue dashed line in Fig. 8 indicates that huge improvement can be achieved with  $\alpha = 1/12$  if the width of device is large. For example, the peak  $f_{max}$  can be enhanced by 100% if  $\alpha$  is changed from  $1/3$  to  $1/12$  for  $W = 10 \text{ }\mu\text{m}$ . However, the gain of  $\alpha = 1/12$  can be quite small (less than 10%) if high  $f_{max}$  is already achieved with a small width ( $W = 1 \text{ }\mu\text{m}$ ).

#### H. Performance Limit Projection and Benchmark

Finally, the high-frequency performance limit is projected in Fig. 9 based on optimal device parameters to achieve the maximum  $f_T$  and  $f_{max}$ . By using  $R_{SHG} = 0.02 \text{ }\Omega/\square$  [20], [27] with  $\alpha = 1/12$ ,  $W = 1 \text{ }\mu\text{m}$ ,  $L_{GS/GD} = 1 \text{ }\mu\text{m}$  and  $R_{S/D} = 0.58 \text{ k}\Omega\cdot\mu\text{m}$ , the peak  $f_T$  of 900 GHz and the peak  $f_{max}$  of 1.2 THz are projected at  $L_{ch} = 10 \text{ nm}$ . In order to benchmark against experimental data [16], [17], we have extrapolated the simulation results up to 1- $\mu\text{m}$  channel length. The measurement data show  $f_T$  of 17.5 GHz and  $f_{max}$  around 14.5 GHz at 250 nm [17], which are still quite smaller than the values projected in Fig. 9. This indicates that there exists large room to improve in fabrication through optimization and engineering various parameters discussed in

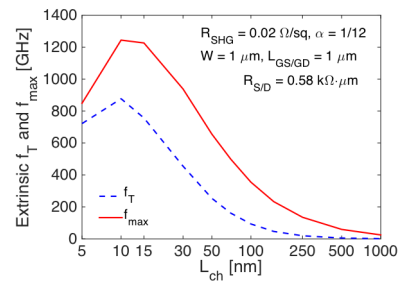


Fig. 9. Performance limit projection of extrinsic  $f_T$  and  $f_{max}$  at  $R_{S/D} = 0.58 \text{ k}\Omega\cdot\mu\text{m}$ ,  $R_{SHG} = 0.02 \text{ }\Omega/\text{sq}$ ,  $\alpha = 1/12$  and  $W = 1 \text{ }\mu\text{m}$ ,  $L_{GS/GD} = 1 \text{ }\mu\text{m}$ , considering scattering and small parasitic capacitance ( $L_{GS/GD} = 1 \text{ }\mu\text{m}$ ).

this study. According to our results shown in Fig. 9, realization of a short-channel BP FET is strongly suggested as both  $f_T$  and  $f_{max}$  exhibit significant improvement if  $L_{ch}$  becomes shorter than 100 nm. With an aggressive scaling of channel length, beyond THz  $f_{max}$  can be achievable with a BP FET, making it very attractive for the future high-frequency applications.

#### IV. DISCUSSION

Since BP has a highly anisotropic band structure, it would be useful to discuss the effect of different orientation. The main significance of heavier effective mass with zigzag orientation in the transport direction is twofold: (i) Ballistic current is reduced due to the small carrier velocity and the less number of transverse mode [42], [43]. (ii) Scattering mean free path becomes shorter due to the heavier effective mass, resulting in lower mobility, as supported by recent experiment [44]. Consequently, it is expected that  $f_T$  and  $f_{max}$  will be limited in zigzag transport direction as compared with armchair orientation. On the other hand, in theory, contact resistance would remain unaffected by different orientations since thermionic emission current in a two-dimensional system depends on density-of-states effective mass [45]. Recent experimental studies also exhibited that the measured current, transconductance, and field-effect mobility are significantly limited in zigzag orientation [39], [44], which indicates that the impacts of effective mass on the ballistic current, mobility, and scattering mean free path are not altered by the minimal influence of different orientations on the contact resistance.

In this study, we used the quasi-static approach considering the equivalent capacitive and resistive elements but neglecting the inductive elements, as is widely used in similar studies [28]–[32], [46], [47]. To validate our approach, we evaluated the LC characteristic frequency [ $f_{LC} = 1/(2\pi\sqrt{L_k C_{gg}})$ ] for the simulated BP FETs, using the kinetic inductance [ $L_k = (m^*/pq^2)(L_{ch}/W)$ ;  $p$  and  $q$  are hole density per unit area and elementary charge] and  $C_{gg}$  extracted from the simulated data, leading to  $f_{LC} \sim 9 \text{ THz}$  for 15 nm channel device. This is significantly higher than the peak frequencies of  $\sim 1 \text{ THz}$  evaluated in this study (Fig. 9), thus validating the quasi-static approximation. Nonetheless, further work will be needed to examine the exact role of kinetic inductance and non-quasi-static effects through time-dependent transport simulations, which is beyond the scope of this study.

## V. CONCLUSION

By using atomistic quantum transport device simulations and equivalent small-signal circuit model, high-frequency behaviors of BP FETs are studied. We have investigated intrinsic and extrinsic  $f_T$  and  $f_{max}$  considering source/drain contact resistance, parasitic capacitance, distributed gate resistance, and device width, and have discussed the impact of each device parameter on the high-frequency performance one by one. Our simulation results and assessment not only reveal the great potential of BP FETs for high-frequency applications, but also shed light on the proper direction to optimizations. The main points of this study can be summarized as follows:

- 1) BP FETs exhibit clear saturation behaviors with increasing drain voltage, unlike graphene FETs, resulting in  $>10$  THz frequencies for both intrinsic  $f_T$  and  $f_{max}$ . While intrinsic  $f_T$  increases monotonically with channel length scaling,  $f_{max}$  starts to degrade at  $L_{ch} < 30$  nm.
- 2) Although extrinsic  $f_T$  and  $f_{max}$  are significantly affected by contact resistance and parasitic capacitance, they can remain near THz frequency range ( $f_T = 900$  GHz;  $f_{max} = 1.2$  THz) through proper engineering, particularly with an aggressive channel length scaling ( $L_{ch} \approx 10$  nm).
- 3) In spite of significantly lower mobility of semiconducting BP compared to that of semi-metallic graphene,  $f_T$  of BP FETs can be comparable to that of graphene FETs. Moreover,  $f_{max}$  of BP FET is unconstrained due to large output resistance. Although the measurement data shows relatively lower values ( $f_T = 17.5$  GHz;  $f_{max} = 14.5$  GHz at  $L_{ch} = 250$  nm)[17] simply because BP FETs are still in their infancy yet, our assessment and benchmark indicate that there exists large room for optimization, suggesting further advancement of high-frequency performance of the state-of-the-art BP FETs for future analogue and RF applications.

## ACKNOWLEDGEMENT

The authors would like to thank Professor John Long for technical discussions. Demin Yin acknowledges the financial support by WIN Nanofellowship.

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