Real time resistance monitoring technology for microjoining process and reliability test

by

Di Xu

A thesis
presented to University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Doctor of Philosophy
in
Mechanical and Mechatronics Engineering

Waterloo, Ontario, Canada, 2017

© Di Xu 2017

Examining Committee Membership

The following served on the Examining Committee for this thesis. The decision of the Examining Committee is by majority vote.

External Examiner	JAN SPELT Professor
Supervisor	MICHAEL MAYER Associate Professor
Internal Members	MIHAELA VLASEA Assistant Professor KEVIN MUSSELMAN Assistant Professor
Internal-external Member	BOXIN ZHAO Associate Professor

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

New microjoining materials are needed for the soldering of electronic components due to environmental concern, reliability concern, and designing restriction. For example, a new low melting point solder is needed due to the thermal stress becoming more harmful as a result of thinner products. Development of such new microjoining materials is helped by fast methods for the testing of more candidate alloys in shorter time. This thesis describes the development of a real time resistance monitoring method, and the use of it to improve the understanding of microjoining process and reliability with four examples: current stressing of solder joints, solder reflow process, silver sintering process, and power cycling of solder joints, respectively.

In the current stressing of solder joints, a high constant DC current is applied to the Sn3Ag0.5Cu (SAC305) solder samples, and the sample resistance is recorded in real time. Complete resistance vs. time curves are obtained from start to failure. Four stages are identified from the resistance curve, and are explained with intermetallic layer growth, crack formation, crack healing and formation, and final open, as observed from cross sectional studies.

In the solder reflow process, two SnPb solder pastes with different levels of freshness are studied. Sample resistances are recorded during the reflow process. Simultaneous multiple sample monitoring is achieved. Characteristic resistance vs. time curves are obtained for both solders. Other than the initial resistance difference between the two solders, a special event of transient high resistance is observed for the older solder, and is explained with flux segregation between the solder balls and the lead fingers, as observed from cross sections.

In the silver sintering process, two special digital multimeters are integrated to cover a large range of resistance values (10^{-4}-10^{10} Ω). The setup can work in different modes, depending on the requirement of fast sampling rate, large resistance range, or massive data for statistics. The

resistance vs. time signal of the silver sintering process is obtained, and typically shows three stages: 1. dropping and rising forming a "V" shape in the range of ~10^4-10^{10} Ω, 2. steady resistance value of ~10^{10} Ω followed by an abrupt resistance drop to <1 kΩ, and 3. steady resistance drop to <1 mΩ. Differential scanning calorimetry (DSC) and cross sectioning are used for understanding resistance signals. As a result, the three stages are correlated to: 1. solvent evaporation, 2. capping agent degradation, and 3. silver sintering.

In the power cycling of solder joints, a total of two different PCB designs, and four solder materials are studied, including SAC305 and three solders that contain Bi. From the first PCB design with Sn57.6Bi0.4Ag solder, two failure modes are observed depending on the peak temperature. When the peak temperature is too high, the resistance signals show insignificant change, and the solder joints becomes grainy. When the peak temperature is moderate, resistance signals show rise until open, and cracks are observed from cross sectioning studies of failed samples. From the second PCB design with a larger resistor size, under the same stressing condition, the Sn57.6Bi0.4Ag solder joints show insignificant resistance change and become grainy in appearance, while all other three solders show resistance rise until open and interfacial cracks in cross sectional studies.

In summary, new methods are developed with real time resistance monitoring technology to study solder joints reliability and microjoining processes. More knowledge is learned for the solder joints reliability such as the finding of crack healing events, and for the microjoining processes such as the discovery of flux segregation.

Acknowledgments

I thank my family for the support during my entire PhD program.

I thank my supervisor Prof. Michael Mayer, for his warm welcome when I first came to Canada, for his always patient education such as explaining the difference between “sparkling” and “sparking”, for correcting my attitude from “hurting” to “enlightening” when my manuscript was rejected, for being a role model with his strictness and humbleness, for his generosity with his time and ideas, for his support when my daughter was born, for his financial aid with his research grant, which is enough to cover my living cost and my tuition fees, and for his last two pieces of advice before my defense “sit before it starts” and “be humble and confident”. For all he has done for me, I can never thank him too much.

I thank Prof. Jae Pil Jung from University of Seoul, the collaboration with whom kicked off my thesis work. He has kindly given me valuable feedbacks on my work with his broad knowledge on materials science, and warm personality.

I thank all my grad student group fellows Michael Hook, Nhat Ly, Jimy Gomes, Alireza Rezvani, Ari Laor, and Depayne Athia for being such nice co-workers, especially Michael Hook, who has shared with me the longest overlapping time in this research group. I thank all the co-op and volunteering students who worked with me: Jasper Chow, Kieran Ratcliffe, Jang Baeg Kim, Megan Jordan, Shuyue Wang, and Jiayun Feng.

I thank all external partners and UW researchers for their support with materials, knowledge, and equipment including but not limited to: Alex Chen in Celestica Inc., Geoff Rivers in UW, Robert Lyn and John Persic in Microbonds Inc., and Watlab in UW.

Last but not least, I thank Prof. Jan Spelt, Prof. Mihaela Vlasea, Prof. Kevin Musselman, and Prof. Boxin Zhao for their careful review of my thesis, and their attendance in my defense.

Table of content

List of Figures

List of Tables

Chapter 1 Introduction

Small or large, common or special, microelectronics packaging technology is used today in many products ranging from credit cards to satellites. Microelectronic packages have the purposes of power distribution, signal distribution, heat dissipation, and mechanical protection of an integrated circuit (IC) chip [1]. Figure 1.1 shows three different levels of electronics packaging in a typical product [2]. For the first level packaging, the semiconductor chips are connected with the leads of the package. For the second level packaging, small packages are connected onto the printed circuit boards (PCBs). The first and second levels packaging usually involve metallurgical joining process such as wire bonding, soldering, and/or isotropically conductive adhesives (ICAs). For the third level packaging, the PCBs are connected onto a mother board, usually with mechanical fixing methods.

A typical cross-sectional illustration showing four stages of packaging corresponding to the first and second level packages is shown in Fig. 1.2 [3]. For the first stage, the chip is mounted to the substrate, usually with adhesive bonding, eutectic bonding, or brazing or soldering. For the second stage, the chips are connected to lead-outs, usually with wire bonding or soldering. For the third stage, the package lid is sealed, usually with adhesive bonding, brazing or soldering, glass sealing, or welding. For the fourth stage, the package is connected to the PCB, usually with soldering, ICA bonding, or parallel-gap resistance welding [3].

1.1 Issues

The main current challenges for microelectronics packaging technology include the continuous miniaturization of IC chips and various product designs. New processes and new joining materials have been continuously investigated to help overcome the challenges.

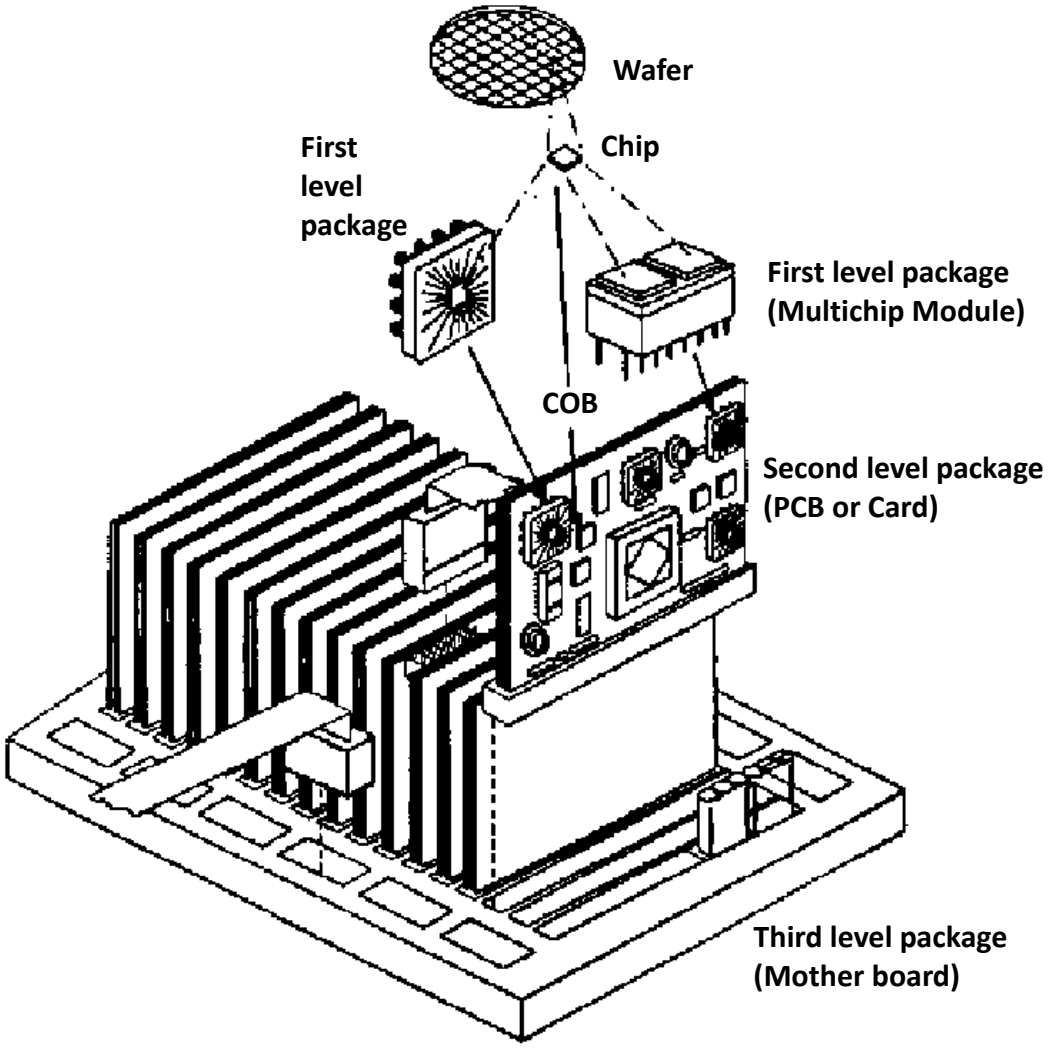

Figure 1.1. Three levels of packaging in microelectronics. [2]

There are some successful new joining materials that have been utilized, and even become the mainstream in the field of microelectronics packaging. For example in wire bonding, Au wire used to be the mainstream, but nowadays Cu wire has overtaken Au due to the high cost of Au. Another example is the Sn-Ag-Cu (SAC) solder replacing SnPb solder due to the environmental concern associated with Pb. Nevertheless, most of the new materials have their own issues and are therefore used with their own specific processes. For instance, Cu is harder and has shorter shelf life than Au, and SnAgCu solder requires a higher reflow temperature than SnPb. Therefore, it is still required to search for new joining materials.

However, selecting a new material requires a lot of effort and resources including full characterization of the new material. The lack of a fast method to acquire information on a new material can slow down process development and/or improvement, and therefore slows down the start of production. Therefore, a fast screening method is needed for testing the materials performance in joining process, and the reliability of the final joint.

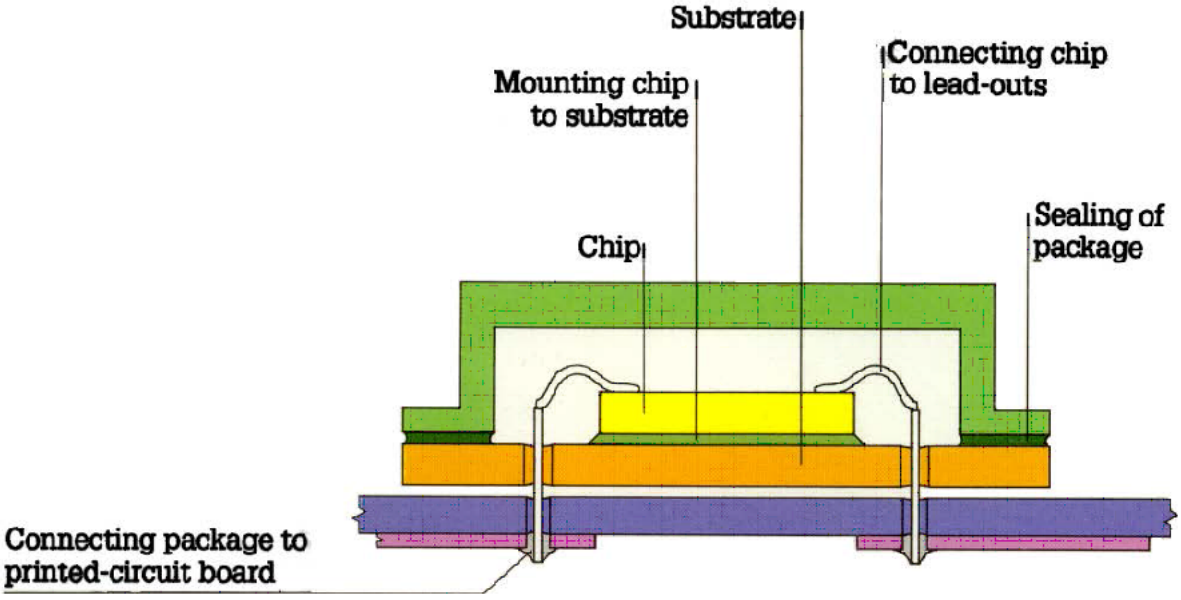

Figure 1.2. Cross-sectional illustration of a package and the four stages of packaging. [3]

1.2 Objectives

This study aims to help improve the quality of the solder joints in industry. The study includes development of new fast non-destructive methods for real-time monitoring of new joining materials during joining process as well as reliability test. Example joining materials are either commercially available or to be provided by an industry partner. The new method together with some traditional metallurgical studies lead to new understanding of the joining process as well as the failure mechanism. The two main objectives are:

(A) Development of new accelerated methods with real time resistance monitoring for solder joints reliability test to qualify new solder materials.

(B) Improve understanding of the joining process, failure mechanisms, and the effect of parameters on quality / failure of the joints, based on real time resistance monitoring during solder reflow.

1.3 Thesis organization

In this thesis, a real time resistance monitoring and power cycling technology is developed for studying the performance of microjoints, and the microjoining processes.

Chapter 1 introduces some background information, current issues in the industry, the objectives, thesis organization, and the current level of knowledge and technology achieved in solder joints electromigration, soldering process, and silver sintering process.

Chapters 2-5 show four examples studies with real time resistance monitoring technology, and are solder joint current stressing, solder reflow, silver sintering, and solder joint power cycling, respectively. All four example studies focus on resistance monitoring technology, while other methods such as cross-sectioning, finite element modelling (FEM), and/or differential scanning calorimetry (DSC) are also used to help understand the features in the different stages observed from resistance signals.

1.4 Literature review

1.4.1 Solder joint electromigration

Whether in chip-scale joining such as flip-chip [4] or in package scale joining such as surface mount technology [5], the solder joint is required to be reliable, especially in harsh applications such as in aerospace.

Electromigration is an atomic migration phenomenon caused by electrons colliding with ions when current, especially high density current, flows through the material, typically metal. Electromigration induced failure is a common failure mode in solder joints, and avoiding electromigration is more challenging with advancing miniaturization of microelectronics connections. The same current results in higher current density in a thinner connection, thus increases the electromigration rate. For example, the peak current density in a flip-chip joint was found to be twelve times higher than the average current density [6].

To study solder joint electromigration, current stressing tests are used. Research has been reported on electromigration of solder joints [7-12]. Particles or nanoindentations were used as markers to study electromigration rate of solder joints, and eutectic SnPb is found to have faster electromigration rate than SAC [7, 8]. Electromigration can also result in protruding of grains due to the stress caused by massive migration of atoms, and this phenomenon was also used to study solder joint electromigration [8, 9]. In some soldering alloy systems such as SnPb, where different elements have obviously different electromigration rate, an element distinguishable method such as scanning electronic microscopy (SEM) with back scattered electron signals can be used to study the joint electromigration [10, 11]. However different electromigration rate of

elements is not seen in SAC solder alloy. Other microstructural observations including cracks, voids, and intermetallic compounds (IMCs) have been discussed in [12].

Example cross sectional images of solder joints that undergoes electromigration are shown in Figs. 1.3a, and b, showing element separation, and interfacial voids formation, respectively [11, 13]. The sample in Fig. 1.3a is a SnPb eutectic solder bump that was subjected to 0.6 A current at 135 °C for 306 h. The sample in Fig. 1.3b is a Sn–3.5Ag lead-free solder bumps with a Cu-based UBM stack that was subjected to 5.16×10^4 A/cm^2 current at ~140 °C for 300 h.

Non-destructive signals from solder connections during current stressing tests are used to obtain more data and understand the aging mechanism better. For example, joint resistance is measured non-destructively during current stressing test [14, 15]. Joint resistance is essential for the performances of microelectronics devices. Chang et al. [14] have demonstrated that the four wire method is very sensitive to void formation and propagation at solder joint interface, and can

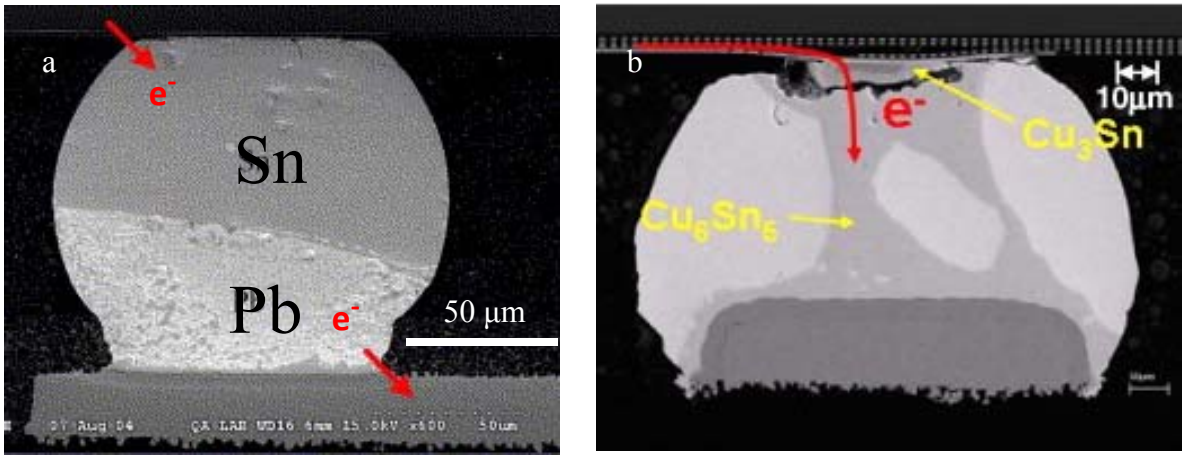

Figure 1.3. Cross sectional images of example solder joints that undergoes electromigration showing: (a) element separation [11], and (b) interfacial voids formation [13].

be adopted in studies of current stressing test systematically. Lin et al. [15] explained the behavior of the resistance aging curve being either concave down or up, depending on whether the IMC growth or crack formation is dominant, respectively, and on the direction of IMC growth. The technique in this thesis adopts the same idea as in [14, 15], while solder sample preparation is on a single substrate instead of two, as described in more detail in Chapter 2.

1.4.2 Solder reflow process

Reflow soldering is widely used in the electronic packaging, especially in surface mount technology (SMT). In a typical reflow soldering process, solder paste is firstly dispensed on the bonding pads, the surface mounted devices are placed afterwards, and the entire PCB is heated to melt the solder for permanent connection of the surface mounted device onto the PCB. Figure 1.4 shows factors, mechanisms, and responses attributed to a typical solder reflow process [16, 17].

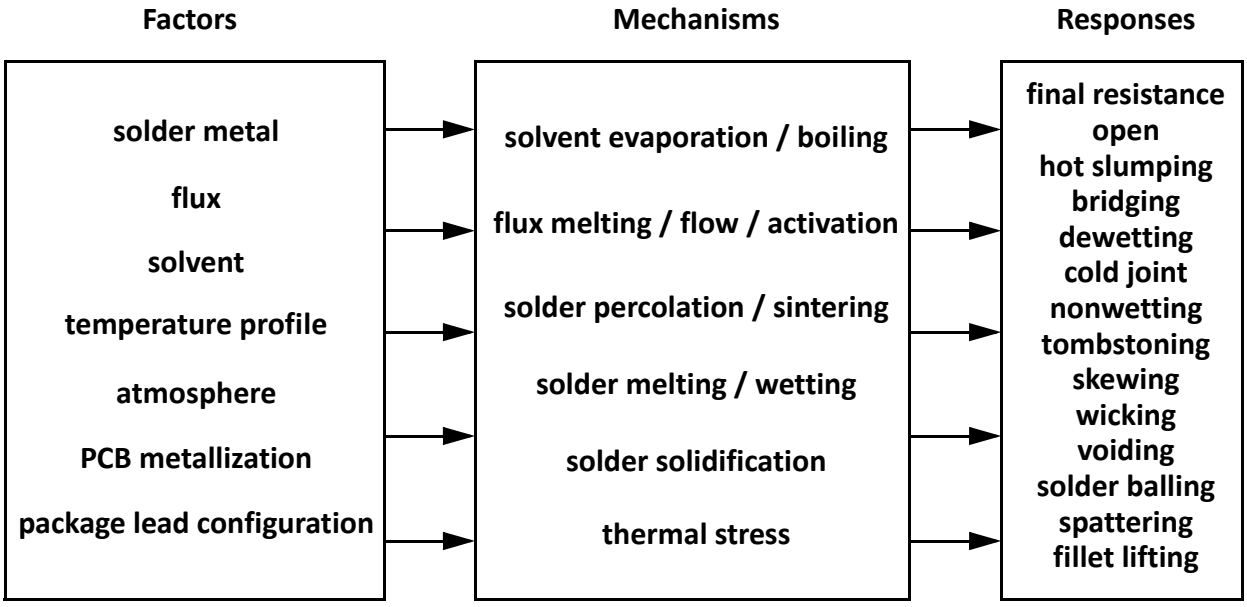

Figure 1.4. The factors, mechanisms, and responses of a typical solder reflow process. [16, 17]

Usually solder bumps, and/or solder paste are used. Solder paste is a mixture of tiny solder balls (typically 25-45 μm) and flux. A typical flux consists of three chemicals, namely rosin, solvent, and activator. Solder and flux properties are carefully adjusted to achieve good wetting and oxidation prevention during soldering. When heated to a high enough temperature, the solder melts, flows, and wets the metallizations on both sides of the connection. Upon cooling the solder solidifies without significantly changing its geometry, forming the final solder joints. However, when coming to lower melting point solders, smaller solder joints, or thinner substrates, classical failure modes such as tombstoning [18], skewing [18], bridging [19], and/or spattering [20] can need attention, as described in chapter 6 of [16].

Tombstoning is the lifting of one end of a leadless surface mounting device (SMD), with the other end connected to the PCB board. It results in an open circuit fault. Skewing is the horizontal movement of the SMD that results in misalignment, and may be considered as early stage of tombstoning. The factors causing tombstoning also typically aggravate skewing. Bridging is solder joining between neighboring solder pads due to excessive solder material. This results in a short connection fault. Spattering is a phenomenon where solder paste flies away from the desired solder joint by up to a few millimeters and can result in either opens or shorts.

Non-destructive real time methods have been used for reflow process monitoring. They include imaging [21-23], temperature distribution on board [24], Auger electron spectroscopy [25, 26], warpage [27, 28], and differential scanning calorimetry (DSC) [29]. They are helpful for improving the process understanding for solder reflow. They can be achieved with little disturbance caused by the monitoring technique. Moreover, an efficient and low cost non-destructive method to acquire information on a solder reflow process can be important for process control and/or solder candidate selection, so as to optimize the final solder joints.

Huang et al. [21-23] used synchrotron radiation X-ray real-time imaging technology to investigate the evolution of interfacial intermetallic grains during reflow soldering, and revealed that the pre-existing intermetallic compounds dissolve into the molten solder when the solder is liquid, and new intermetallic compounds form at the interface during cooling stage.

Srivalli et al. [24] numerically and experimentally investigated the heat flow during the cooling stage of a solder reflow process, and found that the solder joints cool slower than the surrounding materials both before and after solidification.

Bozack et al. [25, 26] discovered in situ segregation of carbon on the solder surface during heating until above melting point of Sn based solder alloy using real time Auger electron spectroscopy. Carbon pre-exists as bulk alloy contamination at room temperature, gradually segregates onto the surface as the temperature rises, and inhibits wetting on non-reactive surface without flux.

Chung et al. [27] and Tsai [28] evaluated warpage of printed circuit board assembly during reflow process, and showed a simulation method to help predict warpage issue in the design stage before mass production.

Zhou et al. [29] used DSC to study premelting behavior of Sn/Cu, and Sn/Ag interfaces. Resulting from the atom interdiffusion and the eutectic reaction, the two systems were found to premelt at temperatures lower than the melting point of pure Sn by 4.9 °C and 10.6 °C respectively.

However, all these methods only sense optical, chemical, thermal, or mechanical signals, with a lack of resistance signals, which is an important property for micro joints. Real-time resistance monitoring is a non-destructive measuring method and has been used in reliability studies [30-31]. With fast enough sampling rates, transient behaviors can also be recorded in a process

such as solder reflow, but this has not been reported yet to the knowledge of the author of this thesis.

1.4.3 Silver sintering process

Silver sintering pastes (SSPs) are used as die attachment material in microelectronics packaging, especially for power electronics devices [32]. Some SSPs have lower bonding temperature than most solders, and can survive a higher temperature than some solder joints once bonded [32]. In [33-35], SSPs are added to epoxy based isotropically conductive adhesives (ICAs) to adjust the conductivity.

Silver sintering pastes are typically mixtures of solvent, capping agent, and silver micro and/or nano particles. The silver particles are usually in the shape of flakes/spheres and covered with a capping agent to avoid low temperature sintering. The silver sintering process is, for example in [36], a sequence of solvent evaporation, capping agent degradation, and silver sintering in elevated temperature according to the thermal gravimetric analysis (TGA). Generally, the smaller the particle sizes, the lower the sintering temperature needed [37]. Magdassi et al. have achieved room temperature sintering of 10 nm silver particles, where the degradation of the capping agent [poly(acrylic acid)(PAA)], is triggered by adding cationic polymer, [poly(diallyldimethylammonium chloride) (PDAC)] [38].

Despite the advantages of low process temperature, challenges remain for the current SSPs, such as the requirement for pressure to densify the joint, which reduce the yield [39]. To overcome such challenges, better SSP sintering process knowledge is required.

To improve the understanding of SSP sintering processes, a common way is to prepare samples at various sintering temperatures and times [36-38]. The samples are analyzed with microscopic images, thermal/electrical conductivity measurement, and shear/tensile test.

For example, Hu et al. [37] studied the tensile strength of silver sintering paste joint between copper wire to copper pad obtained at five temperatures between 100 °C and 300 °C. They found that the tensile strength increases with temperature for 250 μm wire, and remains unchanged with 50 μm wire.

Alternatively, in-situ monitoring can provide real-time information for the sintering process, and transient phenomena can be studied with a fast enough sampling rate. A common in-situ monitoring technology to study SSP sintering process is thermogravimetric analysis (TGA) [32, 36, 40, 41].

For example, Lu et al. [36] used derivative TGA to study six SSPs with different capping agents, and the same solvent (α-Terpineol). For all the SSPs studied, the capping agent degradation happens after or in the end of solvent evaporation. Specifically, silver 2-ethylhexanoate decomposes at the lowest temperature of 190.3 °C. After 350 °C/30min processing, sintered silver is observed if the capping agent degradation temperature is lower than 250.2 °C.

Lately, resistance monitoring technology has been applied to study the curing process of epoxy-based ICA [42-45], while such study on SSP sintering process is not found. Inoue et al. [42-44] found that the change of electrical conductivity can not only be caused by curing reaction of the binder molecules, but also the conductivity change of the inter-filler chemicals, by comparing resistance signals with results from free-damped oscillation method.

Xiong et al. [45] obtained resistance-time curve with ICAs of 65 wt% silver fill loading. The resistance value becomes detectable (< 2.0 MΩ) at 27 min. The resistance drops gradually to

1.4 kΩ at 40 min, and to 8.8 Ω at 80 min, after when the resistance remains unchanged. The resistance decrement is explained with the epoxy resin shrinkage leading to an increase in the contact area between the fillers, which promote the formation of conductive pathways between the filler particles during the curing process.

In summary, in previous studies with resistance measurement for ICA curing process, the resistance values are measured at a few (<20) curing times and/or temperatures [36, 42, 44-48], and/or monitored with a slow sampling rate [45]. Some studies [34, 42-44] have missing resistance values because of the range limit of the Ohm-meter used.

1.5 Summary

In order to help development of new microjoining materials, the solder joint electromigration, solder reflow process, and silver sintering process have been studied with various experimental and numerical methods. This thesis develops new methods to study the above mentioned three topics, as well as power cycling behavior of solder joints. The advantage of the new methods include: lower cost, provide new/improved signals, and simultaneous multi-sample test for fast statistical results.

The new methods are used together with traditional metallurgical methods to improved understanding of the four topics: solder joint electromigration, solder reflow process, silver sintering process, and power cycling of solder joints. The four topics are described in detail in Chapters 2-5, respectively.

Chapter 2 Real time resistance monitoring (RTRM) in current stressing of SAC305

The work described in this chapter has been partly published in [31]. It is about real time resistance monitoring of one single solder joint with four-wire method in a high current stressing condition. It is a collaboration of UW and University of Seoul (UoS). Our partners at UoS contributed the design and fabrication of the test substrate to this work. The contributions I made include the measurement of the resistance signals, finite element modelling, and the cross-sectioning studies.

Section 2.1 describes the preparation of a SAC305 solder bump with 800 μm diameter onto a custom substrate with Cu lines as leads that allow for resistance measurement during current stressing. Section 2.2 describes the current stressing and the real time measurement method. Section 2.3 shows the current distribution with a finite element study. Section 2.4 shows the sample resistance change during current stressing test, and joint interface evolution with cross sectional studies. In Section 2.5, the correlation between the observations from Sections 2.4 is discussed and possibly explanations are given.

2.1 Sample preparation

Figures 2.1a-d show the top views and cross-sections of a typical sample solder joint before and after reflow, respectively. The sample material is a standard lead free SnAgCu (SAC) solder wire purchased from MG Chemicals (catalog number: 4900-112G). The SAC solder has a composition of 3 ± 0.2 wt.% Ag and 0.5 ± 0.2 wt.% Cu (SAC305). Several 0.79 mm long sections are

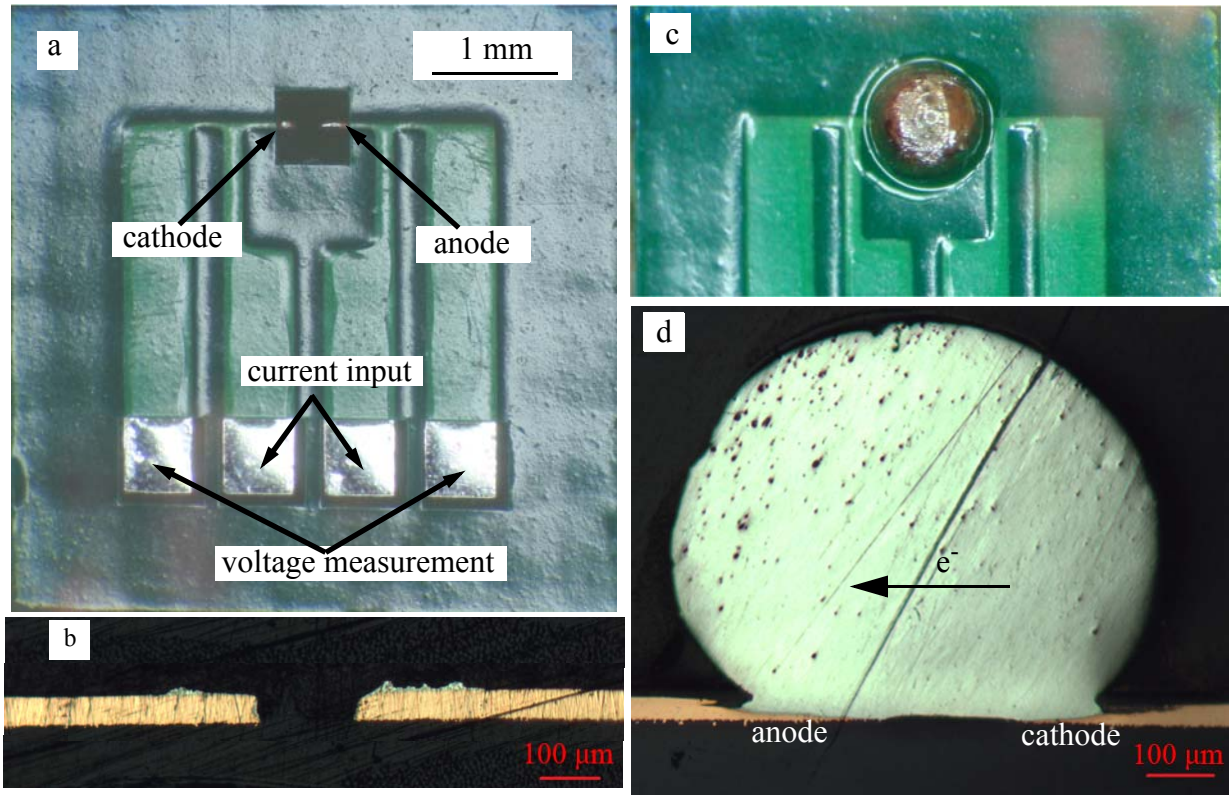

Figure 2.1. The top views (a, c) and cross-sections (b, d) of a test substrate before (a, b) and after (c, d) reflowing of a SAC solder bump. The thicknesses of the copper lines and solder resist are 35.4 ± 1.7 µm and 14.3 ± 0.6 µm, respectively. The average horizontal diameter and height of the solder bumps are 869 ± 33 µm and 710 ± 10 µm, respectively. Errors are standard deviations and samples sizes are 5 for all the measurements.

cut from the solder wire, placed on custom designed test substrates, and heated inside an Omega-lux LMF-3550 oven with a heating rate of 20 °C/min. After 2 min reflow at 240-250 °C, the oven is turned off and the door is opened until the samples cool down to room temperature.

The reflowed solder bumps are subsequently used for high current stressing tests in which current would appear to flow laterally from one side of the ball to the other, a situation different from the usual configuration where current flows vertically through the solder joint. However, the numerical results for our solder bumps show current mainly flows vertically following the path of least resistance into the solder as described in Section 2.3. Figure 2.1d shows substantial dissolution of the copper lines into the solder ball which is typical for SAC solder [51].

2.2 Current stressing test

Figure 2.2 shows the scheme for the current stressing experimental setup. A high current stressing test is used to evaluate the reliability of the solder bump in terms of electromigration. The four wire method is used to measure the joint resistance, as shown in Fig. 2.1a. The four soldering pads on the substrate (see Fig. 2.1a) are soldered to polytetrafluoroethylene (PTFE) insulated wires with SAC305 solder, as shown in Fig. 2.3. To accelerate the aging test, the ambient temperature of the sample is elevated to 160 °C. This temperature level was chosen as high as possible without melting the solder bump together with the thermal input from Joule heat from the

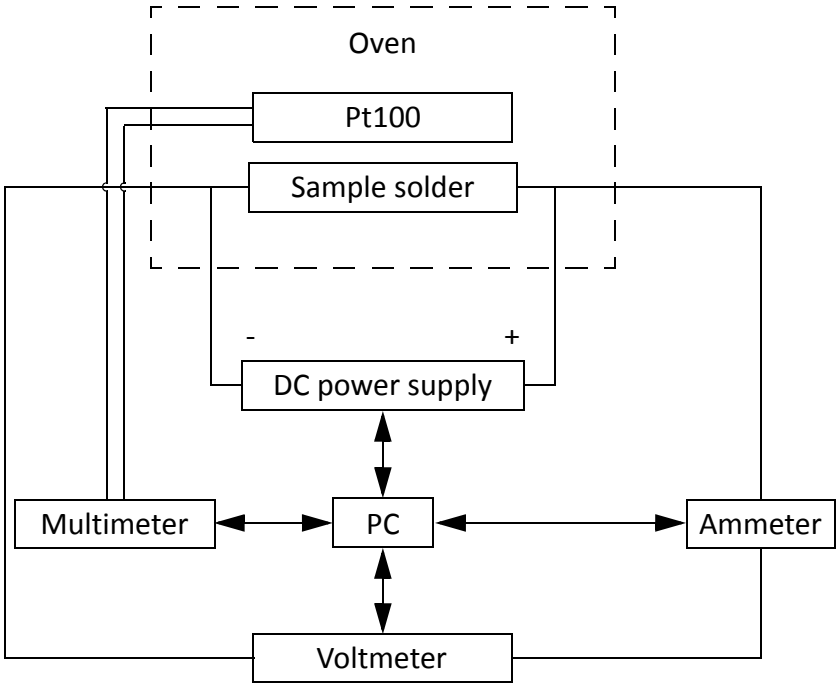

Figure 2.2. Scheme for current stressing experiment setup. Arrows indicate communications, and the lines without arrows indicate electrical connections.

aging current. To minimize sample damage from thermal shock [52, 53] that results from abrupt temperature change, the sample is heated and cooled inside the oven, instead of transferring sample from room temperature into preheated oven or removing sample directly from hot oven to room temperature. The effect of 160 °C thermal aging alone is assumed to be negligible since there is no resistance change.

The aging current is chosen as 2.2 A after several trial and error experiments to find that higher currents result in too much Joule heat and melt the solder bump while lower currents result in no obvious change in observation during 200 h. The current source is a programmable DC power supply with a current resolution of 1 mA and a current range of 5 A. No discernible drifting is seen from recorded output of the power supply over 16 h. A custom software is designed to control the power supply remotely from the PC. The software is typically used through a com-

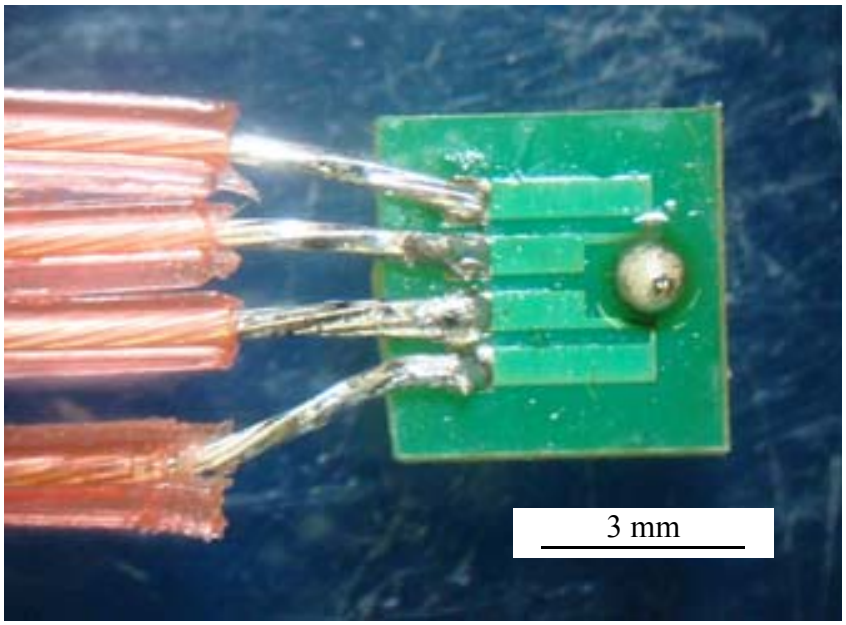

Figure 2.3. Top view of the sample after PTFE wires are joined to the soldering pads.

mand prompt with a Microsoft Windows operation system to send commands through USB port. The sample resistance is monitored with 0.1 A current before switching to 2.2 A stressing current.

A Pt100 temperature sensor is placed near the solder bump inside the oven to monitor the temperature during the test. The temperature and the current are measured with two Keithley 2700 digital multimeters, respectively. An Agilent 34401A digital multimeter is used to measure the voltage. A custom Matlab program is designed to automatically control the power supply, and to record the temperature, voltage, and current throughout the aging test in 4 s intervals. The flow chart of the Matlab program is shown in Fig. 2.4. The file name of the Matlab code is RmonitoringEM_v20170802.m. It is available for download from matlab central [54].

As a result of the substrate geometry and four wire method, the resistance measured also includes part of the copper lines (see Fig. 2.1d), which cannot be measured directly. To better understand the contribution of the copper lines to the resistance signal, the current distribution in the sample, and the contribution of various failure modes to the resistance increase during aging, an FE model is built and explained in the Section 2.3.

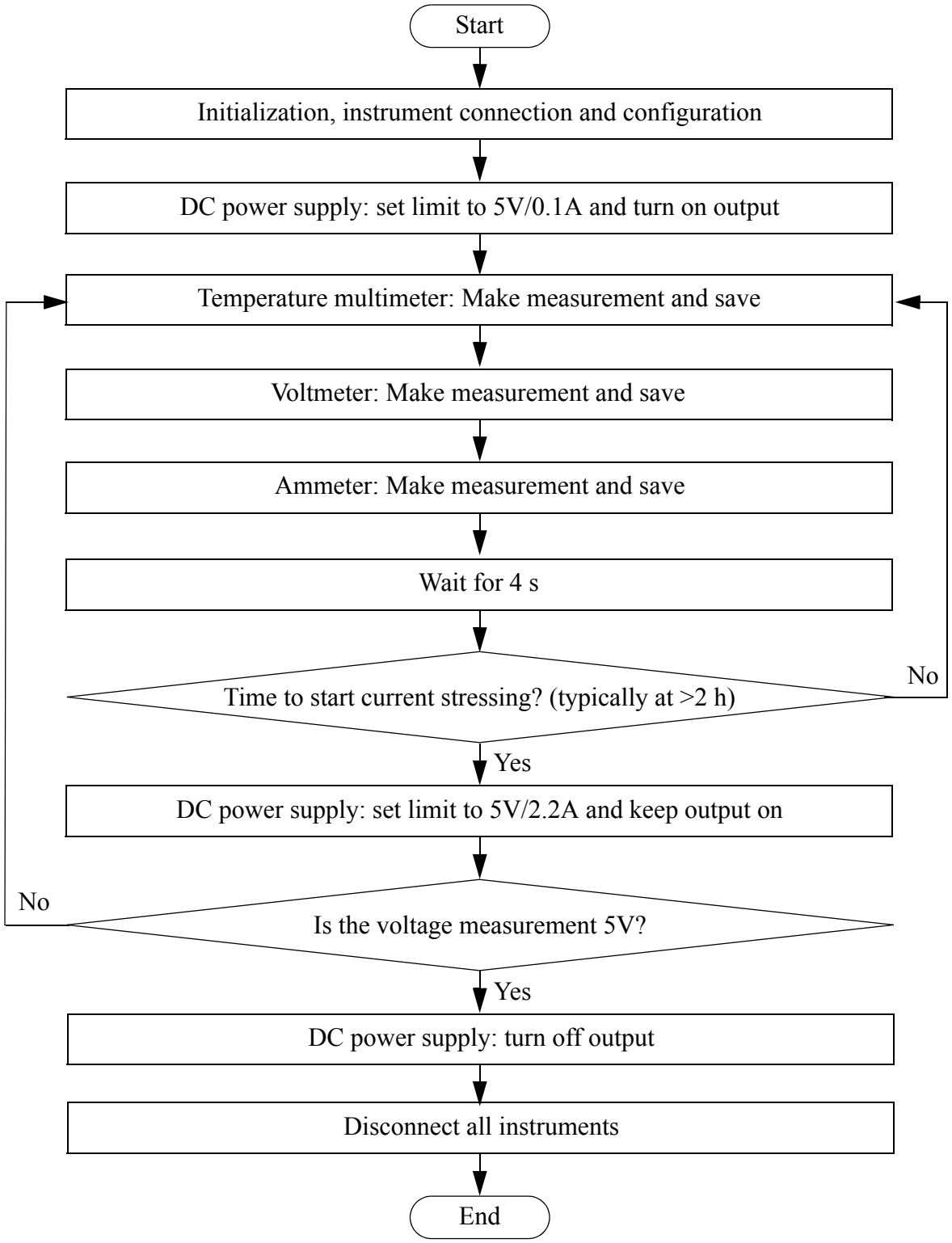

Figure 2.4. Matlab program flow chart for the aging test. (File name: RmonitoringEM.m; Available online at [54] and [55])

2.3 Distribution of Current in Solder Ball (FE Model)

The software used for the FE study is COMSOL 4.3b. Only DC current is simulated. The geometry is modelled in 3D with components shown in a cross-section in Fig. 2.5 with dimensions. The dimensions are chosen to match the measured values. Figures 2.6a, and b show the 3D image, and the mesh, respectively. For simplicity, only two parts of the copper lines, and the solder bump are modelled and any IMCs are neglected. The width of the copper lines is 68 µm, and the diameter of the solder ball is 792 µm. The geometry was meshed with 451224 tetrahedral elements. The calculation lasted about 27 s on a standard PC.

The electrical conductivity values and the resistance values at room temperature and 160 °C are shown in Table 2.1. The solder bump resistance is calculated from the average simulated voltage drop between the two solder/copper interfaces. The copper conductivity is from [56] and the

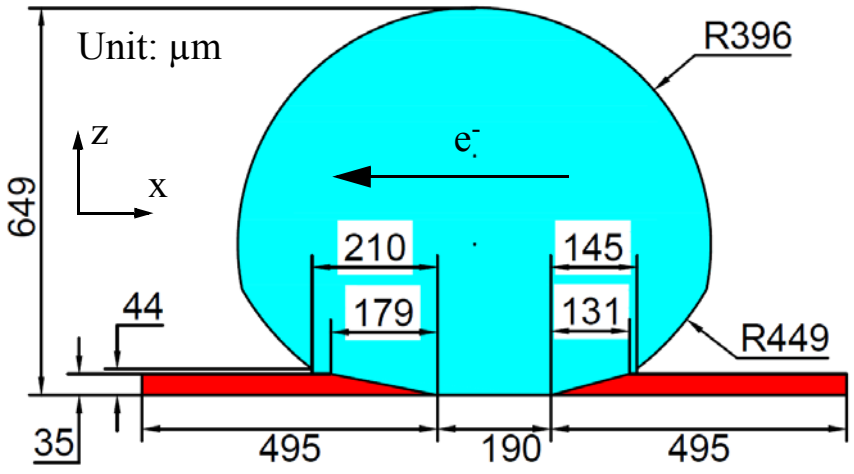

Figure 2.5. Illustrative cross-section of the 3D FE model of solder bump. Cu line width is 68 µm.

SAC conductivity is measured from the as received solder wire. The total resistance is calculated from the voltage drop between outer ends of the copper lines for an applied current of 2.2 A, resulting in a current density of 924 A/mm^2 in the Cu lines.

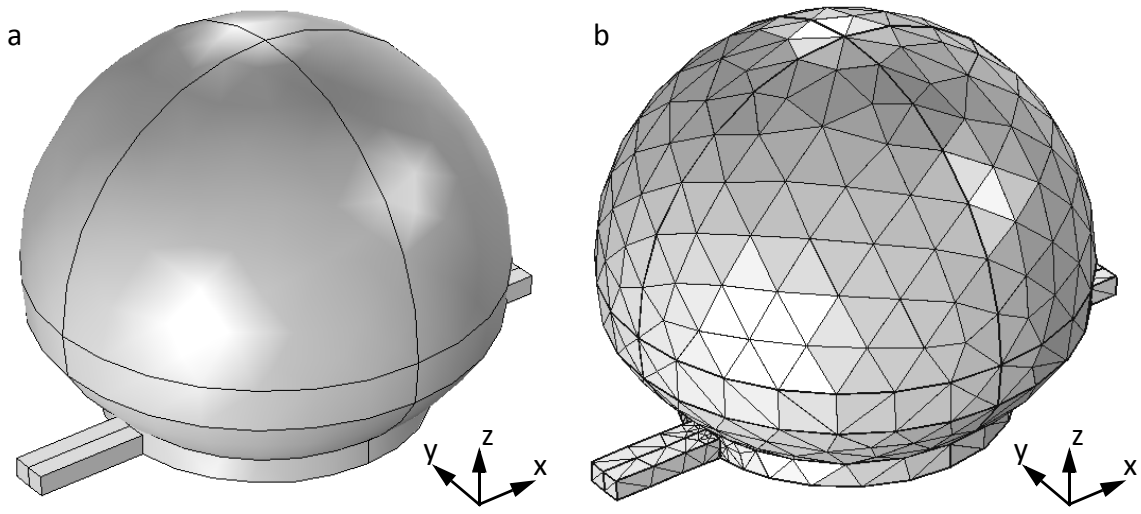

Figure 2.6. The (a) 3D image, and (b) mesh of the FE model

Table 2.1. The electrical conductivities and the calculated resistances in the FE model

	20 °C	160 °C
Copper conductivity [S/μm]	59.6	38.7
SAC conductivity [S/μm]	7.99	4.90
Total resistance [mΩ]	5.94	9.24
Solder bump resistance [mΩ]	0.84	1.36

The current density distribution on the cross-sectional plane of the FE model is shown in Fig. 2.7a. The current density distribution along the cathode interface in this cross-sectional plane is shown in Fig. 2.7b. The current density first drops, and then rises along the interface form point I to II. The highest current density along the cathode interface is at point II in Fig. 2.7b. The highest current densities along the cross-sectioned interfaces are 423 A/mm^2 on cathode side and 394 A/mm^2 on anode side, respectively. The difference is due to the difference in interface length (Fig. 2.5), which is measured from Fig. 2.1d, and varies during current stressing.

The highest current density along the interface is at point II and is directed mainly in vertical direction as shown by the numerical result in Fig. 2.8. The current flows mainly vertically at the SAC-Cu interface since the path of least resistance is through the bulk of the bump, rather than through the more direct but thinner path at the bottom of the bump. Such vertical current flow is consistent with the case of ball grid array (BGA) solder joints interfaces.

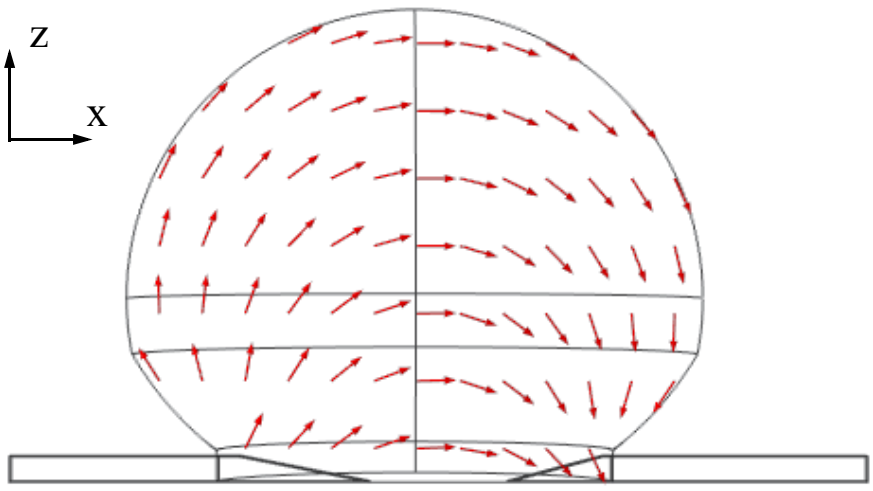

Figure 2.8. Simulated current direction distribution in the cross-sectional plane of the SAC solder bump during current stressing test. Most of the current flows vertically into the bump at the solder/Cu line interface. The arrow size is normalized.

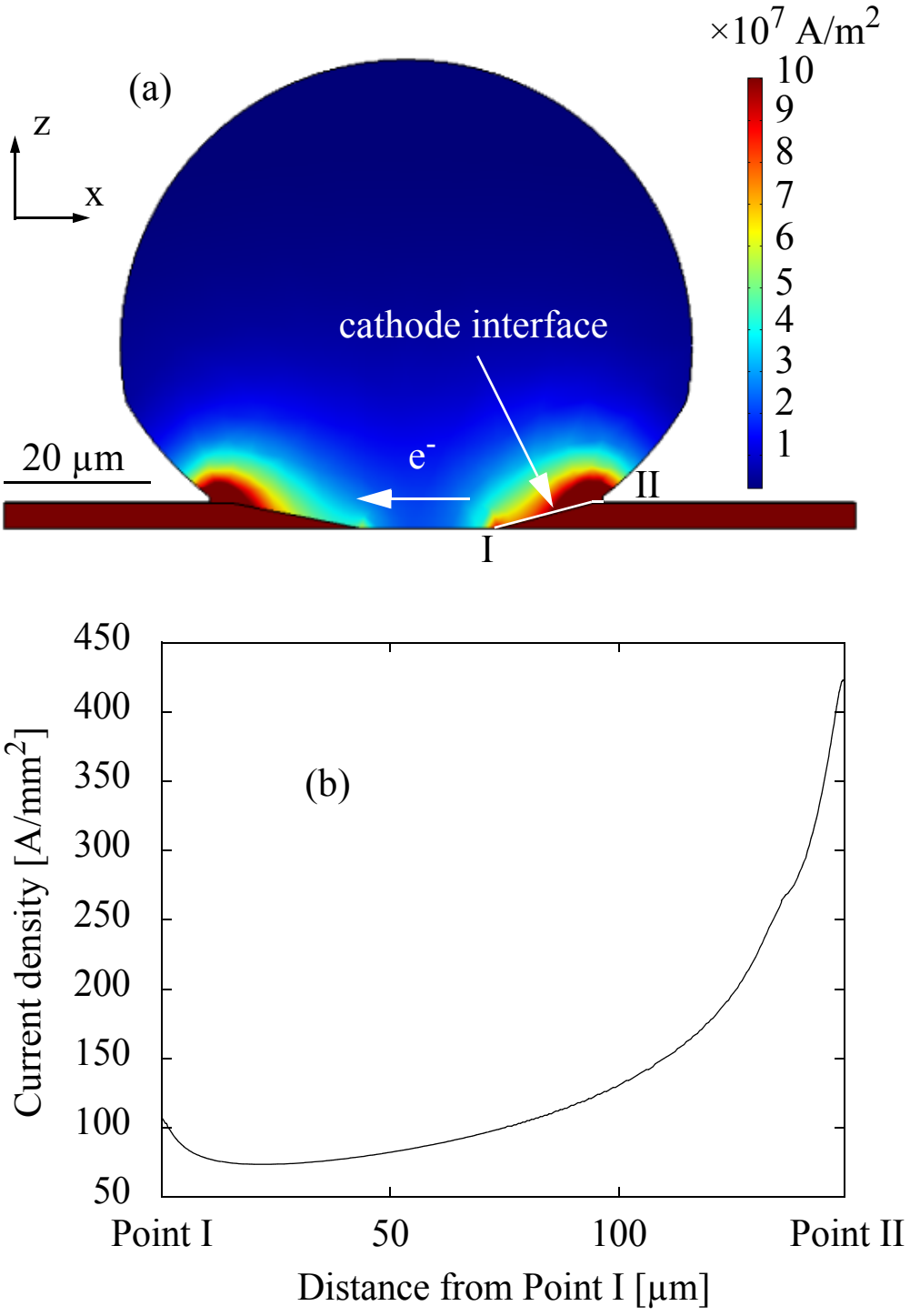

Figure 2.7. (a) Simulated current density distribution in the cross-sectional plane of the unaged SAC solder bump during current stressing test at 160 °C. The current applied to the sample was 2.2 A. (b) the current density distribution along the cathode interface in the cross-sectional plane from points I to II as defined in (a)

2.4 Results

2.4.1 Four Stages of Joint Resistance

A typical resistance signal curve is shown in Figs. 2.9a-c. In this example, the resistance changed from 6.6 mΩ at room temperature to 10.2 mΩ at the elevated temperature. Corresponding average results from five samples are 7.7 ± 1.8 mΩ and 11.8 ± 2.8 mΩ, respectively. Errors are standard deviations. These value ranges are ~15 % larger than the simulated values for the total resistance in Table 2.1 which possibly is due to variations in Cu line thickness or length. Time 0 is defined as when the current was switched from 0.1 A to 2.2 A after the oven temperature was stabilized. Figure 2.9d shows the dR/dt versus time curve, where dR/dt is smoothened using the average over a moving interval of 4000 s, in order to reduce the noise in the dR/dt curve.

Four stages are seen in this example. Stage 1 has a constant slope ranging between 0.09 mΩ/h and 0.25 mΩ/h and lasts until about 15 ks. Afterwards the slope increases to 0.53-1.04 mΩ/h at about 40 ks (Stage 2). After that, abrupt drops of resistance signals start to become dominant (Fig. 2.9b) each followed by a slow rise of approximately equal magnitude (Stage 3). Such drop-rise cycles occur every few minutes and generally get larger as the aging continues, the biggest resistance drop being 4 mΩ in the example of Fig. 2.9b. Similar resistance behavior is also seen in [14]. Stage 4 is characterized by the abrupt rise of the signal leading to complete failure (open circuit) within typically 10-50 s. The mechanism of the resistance drops and rises in current stressing is discussed in Section 2.5.

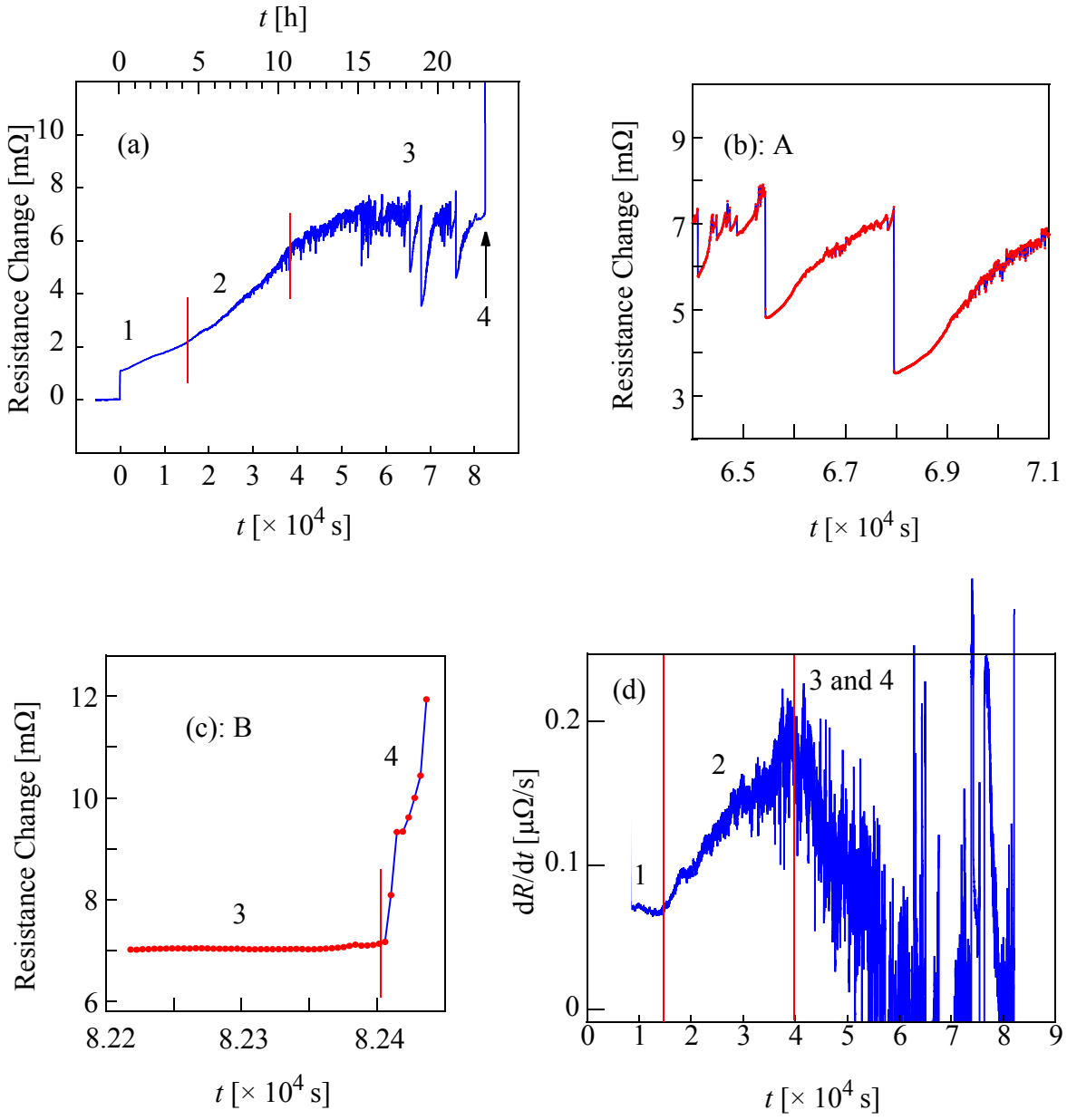

Figure 2.9. The (a) over view, (b) example of abrupt resistance drops, and (c) the final failure of a typical resistance change vs. time curve at 160 °C. Red dots are recorded data. (d) The dR/dt curve of the same example (moving average 4000 s).

To get an idea of the variation of the resistance vs. time curves between samples, four example resistance curves are shown in Fig. 2.10. The contribution factors can include the variation of the substrate, solder material, and/or the oven temperature.

2.4.2 Aging a Cross-Sectioned Sample

A single sample was cross-sectioned and then aged at 4 h intervals and analyzed at 4 h, 8 h, 12 h, 16 h, 20 h, and 24 h, respectively. Due to the destructive nature of cross sectioning method, the sample is an incomplete solder bump. In each step, the sample is cooled slow enough inside the oven to avoid thermal shock induced stress. A similar method for aging a cross-sectioned sam-

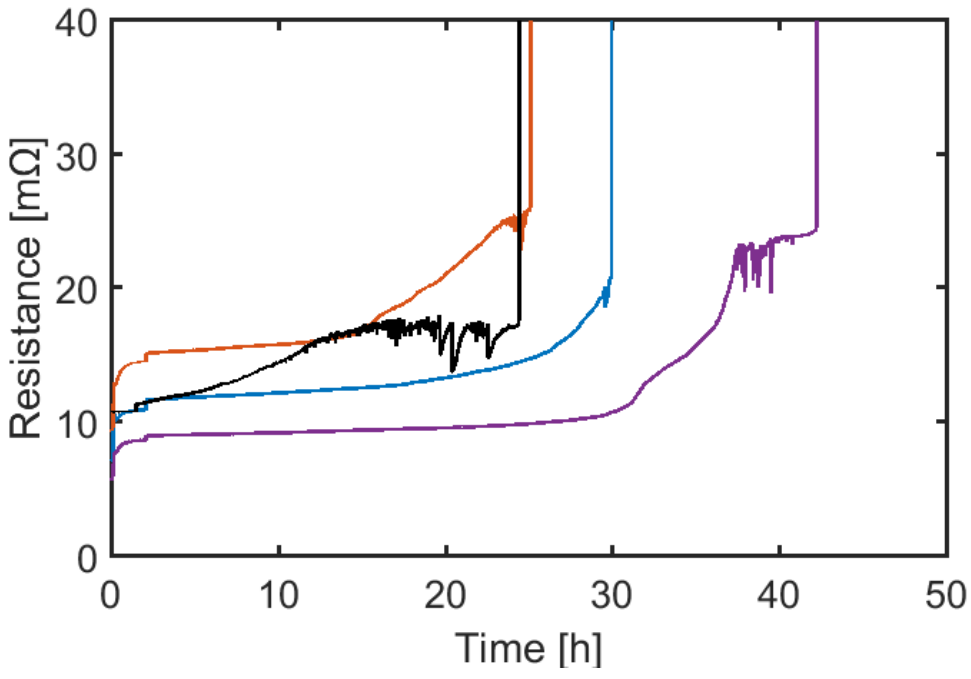

Figure 2.10. Four typical resistance vs. time curves.

ple is also used in [7, 8]. The thickness of the IMC is measured at five locations at different times of aging, as shown in Fig. 2.11. The IMC growing rate is different at different locations along the interface. In locations A and E, the IMC thickness reaches 9.8 and 8.4 μm in 8 and 4 h, at rates of 1.0 and 1.5 μm/h, respectively, and keeps increasing at rates of 0.7 and 0.4 μm/h until 24 h. In the

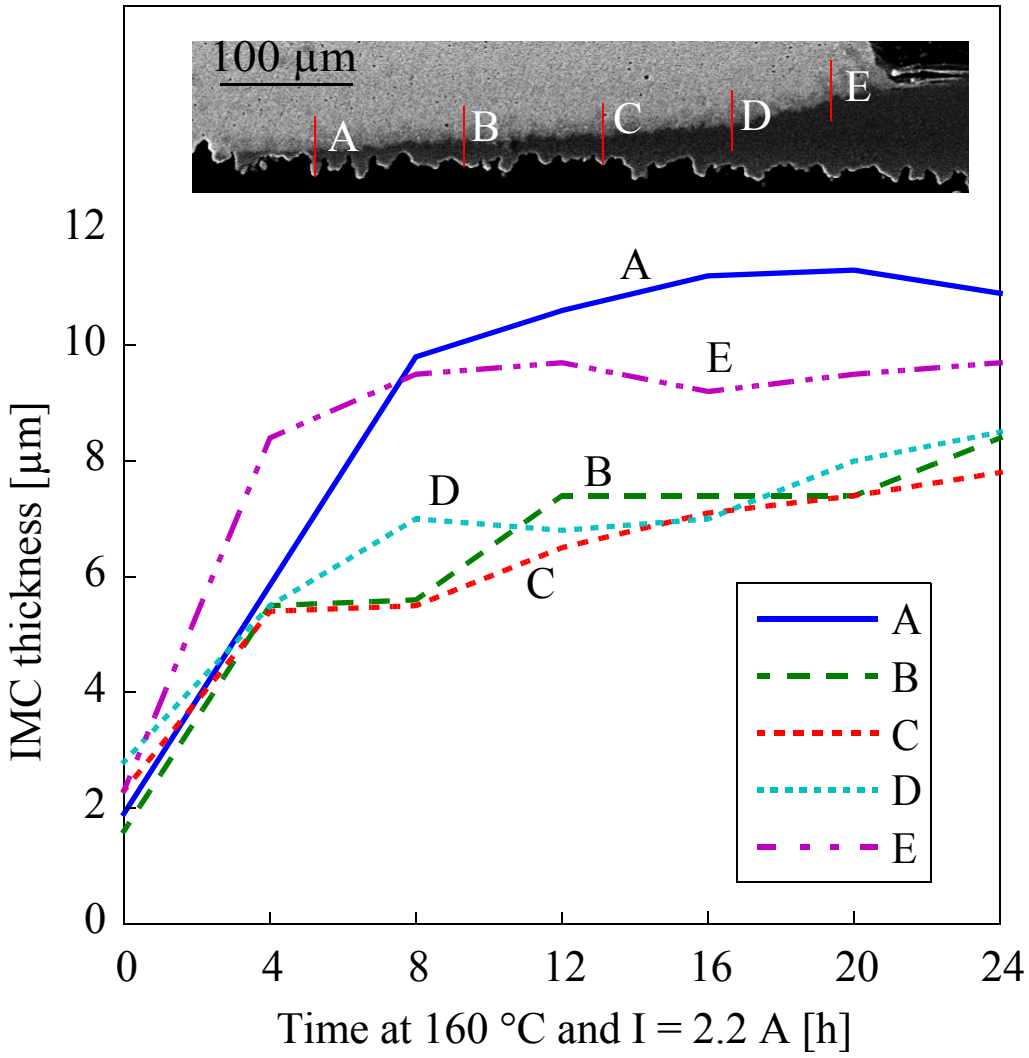

Figure 2.11. IMC thickness at locations A, B, C, D, and E along the cathode interface.

central locations B to D, IMC grows to 5.4-5.5 μm in the first 4 h, and slows down to average rates of 0.13-0.14 μm/h during 4 to 24 h. The average rates are calculated from linear fits.

Thicker IMC layers are observed at the periphery of the interfaces (locations A and E) compared to the central interfacial area (locations B, C, and D). This possibly is due to the current density being higher at the periphery compared to the central area as shown in Fig. 2.7b. Higher current density causes higher rate of Joule heat input and thus higher local temperature, leading to a faster IMC growth rate. Moreover, a higher current density also results in a faster electromigration rate, further accelerating IMC growth.

However, not only Joule heat and electromigration can affect IMC thickness but also Cu atomic concentration in the bump near the interface due to reflow, and/or the temperature distribution due to the effect of geometry. On one hand, the localized reflow history possibly resulted in more Cu dissolved into the SAC near location A where more Cu was dissolved than at other locations along the interface. A thicker IMC layer after aging possibly results from more Cu dissolved into the adjacent bump region during reflow. On the other hand, heat build-up possibly is highest close to the center (location A) because it is farthest from the surface of the bump, which can result in higher temperature than caused by Joule heating alone. These two factors possibly explain why the IMC thickness is highest at location A where the current density is relatively low according to Fig. 2.7.

IMC can also be a barrier for diffusion between SAC and Cu. When the IMC becomes thick enough, the growing rate slows down due to slower diffusion between SAC and Cu. This results in the IMC growing rate at locations A and E to be slower than B to D after 8 h of aging.

The cross-sectional images of the cathode interface after 16 h and 20 h at 160 °C and 2.2 A are shown in Figs. 2.12a-b, respectively. Cracks are observed in after 16 h aging, some of which

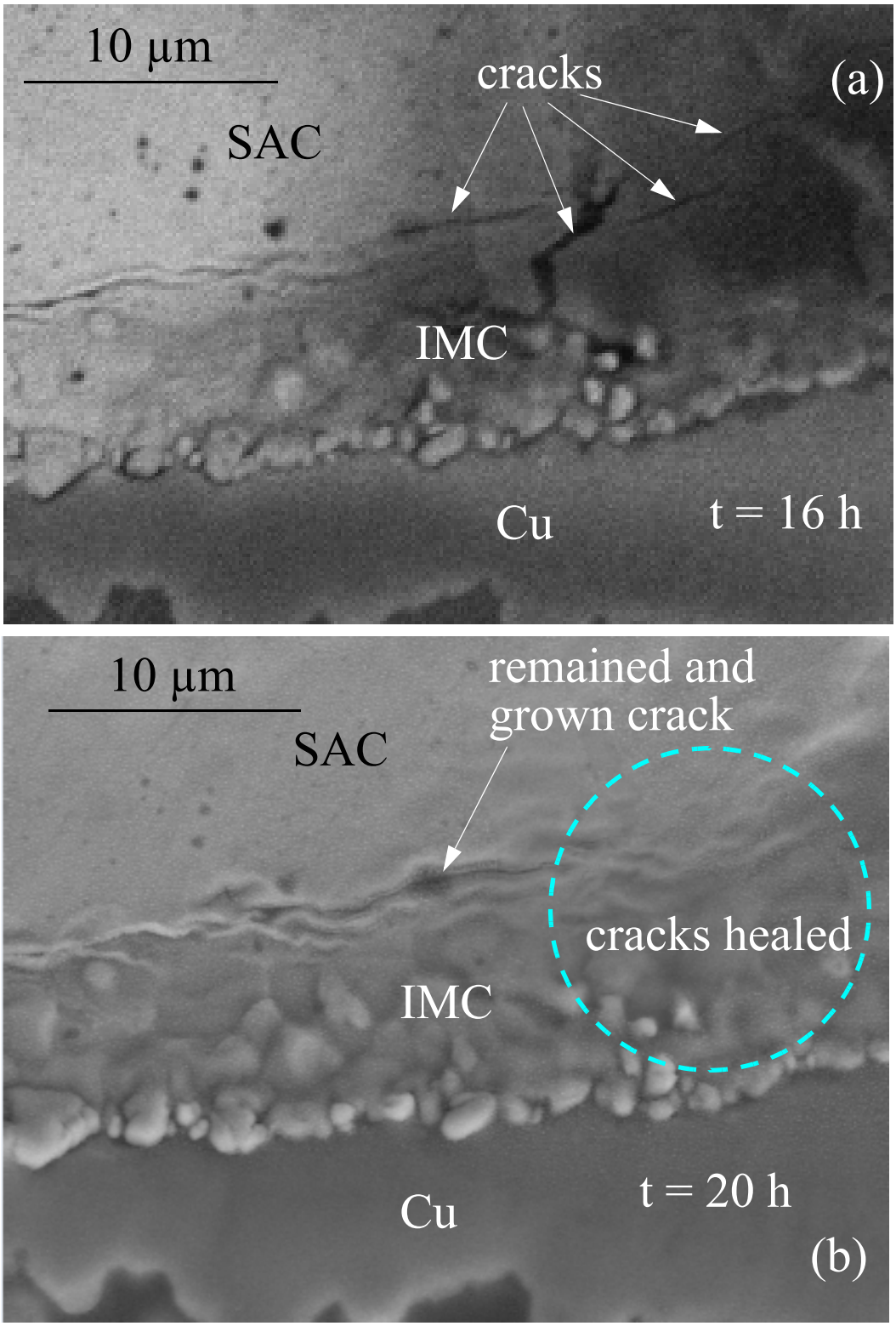

Figure 2.12. The cross-sectional SEM images of a typical cathode joint interface after aging at 160 °C 2.2 A for (a) 16 h, and (b) 20 h, respectively (same sample).

disappeared after 20 h aging, indicating a self-healing process taking place, the mechanism of which is discussed in Section 2.5. The resistance signal of this cross-sectioned sample indicates that it is in Stage 1 before 24 h.

2.4.3 Cross-sections after complete failure

Cross-sectional images of a typical failed sample are shown in Figs. 2.13a-b. This sample was cross-sectioned after the end of the test. The open is shown in more detail in Fig. 2.13b. In all samples complete failure is characterized by open cathode joints.

The original cathode interface disappears after complete failure, and the open locates below the solder resist. On the left side of the open is the SAC. On the right side of the open is the Cu line. From the cross-sectional images, the horizontal distance between the right end of the open and the left end of the solder resist ranges from 20 μm to 48 μm. Both IMC layer and SAC layer are observed on the end of the Cu line. The thickness of both IMC and SAC layers together ranges from 10 μm to 36 μm, and the thickness of all the observed IMC layer is 6 μm.

2.5 Discussion

The observed interface evolution during the aging test include IMC growth (Fig. 2.11), crack formation, crack propagation, crack healing (Figs. 2.12a-b), and opening (Figs. 2.13a-b).

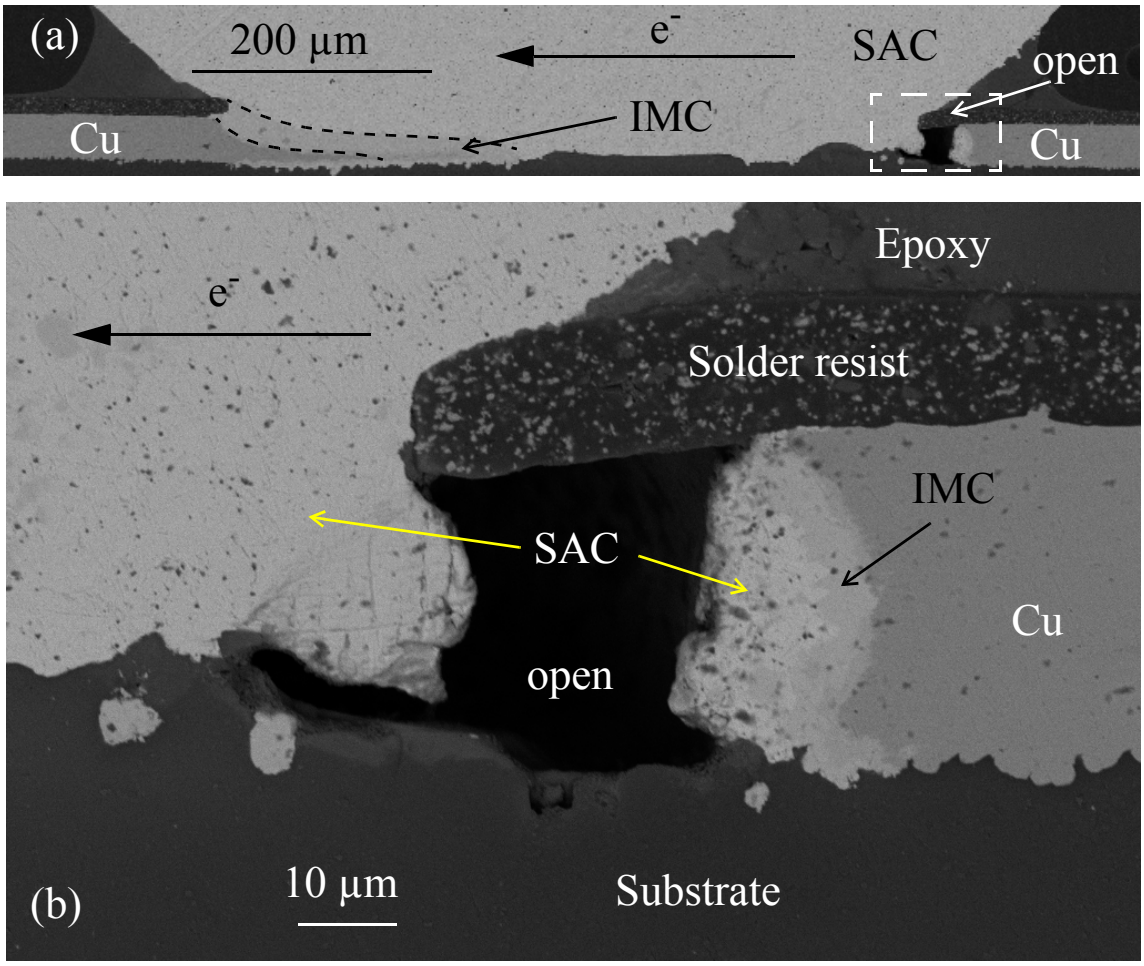

Figure 2.13. (a) The cross-sectional SEM image of a typical solder joint after complete failure at 40.19 h. (b) Magnified image of the rectangular in (a)

These events all affect the resistance signal, and different stages of the resistance signal are dominated by different events.

A possible explanation for the resistance signal showing different stages in Fig. 2.9 is given using the illustrations in Figs. 2.14a-f. In Stage 1, the resistance change is dominated by IMC growth. In Stage 2, in addition to IMC growth, the formation and propagation of cracks at the joint interface becomes dominant on the resistance signal change. As a result, the resistance signal rises faster than in Stage 1. In Stage 3, crack formation and propagation continues, interrupted by sporadic crack healing events, resulting in periodical drop and rise of resistance signals. Though crack formation and healing can be possible in Stage 1, it seems to be too small for affecting the resistance signal in this stage. The association between crack healing event and the sporadic resistance drop is a possible explanation, and is not directly confirmed due to the experimental difficulty. For direct confirmation, the aging process should be interrupted right before the abrupt resistance drop, which requires a feature from the resistance signal that shows the abrupt resistance drop would happen in the next reading. However, there is no feature from the real time resistance signal that indicates the resistance would drop in the next reading. More work would be needed to improve the understanding of the abrupt resistance drops, such as comparing with a higher temperature solder material, which is not studied in this thesis.

The crack in Fig. 2.12 is caused by electromigration [57, 58]. Due to the directional nature of electromigration, cracks preferably form at the cathode [6, 57-61]as observed in this study. Though the cross-sectioned sample underwent thermal cycles resulting from taken out of and put into the oven, the number of such thermal cycles is not large enough to cause cracking at the interface [52, 53].

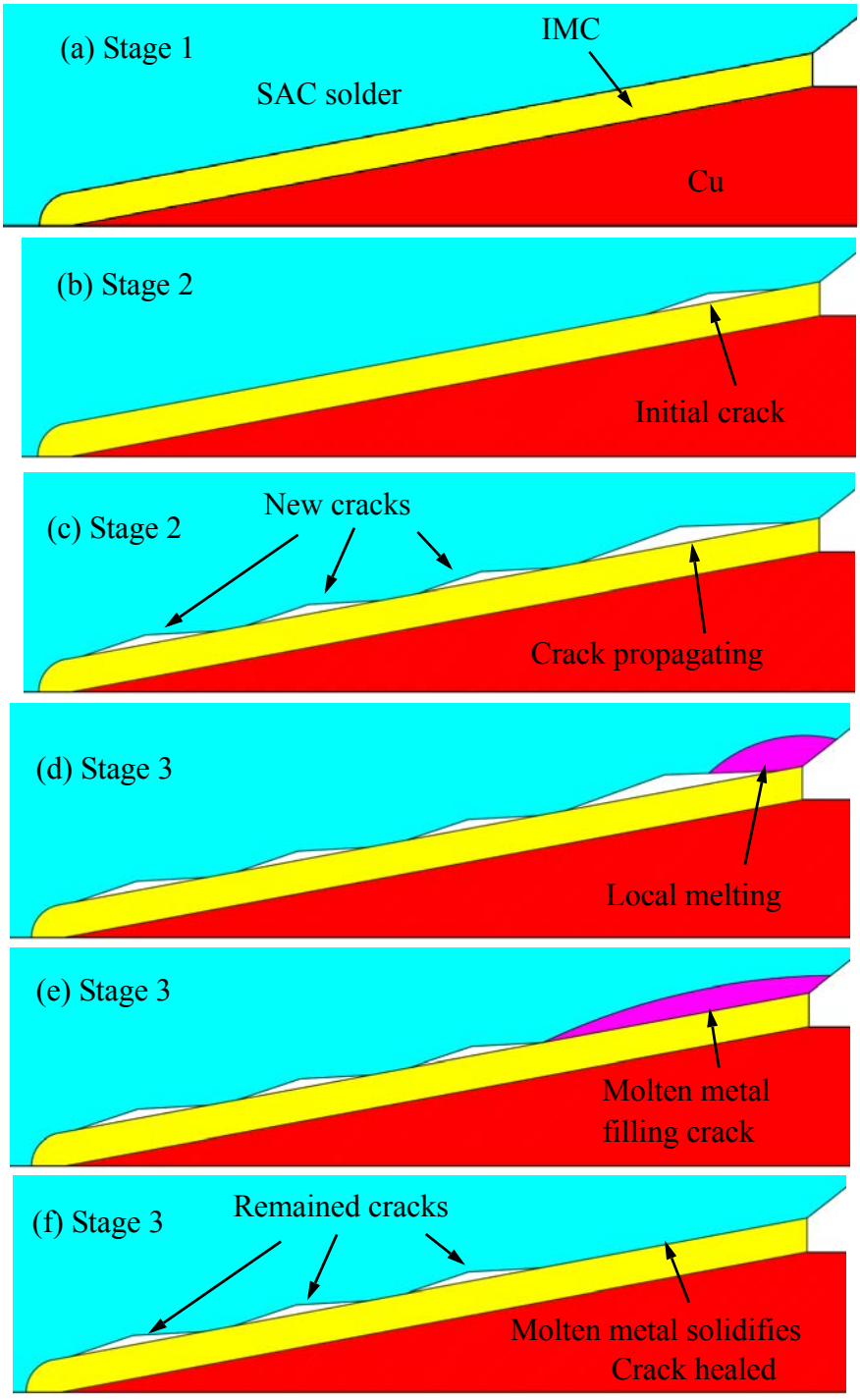

Figure 2.14. The different stages of suggested joint interface evolution during current stressing test. Stage 1: (a) IMC forming at the interface. Stage 2: (b) the initial crack forming, and (c) the crack propagating along the joint interface while new cracks form. Stage 3: (d) local melting at one contacting asperity due to Joule heat, (e) molten metal filler the crack nearby, and (f) molten metal solidifies and new joint interface forms after one crack is healed. Only cathode is shown.

The apparent instantaneous drop in resistance is either caused by rapid atomic diffusion filling a crack or by local melting and crack filling by the molten material, caused by increased Joule heating of interfacial asperities next to the crack. When the joint resistance increases to a critical value due to crack propagation, the Joule heat increases locally due to the current being concentrated. When the Joule heat is so high that the local temperature can reach the melting point of SAC. The SAC melts locally at the interface and fills the cracks nearby. Less current goes through the molten part because of the higher resistivity of liquid metal than solid metal. As a result, the local temperature drops abruptly and the molten metal solidifies.

The process from the start of local melting to the end of solidification can take less than the sampling period of the experimental setup 4 s, and possibly is much shorter, which is consistent with the resistance signal shown in Fig. 2.9, where all drops are shorter than one single sampling period.

2.6 Summary of Chapter 2

By monitoring resistance during current stressing of SAC to Cu joints and comparing with results from cross-sections, it was possible to clearly identify four stages of aging. Possible explanations were given for mechanisms underlying each stage. Specifically in Stage 3, the resistance signals drop and rise periodically, where the drops are abrupt while the rises are relatively gradual. The abrupt resistance signal drops are explained with crack self-healing event found with cross-section studies.

The method presented in this study is well suited for efficient characterization of the reliability of a joint between solder and copper trace, e.g. for quick comparison of different solder types. The method relies on a custom low-cost substrate and involves simply steps of specimen preparation and subsequent testing. The continuous resistance recording provides ample data for efficient reliability characterizations under current and temperature loads. As the resistance data is available in real-time during the test, failing joint can be detected exactly when they fail. So test can be interrupted to save time.

Chapter 3 Real time joint resistance monitoring during solder reflow

The work in this chapter is partially published in [62]. In this chapter, a customized real time resistance monitoring (RTRM) setup is developed to observe the resistance of a solder connection in real-time during reflow to better understand the challenges of soldering. In contrast to Chapter 2, the RTRM method in this chapter can monitor multiple samples simultaneously with a faster sampling rate.

In Section 3.1, the customized RTRM method is described, including both sample solder dispensing and resistance monitoring in reflow. In Section 3.2, two types of solder paste are studied with RTRM. Solder A is fresh while solder B is one year old. Solder B in general has a lower room temperature resistance before reflow than solder A. During reflow, the resistance signals behave differently between solder A and solder B. For example, in solder B, an episode of high resistance (24.40 ± 16.04 kΩ) is observed for 4-58 s not long before melting, while solder A mainly shows resistance drops in the early stage of reflow. Microscopic images and cross-sectioning studies with respect to the special events in the resistance signal show solder compacting, solder sintering, flux segregation, and final open or connection. In Section 3.3, the correlation between the resistance signals and the microscopic observations is discussed.

3.1 Experimental

3.1.1 Solder paste dispensing

The solder paste is purchased from Chipquik (part number: SMD291AX). The solder paste contains 88 wt.% Sn63Pb37 metal balls of 25-45 μm diameter. The flux is standard REL0 flux [63], which has less than 0.05 wt.% halide. The activator is a mixture of carboxylic acids including maleic acid, and the flux activation temperature is 140 °C. The solvent is terpineol with a melting temperature of −35.9 to −28.2 °C and a boiling temperature of 214 to 217 °C.

Two syringes of solder paste are used, and are named solder A and solder B, respectively, in this chapter. The manufacture dates of solder A, and solder B are 2016 March, and 2015 March, respectively. The experiments were carried out in summer 2016.

A total of eight solder bridge samples on one standard 28-pin side-brazed dual in-line ceramic package (SBDIP) are fabricated. The metallization of the lead fingers is >1.5 μm Au over ≈25 μm Ni. The solder paste is dispensed with a Nordson Ultimus I Automatic Fluid Dispenser, as shown in Fig. 3.1. After a few trials and errors, a final dispensing design shown in Fig. 3.2a is adopted. Each sample is designed to bridge two lead fingers. The machine settings for this design are taught via the control panel and the dispensing parameters are given in Table 3.1. The machine

Table 3.1. Solder paste point dispensing parameters

Tip inner diameter [mm]	Time [s]	Pressure [psi]
0.61	6	50

is taught to perform eight-point dispensing. After the substrate is placed, the control panel is used to move the syringe tip to the designed locations, and teach the locations, and the dispensing parameters. The inner diameter of the needle is 0.61 mm. Point dispensing is used with a dispensing time of 6 s and a dispensing pressure of 50 psi. The estimated amount of paste dispensed is 1.9 mm^3. A top view of a SBDIP with all eight samples before and after reflow is shown in Figs. 3.2b and c, respectively. An overview photo of the SBDIP is shown in Fig. 3.2d.

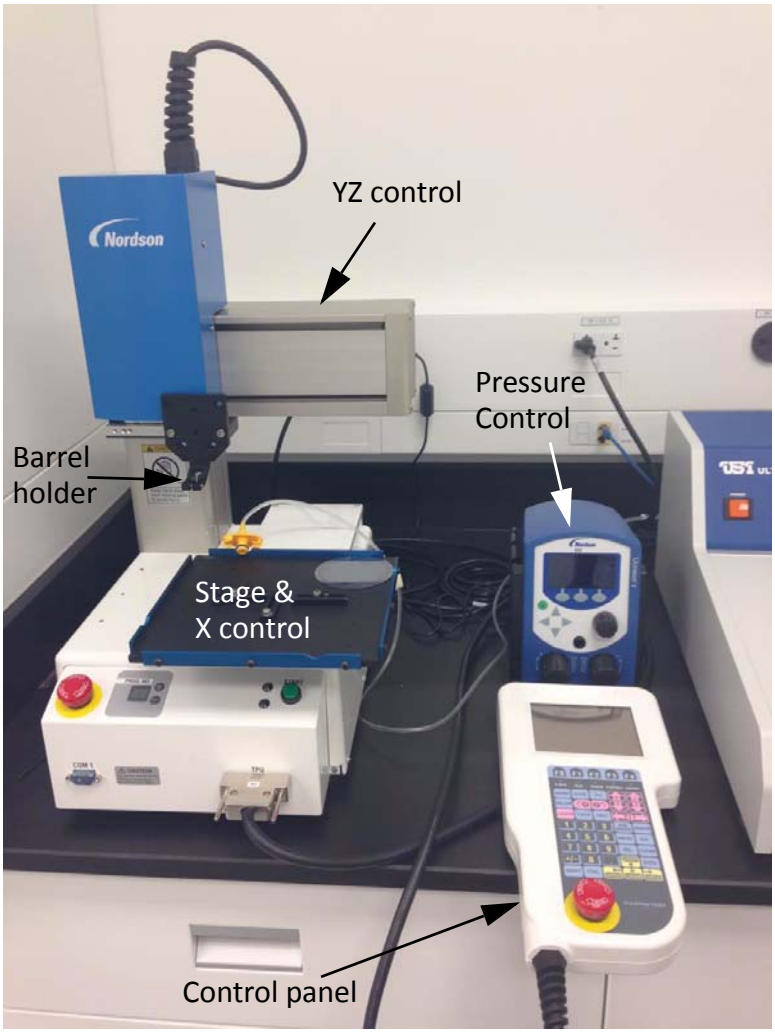

Figure 3.1. Automatic dispensing setup.

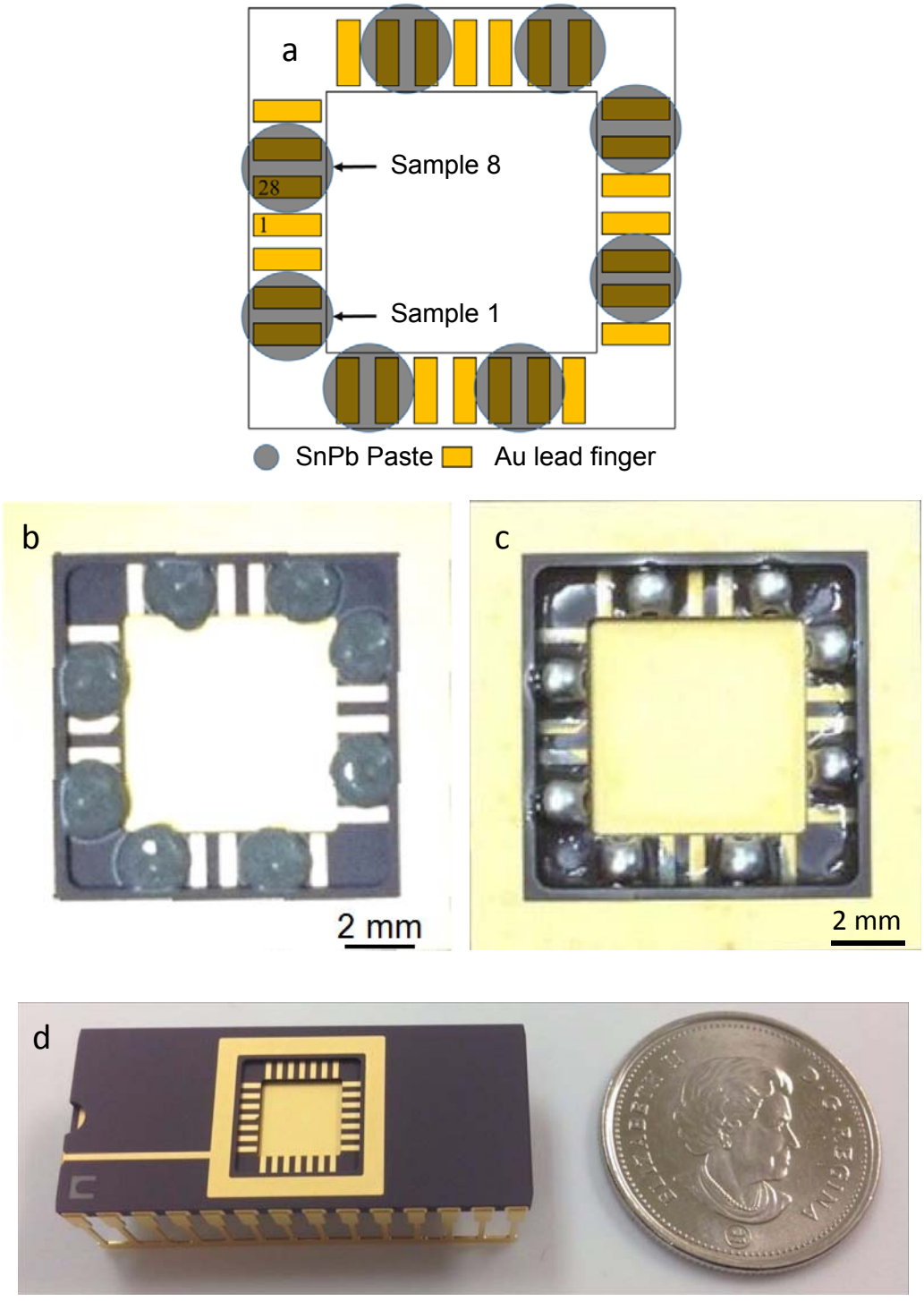

Figure 3.2. (a) Design of solder paste dispensing pattern, with eight samples in total on one SBDIP. Image is not to scale. (b) Top view of a SBDIP with as-dispensed solder paste samples, and (c) reflowed samples. (d) The overview photo of an empty SBDIP substrate, and a 25 cent Canadian coin (diameter = 23.88 mm).

3.1.2 Real-time resistance monitoring system

The design of the resistance monitoring system is illustrated using a block diagram in Fig. 3.3 and a list of components is shown in Table 3.2. The main components are PC with custom recording software, two Keithley 2700 multimeters (one with a multiplexer card integrated), a Pt100 resistive temperature detector, a custom high temperature socket assembly, an oven and cables. The eight samples are connected with a multiplexer inside multimeter 1 (DMM 1) through

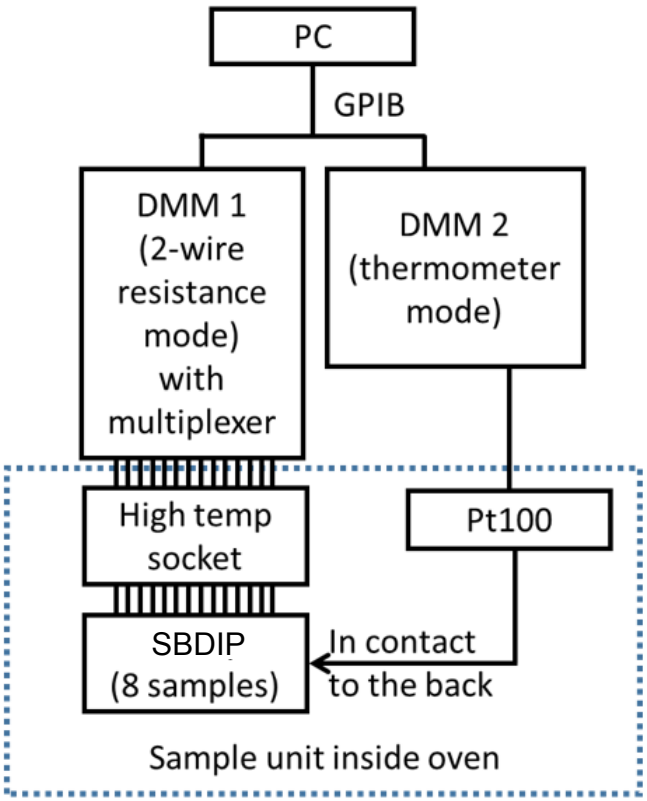

Figure 3.3. Schematic of resistance monitoring system, with both digital multimeters (DMMs) programmed to automatically measure and record sample resistances, and temperature, respectively, all controlled with PC.

the high temperature socket, the PTFE insulated wire cables, the regular flat ribbon cables outside the oven, and some D-sub connectors for flexible assembly and disassembly of the setup. Digital multimeter 2 (DMM 2) measures the temperature using the Pt100. The recording rate in this study is seven readings per second per substrate. The detailed connection between the samples and the multiplexer is shown in Fig. 3.4.

Photographs of the sample unit details and the experimental setup overview are shown in Figs. 3.5a and b, respectively. After samples are dispensed, the SBDIP is inserted into a high temperature socket. The Pt100 is mechanically embedded into the top of the socket so that it is in contact with the back of the SBDIP when the SBDIP is inserted. The socket is connected to the

Table 3.2. List of components in the solder reflow resistance monitoring system

	Component	Description
1	PC	Laptop: Win7 with Matlab
2	Matlab code	RmonitoringReflow_v20170802.m; Available online at [64]
3	DMM1	Keithley 2700 with a 7700 multiplexer card
4	High temp socket	High-Temp (up to 300°C) Universal DIP ZIF Burn-in & Test Sockets, Aries Electronics Inc.
5	SBDIP	SBDIP with eight solder samples (see Fig. 3.2b)
6	DMM2	Keithley 2700
7	Pt100	Temperature sensor
8	Cables	GPIB-USB adapter, regular flat ribbon cables, and high temperature polytetrafluoroethylene (PTFE) insulated cables
9	Oven	Omegalux LMF 3550
10	Others	37-pin D-sub connectors, Kapton tape, Steel block (Weight)

multiplexer through 28 wires. As a result of the sample design, only 16 of the 28 connections are used. Both Pt100 and the high temperature socket are joined to the wires with Sn-3Ag-0.5Cu (SAC305) solder which has a melting temperature of 217-218 °C. A metal block supports the wires to make the SBDIP surface close to horizontal, minimizing movement of the solder paste due to gravity. High temperature tape is used to fix the wires onto the metal frame. All wires inside the oven are insulated with PTFE. In summary, the whole sample unit is built to survive temperature of up to 250 °C with connections to the digital multimeters outside the oven.

The resistance monitoring process controlled with a Matlab code, and the flow diagram is shown in Fig. 3.6. The Matlab code essentially scans all the samples in a loop until the time is

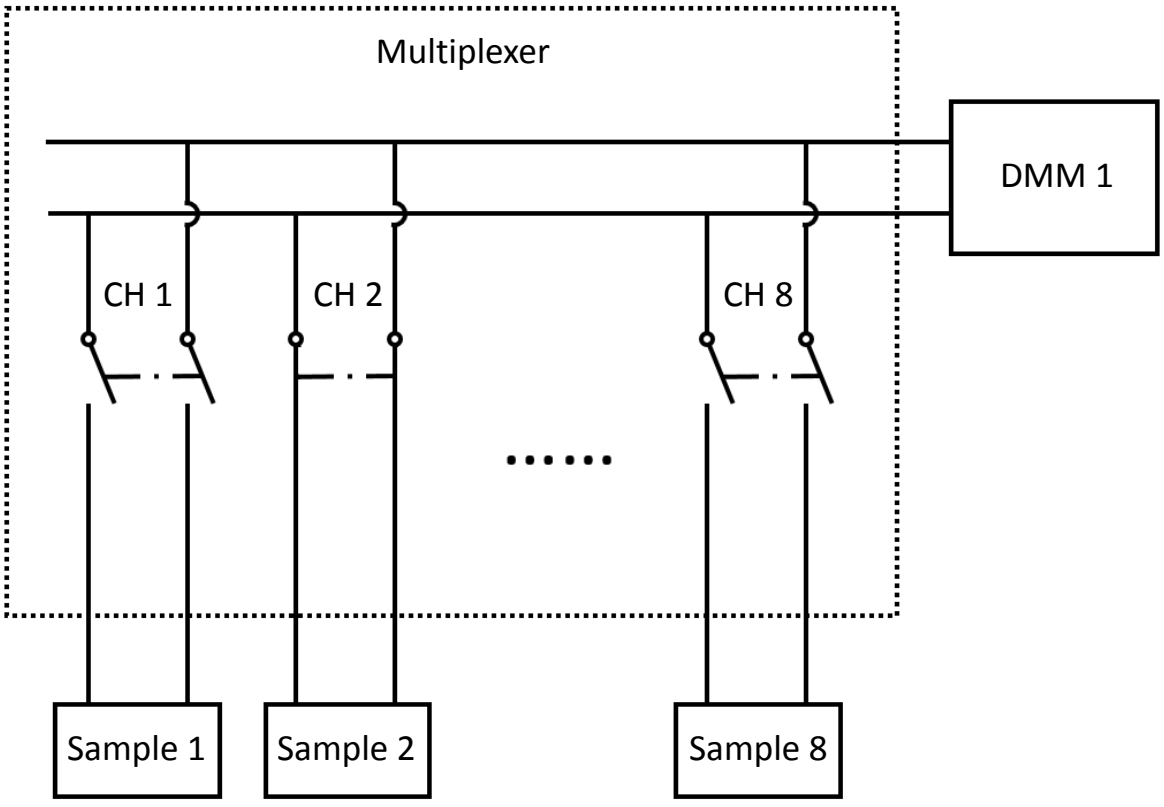

Figure 3.4. Detailed connection between samples, multiplexer, and DMM 1. For example in this figure, sample 2 is connected for measurement while all others are disconnected.

reached to stop recording, typically at 4 hours. The file name of the Matlab code is RmonitoringReflow_v20170802.m. It is available for download from matlab central [64].

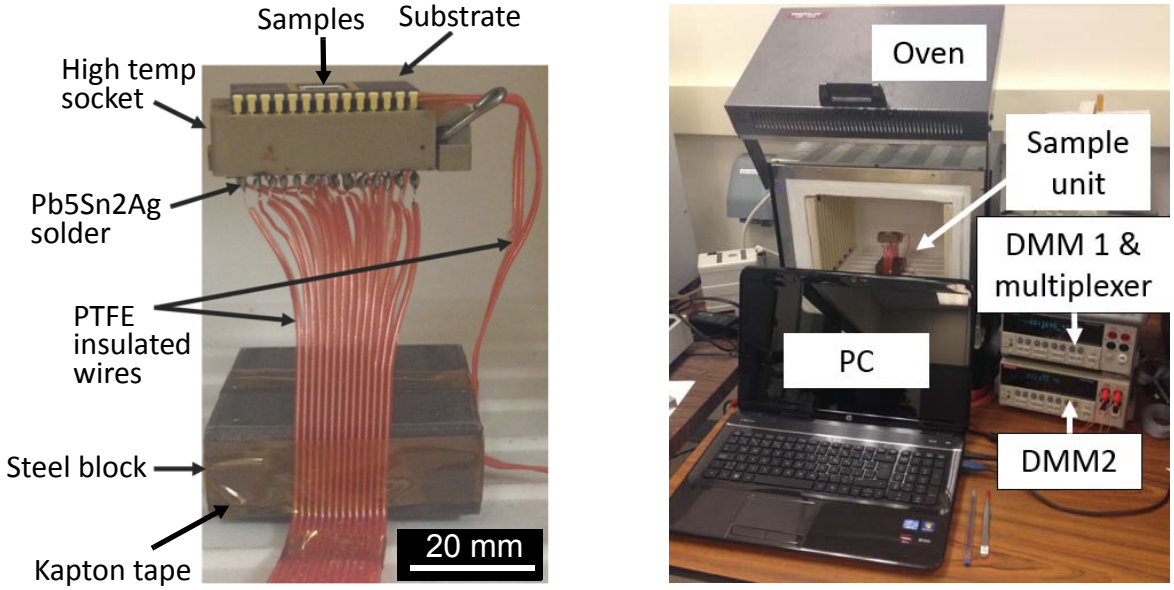

Figure 3.5. (a) High temperature sample unit that can be used up to 250 °C. The socket is mechanically supported by two flat band cables (second cable not shown, behind the first cable). Overview of the experimental setup schematically shown in Fig. 3.3.

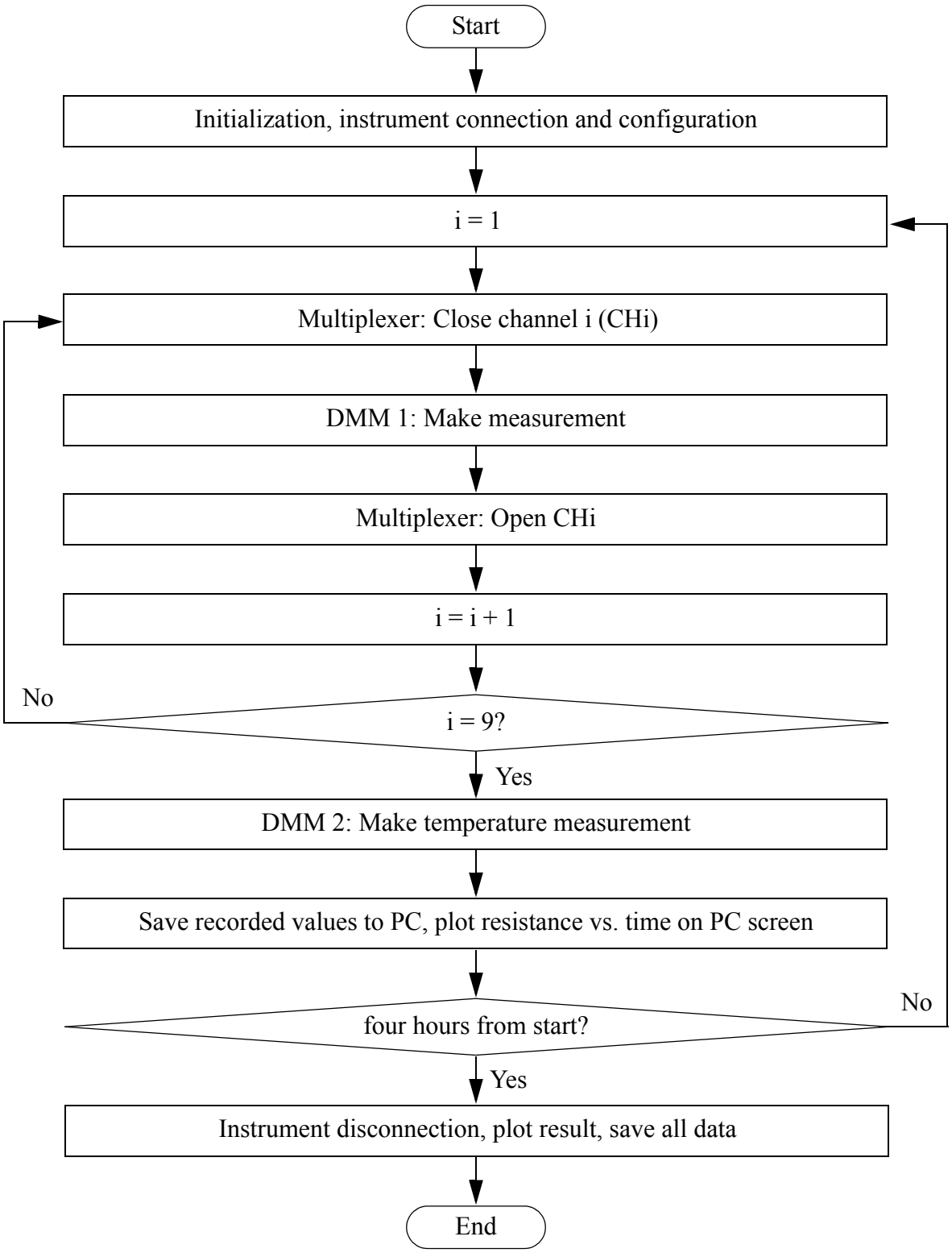

Figure 3.6. Matlab code flow diagram for the resistance monitoring during solder reflow, where each measurement loop takes about 2 s. (File name: RmonitoringReflow_v20170802.m; Available online at [64] and [55]).

3.2 Results

3.2.1 Resistance change during reflow

Figure 3.7 shows an example resistance curve and the recorded temperature during reflow of solder A. Sample resistance at room temperature is typically a few MΩ. In this example, R_{Ainit} = 4.89 MΩ. During ramping up of the temperature, the resistance typically experiences two abrupt drops. In this example, the first resistance drop of ΔR_1 = 0.78 MΩ from R_{before1} = 1.14 MΩ to R_{after1} = 0.36 MΩ takes place at t_{Rdrop1} = 4.6 min when the temperature is T_{Rdrop1} = 130 °C. The second resistance drop of ΔR_2 = 115 kΩ from R_{before2} = 115 kΩ to R_{after2} = 4.58 Ω takes place at t_{Rdrop2} = 5.2 min when the temperature is T_{Rdrop2} = 143 °C. From time = 10 min to the end of the experiment, the resistance signal mainly follows the same trend as the temperature signal. The temperature coefficient is determined to be α = 0.023 °C^{-1}, with reference temperature of 25 °C, using the linear fit result from data between 25 min and 60 min, as shown in Fig. 3.8. For this data, the lead resistance was deducted by the raw data. The lead resistance is measured separately from a sample shorting all the leads, and a top view photo is shown in Fig. 3.9. The lead resistance includes the resistances of the conducting part in the SBDIP, the socket, the wires, the D-Sub connectors, the multiplexer, and all the contact resistances in between. A typical lead resistance is 1.3-1.6 Ω in room temperature, and 1.4-1.9 Ω at 200 °C, respectively.

Figure 3.10 shows four example resistance curves and the recorded temperature curve during the reflow process obtained with solder B. In contrast to solder A, solder B seems to be more conductive at room temperature, where the average resistance is R_{Binit} = 1.84 Ω.The resistance signal drops before about 6 min into heating for all the samples shown. When the recorded tem-

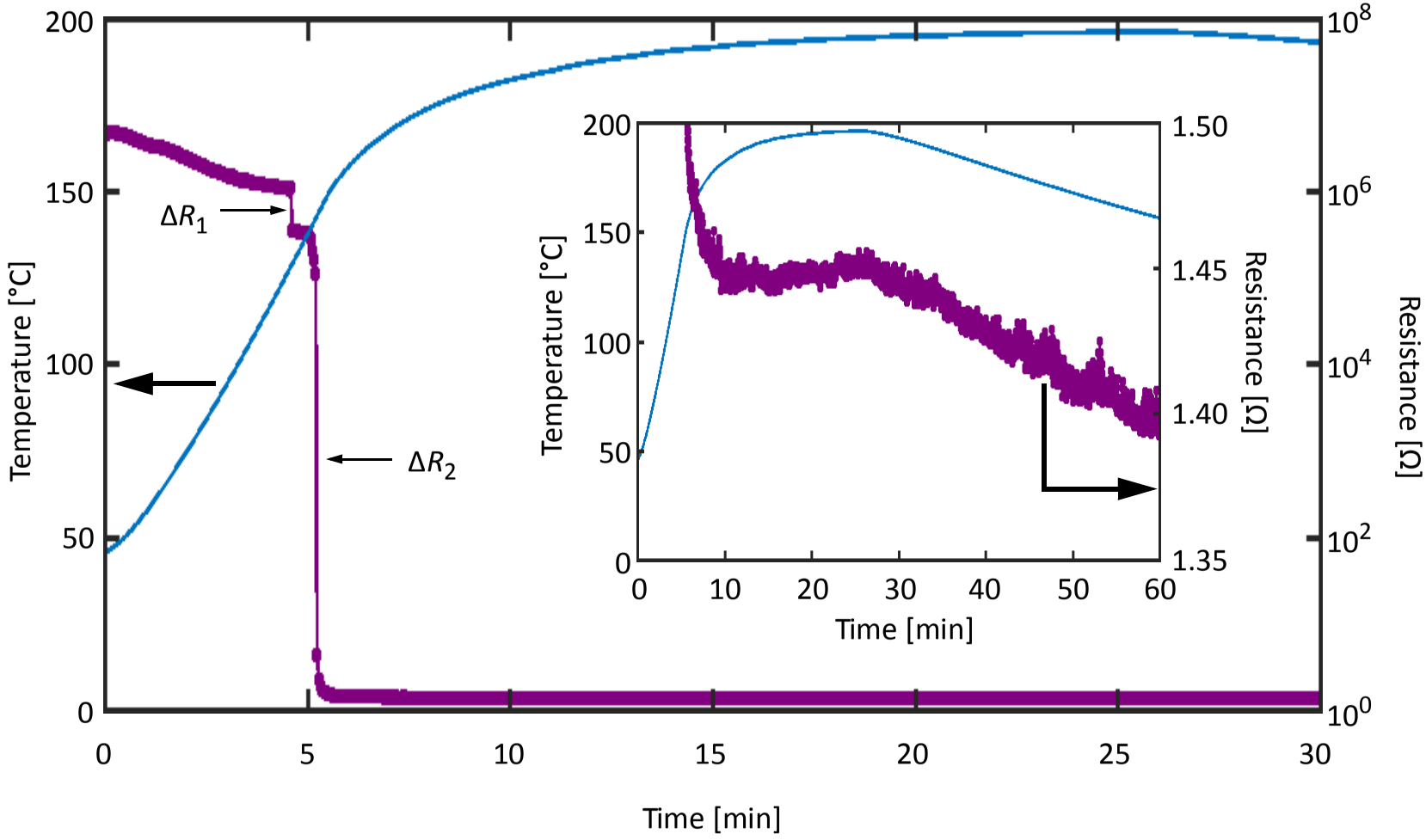

Figure 3.7. Solder A: A typical *R-t* curve and the *T-t* curve. Inset is zoomed at 1.35-1.5 Ω

perature reaches 170 °C, the resistance is R_{B170C} = 1.62 Ω with a standard deviation of 0.11 Ω. Between 8 and 12 min, we observe different behaviors from all the resistance signals: 1. open; 2 and 3. transient high electrical resistance (THER); 4. no sudden change. More details for exam-

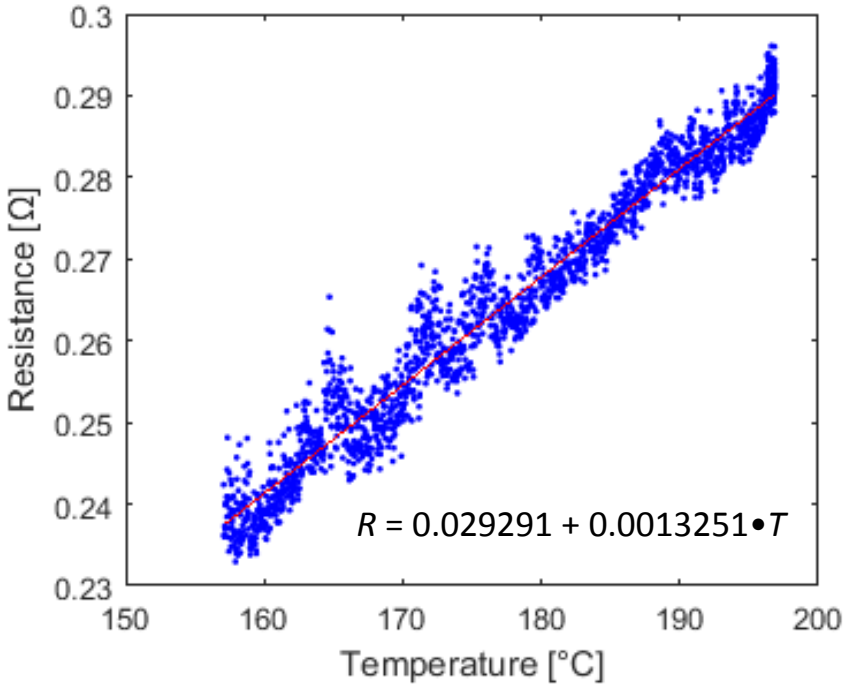

Figure 3.8. *R-T* curve of solder A using data between 25 min and 60 min of *R-t* curve, the lead resistance deducted.

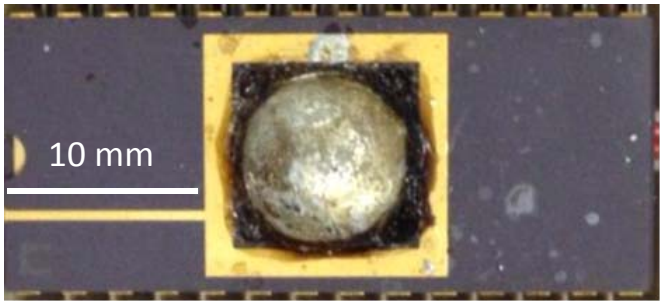

Figure 3.9. Top view photo of the sample used for measuring lead resistances.

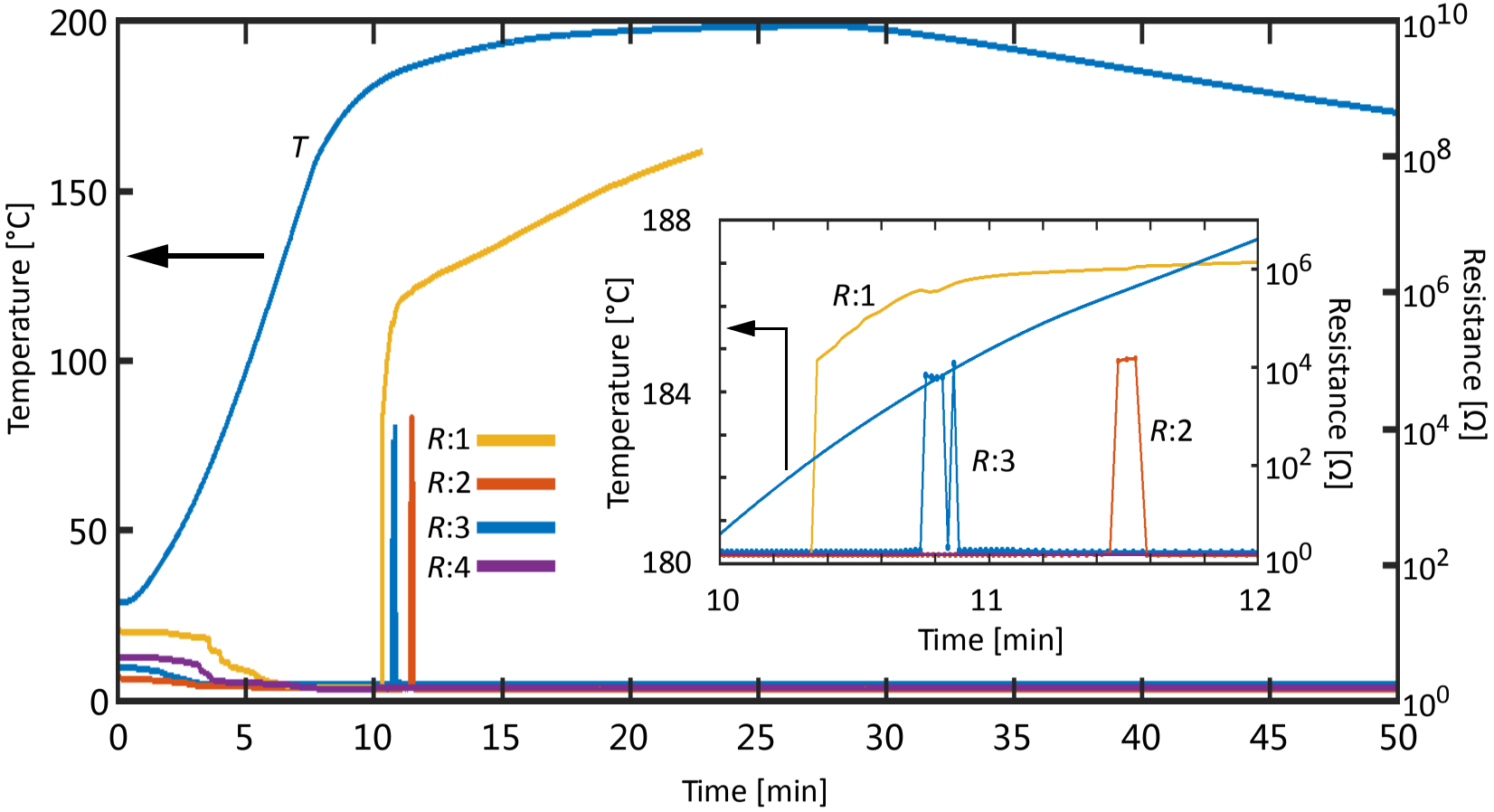

Figure 3.10. Overview of four typical *R-t* curves of solder B that show: 1. open; 2. transient high electrical resistance (THER); 3. multiple THER; 4. no sudden change; respectively, and the *T-t* curve. Inset is the graph zoomed at 10-12 min.

ples 3 and 4 are shown in Fig. 3.11. Such samples with THER behavior have typically 1-3 THER signal spikes. From a total of 82 tested samples, there are 35 open, 16 THER including 5 double THER and 1 triple THER, and 31 with no sudden resistance change.

Figure 3.12 shows a typical resistance curve with THER zoomed at 11-11.5 min, and the corresponding temperature curve. At t_{Bjump} = 11.15 min when the recorded temperature is T_{Bjump} = 185.6 °C, the resistance signal abruptly jumps from R_{Bjump} = 1.7 Ω to R_{THER} = 13.5 kΩ. The resistance signal remains > 10 kΩ until at t_{Bdrop} = 11.39 min when the recorded temperature is T_{Bdrop} = 186.1 °C, and abruptly drops from R_{THER} to R_{Bdrop} = 1.63 Ω. For single THER behavior, the resistance remains at R_{THER} between t_{Bjump} and t_{Bdrop}. For multiple THER behavior, the resistance signal jumps back and forth between > 1 kΩ and < 5 Ω, as shown by the example in Fig. 3.10. In either case, a resistance reading between 5 Ω and 1 kΩ is rarely seen between t_{Bjump} and t_{Bdrop}. The time span between t_{Bjump} and t_{Bdrop} is 4 to 58 s for 16 samples.

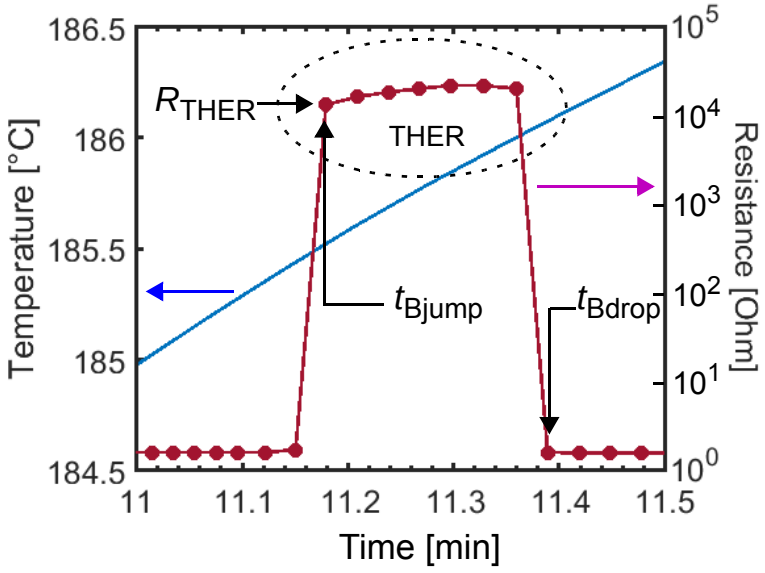

Figure 3.12. Zoomed view of a typical *R-t* curve that shows THER event, and the corresponding *T-t* curve.

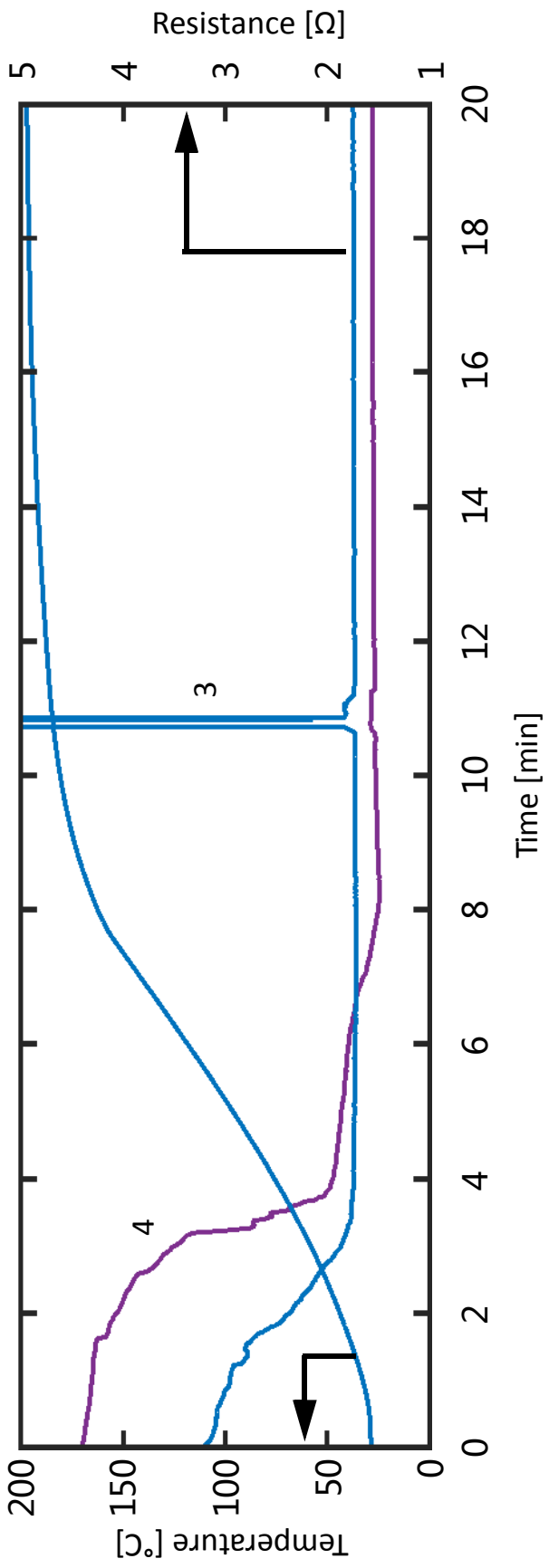

Figure 3.11. Zoomed in of curves 3, and 4 at 0-20 min and 0-5 Ω, and the *T-t* curve in Fig. 3.10. Curves 1 and 2 are removed for clarity.

The data extracted from the reflow signals is summarized in Table 3.3.

3.2.2 Microscopic analysis for solder A

Figures 3.13a-d show optical microscopic images of solder A taken from samples for which the reflow process was at various stages. The stages are as dispensed state, after first resistance drop, after second resistance drop, and after complete reflow process, respectively.

Figure 3.13b shows slumping compared with Fig. 3.13a, which may account for the first resistance drop due to the increased compactness of solder balls. Solder slumping is a common

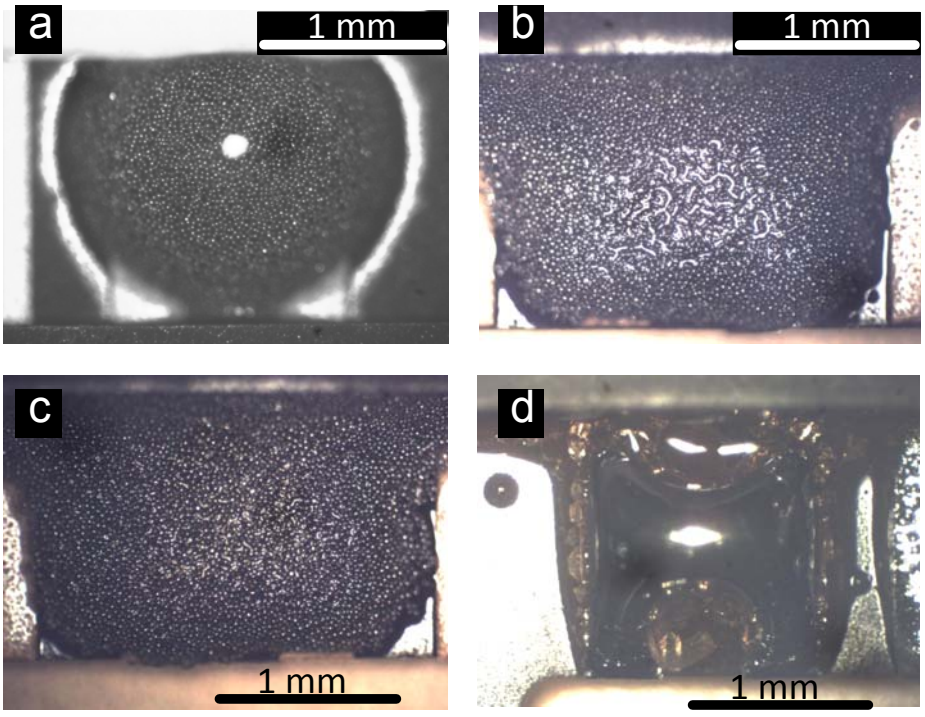

Figure 3.13. Optical top view images of solder A from interrupted reflow process at (a) as dispensed state, (b) between the two resistance drops, (c) less than 10 s after the second resistance drop, and (d) after complete reflow process.

Table 3.3. Data extracted from reflow signals

		Solder A			Solder B		
		μ	σ	n	μ	σ	n
R_{init} [Ω]		11.5×10^6	6.9×10^6	120	1.84	1.54	54
First drop	max rate [kΩ/s]	342	71	111	-	-	-
	t_{Rdrop1} [min]	5.2	1.2	120	-	-	-
	T_{Rdrop1} [°C]	116	19	104	-	-	-
	$R_{before1}$ [MΩ]	1.23	0.08	97	-	-	-
	ΔR_1 [kΩ]	814	158	110	-	-	-
	R_{after1} [kΩ]	502	178	120	-	-	-
Second drop	max rate [kΩ/s]	64.7	25.8	103	-	-	-
	t_{Rdrop2} [min]	6.5	1.5	120	-	-	-
	T_{Rdrop2} [°C]	141	11	104	-	-	-
	$R_{before2}$ [kΩ]	121	52	107	-	-	-
	ΔR_2 [kΩ]	121	52	107	-	-	-
	R_{after2} [Ω]	4.58	2.78	111	-	-	-
Max temp.	T_{max} [°C]	193.5	3.8	48	191.0	4.1	40
	t_{Tmax} [min]	26.3	1.2	40	15.7	8.7	48
	R_{Tmax} [mΩ]	291	55	39	286	108	38
THER	t_{Bjump} [min]	-	-	-	9.32	0.13	11
	T_{Bjump} [°C]	-	-	-	176.8	4.5	23
	R_{Bjump} [Ω]	-	-	-	0.31	0.11	22
	t_{Bdrop} [min]	-	-	-	9.44	0.08	11
	T_{Bdrop} [°C]	-	-	-	178.9	3.6	23
	R_{Bdrop} [Ω]	-	-	-	0.22	0.10	22
	R_{THER} [kΩ]	-	-	-	24.40	16.04	123
Cooling stage	TCR [$10^{-3}K^{-1}$]	16.4	9.3	22	5.24	1.10	39
R_{final} @ 50 °C [mΩ]		131	67	28	148	90	29

phenomenon for solder paste in the early stage of reflow, where solder paste spreads to some extent, and may lead to short circuit in fine pitch soldering. Figure 3.13c shows less coverage of transparent phase among the solder balls than Fig. 3.13b, indicating a loss of flux component during the second resistance drop. Figure 3.13d shows a solder bridge formed with smooth surface due to surface tension before the sample solidifies, and flux residue can be observed around the sample.

3.2.3 Microscopic analysis for solder B

Figure 3.14a shows an optical image of as-dispensed solder B. Figure 3.14b and c show optical and scanning electron microscopic (SEM) images of a sample interrupted at 150 °C during the reflow process, respectively. Comparing Figs. 3.14a and b, the solder ball neighboring distances are 45.8 μm with a standard deviation of 14.4 μm and 35.0 μm with a standard deviation of 3.9 μm, respectively, taking randomly 5 pairs of neighboring solder balls. No evidence of melting or joining can be seen in Fig. 3.14c. The difference between Fig. 3.14a and Fig. 3.14b is difficult to see under the same magnification as in Figs. 3.13a-d.

The solder balls becoming more compact after heated up to 150 °C is consistent with the resistance becoming smaller in the preheating stage. The expected reason for solder compacting is the vaporization of the volatile components in the flux [65-68].

Figures 3.15a-b show SEM images of the cross-section of a typical sample during THER event shown in Fig. 3.12. The sample in Fig. 3.15 is prepared by stopping heating at about 2 s after the resistance jumps are observed. At about 2 s after the resistance jumps are observed, the oven is stopped and opened immediately, and the sample unit is taken out of the oven to cool in

room temperature. No cracks on the ceramic substrate are observed. The same method is used to interrupt soldering process in Chapter 3, as well as the silver sintering process in Chapter 4.

The solder in Fig. 3.15a is partially molten, and the solder balls in Fig. 3.15b are mostly connected already. An opening is observed in Fig. 3.15a between the solder and the substrate. Solidified flux is observed in between the solder and the lead fingers. The flux occupying the space in between the solder metal and the lead fingers possibly results from increased surface tension of the molten flux. Its conductance is possibly the main reason for the finite resistance detected in THER.

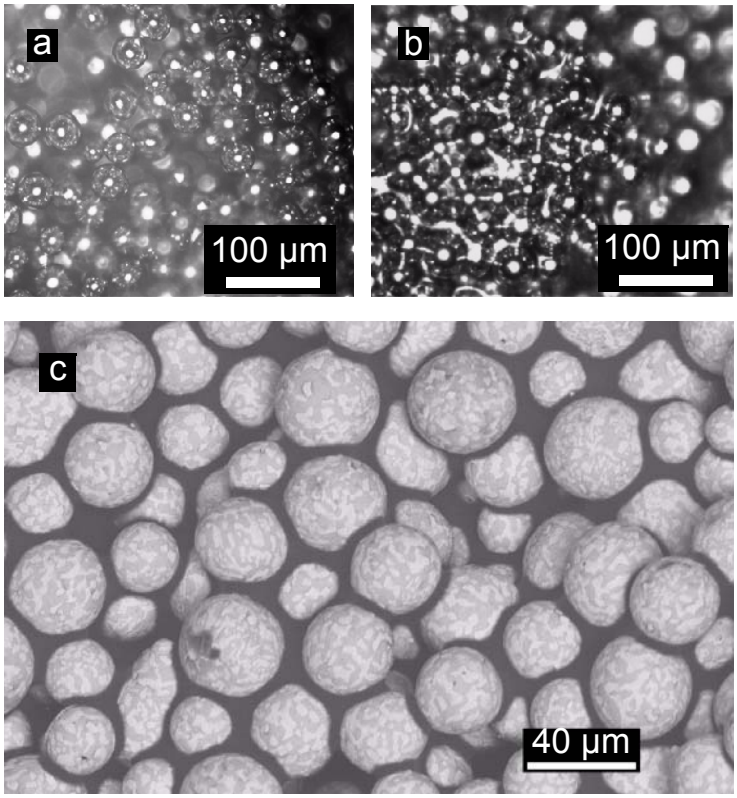

Figure 3.14. Microscopic images of solder B (a) optical, as dispensed, (b) optical, after T = 150 °C, and (c) scanning electron microscopic (SEM), after T = 150 °C.

Figures 3.16a, c, and e show SEM images of samples at 3 s after resistance drops after THER. No evidence of solder melting can be seen in Fig. 3.16a since no solder balls appear joined. However in Figs. 3.16c and e, no individual intact solder balls can be observed. Instead, more uniform solder material is observed in the center of the sample while on the surface is mainly coalition of misshaped solder balls with a few gaps, indicating the occurrence yet incomplete melting of solder sample.

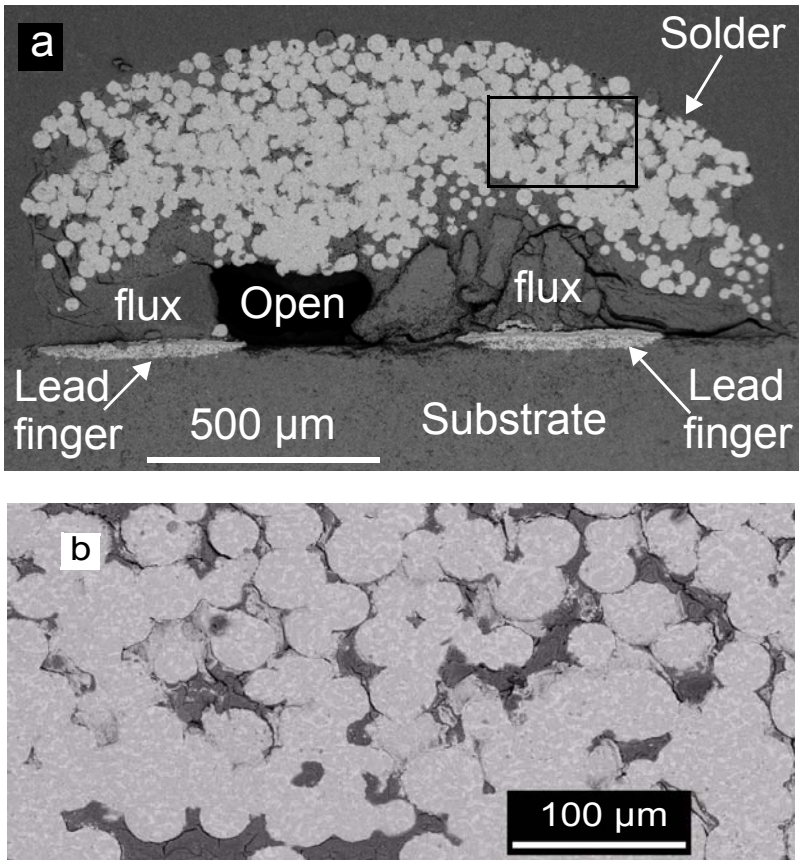

Figure 3.15. (a) Overview, and (b) magnified SEM image of a solder B sample cross-section between t_{Bjump} and t_{Bdrop}. The sample is removed from the oven about 2 s after resistance jump is observed from the real time resistance signal.

Figures 3.16b, d, and f show SEM images of samples taken 8 s after THER. Most solder balls have joined together, and a few exceptions can be observed from Fig. 3.16b, forming small islands on top of the sample. These islands can be solder balls that are still solid or molten solder balls that do not join with neighboring solder materials. Comparing Figs. 3.16c and d, we can also see the shape change due to surface tension of molten solder.

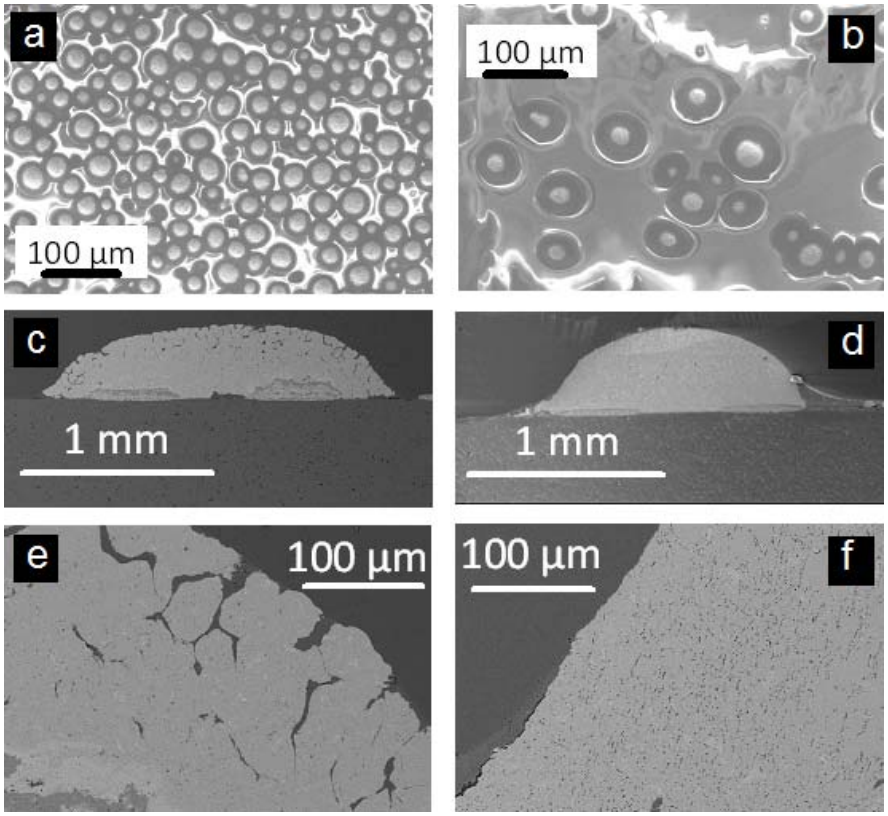

Figure 3.16. The (a, b) top view and (c, d, e, f) cross sectional view of solder B samples interrupted at (a, c, e) 3 s and (b, d, f) 8 s after resistance drops after THER.

3.3 Discussion

Figures 3.17a-f are illustrations of mechanisms identified during solder reflow based on the resistance signal and optical observations. Figure 3.17a shows the as-dispensed fresh solder paste. The solder balls distribute randomly in the matrix of the solder paste forming some conductivity resulting from a few random conductive paths in the solder ball network (percolation network) [69, 70] in the case of solder B only. Such networks seem to not have formed in solder A for which conductivity possibly is only due to ions in the organic matrix of the solder paste. This conductivity corresponds to the initial resistance R_{Ainit}, as shown in Fig. 3.17f.

In Fig. 3.17b, as the solvent in the solder paste vaporizes, the total volume of the flux becomes smaller, and the packing of solder balls becomes more compact, forming more conductive paths in the solder ball network, resulting in a lower [69] resistance reading than in Fig. 3.17a. Solvent vaporization typically happens during the early stage of reflow, and can also happen during long term room temperature storage, which explains the initial low as-dispensed resistance of solder B, as shown in Fig. 3.17f. While the difference of the initial resistance between solder A and B is six orders of magnitude, the final resistance difference is not statistically significant, with $R_{\mathrm{Afinal}} = 131 \pm 67$ mΩ, and $R_{\mathrm{Bfinal}} = 148 \pm 90$ mΩ, as shown in Table 3.3.

In Fig. 3.17c, THER is explained with flux segregation, which is mainly observed in solder B, as shown in Fig. 3.17f. The flux segregation may result from high surface tension of flux when it melts [71-73]. The aging of solder B during the long time in the shelve possibly resulted in a change of the surface tension of the organic parts of the paste, resulting in the flux segregation phenomenon (THER). For confirmation, the dependence of flux surface tension on storage time can be measured, which is not included in this thesis.

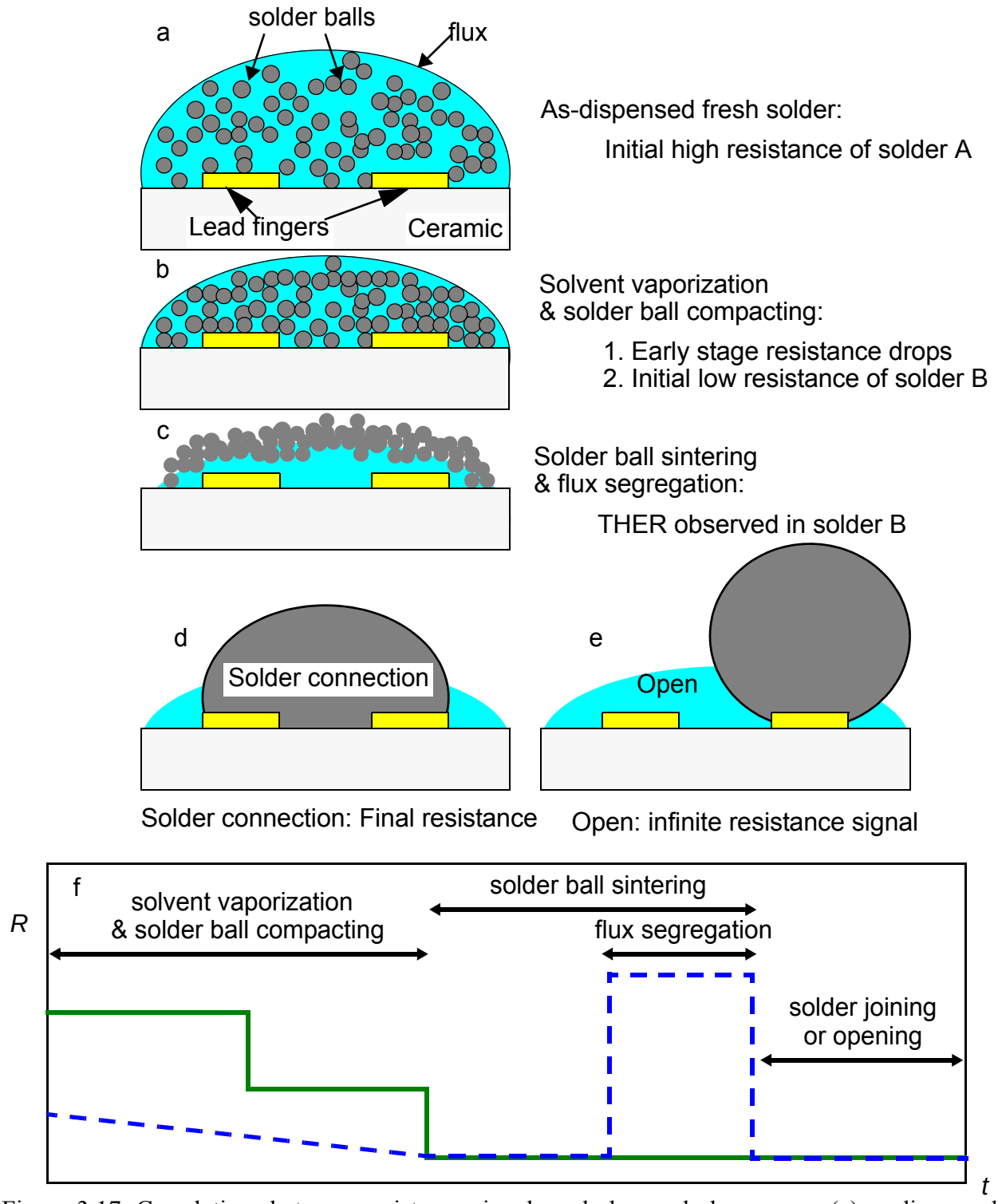

Figure 3.17. Correlations between resistance signals and observed phenomena: (a) as-dispensed fresh solder paste with high initial resistance; (b) solvent vaporization and solder balls getting more compact, with lower resistance signals; (c) solder ball sintering and flux segregation with THER, (d) solder melting and wetting both lead fingers, forming final connection with final resistance, (e) solder detached from one lead finger and joined with the other, with infinite resistance signals, and (f) resistance signal and events summarized.

After THER, melting, solidification, and IMC formation also occur, but none of them can be easily identified with the resistance signals shown. It is possible that more work can be done such as noise reduction of the setup to improve identification of melting and solidification from resistance signals.

Figures 3.17d and e show two typical possibilities after reflow. In Fig. 3.17d, the solder finally melts, wets both lead fingers pushing the flux away, and forms the final joint, which results in a small final resistance reading. In Fig. 3.17e, the solder is detached from one lead finger and is joined with the other, which results in an open, as shown in Fig. 3.17f.

3.4 Summary of Chapter 3

A method is reported to monitor real time resistance signals of microelectronic solder joints during the reflow process of solder paste. No less than 120, and 54 samples are tested for fresh, and 1-year-old SnPb solder pastes, respectively. Example results are presented and compared with microscopic observations.

Essential process mechanisms were detected such as percolation network compacting, flux segregation, and opening. Percolation network compacting in the early stage of solder reflow results in resistance drops. A flux segregation phenomenon was identified with expired solder which can result in open signal in the resistance curve. After reflow, the resistance signal shows immediately whether the joint is open or connected.

The method in this chapter can be used in a real time feedback loop in solder reflow process for process control, and/or efficiently help develop new microjoining materials such as new solder paste, to help overcome some challenges in the microjoining field today due to miniaturization.

Chapter 4 Real time resistance monitoring during sintering of silver paste

In this chapter, the sintering process of silver paste is studied with an improved real time resistance monitoring technology based on the method used in Chapter 3. A larger range of resistance measurement (10^{-5}-10^{11} Ω) is presented, and a more continuous measurement than previous methods [34, 36, 41] is provided.

In Section 4.1, the experimental method is described including the material used, the sample preparation process, the resistance monitoring process, and cross sectioning method. Section 4.2 includes example resistance curves, microscopic studies, finite element (FE) studies to determine material resistivity, and differential scanning calorimetry (DSC) studies. Signals of joint resistance show events such as resistance increase to >10 GΩ, abrupt resistance drop from >10 GΩ to <1 kΩ, and gradual resistance drop to <1 mΩ. Distinct clusters of sintered silver is identified from samples removed from the oven when the resistance drops to ~2.94 Ω. In Section 4.3, based on cross-sectioning of samples at various stages of sintering and DSC results, a correlation between resistance signal and solvent evaporation, capping agent degradation, and silver sintering is proposed.

4.1 Experimental

4.1.1 Materials

The example material is a commercially available SSP, Loctite Ablestik SSP 2020 [74-76]. The ingredients are shown in Table 4.1 [77]. The SSP is a silver sintering paste containing a mixture of silver particles, 2-(2-butoxyethoxy)ethyl acetate as capping agent, and 1,1'-oxydipropan-2-ol as solvent [78].

4.1.2 Sample preparation

The SSP is dispensed with a Nordson Ultimus I automatic dispenser, with parameters shown in Table 4.2. The substrate is ceramic side-brazed dual in-line packages (Spectrum CSB02801). Figure 4.1 shows the top view optical image of the as dispensed samples. All 28 lead fingers are connected with the SSP in order to maximize the use of the 28 terminals on the sub-

Table 4.1. SSP ingredients [77]

Chemical name	wt.%
silver flakes and spheres	balance
2-(2-butoxyethoxy)ethyl acetate (capping agent, boiling point 245 °C, flash point 102 °C)	1-5
1,1'-oxydipropan-2-ol (solvent, boiling point 232.8 °C, flash point 138 °C)	1-5

strate. After dispensing, to minimize sample change such as room temperature sintering, or solvent vaporization, the sample is either used immediately, or covered and stored in a freezer.

Figure 4.2 shows the sample design. Terminal numbers are indicated and the 12 resistance signals R1-R12 are defined. In this configuration, up to 12 segments of SSP can be monitored simultaneously in the sintering process, and all 12 segments of SSP can be measured with 2-wire, and 4-wire methods.

Table 4.2. Silver paste line dispensing parameters

Tip inner diameter [mm]	Speed [mm/s]	Pressure [psi]
0.33	4	15

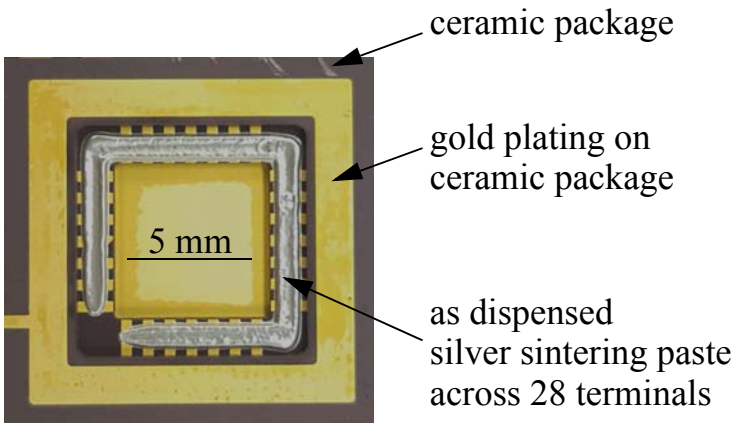

Figure 4.1. A top view optical image of the ceramic package with the as dispensed SSP.

4.1.3 Sintering and resistance measurements

The sintering profile recommended by the manufacturer is 4 hours at 175 °C. The oven is preheated to the sintering temperature. After the sample is connected, the resistance measurement starts running for a short time, typically 9 min, in room temperature, with cover removed at around 5 min, before the sample unit is placed into the oven. After the sintering time is reached, the oven stops heating, and the samples are left inside the oven to cool down.

For the test setup, a list of components is shown in Table 4.3. The oven, multiplexer, connecting materials, and temperature measurement are the same as in Chapter 3. In addition, an Agi-

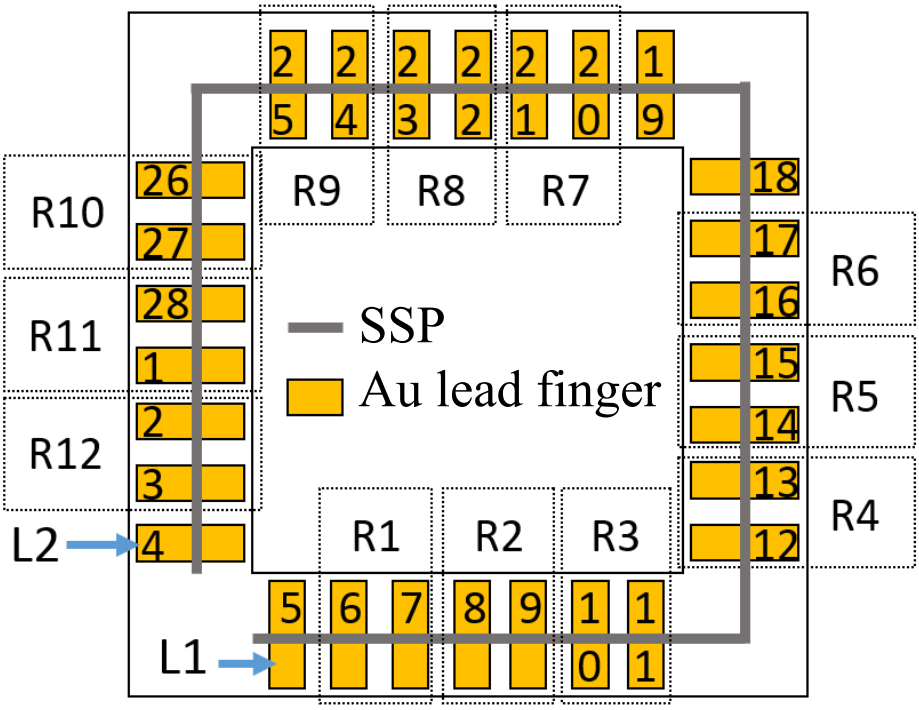

Figure 4.2. SSP resistance measurement scheme.

lent B2911A precision source/measure unit and an Agilent 34420A nanovoltmeter is used for resistance measurement, in 2-wire configuration (for >1 Ω) and 4-wire configuration (for <1 Ω), respectively. In 2-wire configuration, both auto, and manual resistance measurement modes are used with B2911A for low, and high resistance values, respectively. The auto mode of B2911A can measure 1 μΩ-200 MΩ. For manual mode, the voltage and current are set manually for different resistance range requirements. For example, when the voltage and current setting is 20V/100nA, the resistance range is 10 kΩ-20 TΩ. As a result, a total of three resistance measurement modes are used including 4-wire mode with 34420A, 2-wire auto mode, and 2-wire manual mode with B2911A, respectively. When all the three modes are enabled, the resistance measurement range is 1 μΩ-20 TΩ. Single mode can be used for faster sampling rate. For example, with B2911A manual mode only, the sampling rate is 17 readings/s. When all three modes are enabled, the sampling rate is 2.5 s/reading.

Figures 4.3a and b show the connection schemes used for resistance measuring with 2-wire and 4-wire, respectively. Samples R1-R12 are connected to and measured by the multimeter sequentially, by closing one of the 12 switches while opening the other 11 switches in each measurement loop. Both *R-t* and *T-t* curves are visualized in real time on the PC screen.

Table 4.3. List of components in the silver sintering resistance monitoring system

Component*	Description
Matlab code	RmonitoringSSP_v20170802.m; Available online at [79]
Nanovoltmeter	Agilent 34420A
Precision source/measurement unit	Agilent B2911A
SBDIP	SBDIP with SSP samples (see Fig. 4.1)

*In addition to #1, 3, 4, 6-10 in Table 3.2

The measuring process is controlled with a custom designed Matlab program, and the flow chart of an example monitoring process is shown in Fig. 4.4. In this example, all 12 samples are monitored with all three resistance measurement modes. Alternatively, the monitoring process can

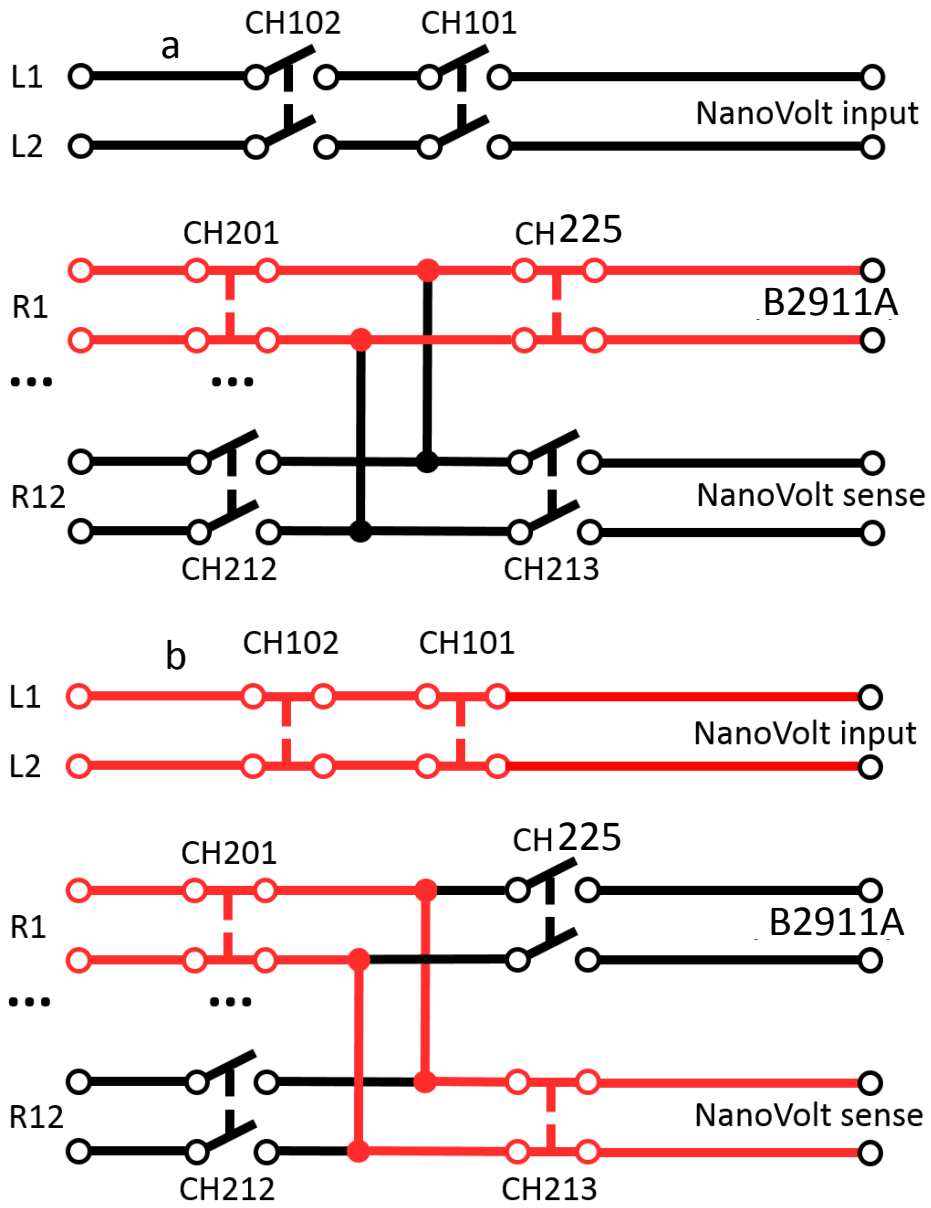

Figure 4.3. Connection scheme for resistance measurement in (a) 2-wire, and (b) 4-wire modes, respectively. CH numbers identify switches within the equipment.

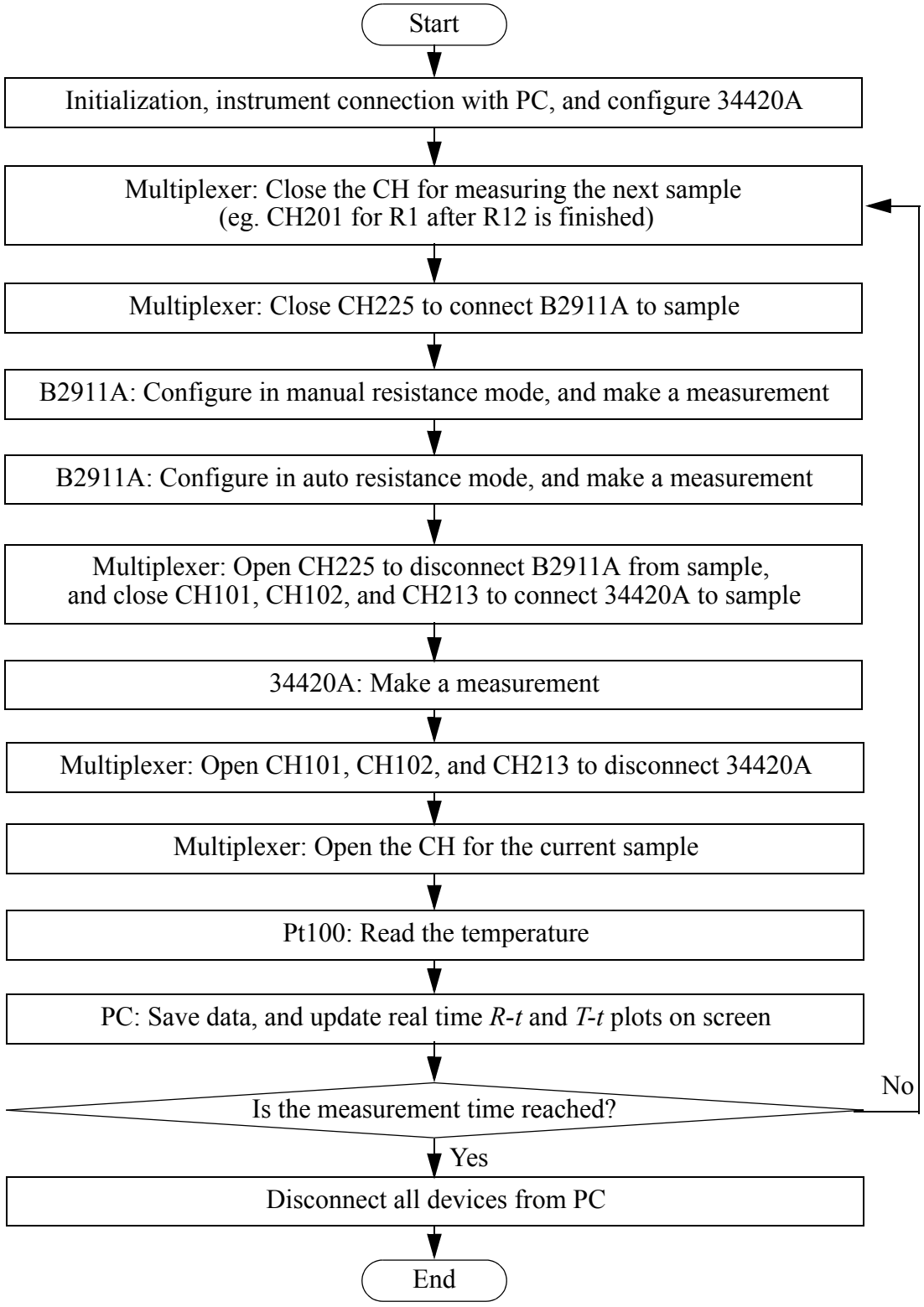

Figure 4.4. Matlab program flow chart of an example monitoring process during silver sintering. (File name: RmonitoringSSP_v20170802.m; Available online at [79] and [55])

be done on fewer samples, and/or with fewer resistance measurement modes, for faster sampling rate. The file name of the Matlab code is RmonitoringSSP_v20170802.m. It is available for download from matlab central [79].

4.1.4 Cross sectioning of interrupted samples

Some samples are interrupted at various times when special events on the resistance signal appear during the sintering process, and are taken out of the oven to cool in air for subsequent cross sectional studies.

The final polishing is done manually with diamond paste for sufficiently hard samples. Some not fully sintered samples are too soft to be polished mechanically at room temperature, and thus are cooled down to -40 °C with liquid nitrogen, and ion milled.

4.2 Results

4.2.1 Sample images and geometry

Figures 4.5a-b show the top view microscopic images of the SSP sample before, and after sintering, all taken with environmental scanning electron microscope (ESEM, WATlab at University of Waterloo). The mass loss after sintering is 9.3 %, as measured using a Sartorius CP124S analytical balance, which has a readability of 0.1 mg, and a range of 120 g.

Figure 4.6 shows cross-sectional outlines of the sample before and after sintering. The coordinates of the points are measured with an optical microscope from the top. The lines are obtained with piecewise cubic interpolation. The areas are calculated with trapezoidal numerical integration.

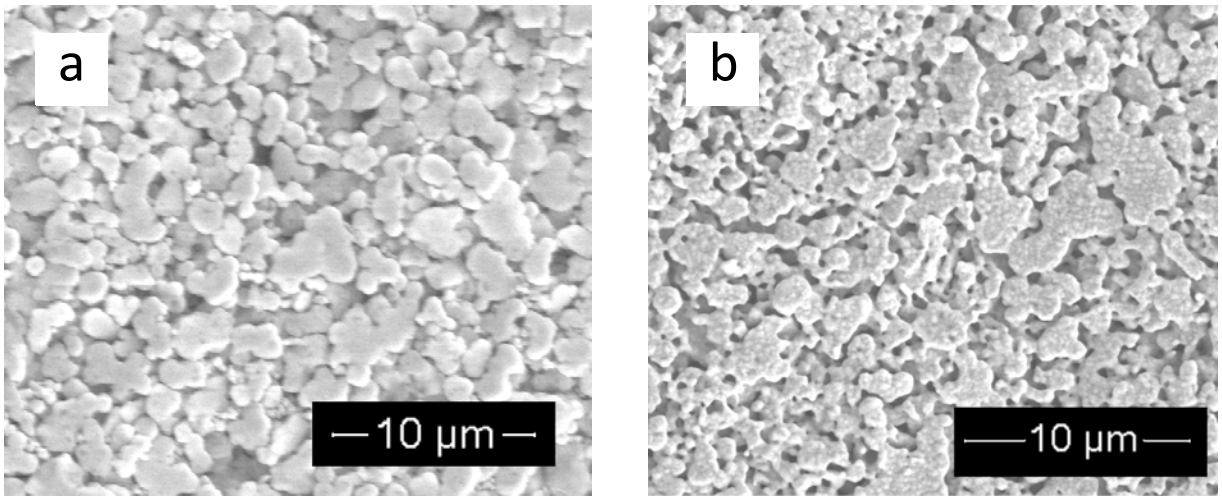

Figure 4.5. Top view microscopic images of (a) as dispensed SSP, (b) sintered SSP, both taken with environmental scanning electron microscope (ESEM, Watlab at University of Waterloo).

4.2.2 Resistance signals

Figure 4.7 shows the overview of raw *R-t* curves obtained from monitoring a single SSP sintering sample (R1 in Fig. 4.2) with all three resistance measurement modes. Due to the different range and configuration, for each mode, the resistance curve is valid only in certain segments. Before 30.85 min, the sample resistance is too large for the 2-wire auto mode or the 4-wire mode to make a measurement, and is only captured by 2-wire manual mode. At about 30.85 min, the sample resistance experiences an abrupt drop into the range of 2-wire auto mode, and becomes too low for 2-wire manual mode to measure. The readings of about 8 kΩ is the lower limit of the 2-wire manual mode. When the sample resistance drops to <1 Ω at about 37.11 min, the 4-wire mode starts making measurements, and the resistance reading difference between 2-wire auto

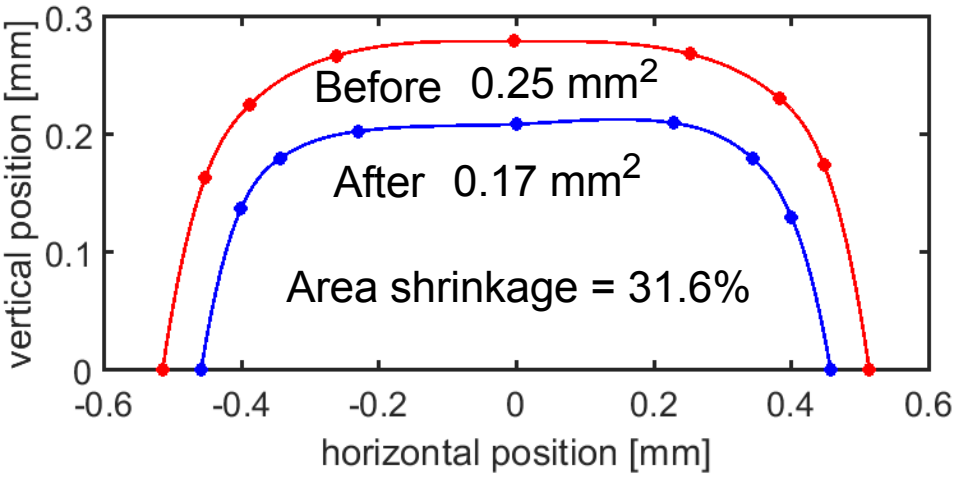

Figure 4.6. Cross-sectional outlines of the SSP before and after sintering, measured with optical microscope. Cross-sectional areas are calculated with piecewise cubic interpolation and trapezoidal numerical integration.

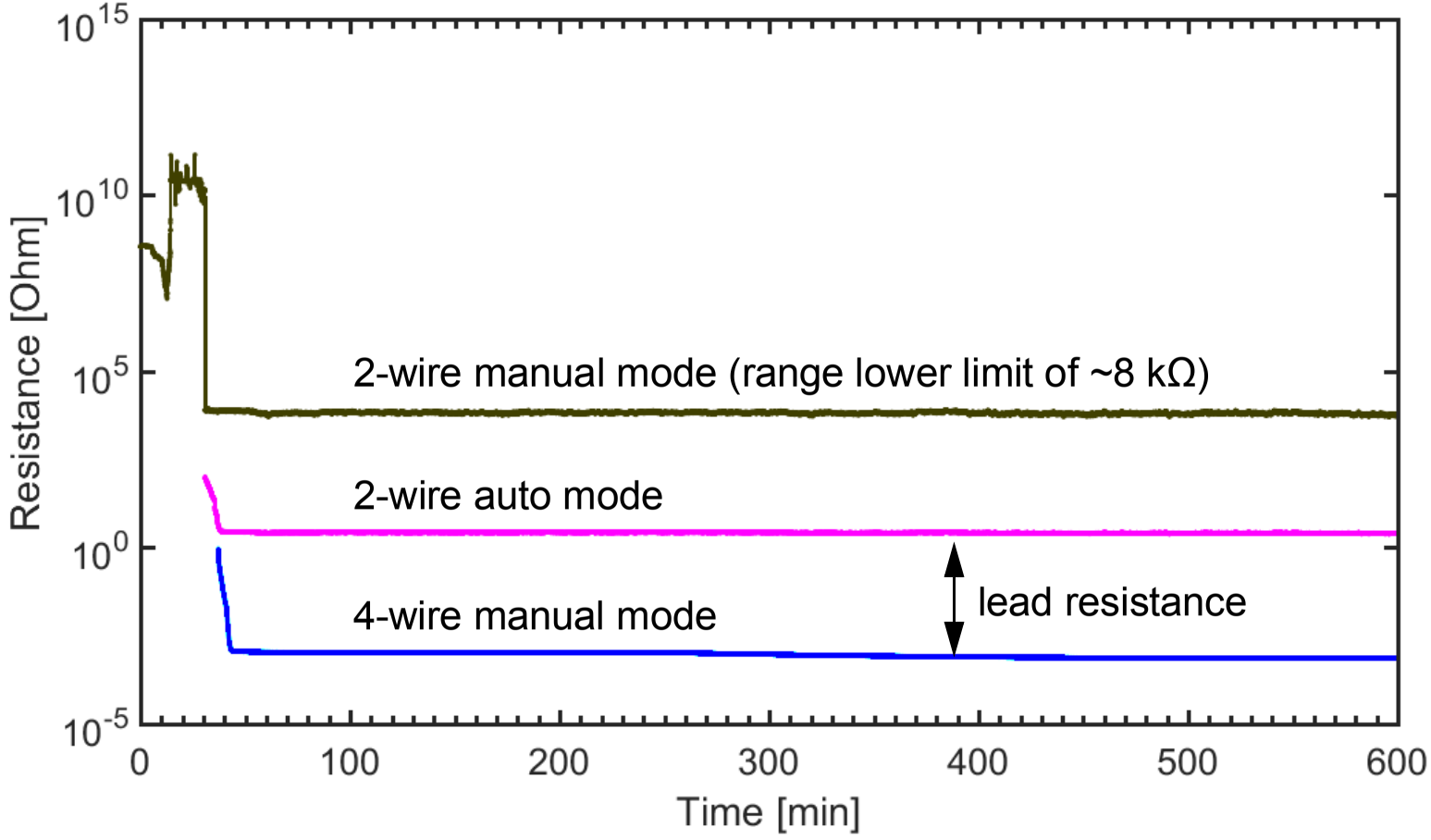

Figure 4.7. Three modes simultaneously: raw *R-t* curves during the SSP sintering obtained from single sample monitoring.

mode and 4-wire mode is the lead resistance, which is about 3 Ω. After raw data is obtained, the valid resistance curve segments from each mode are put together to form a complete resistance curve with only valid readings. The lead resistance is subtracted from the 2-wire resistances.

Figure 4.8 shows the overview *R-t* after post processing of the *R-t* curves in Fig. 4.7, and the corresponding *T-t* curve. Figures 4.9-4.11 show zoomed in parts from typical *R-t* and *T-t* curves. On the *R-t* curves of Fig. 4.9a and Fig. 4.10a, a sequence of six observations is made: 1. room temperature high resistance of 10^6-10^9 Ω, 2. resistance drop and rise forming a "V" shape signal until >10 GΩ, and 3. stable high resistance of 10-30 GΩ, 4. abrupt resistance drop from >10 GΩ to <1 kΩ, 5. steady resistance drop down to <1 mΩ, and 6. resistance change mainly following the temperature change.

A set of characteristic quantities is derived from the *R-t* curve, as shown in Figs. 4.9-4.10, and the values are shown in Table 4.4. R_0 and R_f are initial and final resistances at room temperature, which is approximately 25 °C, t_1 is the time after when the resistance signal is >10 GΩ, and T_1 is the corresponding temperature, t_2 is the time after when the resistance signal is <1 kΩ, and T_2 is the corresponding temperature, t_3 is the time when the resistance signal is 5 Ω, and T_3 is the corresponding temperature. The different sample size in Table 4.4 is because of the use of some incomplete *R-t* profiles from different resistance measurement modes.

Figure 4.12 shows a typical *R-T* curve during cooling. The *R-T* relation is linear. *R* values are interpolated at temperatures T = 60, 70,..., 170 °C and plot vs. T to determine the dR/dT slopes, resulting in correlation coefficient of >0.99 and slopes average and standard error of 2.60, and 0.06 μΩ/°C, respectively (182 samples). The temperature coefficient of resistance (TCR) is α = 4.31 ± 0.02 [10^{-3}K^{-1}], while the TCR of silver [80] is α_{Ag} = 3.8 [10^{-3}K^{-1}]. R_{ref} is the extrapolated resistance value at T_{ref}, and T_{ref} is the reference temperature 20 °C in this work.

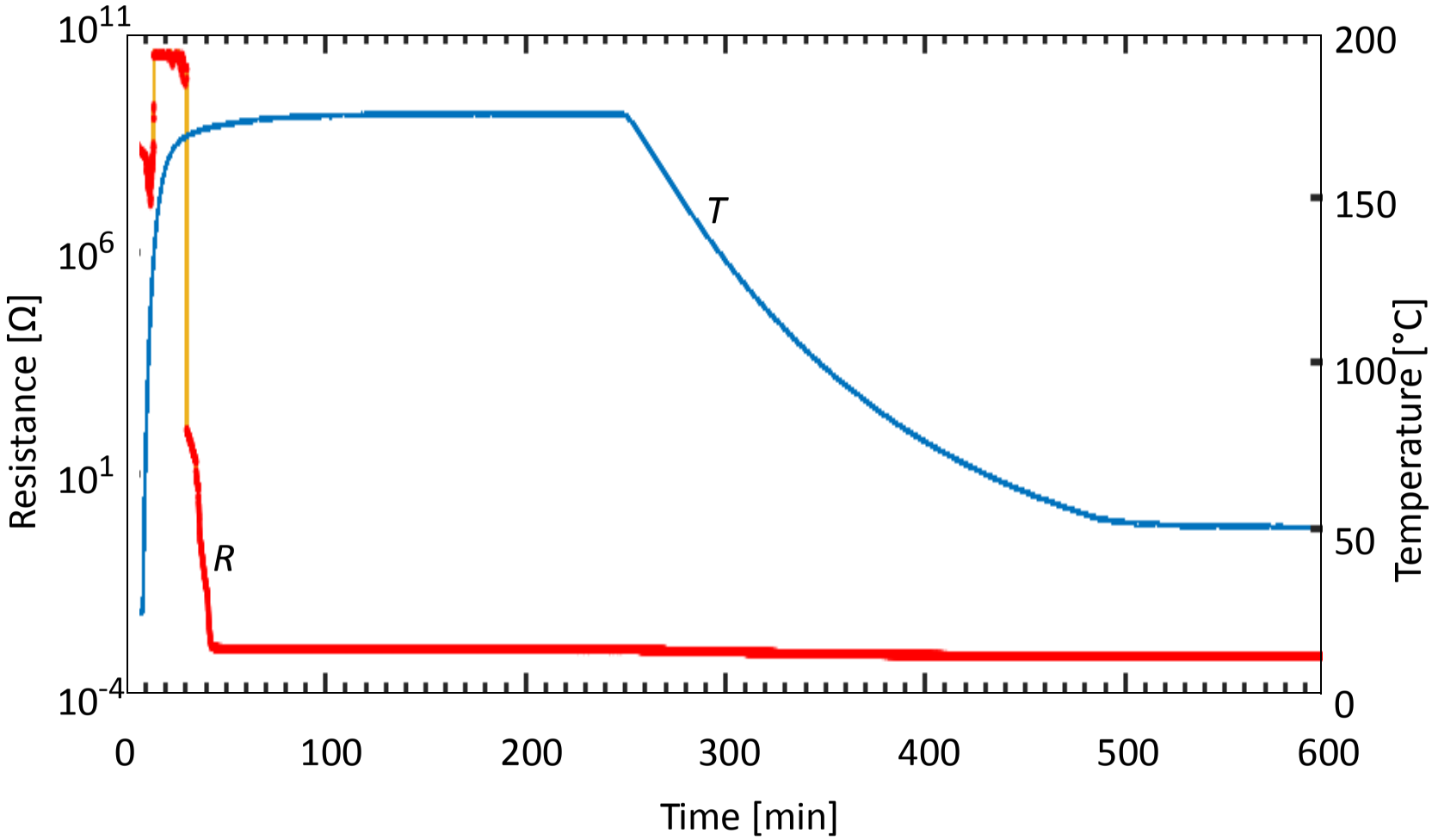

Figure 4.8. The *R-t* curve obtained from Fig. 4.7 by taking valid segments of each curve (0-30.85 min of 2-wire manual mode, 30.85-37.11 min of 2-wire auto mode, and 37.11-600 min of 4-wire mode), and the corresponding *T-t* curve. Lead resistance of 3 Ω is subtracted from the 2-wire readings.

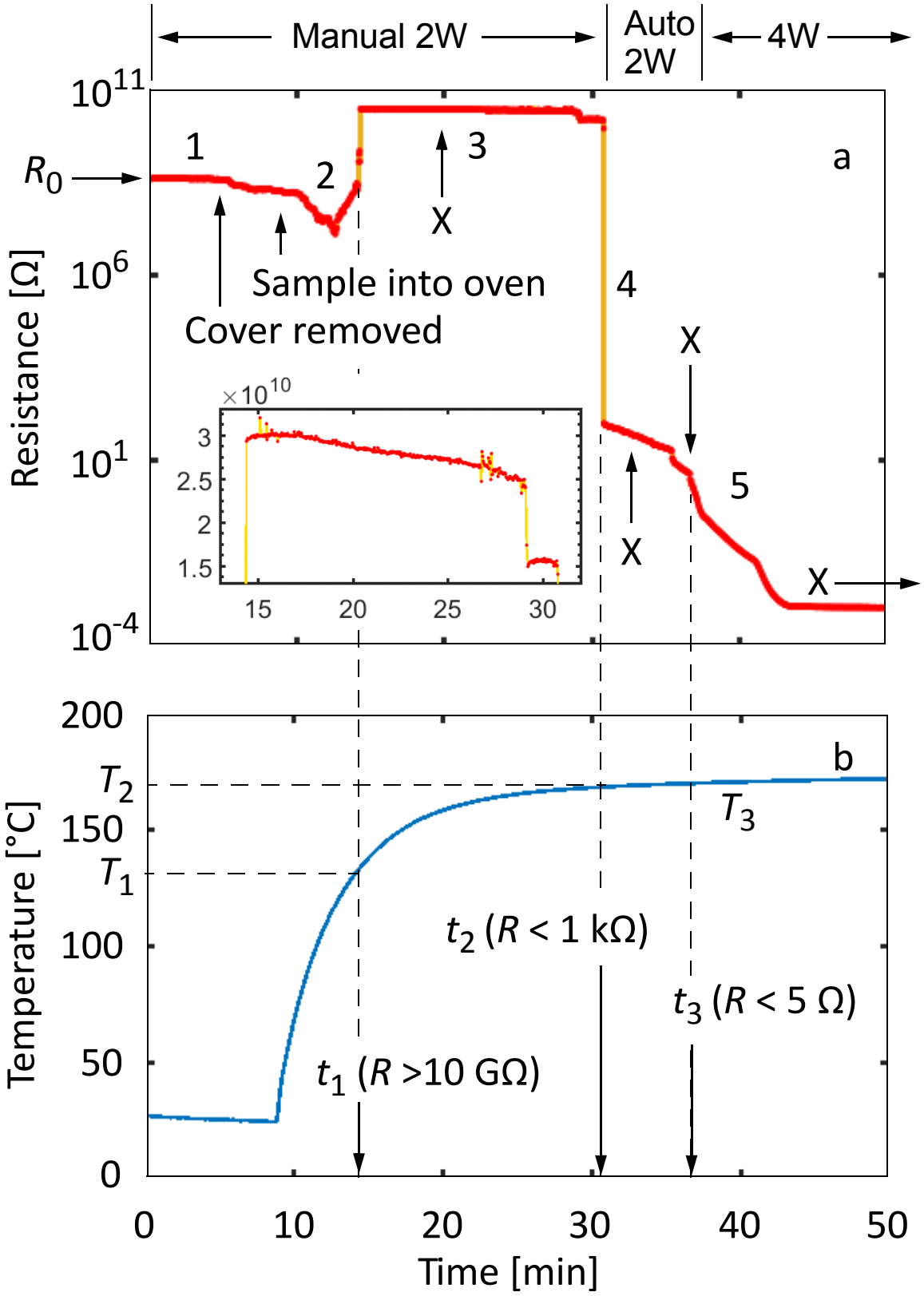

Figure 4.9. (a) *R-t* curve in Fig. 4.8 zoomed at 0-50 min, label X's indicates times when cross-sections are taken. (b) corresponding *T-t* curve. Inset of a is zoomed in at 15-30 GΩ

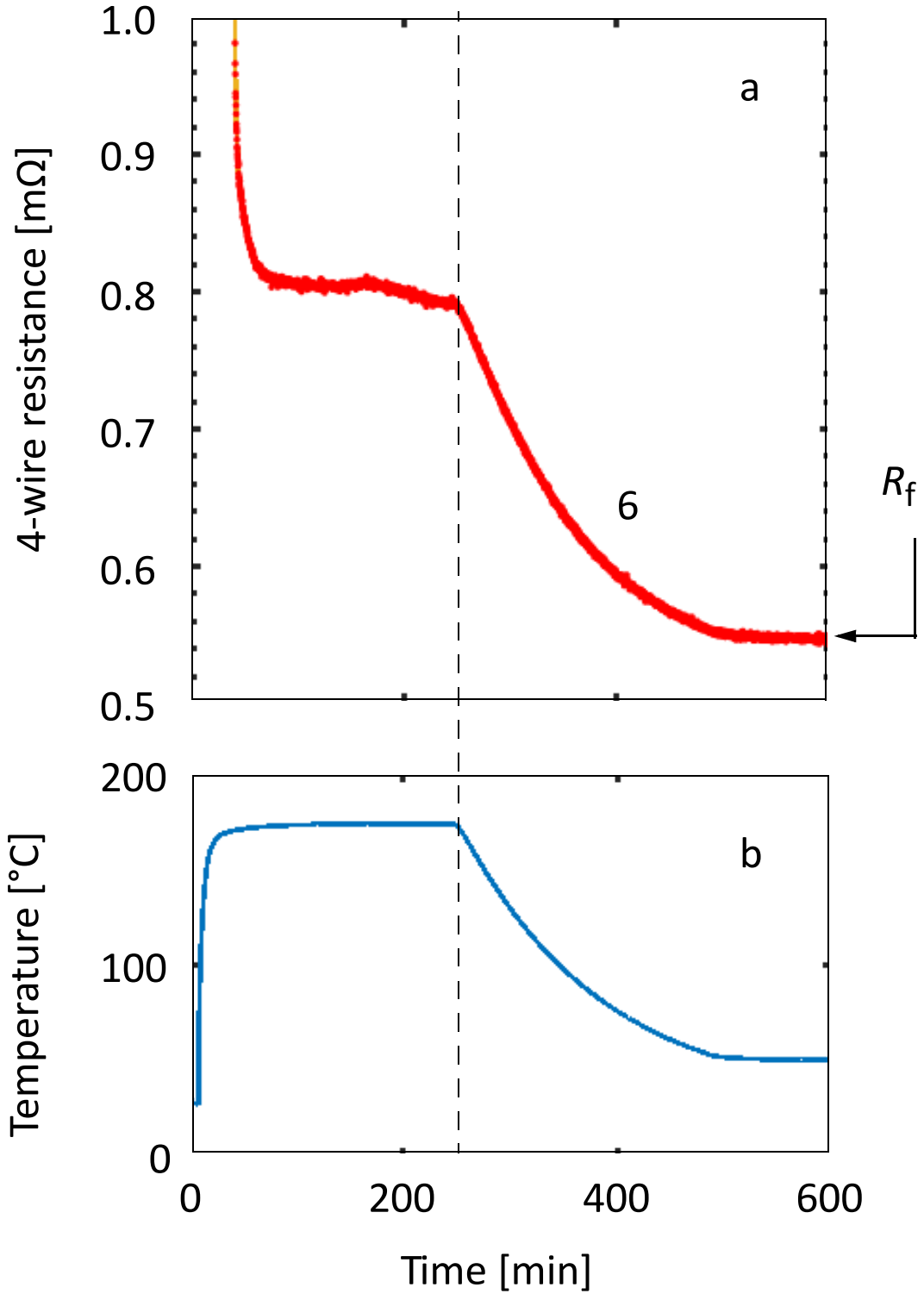

Figure 4.10. (a) *R-t* curve zoomed to 0.5-1 mΩ, and (b) corresponding *T-t* curve.

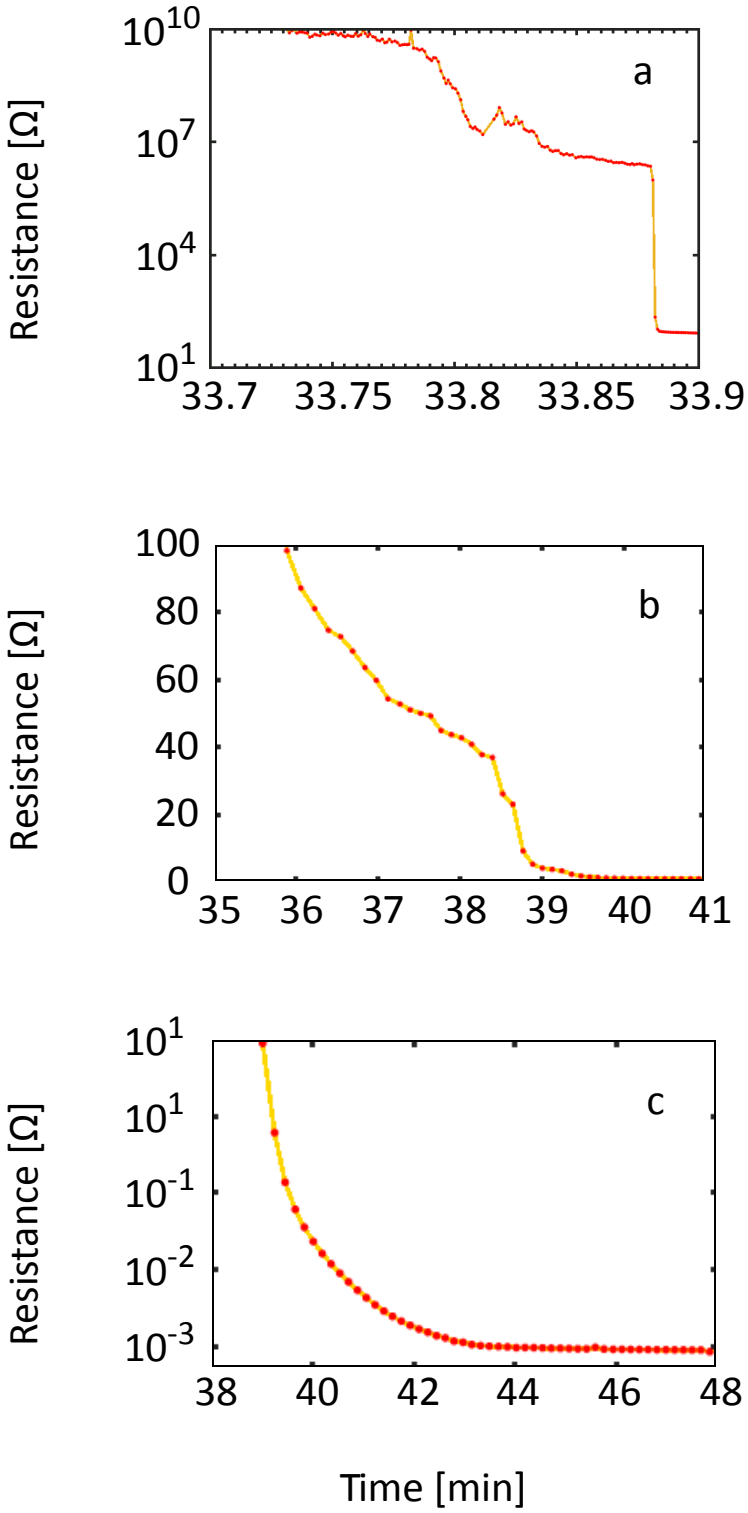

Figure 4.11. Example *R-t* curves zoomed at (a) around t_2 (33.7-33.9 min), (b) around t_3 (0-100 Ω, 35-41 min), and (c) after t_3 (0.5 mΩ-10 Ω, 38-48 min), respectively.

Table 4.4. Characteristic values in sintering

	average	standard deviation	number of SSP samples used in calculation [unit less]
log (R_0/1Ω)	7.3	0.5	222
t_1 [min]	15.1	0.6	63
T_1 [°C]	133.8	5.5	63
t_2 [min]	30.4	3.5	83
T_2 [°C]	168.8	1.2	83
t_3 [min]	36.1	5.6	214
T_3 [°C]	170.7	1.2	214
R_f [mΩ]	0.54	0.25	148

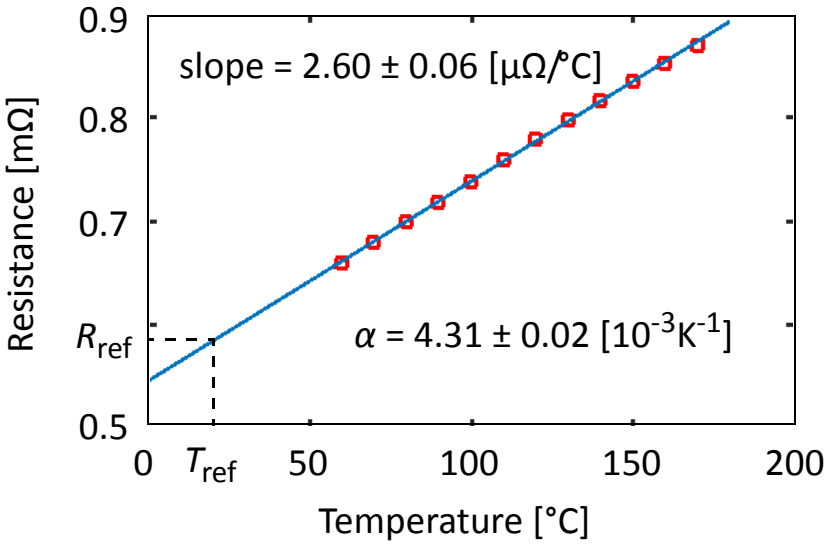

Figure 4.12. An example *R-T* curve in cooling stage of the sintering process. The TCR value is calculated with a reference temperature of 20 °C. The values shown are average ± standard error, with 182 samples. The standard deviations of slope, and α are 0.81 μΩ/°C, and 0.27 [$10^{-3}K^{-1}$].

4.2.3 Determining the resistivity of sintered paste

Figure 4.13, and Fig. 4.14 show the geometry and mesh of a finite element (FE) model for a sintered sample segment, respectively, where the cross section of the sintered paste is taken from Fig. 4.6. The conductivity of the lead fingers is that of Ni 14.3 MS/m. The resistance calculation method is shown in Fig. 4.15.

Figure 4.16 shows the dependence of R_{fem} from the FE study on the SSP conductivity (σ_{SSP}). Taking the value of R_f shown in Table 4.4 as R_{fem}, the resistivity of the sintered SSP is thus calculated as 55-180 nΩ•m, while the resistivity of pure Ag is 1.59 nΩ•m [80].

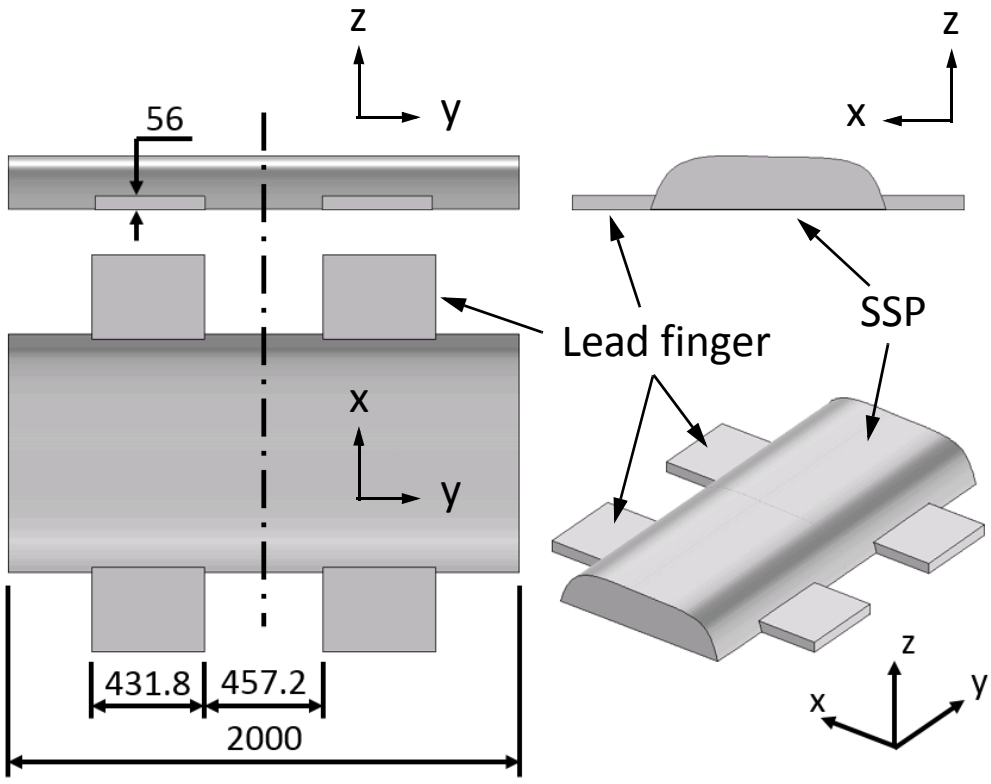

Figure 4.13. FE model geometry (unit: μm), outline of SSP after sintering taken from Fig. 4.6.

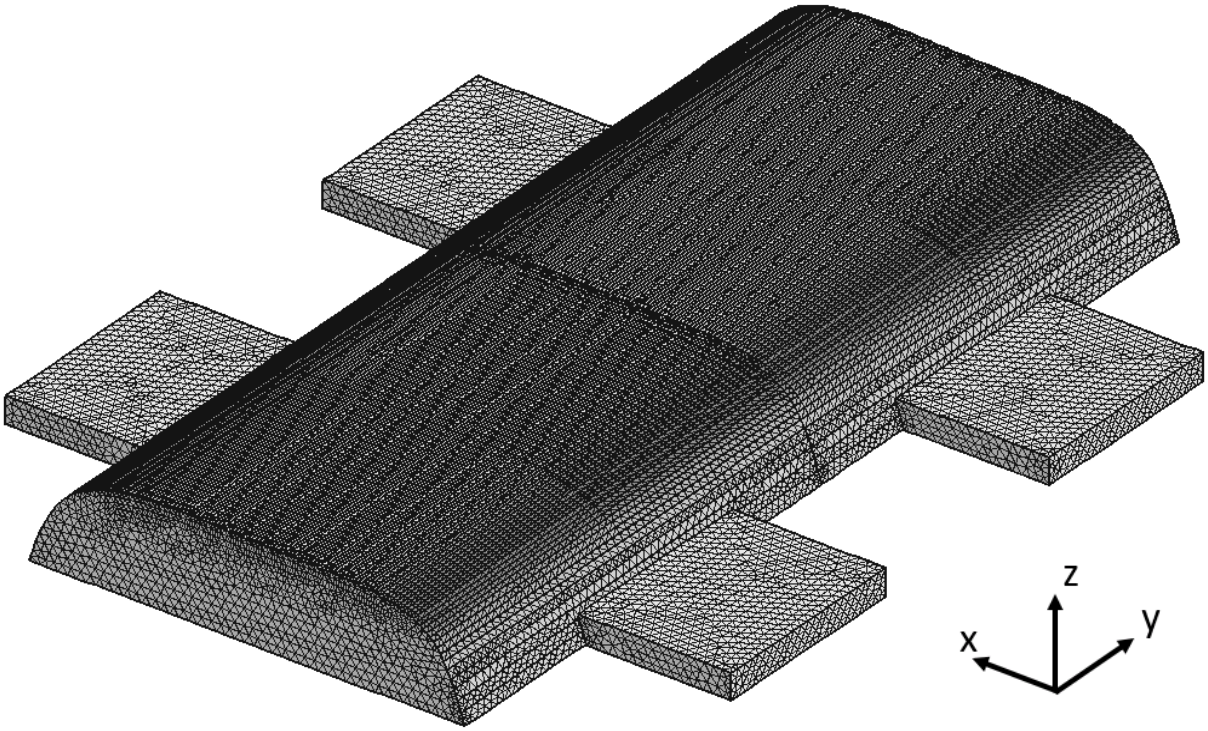

Figure 4.14. Mesh of the FE model.

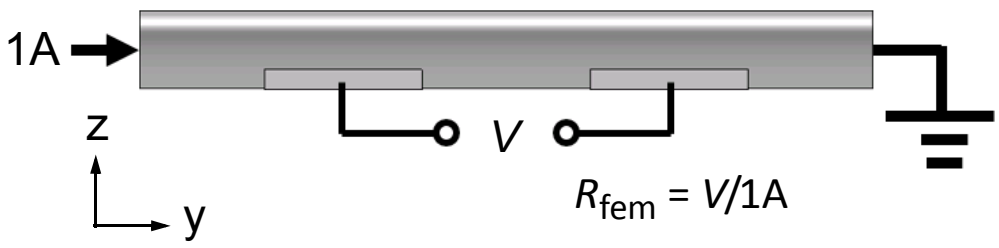

Figure 4.15. Resistance calculation with FE model (side view), where V is the difference between the two surface average potentials

4.2.4 Microscopy of interrupted samples

Figures 4.17a-d show the cross sectional images of the interrupted samples. Specifically, samples are taken out of the oven around t_1, t_2 and t_3, respectively. From the *R*-*t* signals, the sample in Fig. 4.17a is taken out of the oven at about t_1 + 5.4 min, and the resistance signal stays >10 GΩ afterwards. The sample in Fig. 4.17b is taken out of the oven at about t_2 + 2.5 min and the final resistance is 253.2 Ω with standard deviation of 233.5 Ω. The sample in Fig. 4.17c is taken out of the oven at about t_3 and its resistance is 2.94 Ω measured at room temperature. In Fig. 4.17d, the sample sintering is finished (t = 600 min).

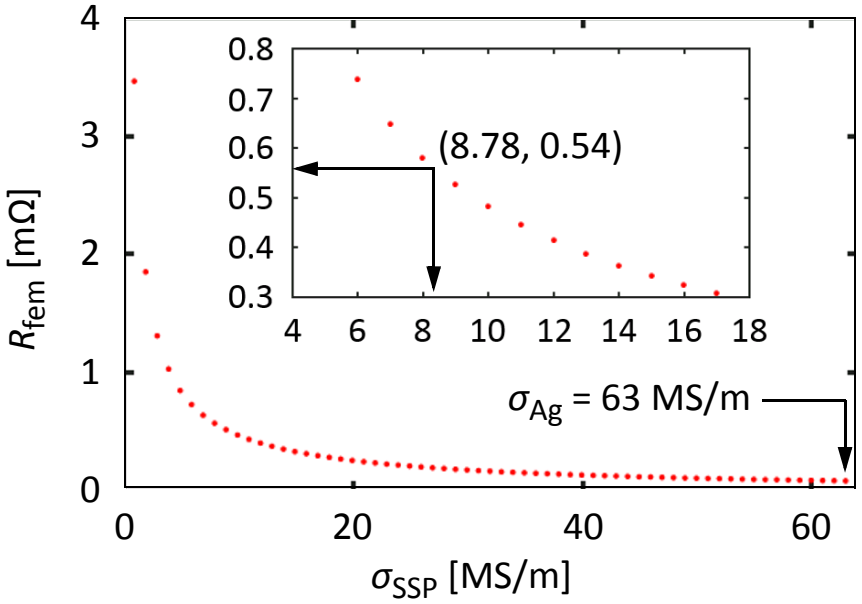

Figure 4.16. R_{fem} vs. SSP conductivity from FE model

As the solvent evaporation continues during cross-section sample preparation, negligible amount of remaining solvent is assumed to exist in any of the samples shown in Figs. 4.17a-d.

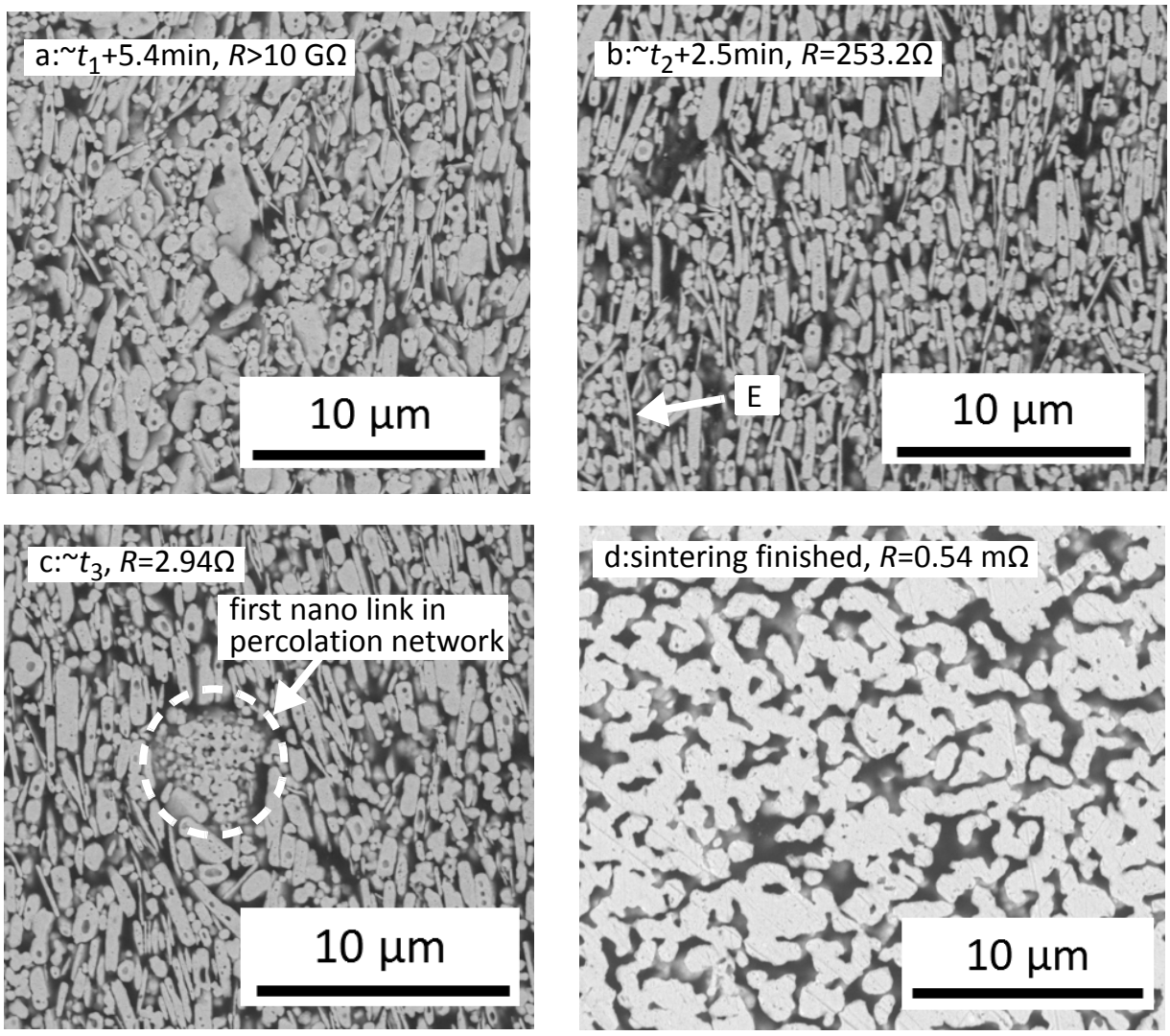

Figure 4.17. Typical cross-sectional images from samples interrupted (a) between t_1 + 4.7 min and t_1 + 6.1 min, (b) between t_2 and t_2 + 5 min, (c) at about t_3, during the sintering process, and from (d) a sample after sintering is finished. All images are taken with environmental scanning electron microscope (ESEM, Watlab at University of Waterloo).

Figures 4.17a and b show high similarity, where mainly seen is a crowd of 200 nm - 4 μm silver particles. Figure 4.17c shows a cluster of sintered silver particles in the center as indicated with the arrow, and is otherwise the same as Figs. 4.17a and b. Three instances of sintered silver clusters made from particles smaller than 1 μm are found in a 500 μm × 200 μm cross-section segment. The distance between neighboring clusters found is >50 μm. Figure 4.17d shows a connected network of sintered silver obtained after 600 min.

4.2.5 Open pan DSC

Figures 4.18a and b show the ramping and isothermal segments of an open pan DSC study of the SSP, respectively. There was no air flow in the experiment. The temperature profile is set to ramp at 10 °C/min from room temperature to 175 °C, and hold at 175 °C for 10 h. The data after 350 min at 175 °C has no obvious peaks, and is not shown. The noise due to temperature profile change is shown in light green color.

One endothermic peak of -33.7 mW/g is observed during ramping stage at 147.7 °C, which is possibly caused by solvent evaporation. Two exothermic peaks of 9.9, and 20.2 mW/g are observed during isothermal stage after 26.3 min and 107.8 min at 175 °C, respectively, which are possibly caused by capping agent degradation, and silver sintering, respectively. The capping agent degradation may involve oxidation or even combustion [81-83].

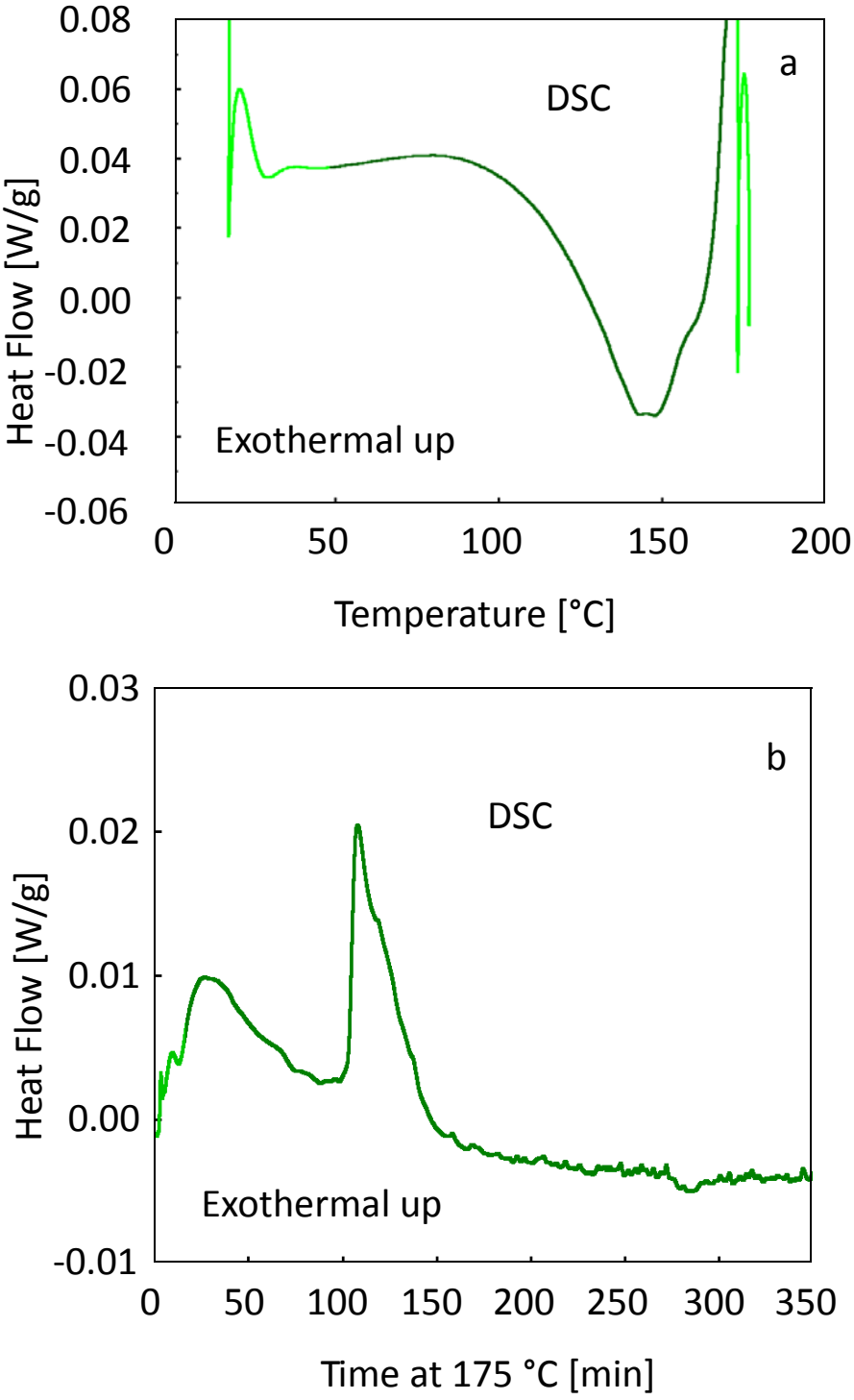

Figure 4.18. Heat flow vs. (a) temperature during ramping stage from room temperature to 175 °C at a rate of 10 °C/min, and (b) time during subsequent isothermal stage at 175 °C. The noisiness in the light color segments of the curves results from change in temperature.

4.3 Discussion

This section discusses the observations and gives possible explanations. Figure 4.19 shows a proposed correlation between the resistance signal and the sintering process.

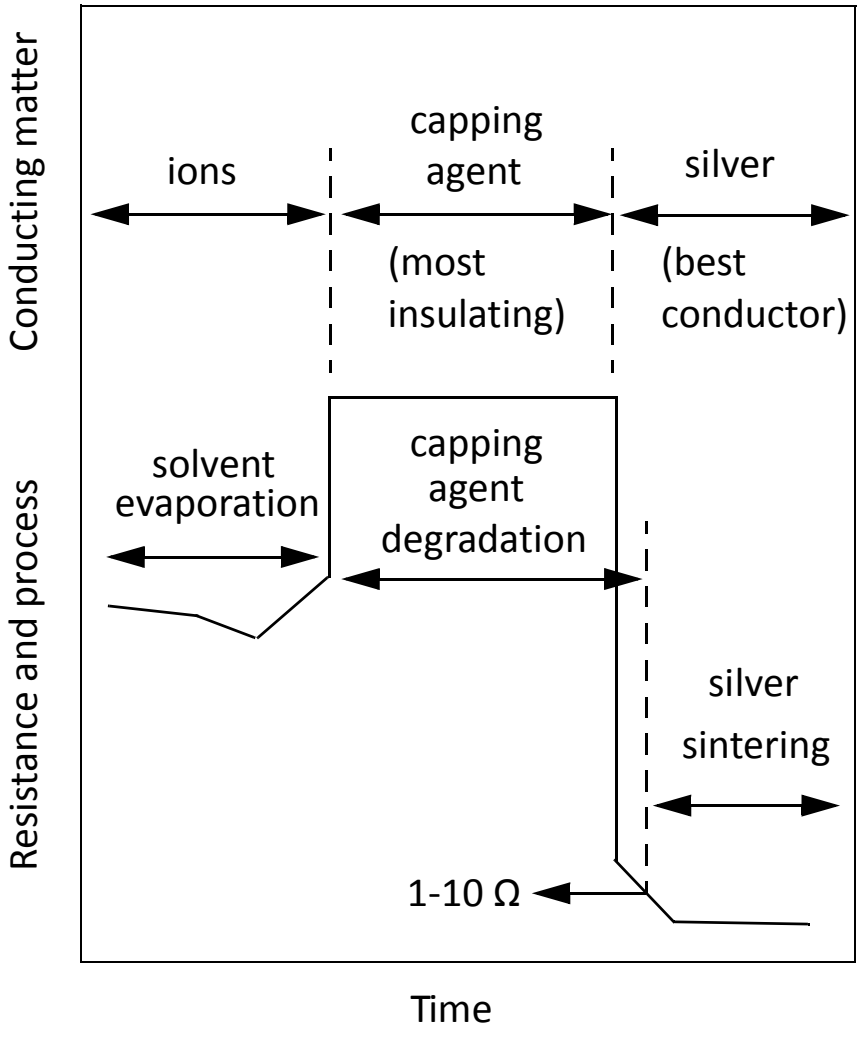

Figure 4.19. Proposed correlation between resistance signal and the sintering process of the SSP.

4.3.1 Solvent evaporation and capping degradation

Initially, due to the existence of solvent and capping agent, it is difficult for free electrons to move between silver particles, leading to high value of R_0. The resistance is dominated by ions in the solvent. Both organic chemicals shown in Table 4.1 are polar molecules, and dissolve free ions, including Cl^-, K^+, and Na^+ [84].

The main event in the early stage of the sintering process is solvent evaporation [85]. According to the DSC study shown in Fig. 4.18a, the solvent evaporation peak temperature is 147.7 °C. During solvent evaporation resistance decreases and subsequently increases as shown in Fig. 4.9a. The resistance decrement is due to the temperature rise as ion mobility increases with temperature. The subsequent resistance increment is caused by the solution amount decrement due to solvent evaporation. At T_1, most of the conducting ions are believed lost with the solvent and the resistance increases strongly.

Between t_1 and t_2, the remaining conducting ions are too few to contribute to the sample conductivity. The high resistance values of 10-30 GΩ are dominated by the insulating property of the capping agent [38].

The capping agent degradation mainly starts after solvent evaporation [86, 87], which is around t_1. The capping agent degradation gradually makes the formation of conductive path easier [38]. The resistance drop at t_2 is possibly caused by the formation of the first conductive path. The steady resistance drop between t_2 and t_3 is possibly caused by further degradation of the capping agent and the formation of more conductive paths.

According to the DSC study shown in Fig. 4.18b, the capping agent degradation peak time is 26.3 min at 175 °C, which approximates t_3 (27.1 min in oven). The heat generated from capping degradation may add to the triggering of Ag sintering at t_3.

4.3.2 Silver sintering

The Ag sintering starts between t_2 and t_3, according to the observation of the first sintered Ag particle clusters observed in Fig. 4.17c. Without capping agent, bare Ag particles are readily joined together [87]. The driving force $\Delta\mu$ is the chemical potential difference between the atoms on the surface and in the bulk, given by [88]:

$$\Delta\mu = \Omega\gamma\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{4-1}$$

where $\Omega=1.7\times10^{-29}$ m^3 is the volume per atom in the solid silver bulk according to its lattice structure; γ is the surface tension, theoretically 890 mJ/m^2 for solid silver [89]; and R_1 and R_2 are the curvature radii of the two dimensions of the surface. For a spherical particle, $1/R_1+1/R_2$ and thus $\Delta\mu$ are the same along the surface. For a flake, $1/R_1+1/R_2$ and thus $\Delta\mu$ are largest on the edge. The thinner the flake, the higher $\Delta\mu$.

The $\Delta\mu$ drives surface atoms to diffuse to the bulk, or a surface with lower value of $1/R_1+1/R_2$. In a mixture of Ag particles, such diffusion can result in particle joining or particle shape change [87], typically reducing the total surface area.

In the case of particle joining, the atoms on the joining surfaces become bulk atoms, and thus the $\Delta\mu$ is reduced for these atoms. The total surface area is reduced by approximately twice

the joining area. In the case of particle shape change, a flake may change into a few small spheres. For example, for a 4 μm diameter and 100 nm thick round-edged disc (see label E in Fig. 4.17b), the $\Delta\mu$ is 3.1×10^{-22} J on the edge, the volume is 1.3 μm^3, and the total surface area is 27.1 μm^2. If it breaks into four identical spheres, assuming no total volume change, the $\Delta\mu$ is 7.1×10^{-23} J on the surface, the radius is 0.43 μm, and the total surface area is 9.1 μm^2. As a result, the maximum atomic $\Delta\mu$ is reduced by 77.1 %, and the total surface area is reduced by 66.4 %.

After t_3, the resistance drop is mainly caused by further Ag sintering and particle size growth in the sintered percolation network. Growth of sintered particles is observed in this work from comparing the cluster in Fig. 4.17c and the network in Fig. 4.17d. A larger size particle typically has lower average atomic $\Delta\mu$ because of the smaller surface area to volume ratio and a smaller $1/R_1+1/R_2$ value on the surface. For example, if four radius 0.43 μm spheres merge to form one large sphere without volume change, the total surface area change from 9.1 μm^2 to 5.8 μm^2, reducing by 36 %, and the surface $\Delta\mu$ changes from 7.1×10^{-23} J to 4.5×10^{-23} J, reducing by 37 %. Assuming the number of surface atoms is proportional to the surface area, the average $\Delta\mu$ is thus reduced by 60 %.

4.4 Summary of Chapter 4

Real time resistance monitoring technology is developed to study the process of silver sintering. The characteristic *R-t* relationship is obtained for the example SSP studied. The resistance change is explained with the physical and metallurgical evolution of the SSP during the sintering process, with the help of DSC and existing knowledge for SSP sintering. Essential mechanisms are detected with resistance signals, including solvent evaporation, capping agent degradation, and formation of first sintered clusters.

The resistance monitoring technology could be tested for process control with a real time feedback loop during the sintering process, and also for gaining knowledge and development of new SSP materials. Ultimately, the resistance monitoring technology may help overcome some current and/or future challenges in electronics packaging industry, such as increasing power density.

Chapter 5 Real time resistance monitoring in power cycling of solder joints

Two real time resistance monitoring setup designs are described with example results for power cycling of solder joints. The two designs are in Sections 5.1, and 5.2, respectively.

In the first design, Sn42Bi57.6Ag0.4 is studied as an example solder. One sample shows open resistance signal after 608 cycles, and cracks are observed between the solder and the chip resistor from the cross sectional images. Some solder joints experiencing too high peak temperatures appear grainy, while the corresponding resistance signals show insignificant change.

The second design has more uniform temperature distribution, and larger size chip resistors. Four solder types are studied with the second design including standard lead free solder SAC305. Resistance rise until open is observed for three solders including SAC305, and from their cross sectional studies, cracks are observed at the interface of the chip resistors and the solder joints. The solder with insignificant resistance change is Sn42Bi57.6Ag0.4, and it undergoes severe thermal degradation from the appearance of the solder joints.

5.1 Study I

5.1.1 PCB design

Figures 5.1a and b show the front and back views of the PCB design for study I. The photos

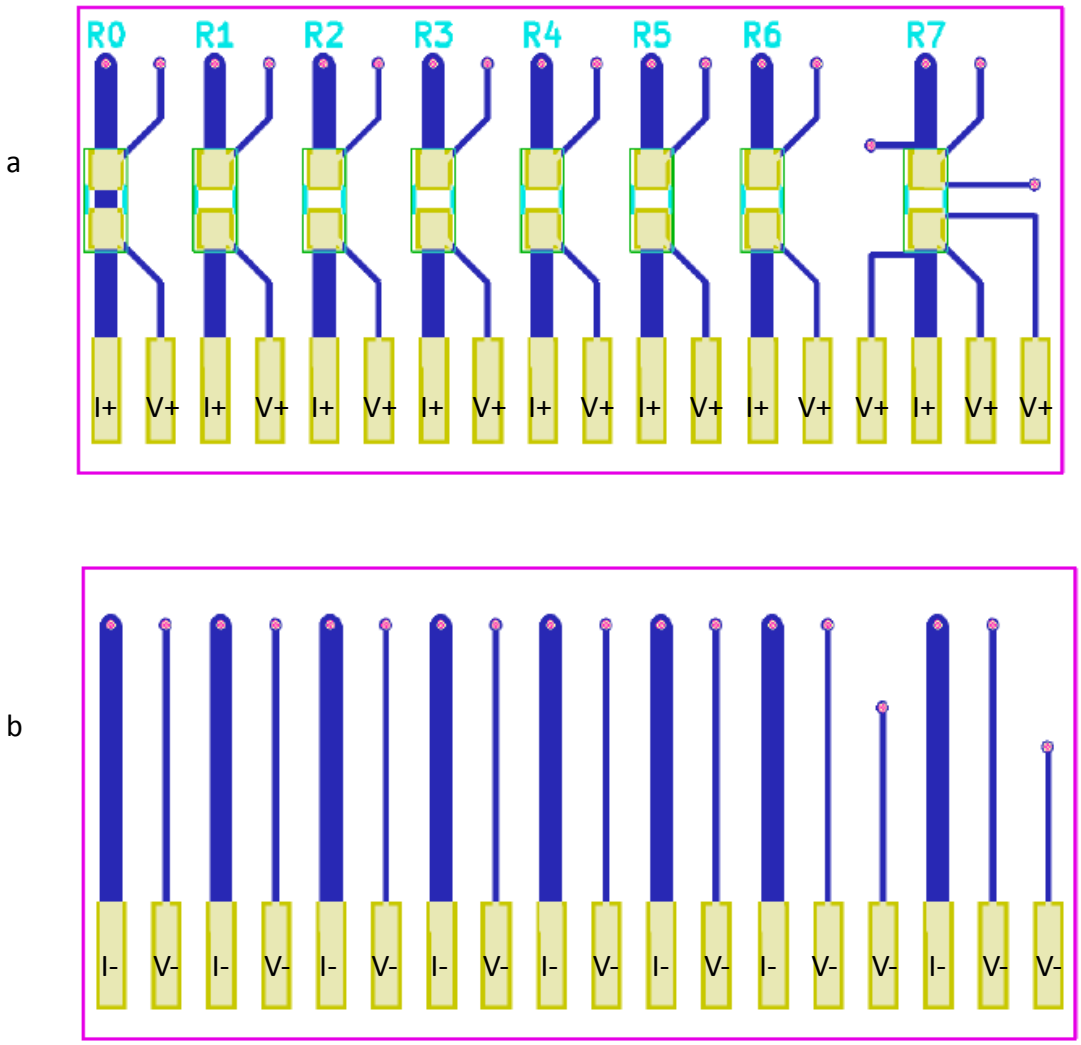

Figure 5.1. The (a) front and (b) back views of the PCB design for study I. The size of the PCB board is 46 mm × 22 mm.

of the front, and back are shown in Figs. 5.2a, and b, respectively. The PCB is designed with KiCAD, and is manufactured in PCBway in China. On one board, seven resistors can be power cycled simultaneously located at R1-R7, respectively. The pattern for R1-R7 is designed for regular chip resistance samples, while R0 is designed as a control group where the two solder pads are shorted, The R0 value is 1.65 mΩ at room temperature of 25 °C, and 2.49 mΩ at 150 °C, respectively.

a

b

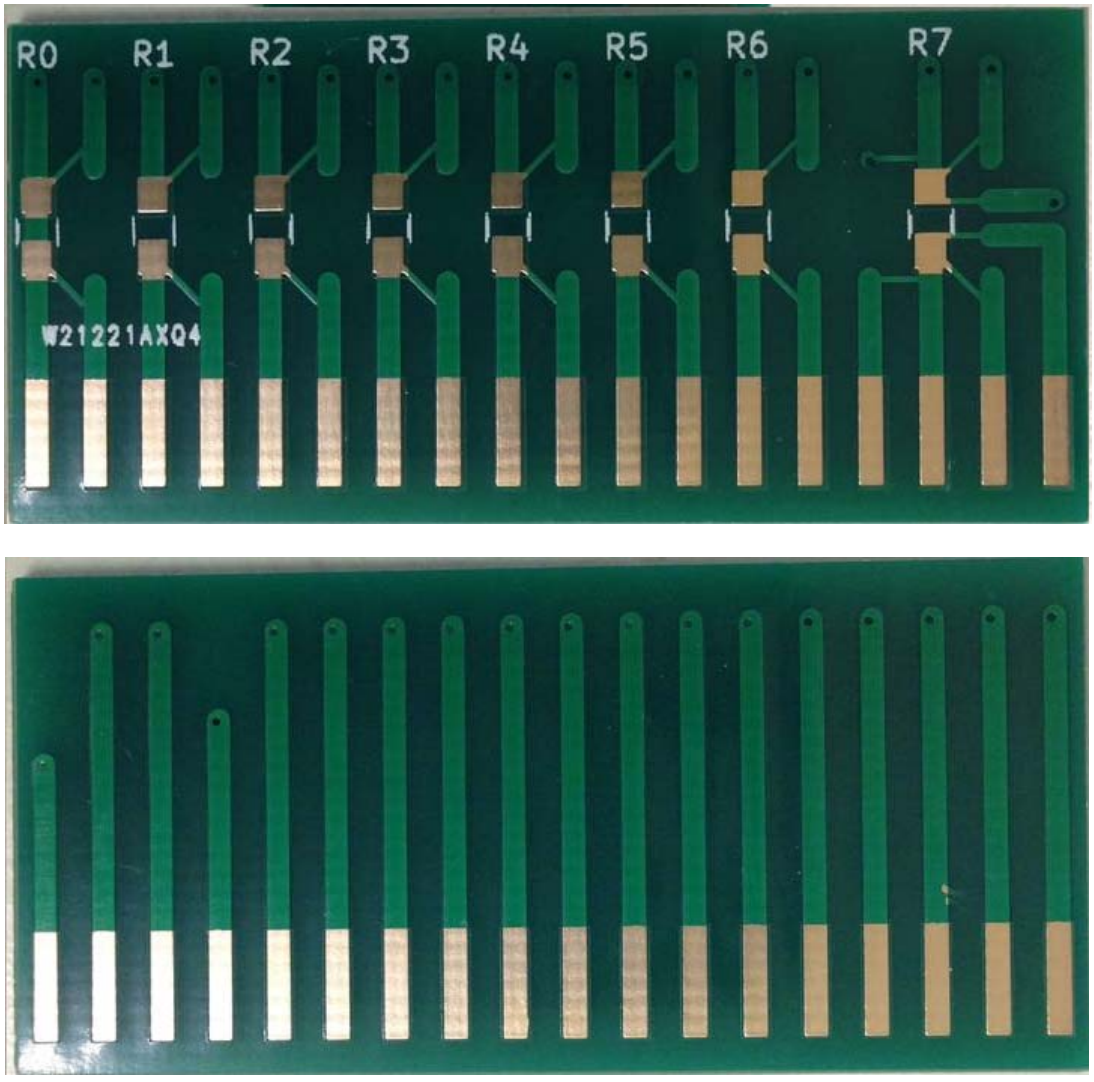

Figure 5.2. The (a) front and (b) back views photos of the PCB for study I.

The conductive copper lines have two different widths of 1 mm, and 0.25 mm, respectively. The wider lines are current lines, and are designed in order to achieve a uniform current density distribution in the solder joint, and to minimize electromigration induced failure due to too high a localized current density. The narrower lines are voltage probes for four-wire resistance measurement.

R0-R6 have one pair of voltage probes each, while R7 has three pairs voltage probes. As a result, a total of ten resistance signals can be measured on one board, including one from R0-R6 each and three from R7. Figure 5.3 shows a photo of an example R7 with a 2 mΩ resistor, and the three resistance values from the three pairs of probes.

The diameter of all the via drills is 0.4 mm. The solder pad size is 1.5 mm × 1.3 mm for all the joints, which is a typical pad size for manually soldered 0805 (2012 metric) chip resistor. The pad array near the edge of the PCB is designed to be compatible with a commercially available socket (Sullins, WMC18DRYN).

5.1.2 Materials and sample preparation

Figure 5.4 shows example photos of the sample preparation procedure from the dispensing process to a final reflowed sample that is ready for power cycling. The solder paste in this study is a commercially available SnBiAg paste (Chipquik, SMDLTLFP), and the main properties are listed in Table 5.1 [90].

The dispensing process is done with a Nordson Ultimus I Automatic Fluid Dispenser (see Fig. 3.1). For each solder pad, a point dispensing process is used, and the dispensing parameters are listed in Table 5.2.

The chip resistors are commercially available thick film resistors (Panasonic, ERJ-P06D2200V). The resistance value is 220 Ω, and the power rating is 0.5 W. The chip resistors are manually placed after dispensing, and the solder joints are reflowed in the Omegalux oven at a nominal peak temperature of 175 °C for 10 min. The measured peak temperature near the sample during reflow is 145 °C.

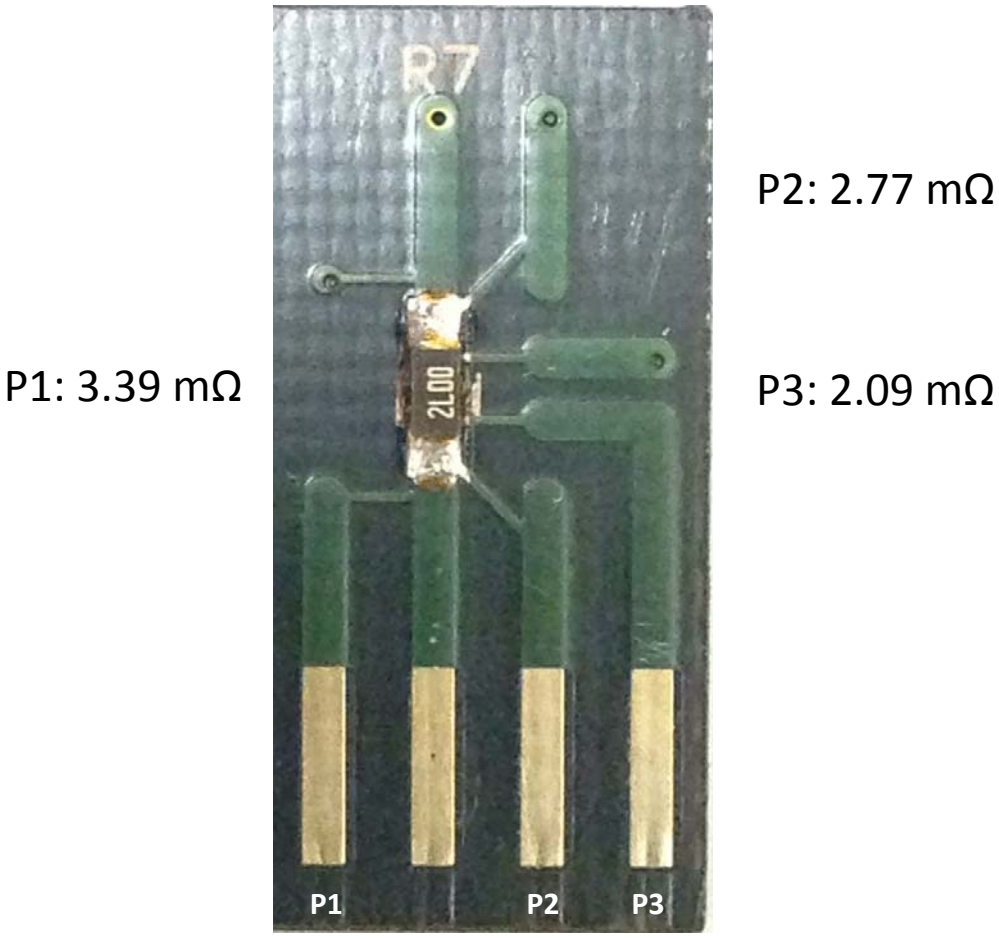

Figure 5.3. A photo of an example R7 with a 2 mΩ resistor, and the resistance readings from the three pairs of probes (P1, P2, and P3), respectively.

5.1.3 Power cycling

Figure 5.5 shows a diagram of the power cycling experimental over view. A list of components are shown in Table 5.3. An Agilent 34420A nanovoltmeter is used to measure the sample

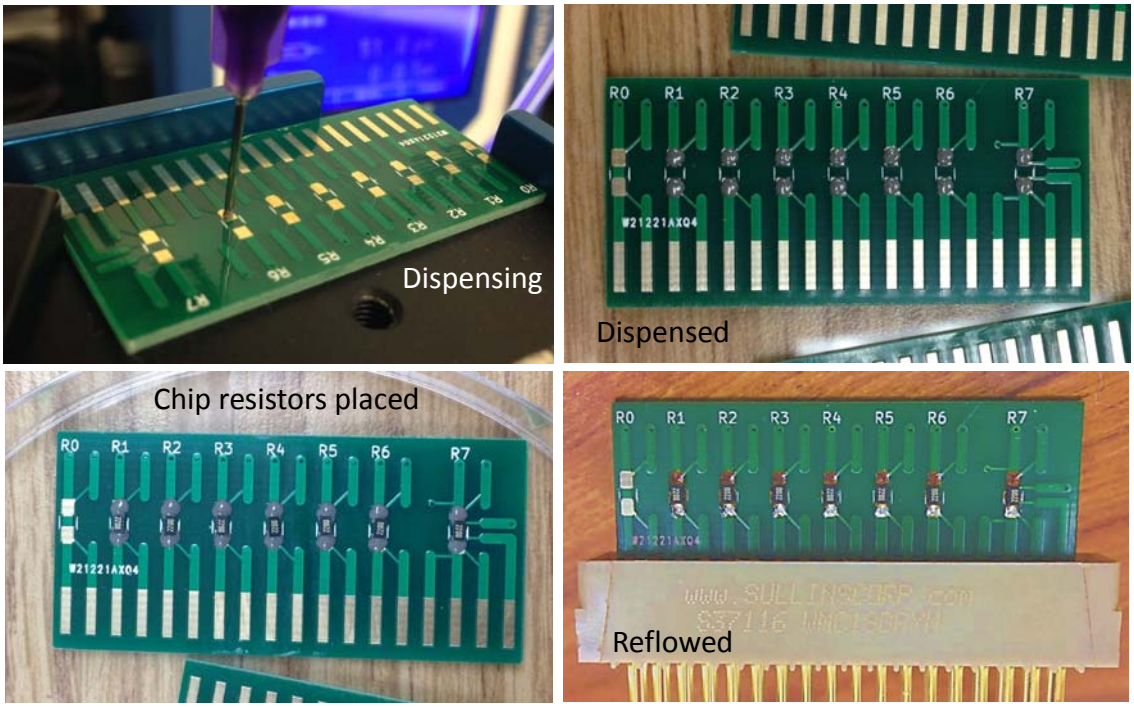

Figure 5.4. The sample preparation procedure from dispensing to reflowed samples.

Table 5.1. Solder paste properties in study I [90]

Alloy	Sn42/Bi57.6/Ag0.4
Ball size	25-45 µm
Metal load	87 wt.%
Melting point	138 °C
Flux classification	REL0

resistance values. A programmable DC power supply is used to apply power cycling stress to the samples. The DC power supply has a maximum output of 32V/5A/160W. A custom designed C# software is used to control the DC power supply remotely with PC through a USB connection. A Keithley 7700 20-channel differential multiplexer module is used in between the samples, nano-voltmeter, and the DC power supply to control the connection. The nanovoltmeter, and the multi-plexer are both connected with the PC through general purpose interface bus (GPIB). The multiplexer, the nanovoltmeter, and the DC power supply are all controlled with a custom designed Matlab program.

Table 5.2. Dispensing parameters

Tip inner diameter [mm]	Pressure [psi]	Dwelling time [s]
0.51	50	4

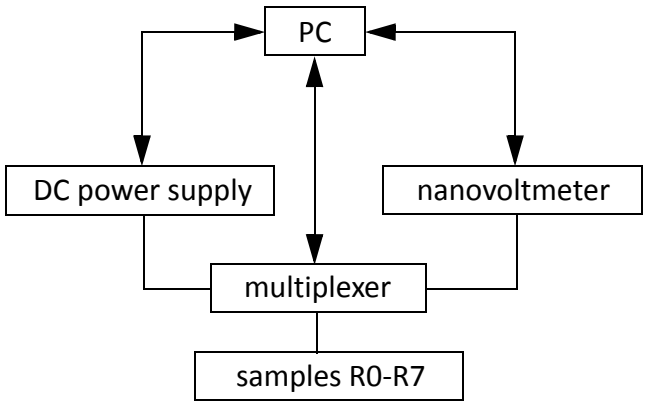

Figure 5.5. Power cycling experimental diagram overview. The communication pathways are shown with arrowed lines, and the electrical connections shown with solid lines.

Figure 5.6 shows the detailed electrical connection map between the samples, the nanovoltmeter, and the DC power supply, with sample R1 shown as an example. Essentially, the mapping is designed so as to achieve: 1. simultaneous parallel connection of samples R1-R7 to the DC power supply through the electrical current wires; 2. each of R0-R6 and the three groups of wires for R7 can independently be connected to the nanovoltmeter in a four wire configuration.

Figure 5.7 shows the flow diagram of an example power cycling experiment. In the configuration stage, the nanovoltmeter is configured to work in four wire resistance mode, with a number of power line cycles (NPLC) of 10. Offset compensation is turned on so as to rule out any voltage drop on the lead introduced by noise source such as thermal electric effect. The voltage output of the DC power supply is set as 11 V, so as to produce 0.55W power on the resistor, which

Table 5.3. List of components in the power cycling setup in Study I

	Component	Description
1	PC	Laptop: Win7 with Matlab
2	Matlab code	RmonitoringPcycling_v20170802.m; Available online at [91]
3	PCB	Custom designed, made by PCBway Inc., see Fig. 5.2
4	Chip resistor	Panasonic, ERJ-P06D2200V (Thick film, 220 Ω, 0.5 W, 0805)
5	Socket	Sullins, WMC18DRYN
6	Power supply	Vantek 32V/5A/160W Programmable DC Power Supply
7	Nanovoltmeter	Agilent 34420A
8	Multiplexer	Keithley 7700
9	Pt1000	Temperature sensor
10	Cables	GPIB-USB adapter, and regular flat ribbon cables
11	Cable connectors	37-pin D-sub connectors

is 10 % higher than the power rating of the chip resistor. The current limit is set to be 1 A, which is high enough for the power supply to work in a constant voltage mode through out the test. Assuming all seven samples are 220 Ω, the total current flow from the power supply is 0.35 A when 11 V is applied. The power on/off times are chosen as 2 min/4 min, respectively for the temperature to stabilize at the end of power on/off, respectively. The file name of the Matlab code is RmonitoringPcycling_v20170802.m. It is available for download from matlab central [91].

For resistance measurement, the samples are connected to the nanovolt meter one by one until all the ten (one from R0-R6 each, and three from R7) signals are recorded. For power cycling, The current lines of R1-R7 are simultaneously connected to the DC power supply, and

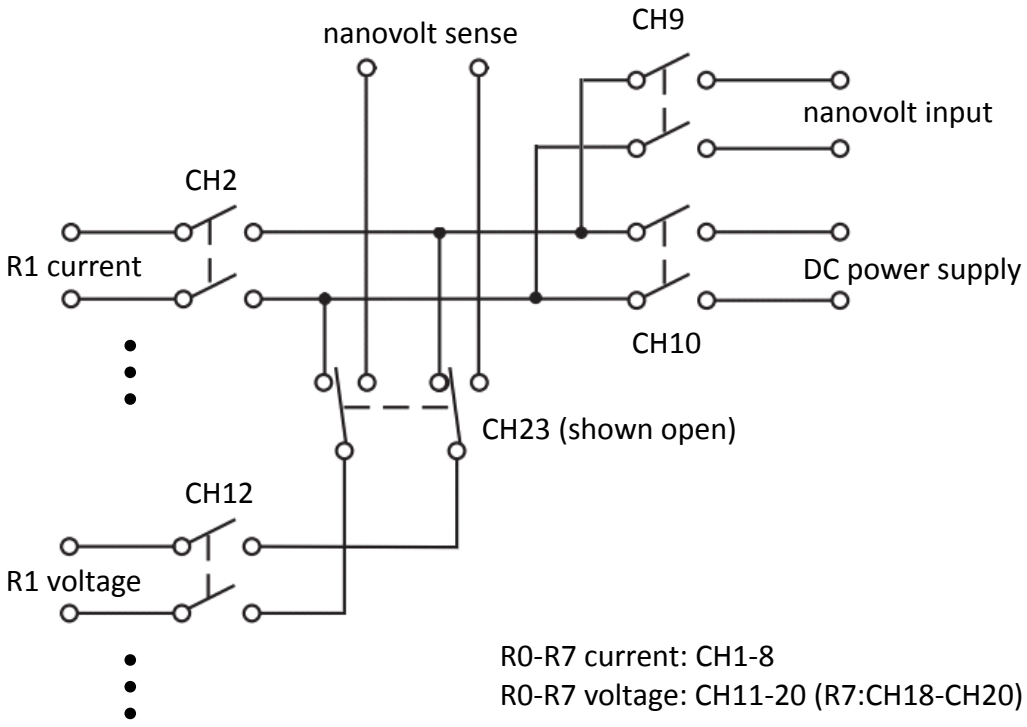

Figure 5.6. Electrical connection map with a multiplexer in power cycling test in study I, with only R1 shown as an example.

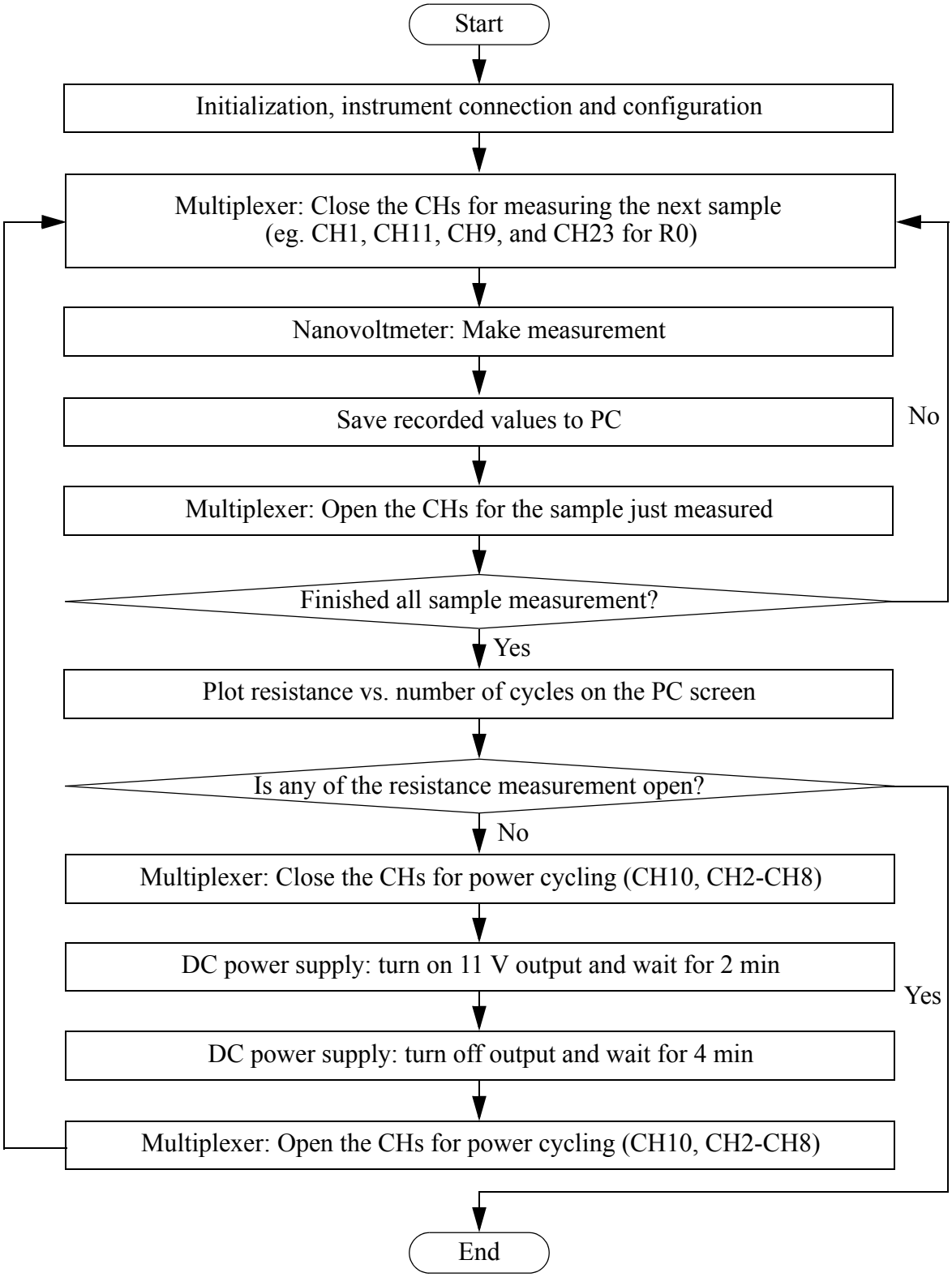

Figure 5.7. Matlab program flow chart of an example power cycling experiment in study I. (File name: RmonitoringPcyclingD1_v20170802.m; Available online at [91] and [55])

one cycle of stress is applied to the samples by turning DC power supply on and off automatically. The sample resistance values are measured in between each power cycle.

5.1.4 Results and discussion

Figure 5.8 shows an over view of the resistance signals for samples R1-R7. The power cycling test is stopped when one of the resistance values is open. As a result, a total of 608 cycles are applied to R1-R7 until R1 is open after the 608th cycle. The resistance values of samples R2-R7 remain around 220 Ω, the nominal resistance of the resistors. The resistance value of R1 rises to be higher than R2-R7 at 569th cycle, and keeps rising to be >221 Ω in six more cycles. The

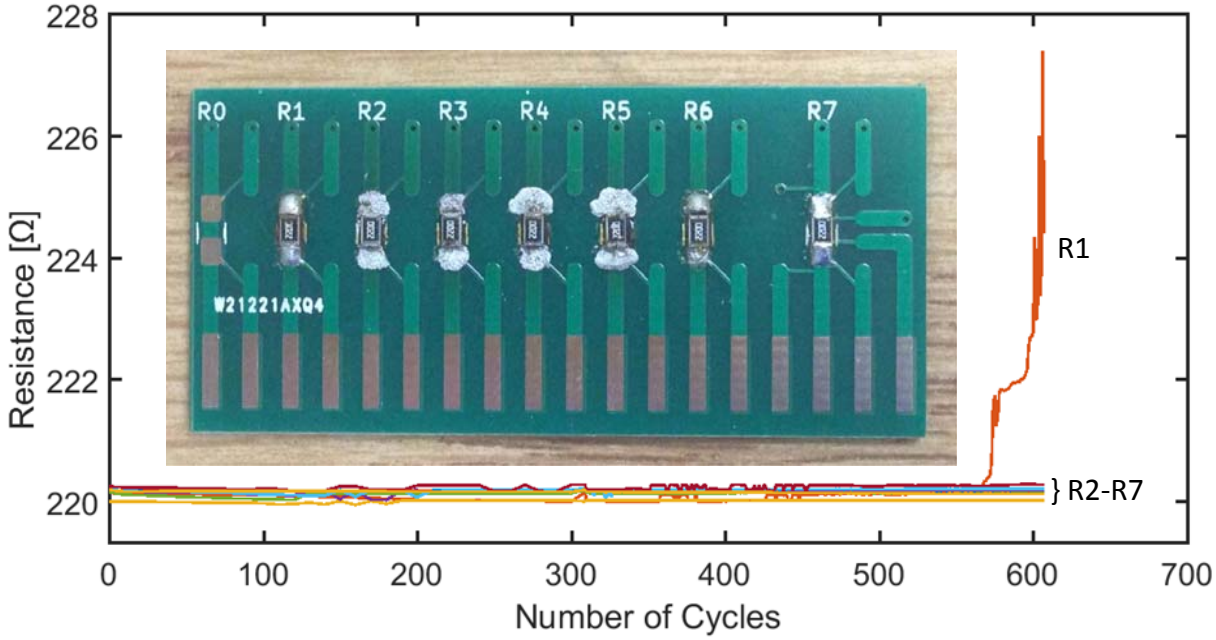

Figure 5.8. Resistance vs. number of cycles. The inset photo is taken after 608 cycles.

maximum recorded value of R1 before open is 227.4 Ω at 607th cycle. It takes 33 cycles for the resistance value to increase from 221 Ω to open.

From the inset of Figure 5.8, different solder joint appearances are observed for the seven samples, indicating different failure mechanisms. The outer samples (R1, R6, and R7) shown smooth solder joints. For the samples in the center (R2-R4), despite the low resistance values (<221 Ω), the solder joints appear grainy, indicating severe degradation. The degradation of R2-R4 solder joints is possibly mainly thermal degradation, and possibly involves oxidation, or inter-metallic compounds (IMCs) formation. Possible binary IMCs include Ag_3Sn, Cu_6Sn_5, and Cu_3Sn.

The different failure mechanisms of the different samples are possibly because of the peak temperature difference between the samples during power cycling. To verify the temperature difference, the sample temperatures are measured during the experiment. Figures 5.9a and b show a setup illustration for the temperature measurement, and the result peak temperature vs. RTD number, respectively. Seven Pt1000 RTDs are used, one for each resistor. The RTD numbers correspond the resistance numbers. The RTDs are attached to the chip resistors with double sided Kapton tapes. Figure 5.9c shows an example temperature vs. time segment. In each power cycle, the temperature of one sample is monitored. The seven sample temperatures are monitored in a loop.

From Fig. 5.9b, the temperature difference is verified, and the difference can be as large as about 40 °C (eg. between R7 and R3). The temperature difference is caused by different heat dissipation efficiency at different locations on the PCB. The closer to the edge of the PCB, the heat dissipates faster, and therefore the peak temperature is lower. Such temperature difference is avoided in an updated PCB design used in another power cycling study, and the details can be

found in Section 5.2. Due to the temperature differences among the joints, the PCB design in Study I is not intended for actual use in future power cycling or current stressing studies.

In order to understand the failure mechanism of R1, a cross section is made and the scanning electronics microscopic (SEM) images are shown in Figs. 5.10a-c. At the solder to resistor

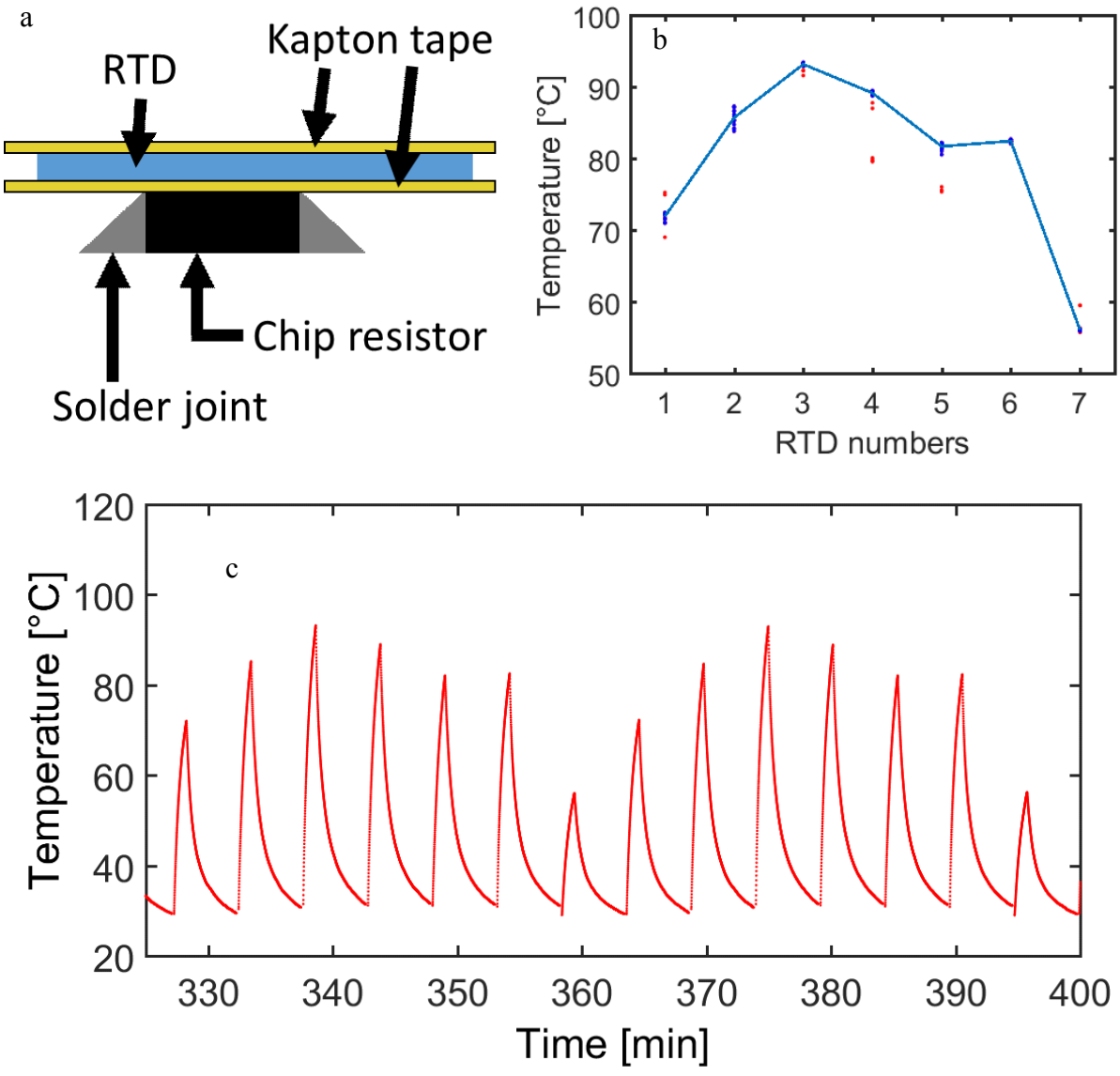

Figure 5.9. (a) A side view illustration for the samples during temperature measurement, (b) the peak temperature vs. resistance temperature detectors (RTD) number, and (c) an example temperature vs. time segment including alternating temperature monitoring of all seven samples.

joint interfaces, cracks are observed on both sides. The crack observed on the right joint interface is along the entire interface, leading to a complete open between the solder and the resistor on this cross sectional plane. The crack on the left joint interface is along the entire vertical interface, while the horizontal interface at the bottom shows a complete connection. The cracks observed in Figs. 5.10a-c explains the electrical open signal of R1.

This study shows that power cycling can lead to two types of failure modes for the solder joints from alloy Sn42Bi57.6Ag0.4. A possible explanation is when the peak temperature is too high (>85 °C), the joint failure is essentially caused by thermal degradation such as oxidation and IMC growth, and when the peak temperature is moderate (around 70 °C), the joint failure is essentially caused by thermal-mechanical degradation. The CTE mismatch between the chip resistor and the PCB may cause cyclic thermal stress in the solder joints during power cycling.

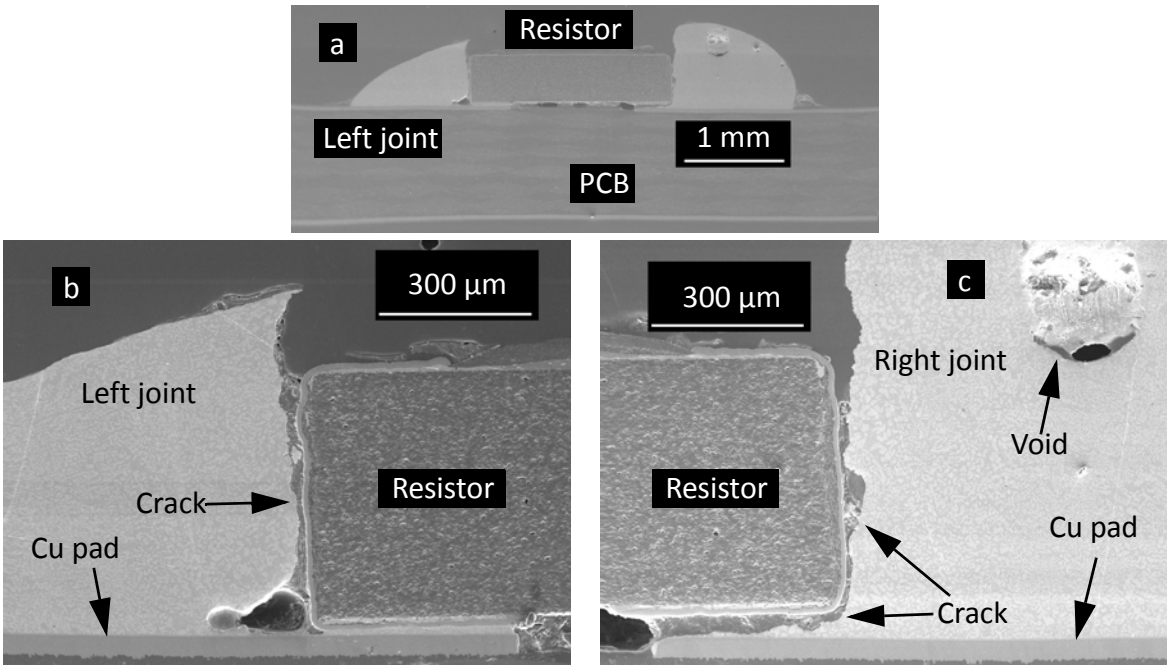

Figure 5.10. The scanning electron microscopic (SEM) images of (a) overview, (b) left joint interface, and (c) right joint interface of the cross section of R1.

The cyclic stress can cause crack formation and propagation along the interface at low temperature, which eventually lead to an open joint. When the peak temperature is too high, the stress may cause plastic deformation instead of cracks, and thus thermal-mechanical degradation is absent.

Based on the explanation above, in the case of thermal degradation, the electrical resistance of the solder joints remains low. In the case of thermal-mechanical degradation, the solder joint resistance is low in the beginning, and starts rising at some extent of degradation. If the power cycling continues, the solder joints eventually become electrically open.

5.2 Study II

5.2.1 PCB design

Figures 5.11a and b show top and side views of the custom made test vehicle. The assembly has two PCB components, namely mother board and daughter board, respectively. The mother board is made in University of Waterloo, and the daughter boards are made in PCBway in China. In addition, the assembly also includes 4-pin headers, USB-A female connectors, ribbon cables, d-sub connectors, solder joints, and mechanical supporting components. Eight chip resistors can be power cycles simultaneously with one assembly. The locations of the eight chip resistors are designed to be equivalent so as to avoid temperature difference between samples.

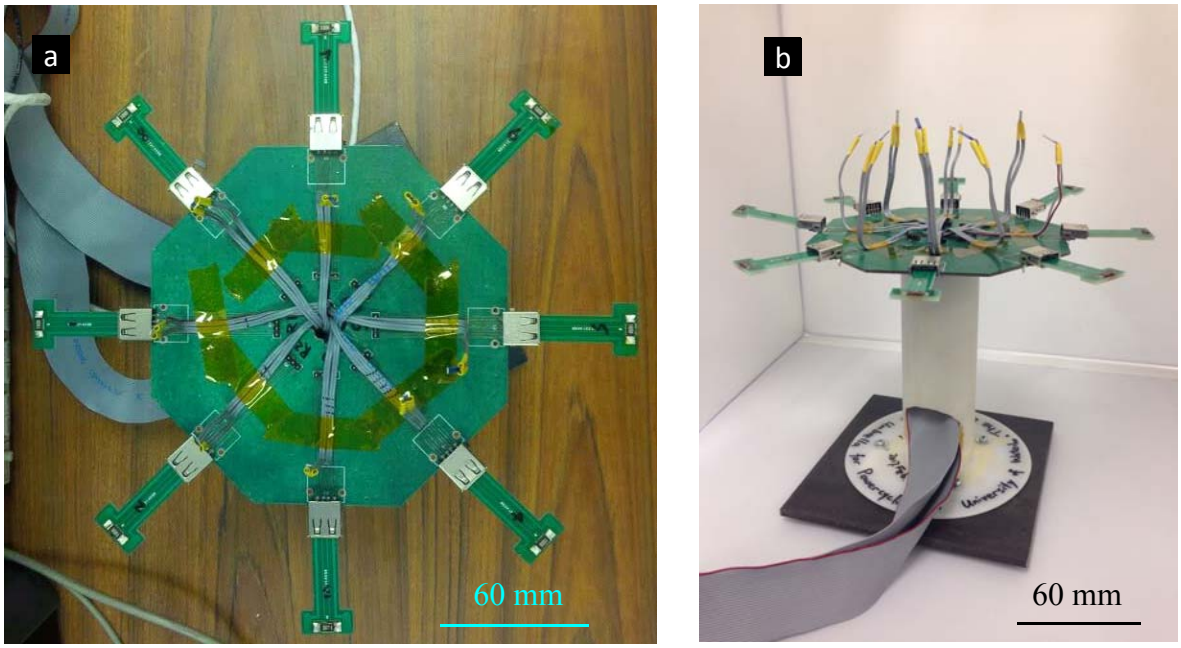

Figure 5.11. (a) Top and (b) side views of the custom made power cycling test vehicle for study II.

Figure 5.12a and b show the details of the daughter and mother boards design, respectively. The daughter board has four terminals for four-wire resistance measurement. The two outer terminals are designed to carry current, and the two inner terminals are voltage probes. The four terminals are positioned to be the same as a standard USB-A connector. USB-A connectors are commercially available four-terminal connectors, and sample change can be easily done with plugging/unplugging actions. The current lines near the resistor have the same width as the solder pads in order to distribute current uniformly in the solder joints. The ends of the voltage probes are on the corner of the solder pads. The resistors are standard 2512 (6332 metric) surface mount chip resistors, which is the largest common size in its family. The mother board is designed in the shape of a regular octagon with side length of 60 mm. The mother board has a USB-A female connector land in the middle of each edge, which is each connected to a four-header-pin connector land in the center through the on board wire lines. Figure 5.13 shows the top view of an example daughter board.

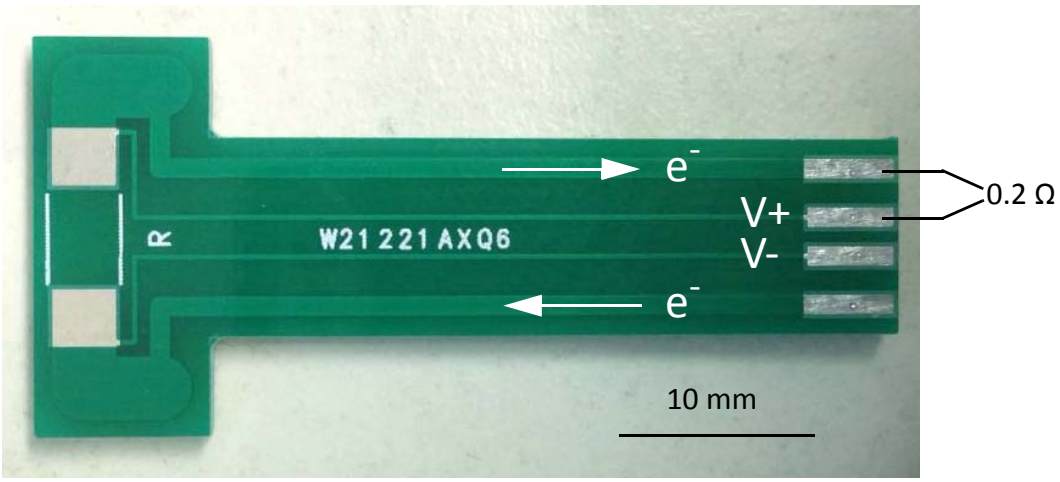

Figure 5.13. Top view optical image of an example daughter board. The line thickness is ~15.3 µm and the hot air solder leveling (HASL) finish is ~2.3 µm. The board material is FR4.

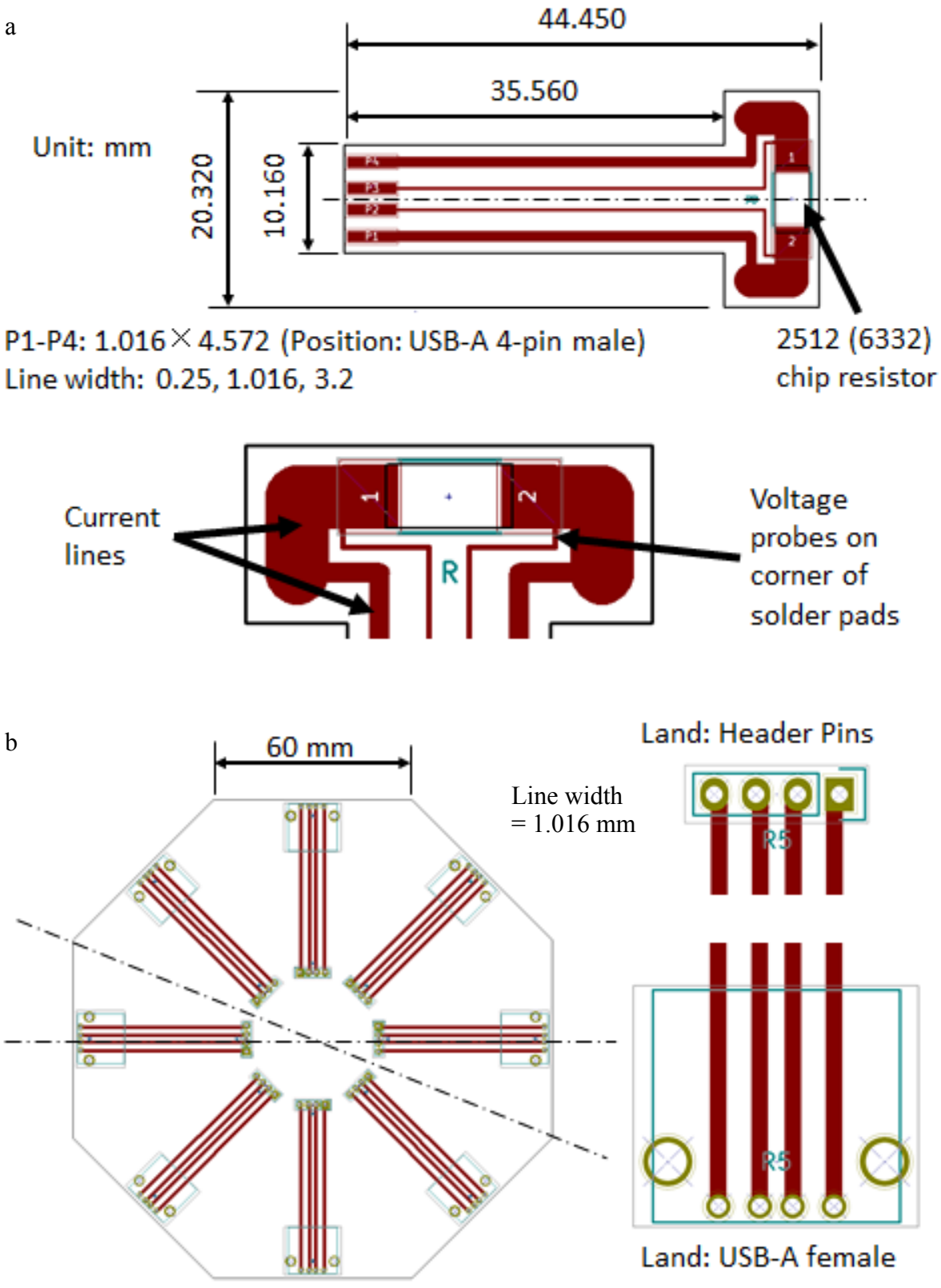

Figure 5.12. PCB design for study II: (a) daughter board, (b) mother board.

5.2.2 Materials and power cycling

Four solder pastes are studied and the information is listed in Table 5.4. All solders are provided by Celestica Inc. All the flux are no-clean flux. Specifically, SAC305 is the most widely used standard lead free solder and its leaded counterpart is Sn37Pb. For comparison purpose, SnAgCu ternary system has one eutectic point and the alloy is Sn95.6Ag3.5Cu0.9. SAC107Bi70, SnBi_NE, and Violet are example bismuth-containing solders. SAC107Bi70, and Violet are SnAgCuBi solders, with small amounts of Bi (<10 wt.%). SnBi_NE is near to a SnBi eutectic alloy (Bi58Sn42) with addition of a small amount of Ag.

All solder pastes come in jars. The solder pastes in jars are transferred to 5cc syringes before usage. The solders are stored in a freezer in -40 °C. For sample preparation, the solder dispensing and resistor placement are both done manually on the daughter boards shown in Section 5.2.1. The reflow for each sample is done with a hot air gun. Afterwards, the daughter boards with the solder samples are inserted into the mother board. For each power cycling run, eight resistors are tested simultaneously, with either the same or different solder materials.

Table 5.4. Solder pastes information

Name	element content in the alloy [wt. %]				Metal load [wt. %]	Flux	Manufacturing
	Sn	Ag	Cu	Bi			
SAC305	96.5	3.0	0.5	0	88.25	Indium 8.9HF1	2015-Apr.-24
SAC107Bi70	91.3	1.0	0.7	7.0	88.5	Indium 8.9	2014-May-06
SnBi_NE	42	0.4	0	57.6	90	Indium 5.7LT	2016-Jul.-12
Violet	91.25	2.25	0.5	6.0	88.25	Indium 8.9HF	2016-Mar.-03

A list of components for the experimental setup is shown in Table 5.5. The wiring and power cycling procedure are based on Section 5.1.3. The same multiplexer, DC power supply, and nanovoltmeter as in Section 5.1.3 are used. The differences are: 1. Instead of the wiring scheme shown in Fig. 5.6, the current lines of samples R1-R8 are connected to CH1-CH8, and the voltage lines are connected to CH11-CH18, respectively; 2. The holding times for power on/off are 5 min/ 10 min instead of 2 min/4 min shown in Fig. 5.7; 3. The chip resistors are 100 Ω each; 4. The constant stressing voltage is 14 V, to apply 2.0 W/0 W power cycles for each chip resistor. The power on/off time are chosen such that the temperature reaches a stable state at the end of power on, or off, respectively.

Figure 5.14a shows an illustration for the clamping scheme, and Fig. 5.14b shows a photo of one example sample during the temperature measurement. A Pt1000 is clamped to the top of each chip resistor with an alligator clamp. Two pieces of PTFE are attached to the tip of the clamp with wraps of Kapton tapes to limit the heat sink effect of the clamp. Figure 5.14c shows a typical

Table 5.5. List of components in the power cycling setup in Study II

Component*	Description
PCB-mother	Custom designed, made in University of Waterloo, see Fig. 5.12b
PCB-daughter	Custom designed, made by PCBway Inc., see Fig. 5.12a
PCB-other	Four-pin headers, USB-A female connectors, solder joints, and mechanical supporting components.
Chip resistor	Bourns Inc., CRM2512-FX-1000ELF (Thick film, 100 Ω, 2 W, 2512)

In addition to #1, 2, 6-11 in Table 5.3

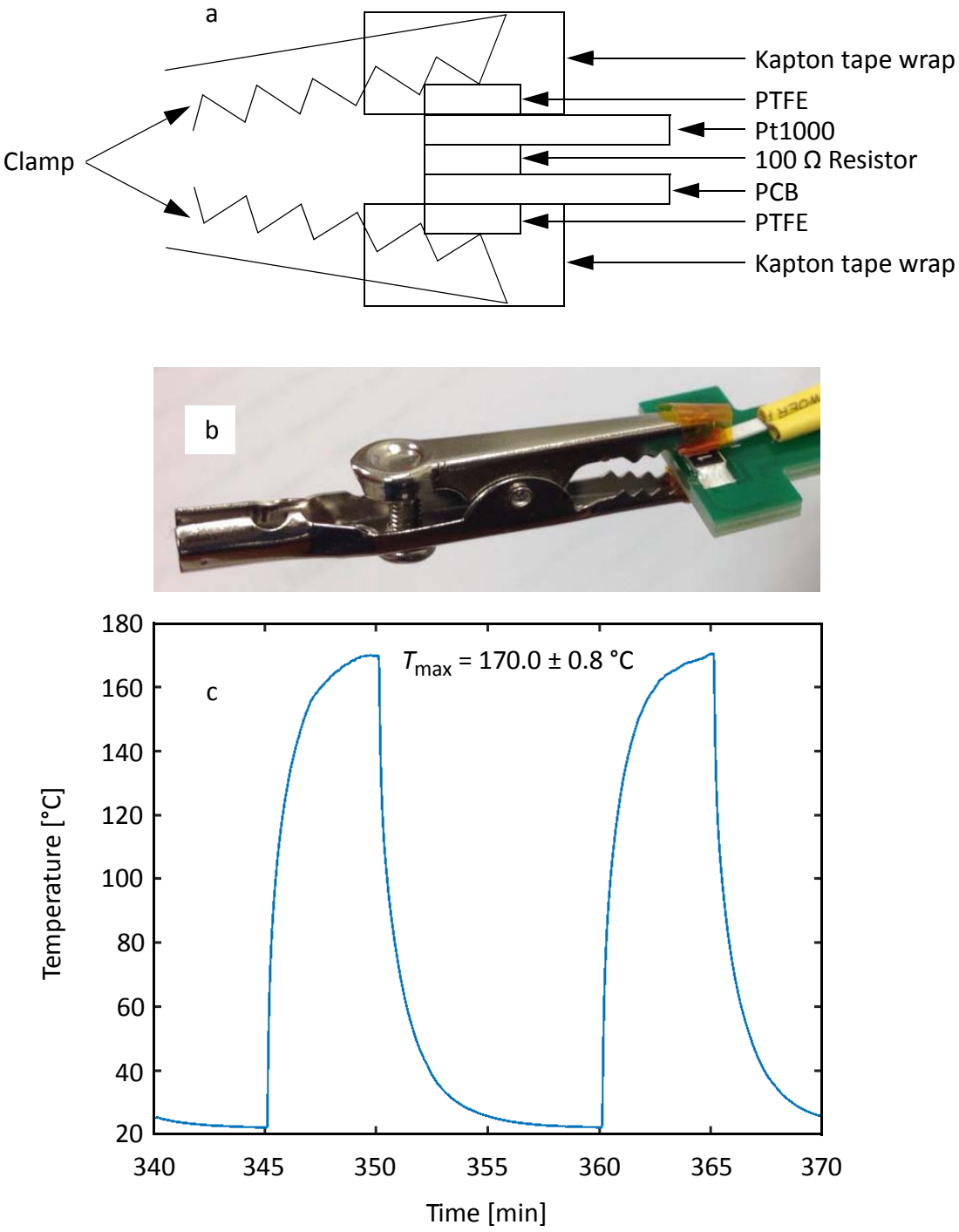

Figure 5.14. (a) The scheme for temperature sensor clamping to the sample, (b) a photo of the sample during temperature measurement, and (c) A typical temperature vs. time segment of the sample in the 2W5min/0W10min power cycling stressing condition. The inset shows the clamping method for the Pt1000.

temperature vs. time segment in about two power cycles. The peak temperature T_{max} holds at 170.0±0.8°C for about 1.4 min. The time below 24 °C during each cycle is about 4.5 min.

5.2.3 Resistance signals

Figures 5.15a-c show a typical resistance signal vs. number of cycles obtained from SAC305, zoomed in at different resistance ranges, and the insets of Fig. 5.15a are top view optical images of example failed solder joints.

We observe three stages from the resistance signals. In the first stage, the resistance change is mainly gradual increment, typically less than 0.1 Ω. In the second stage, the resistance signal experiences a fast rise, typically > 0.4 Ω in less than 10 cycles. In the third stage, the resistance signal starts fluctuating, and keeps rising until >10 kΩ. The signal in the third stage can occasionally drop to a temporary low resistance value (<1 kΩ) for some samples.

A possible explanation for the occasional temporary low resistance is self healing effect, the mechanism of which is possibly the same as in the crack healing effect in Figs. 2.14d-f. When the resistance rises, the constant voltage produces less power and thus the stressing condition is milder. The joints may experience some healing effect when the resistance values are high (>10 kΩ). The healing effect may result in a temporary low resistance values (<1 kΩ) in the third stage. The resistance curves from SAC107Bi70 and Violet typically experience the same three stages as SAC305.

Figure 5.16 shows a typical resistance vs. number of cycles curve of SnBi_NE, up to 1000 cycles, and the insets are top view optical images of example solder joints after 1000 cycles of stressing. The resistance change is small (<200 mΩ) compared to SAC305, SAC107Bi70, and

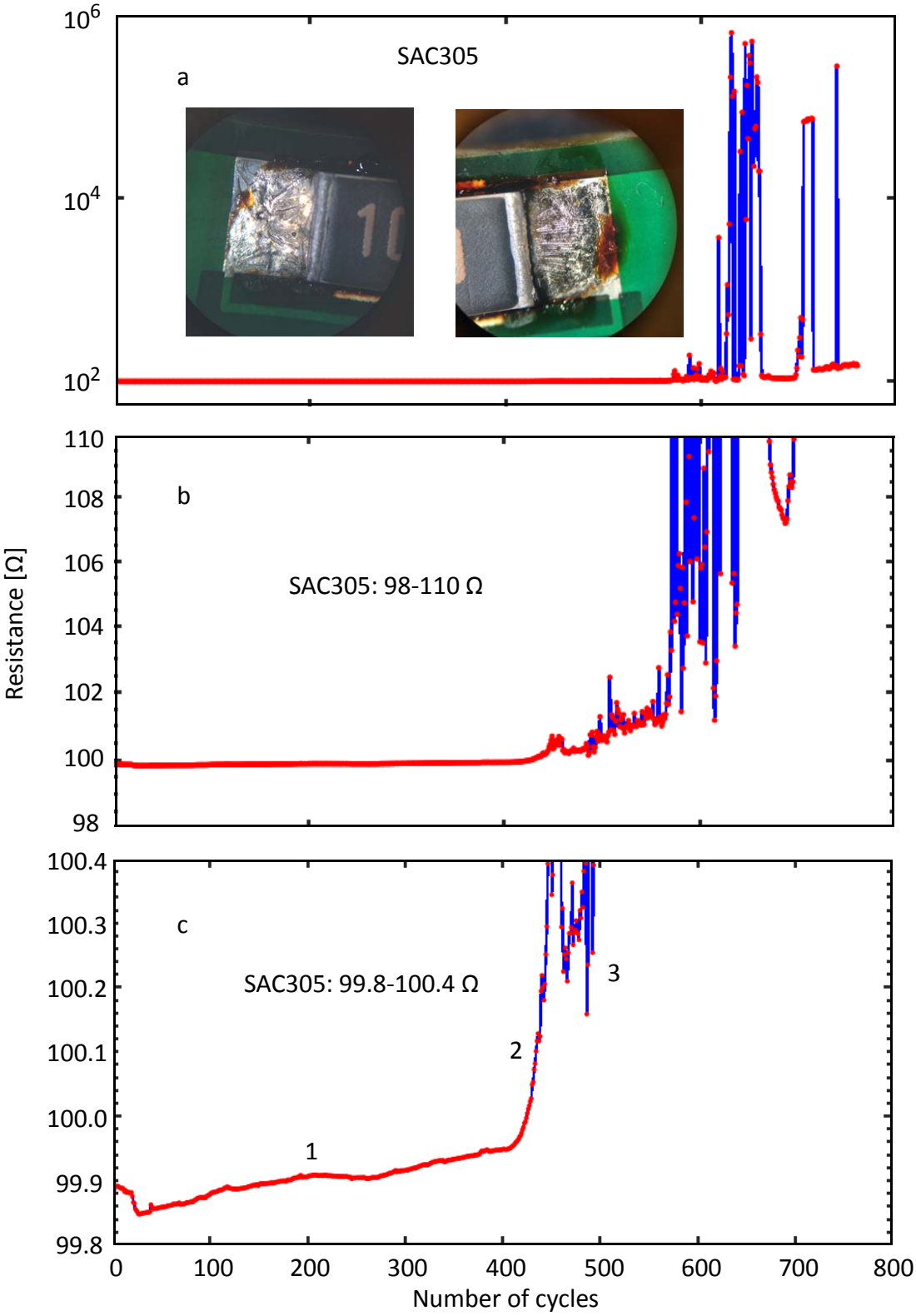

Figure 5.15. A typical curve of resistance signal vs. number of cycles obtained from SAC305: (a) overview, insets being top view optical images of example failed solder joints, (b) zoomed at 98-110 Ω, and (c) zoomed at 99.8-100.4 Ω.

Violet, while the appearance of the solder joints shows more severe degradation than SAC305, SAC107Bi70, and Violet, as seen in the insets of Fig. 5.16a and Fig. 5.15a. Such severe appearance change of SnBi_NE is considered joint failure in this thesis.

The failure mechanism of SnBi_NE in this study is possibly the same as R2-R5 in Fig. 5.8. The peak temperature is higher than the highest temperature shown in Fig. 5.9c, and thermal degradation is faster than thermal-mechanical degradation. The degradation of SnBi_NE has less effect on the resistance signal than the degradation of SAC305, SAC107Bi70, and Violet.

Figures 5.17a, and b show the number of cycles to 1 Ω resistance change for SAC305, SAC107Bi70, and Violet, and the number of cycles to 0.01-1 Ω resistance change for SAC305, respectively. The red dots in Fig. 5.17 are individual data points, and there are 18 samples for each boxplot. Figures 5.18a, and b show weibull cumulative probabilities corresponding to Figs. 5.17a,

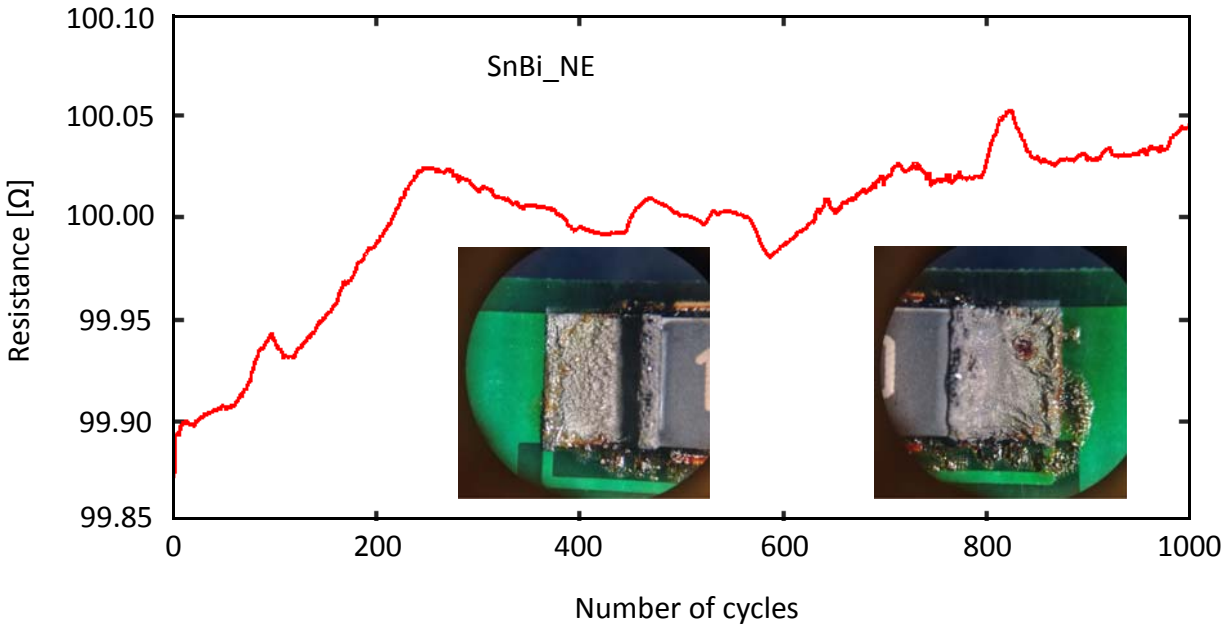

Figure 5.16. A typical curve of resistance signal vs. number of 2W5min/0W10min cycles obtained from SnBi_NE.

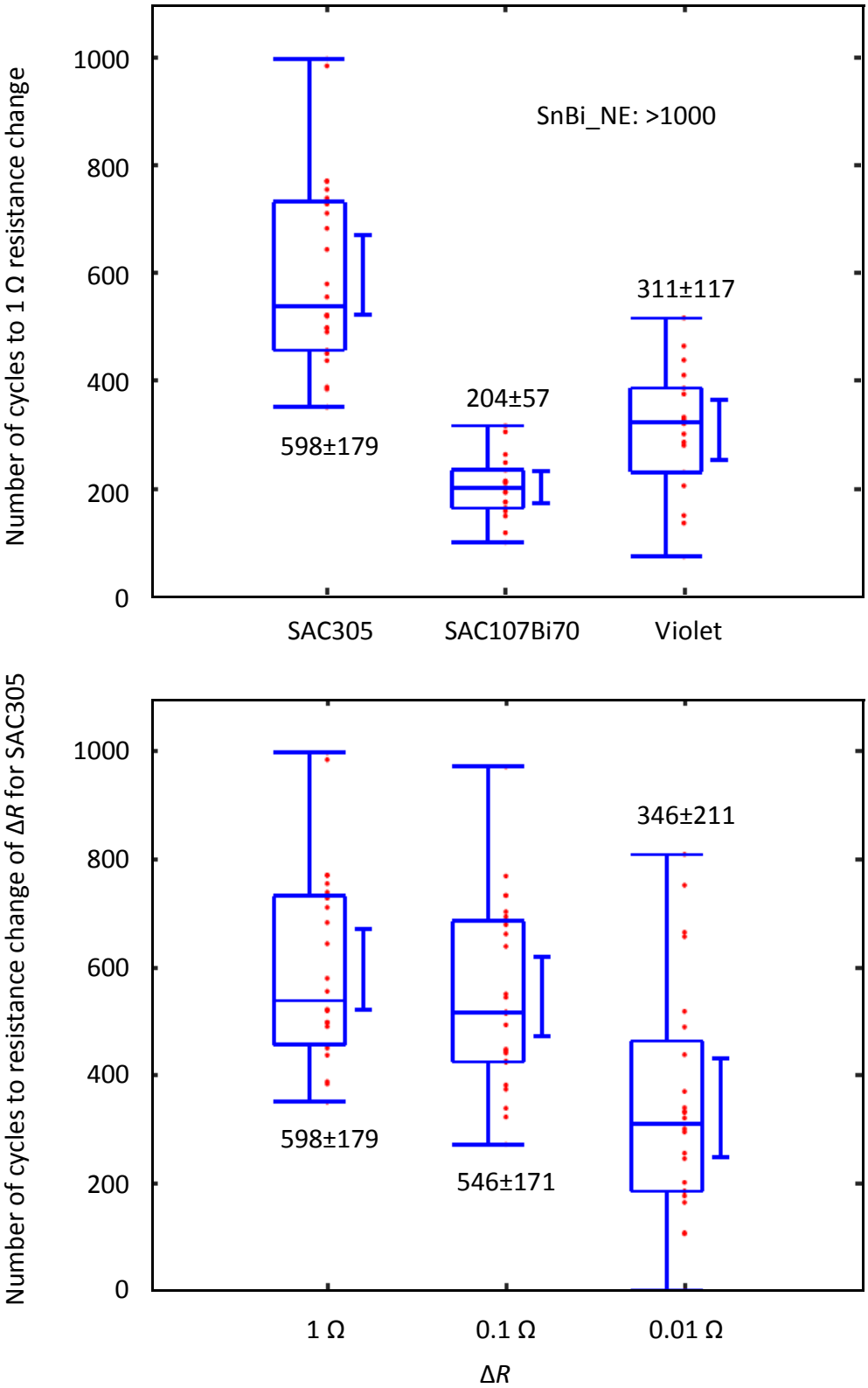

Figure 5.17. Number of cycles to (a) 1 Ω resistance change of SAC305, SAC107Bi70, and Violet, and (b) 0.01-1 Ω resistance change for SAC305. The numbers are average ± standard deviation number of cycles. The bars by the boxplots are Weibull 95 % confidence intervals of the average.

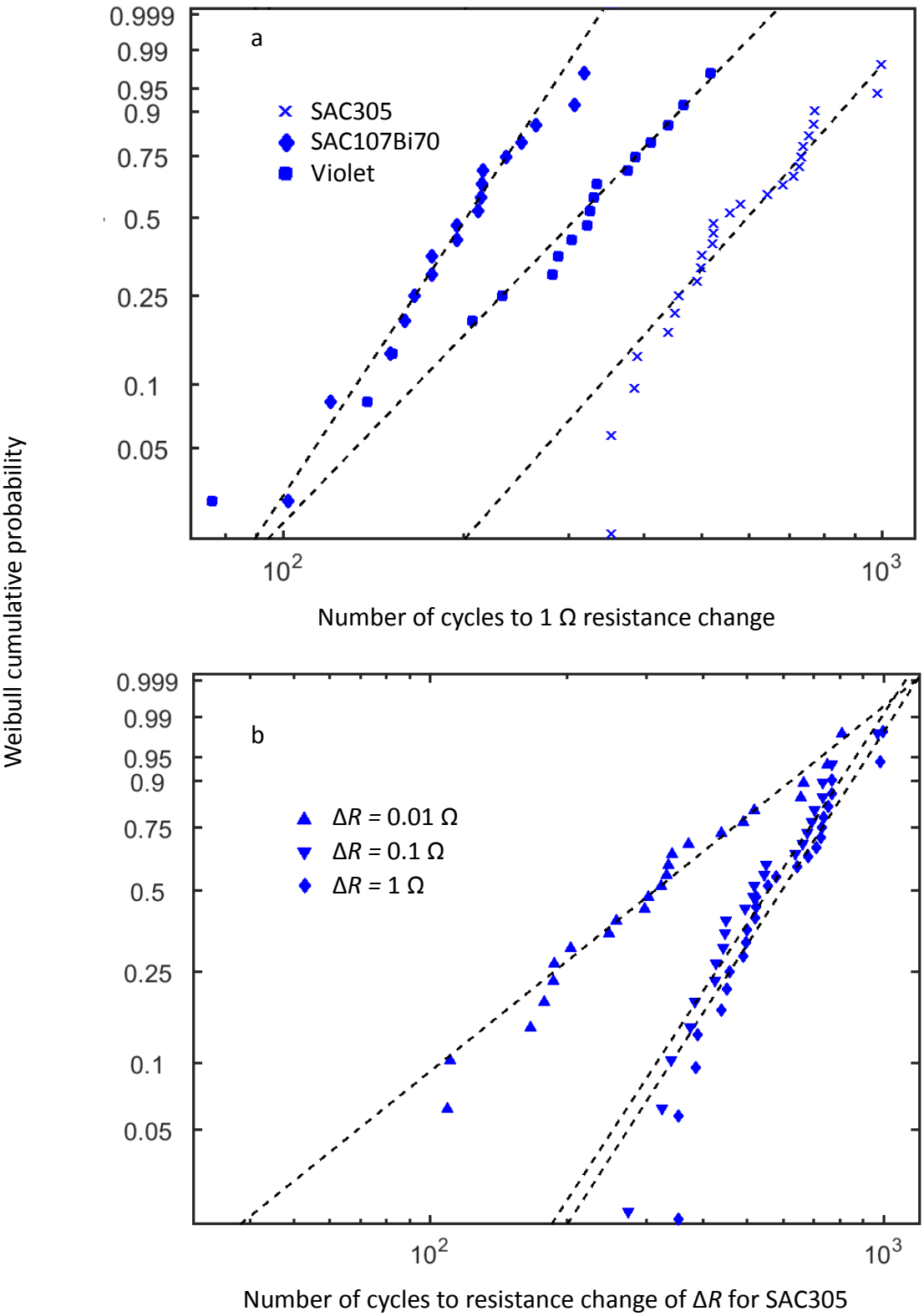

Figure 5.18. Weibull cumulative probabilities of (a) 1 Ω resistance change for SAC305, SAC107Bi70, and Violet, and (b) different numbers of resistance change for SAC305, with respect to the number of cycles.

and b, respectively. SnBi_NE is ruled out from Fig. 5.17a because of its low resistance change. Comparing the three solders, SAC305 has the longest life and fails at 598 ± 179 cycles, SAC107Bi70 has the shortest life and fails at 204 ± 57 cycles. Generally, the bismuth containing solders survive shorter than SAC305 solder in this power cycling test.

5.2.4 Cross sections

Figures 5.19a-f show the anode side cross section overviews of as reflowed, and failed solder joints for SAC305, SAC107Bi70, and Violet, and Figs. 5.20a-c show the cathode side of the same samples in Figs. 5.19b, d, and f, respectively. For all the three solders, cracks can be observed near the interface between the chip resistors and solder joint on both the anode and the cathode sides. SAC107Bi70, and Violet show more severe thermal degradation and wider cracks than SAC305. In all cases, the PCB degradation is observed below the chip resistor, which may be reduced by using higher temperature rated PCBs to avoid failure mechanisms that are not seen in service. The cracks possibly result from the stress caused by CTE mismatch between the chip resistor and the PCB board.

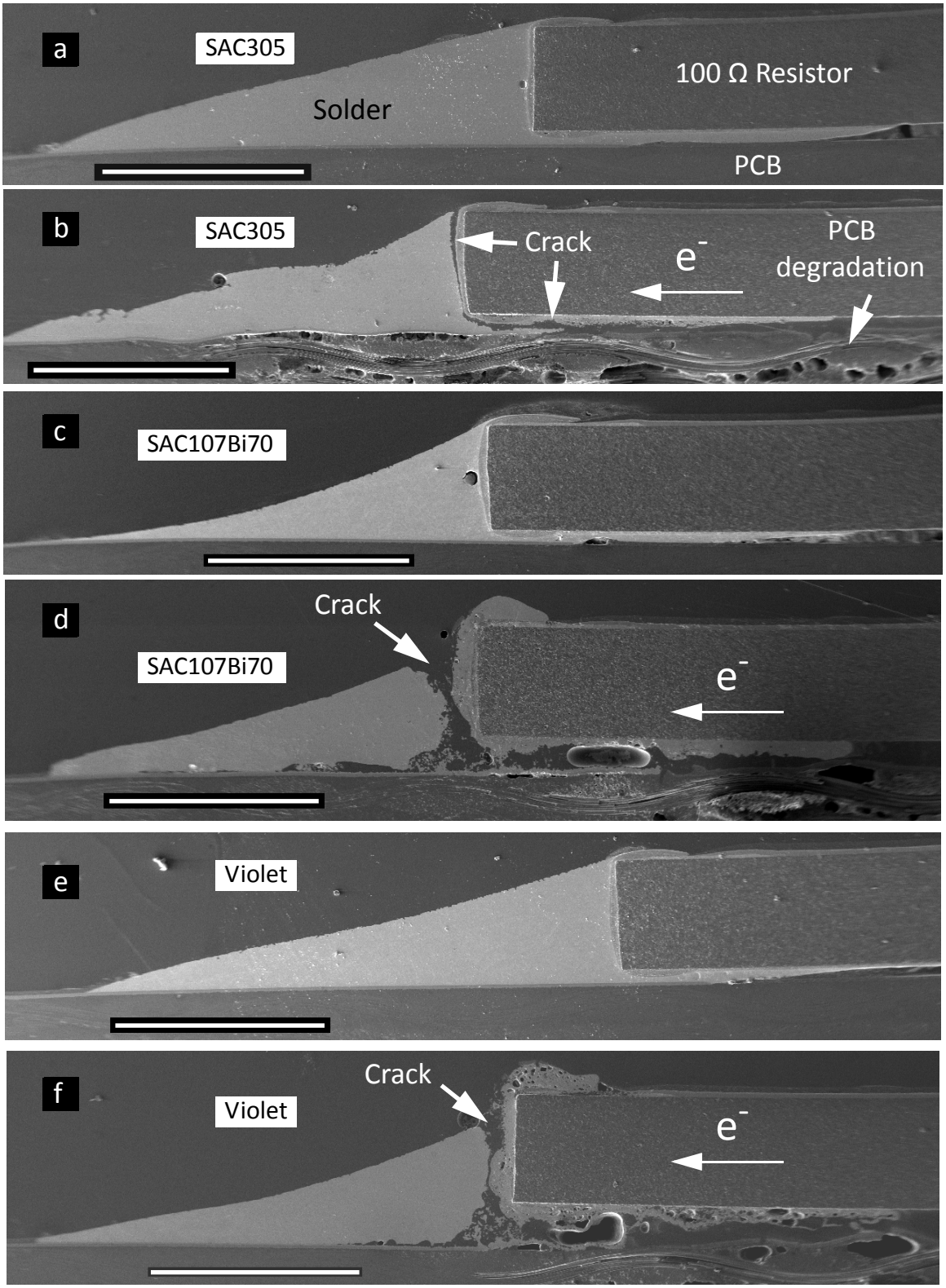

Figure 5.19. Anode side cross section overviews of (a, b) SAC305, (c, d) SAC107Bi70, and (e, f) Violet joints in (a, c, e) as reflowed condition, and (b, d, f) failed after power cycling. The scale bars are 1 mm.

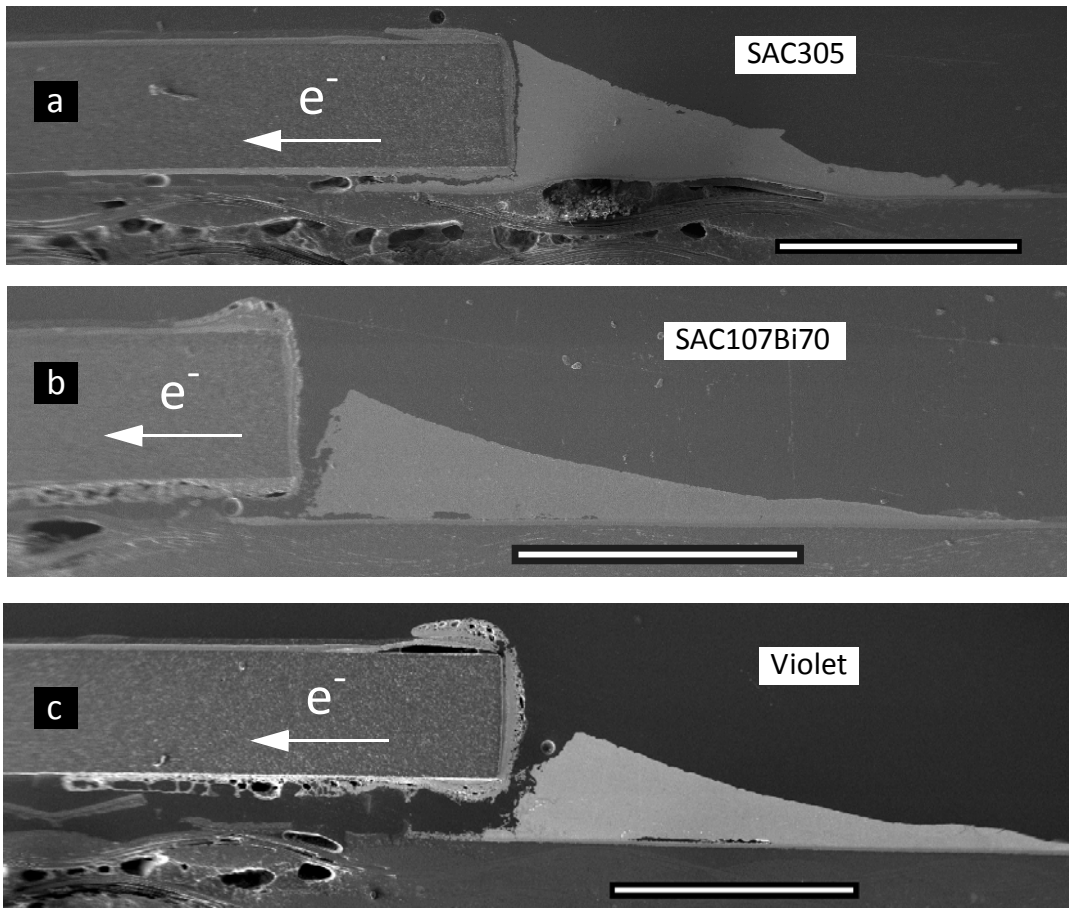

Figure 5.20. Cathode side cross section overviews of failed (a) SAC305, (b) SAC107Bi70, and (c) Violet joints after power cycling. The images are from the same samples as shown in Figs. 5.19b, d, and f, respectively. The scale bars are 1 mm.

5.3 Summary of Chapter 5

Two custom resistance monitoring test vehicles are shown with example results to study the behavior of solder joints under power cycling stressing conditions. Specifically in the first study with Sn42Bi57.6Ag0.4 solder, both thermal degradation, and thermal-mechanical degradation are observed, depending on the peak temperature being high, and low, respectively. In the second study with four solder types, under the same power cycling condition, Sn42Bi57.6Ag0.4 shows mainly thermal degradation, while SAC305, Sn91.3Ag1.0Cu0.7Bi7.0, and Sn91.25Ag2.25Cu0.5Bi6.0, show thermal-mechanical failure, as observed with cross sectioning study. In the case of thermal-mechanical failure, the SAC305 solder survives longer than the other two solders in terms of resistance signal.

For thermal degradation, the resistance change is insignificant (<1 Ω), while for thermal-mechanical degradation, the resistance signal rises and eventually becomes open. Resistance monitoring technology can help detect thermal-mechanical failure in solder joints, and can be used as a screening technology in the development of new solder materials.

Chapter 6 Conclusions

Two new accelerated reliability test methods with real time resistance monitoring for solder joints are developed, and are current stressing, and power cycling, respectively. The resistance signals is obtained in real time, and is used to control the termination of the stressing condition automatically for the first time. Additionally, resistance monitoring technology is successfully used in solder reflow for the first time, and the resistance curve in silver sintering process is obtained with highest level of completeness. The new methods directly lead to new discoveries such as flux segregation phenomenon in solder reflow, and nano link clusters formation in silver sintering process.

In the two example accelerated reliability tests, the failure conditions of standard lead free solder SAC305 are obtained. The other solder materials can be promptly tested and compared with SAC305 using the same test method. Specifically in power cycling, example solders containing Bi are studied, and they are found to fail faster than SAC305. The resistance monitoring setup is portable, and may also be integrated with other reliability test methods such as high temperature storage (HTS), thermal cycling, and vibration, for qualification of new solder materials.

Understanding of the solder reflow, and silver sintering processes is improved. Signature resistance curves are obtained for each process. Different stages such as resistance rise/drop at different rates, and/or some special events such as open are identified from the resistance curves. Example new findings include flux segregation in solder reflow, and nano link clusters formation in silver sintering. Flux segregation may or may not happen, depending on the quality of the flux, typically before solder melting. Whether flux segregation can affect the final solder joint quality is still unclear, which may require some additional reliability tests. The nano link clusters in silver

sintering process indicates a silver flakes breakdown event. While possible explanation is given for silver flakes breakdown, more careful work is needed to fully understand the new phenomenon, such as molecular dynamics simulation.

Understanding of the failure mechanism for SAC305 solder joints is improved. The failure in current stressing test is identified as the cathode joint open. A new finding is a sequence of intermittent crack healing events before the final open. The failure in power cycling test is identified as cracks formation near the solder joint interfaces.

This study includes joints reliability monitoring and joining process monitoring. However, this study does not include the effect of process parameters on quality / failure of the joints. For any new microjoining material, the effect of process parameters on the quality / failure of the joints is of interest. The microjoints performance needs to be optimized in the industry, and therefore a guideline for process selection is helpful for any new microjoining material. For future work involving new microjoining materials development, the methods described in this thesis can be used to study the effect of process parameters on quality / failure of the joints.

The resistance monitoring technology adopted in this thesis does not detect solder melting, solder solidification, or silver sintering paste densification. Possibly with further increased signal-to-noise ratio can these phenomena be detected with resistance signals. Furthermore, integration of multiple real time monitoring technologies such as resistance, TGA, DSC, and imaging, in one setup may be helpful for learning more about the microjoining processes and the microjoints reliability.

References

[1] Tummala RR, Rymaszewski EJ, Lee YC. Microelectronics packaging handbook.

[2] Lau JH. Flip chip technologies. McGraw-Hill Professional; 1996 Jun 1.

[3] TWI, Microjoining for Electronics, Reference C11-85, 1985

[4] Lau, John H. Flip chip technologies. Vol. 1. New York: McGraw-Hill, 1996.

[5] Mangin, C-H., and Stephen McClelland. "Surface Mount Technology." (1987).

[6] Yeh, Everett CC, W. J. Choi, K. N. Tu, Peter Elenius, and Haluk Balkan. "Current-crowding-induced electromigration failure in flip chip solder joints." Applied Physics Letters 80, no. 4 (2002): 580-582.

[7] Lee, T. Y., K. N. Tu, and D. R. Frear. "Electromigration of eutectic SnPb and SnAg 3.8 Cu 0.7 flip chip solder bumps and under-bump metallization." Journal of Applied Physics 90, no. 9 (2001): 4502-4508.

[8] Xu L, Pang JH, Tu KN. Effect of electromigration-induced back stress gradient on nanoindentation marker movement in SnAgCu solder joints. Applied physics letters. 2006 Nov 27;89(22):221909.

[9] Liu, C. Y., C. Chih, C. N. Liao, and K. N. Tu. "Microstructure-electromigration correlation in a thin stripe of eutectic SnPb solder stressed between Cu electrodes." Applied Physics Letters 75, no. 1 (1999): 58.

[10] Lee, T. Y., K. N. Tu, S. M. Kuo, and D. R. Frear. "Electromigration of eutectic SnPb solder interconnects for flip chip technology." Journal of Applied Physics 89, no. 6 (2001): 3189-3194.

[11] Lai, Yi-Shao, Kuo-Ming Chen, Chin-Li Kao, Chiu-Wen Lee, and Ying-Ta Chiu. "Electromigration of Sn–37Pb and Sn–3Ag–1.5 Cu/Sn–3Ag–0.5 Cu composite flip–chip solder bumps with Ti/Ni (V)/Cu under bump metallurgy." Microelectronics Reliability 47, no. 8 (2007): 1273-1279.

[12] Lai, Yi-Shao, Chiu-Wen Lee, and Chin-Li Kao. "Effect of test conditions on electromigration reliability of Sn–Ag–Cu flip-chip solder interconnects." Journal of Electronic Packaging 129, no. 1 (2007): 56-62.

[13] Chao, B. H. L., Zhang, X., Chae, S. H., & Ho, P. S. (2009). Recent advances on kinetic analysis of electromigration enhanced intermetallic growth and damage formation in Pb-free solder joints. Microelectronics Reliability, 49(3), 253-263.

[14] Chang, Y. W., S. W. Liang, and Chih Chen. "Study of void formation due to electromigration in flip-chip solder joints using Kelvin bump probes." Applied physics letters 89, no. 3 (2006): 032103.

[15] Lin, C. K., Yuan Wei Chang, and Chih Chen. "Experimental and simulation analysis of concave-down resistance curve during electromigration in solder joints." Journal of Applied Physics 115, no. 8 (2014): 083707.

[16] Lee NC. Reflow soldering processes and troubleshooting: SMT, BGA, CSP, and flip chip technologies. Newnes; 2002.

[17] Lee YC, Chen WT. Manufacturing Challenges in Electronic Packaging. London: Chapman & Hall; 1998.

[18] Klein Wassink RJ, van Gerven JA. Displacement of Components and Solder during Reflow Soldering. Soldering & Surface Mount Technology. 1989 Jan 1;1(1):5-10.

[19] Roos-Kozel BL. Parameters Affecting the Incidence of Pad Bridging in Surface Mounted Device Attachment. Microelectronics International. 1985 Feb 1;2(2):5-8.

[20] Berntson RB, Sbiroli DW, Anweiler JJ. Minimizing solder spatter impact. SMT SURF MOUNT TECHNOL MAG. 2000;14(4):5.

[21] Huang ML, Yang F, Zhao N, Zhang ZJ. In situ study on dissolution and growth mechanism of interfacial Cu6Sn5 in wetting reaction. Materials Letters. 2015 Jan 15;139:42-5.

[22] Huang ML, Zhang ZJ, Zhao N, Yang F. In situ study on reverse polarity effect in Cu/Sn–9Zn/Ni interconnect undergoing liquid–solid electromigration. Journal of Alloys and Compounds. 2015 Jan 15;619:667-75.

[23] Qu L, Zhao N, Ma H, Zhao H, Huang M. In situ study on the effect of thermomigration on intermetallic compounds growth in liquid-solid interfacial reaction. Journal of Applied Physics. 2014 May 28;115(20):204907.

[24] Srivalli C, Abdullah MZ, Khor CY. Numerical investigations on the effects of different cooling periods in reflow-soldering process. Heat and Mass Transfer. 2015 Feb:1-1.

[25] Bozack MJ, Suhling JC, Zhang Y, Cai Z, Lall P. Surfaces of mixed formulation solder alloys at melting. Journal of Vacuum Science & Technology A. 2011 Jul 1;29(4):041401.

[26] Bozack MJ, Suhling JC, Zhang Y, Cai Z, Lall P. Influence of Surface Segregation on Wetting of Sn-Ag-Cu (SAC) Series and Pb-Containing Solder Alloys. Journal of electronic materials. 2011 Oct 1;40(10):2093-104.

[27] Chung S, Kwak JB. Realistic warpage evaluation of printed board assembly during reflow process. Soldering & Surface Mount Technology. 2015 Sep 7;27(4):137-45.

[28] Tsai MY, Ting CW, Huang CY, Lai YS. Determination of residual strains of the EMC in PBGA during manufacturing and IR solder reflow processes. Microelectronics Reliability. 2011 Mar 31;51(3):642-8.

[29] Zhou MB, Ma X, Zhang XP. Premelting behavior and interfacial reaction of the Sn/Cu and Sn/Ag soldering systems during the reflow process. Journal of Materials Science: Materials in Electronics. 2012 Aug 1;23(8):1543-51.

[30] Sharma A, Xu DE, Chow J, Mayer M, Sohn HR, Jung JP. Electromigration of composite Sn-Ag-Cu solder bumps. Electronic Materials Letters. 2015 Nov 1;11(6):1072-7.

[31] Xu DE, Chow J, Mayer M, Jung JP, Yoon JH. Sn-Ag-Cu to Cu joint current aging test and evolution of resistance and microstructure. Electronic Materials Letters. 2015 Nov 1;11(6):1078-84.

[32] Wang T, Chen X, Lu GQ, Lei GY. Low-temperature sintering with nano-silver paste in die-attached interconnection. journal of electronic materials. 2007 Oct 1;36(10):1333-40.

[33] Zhang R, Moon KS, Lin W, Wong CP. Preparation of highly conductive polymer nanocomposites by low temperature sintering of silver nanoparticles. Journal of Materials Chemistry. 2010;20(10):2018-23.

[34] Rivers G, Marzbanrad E, Hook MD, Lee-Sullivan P, Zhou YN, Zhao B. Highly-stable silver nanobelts joined via diffusion-free attachment. Nanotechnology. 2016 Jun 13;27(29):295606.

[35] Pashayi K, Fard HR, Lai F, Iruvanti S, Plawsky J, Borca-Tasciuc T. High thermal conductivity epoxy-silver composites based on self-constructed nanostructured metallic networks. Journal of Applied Physics. 2012 May 15;111(10):104310.

[36] Lu CA, Lin P, Lin HC, Wang SF. Effects of metallo-organic decomposition agents on thermal decomposition and electrical conductivity of low-temperature-curing silver paste. Japanese journal of applied physics. 2006 Sep 7;45(9R):6987.

[37] Hu A, Guo JY, Alarifi H, Patane G, Zhou Y, Compagnini G, Xu CX. Low temperature sintering of Ag nanoparticles for flexible electronics packaging. Applied Physics Letters. 2010 Oct 11;97(15):153117.

[38] Magdassi S, Grouchko M, Berezin O, Kamyshny A. Triggering the sintering of silver nanoparticles at room temperature. ACS nano. 2010 Apr 7;4(4):1943-8.

[39] Siow KS. Are sintered silver joints ready for use as interconnect material in microelectronic packaging?. Journal of electronic materials. 2014 Apr 1;43(4):947.

[40] Zhang Z, Lu GQ. Pressure-assisted low-temperature sintering of silver paste as an alternative die-attach solution to solder reflow. IEEE Transactions on electronics packaging manufacturing. 2002 Oct;25(4):279-83.

[41] Lei TG, Calata JN, Lu GQ, Chen X, Luo S. Low-Temperature Sintering of Nanoscale Silver Paste for Attaching Large-Area (>100 mm^2) Chips. IEEE Transactions on Components and Packaging Technologies. 2010 Mar;33(1):98-104.

[42] Sakaniwa Y, Iida M, Tada Y, Inoue M. Conduction path development in electrically conductive adhesives composed of an epoxy-based binder. Electronics Packaging and iMAPS All Asia Conference (ICEP-IACC), 2015 International Conference on 2015 Apr 14 (pp. 252-257). IEEE.

[43] Inoue M, Sakaniwa Y, Tada Y. In-situ analysis of electrical conductivity evolution in epoxy-based conductive adhesives with Ag loading during curing process. CPMT Symposium Japan (ICSJ), 2014 IEEE 2014 Nov 4 (pp. 190-193). IEEE.

[44] Sakaniwa Y, Tada Y, Inoue M. Effect of chemical factors on the evolution of electrical conductivity during curing in Ag-loaded conductive adhesives composed of an epoxy-based binder—A new understanding of electrically conductive adhesives. Electronics Packaging (ICEP), 2014 International Conference on 2014 Apr 23 (pp. 176-180). IEEE.

[45] Xiong N, Li Z, Li J, Xie H, Wang Y. Influence of curing procedures on the electrical properties of epoxy-based isotropic conductive adhesives. In Proc. Electronic Packaging Technology (ICEPT), 2014 15th International Conference on 2014 Aug 12 (pp. 373-377). IEEE.

[46] Cui HW, Fan Q, Li DS, Tang X. Formulation and characterization of electrically conductive adhesives for electronic packaging. The Journal of Adhesion. 2013 Jan 1;89(1):19-36.

[47] Cui HW, Jiu JT, Nagao S, Sugahara T, Suganuma K, Uchida H, Schroder KA. Ultra-fast photonic curing of electrically conductive adhesives fabricated from vinyl ester resin and silver micro-flakes for printed electronics. RSC Advances. 2014;4(31):15914-22.

[48] Cui HW, Du WH. Novel Fast-Curing Electrically Conductive Adhesives from a Functional Epoxy and Micro Silver Flakes: Preparation, Characterization, and Humid-Thermal Aging. The Journal of Adhesion. 2013 Sep 2;89(9):714-26.

[49] Macdonald, J. R., & Barsoukov, E. (2005). Impedance spectroscopy: theory, experiment, and applications. History, 1(8).

[50] Sluyters JH, Oomen JJ. On the impedance of galvanic cells: II. Experimental verification. Recueil des Travaux Chimiques des Pays-Bas. 1960 Jan 1;79(10):1101-10.

[51] Snugovsky, L., P. Snugovsky, D. D. Perovic, S. Bagheri, and J. W. Rutter. "Microstructures formed from mixed solders on copper substrate." Materials Science and Technology 25, no. 12 (2009): 1467-1473.

[52] Kim, Dae-Gon, Jong-Woong Kim, and Seung-Boo Jung. "Evaluation of solder joint reliability in flip chip package under thermal shock test." Thin solid films 504, no. 1 (2006): 426-430.

[53] Laurila, Tomi, T. Mattila, V. Vuorinen, J. Karppinen, Jue Li, M. Sippola, and Jorma K. Kivilahti. "Evolution of microstructure and failure mechanism of lead-free solder interconnections in power cycling and thermal shock tests." Microelectronics Reliability 47, no. 7 (2007): 1135-1144.

[54] https://www.mathworks.com/matlabcentral/fileexchange/63967-rmonitoringem-v20170802

[55] http://www.eng.uwaterloo.ca/~d9xu/

[56] Giancoli, D. "25. Electric Currents and Resistance”." Physics for Scientists and Engineers with Modern Physics (4th edition ed.). Upper Saddle River, New Jersey: Prentice Hall (1984): 658.

[57] Chang, Y. W., T. H. Chiang, and Chih Chen. "Effect of void propagation on bump resistance due to electromigration in flip-chip solder joints using Kelvin structure." Applied Physics Letters 91, no. 13 (2007): 132113.

[58] Tseng, H. W., C. T. Lu, Y. H. Hsiao, P. L. Liao, Y. C. Chuang, T. Y. Chung, and C. Y. Liu. "Electromigration-induced failures at Cu/Sn/Cu flip-chip joint interfaces." Microelectronics Reliability 50, no. 8 (2010): 1159-1162.

[59] Choi, W. J., E. C. C. Yeh, and K. N. Tu. "Mean-time-to-failure study of flip chip solder joints on Cu/Ni (V)/Al thin-film under-bump-metallization." Journal of applied physics 94, no. 9 (2003): 5665-5671.

[60] Liu, Y. H., and K. L. Lin. "Damages and microstructural variation of high-lead and eutectic SnPb composite flip chip solder bumps induced by electromigration." Journal of materials research 20, no. 08 (2005): 2184-2193.

[61] Yamanaka, Kimihiro, Yutaka Tsukada, and Katsuaki Suganuma. "Studies on solder bump electromigration in Cu/Sn–3Ag–0.5 Cu/Cu system." Microelectronics Reliability 47, no. 8 (2007): 1280-1287.

[62] Xu DE, Hook MD, Mayer M. Real time joint resistance monitoring during solder reflow. Journal of Alloys and Compounds. 2016 Nov 25.

[63] IPC J-STD-004B (2008), "Requirements for Soldering Fluxes", Joint Industry Standard,Supercedes J-STD-004A

[64] https://www.mathworks.com/matlabcentral/fileexchange/63964-resistance-monitoring-of-solder-reflow-process

[65] Shu Y, Rajathurai K, Gao F, Cui Q, Gu Z. Synthesis and thermal properties of low melting temperature tin/indium (Sn/In) lead-free nanosolders and their melting behavior in a vapor flux. Journal of Alloys and Compounds. 2015 Mar 25;626:391-400.

[66] Gao F, Rajathurai K, Cui Q, Zhou G, NkengforAcha I, Gu Z. Effect of surface oxide on the melting behavior of lead-free solder nanowires and nanorods. Applied Surface Science. 2012 Jul 15;258(19):7507-14.

[67] Jin Y, Hu J, Lu D. Investigation of the fundamental interactions among the ingredients of flux by the group contribution method. InElectronic Packaging Technology & High Density Packaging, 2009. ICEPT-HDP'09. International Conference on 2009 Aug 10 (pp. 894-899). IEEE.

[68] Hance WB, Lee NC. Voiding mechanisms in SMT. Soldering & Surface Mount Technology. 1993 Jan 1;5(1):16-21.

[69] Nam S, Cho HW, Kim T, Kim D, Sung BJ, Lim S, Kim H. Effects of silica particles on the electrical percolation threshold and thermomechanical properties of epoxy/silver nanocomposites. Applied Physics Letters. 2011 Jul 25;99(4):043104.

[70] Liang J, Li L, Tong K, Ren Z, Hu W, Niu X, Chen Y, Pei Q. Silver nanowire percolation network soldered with graphene oxide at room temperature and its application for fully stretchable polymer light-emitting diodes. ACS nano. 2014 Jan 29;8(2):1590-600.

[71] Lau JH. Solder joint reliability: theory and applications. Springer Science & Business Media; 1991 May 31.

[72] Li T, Tan JY, Khoo SA, Breach CD, Hawkins JA. Thermal and Wetting Properties of Water-Soluble Fluxes and Solder Pastes. Components, Packaging and Manufacturing Technology, IEEE Transactions on. 2014 Nov;4(11):1871-8.

[73] Chung CL, Moon KS, Wong CP. Influence of flux on wetting behavior of lead-free solder balls during the infrared-reflow process. Journal of electronic materials. 2005 Jul 1;34(7):994-1001.

[74] Yu F, Cui J, Zhou Z, Fang K, Johnson RW, Hamilton MC. Reliability of Ag Sintering for Power Semiconductor Die Attach in High Temperature Applications. IEEE Transactions on Power Electronics. 2016 Nov 21.

[75] Modugno MC, Wereszczak AA, Waters SB. Toward Interpreting Failure in Sintered-Silver Interconnection Systems. Additional Papers and Presentations. 2016 Jan;2016(HiTEC):000234-41.

[76] Wereszczak AA, Modugno MC, Waters SB, DeVoto DJ, Paret PP. Method to Determine Maximum Allowable Sinterable Silver Interconnect Size. Additional Papers and Presentations. 2016 Jan;2016(HiTsEC):000207-15.

[77] LOCTITE ABLESTIK SSP 2020 MSDS [Online]; Henkel Electronic Materials LLC: Irvine, CA, Oct 23, 2014. http://hybris.cms.henkel.com/henkel/msdspdf?matnr=1735608&country=US&language=EN (accessed Feb 27, 2017).

[78] Jenny England, Xinpei Cao, Hajime Inoue, Steven Josso, Anja Henckens. Silver Sintering for Power Electronics. MEPTEC, October 23, 2014

[79] https://www.mathworks.com/matlabcentral/fileexchange/63963-resistance-monitoring-of-silver-sintering-process

[80] Kuphaldt TR. Lessons from electric circuits, Volume I – DC, Chapter 12 - Physics Of Conductors And Insulators. (2007)

[81] Lu D, Tong QK, Wong CP. A study of lubricants on silver flakes for microelectronics conductive adhesives. IEEE Transactions on Components and Packaging Technologies. 1999 Sep;22(3):365-71.

[82] Lu D, Wong C. Thermal decomposition of silver flake lubricants. Journal of thermal analysis and calorimetry. 2000 Jul 1;61(1):3-12.

[83] Akada Y, Tatsumi H, Yamaguchi T, Hirose A, Morita T, Ide E. Interfacial bonding mechanism using silver metallo-organic nanoparticles to bulk metals and observation of sintering behavior. Materials transactions. 2008 Jul 1;49(7):1537-45.

[84] LOCTITE ABLESTIK SSP 2020 Technical Data Sheet [Online]; Henkel Electronic Materials LLC: Irvine, CA, Oct, 2012. https://tds.us.henkel.com/NA/UT/HNAUTTDS.nsf/web/07277E203E5FED5E85257B080060D5FE/$File/LOCTITE%20ABLESTIK%20SSP%202020-EN.pdf (accessed Mar 07, 2017).

[85] Wakuda D, Kim KS, Suganuma K. Room temperature sintering of Ag nanoparticles by drying solvent. Scripta Materialia. 2008 Sep 30;59(6):649-52.

[86] Ide E, Angata S, Hirose A, Kobayashi KF. Metal–metal bonding process using Ag metallo-organic nanoparticles. Acta materialia. 2005 May 31;53(8):2385-93.

[87] Peng P, Hu A, Gerlich AP, Liu Y, Zhou YN. Self-generated local heating induced nanojoining for room temperature pressureless flexible electronic packaging. Scientific reports. 2015;5.

[88] Zhou W, Zheng Z, Wang C, Wang Z, An R. One-Step Fabrication of 3D Nanohierarchical Nickel Nanomace Array To Sinter with Silver NPs and the Interfacial Analysis. ACS applied materials & interfaces. 2017 Jan 30;9(5):4798-807.

[89] Kinloch A. Adhesion and adhesives: science and technology. Springer Science & Business Media; 2012 Dec 6.

[90] SMDLTLFP Solder Paste No-Clean Sn42/Bi57.6/Ag0.4 in 5cc Syringe 15g T3 Mesh Technical Data Sheet [Online]; Chip Quik Inc., http://www.chipquik.com/datasheets/SMDLTLFP.pdf (accessed June 02, 2017).

[91] https://www.mathworks.com/matlabcentral/fileexchange/63966-resistance-monitoring-in-power-cycling

Appendix A - List of publications

Journal papers

- **Xu DE**, Kim JB, Hook MD, Jung JP, Mayer M. Real time resistance monitoring during sintering of silver paste. Journal of Alloys and Compounds. 2017 Oct 12. (Accepted)

- **Xu DE**, Hook MD, Mayer M. Real time joint resistance monitoring during solder reflow. Journal of Alloys and Compounds. 2017 Feb 25;695:3002-10.

- **Xu DE**, Chow J, Mayer M, Jung JP, Yoon JH. Sn-Ag-Cu to Cu joint current aging test and evolution of resistance and microstructure. Electronic Materials Letters. 2015 Nov 1;11(6):1078-84.