MEMS Switches Implemented in Different Technologies for RF Applications

by

Ahmed Abdel Aziz

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Examining Committee Membership

The following served on the Examining Committee for this thesis. The decision of the Examining Committee is by majority vote.

External Examiner	NAME: **Luc G. Fréchette** Title: Professor, Université de Sherbrooke
Supervisor(s)	NAME: **Raafat R. Mansour** Title: Professor
Internal Member	NAME: **Siva Sivoththaman** Title: Professor
Internal Member	NAME: **Christopher Backhouse** Title: Professor
Internal-external Member	NAME: **Patricia Nieva** Title: Professor

Author's Declaration

I hereby declare that I am the sole author of the thesis. This is a true copy of the thesis, including any required final revisions, as accepted by the examiners. I understand that the thesis may be made electronically available to the public.

Abstract

Microfabrication technologies allow building micro-scale and nano-scale mechanical switches. Despite the fact that the solid-state switches exhibit superior performance as compared to their micro-mechanical competitors in terms of speed and lifetime, mechanical switches exhibit various attractive features such as low power consumption, high linearity, high isolation and low loss.

This work summarizes the design, fabrication and testing of several micro-mechanical switches for Radio Frequency (RF) applications and using different microelectromechanical systems (MEMS) technologies. The implementation is carried out through four approaches for realizing MEMS switches.

In the first approach, the switches are built by post-processing chips fabricated in a standard complementary metal-oxide semiconductor (CMOS) fabrication process. The structural layers of the electrostatic MEMS switches are implemented in the four metal layers of the back end of line (BEOL) in the standard CMOS 0.35µm process. In addition, an enhanced post-processing technique is developed and implemented successfully. The switches presented include a compact 4-bit capacitor bank, a compact 4-bit phase shifter / delay line, a W-band single pole single through (SPST) series capacitive switch, SPST shunt capacitive switches with enhanced capacitance density, and a proposed compact T-switch cell with metal-to-metal contact switches.

In the second approach, a standard multi-user MEMS process is implemented. Electrothermal and electrostatic MEMS switches designed, fabricated and tested for low-frequency high-power RF applications using the MetalMUMPs process. The devices include a 3-bit capacitor bank, a compact discrete capacitor bank that can be configured for 2-bit / 3-bit operation depending on the stroke of the electrothermal actuators, and a novel rotor-based electrostatic multi-port switch.

In the third approach, an in-house university-based microfabrication process is developed in order to build reliable MEMS switches. The UWMEMS process, which was developed at the Center for Integrated RF Engineering (CIRFE), is used in this research to fabricate novel switch configurations. Moreover, the capabilities of the standard UWMEMS process are further expanded in order to allow for building geometric confinement (GC) or anchorless switches and other novel switches. The gold-based UWMEMS switches presented include compact T-switches, R-switches and C-switches, GC SPST shunt and series switches. Additionally, other novel switch architectures such as the hybrid self-actuation switch (HSAS) and thermally-restored switches (TRS).

In the fourth approach, which is a hybrid approach between the first and third approaches, the MEMS switches are built and packaged in one fabrication process, and without the need for sacrificial layer, by means of a wafer-level packaging technique. Adopting silicon wafers for the microfabrication necessitates using silicon-core switching, which offers few attractive advantages as compared to the metal-based

switches implemented by the third approach. The designed switches to be fabricated in a state-of-the-art industrial facility include a variety of simple SPST contact-type switches as well as compact designs of T-switch, C-switch, a novel four-port gimbal-based switch (G-switch) introduced in this work, SP4T cells, and a seesaw push-pull SPST switch design is included.

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Dedication

All my time and efforts in the past years is dedicated to the love of my family.

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Chapter 1: Introduction

1.1 Motivation

Microfabrication technology enables realizing micro-electromechanical systems (MEMS) and nano-electromechanical systems (NEMS) that are employed nowadays in many applications such as inertial navigation systems, energy harvesting, communications, pharmaceuticals, etc. Among this variety, MEMS and NEMS allow building mechanical switches for microwave and RF applications. While, IC-based or solid-state switching outperforms its mechanical counterparts in terms of speed and durability / reliability due to the fundamental differences between their physics of operation, mechanical switching exhibits several attractive features such as low insertion loss and excellent linearity performance. Other advantages include ultra-low power operation for the widely used electrostatically actuated switches. Recent research demonstrates that the leakage and switching power consumption of micromachined mechanical switches can be as low as three orders of magnitude less than that of the electronic switching.

The major reliability concerns of RF MEMS switches are mechanical fatigue, dielectric charging, stiction and contacts wear. The mechanical fatigue exists due to the presence of bending stresses associating the switching operation. The stiction and contact wear problems are inevitable if there is a need for physical contact between two surfaces, which is mandatory for direct metal-metal interfaces encountered in RF MEMS contact-type switches. Besides, dielectric charging is encountered if the electrostatic actuation is employed with relatively large values of potential differences (or, more accurately, electric fields) across thin layers of dielectrics.

In this work, enhanced and new designs of MEMS switches are realized in different microfabrication technologies with a focus on improving switch reliability. Four main approaches for building MEMS switches are considered, exploiting the relative advantages of each technology as well as allowing the comparison of the performance differences between the switches implemented. It is also possible to explore the possibilities for hybridization or integration of switches using more than one technology.

In the first method, the switches are built by post-processing chips fabricated in a standard IC fabrication process, where the MEMS switches are implemented in the metal layers in the back end of line (BEOL) of the standard CMOS processes. This provides high consistency and reproducibility of results while restricting the structural layers to specific materials and thicknesses. It is also very advantageous to have the potential for monolithic integration with the MEMS interface circuitry. One main challenge with such post-processing technique is the implementation of the metal-metal contact-type switches. Another challenge is coping with the loss due to the low conductivity of the silicon substrate.

In the second approach, a standard multi-user MEMS process, MetalMUMPs, was utilized to realize high RF power switches. It is typically desirable to use thick metal layers. Also, the operation under high power would necessitate careful considerations for the immunity towards self-actuation. Taking into consideration as well the need for high restoring force, especially for the ON state at high RF power operation and for hot switching, the MetalMUMPs process appears to be the most attractive option even though there is only one metal layer in this MetalMUMPs process that makes implementation of RF and microwave circuits very limited. It is worth noting that, in addition to using wire bonding for a second metal layer, flip-chip techniques can join more than one chip together. On another positive side, that feature itself can potentially help in building redundancy switch matrices. Moreover, the thermal actuation mechanism should not be considered negatively in terms of high actuation power consumption due to the feasibility of mechanical latching and reconfigurability. It is worth noting that the electrostatic actuation is still a possible option, though it is inefficient in terms of force level due to the minimum feature size allowed.

Thirdly, a custom process is developed in order to build the MEMS switches. The UWMEMS process introduced in early 2000s and developed gradually over the past years for RF applications would be a good starting point; it can be further expanded and optimized for RF switches. This gold-based ceramic-substrate surface micromachining process with its two relatively thin metal layers allows for building metal-metal contact-type switches as well as capacitive switches. However, there is still a lot of room for expansion. For instance, adopting high resistivity silicon (HRS) for the substrate material would pave the way for the packaging of the fabricated switches and integrating with modern silicon-based technologies such as through-silicon via (TSV). Also, in order to have much more reliable contact-type switches, a tough contact pair (e.g. Au-Ru) can be employed. That would necessitate high-forcing electromechanical design of the actuators. For a reasonable footprint of the actuator, the thickness of the structural layer would need to be increased considerably, which is also feasible.

Furthermore, the degrees of freedom in implementing different switch architectures can be increased significantly by means of using different approaches for post-processing the UWMEMS chips. For instance, sacrificing the first dielectric layer in the process would allow for the release of the first metal layer, i.e. resulting in two structural layers instead of one. The post-processing as well can include mask-less dry etching of the original polymer-based sacrificial layer of the second metal that is the structural layer. As a result, it is then possible to implement the anchorless or geometric confinement (GC) micro-beams by sacrificing the first and second dielectric layers depending on the post-processing sequence. Anchoring necessitates the bending of the micro-beam throughout the switching action, which induces stresses in its material that significantly affect the switch lifetime or evolution of its mechanical performance due to the mechanical fatigue. In addition, anchoring necessitates incorporating mechanical stiffness, which does not allow tuning MEMS and NEMS dynamics using only different domains such as electrostatic and magnetic.

Also, the mechanical boundary conditions associated with clamping limit the maximum attainable out-of-plane deflections, especially for the electrostatically driven switches. Controllable large out-of-plane deflections can be useful, for instance, in achieving higher isolation in RF MEMS switches. In view of the commonly used attractive actuation fields, the out-of-deflections are only towards the substrate, which limits the degrees of freedom of the switch design and performance. It is worth noting here that the great majority of the ongoing research does not focus on having the switch beam flat (i.e. released and rigid – or thick-enough) during switching or, in other words, decoupling the basic "connect-disconnect" functionality of mechanical switches from the need to bend or to clamp the beams. Another important by-product of the GC concept is the remote electrostatic actuation (REA) that is a must for actuating the essentially loose GC micro-beams by a capacitive voltage divider similar to the gating or control of the scratch drive actuators (SDA).

Finally, in the fourth approach, which is actually a hybrid result based on the first and third aforementioned approaches, the MEMS switches can be built and packaged in the same processing sequence and even with no need for the conventional sacrificial layer essential for surface micromachining. This is possible by virtue of wafer-level packaging technology. It is worth mentioning that adopting silicon wafers for such microfabrication process necessitates using silicon-core switching, which offers some attractive advantages as compared to the metal-based switches implemented typically in the first three approaches.

1.2 Thesis Main Objectives

Objective 1:

Development and analysis of multi-port RF MEMS switches with a focus on reliability improvement

Objective 2:

Investigation and implementation of several microfabrication processes for realizing reliable RF MEMS switches:

Developing reliable post-processing techniques for building the CMOS-MEMS switches

Exploiting the advantage of the MetalMUMPs process in building high RF power switches

Further development and expansion of the UWMEMS process and post-processing sequences

Packaging of the fabricated switches in order to test their reliability in typical operating conditions

1.3 Thesis Outline

Chapter Two:

In this chapter, the literature survey on the typical requirements for reliable MEMS switches for RF applications is provided.

Chapter Three:

Using the first approach, different designs of CMOS-MEMS RF switches are discussed with regards to their operation and the fabrication / measurement results. The devices are all implemented in the 0.35μm technology.

Chapter Four:

By means of the second approach, nickel-based switch designs fabricated in the MetalMUMPs multi-user MEMS process are reported and discussed in view of their design and fabrication / measurement results. The switches presented are mostly reconfigured using electrothermal actuation with latching for the sake of low actuation power consumption.

Chapter Five:

Using the third approach, the UWMEMS surface-micromachined gold-based switches fabricated are presented and analyzed. In addition, the novel switches employing the expanded version of the UWMEMS process introduced by virtue of an enhanced and more general chip post-processing process are discussed.

Chapter Six:

Following the fourth and last approach to be presented in this work, a new wafer-level packaging microfabrication process is presented, and the silicon-core high-forcing hermetically sealed MEMS switches designed for the first generation of fabrication are discussed.

Chapter Seven:

Finally, the summary of design and fabrication results is provided in this chapter. This is followed by the listing of the main conclusions and recommendations for future work.

Chapter 2: The Need for RF MEMS Switches

This chapter discusses the major considerations for building reliable RF MEMS switches. First, the RF switch is described with focus on the reliability concerns encountered due to its architecture and physics of operation. Second, the main design challenges are addressed.

2.1 Mechanical Switches

A mechanical switch is constituted of a conducting beam that is switched by a control force between two terminals such that the beam connects or disconnects these terminals [1-4]. The basic architecture of the mechanical switch is illustrated in Fig 2.1. MEMS and NEMS switches are normally in the OFF state (open) after being released, which prevents the electrical signal flow or electrical connection between the two terminals unless the control force is present and the switch becomes in the ON state (closed), and connects the two terminals 1 and 2.

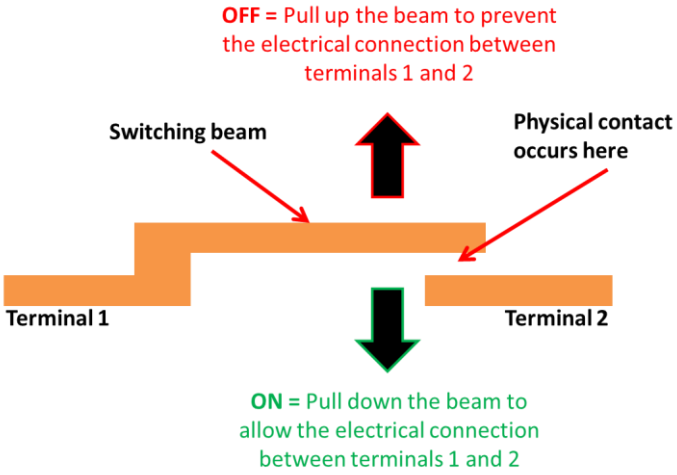


Fig 2.1: The basic architecture of a mechanical switch

The components of a mechanical switch are illustrated in Fig 2.2. Switching from OFF state to ON state necessitates that the beam undergoes bending to bring the tip of the beam in contact with terminal 2. This is governed by the net force, depending on the actuation and restoring forces, F_A and F_R, respectively. The physical nature of these forces (i.e. mechanical, electrostatic, magnetic, etc.) and their magnitudes affect the switching time of the switch. In addition, the switch must provide an appropriate amount of contact force F_C between the free end of the switching beam and terminal 2 such that the contact resistance is

appropriate for the application for which switch is used. This imposes strict limitations on the cleanliness of the contact surface as well as preserving high quality surface through the lifetime of the switch [2]. When the electrical connection is not required, the restoring force F_R should also be enough to pull the beam back. The restoring force controls the ON to OFF switching time. If the force is large, not only the restoring time is shorter, but it can overcome more efficiently the existing surface force between the two contacting surfaces.

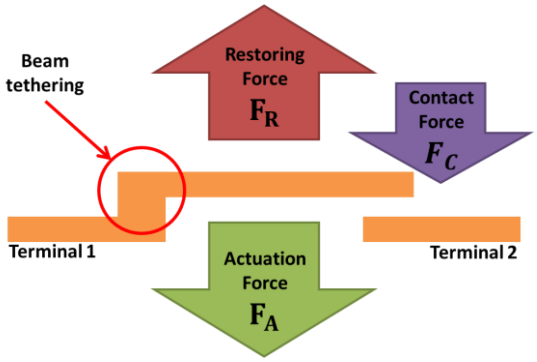


Fig 2.2: Main components of the operation of a mechanical switch

The idea of contact-type switches represents the mechanical analogue of solid state switches or electronic transistors that are based on the widespread semiconductor technology such as the P-type-Intrinsic-N-type (PIN) diodes, where a current switches the connection between the N-doped and P-doped terminals, and field effect transistors (FET), where an appropriate voltage at one of the transistor's terminals (gate) switches the electrical signal between two other terminals (drain and source) [5]. The major drawback of PIN diodes, in conjunction with high power consumption, is their low frequency limitation that is typically in the KHz-MHz range. On the other hand, the main drawback of FET switches is the degraded high frequency isolation performance due to the drain to source capacitance that is typically in the vicinity of 10-50fF.

There are major differences between the switching mechanisms and switching performance of solid state and mechanical switches [2, 3]. This becomes clear if micromachined mechanical switches are compared to their solid-state counterparts. MEMS switches outperform well the solid-state switches in terms of power consumption, isolation, insertion loss in conjunction with linearity and intermodulation [2, 3, 5]. The isolation describes the ability of the switch to isolate the terminals electrically whereas the insertion loss indicates the power loss due to the electric signal transmission between the terminals of the switch [6]. Even though some MEMS devices require more than 100V for their electrostatic actuation, they do not dissipate current, and typically energy of less than 100nJ can be wasted per switching cycle [3]. Other more

dissipative techniques such as thermal and electromagnetic actuation can be designed to latch when switched, and this also makes their overall power consumption less than that of solid state devices. Additionally, MEMS switches possess actuation air gaps on the order of 1-3μm, which makes their OFF state capacitance as low as 1-4fF. This necessarily means very good isolation for frequencies up to 60GHz [3, 5]. The more the isolation, the better the filtering and lower the interference.

Moreover, the insertion loss of MEMS switches can be better than 0.1dB. For switching networks, an electrical signal typically passes by several switches in series (depending on the routing), which makes it crucial to have mechanical switches rather than solid-state switches where the insertion loss is as low as 0.5 dB per switch. As a rule of thumb, it is always beneficial to reduce the number of connections in the networking or routing system. Furthermore, MEMS switches are much more linear, and the linearity concerned in comparison is the electrical linearity in terms of electrical performance and their intermodulation products. The mechanical linearity is meaningless for solid-state switches. Actually, MEMS switches allow for 30-50dB more linearity as compared to solid state switches. More linearity leads to less generated noise that accumulates in an unwanted fashion if there are several switches encountered in the signal path.

Besides the superior electrical performance, mechanical switching exhibits major drawbacks as compared to solid-state devices. The limitations include low switching speed, high voltage or current requirements, high power handling capability issues, reliability and packaging issues [2, 3, 5]. First, mechanical switching requires the deformation or the movement of a given mass, and the solid-state switches are then expected to be faster. The fastest MEMS switches are those actuated electrostatically, and they can have switching times as low as 1-10μsec [5]. However, this switching speed is not acceptable for some communication and radar systems. Second, MEMS mechanical switches require high voltage operation and almost no current for the electrostatically actuated devices whereas the thermally actuated devices can operate with as low as 1-3V driving large currents up to 100 mA [3]. For portable devices, such ratings are problematic.

Third, most of MEMS switches cannot handle signal powers up to 5-10 W [5]. Some of these switches can easily undergo self-actuation due to high power levels. Fourth, MEMS switches suffer from reliability problems. This fact limits their cycling lifetime typically to 10s billion cycles, and has been the main reason behind their limited commercialization. In fact, the reliability of contact-type switches has been limited by the metal-to-metal interface, whereas the reliability of capacitive MEMS switches used to be mainly limited by dielectric charging [7]. Recently, researchers focus on developing dielectric-less capacitive switches, which eliminates the charging problem. Finally, in order to keep the contact surfaces reliable as much as possible, packaging of MEMS switches requires inert and low humidity environment for sealing them, which necessitates employing hermetic packaging [2, 4, 8, 9]. Table 2.1 compares between the solid state and mechanical switching [2].

Table 2.1: Reproduced data for solid-state and mechanical switching from [2]

Type of Switch	Insertion loss	Isolation	Linearity	Power	Speed
Solid-state	0.5 dB	25 dB	40 dBm	5 mW	< 100 ns
MEMS	0.1 dB	35 dB	65 dBm	10 µW	< 10 µs

Actuation of MEMS switches can be electrostatic, piezoelectric, magnetic, electromagnetic, thermal or electro-thermal [3, 5, 10, 11]. Most of the reliable RF MEMS switches demonstrated to date are based on electrostatic actuation [5, 9]. They can operate up to 100GHz at relatively low RF power for contact-type and medium RF power for the capacitive-type switches. The major advantages of electrostatic actuation are the very low power consumption and the design simplicity. However, it relatively provides small forces and requires often-high voltage levels. Thermal actuation can be accomplished using dissimilar thermal expansion coefficients of two or more dissimilar materials in order to induce motion if heated or cooled. It can also employ a single material type carrying an electric current and heated non-homogeneously using this current, which is recognized as electro-thermal actuation. The major drawbacks of thermal actuation are low speed operation and high power consumption [3, 10, 11]. The disadvantage of electromagnetic actuation is that it dissipates high current leading to high power consumption [5, 12]. Employing hybrid actuation physics allows making use of the advantages of both techniques. For instance, the work in [12] utilizes hybrid electromagnetic and electrostatic actuation scheme in order to suppress the required voltage down to 3.3V. This is at the expense of supplying 50mA current.

2.1.1 Metallic Contact

At high frequencies such as in RF applications, it is very common to encounter metal-to-metal contacts for high performance devices. In order to monitor the reliability of such contacts, the value of the contact resistance can be estimated from the measured insertion loss or from DC contact resistance measurements during the cycling of the mechanical switch. It can also be characterized using nano-indentation apparatus that is combined with highly sensitive source in order to emulate the cycling of a switch without fabrication [2, 4]. The mechanism of nano-indentation provides accurate monitoring of the contact force and displacement while the sensitive electronics measure the corresponding contact resistance. High performance metal contact switches should exhibit the lowest possible contact resistance and the highest possible lifetime. To accomplish this, it is essential to maintain clean surface for the contact. Organic residues are among the typical problems imposing cleanliness limitations. For the cases where the sacrificial layer is not a polymer (e.g. sacrificial metal), the contact resistance is much more improved [2,13]. For

instance, sacrificial Aluminum or Copper can be used for to release structural gold switches. Also, wafer storage prior to bonding or packaging leads to undesirable deposition of contaminants from the environment on the contact surface, which results in the degradation of contact resistance and reliability. Plasma cleaning can be used to clean the contact surfaces for storage wafers before their packaging or hermetic sealing. Such plasma cleaning can sometimes render the contact surface even cleaner than that of the as-fabricated, however, clean contact surfaces are reported to aggravate the metal to metal stiction problems especially for the soft metals such as pure gold [2].

Moreover, even though the current driven through mechanical contact-type switch is relatively small, the current density can be very large in view of the very small contact area that can be as low as 100nm in diameter [2, 4]. As a result, there can be local melting at the contact area due to the generated heat. In addition, high electric fields can polymerize nearby organic molecules, which can degrade the surface. The absence of organic molecules in the ambient of the contact surface is clearly crucial, and this reveals the need for hermetic packaging. In general, the selection of contact metal depends on its hardness, electrical resistivity, melting temperature as well as its processing flexibility. Gold offers an attractive electrical resistivity, but its hardness is relatively small, and it limits its performance as a contact metal. In addition, gold exhibits very low chemical reactivity, which makes it the most inert material in terms of oxidation. Traces of oxide can still exist even within hermetic packaging [5], and a tiny layer of oxide can cause remarkable increase in the contact resistance when the contact force is low. Harder metals include Rhodium, Ruthenium and Tungsten. The harder the material, the less stiction problems it causes even with very high contact forces that are then crucial for attaining reasonable contact resistance values due to the very small contact area. Even though harder materials such as Ru and Rh are better candidates in order to avoid stiction at contact, they tend to absorb organic vapor from air and form a contaminating film [4]. In general, bimetallic or asymmetric contacts have superior stiction immunity as compared to monometallic or symmetric contacts [4, 9]. Table 2.2 compares some of contact materials in terms of the aforementioned properties.

Table 2.2: Reproduced data for contact material properties [2]

Contact Material	**Resistivity (Ω.cm)**	**Hardness (MPa)**	**Melting point (^{0} C)**	**Chemical Reactivity**	**Process Complexity**
Au	2.2×10^{-6}	250	1060	Lowest	Simple etching
$AuNi_5$	12×10^{-6}	1600	1040	Very low	Simple etching
Rh	4.3×10^{-6}	2500	1960	Low	Difficult etching
Rn	7.1×10^{-6}	2700	2330	Low	Difficult etching
Ir	4.7×10^{-6}	2700	2460	Low	Difficult etching

W	$5.5x10^{-6}$	> 3000	3420	Medium	Simple etching
Mo	$5x10^{-6}$	2000	2620	Medium low	Simple etching

For metal-to-metal contacts where the contacting metals are the same, the contact resistance R_c can be written in terms of the material hardness H and the contact force F_c as in Eq. 2.1. The contact resistance is also inversely proportional to the square root of the contact area A_c as shown in Eq. 2.2. The model in Eq. 2.1 corresponds to plastic deformation of the contact area, and, accordingly, it does not apply for small forces leading to elastic or hybrid elastic-plastic deformation of the contact area [2, 4].

$$R_c \propto \sqrt{\frac{H}{F_c}} \qquad \text{Eq. 2.1}$$

$$A_c \propto \frac{F_c}{H} \qquad \text{Eq. 2.2}$$

As compared to Rh contact coating, pure Au and AuNi contact surfaces show comparatively stable contact resistance with contact forces below 30µN. On the other hand, Rh contact layers show stable contact resistance values for contact forces above 50µN. If the material is harder such as W and Ir, there is a need for more contact force in order not only to obtain appropriate resistance values but also to overcome the oxidation layer caused by the chemical reactivity of such harder metals, and this is where the trade-off lies. Moreover, although hard metals provide unmatched contact reliability performance in terms of stiction, they are not also easily integrated into fabrication processes, and they are not suitable at all for low contact force switches (below 100µN) [5, 9]. W and Mo allow for more hardness along with higher thermal budget for the operation in terms of their high melting temperatures. Such temperatures make it easy to handle high power signals without significant degradation of the contact, but the major drawback of using W and Mo is they are more prone to oxidation. Clearly, the material selection should be made through compromise between the different properties of the contact material in mechanical and electrical domains. Table 2.3 includes the main selection criteria.

Table 2.3: Main selection criteria for the contact material

Contact Material Property	**Main Reason**
Low electrical conductivity	To reduce the conduction losses
High melting point	To handle high power
High hardness	To avoid stiction at the contact
Low chemical reactivity	To avoid oxidation

The contact resistance for micromachined switches results from the electrical conduction through a very small area. As a result, micro-scale contacts are significantly different from their macro-scale counterparts. The contact in micro-scale is very sensitive to the surface roughness of the contact materials, and surface protrusions (or asperities) are responsible for the electrical conduction. Depending on how the electrical conduction is performed, different contact resistance models are built and experimented [4,14]. If the electronic mean free path in the material is much smaller than the contact size, the Ohmic contact model is then assumed. For an electrical resistivity ρ and contact size a, the contact resistance R_c is given in Eq. 2.3. The current density can be relatively very large depending on the contact area, and this can lead to serious high power issues including localized melting. In addition, the Ohmic model assumes no interdependences between the asperities. This means that the overall resistance for a given area is simply the parallel combination of the contact resistance imposed by the different spots available in that area.

$$R_c = \frac{\rho}{2a} \qquad \text{Eq. 2.3}$$

On the other hand, if the mean free path of electrons is much larger than the contact size or contact radius, the transport of electrons through the contact surface is then ballistic, and the resistance model is referred to as ballistic contact [4]. In ballistic transport of electrons, the electrical resistance does not result from scattering. As a matter of fact, the motion is similar to that of projectiles, and electrons are assumed to collide elastically given the constriction. The contact resistance is accordingly modeled using Sharvin's resistance formula given in Eq. 2.4. In the equation, a is the effective contact radius and K is the electronic Knudsen number that is the ration between the electronic mean free path and contact size. If the mean free path of the electrons is on the same order as that of the contact size, the contact resistance model is then a hybrid model between Ohmic (Holm's) and ballistic (Sharvin's) models, and it is quasi-ballistic contact resistance model then.

$$R_c = \frac{4\rho K}{2\pi a} \qquad \text{Eq. 2.4}$$

Since the current flow through contact is localized to the contact asperities, the heating of the contact is consequently localized, so the switch can operate at room temperature while the contact areas undergoes softening or melting. If the contact is Ohmic, the temperature is then proportional to the contact voltage and its ambient temperature. Moreover, since the temperature rises at the contact, the resistivity of the contact material must consider its temperature dependent evolution through specific temperature coefficient. Furthermore, the switching triggers thermal cycling at the contact, which affects the creep performance of

the contact [4]. Recalling the asperity deformation, if the softening temperature is attained, the plastic deformation is more pronounced at lower values of contact pressure, and the effective contact area is larger which leads to lower contact resistance. The softening temperature of gold contacts is around 100^0 C, and it corresponds to 70-80mV and 40mA contact current whereas that for ruthenium contacts is about 430^0 C, corresponding to 200mV and 30mA at room temperature [2]. When softening temperature is reached, the contact temperature does not anymore depend strongly on high contact current. Also, metal softening triggers strain hardening leading to the wear of the contact area.

Based on the value of the contact resistance, a figure of merit FOM for MEMS switches can be calculated as given in Eq. 2.5. R_{on} is the series resistance of the switch when it is ON or actuated and C_{off} is the OFF-state capacitance of the switch. The contact resistance is the main constituent of R_{on} and it has to be suppressed as much as possible in order for FOM to be the highest possible. If the values of FOM for mechanical and solid-state switches are compared, it is found to be remarkably higher for the mechanical switches. The FOM for FET and GaAs switches is up to 250GHz whereas, for instance, its value for the MEMS switch in [15] is reported as 3.8THz, i.e. 12 times higher.

$$FOM = \frac{1}{2\pi R_{on} C_{off}} \qquad \text{Eq. 2.5}$$

2.1.2 Actuation Force, Contact Force and Restoring Force

Since low and stable contact resistance requires generally high contact force, it should be noted that Fig 2.2 uncovers a trade-off between contact force and restoring force for the fact that their sum has to be anyway equal to the actuation force according to Eq. 2.6. In fact, the equation reveals that an increase of the contact force must be accompanied by a decrease of the restoring force, and vice versa. This trade-off is undesirable since a reliable switch should have high contact force while having high restoring force for high stiction immunity especially for soft contact materials in conjunction with high OFF to ON switching time.

$$F_A = F_C + F_R \qquad \text{Eq. 2.6}$$

Taking this trade-off into consideration, it is obvious that in order to increase the contact and restoring force simultaneously, the actuation force itself has to be increased significantly. For the widely used electrostatic actuation switches, the force can be increased by simply increasing the voltage difference, or by reducing the electrostatic actuation gap. However, depending on the design specifications, reducing the air gap may not be possible due to the isolation constraints. Moreover, there can be voltage constraints that do not allow

for more contact force. An efficient solution for such a problem is increasing the voltage starting from an intermediate state in which the tip of the beam is already pulled-in and touching the contact electrode where the entire beam is close to the actuation electrodes. In other words, the basic operation of the mechanical switch has to be modified in a way such that there are two steps for the actuation force resulting into different levels for each of the restoring and contact forces [16, 17]. The approach described here is illustrated in Fig 2.3 that is reproduced from [2].

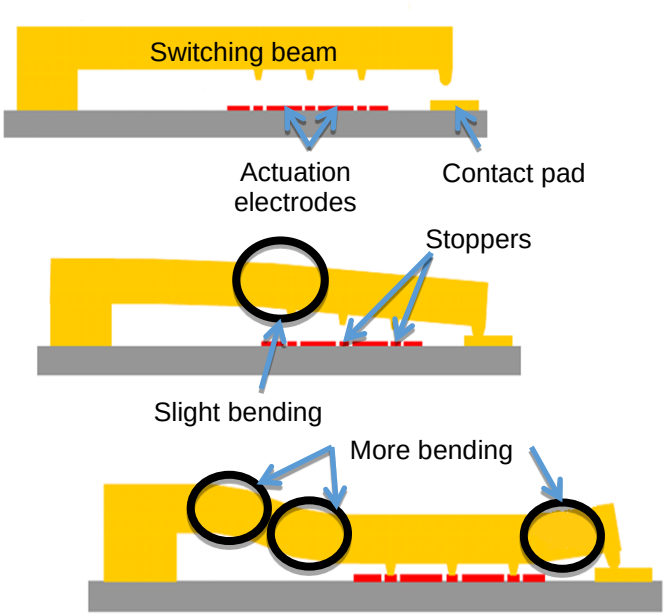


Fig 2.3: Mechanical solution towards increased contact force; adapted from [2]

The basic switch of Fig 2.3 is referred to as the collapsing switch or two-position switch. In step 0 that is the non-actuated state, the lumped stiffness at the tip of the cantilever is K_1; not all the length of the beam contribute to this stiffness. Step 1 represents the intermediate state mentioned above where the tip of the beam is landed on the contact metal. The actuation voltage required to attain step 1 is within the typically applied values; however, when the voltage is not much increased, the beam snaps down or collapses such that its stoppers are all landed, and the lumped stiffness for that case is made of K_1 and K_2 together leading to step 2. Encountering K_1 and K_2 together necessitates that the restoring force must increase when the contact force increases. Another more advantageous version of the two-position MEMS switch reported in [16] is displayed in Fig 2.4. The switch is capable of providing up to 1mN contact force in conjunction with 0.5mN restoring force when the actuation voltage is 90V. Two actuation or pull-down electrodes are employed. The force F_1 contributes the most to the first step of cantilever bending leading to physical

contact between the tip of the cantilever and the dielectric stopper. In the second step, the force F_2 is much more effective leading to partial collapsing of the cantilever. Other switches with similar architecture exhibiting high contact and restoring forces are reported in [17]. The force F_2 is large with not much voltage increase due to the small actuation air gap between the electrode and the switched beam.

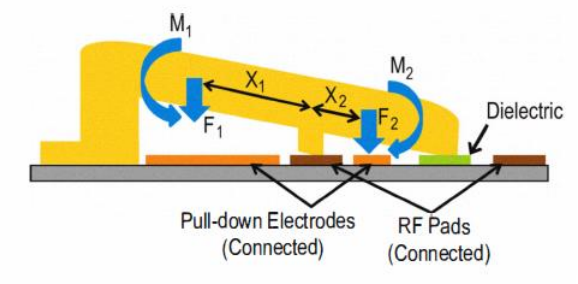


Fig 2.4: Two-position contact-type switch; reproduced from [16]

2.1.3 Mechanical Properties of the Switching Beam

In conjunction with the implications of direct metal-metal contacts in contact-type switches, it is instructive to address another major reliability concern that is the mechanical performance of the switching beam that depends on that of the structural layers. The study of the mechanical properties of micromachined structures is crucial for analyzing their reliability. Since most of the mechanical properties of materials depend on their microstructure, there are significant differences between such properties for micro-scale and macro-scale structures. In micro-scale domain, the size of the entire structure can be of the order of a grain size. For instance, bulk micromachining of silicon structures renders the structural layer almost the same properties of bulk material due to that the micromachined structure possesses the same crystal orientation. If surface micromachining is used, the layers are not single crystalline anymore, and their grain microstructure affects vehemently their mechanical performance. Ultimate tensile strength, proportional limit strength and fracture strength, Young's modulus, fatigue and creep are among the properties that depend strongly on the level of miniaturization of mechanical systems [18,19]. The properties also depend on the architecture of the structural layer. For instance, plates and wide surface micromachined beams are typically perforated for the feasibility of their wet release as well as for damping-related issues. The etching or release holes are reported to induce up to 50% reduction in the tensile strength of some poly-silicon thin films in conjunction with approximately 20% reduction in the Young's modulus [18].

The cyclic loading and unloading of the switching beam under the effect of frequent actuation trigger mechanical fatigue. In other words, when loading and unloading is associated with deformation such as

bending, mechanical fatigue is pronounced. This is one of implications of clamping the switching beams, in addition to the increased stiffness due to such cross-sectional fixation. Conventionally, micromachined mechanical switches are based on clamped-clamped or clamped-free beams [1, 5]. The anchoring has been an essential design component implying that the maximum stress is located at the anchor, and its value depends on the mechanical design that depends on the actuation and restoring forces. As a result of anchoring, not only fatigue exists, but also energy loss through coupling to the support or the substrate [20]. Also, the fatigue performance of amorphous materials is different from that of crystalline or polycrystalline structural layers. For example, the fatigue effects and the degradation of deflection performance are much less pronounced in thermally grown SiO_2 films as compared to metals, and this is attributed to the amorphous nature of such dielectrics, and around 10^{10} cycles with insignificant performance degradation was reported [1].

The creep performance of structural layers is important if the components are operated at high temperatures or for materials that can creep at room temperature such as polymers [1,19]. Since the creep performance is the outcome of temperature cycling, the most sensitive devices to creep or thermal cycling are those that are thermally or electro-thermally actuated. Similar to fatigue and creep, Young's modulus and residual stresses depend strongly on how structural layers for micromachined devices are fabricated. If the switching beam is not subjected to cyclic thermal loading, the mechanical fatigue can be the dominant failure mode, especially when the contact reliability is not the bottleneck (as in capacitive switching where there is no need for contact current). Similar to the experimentation of metallic contact reliability that must allow precise control of the contact force and displacement as well as the accurate measurement of the contact resistance, the mechanical fatigue testing procedure must also be capable of two main functions. First, it should allow the generation of various forcing and deformation levels in order to provide a wide range of stresses to be tested. Second, it must be feasible to monitor specific degradation of performance or material damage during the cycling of the beam [19].

In literature, resonant frequency, quality factor and electrical resistance measurements are widely used as damage or performance degradation detectors for the sake of characterizing the fatigue. Employing the pull-in voltage of an electrostatically actuated beam as fatigue detector was recently reported [18]. Through the evolution of an intermittent cyclic loading, the pull-in voltage of the beam is measured and stored periodically after certain number of cycles. The collapse criterion can be set such that, for instance, when the measured pull-in voltage is changed by at least 10%, damage can then be declared. In this technique of fatigue detection, the frequency of the AC voltage signal should not hit the mechanical resonance frequency of the structure due to that dynamic amplification disturbs the evaluation of internal stresses of the beam material and the technique is based on detecting changes to stiffness which in turn necessitates the shift of the resonant frequency. This is actually how the measurement of resonant frequency can be used as damage

detector for fatigue testing. The analysis reported in [18] for clamped-free gold micro-beams before and after failure due to mechanical fatigue confirms the fact that the damage is induced at the clamped region where the maximum stress exists. The reason behind the damage seen in the scanning electron microscopy (SEM) at the surface of the micro-beam is the fact that this surface is subjected to tension, and tensile loading produces faster degradation in metals during fatigue testing. The local surface yielding of the failing micro-beams is related strongly to the loss of stiffness and pull-in voltage reduction. This correlation matches the findings in [21], and the testing using static actuation reveals that there is no loss of stiffness for the gold micro-beam as pronounced by the unchanged pull-in voltage. This means that the structural stiffness of the device was not affected by static loading, and the stiffness loss is just triggered dynamically. However, if the static loading induces plastic deformation, the mechanical behavior of the gold thin films depends as well on their dimensions [22].

2.1.4 Dielectric Material for Electrostatic Actuation

Besides the ability to use it as a stopper (Fig 2.3 and Fig 2.4), the presence of the dielectric on top of the actuation electrode offers three other advantages. First, it allows the protection of the voltage source from short circuit if the beam collapses on the actuation electrode (due to absence or inappropriate design of stoppers). Second, the physical contact between metal and dielectric is more efficient in terms of contact stiction that is more pronounced for direct metal-to-metal contact. Third, if an air gap is filled partially with a dielectric, the effective air thickness of that dielectric is equal to its physical thickness divided by its permittivity. This fact is very advantageous when the released beam is to have a small actuation air gap (effectively) while it is isolated from the contact pad with large enough actual air gap.

However, placing a thin film of dielectric between two conductive electrodes with high enough voltage across them induces dielectric charging problems, which imposes a serious reliability concern for capacitive MEMS switches for RF applications [5, 6, 23-26], for instance, this dielectric charging occurs leading to drifts in the pull-in voltage [7]. The exact mechanism by which electric charges get into the dielectric and end up to be trapped is not completely understood, however, the effect of dielectric charging can be easily measured and quantified. Since the capacitance for such RF MEMS switch is required to be the highest possible when the dielectric layer separates the electrodes, the layer is made relatively too thin, and it is below 100nm typically [5, 23, 24]. The voltage across the layer can be up to 50-70V, which necessitates having an electric field across the layer on the order of 1-10MV.cm^{-1}. It is thought that under such high field conditions, the electric charges can tunnel through the dielectric layer while a portion of the charges get trapped into the layer, sometimes for few days depending on the recombination rate and amount of trapped charges. The tunneling is thought to be similar to Frenkel-Poole emissions in insulating films for which the current density is exponentially related to the voltage across the layer, and, accordingly, the

electric field [23]. Charge trapping into the dielectric causes serious problems for the ON state as well as the OFF state of a RF MEMS capacitive switch or a conventional switch with dielectric protecting the actuation electrode. The trapped charges result in screening effects for the electric fields used in actuation. The screening hinders generally the operation of the switch. If the switch is required to switch from ON to OFF, the build-up of charges generated a voltage drop that opposes the applied voltage. If the applied voltage is not high enough to counteract charging, the actuation can be impossible at some point. When the actuation voltage is removed so that the switch goes back to the non-actuated state or OFF state, the build-up charges can hold the switch in the actuated position, thus preventing it from switching. This is well recognized in literature as stiction problem leading normally to failure of the switch.

If the switching voltage is composed of AC only, then the forcing frequency is double the input frequency only since the electrostatic force is proportional to the square of the voltage difference. However, if there is DC and AC, the forcing has two components at two different frequencies, one of them at the input frequency whereas the other one is at the double. Dielectric charging causes DC build-up of reverse polarity. To investigate experimentally the presence of dielectric charging, AC only can be used to actuate the beam, and if there is a component of the signal at the input frequency, then there are charges across the dielectric [27]. To get rid of such charges, there is a need to reverse the polarity of the applied DC component of the actuation voltage. The amount needed to annihilate the forcing component at the input frequency can be used to quantify the dielectric charging. It is worth noting that dielectric charging is significant when the switching beam comes into contact with the dielectric [28]. This can be avoided using stoppers as mentioned previously (see Fig 2.3 and Fig 2.4). In fact, for dielectric-less switching, the reliability of the mechanical switches is then mainly affected by the contact and mechanical performance of the switching beam [2, 4].

2.2 Mechanical Switches in RF Applications

The previous sections report on the almost ideal electrical response of micromachined mechanical switches. They have been employed typically in various applications, including RF and microwave applications such as switching networks, matching networks, tunable filters and phase shifters [5, 6, 8, 9, 30]. The term RF MEMS refers to the design and fabrication of MEMS devices that serve as main components of RF integrated circuits (RFIC) in addition to enhancing discrete elements that are used for RF operation [3, 5, 31]. For instance, in communication industry, the switches are used for signal routing. Such switches can also be used to share one antenna between a transmitter and a receiver. Fig 2.5 displays the block diagram of switching networks in addition to the SEM micrographs of a previously fabricated 3-by-3 switching matrix at CIRFE [32, 33]. For certain configuration of the mechanical switches all over the network, the signal can be routed from any port to the other. It is obvious that the number of ports and, accordingly, the

number of routing alternatives are critical information for the design of such matrices. As mentioned previously, for large matrices, a single route can be formed using several contact-type mechanical switches in series along the signal path. As a result, it is very important to reduce the insertion loss per switch as highlighted previously. Not only the insertion loss is to be minimized, but also the switching time of individual switches is required to be reduced as much as possible.

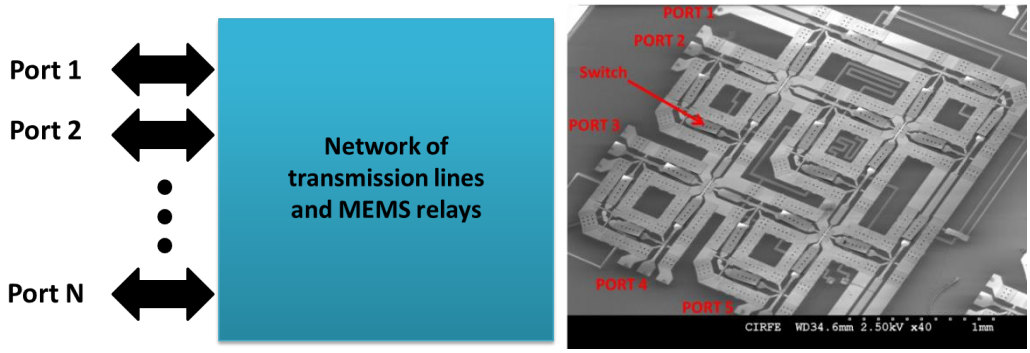


Fig 2.5: (Left) Block diagram for RF switching network; (right) CPW-based previously fabricated switched network at CIRFE

In Fig 2.6, the basic block diagram of a phase shifter is shown and camera photo of a previously fabricated shifter at CIRFE. Given certain ON/OFF setting for the MEMS switches, the path taken by electrical signals between two ports (i.e. ports 1 and 2) can change such that a different time delay is associated with each of these paths.

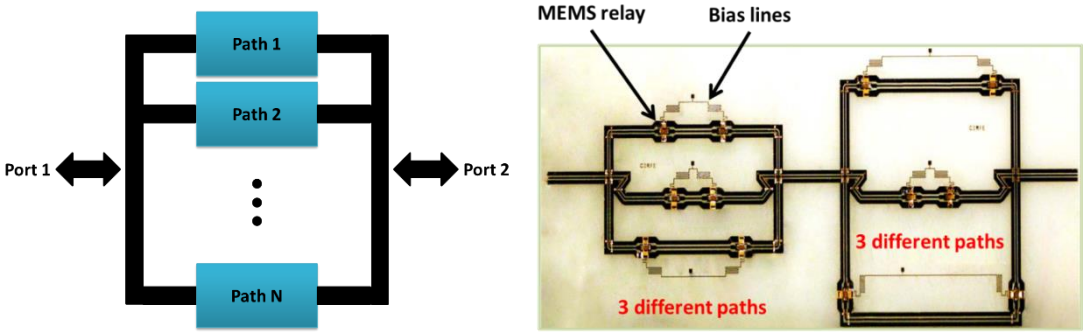


Fig 2.6: (Left) Block diagram for reconfigurable phase shifters; (right) CPW-based phase shifter previously fabricated at CIRFE

Similarly, MEMS switches can be employed in improving the gain of an antenna [34]. Due to the increased demands for higher bit rates, wireless systems shift from 2.5- 5GHz band to 60GHz band. However, the

attenuation due to path loss at that range is aggravated by more than 20dB, and the operation of CMOS at such frequencies imply lower transmit power; hence, the gain of the antenna at such frequencies is very critical. On the other hand, increasing the frequency to 60GHz necessitates decreasing the wavelength by the same factor, which allows integrating multiple antennas in phased arrays. Such phased arrays are typically used in steering the beam and achieving high gain antenna. The phase differences between the radiating elements are performed by means of switching, which is where MEMS switches exist for the fact that they exhibit relatively much lower insertion loss at frequencies above 40GHz as compared to their ferroelectric and solid state switches [5, 34].

In addition to this, Fig 2.7 shows the block diagram of a capacitance bank for CPW termination and the SEM micrographs of a previously fabricated capacitance bank at CIRFE. Depending on the configuration of the individual switches, a different value of capacitance can be loaded to the shunt termination of the CPW line. For N switches with only two states per switch, the overall number of states is 2^N. This determines directly the number of discrete values for the loading capacitance.

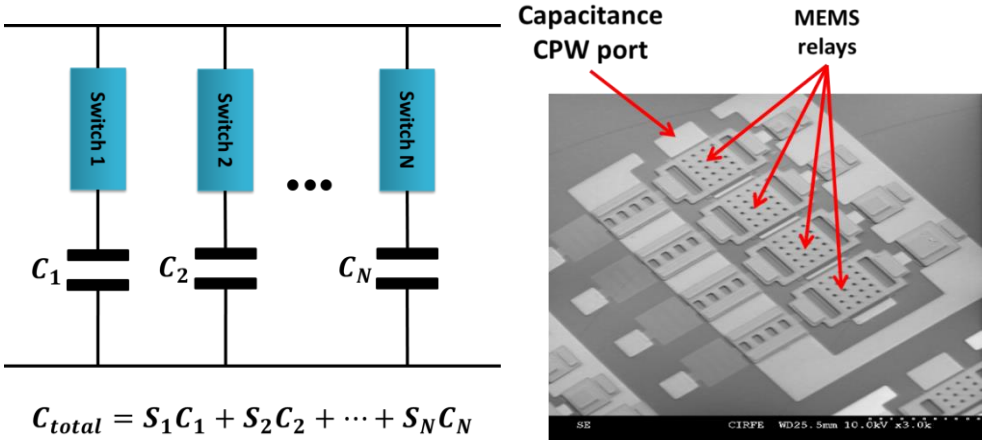


Fig 2.7: (Left) Block diagram for the tunable capacitance; (right) CPW-based capacitance bank previously fabricated at CIRFE

2.2.1 Series RF MEMS Switch

There are two main architectures for RF MEMS switches, namely, series and shunt [5]. In series switching, the switch beam is part of the transmission line. Fig 2.8 displays the widely used electrostatic actuation co-planar waveguide (CPW) series switch, where the switched beam is part of the signal line of the CPW. To actuate the cantilever beam such that it connects the CPW signal lines from ports 1 and 2, the appropriate voltage difference must exist between the center line to which the beam is anchored (port 1) and the DC

bias pad. The resistive bias lines exist to prevent loading the signal line at high frequencies of the signal line when the switch is actuated. The bias lines should be resistive enough; however, depending on the value of the actuation capacitance, this may result in an increase of the RC time constant for the switching action, which is undesirable. In fact, using this architecture, there is always a tradeoff between the loading cancellation and the time constant of the actuation capacitance through the resistive bias lines to the DC pad that is ground for the RF signal.

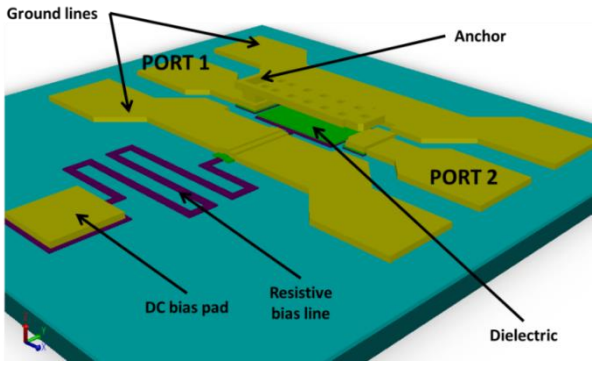


Fig 2.8: Conventional series RF MEMS switch

It is worth noting that the RF signal of the CPW can be switched ON and OFF through switching not only the signal line of the CPW, but also through its ground lines, but the ground levels of the two ports are normally connected within the measurement devices situated in the same laboratory, this approach is not practically employed.

2.2.2 Shunt RF MEMS Switch

In addition to the series contact-type switches, shunt RF switches as illustrated in Fig 2.9 are widely used as basic elements for various RF MEMS switching applications. The operation for the shunt switch is the opposite of that for the series switch. If the series switch is not actuated, the signal is not transmitted and the ports are isolated from each other with reflections due to the open circuit in the signal line. As soon as the series switch is closed, the two ports are connected and the signal can be transmitted with some insertion loss. On the other hand, for shunt switches, the signal is transmitted as long as the shunting beam is not actuated. When the bridge is switched, it results in short circuit termination for the contact-type shunt switching and high-frequency short circuit termination for the capacitive type shunt switching involving dielectric as demonstrated in Fig 2.9.

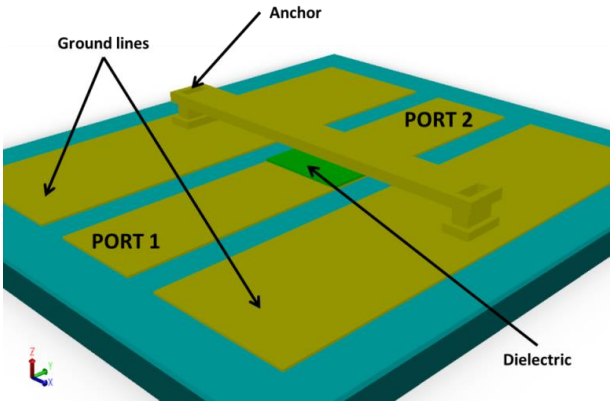


Fig 2.9: Conventional shunt RF MEMS switch

The shunt capacitive switching is widely used, and dielectric materials with high permittivity are highly recommended such that the loading capacitance is the highest possible, thus exhibiting accurately short circuit termination at the frequency range of interest. Fig 2.10 shows the ON and OFF states of the basic shunt capacitive MEMS switch. Typically, actuated to non-actuated capacitance is to be at least 100 times for acceptable performance [5]. The shunt beam is electrostatically actuated by means of a voltage difference between the signal line of the CPW and its ground lines. It is worth noting that reducing the actuation voltage of the RF MEMS switches make them more appealing to industry as well as wider range of applications where not only the power consumption is limited, but also the voltage supply is limited. However, reducing the switching voltage has a lower bound. In fact, self-actuation in response to high power signals imposes the lower limit for the switching voltage [35]. If the bridge is not stiff enough mechanically, the switch is then allowed to self-actuate independent of the voltage applied to it and depending primarily on the RF power level.

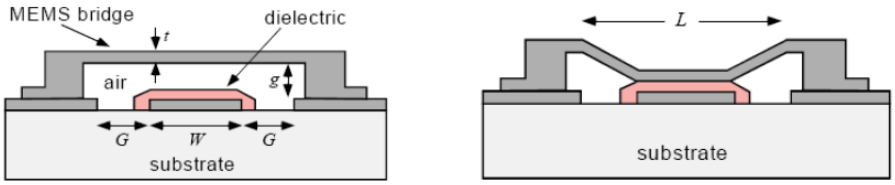


Fig 2.10: The operation of capacitive shunt RF MEMS switch

In general, there are two actuation mechanisms that can be applied to mechanical switches: static actuation and dynamic actuation [27, 36]. In electrostatic actuation, the term "static" refers to the case when only DC voltage is employed in switching. Besides, the term "dynamic" refers to the case when AC voltage is

involved in the electrostatic actuation process. The main advantage of the dynamic electrostatic actuation is the significant voltage reduction that can be up to 70% [27, 34, 37]. The major drawback of the dynamic mechanism is the switching speed that is remarkably larger than that associated with the static actuation.

Chapter 3: RF CMOS-MEMS Switches

The fabrication of RF MEMS switches can be accomplished in a multitude of different ways including the post-processing of a fabricated chip where the technology is not necessarily a MEMS technology. This chapter considers such cases and reports on the design and fabrication of various RF MEMS switches based on the mask-less post-processing of as-received CMOS chips using the standard 0.35µm technology. It is worth mentioning that similar post-processing procedures can be accomplished in similar technologies including the more advanced CMOS technologies such as 0.18µm. That would generally benefit from more degrees of freedom in terms of implementing different MEMS switch architectures in conjunction with the possibility for monolithic integration with solid state devices / circuits running at higher frequencies, e.g. mm-Wave. This is all at the cost of significantly higher price per chip.

Section 3.1 demonstrates the design and post-processing of CMOS-MEMS capacitive switches whereas section 3.2 covers the design and fabrication of another CMOS-MEMS compact switching cell employing metal-metal contact.

3.1 Design and Fabrication of CMOS-MEMS Capacitive Switches

The post-processing of CMOS chips in order to fabricate MEMS devices has mostly been employing the back end of line (BEOL) layers where the different stacking of metal and insulating oxide layers are used to build the structural layer(s) of the MEMS device [8, 51, 55].

3.1.1 Compact CMOS-MEMS Digital Capacitor Bank

Digital MEMS switched capacitor banks are key components in the design of tunable RF devices [51]. They offer a superior performance in both linearity and Q in comparison with their semiconductor counterparts. While it is feasible to realize switched capacitor banks by integrating SPST MEMS switches with bank of capacitors, such approach often leads to high losses and very low self-resonance frequency. More recently, monolithically integrated MEMS switched capacitor banks have been reported in [8, 52-54]. While offering excellent performance, they are generally limited to low frequency application. With the emergence of 5G systems, there is a need to develop monolithic switched capacitor banks that can operate in the 4-6GHz range.

The 4-bit compact capacitor bank proposed utilizes capacitive loading of a CPW signal line by means of MEMS clamped-free beams that connect the loading capacitance to ground. The micromachined beams of the corresponding bits are all initially warped with significantly large deflection of their tips representing the up-state, or state “0000” of the capacitor bank in order to increase the capacitance tuning ratio. Engaging

any of the 4 bits requires applying a DC voltage to its designated micro-beams such that the voltage difference between the warping beam and the CPW ground plane pulls-in the beam and loads the signal line with significant capacitance. The structure of the capacitor bank is displayed in Fig 3.1.

Fig 3.2 demonstrates the HFSS simulation results of the 16 different states of the compact capacitor bank. The simulated self-resonance exceeds 16GHz whereas the up-state capacitance (state 1) is around 50fF. The footprint of the capacitor bank is 0.6mm x 0.9mm including the 150µm DC pads.

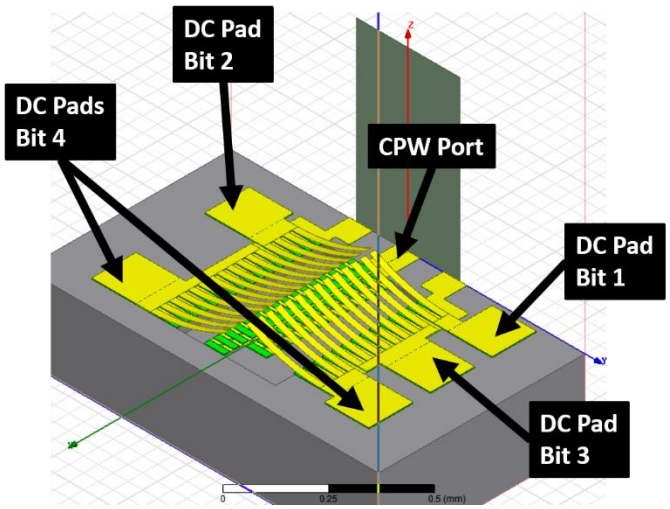


Fig 3.1: 3D structure of the proposed compact 4-bit CMOS capacitor bank designed and simulated

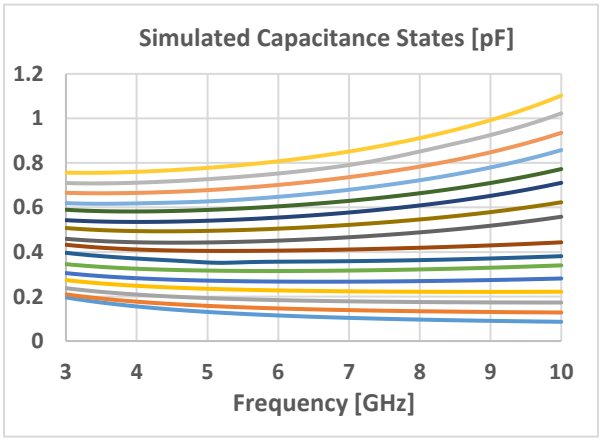


Fig 3.2: Simulated capacitance values for the first state (all beams up) and last state (all beams down)

The device fabrication employs a mask-less post-processing of the silicon-substrate chips fabricated using standard CMOS technology [56]. The main post-processing steps are illustrated with the cross-sections in Fig 3.3. The layout for the as-received CMOS chips was designed as shown in Fig 3.3a, where the uppermost metal layer (M4) is primarily used as a hard mask for the subsequent dry etching of the exposed oxide layers as well as the isotropic etching of low-resistivity silicon in the substrate. Reducing the mass of such lossy silicon in contact with and near the RF circuit is very critical for the overall performance of such devices given the low-resistivity nature of the standard CMOS substrates [63, 64, 66]. The impact of such significant conductivity is addressed more in the next pages where the measurement results are discussed and analyzed.

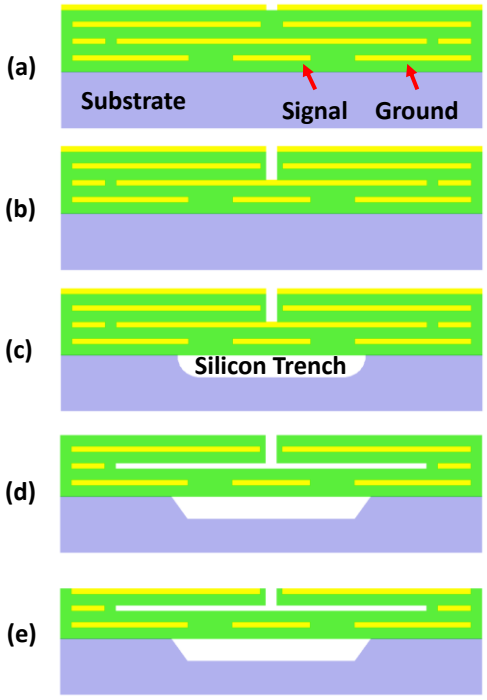


Fig 3.3: The employed fabrication procedure based on the mask-less post-processing of standard CMOS 0.35µm chips

In Fig 3.3b, the dry etching of the exposed oxide allows access to the second metal layer (M2), which is to be later sacrificed through wet etching along with the M4 layer. For large areas to be micromachined, there must be release holes. For the sake of simplicity, they are not shown in Fig 3.3. Also, such holes can expose the silicon volumes to be etched upon the complete dry etching of oxide layer. The subsequent isotropic etching of the exposed silicon is illustrated in Fig 3.3c, and the result of the wet etching step of Al along with the thin adhesion layers of TiN as well as the optional wet etching of the silicon pits is shown in Fig

3.3d. It should be noted that the last wet etching step of silicon in KOH has the advantage of thinning the oxide layers of the micro-beam, which improves the capacitance tuning ratio. Finally, after the proper drying of the wet-released chips in the critical point drier (CPD), the third and first metal layers (M1 and M3) are exposed by a second dry etching step of the oxide layer covering them.

The ability to control the residual stress in the micromachined composite beams of aluminum-oxide layers is the most critical for the tuning of the initial warpage of the beams and the RF performance. That is in terms of the up-state capacitance and the tuning ratio of the capacitor bank in conjunction with the electromechanical performance in terms of the restoring force in down-state and the required pull-in voltage. The inherent or as-fabricated stresses in the different chip layers can be analyzed following the same post-processing steps above while keeping the chip at low-enough temperatures (~ 10ºC) during the different dry etching steps. That was performed using an Oxford Instruments RIE with cryogenic cooling. In Fig 3.4, a scanning electron microscope (SEM) image of a capacitor bank post-processed while maintained at low temperature (i.e. without acquiring residual stress due to processing) reveals that the as-received stresses are not capable of providing the initial warpage required for the operation of the capacitor bank.

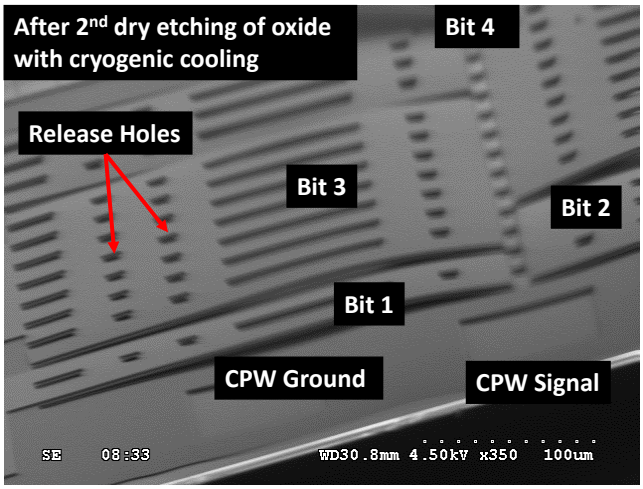


Fig 3.4: A scanning electron microscope (SEM) image of a released device using the post-processing step and cryogenic cooling of the chips (keeping them at ~ 10 ºC) during all the high-plasma-power dry etching steps

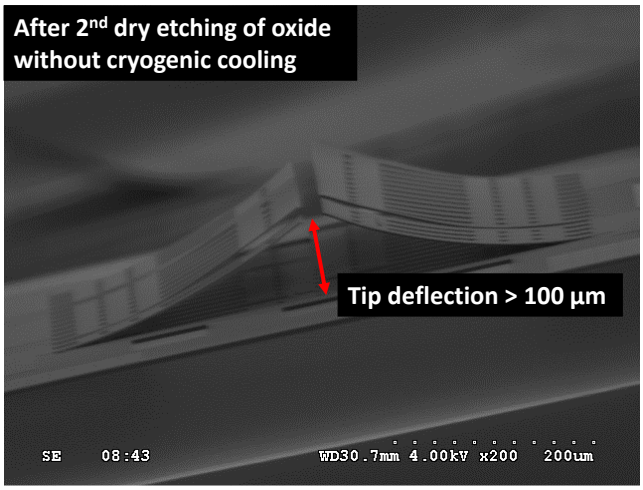


Fig 3.5: A scanning electron microscope (SEM) image of a released device using the post-processing step without using cryogenic cooling for the second dry etching step where the acquired stress is controlled via the duty cycle of the plasma generation in addition to the power level of the plasma

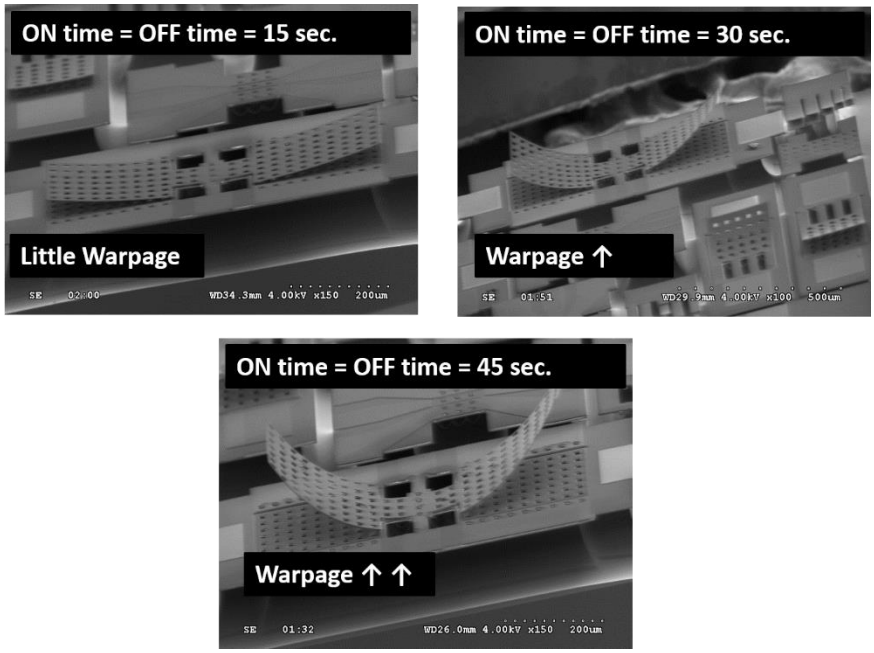


Fig 3.6: Impact of the post-processing timing on the warpage profile of the suspended structures in the absence of the cryogenic cooling. The power is 2.5 KW for the three cases

However, with good control of the duty cycle of the plasma etching (10-30sec intervals) and its high-power level (1-2.5 KW) in the last post-processing step aforementioned (where the dry etching of the oxide layer on top of the probing pads and the switched beams is performed), it is possible to tune the final residual

stress in the beams such that they warp in the desired orientation as demonstrated in Fig 3.5 and Fig 3.6. The tip deflection shown exceeds 100µm for the 250µm-long beams.

The different 16 states of the capacitor bank were measured, and the extracted capacitance values are plotted in Fig 3.7 for the frequency band of interest. Due to the thinning of the oxide layers during the KOH wet etching step of the silicon trench, the down-state capacitance increases significantly for each switched beam resulting in an overall increase in the capacitance values by more than 10%. Additionally, the measured tuning ratio is almost 10:1.

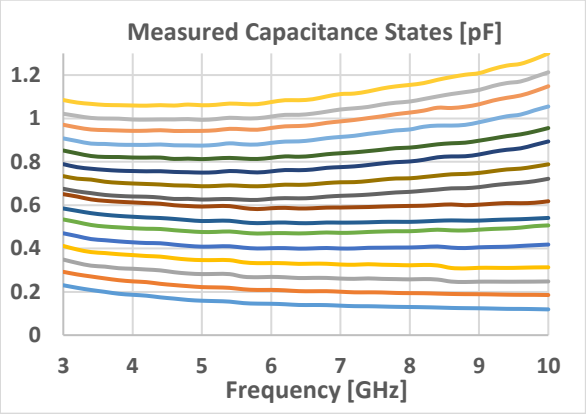


Fig 3.7: Measured capacitance values of the 16 different states of the proposed 4-bit capacitor bank

The measured Q is found to be less than five, which is significantly smaller than the simulated value that is up to 15 for a silicon trench depth of 50µm and no significant silicon undercut. This is due to the insufficient removal of low-resistivity-silicon in contact with or in the vicinity of the signal line, especially at the RF probing pads. Fig 3.8 shows the measured return loss at the maximum capacitance (state "1111") versus the extracted return loss using ADS after de-embedding the probing pads where it is clear that further dry and/or wet etching of the substrate silicon would alleviate the issue with the low Q of the proposed device [56, 63]. Tuning the lateral or isotropic etching component in the silicon dry etching while optimizing the design of the release holes would allow controlling the removal of silicon from underneath the capacitor bank without affecting the structural integrity of the device. Varying the trench depth and silicon undercut in HFSS of the structure in Fig 3.1 confirms that. It is worth noting that a slow-wave structure design can help reduce the overall loss without the need for trenching [60-62]. Such solution can lead to higher capacitance tuning ratios and relatively high values of Q can be achieved accordingly [57, 65].

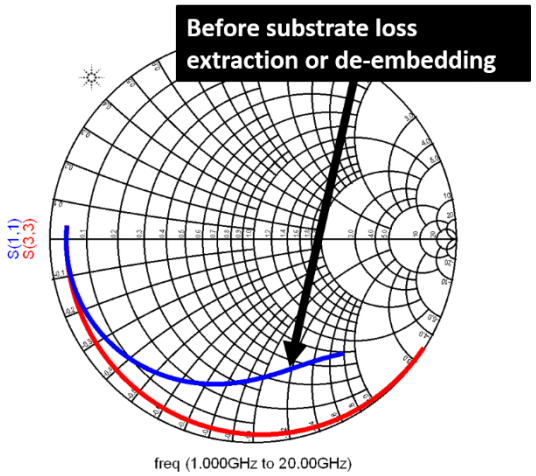


Fig 3.8: Measured return loss at the maximum capacitance (state "1111"), S11, versus the extracted return loss after de-embedding the probing pads, S33

3.1.2 CMOS-MEMS Digital Phase Shifter / Delay Line

Fig 3.9 demonstrate the design of a compact 4-bit phase shifter based on a similar concept of the capacitive switching and controlled warpage presented in the previous section. The same structure can be used as a delay line. The actuation voltage found experimentally is ~ 60-80V depending on the resulting warpage, and comparable values were obtained in COMSOL electromechanical simulations. As in the case of the compact 4-bit capacitor bank, it is possible to use a holding voltage using a bias tee connected to the signal line. In addition, depending on the power level, the low self-actuation immunity of the design can help hold the beams down in the absence of the actuation voltage.

Moreover, the symmetric design employed in the phase shifter offers relatively better matching for no significant deviation in the phase shift performance. Also, only one side can be used actuated if the loading capacitance per bit is to be less. The SEM picture of the post-processed phase shifter is displayed in Fig 3.10 where the tip deflection is ~ 100µm. This is the value that was used in the HFSS electromagnetic simulation (Fig 3.9).

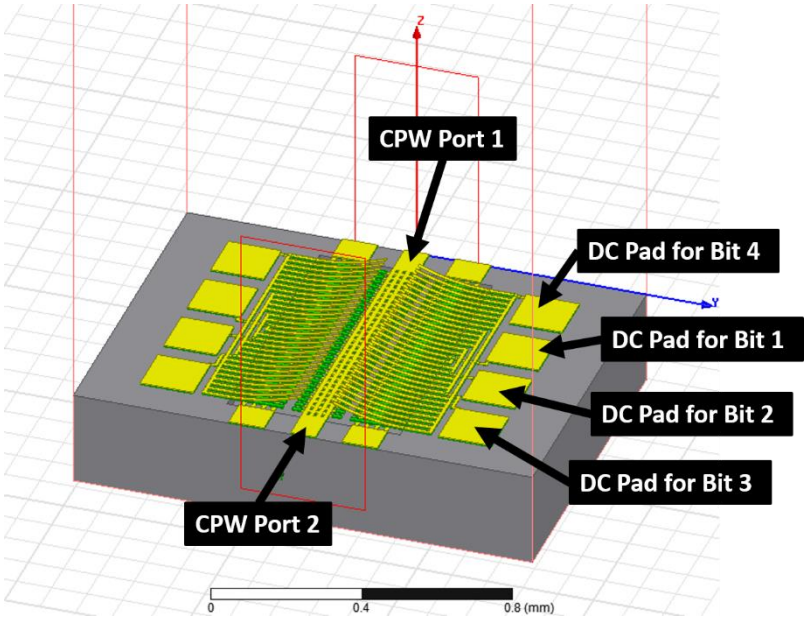


Fig 3.9: 3D structure of the proposed compact 4-bit CMOS-MEMS phase shifter / delay line

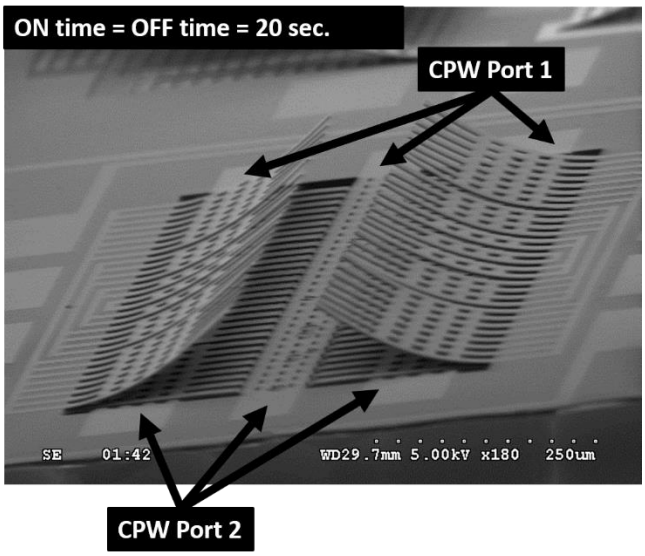


Fig 3.10: SEM of the fabricated compact 4-bit CMOS-MEMS phase shifter / delay line

Among the most important performance parameters for the design of phase shifters is the insertion loss as well as the insertion loss variation. For the different phase values or states of the device, it is always desirable to have the smallest possible variation of the phase shift more than the need for having low insertion loss. The HFSS electromagnetic simulation results in Fig 3.11 confirm the fact that the maximum

variation of the insertion loss over the operation bandwidth is ~ 1dB, which is relatively very good [67, 68]. Also, the insertion loss is acceptable. It should be noted that the matching and insertion loss strongly depends on the silicon trench shape and depth. The design and simulations assume 60µm trench depth.

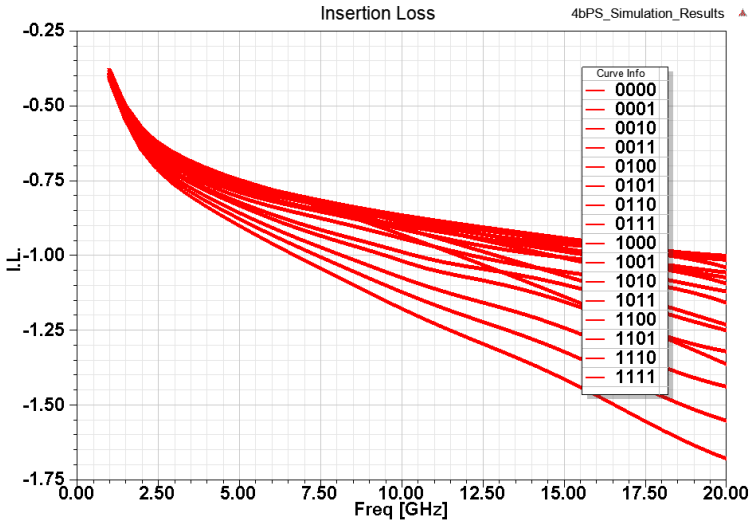


Fig 3.11: HFSS electromagnetic simulation results of the insertion loss for all the 16 states of the proposed phase shifter. The results show good RF performance in terms of the insertion loss and insertion loss variation

The relatively low insertion loss variation across all the 16 states of the proposed phase shifter is confirmed by the measurement results in Fig 3.12.

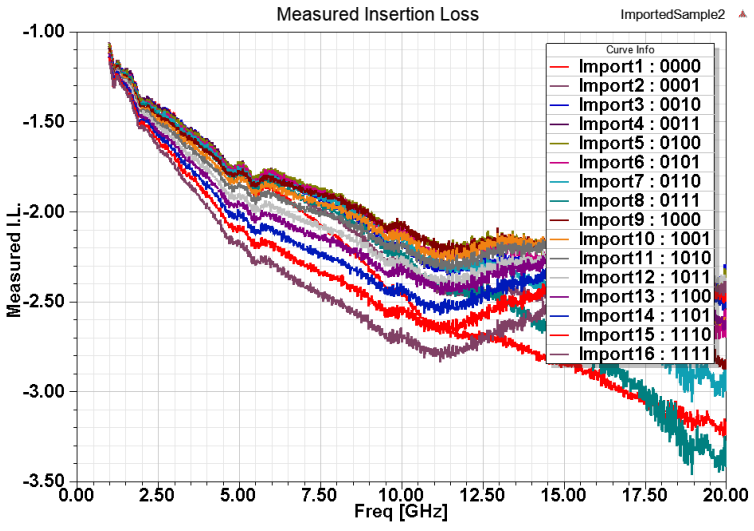


Fig 3.12: The measured insertion loss for all the 16 states of the proposed phase shifter

In addition, the phase curve in Fig 3.13 shows that a maximum phase change of ~ 50º is achievable. If the capacitive loading per bit is increased, the phase change can be made considerably larger. Actually, the measurement results of the phase variation in Fig 3.14 demonstrate that. The large range of variation is attributed to the thinner thickness of silicon dioxide layers use for the capacitive loading, which takes place mainly in the KOH etch step for finalizing the trench patterning.

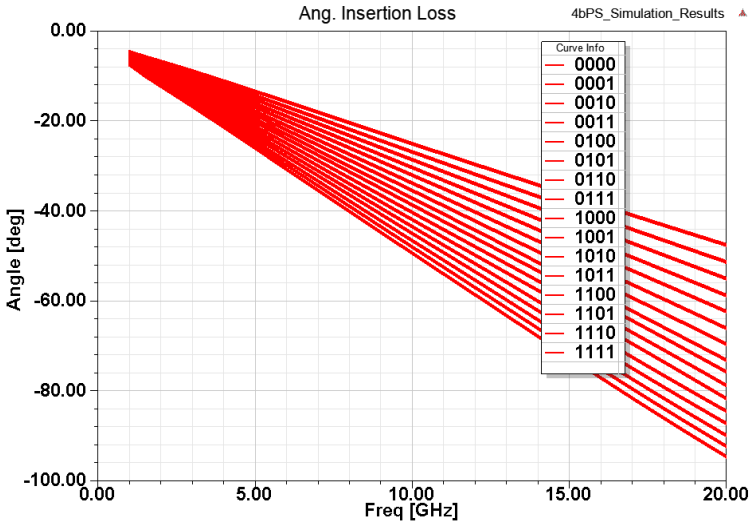


Fig 3.13: HFSS electromagnetic simulation results of the phase variation for all the 16 states of the proposed phase shifter

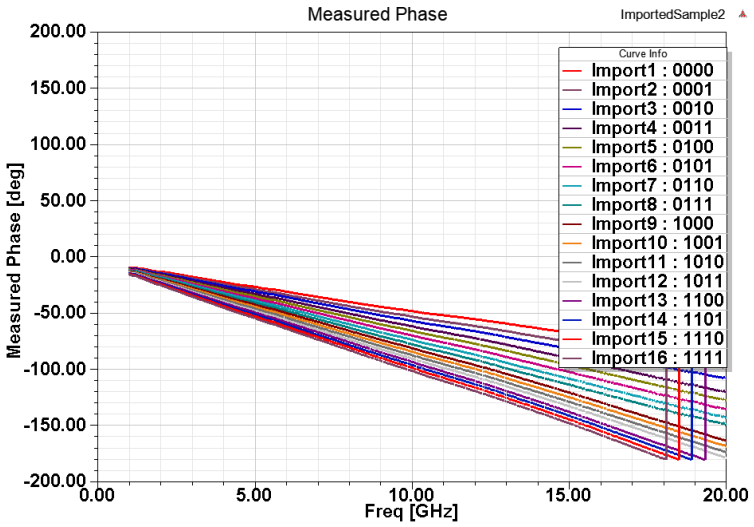


Fig 3.14: Measured results of the phase variation for the 16 different states of the proposed compact phase shifter

3.1.3 CMOS-MEMS W-band Switch

The low capacitance density or capacitance per unit area is suitable for higher frequency applications, for instance, mm-wave frequencies or higher. The structure of a new design of W-band CMOS-MEMS switch is presented in Fig 3.15. The actuation electrode is used to collapse the clamped-free plate such that the series capacitance between the two ports increases to several pF, which can be treated as a perfect short circuit at such high frequencies. Applying a voltage to the holding electrode can be used in the down-state / ON-state to hold the beam if the actuation signal is to be removed. The CPW signal line and ground plane are suspended on top of a 60µm silicon trench, and they are mechanically reinforced by the thick oxide layers in the BEOL stack.

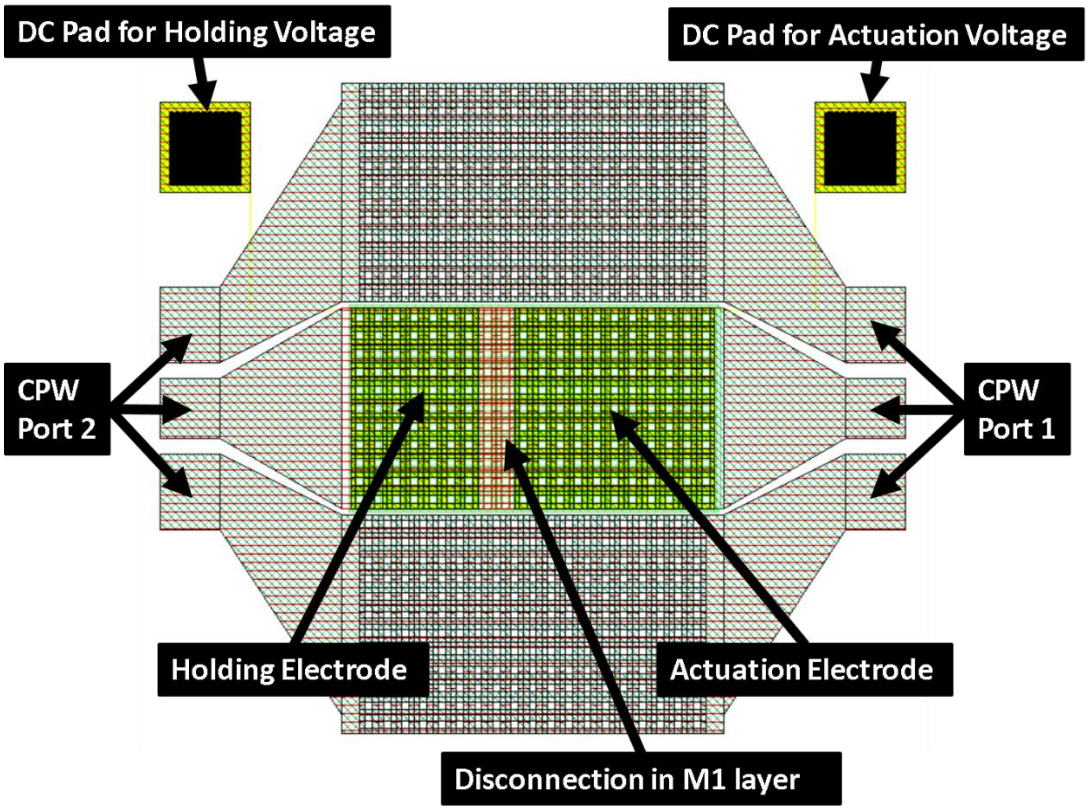


Fig 3.15: An exact layout of the proposed W-band CMOS-MEMS switch design

The SEM pictures of the different post-processing conditions of the switches confirm that the warpage of the same design / layout can be controlled depending on the level of isolation required in the OFF state (see Fig 3.16). Depending on the tip deflection, or the warping profile of the structural layer, good isolation can be obtained, as shown in Fig 3.17. This simulation result assumed a tip deflection of more than 200µm.

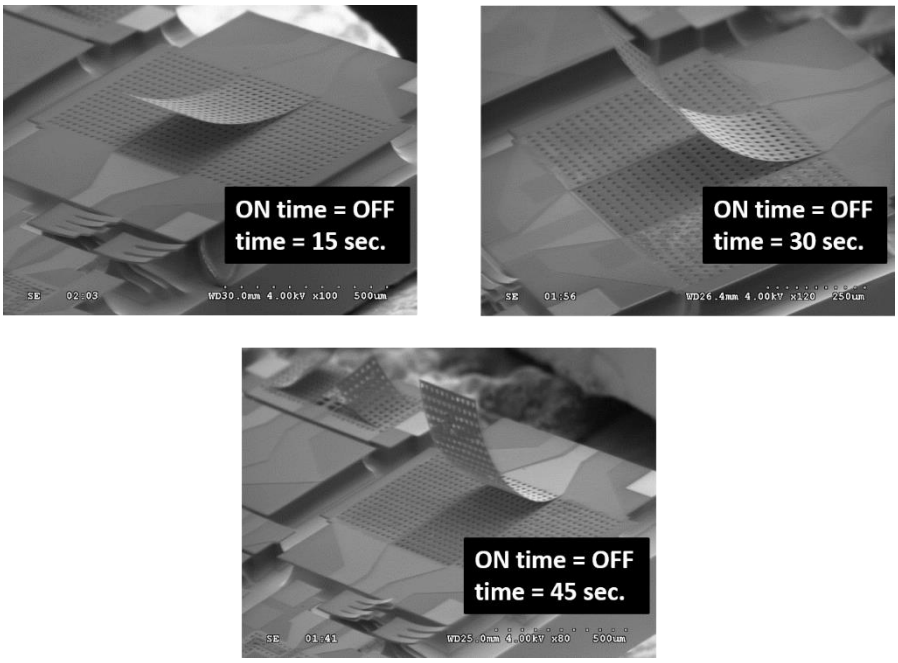


Fig 3.16: SEM pictures of the fabricated W-band switches using different non-cryogenic post-processing conditions for the sake of controlling the warpage at the expense of the increase in actuation voltage

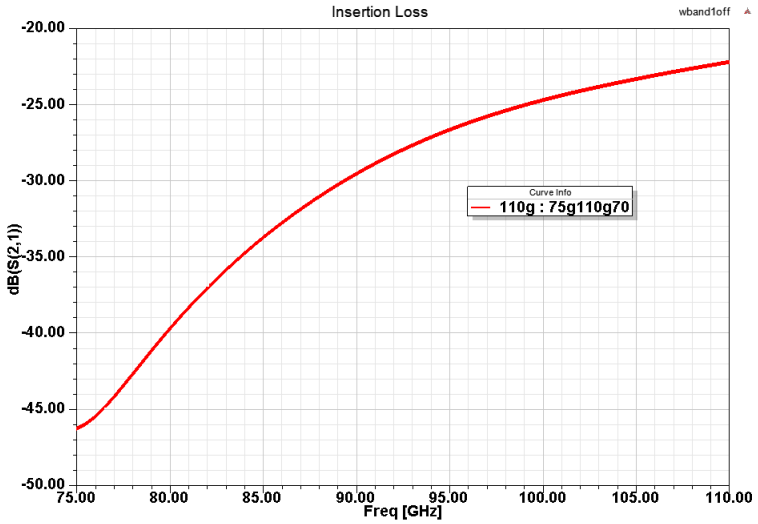


Fig 3.17: HFSS electromagnetic simulation results of the return loss and insertion loss of the proposed W-band switch in the OFF state

3.1.4 Capacitive Switching with Improved Capacitance Density

For capacitive switching at lower RF frequencies, it is possible to improve the capacitance density by using arrays of W via / pillars between the M1 and M3 layers. There are two main approaches that can be followed. In the first approach, the W pillars attached to M1 and M3 layers can be misaligned like the upper and lower tooth of an alligator. Depending on the interleaving distances, the capacitance density can be increased by more than a factor of 10 as compared to the maximum attainable density published [63, 64]. This is illustrated in Fig 3.18and Fig 3.19. Following this approach would require controlled oxide etching around the via features.

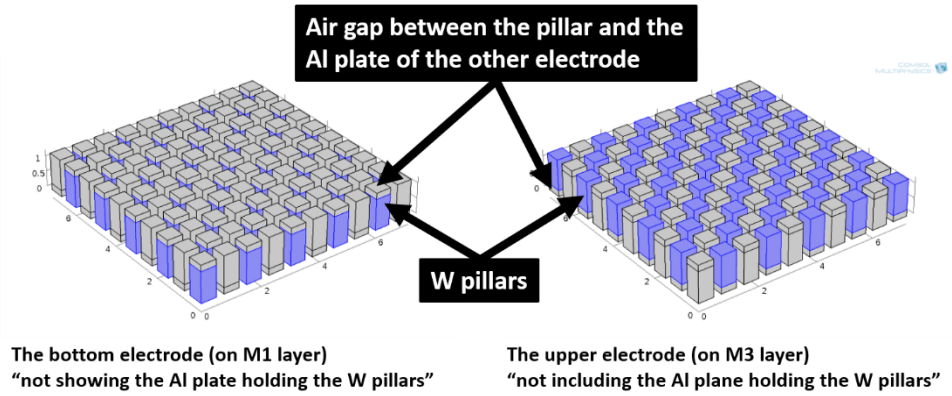


Fig 3.18: : COMSOL 3D illustration of the interleaving of the upper and lower W pillars for the sake of increasing the maximum attainable capacitance density published [63, 64]

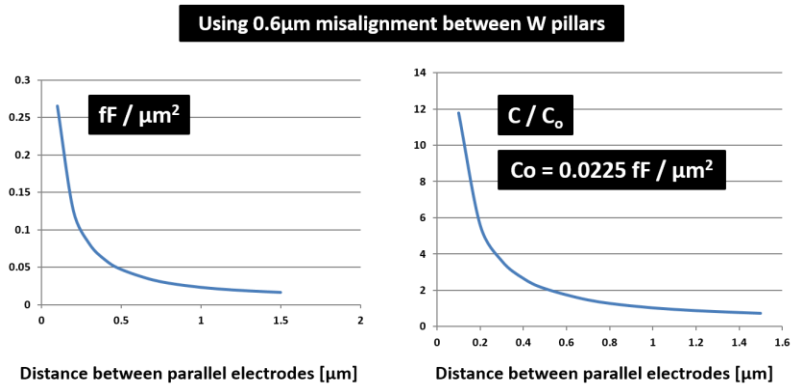


Fig 3.19: Simulation results of the interleaving of the upper and lower W pillars for the sake of increasing the maximum attainable capacitance density published [63, 64]

On the other hand, instead of interleaving the W pillars connected to the M1 and M3 layers, it is possible to have them perfectly aligned such that the distance between the electrodes for at least 25% of the area is the minimum possible. This technique is easier, but it would not yield much increase in the capacitance density as compared to the first approach. This is illustrated in Fig 3.20 and Fig 3.21.

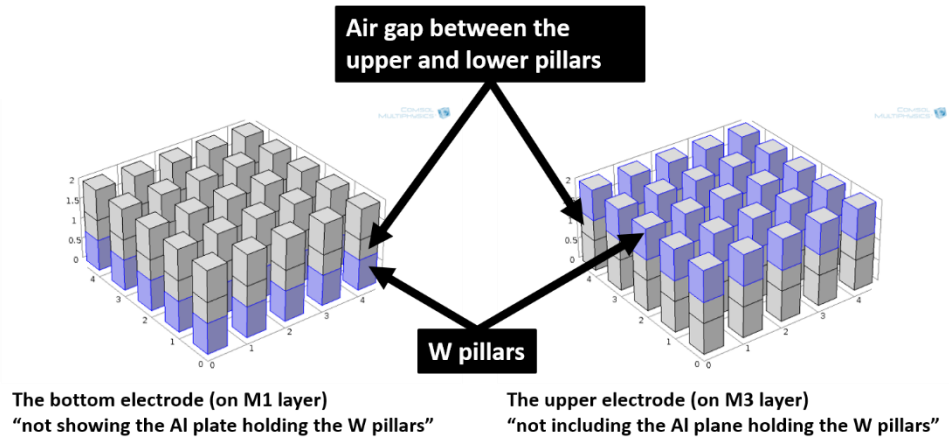


Fig 3.20: COMSOL 3D illustration of the alignment of the upper and lower W pillars for the sake of increasing the maximum attainable capacitance density published [63, 64]

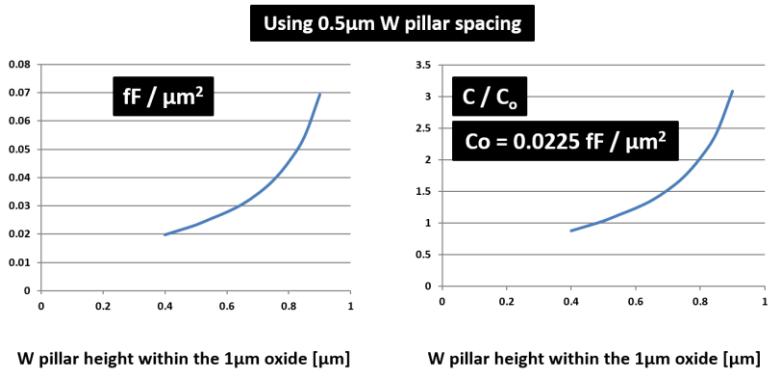


Fig 3.21: Simulation results of the alignment of the upper and lower W pillars for the sake of increasing the maximum attainable capacitance density published [63, 64]

As a result of the increase in capacitance density, significantly improved capacitive switching results at lower RF frequencies can be obtained. Two capacitive switch SPST designs are shown in Fig 3.22 and Fig 3.23. The fabrication results for the switch in Fig 3.23 are provided in the SEM pictures in Fig 3.24. The design in Fig 3.22 is identical to the design in the SEM pictures of Fig 3.6. It is an enhanced version of the

design published in [64] where the capacitance density is increased significantly by virtue of interleaving the W pillars with 0.6µm misalignment.

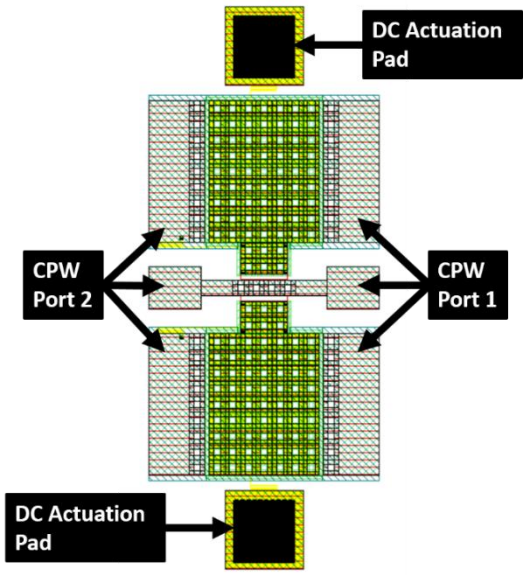


Fig 3.22: An improved design of the capacitive SPST switch in [64] where the capacitance density is increased using the first approach, i.e. interleaving the W pillars

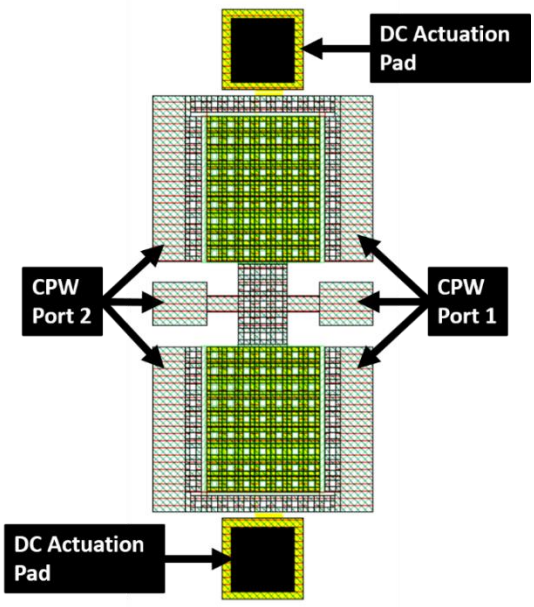


Fig 3.23: An alternative design to the capacitive SPST switch in [64] where the capacitance density is increased using the second approach, i.e. alignment of W pillars

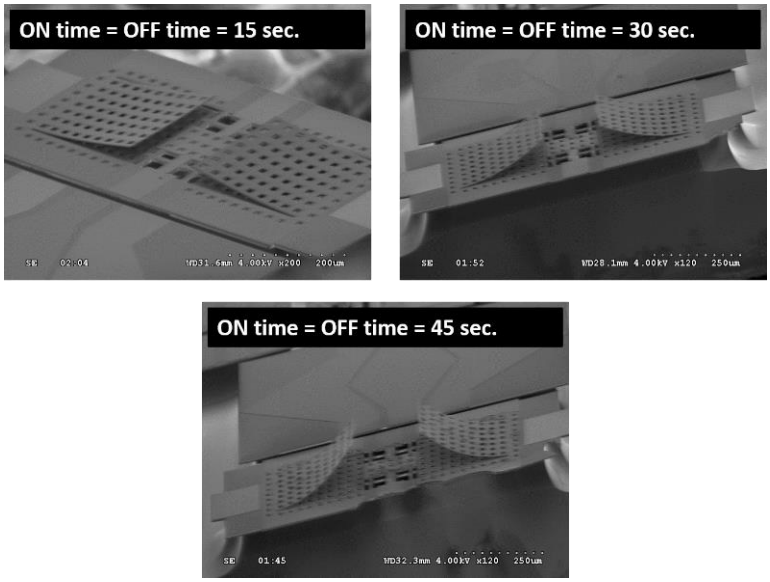


Fig 3.24: SEM of the fabricated devices following the alternative design to the capacitive SPST switch in [64] where the capacitance density is increased using the second approach, i.e. alignment of W pillars. Three levels of warpage are shown where the up-state capacitance is further suppressed in order to increase the capacitance ratio

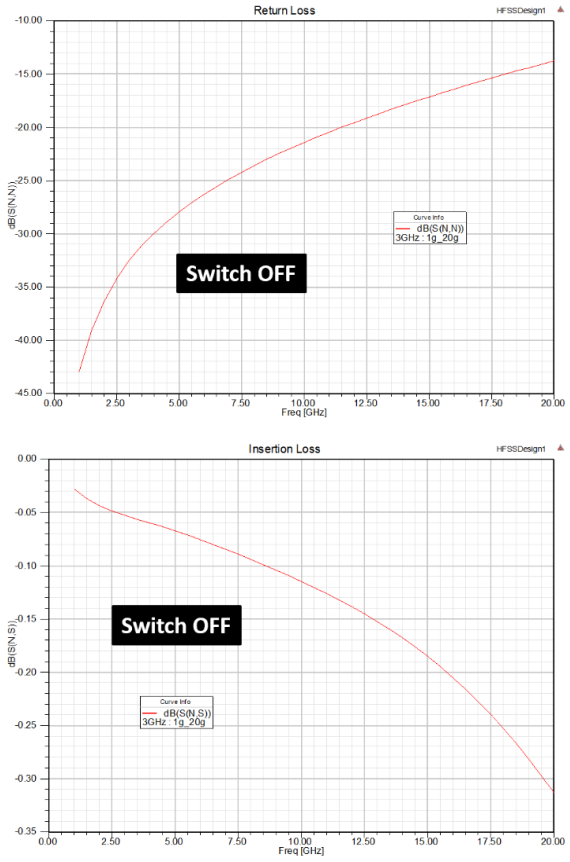


Fig 3.25: HFSS simulated results of the alternative design to the capacitive SPST switch in [64] for the OFF state

The HFSS electromagnetic simulation results for the return loss and insertion loss of the alternative design demonstrated in Fig 3.22 and Fig 3.23 are displayed in Fig 3.25 and Fig 3.26 for the OFF and ON states, respectively.

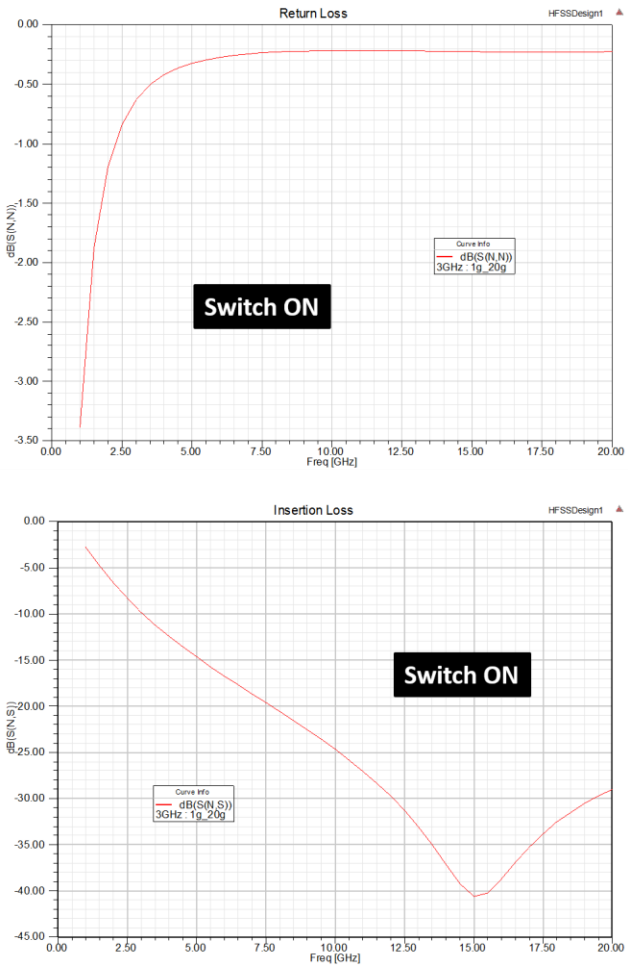


Fig 3.26: HFSS simulated results of the alternative design to the capacitive SPST switch in [64] for the ON state

3.2 Design and Fabrication of CMOS-MEMS Metal-Contact Switches

Besides the capability for building capacitive switches, it is possible to sacrifice a portion or all of the silicon dioxide between the metal layers in order to perform metal-metal contacts for switching. That is the focus of this section, and a compact multi-port switch is presented in terms of the design and fabrication.

3.2.1 Compact CMOS-MEMS T-Switch

T-type, C-type and R-type switches are required for different applications in satellite communications such as the redundancy switch matrices allowing a signal to be re-routed from a malfunctioning or damaged component to a replacement or spare component [78, 80]. However, T-type switches provide the largest count of degrees of freedom in terms of signal routing paths if they are compared with R-type and C-type switches [32]. Also, implementing such switches in standard CMOS technology not only allows monolithic integration, but also it allows further compaction to their sizes as well as reproducibility of RF performance of the individual switches in a large matrix, which is due to the high reliability and maturity of standard CMOS processes. In this section, a relatively compact T-type switch design is proposed and analyzed in terms of its design and simulated RF performance, fabrication process and initial fabrication results.

The design of the RF MEMS T-type switch presented employs a two-fold symmetric architecture with the four CPW ports at 90º. In order to implement the switch in the back end of line (BEOL) of the CMOS 0.35µm chip as proposed, metal1 (M1) and metal3 (M3) layers are used to build the circuit and MEMS switches, where M3 is part of the structural layer. The layers for metal2 (M2) and metal4 (M4) are used mainly as sacrificial layers. Fig 3.27 shows the HFSS 3D of the proposed T-type switch.

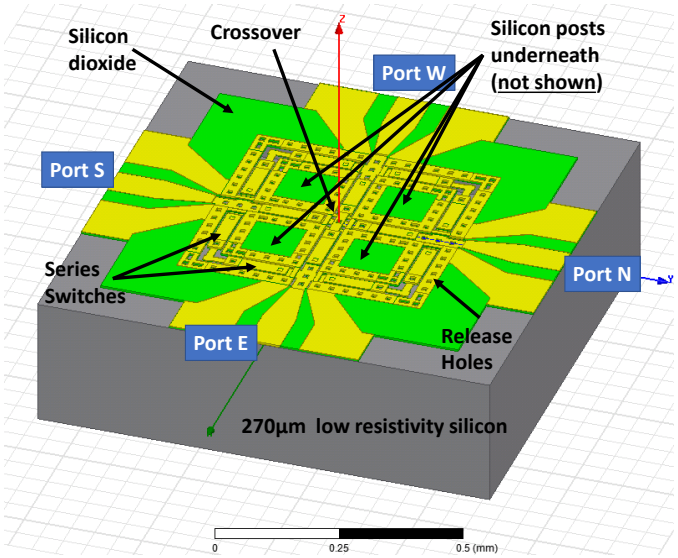


Fig 3.27: HFSS 3D view of the proposed RF MEMS compact T-type switch using a mask-less post-processing of standard CMOS 0.35µm chips. The DC actuation pads and biasing resistors are not shown. The core size of the circuit is ~ 0.5 mm

In each of the four 90º and two 180º signal paths, there are two clamped-free (i.e. cantilever-type) series switches that are actuated electrostatically in order to connect the corresponding two ports, or two pairs.

The contact can be made using an array of one 0.5µm W via on a contact area of Al (in M1) or two opposing W arrays of via12 and via23 features. Employing arrays helps improve the contact resistance, provided that an adequate contact force is applied, which would lead to a suitable contact pressure. In addition, using two contact series switches in each signal path helps improve significantly the isolation when the switches are OFF and it simplifies the matching of the different ports when one of the three paths (per port) is ON.

Fig 3.28 provides a top view from the actual layout of the fabricated switch where only M1-M3, Poly2 and Contact layers are shown in order to clarify the details of the design. The relatively very narrow biasing resistors (> 20KΩ) are built using the Poly2 layer. The series switches are each 130µm long and 30µm wide, where the suspended length is 100µm and the gap from ground planes is 5µm. The width of all the CPW line is 100µm. The signal crossover is made with 20µm wide lines, and all air bridges are 10µm wide. Such dimensions are all for a silicon trench that is 60µm deep.

Moreover, the bottom electrodes of individual switches are connected to the RF ground planes through the highly resistive Poly2 bias resistors mentioned above. That allows for having only one DC actuation pad connected to both anchors of the suspended switches, which can switch ON a desired signal path or switch state (using two pads).

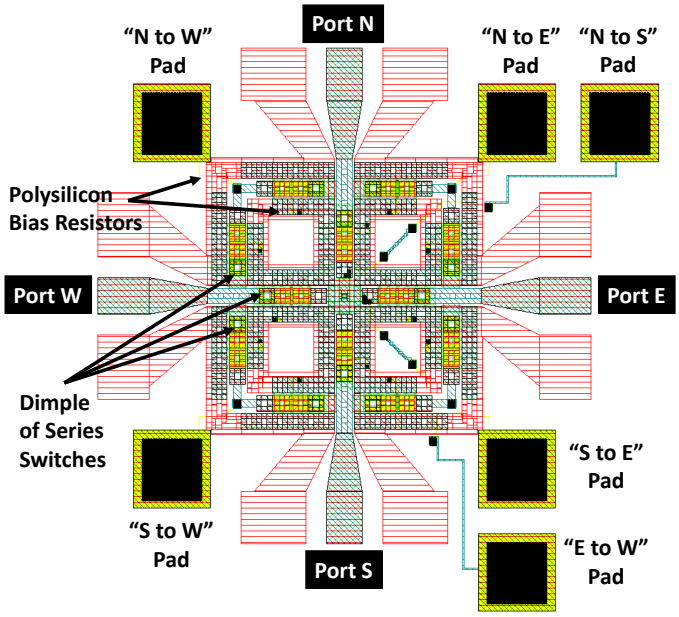


Fig 3.28: Top view of the T-type switch design from its layout showing the 150µm actuation pads for the six different signal routing paths. The layers for via12, via23 and M4 hard mask are not shown

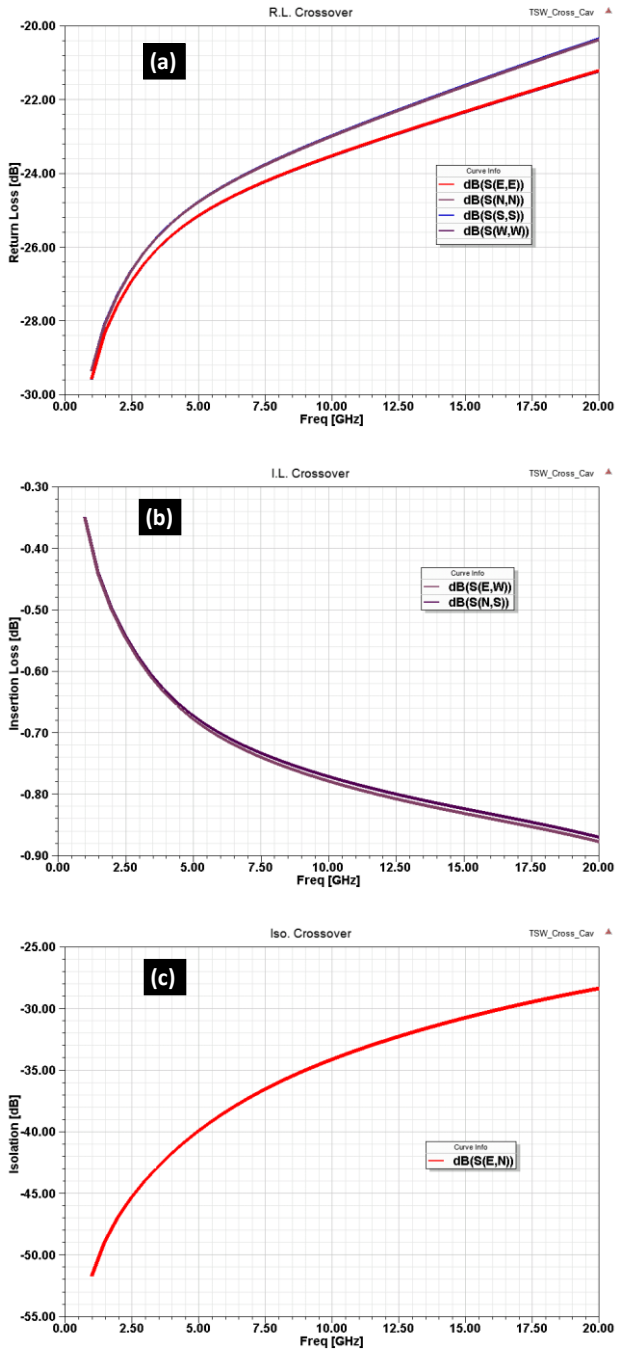


Fig 3.29: HFSS simulation results for 180° signal paths (i.e. when the signal crossover is needed); (a) return loss in dB; (b) insertion loss in dB; (c) isolation in dB; the simulated results are for a 60μm deep silicon trench

The RF design and simulation of the T-type switch was performed in HFSS, where the different states of the proposed design were tested. For the signal crossover states, i.e. "N to S" and "E to W", Fig 3.29a shows the return loss revealing good matching by virtue of the deep silicon trench. Moreover, the insertion loss in Fig 3.29b confirms the exigent need for deep silicon etching. If there is no trench in silicon, the return loss

would be ~ 10dB, and the insertion loss would increase by at least 2dB. In Fig 3.29c, the isolation between both paths is relatively very good. It is worth noting here that the overlap between the crossover lines is 20µm x 20µm. On the other hand, for the 90º signal paths (i.e. C-type operation), e.g. "N to E" and "S to W", Fig 3.30a shows the return loss of two connected ports, which again reveals good matching up to 20GHz. Besides, Fig 3.30b demonstrates the insertion loss for the 90º signal routing. It is clear that the design for the crossover and C-type states is close, which is a desirable feature [32, 79]. The results for isolation are almost the same like those in Fig 3.29c; hence, they are not shown.

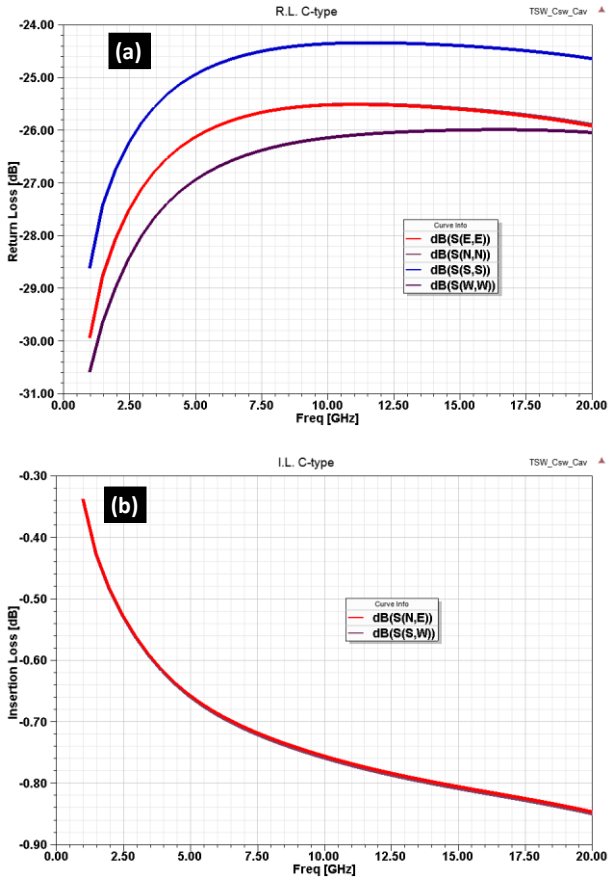


Fig 3.30: HFSS simulation results for the 90º paths (i.e. C-type operation); (a) return loss in dB; (b) insertion loss in dB; the simulated results are for a 60µm deep silicon trench

The fabrication of the T-type switch utilizes a mask-less post-processing of CMOS 0.35µm. The process is significantly different from previously reported post-processing procedures. Indeed, the design and architecture of the proposed MEMS switch impose such difference. The cross-sections of one of the signal paths in Fig 3.31 illustrate the main post-processing steps.

Fig 3.31a shows the as-received chip with a given relative alignment of the different metal layers on top of the CMOS active parts (not shown). M4 serves primarily as a hard mask for the subsequent reactive ion etching (RIE) of all exposed oxide areas on the chip as well as the deep reactive ion etching (DRIE) - or RIE for isotropic etching - of the low-resistivity silicon in the substrate. Fig 3.31b and Fig 3.31c show the cross-sections for such steps. In order not to change the as-received stresses in the different layers while being able to process the chips in reasonable time, dry etching with cryogenic cooling is adopted, which is a main deviation from previously reported processes. Also, creating the trench in the low-resistivity silicon substrate (Fig 3.31c) under the CPW lines is very critical for the overall RF performance of such devices. This is the main reason for the distribution of release holes (Fig 3.27 and Fig 3.28) across all the CPW sections of the switch, as they allow etching the oxide stack down to silicon. Accordingly, such holes allow attacking of the lossy silicon near the CPW lines, which improves matching of the different signal paths as well as the overall insertion loss.

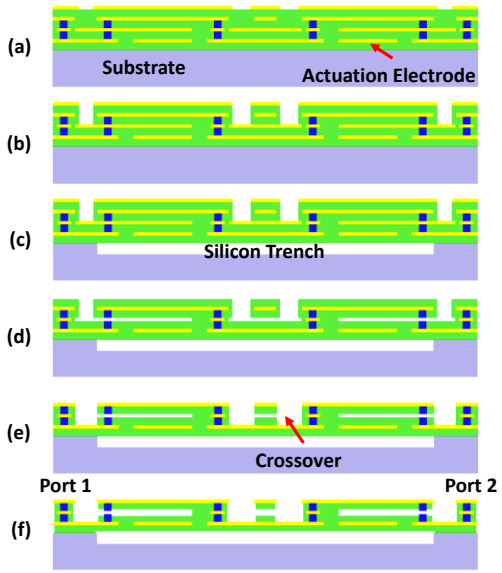


Fig 3.31: The CMOS mask-less post-processing procedure using the relative alignment of metal layers in the standard CMOS 0.35µm BEOL; (a) As-received chip; (b) after dry etching of oxide; (c) after dry etching of low resistivity silicon or trench creation; (d) after wet etching of the sacrificial M2 and M4 layers as well as the adhesion layer; (e) after the dry etching of oxide on top of M3 / M1 probing areas and released switches; (f) after thinning the oxide layer around the tungsten pillars or contact dimples. For the sake of simplicity, the details of release holes are not shown

In Fig 3.31d, the primary sacrificial layer M2 is stripped through wet etching in Al etchant (PAN) along with M4 as hard mask. M4 cannot be protected in this procedure. The thin adhesion layers of TiN are wet etched in H_2O_2. At this stage of processing, an important deviation from previously reported processes takes place. In fact, after the stripping of Al and TiN, wet etching of the resulting silicon pits using KOH [63, 64]

cannot be performed due to the presence of W vias to be employed in the contacts of the series switches as proposed. Another main difference is that KOH etching would help thin the oxide layers around M1 and M3 layers, which would then allow for higher capacitance densities for the sake of building better capacitive switches. However, it does not make any difference for the contact-type switch presented, and, as a result, there is no gain from using such wet etching.

Instead of using KOH for finalizing the shape of the trench, a combination of 40-50µm DRIE (using standard Bosch process) and dry isotropic etching steps of 10-15µm have been employed successfully leading to the removal of most of the silicon near CPW lines. More isotropic etching could be done, but it would at the cost of increasing the size of probing pads, which would harm the compaction process. A critical point drier (CPD) system is then used to properly dry the chips. In Fig 3.31e, another major deviation has been introduced, where the second RIE of the remaining oxide layer on top of M3 structural layers and probing pads is etched while allowing the released oxide-metal-oxide beams to heat up, i.e. without cryogenic cooling, in a controlled way depending primarily on the ON and OFF times of the plasma ignition. This way, the warpage of the release structures and the deflection of the contact dimples in the OFF state as well as the required pull-in voltage for the switches can be well-controlled for the same design/layout.

Fig 3.31f demonstrates the need for etching the oxide layers attached to M1 and M3 in order to uncover W vias partially. That is a second wet etching step that can be performed using silicon dioxide etchants optimized for minimal attack of the Al metallization. Products such as Silox Vapox III or AlPAD Etch 639 from Transene Inc. are good candidates [69]. Both have been used for the post-processing reported in this work, and their etching performance has been highly comparable. Finally, a second CPD step is required in order to finalize the fabrication.

Fig 3.32 displays a DC contact resistance test switch after undergoing the first dry etching steps while keeping the cryogenic cooling then the wet release steps. It is clear that the inherent or as-received stresses in the different layers including those of released beams do not provide a desirable warpage.

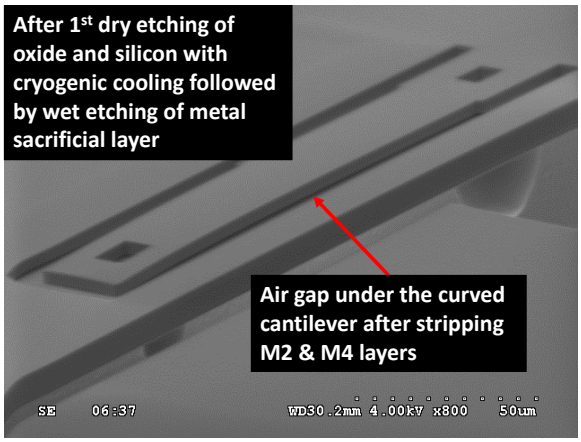
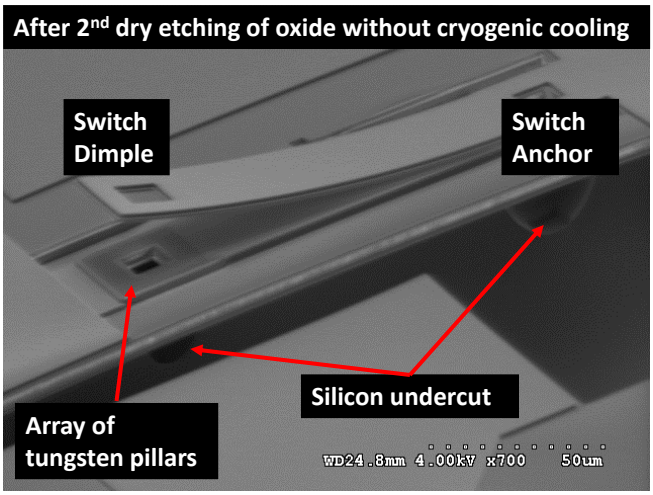


Fig 3.32: SEM picture demonstrates an identical test switching element (for DC contact resistance characterization) after the first dry etching steps with the cryogenic cooling, wet release of switch and drying using CPD

As previously discussed, if the oxide-metal-oxide released micro-beam encounters a controlled over-heating, the desired warpage of the individual switches can be reliably obtained. Fig 3.33 proves that where the same DC contact resistance test switch was subjected to second dry etching step of oxide with the same plasma power level, but relatively long bombardment time. On the other hand, when same switches were subjected to a significantly shorter intervals of bombardment, the overall warpage is obviously less, which would help reduce the pull-in voltage of the zipper actuator made by the fabrication process.

(a)



(b)

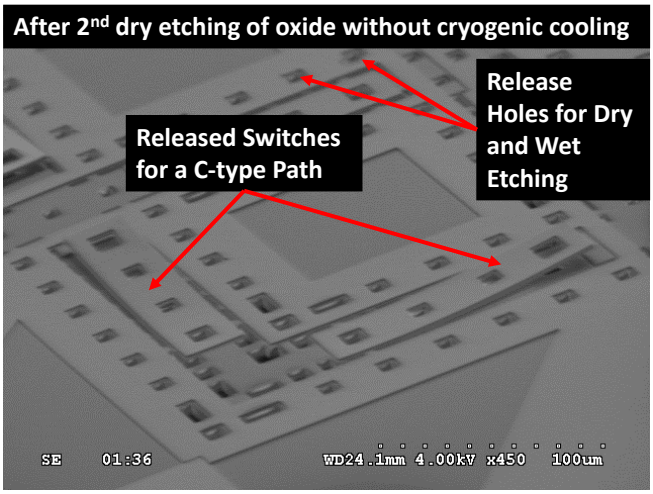


Fig 3.33: SEM picture of different switching elements after the second dry etching of oxide without the cryogenic cooling; (a) DC contact resistance test switch with a relatively long plasma bombardment duration, and (b) C-type path switches of the T-switch cell with a moderate duration for plasma bombardment, which results in less membrane warping and lower actuation voltage

Chapter 4: MEMS Switches Using MetalMUMPs Process

In this chapter, RF MEMS switches using the standard MetalMUMPs process by MEMSCAP Inc. are presented in terms of the design, fabrication and measurement results. The fabricated devices employ mainly electrothermal actuation, but they can still be considered for low DC power applications by virtue of the adopted mechanical latching or reconfigurability of individual switching cells. The devices presented include a compact discrete capacitor bank with the core as a latching conventional comb-drive varactor for high power applications, a novel low-frequency high-power 3-bit capacitor bank, and a rotor-based 4-port RF switch design that is capable of switching two signal lines simultaneously with opposite states or can be configured as Single Port Two Throws (SP2T) switch.

4.1 Advantages of Using MetalMUMPs Process

In order to build RF MEMS switches, it is generally possible to rely on a standard multi-user MEMS process such as PolyMUMPs, MetalMUMPs, SUMMIT, etc. For low frequency and high power applications, it is desirable to use thick metal layers taking into consideration the large skin depth. The operation under high RF power would necessitate careful considerations for the immunity towards self-actuation, which can be employed instead of a holding electrostatic actuation voltage, as highlighted briefly in chapter 3.

By considering the need for a relatively high restoring force (in the mN range), especially for the ON state at high RF power operation (10-30W) and for hot switching, the MetalMUMPs process appears to be the most attractive option. The process features only one metal layer made of 20μm thick electroplated nickel [70]. That makes the realization of RF circuits limited to some extent due to the signal routing constraints to one level / plane. However, it should be noted that wire bonding and even flip-chip techniques can join more than one chip together, and, accordingly, solve the problem.

Moreover, the process has been introduced (historically) in order to realize a high-reliability thermally actuated switch. As a result, the implementation of the in-plane electrostatic actuation would require large footprints of devices for the sake of obtaining enough actuation forces. That is certainly due to the minimum feature size allowed for the metal layer as well as the limited thickness [70]. The thick nickel layer would not allow an efficient out-of-plane electrostatic actuation, even if there is a second metal layer to employ for switching and / or building the circuit. It should be noted though that thermal actuation mechanism should not be considered negatively in terms of its high actuation power consumption due to the feasibility of mechanical latching and reconfigurability. It is worth noting that the electrostatic actuation is still a possible option, though it is inefficient in terms of force level due to the minimum feature size allowed.

4.2 MetalMUMPs Devices Fabricated

In this section, some of the MetalMUMPs devices fabricated and released are demonstrated. An overview of the MetalMUMPs process layers is provided in the cross-sections displayed in Fig 4.1 [70].

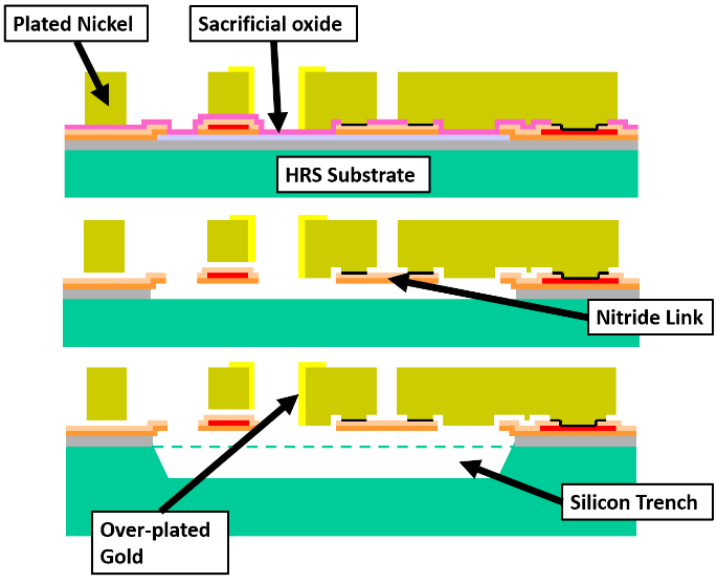


Fig 4.1: Cross-sections of the MetalMUMPs process by MEMSCAP Inc. [70]

Briefly, the substrate used is made of high resistivity silicon (HRS), with an electrical resistivity higher than 4KΩcm. That is required for the operation of low-loss RF devices. Otherwise, deep trenching in silicon would be required as discussed earlier in chapter three. Two sacrificial oxide layers (pink and purple in the figure) are employed in the process, and only one resistive layer of polysilicon can be used for implementing micro-heaters for thermal actuation as well as possibly biasing resistors for RF switching. The gold over-plating up to 2µm can typically be used in between nickel features for the sake of realizing direct gold-to-gold switch contacts and for reducing the in-plane air gaps for electrostatic actuation. The device release is finalized by a step of bulk micromachining to a trench depth of 25µm using KOH.

4.2.1 Compact RF MEMS Discrete Capacitor Bank

The first device to present in this chapter is a reconfigurable compact discrete capacitor bank that is shown in Fig 4.2 using an exact layout of a fabricated device. Depending on the maximum possible displacement or the stroke of the thermal actuator, the number of states and, accordingly, the number of equivalent bits can be determined. The undocked (i.e. initial) state is considered the first state.

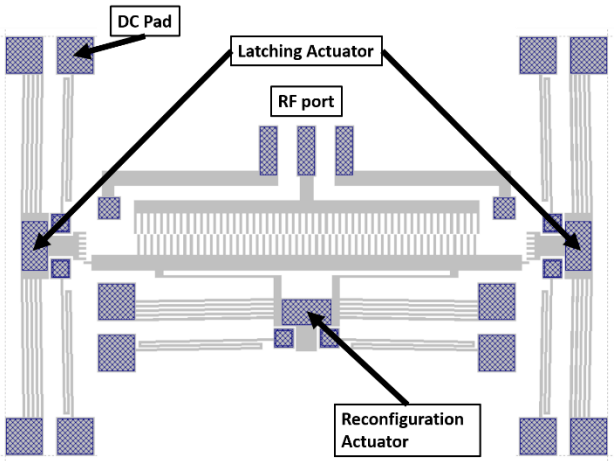


Fig 4.2: Layout of the MetalMUMPs compact capacitor bank of the second generation

The capacitance is formed by the overlap distance in the comb drive actuator. In order to perform the reconfiguration of the capacitor, the latching actuators are first activated by the required DC input power such that the latching or docking tips in the vernier shown in Fig 4.3 are pulled away from the pivot on the movable electrode of the comb drive fingers. The same voltage and current can be used for all the latching actuators. This is not the case for the reconfiguration actuation. More input power would be required for higher states where more displacement is needed. After setting the displacement of the reconfiguration actuator, the latching actuators are released in order to dock the movable side of the comb drive and get it locked firmly at a specific position.

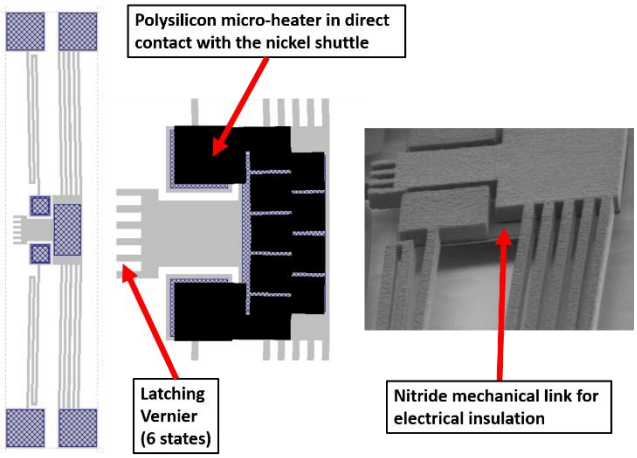


Fig 4.3: Layout of the latching electrothermal actuator showing the polysilicon micro-heater

A closer look at the docking mechanism as illustrated in Fig 4.4 suggests a minimum initial reconfiguration displacement of 25µm and a corresponding minimum reconfiguration step (i.e. from a docked state to the following / higher docking state) of 18µm. That is imposed by the minimum feature size and minimum spacing design rules of the process, which is 8µm for both cases, and by assuming a minimum practical docking clearance of 1µm. It is worth noting that using the gold over-plating layer can help achieve good contact resistance between the latching actuator and the movable comb drive electrode, but it cannot help with reducing the minimum requirement for the reconfiguration step.

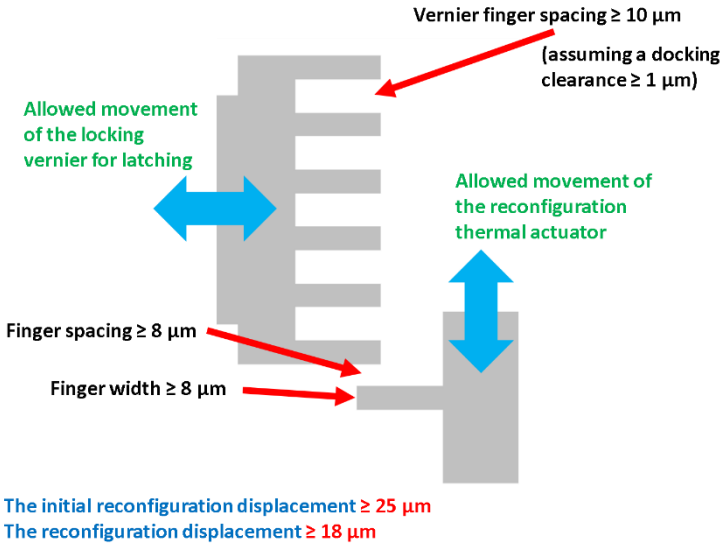


Fig 4.4: The latching or docking mechanism and typical geometrical dimensions imposed by the intra-layer design rules for the metal layer in the MetalMUMPs process

As a result, the displacement required for the second docked state, or the third state, would be more than or equal to 43µm, and the displacement required for the following state would be 61µm. As mentioned above, there is accordingly an exigent need to design a thermal actuator with a relatively large stroke in order to abide to the reconfiguration restrictions imposed by the design rules. For a relatively high numbers of equivalent bits (i.e. $n \geq 3$), actuator displacements up to 100µm would be required.

There are two actuation schemes that can be used for the operation of the electrothermal actuator in air as well as in vacuum. This is explained in Fig 4.5. In scheme 1, the polysilicon micro-heater in direct contact with the suspended nickel shuttle (through the thin silicon nitride layer) can be employed. Typical resistance of the micro-heater would be few 100Ω. The corresponding measured power consumption in air is around 200mW [71, 74-76] for a displacement exceeding 30µm. Following scheme 1, the operation of the thermal

actuator then is based on two sets of 2-domain physics. Solving for two coupled domains in Multiphysics problems is generally more accurate than solving for three coupled domains as in the case of scheme 2.

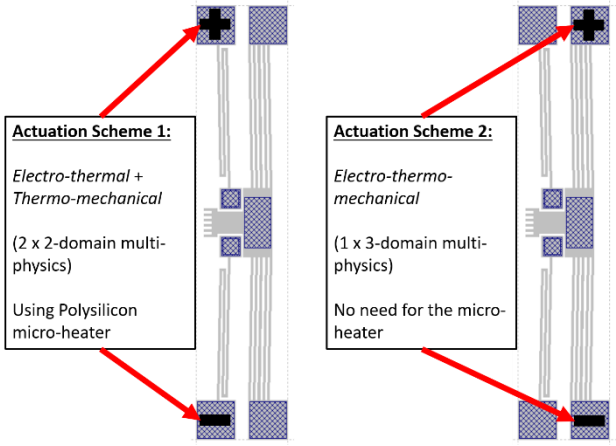


Fig 4.5: Two different actuation schemes are possible for the electrothermal actuators

The COMSOL thermo-mechanical analysis of only the thermal actuator in scheme 1 helps study and tune the performance of thermal actuator for both schemes in view of the different design specifications and constraints including the required reasonable footprint (i.e. compaction) and acceptable electrical lumped model, especially the inductance for the sake of controlling the self-resonance frequency (SRF) of the net capacitance.

In order to maximize the displacement of the thermal actuator at a given input thermal power, the slanting offset of the chevron beam is to be generally close or almost equal to the width of the chevron beams. This is considered for all the chevron thermal actuators in this chapter. Depending on the length of the chevron beams on each side of the shuttle mass (that is 100µm x 200µm), the optimal slanting angle can then be calculated. For the sake of compaction, beam lengths up to 600µm are possible.

In addition, the Joule heating mechanism in the micro-heater that is in direct contact with the shuttle mass (with the 0.35µm thick LPCVD silicon nitride) provides the input thermal power to the thermal actuator, thus acting as the source of the thermal energy. The substrate acts as heat sink at room temperature as well as the anchored pads (typically 100-150µm in size, and $\geq$ 60µm by the design rules). If the pads are probed or wire-bonded to another platform, they should accordingly be modeled as heat sinks at room temperature independent of their sizes.

Considering an input thermal current from the micro-heater, increasing the overall thermal resistance of the chevron beams would help increase the temperature difference between the shuttle mass temperature (that is the maximum temperature in both schemes, considering the symmetry) and the room temperature at the

heat sinks. The heat flux to the ambient air can be neglected, which is valid to an acceptable extent for the operation under vacuum or in relatively low pressure such as being packaged [95].

Adopting narrow and long chevron beams for the thermal actuator would help increase the overall thermal resistance significantly and increase the deflection for a given input thermal current. However, that would result in a significant increase in the equivalent inductance of the chevron beams and decrease in the capacitor's SRF. A compromise should be made between the thermomechanical and RF performances. In addition, lowering the maximum stress encountered in the metal beams is important for the sake of extending the lifetime and reliability of the thermal actuator. For reliable switches based on thick plated metals such as Au and Ni, the literature to keep the maximum stress below 50-100MPa [9].

For a relatively compact design and acceptable RF performance, few to several 8µm-wide chevron beams can be used. Fig 4.6 displays the COMSOL thermomechanical simulation results that demonstrate the dependence of the thermal actuation distance on the input thermal power considering several different configurations assuming three to seven chevron beams on each side of the shuttle mass. The increase of the number of beams results in a decrease of the thermal resistance, which decreases the temperature drop across the chevron actuator and, accordingly, decreases the thermal expansion component due to such temperature difference across the chevron beams.

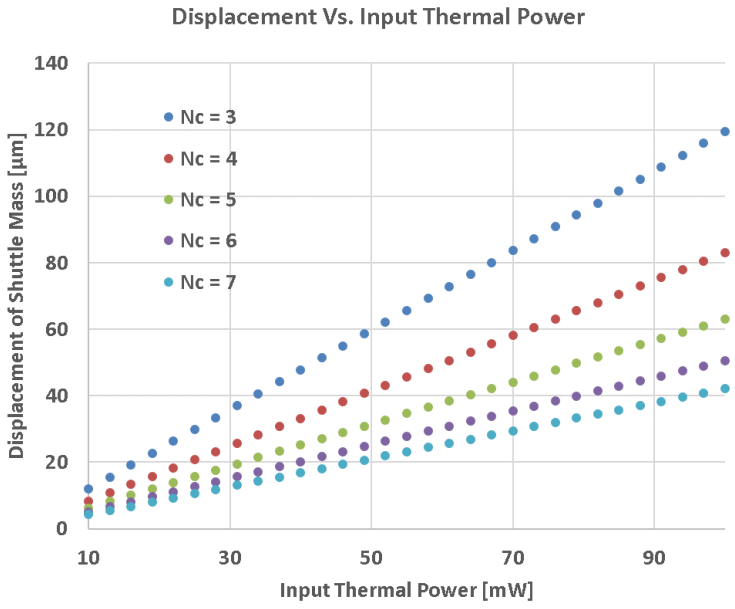


Fig 4.6: COMSOL thermomechanical simulation results of the thermal actuator showing the displacement versus the thermal input power to the shuttle mass (provided by the Joule Heating mechanism taking place in the micro-heater)

This can be further investigated and confirmed by looking at the curve for the dependence of the maximum temperature (i.e. the temperature of the actuator's shuttle) on the input thermal power that is displayed in Fig 4.7. Reducing the number of chevron beams from seven to three results in increasing the temperature of the shuttle mass by ~ 400℃ at the same input power level.

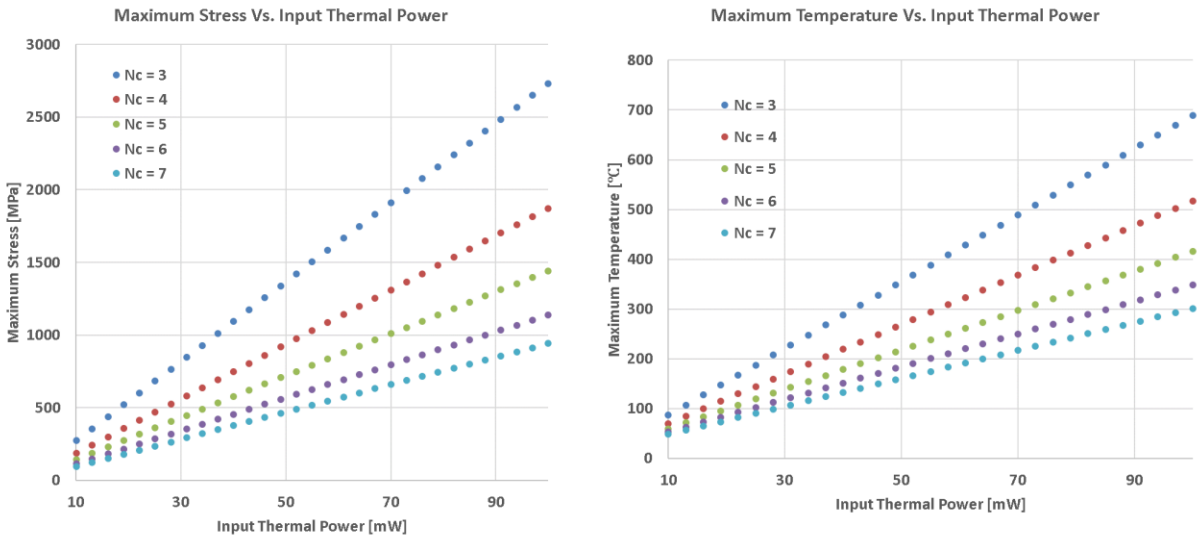


Fig 4.7: COMSOL thermomechanical simulation results of the thermal actuator showing the maximum stress and maximum temperature versus the thermal input power to the shuttle mass (provided by the Joule Heating mechanism taking place in the micro-heater)

There are two possible RF configurations for the circuit of the switched reconfigurable capacitor. This is illustrated in Fig 4.8 and Fig 4.9. The drawback of the first configuration is the dependence of the RF performance of the reconfigurable capacitor on the equivalent lumped elements corresponding to the flexures holding the movable side of the comb drive. In the figures, the gold wire bonding employed represents the second metal layer needed by the circuit. Using wire bonding is generally inevitable if the RF circuits are to be implemented in MetalMUMPs, and it has been one of the main drawbacks of using such process, especially for larger circuits where there are more chances for the need to de-embed the wire bonds.

Following the second configuration, the RF performance can be independent of the geometry or mechanical design of the flexure. This allows optimizing as much as needed the mechanical latching mechanism while obtaining higher SRF or less overall equivalent inductance of the micromechanical components. It is worth noting that a flexure that is considerably less stiff was found to be more compliant experimentally with the docking operation described earlier, thus resulting in less short-circuit failures after the reconfiguration of

the capacitor. However, the stiffness of the flexure is a critical factor determining the immunity of the capacitor to self-actuation under high RF power.

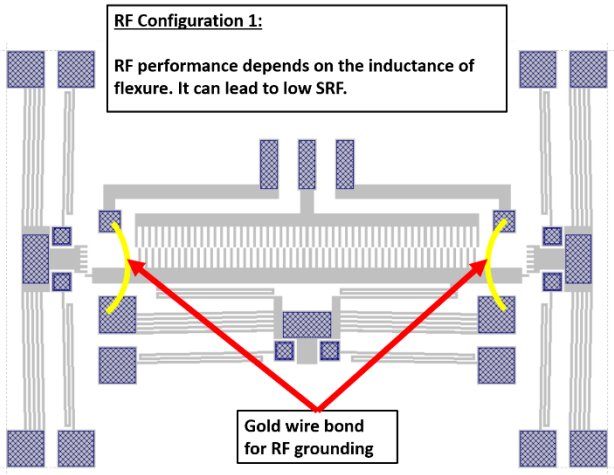


Fig 4.8: First RF configuration of the capacitor's circuit with the RF grounding through the equivalent lumped elements of the actuator flexures in addition to the equivalent lumped elements of the chevron beams

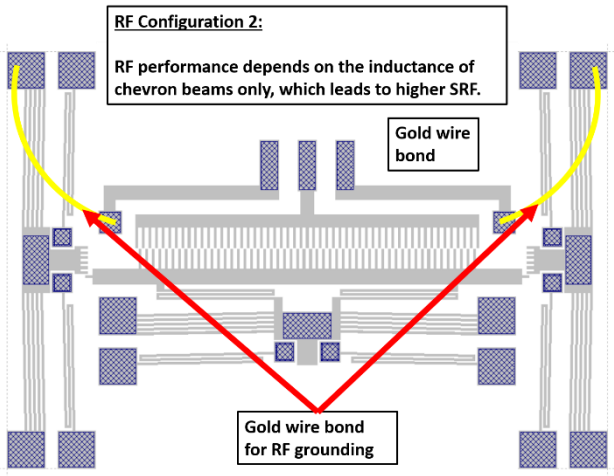


Fig 4.9: Second RF configuration of the capacitor's circuit with the RF grounding through only the equivalent lumped elements of the chevron beams, independent of the flexure design in the actuator

Fig 4.10 displays the 3D structure of the discrete capacitor simulated and analyzed in HFSS taking into consideration the approximate geometry of the ~ 200µm-high and 40µm-thick gold wire bonding that was used experimentally to realize the compact capacitor on the fabricated chip.

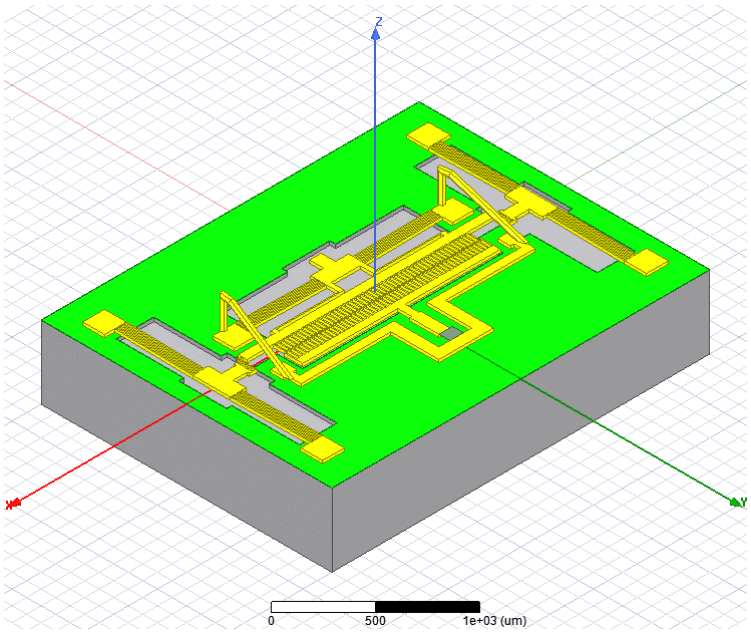


Fig 4.10: HFSS simulated structure following scheme 1 and taking into consideration the required 200µm-high and 40µm-thick gold wire bonding in addition to the 25µm trench in the HRS substrate

The HFSS electromagnetic simulation results of the compact discrete capacitor are shown in Fig 4.11 and Fig 4.12. It can be seen that the SRF values are almost the same for both cases (Fig 4.12). This can be attributed to the relatively small value of capacitance, where the little differences between the equivalent inductances in each case would not result in significant change in the corresponding SRF values.

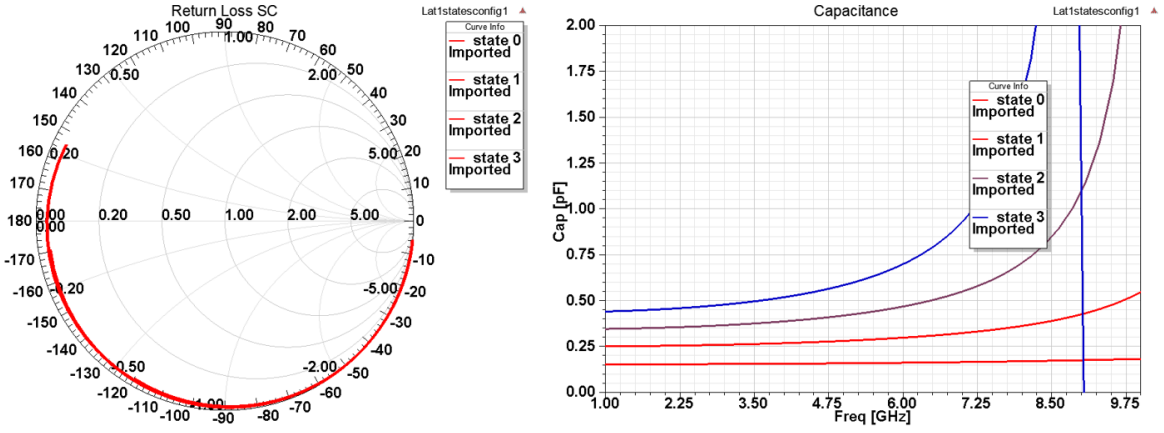


Fig 4.11: HFSS electromagnetic simulation of the first four states of the compact discrete capacitor in Fig 4.10 following the first RF configuration

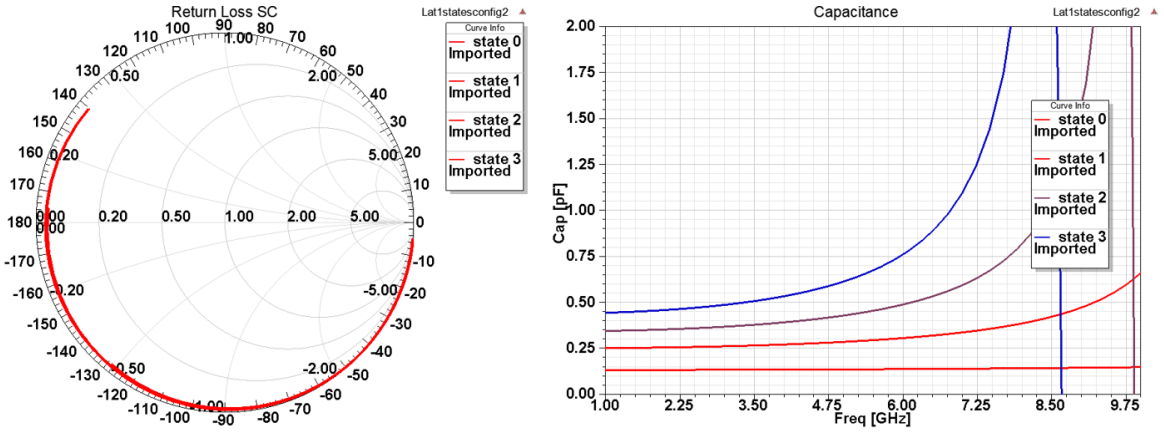


Fig 4.12: HFSS electromagnetic simulation of the first four states of the compact discrete capacitor in Fig 4.10 following the second RF configuration

On the other hand, considering the experimentally more reliable flexure design shown in Fig 4.13, the equivalent inductance is expected to be higher in the first RF configuration. As a result, the SRF value should be significantly lower, which is confirmed by comparing the HFSS electromagnetic simulation results for the extracted capacitance curves in Fig 4.14.

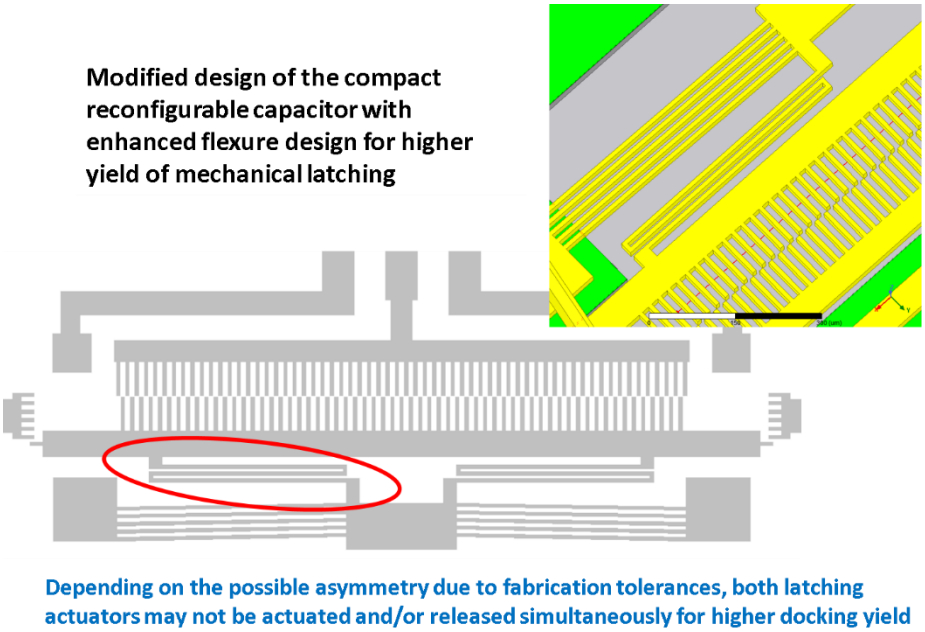


Fig 4.13: An exact layout and 3D structure of a compact reconfigurable capacitor with an improved mechanical design of the flexure leading to higher yield in mechanical latching

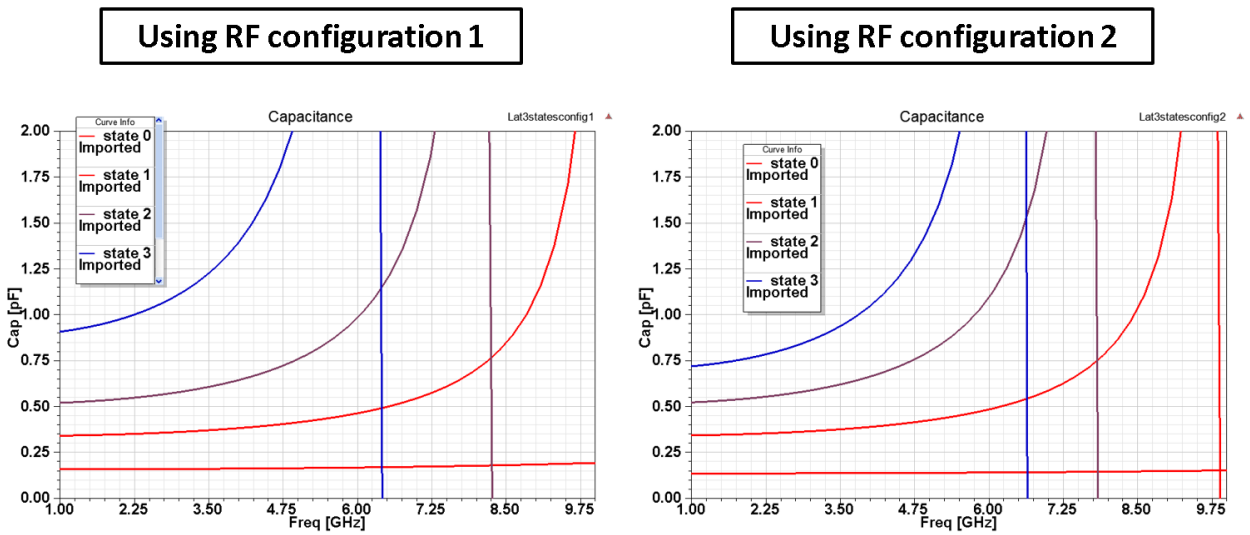


Fig 4.14: HFSS electromagnetic simulation results for the extracted capacitance of the compact design in Fig 4.13. The results of using the first and second RF configurations are compared

Several other flexure designs were also considered for the design and fabrication of the compact discrete capacitors proposed, including the mechanical design in Fig 4.15, which exhibited a comparatively lower latching yield experimentally.

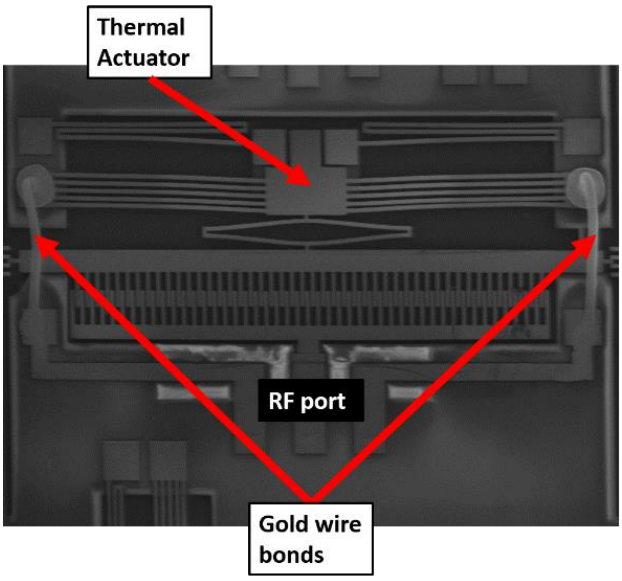


Fig 4.15: SEM of a fabricated five-state compact discrete capacitor of the first generation. The smallest gold wire bonds were 200μm-high on average with the wire diameter of 40μm

The measurement results of the capacitor bank in Fig 4.10 are displayed in Fig 4.16. Due to the warpage issues with the stressed nitride layer as shown in Fig 4.17, the fourth state could not be measured. From the measured states, the SRF value is low ~ 6GHz, but the RF performance is acceptable for the operation up to that frequency.

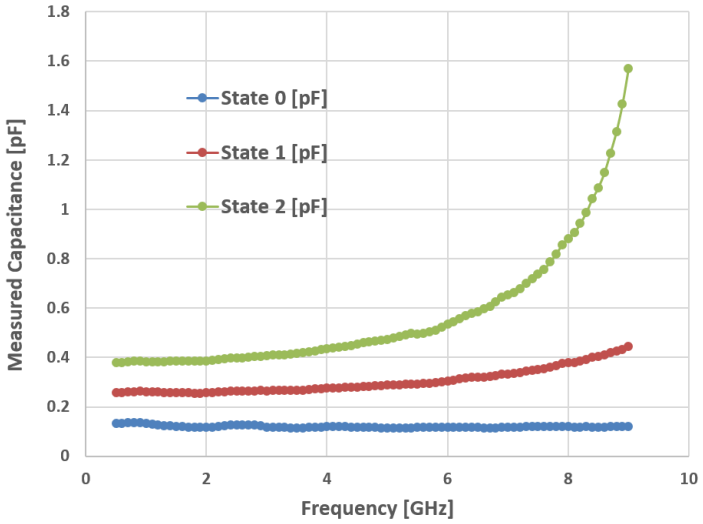


Fig 4.16: Measurement results of a compact capacitor bank of the first generation

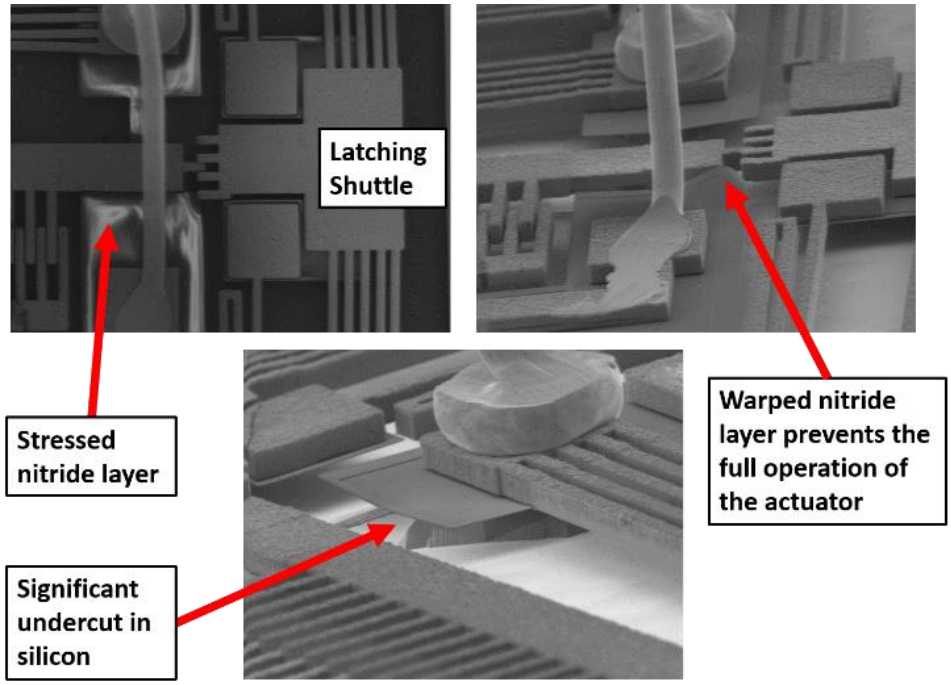


Fig 4.17: SEM pictures showing some of the main issues with the first generation of fabricated compact capacitor banks

As highlighted previously, it is critical to increase the stroke of the thermal actuators. One way to do that is using the novel mechanical displayed in Fig 4.18 where the stroke of the thermal actuator demonstrated earlier can be almost doubled. This is mainly achieved by the proposed cascade of a second stage of chevron thermal actuator that expands relative the position of the driving shuttle of the primary actuator rather than anchors. The overall thermal loading on the micro-heater is expected to be higher, but the proposed cascading provides the large stroke of the actuator without affecting negatively the compaction of the overall device size.

Due to the increased equivalent inductance of the modified thermal actuator, and depending on the maximum reconfigured value of the capacitance, adopting the second RF circuit configuration may ensure a higher SRF and better overall RF performance.

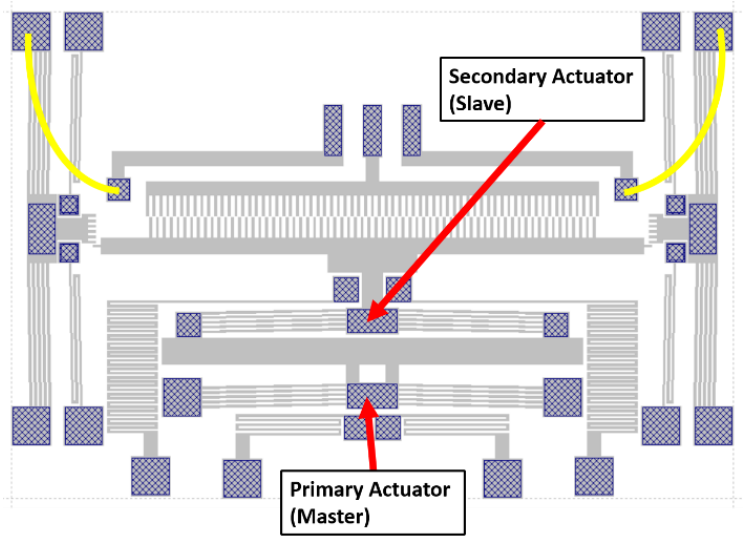


Fig 4.18: Second RF configuration of the capacitor's circuit using a thermal actuator design with enhanced stroke

The first generation of the enhanced thermal actuator design was characterized in terms of the feasibility of using the low stress nitride layer as the mechanical coupling frame, which has not been successful as shown by the SEM pictures in Fig 4.19.

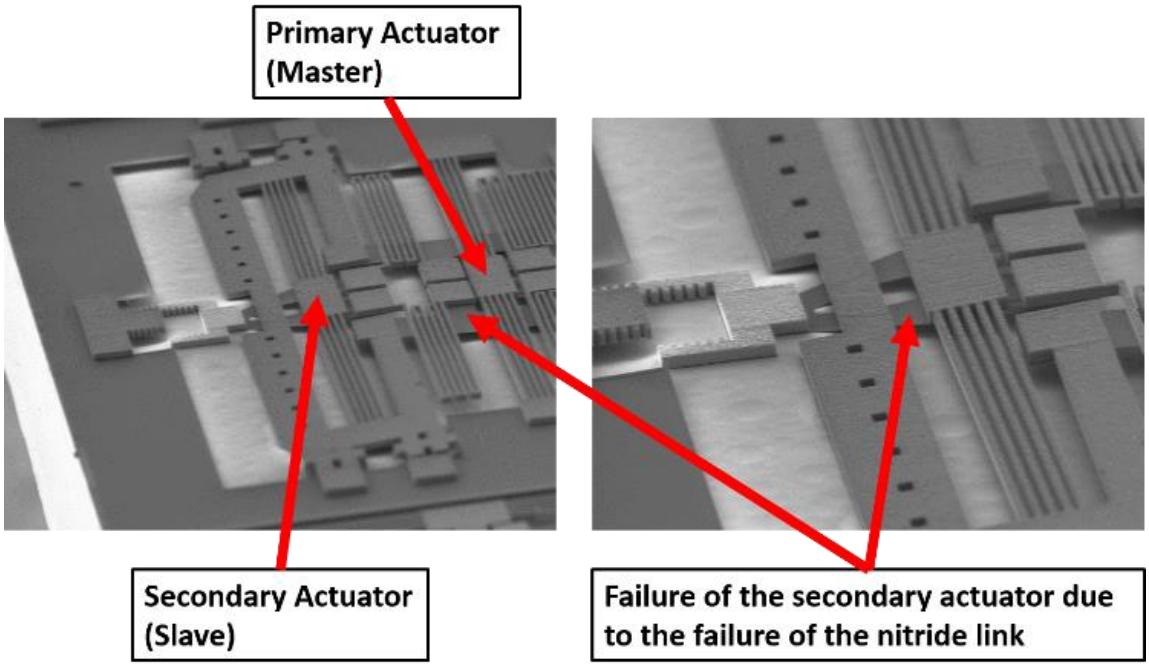


Fig 4.19: SEM pictures of the first generation thermal actuators with enhanced stroke revealing the failure due to the flexible nitride mechanical link

4.2.2 Low-Frequency High-Power 3-Bit Capacitor Bank

The second device considered in this chapter is a 3-bit capacitor bank based on the parallel connection of three comb-drive fixed-value air-filled capacitors that are series-switched for the sake of performing the required engage / disengage operations for the individual capacitors representing each bit. In order to design a binary capacitor bank in this way for a binary operation, if the value of the small capacitance is C_0, the value of the second capacitance should be 2 C_0, the value of the third capacitance should be 4 C_0, the value of the fourth capacitance is to be 8 C_0, etc. The values should take into consideration as well the inevitable parasitic capacitances in the RF circuit. The switching uses mechanical latching as illustrated in Fig 4.20 and Fig 4.21 in order to ensure low reconfiguration or DC power consumption.

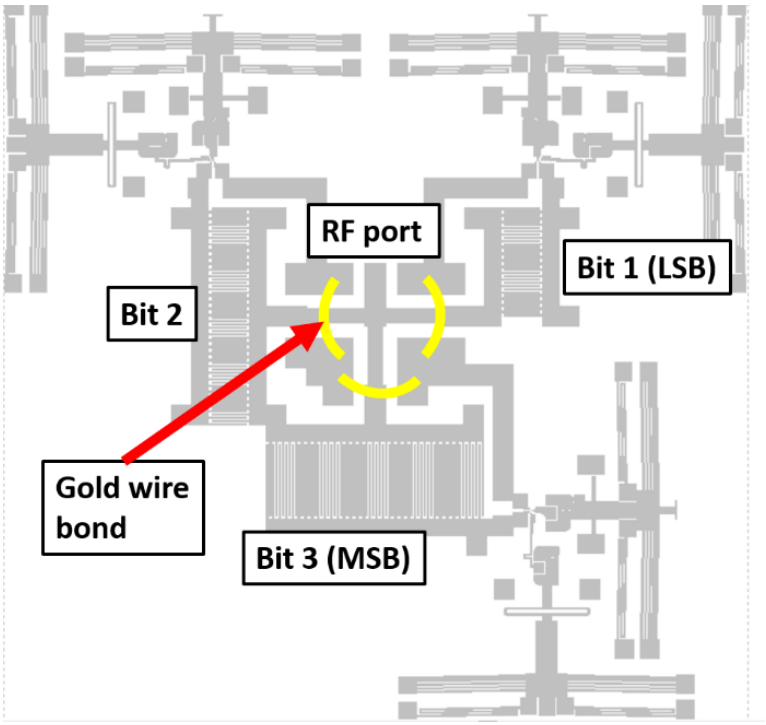


Fig 4.20: An exact layout of the proposed 3-bit capacitor bank for low frequency and high power RF applications

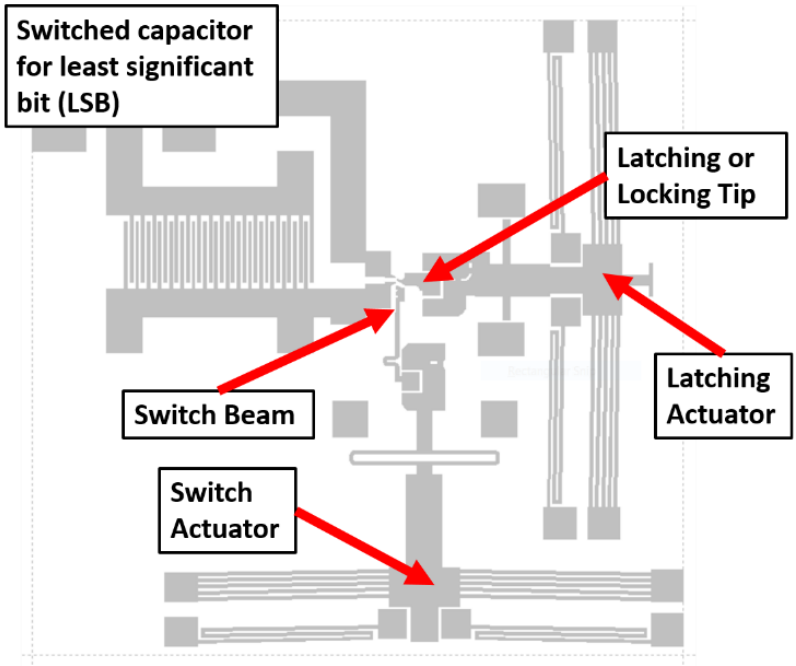


Fig 4.21: An exact layout of a single bit demonstrating the mechanical latching mechanism employed and the structure of the individual bit

The mechanical latching mechanism is further explained by the SEM pictures shown in Fig 4.22, where an insulated latching actuator tip is initially pulled back in order to allow the insulated switch beam to be actuated forward towards the two tips to be connected. The release of the locking tip would keep the switch beam docked for the ON state, and there would no more need for DC biasing the switch beam actuator. Therefore, the overall energy consumption of the reconfiguration is low, and the thermally-reconfigured device does not generally consume energy since it carries zero current for all the time, except during switching or reconfiguration.

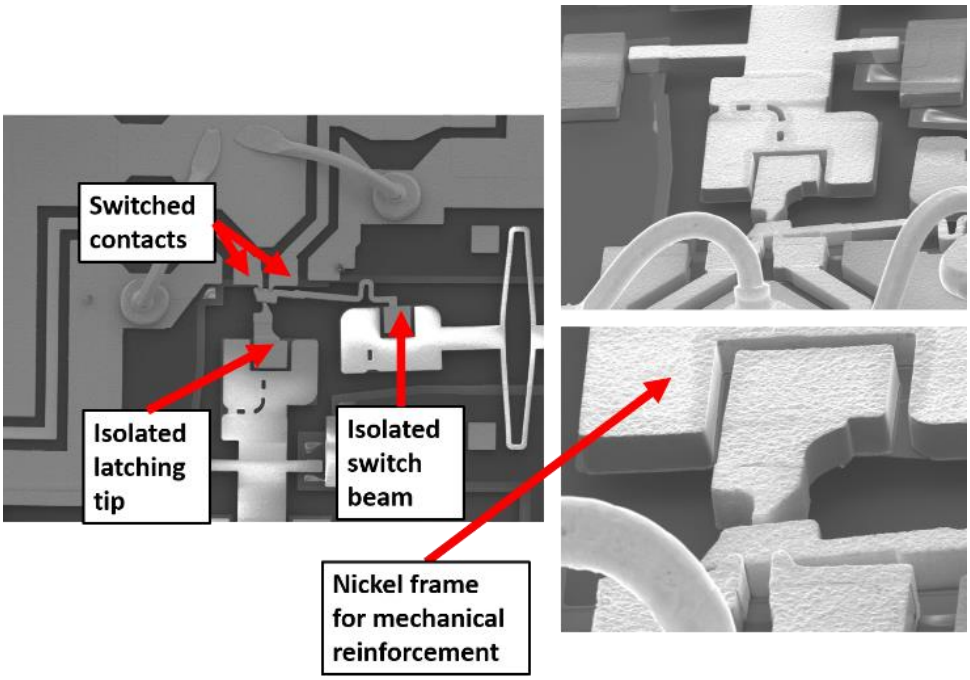


Fig 4.22: SEM pictures of the fabricated thermal actuators showing the mechanical latching mechanism employed [74]

In order to perform the switching and mechanical latching needed, a stroke of up to ~ 40µm is needed, which would correspond to a maximum DC voltage < 13V and current < 20mA in air [74]. In Fig 4.22, a U-shaped nickel mechanical reinforcement structure was used for the low-stress thin nitride links to which the insulated locking tip and switch beams are connected. Otherwise, the insulated structures would experimentally fail and get disconnected from the nitride membrane. In fact, there is still a little warpage that can be observed underneath the locking tip with the presence of the rigid u-shaped nickel frame.

The HFSS electromagnetic simulation results of the extracted capacitance for the three individual bits are shown in Fig 4.23 for the OFF and ON states. When all the bits are engaged (i.e. switched ON), the SRF value is expected to be worse than the SRF value of the largest capacitor, or the most significant bit.

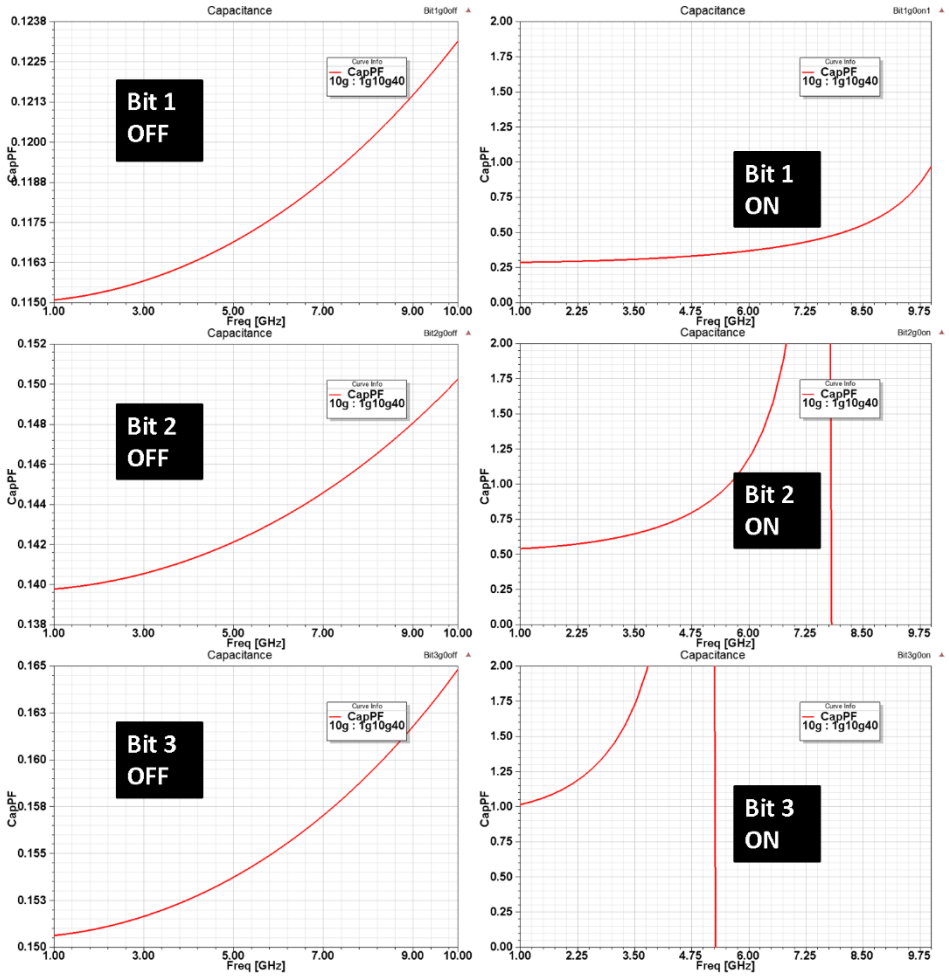


Fig 4.23: HFSS electromagnetic simulation results for the extracted capacitance of the three individual bits that make the capacitor bank

In the figure, it is clear that the off-state capacitance for the individual bits is comparable, which is expected from the disengaged state where the second terminal of each of the three capacitors is physically disconnected from the RF ground plane, and ensuring the smallest possible value for the OFF capacitance. The OFF-state for the capacitor bank is expected to be slightly higher than the sum of all the three OFF-state capacitance values of the individual bits. This is due to the parasitic / unwanted capacitance from the substrate and how the RF circuit of the capacitor is built. It is worth noting here that a significant inductance can be observed for each of the individual capacitors. This is mainly attributed to using the comb-drive actuator design, which is necessary for achieving high capacitance density or capacitance per unit area, based on the design rules for the nickel layer in the MetalMUMPs process. For all the individual bits, the comb-drive finger widths are set to the min. feature size of 8µm.

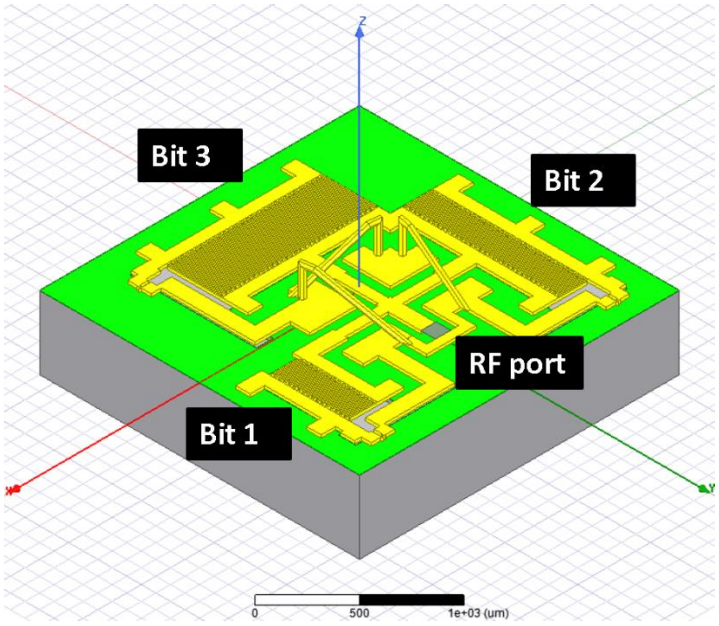


Fig 4.24: The structure of the 3-bit high-power capacitor bank simulated and analyzed in HFSS. The analysis takes into consideration the required 200μm-high and 40μm-thick gold wire bonding in addition to the 25μm trench in the HRS substrate

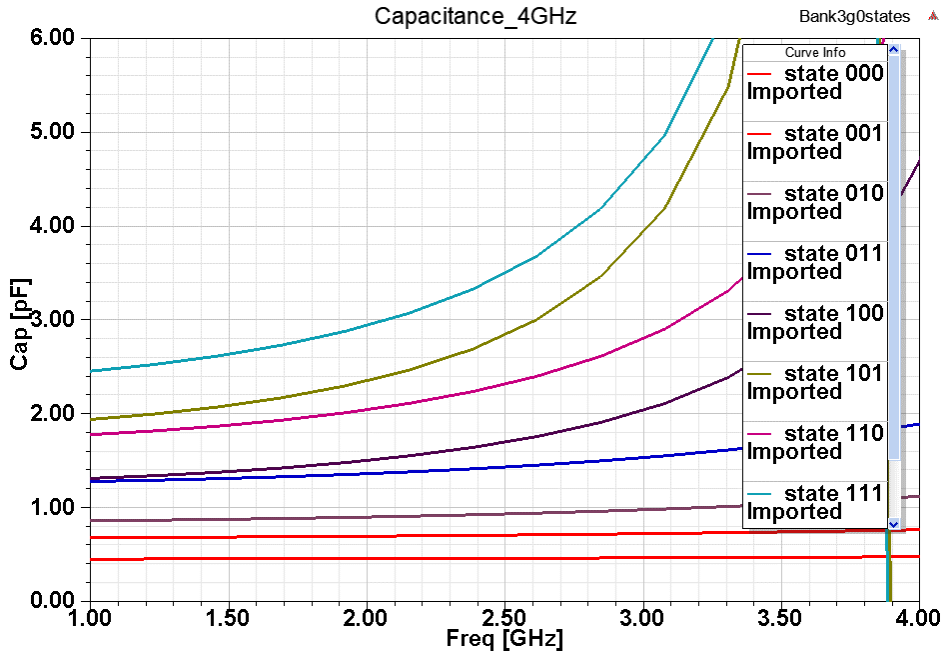


Fig 4.25: HFSS electromagnetic simulation results for the extracted capacitance of the three individual bits that make the capacitor bank

The 3D structure of the proposed 3-bit capacitor bank that was electromagnetically simulated and analyzed in HFSS is demonstrated in Fig 4.24 taking into consideration the extracted geometry of the three 200µm-high and 40µm-thick wire bonds used to connect all the ground terminals of the three individual capacitors. The extracted values of capacitance for the eight different states are provided in Fig 4.25.

In Fig 4.25, it can be observed that the OFF-state capacitance (in the state "000") is comparable to the sum of the three OFF-state capacitances, which reveals that the added parasitic capacitance due to the substrate and wire bonding is negligible. The overall SRF value of the 3-bit capacitor limits its maximum operating frequency to ~ 3GHz, where the net SRF value is dominated by the SRF value of the most significant bit in Fig 4.23. The simulation results and RF performance is further confirmed from the measurement results in Fig 4.26 for all the eight states of the proposed capacitor. In Fig 4.26 and Fig 4.27, the measurement results and the extracted capacitance of the various states are displayed. Significant self-resonance would take place beyond the 3GHz range.

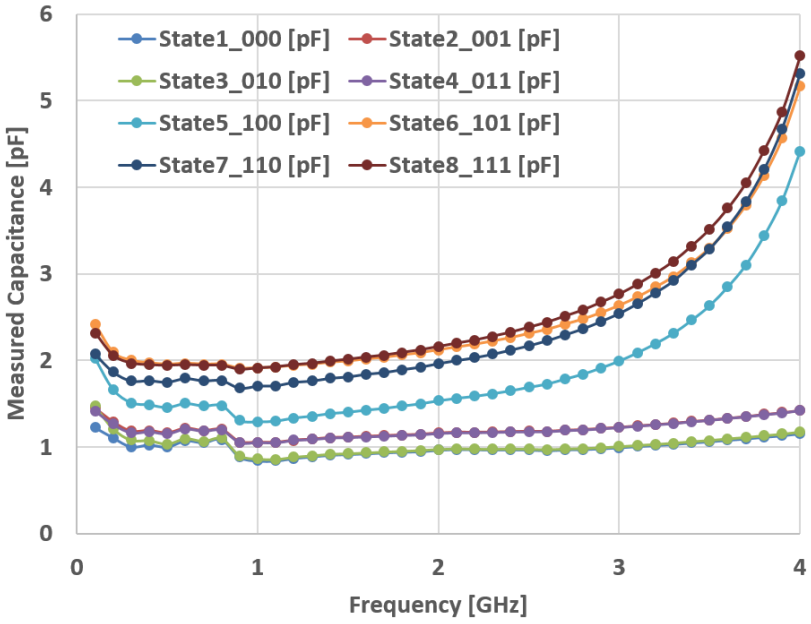


Fig 4.26: Measurement results of the eight different states of the 3-bit capacitor bank

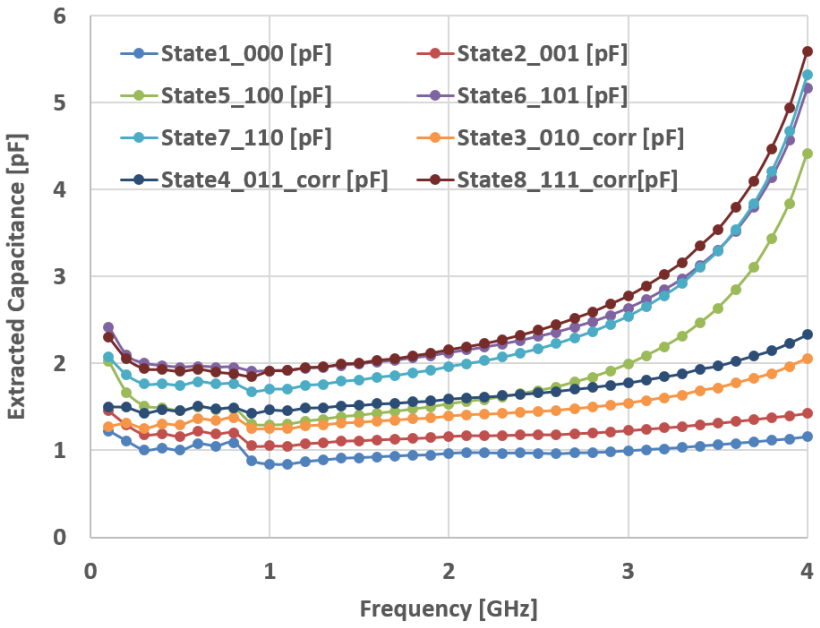


Fig 4.27: Capacitance extracted results of the eight different states of the 3-bit capacitor bank based on the measurement in order to correct for a malfunctioning bit

4.2.3 Rotor-based RF MEMS Switch

In this section, the design of a rotating-beam multi-port switch for high-power RF applications is presented. It is referred to as the rotor-based switch, and it can be operated as SPST switch if only two of the four ports are used. The concept is demonstrated in Fig 4.28 and Fig 4.29 for the first generation of devices. The rotating switch beam is trapped spatially by means of the silicon nitride and nickel layers in order to allow for the geometric confinement of the anchorless structure. Two narrow beams of silicon nitride prevent the suspended beam from falling into the 25µm silicon trench, and the nitride disc to which the central part of the beam is anchored keeps the untethered beam in plane, and prevents it from leaving the wafer surface during the different release steps of the MetalMMUPs chips. The concept of geometric confinement of untethered structures is further exploited in chapter five.

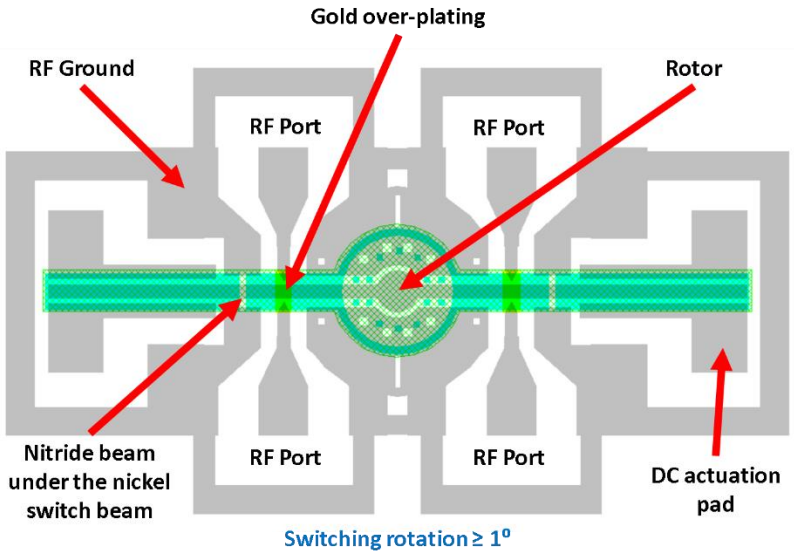


Fig 4.28: An exact layout of the first generation design of the rotor-based switch implemented in the MetalMUMPs process. The nickel beam is supported by two narrow nitride beams in the locations shown. Applying the potential difference diagonally would result in the rotation of the nickel beam such that two ports at a time are diagonally connected

In order to actuate / rotate the electrically floating beam, two actuation electrodes should be diagonally used as shown in Fig 4.29. The capacitive potential divider between the two electrodes would assign a potential to the initially floating beam, and the fact that the two electrodes are on different sides allows for an actuation moment that rotates the beam. The analysis on the electrostatic actuation of anchorless structures is provided in chapter five under the remote electrostatic actuation (REA) section. Using the two electrodes for actuator 1 (in the figure) switches the beam such that ports 1 and 3 are connected whereas ports 2 and 4 are disconnected. The electrodes forming actuator 2 can be used then to restore the switch beam and connect ports 2 and 4. In fact, when the rotor-based switch is released, all ports are disconnected. However, in operation, the switch has only two stable states where either ports 1 and 3 are connected, or ports 2 and 4 are connected.

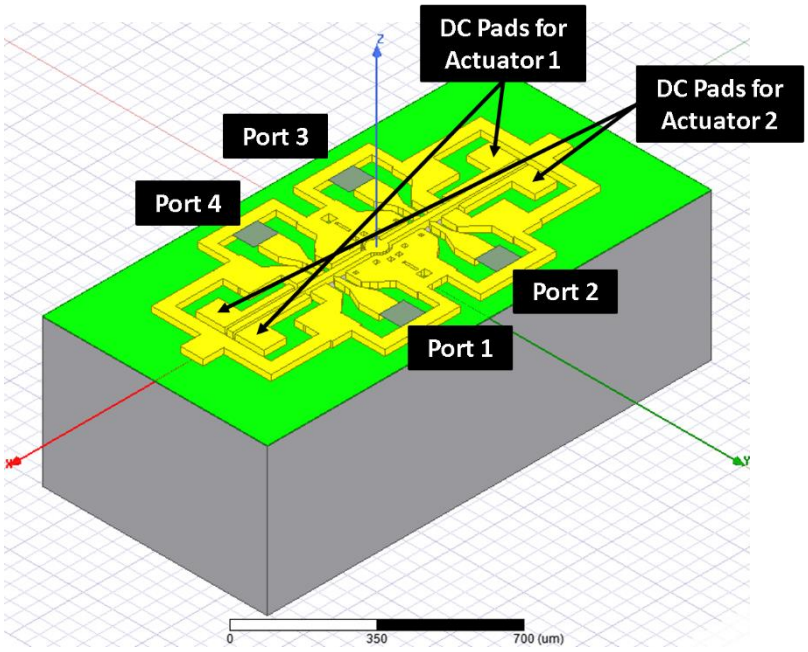


Fig 4.29: The 3D structure of the first generation of the proposed rotor-based switch for low-frequency and high-power RF applications. The pairs of electrostatic actuation electrodes must be assigned diagonally as shown in order to rotate the switch beam. The patches at the RF ports are the lumped ports used for the simulation of the switch

The HFSS electromagnetic results displayed for the OFF state in Fig 4.30 are only possible when the switch is not in operation or immediately after the release, and the expected RF isolation should accordingly be better than the simulated values where all ports are disconnected from the beam. This what the ON state results reveal in the figure. That is due to the fact that the connection of two ports necessitates achieving the minimum possible capacitance between the two other ports, assuming a rigid beam, which is valid for the considered geometry. The switching function can be regarded as an in-plane seesaw operation.

Moreover, Fig 4.30 demonstrates good RF performance of the switch up to 6GHz where the return loss is better than 20dB in the ON state together. Further tuning and optimization of the switch geometrical parameters can provide better matching up to the same frequency or acceptable matching up to a higher frequency of operation. The insertion loss results show excellent contact performance, which is expected from using gold-to-gold contact by virtue of the vertical coating of the over-plating layer.

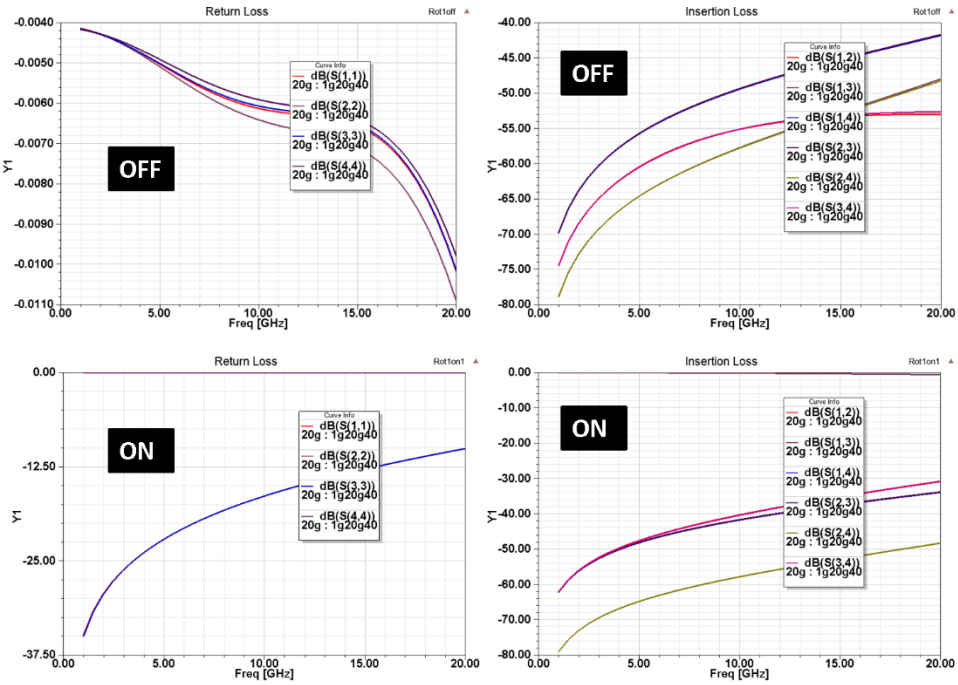


Fig 4.30: The HFSS electromagnetic simulation results of the proposed rotor-based RF MEMS switch revealing its acceptable performance up to 5GHz

Despite the advantages of the proposed switch architecture, there are some important drawbacks. The first drawback lies in the high actuation voltage required (>100V) due to the relatively large spacing between the nickel features as imposed by the design rules, and assuming up to 2µm of added gold wall thickness. Second, depending on the distance between the contact tips of the signal lines and the center of rotation of the beam, and the thickness of the over-plating gold, the rotating beam was experimentally found to mostly touch first the actuation electrodes rather than the ports to be connected. A rotation angle ~ 1º is required for switching. Increasing the gap between the electrodes would increase the switching voltage drastically. Third, using longer beams would allow reducing the actuation voltage and/or exerting higher contact forces, but it would make the RF matching more difficult in view of the parasitic stub due to the fact that the beam becomes part of the signal line when the connection is made. It is worth noting here that current architecture of the switch (in Fig 4.28) provides a more compact design as compared to other possible architectures where the switch beam can include nitride mechanical links, which would suppress the unwanted stub effect. Without the mechanical insulating link, the DC voltage should be applied to the actuation electrodes through biasing resistors, which can be implemented in the polysilicon layer of the process.

Furthermore, it is possible to overcome the challenge with the actuation range in the first generation of the rotor-based switch design while reducing the switching voltage required. This can be achieved by adopting the architecture in Fig 4.31 and Fig 4.32, which was used for the second generation of the rotor-based switch

design. Considerably larger rotation angles are possible, which would help increase the actuation voltage beyond the level needed for switching in order to exert more contact force if needed. Also, the restoring voltage required would be significantly less due the circular geometry of the comb-drive actuator.

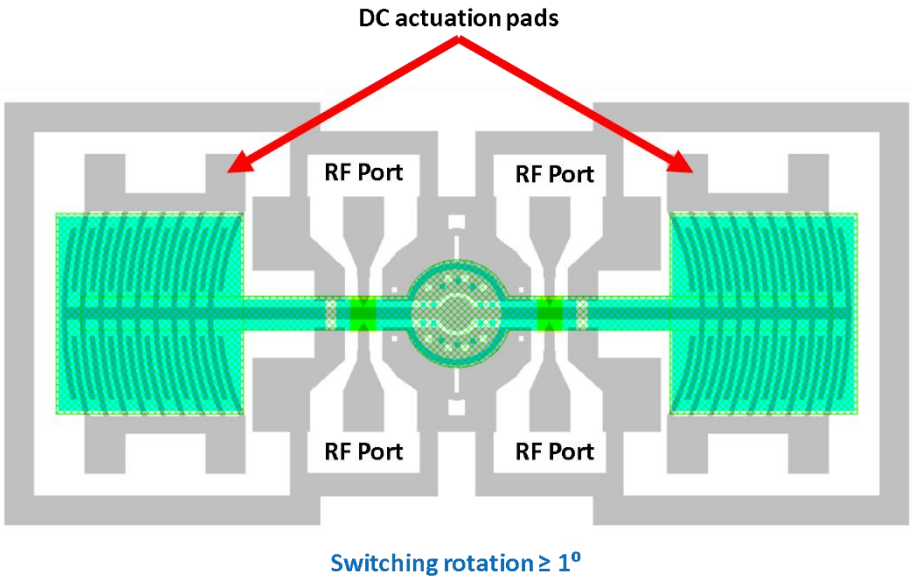


Fig 4.31: An exact layout of the enhanced design of the rotor-based switch where larger rotation angles are possible and higher actuation capacitance is achieved, thus lowering the switching voltage

The HFSS electromagnetic simulation results of the improved rotor-based switch design are demonstrated in Fig 4.33. Due to the added nickel volumes to the switch beam (making the circular comb-drive movable electrode), the parasitic stub effect and radiation loss are more pronounced, and the maximum operating frequency with acceptable RF performance is reduced to 5GHz. However, the greatest gain with such switch would be in the high power handling capability and the strong immunity to self-actuation.

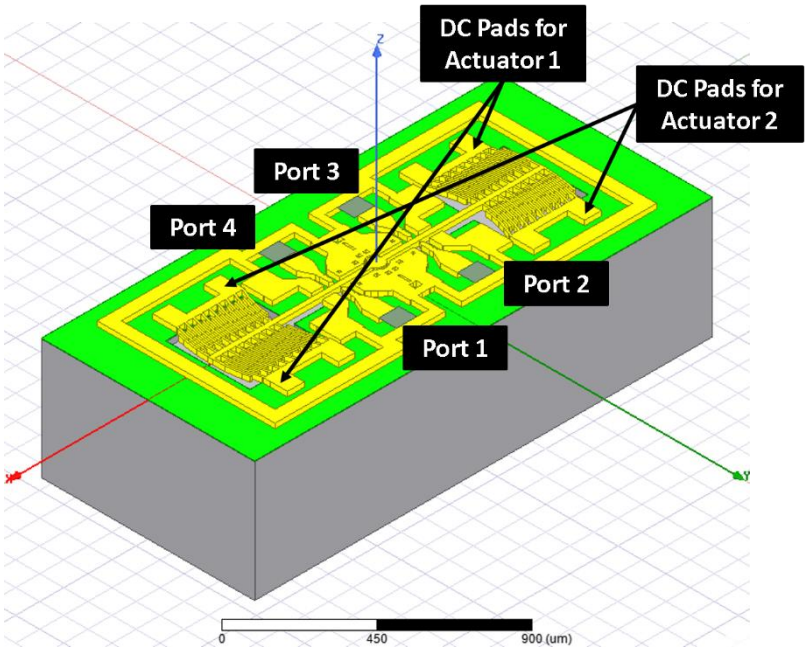


Fig 4.32: The 3D structure of the improved design of the proposed rotor-based RF MEMS switch for low-frequency and high-power applications. The patches at the RF ports are the lumped ports used for the simulation of the switch

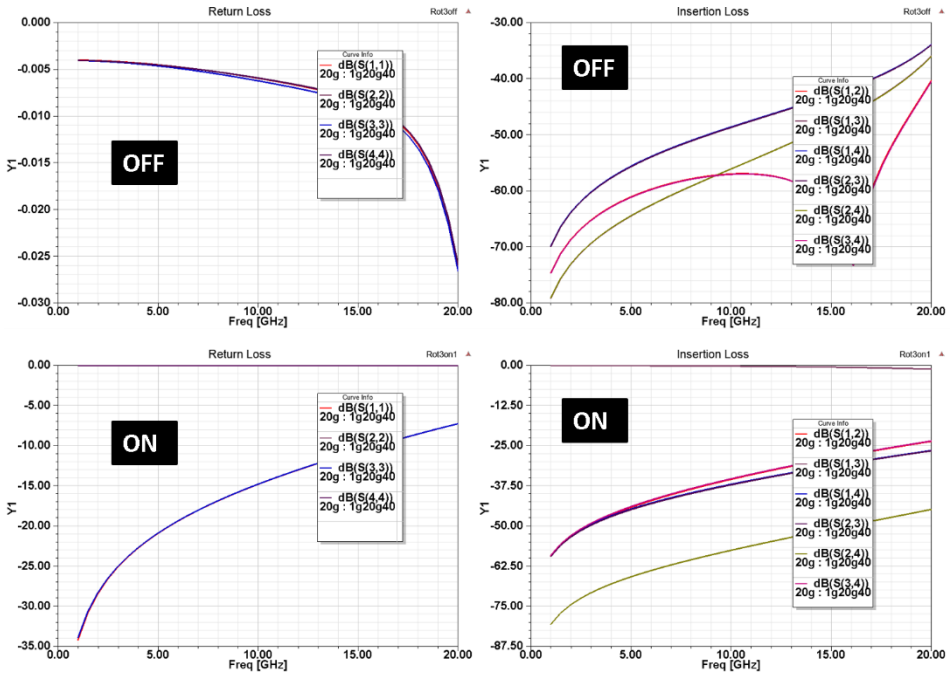


Fig 4.33: The HFSS electromagnetic simulation results of the second generation of the proposed rotor-based RF MEMS switch revealing its acceptable performance up to 5GHz

Chapter 5: RF Switches Implemented in Standard UWMEMS and a New Post-Processing Procedure for More Complex Architectures

As defined previously, the third approach considered in this thesis for building the RF MEMS switches is through the development of a microfabrication process. In this chapter, the designs and simulation results of several RF switches implemented in the standard UWMEMS process and post-processing are presented. In addition, the development of an expanded version of the existing UWMEMS process and post-processing is described along with more switch designs enabled by the post-processing sequence introduced. The new architectures include devices based on the geometric confinement of electroplated gold structural layers.

5.1 Overview of the UWMEMS Process

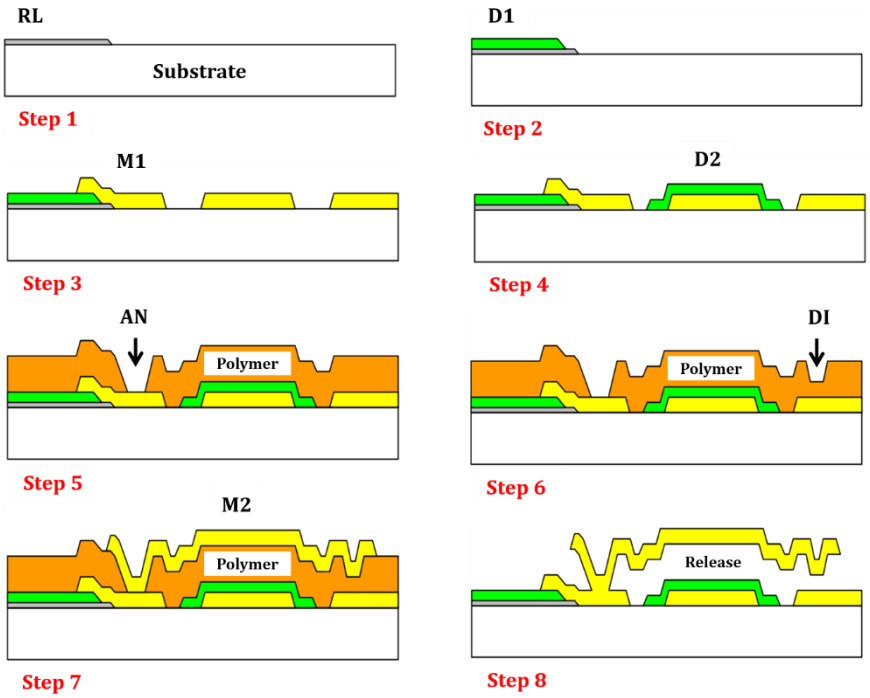


Fig 5.1: Cross-sectional view of the main UWMEMS process steps [77]

In this section, the physical layers and processing sequence of the UWMEMS surface micromachining process are described. The typical substrate in the process is alumina, which is the same type of substrate assumed for all the RF switches discussed in this chapter. Glass and silicon substrates can also be used. All

the designs reported in this chapter utilize coplanar waveguide (CPW) transmission lines. Microstrip-based circuits can be implemented in the same way, and can be fabricated in the standard UWMEMS.

Fig 5.1 illustrates the main fabrication steps of the standard UWMEMS process [77]. In the first step, a resistive thin layer (RL) of chromium / titanium / titanium tungsten is deposited. This layer is primarily used for the decoupling of the RF and DC signals through large resistance values (10-100KΩ typically). It can also serve as bottom or fixed electrode for electrostatic actuation. It is also possible to use it for micro-heating in the case of thermal actuation. In the second step, an insulating layer of silicon dioxide or silicon nitride dielectric (D1) is deposited. It is needed in order to allow overlapping between the resistive layer and the first gold layer (M1) utilized in making the RF circuits and signal routing. It can be used for making the bottom or fixed electrode in electrostatic actuators. The deposition and patterning of that gold layer is shown in the third step. In the fourth step, a second dielectric layer (D2) is employed for the sake of building metal-insulator-metal (MIM) capacitors.

After the successful patterning of the first four layers, a polymer sacrificial layer (SL) is spun on the substrate. Before the deposition and patterning of the second electroplated gold layer (M2) representing the structural layer, the polymer sacrificial later is dry etched such that the openings for anchoring (AN) and dimples (DI) are formed. Finally, the polymer sacrificial layer is stripped in wet etching prior to loading the UWMEMS chips in a liquid CO_2 critical point drier (CPD) that is essential for completing the release process without significant stiction failures.

5.2 RF Switches in Standard UWMEMS Fabrication and Post-Processing

Different designs for RF switches were implemented based on the standard post-processing of UWMEMS process. The devices include 4-port designs of T-switch, R-switch and C-switch cells that are important for switch matrices. Moreover, new designs for RF-power driven actuation (i.e. self-actuation) switches are analyzed.

5.2.1 Four-Port Switching Cells for Switch Matrices

T-switch, R-switch and C-switch 4-port configurations are typically employed in switch matrix applications and redundancy networks employed in satellite communications [80, 82]. The difference between such designs lies in the allowed routing states. Fig 5.2 displays a diagram illustrating all possible states of each of the three designs. It is clear that the states of a T-switch include the states of C-switch and those of the R-switch. In fact, the distinctive feature of the T-switch is the ability to connect two orthogonal RF signal paths simultaneously, which is achieved by means of a signal crossover.

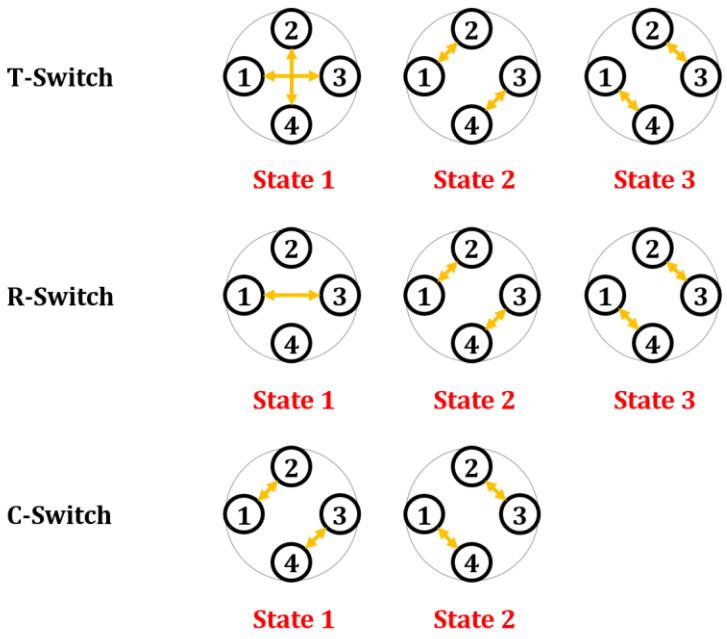


Fig 5.2: Diagram illustrating the distinct states of the T-switch, R-switch and C-switch designs

Starting with the T-switch cell, Fig 5.3 displays an exact UWMEMS layout of the design using two switches in series per signal path. Such design allows for a more efficient RF design in terms of the suppression of unwanted stub effects in conjunction with higher isolation in the OFF state.

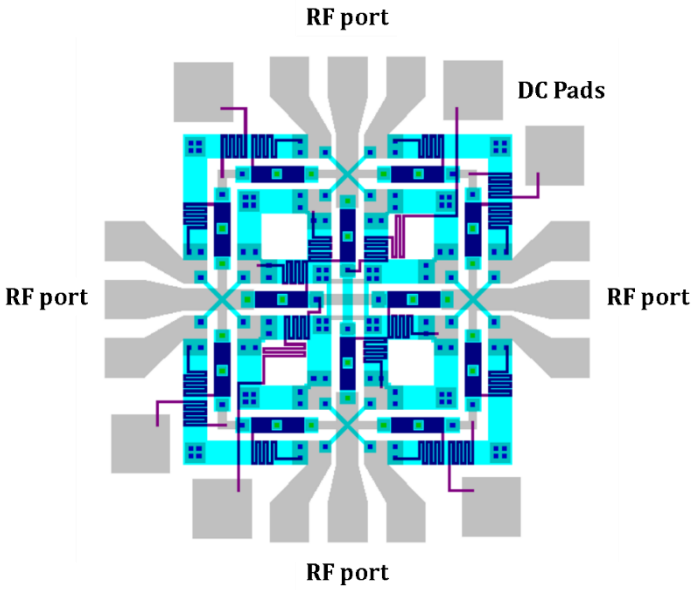


Fig 5.3: Design of T-switch cell in standard UWMEMS process. Other more compact designs have been also developed using a single series switch element per signal path. DC pads are 100µm each

Fig 5.4 shows the 3D electromagnetic simulation results in HFSS of the T-switch cell up to 20GHz in the ON state with the crossover or 180º state enabled. Similarly, Fig 5.5 provides the simulation results with the periphery or 90º state enabled. In both figures, good matching all over the operation bandwidth can be observed. Despite using two series contacts exist per signal path, the overall insertion loss is very good.

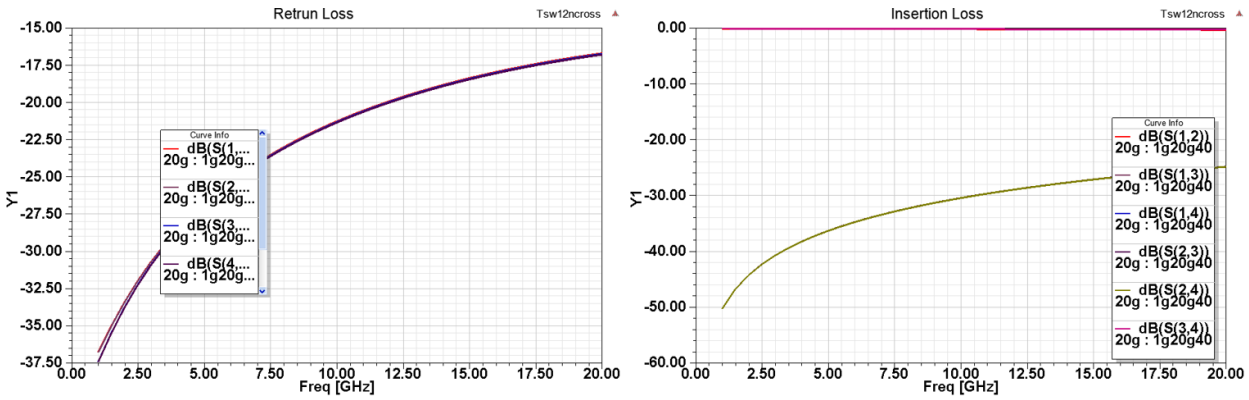


Fig 5.4: HFSS 3D electromagnetic simulation results of the T-switch cell in the ON state with the cross-over or 180º state enabled

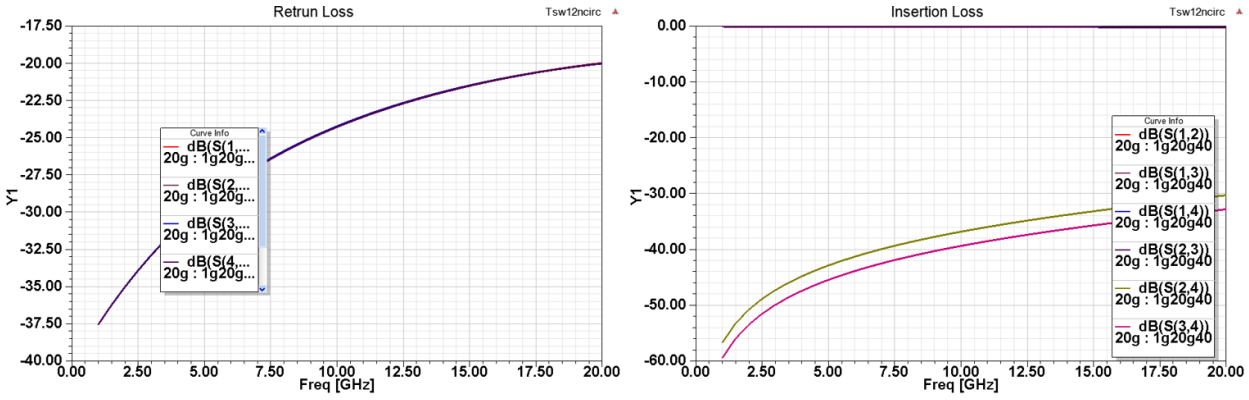


Fig 5.5: HFSS 3D electromagnetic simulation results of the T-switch cell in the ON state with the peripheral or 90º state enabled

The OFF state high isolation of the T-switch cell is demonstrated in the simulation results in Fig 5.6. Using a single switch or contact per signal path would result in less isolation.

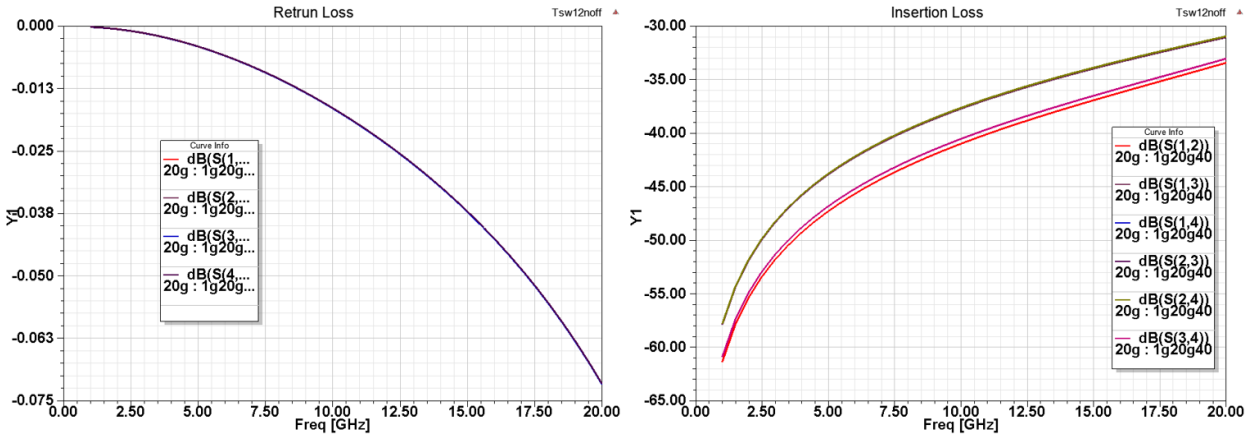


Fig 5.6: HFSS 3D electromagnetic simulation results of the T-switch cell high isolation in the OFF state

Moreover, the R-switch design is provided in Fig 5.7. Obviously, it offers only five signal paths rather than six signal paths as in the case of the T-switch, which corresponds to the allowed states illustrated in Fig 5.2.

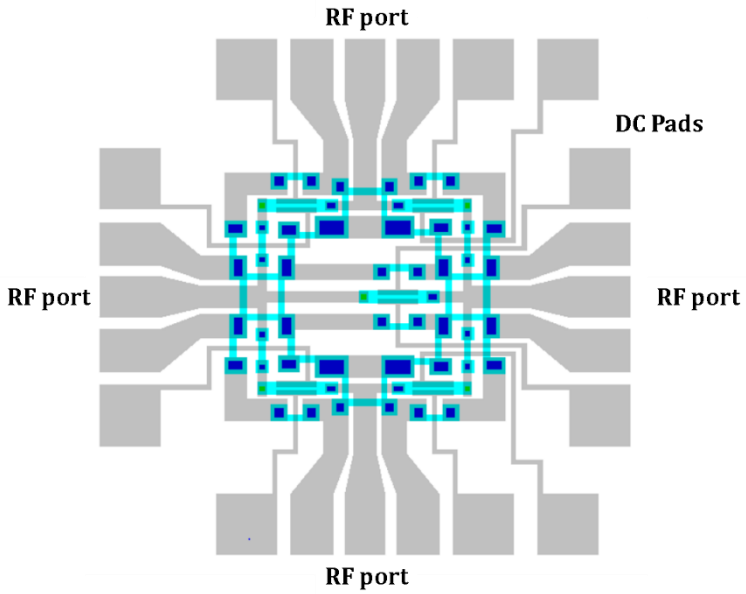


Fig 5.7: Design of R-switch cell in standard UWMEMS process . Other designs have been also developed based on having two series switch elements per signal paths for the sake of better RF matching. DC pads are 100µm each

Fig 5.8 and Fig 5.9 display the HFSS electromagnetic simulation results of the R-switch in the ON state with the 180º state and 90º state enabled, respectively.

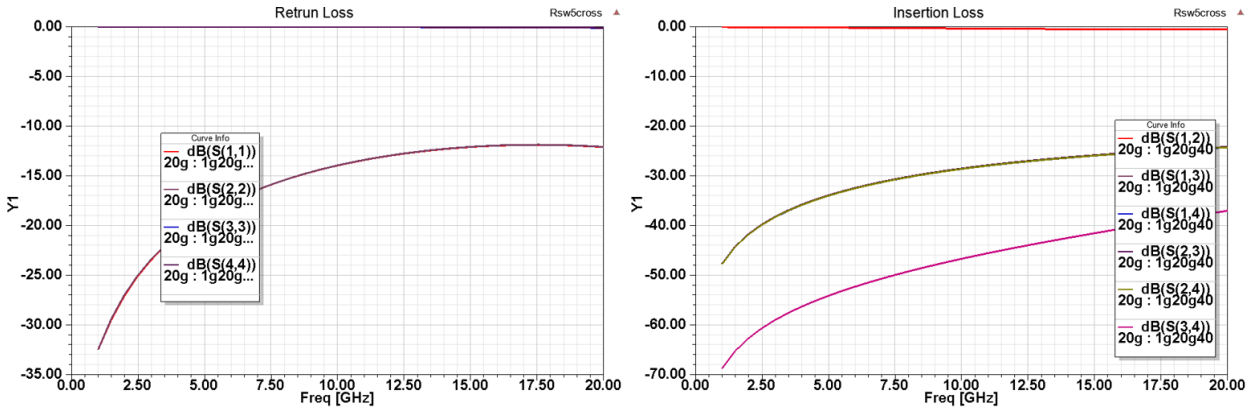


Fig 5.8: HFSS 3D electromagnetic simulation results of the R-switch cell in the ON state with the 180° state enabled

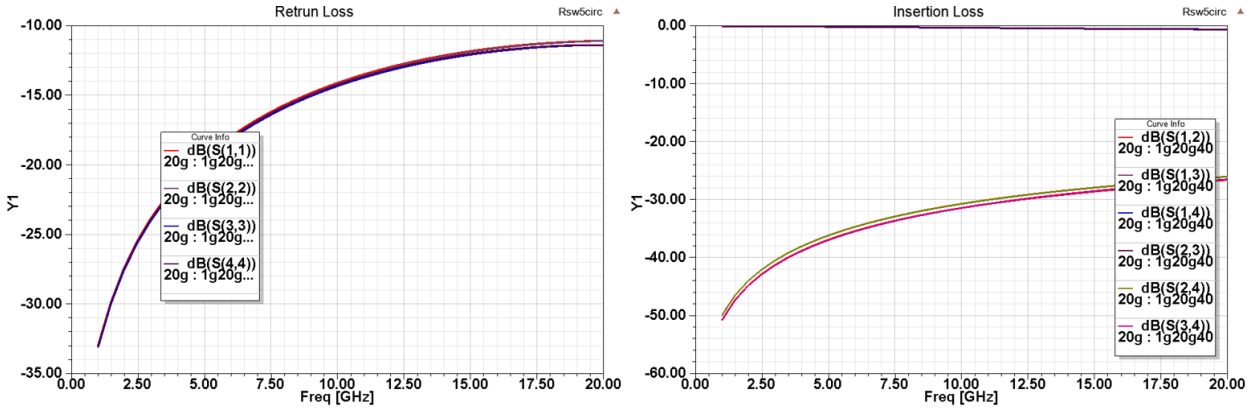


Fig 5.9: HFSS 3D electromagnetic simulation results of the R-switch cell in the ON state with the peripheral or 90° state enabled

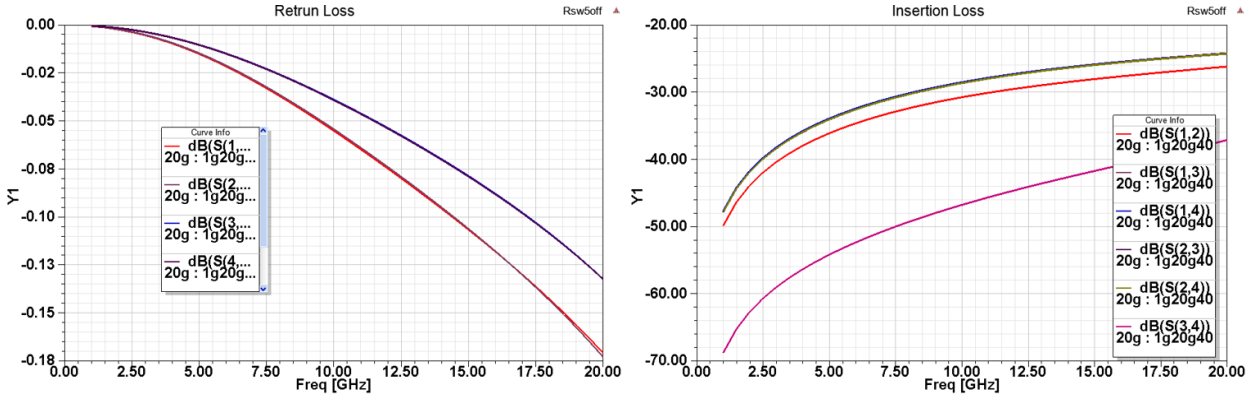


Fig 5.10: HFSS 3D electromagnetic simulation results of the R-switch cell in the OFF state

Furthermore, the design of the C-switch cell is demonstrated in Fig 5.11. As discussed previously, only the peripheral or 90º state is allowed in this design as explained in Fig 5.2.

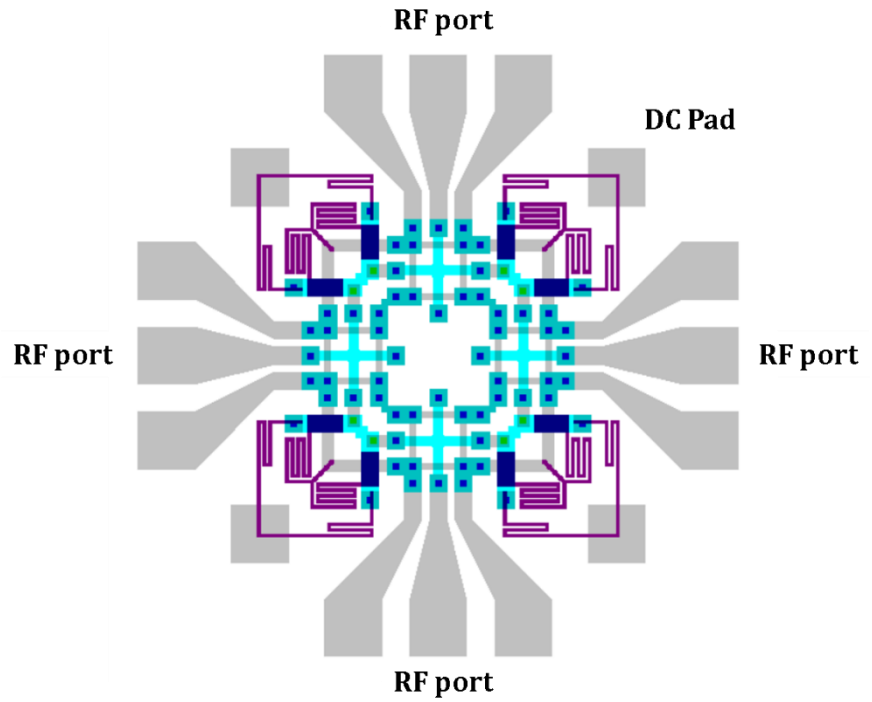


Fig 5.11: Design of C-switch cell in standard UWMEMS process . Other designs have been also developed based on having two series switch elements per signal paths. DC pads are 100µm each

Fig 5.12 and Fig 5.13 show the 3D electromagnetic simulation of the C-switch design in the ON and OFF states, respectively. The results are comparable to the obtained results in the case of the T-switch and R-switch designs, and they confirm good matching up to 20GHz with high isolation in the OFF state.

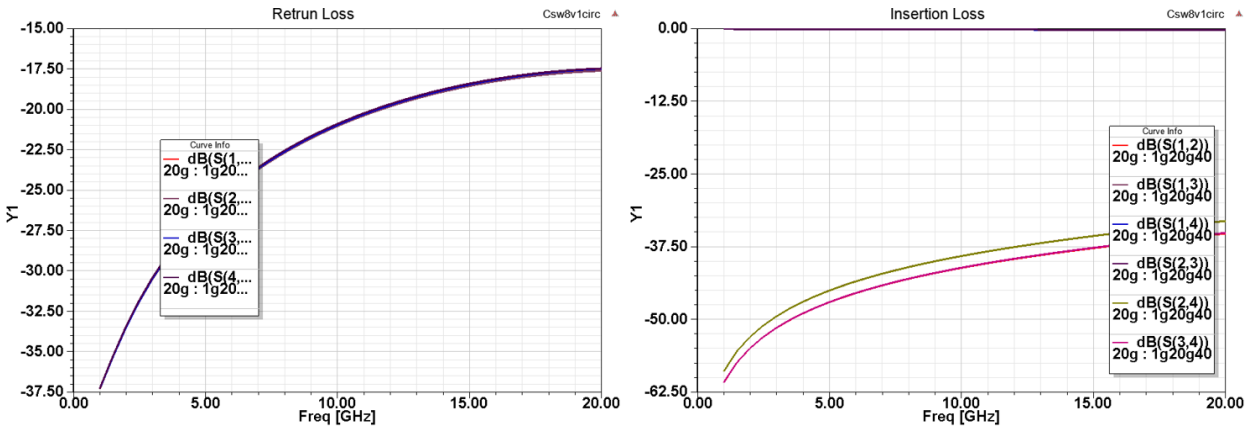


Fig 5.12: HFSS 3D electromagnetic simulation results of the C-switch cell in the ON state

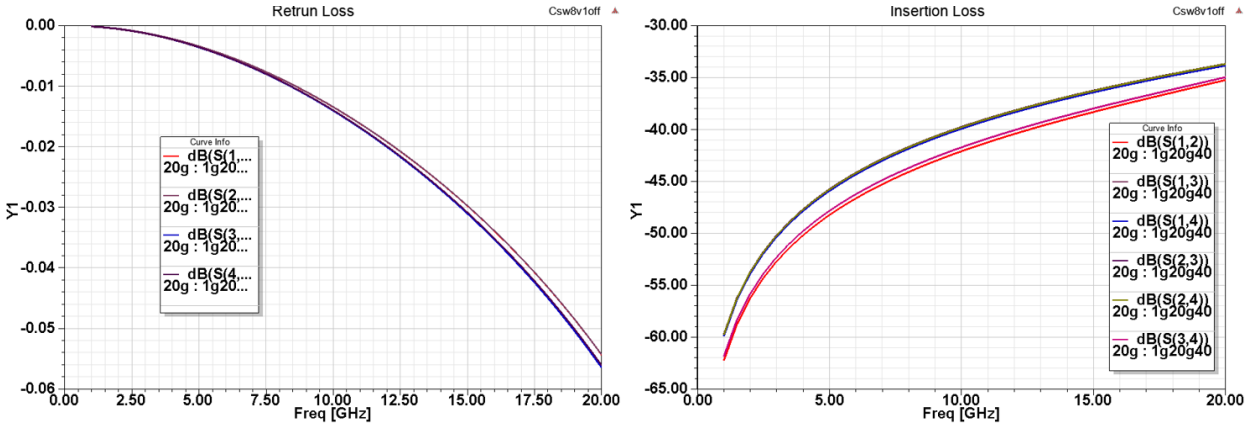


Fig 5.13: HFSS 3D electromagnetic simulation results of the C-switch cell in the OFF state

Besides the three ubiquitous designs of the 4-port switch cells, a new 4-port switch cell is introduced in this work based on a gimbal-based electromechanical design. Similar to the operation of the C-switch, only peripheral or 90º state is possible with high isolation for the two other ports that remain disconnected. As a matter of fact, in the ON state, two ports are connected while the other two ports are not, which is not the case for the C-switch as well as the T-switch and R-switch designs. The description of the operation of such gimbal-switch (G-switch) is provided in chapter six along with the device layout and performance results.

5.2.2 Self-Actuation Switches

Very commonly, the RF MEMS switch is turned ON through using a DC or low frequency control / gating signal. In typical switches with electrostatic actuation including commercial products, the equivalent DC voltage of the RF signal (i.e. the RMS value) can lead to unwanted actuation known as self-actuation. If the

self-actuation power level of the switch can be preset or tuned, it is possible to develop a new set of RF switches where the gating signal is part of the input RF power. An attractive application for such switches is in implementing RF MEMS isolators (i.e. directional switches) and circulators [83].

It should be noted at this stage that the self-actuation physics is electrostatic, and a MEMS switch with an electrostatic actuator would then be the best candidate for such implementation. The diagram in Fig 5.14 illustrates the alternatives for the design of a self-actuation electrostatic switch. In scheme 1, the simplest form of self-actuation design is displayed where the significant capacitance (i.e. leading to reasonable values of pull-in voltage) exists between the two ports. However, the major drawback of such architecture lies in the trade-off with RF isolation. In scheme 2, the RF isolation in the OFF state can be made higher, however, the drawback would be the need for higher voltage or input RF power in order for the RMS value of the RF voltage to attain the pull-in level. It is worth mentioning that the switched beam in this case can be displaced using any type of actuator as previously mentioned. Also, the mechanical design should allow the RMS voltage level of the threshold RF power to retain the switch state if the DC applied component is removed.

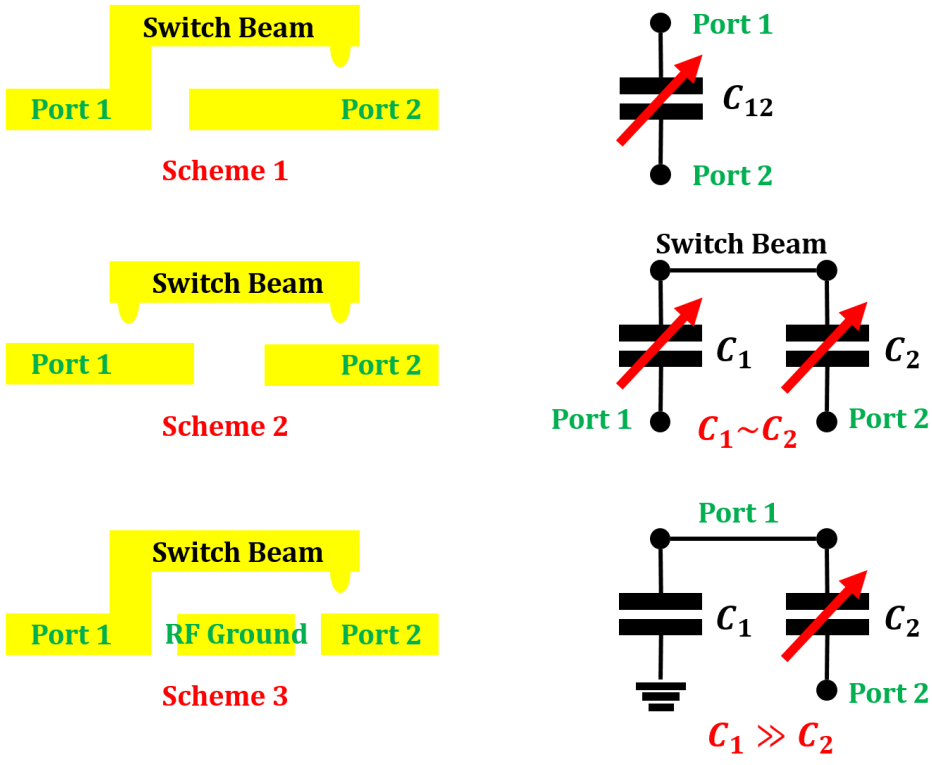


Fig 5.14: Diagram illustrating the different options for the operation of an electrostatic self-actuation switch

However, due to the small increments required for the actuation distance or displacement of the switch beam depending on the tuning specifications targeted by design, achieving low DC power consumption by virtue of mechanical latching techniques as in [71, 73, 74] would not be a possible option practically. Therefore, if the electrostatic actuation cannot be employed for the sake of latching or holding, developing such self-actuation switches should not rely on thermal actuation for reliable tuning of the self-actuation level, i.e. the threshold of the RF power.

Moreover, after further inspection of the self-actuation operation in scheme 1 and scheme 2, it can be seen that both ports have to be initially connected to the rest of the RF circuit such that there is a closed loop for the equivalent DC voltage to be able to pull-in the switch beam. In relatively large circuits and for the sake of extra design flexibility, it would be advantageous to design a switch that operates depending on the incident power level at one port while the second port is initially disconnected, i.e. floating. This critical aspect of operation along with the high isolation between the two ports in OFF state is satisfied by the design in scheme 3. As a matter of fact, the architecture is scheme 3 is unidirectional, not bidirectional as in scheme 1 and scheme 2. The architecture represents a simple form of hybridization of shunt capacitive switching and series contact switching using only one stage rather than cascading the two stages, and it is referred to as Hybrid Self-Actuation Switch (HSAS) in this work.

5.2.2.1 Single-Cap HSAS Design

The single-capacitor HSAS architecture in Fig 5.14 is clamped-free for simplicity. However, the clamped-clamped architecture can definitely be used as well. The primary reason for having a single-capacitor undergoing self-actuation following scheme 3 is the fact that the equivalent DC voltage of the RF power as well as the actual DC voltage both contribute equally to the gating signal, i.e. with equal weights. In the next sub-section, the effect of having different weights is analyzed towards better tunability.

Following the analysis approach in [35], and assuming a RF MEMS switch with a relatively low pull-in voltage of 30V, the switch is driven to pull-in if the control / gating voltage V_g applied through port 1 (i.e. using bias resistor or bias-tee for RF-DC decoupling) is equal to or exceeds the pull-in voltage V_{PI} level imposed by the electromechanical design of the switch as shown in Eq. 5.1. The gating signal is composed of the actual DC input voltage applied V_{dc} in addition to the effective or apparent DC voltage equivalent of the open circuit RF voltage V_{oc}, which is the RMS value and referred to as V_{rms} as provided in Eq. 5.2 and Eq. 5.3.

$$\boldsymbol{V_g \geq V_{PI}} \qquad \text{Eq. 5.1}$$

$$\boldsymbol{V_g = V_{dc} + V_{rms}} \qquad \text{Eq. 5.2}$$

$$\boldsymbol{V_{rms} = \frac{V_{oc}}{\sqrt{2}}} \qquad \text{Eq. 5.3}$$

Due to the initial open circuit (prior to self-actuation) seen at port 1, i.e. the RF input and gating port, the standing wave made of the incident and reflected waves together would result in an open circuit voltage amplitude that can be assumed to be the double of the incident voltage, as provided in Eq. 5.4. The incident power P_{inc} is as shown in Eq. 5.5, which leads to the conclusion in Eq. 5.6 in terms of the relation between the incident power at port 1 and the actual DC voltage drop applied for the sake of tuning.

$$\boldsymbol{V_{oc} \sim 2\, V_{inc}} \qquad \text{Eq. 5.4}$$

$$\boldsymbol{P_{inc} = \frac{(V_{inc})^2}{2\, Z_0}} \qquad \text{Eq. 5.5}$$

$$\boldsymbol{P_{inc} = \frac{(V_{PI} - V_{dc})^2}{4\, Z_0}} \qquad \text{Eq. 5.6}$$

Based on the previous equations, Fig 5.15 displays the voltage and power self-actuation charts of a RF MEMS series switch corresponding to the architecture in scheme 3 (see Fig 5.14). In the figure, the degree of tunability of the incident power triggering self-actuation is relatively high and is almost linear for low DC voltage inputs. It should be noted that depending on the actuation area, initial or up-state actuation gap and the mechanical stiffness matrix exhibited by the structural layer, the level of the pull-in voltage can be designed. However, only the value of the pull-in voltage of the single capacitor is what should be used for the analysis. In fact, this is a strong aspect of not only the analysis provided, but also the design / operation of the switch.

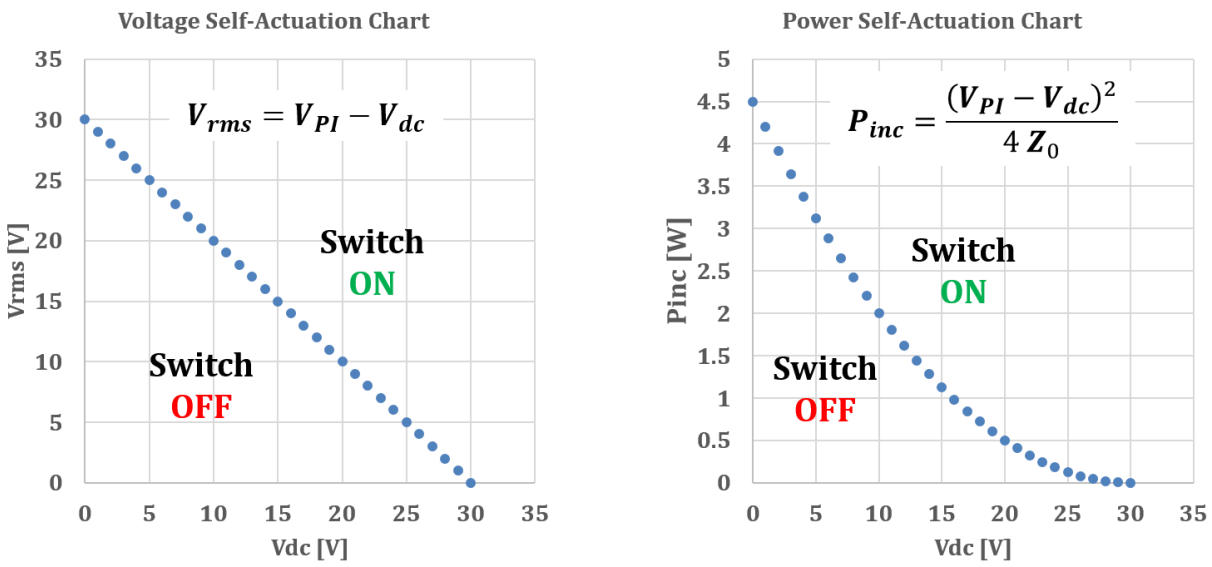


Fig 5.15: An example of the self-actuation charts as a result of scheme 3 using the RMS value and the incident power level of the input RF signal at different DC voltage values. The electromechanical example assumes 30V pull-in onset

Fig 5.16 displays a 3D of the proposed single-capacitor HSAS design where the port 1 is the input and gating port, i.e. the only port that determines whether the switch is in the ON or OFF state. It is the port where the switch is anchored while overlapping with the transverse shunting connection of both ground planes of the CPW transmission line. As mentioned previously, other configurations of transmission lines such as microstrip and slot-line can still be used in the same way.

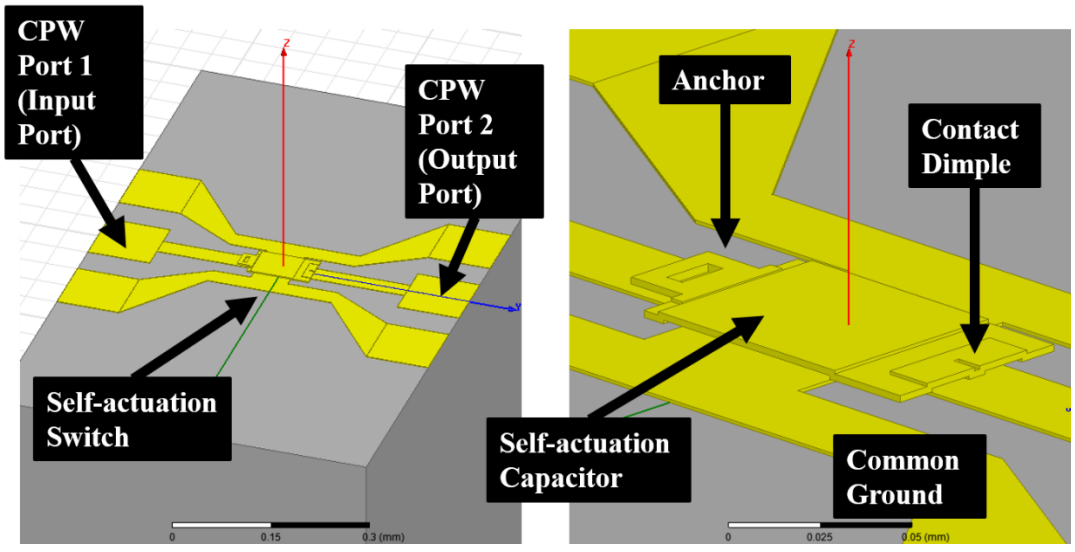


Fig 5.16: 3D of the single-capacitor HSAS design

The HFSS electromagnetic simulation results of the single-capacitor HSAS design is reported in Fig 5.17 up to 20GHz. Incorporating the single capacitor for 30V self-actuation does not contradict obviously with good RF design in terms of isolation in the OFF state and matching in the ON state.

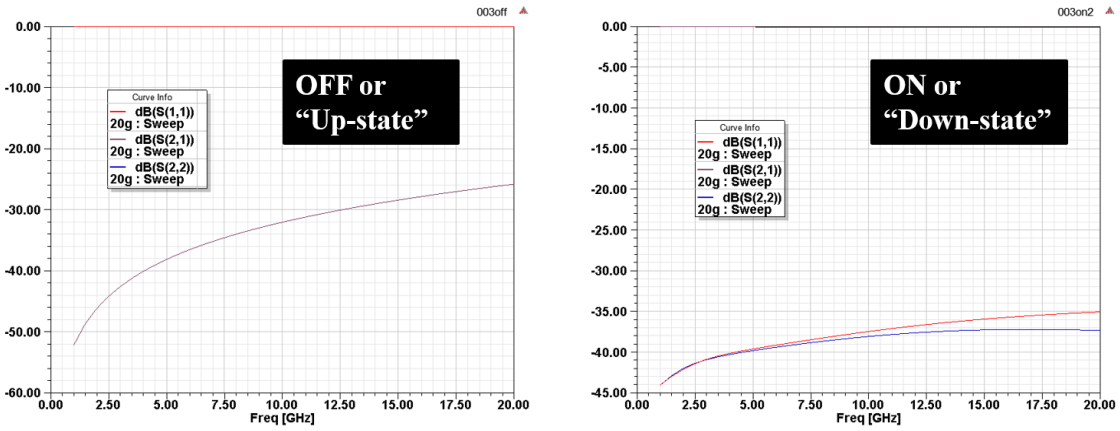


Fig 5.17: HFSS electromagnetic simulation results for the single-capacitor HSAS design

In order to check the unidirectional operation of the single-capacitor HSAS design, an electromagnetic simulation in HFSS was used where each port was exclusively excited with 1W input RF power. Two cross-sections for electric field plotting were employed as shown in Fig 5.18.

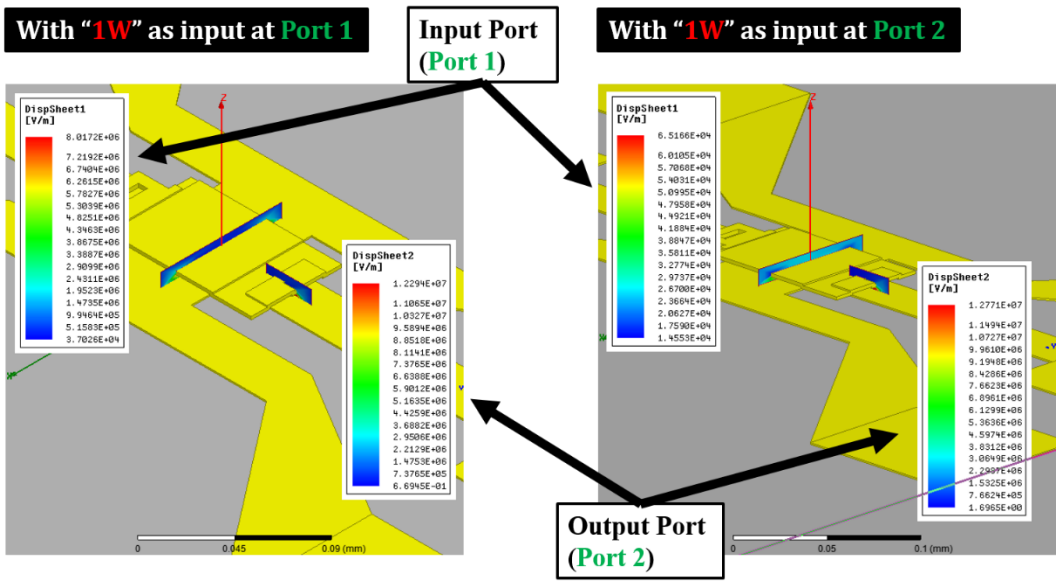


Fig 5.18: HFSS electromagnetic simulation results for the analysis of the unidirectional operation of the proposed single-capacitor HSAS design

Upon the inspection of the plotted magnitude of the electric fields in both cases of excitation and using the two cross-sections, Fig 5.19 reveals that the electric field with excitation at port is almost two orders of magnitude of the corresponding electric field (i.e. in the same location) if the excitation is applied to port 2. This confirms that port 1 is the input / gating port and the switch is unidirectional as designed.

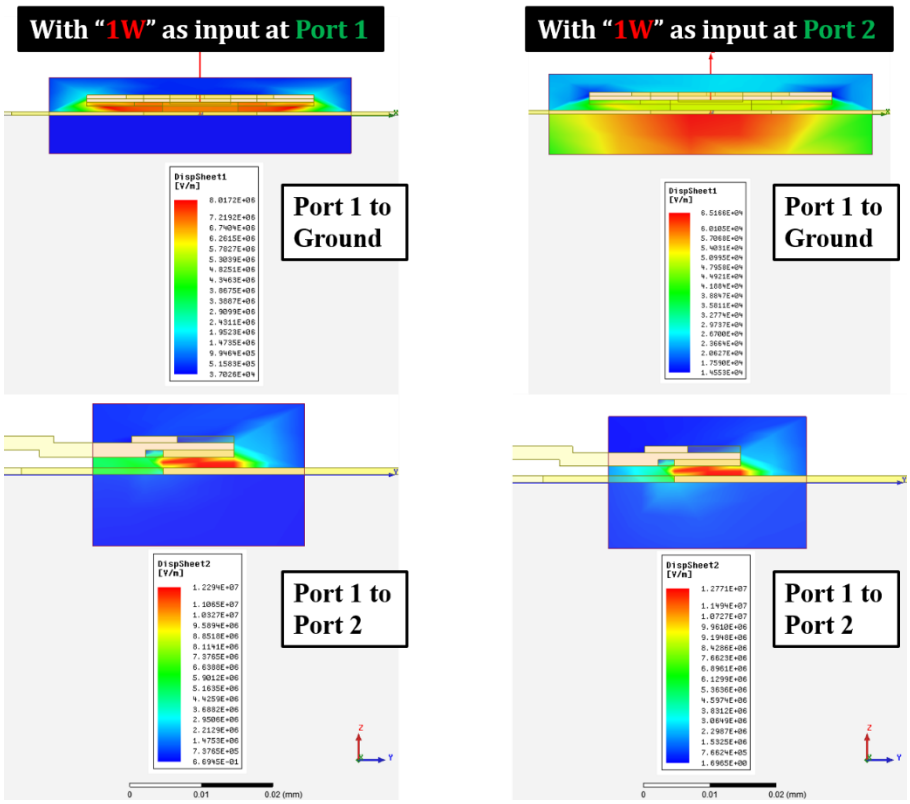


Fig 5.19: HFSS electromagnetic simulation results for the analysis of the unidirectional operation of the proposed single-capacitor HSAS design

It is worth noting that knowing the electrostatic actuation gap (which is 2.5µm) or the contact gap (which is 1.5µm) in the standard UWMEMS process allows calculating the open circuit voltage in a more accurate way in terms of the relation to the incident power. That is mainly due to taking into consideration the lack of perfect matching, i.e. $Z_0 \neq 50\Omega$. It should be noted as well that the estimated voltage is approximately the double of the incident voltage in the OFF state as discussed earlier in this section. In addition, the simulated S-parameters allow for an accurate estimation of the reflection coefficient at the input port in such state. Taking all this into consideration, using 1W would result in around 9.5V of incident voltage, which reveals a transmission line impedance of ~ 45Ω. However, the geometrical tuning of the input CPW geometrical parameters must consider the overall matching in the ON state, and there is generally a trade-off between the tuning of the reflection coefficient in the OFF state and matching in the ON state.

5.2.2.2 Two-Capacitor HSAS Design

The voltage and power self-actuation charts can be further tuned in terms of the DC applied voltage if the HSAS design involves more than one capacitor including the collapsing or pulled-in capacitor required for

series connection between the two ports. This can simply be performed by using two different capacitive paths or overall capacitance to induce self-actuate in the DC and RF domains. In other words, the applied DC voltage and the RMS value of the open circuit voltage are forced to contribute unequally to the pull-in voltage that switches the primary capacitor connecting the two ports. If this is case, Eq. 5.2 can be re-written as in Eq. 5.7 involving the two weight factors α and β for the DC and RMS of the open circuit RF voltage, respectively.

$$\boldsymbol{V_g = \alpha V_{dc} + \beta V_{rms}} \qquad \text{Eq. 5.7}$$

This allows then to re-write Eq. 5.6 as in Eq. 5.8 where the significant impact of the scaling factors on the tuning of the incident RF power is clear.

$$\boldsymbol{P_{inc} = \frac{(V_{PI} - \alpha V_{dc})^2}{4 \beta^2 Z_0}} \qquad \text{Eq. 5.8}$$

In fact, the slope of the curve is a direct and important measure of the tunability achieved by the HSAS design. The slope of the curve is given in Eq. 5.9 and Eq. 5.10.

$$\boldsymbol{\frac{\partial P_{inc}}{\partial V_{dc}} = -\alpha \frac{(V_{PI} - \alpha V_{dc})}{4 \beta^2 Z_0} = \frac{-\alpha V_{rms}}{4 \beta Z_0}} \qquad \text{Eq. 5.9}$$

$$\boldsymbol{\frac{\Delta P_{inc}}{\Delta V_{dc}} \propto \frac{-\alpha}{\beta}} \qquad \text{Eq. 5.10}$$

Fig 5.20 displays the voltage and power self-actuation charts considering only the sweep of the scale factor β and unity value for α. In order to obtain the values of the scaling factor β in the figure, a capacitive divider can be used.

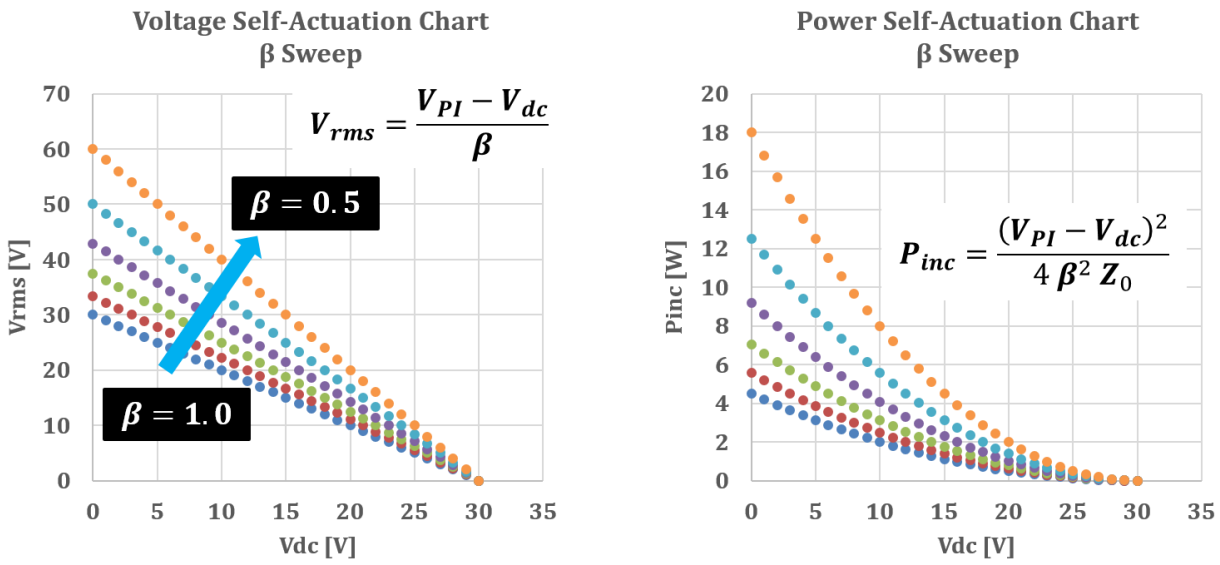


Fig 5.20: Voltage and power actuation chart for the two-capacitor HSAS design with β sweep

The slope of the power self-actuation chart can be further increased for higher tunability if the value of α is more than unity as shown in Fig 5.21. In order to obtain the scaling factor α that is more than unity, i.e. performing an amplification of the voltage, the same capacitive divider used for obtaining the β values in Fig 5.20 can be employed. This can become much clearer by looking at the layout of the two-capacitor HSAS design proposed and the lumped circuit model of the design shown in Fig 5.22 and Fig 5.23, respectively.

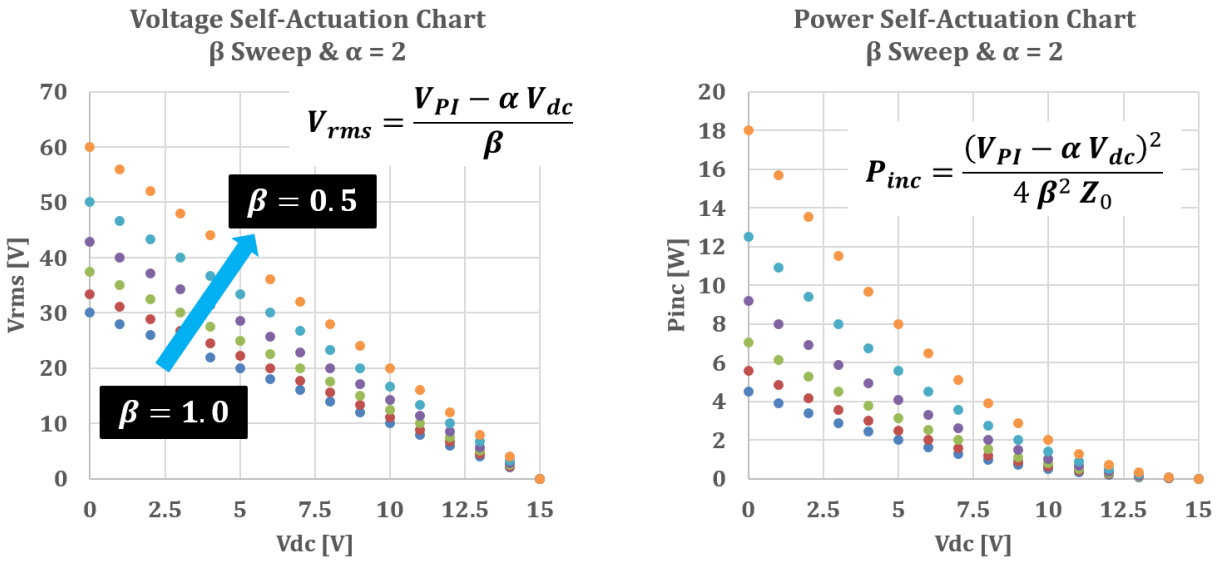


Fig 5.21: Voltage and power actuation chart for the two-capacitor HSAS design with α and β sweep

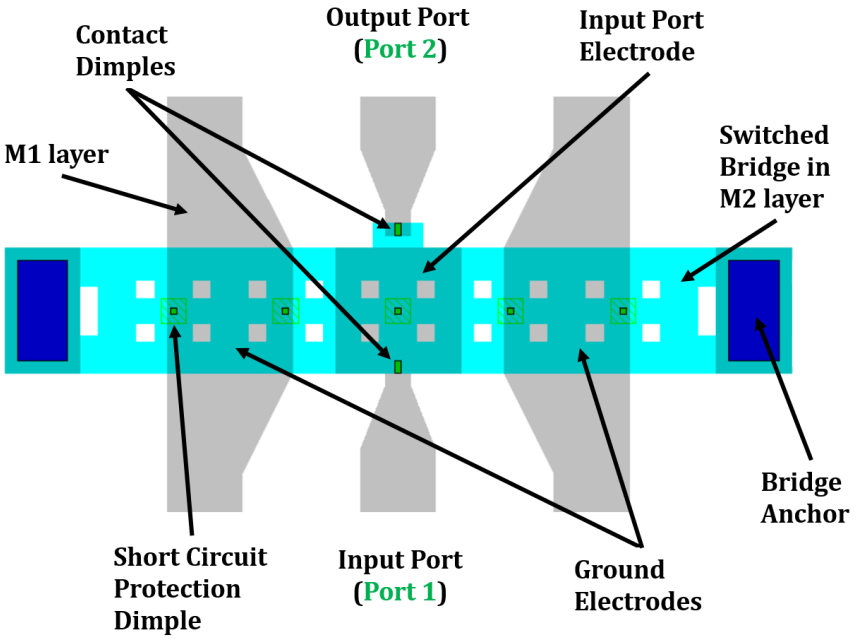


Fig 5.22: Typical UWMEMS layout of the proposed two-capacitor HSAS design

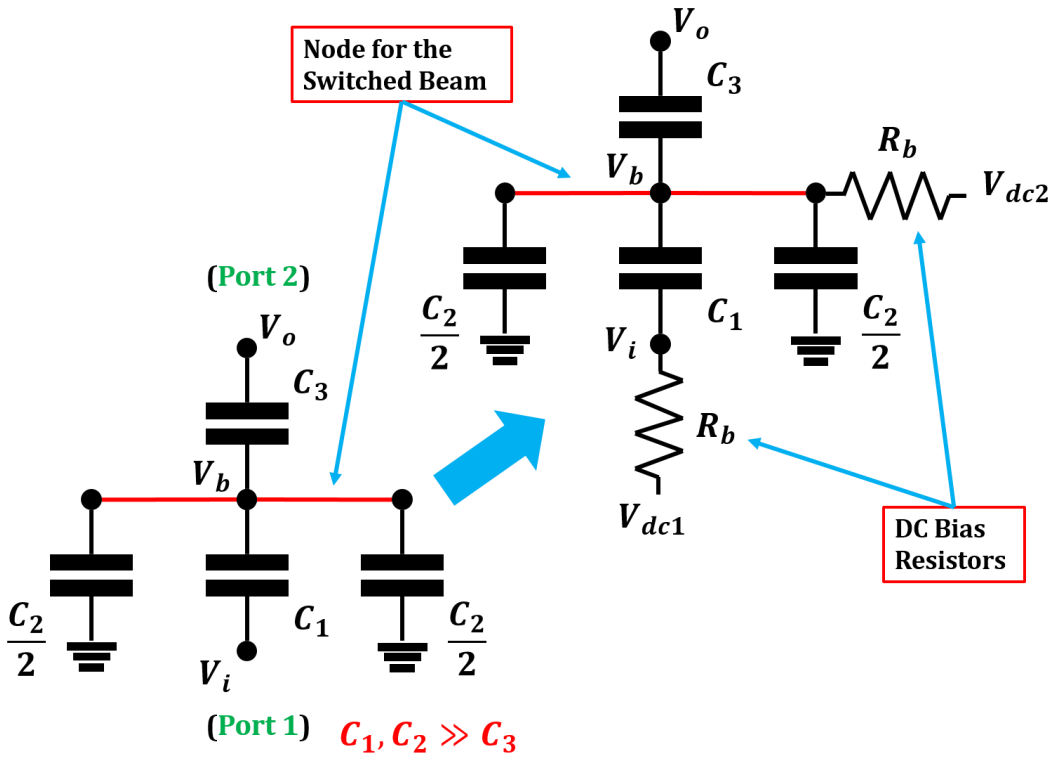


Fig 5.23: Lumped circuit model of the proposed two-capacitor HSAS design

In the two-capacitor HSAS design proposed, the RF voltage is forced to be applied across a shunting capacitor made of two capacitors placed in series as seen from the input port, i.e. port 1. The first capacitor, which is the primary capacitor that solely can connect the two ports, is C_1 in Fig 5.23. Such capacitor corresponds to the primary capacitor used in single-capacitor HSAS design discussed earlier. Eq. 5.11 relates the input voltage to the voltage across the main capacitor C_1 and the secondary capacitor C_2.

$$V_i = V_{C1} + V_{C2} \qquad \text{Eq. 5.11}$$

The voltage across the secondary capacitor is actually the potential of the switched beam / bridge (Eq. 5.12).

$$V_{C2} = V_b \qquad \text{Eq. 5.12}$$

The relation between the voltage across the primary capacitor and the input voltage at port 1 can be found as follows in Eq. 5.13, Eq. 5.14 and Eq. 5.15.

$$\boldsymbol{V_i = V_{C1}\left(1 + \frac{V_{C2}}{V_{C1}}\right)} \quad \text{Eq. 5.13}$$

$$\boldsymbol{\frac{V_{C2}}{V_{C1}} = \frac{Z_{C2}}{Z_{C1}} = \frac{C_1}{C_2}} \quad \text{Eq. 5.14}$$

$$\boldsymbol{V_i = V_{C1}\left(1 + \frac{C_1}{C_2}\right)} \quad \text{Eq. 5.15}$$

The switch can be turned ON if the voltage across the primary capacitor is equal to or more than the pull-in voltage (Eq. 5.13), which depends on the electromechanical design of the switched beam as mentioned earlier. In the case of RF input only, the RMS value of the open circuit voltage should be equal to the pull-in voltage as in Eq. 5.17.

$$\boldsymbol{V_{C1} = V_{PI}} \quad \text{Eq. 5.16}$$

$$\boldsymbol{V_{rms} = V_{PI}\left(1 + \frac{C_1}{C_2}\right)} \quad \text{Eq. 5.17}$$

Comparing the result in Eq. 5.17 to that in Eq. 5.7 using no DC voltage across the primary capacitor, the scaling factor β can accordingly be found as shown in Eq. 5.18.

$$\boldsymbol{\beta = \frac{1}{1+\frac{C_1}{C_2}}} \quad \text{Eq. 5.18}$$

In general, the capacitance values for the primary and secondary capacitors are not independent each other / the applied voltages, especially for the architecture of the two-capacitor HSAS design analyzed in this sub-section. The electromechanical analysis of the clamped-clamped beam in COMSOL can provide the necessary information regarding the relation between the RMS value of the voltage at the input port and the capacitance values of the two capacitors.

Fig 5.24 displays the analyzed bridge in the proposed HSAS design, the electromechanical simulation results of the primary capacitor's pull-in as part of the bridge's pull-in voltage and deflection as well as the variation of the bridge potential / voltage drop across the secondary capacitor, which appears to be almost a linear relation. Subtracting the voltage drop across the secondary capacitor from the overall applied voltage would provide the voltage across the primary capacitor.

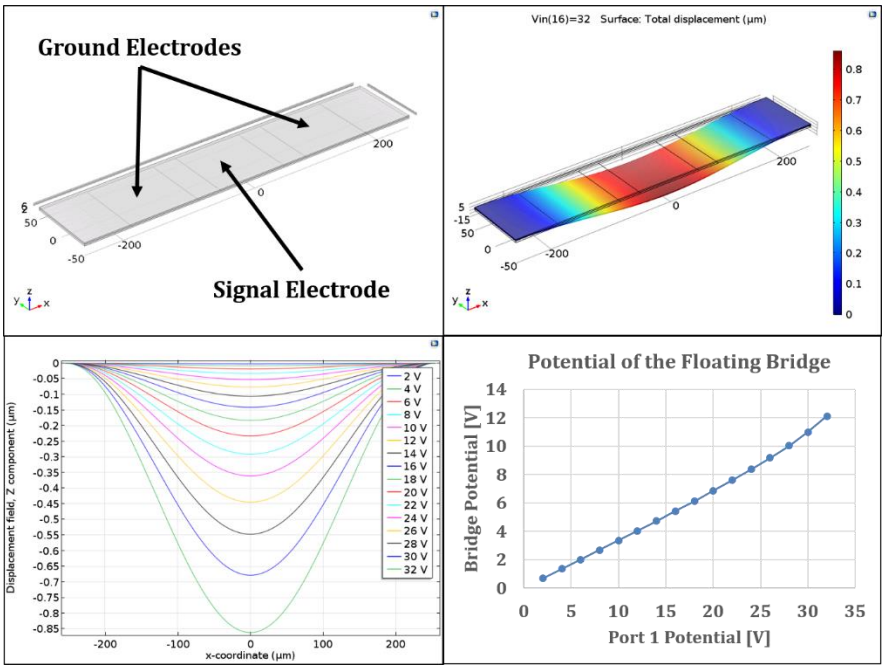


Fig 5.24: COMSOL electromechanical simulation results of the switched bridge at the input port of the two-capacitor HSAS design

Fig 5.25 displays the dependence of the total capacitance seen at the input and the corresponding total charge, which is used to obtain the dependence of the individual capacitances on the applied voltage at the input port.

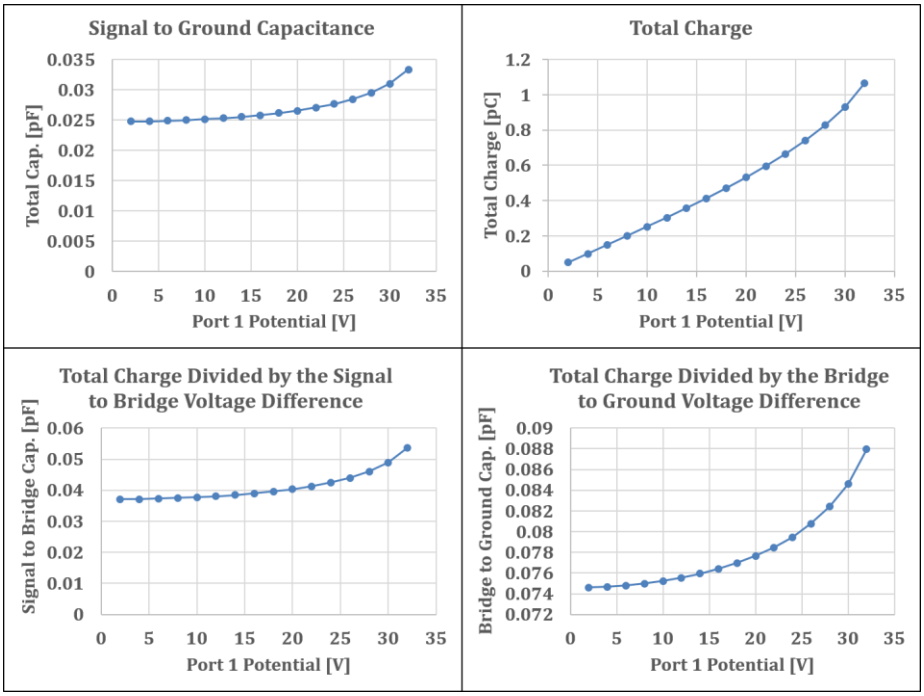


Fig 5.25: COMSOL electromechanical simulation results of the actuation-dependent capacitance values at the input port of the two-capacitor HSAS design

Based on the COMSOL electromechanical analysis, it can be seen that the capacitance ratio of the primary to secondary capacitors is almost 50%, and, accordingly, the scale factor β is close to 67%.

$$\frac{C_1}{C_2} \sim \mathbf{0.5} \qquad \text{Eq. 5.19}$$

$$\boldsymbol{\beta} \sim \frac{\mathbf{2}}{\mathbf{3}} \qquad \text{Eq. 5.20}$$

At this stage, it is worth looking back at the lumped circuit model of the proposed two-capacitor HSAS design in Fig 5.23 where two main DC actuation schemes can be implemented. In the first scheme, the DC actuation voltage is applied across the primary capacitor only by means of the electrical nodes V_{dc1} and V_{dc2} together. This scheme would result in a scaling factor α that is unity as discussed previously. In the second scheme, the electrical node V_{dc1} is set to ground while the node V_{dc2} is set to the desired DC voltage. Such implementation ensures a value for α that is more than unity.

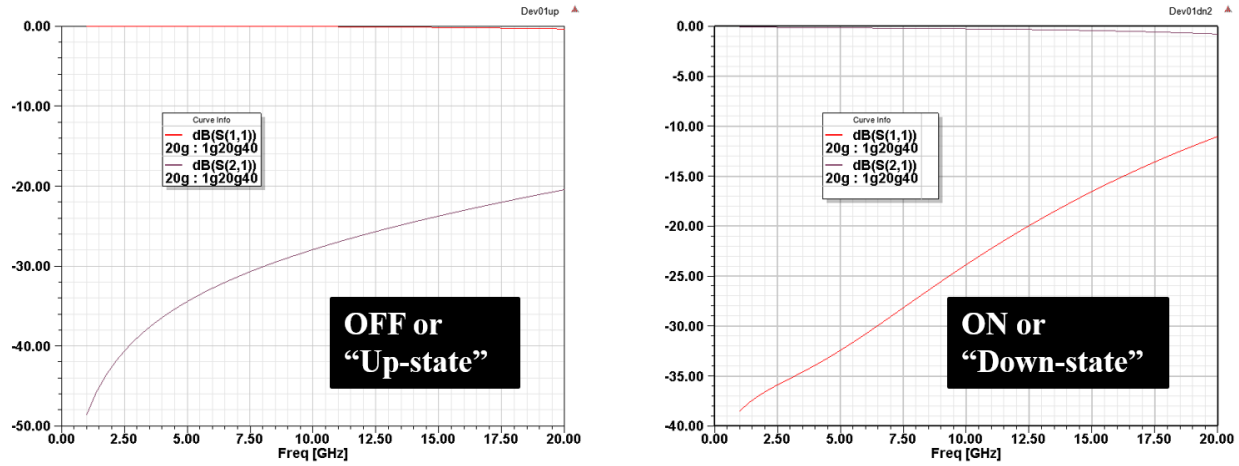


Fig 5.26: HFSS electromagnetic simulation results for the two-capacitor HSAS design

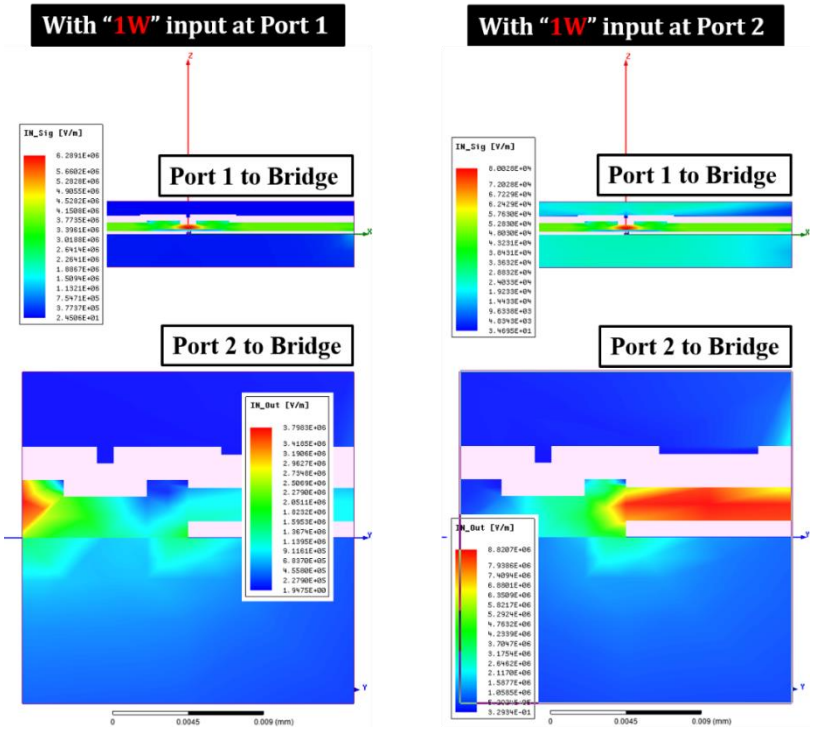


Fig 5.27: HFSS electromagnetic simulation results for the analysis of the unidirectional operation of the proposed two-capacitor HSAS design

The electromagnetic simulation results in HFSS for the two-capacitor switch are shown in Fig 5.26. Besides, the unidirectional operation of the switch was verified in HFSS with two cross-sectional patches for electric field plotting (similar to the ones in Fig 5.18). The results in Fig 5.27 demonstrate a ratio of

almost two orders of magnitude between the electric field within the primary capacitor in the case where the incident RF power is applied to port 1 and applied to port 2, respectively.

The operation of the two-capacitor HSAS designs was verified experimentally. Fig 5.28 shows one of the fabricated HSAS devices included in the first generation. The folded suspension employed at the anchors helped lower the pull-in voltage of the switch for the sake of lowering the incident RF power required for the self-actuation / switching. The CPW input and output ports (port 1 and port 2, respectively) are not shown in the picture.

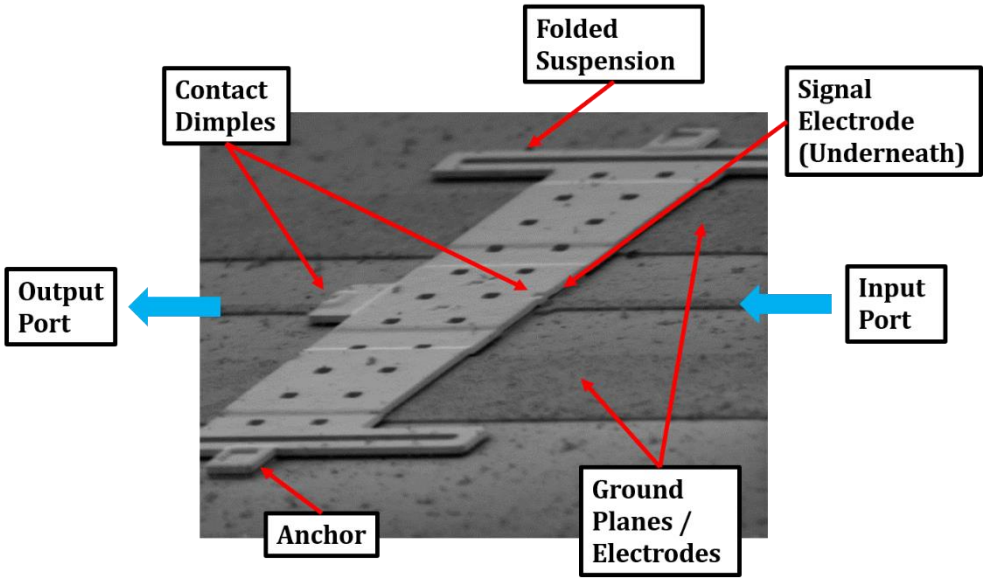


Fig 5.28: SEM of the first generation of fabricated two-capacitor HSAS design with folded suspension beams at the anchors of the bridge for the sake of lowering the pull-in voltage and self-actuation input RF power

Fig 5.29 demonstrates the different building blocks of the test setup utilized. Since the ~ 42dB power amplifier (PA) is limited to a maximum frequency ~ 3GHz, the measurement was performed on several switches using single tone signals of 1GHz / 2GHz provided by a signal generator to the power amplifier through a short RF cable as shown in the figure. An isolator was used after the power amplifier in order to safely dispose of unwanted reflections before the self-actuation of the switch is triggered. The couplers and attenuators allow measuring the input and output signals crossing the HSAS device (i.e. DUT). The overall attenuation of the signal delivered from the coupler's sensing port to the PC-based power meter is ~ 46dB. In order to calibrate the measurement, the same setup was used without the switch such that the loss through the couplers, cables connected to the probes, and the RF probes as well is estimated. This net loss was found to be ~ 1.5dB.

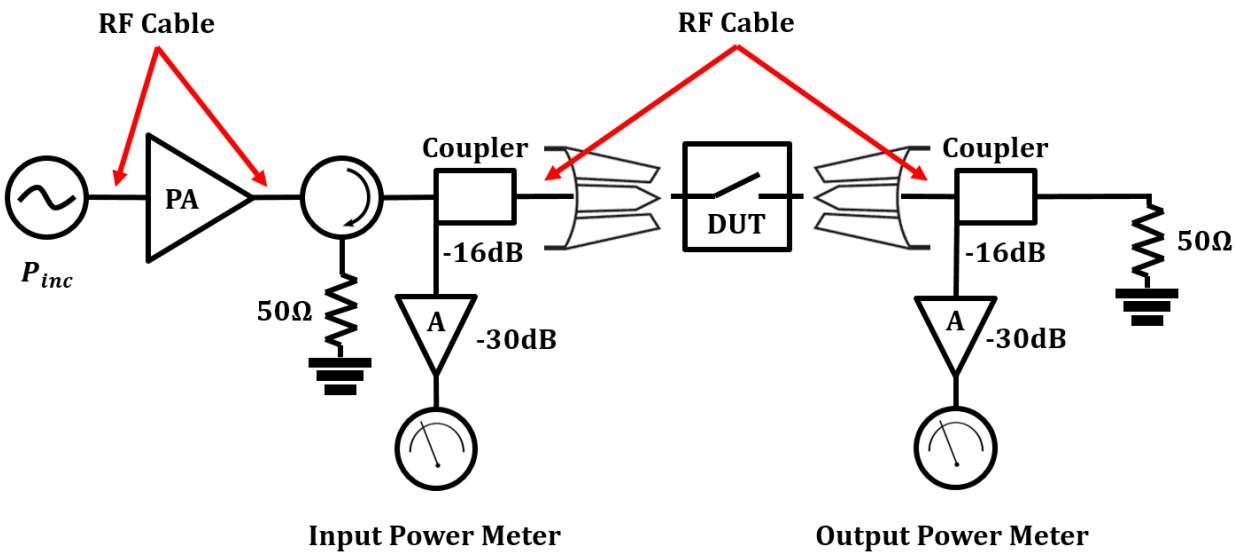


Fig 5.29: Block diagram of the experimental setup used to validate the operation of the two-capacitor HSAS design; "PA" is a RF power amplifier; "A" is an attenuator

Without applying DC voltage for the sake of tuning the threshold RF power level, the measurement results show that the self-actuation input power to the switch varied from 10dBm to 20dBm (i.e. 10-100mW) depending on the length of the suspended beam as well as the length of the folded suspension attaching the beam to the anchor. As a matter of fact, this is a relatively very low level of self-actuation power that can be achieved in a small area due to relying on thin electroplated layers of gold for building the structural layer in UWMEMS. Additionally, such low onset RF power for switching is a very attractive feature of the proposed scheme (scheme 3) illustrated in Fig 5.14 as compared to scheme 1 and scheme 2 in the same figure.

In the next sections of this chapter, more degrees of freedom in building the HSAS architectures will be discussed. It will be shown that it is possible to further control the pull-in voltage of the primary capacitor in the two-capacitor HSAS design by means of bidirectional out-of-plane deflection of the suspended beam. This definitely increases the tunability of the HSAS device and increases the reliability of the switch in terms of stiction immunity.

5.3 MEMS Switches Using Geometric Confinement of Beams

MEMS switches have been traditionally made of micro-beams that are clamped-free or clamped-clamped. This is achievable in the standard UWMEMS process and post-processing. However, depending on the post-processing equipment and sequence of the fabricated UWMEMS chips, it is possible to fabricate

micromachined beams that are fully detached from the substrate, i.e. an exact implementation of free-free beams rather than the loosely anchored versions. In order to localize such structures spatially, there is a need for geometric trapping, or a need for what this work refers to as the geometric confinement (GC) of beams. Fig 5.30 illustrates the basic operation of a MEMS switch with an untethered beam (or rigid beam) as well as an illustration of how GC of the released beams can be performed using clamped-clamped beams in the form of brackets [90]. Such bridges represent micromachined hinges, which were introduced many years ago for different applications, e.g. MEMS assembly and reconfigurable optical devices [40, 41].

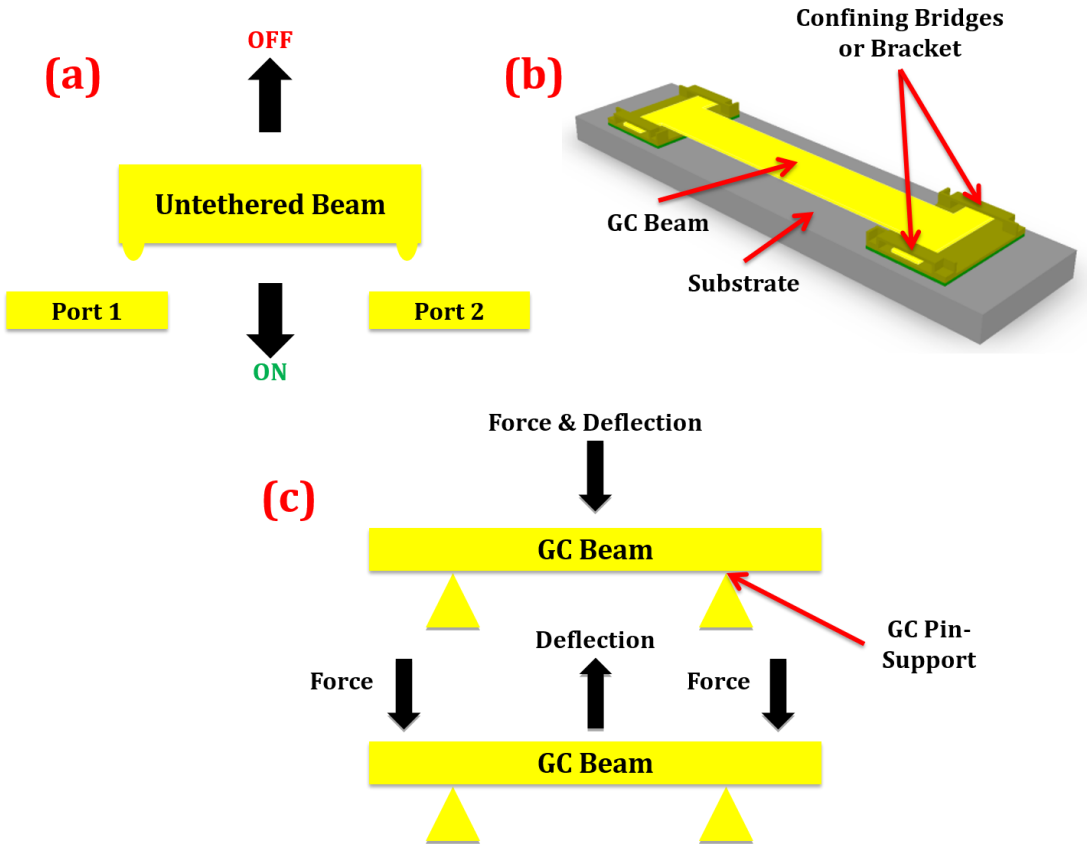


Fig 5.30: Illustration of the concept of geometric confinement (GC) of beams for MEMS switches; (a) switching with an untethered (rigid) beam; (b) an example of using brackets for implementing GC beams; (c) exact implementation of the free-free and pinned-pinned beams is possible using GC beams

In the figure, in addition to the ability to move a confined rigid beam parallel to the substrate, the confined beam can also be actuated on pin-supports. The beam can be designed to rest on posts after the full release, and a force pulling it from the middle part against the posts causes it to bend towards the substrate whereas appropriate forces at the extremities of the beam against the posts allow the beam to bend out-of-plane away from the substrate. In fact, bidirectional out-of-plane deflection or seesaw operation of the beam is possible

without the need for the conventional torsional hinges. The pinned-pinned beams can generally exist in three states, i.e. unactuated (i.e. flat), actuated downwards, and actuated upwards. A combination of both directions of forcing would allow, for instance, the fabrication of more versatile MEMS switches with high RF power handling capability [35] as well as more tunable / reconfigurable HSAS devices.

In fact, the architectural approach in GC-based switches allows replacing the mechanical stiffness by electrostatic and/or magnetic stiffness, which would lead to switching dynamics that are almost solely electrically and/or magnetically tunable. It also suppresses two common mechanisms of energy loss in MEMS devices, namely the thermo-elastic energy dissipation (TED) due to interaction with phonons, and the mechanical support losses due to the coupling of acoustic energy associated with beam vibration to the substrate [20]. The suppression of TED is because the strain gradient associated with cycling is greatly inhibited, and the elimination of most of the support loss is because of the absence of clamping.

In addition, employing GC beams enables the decoupling of two major failure mechanisms for mechanical switches, namely, the failure due to mechanical fatigue and the failure due to the degradation of the contact. In fact, GC beams are advantageous from two perspectives, reliability performance and reliability testing. From the side of performance, they should exhibit the ultimate durability by eliminating the mechanical fatigue component. The contact-related damages cannot be eliminated due to that impact is always associated with the mechanical switching, and can only be optimized typically. From the perspective of testing, the uncommon architectures based on GC can be used to investigate whether mechanical fatigue can eventually be the failure bottleneck rather than contact-related failure.

5.3.1 Remote Electrostatic Actuation and Decoupled Actuation

The fabrication of GC structural layers necessitates coping with loose physical contact between GC beams and their confining structures. The electrical and thermal contacts are accordingly uncommon, which leads to several advantages and disadvantages depending on the targeted application and/or design constraints. The major drawback of the loose electrical contact is the impossibility to apply an electrical signal directly to the GC beam. A capacitive divider would then be needed in order to apply a potential to the floating untethered beam, as in the case of scratch drive actuators (SDA), etc. [86, 87]. Such inevitable capacitive divider that is referred to in this work as remote electrostatic actuation (REA) mechanism would result in significant increase in the actuation and pull-in voltage of the switch for the same footprint of a conventional (anchored) device. The way the capacitive divider is designed and operated is illustrated in Fig 5.31 using the lumped circuit model for each electrostatic actuator design.

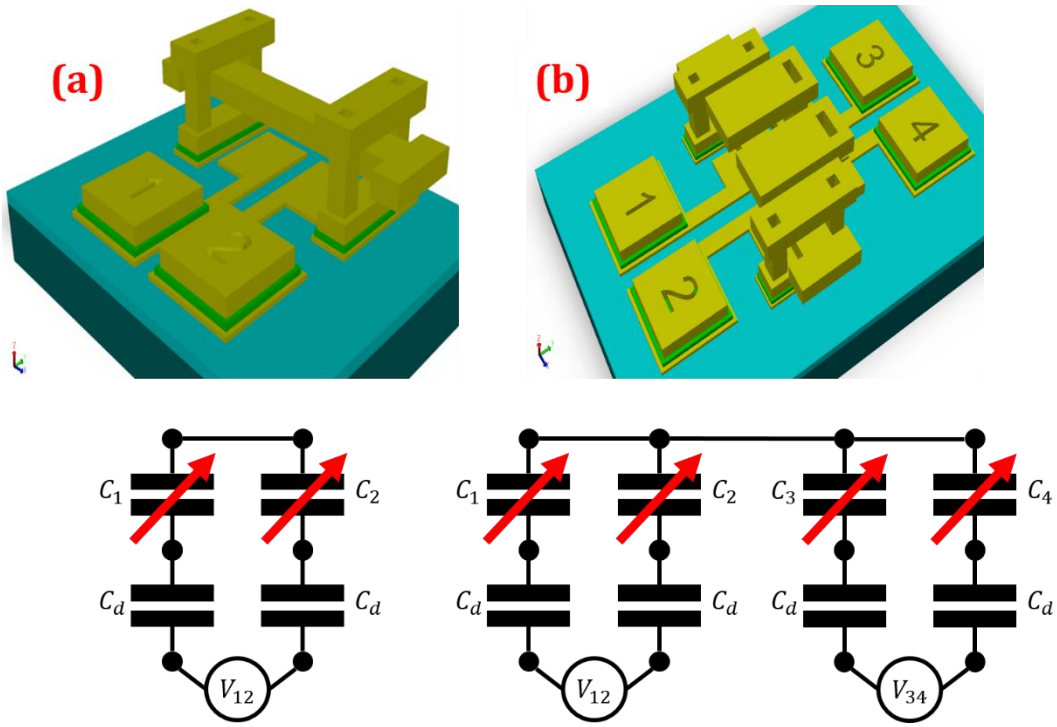


Fig 5.31: Illustration of the remote electrostatic actuation (REA) for: (a) single-actuator switch; (b) two-actuator switch

If any actuation voltage difference V_{12} is applied between pads 1 and 2, it will then be applied between the two electrodes underneath the GC beam through the dielectric capacitances used typically for short circuit protection of the actuation voltage source. C_d is the capacitance across the dielectric layers, and C_1 and C_2 are the capacitances in air between the electrodes and the beam material. Typically, C_d is much larger than C_1 and C_2 such that the overall capacitance is equal to the series combination of C_1 and C_2.

Eq. 5.21 gives the attractive electrostatic potential energy U_{12} of the system, where C_{12} is the overall capacitance across the two terminals of the voltage source. The energy is deflection dependent, which is the physical reason behind the attraction of the various beam sections towards the electrodes under constant V_{12} in order to take the overall potential energy to its lowest possible. The deflection-dependent actuation force F_{12} and electrostatic stiffness K_{12} are provided in Eq. 5.22 and Eq. 5.23, respectively, assuming that the deflection towards the electrode is x.

$$\boldsymbol{U_{12} = -\frac{1}{2}C_{12}{V_{12}}^2 \approx -\frac{1}{2}\left\{\frac{C_1C_2}{C_1+C_2}\right\}^2 {V_{12}}^2} \qquad \text{Eq. 5.21}$$

$$\boldsymbol{F_{12} = -\frac{\partial U_{12}}{\partial x} = \frac{1}{2}\frac{\partial C_{12}}{\partial x}{V_{12}}^2 \approx \frac{1}{2}\frac{\partial}{\partial x}\left\{\frac{C_1C_2}{C_1+C_2}\right\}^2 {V_{12}}^2} \qquad \text{Eq. 5.22}$$

$$K_{12} = \frac{\partial F_{12}}{\partial x} \approx \frac{1}{2}\frac{\partial^2}{\partial x^2}\left\{\frac{C_1 C_2}{C_1+C_2}\right\}^2 V_{12}{}^2 \qquad \text{Eq. 5.23}$$

If the conventional electrostatic actuation is compared to that in the REA mechanism, and assuming the existing symmetry, and a perfectly valid parallel-plate approximation, it is obvious that there is a need in the latter scheme to apply double the voltage difference in order to have the same deflection, ideally. For the cases where the actuation voltage is doubled, such disadvantage in terms of the voltage-budget is overshadowed by another advantage of the REA technique that lies in the fact that a relatively much more conductive beam (e.g. short circuit) can be actuated independent of its electrical signal or voltage level relative to another circuit. To understand this issue from the perspective of electrical circuits, it is informative to consider the double-sided REA scheme in Fig 5.31. The pads 3 and 4 provide the actuation voltage to the upper (suspended and rigid) electrodes in the same way the pads 1 and 2 are connected to the substrate or lower electrodes.

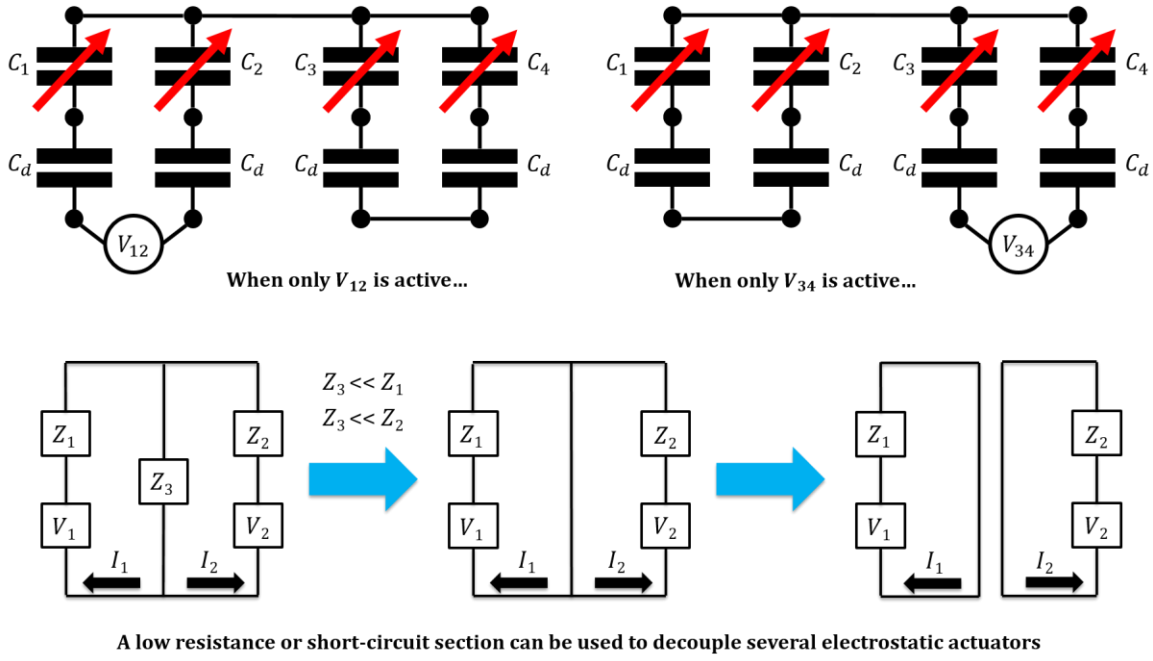


Fig 5.32: Illustration of the electrical decoupling of more than one electrostatic actuator using REA

Supposing that two different voltage sources V_{12} and V_{34} are connected across the pads {1, 2} and the pads {3, 4}, respectively, and that the two voltage sources are completely decoupled in the sense that they don't have the same voltage reference or ground, the equivalent circuit of the entire structure is displayed in Fig

5.31. The entities C_3 and C_4 are the air capacitances between the upper electrodes and the GC beam, in a similar way to how C_1 and C_2 were defined for the single-actuator device. Fig 5.32 displays the lumped circuit model for the case where V_{12} is active and the circuit model if V_{34} is active. For more than two sources of current or voltage, only one source would be activated in the analysis at a time according to the basic circuit theory by virtue of the superposition technique. The electrical equivalent of the beam sustains complete decoupling between the two sets of electrodes such that both voltage sources are not affecting each other's loading capacitance by any means.

The circuit analysis reveals the fact that each circuit can function completely independent of the other one, and they can then be separated in terms of electrical analysis and modeling as in Fig 5.32. The results of this analysis do not only show the possibility of implementing electrostatic suspension or restoring force that is fully decoupled from an electrostatic actuating force, but it also proves the advantage highlighted above that is the independence of one or more actuation circuits from the signal carried by the switched beam. The decoupling between the circuits for the upper and lower parts of the beam can also be demonstrated by examining the overall capacitance at the terminals of each voltage source. Eq. 5.24 and Eq. 5.25 give the electrostatic potential energies U_{12} and U_{34} contributed by each source, where the notation is consistent with the same notation employed in Eq. 5.21.

$$\boldsymbol{U_{12} = -\frac{1}{2}C_{12}{V_{12}}^2 \approx -\frac{1}{2}\left\{\frac{C_1C_2}{C_1+C_2}\right\}^2 {V_{12}}^2} \qquad \text{Eq. 5.24}$$

$$\boldsymbol{U_{34} = -\frac{1}{2}C_{34}{V_{34}}^2 \approx -\frac{1}{2}\left\{\frac{C_3C_4}{C_3+C_4}\right\}^2 {V_{34}}^2} \qquad \text{Eq. 5.25}$$

The overall capacitance from a given actuation circuit is solely affected by the capacitances through the air gaps between its respective electrodes and the beam being actuated. In addition, the parasitic capacitances due to overlap areas of upper and lower electrodes are negligible. Additionally, there can be no direct capacitance between the electrodes at the bottom with their opposing electrodes on top because the voltage sources are fully decoupled from each other in terms of voltage references, so it is meaningless to expect capacitances between them. The force and electrostatic stiffness for each set of electrodes are derived exactly as in Eq. 5.22 and Eq. 5.23, respectively.

5.4 New Post-Processing of a Modified UWMEMS Process

Referring to the standard UWMEMS process and post-processing discussed earlier, it can be seen that the implementation of GC structures would be possible by means of sacrificing at least the first dielectric layer

(i.e. D1 as defined previously). For instance, the wet etching of the polymer (using EKC 265, Kwik Strip, etc.) followed by wet etching of the dielectric layers (using buffered HF) can be performed. Aside from the limited choices of materials to be involved in the UWMEMS processing steps, there are some important drawbacks for sacrificing the dielectric layer(s) in the standard process. The first drawback lies in the absence of a thick enough layer underneath the first metal layer, M1. Such layer would be needed for the implementation of a post. The thickness of the resistive layer could be increased significantly up to 0.5µm depending on the resistivity of the material used. However, all the depositions performed are largely conformal, especially for the dielectric layers where chemical vapor deposition (CVD) is employed.

Another major drawback is the inevitable stripping of the second dielectric layer, D2, while wet etching the first dielectric for the sake of releasing M1. Such attack would set a strong limitation on implementing several switch architectures, especially the capacitive switches and capacitor banks where the only layer for building MIM capacitors is D2.

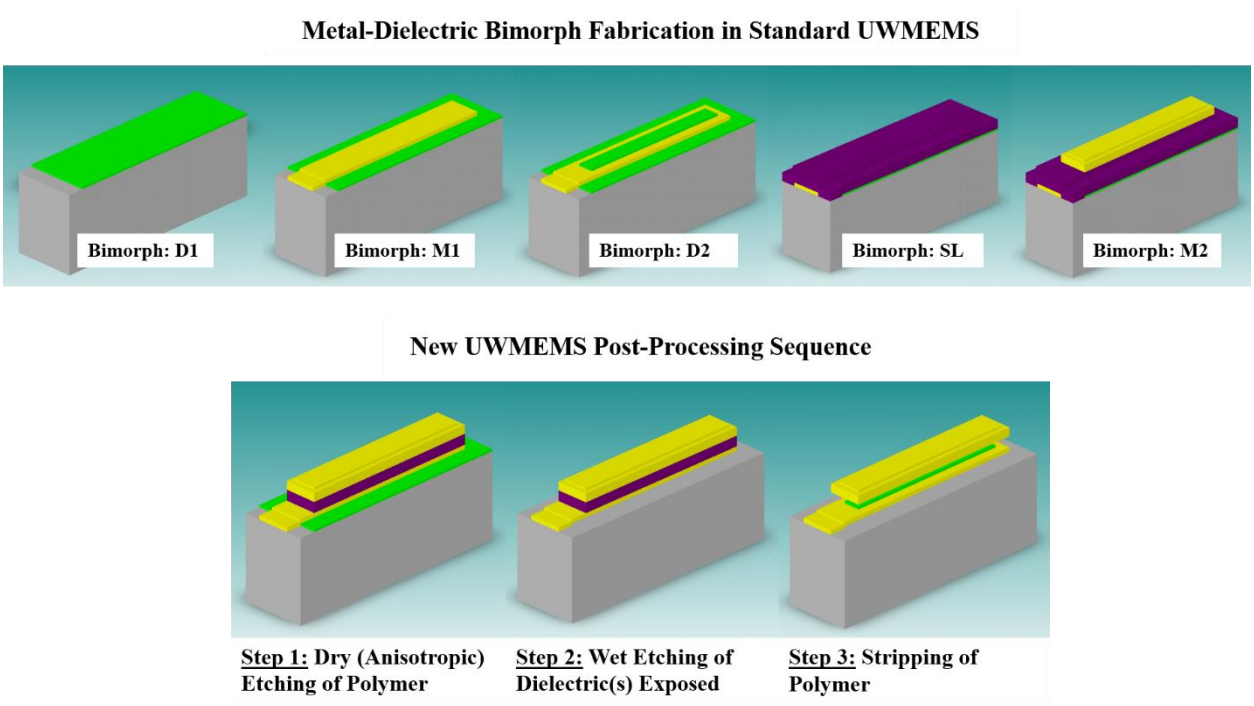


Fig 5.33: Bimorph microfabrication in standard UWMEMS process and a new post-processing sequence enabling more architectures and capabilities for MEMS devices

In view of such drawbacks, there is a need to modify at least the post-processing sequence. It is also possible to change the process, but it is highly advantageous not to introduce extra physical layers / masks as well as to keep such modified or expanded post-processing mask-less in order not to induce more fabrication

complexity, which would result in yield degradation normally. An efficient approach to prevent the inevitable attack of the D2 layer while wet etching D1 is to use dry etching of the polymer sacrificial layer such that the D2 features are encapsulated and protected by the polymer. The new post-processing sequence then should start with the dry etching of polymer and end with the wet etching of the polymer (as in the standard post-processing). The new and more general post-processing technique is illustrated in Fig 5.33 where a novel switch architecture is used for the demonstration of the developed technique.

In the figure, a switch beam on the M2 layer can be released along with an underlying bimorph made of M1 and the protected / encapsulated D2 layer. The demonstrating architecture is actually the core building block for a novel low-voltage electrostatic actuator that is restored electro-thermally. In fact, the entire switch operation would be relatively low power due to the fact the thermal actuation is pulsed, and there is no need for employing mechanical /electrostatic latching for the sake of suppressing the power consumption as in [73-76]. The design and results for that type of switches with thermal restoration is provided in a following section in this chapter.

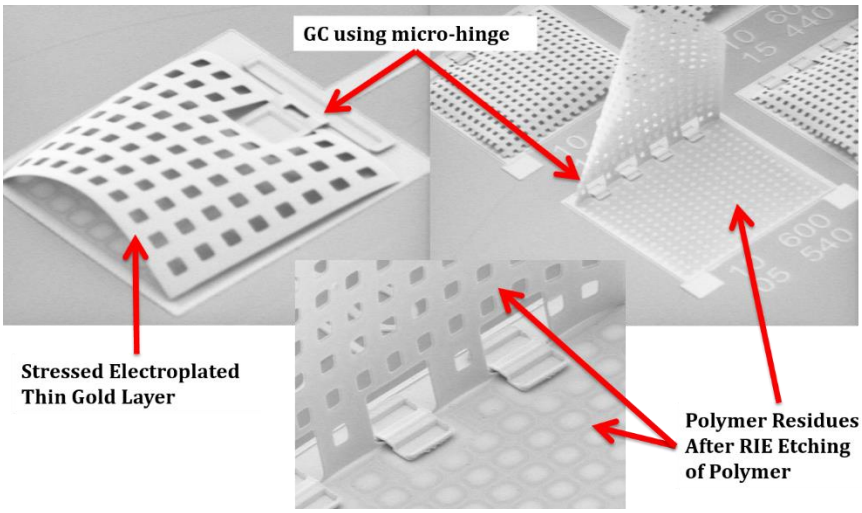


Fig 5.34: SEM pictures of fabricated GC repulsive electrostatic test structures demonstrating the overheating stresses encountered with dry stripping of the polymer sacrificial layer in RIE

At this stage, it should be noted that prolonged dry etching or dry stripping of the sacrificial polymer could be seriously problematic, especially for the release of the MEMS switches. In fact, the extended bombardment would tend to over-heat the structural layer in a way such that it ends up warping due to residual stress. The resulting plastic deformation shown in Fig 5.34 could still be very useful in terms of fabricating initially bowing / warped plates, e.g. curved beams for higher stiffness / restoring mechanical force. In addition, the dry stripping would generally be associated with polymer re-polymerization residues

as shown in the figure. Such residues cannot be tolerated for contact-type switches, and using wet stripping of the polymer sacrificial layer would still be required.

It is worth mentioning that the wet stripping of the dielectric layer(s) would necessitate drying the chips using liquid CO2 in CPD. This means that the dry stripping of the polymer sacrificial layer would not result in an increase of the post-processing yield. In the case of initially warped / stressed structures, the post-processing would be: (1) dry etching of polymer for encapsulation, (2) wet stripping of exposed dielectric layer(s), (3) dry stripping of the sacrificial layer, (4) optional wet stripping step to ensure the absence of polymer residues, (5) drying of chips in CPD.

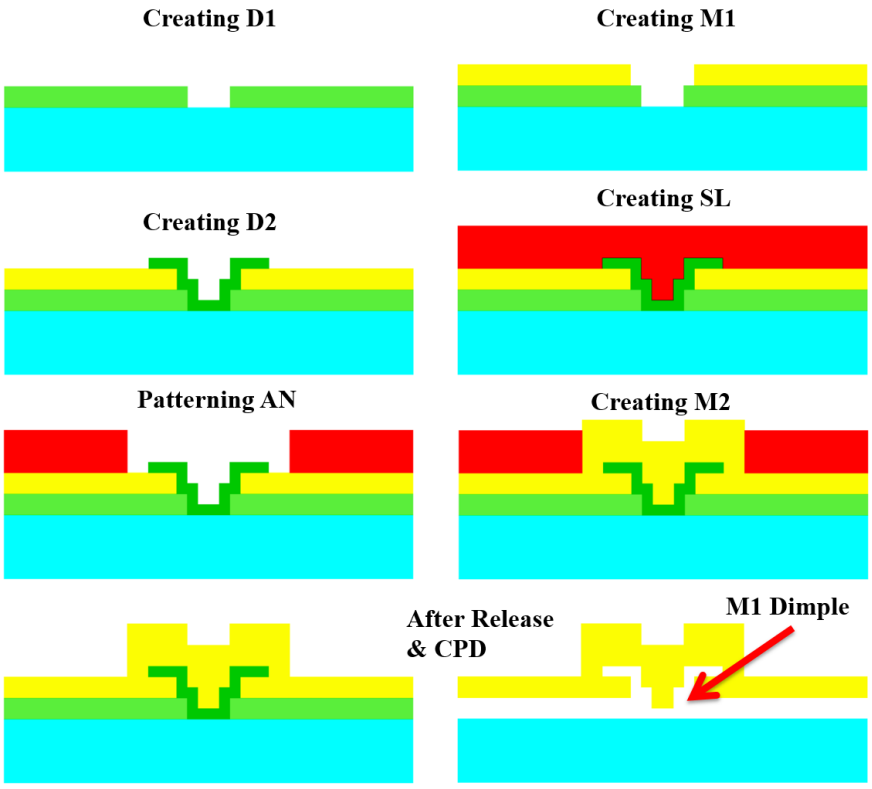


Fig 5.35: Modification of the standard UWMEMS process allowing the implementation of a dimple for the first metal layer. The spinning of the polymer is assumed planar for simplicity. The M1 dimple thickness is the difference between the D1 and D2 thicknesses

So far, the challenge in terms of the attack of the second dielectric layer (D2) has been addressed, but there is still a need to address the challenge with implementing a post underneath the first metal layer upon release. Actually, a dimple for the M1 layer is a reasonable solution. In the standard process, the layer DI includes all the dimple openings in the sacrificial polymer before the deposition and patterning of the M2 structural layer. Following the same procedure would result in adding an extra mask and the corresponding

depth-controlled etching in the first dielectric layer. In order to prevent such added complication and cost, UWMEMS process would only need to be modified in terms of the thickness of the first dielectric. Making the first dielectric layer thicker than the second dielectric layer as demonstrated in the cross-sections of Fig 5.35 allows the fabrication of a second dimple / protrusion for M1 layer if an anchoring between of M2 and M1 exists (~ 30-50µm depending on the layout design rules).

In fact, in the standard UWMEMS process, the thicknesses of the first and second dielectric layers has been equal (~ 0.5-0.7µm). However, the thickness of the second dielectric is the critical thickness in the process in terms of MEMS / RF design due to that it is the main parameter controlling the capacitance density for a UWMEMS MIM capacitor (e.g. in capacitive switches or capacitor banks). If the thickness of the first dielectric increases by ~ 0.5µm, the net topography increase on the UWMEMS wafer would be negligible while the DC short circuit protection for electrostatic actuation is further improved in terms of immunity to charging and breakdown. The dimple depth for M1 structural layer would be equal to the difference between the thicknesses of D1 and D2 dielectric layers.

In view of the previous discussion in this section, an enhanced process and a generic post-processing method has been introduced. Due to such significant expansion of the process, in the following sub-sections, the design and simulation results of more UWMEMS devices are presented.

5.4.1 GC Pinned-Pinned Shunt and Series SPST Switches

The GC pinned-pinned SPST RF MEMS switches can be used efficiently to build RF MEMS switches with interesting decoupled actuation and relatively high power handling capabilities in conjunction with high RF isolation in the OFF state. The proposed GC switches can be implemented using microstrip or CPW lines with shunt contact-type or capacitive switching. In addition, they can be implemented in series contact-type switching. The different schemes for implementing the shunt and series switches are displayed in Fig 5.36.

In scheme 1 for the shunt switch, the REA voltage difference for switching is applied directly through the CPW signal line and its ground planes. On the other hand, in scheme 2, a better design of the shunt switch is demonstrated. If the voltage difference between the signal line and ground planes does not contribute significantly to the actuation or ON-switching of the device, the switch would exhibit better high-power handling capability. The restoring or power-balancing electrodes in the figure can serve to induce out-of-plane deflections away from the substrate for the sake of lower capacitive loading of the signal line in shunt switching or higher isolation in the OFF state of the series switch. In fact, this does not only suppress the propensity towards self-actuation due to high power transmission in the shunt switches, but it also improves the matching of the line by minimizing the capacitance between the signal line and its ground plane through the shunting metal beam, i.e. it allows achieving higher ratio of down-state to up-state capacitances.

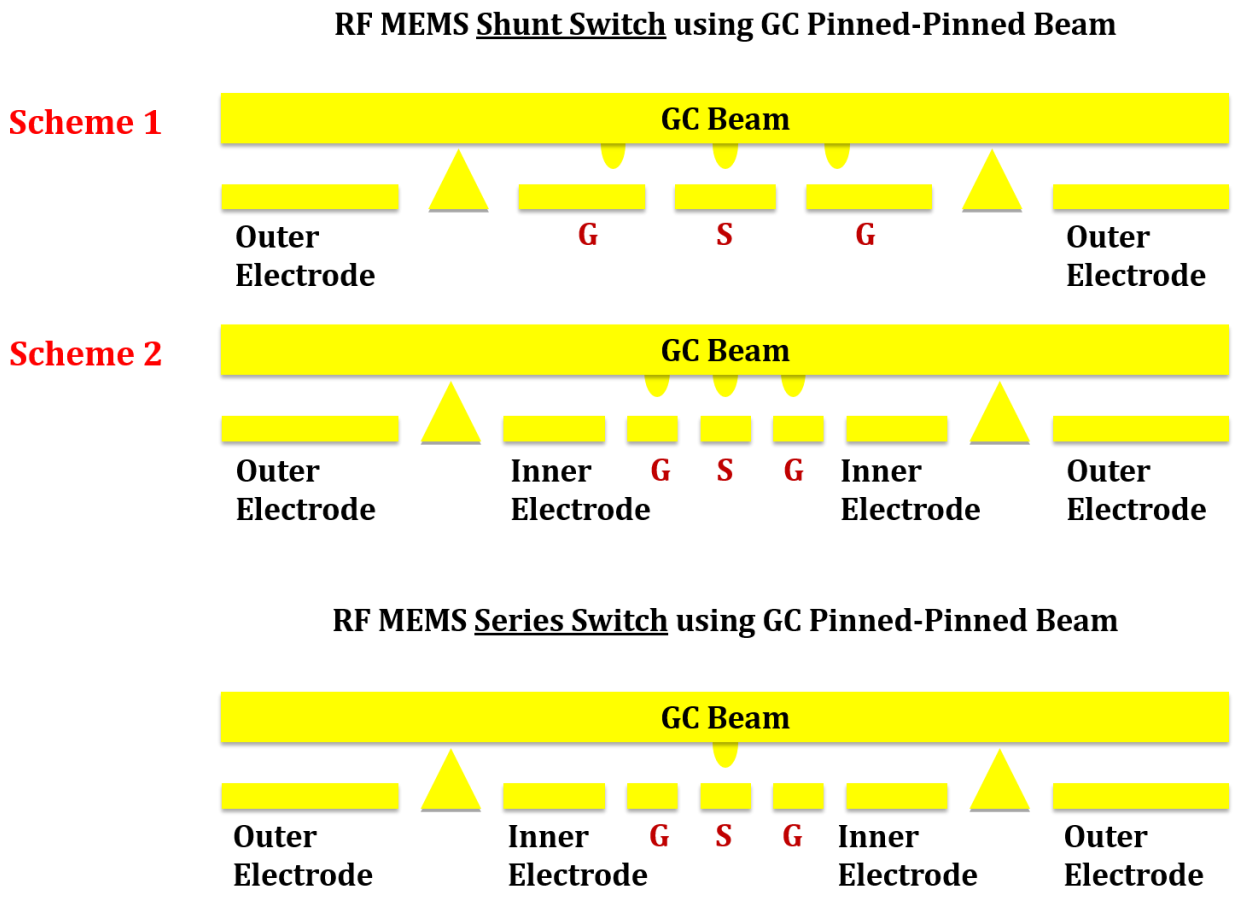


Fig 5.36: The different schemes for the implementation of the shunt and series SPST switches using GC pinned-pinned

It is expected that the pinned-pinned beam is remarkably less stiff as compared to clamped-clamped beam with the same device footprint. The mechanical restoring force would tend to be weaker for the thin gold-based membranes fabricated in the UWMEMS process [77]. The fact that the beam is anchored necessitates not only bending it, but also stretching it axially (i.e. mid-plane stretching). The associated nonlinearity and hardness is higher accordingly [44, 45].

In Fig 5.37, the RF shunt switch is designed for 50Ω line impedance. The width of its signal line is 90μm, and the gap between signal line and ground plane is ~ 45μm. The width of the ground is 135μm. The pull-in voltage is around 24V for the clamped-clamped beam with the same dimensions. For the pinned-pinned GC beam, the pull-in voltage simulated is ~ 10.6V. The fact that the required actuation voltage is reduced by more than 50% means that the electrostatic force associated is reduced by more than 75% for the fact that the electrostatic force proportional to the squared voltage difference. The first generation of the switch shown in the figure. The measured pull-in voltage for many identical devices was between 11-15V.

In the figure, the pull-in performance revealed by the static deflection of the mid-point of the 2µm beam is compared to that of 3µm, 4µm and 5µm thick beams, and the impact of the restoring / balancing outer electrodes on the midpoint deflection, eigenfrequency and pull-in voltage of the beam is displayed.

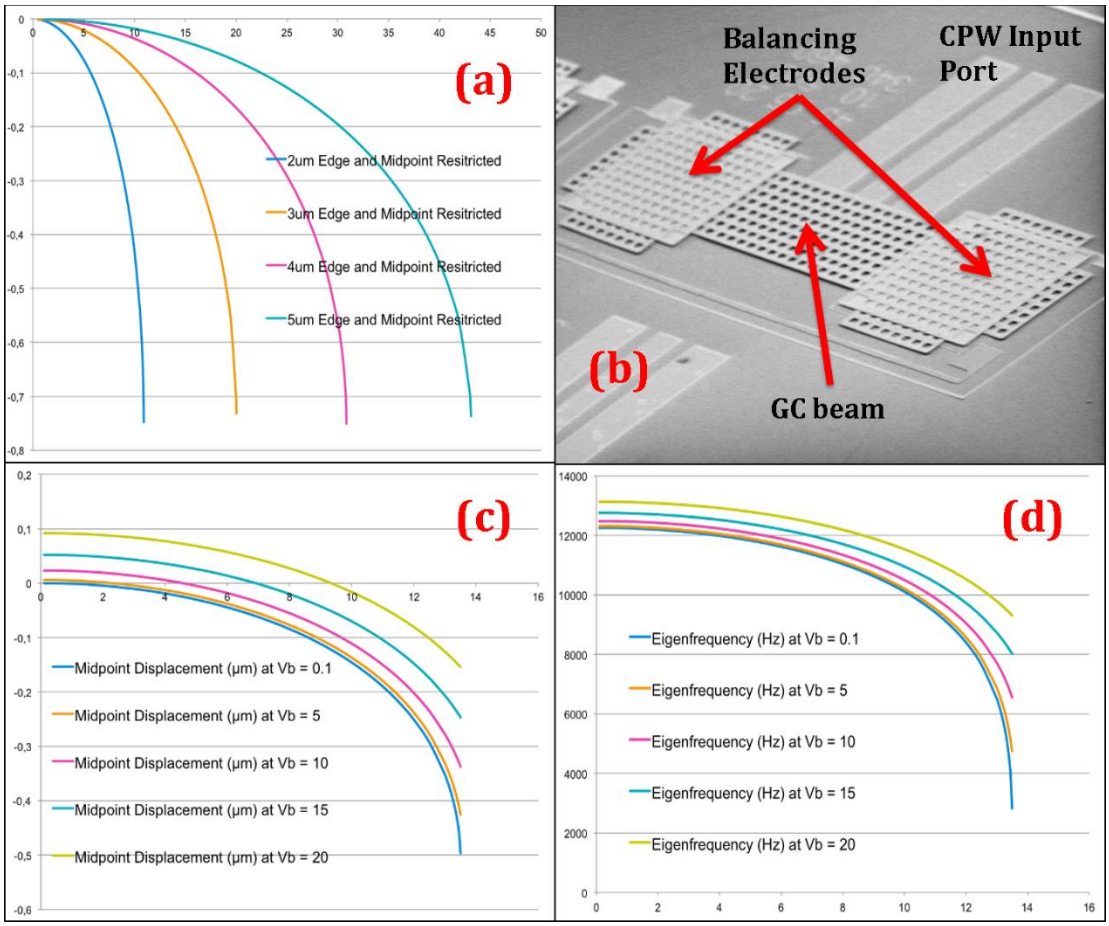


Fig 5.37: COMSOL electromechanical simulation results of the GC pinned-pinned beam and SEM of the first generation of the fabricated shunt switches following scheme 1. (a) impact of beam thickness on the pull-in voltage, (b) single-port shunt switch from first generation of fabrication, (c) impact of the restoring or balancing voltage difference on the GC beam midpoint deflection and the pull-in voltage for a shorter version of the switch, and (d) impact of the restoring or balancing voltage difference on the eigenfrequency and pull-in voltage

The electromechanical simulation reveals that little voltage difference between the beam and the balancing electrodes can shift significantly the pull-in voltage of the beam, thus affecting its high power handling capability. It is worth noting here that depending on the phase of the signal applied through the balancing electrodes relative to the actuation signal, it is possible to emulate a mass, damping or stiffness electrostatically, which is obvious from the phase relations between the different terms of an equation of

motion. Besides, the eigenfrequency analysis in the figure shows that the electrostatic tuning capability of the pinned-pinned beam if it is used as an autonomous oscillator, etc.

Simulating the pinned-pinned boundary conditions depends on the expected deflections in the beams with respect to the fabricated devices. If the beam is being actuated while the balancing electrodes are involved, no slipping can be assumed at the pin-supports. The electroplating process would generally result in rough pins (made by M2 gold layer). If the confined beam possesses a rough surface as well, it is more realistic to assume no slipping at the pins, even when the balancing electrodes are not used. In fact, the beam to be modeled is to be restricted at the points of intersection with the pins. Due to the symmetry, the midpoint of the beam can also be restricted in terms of in-plane motion. These assumptions were applied for the analysis results in Fig 5.37.

In fact, considering such boundary conditions in the case of GC pin-supported beams, a fundamental difference exists between pinned-pinned and clamped-clamped beams that is the difference between fixing the beam at the skin versus fixing the cross-section of the beam. This has a direct impact on the structural behavior of the beam in the presence of the electrostatic field. Partial clamping of the beam's extremities can be used to study such difference using FEM analysis. It can be found that the pin-support condition with the encountered skin fixation rather than clamping necessitates the violation of the basic assumptions of the Euler Bernoulli equation, where clamping is assumed [44, 46], which is clear in the general Euler Bernoulli equation. Furthermore, in view of the aspect ratio of the length of the GC beam considered to its thickness, Timoshenko's model cannot be considered.

Based on the discussion above, the design of GC pinned-pinned SPST series switch is demonstrated in Fig 5.38, and the 3D electromagnetic simulation results in HFSS are provided in Fig 5.39 and Fig 5.40 for the ON and OFF states, respectively. Obviously, the matching and overall RF performance of the switch can be tuned well up to 20GHz even though the relatively wide plate (~ 300μm) becomes part of the signal line when the switch is in the ON state. In fact, the tuning of the RF performance takes into consideration the resulting stub. Since the OFF state involves two contacts in series that are open, the good isolation performance in Fig 5.40 is expected.

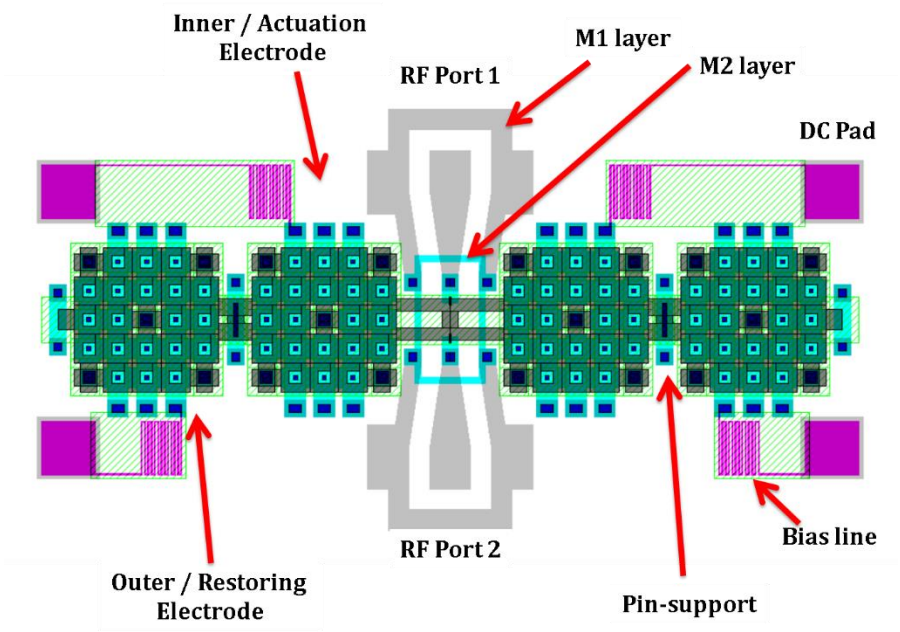


Fig 5.38: Design of GC pinned-pinned SPST switch using the expanded UWMEMS process and new post-processing

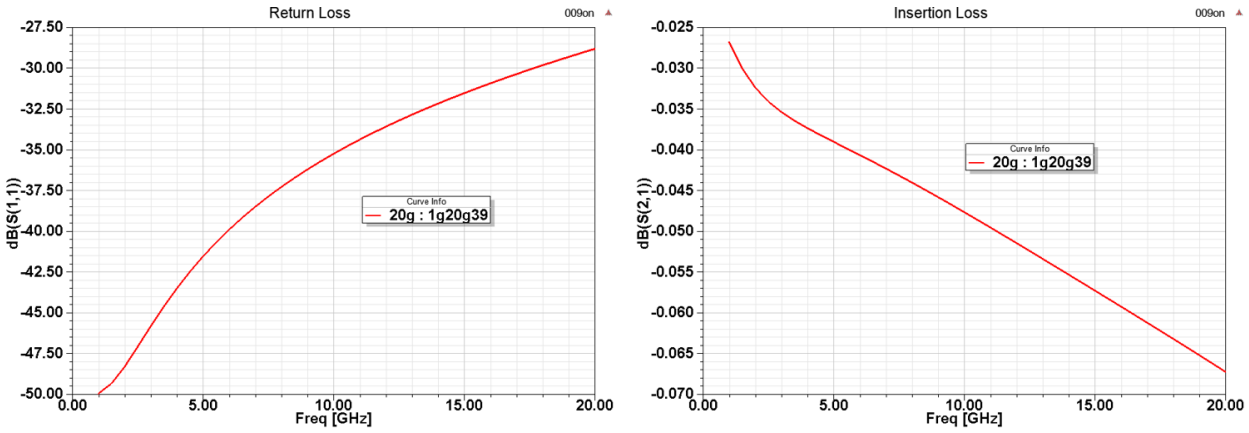


Fig 5.39: 3D electromagnetic simulation results in HFSS for the GC pinned-pinned SPST switch in the ON state

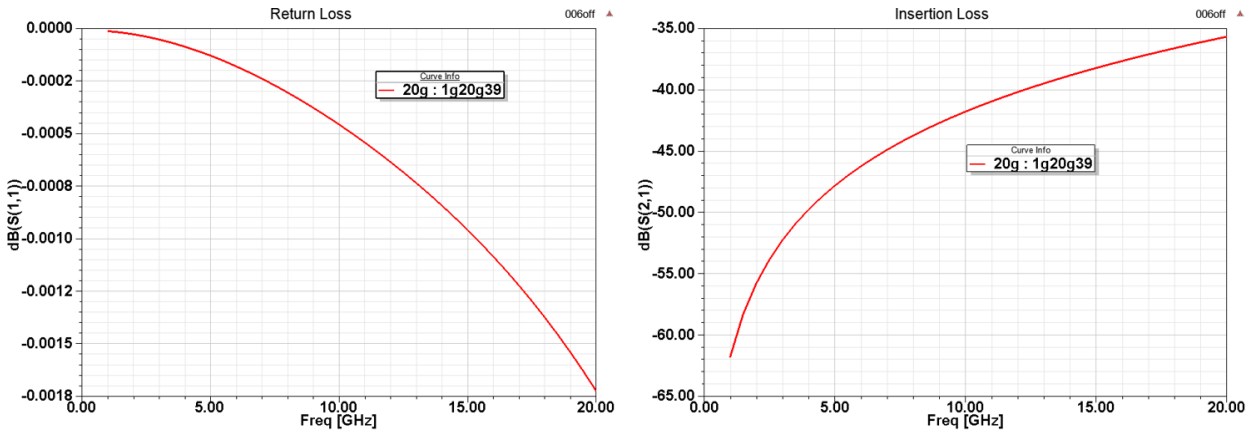


Fig 5.40: 3D electromagnetic simulation results in HFSS for the GC pinned-pinned SPST switch in the OFF state / isolation

5.4.2 Thermally Restored Switch (TRS)

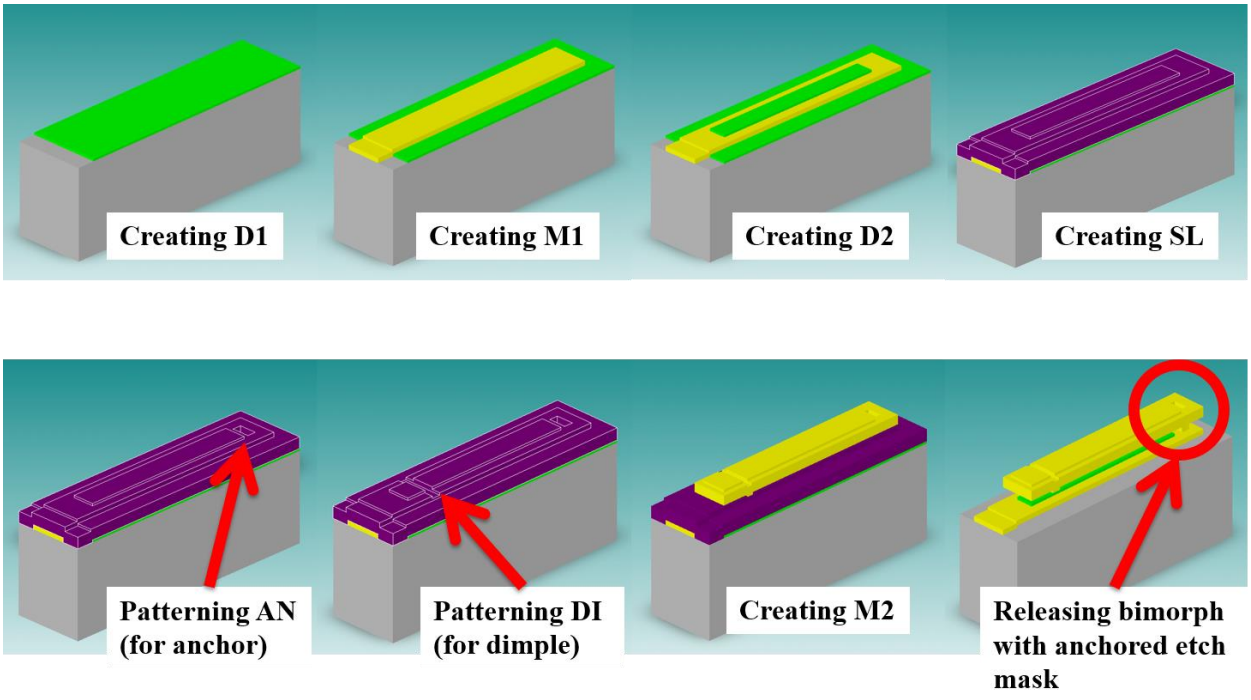


Fig 5.41: Bimorph microfabrication in the expanded UWMEMS process and the expanded post-processing approach. The dry etch-mask feature on M2 is anchored to the structural M1 feature of the M1-D2 bimorph

As mentioned previously, the new and more general post-processing sequence that was developed in this work (see Fig 5.33) allows fabricating M1-D2 bimorph structures that can be used in building different types of switches. However, the M2 features cannot be totally disconnected from the released structures as illustrated in Fig 5.33. In fact, it is possible to anchor the etch-masking M2 feature to the M1 beams as demonstrated in Fig 5.41. Using such architecture, staggered bimorph actuators can be easily built, as shown in Fig 5.42 by means of the CoventorWare thermomechanical simulation. It is clear that deflections of more than 100µm and out-of-plane deflection angles of ~ 90º can be easily achieved. Such specifications would be crucial for fabricating waveguide MEMS switch as in [84, 85] as well as very high-isolation switches that would very attractive for mmWave frequencies and above.

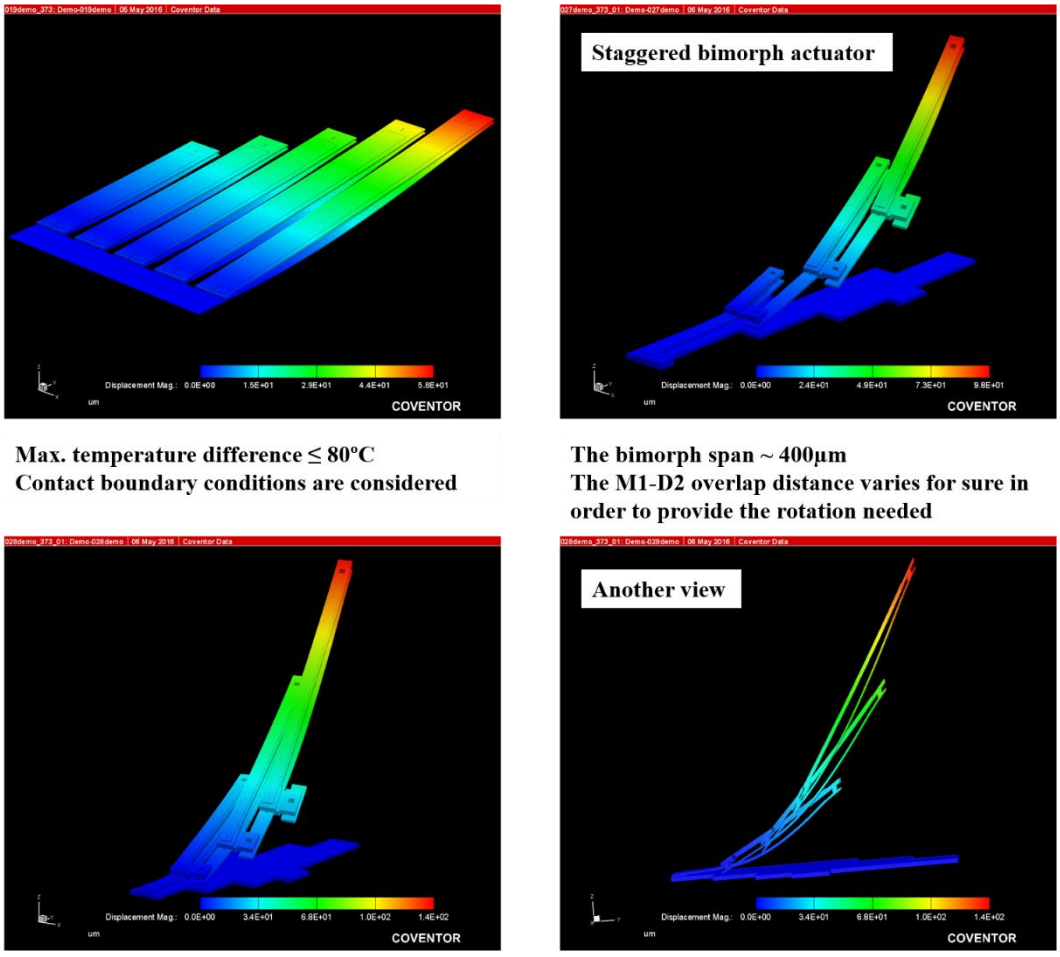


Fig 5.42: Coventor thermo-mechanical simulation results of the metal-dielectric UWMEMS bimorph. A more typical implementation would be practically based on electro-thermo-mechanical actuator (i.e. with the metal as micro-heater). It would be even more practical to implement such approach for the staggered bimorph actuator

Moreover, it is possible to use the same etch-masking M2 feature as part of the structural layer of a series switch that the switch can be electrostatically actuated using low voltage and restored with a pulsed thermal actuation. This allows the switch to exhibit high RF performance while consuming low power / energy. The operation of such thermally-restored switch (TRS) is illustrated in the Coventor electro-thermomechanical simulation results in Fig 5.43.

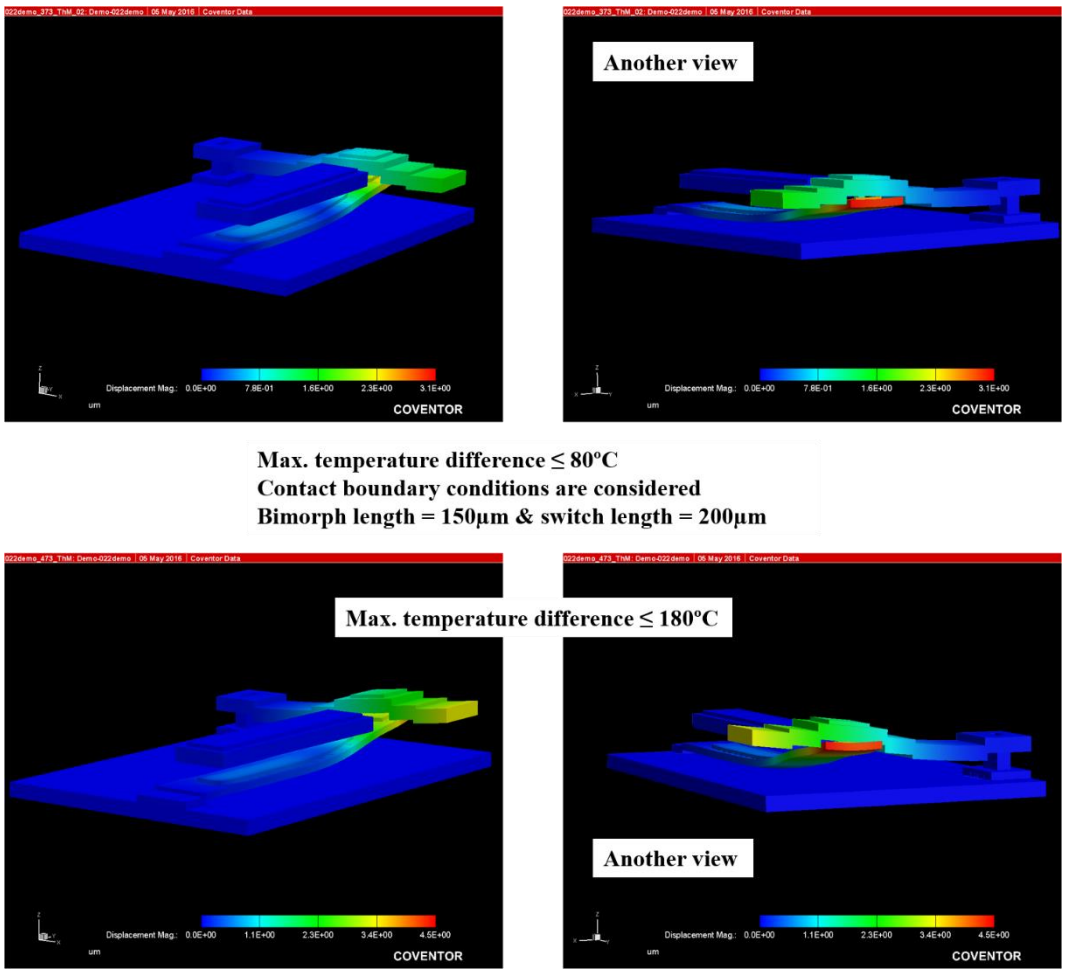


Fig 5.43: Coventor thermo-mechanical simulation results of the metal-dielectric UWMEMS bimorph for the thermal restoring function the series switch

As a matter of fact, using the bimorph would necessitate having the restoring beam as an RF ground, which can cause capacitive loading on the signal line at the overlap between the bimorph and the clamped-free beam that is part of the signal line. However, the little overlap required for the restoring force and the presence of the D2 dielectric on top of the beam does not allow such loading capacitance to affect the

overall performance. The 3D electromagnetic simulation results of a TRS design in the ON and OFF states are given in Fig 5.44 and Fig 5.45, respectively.

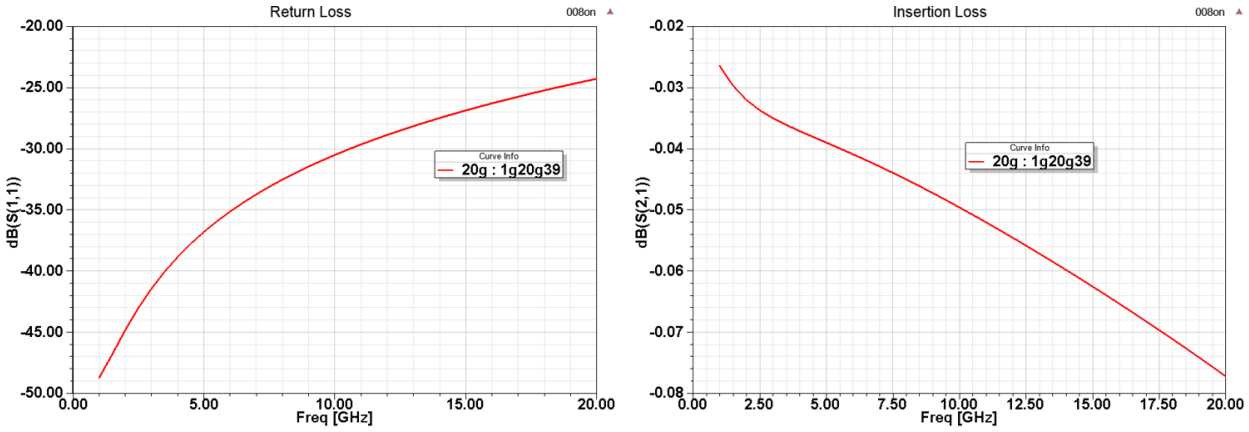


Fig 5.44: HFSS electromagnetic simulation results for the proposed TRS design in the ON state

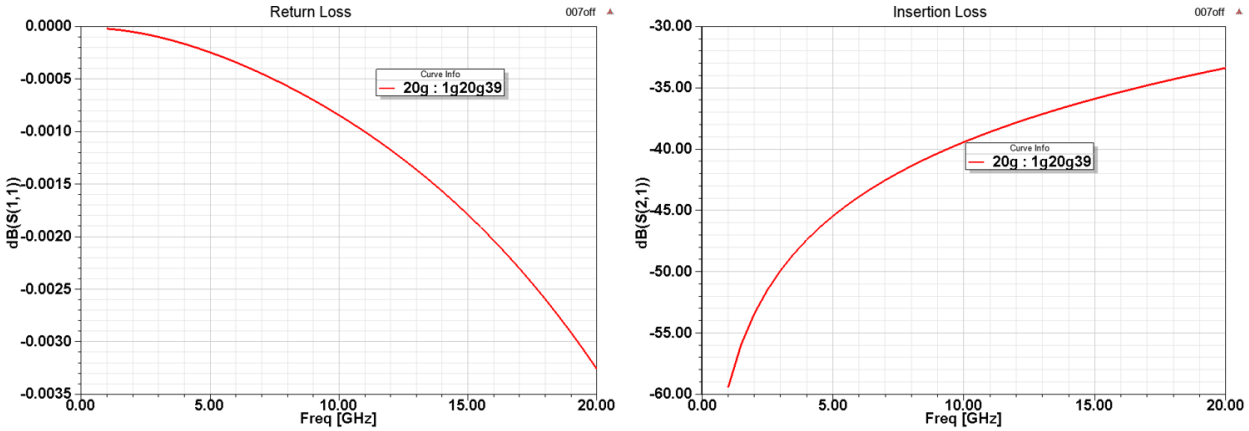
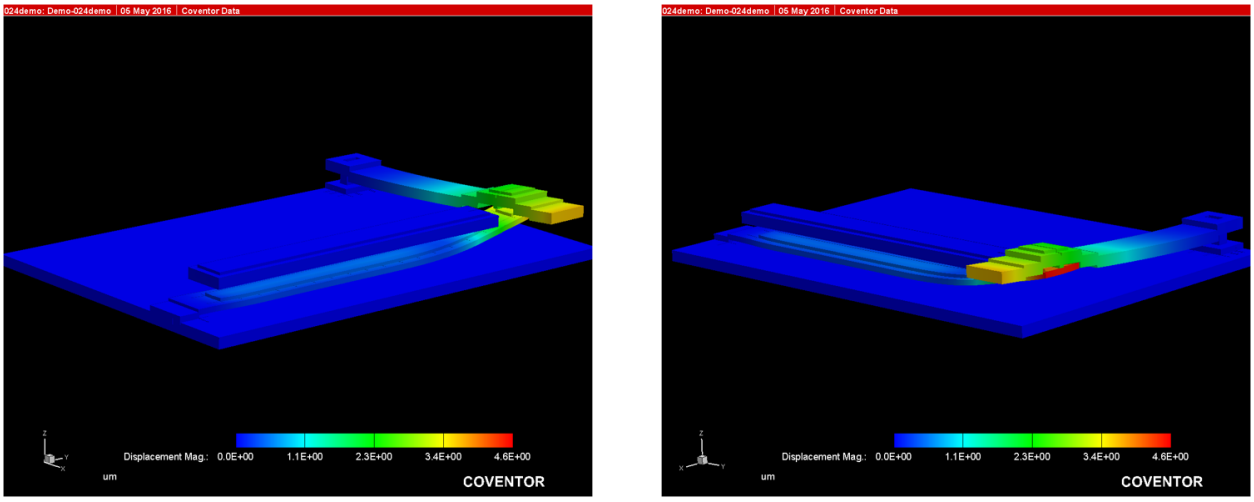


Fig 5.45: HFSS electromagnetic simulation results for the proposed TRS design in the OFF state

Since the device size is generally compact, increasing the length of the bimorph section would not affect significantly the overall switch footprint in a negative way; however, it can help limit the maximum temperature across the M1-D2 bimorph, which would certainly improve the reliability of the switch. The temperature difference becomes clear by comparing the CoventorWare results in Fig 5.46 with the results in Fig 5.43.



Max. temperature difference ≤ 80°C
Contact boundary conditions are considered
Bimorph length = 300µm & switch length = 300µm

Fig 5.46: Coventor thermo-mechanical simulation results of the metal-dielectric UWMEMS bimorph with longer bimorph and switch in order to reduce the maximum working temperature for higher reliability

Chapter 6: Si-Core RF MEMS Switches with Wafer Level Packaging

NOTE: "All the content of this chapter is confidential as per a Non-Disclosure Agreement (NDA)"

In this chapter, several packaged silicon-core (Si-core) RF MEMS switch designs are presented. In the first section, the concept of Si-core MEMS switches is explained. In section 6.2, the proposed microfabrication process employing wafer level packaging (WLP) towards hermetic sealing is analyzed in terms of the main fabrication steps. Section 6.3 analyzes the major RF and electromechanical design considerations in view of the constraints imposed by the proposed fabrication process and the associated material properties. Finally, section 6.4 summarizes the main simulation results for a group of different switch designs undergoing microfabrication as part of the first generation of devices.

6.1 Si-Core MEMS Switches

The term "Si-core" refers to a class of MEMS switches where the core or the main constituent of the suspended structural layer is made of silicon, more precisely or ubiquitously, crystalline silicon [91]. Typically, the silicon structural layer is coated with a thin metal layer that is required for implementing MEMS switches and building the RF circuits as well.

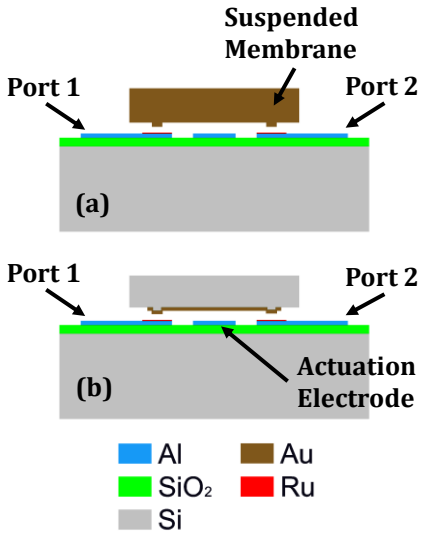


Fig 6.1: An illustration of a conventional MEMS switch using (a) plated thick metal membrane, (b) silicon-based membrane with thin metal coating. The contact is assumed to be Au-Ru, which is among the most reliable contact pairs reported

A simple comparison between an all-gold reliable switch (with typical thickness ~ 5-10μm) [90, 9] and a Si-core switch with the same thickness including a thin gold coating (with typical thickness ~ 0.5-1μm) reveals that adopting a Si-core architecture results in an overall reduction in the effective mass of more than 85 % in conjunction with an increase in the stiffness by a factor of ~ 2. Since the switching speed is proportional to the natural resonant frequency of the actuator [90], it can be found that the switching speed can be increased by a factor of ~ 4.

In addition to the guaranteed improvement of speed that can be coupled with further improvements by virtue of lowering the effective mass as well as damping using perforations, the overall mechanical fatigue and creep performance of the MEMS Si-core switch would be improved much due to incorporating crystalline silicon as the main constituent of the structural layer. Employing a plated metal would put strict constraints on the upper bound of the maximum deformation stress (upon actuation) if the reliability of the switch is concerned, and such maximum value is ~ 50MPa [9]. Such low level of stress necessitates generally the use of thick structural layers ~ 5-10 times the distance to contact (see section 6.3.2), which would result in a relatively high pull-in voltage or a significantly large footprint of the actuator if the pull-in voltage is to be reduced.

Moreover, the adoption of Si-core switches rather than metal-based switches allows for a smooth integration with other silicon-based technologies such as Through-Silicon-Via (TSV) and WLP [88, 89]. Packaging is certainly needed for the sake of close controlling the operating environment of the switch in order to have a reliable MEMS device, and together with TSV, a compact and highly reliable MEMS switch development platform can be developed.

Before proceeding with the proposed process for fabrication of the first generation of WLP Si-core switches in the next section, it is worth noting that one of the major drawbacks of using silicon as the core of the structural layer is the tendency towards the increase of the pull-in voltage for the same actuator footprint and forcing levels (i.e. contact and release / restoring forces). The analysis in section 6.3.2 clarifies that issue with lumped model analysis. Another drawback of Si-core switches lies in the need to relieve residual stresses that are inevitable with the physical vapor deposition (PVD) of metal thin films, especially if the thickness of the metal layer, ubiquitously made of gold for Au-Ru contacts [97], is to be ~ 1-2μm for acceptable RF performance at low frequency due to the larger skin depth. Without efficient thermal annealing or pulsed laser annealing [58, 59], the thickness of the silicon layer would need to be large enough in order to prevent unwanted initial warpage of the actuator membrane. It should be noted here that in an industrial process, plating of the metal layer would not be an option. Besides, plating of the metal layer would generally degrade the overall RF performance of the switch at relatively high frequencies due to surface roughness. Finally, another drawback lies in the fact that two contacts would be generally required

for RF MEMS switching. If the contact pressure is not high enough such that the contact resistance is low, the insertion loss can be negatively impacted.

6.2 Microfabrication Process Employing WLP

At this stage, it is evident that the targeted switch with the required hermetic sealing can be implemented easily by the adoption of Si-core topology and WLP. An example of an architecture for such a packaged switch is displayed in Fig 6.2. Referring to the literature survey in chapter 2, the contacting materials are selected to be Au and Ru in order to obtain the highest possible / reported contact reliability of the fabricated switch. Employing Au-Ru for the metal-metal contact switch necessitates the use of a comparatively large contact force in conjunction with a similarly large release or contact-breaking force [97]. As a matter of fact, this need suits more the choice of the Si-core topology due to the tendency of the actuator towards exhibiting large stiffness. As discussed later in section 6.3.2 of this chapter, designing the Si-core electrostatic actuator in order to operate with relatively large restoring forces (in the mN range) helps keep its footprint comparable to the switch with metal-based structural layer.

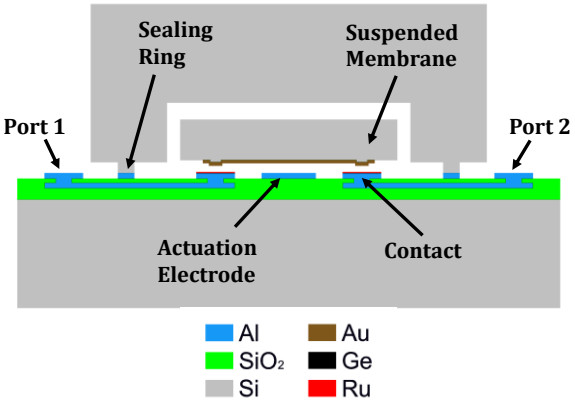


Fig 6.2: An example of the targeted RF MEMS switch being wafer-level packaged and operated by electrostatic actuation. The example does not consider the possibility of adopting TSV technology (for the first generation)

Stemming from the aforementioned advantages of Si-core RF MEMS switches, the design in Fig 6.2 assumes an all-silicon solution for the packaged switch where the main substrate carrying the RF circuit can typically be made of high resistivity silicon (HRS) in order to tune the overall matching and limit the insertion loss to acceptable levels. For the same reasons, the suspended membrane holding the switched metal connector should be made of HRS. Regarding the sealing wafer that should ensure the required

hermetic sealing, the option for low resistivity silicon (LRS) is still possible, which would be more attractive in terms of cost.

Moreover, assuming Al-based transmission lines as well would further suppress the overall cost of the switch while aligning more the process to standardized and mature microfabrication processes. Considering the use of Al-based alloys for the metal layers on the main substrate and silicon for the sealing / capping wafer, one of the very promising options for hermetic sealing would then be Eutectic bonding involving Al, and, in view of the thermal budget for such a critical WLP step, Al-Ge eutectic bonding seems to be a suitable compromise [93, 94].

It is worth noting that Fig 6.2 does not clearly show how the suspended membrane would be formed or anchored to the main substrate where the wafer and actuation electrode is present. However, the fabrication process, especially for the eventual scope of making a real product with competitive / affordable price, would be impractically complex and costly if a 2-step bonding process is employed. One possible solution – or perhaps the only practical solution – for that implementation bottleneck is to have the suspended membrane together with the sealing wafer as part of one silicon-on-insulator (SOI) wafer. Such SOI wafer would be fabricated in a non-conventional way though. Conventionally, the end result of SOI bonding process is a device layer (typically ~ 10-50μm) and handle layer (typically > 400μm) with a silicon dioxide layer between them (typically ~ 1-4μm). This stacking of layers would not allow the actuator membrane to be movable / released. As a result, the SOI bonding of the two wafers or silicon layers should take place after making a trench or cavity in the handle wafer. The architecture of the proposed switch in demonstrated in Fig 6.3, and the step-by-step microfabrication process is illustrated in the following.

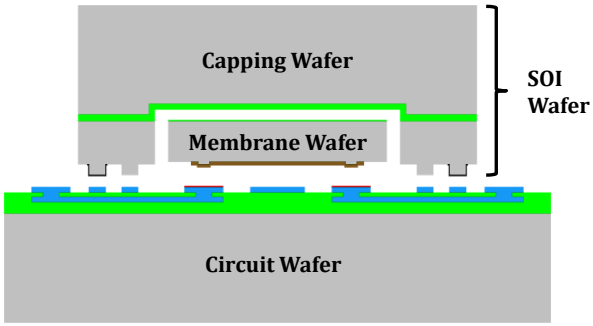


Fig 6.3: The proposed architecture of the first generation of the RF MEMS switch with WLP. The capping / encapsulation and membrane / MEMS wafers are both parts of one SOI wafer with an initially buried trench in the capping wafer

Furthermore, and considering the proposed architecture of the packaged switch in Fig 6.3, in order to have a high-yield bonding process while being able concurrently to ensure a precise control of the contact and

actuation gaps of the electrostatic actuators, at least one planarization step is mandatory. Additionally, there must be at least two metal routing layers for implementing a given circuit plus the necessary eutectic Al-Ge bonding due to the fact that the signal lines feeding into the sealed volume and leaving it cannot be shorted to the metal ring that bonds to the corresponding Ge ring on the capping silicon wafer. The bonding metal layer would then be as well the uppermost metal layer, which should be taken into account when the actuator is designed.

Before proceeding with the illustrated step-by-step description of the fabrication processes of the circuit and SOI wafers, it is worth noting that the secondary bump (i.e. without Ge thin film) on the SOI wafer in Fig 6.3 is present in order to act as stopper or a limiter for the Al-Ge bonding taking place at the primary bumps. That is how the final gap between the circuit wafer and the membrane / device layer on the SOI wafer can be precisely controlled. Similar to the uppermost Al-based layer and the Ge layer, the primary bump used for hermetic sealing must form a closed-loop path or a ring. However, depending on the size / area of the sealed volume, the secondary bump size and the pressure applied during the bonding operation, there can be only a need for a limited count of secondary bump, i.e. not making a secondary ring.

The first part of the microfabrication process of the packaged switch comprises the different steps of fabrication of the circuit wafer as well as its necessary planarization required for bonding. Fig 6.4 shows the first main step of the fabrication procedure where a thick-enough passivation layer of thermally grown silicon dioxide is prepared. In fact, this layer may not be required depending on the resistivity of the silicon wafer. For LRS substrate (typically ~ 1-50Ω.cm), the thickness of this layer would generally need to be at least 2-3µm in order to be able to provide acceptable matching. It should be noted here that using LRS for the substrate in conjunction with trenching under the signal line cannot be performed in this microfabrication process due to the encountered packaging.

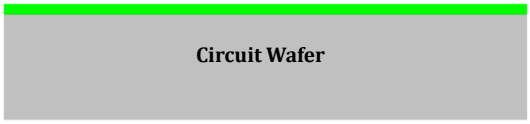


Fig 6.4: The first main step in the fabrication of the circuit wafer. A passivation layer of thermal oxide is grown

After growing the passivation layer, the first Al-based metal layer can be deposited by PVD. For low frequency operation, a coplanar waveguide (CPW) with a thickness ~ 1µm would exhibit an acceptable performance, and sputtering can be used for the deposition. This first metal layer is primarily used for

implementing transmission lines (micro-strip, slot-line, CPW, etc.), fixed actuation electrodes and routing for DC biasing. Fig 6.5 illustrates this fabrication step.

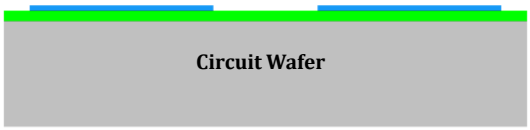


Fig 6.5: The second main step in the fabrication of the circuit wafer. The first Al-based metal layer is deposited by PVD. This is the main layer for building the RF circuits, implementing the actuation electrodes and crossing to and out of the sealed volume

After the patterning of the first metal layer, an insulating layer must be deposited in order to isolate the first and second metal layers from each other. A thick-enough layer of silicon dioxide can be deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD). That is due to the fact that chemical mechanical polishing (CMP) should be performed after the deposition. Fig 6.6 demonstrates that step. If the thickness of the first metal layer is 1μm and the thickness of the dielectric between the first and second metal layers is 0.5μm, the thickness of the deposited oxide layer should initially be at least 2.5μm. It is clear at this stage of the fabrication that the thickness of the first metal layer cannot be increased significantly due to the required planarization with a relatively high yield. Also, serious issues to due to stresses in the deposited oxide layer can be encountered.

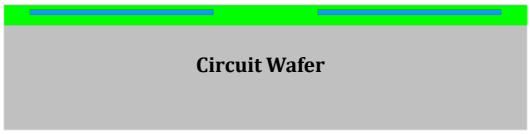


Fig 6.6: The third main step in the fabrication of the circuit wafer. A thick-enough silicon dioxide layer is deposited by PECVD then planarized by CMP in order to prepare for the deposition of the second metal layer and subsequent eutectic bonding

After the CMP is performed, the thin oxide layer on top of the first metal can be etched in the locations where direct contact with the second metal layer, i.e. via, is needed. This is displayed in Fig 6.7. Referring to Fig 6.3, it is evident that the routing to the second metal layer would be required for the sake of probing or bonding to the RF and DC pads, connecting to actuation electrodes (for the smallest actuation gaps, and, accordingly, the minimum possible pull-in voltage) and for the metal-metal contacts.

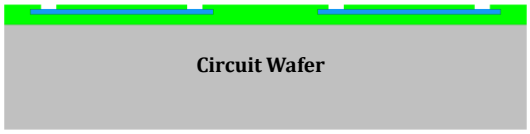


Fig 6.7: The fourth main step in the fabrication of the circuit wafer. The thin oxide layer between the two metal layers can be etched in the locations where via is needed

In Fig 6.8, after via patterning, the second metal layer PVD can be performed. Again, sputtering can be employed. It should be noted that a RF etch step would normally be required in order to ensure the direct contact between the first and second metal layers. Similar to the first metal layer, a thickness of ~ 1µm can be used for the second metal layer for the sake of an acceptable RF performance.

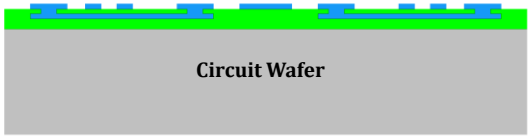


Fig 6.8: The fifth main step in the fabrication of the circuit wafer. The second metal layer is deposited. The cross-section assumes a planar fill for that second layer for simplicity, and a second planarization step is not necessarily implied

Upon the patterning of the second metal layer, the gold contacting material, i.e. Ru, on the circuit wafer can be deposited by PVD, which is demonstrated by Fig 6.9. Again, RF etch of the surface of the Al-based metallization layer would be required in order to provide a direct contact with the Ru thin layer. Based on literature on contact reliability using hard materials such as Ru, a thickness of ~ 0.15µm should be enough [17]. It is worth mentioning that prior to completing the actuator designs and starting the full fabrication, the thickness would need to be tested in short loops of deposition and indentation at typically attainable forcing levels (~ up to 100s of µN) [17].

The thickness and performance of the thin Ru layer is crucial for the contact reliability as well as the achievable overall insertion loss between the two connected ports in the ON state of the switch, especially that a minimum of two Au-Ru contacts in series is required for connecting any two ports. As highlighted in the first section of this chapter, this is one of the main drawbacks of adopting the Si-core topology for RF MEMS switches.

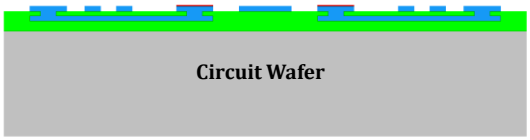


Fig 6.9: The sixth and last main step in the fabrication of the circuit wafer. The gold contacting material is deposited and patterned in the locations where the second metal layer is to make a reliable contact with the gold layer on the SOI wafer

At this stage, the fabrication of the circuit wafer is completed, and the second part of the entire fabrication process can be now discussed, which is the fabrication of the capping and membrane wafers in the form of one SOI wafer with a buried trench. In Fig 6.10, the capping wafer is first etched such that a cavity is formed at the back of the released membrane in the finalized MEMS wafer to be bonded to the circuit wafer. The depth of the trench can be set to ~ 10µm in order to reduce the squeeze-film damping exerted on the membrane while switching. This can positively affect the restoring time of the switch.

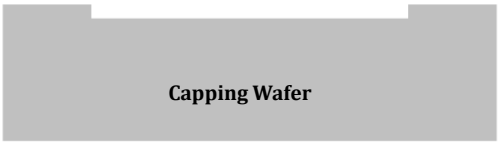


Fig 6.10: The first main step in the fabrication of the SOI wafer. A trench is made in the capping wafer in order to have the buried cavity in the SOI wafer upon the bonding of the capping and membrane wafers

It is worth noting here that etching deeper trenches would not have a significant impact on the dynamic performance of the switch, but it can affect the sealing yield in terms of changing the volume of the sealed cavity [93].

After the trench is patterned in the LRS capping wafer, a dielectric is needed in order to insulate the different anchor regions of the suspended structures. Otherwise, cross-actuation of the different switches may occur. That will be clearer in sections 6.3 and 6.4 where 3D illustrations of the actuators and switches are provided. A 1µm thermally grown silicon dioxide layer would be enough for DC / low frequency biasing. Fig 6.11 demonstrates that step.

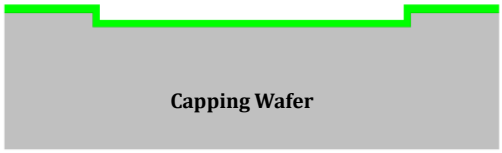


Fig 6.11: The second main step in the fabrication of the SOI wafer. An insulating layer of silicon dioxide is thermally grown on the capping wafer before bonding it to the membrane wafer

The preparation of the capping wafer is finished at this stage, and the membrane wafer can now be bonded to the passivated capping wafer in order to form the SOI wafer to be eutectic-bonded later to the circuit wafer. In Fig 6.12, the membrane wafer is oxide-bonded to the capping wafer then it is thinned down to the desired thickness of the membrane wafer in addition to the height of the anchor / stopper bumps.

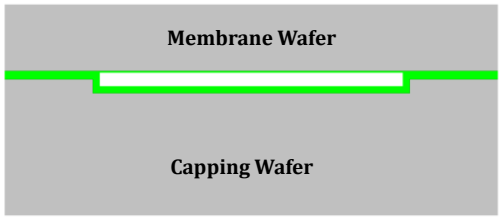


Fig 6.12: The third main step in the fabrication of the SOI wafer. The membrane wafer is bonded to the capping wafer and etching is performed on the membrane wafer in order to thin it down to the required thickness

Fig 6.13 shows the SOI wafer after further thinning of the wafer except for the areas where the anchor / stopper bumps are to be present. The height of the bump (i.e. the depth of silicon etching) depends on the required actuation gap, and it should take into consideration as well the thickness of the metal layer on the suspended membrane as well as the depth of the recess required for implementing the dimples for contact, which is illustrated in Fig 6.14. Referring to the topographies of the circuit and SOI wafers in Fig 6.3, the minimum electrostatic actuation gap – corresponding to the minimum pull-in voltage and actuation voltage budget – would be the distance between the surface of the second metal layer covered by the contact material on the circuit wafer and the metal layer on the suspended membrane.

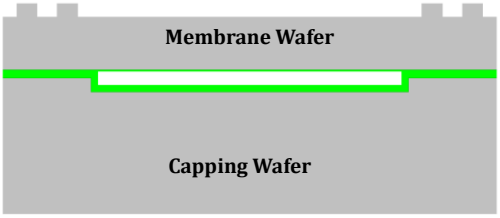


Fig 6.13: The fourth main step in the fabrication of the SOI wafer. The bumps for eutectic bonding and the stoppers are patterned in the membrane layer

Accordingly, the height of the bump is equal to the minimum actuation distance and the thickness of the metal layer after subtracting the depth of the recess or the height of the contact dimple illustrated in Fig 6.14. It should be noted that without the recess in silicon, not only the dimple cannot be implemented, but the minimum actuation distance would result in the collapse of the movable metal layer (on the suspended membrane) and the second metal layer on the circuit wafer. In section 6.3.2, the impact of the height of dimple on the electromechanical performance is analyzed for the special case where the actuation distance is minimum.

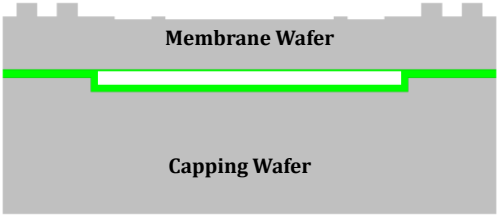


Fig 6.14: The fifth main step in the fabrication of the SOI wafer. A recess in the membrane layer is patterned in order to implement the contact dimples after the deposition of the metal layer

After the patterning of the bumps and the recess, the metal layer deposition and the Ge deposition can be performed, as demonstrate in Fig 6.15 and Fig 6.16, respectively. The deposition of the suspended metal layer is among the most critical steps of the fabrication process, and there are several reasons for that. First of all, the thickness of the metal layer affects significantly the actuation voltage as indicated previously, and it should be coupled with the etching depth of the bumps. Second, depending on the recess depth or

dimple height, which would affect the electromechanical in conjunction with the RF performance, a minimum PVD thickness is required in order to ensure an enough step coverage. Third, the residual stress after the deposition should be minimized. Otherwise, an initial warpage of the composite structural layer made of the membrane and metal layers can be problematic. That would depend on the choice of actuation gap and the membrane thickness. The more the membrane thickness is, the less it would warp initially with any residual stress in the metal layer.

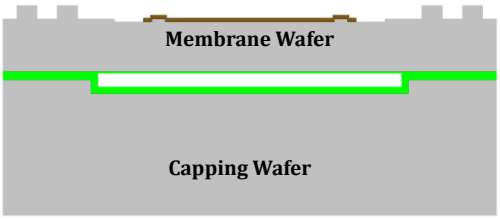


Fig 6.15: The sixth main step in the fabrication of the SOI wafer. The metal layer is deposited on the membrane layer where the metal connector of the switch is to be present. In addition, metal can be deposited in areas where the moving electrode is to be

The thickness of the Ge layer deposited for the sake of performing the eventual Al-Ge eutectic bonding between the SOI and circuit wafers would need to be ~ 0.3-0.5µm [94].

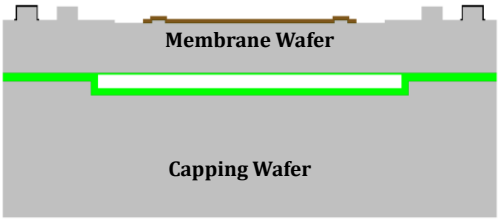


Fig 6.16: The seventh main step in the fabrication of the SOI wafer. Ge is deposited, and the Ge ring is patterned where the eutectic bonding is to take place. The same procedure is done for the areas where the suspension beams are to be anchored

Finally, the last step in the fabrication of the SOI wafer is to define the suspended regions, which is performed by the dry silicon etching of the membrane layer as well as the thin backside silicon dioxide layer resulting from the SOI bonding process. Fig 6.17 illustrates that step.

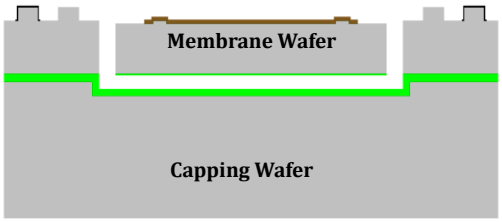


Fig 6.17: The eighth and last main step in the fabrication of the SOI wafer. A dry silicon etching step is required in order to define the suspended membrane and suspension beams on the SOI wafer prior to the bonding of SOI and circuit wafers

A summary of the material properties and thicknesses of different layers assumed for the first generation of the fabricated designs is provided in Table 6.1. Some values are based on fabrication restrictions whereas the majority of the numbers stem from preliminary analysis in conjunction with the electromagnetic and electromechanical simulation results.

Table 6.1: Summary of the material properties and thicknesses of the main layers for the first generation of fabrication

Wafer	Layer	Material	Thickness (μm)	Property
Circuit	Circuit Substrate	Si	725	Resistivity ~ 40Ω.m
	Thermal Oxide	SiO_2	2.2	Permittivity ~ 4.0
	Metal 1	AlCu	1.0	Conductivity ~ 2.7E7S/m
	Insulating Oxide	SiO_2	0.5	Permittivity ~ 5.0
	Metal 2	AlCu	1.0	Conductivity ~ 2.7E7S/m
	Contact Metal	Ru	0.15	Conductivity ~ 1.0E5S/m
SOI (Capping + Membrane)	Capping Substrate Cavity / Trench	Si	725 -50	Resistivity ~ 0.1Ω.m
	Thermal Oxide	SiO_2	1.0	Permittivity ~ 4.0
	Membrane Substrate Bump Dimple	Si Si Si	30 2.15 0.25	Resistivity ~ 40Ω.m
	Metal 3	TiN + Au	1.0	Conductivity ~ 3.0E7S/m
	Eutectic Bonding	Ge	0.4	Resistivity ~ 0.5Ω.m

In the next section, the major considerations for the RF as well as electromechanical switch design are discussed prior to the discussion of the different switch designs developed and being fabricated as part of the first generation of devices.

6.3 Switch Design

By looking at the end result in Fig 6.3 of the proposed microfabrication process with WLP, some of the main guidelines and considerations for the RF as well as the electromechanical designs of the MEMS switch can be immediately deduced, which is the focus of this section. The different analyses performed in view of such design guidelines led to the selection of some of the thicknesses and / or physical properties in Table 6.1, primarily for the selection of the resistivity values of the silicon layers and thicknesses of the silicon dioxide layers.

6.3.1 Important Considerations for the RF Design

In terms of the RF design of the switch, the most critical consideration is the inevitable crossing of the seal ring where an overlap between the first and second metals must exist due to that the second metal layer on the circuit wafer is required for the ring of Al-Ge eutectic bond. Fig 6.18 displays a typical overlap of a coplanar waveguide (CPW) line with the sealing ring. It is worth noting that due to the absence of TSV in the first generation of the packaged switch presented in this chapter, CPW implementation of the RF circuits is the most suitable option.

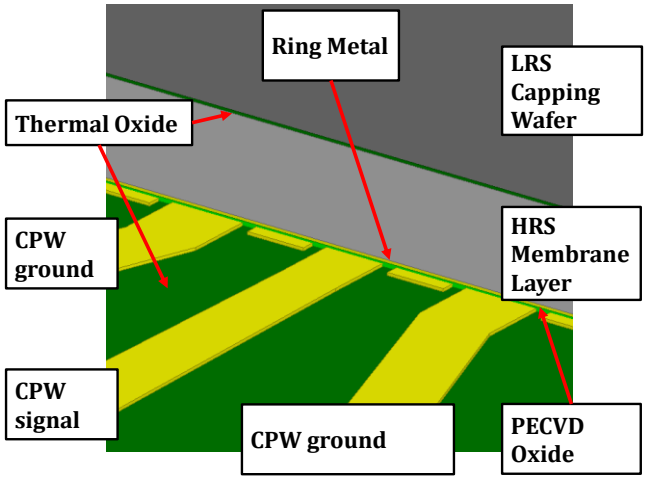


Fig 6.18: A 3D close-up on a typical overlap between the first and second metals on the circuit wafer for the sake of crossing the seal ring. The floating patches of the first metal layer are required for better CMP and bonding yields

In Fig 6.18, the floating patches on the first metal layer are required for the sake of improving the yield of the CMP process, and, accordingly, the yield of the eutectic bonding step. Such presence of a floating metal layer in the gap of the CPW line should be considered carefully in the RF design in terms of tuning the

characteristic impedance of the line including the crossing at the input port as well as at the output port. In addition, depending on the number of ports involved in the packaged RF MEMS switch, there can be different parasitic inductance values between the signal lines of the ports depending on the length of the second metal layer between two ports. Also, the matching and isolation at the ports would depend strongly on the perimeter of the ring, i.e. the size of the package. Fig 6.19 illustrates that issue assuming a CPW-based RF MEMS switch design.

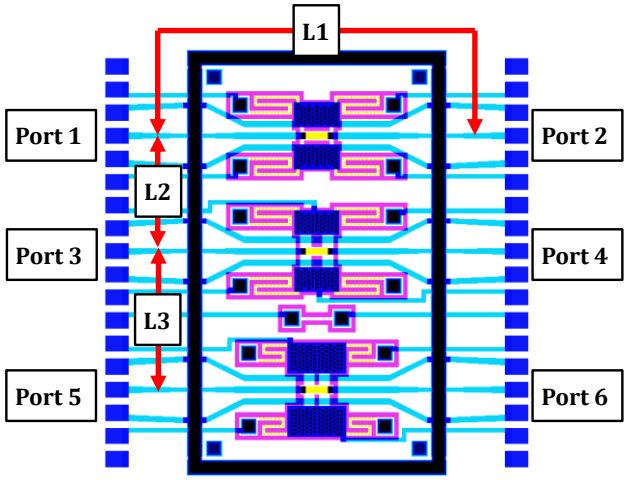


Fig 6.19: An illustration of the design-dependent parasitic inductance between the different RF ports at the crossing of the seal ring. Each value of inductance depends mainly on the length of the ring metal between the corresponding ports. The picture is from an exact layout of three SPST switches with some layers hidden for simplicity

The different signal lines and corresponding CPW ground planes would each have a minimum capacitance of ~ 0.1-0.2pF to the metal layer of the ring. That is caused by the minimum feature sizes allowed by the layout design rules imposed by the microfabrication procedure and materials selection as well as the dimensions imposed by the RF design itself, e.g. overall insertion loss, etc. As a result, the distributed capacitor along the seal ring along with the varying lengths of the ring metal between them would make the RF design further difficult and more dependent of the package size and number of ports involved.

Therefore, an efficient and simple solution to such a challenge lies in the RF grounding of the seal ring metal. For a given limitation on the minimum width of the ring metal, the appropriate feature sizes for the first metal and the minimum thickness of the dielectric layer between the two metal layers, the RF design of each port would be independent of the size of the package as well as the number of other ports crossing the same seal ring.

Moreover, Fig 6.20 demonstrates another approach to the RF design of the circuit inside the package where the membrane layer on top of the transmission lines as well as the silicon capping wafer is etched. Using the numbers in Table 6.1, this forms an air gap of ~ 80μm on top of the transmission lines, which would not be significantly different from having a transmission line outside the package (i.e. with the circuit wafer underneath and air on top). Such decrease in the relative permittivity on top of the transmission line helps reduce the gap between the CPW signal line and its ground planes for the same line impedance, which in turn helps shrink the size of the circuits. Furthermore, the RF design would depend mainly on the selection of the materials stack in the circuit, and, accordingly, would be greatly independent of the selection of the resistivity values for the membrane and capping wafers.

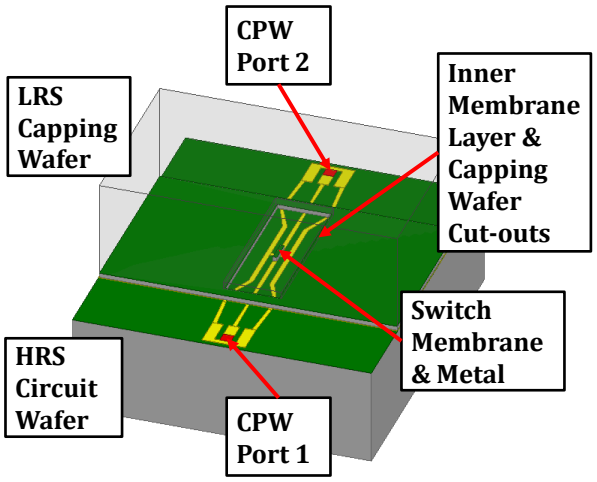


Fig 6.20: A 3D illustration of the additional etching of the membrane layer and cavity wafer on top of the transmission lines, which would help shrink the size of the circuit inside the sealed volume

In order to improve the overall insertion loss of the switch, another useful RF design approach for the proposed fabrication process would be to use thicker metal layer for the transmission lines, switched lines and tapering inside / outside the package, which can be done easily by connecting the first and second metal layers wherever possible using the via opening (see Fig 6.7). Finally, the RF design guidelines addressed in this section are employed in the design of the different switches presented in section 6.4.

6.3.2 Important Considerations for the Electromechanical Design

In view of the proposed process, the previous section addressed the major challenges to the RF design of the switch especially in terms of the design of transmission lines and seal ring crossover. For a complete RF MEMS switch design, those challenges should be coupled with the electromechanical challenges. In

order to understand more the tradeoffs of the electromechanical design, consider first the general model of the mechanical switch in Fig 6.21.

The model presented in this section can be used for the electromechanical design of a two-contact or multi-contact MEMS switch as well as electromechanical test structures of the contact resistance that forms upon the physical contact – assuming proper contact pressure – between the contact materials to be used, where the contact force can be well-estimated based on the lumped electromechanical model included in conjunction with finite element method (FEM) analysis as needed. The main assumptions of the modeling are: (1) The plate is rigid and moves parallel to the substrate surface which includes the fixed electrode and the two ports to be connected upon actuation, i.e. the switch is of the normally-open (NO) type; (2) The overall mechanical stiffness that is tethering the movable electrode or plate to the substrate is linear, i.e. independent of the actuation distance or force.

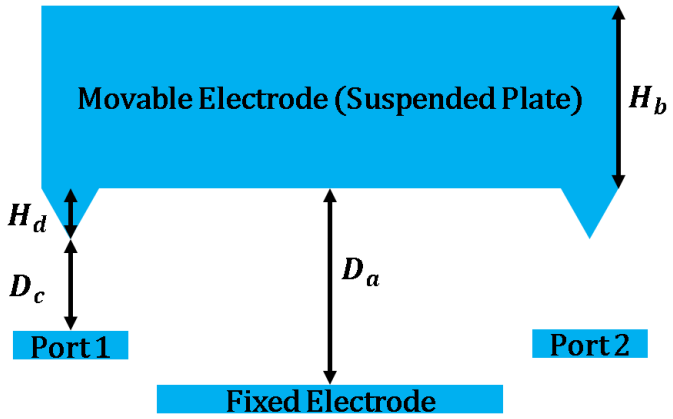


Fig 6.21: Generic model of the electrostatic actuator where the actuation (or fixed) electrode does not have to be in the same level as the ports to be switched on the substrate surface

In Fig 6.21, H_d is the height of the contact dimple, D_c is the contact gap, D_a is the electrostatic actuation gap, and H_b is the membrane thickness (that is the thickness of the plate and suspension beams based on the proposed process for the first generation of fabrication), which will be used later in this section in the calculation of the dimensions of the micro-beams depending on the level of the mechanical restoring force by design.

The maximum total mechanical restoring force F_r – assuming pull-in without collapsing – takes place in the contact state (or down-state). In such a state, the deflection of the plate is also at maximum, and it is equal to the contact gap D_c. The ratio of the restoring force to the deflection is simply the equivalent total stiffness K_p of the tethering beams that suspend the plate as demonstrated in Eq. 6.1.

$$\boldsymbol{F_r = K_p D_c} \qquad \text{Eq. 6.1}$$

Since the contact is to be made through electrostatic actuation with high enough contact force, it is required to operate the actuator beyond the pull-in range where the electrostatic actuation force would always be larger than the restoring mechanical force. That necessitates the inequality in Eq. 6.2 between the contact gap and the actuation gap. It is worth noting here that this is only valid in the ideal case, where the overall mechanical stiffness is linear according to the second main assumption of the lumped model.

$$\boldsymbol{D_c \geq \frac{1}{3} D_a} \qquad \text{Eq. 6.2}$$

As a result, the restoring mechanical force can be easily related to the pull-in voltage V_{PI} and the actuation area A as provided in Eq. 6.3 that gives the well-known relation between the pull-in actuation voltage, the overall mechanical stiffness holding the movable electrode, and the area of the capacitance between the two electrodes. Eq. 6.4 and Eq. 6.5 demonstrate how to connect the mechanical restoring force to such actuator parameters.

$$\boldsymbol{V_{PI} = \sqrt{\frac{8K_p D_a^3}{27\varepsilon_0 A}}} \qquad \text{Eq. 6.3}$$

$$\boldsymbol{K_P = \frac{F_r}{D_c} = \frac{27\varepsilon_0 A V_{PI}^2}{8D_a^3}} \qquad \text{Eq. 6.4}$$

$$\boldsymbol{F_r = \frac{27\varepsilon_0 A V_{PI}^2}{8D_a^3} D_c = \frac{27\varepsilon_0 A V_{PI}^2}{8D_a^2} \frac{D_c}{D_a}} \qquad \text{Eq. 6.5}$$

For the sake of simplicity and easiness of parametric study in conjunction with the generalization of the model, the ratio of the contact gap to the actuation gap will be referred to as γ, which is given in Eq. 6.6 and will be used later in this section for the different characteristic actuator plots.

$$\boldsymbol{\gamma = \frac{D_c}{D_a}} \qquad \text{Eq. 6.6}$$

Eq. 6.5 can be further simplified if the term for the minimum electrostatic actuation force at the pull-in voltage, which is the up-state actuation force F_{up} is included. This force is shown in Eq. 6.7, and the simplified equation for the maximum restoring force is then in Eq. 6.8.

$$\boldsymbol{F_{up} = \frac{1}{2}\frac{\varepsilon_0 A V_{PI}^2}{D_a^2}} \qquad \text{Eq. 6.7}$$

$$\boldsymbol{F_r = \frac{27}{4}\gamma F_{up}} \qquad \text{Eq. 6.8}$$

In the contact state, which is within the pull-in region, it is certain that the actuation force F_a necessarily exceeds the mechanical restoring force F_r. The difference between the two forces contributes towards the contact force F_c. This is given in Eq. 6.9, which can be reformulated as in Eq. 6.10, where the ratio of the contact force to the mechanical restoring force will be referred to as R_F as in Eq. 6.11.

$$\boldsymbol{F_a = F_r + F_c} \qquad \text{Eq. 6.9}$$

$$\boldsymbol{\frac{F_c}{F_r} = \frac{F_a}{F_r} - 1} \qquad \text{Eq. 6.10}$$

$$\boldsymbol{R_F = \frac{F_c}{F_r} = \frac{F_a}{F_r} - 1} \qquad \text{Eq. 6.11}$$

The actuation force in the state of contact and at the pull-in voltage F_a can be written as given in Eq. 6.12 in terms of the actuator parameters.

$$\boldsymbol{F_a = \frac{1}{2}\frac{\varepsilon_0 A V_{PI}^2}{(D_a - D_c)^2} = F_{up}\frac{1}{\left(1-\frac{D_c}{D_a}\right)^2} = F_{up}\frac{1}{(1-\gamma)^2}} \qquad \text{Eq. 6.12}$$

The ratio of electrostatic actuation forces R_{AF} is given in Eq. 6.13.

$$\boldsymbol{R_{AF} = \frac{F_a}{F_{up}} = \frac{1}{(1-\gamma)^2}} \qquad \text{Eq. 6.13}$$

It should be noted that F_a is the down-state actuation force, and the ratio of this down-state force to the up-state force F_{up} can be plotted versus the contact gap to the actuation gap ratio γ as shown in Fig 6.22.

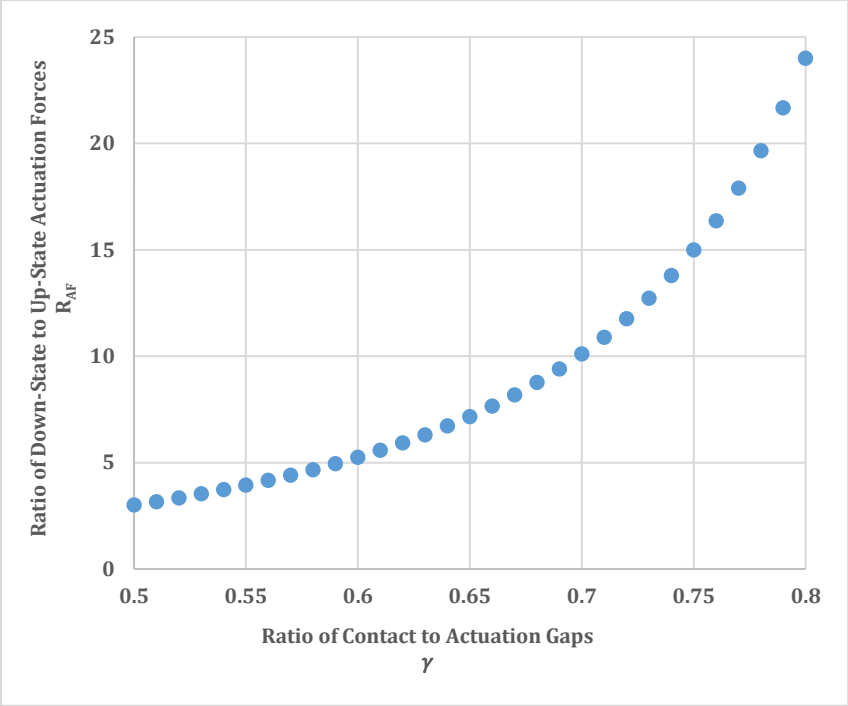


Fig 6.22: The down-state to up-state actuation forces ratio R_{AF} versus the contact to actuation gaps ratio γ

By combining Eq. 6.8 and Eq. 6.13, the force ratio R_F can be found as in Eq. 6.14.

$$\boldsymbol{R_F = \frac{4}{27}\frac{1}{\gamma(1-\gamma)^2} - 1 = \frac{4}{27}\frac{R_{AF}}{\gamma} - 1} \qquad \text{Eq. 6.14}$$

Eq. 6.14 can be plotted as shown in Fig 6.23 where the dependence of the force ratio on the out-of-plane electrostatic parameters (i.e. the gaps) can be understood easily.

So far, it is clear that studying the ratio of forces can be performed independent of the different absolute values of the contact or release forces. Such values can be designed based on the selection of the contact materials to be used (e.g. Au-Ru, Au-Ni, Au-Ti, etc.) [2, 4, 97]. The force ratio can be set based on the processing parameters (i.e. patterning of Si membrane for a Si-core MEMS switch or Au membrane for the sake of the high-power operation of the MEMS switch).

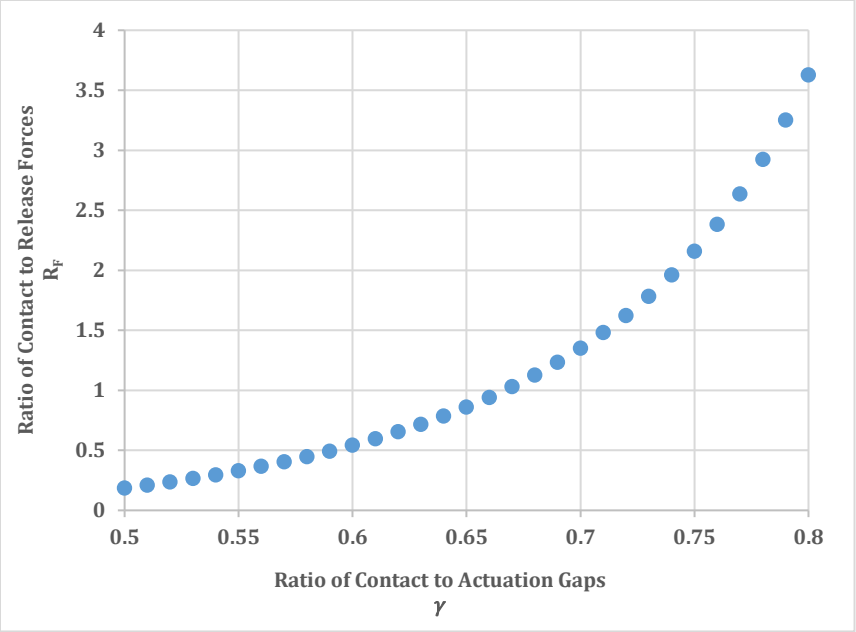


Fig 6.23: The total contact to release forces ratio R_F versus the contact to actuation gaps ratio γ

Referring to Table 6.1, the contact gap D_c is selected to be ~ 0.75µm whereas the actuation gap D_a is ~ 1µm and is equal to the sum of the contact gap and dimple height H_d that is 0.25µm. In view of such values and based on the analysis presented in this section, the value of γ is ~ 0.75. As a result, a value of 2.16 approximately for the contact to release forces ratio R_F can be obtained, which is appropriate for Au-Ru contacts. Also, the ratio of the down-state to the up-state electrostatic forces R_{AF} is around 16.

Depending on the switch design to be adopted, the number of contacts / dimples N_d may vary (including dummy dimples for the actuator short circuit protection – due to the lack of dielectric), which would then change the share of each dimple from the overall contact force F_c. Eq. 6.15 gives the contact force per dimple F_{cd} for a given number of dimples.

$$\boldsymbol{F_{cd} = \frac{F_c}{N_d}} \qquad \text{Eq. 6.15}$$

At this stage, identifying the exact values of contact and release forces as well as the targeted pull-in voltage allows to determine the rest of design parameters of the electrostatic actuator. Fig 6.24 and Fig 6.25 display the relation between the side lengths L_p of a square plate versus the pull-in voltage of the actuator.

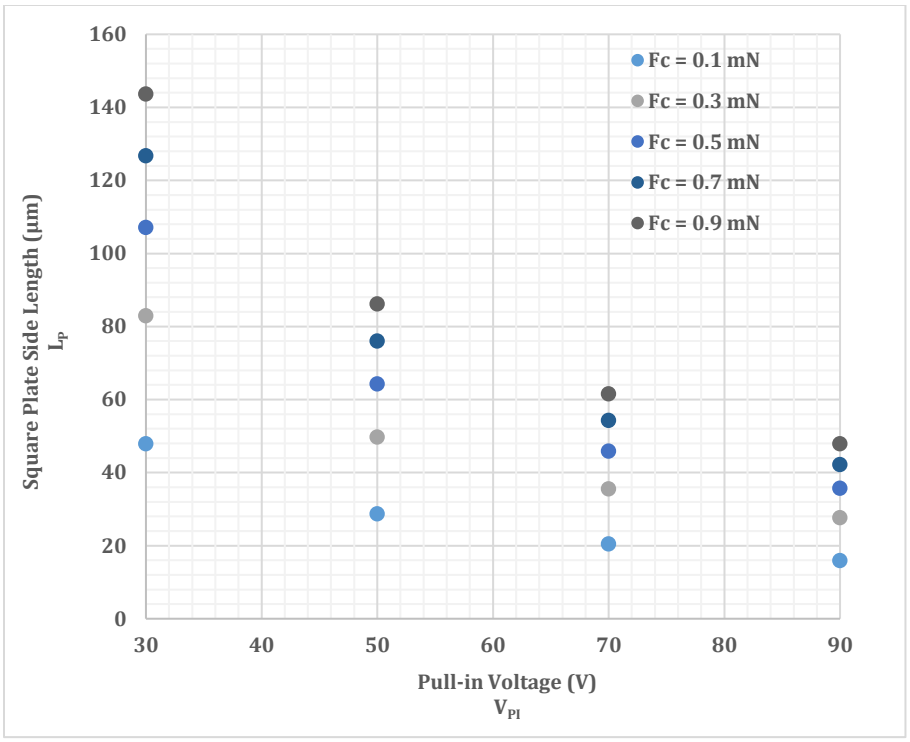


Fig 6.24: Square plate side lengths L_P (in µm) versus the pull-in voltage V_{PI} for various low contact forces F_c

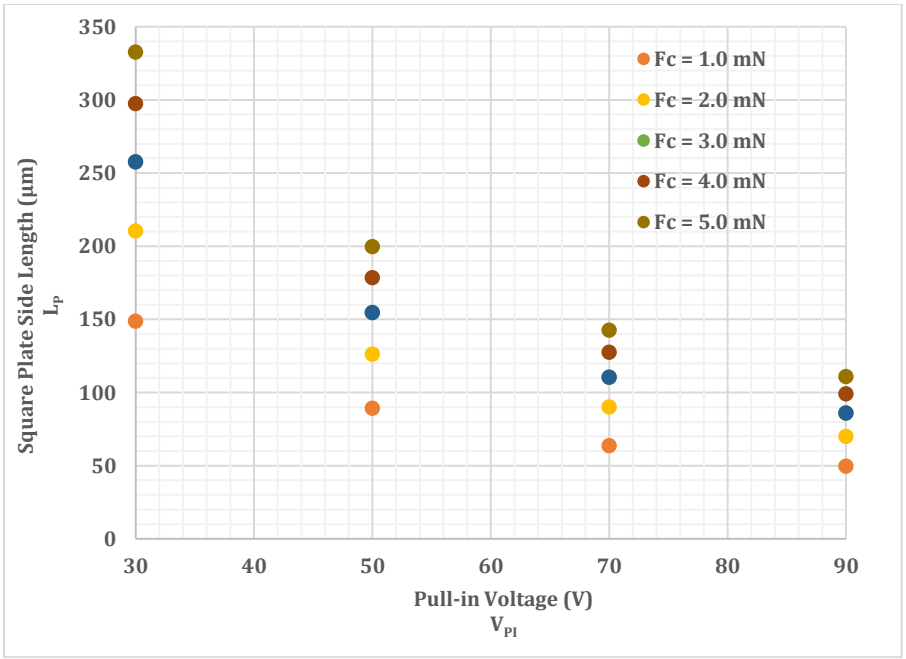


Fig 6.25: Square plate side lengths L_P (in µm) versus the pull-in voltage V_{PI} for various high contact forces F_c

Up to this stage, the release forces are also known, and their values can be easily related to the overall mechanical stiffness as in Eq. 6.16 where K_b is the individual beam stiffness and N_b is the number of identical beams tethering the plate.

$$\boldsymbol{K_p = \frac{F_r}{D_c} = N_b K_b} \qquad \text{Eq. 6.16}$$

Conventionally, N_b is selected as 4 towards reliable clamped-clamped devices exhibiting two-fold symmetry. Since the plate is to move parallel to the substrate, the beams should be arranged accordingly. Also, such movement necessitates a guided-end mechanical boundary condition for all the beams. This leads to the individual beam stiffness K_b provided in Eq. 6.17, where the Young modulus of the beam material is Y_b, the beam width is W_b, and the beam length is L_b. H_b, as mentioned previously, is the thickness of the suspension beam, assumed to be equal to the plate thickness for simplicity.

$$\boldsymbol{K_b = Y_b W_b \left(\frac{H_b}{L_b}\right)^3} \qquad \text{Eq. 6.17}$$

Eq. 6.16 can be re-written as in Eq. 6.18.

$$\boldsymbol{K_p = \frac{F_r}{D_c} = \frac{F_c}{R_F D_c} = 4 Y_b W_b \left(\frac{H_b}{L_b}\right)^3} \qquad \text{Eq. 6.18}$$

Identifying the beam material and thickness H_b, depending primarily on the reliability and reproducibility of a given microfabrication process, allows to plot the beam length L_b versus beam width W_b for different values of contact forces F_c. Other types of plots are also possible.

Assuming four tethering beams for a Si-core MEMS switch with 30μm thick membrane and 170GPa Young's modulus, Fig 6.26 displays the different values of the beam length L_b versus the beam width W_b for different values of low contact or release forces. Fig 6.27 gives more values for beam design parameters if the contact or release forces are significantly higher. It is clear that the operation under higher forcing can help shrink the size of the actuator, and, accordingly, the entire MEMS switch.

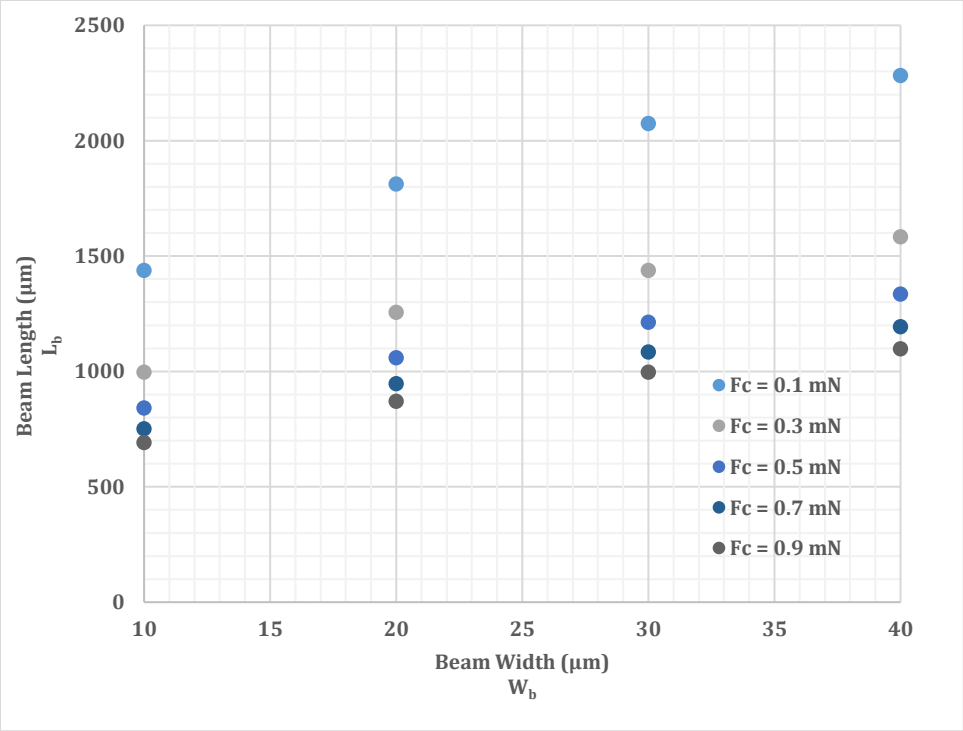


Fig 6.26: Beam length L_b (in µm) versus beam width W_b (in µm) for various low contact forces F_c

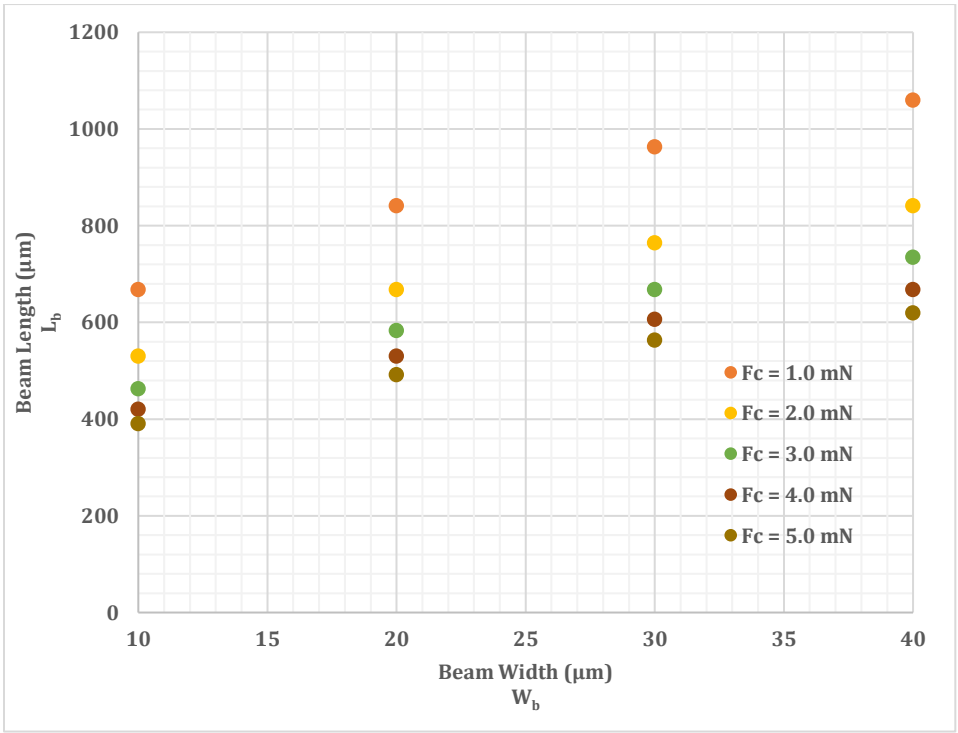


Fig 6.27: Beam length L_b (in µm) versus beam width W_b (in µm) for various high contact forces F_c

The simple approach introduced in this section towards the electromechanical design reveals the following important design considerations and tools:

(1) There can be a direct relation in the form of a ratio between the total contact force at the pull-in voltage and the total release force in the contact position. The ratio between the two total forces can be set actually by the ratio of the contact gap to the actuation gap, provided that the difference between the two gaps is the dimple height.

(2) The value of the pull-in voltage cannot be dealt with as a measure of the forcing level. It is clear that at the same pull-in voltage, the total forces can be increased by augmenting the actuated area. In addition, for a given actuator in contact position, the contact force can be increased as needed by increasing the actuation voltage beyond the value of the pull-in voltage. As a matter of fact, this helps a lot in changing the ratio between the total forces from an initially designed value. In other words, the actuator can assume a smaller ratio in order to reduce the pull-in voltage and/or actuator area, then the ratio can be increased in the contact position only where the restoring force is to be the same assuming no collapse of the actuator.

(3) In order to reduce the lengths of the suspension beams of a given actuator, more than one dimple per contact and/or dummy dimples (such as the actuator collapse protection dimples) can be used in high-force actuator design. In addition, the choice of the shape of the actuated plate can allow using 3 beams instead of the conventional 4 beams. For instance, a triangular, circular or hexagonal shape can be used in order to implement the 3-beam actuator. It is worth noting that using 2 suspension beams would not be generally reliable due to the associated torsional modes. In some special cases, however, it is still possible to rely on 2 suspension beams only, which would result in a significant reduction of the footprint of the actuator.

(4) After an electromechanical design is complete using the design sequence provided in this section, the pull-in voltage can still be made less by applying the electrostatic pressure to all the structure, i.e. the plate and its suspension beams, not only the plate. That is generally capable of reducing the pull-in voltage by about 10-15%, depending on the length to width ratio of the suspension beams, or reducing the actuated area and the overall footprint of the actuator while keeping the value of the pull-in voltage.

(5) In order to bias the actuator while decoupling the RF and low frequency circuits, there is no need to use a bias resistor as conventionally performed. That is due to the adoption of HRS for the membrane layer. However, relying solely on the resistance of the HRS layer would result in a resistance of several MΩ at least for the biasing resistor even for the shortest possible suspension beams (associated with high forcing actuator designs). Together with a pF range of the actuation capacitance, the RC time of the actuator would tend easily to be much longer than the mechanical switching time (< 50μsec), which is not desirable. That would as well oppose one of the major reasons for switching to Si-core topology that is increasing the switching speed such that the switching time can be further suppressed to few μsec if sub-μsec time is not attainable [90].

In order to solve that issue, the metal layer on the suspended membrane can be used as well on the suspension beams, thus applying a short circuit to most of the biasing resistance. The presence of significant residual stress in the metal layer can be more detrimental to the actuator design in this case, especially for a clamped-free architecture (i.e. cantilever) due to the initial warpage of the actuator. If the warpage is away from the circuit wafer, then the pull-in voltage would significantly increase. On the other hand, if the warpage is towards the circuit wafer, the isolation and RF performance would be reduced. In an extreme case of stress, the switch may be of the normally-closed (NC) type upon the assembly of the entire switch, which may still be another interesting switch design trick.

Finally, the next section provides more insights on some of the design degrees of freedom in addition to the main design and microfabrication constraints throughout the discussion of the analysis and simulation results for a group of the first generation switch designs.

6.4 First Generation of Si-Core RF MEMS Switches

In view of the main design guidelines and limitations highlighted in the previous section especially in terms of the MEMS design, it is clear that the RF switch dimensions would depend primarily on the dimensions of its electrostatic actuator, which in turn would depend on the forcing level and the architecture of the switch / actuator. In addition, since the proposed microfabrication process is to be eventually an industrial process for the sake of production, strict design rules and limited overall device areas are imposed. Therefore, being able to decide regarding the footprint of the actuator is crucial.

In order to have a closer look at the possible dimensions of the MEMS actuator in the switch, Table 6.2 and Table 6.3 provide values for the different footprints of the actuators for different pull-in voltages towards low and high forcing levels in contact position and at the corresponding pull-in voltages. In each table, a comparison of actuators with 2, 3 and 4 clamped-guided beams are provided. Also, the pull-in voltage values for the high forcing actuators are relatively higher in order to help with the compaction of the footprints of the actuator, and, accordingly, the RF switch especially for multi-port switching.

Table 6.2: Typical MEMS actuator footprints as function of the pull-in voltages and low forcing levels assuming 2, 3 and 4 clamped-guided beams as the suspensions of the actuator's plate and a beam width of 20μm

Pull-in Voltage V_{PI} (V)	Contact Force / Restoring Force F_c / F_r (mN)	4-Beam Actuator Footprint (mm^2)	3-Beam Actuator Footprint (mm^2)	2-Beam Actuator Footprint (mm^2)
20	0.2 / 0.09	0.125	0.089	0.056
	0.4 / 0.19	0.112	0.083	0.057
	0.6 / 0.28	0.111	0.085	0.063
	0.8 / 0.37	0.114	0.091	0.070
	1.0 / 0.46	0.119	0.097	0.078
30	0.2 / 0.09	0.120	0.083	0.050
	0.4 / 0.19	0.101	0.071	0.045
	0.6 / 0.28	0.094	0.068	0.045
	0.8 / 0.37	0.091	0.068	0.047
	1.0 / 0.46	0.090	0.069	0.050
40	0.2 / 0.09	0.118	0.081	0.048
	0.4 / 0.19	0.096	0.067	0.041
	0.6 / 0.28	0.088	0.062	0.039
	0.8 / 0.37	0.083	0.060	0.039
	1.0 / 0.46	0.080	0.059	0.040
50	0.2 / 0.09	0.117	0.080	0.047
	0.4 / 0.19	0.095	0.066	0.040
	0.6 / 0.28	0.085	0.059	0.037
	0.8 / 0.37	0.079	0.056	0.035
	1.0 / 0.46	0.076	0.054	0.035

Table 6.3: Typical MEMS actuator footprints as function of the pull-in voltages and low forcing levels assuming 2, 3 and 4 clamped-guided beams as the suspensions of the actuator's plate and a beam width of 20μm

Pull-in Voltage V_{PI} (V)	Contact Force / Restoring Force F_c / F_r (mN)	4-Beam Actuator Footprint (mm²)	3-Beam Actuator Footprint (mm²)	2-Beam Actuator Footprint (mm²)
40	2 / 0.9	0.079	0.062	0.047
	4 / 1.9	0.094	0.081	0.068
	6 / 2.8	0.114	0.103	0.092
	8 / 3.7	0.137	0.126	0.117
	10 / 4.6	0.160	0.150	0.141
60	2 / 0.9	0.065	0.048	0.033
	4 / 1.9	0.065	0.052	0.040
	6 / 2.8	0.071	0.060	0.049
	8 / 3.7	0.080	0.069	0.059
	10 / 4.6	0.089	0.079	0.070
80	2 / 0.9	0.060	0.043	0.028
	4 / 1.9	0.055	0.042	0.030
	6 / 2.8	0.056	0.045	0.034
	8 / 3.7	0.059	0.049	0.039
	10 / 4.6	0.064	0.054	0.045
100	2 / 0.9	0.058	0.041	0.025
	4 / 1.9	0.051	0.037	0.025
	6 / 2.8	0.049	0.038	0.027
	8 / 3.7	0.050	0.039	0.030
	10 / 4.6	0.052	0.042	0.033

Upon inspecting the numbers in both tables, it is clear that for the low forcing actuators (Table 6.2), the increase in the pull-in voltage does not help much with reducing the footprint of the actuator. In addition, it can be observed that reducing the number of suspension beams affect significantly more the footprint. This is due to that most of the area occupied by the actuator is for the suspension beams implementing the overall stiffness or restoring force. On the other hand, for high forcing actuators (Table 6.3), it can be observed that increasing the pull-in voltage leads to significant shrinking of the overall actuator area. This is the result of having most of the area occupied by the movable plate rather than the suspension beam.

Another interesting observation is the fact that depending on the forcing level and number of suspension beams holding the actuator plate, the minimum footprint is not necessarily attained using the plate area corresponding to the maximum pull-in voltage. This tends to be more pronounced for low forcing actuators,

for instance, in the 4-beam 20V and 3-beam 30V actuators. The same behavior can be noticed as well in all the high forcing actuators at 100V.

6.4.1 Clamped-Clamped SPST Switch Designs

In order to test the first generation of fabricated devices along with the proposed microfabrication and WLP process itself, several designs of Single-Pole Single-Throw (SPST) switch designs have been developed. First, it is worth noting that in-line switching (or cantilever-based switching, where the switched membrane is anchored to one of the two ports) would not be possible due to, mainly, the incorporation of HRS for the membrane material. That means that a minimum count of two dimples / contacts is required for the switch, and it should be taken into consideration for the design of the total contact and restoring force.

Second, since the transmission lines are CPW-based, there are two options for the switch architecture: (1) the switching can be made by switching the CPW signal lines only, as conventionally performed; (2) the switching can be realized by switching the CPW signal lines in conjunction with the switching of the ground planes, which necessarily means having 3 times the count of dimples needed if the line only is switched. Fig 6.28 displays the two cases, where the switching of the ground planes can help improve the isolation in the OFF state of the switch.

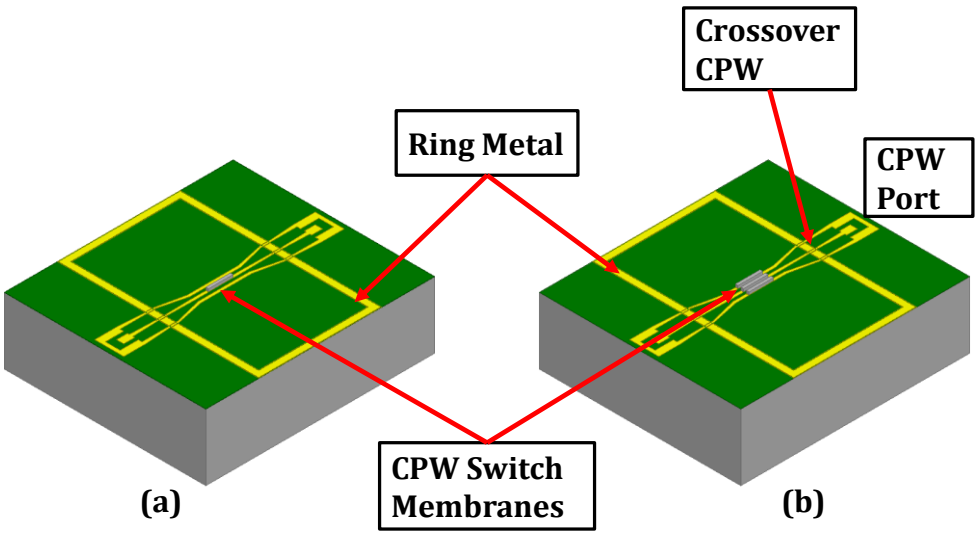


Fig 6.28: Two possible designs for the proposed CPW-based SPST switches: (a) switching of signal line only; (b) switching of the signal line and the ground planes all together. The pictures are from parameterized HFSS simulation files, and the SOI wafer is hidden

Third, as indicated previously, the crossover with the seal ring metal is one of the major RF design considerations. In order to tune the overall RF performance of the switch, some length parameters need to

be tuned efficiently, especially with the strict limitations on the area of the sealed region and the overall die footprint. Fig 6.29 shows such parameters on a 3D HFSS fully-parametrized structure where the tuning and optimization of the crossover was performed.

In the figure, the main tuning parameters are the first and second tapering distances, L1 and L2, respectively, in addition to the gap between the signal line and ground planes of the crossover transmission line, G1. Due to the fabrication constraints in terms of the dicing and tabbing margins from the probing pads, there is a relatively very narrow window for the tuning to the distance L1, and it is then fixed to be ~ 300µm. On the other hand, there is a significantly wider window for the tuning of L2 depending on the width of the sealed rectangular region, which is selected to be ~ 1mm x 2mm due to the limited reticle area of 10mm x 10mm for the projection lithography system to be employed in the different pattern definition steps.

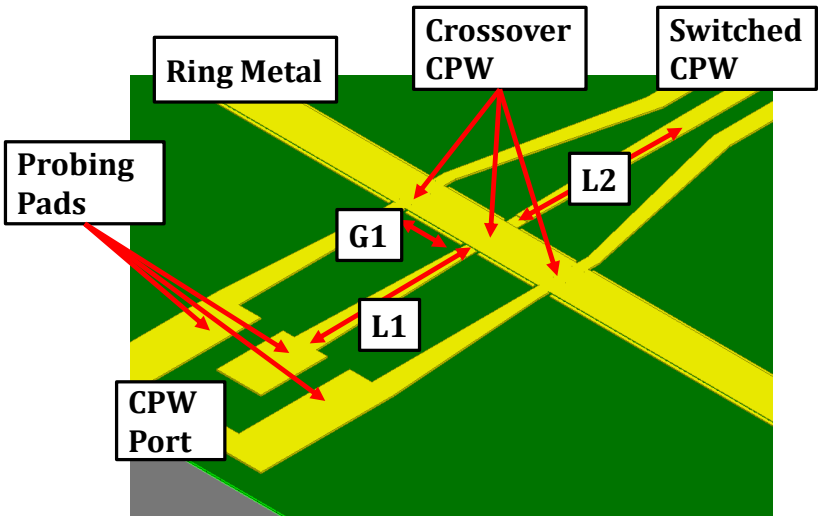


Fig 6.29: Main design parameters for the efficient tuning of the matching of the crossover of RF transmission line and the seal ring metal. The picture is from a parameterized HFSS simulation file, and the SOI wafer is hidden for the sake of clarity

Moreover, in order to have the maximum possible count of identical probing pads for every 2.5mm x 2.5mm die (which would help the most with implementing multi-port switching with the required DC pad(s) per switch / state) while being able to perform RF probing on the circuit wafer with enough matching, the width of the pad was selected to be 80µm whereas the gap between the pads was 40µm. For a conservative width of 20-30µm for the first metal features in the crossover CPW, the maximum gap distance G1 is accordingly 135-150µm. It is found that keeping G1 at the maximum value helps more with the overall matching and/or reducing the tapering length L2 inside the sealed region, which in turn offers more area for the actual circuit and actuators to be packaged.

Another important design approach for better crossover matching is to limit the width of the tapered CPW line and ground planes as show in the figure, especially for the first tapering outside the sealed region. Following the design guidelines discussed up to this stage, a HFSS 3D electromagnetic simulation of the switch can lead to the ON state return loss and insertion loss displayed in Fig 6.30 and Fig 6.31 with no major differences between the results for the aforementioned 2-contact and 6-contact designs.

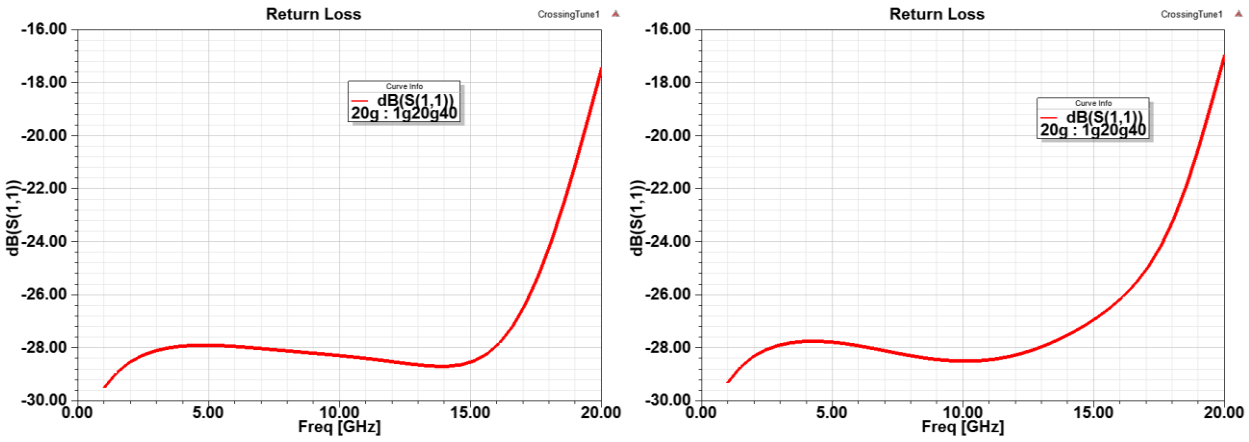


Fig 6.30: HFSS simulation of the return loss of the SPST switch in ON-state: (a) the 2-contact switch with signal line switching only; (b) the 6-contact switch design with signal line and ground plane switching

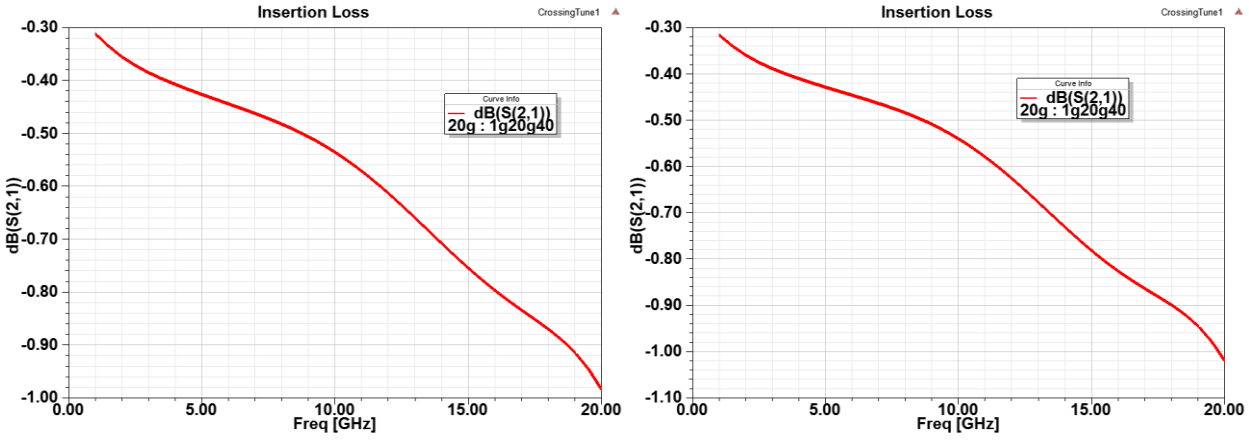


Fig 6.31: HFSS simulation of the insertion loss of the SPST switch in ON-state: (a) the 2-contact switch with signal line switching only; (b) the 6-contact switch design with signal line and ground plane switching

On the other hand, in the OFF state of the SPST switch, the HFSS electromagnetic simulation confirms higher isolation for the 6-contact switch where the ground planes are also switched. This is demonstrated in Fig 6.32 and Fig 6.33.

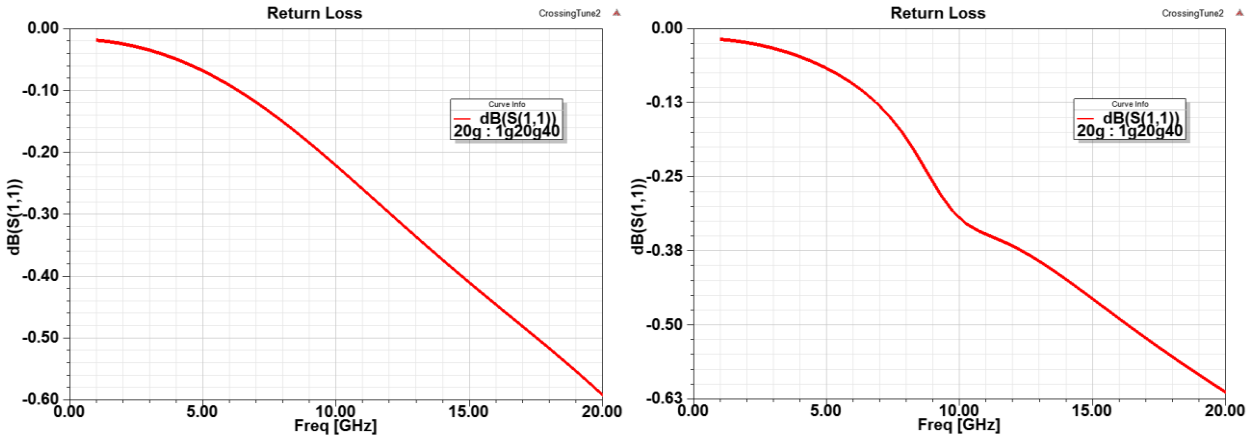


Fig 6.32: HFSS simulation of the return loss of the SPST switch in OFF-state: (a) the 2-contact switch with signal line switching only; (b) the 6-contact switch design with signal line and ground plane switching

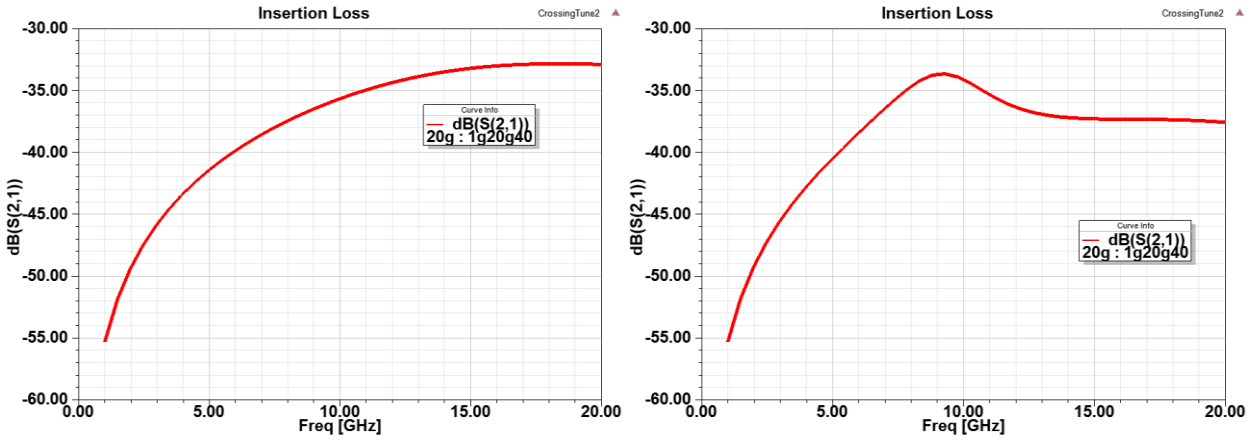


Fig 6.33: HFSS simulation of the isolation of the SPST switch in OFF-state: (a) the 2-contact switch with signal line switching only; (b) the 6-contact switch design with signal line and ground plane switching

Furthermore, since the pull-in voltage for some of the developed first generation of switches is required to be relatively low, e.g. 20-30V, the footprints for high forcing actuators tend to be relatively large and, accordingly, can be critical in the presence of significant residual stress in the suspended metal layer deposited by PVD. It is worth noting here that the final assembly of the SOI wafer and the circuit wafer should be performed at temperatures up to ~ 450ºC. The preliminary analysis and fabrication short loops suggest that a worst case average tensile stress of 400MPa can be present, which should be considered carefully for the design of the actuators. In fact, FEM simulations in COMSOL confirm that the initial warpage in the membrane due to such worst case residual stress can be up to 1-2µm, which is detrimental to the operation of the actuator.

It should be noted that the presence of the metal layer reduces the actuation gap to the designed value of 1µm as discussed previously, and the choice of the actuation gap should take into consideration the

thickness of that metal layer. Also, the presence of the metal layer serves to reduce much the RC time of the actuator. If the warpage is to be prevented, but not completely due to the inevitable presence of the metal strip for connecting the desired ports, the areas on the movable plate where the electrostatic pressure is to be applied can be suspended without the metal layer. However, this would be an expensive solution in terms of doubling the actuation gap and almost increasing the pull-in voltage by a factor of 3. Besides, the RC time of the actuator would be dramatically increased relative to the mechanical switching time.

There exists a better solution through which the majority of the worst case initial warpage is suppressed completely while the actuator exhibits a relatively low to moderate pull-in voltage. As a matter of fact, the metal layer can still be applied to the movable plate as well as the suspension beams in the form of metal patches instead of a continuous sheet of metal. That way, most of the resistance through the HRS layer would also be shorted by the metal layer towards a reasonable switching speed. Fig 6.34 demonstrates employing the metal patches in a typical SPST switch layout. Moreover, the initial warpage of the movable plate is plotted in Fig 6.35 versus the fill factor percentage of the metal layer on the membrane at the worst case residual stress of 400MPa and for different levels of forcing in the designed actuators.

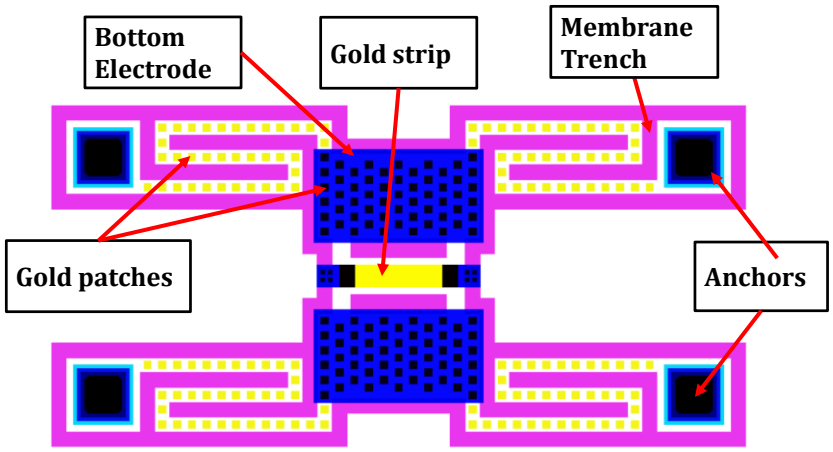


Fig 6.34: Illustration of employing metal patches on the actuator's membrane rather than a continuous metal layer. The picture is from an exact layout of high forcing SPST switch design that assumed a fill factor of ~ 25%

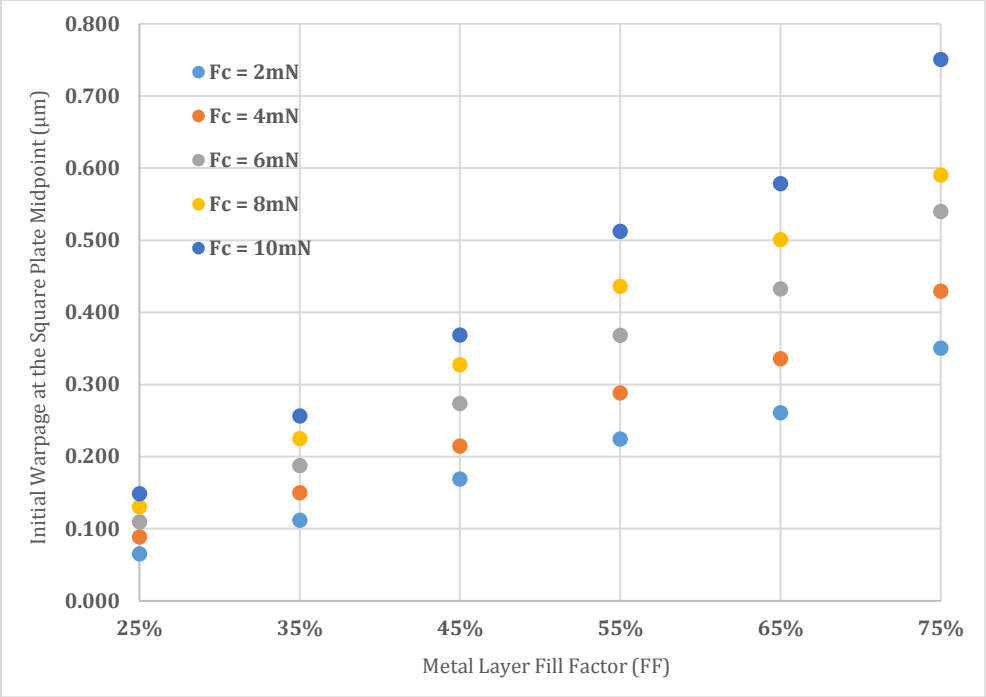


Fig 6.35: COMSOL simulation results of the worst case initial warpage at the midpoint of the square membrane versus the fill factor of the metal layer coating for different levels of forcing in the designed actuators

6.4.2 Seesaw Push-Pull SPST Switch Design

In addition to the conventional clamped-clamped and clamped-free switch architectures, it is possible to implement seesaw switches with push-pull actuation as illustrated in the COMSOL electromechanical simulation in Fig 6.36. In order to connect ports 1 and 2 demonstrated in the exact layout of Fig 6.37, the inner electrodes are used for the actuation. Aside from the mechanical restoring of the suspended membrane, the outer electrodes can be used for the restoring as well as increasing the isolation between the two ports by increasing the out-of-plane deflection of the gold switch beam (see Fig 6.38) away from the contact areas.

Fig 6.37 displays an exact layout of the switch relative to the size of the seal ring (~ 1mm x 2mm). The footprint of the switch is not large relatively. The actuation voltage is ~ 50V. If the actuation voltage and forcing levels are increased further, two identical switches can fit in the same sealed area. Torsional hinges only can be used for the clamped-clamped seesaw action; however, a dummy silicon bumper can be used as well in order to serve as the required pin-support. In this case, the torsional hinge would be designed to have the lowest possible stiffness. The two locations of the silicon bumpers are demonstrated in Fig 6.38.

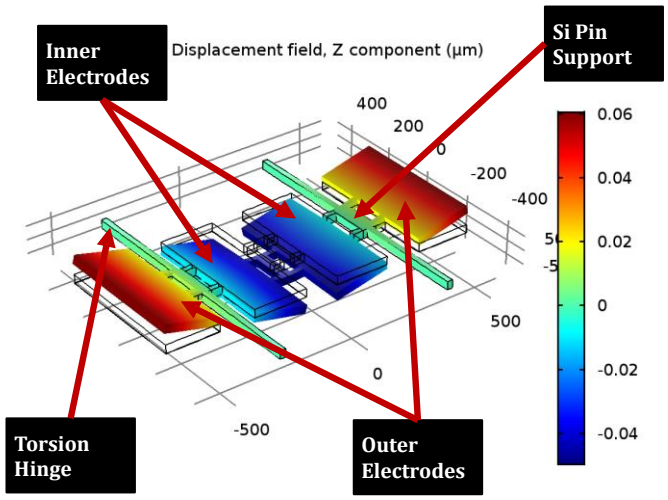


Fig 6.36: COMSOL simulation of the seesaw push-pull SPST switch showing the push-pull action

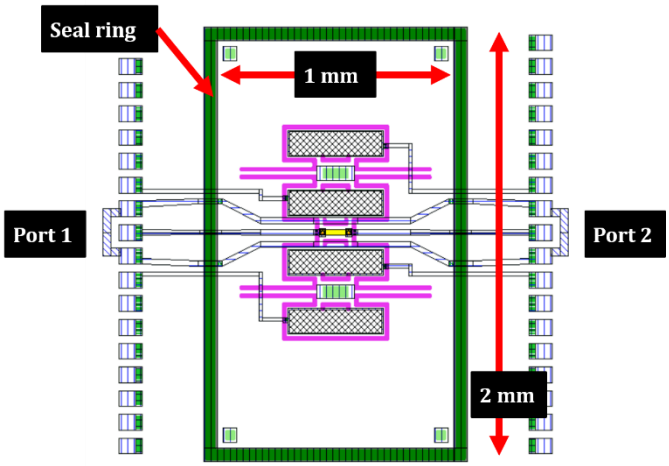


Fig 6.37: An exact layout of the seesaw push-pull SPST switch showing its actual size

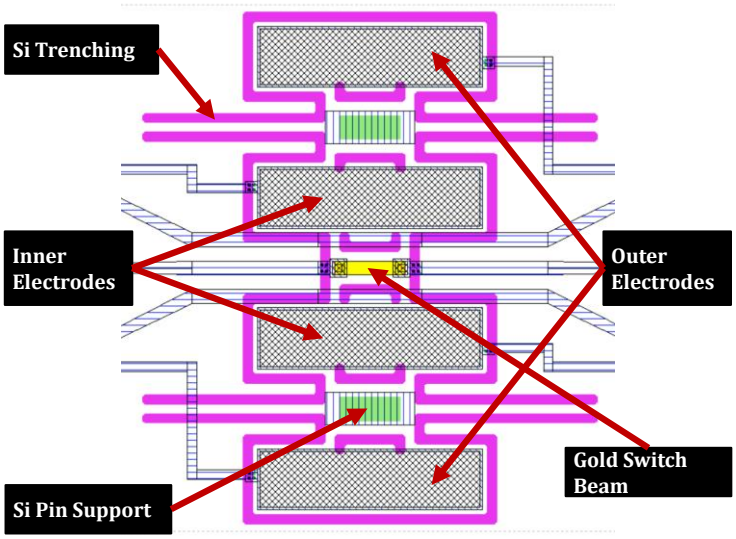


Fig 6.38: An exact layout of the seesaw push-pull SPST switch

6.4.3 Compact T-Switch Crossover Design

Fig 6.39 to Fig 6.42 demonstrate the design and operation of a compact cross-over state that is essential for the design and fabrication of a compact T-switch. Fig 6.39 reveals the actual size of the compact cross-over designed, which is ~ 0.5mm x 0.5mm. In order to improve the RF performance of the cross-over, the bridges for connecting each couple of ports (i.e. ports {1, 3} and ports {2, 4}) are designed as air bridges. This necessarily means that the gold layer on the MEMS wafer is used for the switching (see Fig 6.40). In view of that, the switched circuit on the device / circuit wafer should be designed as shown in Fig 6.41.

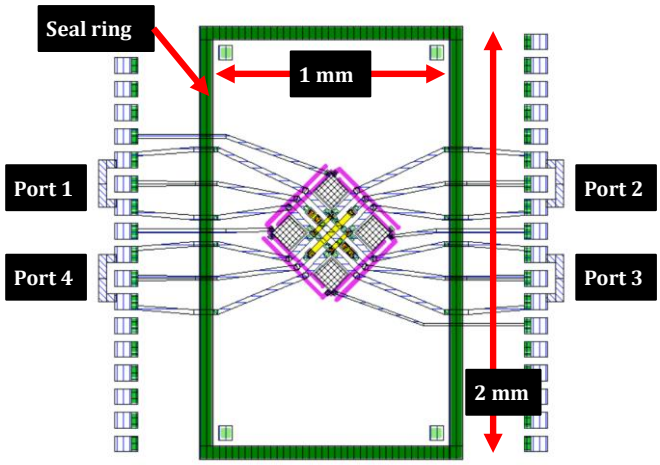


Fig 6.39: Exact layout of the proposed compact T-switch crossover design showing its actual size

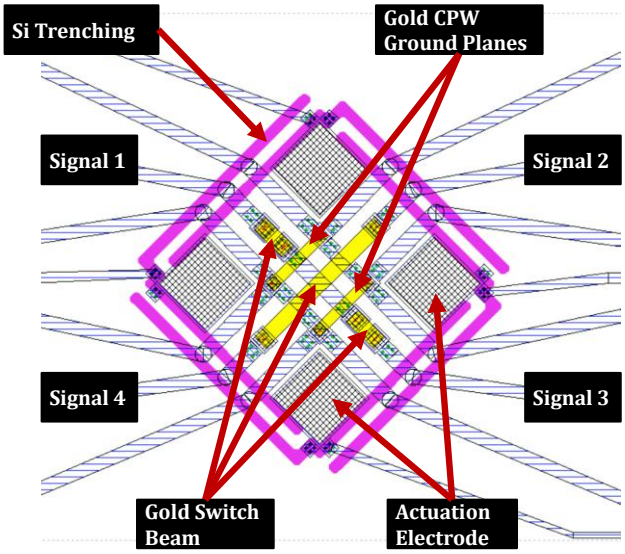


Fig 6.40: Exact layout of the compact T-switch air crossover switching cell

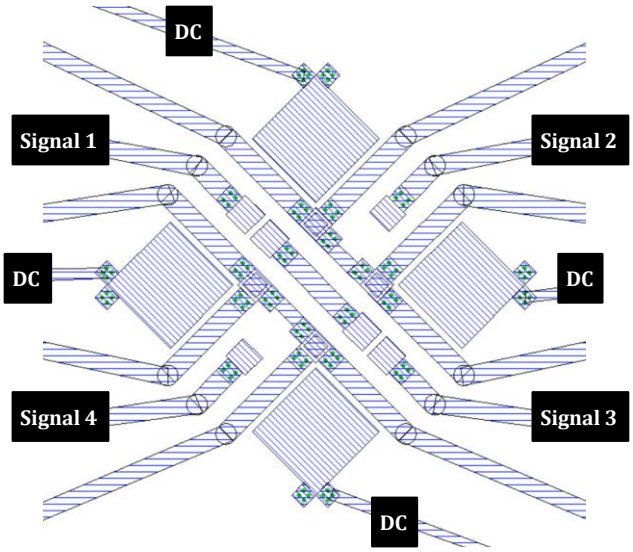


Fig 6.41: Exact layout of the CPW-based circuit in the T-switch crossover

Fig 6.42 illustrate the electromechanical operation of the actuator. Due to the relatively large number of dimples and forcing levels required, the design could be made that compact by means of ~ 90V actuation voltage.

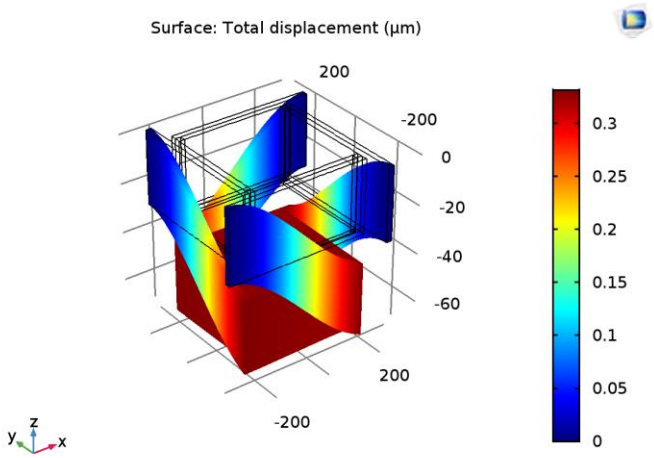


Fig 6.42: COMSOL electromechanical simulation of the T-switch crossover cell

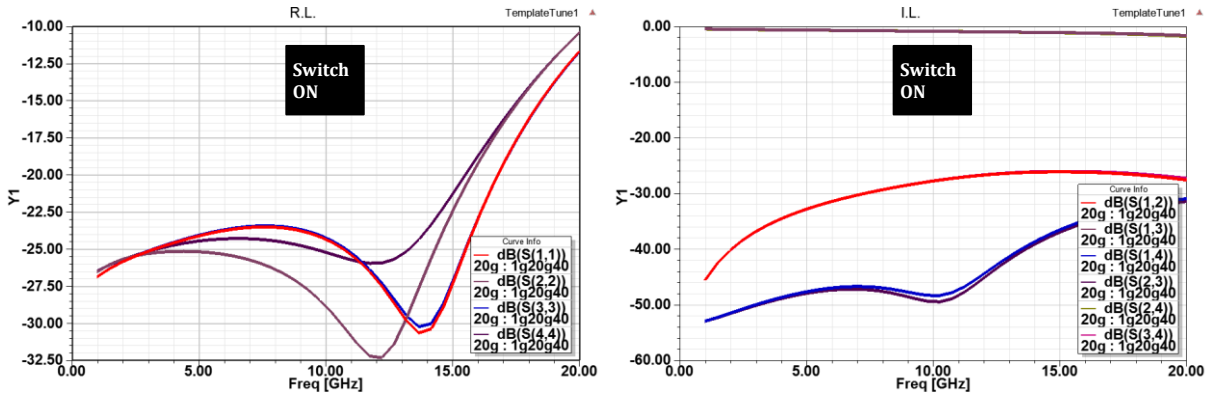


Fig 6.43: HFSS simulation of the return loss, insertion loss and isolation of the T-switch cross-over in ON-state

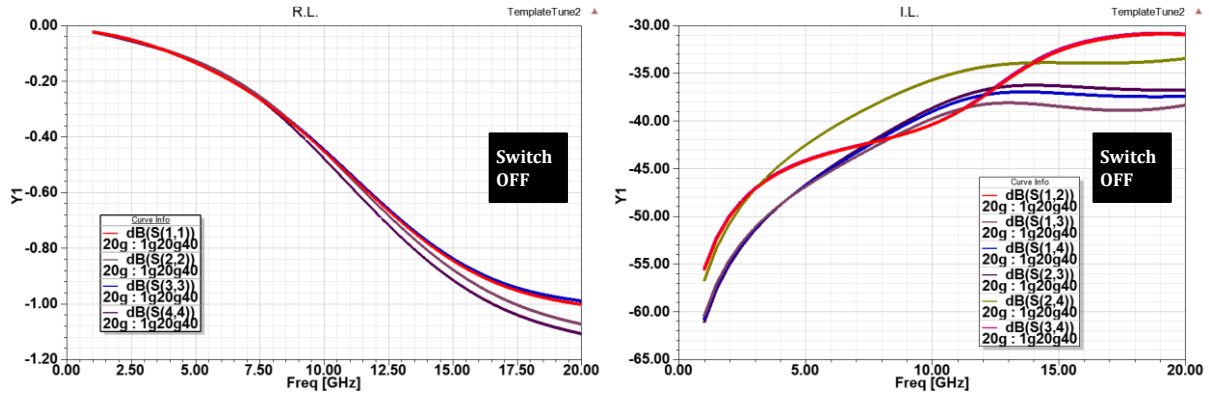


Fig 6.44: HFSS simulation of the return loss and isolation of the T-switch crossover in OFF-state

Fig 6.43 and Fig 6.44 show the simulated RF performance of the air cross-over in the ON and OFF states. In the ON state, the cross-over performance is reliable up to 15GHz at least, and the insertion loss at 15GHz is ~ -1.25dB. It can be seen as well that the isolation of the disconnected ports is better than 26dB. In addition, the isolation in the OFF state is better than 30dB up to 20GHz.

6.4.4 Compact C-Switch Design

Fig 6.45 to Fig 6.47 demonstrate the C-switch design that is close to that of the compact cross-over in terms of the footprint (see Fig 6.45) and the RF circuit tuning including the seal ring grounding. The actuation voltage is ~ 60V, and the RF simulation results in the ON and OFF states are comparable to those in Fig 6.43 and Fig 6.44. The actual size of the compact C-switch is shown in Fig 6.45 whereas the detailed design is provided in Fig 6.46.

In this design, a biasing resistor should be used in order to prevent the signal line loading by the DC biasing (Fig 6.46). The resistive layer can be incorporated in the presented microfabrication process before the deposition and patterning of the first metal layer. Simply, a metal layer can be used similar to the UWMEMS process presented in chapter 5. Cr, Ti, TiW, SiCr, NiCr, etc. can be employed, and the sheet resistance is typically ~ 50Ω/□.

Fig 6.47 demonstrates the design of the switched circuit in the compact C-switch cell where the circular CPW sections are tuned for the sake of controlling the overall RF matching in the ON state.

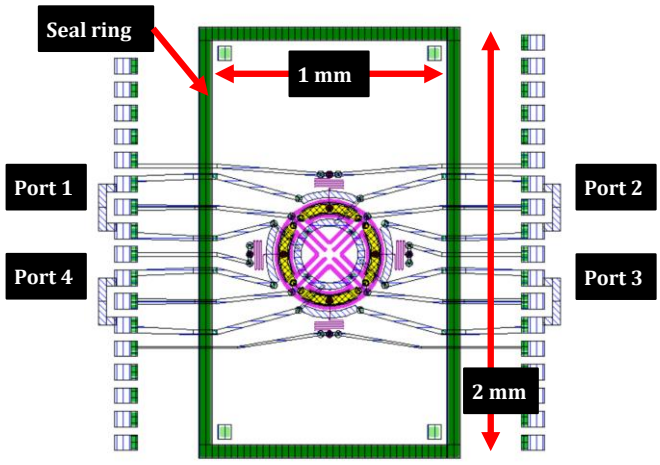


Fig 6.45: Exact layout of the compact C-switch showing its actual size

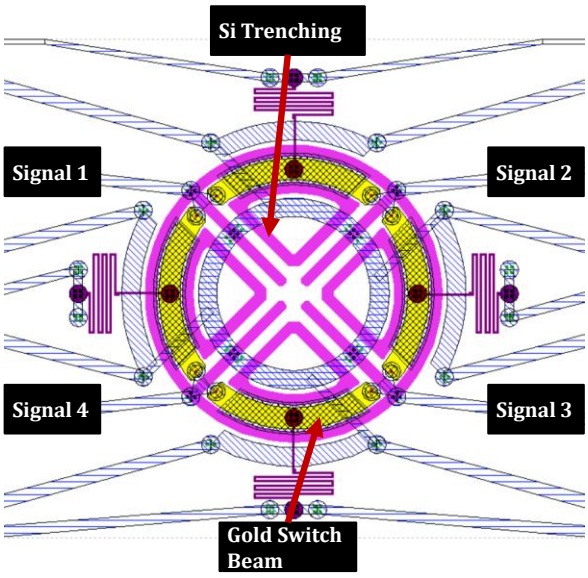


Fig 6.46: Exact layout of the compact C-switch actuator

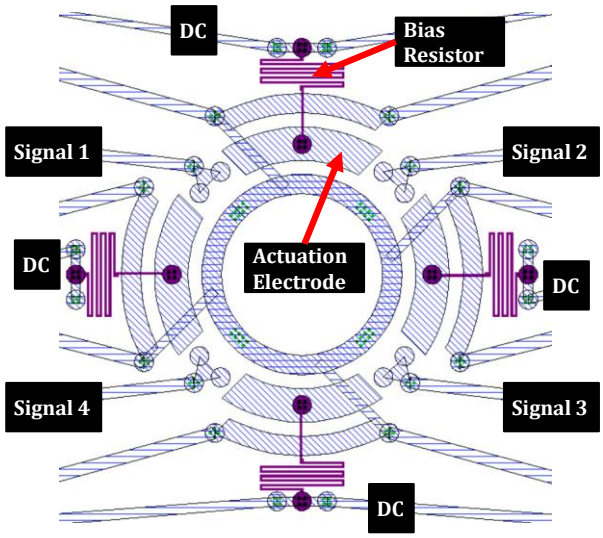


Fig 6.47: Exact layout of the CPW-based circuit in the compact C-switch

6.4.5 Gimbal-Switch Design (G-switch)

In addition to the variations of the SPST switches discussed so far as well as the compact T-switch cross-over and C-switch designs, a novel switch design introduced in this work is based on a gimbal architecture, which is used in a similar way to that of inertial sensors but for the sake of building a high forcing compact multi-port switch [98, 99]. As indicated previously, the compaction is critical in view of the strict limitations on the maximum area of the sealed region as indicated previously.

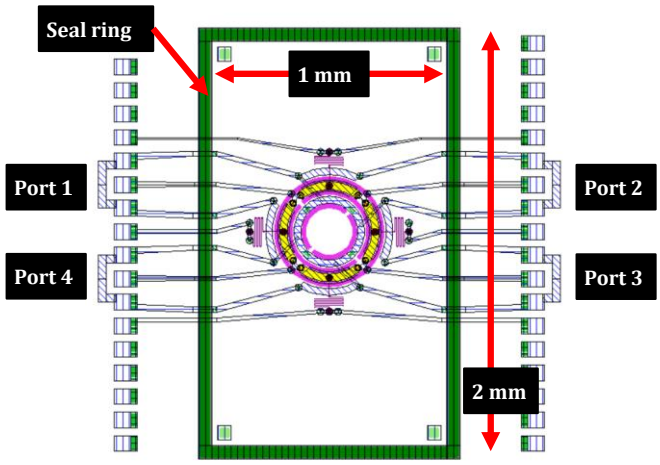


Fig 6.48: Exact layout of the gimbal-based switch showing its actual size

Fig 6.48 and Fig 6.49 show the exact layout of the gimbal-based switch design. It is clear that it is similar to a great extent to that of the compact C-switch design, which is true. Also, the switched circuit is identical to that of the C-switch displayed in Fig 6.47. However, the operation and design of the MEMS actuator is different. Fig 6.50 demonstrates the 3D architecture of the gimbal switch where the tilting of the suspended outer ring is allowed in two directions due to employing the inner and outer torsional hinges such that the tilting of the inner ring is only allowed in only one direction. The four movable actuation electrodes then can switch four connections depending on which fixed electrode is active.

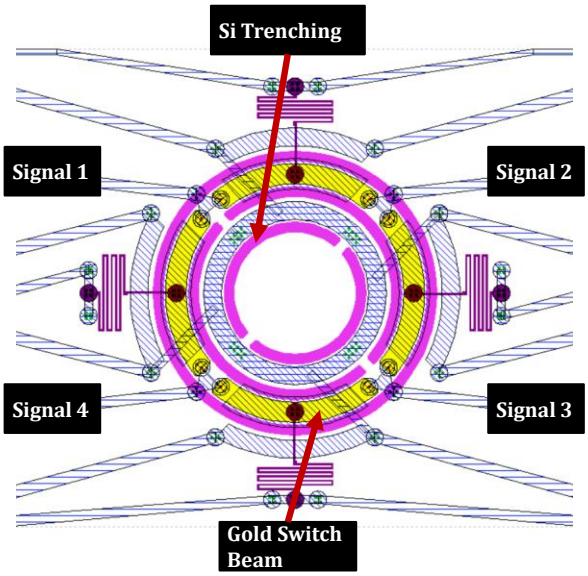


Fig 6.49: Exact layout of the gimbal switch actuator

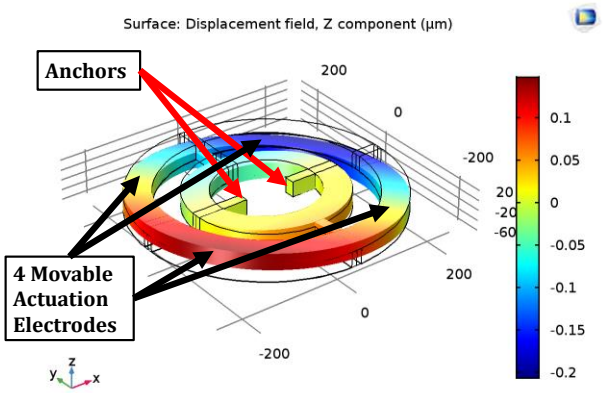


Fig 6.50: COMSOL simulation of the gimbal actuator

Chapter 7: Conclusions & Future Work

7.1 Conclusions

The thesis has presented the design, simulation and fabrication of several MEMS switches suitable for various RF applications including redundancy switch matrices for satellite communication systems, reconfigurable RF circuits and passives, and automated test equipment (ATE). The microfabrication of the switches is carried out in four fabrication technologies / approaches.

First, the MEMS switches are realized by post-processing the standard CMOS 0.35µm chips such that the structural layers of the electrostatic MEMS switches are implemented in the four metal and oxide insulating layers of the BEOL. An enhanced post-processing technique is developed and employed successfully. The technique is capable in fact of providing different warping profiles for the same device layout, which would make the isolation of a given switch, for instance, post-processing-dependent along with the pull-in voltage of the switch. The profile depends on the pulsed thermal treatment of the chip that takes place during the dry etching step of silicon dioxide in an advanced RIE system without cryogenic cooling. The switches presented include a compact 4-bit capacitor bank for 3-10GHz, a compact 4-bit phase shifter / delay line for a wider bandwidth, a W-band SPST series capacitive switch, SPST shunt capacitive switches with enhanced capacitance density by means of interleaving the via structures between the metal plates, and a compact T-switch for up to 20GHz applications.

Second, the standard MetalMUMPs process is used for realizing RF MEMS switches for high RF power applications. The electrothermal MEMS switches designed and fabricated include a 3-bit capacitor bank, a compact discrete capacitor based on the mechanical latching of a conventional comb-drive varactor, which can be configured for 2-bit / 3-bit operation depending on the stroke of the actuator, and a rotor-based electrostatic multi-port series switch for high RF power applications up to 6GHz.

Third, the UWMEMS process is adopted and further expanded. A new post-processing of the fabricated devices is introduced where the first metal layer can be released similar to the second metal layer that has been the only structural layer. Also, depending on the new post-processing sequencing of wet and dry etching steps, uncommon and novel architectures can be realized easily. This includes geometric confinement (GC) switches and structures with composite beams such as thermal bimorphs that are accordingly employed in thermally-restored switches (TRS) where the switch beam is electrostatically actuated with low voltage and thermally restored by a pulse, i.e. with low power consumption. The restoring pulse is the result of a current pulse in an electrothermally actuated bimorph underneath the suspended switch beam. The gold-based switches presented include compact T-switch, R-switch and C-switch designs,

GC SPST switch cells, a novel switch design referred to as Hybrid Self-Actuation Switch (HSAS) where the switch can be turned ON at certain level of input RF power which can be controlled, novel TRS designs. Finally, in the fourth method, packaged silicon-core switches are realized by means of a new wafer-level packaging microfabrication process. The silicon-core nature of the switches features attractive advantages as compared to the metal-based switches used in the three other approaches, especially in terms of mechanical reliability and speed. Since the switches are all hermetically sealed, it is possible to perform reliability testing on them efficiently and without the need for the emulation of a typical package environment. The designed switches to be fabricated as part of the first generation include simple SPST contact-type switches for the sake of RF and reliability testing as well as novel and compact designs of T-switch crossover, 4-port gimbal-switch (referred to as G-switch) and C-switch. In addition to that, a seesaw push-pull SPST switch design is included, which serves as the core of a HSAS switch.

The main conclusions of this work are summarized as follows:

(1) Compact CMOS-MEMS switches are designed, fabricated and tested for up to 10GHz applications
(2) New CMOS-MEMS post-processing procedure is introduced and implemented successfully where the initial warping profile of the suspended structures can be different for the same device design, and the thermal treatment leading to the residual stress or plastic deformation in the MEMS structure takes place during the same dry etching step of the previous post-processing procedures by virtue of using an advanced RIE equipped with cryogenic cooling
(3) Enhanced designs of high RF power switches are fabricated and tested using the MetalMUMPs process
(4) Expanded version of the UWMEMS process is reported. A new post-processing procedure is developed allowing to implement several uncommon and new switch designs
(5) New switch designs are reported such as the hybrid self-actuation switch (HSAS), the thermal-restoring switch (TRS) and the 4-port gimbal-based switch (G-switch)
(6) New wafer-level packaging microfabrication process is developed and employed in building packaged RF MEMS switches with high yield and hermetic sealing, which are essential for building a realizing competitive devices and commercial products

7.2 Future Work

(1) Further development and characterization of the new CMOS-MEMS post-processing procedure, especially for implementing metal-metal contact-type switches and other novel structures towards high Q monolithically integrated passives and RF circuits

(2) Continuing the expansion and development of the UWMEMS processing in terms of incorporating HRS substrates, thicker structural layers and a reliable contact pair (e.g. Au-Ru). This would allow the implementation of PolyMUMPs-compatible and MetalMUMPs-compatible RF MEMS devices in the UWMEMS process

(3) Further characterization and optimization of the novel UWMEMS devices

(4) Characterization of the first-generation of silicon-core packaged switches and further optimization towards the second generation

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