Hybrid Amorphous Selenium-CMOS Photon-Counting X-ray Imager

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Many medical imaging modalities, such as mammography and micro-computed tomography, utilize digital X-ray imagers to observe human anatomy. Direct digital X-ray imagers rely on a sensor layer (typically a photoconductor) to convert X-ray photons to electrical charge, which can then be collected by pixel readout circuits. Whereas traditional integration-mode X-ray imagers typically integrate charge for long durations to acquire image frames, X-ray photon-counting imagers (PCIs) resolve each incident photon as it arrives. This allows for equal energy-weighting of photons and multi-spectral image capture, both of which enhance contrast in images. Furthermore, PCIs also allow for higher dynamic range since count rates are not limited by integration well capacity. Many hybrid X-ray PCIs have been reported in the literature using photoconductors such as CdTe and HgI_2. However, these photoconductors are expensive to fabricate, suffer from low yield over large areas, and have limited spatial resolution.

This thesis describes the design and characterization of the first hybrid X-ray amorphous selenium–CMOS PCI for mammography and micro-computed tomography. Amorphous-selenium (a-Se) can be thermally deposited over large areas, allowing for cheaper and scalable fabrication as well as higher spatial resolution. Two arrays of 26×196 pixels are implemented in CMOS and interface directly to an a-Se sensor layer. Counter arrays neighbor the pixel arrays and have a one-to-one relationship with pixels, incrementing every time a photon is detected. Novel readout circuits allow for ultra high-resolution pixels, each occupying only $11.44 \times 11.44\,\mu m^2$. Finally, the design of a custom PCB and FPGA system for characterizing the electronic performance of the PCI is described. The measured input-referred noise and threshold spread of the PCI are $41\,e^-_{rms}$ and $107\,e^-_{rms}$, respectively, when operating the imager as a row scanner. This will enable an energy resolution of 5.7 keV, suitable for the proposed applications. Further analysis was done to identify methods of reducing threshold spread as well. Finally, the concluding chapter summarizes this work, compares its performance to other PCIs in the literature, and identifies future work to improve its performance.

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Dedication

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Table of Contents

List of Tables

List of Figures

Abbreviations

μ-CT micro-computed tomography 1, 3, 9, 88

a-Se amorphous selenium xi, 2–5, 9, 10, 29–31, 37, 80, 87, 88

AD Analog Devices 65

ADC analog-to-digital converter 5, 13

CDF cumulative density function 7, 8, 34, 64, 71, 72, 78, 80, 85

CMFB common-mode feedback 13

CMOS complementary metal-oxide-semiconductor 2, 3, 6, 11, 23, 24, 88, 89

DAC digital-to-analog converter ix, xiii, 6, 61, 64–66, 68

DNL differential nonlinearity 65

DRAM dynamic random access memory 68

ehp electron-hole pair 3

ER error rate xii, 7, 8, 10, 31, 34, 35, 85, 87

ESD electrostatic discharge 52

FDA fully-differential amplifier 13

FET field-effect transistor 14, 23, 30

FF flip-flop xii, 45, 46, 49, 51

FIFO first-in, first-out 68

FPGA field-programmable gate array xiii, 42, 61, 62, 64, 66, 68

FSM finite-state machine 66

I/O input/output 42, 43, 52, 53

IC integrated circuit xiii, 61, 62, 65

INL integral nonlinearity 65

IOS input-offset subtraction xi, xiii, 16, 21, 23, 24, 26, 31, 96

LDO low-dropout regulator 61

LSB least-significant bit 49, 72, 74, 79, 85

MIMCAP metal-insulator-metal capacitor xii, 14, 23, 25, 29, 30, 34, 36, 37, 39, 51

MOS metal-oxide-semiconductor 11, 21

MSB most-significant bit xii, 43, 45, 46, 53, 54

NMOS N-channel metal-oxide-semiconductor 24, 42, 47, 63, 80, 83, 85

OOS output-offset subtraction xi, xiii, 14, 16, 21, 23–25, 27, 29, 31, 97

PA pre-amplifier ix, xi, xiii, 5, 12–19, 21, 23–27, 30, 34, 37, 38, 47, 49, 69, 72, 80, 83, 84, 89

PCB printed circuit board xiii, 60, 62, 63

PCI photon-counting imager iii, vi, ix, x, xiii, 3, 5, 6, 10, 11, 40, 60, 62, 69, 87–89

PCP photon-counting pixel 6–8, 10–12

PD probability of detection xii, 7, 8, 10, 31, 34, 35, 85, 87

PMOS P-channel metal-oxide-semiconductor xii, 24, 32, 42, 47, 63, 74, 78–80, 83

PSD power spectral density 64, 65

QE quantum efficiency xi, 3, 4, 9

RMS root-mean square 7, 64

SNR signal-to-noise ratio 6, 30

SPI serial peripheral interface 65, 68

USB Universal Serial Bus 61, 68

Chapter 1

Introduction

X-ray radiation and sensing are the basis of many medical imaging modalities such as micro-computed tomography (μ-CT) and mammography. The general approach in X-ray imaging is to radiate an object and sense the amount of radiation transmitted through the object. Since different substances attenuate X-rays to various extents, a shadow image is formed on the sensor. Mammography is the use of X-ray imaging to detect tumors and cancer precursors (e.g. microcalcifications) in human breast tissue [1]. Mammograms typically utilize low-energy X-rays (up to 30 keV) to image soft tissue, but studies have shown that dual-energy imagers can significantly improve contrast and reduce patient dose [2, 3]. μ-CT also benefits from dual-energy detectors, enabling better discrimination between tissues and materials in small animals [4]. In μ-CT, many X-ray images are taken from various angles and reconstructed algorithmically to produce a cross-sectional image of the object [5]. It is often used in small-animal research studies since it is non-invasive [4, 6].

This thesis describes the design and characterization of a novel photon-counting X-ray imager for mammography and μ-CT applications. Photon-counting imagers present many advantages, including energy discrimination for dual-energy imaging. This chapter will present a brief background on X-ray imaging and detection using semiconductor devices. It then proceeds to describe photon-counting imagers, their characterization, and finally outlines the specifications of this work to meet the needs of our applications.

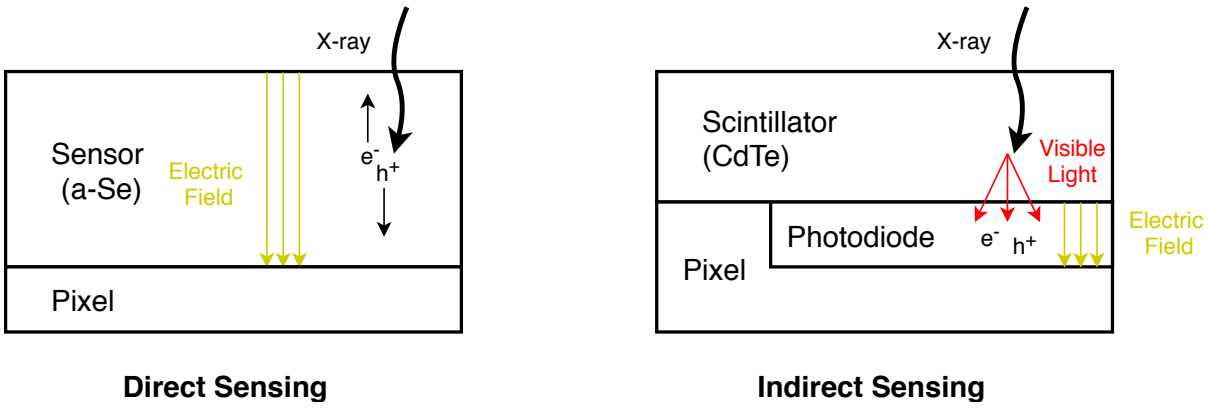


Figure 1.1: Comparison between direct and indirect X-ray sensors.

1.1 Digital X-ray Image Sensors

1.1.1 Background

X-ray sensing evolved over the last few decades from using traditional photographic films to digital sensors, allowing quicker image acquisition, easier image manipulation, and better dose efficiency [7]. Digital X-ray sensors utilize electronic circuits within pixel arrays on a complementary metal-oxide-semiconductor (CMOS) chip to sense the amount of incident radiation and form an image. A digital X-ray sensor can detect X-rays either indirectly or directly. Indirect sensing utilizes an intermediary scintillator to convert X-rays to visible light, which in turn is typically detected by a photodiode. On the other hand, a single sensing layer is used in direct sensing to convert X-rays to electrical charges, which are then sensed by dedicated pixel read-out circuits. When an X-ray strikes the sensor (typically a photoconductor), it creates a charge cloud within the sensor. Holes and electrons within the cloud are separated and collected by applying a high-voltage across the sensor. Figure 1.1 illustrates the difference between direct and indirect sensing.

1.1.2 Amorphous Selenium X-ray Sensor

Amorphous selenium (a-Se) is a photoconductor commonly used in X-ray imaging. It was first made popular and technologically matured in Xerox photocopiers, but has since proved suitable for X-ray imaging. Due to its amorphous nature, it is easily deposited over large areas. Crystalline photoconductors (such as cadmium telluride, CdTe), on the other

hand, require expensive bonding processes and suffer from low yield over large areas [8]. Another critical benchmark for X-ray sensors is their ability to stop X-rays. This is known as quantum efficiency (QE) and is quantified as

$$\mathrm{QE}(E_{ph}) = 1 - e^{-\mu(E_{ph})d} \ , \tag{1.1}$$

where d is the sensor's thickness, E_{ph} is the photon energy, and $\mu(E_{ph})$ is the sensor's linear attenuation coefficient at a particular photon energy [9]. Figure 1.2 shows the QE of a-Se over the diagnostic X-ray energy range for a few sensor thicknesses of interest [10].

The charge released Q_{ph} due to a photon interaction with a-Se is given by

$$Q_{ph} = E_{ph}/W_{\pm} \ , \tag{1.2}$$

where $W_{\pm}$ is the conversion gain, typically given in keV/electron-hole pair (ehp). $W_{\pm}$ depends on many factors including sensor thickness, electric field (i.e., bias voltage), and photon energy. At 10 V/µm and for diagnostic X-ray energies, $W_{\pm}$ ranges between 30-70 eV/ehp [11]. A major trade-off with conversion gain is dark current, which is the electric current flow through a-Se in the absence of photons (typically given in $\mathrm{mA/mm^2}$). Dark current can saturate a pixel, preventing it from detecting photons should they arrive. Increasing the bias voltage across a-Se reduces charge carrier travel times, increasing charge collection efficiency and therefor decreasing $W_{\pm}$ at the cost of higher dark current [12, 11].

The first hybrid a-Se-CMOS image sensor in [13, 14] demonstrated that a thermally deposited layer of a-Se can be coupled to an array of pixels. Most notably, it was (and remains) the highest-resolution direct X-ray image sensor to date.

1.2 Photon-Counting X-ray Imagers

Unlike integration-mode imagers, where a pixel integrates photocurrent for a (relatively long) duration during exposure, photon-counting imagers (PCIs) aim to detect and report every photon as it arrives. In the context of X-ray imagers, this effectively translates to very short integration times and highly sensitive pixel circuits. It has been demonstrated that PCIs are useful in diagnostic medical imaging of low-contrast tissue for various applications including μ-CT and mammography [15, 16]. PCIs are especially useful for the following reasons:

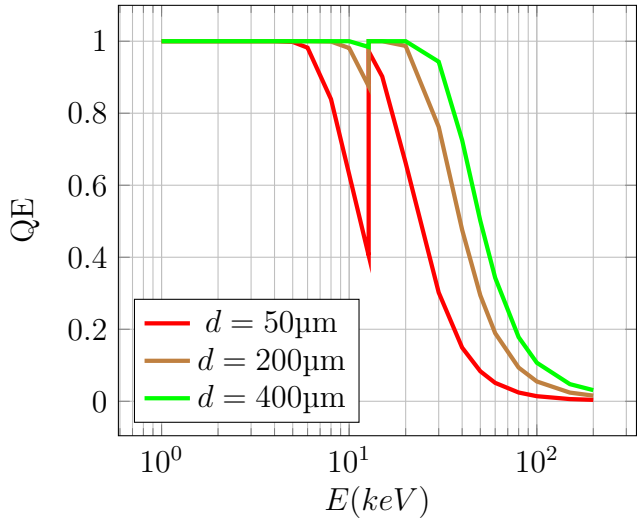


Figure 1.2: QE of a-Se over diagnostic X-ray energy range for various sensor thicknesses. K-edge is observed at 13 keV due to photoelectric absorption when the photon energy exceeds the orbital energy of the K shell.

1. Equal energy-weighting of photons: Each detected photon resolves to a single count regardless of its energy, unlike integration-mode sensors where higher energies are weighted more heavily. This translates to higher contrast for low-density objects [16].

2. Multi-spectral image capture: These can be captured by simultaneously setting different detection thresholds within pixels. This way, images of only low-density (e.g. breast tissue) or high-density objects (e.g. microcalcifications) can be reconstructed from a single exposure. Furthermore, contrast agents such as iodine can be used within a single exposure as well, significantly reducing patient dose and motion artifacts [17].

3. High dynamic range: The maximum count is limited by a pixel's count rate, which is highly dependent on the sensor's temporal characteristics rather than read-out circuit architecture. On the lower end, pixel dark count can be effectively eliminated by setting the detection threshold high enough to neglect dark current, leakage and noise.

4. Linearity: The image sensor's response is linear regardless of exposure since each photon is detected independently [8].

5. In-pixel digitization: Information is digitized as close to the X-ray sensor as possible, circumventing many typical read-out issues such as cross-coupling, noise contributions along the signal path from pixel to analog-to-digital converter (ADC), and buffer settling issues.

However, photon-counting also presents several limitations and challenges, some of which are exacerbated by the use of a-Se as a photodetector:

1. Crosstalk: An incident photon's charge cloud may be collected by several pixels, causing erroneous extra counts if its energy is sufficient to excite several pixels, or lost counts if it is not. In a multi-spectral detector, this may also cause a high-energy photon to be mistaken for a few low-energy photons. This is highly dependent on the a-Se's spatial resolution and limits the minimum pixel pitch.

2. Dead time: Pixels will typically exhibit a dead-time during reset when they are insensitive to incoming photons.

3. Pile-up: Charge "pile-up" may occur if photons arrive shortly after one another, increasing the perceived energy of a photon and potentially causing false counts.

4. Slow temporal response: The slow electron response of a-Se causes a long tail to follow the initial spike in pixel response upon the arrival of a photon. This increases risk of charge pile-up (above) and limits the count-rate as well. However, it has been demonstrated that pixels of pitch much less than the sensor depth are less susceptible to this effect [16]. This is known as the small-pixel effect.

1.2.1 PCIs in the Literature

Many X-ray PCIs are reported in the literature with a few common components. Namely, every pixel includes a charge pre-amplifier (PA), a comparator for energy thresholding, and at least one counter. Charge PAs are implemented using explicit capacitors in an amplifier's feedback loop and are often followed by a pulse shaper to remove dc offsets and attenuate charge pile-up issues. Many pixels include several comparators and counters to separate photon energies as well. This review is not meant to be exhaustive but will highlight a few works that are worth noting.

Perhaps the most significant and ongoing project is the Medipix, an on-going effort at CERN for medical imaging, high energy physics and other applications. The Medipix PCI

Reference	[21]	[20]	[23]	[24]
CMOS process (nm)	130	130	130	40
Sensor	CdTe	HgI_2	Si	Si
Active array size	8×4	128×128	128×128	24×18
Pixel size (μm^2)	756×800	60×60	75×75	100×100
Number of energy bins	256	3	1	1
Power per pixel (μW)	10000	4.6	26	35
Maximum count rate ($cps/\mu m^2$)	13	103	213	120
Input-referred noise (e^-_{rms})	-	68	123	117

Table 1.1: Comparison of X-ray PCIs in the literature.

has gone through three revisions thus far, with Medipix4 announced in 2017 but not yet released as of the time of writing. The Medipix3 stands out for its flexibility in operating modes, allowing trade-offs between pixel size ($55 \times 55\,\mu m^2$ or $110 \times 110\,\mu m^2$) and the number of photon energy bins. It also provides a mechanism to reduce charge sharing from an incident photon between several pixels [18, 19]. Another $60 \times 60\,\mu m^2$ pixel architecture reported in [20] saves area and power by utilizing a single comparator in conjunction with successive-approximation-like control logic to classify photons into three energy bins. The pixel also operates asynchronously, only resetting after a photon is detected and reducing the amount of dead-time. Reference [21] demonstrates a much larger pixel ($756 \times 800\,\mu m^2$) with more elaborate pulse-shaping and pile-up correction circuits. Some pixels opt for analog counters to reduce pixel area as well by accumulating discrete quanta of charge on a capacitor, as in [22]. Pixels in [23, 24] include in-pixel trimming digital-to-analog converters (DACs) to calibrate mismatches and attain tighter energy discrimination at the cost of larger pixels. Table 1.1 compares key metrics across a few PCIs.

1.3 Performance of Photon-Counting Pixels

Due to the digital output of photon-counting pixels (PCPs), performance must be characterized differently compared to integration-mode pixel architectures. Whereas the latter architectures are characterized by analog specifications such as signal-to-noise ratio (SNR),

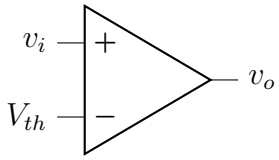


Figure 1.3: An ideal comparator.

well capacity, and noise floor, PCPs are characterized by maximum count rate, error rate (ER), and probability of detection (PD). This section will elaborate further on each of these specifications and more.

1.3.1 Comparator Probability of Output

At the heart of a PCP is a comparator as shown in Figure 1.3. An ideal comparator's output v_o is deterministic: if the input v_i is lower than the threshold V_{th}, the output is logic 0. If the threshold is exceeded, the output switches to logic 1. However, several non-idealities arise in practical comparators:

- Temporal noise v_n: Devices within the comparator exhibit noise (e.g. thermal noise), which can be modeled at the inputs of the comparator. Since it is additive to v_i, the comparator's output is statistical in nature, rather than deterministic. If the noise profile is Gaussian, the probability of output being 1 ($Pr(v_o = 1)$) is given by a sigmoid centered at V_{th}.
- Static input offset voltage V_{os}: Static input offset causes a shift in $Pr(v_o = 1)$ and can either be systematic or random. Systematic offset can arise due to comparator architecture or systematic device mismatches. On the other hand, random offset is statistical in nature and occurs due to random device mismatch.

These sources of uncertainty can be modeled at the comparator input as shown in Figure 1.4. Figure 1.5 shows an ideal comparator's deterministic output and a non-ideal comparator's statistical output, given as $Pr(v_o = 1)$. Note that the effective threshold $V_{th} + V_{os}$ is now defined as the input voltage at which $Pr(v_o = 1) = 0.5$. In other words, it is the input voltage for which v_o can be either 1 or 0 with equal probability. It can be shown that $Pr(v_o = 1)$ is a cumulative density function (CDF) of a normal distribution, and hence v_n (as a root-mean square (RMS)) can be extracted by observing $Pr(v_o = 1)$ at known confidence intervals [25]. For the example given in Figure 1.5, V_{os} can be directly

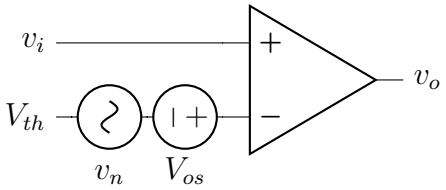


Figure 1.4: Comparator with input-referred noise and offset

observed as 1 mV. v_n is most conveniently calculated by observing the input at which $Pr(v_o = 1) = 67\%$ (in relation to V_{os}), given here as $v_n = 1.5\,\text{mV} - 1\,\text{mV} = 0.5\,\text{mV}_{\text{rms}}$.

A CDF similar to that in Figure 1.5 can be obtained experimentally by slowly sweeping v_i while keeping V_{th} constant and, at each point, observing $Pr(v_o = 1)$. Alternatively, V_{th} can be swept instead, which may be easier to implement for a given comparator as is the case in our work. If $Pr(v_o = 1)$ is plotted against V_{th}, the CDF is simply a mirrored version of the original and the analysis above applies directly.

V_{os} was assumed to be static and known so far. However, on the array level, each pixel will demonstrate its own random offset with standard deviation $\sigma(V_{os})$. If a global threshold is used (which is usually the case), the total uncertainty in the threshold applied on each pixel is given by

$$\sigma^2(V_{th}) = \sigma^2(v_n) + \sigma^2(V_{os}) \ , \tag{1.3}$$

where $\sigma^2(.)$ denotes the variance of the random variable. An analogous quantity that is more relevant for imaging purposes is the uncertainty in photon energy threshold $\sigma(E_{th}) = \sigma(V_{th})C_i W_{\pm}/q$, where C_i is the capacitance on which charge from an incident photon is collected and q is the unit of elementary charge.

1.3.2 Photon-Counting Pixel Specifications

We can now define several metrics for the performance of PCPs:

- PD is given by $Pr(v_o = 1)$ for a given input voltage v_i that is developed due to an incident photon of energy E_{ph}.
- ER is given by $Pr(v_o = 1)$ in the absence of photons (i.e., $v_i = 0$). Note that ER can be non-zero due to temporal noise and potential systematic issues.

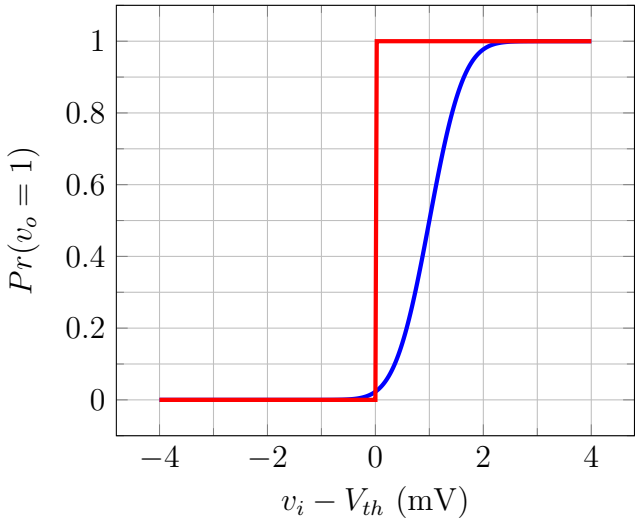


Figure 1.5: Probability of output for ideal comparator (red) and non-ideal comparator with $V_{os} = 1\,\text{mV}$ and $v_n = 0.5\,\text{mV}_{\text{rms}}$ (blue).

- Maximum count rate is the number of photons a pixel can detect within unit time, typically given in counts/second (cps). This is often normalized by area as well and typically reported in cps/mm^2. Count rate can be limited by the X-ray sensor layer (a-Se), pixel architecture, or system architecture.

1.4 Summary of Application Requirements and Specifications

We derive requirements for the imager based on the target applications of mammography and μ-CT [15, 16]. Given a photon energy range of 20-50 keV, a-Se must be greater than 200 µm thick to guarantee a QE $> 30\%$ for all photon energies of interest. In order to take advantage of the small-pixel effect, the pixel pitch should be 10-20x smaller than that [16]. We aim for at least 15x smaller, yielding a maximum pixel pitch of 13.3 µm.

Photon energy discrimination and the minimum detectable energy are driven by the same specification. That is, to detect a 20 keV photon is equivalent to discriminating between photons with an energy resolution of 20 keV. Assuming 6σ separation in $Pr(v_o = 1)$ between the presence and absence of a photon, and given a minimum photon energy of $E_{ph} = 20\,\text{keV}$, the uncertainty of energy threshold $\sigma(E_{th}) < 3.3\,\text{keV}$. This translates to

Parameter	Specification
Sensor	a-Se
Sensor thickness (µm)	200
Pixel area (µm^2)	$\leq 13 \times 13$
Minimum detectable E_{ph} (keV)	20
Uncertainty of photon energy threshold $\sigma(E_{th})$ (keV)	3.3
Probability of detection ($E_{ph} = 20\,\text{keV}$)	99.87%
Error rate ($E_{ph} = 20\,\text{keV}$)	0.13%
Maximum count rate (cps/µm^2)	250

Table 1.2: Summary of specifications for PCI in this work.

a PD and ER of 99.87% and 0.13%, respectively. Lastly, we aim to achieve a maximum count rate greater than the highest we found in literature [23]. Note that a-Se will likely be the limiting factor here rather than the read-out circuit.

A summary of imager specifications is given in Table 1.2.

1.5 Thesis overview

This thesis describes the design of a novel PCI. It is organized as follows:

- Chapter 2 begins with a generic model of a PCP then proceeds to describe the analysis, design and optimization of a transistor-level implementation.
- Chapter 3 describes the PCI system architecture including power distribution, control signal and bias generation, pixel counters, and verification.
- Chapter 4 describes the characterization setup and discusses the PCI's bench-top performance.
- Chapter 5 concludes this work with a brief summary.

Chapter 2

Pixel Design, Modeling and Simulation

This chapter focuses on the design of our PCP. It begins by introducing a simple architecture and implementation of a PCP in CMOS technology. Since such an architecture does not meet our specifications for input offset uncertainty due to random mismatch, the following sections describe methods to reduce mismatch. We then analyze the finalized pixel architecture and design it to meet the specifications in Table 2.1, including the pixel layout. Each of these subsections are accompanied with simulations to aid the design process. Finally, we describe the design of test pixels that enable easier bench-top characterization of the complete X-ray PCI.

We derive pixel specifications based on the imager specifications in Table 1.2. Assuming the pixel pitch requirement is met, photon count rate translates directly to a minimum pixel count rate of 42 000 cps/pix. It is often more convenient to cite its reciprocal, pixel period $T_{pix} < 240\,\mu s$ during which a complete integration to resolve a photon is completed. Note T_{pix} is much longer than the expected duration of a photon event, which is on the order of a few microseconds [12]. Therefore, we choose a more strict specification $T_{pix} < 10\,\mu s$.

The minimum detectable photon energy E_{ph} (and hence, $\sigma(E_{th})$) drive the specifications for voltage threshold uncertainty $\sigma(V_{th})$. Early estimates of integration capacitance C_i yield 8-12 fF, including a top electrode and a few metal-oxide-semiconductor (MOS) devices. Assuming $C_i \approx 10\,fF$ and $W_{\pm} = 50\,eV/ehp$, $\sigma(V_{th}) < 1.06\,mV_{rms}$. If we assume temporal noise v_n and random offset $\sigma(V_{os})$ contribute equally, each must be less than $0.75\,mV_{rms}$. Table 2.1 summarizes pixel specifications which will guide the design process below.

We chose a TSMC 180 nm CMOS process since a hybrid selenium-CMOS image sensor

Pixel pitch	13.3 µm
$\sigma(V_{th})$	1.06 $\mathrm{mV_{rms}}$
v_n	0.75 $\mathrm{mV_{rms}}$
$\sigma(V_{os})$	0.75 $\mathrm{mV_{rms}}$
T_{pix}	10 µs

Table 2.1: Summary of pixel specifications.

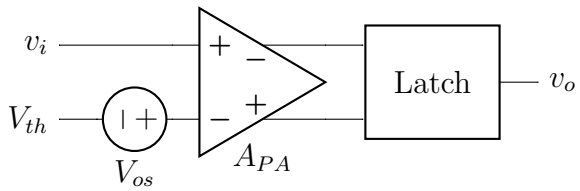


Figure 2.1: Comparator with input-referred random offset, composed of a PA followed by a dynamic latch.

was already demonstrated in this technology [13]. Relevant parameters for this process are introduced throughout the text as necessary.

2.1 Pixel Architecture

We start with the simplest PCP, composed of a comparator. Within the comparator is a pre-amplifier (PA) followed by a dynamic latch as shown in Figure 2.1. This pixel has two phases: track and latch. During the track phase, the voltage developed on an input capacitance due to an incident photon is compared to a threshold V_{th}. During the latch phase, the latch is enabled to conclude a comparison and utilizes positive feedback to output digital signal levels. The PA's purpose is two-fold: to amplify input signals to inhibit latch mismatch as well as minimize kickback from the latch onto the input node when the latch is enabled [25]. Note that the input signal here is a voltage and not a current, which should be the case for an incoming photon. We will first develop a model and design suitable for voltage comparison then modify it for a current input integrated onto a capacitor.

Each stage of the comparator exhibits an input-referred offset due to random transistor

mismatch mismatch $\sigma(V_{os})$ given by

$$\sigma^2(V_{os}) = \sigma^2(V_{os,PA}) + \frac{\sigma^2(V_{os,latch})}{A_{PA}^2} \ , \tag{2.1}$$

where $V_{os,PA}$ and A_{PA} are the input-referred offset and gain of the PA, respectively, and $V_{os,latch}$ is the input-referred offset voltage of the latch. All offsets are Gaussian random variables for which σ^2 represents the variance. This assumes no systematic input offset as well (i.e., mean is 0 V). Depending on the architecture, a typical PA exhibits an input offset due to random transistor mismatch on the order of $\sigma(V_{os,PA}) \approx 15\,\mathrm{mV_{rms}}$. Similarly, a typical latch exhibits an input offset due to uncertainty on the order of $\sigma(V_{os,latch}) \approx 17\,\mathrm{mV_{rms}}$. Even if the latch's offset is eliminated, we are still limited here by $V_{os,PA}$.

2.1.1 Pre-Amplifier Implementation

The purpose of PA is to provide the necessary gain to attenuate the latch's offset and isolate the input node to avoid latch kickback. Therefore, it must exhibit low mismatch as well. It must also have minimal input capacitance, since this will contribute directly to the pixel's input capacitance. Reference [26] suggests a PA architecture for a flash ADC, which has similar requirements to our pixel. This is shown in Figure 2.2. In order to understand this topology, first assume M7 and M8 are removed from the circuit. With M7 and M8 removed, this is a fully-differential amplifier (FDA) with cascodes (M3 and M4) at the input to reduce the Miller effect (and hence, input capacitive loading). Diode-connected devices M5 and M6 are used for loads, and hence the output common-mode level is set by the source-to-gate voltage V_{SG} of these devices. This eliminates the need for a common-mode feedback (CMFB) circuit, significantly reducing area and simplifying the design. The dc gain of the PA A_{PA} can be expressed as

$$A_{PA} \approx \frac{g_{m1}}{g_{m5}} = \sqrt{\frac{\mu_n(W_1/L_1)}{\mu_p(W_5/L_5)}} \ , \tag{2.2}$$

where μ_n and μ_p are the transistor electron and hole mobilities, respectively, and W_i and L_i are the channel width and length of device i, respectively. Since this is independent of bias current, the output common-mode range can be set independently from the gain.

We now consider the effect of M7 and M8. These devices are used to source more current into the input pair, increasing the small-signal transconductance g_{m1} without affecting the output common-mode level (assuming their output resistance is high). As a

result, A_{PA} becomes:

$$A_{PA} \approx \frac{g_{m1}}{g_{m5}} = \sqrt{\frac{\mu_n (W_1/L_1) I_{D1}}{\mu_p (W_5/L_5) I_{D5}}} \ , \tag{2.3}$$

where I_{Di} is the bias current of device i.

Of critical importance, especially for output-offset subtraction (OOS) (explained below), is the output swing of the PA. On the lower end, M3 must remain in saturation in order to limit the voltage swing at the drain of M1. On the upper end, it is limited by M5 remaining on (this will likely occur before M7 enters triode). Similarly, the input common-mode range is bound on the lower end by M1 remaining on and M9 remaining in saturation. On the upper end, it is bound by M1 remaining in saturation. Therefore:

$$V_{G3} - V_{t3} < v_o^- < V_{DD} - |V_{t5}| \ , \text{ and} \tag{2.4}$$

$$V_{t1} + V_{ov1} + V_{ov9} < v_i^+ < V_{G3} - V_{ov3} + V_{t1} - V_{t3} \ , \tag{2.5}$$

where V_{ti} and V_{ovi} are the threshold and overdrive voltages of device i, respectively. These present a trade-off between input and output swing depending on V_{G3}. A lower V_{G3} provides wider output swing at the expense of a narrower input swing. This can be optimized since input signal levels are known (and quite low). Input common-mode level in the final pixel design (described in section 2.3) can be set by V_{rst}.

As will be shown in the final pixel design, the load capacitance seen by a PA during reset is dominated by C_{os}. This is chosen as the minimum metal-insulator-metal capacitor (MIMCAP) size (20 fF). Assuming a typical system clock period of 20 ns and 7 time constants (7τ) for settling, $\tau < 2.9$ ns and the maximum output resistance R_o of the PA is

$$R_o = (1/g_{m5}) /\!/ r_{o5} /\!/ r_{o7} \approx 1/g_{m5} < \frac{2.9\,\text{ns}}{20\,\text{fF}} = 143\,\text{k}\Omega \ , \tag{2.6}$$

where r_o is the output resistance of a field-effect transistor (FET) in saturation. Note that the bandwidth requirements are set solely by M5 as a first-order approximation.

During the initial design, the PA was parameterized in order to facilitate the design of multiple stages with various gains, as will be shown in later sections. Current density in all devices is set constant, while A_{PA} can be tuned easily by adjusting a common transistor

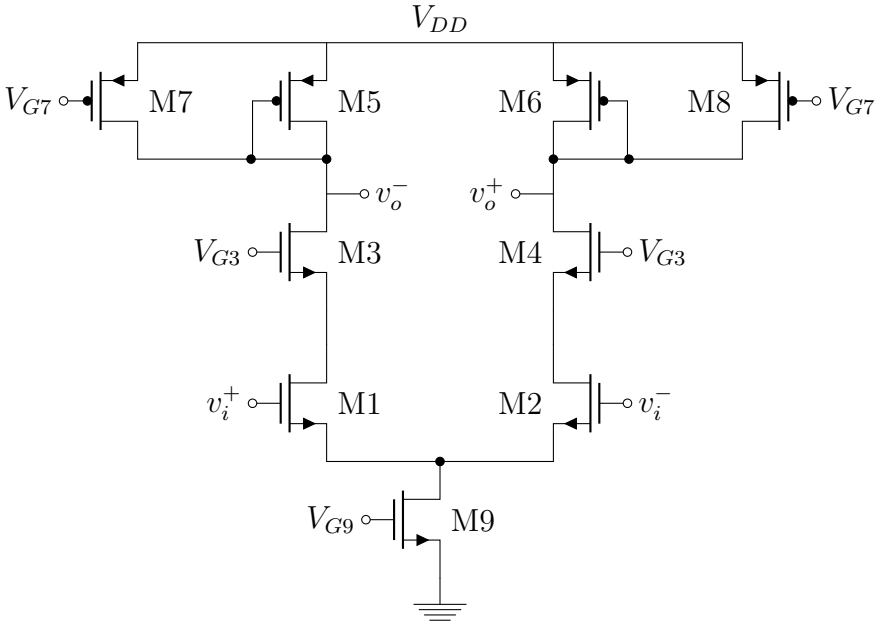


Figure 2.2: PA schematic.

width factor W_{fac}. The bias points of devices are chosen to reduce mismatch effects; that is, the input device M1 is biased at a low overdrive voltage V_{ov} while current mirrors M7 and M9 are biased at higher V_{ov} [27]. The load device M5 size is not dependent on W_{fac} and is biased to sink a constant current such that the output common-mode level is centered within the output swing. Lastly, M3 is set to match M1 in size and bias conditions for simplicity. Table 2.2 summarizes the geometry and bias points of all devices.

Device	W (nm)	L (nm)	$\lvert I_D \rvert$ (µA)	V_{ov} (mV)
M1	$220 \cdot W_{fac}$	200	$3.5 \cdot W_{fac}$	110
M3	$220 \cdot W_{fac}$	200	$3.5 \cdot W_{fac}$	110
M5	220	1000	3.5	-
M7[1]	$220 \cdot W_{fac}$	300	$3.5 \cdot W_{fac}$	250
M9	$220 \cdot W_{fac}$	400	$7 \cdot W_{fac}$	235

Table 2.2: Geometry and bias point of PA devices.

Figure 2.3 shows a few key simulation results while sweeping W_{fac} that can summarize the PA's performance. Its gain A_{PA} and the input-pair's transconductance g_{m1} increase linearly as expected, while bandwidth is relatively constant at 80 MHz (not shown). Figure 2.4 shows the statistical distribution of $V_{os,PA}$ for $W_{fac} = 4$. It is Gaussian as expected, and its spread is inversely proportional to W_{fac}^2 as expected from mismatch models.

2.1.2 Latch Implementation

A dynamic latch is used to provide the large gain needed at the end of a comparison in order to output digital logic levels. Such a latch is proposed in [25], which consists of two back-to-back inverters and a few switches as seen in Figure 2.5. The latch begins with its input `latch` signal low, allowing the previous stage to set the initial voltage at nodes v_o' and $\overline{v_o'}$. Note that M7 and M8 are both off, disabling the inverters. When `latch` switches high, M5 and M6 turn off while M7 and M8 turn on, enabling positive feedback. Digital buffers are added to the outputs in order to drive column buses and match capacitive loads at v_o' and $\overline{v_o'}$.

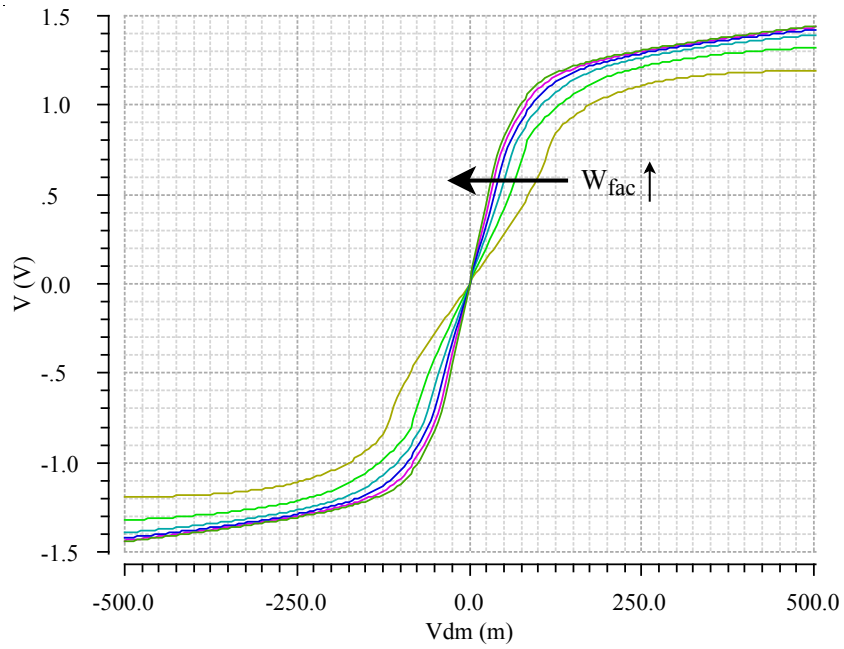
The latch's mismatch is simulated in a transient analysis. A fast clock signal continuously triggers the latch while its inputs are ramped slowly, and $V_{os,latch}$ is defined as the input `Vip` − `Vin` when v_o resolves to 1 for the first time. Note that the resolution of this experiment is limited by the ratio of clock speed to input ramp speed, which is made sufficiently high to attain a meaningful result.

Figure 2.6 shows $V_{os,latch}$ for increasing device sizes. All input devices M1-4 are sized equally for simplicity. The result is inversely proportional to the input device's area (i.e. square of its width, since its length is constant), which follows mismatch models as expected.

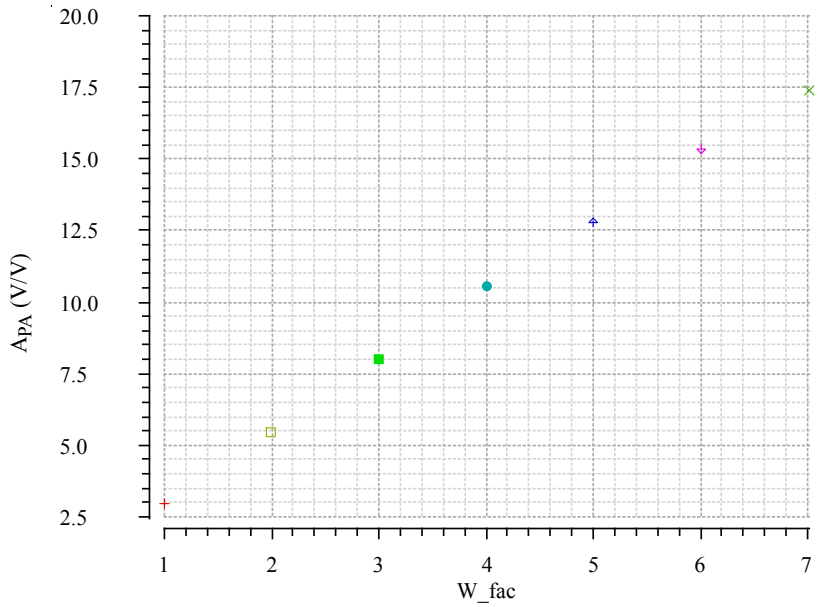
2.2 Offset Correction

One method to reduce the effective offset of the PA is to store it on a capacitor during a reset phase, then connect the capacitor during comparison such that the offset is removed. There are two methods of storing the offset of a PA: input-offset subtraction (IOS) and output-offset subtraction (OOS) [28]. In IOS, the PA is connected in a unity-gain feedback

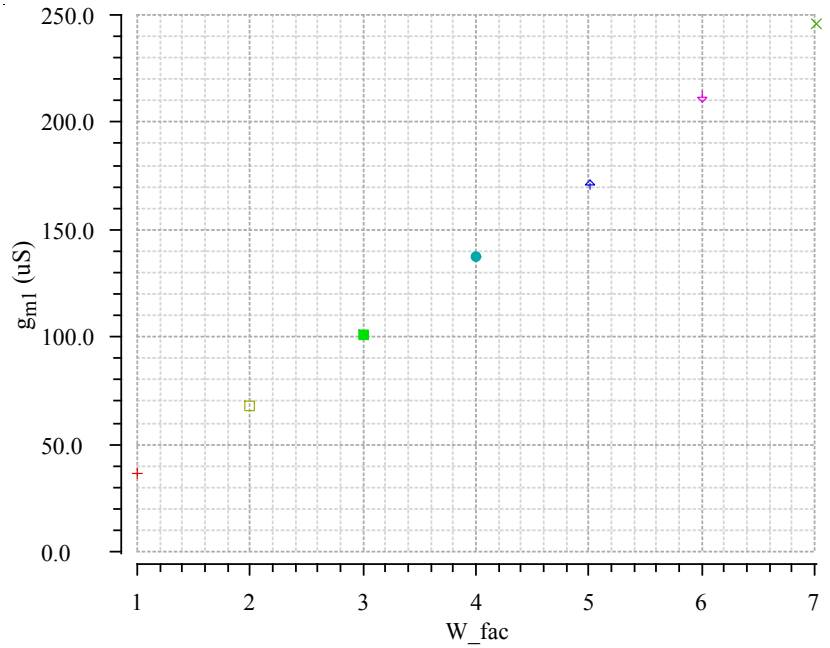
[1] This is a slight deviation from the correct width of $220(W_{fac}-1)$ to maintain the same operating point. However, this has a minimal effect on its overdrive V_{ov} and the drain current is set correctly regardless since its bias V_{G7} is adjusted accordingly.



(a) Differential output of PA vs differential input (common-mode input 1.1 V). Steeper curves correspond to higher W_{fac}.

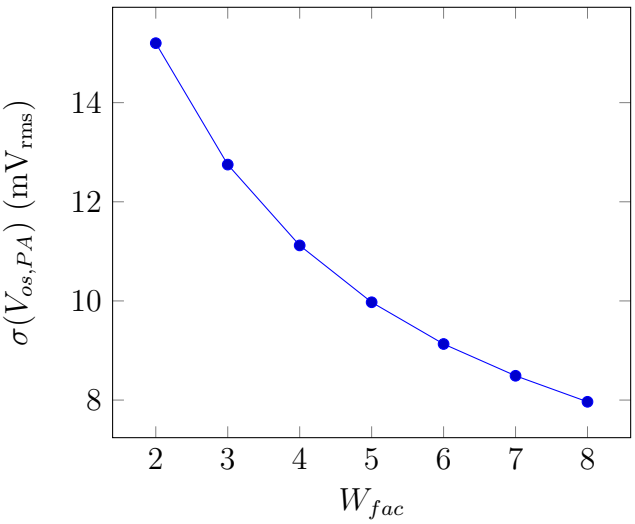


(b) dc gain A_{PA} of PA.

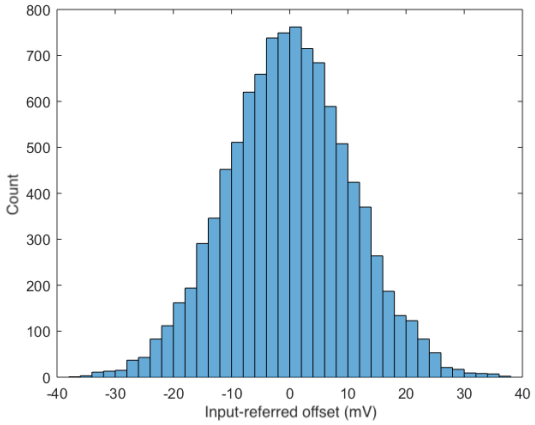


(c) Small-signal transconductance g_{m1} of input device M1 in PA.

Figure 2.3: Effect of W_{fac} on PA voltage transfer characteristic and dc gain from circuit simulations.



(a) Input-referred voltage offset of PA due to random mismatch for increasing device sizes.



(b) Statistical distribution of PA input-referred offset $V_{os,PA}$ for $W_{fac} = 4$. $\sigma(V_{os,PA}) = 10.7\,\mathrm{mV_{rms}}$ (10,000 points).

Figure 2.4: Input-referred offset voltage of PA due to random mismatch from Monte Carlo simulations.

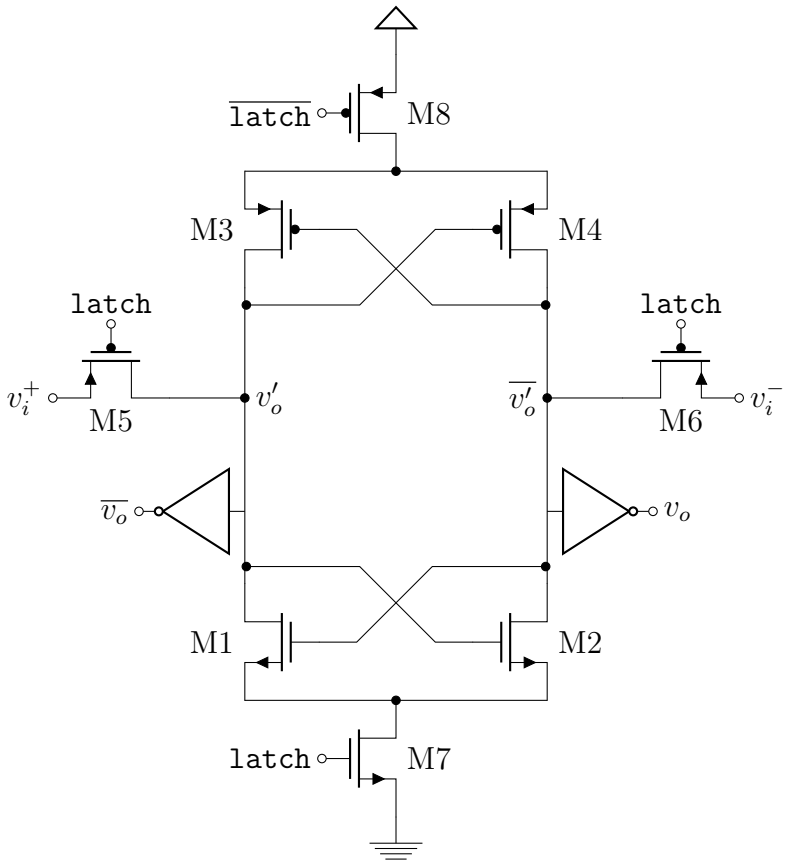


Figure 2.5: Dynamic latch schematic.

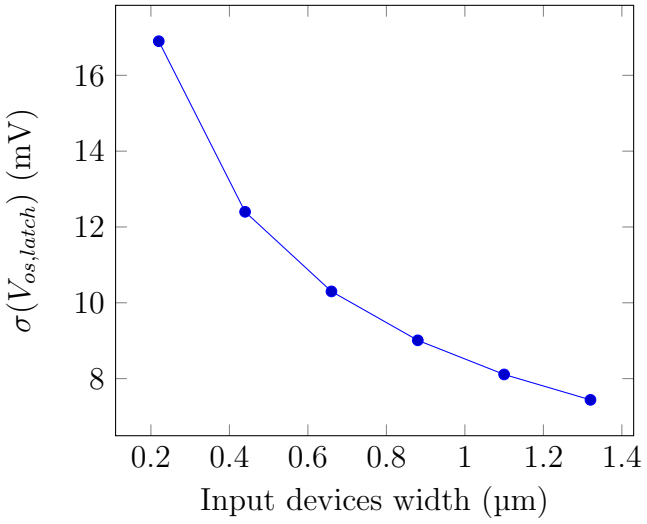


Figure 2.6: Latch input-referred random offset due to mismatch.

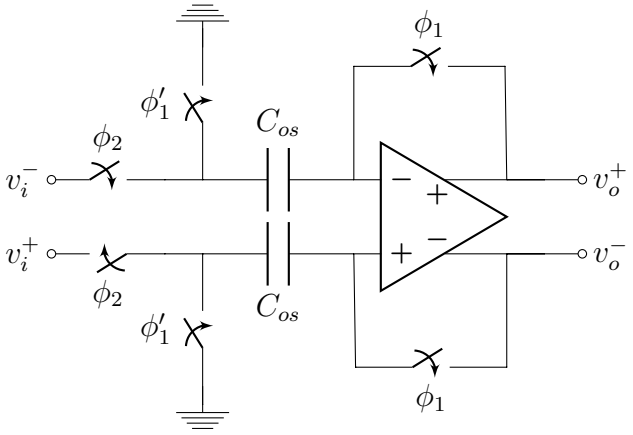
configuration and the offset is stored on input coupling capacitors. In OOS, the PA inputs are shorted and the (amplified) offset is stored on coupling capacitors at the output. These two topologies are shown in Figure 2.7. Note that all switches shown are active-high.

Both circuits operate in two phases: reset and track (note the absence of a latch). The offset is stored on the input/output capacitors C_{os} during the reset phase, then used to cancel the offset during the track phase. Timing for both of these circuits is as follows:

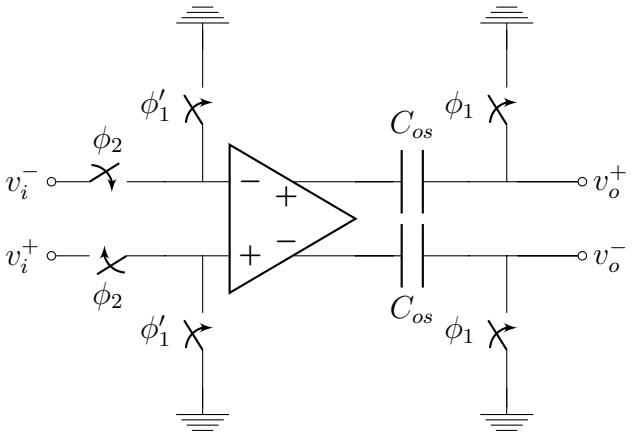
1. Reset: ϕ_1 and ϕ_1' are both on and ϕ_2 is off. The offset of the PA is stored on the capacitors C_{os}. ϕ_1 shuts off first, releasing charge onto C_{os} due to MOS switch non-idealities. ϕ_1' then shuts off, also releasing charge onto floating capacitances on its terminals. This concludes the reset phase.

2. Track: ϕ_2 turns on, connecting the input signals v_i^+ and v_i^- to the PA. The charge released by ϕ_1' shutting off is discharged through the inputs. Capacitors C_{os} are connected in series such that offsets are subtracted from the PA's input or output (in IOS and OOS, respectively).

More detail on the operation of these circuits can be found in [28]. A residual offset remains due to clock feedthrough from MOS switches, imperfect offset storage, and capacitor mismatch. The variance of input-referred residual offset voltages $\sigma^2(V_{ios})$ and $\sigma^2(V_{oos})$



(a) Input-offset subtraction.



(b) Output-offset subtraction.

Figure 2.7: Offset correction schemes.

can be expressed as

$$\sigma^2(V_{ios}) = \frac{\sigma^2(V_{os,PA})}{(A_{PA}+1)^2} + \frac{\sigma^2(\Delta Q_{sw})}{C_{os}^2} + \frac{\sigma^2(\Delta C_{os})}{C_{os}^2}\frac{Q_{sw}^2}{C_{os}^2} \text{ , and} \tag{2.7}$$

$$\sigma^2(V_{oos}) = \frac{1}{A_{PA}^2}\left[\frac{\sigma^2(\Delta Q_{sw})}{C_{os}^2} + \frac{\sigma^2(\Delta C_{os})}{C_{os}^2}\frac{Q_{sw}^2}{C_{os}^2}\right] , \tag{2.8}$$

where C_{os} and ΔC_{os} are the nominal and mismatch capacitance of the offset storage capacitors, and Q_{sw} and $\Delta(Q_{sw})$ are the nominal and mismatch in charge released onto C_{os} when ϕ_1 switches off, respectively. Switch ϕ_1' does not contribute to offset since any charge errors due to switching are drained by switch ϕ_2 during comparison.

As shown in Equations 2.7 and 2.8, OOS can result in a lower residual offset since $V_{os,PA}$ is eliminated completely and the voltage developed on C_{os} when ϕ_1 is attenuated by A_{PA}. However, A_{PA} should be limited to ensure the PA is operating within the linear region. Care must also be taken to ensure its inputs are within the common-mode input range since they are dc-coupled. Neither of these is a concern in IOS since it resets in unity-gain feedback and inputs are ac-coupled. The PA must be stable in unity-gain feedback but this is guaranteed since it consists of a single stage only. IOS presents a higher input capacitance than OOS as well, making it unsuitable as a first stage for our pixel.

The term $\frac{\sigma^2(\Delta C_{os})}{C_{os}^2}\frac{Q^2}{C_{os}^2}$ in Equations 2.7 and 2.8 is the contribution of mismatch between coupling capacitors C_{os}. Mismatch between two closely-placed MIMCAPs is given by [29]

$$\frac{\sigma(\Delta C_{os})}{C_{os}}(\%) = \frac{2.5563}{\sqrt{(WL)_{os}(\mu m^2)}} , \tag{2.9}$$

where $(WL)_{os}$ is the MIMCAP area. In the TSMC 180 nm CMOS process, MIMCAPs have a density of 1 fF/µm^2, and the smallest size allowed is a 4 x 4 µm^2 with a nominal capacitance of 20 fF (including parasitics).

There are two non-ideal effects when we operate FET switches. Charge injection is a phenomenon whereby charge stored in the FET channel are released to the drain and source terminals when it is shut off. Similarly, clock feedthrough occurs when the gate control signal toggles and couples charge onto the drain and source terminals through the gate-drain and gate-source overlap capacitances. The charge injected onto the drain or source terminal is given by [25]

$$Q_{ch} = W_{ch}L_{ch}C_{ox}(|V_{GS}| - |V_t|)/2 , \tag{2.10}$$

where W_{ch} and L_{ch} are the channel width and length, C_{ox} is the gate oxide capacitance per unit area, and V_{GS} and V_t are the gate-source and threshold voltages, respectively (shown in absolute value for both N-channel metal-oxide-semiconductor (NMOS) and P-channel metal-oxide-semiconductor (PMOS) devices). It has been demonstrated that the charge will split equally between the source and drain if the gate voltage rise/fall time is fast enough, hence the factor of 2 [30]. Since charge injection Q_{ch} is usually dominant over clock feedthrough, the total charge released into the drain or source is $Q_{sw} \approx Q_{ch}$. The last term $\frac{\sigma^2(\Delta Q_{sw})}{C_{os}^2}$ in Equations 2.7 and 2.8 is due to the mismatch in charge injection and feedthrough ΔQ_{sw}, which is typically 1-2 orders lower than Q_{sw} [25, 28]. In the TSMC 180 nm CMOS process, the minimum W_{ch} and L_{ch} are 220 nm and 180 nm respectively. C_{ox} is nominally $8.85\,\mathrm{fF/\mu m^2}$, V_{tn} is nominally 490 mV, and V_{tp} is nominally −492 mV. Given these parameters, the standard deviation of total mismatch due to switch and capacitor non-idealities is approximately $0.4\,\mathrm{mV_{rms}}$.

If the latch is included, its offset $V_{os,latch}$ is attenuated by A_{PA} (refer to Equation 2.1). This is likely to dominate and can be reduced by increasing the gain A_{PA} or adding more gain stages. In the case of IOS, $V_{os,PA}$ is the second-largest contributor to offset and can also be reduced by increasing A_{PA}, but other factors will often limit how high it can go. Since A_{PA} is also limited in OOS, we will require multiple gain stages as Section 2.3 will describe. Offset due to C_{os} mismatch is negligible and will be ignored in upcoming sections.

2.2.1 Input-Offset Subtraction Simulations

Figure A.1 (see Appendix A) shows the testbench used to verify IOS. A transient simulation is used since a sequence of events is needed. `RST` and `RST_D` are asserted first (`RST_B` is simply the inverse of `RST` for PMOS switches), with the latter remaining high slightly longer to minimize charge injection errors as explained before. `COMP` is a non-overlapping signal that is asserted afterwards and throughout a comparison to connect the input signals to the PA (`COMP_B` is the inverse of `COMP`). Inputs `vip` and `vin` are both ramped in opposite directions to simulate the output of a previous differential stage, and key design parameters are defined as:

1. Gain $A_{PA} = \frac{dv_o}{dv_i}$ when $v_i = 0$, where $v_i = \texttt{vip} - \texttt{vin}$ and $v_o = \texttt{vop} - \texttt{von}$.
2. Intrinsic input-referred mismatch $V_{os} = v_{i3}$ when $v_o = 0$, where $v_{i3} = \texttt{vip3} - \texttt{vin3}$.

3. Corrected mismatch $V_{ios} = v_i$ when $v_o = 0$.

Figure 2.8 shows the standard deviation of intrinsic and corrected offsets $\sigma(V_{os})$ and $\sigma(V_{ios})$, respectively. $\sigma(V_{os})$ matches the results from dc simulations and $\sigma(V_{ios})$ shows 7x reduction in mismatch after correction. A_{PA} also matches results of dc simulations (refer to Figure 2.4). $\sigma(V_{ios})$ follows the trend as expected, ultimately limited by clock injection. The asymptotic limit is approximately 0.45 mV, which reasonably matches our model.

2.2.2 Output-Offset Subtraction Simulations

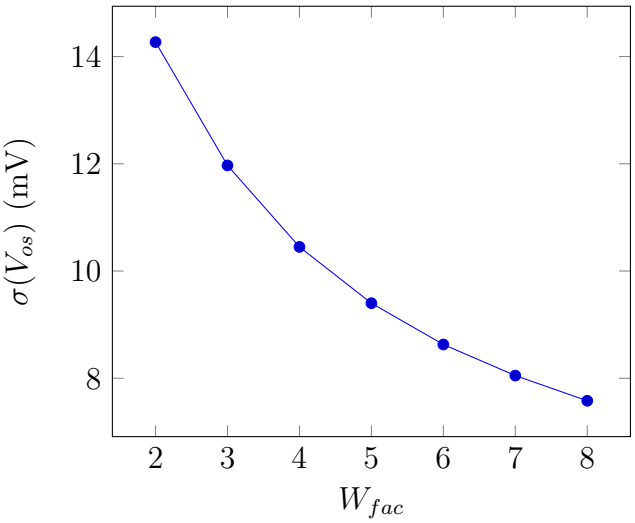
Figure A.2 (see Appendix A) shows the testbench used to verify OOS. A transient simulation is used since a sequence of events is needed. `RST` and `RST_D` are asserted first, with the latter remaining high slightly longer to minimize charge injection errors as explained before. `COMP` is a non-overlapping signal that is asserted afterwards and throughout a comparison to connect the input signals to the PA. The negative input signal `vin` is fixed at a specified "reset level", while the positive input `vip` is ramped during comparison. Key design parameters are defined as:

1. Gain $A_{PA} = \frac{dv_o}{dv_i}$ when $v_i = 0$, where $v_i = \texttt{vip} - \texttt{vin}$ and $v_o = \texttt{vop\_oos} - \texttt{von\_oos}$.
2. Intrinsic input-referred mismatch $V_{os} = v_i$ when $v_{o1} = 0$, where $v_{o1} = \texttt{vop\_fdp} - \texttt{von\_fdp}$.
3. Corrected mismatch $V_{oos} = v_i$ when $v_o = 0$.

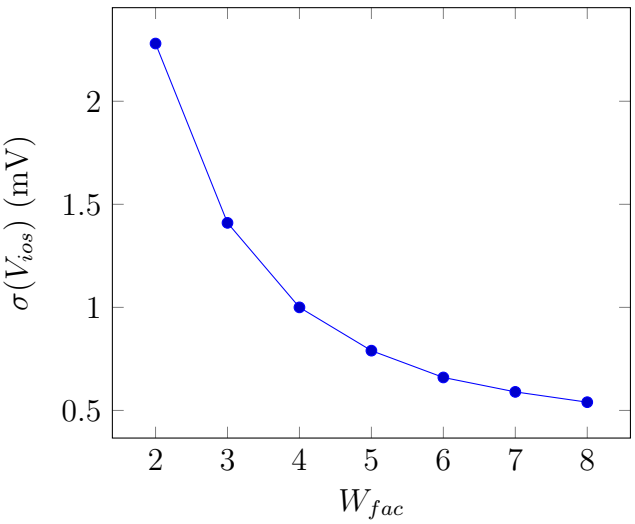
Figure 2.9 shows $\sigma(V_{os})$ and $\sigma(V_{oos})$ while sweeping W_{fac} from a Monte Carlo simulation. Extracting $V_{os,PA}$ in this testbench is primarily useful to compare with the values obtained from dc simulations and matches them closely. Notice that V_{oos} is less than 50 µV and decreasing for small geometries but increases drastically when $W_{fac} \geq 5$. This is because pixels begin to saturate during reset, causing imperfect offset storage and correction.

2.3 Finalized Pixel Design

Figure ?? shows the final pixel architecture and timing of digital control signals. A few changes were made here. First, two PA stages are used, with only one set of MIMCAPs used to store the offsets of both stages. This is mainly to minimize the pixel pitch, as

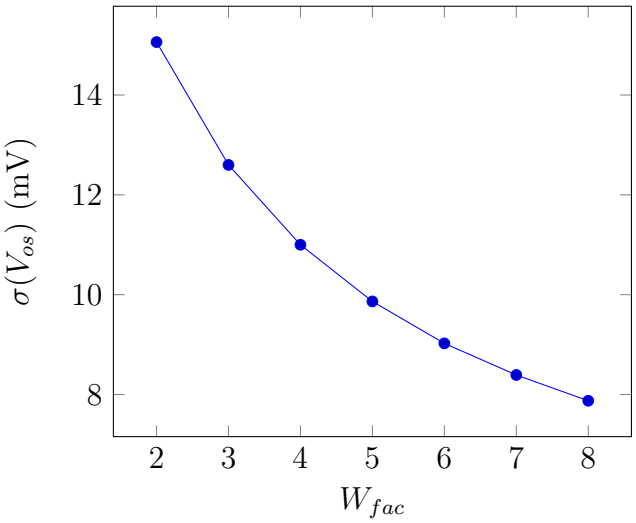


(a) Intrinsic input-referred random offset of PA.

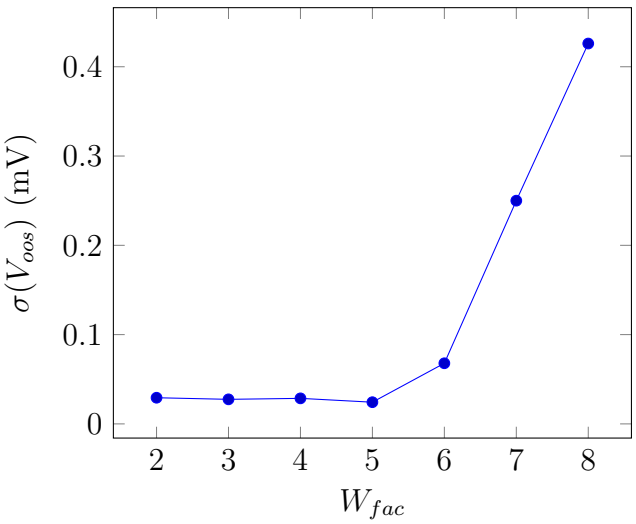


(b) Corrected input-referred random offset of PA.

Figure 2.8: Transient simulations sweep of W_{fac} in IOS testbench.

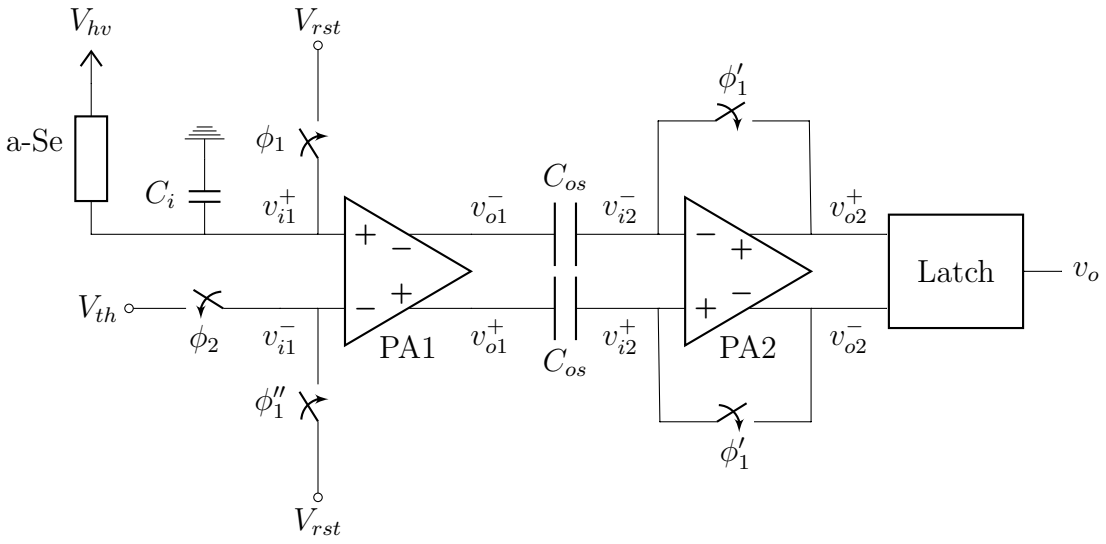


(a) Intrinsic input-referred random offset of PA.

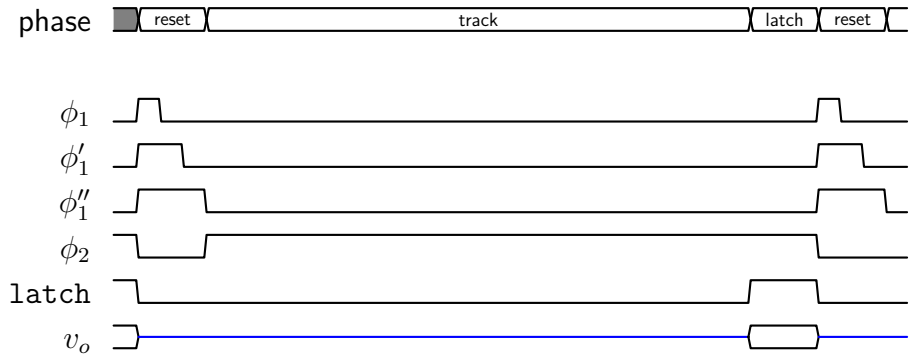


(b) Corrected input-referred random offset of PA.

Figure 2.9: Transient simulations sweep of W_{fac} in OOS testbench.



(a) Pixel architecture.



(b) Pixel timing diagram.

Figure 2.10: Pixel architecture and timing diagram.

MIMCAPs are relatively large. Also, current input from a-Se is integrated onto a parasitic capacitor C_i at the input node. Subsequent sections will elaborate on these changes.

Similar to previous topologies, reset takes place when ϕ_1 (and its delayed versions) switches are on. ϕ_2 connects V_{th} to the pixel and enables comparison, which is concluded after the integration period when the latch is enabled. The following steps illustrate this in detail:

1. Reset:
   (a) ϕ_1, ϕ_1', and ϕ_1'' are all on. PA1 inputs are shorted to V_{rst}, PA2 is in unity-gain feedback, and both of their offsets are stored on C_{os}. Any charge from the previous cycle that was integrated onto the integration capacitor is also discharged.
   (b) ϕ_1 switches off, injecting charge onto the integration node and adding an offset (both systematic and random). However, since ϕ_1' is still on, this offset is also stored on C_{os} and corrected for.
   (c) ϕ_1' shuts off, contributing to random offset as seen before in OOS. C_{os} now store the net offset since its right-hand side is connected to a high-impedance.
2. Track: ϕ_1'' turns off and ϕ_2 turns on, connecting V_{th} to the pixel and enabling comparison.
3. Latch: `latch` turns on and a digital output is resolved at v_o.

Finally, the uncertainty in the pixel's input-referred offset voltage due to random mismatch is

$$\sigma^2(V_{os,pix}) = \frac{1}{A_1^2}\frac{\sigma^2(\Delta Q_{sw})}{C_{os}} + \frac{1}{A_1^2(A_2+1)^2}\sigma^2(V_{os,2}) + \frac{1}{A_1^2 A_2^2}\sigma^2(V_{os,latch}) \ , \tag{2.11}$$

where A_i and $V_{os,i}$ are the gain and input-referred offset of PAi, respectively, and ΔQ_{sw} is the mismatch in charge released onto C_{os} when ϕ_1' switches off.

Integration Capacitor

As mentioned before, photons striking a-Se are converted to charge, which is then collected at the pixel electrode. There can be many sources of noise and uncertainty on this node,

including but not limited to a-Se dark current, sub-threshold leakage on FET ϕ_1, and sampled thermal noise. Due to very short integration times however, a-Se dark current and FET leakage are negligible. Thermal noise given by $Q_n = \sqrt{k_B T C_i}$ presents a fundamental limit for noise on that node and is dependent on the integration capacitance C_i, which can either be a parasitic capacitor or an explicit one (e.g., a MIMCAP). Assuming thermal noise Q_n is dominant, SNR at the input node is

$$SNR_i = \frac{Q_i^2}{k_B T C_i} \ , \tag{2.12}$$

where k_B is Boltzmann's constant, T is the absolute temperature in Kelvin, Q_i is the charge from an incident photon, and C_i is the total input capacitance. Ideally, C_i should be minimized. Therefore, we do not use an explicit capacitor and C_i is a combination of parasitic capacitances from of FET switch terminals, the PA input, and the pixel input electrode. This amounts to 8-12 fF depending on the PA sizing according simulations on a layout with extracted parasitics (also known as an extracted view).

2.3.1 Pre-Amplifier Stages Optimization

Given an integration capacitance $C_i \approx 10\,\text{fF}$, temporal noise due to sampled thermal noise Q_n alone is $0.6\,\text{mV}_{\text{rms}}$. Since this sets a lower limit for uncertainty, we aim to achieve a mismatch specification $V_{os,pix}$ lower than this in order for the pixel to be noise-limited. The approach is as follows:

1. Latch random offset $V_{os,latch}$ is inhibited by the product of PA gains $A_1 A_2$. With a typical latch mismatch of $17\,\text{mV}_{\text{rms}}$, $A_1 A_2 > 60\,\text{V/V}$. This is also high enough to inhibit mismatch due to the 2nd stage.

2. Mismatch in charge released when ϕ_1' turns off ΔQ_{sw} is inhibited by $A_1 C_{os}$. However, C_{os} is set to the minimum size possible (20 fF) to meet area constraints. Therefore $A_1 > 4.5\,\text{V/V}$.

Note that these conditions constrain each mismatch contributor on its own (i.e., each term in equation 2.11), but in reality these sources will add in quadrature assuming they are uncorrelated. Therefore, total mismatch would be worse, and these conditions need to be more stringent. Also, this analysis assumes that the first stage operates within its linear region; a condition that is best met by limiting its gain $A_1 < 10$ V/V [28]. This

becomes more challenging especially with clock feedthrough from the reset phase causing the PA1's output to swing away from its nominal mid-level, increasing the likelihood that it saturates. We conclude by choosing $W_{fac,1} = 4$ and $W_{fac,2} = 7$. Gain can still be tuned dynamically by adjusting current biases (and hence, device operating points as well).

2.3.2 Simulations

The pixel testbench is similar to those of the IOS and OOS. A simplified a-Se model is used to input photocurrent onto the pixel, whereby a photon results in square pulse of current I_i. The length of the pulse is set to 3 µs, and its height is such that $E_{ph}/W_{\pm}$ charge is deposited onto the pixel electrode. A more sophisticated model could be used that includes dark current and parasitic capacitance, but these effects were negligible. An improved model would incorporate other characteristics of a photon's response, namely the fast rise-time (hole response) and longer fall-time (electron response) [12]. Note that the capacitor at the input node is only used when simulating the schematic view, and is meant to model parasitic capacitance mainly due to the large top electrode.

Pixel input waveforms are shown in Figure 2.11. All control inputs have a period T_{pix}, set to 10 µs in this simulation, which determines the pixel's count rate. A portion of this time t_{dead} is used to discharge the input node and renders the pixel insensitive to incoming charge. The remainder of time t_{int} is the effective integration time, and accounts for 9.4 µs in this simulation. Note that the input current I_i has double the period to simulate the pixel with and without photon input to quantify PD and ER, respectively.

Referring back to Figure 2.10a, $v_{oi} = v_{oi}^{+} - v_{oi}^{-}$ is the output voltage of PAi. A_i is defined as $\frac{dv_{oi}}{dv_{ii}}$. If the pixel output v_o is high for a cycle with photon input, it is considered a true positive ($TP = 1$), otherwise $TP = 0$. Similarly, if the pixel v_o is low for a cycle without photon input, it is a false positive ($FP = 0$), otherwise $FP = 1$. These results are highly dependent on threshold V_{th} chosen, which will be swept in later simulations. Figure 2.12 shows intermediate pixel waveforms as well as the final output for the simulation of a schematic and extracted view. Note that the absolute threshold V_{th} needs to be shifted to compensate for capacitive coupling effects, but since these are deterministic, they should not affect its spread (i.e., mismatch). A few signals from Figure 2.11 are also shown for reference.

Mismatch is now defined in terms of the input charge required to trip the pixel. This can also be translated to mismatch in terms of photon energy by simply dividing by the conversion gain $W_{\pm}$. We use two simulation setups to quantify mismatch, both utilizing Monte Carlo simulations:

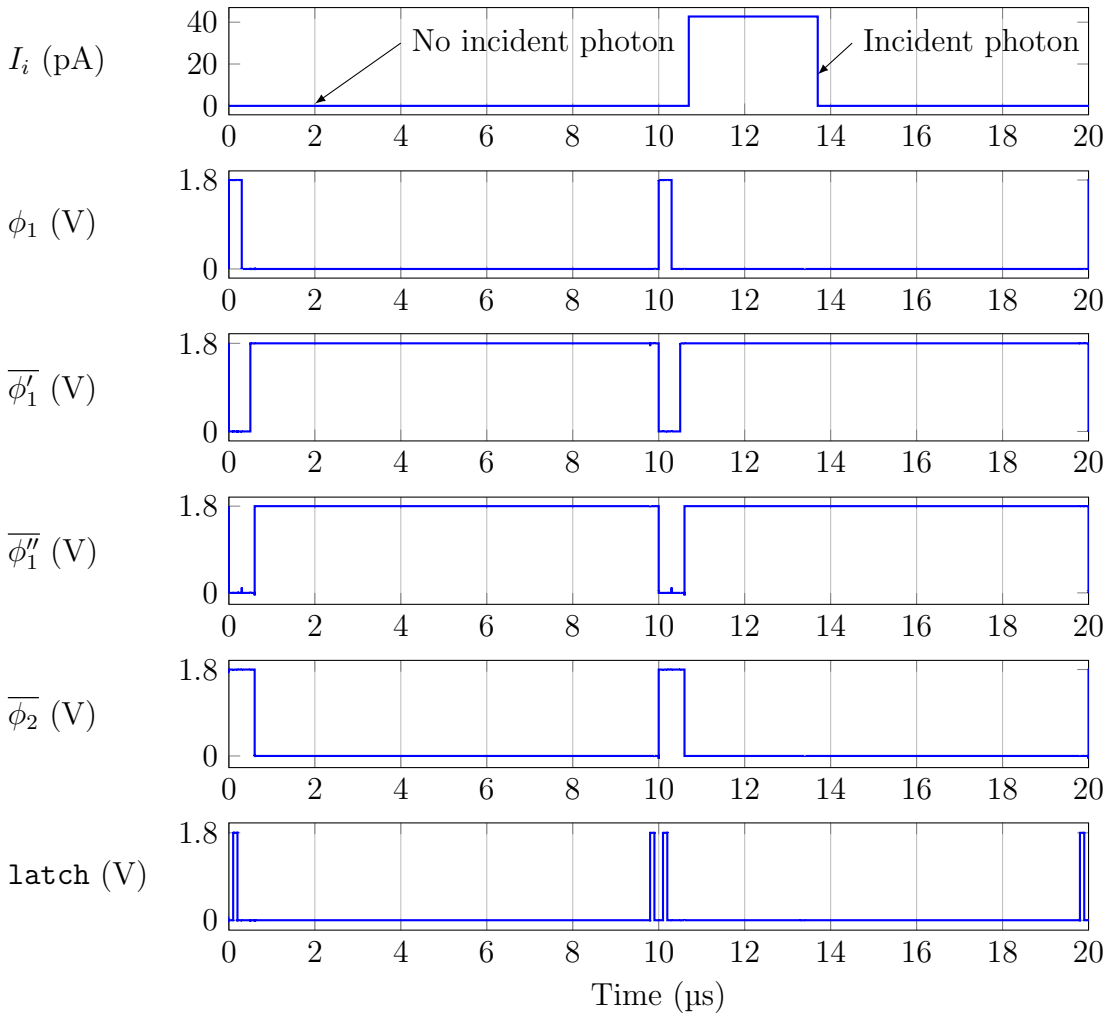


Figure 2.11: Pixel simulation input waveforms showing two 10 µs integration cycles, with and without a photon input respectively. Inverted control signals correspond to PMOS switches.

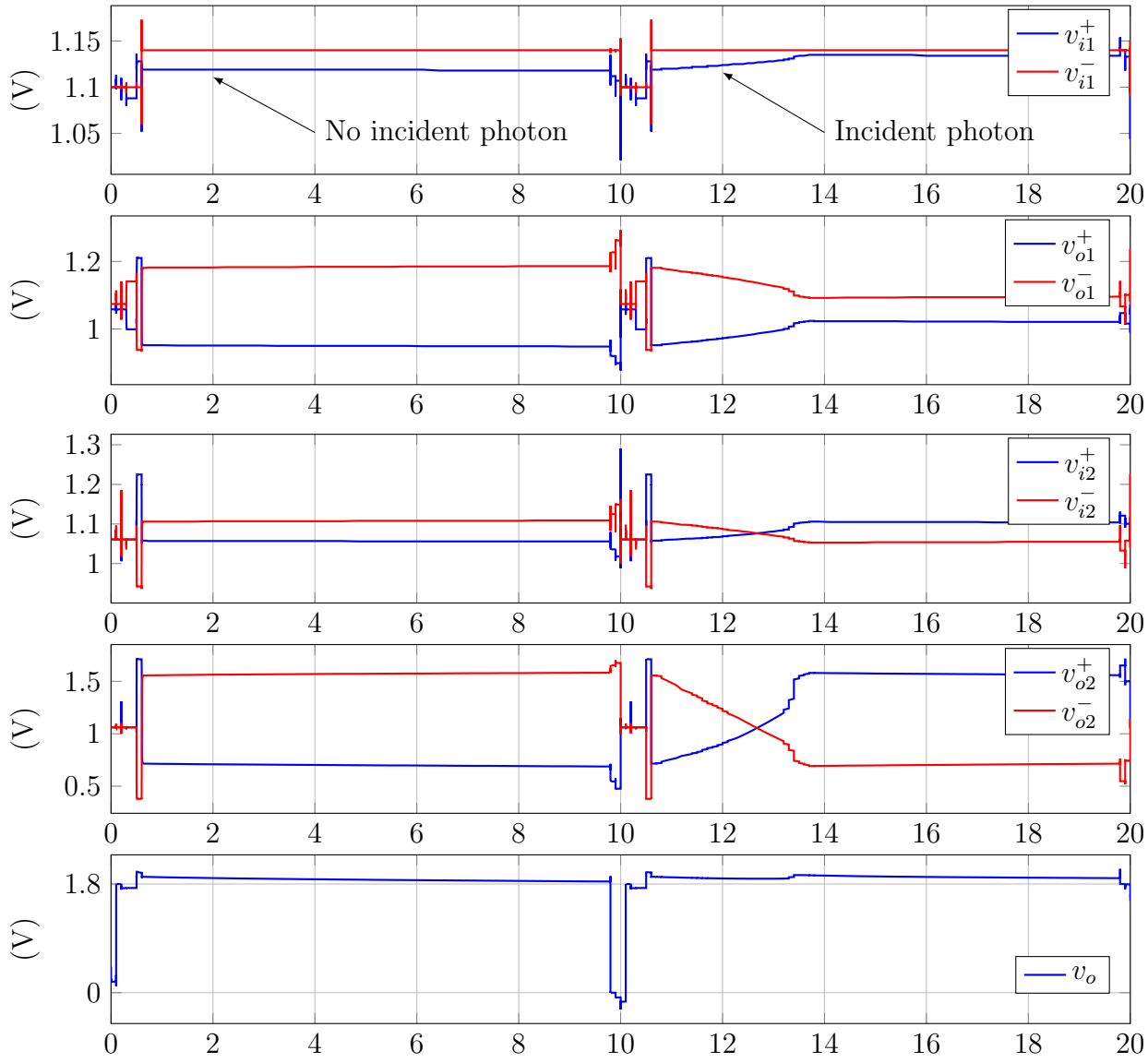


Figure 2.12: Pixel simulation intermediate and output waveforms for a parasitic extracted netlist showing two 10 µs integration cycles, with and without a photon input. Refer to Figure 2.10a.

View	Target	Schematic	Extracted
C_{eff} (fF)	–	7.99	8.00
A_1 (V/V)	> 4.5	10.7	11.8
A_2 (V/V)	–	17.9	16.5
A_{12} (V/V)	> 60	169.3	104.4
v_n ($\mathrm{mV_{rms}}$)	0.75	0.72*	0.72*
$\sigma(V_{os})$ ($\mathrm{mV_{rms}}$)	0.75	0.08	0.03
$\sigma(E_{th})$ (keV)	3.3	1.8	1.8

Table 2.3: Results of Monte Carlo mismatch simulations. C_{eff} and gains shown are average values. v_n calculated analytically assuming only thermal noise latched onto C_{eff}.

1. Define $Q_{th} = \int_{t_0}^{t_{cross2}} i_i dt$, where t_0 is the beginning of an integration and t_{cross2} is the time point when v_{o2} crosses 0. This does *not* include latch offset, but that is assumed to be a minor contributor. It is more convenient however, since no sweep of V_{th} is necessary. Cadence reports $\sigma(Q_{th})$ directly. Other useful results are the effective input capacitance C_{eff}, A_1, A_2, and the total PA gain A_{12}. A_{12} is less than $A_1 A_2$ mainly due to a parasitic capacitive division at the 2nd stage's input. These results are summarized in Table 2.3 for both schematic and extracted views.

2. Sweep V_{th} for each Monte Carlo set and observe PD and ER given by $Pr(TP)$ and $Pr(FP)$, respectively. The result is a CDF which can be fitted to a Gaussian to estimate $\sigma(E_{th})$, as shown in Figure 2.13. ER was 0 throughout (not shown) since the number of runs was not enough to show error rates below 0.25%. The resulting uncertainty in photon energy threshold $\sigma(E_{th}) \approx 0.4\,\mathrm{keV}$ and analogously, $\sigma(V_{th}) \approx 0.15\,\mathrm{mV}$.

2.3.3 Pixel Layout

Figure 2.14 shows the pixel layout with and without layers M5-M6 (mainly for MIMCAPs and integration electrode). Careful attention was paid to make the design symmetrical near critical devices (especially differential-pairs) to minimize mismatch effects while still keeping it compact.

Digital inputs enter the pixel horizontally to allow for row-wise operation, while the pixel output is column-wise (more on this in later sections). Otherwise, biases can enter the pixel in either direction since they are distributed to all pixels. Power rails can be

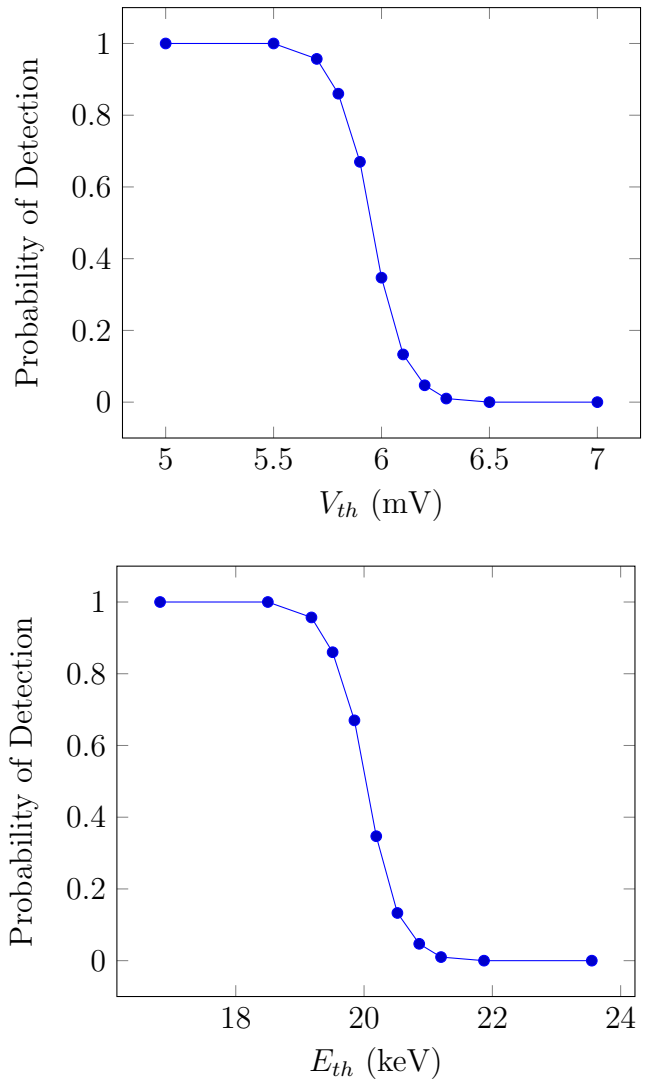
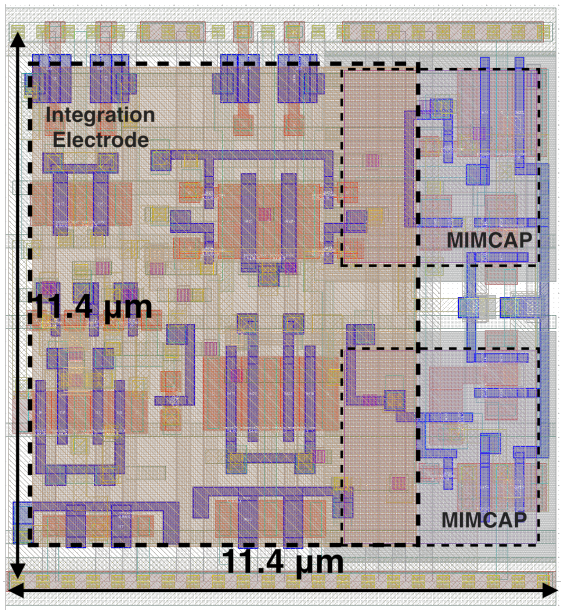
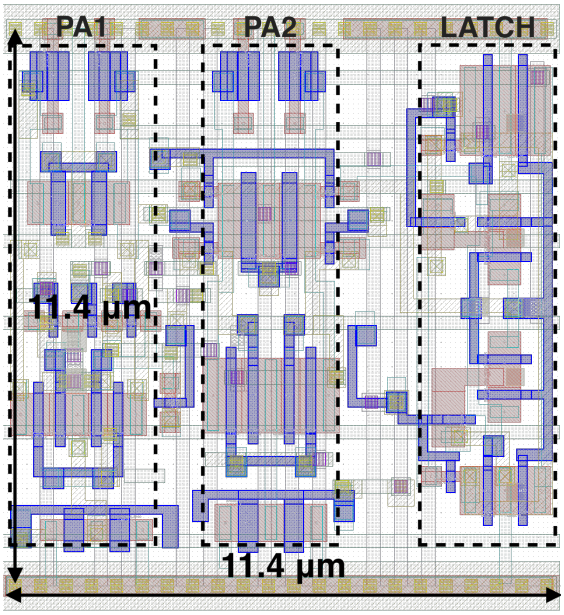


Figure 2.13: Probability of output with photon input (PD) of energy $E_{ph} = 20\,\text{keV}$ as threshold V_{th} (and E_{th}) increases. ER is 0 (not shown) for range of threshold sweep due to small sample size (400 Monte Carlo runs per point).



(a) Pixel layout showing integration electrode (in orange, left) and MIMCAPs (in gray, right).



(b) Pixel layout showing only lower metal layers and devices.

Figure 2.14: Pixel layout.

seen along the edges of the pixel. They are multi-layered and made wide enough to meet electromigration rules as specified by the technology, assuming each column of pixels will share the same power rails. Lastly, note that columns will be mirrored to allow neighboring pixels to share power rails.

2.4 Test Pixels

In order to gain better insight into the pixel operation and dc biasing conditions in the fabricated imager, test pixels were designed to include probes at the output of each PA as well as the latch. Since the pixel inputs V_{rst} and V_{th} are also provided off-chip, this gives comprehensive access to the critical nodes within the pixel.

Another variation of test pixels was also designed to allow for coupling of a known amount of charge onto the pixel's input node. This would enable us to characterize the sensor's performance before operating it as an image sensor (i.e., with the selenium layer and an X-ray source and apparatus). It would also allow us to calibrate the pixel thresholds with a gamma source (with precise photon energies) and quantify the energy resolution of our sensor. The coupling of a known amount of charge onto the pixel can be done by adding a series capacitor to the input node as seen in Figure 2.15. Some test pixels have exposed input electrodes to allow probing of internal nodes while operating the imager with a a-Se layer. If a voltage step is applied at the test input V_t, the charge deposited onto the input node is

$$Q_t = \Delta v_t C_t \ , \tag{2.13}$$

where Q_t is the test charge, Δv_t is the voltage step at v_t, and C_t is the test input capacitance. The consequential voltage change at the pixel input is

$$\Delta v_i = \Delta v_t \frac{C_t}{C_i} \ . \tag{2.14}$$

C_t should be small enough to allow for fine amounts of charge to be coupled into the pixel. Since the minimum MIMCAP allowable is 20 fF, we connect 4 MIMCAPs in series to achieve an approximate effective capacitance $C_t = 5$ fF. With this value, the voltage-to-charge conversion is 31 e^-/mV. Adding capacitors significantly increases the pixel area, which limits test pixels to the edges of the array to avoid irregularities. If the test pixel is

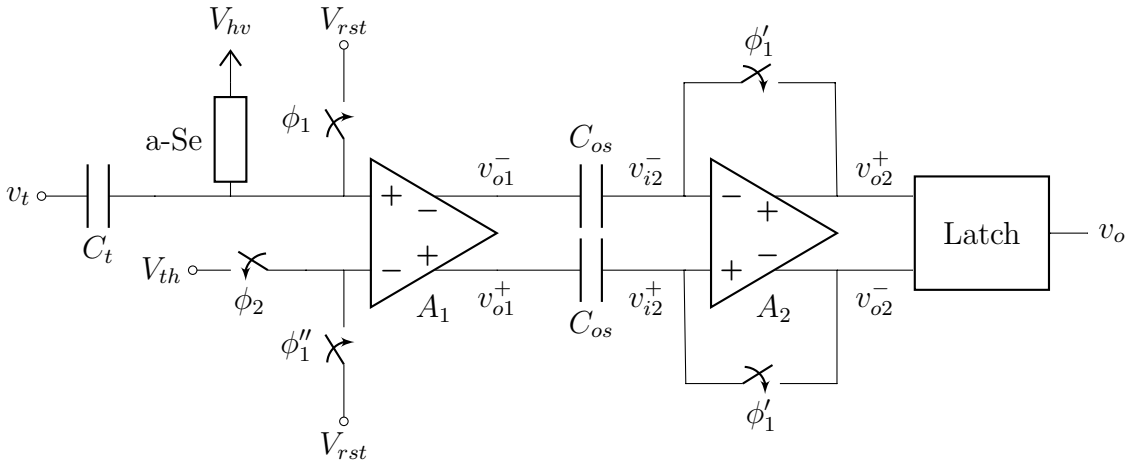


Figure 2.15: Test pixel architecture showing input charge-coupling capacitor to v_t.

to be operated with selenium, v_t must be left floating in order not to increase the effective input capacitance (C_t appear be in parallel with C_i if v_t is grounded).

2.4.1 Test Pixel Layout

Test pixels are mostly replicas of regular pixels except for the following differences:

1. Test input capacitors are instantiated beside the pixel.
2. PAs are sized slightly smaller to allow for probe switches.
3. Probe lines exit the pixel row-wise.

Figure 2.16 shows the test pixel layout.

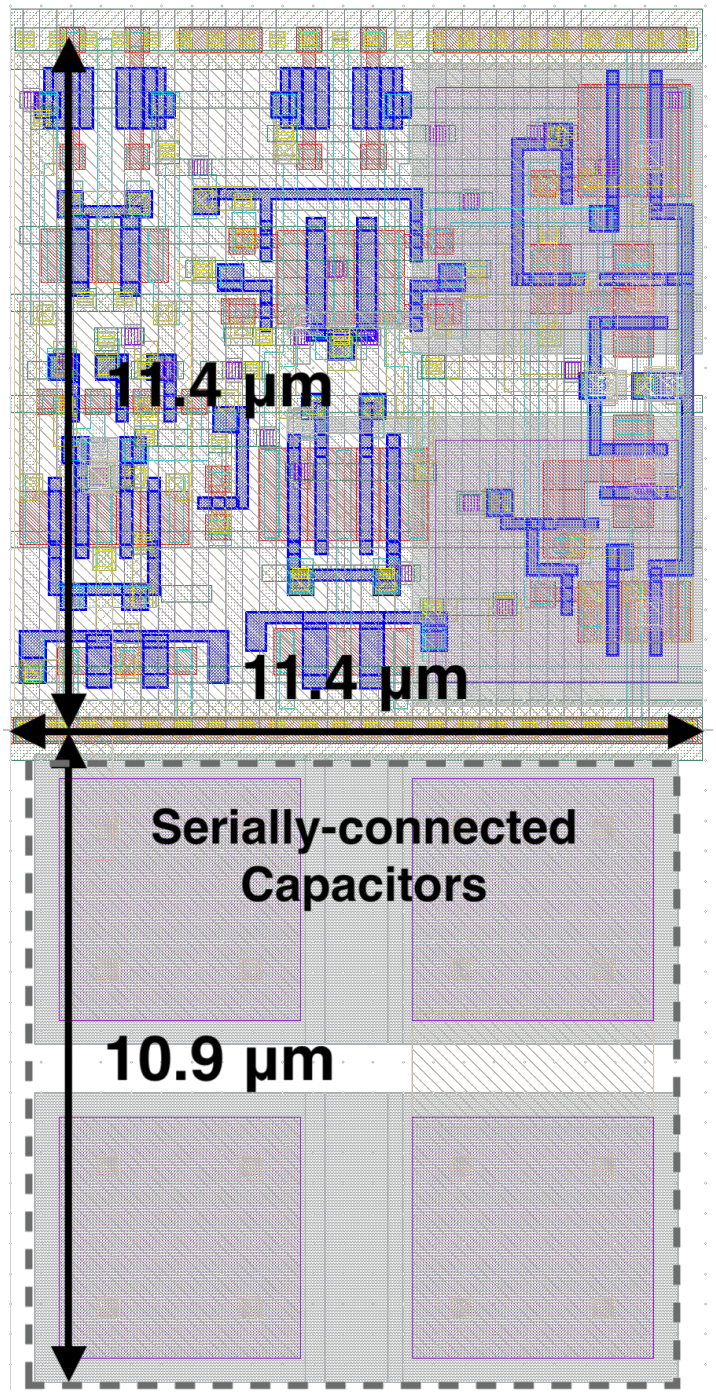


Figure 2.16: Test pixel layout showing test input MIMCAPs.

Chapter 3

Imager Architecture, Physical Design and Verification

This chapter describes the overall design of our PCI beyond the pixel itself. It begins with the split of power and clock domains in order to minimize interference on pixels and enable fast off-chip read-out. Afterwards, blocks for pixel control signals and bias generation, counters, and off-chip interfacing are designed with special attention to the trade-offs between array size and ease of data read-out. Finally, verification results are done by utilizing block-level simulations, miniaturized arrays, and simplified analyses to ensure the chip functions as expected.

3.1 Chip Architecture

The overall chip consists of two mostly identical arrays (Array 1 and Array 2), where each array includes pixels, counters, scan chains, and output shift registers. Both arrays include test pixels which can be probed for internal nodes, but only the Array 1's test pixels include coupling capacitors for test inputs. Also, a subset of Array 2's pixels utilize a smaller top electrode. Figure 3.1 shows the functional block diagram of a single array. Grey blocks are shared between both arrays.

The overall system works as follows. Pixels and counters are operated in a row-wise fashion, whereby each pixel has a corresponding counter. Pixel columns share an output bus that crosses down to the counter array as an input to increment counters. However, only one pixel and its corresponding counter are enabled at a time. This operation is

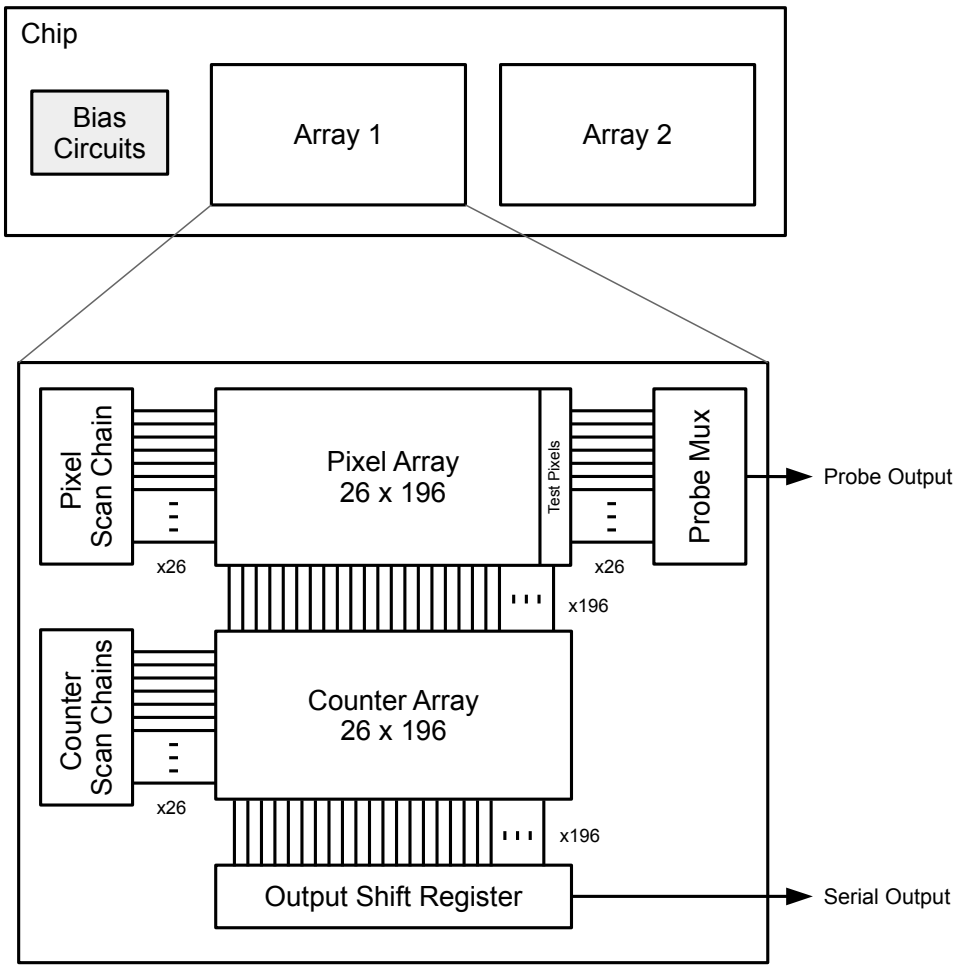


Figure 3.1: Chip block diagram showing two arrays with a closer look at the blocks and connectivity within an array.

synchronized by the Pixel Scan Chain and Counter Scan Chains. In addition, scan chains provide other control signals (e.g. reset) to pixels and counters. Once counters within a row reach their maximum capacity, they are output in parallel to the Output Shift Register and reset accordingly. The Output Shift Register then outputs counter data serially off-chip through an input/output (I/O) pad. Test pixel probes will be explained in a later section.

3.1.1 Power Domains

The chip is split into analog and digital power domains (both typically 1.8V). Pixel arrays and biasing circuits are provided with analog power and ground rails (AVDD and AVSS, respectively) while the remainder of blocks operate on digital rails (DVDD and DVSS). This is done to minimize coupling from noisy digital blocks to sensitive analog blocks. Since PMOS devices exist within N-wells, their bodies are easily biased with the correct domain by biasing the N-well through a metal contact. However, NMOS devices interface directly with the substrate, and ground isolation is achieved using a deep N-well beneath all analog circuitry as recommended by the process manuals [31]. A separate 3.3 V power supply (DVDD33) is used for I/O pads in order to allow for flexibility in interfacing with external circuits like a field-programmable gate array (FPGA).

3.1.2 Clock Domains

Digital circuits are split into two synchronous clock domains (blocks are shown in Figure 3.1):

1. Pixel Clock Domain (`clk_pix`): includes Pixel Array, Pixel Scan Chain and Probe Mux.
2. Counter Clock Domain (`clk_cntr`): includes Counter Array, Counter Scan Chains, and Output Shift Register.

The reason for this split is to allow for higher serial data read-out speeds from counters while still having relaxed specifications on pixel clock speeds. Except for the purposes of debugging, the only digital outputs are serial counter read-out lines. However, a single clock can be used for both `clk_pix` and `clk_cntr` if photon count rates are low enough.

3.1.3 Counters

Data Compression

While pixel outputs could simply be buffered and sent off-chip directly since they are digitally encoded, this would require impractically high off-chip data bitrates. The off-chip data bitrate on a single lane (i.e., a physical pad or trace) would be

$$\mathrm{BR}_{\mathrm{lane}} = \mathrm{BR}_{\mathrm{chip}} = \mathrm{BR}_{\mathrm{array}} = \frac{N_{rows} \cdot N_{cols}}{T_{pix}} \ , \tag{3.1}$$

where T_{pix} is the pixel reset period (reciprocal of count rate), and N_{rows} and N_{cols} are the number of array rows and columns respectively. Counters effectively compress counting information to allow for lower off-chip bitrates. The off-chip bitrate using counters is reduced to

$$\mathrm{BR}_{\mathrm{lane}} = \mathrm{BR}_{\mathrm{chip}} = \mathrm{BR}_{\mathrm{array}} \cdot \frac{N_{bits}}{n_{en}} = \frac{N_{rows} \cdot N_{cols}}{T_{pix}} \cdot \frac{N_{bits}}{n_{en}} \ , \tag{3.2}$$

where n_{en} is the number of times the counter is enabled to read from a pixel (i.e., `inc_en` is asserted) before the former is read and accordingly reset. n_{en} is nominally the maximum count a counter can hold, which is limited to $2^N_{bits} - 1$, and the compression ratio is $N_{bits}/(2^{N_{bits}} - 1)$. Counters can also be operated such that n_{en} is greater for better compression. Finally, off-chip serial data can be split over parallel lanes to provide even lower data rates:

$$\mathrm{BR}_{\mathrm{lane}} = \frac{\mathrm{BR}_{\mathrm{chip}}}{N_{lanes}} = \frac{N_{rows} \cdot N_{cols}}{T_{pix}} \cdot \frac{N_{bits}}{n_{en}} \cdot \frac{1}{N_{lanes}} \ , \tag{3.3}$$

where N_{lanes} is the number of lanes used and is mainly limited by the number of I/O pads available.

Implementation

We use standard 5-bit binary counters ($N_{bits} = 5$), with the exception that the most-significant bit (MSB) remains high if an overflow occurs. The reason behind the overflow bit as well as the optimization of N_{bits} are in upcoming sections, and scaling this design is easy. Figure 3.2 shows the counter schematic. The main features here are a masked increment input `inc` and parallel gated outputs.

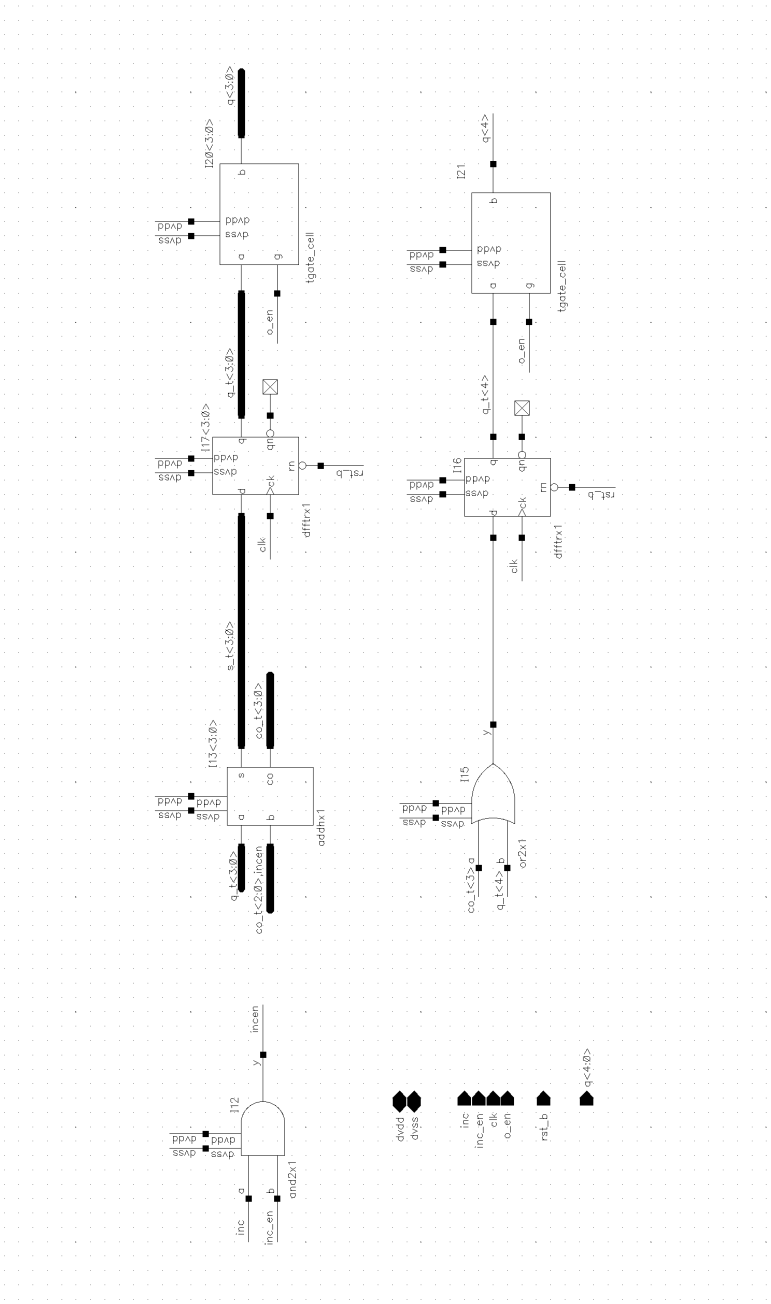


Figure 3.2: 5-bit Binary Counter Schematic.

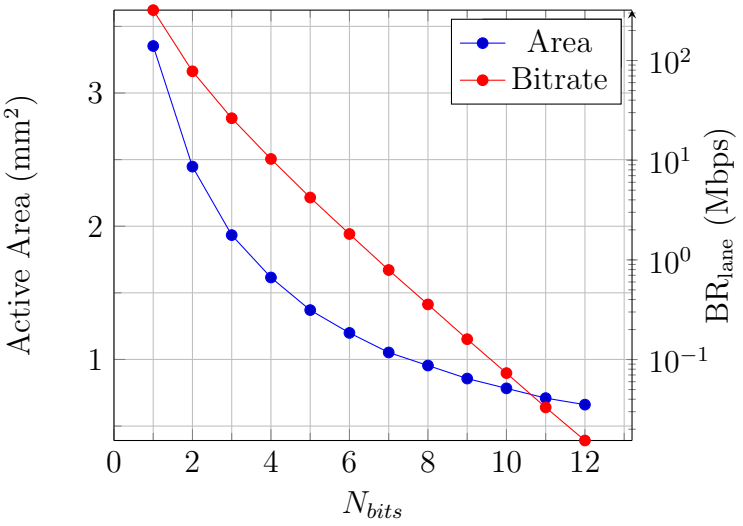


Figure 3.3: Optimization of counter N_{bits} showing area and lane bitrate trade-off.

Area Trade-off and Optimization

Since the chip size is limited and we would like to maximize the active pixel area, counters should occupy as little area as possible while still meeting count rate specifications. Counter area scales proportionally to N_{bits}, since each extra bit requires a flip-flop (FF), half adder, and output transfer gate. Given a fixed area for pixels and counters, pixel pitch, digital cell areas, and target count rate $1/T_{pix}$, the active area (or number of pixels/counters) and lane bitrate can be estimated for increasing N_{bits}.

Figure 3.3 shows the trade-off between active area and lane bitrate $\mathrm{BR}_{\mathrm{lane}}$ for $T_{pix} = 10\,\mu\mathrm{s}$ and assuming 8 data lanes. Bitrate would scale linearly for shorter T_{pix}, and so a reasonable margin is used to allow easy digital read-out. N_{bits} between 4-6 seems reasonable, so 5 is chosen.

Operation Modes

Counters can be operated in two modes thanks to the overflow MSB:

1. Deterministic, whereby $n_{en} \leq 2^{N_{bits}} - 1 = 31$. The counter is effectively a standard 5-bit binary counter.

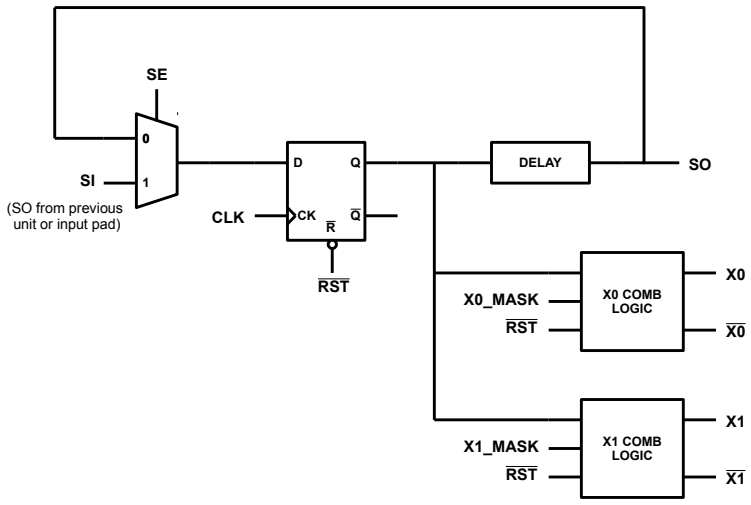


Figure 3.4: Generic scan chain unit showing FF and two signals.

2. Indeterministic, whereby $n_{en} > 31$. In this case, overflow is possible and hence the MSB acts as an overflow bit. The counter is now effectively 4 bits wide only, with a maximum count of 15. This mode should be used when the photon flux per pixel is much lower than the count rate, and allows for slower read-outs are needed.

3.1.4 Scan Chains

Scan chains are a series of FFs and logic designed to provide arrays with necessary control signals. The FFs are loaded serially, with typically only one FF (corresponding to a single row) being enabled at a time. Various control signals are then generated by masking the FF output. This allows for a great deal of flexibility in the timing of control signals, which is useful for testing, characterization, and calibration purposes. Figure 3.4 shows a generic scan chain unit to illustrate this concept. Masks can either set or reset a signal (its default value would be 0 or 1, respectively). Similarly, signals are set to predetermined values if reset is asserted on the chip level. A scan chain is simply composed of many units linked together. A delay block is added between successive FFs to avoid hold-time violations.

Scan chain outputs must drive very different capacitive loads, depending mainly on how many devices they drive within an array element (e.g. pixel). To estimate these loads, the input capacitance of every input of a single element's extracted view was calculated from

Signal	Net	Mask	Default value	Masked value	Reset value
ϕ_1	rst_p0	rst_p0_mask	0	1	1
$\overline{\phi_1}$	rst_p0_b	rst_p0_b_mask	1	0	0
$\overline{\phi_1'}$	rst_p1_b	rst_p1_mask	1	0	0
$\overline{\phi_1''}$	rst_p2_b	rst_p2_mask	1	0	0
$\overline{\phi_2}$	comp_b	comp_mask_b	0	1	1
latch	latch	latch_mask	0	1	0
$\overline{\text{latch}}$	latch_b	latch_mask	1	0	0

Table 3.1: Outputs of Pixel Scan Chain.

simulation, then scaled by the number of elements. This includes all parasitic capacitances since elements are laid out with row and column wires such that they can be abutted, and hence should scale proportionally.

Three scan chains operate coherently to control pixels and counters:

1. Pixel Scan Chain: resets pixels and enables latches at end of comparison.
2. Counter-Enable Scan Chain: synchronizes with Pixel Scan Chain to enable the counter input when the pixel output (i.e., latch) is enabled.
3. Counter-Read Scan Chain: synchronizes with Counter-Enable Scan Chain for counters to accumulate counts and periodically transfer data to Output Shift Register.

Pixel Scan Chain

Table 3.1 lists the outputs of the Pixel Scan Chain and their masks, default values (when not masked), and reset values. Note that some signals, such as ϕ_1' and ϕ_2, are used in their complemented form. During chip-level reset, signals are set such that the PAs are in a known state and the latch is off. The net name in Cadence is also included for reference during verification. Lastly, note that ϕ_1 and $\overline{\phi_1}$ are generated from different masks to allow for more flexible control of NMOS and PMOS switches at the integration node.

Signal	Net	Mask	Default value	Masked value	Reset value
inc_en	inc_en	inc_en_mask	0	1	0

Table 3.2: Outputs of Counter-Enable Scan Chain.

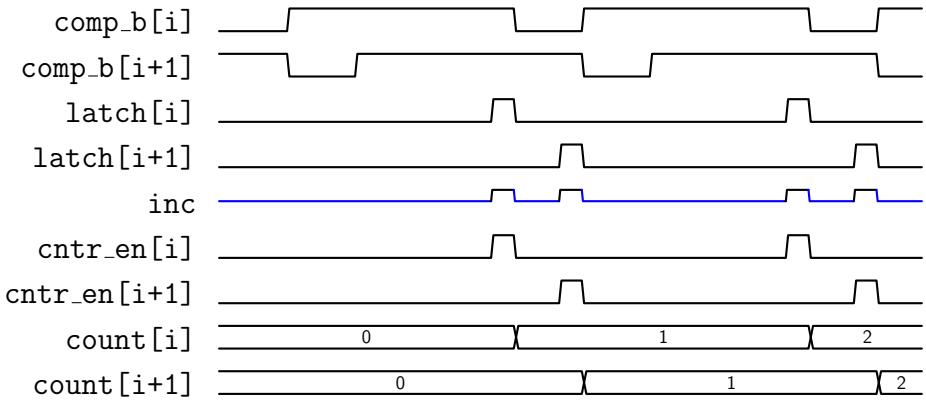


Figure 3.5: Synchronization of Pixel Scan Chain and Counter-Read Scan Chain, showing how pixels from different rows only increment their respective counters.

Counter-Enable Scan Chain

Table 3.2 shows the Counter-Enable Scan Chain output and is analogous to Table 3.1. `inc_en` must be coincident with a pixel row's `latch`, but not vice-versa. For example, if counters are operating at 2x pixel clock speed, `inc_en` would only be enabled for a single cycle on `clk_cntr` (and half a cycle on `clk_pix`) to prevent counting the same photon twice.

Synchronization between the Pixel Scan Chain and Counter-Read Scan Chain is critical since pixels drive a common output bus. Figure 3.5 shows how multiple pixels within a column increment their respective counters. It is assumed that photons strike in integration period.

Counter-Read Scan Chain

Table 3.3 shows the Counter-Read Scan Chain output and is analogous to table 3.1. This chain works slower than the Counter-Enable Scan Chain, since a `inc_en` can be asserted at least $2^{N_{bits}} - 1$ times before it overflows. Counters can be read even slower if photon flux

Signal	Net	Mask	Default value	Masked value	Reset value
cntr_rd	cntr_rd	cntr_rd_mask	0	1	0
$\overline{\texttt{cntr\_rst}}$	cntrrst_b	cntrrst_mask	1	0	0

Table 3.3: Outputs of Counter-Read Scan Chain.

on a pixel is expected to be much lower than the pixel reset period. It is easier, although perhaps not necessary, to make the counter read-out frequency an integer multiple of the counter enable frequency.

3.1.5 Output Shift Register

The Output Shift Register consists of N_{cols} elements of N_{bits} FFs that are loaded in parallel from a row of counters. This operation is tightly coupled with the Counter-Read Scan Chain, whereby counter outputs are enabled and drive column buses that connect to masked Output Shift Register inputs. FFs within each element are linked such that they scan out in little-endian format (i.e., least-significant bit (LSB) first). Figure 3.6 shows the schematic of a single element in the chain.

Elements in the Output Shift Register are linked such that they scan out in big-endian format (i.e., last column first). To reduce read-out times, four equally spaced taps are placed along the chain to output four lanes in parallel, hence reducing the lane bitrate by a factor of four. These are at the outputs of elements 48, 97, 146, and 195 (the last one). Figure 3.7 shows a sample output waveform. If `se` were to be held longer than shown, counter data from each tap will bleed into the next one and `si` would appear at the output. This gives the user flexibility in using as many data lanes as needed. It is up to the user to determine if data is valid at the output however, should `se` be asserted longer than $N_{bits}N_{cols}/N_{lanes}$ (nominally 245) clock cycles.

3.1.6 Bias Circuits

Each pixel PA requires biases for the current mirrors, cascode devices and pixel inputs (V_{rst} & v_{th}). Each half array has different pixel input but the two arrays share device biases. Cascode gates and pixel inputs are connected to pads directly for off-chip biasing. On the other hand, the current sinks and load devices are biased by simple current mirrors that similarly connected to pads for off-chip biasing. Mirrors are instantiated with a ratio

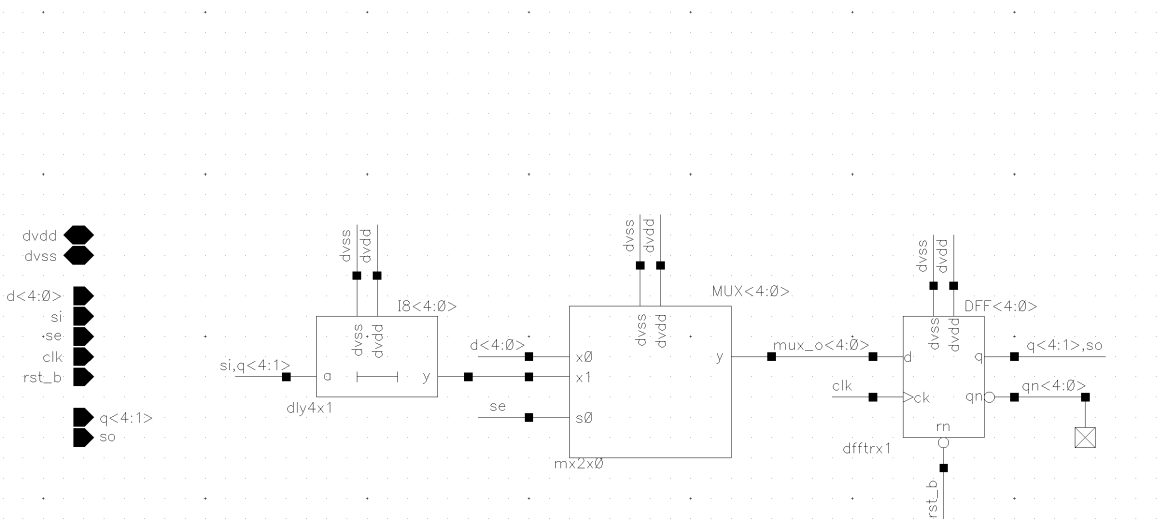


Figure 3.6: 5-bit unit element in Output Shift Register.

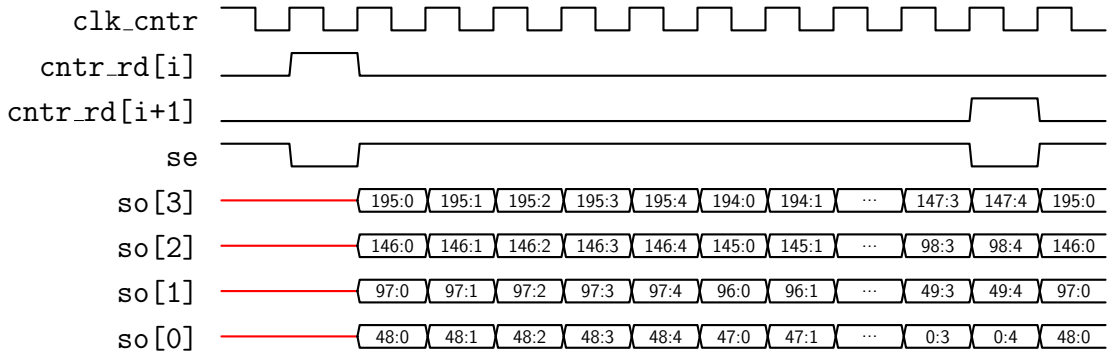


Figure 3.7: Output Shift Register sample waveforms

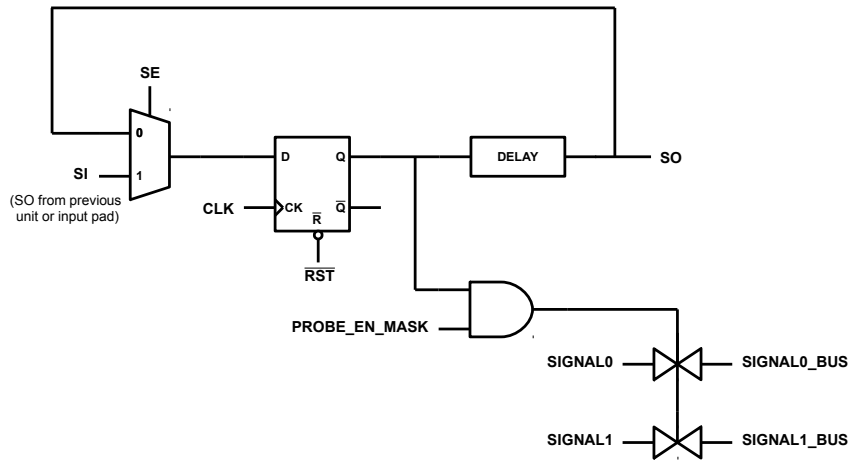


Figure 3.8: Unit of probe multiplexer scan chain showing two multiplexed signals.

of 10:1 to reduce mismatch effects, while maintaining matching with pixels as much as possible by using the same unit transistor layouts.

MIMCAPs are instantiated at bias inputs as well to attenuate high-frequency noise and interference. Maximum size MIMCAPs (30 x 30 µm^2) units of 952 fF are connected in parallel. Current mirror biases each have a total capacitance of 40.9 pF, while $V_{rst,A}$, $V_{rst,B}$, $V_{th,A}$ and $V_{th,B}$ (separate biases for Array 1 and Array 2) each have a total capacitance of 34.2 pF.

3.1.7 Probing circuits

Test pixel probes are multiplexed by means of a scan chain. Similar to other scan chains, the backbone of FFs select which row is to be probed, while a global mask is used to enable or disable probing. Only one FF should be high at a time to prevent multiple drivers on the multiplexer output (or none if probing is off). Figure 3.8 shows a single unit's schematic from the chain with two sample signals.

3.1.8 I/O Pads

Custom pads were designed for analog signals, digital signals, and power buses. Each pad provides electrostatic discharge (ESD) protection by means of diodes to suitable power rails. In addition to this, ground rails of different domains are also connected to one another by means of reverse-biased diodes to ensure no large potential develops across ground domains. Pads are designed as follows:

- Analog signal: series 200 Ω resistor to reverse-biased diodes connecting to analog power rails.
- Digital input: series 200 Ω resistor to reverse-biased diodes connecting to digital power rails, followed by 3.3V to 1.8V level-shifter and buffer.
- Digital output: series 200 Ω resistor to reverse-biased diodes connecting to digital power rails, followed by 1.8V to 3.3V level-shifter and buffer.
- Analog power (AVDD): reverse-biased diodes connecting to analog ground (AVSS).
- Analog ground (AVSS): reverse-biased diodes connecting to analog power (AVDD).
- Digital I/O power (DVDD33): reverse-biased diodes connecting to digital ground (DVSS).
- Digital I/O ground (DVSS33): reverse-biased diodes connecting to digital I/O power (DVDD33).
- Digital power (DVDD): reverse-biased diodes connecting to digital ground (DVSS).
- Digital ground (DVSS): reverse-biased diodes connecting to digital power (DVDD).

3.2 Chip Verification

The following section shows how analog and digital blocks were verified and concludes with full-chip simulations. All digital cells were verified at the maximum clock frequency of 50 MHz. Simulation of smaller blocks was done in Spectre (analog). Higher level blocks were simulated in UltraSim however, since Spectre is not optimized for large designs. All blocks were verified over 6 corners: fff, ff, fs, sf, ss, and sss, at operating temperatures up to 70 °C.

3.2.1 Counters

In this testbench, inputs are buffered and outputs are loaded with capacitors in place of other counters on the bus. Capacitance of other counters is estimated by summing the capacitance of a single counter while its output is disabled from an extracted view, then multiplied by the number of rows (since this is a column bus). The capacitance of each output pin on a counter is approximately 6.5 fF.

Figure 3.9 shows simulation waveforms on an extracted counter view including parasitic capacitances. Note that counter outputs only appear on the bus when `O_EN` is asserted. The MSB also remains high in the case of overflow as intended.

3.2.2 Scan Chains

A chain of five units is used to reduce simulation times and memory usage. All inputs are buffered and each output is loaded with a capacitor equivalent to the row signal's input capacitance. Figure 3.10 shows how the chain is loaded with a bit, how that bit propagates through the chain as expected, and how outputs are masked successfully. Other scan chains were verified in the same manner.

3.2.3 Output Shift Register

Figure 3.11 shows the sequence of events to shift counter bits out serially. The parallel inputs `d<4:0>` (in place of the counter output bus) are set to a known sequence that is loaded then shifted serially to the output `so` followed by the sequence at `si`. Outputs `q<4:1>` show the intermediate state of the Output Shift Register.

3.2.4 Bias Circuits

All four current mirrors were verified in a single testbench. The current in each mirror is set by a resistor to the appropriate supply and verified in a dc analysis.

3.2.5 Sub-Array Functional Verification

A small-scale replica of the chip top level (except I/O pads) was created to allow for end-to-end simulations of the signal chain beginning in the Pixel Array and all the way until the

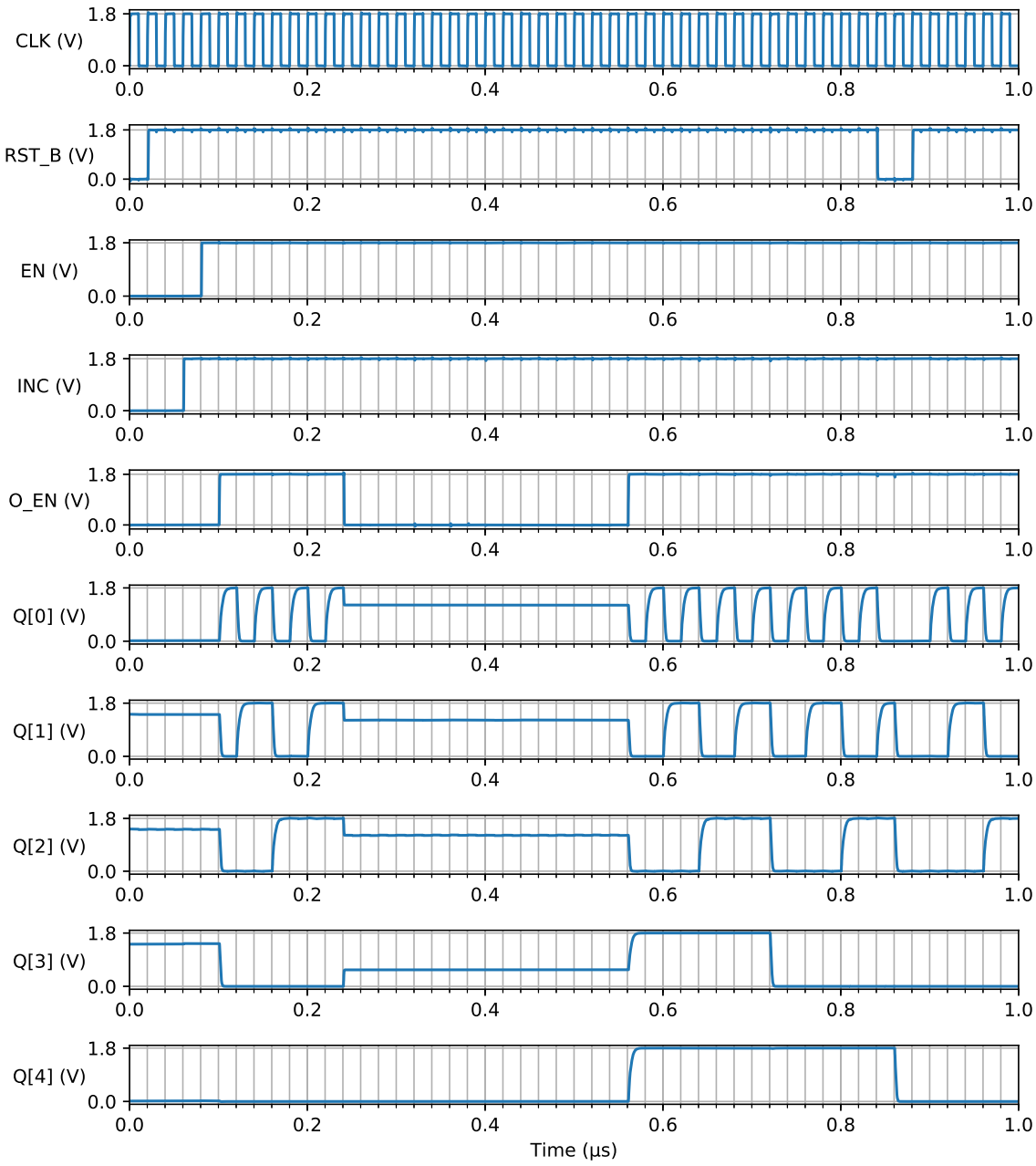
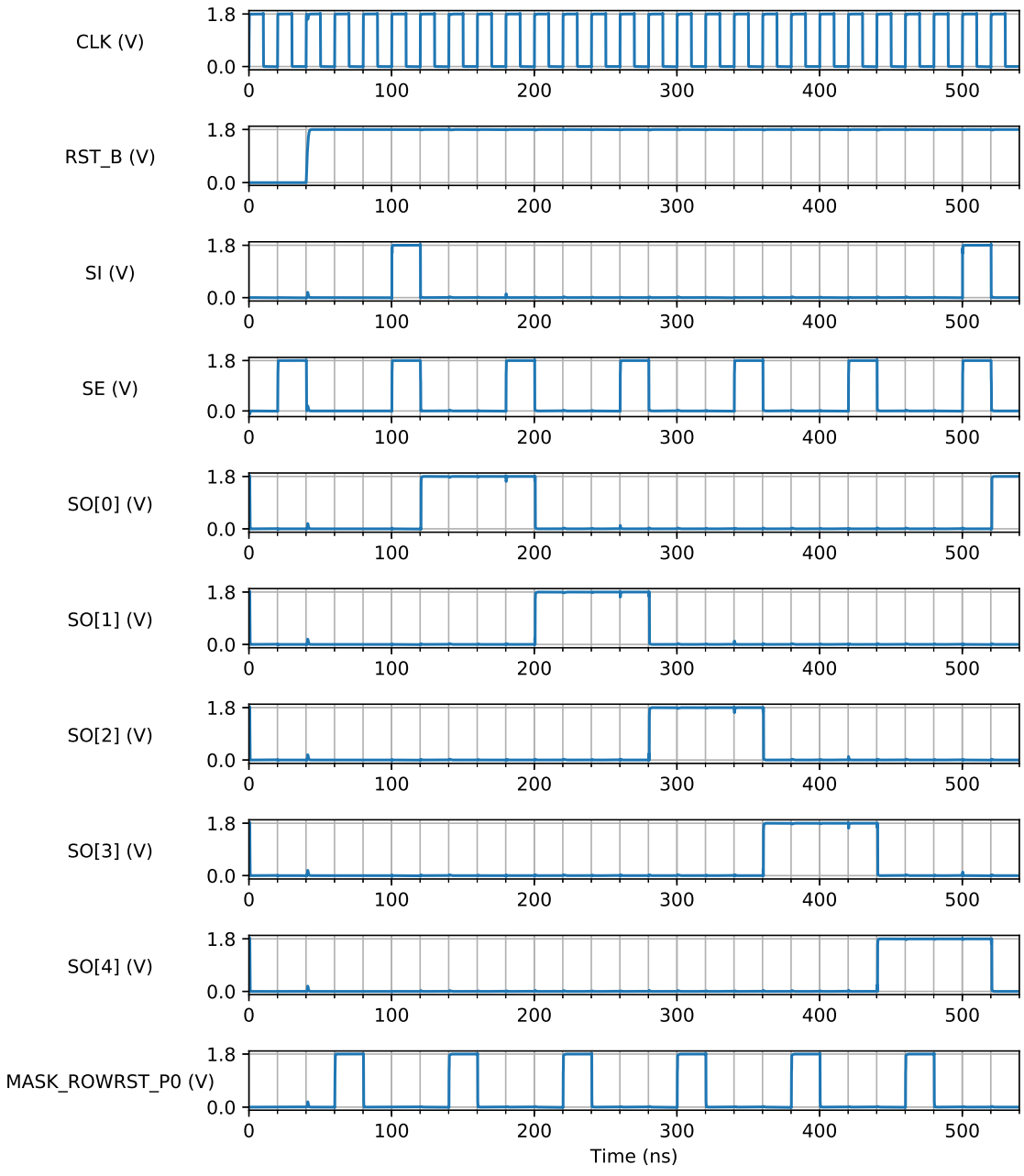
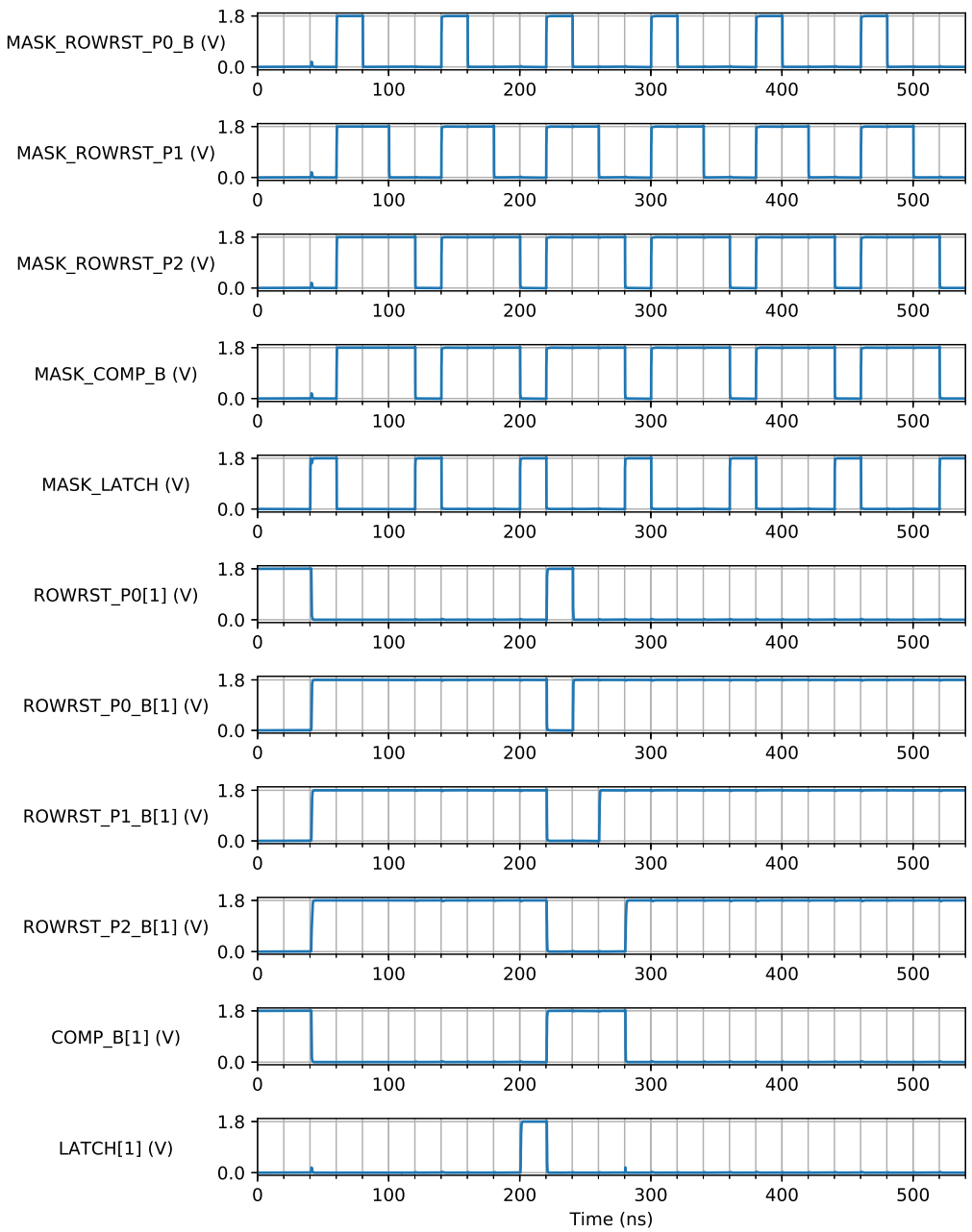


Figure 3.9: Counter testbench waveforms. Outputs `Q[4:0]` are probed on the bus (i.e., after a transmission gate) and only driven when `O_EN` = 1. Switching of transmission gates causes glitches on undriven busses (e.g., 0.24 µs to 0.56 µs). Outputs only increment when `EN` = 1. `Q[4]` (MSB) does not reset to 0 in the event of an overflow at 0.72 µs.


CLK (V)
RST_B (V)
SI (V)
SE (V)
SO[0] (V)
SO[1] (V)
SO[2] (V)
SO[3] (V)
SO[4] (V)
MASK_ROWRST_P0 (V)
1.8
0.0
0
100
200
300
400
500
Time (ns)

(a) Part 1.



(b) Part 2.

Figure 3.10: Pixel Scan Chain testbench waveforms. Bits propagate through the chain as expected and signal masks only affect the enabled row. Signal default, masked, and reset values match those in Table 3.1.

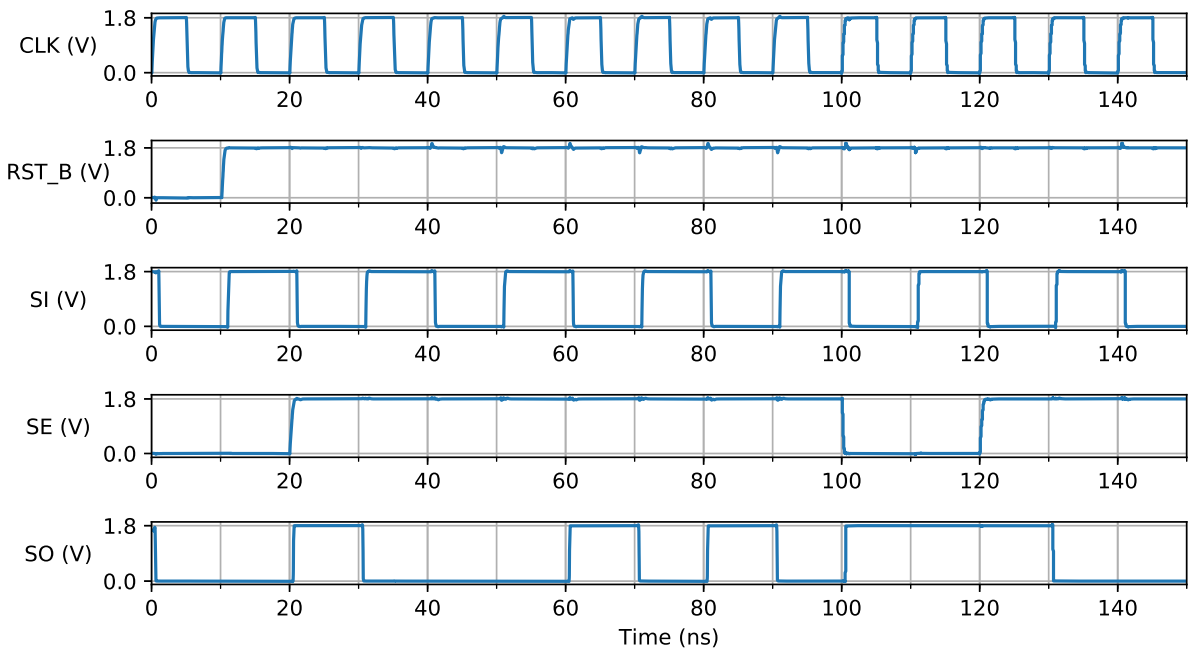
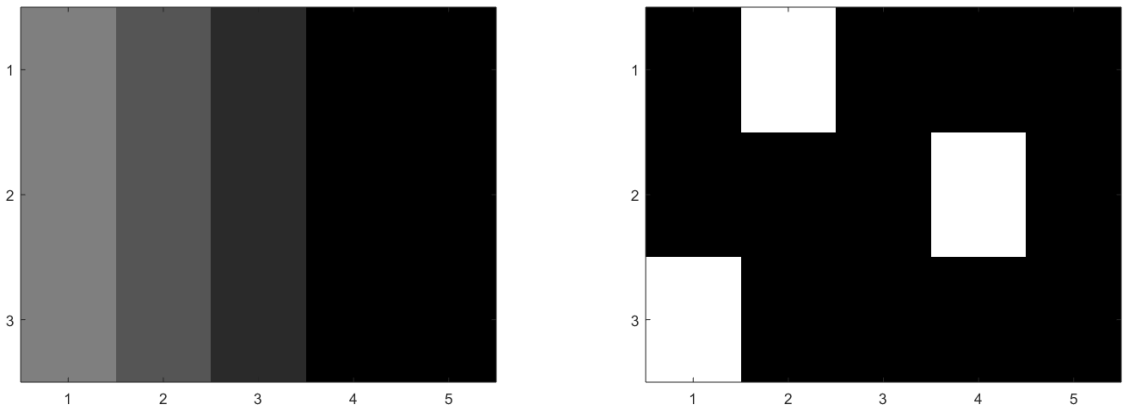


Figure 3.11: Output Shift Register unit testbench waveforms for an input `D[4:0]` = 10001. Registers are loaded while `SE` = 0 then shifted through `SO` when `SE` = 1. If `SE` = 1 after all bits are shifted, `SO` tracks `SI`.



(a) Gradient.

(b) Arbitrary bright pixels.

Figure 3.12: Output images from 3x5 top level simulation.

Output Shift Register. Vector files provide individual pixel inputs and allow for various image patterns to be generated. The Output Shift Register output is then exported to MATLAB to deserialize and parse counter data, finally producing an image. Two vector files were used, one to produce a gradient and another to produce arbitrary (but known) bright pixels, and their resulting images are shown in Figure 3.12. Both results are as expected and verify that the signal chain works.

The UltraSim engine was used for these simulations since Spectre does not handle large designs as well. All blocks were simulated in mixed-signal (ms) mode except for the pixels themselves, which ran in analog (a) mode.

Since the top level was too large to simulate on our local machine, we opted for a few simulations that would verify individual blocks within the top level with confidence that it would work in totality since the small-scale replica worked as expected. This would also include pads for a complete end-to-end verification (although pads were also verified separately). Verification was done on the following levels:

1. Digital only (transient): all analog biases were turned off (i.e., current biases open, voltage biases grounded) and digital inputs were provided such that scan chains operate as expected. Pulses arrived at scan chain outputs as expected and control signals were probed within the first and last rows of pixels to verify connectivity throughout the chain.

2. Analog only (dc): analog biases were set at nominal values and the chip was in global reset. The total analog current flowing into the chip was 753 mA. All analog biases were probed within arbitrary pixels and observed at their expected levels.

Chapter 4

Experimental Results

This chapter begins with the design of a printed circuit board (PCB) to experimentally validate the electronic performance of our PCI. We focus on sensitive blocks that significantly affect pixel performance. Later sections describe experimental results of electrical tests and reconcile results with the theory presented in Chapter 2. Since these tests are all electrical in nature, a final section relates these results back to the chip's performance as an imager.

4.1 Printed Circuit Board Design

A PCB was designed and manufactured to operate the image sensor, characterize its performance, and ultimately acquire images. This entails:

1. Biasing sensor analog voltage and current inputs.
2. Generating digital signals to operate sensor scan chains and other circuits on the imager chip.
3. De-serializing chip outputs and transferring them to a PC for further analysis.
4. Distributing power throughout the system while maintaining analog/digital isolation.

Figure 4.1 shows the PCB used to characterize the imager. It is separated into two domains: analog and digital. The analog domain contains our imager, biasing circuits

and DACs, and low-dropout regulators (LDOs) for analog power rails. The digital domain contains an FPGA that generates digital control signals and acquires serial data, followed by a Universal Serial Bus (USB) bridge to interface with a PC. It is also powered by separate LDOs. The board consists of 4 layers: two outer routing layers and two inner power/ground layers.

Experiments are set up in software by setting FPGA parameters to operate the sensor in various configurations. Frames are acquired by the PC over USB and saved in binary files, which are then imported into MATLAB for processing and characterization. This setup allows a wide range of flexibility, including timing of all control signals, clock speeds, and bias sweeps.

4.1.1 Analog and Digital Isolation

Much effort was made to separate the analog and digital domains to minimize digital noise or interference from coupling onto analog signals. Since the image sensor's counter outputs are exclusively digital, the main concern is coupling onto analog biases. Several precautions were taken:

1. Ground plane was split (physically) into two halves, each housing its respective domain. Grounds were connected at a single point on the PCB, closest to the power supply.
2. Power plane was split similarly, avoiding any overlap between analog power and digital ground or vice versa. Separate regulators were used for each domain as well.
3. Digital buffers were used between the image sensor's outputs and the digital domain to minimize coupling back onto the sensor's outputs.
4. De-coupling capacitors were placed near every IC power pin.
5. Ferrite beads were placed in series at the image sensor's digital power pins to attenuate high-frequency digital transients from affecting the analog power rails.

4.1.2 Biases

The image sensor requires biases for current mirrors, cascode devices, and reset devices. These biases are generated in various ways as outlined below.

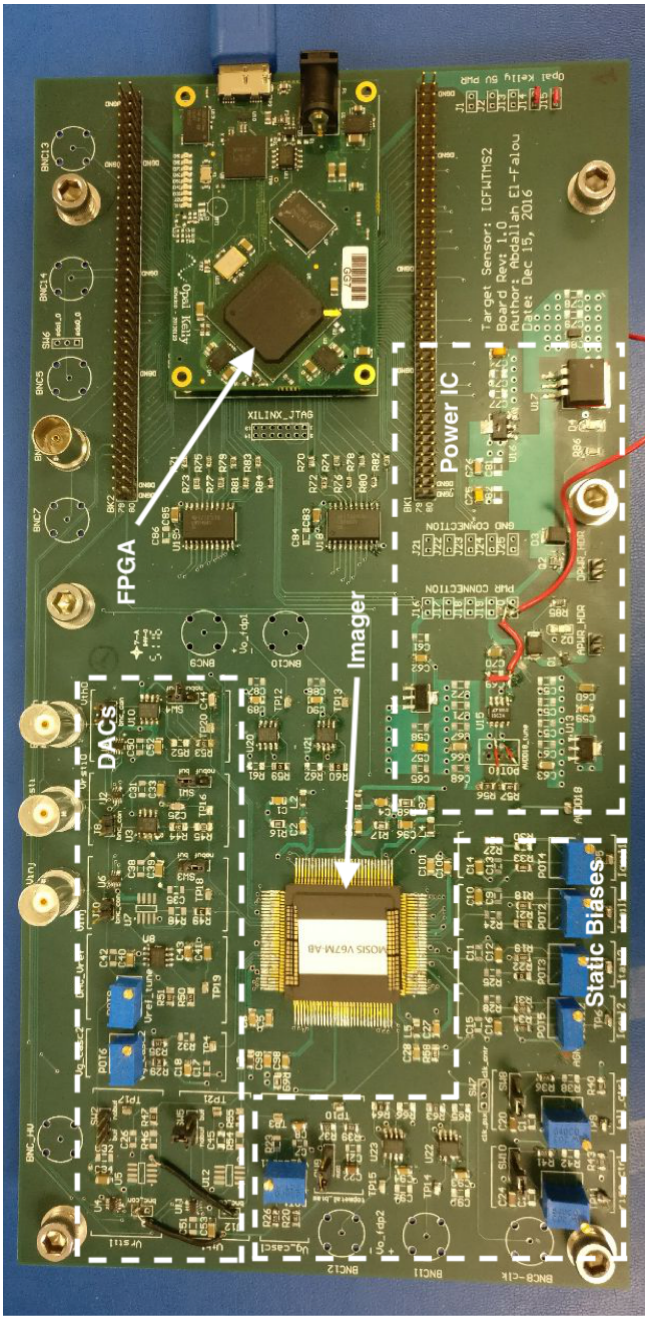
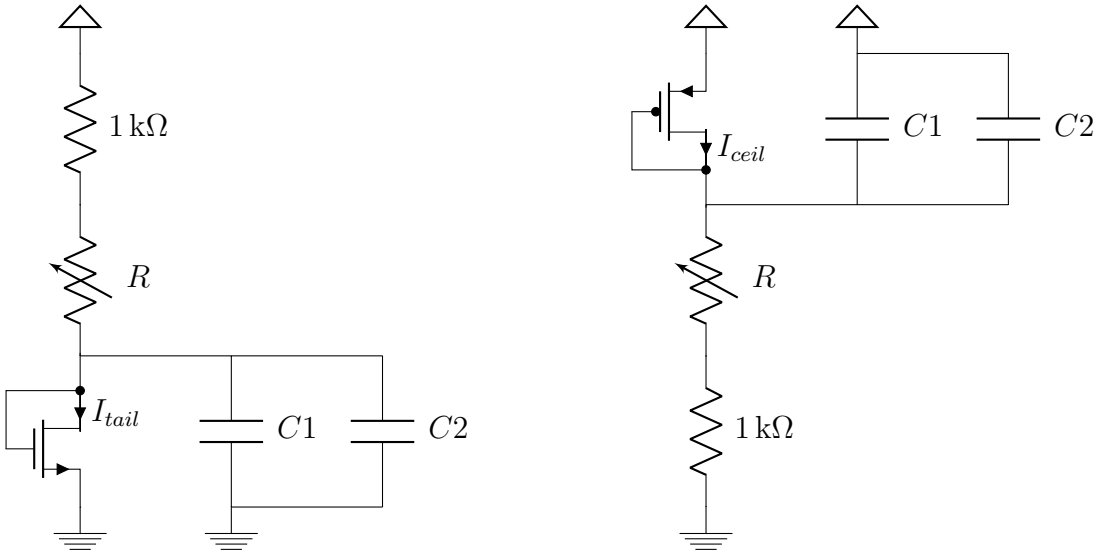


Figure 4.1: System PCB design showing PCI, FPGA, biasing circuits, and power integrated circuit (IC).



(a) NMOS current mirror bias circuit.

(b) PMOS current mirror bias circuit.

Figure 4.2: Current mirror biasing circuits with on-chip devices shown for clarity (they do not exist on PCB).

Current Mirrors

Current biases are generated using a simple resistive network. The voltage across a precise 1 kΩ resistor gives a convenient current reading in mA. A variable resistor is connected in series to allow for fine tuning. Figure 4.2 shows the bias circuit for NMOS and PMOS current mirrors. Two of these circuits are instantiated, one for each array on the imager. A large capacitor is placed in parallel to attenuate low- and mid-frequency noise, as well as a smaller one for high-frequency noise. These appear in parallel to on-chip decoupling capacitors.

Biases were slightly tuned after system bring-up to maximize performance. Typical values for each sub-array are shown in table 4.1.

Cascodes

Cascode gates are biased by resistive dividers. A potentiometer allows for fine tuning of the voltage output and can be replaced by a fixed resistor if need be.

Mirror	Bias Current (µA)
I_{tail1}	254
I_{ceil1}	95.8
I_{tail2}	395
I_{ceil2}	165

Table 4.1: Bias values of current mirrors.

Pixel Inputs

These biases include the pixel threshold and reset voltages V_{th} and V_{rst}, respectively, for each array. These are the most critical biases for several reasons. In order to allow for automatic sweep experiments, DACs controlled by the FPGA supply these voltages. Any noise added by biasing circuits will directly affect the pixel's performance since they connect to high-gain nodes (differential amplifier inputs). Noise will also appear as a differential signal unlike previous biases. For the reasons mentioned, extra care must be taken in the design of these circuits.

We designed pixels for noise performance of $v_n < 600\,\mu V_{rms}$ and mismatch $\sigma(V_{os})$ of similar magnitude. In order to measure these effectively, we design biasing circuits with noise at most an order magnitude below that. Bias sources must also allow for fine sweeps of voltage (namely V_{th}) to generate CDFs. We set an upper bound on the step voltage $V_{step} = 100\,\mu V/LSB$ (that is, $1/6\sigma$) but finer tuning is preferable to accurately fit CDFs curves. Since V_{th} and V_{rst} are dc biases, their bandwidth can be set as low as needed to meet noise specifications.

The main sources of noise along the bias signal chain are the voltage reference, DAC, and output buffer. Some DACs include internal references and output buffer stages so these parts may be excluded. It is convenient to analyze low-frequency noise and high-frequency noise separately. Low-frequency noise is reported as a peak-to-peak value integrated over a specified interval that includes the 1/f region. On the other hand, high-frequency noise is reported as a power spectral density (PSD) at a specified frequency beyond the 1/f corner and is typically flat for greater frequencies. We convert low- and high-frequency noises for each component to a RMS value then add them in quadrature. Peak-to-peak noise scales directly to RMS noise by a factor of $1/2\sqrt{2}$. On the other hand, high frequency noise must be integrated over the noise bandwidth. Assuming a first-order response, high-frequency RMS noise is given by

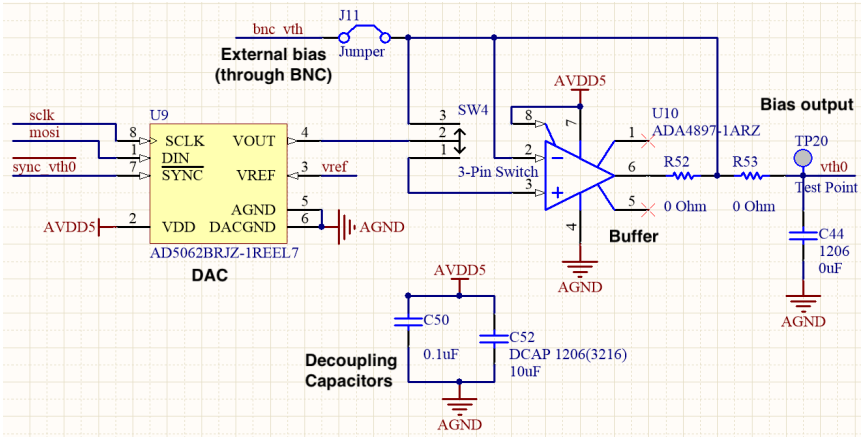


Figure 4.3: DAC circuit including unity-gain buffer.

$$v_{n,hf}^2 = v_{psd}^2 \times \pi/2 \times BW \ , \tag{4.1}$$

where v_{psd} is the noise PSD in $\mathrm{V}/\sqrt{\mathrm{Hz}}$ and BW is the signal bandwidth in Hz. Noise contributions of each component along the signal path are uncorrelated and added in quadrature as well.

A 16-bit unbuffered Analog Devices (AD) AD5062 DAC was used for its low noise, good linearity (low integral nonlinearity (INL) and differential nonlinearity (DNL) errors), guaranteed monotonicity, fast settling time, and convenient serial peripheral interface (SPI). The DAC is followed by a AD OP193 unity-gain buffer to limit bandwidth and minimize output impedance. This op amp specifically was chosen for its low noise, suitable bandwidth, wide input and output ranges, stability in unity-gain feedback, and low voltage and current offsets. The complete DAC setup is shown in Figure 4.3. Jumpers allow for the buffer to be bypassed, or alternatively for the bias to be supplied directly by a BNC instead. Lastly, an AD ADR420 reference IC was used to supply a 2.048 V reference directly to all DACs. Noise was analyzed from the reference, through the dac, and finally at the output of the buffer. Table 4.2 shows the noise contribution of each component. Low-frequency noise is integrated over a bandwidth of 0.1 to 10 Hz for all the components mentioned.

The total noise seen at the output of the buffer, given an op amp bandwidth of 35 kHz, is 22 $\mu\mathrm{V}_{\mathrm{rms}}$. This is negligible compared to the expected pixel noise. Given a reference of 2.048 V and 16 bits, $V_{step} = 31.25\,\mu\mathrm{V/LSB}$, allowing very fine sweeps of bias voltages. This analyses could be expanded to include noise coupling in from power and ground, but it is

Component	Low-frequency noise (μV_{p-p})	High-frequency noise ($nV/\sqrt{Hz}$)
AD420 (voltage reference)	1.775	60
AD5062 (DAC)	6	24
OP193 (buffer)	3	65.4

Table 4.2: Noise contributions of voltage reference, DAC and buffer. The buffer's figures include both voltage and current noises assuming a DAC output impedance of 8 kΩ (typical). Low-frequency noise is integrated over a bandwidth of 0.1 to 10 Hz.

assumed to be negligible especially since the rails are very heavily de-coupled.

4.2 FPGA RTL Design

The FPGA implements digital hardware that is not tightly coupled to the sensor array, reducing cost but more importantly allowing for much more flexibility in design. A few important aspects of the design will be elaborated on in sections below. A digital model of the image sensor was written in Verilog to enable verification.

Due to the differences in path delays within the FPGA and on the board, each output was tuned using Xilinx IODELAY2 resources such that they arrive just after the system clock at the image sensor's pins. All FPGA outputs are registered as well.

4.2.1 Scan Chains

Each scan chain on the image sensor has a corresponding control module on the FPGA to generate its scan controls (`si`, `se`, etc) as well signal masks. The control module is implemented using a finite-state machine (FSM) and configured by setting parameters in software that correspond to registers on the FPGA. These parameters are shown below:

- `clk_per_row`: number of clock periods spent within each row where masks can take effect.
- `mask_del`: number of clock periods within a row before `mask` is enabled.
- `mask_len`: number of clock periods within a row that `mask` is enabled for.

Scan chains can operate the chip in two modes: *Array Mode* and *Single Row Mode*. These will be elaborated on in the sections below. Both modes regularly validate chip scan chains by comparing their scan outputs `so` to the expected output and report errors as soon as they occur.

Array Mode

Scan chains cycle through all pixel and counter rows during *Array Mode*. Some key sensor parameters and how they relate to the scan chain parameters above are explained below. The prefixes `pixscnch_`, `cntrscnchen_` and `cntrscnchrd_` refer to parameters of the Pixel Scan Chain, Counter-Enable Scan Chain and Counter-Read Scan Chain respectively. Counter-Enable Scan Chain scanning parameters are typically equivalent to those of the Pixel Scan Chain.

- T_{clk}, the system clock period, is given by $\frac{\mathrm{M_{clk}}}{\mathrm{D_{clk}}} \times 100\,\mathrm{MHz}$.
- T_{pix}, the pixel reset period (and reciprocal of count rate), is given by $26 \times T_{clk} \times$ `pixscnch_clk_per_row`.
- n_{en}, the maximum count attainable in a counter per frame, is given by $\frac{\texttt{cntrscnchrd\_clk\_per\_row}}{\texttt{cntrscnchen\_clk\_per\_row}}$.
- T_{frame}, the time taken to acquire a frame, is given by $n_{en} \times T_{pix}$.

This mode utilizes the whole array of pixels but can introduce array-level issues such as column cross-talk.

Single Row Mode

This mode allows the user to lock all masks onto a single arbitrary row, such that it is continuously resets, integrates and latches. Other rows receive no masks and therefore remain in their default state. The only sensor parameter that changes here is T_{pix}, which is now simply $T_{clk} \times$ `pixscnch_clk_per_row`. Other parameters based on this change accordingly.

The *Single Row Mode* is useful in operating the sensor as a line scanner and to reduce row cross-talk through column buses.

4.2.2 Data Path

Counter data is serially output by the image sensor on up to 4 parallel lanes per array. The receiving module receives data from all lanes and packs it coherently (according to column index) before passing it onto a first-in, first-out (FIFO) buffer. A Pipe Out module (provided by Opal Kelly) receives data from the FIFO and transfers it over USB to the PC. Data rates over USB vary widely, which may cause the FIFO to overflow. This only occurs at high count rates and is reported when it occurs, notifying the user and allowing them to repeat an experiment if need be.

A major limitation of the data path at time of writing is that it can only receive data from one array at a time. The limiting factor here is bandwidth and/or latency on the USB bridge and can be rectified by either:

1. Increasing the FIFO depth (which would require a larger replacement FPGA),
2. Utilizing the Opal Kelly on-board dynamic random access memory (DRAM) as a buffer instead of the FIFO, or
3. Collapsing consecutive frames together (analogous to increasing the on-chip counter width N_{bits}).

4.2.3 Digital to Analog Converters

A single module handles all SPI components on the board and is configured by setting parameters on the PC, similar to previous modules. The main components of interest here are DACs. Pixel input biases V_{th1}, V_{th2}, V_{rst1} and V_{rst2} are set to dc values before the reset is deasserted on the sensor and are simple enough to control.

The test pixel input v_t, however, must be stepped at precise times to couple charge onto the pixel while it's integrating. This particular DAC is controlled by a separate module to generate a series of periodic pulses with parameterized period, delay, pulse width, and voltage levels. The user must however calibrate timing of the DAC waveform in relation to pixel waveforms by tuning its delay, since writing over SPI introduces delays (as well as internal delays in the DAC before it settles).

4.3 Imager Characterization

The PCI's performance is experimentally characterized in this section. Figure 4.4 shows our fabricated PCI. In order to measure pixel temporal noise and validate the offset correction scheme, we begin by operating pixels in *Voltage Mode*. In this mode, pixels are configured like voltage comparators and no current integration takes place. This eliminates current leakage, capacitive coupling and non-ideal switch effects on the integration (i.e., input) node. Note that *Voltage Mode* is only used for characterization and troubleshooting purposes; since no charge integration takes place, it cannot be used for imaging.

We then proceed to *Charge Mode*. This mode is useful for imaging, since current is integrated for a specified period at the pixel input. However, the effects of current leakage, capacitive coupling and non-ideal switches at the integration node manifest in this mode and may deteriorate performance. The purpose of operating in this mode is to characterize temporal noise and pixel-to-pixel mismatch in order to quantify the photon energy resolution of our pixel.

In each of *Voltage Mode* and *Charge Mode*, scan chains are first operated in *Single Row Mode* to minimize array-level effects (e.g., column cross-talk) and then in *Array Mode* for full-scale array operation. Test pixels operating in *Charge Mode* can also have a test voltage applied at their inputs. Every experiment is a sweep, whereby V_{rst} is set constant and V_{th} is swept. V_{th} will be defined relative to V_{rst} in this section to avoid the need of referring to each of them repeatedly. Since switch non-idealities play a significant role in the pixel's performance, experiments were conducted to better understand these phenomena in the context of our imager. Lastly, the pixel PA is characterized as well.

Because many of the results below are statistical in nature, it is important to note the sample size as well. In general, the sample size (or number of comparisons performed by a pixel) is calculated as the maximum count per frame n_{en} multiplied by the number of frames acquired N_{frame}. All experiments below utilize a sample size of at least 10,000.

4.3.1 Pixel: Voltage Mode

The objective of operating in *Voltage Mode* is to validate the basic pixel operation and quantify temporal noise v_n and pixel mismatch $\sigma(V_{os})$ with minimal complexity. Pixels are operated like voltage comparators in this mode with V_{rst} applied at the positive input and V_{th} at the negative input. No current integration occurs here since the integration node is always driven to V_{rst}. This is implemented by eliminating the first phase of reset (i.e., ϕ_1' remains high). Figure 4.5 shows the pixel configuration and typical waveforms in

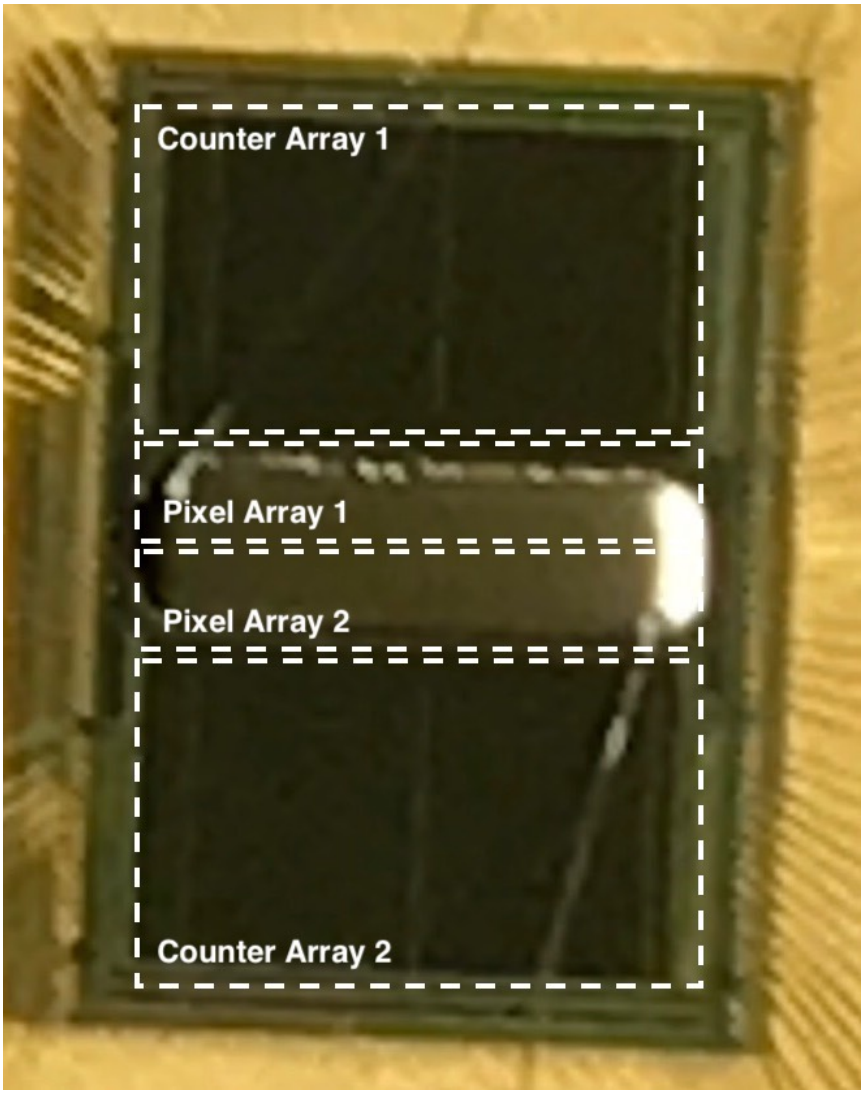
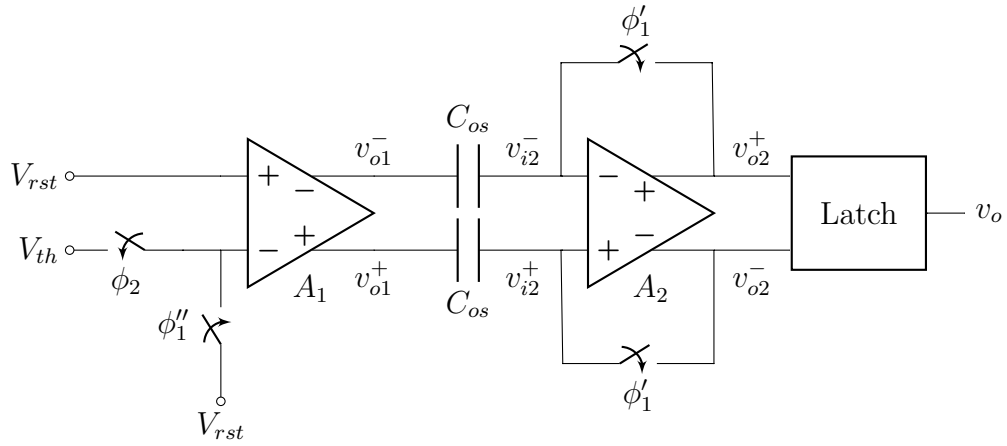
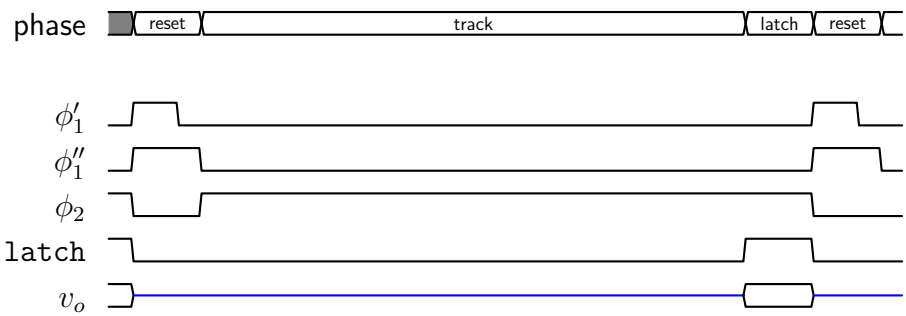


Figure 4.4: Fabricated image sensor showing pixel and counter arrays.



(a) Pixel topology.



(b) Pixel timing diagram.

Figure 4.5: Pixel configuration in *Voltage Mode*.

this mode. Leakage, charge injection and capacitive-coupling effects at the this node is therefore eliminated, and pixel cross-talk is minimal.

Single Row Mode

An experiment was run with the parameters shown in 4.3. Figure 4.6a shows the probability of output $Pr(1)$ as V_{th} is swept, which results in a typical CDF as expected. Input-referred temporal noise of each pixel is extracted numerically, yielding a mean noise of $v_n = 609\,\mu\mathrm{V_{rms}}$. This closely matches our analysis in Chapter 2 that thermal noise ($k_BTC = 600\,\mu\mathrm{V}$) is the dominant noise source.

Parameter	Value
ΔV_{th}	93.75 µV (3 LSB)
T_{pix}	1.5 µs
T_{frame}	46.5 µs
N_{frame}	8795

Table 4.3: *Voltage Mode* row experiment parameters.

Parameter	Value
ΔV_{th}	93.75 µV (3 LSB)
T_{pix}	1 µs
T_{frame}	806 µs
N_{frame}	999

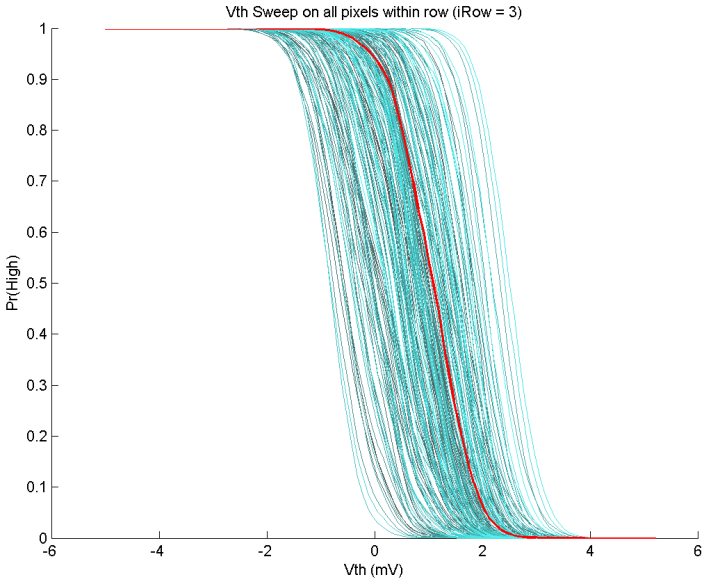
Table 4.4: *Voltage Mode* array experiment parameters.

Pixel offset is also extracted numerically by interpolating each CDF at $Pr(1) = 0.5$ and a histogram of offsets is shown in Figure 4.6b. The distribution is Gaussian as expected, although the sample size is somewhat small for a single row (only 194 pixels). Offset mismatch is characterized by the standard deviation $\sigma(V_{os}) = 691\,\mu V_{rms}$. This is much lower than mismatch of the PA itself and therefore shows that offset-correction works as expected. However, mismatch is greater than our simulation result of $\sigma(V_{os}) = 150\,\mu V$ and slightly exceeds our design target of $\sigma(V_{os}) < 600\,\mu V_{rms}$.

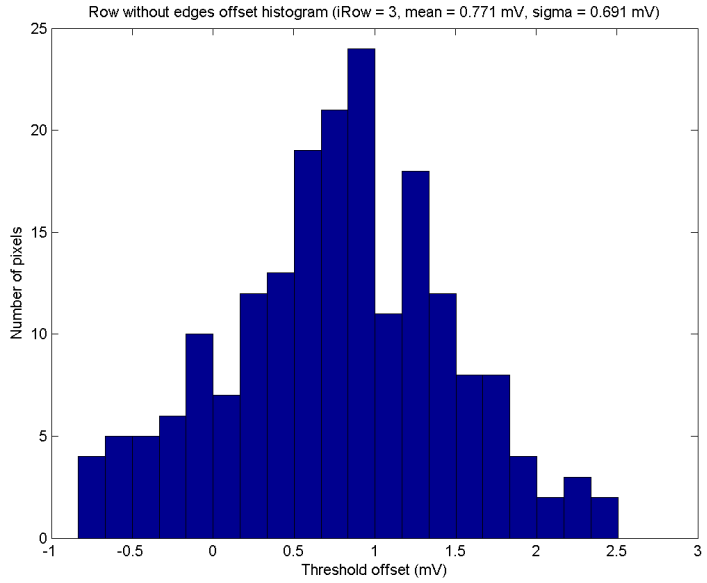
Array Mode

Table 4.4 summarizes the parameters of this experiment. As expected, results from this mode are essentially identical to the *Single Row Mode* since the pixel input node is not susceptible to leakage, coupling, charge injection, or other second-order effects. However, the significantly larger number of pixels allows for a better characterization of mismatch $\sigma(V_{os})$. Figure 4.7 shows all pixel CDFs and a histogram of pixel offsets V_{os}.

The mean temporal noise of all pixels and offset mismatch are numerically extracted as $v_n = 588\,\mu V_{rms}$ and $\sigma(V_{os}) = 577\,\mu V_{rms}$, respectively. The distribution of offsets is even more clearly Gaussian than in Figure 4.3.1, likely due to the larger sample size. This is also probably the reason behind the slight differences in v_n and $\sigma(V_{os})$ between *Single Row*



(a) Pixel probabilities of output over V_{th} sweep. Red curve corresponds to test pixel.



(b) Histogram of pixel offsets excluding row edges (194 pixels).

Figure 4.6: Results of *Voltage Mode* row experiment.

Parameter	Value
ΔV_{th}	187.5 µV (6 LSB)
T_{pix}	10.6 µs
T_{frame}	328.6 µs
N_{frame}	9291
t_{integ}	10 µs
ϕ_1 device	PMOS

Table 4.5: *Charge Mode* row experiment parameters.

Mode and *Array Mode*.

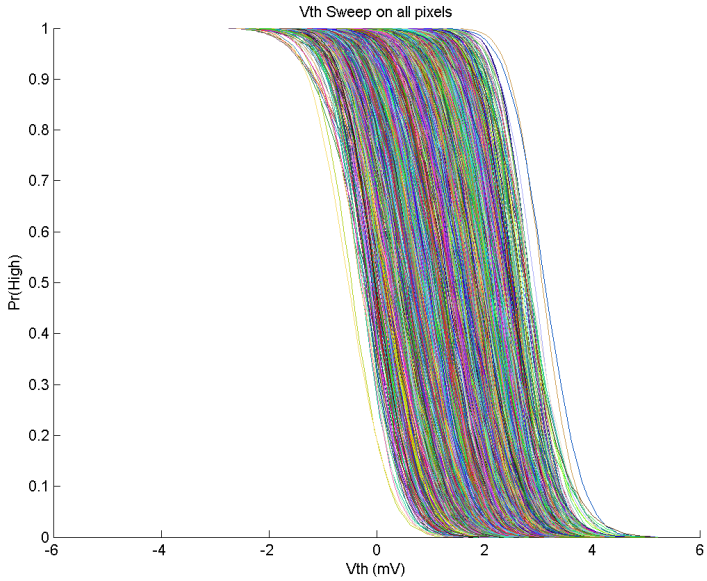
4.3.2 Pixel: Charge Mode

Pixels operate as they would during an imaging operation in this mode. The input node is left floating (i.e., integrating) for some time before a comparison is made. However, leakage, charge injection and capacitive-coupling effects can significantly affect the input node in this mode.

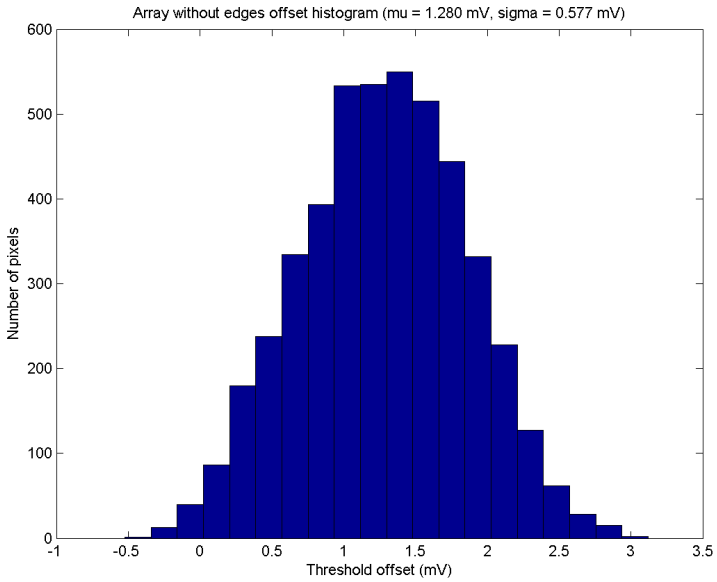
Single Row Mode

The parameters for this experiment are shown in Table 4.5. Integration time t_{integ} is defined as the time between the fall of ϕ_1'' and rise of `latch` within the pixel (refer to Figure 2.10a). Results are shown in Figure 4.9. The average temporal noise increased slightly to $v_n = 650\,\mu V_{rms}$, while mismatch tripled to $\sigma(V_{os}) = 1.659\,mV_{rms}$. This is not at all surprising given the effects of charge injection, coupling and leakage. Noise and mismatch add in quadrature to yield an equivalent uncertainty of energy threshold $\sigma(E_{th}) = 5.6\,keV$. The test pixel also sees a significant offset compared to others, which is likely due to edge effects and the difference in capacitance at its integration node due to the test circuitry. Since v_t is grounded, the non-trivial capacitance C_t adds to the total input capacitance (refer to Figure 2.15).

An interesting phenomenon in this experiment is the apparent gradient down the row in pixel offsets, as seen by the color gradient in Figure 4.9a. The trend is seen much more clearly in Figure 4.10, which simply plots the pixel offsets across the row. This trend

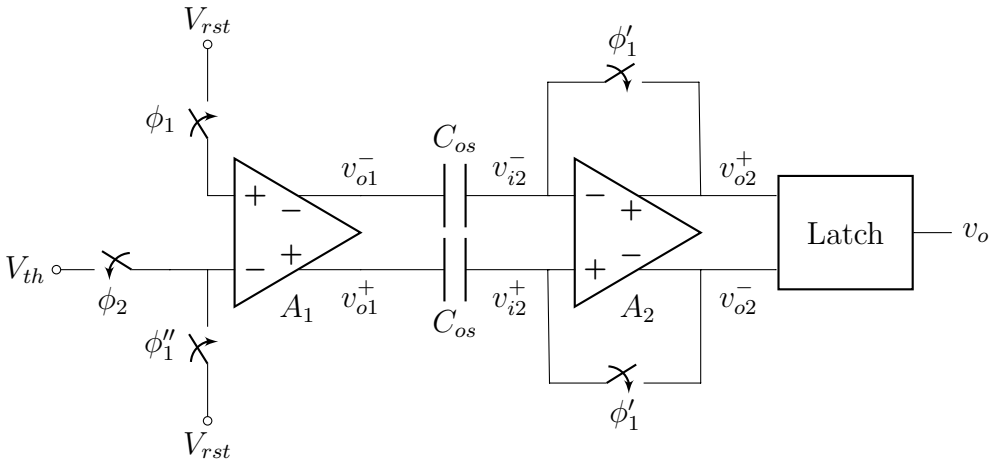


(a) Pixel probabilities of output over V_{th} sweep.

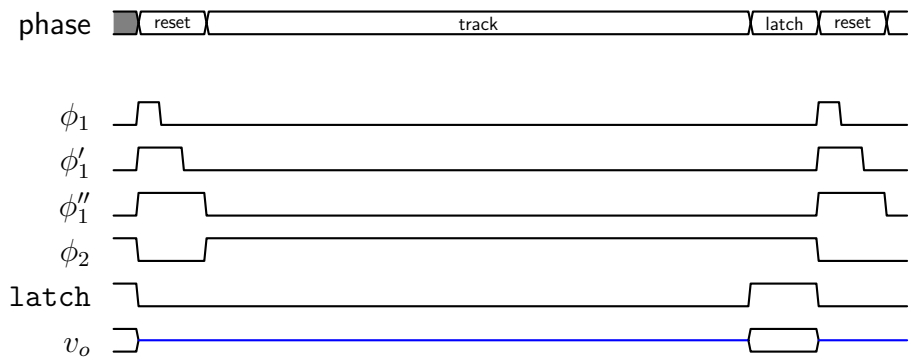


(b) Histogram of pixel offsets excluding array edges.

Figure 4.7: Results of *Voltage Mode* array experiment.

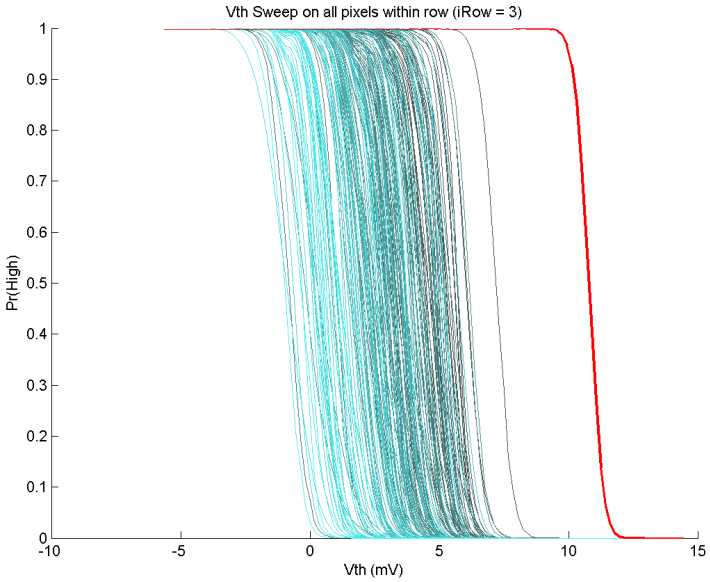


(a) Pixel topology.

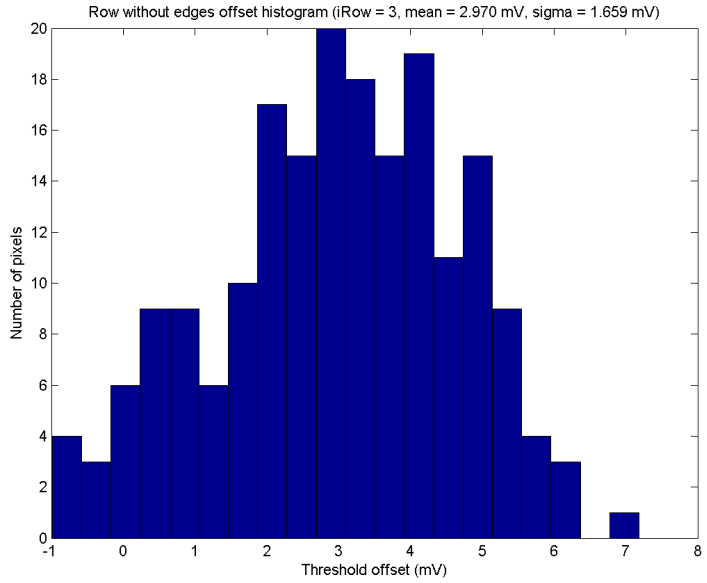


(b) Pixel timing diagram.

Figure 4.8: Pixel configuration in *Charge Mode*.



(a) Pixel probabilities of output over V_{th} sweep. Brighter curves correspond to higher column indices. Red curve corresponds to test pixel.



(b) Histogram of pixel offsets excluding row edges (194 pixels).

Figure 4.9: Results of *Charge Mode* row experiment.

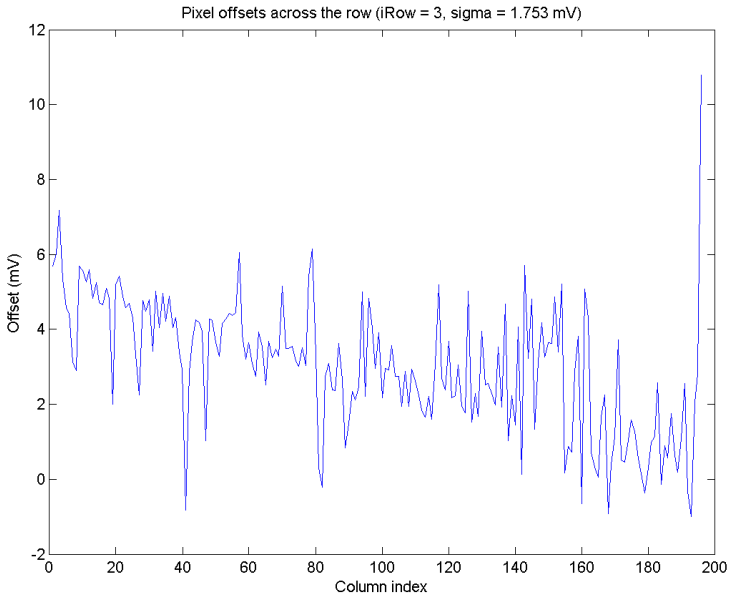


Figure 4.10: Pixel offset vs. column index showing gradient in offsets.

suggests that the net charge deposited onto the integration node follows a gradient across the chip. This could be due to decrease in the PMOS threshold voltage V_{tp} down the row, which would reduce positive charge injection. It also suggests that the first stage may be entering a non-linear region during reset causing imperfect offset correction.

Temporal Response

CDFs and histograms do not necessarily give the complete picture since the frames are summed, and hence any sense of time is lost. The temporal response can be seen by plotting an arbitrary pixel's output in every frame as seen in Figure 4.11. A transient is observed on all pixel responses that settles after approximately 0.8 s. This is because all other rows in the array are in their default mode (i.e., integrating) and will leak for some time after reset and finally settle. Therefore, frames within this time period are ignored. This was applied to obtain the results in Figure 4.6 as well.

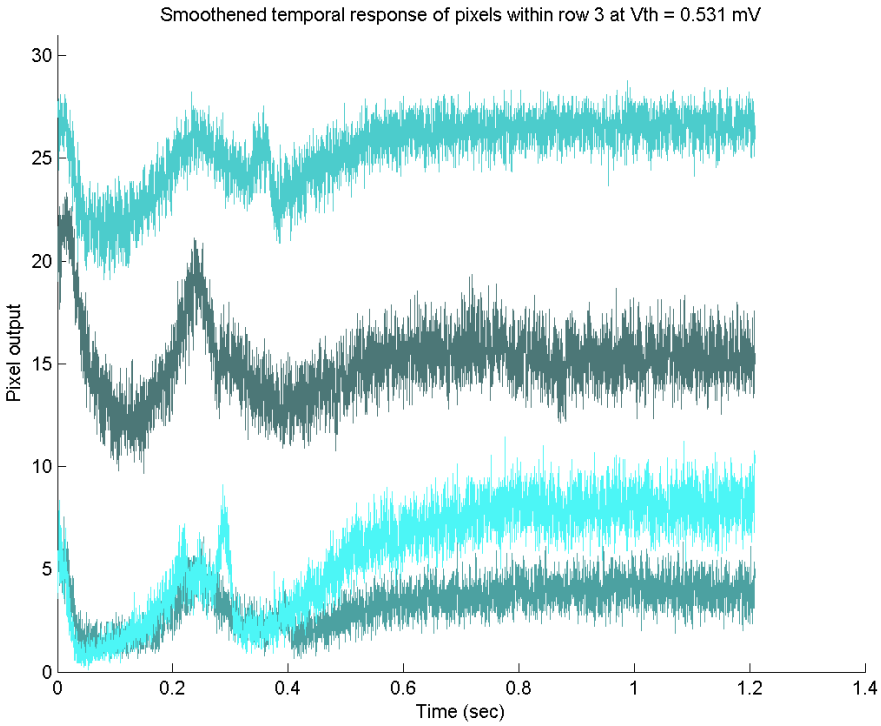


Figure 4.11: Temporal response of four arbitrary pixels in a *Voltage Mode* row experiment. A moving mean filter is applied to smoothen the curves.

Parameter	Value
ΔV_{th}	187.5 µV (6 LSB)
T_{pix}	10.6 µs
T_{frame}	328.6 µs
N_{frame}	3311
t_{integ}	10 µs
ϕ_1 device	PMOS

Table 4.6: *Charge Mode* test pixel experiment parameters.

Test Pixel

An Agilent 33250A wave generator was used to generate pulses at the test pixel's input v_t. Several sweep experiments were performed with different peak-to-peak test inputs Δv_t. These are shown in Figure 4.12a.

Increasing Δv_t shifts CDFs to the right as expected. For each of these curves, the mid-point crossing was extracted and plotted against Δv_t , as shown in Figure 4.12b. The pixel's input capacitance C_i can be estimated from the inverse slope of this curve by

$$C_i = C_t \left(\frac{\Delta v_t}{\Delta V_{os}} - 1 \right) \ , \tag{4.2}$$

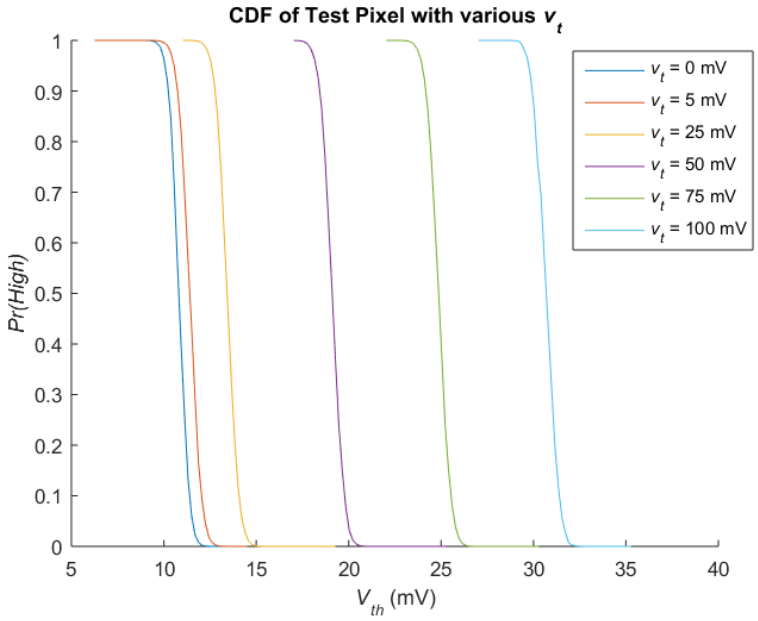
assuming $C_t = 5\,\text{fF}$ (its nominal design value), $C_i \approx 22\,\text{fF}$. This is considerably higher than expected from simulations. However, test pixels likely have larger input capacitances due to the parasitic capacitance of C_t and the presence of PA probes (these are row-wise strips that span the whole pixel). The voltage noise observed on this test pixel $v_n = 453\,\mu\text{V}_{\text{rms}}$ is lower than that of regular pixels. Assuming thermal noise is dominant here, this corresponds to a capacitance $C_i = 20\,\text{fF}$ and strongly supports the idea that test pixel capacitance is indeed higher than regular input capacitance. Note that a lower thermal voltage noise here is analogous to a higher thermal charge noise, meaning regular pixels should perform better than test pixels when operated with a biased a-Se layer.

The same experiment was done for all rows (albeit with fewer Δv_t test points), yielding histograms of test pixel offsets and input capacitances (see Figure 4.13).

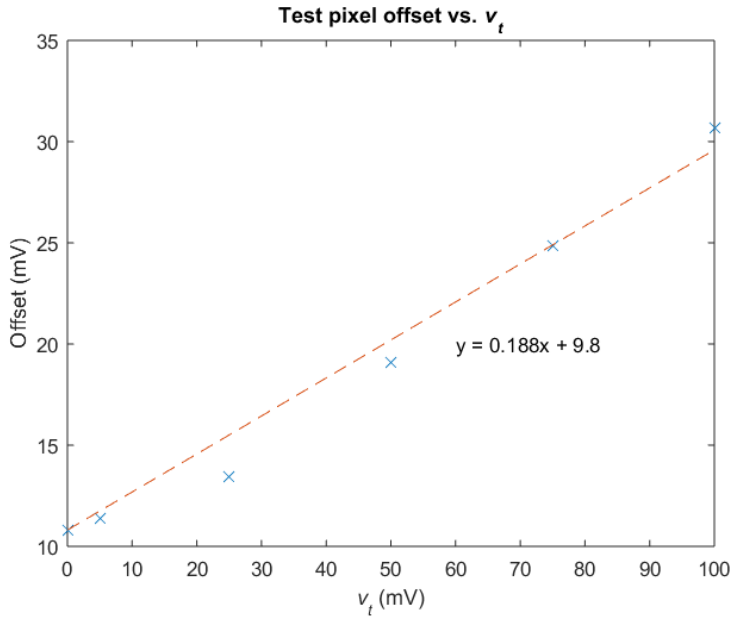
Pre-Amplifier Saturation

Noting the increase in mismatch $\sigma(V_{os})$ from *Voltage Mode* to *Charge Mode*, we investigate the changes on the integration node more closely. We suspect that the biggest culprits are charge injection and clock feedthrough from reset switches. These effects result in a non-zero voltage offset $V_{os,sw}$ at the first PA's input (in addition to its inherent offset). If this offset is large enough, it can push the PA out of its linear region. Note that all digital signals toggling after ϕ_1' switches off will couple onto the integration node as well. With a swing of 1.8 V, even stray capacitances can be significant.

We quantify $V_{os,sw}$ by resetting pixels as if in *Voltage Mode*, storing (and correcting) the PA's offset only, then switching ϕ_1' off. In other words, ϕ_1' is delayed until ϕ_2 rises (refer to Figure 2.10b). This was repeated using PMOS and NMOS reset devices separately, both

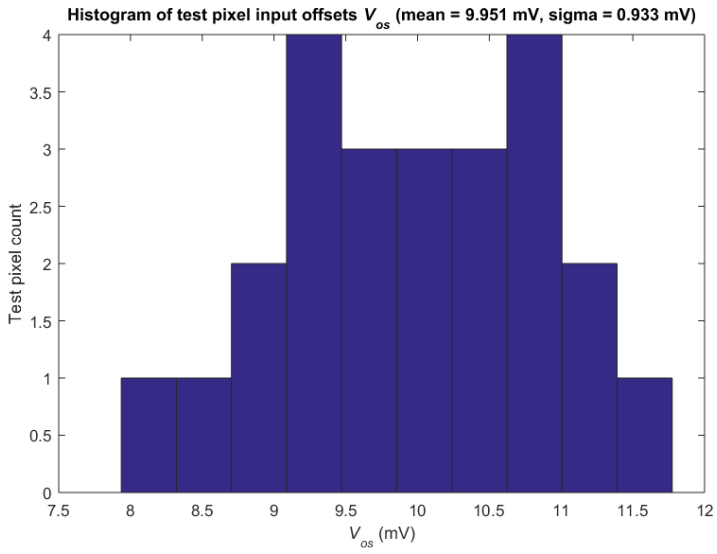


(a) Test pixel probability of output over V_{th} sweep for various v_t inputs.

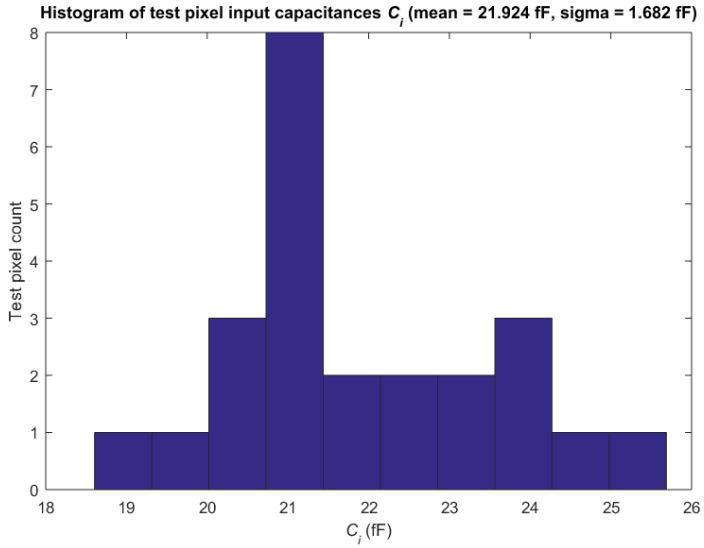


(b) Test pixel change in offset vs. change in test input v_t.

Figure 4.12: Results of *Charge Mode* test pixel experiment.



(a) Test pixel input offset V_{os} distribution.



(b) Test pixel input capacitance C_i distribution

Figure 4.13: Results of *Charge Mode* single row test pixel experiment for all rows.

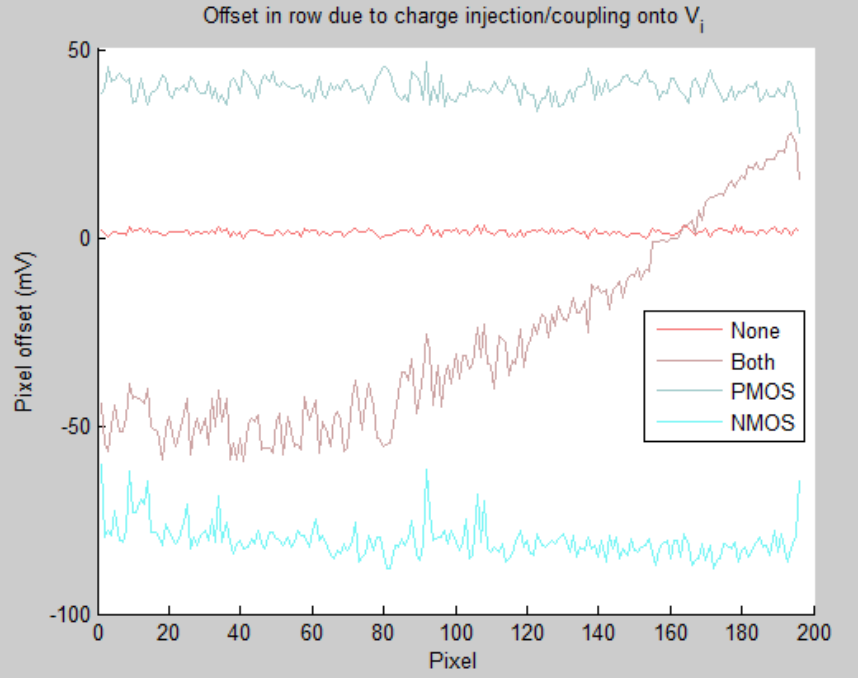
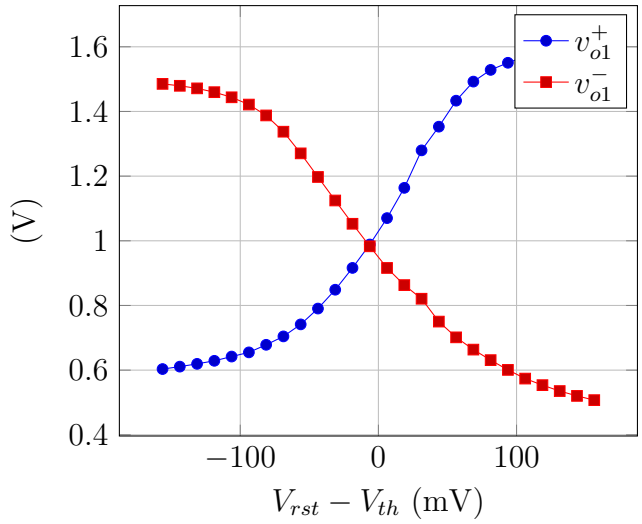


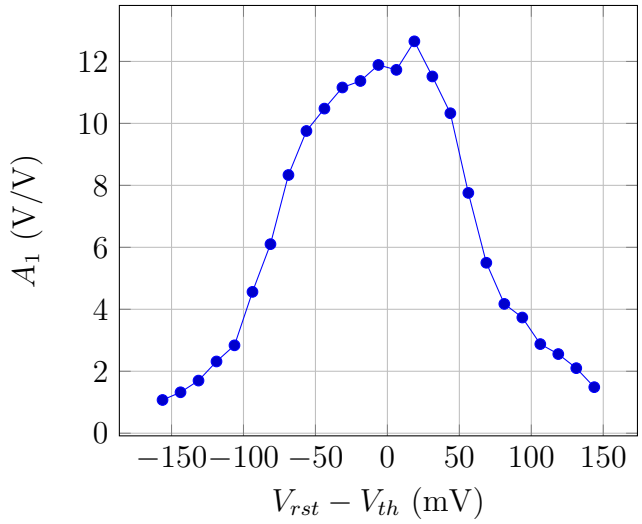
Figure 4.14: Offset voltage $V_{os,sw}$ developed on integration node due to switch non-idealities and capacitive coupling from pixel control signals (row 3).

devices, and neither for reference. Results are shown in Figure 4.14. $V_{os,sw}$ is for PMOS and NMOS devices is approximately 40 mV and −80 mV, respectively. Referring back to the PA transfer curve in Figure 2.3, it is likely that the PA entered its non-linear region. This causes imperfect offset correction, and hence the increase in $\sigma(V_{os})$ for *Charge Mode*.

To validate this, we characterized the first PA's transfer curve by operating it in *Voltage Mode*, sweeping V_{th}, and observing its output in a test pixel. Results are shown in Figure 4.15. The output swings as expected with a peak gain of 11.89 V/V (neglecting the slight glitch at $V_{rst} - V_{th} \approx 10\,\text{mV}$). However, the PA is only linear within the range of $-43\text{mV} \leq V_{rst} - V_{th} \leq 43\text{mV}$, as defined by the 1 dB compression point. Given the magnitude of $V_{os,sw}$, this supports the hypothesis that offset is imperfectly stored, and hence the increase in $\sigma(V_{os})$.



(a) First PA input-output characteristic curve. Outputs were sampled after settling on an oscilloscope.



(b) Gain of first PA, calculated as a numerical derivative of the input-output characteristic curve above.

Figure 4.15: Characterization of first PA stage. V_{rst} is set to 1.1 V and V_{th} is swept over a range of 300 mV.

Parameter	Value
ΔV_{th}	343.76 µV (11 LSB)
T_{pix}	26 µs
T_{frame}	806 µs
N_{frame}	1001
t_{integ}	25.2 µs
ϕ_1 device	NMOS
v_t (dc)	1 V

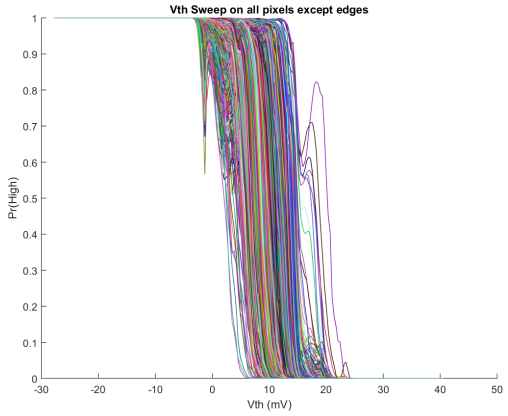
Table 4.7: *Charge Mode* array experiment parameters.

Array Mode

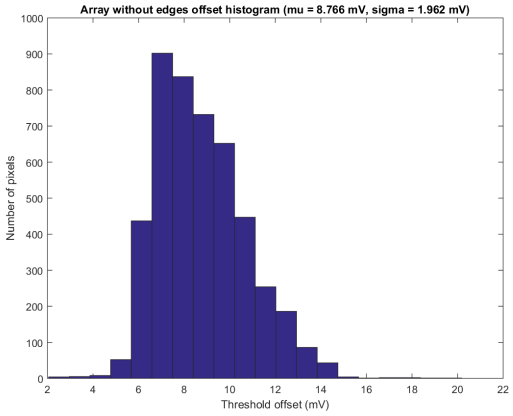
Table 4.7 summarizes the parameters of this experiment. Scan chains are configured to reset each row, leave it integrating while cycling through other rows, and finally concluding the row's cycle by latching.

Figure 4.16 shows all pixel CDFs and a histogram of pixel offsets V_{os} (excluding edges). Note that pixel CDFs are not monotonically decreasing. The glitches seen are due to deterministic effects (e.g. interference) and not random noise, since the latter would have simply resulted in more gradual slopes. The distribution of V_{os} is skewed, but this may be due to interference or imperfect offset storage. Pixel offset mismatch is extracted numerically as in previous experiments as $\sigma(V_{os}) = 1.962\,\mathrm{mV_{rms}}$. This is a slight increase from the single row's mismatch. However, the glitches observed in pixel CDFs effectively increase the spread between PD and ER, increasing uncertainty. We fit them to Gaussian profiles nevertheless, resulting in a measured noise of $v_n = 2.250\,\mathrm{mV_{rms}}$. This now is the dominant source of uncertainty and the major limiter of photon energy resolution. To achieve the same ER and PD as specified in Table 1.2, the minimum detectable photon energy is $E_{ph} > 42\,\mathrm{keV}$.

Since row-wise interference would have appeared in the single row experiments, we focus on column-wise interference. Pixel columns share biases and the digital pixel output v_o (refer to Figures 2.10a and 2.14). Biases are unlikely to cause interference since they are heavily decoupled. However, the output bus is not driven except when a pixel on the column is latched. Furthermore, the bus's value toggles throughout a pixel's integration period depending on the output of other pixels on the same column. Since v_o has a large swing of 1.8 V and the pixel is tightly packed, v_o toggling can result in significant coupling



(a) Pixel probabilities of output over V_{th} sweep.



(b) Histogram of pixel offsets excluding edges (4656 pixels).

Figure 4.16: Results of *Charge Mode* array experiment excluding edges.

onto the integration node. Parasitic extraction of the pixel layout estimates a coupling capacitance of 50 aF, which would result in approximately 560 e^- being coupled onto the node per toggle (positive or negative). This is equivalent to the incidence of a 28 keV photon and can severely deteriorate performance. The effect is different for single row and array experiments:

- Single row: no other pixels toggle v_o, therefore its value is determined by the pixel's previous latch result and does not toggle during integration. However, leakage on v_o will vary depending on its previous value, possibly causing a hysteric effect.
- Array: every time v_o toggles due to another pixel's output, charge is coupled onto the integration node. Since we can not guarantee that the number of positive and negative edges are equal, a net voltage will likely result. Leakage effects on v_o also contribute to uncertainty here.

We employed a workaround in single row experiments to reduce coupling effects, whereby the pixel output is driven during reset to set it at a consistent initial condition. This is implemented by asserting `latch` for a short duration while $\phi_1' = \phi_1'' = \phi_1''' = 1$. However, the state varies on a per-pixel basis. This is not ideal, but performance was improved nevertheless. Results shown in the *Charge Mode* single row experiment incorporated this improvement already. Unfortunately, our scan chain architecture does not allow for a sim-

	Specification	Measured Performance
a-Se thickness µm	200	N/A
Pixel area (μm^2)	$\leq 13 \times 13$	11.44×11.44
Minimum detectable E_{ph} (keV)	20	33
Uncertainty of photon energy threshold $\sigma(E_{th})$ (keV)	3.3	5.6
Probability of detection ($E_{ph} = 20\,\text{keV}$)	99.87%	97.32%
Error rate ($E_{ph} = 20\,\text{keV}$)	0.13%	2.68%
Photon count rate (cps/μm^2)	250	830
Input-referred noise (e^-_{rms})	47	41
Input-referred random offset (e^-_{rms})	47	104

Table 4.8: Summary of the PCI's performance in this work.

ilar workaround in array experiments. Ideally, v_o would be driven to a known state when no pixels are latched to begin and end every integration consistently.

4.4 Performance Summary

Pixel mismatch and noise performance are expressed above in the voltage domain but we are ultimately interested in the imager's ability to detect photons and distinguish between different photon energies. Chapters 1 and 2 explained how voltage, charge, and photon energy quantities can be converted given assumptions on pixel integration capacitance C_i and a-Se conversion gain $W_\pm$. We assume $C_i = 10\,\text{fF}$ and $W_\pm = 50\,\text{eV/ehp}$. Table 4.8 summarizes the specifications and achieved results.

Unfortunately, we did not have a chance to complete characterization of our PCI's performance with an X-ray source as of the time of writing due to time constraints. Such experiments would require deposition of a-Se on the chip and setting up an X-ray testing apparatus. This is an ongoing effort.

Chapter 5

Conclusion and Future Work

This thesis presents a novel hybrid a-Se-CMOS X-ray PCI for use in mammography and μ-CT. We demonstrate a 11.4 µm pixel with low noise and mismatch, enabling the use of multiple thresholds in the future for multi-spectral imaging. The PCI meets all specifications when operated in *Single Row Mode* except the minimum detectable energy (33 keV measured), but is still useful within the X-ray range of our target applications. Pixel crosstalk is a major performance limiter in *Array Mode*, increasing the minimum detectable energy up to 42 keV. Our PCI's performance is summarized and compared with other reported PCI's in Table 5.1. We achieve a lower input-referred noise than other imagers in the literature, enabling very precise imaging modalities. Although input-referred random offset is higher than we targeted, it can potentially be corrected using image processing techniques since per-pixel offsets are consistent. Our imager can also be utilized for other imaging modalities which utilize higher X-ray energies.

5.0.1 Future Work

The following items highlight the main areas that can be improved in the next generation of our PCI:

- Design a circuit external to the pixel array that would drive pixel output column buses (v_o) to a known voltage when no pixels are latched. This will guarantee that each integration cycle begins and ends with the same conditions.
- Repeat the pixel layout with more stringent guarding of the integration node from all switching signals. Also consider using complementary signals to reduce switching

Reference	This work	[21]	[20]	[23]	[24]
CMOS process (nm)	180	130	130	130	40
Sensor	a-Se	CdTe	HgI_2	Si	Si
Active array size	52×196	8×4	128×128	128×128	24×18
Pixel size (μm^2)	11.44×11.44	756×800	60×60	75×75	100×100
Number of energy bins	1	256	3	1	1
Power per pixel (μW)	63	10000	4.6	26	35
Maximum count rate ($cps/\mu m^2$)	826	13	103	213	120
Input-referred noise (e^-_{rms})	41	–	68	123	117
Input-referred random offset (e^-_{rms})	104	–	134	19	36

Table 5.1: Comparison of this work and other X-ray PCIs in the literature.

effects further. This will come at the cost of an increased pitch but our specification allows for this.

- Reduce the gate drive of integration node reset devices (ϕ'_1) and limit their operation to weak-inversion to reduce charge injection and clock feedthrough onto the integration node. By reducing these effects, the PA can operate within its linear region and offset can be corrected more accurately.

- Reduce overall power of imager by only enabling the PAs of pixels for a short duration before they are latched. That is, the vast majority of pixels can have their PAs off most of the time. This may also reduce interference since the array will be more "quiet" in general.

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APPENDICES

Appendix A

Simulation Testbenches

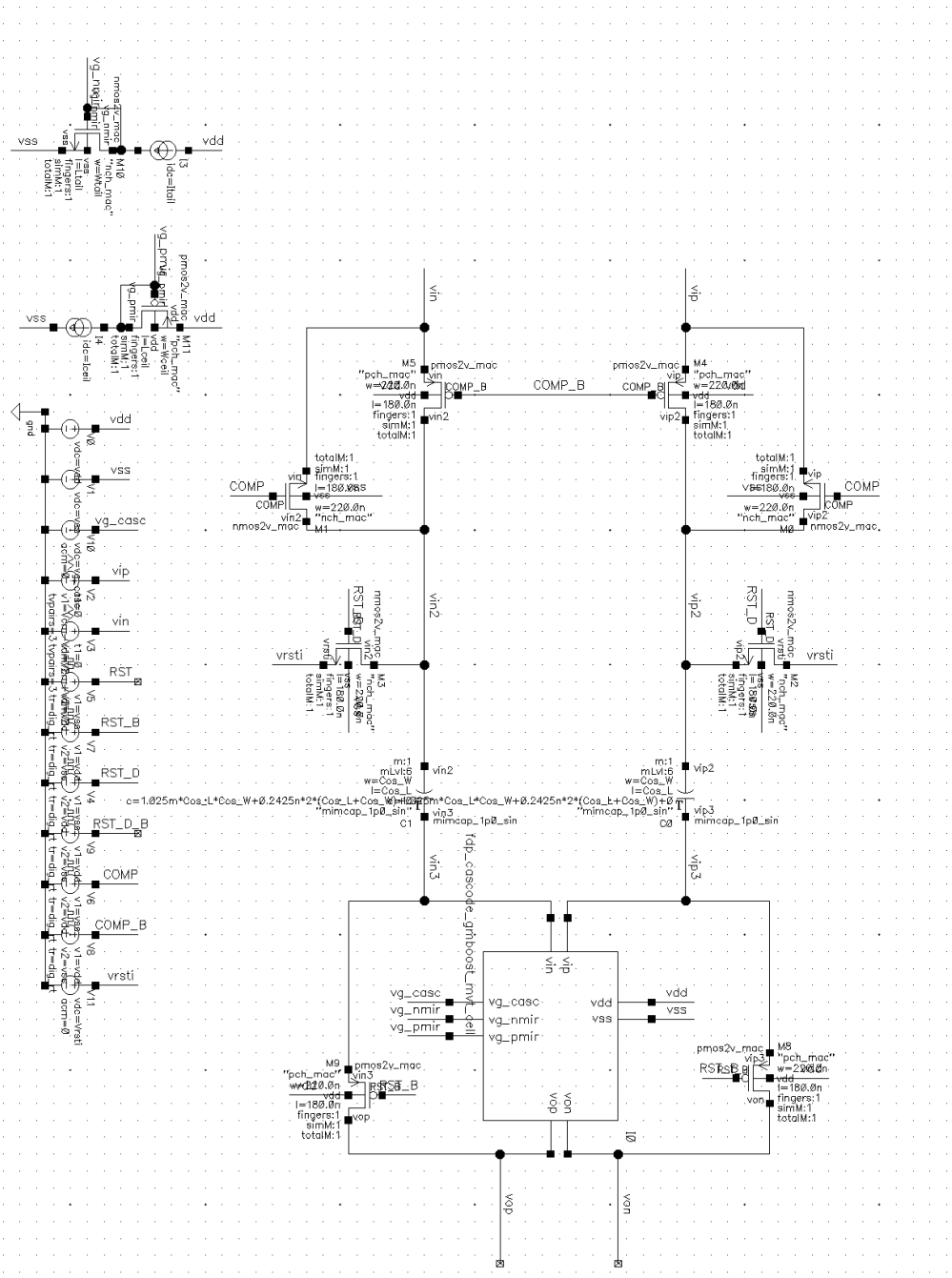


Figure A.1: Testbench to simulate IOS.

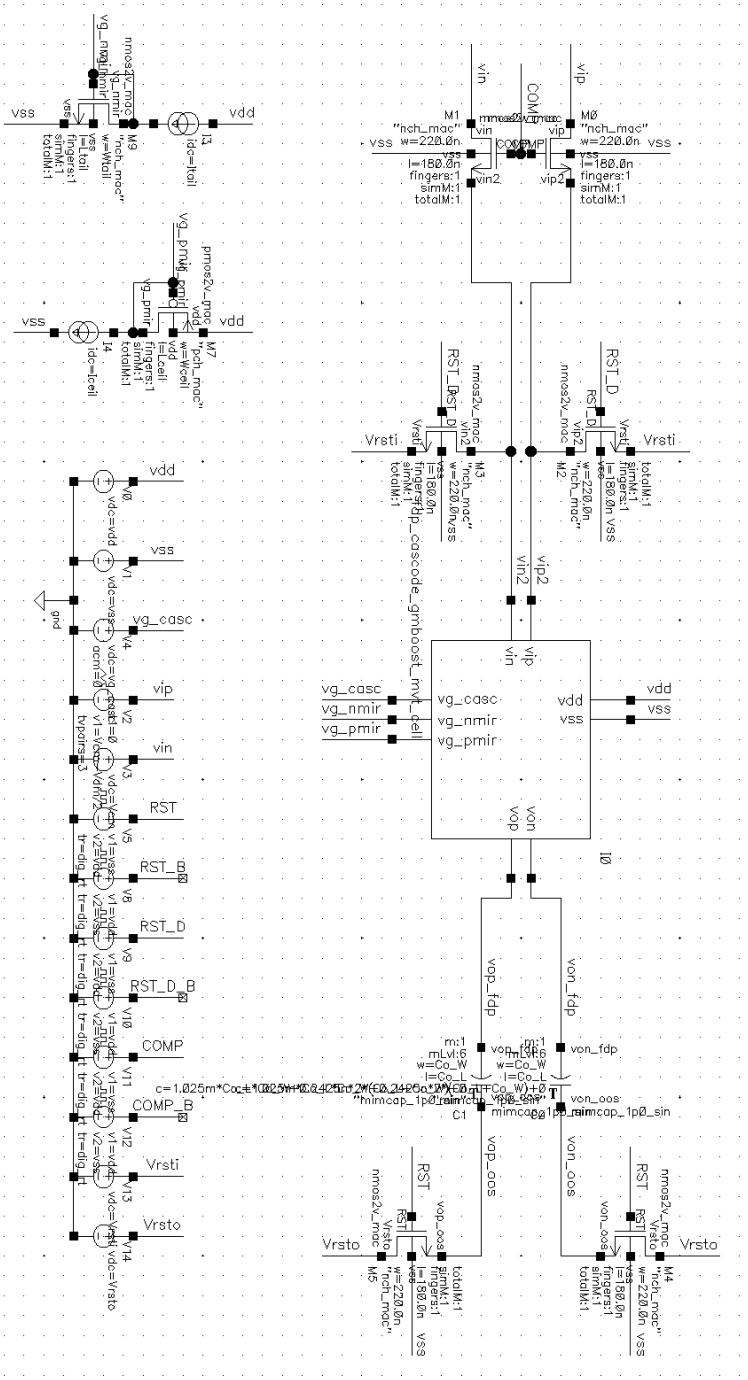


Figure A.2: Testbench to simulate OOS.

Appendix B

Pin List

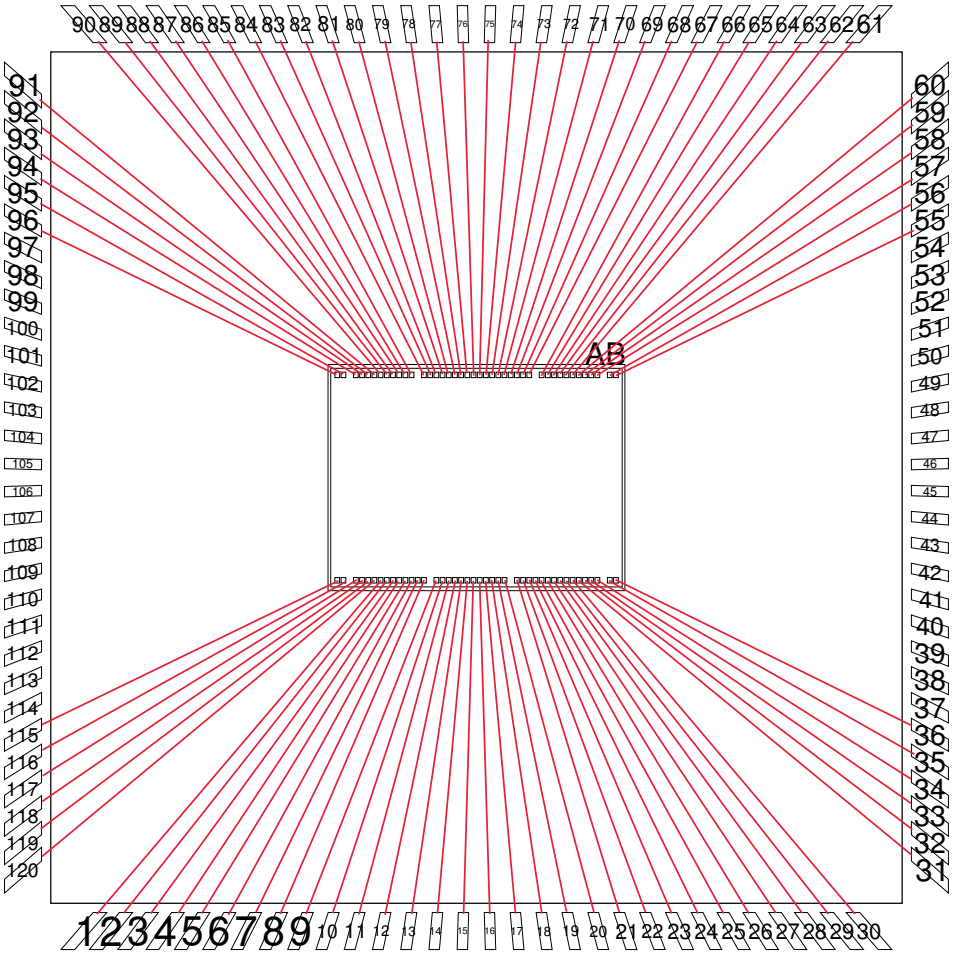
PIN	SIGNAL	ANA/DIG/PWR	I/O	NOMINAL VALUE OR RANGE
1	clk_cntr	DIG	I	5 to 50 MHz
2	cntrrst_mask	DIG	I	-
3	cntr_rd_mask	DIG	I	-
4	cntrscnchrd_se	DIG	I	-
5	cntr_en_mask	DIG	I	-
6	cntrscnchen_se	DIG	I	-
7	iovss	PWR	-	0 V
8	iovdd	PWR	-	3.3 V
9	avss	PWR	-	0 V
10	avdd	PWR	-	1.8 V
11	id_ceil2x10	ANA	I	165 µA
12	itail2x10	ANA	I	395 µA
13	pixscnch_risectrl	ANA	I	0 V
14	avss	PWR	-	0 V
15	avdd	PWR	-	1.8 V
16	pixscnch_fallctrl	ANA	I	1.8 V
17	id_tail1x10	ANA	I	254 µA
18	id_ceil1x10	ANA	I	96 µA
19	avdd	PWR	-	1.8 V
20	avss	PWR	-	0 V
21	cntrscnchrd_si	DIG	I	-
22	cntrscnchen_si	DIG	I	-
23	pixscnch_si	DIG	I	-
24	clk_pix	DIG	I	5 to 50 MHz
25	pixscnch_se	DIG	I	-
26	comp_mask_b	DIG	I	-
27	rowrst_p1_mask	DIG	I	-
28	rowrst_p0_b_mask	DIG	I	-
29	rowrst_p2_mask	DIG	I	-
30	latch_mask	DIG	I	-
31	rowrst_p0_mask	DIG	I	-
32	shiftreg_se	DIG	I	-
33	iovss	PWR	-	0 V

PIN	SIGNAL	ANA/DIG/PWR	I/O	NOMINAL VALUE OR RANGE
34	iovdd	PWR	-	3.3 V
35	dvss	PWR	-	0 V
36	dvdd	PWR	-	1.8 V
43	ase_bias	ANA	I	-
44	ase_bias	ANA	I	-
45	ase_bias	ANA	I	-
46	ase_bias	ANA	I	-
47	ase_bias	ANA	I	-
55	dvdd	PWR	-	1.8 V
56	dvss	PWR	-	0 V
57	iovdd	PWR	-	3.3 V
58	iovss	PWR	-	0 V
59	shiftreg_so0<0>	DIG	O	-
60	shiftreg_so0<1>	DIG	O	-
61	shiftreg_so0<2>	DIG	O	-
62	shiftreg_so0<3>	DIG	O	-
63	vo_prb	DIG	O	-
64	prbscnch_so	DIG	O	-
65	rst_b	DIG	I	-
66	prbscnch_se	DIG	I	-
67	avss	PWR	-	0 V
68	avdd	PWR	-	1.8 V
69	vth0	ANA	I	1 to 1.2 V
70	vrsti0	ANA	I	1.03 V
71	testpix_vinj	ANA	I	0 V
72	vop_fdp1_prb	ANA	O	-
73	von_fdp1_prb	ANA	O	-
74	vop_fdp2_prb	ANA	O	-
75	von_fdp2_prb	ANA	O	-
76	avdd	PWR	-	1.8 V
77	avss	PWR	-	0 V
78	topmetal_bias	ANA	I	1.8 V
79	vg_casc2	ANA	I	1.4 V

PIN	SIGNAL	ANA/DIG/PWR	I/O	NOMINAL VALUE OR RANGE
80	vrsti1	ANA	I	1.03 V
81	vth1	ANA	I	1 to 1.2 V
82	vg_casc1	ANA	I	1.4 V
83	avdd	PWR	-	1.8 V
84	avss	PWR	-	0 V
85	iovss	PWR	-	0 V
86	iovdd	PWR	-	3.3 V
87	probe_en_mask	DIG	I	-
88	prbscnch_si	DIG	I	-
89	shiftreg_si	DIG	I	-
90	pixscnch_so1	DIG	O	-
91	shiftreg_so1<3>	DIG	O	-
92	shiftreg_so1<2>	DIG	O	-
93	shiftreg_so1<1>	DIG	O	-
94	shiftreg_so1<0>	DIG	O	-
95	dvss	PWR	-	0 V
96	dvdd	PWR	-	1.8 V
103	ase_bias	ANA	I	-
104	ase_bias	ANA	I	-
105	ase_bias	ANA	I	-
106	ase_bias	ANA	I	-
107	ase_bias	ANA	I	-
115	dvdd	PWR	-	1.8 V
116	dvss	PWR	-	0 V
117	cntrscnchen_so1	DIG	O	-
118	cntrscnchrd_so1	DIG	O	-
119	cntrscnchrd_so0	DIG	O	-
120	cntrscnchen_so0	DIG	O	-

Appendix C

Package Bonding Diagram



Qty: 5	V67M-AB (94318)	CQFP120B
Customer Providing Diagram		
Minimum pad size: 75 x 65; minimum pad pitch: 85 um		
MOSIS	Design_name: WTMS2 - 1602CF	
	Customer Account: 244	
	Die Size: 4074 x 3104 um	
	Die Rotation in Cavity: None	
	Cavity Size: 11684 um x 11684 um	21-SEP-2016 11:55:56