Phase Shifter and LNA Design for Satellite Communication

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Phased arrays are being used in satellite communication systems in order to provide wireless data to mobile vehicles, ships and even aircrafts. This thesis focuses on the design of phase shifter, which is designed for the transmitter chain and low noise amplifier, which will be used in the receiver chain.

The phase shifter is controlled using a digital-to-analog controller. This gives rise to quantization lobes which can fail the spectrum efficiency test. Careful analysis indicates that a minimum phase resolution needed for this application is around 6-bit. This research reviews various integrated circuit phase shifter topologies to come up with one that will meet the specifications for this system. A combination of reflective-type phase shifter and switch-type phase shifter is designed using 65-nm CMOS technology to provide a full 360°phase shift range with no power consumption. The measured insertion loss is about 13.05 $\pm$ 2.75 dB at 29.75 GHz with a return loss of about 10 dB or greater.

The antenna gain-to-temperature ratio, which is a common figure of merit used in satellite communication, must be met on the receiver side of the phased array system. Through link budget analysis, it was decided that two low noise amplifiers are needed to satisfy the specified gain-to-noise ratio; one off-chip low noise amplifier that is closer to the antenna and another on-chip low noise amplifier. This alleviates the constraints on both low noise amplifiers and allows for a more simple and cost-efficient design. This research focuses on the design of the on-chip low noise amplifier using 130-nm CMOS technology. The receiver chain operates in k-band; thus, the low noise amplifier is designed at 20 GHz. A gain of about 21 dB is achieved, with an output return loss above 10 dB, a 1-dB compression point at -23 dBm and a nominal power consumption of about 6.84 mW. The simulated noise figure for this low noise amplifier design is about 3.7 dB.

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I would like to thank Mohsen for giving me the specifications for my phase shifter and for helping me understand the concept behind phased array systems. Thank-you Behrooz for giving me some insight to the world of electromagnetic theory and for sharing your enthusiasm and love for science with me. Also, I would like to thank Phil Regier for giving me so much IT support during my masters degree.

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I would like to thank C-COM Satellite Systems Inc. and NSERC for funding this project.

I would finally like to give a special thank-you to my family and friends for supporting me throughout this journey.

Dedication

This thesis is dedicated to my family. This thesis would of been dedicated to my dog but since I do not have a dog, then I would also like to dedicate this thesis to my future dog.

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Chapter 1

Introduction

1.1 Introduction to Phased Array Systems

Phased array systems have increased its popularity over the years. At first it was used during World War II in a radar system used for aircrafts. It then evolved to weather research usage, RFID systems, and space probe communication.

1.1.1 Application of Phased Array in Satellite Communication

Phased array systems are commonly used in satellite communication. One of the main benefits for satellite communication is that it enables wireless communications over very long distances. Satellite communication has the ability to provide full coverage, even in the harshest conditions, no matter where you are [12]. There are two types of phased array systems; mechanically-steered and electronically-steered.

Mechanically-steered phased arrays are antennas mounted on a pedestal that basically steers the antenna in a given direction using a beam steering algorithm.

Contrast to mechanically-steered phased arrays, electronically-steered phased arrays have fixed antennas that are evenly spaced out. The beam steering occurs due to the transmitter and receiver channel that changes the phase of each signal coming out of the antenna.

Mechanically-steered phased arrays are generally slower. They have a larger blind spot and are more susceptible to mechanical errors. Where as, an electronically-steered phased

array can quickly change the beam position and have a much better beam steering range [12].

Thus, for this application we have decided to design an electronically-steered phased array system. The focus of the thesis is the phase shifter design and the LNA design.

1.2 Importance of Phase Shifter in Phased Array Systems

A phased array is defined as a set of antennas that combine together in order to produce a desired radiation pattern. Each antenna is associated with a Rx and a Tx channel which includes a phase shifter. The relative phase of each channel is altered using the phase shifter such that the combination of channels produces a beam that can be electronically steered to a desired angle, as shown in figure 1.1 where θ is the angle of the main beam and ϕ is the phase of the phase shifter in each Tx channel.

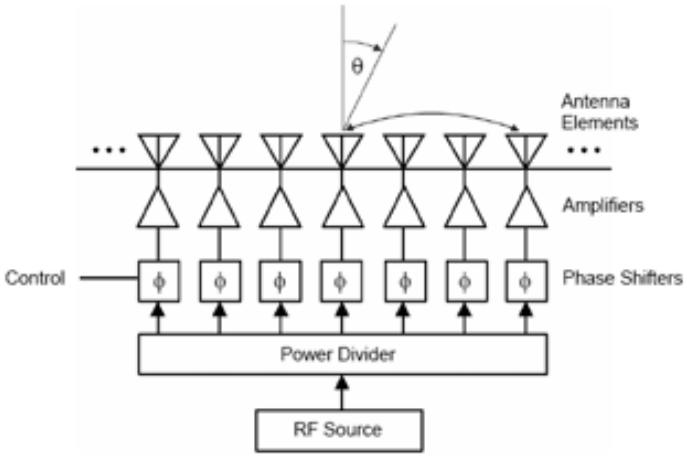


Figure 1.1: Block Diagram of an Electronically Steered Tx Phased Array [7]

An array factor is the sum of the directivity of each individual antenna to come up with the overall beam pattern of the antenna array. The array factor of the simplified horizontal isotropic antenna array is shown in equation (1.1).

$$AF(\theta_0) = \sum_{n=1}^{N} e^{j(N-n)(k_0 d \sin(\theta_0) - \Delta\phi)} \tag{1.1}$$

"N" represents the total number of antennas in the array, "n" represents the n^{th} antenna, "d" represents the distance between each antenna, k_0 represents the wavenumber, θ_0 represents the angle of the main-beam with respect to the array normal and $\Delta\phi$ represents the ideal progressive phase shift between each array element [30]. The equation for the ideal progressive phase shift is shown in equation (1.2). An illustration of how the progressive phase shift plays a role in phased array systems is shown in figure 1.2.The array factor equation becomes a bit more complex depending on the structure of the array.

$$\Delta\phi = k_0 d \sin(\theta_0) \tag{1.2}$$

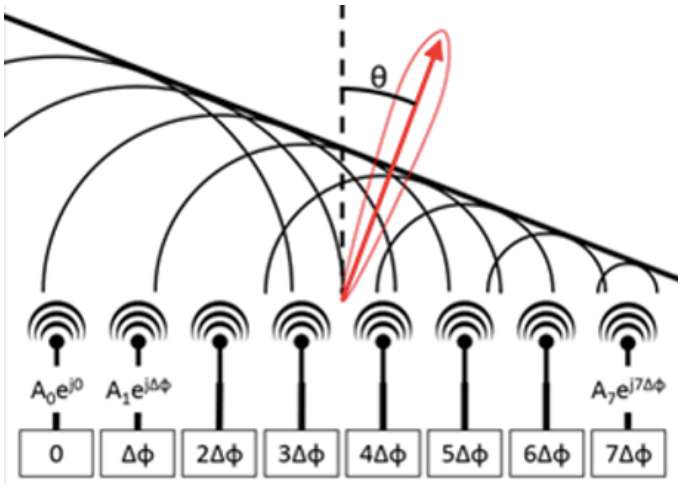


Figure 1.2: Continuous Progressive Phase Step in a Phased Array System [23]

A typical transmitter element of a phased array system is shown in figure 1.3. It consists of a PS, a VGA and a PA.

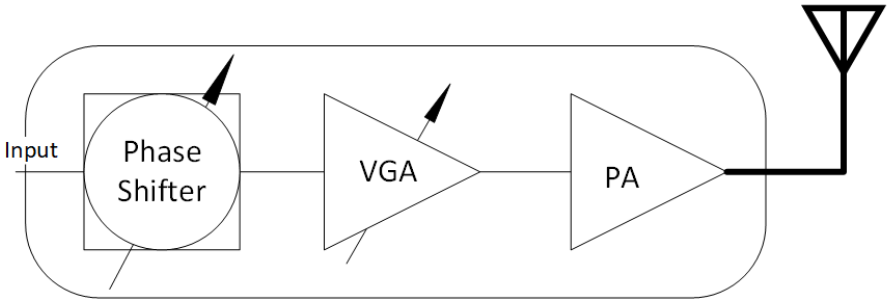


Figure 1.3: Block Diagram of a Simplified Tx Chain

Depending on the design of the transmitter chain, the VGA can be placed first before the phase shifter. The purpose of the phase shifter, as mentioned earlier, is to change the phase of the signal such that the combination of channels with different phases can steer the main beam, from the antenna array, to a desired location.

Depending on the design of the phase shifter, it may also change the amplitude of the signal which we do not have control over. That is where the VGA comes to play. The purpose of the VGA is to correct the amplitude variation in the phase shifter while also being used for pattern tapering with minimal phase variation. Amplitude tampering is commonly used in a beam-forming network to reduce the side-lobes and to widen the main beam [30].

The purpose of the power amplifier is to provide sufficient output power such that it meets the required gain-to-temperature ratio specified in order to decipher the signal correctly when received by the geostationary satellite.

1.3 Link Budget Analysis

The performance of any telecommunication system, on the receiver end, highly depends on the SNR at the receiver's input. The circuit within the receiver chain generates its own noise. However, majority of the noise comes from the antenna.

The potential contributor to the noise coming out of the antenna is the loss resistance of the antenna due to its design or its environment. In this thesis, we will mainly be focusing on thermal noise. Thermal noise is defined as the noise generated due to the random motion of electrons. Thermal noise is a function of temperature but it is independent

of frequency. In satellite communication, the sun contributes to majority of the thermal noise.

Thermal noise power present in a specific bandwidth (B) is defined in equation (1.3).

$$N = kTB(W) \tag{1.3}$$

"k" represents Boltzmann's constant and "T" represents the absolute temperature in Kelvin.

It is important to note that due to the huge distance between the geostationary satellite and the phased array antenna that sit upon moving vehicles, the electromagnetic radiation from the satellite will spread out as it propagates. If the satellite was an isotropic antenna, then flux density of the signal is defined in equation (1.4).

$$S = \frac{P_t}{4\pi r^2}(Wm^{-2}) \tag{1.4}$$

P_t represents the transmitted power of the isotropic antenna and "r" represents the distance between the transmitting antenna and the observation point. There are very few isotropic antennas in satellite communication. Majority of them send out a beam which concentrates the power in the direction of interest (usually along the bore-sight of the antenna) with a specific beam width, while reducing the power in other directions. Let G_t represent the transmitted antenna gain of the non-isotropic antenna. Therefore, the effective flux density is defined in equation (1.5).

$$S = \frac{G_t P_t}{4\pi r^2}(Wm^{-2}) \tag{1.5}$$

The receiving end of the phased array is adjusted such that it intercepts a portion of the transmitted power. The area in which the main beam of the receiving antenna intercepts with the main beam of the transmitted antenna is called the effective area. Let A_e represent the effective area and G_r represent the receivers antenna gain of the non-isotropic antenna.

$$A_e = \frac{\lambda^2}{4\pi} G_r(m^2) \tag{1.6}$$

The power received by the phased array antenna is thus:

$$P_r = A_e S = G_t P_t G_r \frac{\lambda}{4\pi r}^2 (W) \tag{1.7}$$

G_tP_t represents the EIRP and $(\frac{\lambda}{4\pi r})^2$ represents the free-space attenuation (L_{fsp}). The SNR is defined as the received signal (P_r) to noise (N) ratio. Thus, combining equation (1.3) and (1.7), we get the following equation for the SNR ratio.

$$SNR(dB) = P_r(dBW) - N(dBW) \tag{1.8}$$

$$SNR(dB) = 10log_{10}(G_tP_t) + 10log_{10}(G_r) - 20log_{10}(\frac{4\pi r}{\lambda}) - 10log_{10}(kT_{sys}B) \tag{1.9}$$

$$SNR(dB) = EIRP(dBW) + 10log_{10}(\frac{G_r}{T_{sys}}) - L_{fsp}(dB) - 10log_{10}(kB) \tag{1.10}$$

Other than free-space attenuation, there are other types of losses that needs to be considered in satellite communication, such as atmospheric losses.

$\frac{G_r}{T_{sys}}$ is the antenna gain-to-noise temperature. It is the figure of merit for satellite systems. Note that in equation (1.10), T_{sys} represents the noise temperature of the phased array system, which consists of the noise temperature of the receiver (T_{Rx}) and the antenna temperature (T_A). The antenna temperature is a parameter that is used to describe the amount of noise that an antenna (or an array of antennas) produces in a given environment.

1.4 Importance of an On-Chip and Off-Chip LNA

A 12 dB/K gain-to-temperature ratio (G/T) is required in order to successfully receive a transmitted signal from the satellite. A low noise amplifier is a circuit that amplifies the input signal while minimizing the deterioration of the SNR ratio such that the received signal can be deciphered correctly. In this work a low noise amplifier with the following specifications is targeted. In this work A 42 dBi antenna gain and a 3 dB pre-LNA loss is expected with a 15 dB post-LNA loss. The pre-LNA loss is mainly due to the feed lines from the antenna to the integrated circuit.

$$\frac{G_r}{T_{sys}}(dB/K) = G_r(dBi) - 10 * log_{10}(T_{sys}) \tag{1.11}$$

$$12(dB/K) = 42dBi - 10 * log_{10}(T_{sys}) \tag{1.12}$$

$$10 * log_{10}(T_{sys}) = 42dBi - 12dB/K \tag{1.13}$$

$$T_{sys} = 10^3K \tag{1.14}$$

As mentioned in the previous section, the system noise temperature (T_{sys}) consists of the antenna temperature and the noise temperature of the receiver. Note that the system noise temperature reference plane is right in front of the receiver, as shown in figure 1.4.

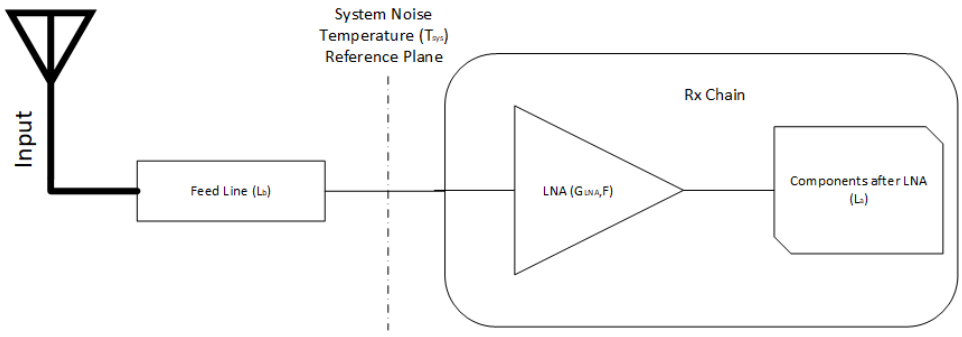


Figure 1.4: Block Diagram of a Simplified Rx Chain

Thus, the equation for the system noise temperature is shown in equation (1.16). Assuming that the antenna temperature is equivalent to the standardized room temperature (290 K), then by substituting equation (1.14) into equation (1.16) the receiver noise temperature is 710 K. "T_o" represents the standardized room temperature. Thus by substituting the values above, the equivalent noise factor of the receiver chain (F_{eq}) is about 3.45 W/W.

$$T_{sys} = T_a + T_{Rx} \tag{1.15}$$
$$T_{Rx} = T_o * (F_{eq} - 1) \tag{1.16}$$
$$\tag{1.17}$$

As per simulation and measurement, the approximate loss between the antenna and the receiver (L_b) is around 3 dB. The estimated loss after the LNA (L_a) is about 15 dB. According to Friis equation, the gain of the LNA has to be high enough to suppress the high noise figure (loss) after the LNA. The estimated gain needed to suppress the high noise figure after the LNA is about 27 dB.

The equation shown in (1.18) is in linear scale. Substituting the linear scale values in table 1.1 to equation (1.18), we can calculate the required noise figure of the LNA (F).

Table 1.1: Receiver Chain Specifications

Symbol	***Value in Logarithmic Scale (dB)***	***Value in Linear Scale (W/W)***
F_{eq}	5.38	3.45
L_b	3.00	2.00
L_a	15.0	31.6
G_{LNA}	27.0	501

$$F_{eq} = L_b + L_b(F-1) + \frac{L_b}{G_{LNA}}(L_a - 1) \tag{1.18}$$

The required noise figure for the LNA is about 2.22 dB. The frequency band for the receiving antenna in the phased array system is from 19 GHz to 21 GHz (k-band).

There are many factors that comes into play when choosing the technology for the LNA design, such as; minimum possible noise figure (F_{min}), gain, power dissipation, 1dB compression point (P_{1dB}) and cost.

Selecting the technology is the first and most important step in designing a LNA. The transistor technology selected should meet the lowest possible power consumption and cost while meeting the gain, noise figure and 1 dB compression point specifications.

CMOS, SiGe BiCMOS and InP HBT are common technologies used to design IC circuits in the k-band frequencies. CMOS technologies are more favorable due to its low cost and maturity. However, SiGe BiCMOS and InP HBT generally have much better noise figure and higher gain (due to its high transition frequency and maximum power gain frequency).f_T is defined as the transition frequency in which the current gain of the transistor falls to unity. If the transistor is operating any higher than this frequency, then it behaves more like a passive device than as an amplifier. f_T is also coined as the gain bandwidth product.

Figure 1.5 shows how f_T increases as the CMOS technology scales down. It also shows how IBM SiGe BiCMOS, HBT and other BiCMOS technologies have a higher f_T compared to CMOS. However, SiGe BiCMOS is more expensive compared to CMOS for the same minimum length of the transistor.

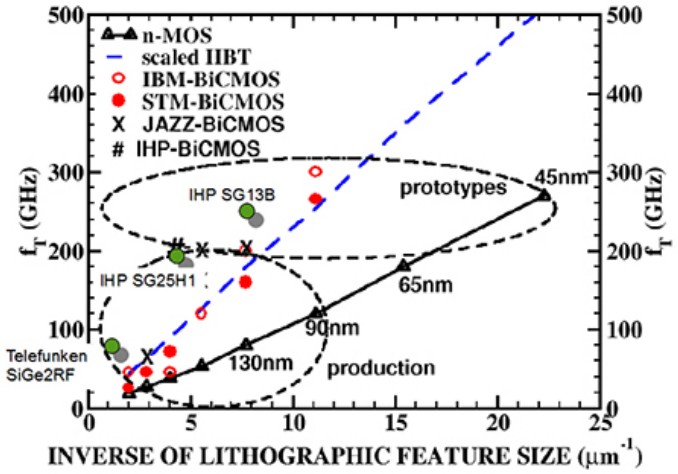


Figure 1.5: Comparison of CMOS and SiGe-HBT technologies with respect to f_T [2]

As you can see in figure 1.6, CMOS technologies generally have a much higher noise figure compared to SiGe-HBT, especially at k-band.

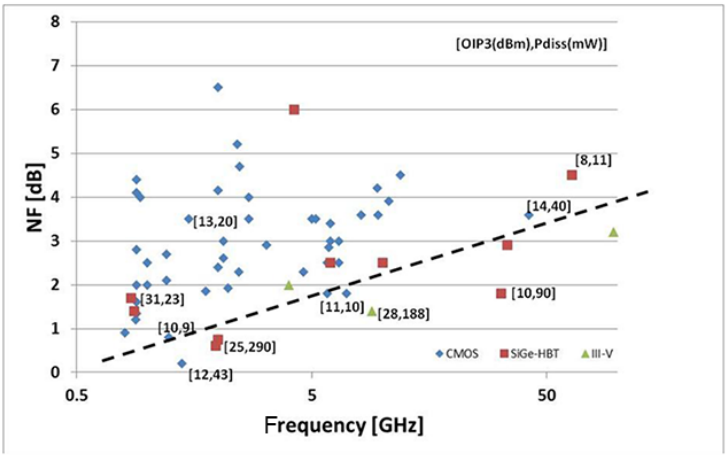


Figure 1.6: Noise Figure vs. Frequency for LNAs reported in recent papers [17]

In order to meet the 2.22 dB noise figure and at least 27 dB gain, we need to use a more expensive technology such as SiGe-HBT. However, this will increase the cost of the phased-array system especially if the whole receiver chain is designed with that technology.

Another approach is to design a LNA closer to antenna using a more exotic technology, such as SiGe-HBT. And then design the whole receiver chain which includes another LNA using a cheaper technology such as CMOS IBM 130nm. Figure X illustrates this concept.

Thus, the total noise figure of the LNA and effective gain of the LNA are are shown in equation (1.19) and (1.20) respectively.

$$F = F_{off-chipLNA} + \frac{L_{intermediate} - 1}{G_{off-chipLNA}} + \frac{F_{on-chipLNA} - 1}{G_{off-chipLNA}} L_{intermediate} \tag{1.19}$$

$$G_{LNA}(dB) = G_{off-chipLNA} + L_{intermediate} + G_{on-chipLNA} \tag{1.20}$$

1.5 Objective of Thesis

The objective of this thesis is to design two key circuit components needed in this phased array project. The first is to design a phase shifter that provides a full phase shift range and that can provide the phase resolution that is needed in this project without consuming a lot of power. The second objective of this thesis is to design a simple and cost-efficient on-chip low noise amplifier.

1.6 Thesis Outline

This thesis is organized into 5 chapters and is devoted to phase shifter design followed by a simple on-chip LNA design for phased array systems in satellite communication.

The first chapter is an introduction and it outlines the application of phased array systems. Followed by the importance of a phase shifter and a low noise amplifier in a phased array system. This section also does link budget analysis to justify why two low noise amplifiers are needed for this project; one on-chip and another off-chip low noise amplifier.

The second chapter goes over the effect of phase quantization and why this project needs a high resolution. Followed by the specifications of the phase shifter for this project. Furthermore, this chapter goes over the advantage and disadvantages of the top four phase shifter integrated circuit topologies used in phased array systems.

The third chapter will reveal the theory and design of the selected phase shifter topology, along with the simulation and measurement results.

The fourth chapter will go over the design and analysis of a simple on-chip low noise amplifier.

Finally, the fifth chapter will conclude and indicate future improvements to the phase shifter. Followed by, next steps in the design of the low noise amplifier.

Chapter 2

Phase Shifter Architectures - Literature Review

As mentioned in Chapter 1, phase shifters are important in phased-array systems in order to steer the signal beam. It is essential for the phased array system to meet the radiation masks for all beam-scanning angles imposed by ka-band satellite communication standards while operating in Tx mode. Thus, it is essential to see how the phase shifter effects the radiation pattern of the phased array system.

2.1 Effects of Phase Quantization

As shown in equation (1.1), the progressive phase shift between adjacent array elements is $\Delta\phi$. Ideally, the progressive phase shift will be $\Delta\phi = k_0 d \sin(\theta_0)$ in order to prevent any significant side lobes from occurring.

Most phase shifters are digitally controlled using a M-bit digital-to-analog converter (DAC), which has about 2^M phase states. Assuming that the phase shift is linear across the controlled input, then the progressive phase step is the following:

$$\Delta\phi_S = \frac{2\pi}{2^M} \tag{2.1}$$

Figure 2.1 shows the 3-bits quantized phase shift (red line) in comparison to the ideal linear phase shift (blue line). As you can see, each phase in the linear phase shifter is

rounded to the nearest quantized phase. This produces quantization errors. This quantization error depends on the resolution of the phase shifter, which is about $\pm\frac{\Delta\theta_S}{2}$. For a 3-bit phase shifter, the progressive phase step is 45°. Thus, the phase quantization error is ±22.5°, as shown in figure 2.2.

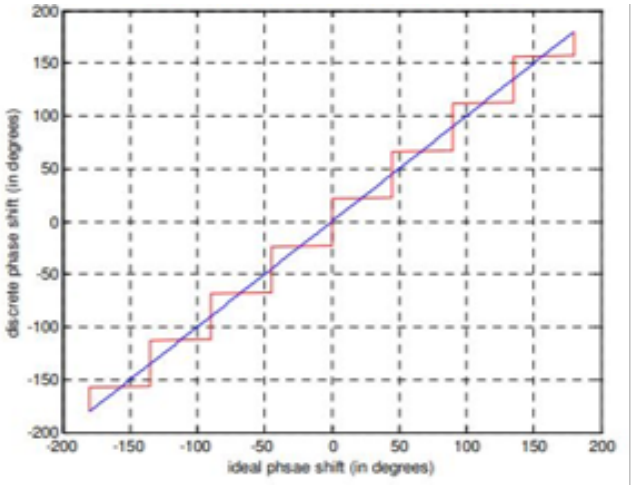


Figure 2.1: Quantized 3-bit Progressive Phase Step in a Phased Array System [27]

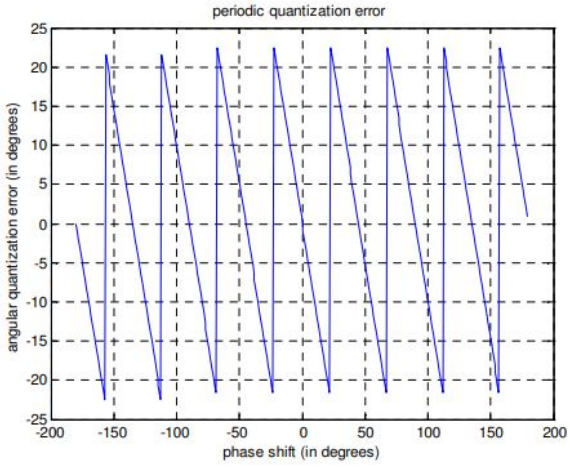


Figure 2.2: Periodic Quantization Error with a 3-bit DAC [27]

This phase quantization error produces significant side lobes commonly known as quantization lobes (QLs). These quantization lobes can be modeled with a predictable power

level and angle when the number of elements in the array is greater than the number of phase steps. For this application, there are about 4000 elements in the phased array system. The resolution of the DAC that are used in products is a 10-bit DAC. Thus, there are more than one element per phase step. The number of elements in each phase step is shown in equation (2.2) [10].

$$J = \frac{N}{(N-1)2^M(\frac{d}{\lambda})\sin(\theta_0)} \tag{2.2}$$

Thus, the M-bit quantized phase state in the N-elements phased array can be broken down to m sub-arrays each with J elements where the quantized phase state is defined for each sub-array instead of each channel in the array. This phenomenon is what causes quantization lobes. An illustration of this is shown in figure 2.3.

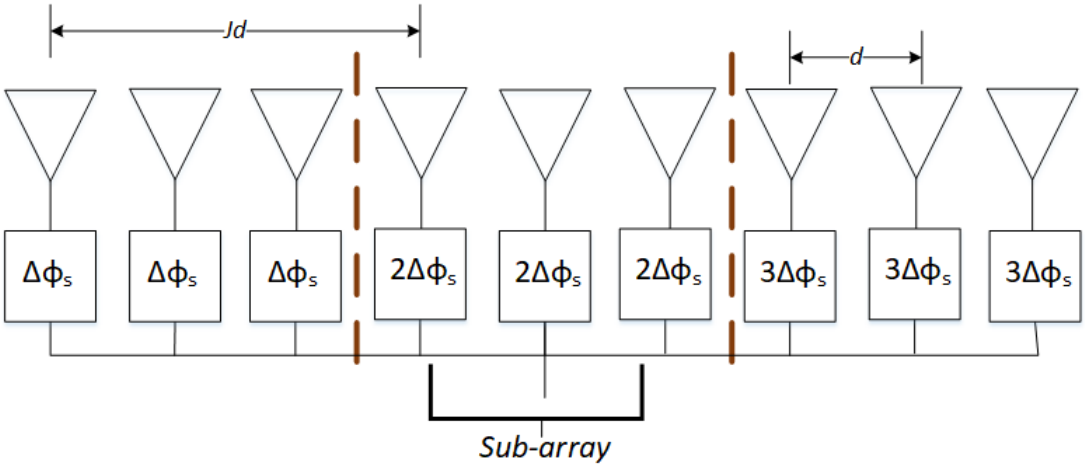


Figure 2.3: Quantization Block Diagram of a Phased Array System

Thus, the pattern of the phased array can be broken down to an array pattern of J elements (f_J) multiplied by the array factor of m sub-arrays (AF_m) [20].

$$AF(\theta_0) = (AF_m)(f_J) \tag{2.3}$$

$$AF(\theta_0) = \left(\frac{1}{m}\sum_{q=-\frac{m-1}{2}}^{\frac{m-1}{2}} w_q e^{jq(\frac{2\pi Jd}{\lambda}\sin(\theta_0)-\Delta\phi)}\right) * \left(\frac{1}{J}\sum_{i=-\frac{J-1}{2}}^{\frac{J-1}{2}} e^{j(\frac{2\pi d*i}{\lambda}\sin(\theta_0)-q*\Delta\phi_s)}\right) \tag{2.4}$$

The equation for beam angles in a phased array system is shown in equation (2.5), where r and m represent integers. When r=0 and z=0, that represents the angle of the main beam [25]. When r $\neq$ 0, that represents the angles of the unwanted grating lobes and when z $\neq$ 0, then that determines the angles of the unwanted quantization lobes.

$$\theta_{rz} = \arcsin\left(\frac{\lambda r}{d} + (1 + \frac{2\pi}{\Delta\phi_s} z)\sin(\theta_0)\right) \tag{2.5}$$

The general expression for the power located at the p^{th} quantization lobe (r = 0 and z $\neq$ 0) is written in equation (2.6) [21].

$$QL_{dB} = envelope(dB) + 20\log(\frac{\pi}{2^{2M}}) \tag{2.6}$$

$$envelope(dB) = -20\log(J\sin(p'\frac{\pi}{J})) \tag{2.7}$$

$$p' = p + \frac{1}{2^M} \tag{2.8}$$

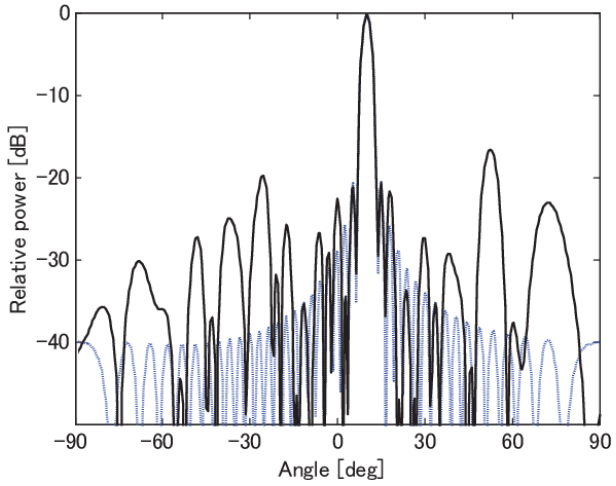


Figure 2.4: Spectrum Efficiency of the Phased Array System with an Ideal Phase Shifter vs. a Quantized Phase Shifter [14]

As you can see in figure 2.4, assuming the phase shift is linear with respect to the control voltages a simulation of the radiation pattern with a quantized phase shifter (shown in the

black line) is compared with that of the ideal phase shifter (shown with a blue line). As you can see, the radiation pattern with the quantized phase shifter produced significant side lobes. Through simulation it was determined that a resolution of about 6-bit or greater is required in order to comply with the specified FCC mask for this project. In other words, the phase shifter needs to have a progressive phase step of about 5.625°.

2.2 Requirements

The following design requirements and constraints have to be considered for the design of the phase shifter in phased array applications.

The phase shifter must have the full phase control range (full 360 °). There should be no significant blind spots where the phase shifter cannot reach the required phase range. Theoretically, analog phase shifters have infinite precision, assuming that there is no blind spots and that it has the full 360 degree phase shift; therefore, there phase resolution is really high. In practice, digital-to-analog converters are needed to control the analog phase shifter and that has its own corresponding resolution.

Insertion loss and insertion loss variation needs to be considered. If the insertion loss variation is high that puts a lot of constraint on the VGA and requires a more complex design with a high dynamic range and low phase variation. If the insertion loss is high that requires a higher gain from the VGA and the PA.

For active phase shifters, 1-dB compression point (P_{1dB}) and third order intercept points at the input (IIP_3) needs to be considered.

Finally, power consumption, chip size and cost of the design needs to be considered.

The constraints listed above is what makes designing a phase shifter challenging. Depending on the topology, increasing the phase shift range can ultimately increase the insertion loss variation or the cost of the chip. There are trade-offs when designing the phase shifter. It ultimately depends on the phased array system requirements. The phase shifter specifications for this application is shown in table 2.1.

Table 2.1: Phase Shifter Specifications

Parameter	***Units***	***Value***
Bandwidth	GHz	28 - 30
Phase Shift Range	°	360
Power Consumption	mA	* as small as possible *
Input and Output Return Loss	dB	>10
Insertion Loss	dB	<10
Insertion Loss Variation	dB	± 3
Progressive Phase Step	°	≤ 5.625

2.3 Topologies

A variety of fully integrated passive and active phase shifter circuits have been designed to meet various specifications. The pros and cons of each design are discussed below.

2.3.1 Digital Phase Shifter

Instead of using a complex high resolution DAC, digital switched type phase shifters require a control voltage that has only 2 states; a high state (i.e. 1 V) and a low state (i.e. 0 V) as shown in figure 2.5. The concept behind a switched type phase shifter is to provide a different phase path for each controlled voltage. The number of bits in the switched type phase shifter is equivalent to the number of controlled voltages.

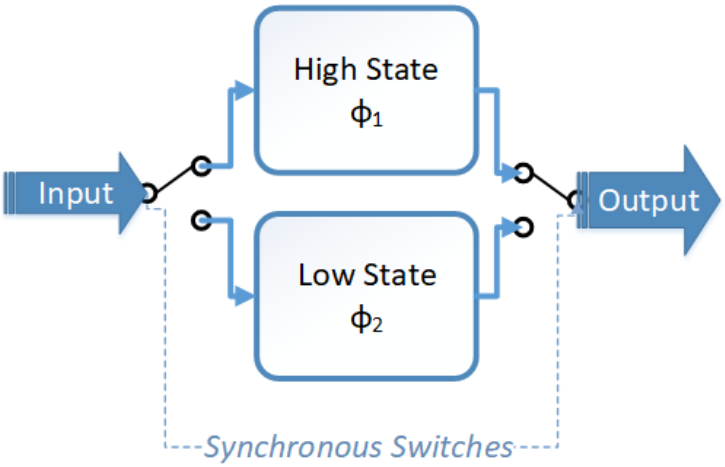


Figure 2.5: Generalized Schematic Diagram of a Switch Type Phase Shifter

True Time-Delay Type Phase Shifter

The individual phases can be implemented using different time delays (this type of phase shifter is called a true time-delay type phase shifter). These delays can be realized with transmission lines.

A conventional time-delay type phase shifter consists of two transmission line segments with different lengths.

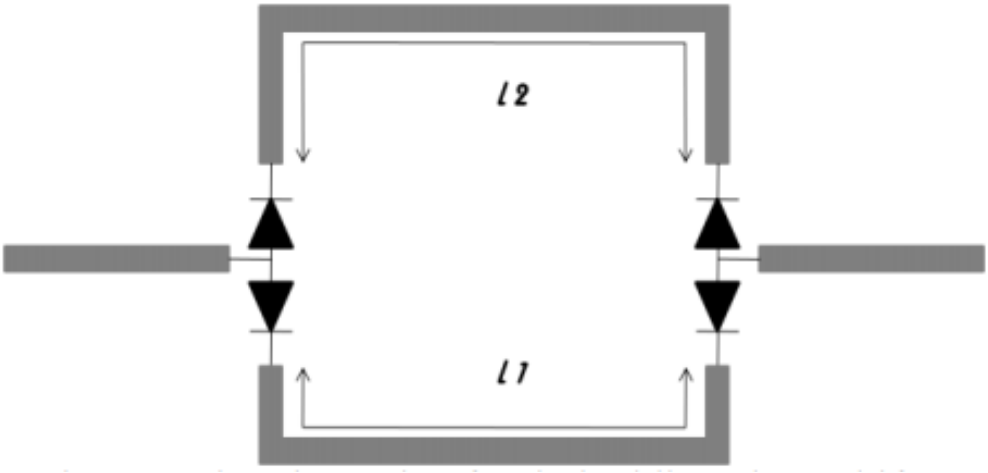


Figure 2.6: Schematic of a True Time-Delay Type Phase Shifter [3]

As you can see in figure 2.6, the true-time delay type phase shifter has a differential phase shift shown in equation (2.9) where β is the propagation constant of the transmission.

$$\Delta\theta = \beta(l_2 - l_1) \tag{2.9}$$

An important advantage to this type of phase shifter is that it is that if the transmission line is operating in TEM or quasi-TEM mode, then the phase shift is linear across a very wide frequency range.

However, the insertion loss of this phase shifter is dependent on the length of the transmission line, which has unequal lengths in its path. Hence, there will be a significant insertion loss variation between the two states. Also, a really long transmission line is needed to realize large time delays.

A more compact solution would be to design a high-pass low-pass phase shifter.

High-Pass Low-Pass Type Phase Shifter

A more compact solution is to use high-pass low-pass phase shifter, since it uses lumped components to achieve the phase shift instead of a transmission line, and its low insertion loss variation. This type of phase shifter is also known as a switch-type phase shifter (STPS).

These high-pass low-pass filters are designed for a linear phase response. The circuit design for these filters are shown in the figures below. The equations for the lumped components are also shown below [9].

These 3-element lumped component filters can create a phase shift $-90° \leq \theta \leq 90°$ at center frequency ω_0 and characteristic impedance Z_0.

$-90° \leq \theta < 0°$:

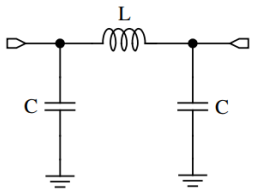


Figure 2.7: Low-Pass $\prod$ Filter

$$L = \frac{Z_0 \sin|\theta|}{\omega_0} \tag{2.10}$$

$$C = \frac{\tan|\frac{\theta}{2}|}{Z_0\omega_0} \tag{2.11}$$

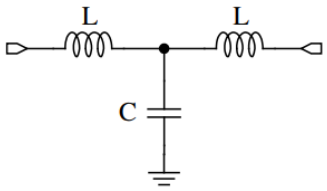


Figure 2.8: Low-Pass $\boldsymbol{T}$ Filter

$$L = \frac{Z_0 \tan|\frac{\theta}{2}|}{\omega_0} \tag{2.12}$$

$$C = \frac{\sin|\theta|}{Z_0\omega_0} \tag{2.13}$$

$0° < \theta \leq 90°$:

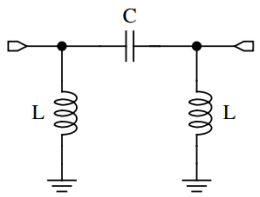


Figure 2.9: High-Pass $\prod$ Filter

$$L = \frac{Z_0}{\omega_0 \tan|\frac{\theta}{2}|} \tag{2.14}$$

$$C = \frac{1}{Z_0 \omega_0 \sin|\theta|} \tag{2.15}$$

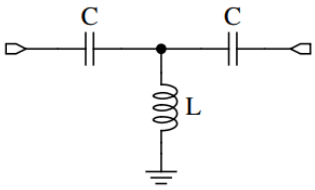


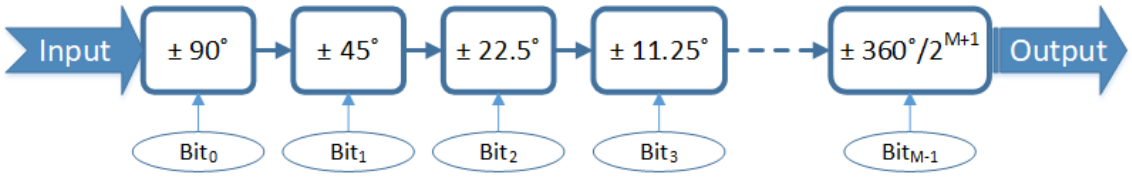
Figure 2.10: High-Pass $\boldsymbol{T}$ Filter

$$L = \frac{Z_0}{\omega_0 \sin|\theta|} \tag{2.16}$$

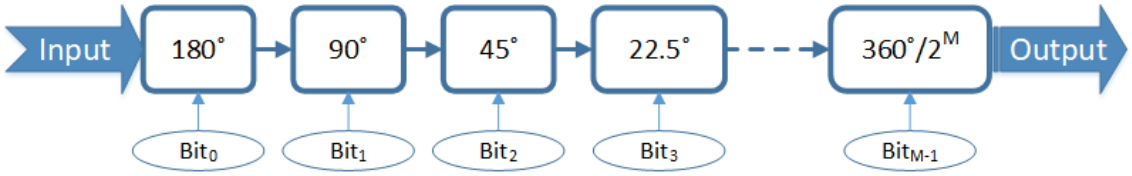
$$C = \frac{1}{Z_0 \omega_0 \tan|\frac{\theta}{2}|} \tag{2.17}$$

The $\prod$ and the $\boldsymbol{T}$ networks have a broadband characteristic. However, the high-pass low-pass phase shifter requires the design of a switch with high isolation and low insertion loss.

The high-pass low-pass phase shifter can be cascaded together to provide the necessary phase resolution needed, as shown in figure 2.11.



(a) Absolute Phase of Each State



(b) Relative Phase of the High State compared to it's Low State for Each Stage

Figure 2.11: Block Diagram of M-bit Digital High-Pass Low-Pass Type Phase Shifter

Equation (2.18) shows the calculation for the total phase shift. This can be easily programmed using a micro-controller.

$$\Delta\theta = 180^\circ \times Bit_0 + 90^\circ \times Bit_1 + 45^\circ \times Bit_2 + 22.5^\circ \times Bit_3 + ... + \frac{360^\circ}{2^M} \times Bit_{M-1} \quad (2.18)$$

The downfall to the cascaded high-pass low-pass phase shifter approach is that the insertion loss of each stage accumulates resulting in a very high insertion loss. Furthermore, it is extremely difficult to implement a high-pass low-pass phase shifter that requires a resolution greater than 5-bit. The inductance and capacitance needed to design a high resolution low-pass will be very small and almost equivalent to the parasitic inductance and capacitance, especially at ka-band. Likewise, the lumped components needed to design the high-pass filter will be extremely large in which case it will be very costly to implement that stage.

For an example, say we were to design a a 6-bit high-pass low-ass phase shifter and we are designing the very last stage. Say we were to design a high-pass $\boldsymbol{T}$ filter and a low-pass $\prod$ filter for that stage, where $\theta = \pm\frac{360^\circ}{2^{6+1}} = \pm 2.8125^\circ$. Let $f_0 = 30$ GHz and $Z_0 = 50\ \Omega$.

Thus, using equations (2.16) and (2.17) the value of the lumped components in the high-pass filter are L = 5.2 nH and C = 4.3 pF. The values for the lumped components are very large and will take up a great deal of space to design this filter.

For the low-pass filter, using equations (2.10) and (2.11) the value of the lumped components are L = 13.0 pH and C = 2.6 fF. The values of these lumped components are very small, which means that this low-pass network is very sensitive to parasitics.

2.3.2 Continuous Phase Shifter

Continuous phase shifters are ideal for applications that require a high-resolution progressive phase shit. These phase shifters can be controlled using a DAC. The two most common continuous IC phase shifters are the vector-sum phase shifter and the reflective-type phase shifter.

Vector-Sum Phase Shifter

The vector-sum phase shifter, also known as the vector modulator, takes the input signal and divides it into two with equal amplitude and a 90° offset (in-phase and quadrature signal). The amplitude of these two signals are then altered using VGAs and then combined to provide the necessary phase shift. The block diagram of the vector-sum phase shifter is shown in figure 2.12.

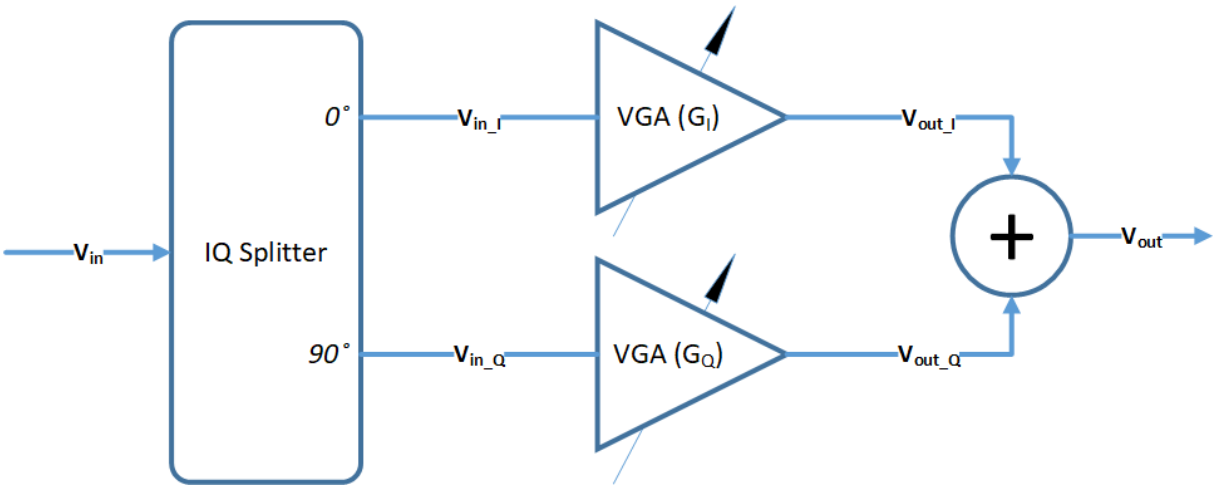


Figure 2.12: Block Diagram of Vector-Sum Phase Shifter

An analysis of the vector modulator is shown below. The signals along the back of the phase shifter, shown in figure 2.12, are represented using phasor notations. The VGAs in the phase shifter are assumed to have a dynamic gain from [-A,A].

Assuming that the input signal is:

$$\boldsymbol{V_{in}} = V_{in}\angle 0^\circ \tag{2.19}$$

Then, the in-phase and quadrature signal after the IQ splitter are:

$$\boldsymbol{V_{in_I}} = \frac{V_{in}}{\sqrt{2}}\angle 0^\circ \tag{2.20}$$

$$\boldsymbol{V_{in_Q}} = \frac{V_{in}}{\sqrt{2}}\angle -90^\circ \tag{2.21}$$

As indicated in figure 2.12, the gain of the in-phase and quadrature VGAs is G_I and G_Q respectively. Thus, the output signal of the vector-sum phase shifter is:

$$\boldsymbol{V_{out_I}} = \boldsymbol{G_I V_{in_I} V_{out_I}} = G_I\angle\theta_I \frac{V_{in}}{\sqrt{2}}\angle 0^\circ \tag{2.22}$$

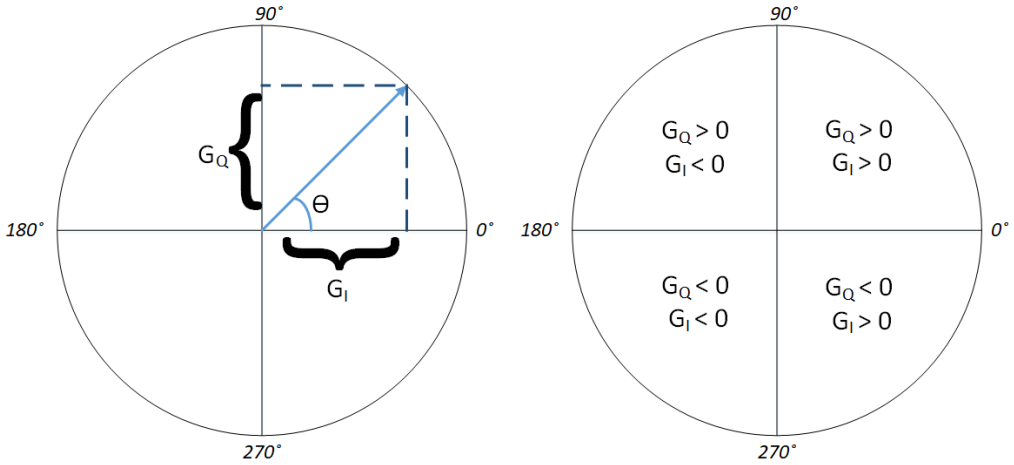
$$\boldsymbol{V_{out_Q}} = \boldsymbol{G_Q V_{in_I}}^\circ \boldsymbol{V_{out_Q}} = G_Q\angle\theta_Q \frac{V_{in}}{\sqrt{2}}\angle -90^\circ \tag{2.23}$$

$$\boldsymbol{V_{out}} = \boldsymbol{V_{out_I}} + \boldsymbol{V_{out_Q}} \boldsymbol{V_{out}} = \frac{V_{in}}{\sqrt{2}}\Big(G_I\angle\theta_I + G_Q\angle(-90^\circ + \theta_Q)\Big) \tag{2.24}$$

$$|\boldsymbol{V_{out}}| = \frac{V_{in}}{\sqrt{2}}\sqrt{\Big(G_I\cos(\theta_I) + G_Q\cos(-90^\circ + \theta_Q)\Big)^2 + \Big(G_I\sin(\theta_I) + G_Q\sin(-90^\circ + \theta_Q)\Big)^2} \tag{2.25}$$

$$\angle\boldsymbol{V_{out}} = \arctan\Big[\frac{G_I\sin(\theta_I) + G_Q\sin(-90^\circ + \theta_Q)}{G_I\cos(\theta_I) + G_Q\cos(-90^\circ + \theta_Q}\Big] \tag{2.26}$$

In order to get the full 360°phase shift, as you can see in figure 2.13, the ideal angle for the in-phase and quadrature signal after the VGA would be $\theta_I = 0° \; or \; 180°$ and $\theta_Q = 0° \; or \; 180°$.



(a) IQ Phase Vector Diagram

(b) Quadrant Selection Based on the Sign of the Gain of the VGA

Figure 2.13: Vector-Sum Phase Shifter Vector Diagram Analysis

Thus, equations (2.25) and (2.26) can be simpified to:

$$|\boldsymbol{V_{out}}| = \frac{V_{in}}{\sqrt{2}}\sqrt{(G_I)^2 + (G_Q)^2} \tag{2.27}$$

$$\angle \boldsymbol{V_{out}} = \arctan\left[\frac{G_Q \sin(-90° + \theta_Q)}{G_I \cos(\theta_I)}\right] \tag{2.28}$$

The advantages of the vector-sum phase shifter is that it can give you gain and phase control. However, at ka-band we will most likely be getting an insertion loss instead of a gain. One of the main disadvantages to the vector-sum phase shifter is due to the fact that the design gives rise to significant non-linearities.

The IQ splitter can have amplitude and phase imbalance. However, the VGAs gives rise to non-linearities where the phase of the VGA can vary significantly as the gain changes. This makes the calibration process a lot more complicated [16].

Ideally, the constellation diagram of the vector-sum phase shifter will be circular. However, due to the amplitude and phase imbalance in the VGAs, the resulting constellation would be rectangular with curled sides as shown in figure 2.14.

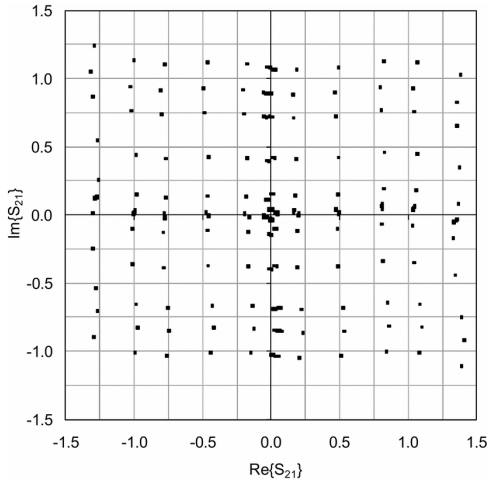


Figure 2.14: Measured Constellation of the Vector-Sum Phase Shifter (S_{21}) [13]

Thus, a massive look-up table is required to provide the necessary gain and phase of the vector modulator. The calibration is a two step process, where the first step is to linearly sweep the controlled voltages of the VGA to come up with a constellation diagram like figure 2.14. The second step of the calibration algorithm requires defining gain circles and then coming up with an intensive iterative technique to locate the precise controlled voltages for the VGAs [11].

Reflection Type Phase Shifter

The reflective type phase shifter (RTPS) is a passive design that can provide 360° phase shift range. A typical block diagram of a RTPS is shown in figure 2.15.

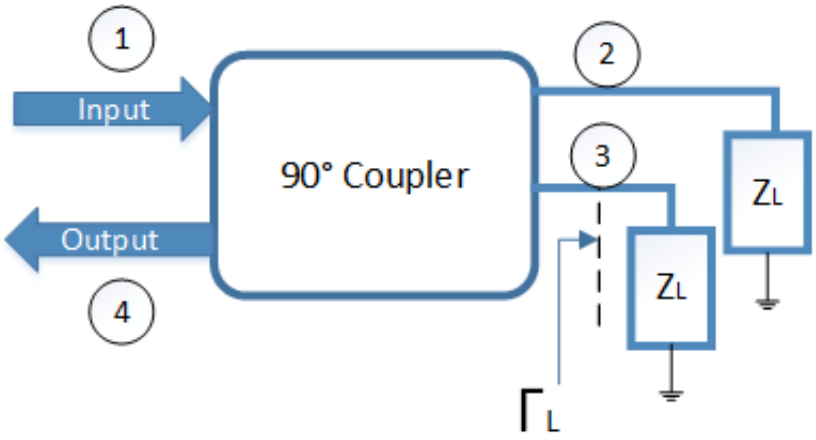


Figure 2.15: General block diagram of a Reflective Type Phase Shifter

The phase shift of the reflective-type phase shifter can be altered by varying the load impedance (Z_L). Varactors with various load topologies are used to achieve a full phase-shift range.

The limited tune-ability of the varactor and the quality factor of the lumped components limits the phase shift range and provides a high insertion loss. However, this design is simple to calibrate and it does not consume any power.

2.3.3 Summary of Phase Shifter Topologies

The advantages and disadvantages of the various phase shifter designs are summarized in tables 2.2 and 2.3 [6].

Table 2.2: Typical Performance of Common Phase Shifter Designs

Type of Phase Shifter	***Power Consumption***	***Resolution***	***IL Variation***	***Size***
True Time-Delay	~0	Limited by number of stages	Large	Large
High-Pass Low-Pass	~0	Limited by number of stages	Medium	Medium
Vector-Sum	Medium	Continuous - limited by DAC	Medium	Medium
Reflective	~0	Continuous - limited by DAC	Small to Medium	Small

Table 2.3: Other Advantages and Disadvantages of Common Phase Shifter Designs

Type of Phase Shifter	***Other Advantages***	***Other Disadvantages***
True Time-Delay	Linear phase shift over a very wide frequency range. Very simple calibration procedure.	
High-Pass Low-Pass	Very simple calibration procedure.	Very high insertion loss. Unreasonable values for lumped components for a smaller progressive phase step.
Vector-Sum	Amplitude and phase control.	Significant non-linearities results in a more complex calibration procedure.
Reflective	Simple Calibration Procedure.	Phase shift range and insertion loss limited by the tuneable load.

Chapter 3

Analysis and Design of Phase Shifter

3.1 Choice of Phase Shifter Topology

A coupler-based analog reflective type phase shifter was chosen for this phased array project due to its very low power consumption, capability of achieving a high phase resolution, compact size and ease of calibration compared to a vector-sum phase shifter.

As mentioned in the literature review, the challenges with the reflective type phase shifter is the insertion loss (IL) variation over phase, which will affect the radiation pattern of the antenna array. Another way to compensate for the insertion loss variation is to implement a variable gain amplifier.

3.2 Theory

The general block diagram of a reflective-type phase shifter is shown in 2.15.

Let Z_L represent the tunable load impedance, and Γ_L represent the reflection looking into that load.

The diagram in 2.15, displays a traditional 3 dB 90° coupler, in which port 1 is the input, the isolation port 4 is the output, and the through and coupled ports are ports 2 and 3 respectively. The s-parameters of 3-dB 90° coupler is shown in 3.1.

$$[S] = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix}$$

Figure 3.1: S-parameters of a 3-dB 90° coupler

By taking the general s-parameters of a 3-dB 90° coupler and the reflection of the two loads, we can deduce the overall s-parameters of the RTPS topology. The following power wave analogy is with respect to that of the hybrid coupler; thus, the output power waves (b) points away from the hybrid coupler and the input power waves (a) points towards the hybrid coupler.

$$b_1 = -(1/\sqrt{2})(j * a_2 + a_3) \tag{3.1}$$
$$b_4 = -(1/\sqrt{2})(a_2 + j * a_3) \tag{3.2}$$
$$\tag{3.3}$$

Knowing the reflection coefficient (Γ) of port 2 and port 3, then the relationship between (b_2, a_2) and (b_3, a_3) is the following.

$$a_2 = \Gamma_2 * b_2 \tag{3.4}$$
$$a_3 = \Gamma_3 * b_3 \tag{3.5}$$

Substitute (3.4) and (3.5) into (3.1) and (3.2):

$$b_1 = -(1/\sqrt{2})(j * \Gamma_2 * b_2 + \Gamma_3 * b_3) \tag{3.6}$$
$$b_4 = -(1/\sqrt{2})(\Gamma_2 * b_2 + j * \Gamma_3 * b_3) \tag{3.7}$$
$$\tag{3.8}$$

Furthermore, b_2 and b_3 can be deduced from 3.1.

$$b_2 = -(1/\sqrt{2})(a_4 + j * a_1) \tag{3.9}$$
$$b_3 = -(1/\sqrt{2})(a_1 + j * a_4) \tag{3.10}$$

If port 4 is matched to 50Ω , then equations (3.9) and (3.10) becomes...

$$b_2 = -(1/\sqrt{2})(j * a_1) \tag{3.11}$$
$$b_3 = -(1/\sqrt{2})(a_1) \tag{3.12}$$

Substitute (3.11) and (3.12) into (3.6) and (3.7):

$$b_1 = (1/2)(-\Gamma_2 * a_1 + \Gamma_3 * a_1)$$
$$b_1/a_1 = 1/2(\Gamma_3 - \Gamma_2) \tag{3.13}$$

$$b_4 = (1/2)(\Gamma_2 * j * a_1 + j * \Gamma_3 * a_1)$$
$$b_4/a_1 = j1/2(\Gamma_2 + \Gamma_3) \tag{3.14}$$

In general, we want to achieve a good input reflection. Then, in order to set equation (3.13) to be equal to zero, the reflection coefficient of port 2 and port 3 must be the same ($\Gamma_2 = \Gamma_3 = \Gamma_L$), which means that the two loads must be equal to each other. This simplifies (3.14) to the following:

$$b_4/a_1 = j\Gamma_L \tag{3.15}$$

$$\angle b_4/a_1 = 90^\circ + \angle\Gamma_L \tag{3.16}$$

Let the load impedance $Z_L = X_L + \mathrm{j}Y_L$.

$$\Gamma_L = \frac{(X_L - Z_0) + jY_L}{(X_L + Z_0) + jY_L}$$

$$\angle\Gamma_L = \arctan\frac{Y_L}{X_L - Z_0} - \arctan\frac{Y_L}{X_L + Z_0}$$

If we assume that $X_L << Z_0$, then...

$$\angle\Gamma_L = -2 * \arctan\frac{Y_L}{Z_0}$$

Hence (3.16), becomes...

$$\phi = \angle b_4/a_1 = 90^\circ - 2 * \arctan\frac{Y_L}{Z_0} \tag{3.17}$$

Thus, the maximum phaser shift range $\Delta\phi$ is the following...

$$\Delta\phi = \phi_{max} - \phi_{min} = -2(\arctan\frac{Y_L max}{Z_0} - \arctan\frac{Y_L min}{Z_0}) \tag{3.18}$$

Using the trigonometry identity where $\arctan\frac{x+y}{1-x*y} = \arctan x + \arctan y$, equation (3.18) can be simplified to equation (3.19).

$$\Delta\phi = -2\arctan\frac{(Y_L max - Y_L min) * Z_0}{(Z_0)^2 + Y_L max * Y_L min} \tag{3.19}$$

3.2.1 Theory and Design of Hybrid Coupler

The hybrid coupler is implemented using a lumped equivalent model of the transmission coupled-line hybrid coupler. A schematic diagram of the hybrid coupler is shown in figure 3.2. The equations for the value of the lumped components in this hybrid coupler is given in equations (3.20), (3.21) and (3.22). This hybrid coupler is designed at 29.75 GHz with a characteristic impedance of 50Ω. The simulation of the hybrid coupler is shown in Appendix A.

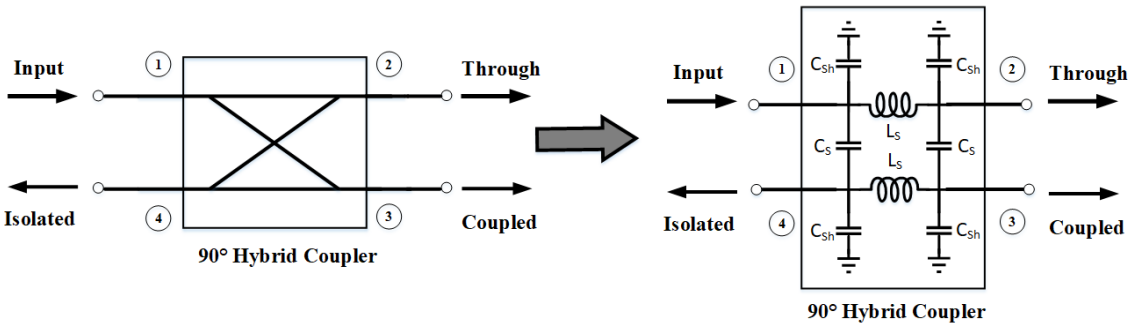


Figure 3.2: Schematic Diagram of Hybrid Coupler

$$C_s = \frac{1}{\omega_0 Z_0} \tag{3.20}$$

$$L_s = \frac{Z_0}{\omega_0 \sqrt{2}} \tag{3.21}$$

$$C_{sh} = \frac{1}{{\omega_0}^2 L_s} - C_s \tag{3.22}$$

The following reflective loads were implemented with this hybrid coupler in order to evaluate the overall performance of the reflective type phase shifter.

3.3 Reflective Loads

There are various load networks that can be implemented in this phase shifter to provide the necessary phase shift range. This section goes in-depth about the challenges of various load topologies.

3.3.1 Types of Varactor

Varactors are commonly used as tuning components that dynamically vary the impedance in any given circuit.

If a single varactor, that can ideally go from zero up to infinite, was used as a reflective load in the RTPS design, then the phase shift range can go up to 180°. However, the

tuning range of the capacitor is limited. The maximum and minimum capacitance is finite and it depends on the physical dimensions of the varactor.

TSMC 65nm technology offers two classes of varactors; a junction varactor and a MOS varactor.

A junction varactor, most commonly known as a diode varactor alters the capacitance at the p-n junction by varying the reverse biasing voltage. The capacitance of a diode is mainly determined by the doping levels at the p-n junction.

Accumulation-mode MOS varactor uses the gate bias (V_G) or the drain bias (V_D) to alter the capacitance at the gate (C_{ox}). The bias voltage of the sub-strate (V_{sub}) is set to 0 V. The cross section of the accumulation-mode MOS varactor is shown in figure 3.4.

In general, MOS varactors have a steep variation between the minimum and maximum equivalent capacitance, as shown in figure 3.3a, which means that a high-resolution DAC is needed in order to fine tune the MOS varactor.

However, junction varactors has a narrow tuning range compared to the MOS varactor, as shown in figure 3.3b. A larger junction varactor is required since the capacitance per unit area is smaller than that of a MOS varactor. The Q-factor of the junction varactor drops significantly especially when operating in accumulation-mode. This steep drop in the Q-factor results in a high insertion loss variation [4].

Thus, MOS varactor was choosen to be the tunable component in the load of the reflective-type phase shifter.

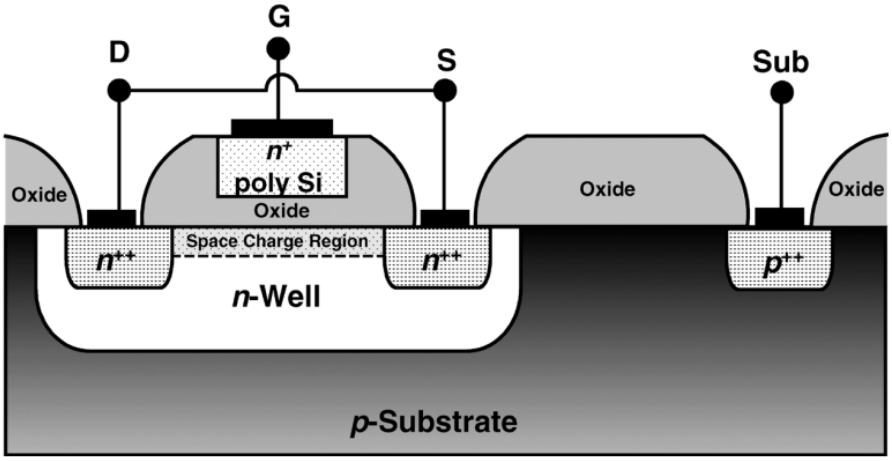
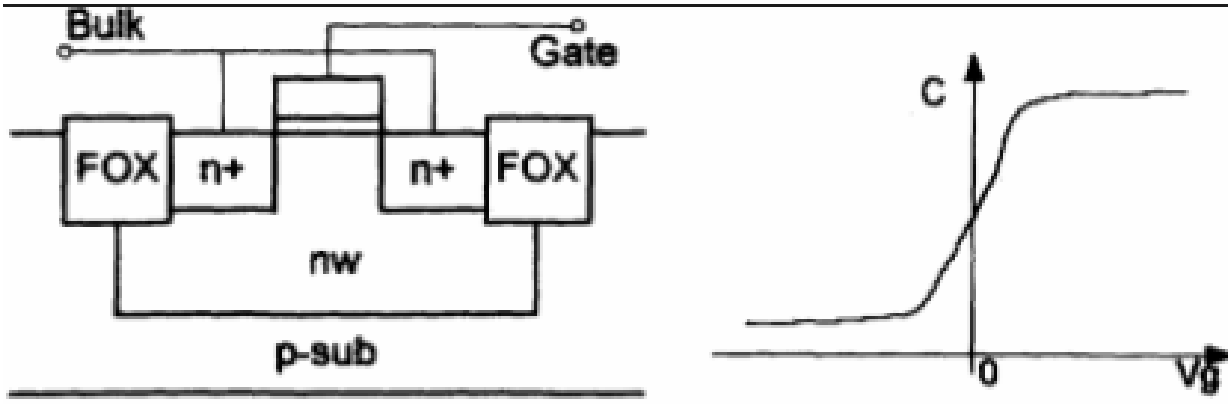
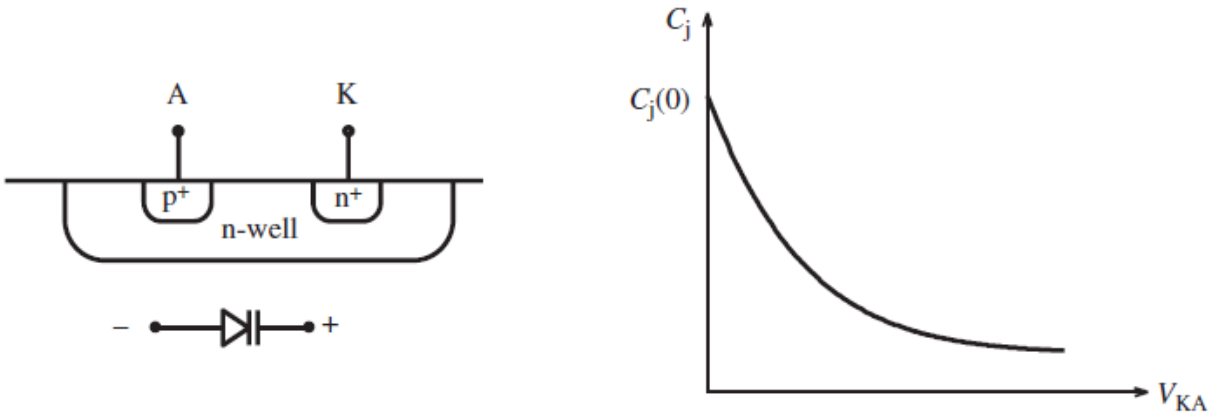


Figure 3.4: Cross-section of Accumulation-Mode MOS Varactor [31]



(a) MOS Varactor



(b) Junction Varactor

Figure 3.3: Typical Layout and Performance of a MOS and Junction Varactor [15]

When V_{MOS} is either positive or negative, the space charge region (SCR) expands or contracts respectively. The MOS capacitance C_{ox} is determined by the the gate oxide thickness.

Let $V_{MOS} = V_G - V_D$. Furthermore, let V_T represent the threshold voltage and V_{FB} represent the flat-band voltage.

If the voltage V_{MOS} increases, where $0V < V_{MOS} < V_{FB}$, the electrons start to accumulate under the gate eventually expanding the SCR and thus increasing the equivalent capacitance of the MOS varactor. The accumulation layer formed under the gate results in a low equivalent series resistance. This region indicates that the MOS varactor is operating

in accumulation-mode [31].

If $V_{MOS} > V_{FB}$, then there will be very little change to the equivalent capacitance of the MOS varactor due to the fact that there is already a large concentration of heavily accumulated surface layer underneath the gate. The capacitance saturates at some maximum value. This mode of operation is called the saturation region [31].

If the voltage V_{MOS} decreases below 0 V, where $V_T < V_{MOS} < 0V$, additional mobility carrier (holes) are induced under the gate, which contracts the SCR and thus decreases the equivalent capacitance. This mode of operation is called the depletion-mode. The equivalent series resistance of the depletion mode is high since the current must flow the resistance of the gate plus the resistance of the n-well, which is decreasing the conductive region of the n-well with a thick depletion region [31].

If $V_{MOS} < V_T$, then there will be very little change to the equivalent capacitance of the MOS varactor due to the fact that substrate depletion region reached its maximum depth. The capacitance saturates at some minimum value. This mode of operation is called the inversion region [31].

An example of the simulation results of a MOS varactor in TSMC 65-nm is shown in figure 3.5.

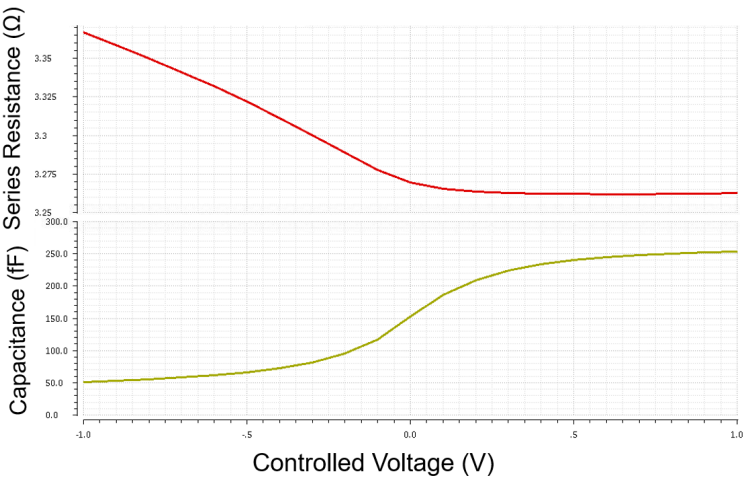


Figure 3.5: Equivalent Series Resistance and Capacitance of a CMOS 65-nm MOS Varactor

The capacitance of the MOS varactor, as shown in the figure above, goes from 50 fF to around 250 fF if the control voltage goes from -1 V to 1 V. Furthermore, the equivalent series resistance of this MOS varactor goes from 3.26 Ω to 3.28 Ω.

3.3.2 Reflective Load Topology

As mentioned in the sub-section above, if the MOS varactor can tune it's value from 0 to ∞ then you can achieve a 180° phase shift range from its reflection, as shown in 3.6. However, the typical tunning ratio between the minimum and maximum capacitance is about 3. Thus, the phase shift range will be lesser than 180°.

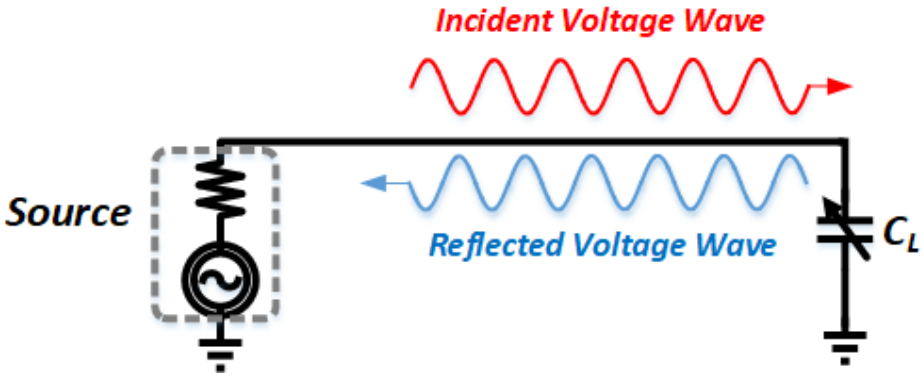


Figure 3.6: Diagram of a MOS Varactor Load with Power Waves

One way to overcome this problem is to add an inductor that resonates out the maximum or minimum capacitance of the MOS varactor. This will ensure that you will get a much wider phase shift range.

However, this doesn't give you the full phase shift range. One reflective load that can be used to achieve a 360° phase shift range can be achieved by using a dual-resonant load. A schematic diagram of the dual resonant load is shown in figure 3.7.

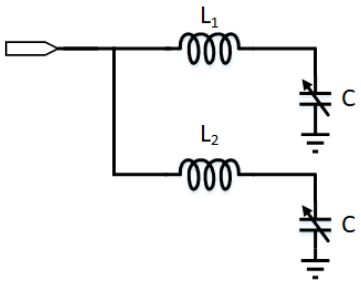


Figure 3.7: Schematic Diagram of Dual Resonant Load

If we let the MOS varactor go from C_{min} to C_{max}, then the equation for the design of the dual resonant load is shown in equations (3.23) and (3.24).

$$L_1 = \frac{1}{{w_0}^2 C_{min}} \tag{3.23}$$

$$L_2 = \frac{1}{{w_0}^2 C_{min}} \tag{3.24}$$

A large phase shift range was simulated using this configuration. Assuming that the control voltage bias goes from 0V to 1V, then the simulated phase shift range is 356°. Unfortunately, this reflective load topology produces significant insertion loss variation, as shown in figure 3.8.

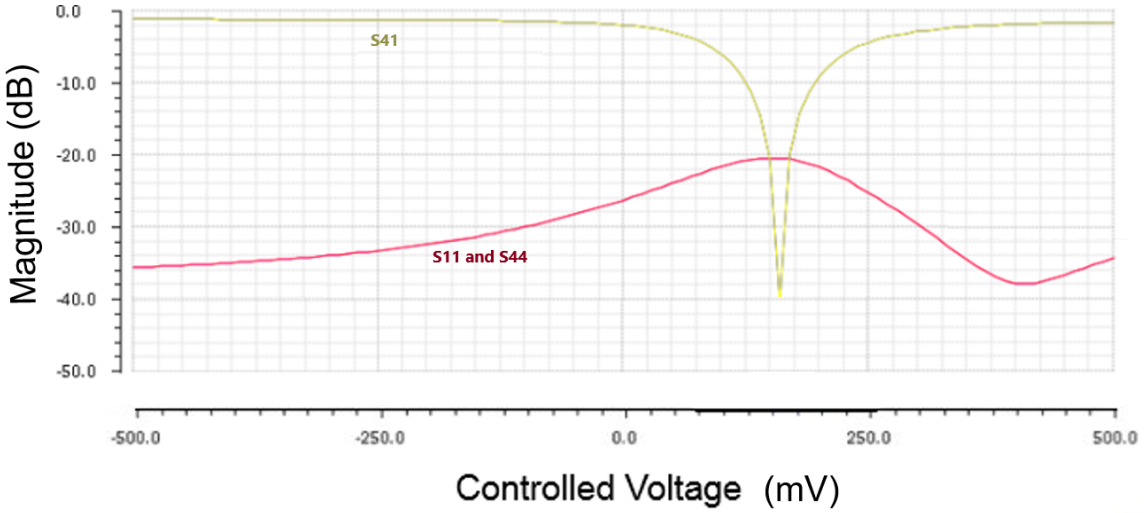


Figure 3.8: Simulation of a Reflective Type Phase Shifter with a Dual Resonant Load

This is due to the fact that at some point the real equivalent impedance of the dual resonant load is very close to the reference impedance (50 Ω). Ideally in a reflective type phase shifter, the reflection coefficient of the reflective load will be ± 1. However, in this case, majority of the input signal will get absorbed into the reflective load instead of getting it reflected back to the output port.

A simple LC transformation network in front of the dual resonant load can be added to decrease the insertion loss variation. However, this will increase the mean insertion loss.

A schematic diagram of this topology is shown in figure 3.9 and the equations for the LC transformation network is shown in equations (3.25) and (3.26).

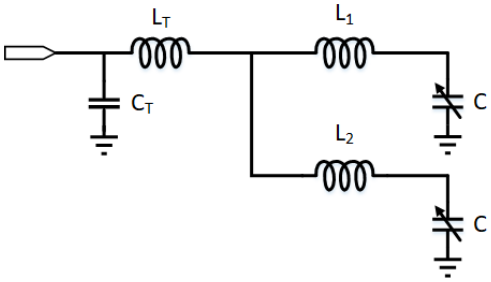


Figure 3.9: Schematic Diagram of LC transformation network in a Dual Resonant Load

$$L_T = \frac{1}{{w_0}^2 C_{avg}} \tag{3.25}$$

$$C_T = \frac{1}{{w_0}^2 L_T - \frac{1}{C_{max}} - \frac{1}{C_{min}}} \tag{3.26}$$

As shown in figure 3.10, the insertion loss variation decreases significantly to 4.7 $\pm$ 2 dB. The phase shift range still stays the same from 0 V to 1 V, which is about 356°. There is a blind spot in the first quadrant from 37.5° to 41.5°.

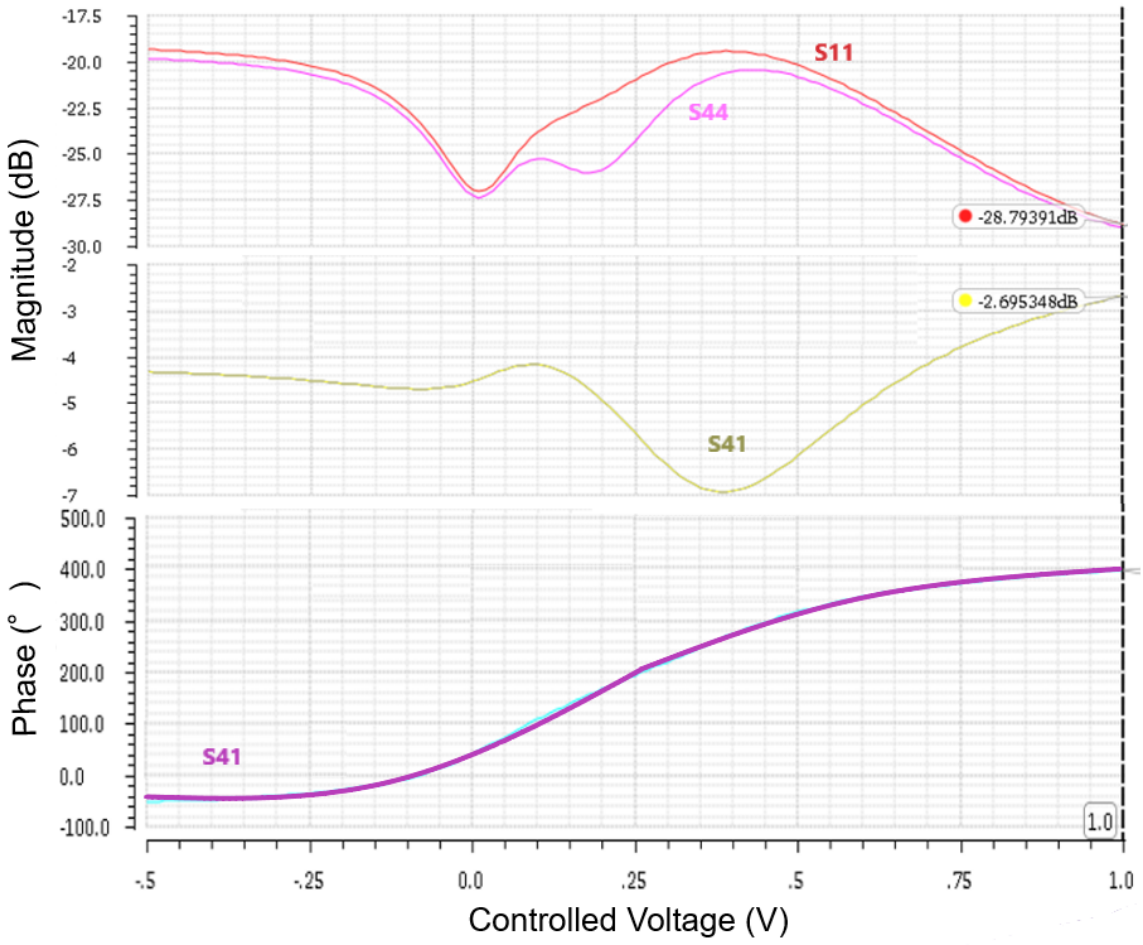


Figure 3.10: Simulation of a Reflective Type Phase Shifter with a LC-transformation Dual Resonant Load

This LC-transformation network dual-resonant load topology provides a very wide phase shift range with good insertion loss variation and reflection at the 29.75 GHz. However, there are some blind spots and so it does not cover the full 360° phase shift range. Furthermore, since each reflective load requires three inductors, then eight inductors are needed for this reflective load topology. Since we are designing this phase shifter at ka-band, then the size of these inductors will be significant and thus this phase shifter topology will no longer be compact.

Another solution is to design a compact π reflective load topology as shown in figure 3.11. Although this topology would not provide a full 360° phase shift range it is compact

compared to the other reflective load topologies.

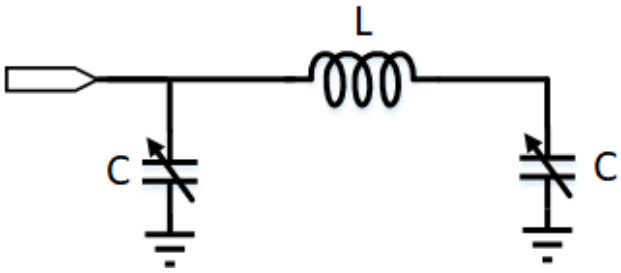


Figure 3.11: Schematic Diagram of a π Load

3.4 Other Design Considerations and Challenges

In order to get the full 360° phase shift range with no significant blind spots using the pi-network reflective load topology shown in figure 3.11, then we must add another component in series with the reflective load type phase shifter. 180° high pass low pass phase shifter was selected. This will provide a full 360° phase shift range without any additional insertion loss variation and it is the most compact solution.

A schematic diagram of the 180° high-pass low-pass phase shifter is shown in figure 3.12. A single-pole double-throw (SPDT) switch was designed in order to provide high isolation.

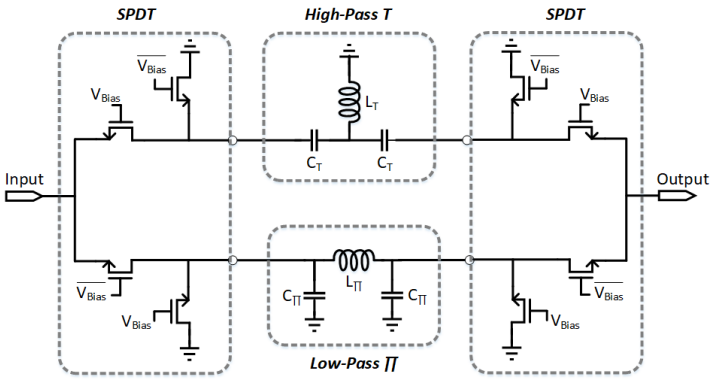


Figure 3.12: Schematic of a Compact High-pass Low-Pass Phase Shifter

All transistors have minimum length and have a width of approximately 36μm. Triple well N-type MOSFET were used as the switch core transistors in order to reduce signal and noise coupling. The high-pass $\boldsymbol{T}$ filter and the low-pass $\prod$ filter was chosen due to its compact network. The values for these lumped components can be obtain from equations (2.10), (2.11), (2.12) and (2.13) where the the high-pass phase is +90°, the low-pass phase is -90°, frequency is 29.75 GHz and the reference impedance is 50Ω.

This high-pass low-pass phase shifter produces an insertion loss of 2.6 ± 0.5 dB and a phase shift of about 176.9° at 29.75 GHz.

When cascading these two phase shifters together, the reflective load topology had to be re-tuned due to the loading of the parasitic capacitance from the high-pass low-pass type phase shifter. Furthermore, since the phase shifter is completely passive, then it is sensitive to the ground plane of the integrated circuit. In other words, this phase shifter design is sensitive to its return path. We had to place the ground pins in order to ensure that the loop caused by the path of the input signal and the path of the return signal is as small as possible. Furthermore, we had to ensure that there was a ground wall with all the metal layers in between the two reflective loads to ensure that there were not any coupling.

The schematic diagram of the overall phase shifter the produces a 360° phase shift range is shown in figure 3.13.

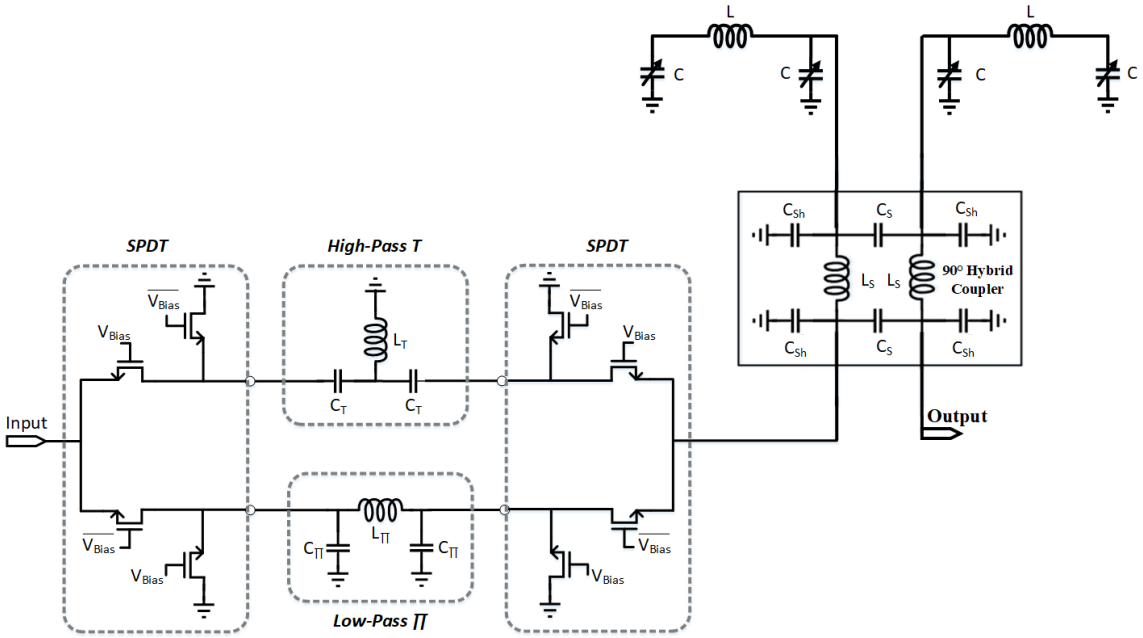
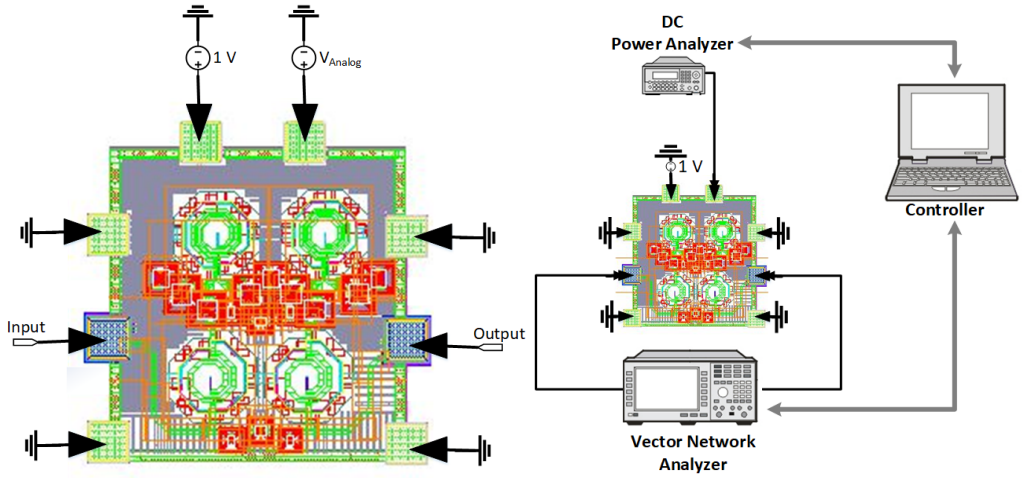


Figure 3.13: Schematic Diagram of Cascaded Phase Shifter

3.5 Simulation and Measurements

The test setup in order to measure the reflective-type phase shifter is shown in figure 3.14. A python script was used in order to control the DC power analyze, which controlled the voltages and measured the current, as well as the vector network analyzer, which measured the S-parameters for each bias voltage, through a GPIB-to-USB controller.



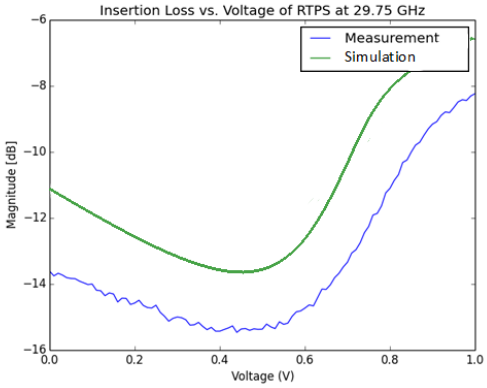
(a) Biasing the Integrated Circuit Design (b) Test Setup

Figure 3.14: Test Setup of the Reflective Type Phase Shifter for Measurements

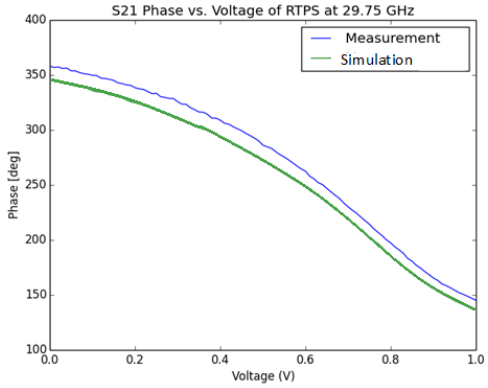
The fabricated circuit was measured using on-wafer probing. The measurement and simulation of this circuit is shown in figure 3.15 at the desired frequency of interest, which is at 29.75 GHz. A phase shift range of 203.7° was achieved with a return loss well below 10 dB.

Table 3.1: Summary of the Performance of the Reflective Type Phase Shifter

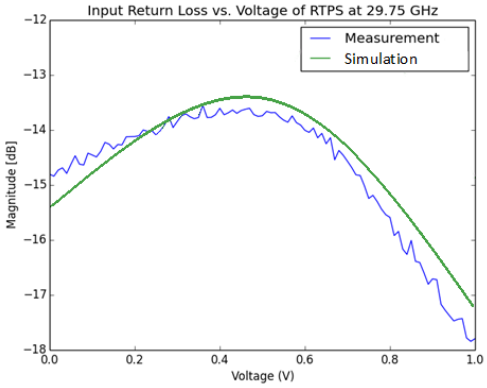
Feature	***Value***	
	Simulation	***Measurement***
Frequency (GHz)	29.75	
Topology	RTPS	
Technology	65-nm CMOS	
Control Voltage(V)	0 to 1	
Phase Control Range (°)	205.8	203.7
Insertion Loss (dB)	9.75 ± 2.4	10.64 ± 2.625
Input Return Loss (dB)	>13.5	>13.92
Output Return Loss (dB)	>13.7	>10.78
Chip Size (mm^2)	0.414 X 0.414	



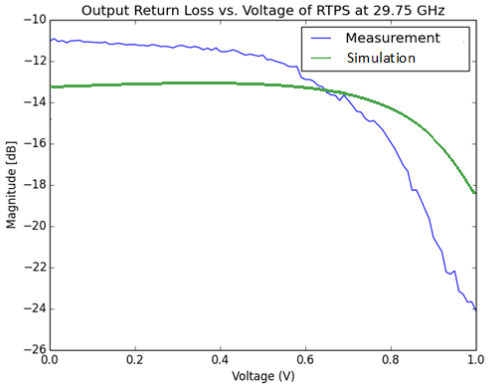
(a) Insertion Loss



(b) Phase of the Output Signal Relative to the Input Signal



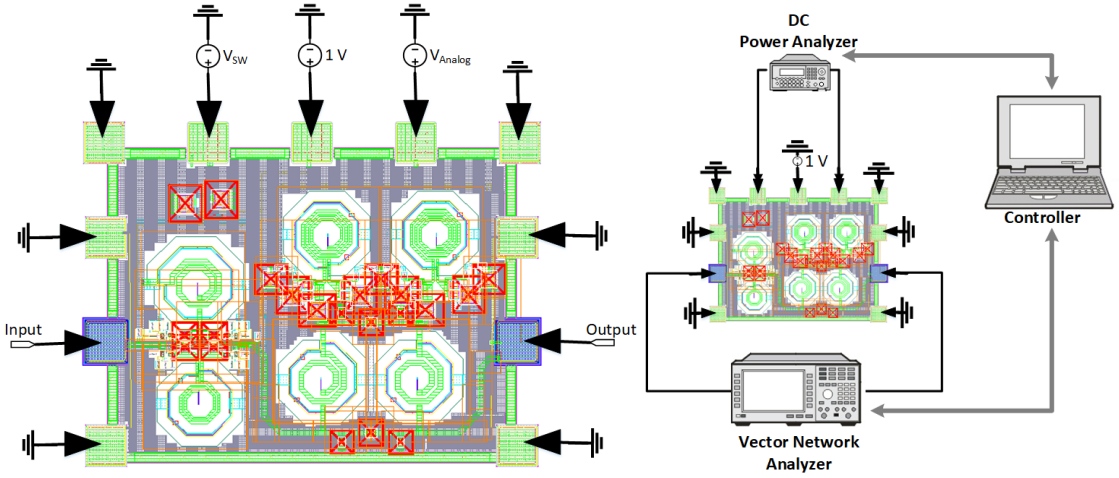
(c) Input Return Loss



(d) Output Return Loss

Figure 3.15: Simulated and Measured Results of the Reflective Type Phase Shifter at 29.75 GHz

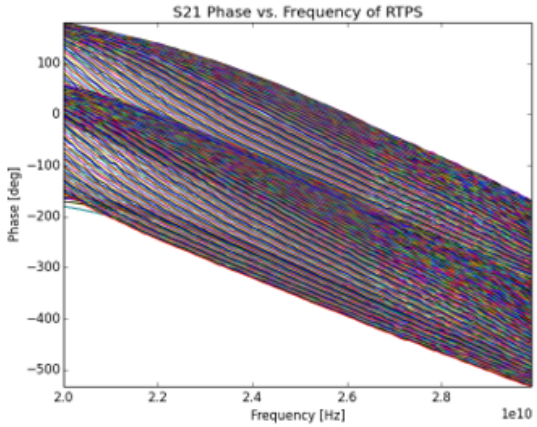
The test setup in order to measure the cascaded phase shifter is shown in figure 3.16. This test setup is very similar to that of the reflective type phase shifter. A table that summarizes the performance of the cascaded phase shifter is shown in table 3.2. The measurement and simulation of this circuit is shown in figure 3.17. A full phase shift range was achieved with a return loss of about 10 dB or greater. As shown in figure 3.18, assuming that the the amplitude variation is corrected using a variable gain amplifier, then the IQ vector diagram shows that at least an 8-bit DAC is needed to control the cascaded phase shifter in order to achieve a phase resolution of 5.625°. Looking at the worst case scenario, the group delay of the cascaded phase shifter at 29.75 GHz with a 1 MHz bandwidth is about 96.26 ± 37.76 ps. In theory, since this cascaded phase shifter is passive there should not be any power consumption; however, there was some leakage current caused by the parasitic resistance of MOS varactor and the SPDT switches. The nominal current consumed by this phase shifter topology is about 56μA.



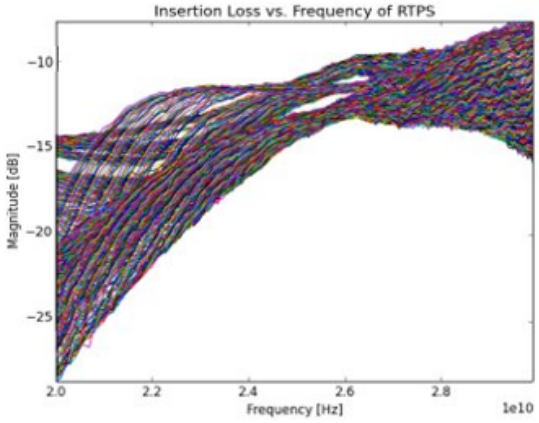
(a) Biasing the IC

(b) Test Setup

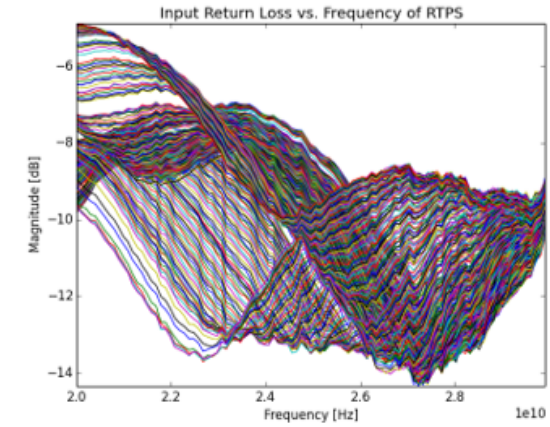
Figure 3.16: Test Setup of the Cascaded Phase Shifter for Measurements



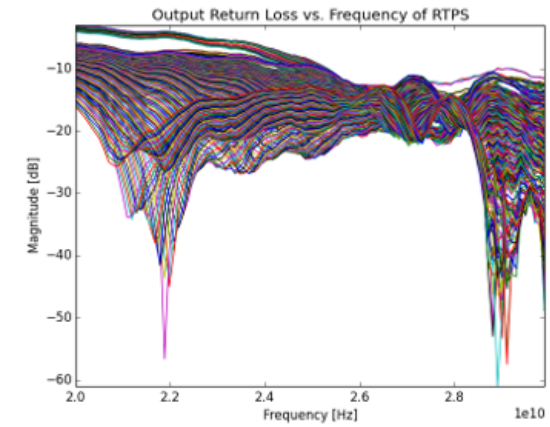
(a) Insertion Loss



(b) Phase of the Output Signal Relative to the Input Signal



(c) Input Return Loss



(d) Output Return Loss

Figure 3.17: Simulated and Measured Results of the Cascaded Phase Shifter with Various Bias Voltage

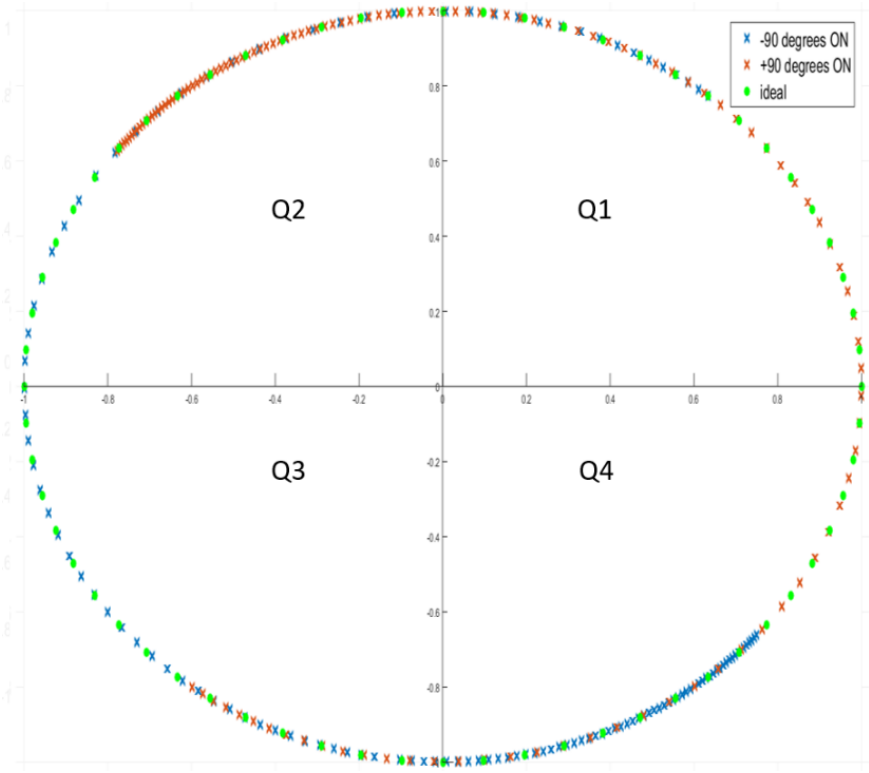


Figure 3.18: IQ Vector Diagram when the Phase Shifter is Controlled Using an 8-bit DAC

Table 3.2: Comparison of Similar Phase Shifter Designs in K\Ka-Band

Reference	[19]	[32]	[22]	[8]	***This Work***
Frequency (GHz)	23	22	30	28	29.75
Topology	180° RTPS + 180° STPS	180° RTPS + 180° STPS	RTPS	RTPS	RTPS + 180° STPS
Technology	180-nm CMOS	180-nm CMOS	130-nm SiGe	65-nm CMOS	65-nm CMOS
Control Voltage(V)	-1.2 to 0.8	-0.5 to 0.8	0 to 1.5	0 to 2	0 to 1
Phase Control Range (°)	275	336	206	360	360
Insertion Loss (dB)	12.6±0.6	16±1.3	4.8±0.4	7.75±0.3	13.05±2.75
Input Return Loss (dB)	>8.2	>8.5	>10	>6.7	>9.6
Output Return Loss (dB)	>8.9	>12	>10	>7.5	>12.17
Chip Size (mm^2)	0.95X0.47	0.40X0.37	0.78X0.83	0.76X0.3	0.55X0.41

Chapter 4

Analysis and Design of On-Chip Low-Noise Amplifier

4.1 Design Analysis

Low noise amplifier serves as the first key block in any radio frequency system. The purpose of the LNA is to provide enough gain such that the signal is much higher than that of the noise floor from the entire Rx chain. CMOS LNA circuits operating at high frequency are very close to their unity gain frequency (f_T). The unity gain frequency is defined as the frequency in which the current gain is equal to 0 dB. In contrast, the maximum frequency (f_{max}) is defined as the frequency in which the maximum possible gain is equal to 0 dB. Thus, at high operating frequencies the CMOS LNA will operate with a lower gain, narrower bandwidth and higher power consumption compared CMOS amplifiers operating at lower frequencies.

The specifications of the on-chip LNA for this project is shown in table 4.1.

Table 4.1: Low Noise Amplifier Specifications

Parameter	***Units***	***Value***
Bandwidth	GHz	19 - 21
Gain	dB	>20
Noise Figure	dB	<3.5
Isolation	dB	<-35
1-dB Compression Point	dBm	>-25
Input and Output Return Loss	dB	>10
Power Consumption	mW	<6.5

From the plots shown in figure 4.1, the highest f_{max} that can be achieved with this technology is about 145 GHz. Thus, at 20 GHz, the maximum available gain is about 17 dB, as shown in equation (4.1) [26].

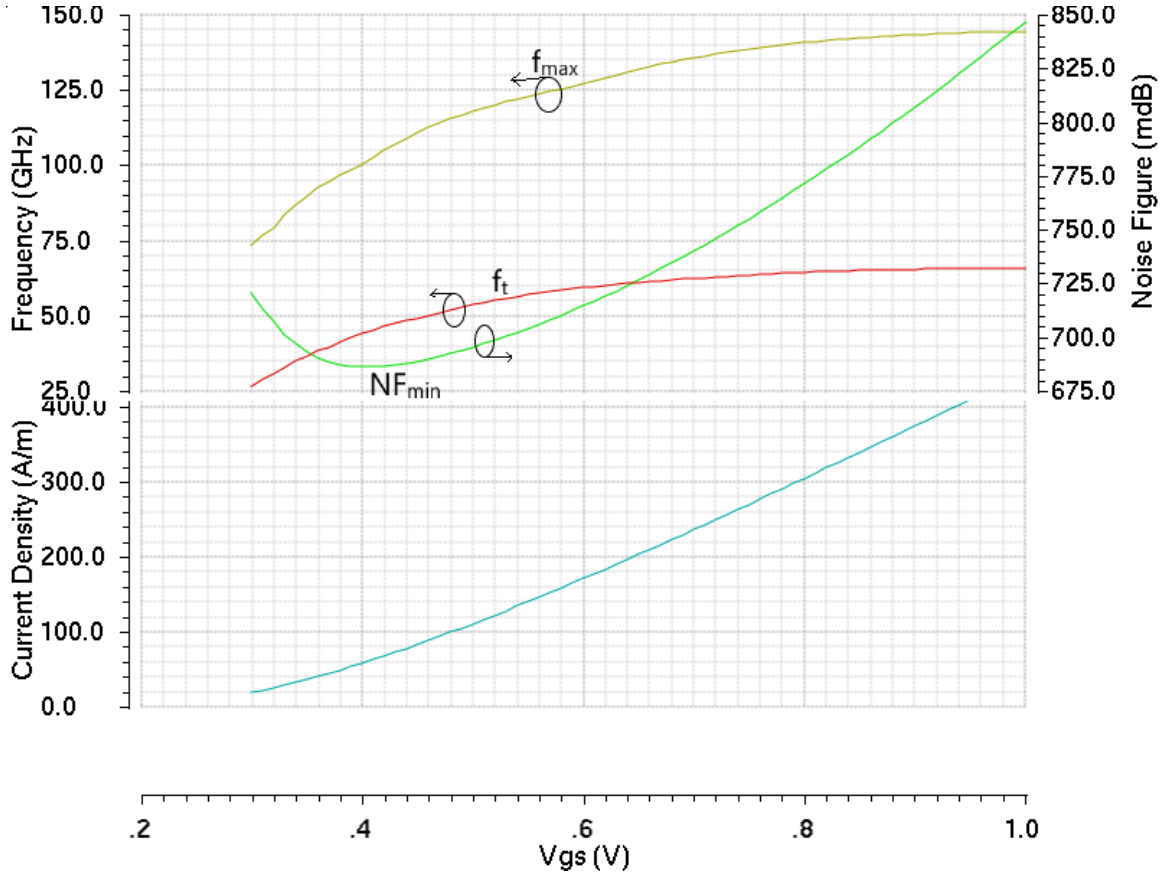


Figure 4.1: Minimum Noise Figure at 20 GHz, f_T and f_{max} vs. Current Density for CMOS 130 nm

$$G_{MAX} = 20 \log \frac{f_{max}}{f_0} \approx 17dB \tag{4.1}$$

We want a gain of about 20 dB while achieving low noise figure. Thus, this LNA will require two stage amplifier to meet the specifications, which leaves a lot of flexibility in how we size and and do impedance matching on the transistors. We can design it to be as compact as possible while giving us a reasonable noise figure.

The impedance presented at the input of the LNA is what determines the noise figure of the block; thus, the first stage is biased for low noise while the second stage is biased for high gain and dynamic range. The block diagram of a two-stage LNA is shown in figure 4.2.

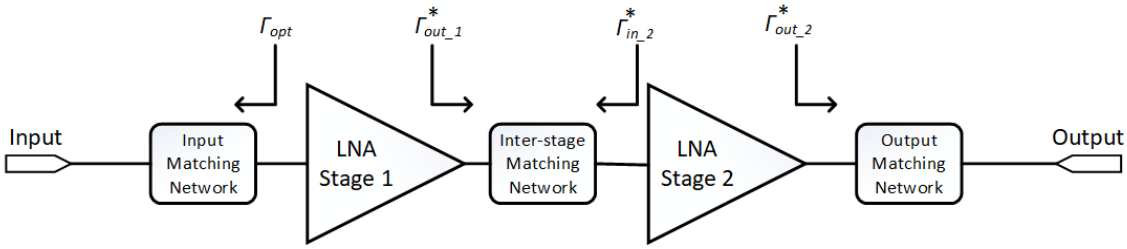


Figure 4.2: Block Diagram of a General 2-Stage Low Noise Amplifier

Since we want to have the lowest possible noise figure for the first stage while still getting some adequate gain to relax the specifications on the second stage, then a current density of 50 A/m was selected. The smallest noise figure is achieved at this current density ($NF_{min} \approx 0.685$ dB) and it provides a maximum possible gain of about 15 dB, using equation (4.1) where $f_T \approx 110$ GHz.

For the second stage, a current density of 92 A/m was selected. It still provided an adequate gain of about 16 dB ($f_T \approx 130$ GHz) while still providing a relatively low NF_{min}.

In theory, the transistors are sized so that there is simultaneous gain and noise matching. However, in this case, the amount of current consumed by the LNA, if the transistor is sized for simultaneous matching, is beyond the current limit. The LNA is biased at 1.2 V and the total power budget for the on-chip LNA is 6.5 mW; thus, the maximum amount of current that can be consumed by the LNA is about 5.5 mA. If we were to allocate equal amount of current for both stages, then that means that the first stage and second stage can only consume a maximum of 2.7 mA.

4.1.1 Cascode Amplifier Analysis

Each stage is designed with a cascode amplifier since it provides better isolation between the input and output port, a higher input impedance and a higher output impedance. This means that the ratio between the output impedance to 50Ω will be closer to 1 with a cascode amplifier than with a common-source amplifier. However, this will increase the noise figure of the LNA.

By doing small signal analysis of a cascode amplifier, as shown in figure 4.3, and assuming that the cascode transistors are sized the same then the maximum power gain is shown in equation (4.2). Furthermore, the first pole and the unity gain frequency are shown in equations (4.3) and (4.4) [28]. Let $Z'_L = Z_L + \text{jwL}$, and then let the load impedance Z'_L

$= R_L + \frac{1}{jwC_L}$. Thus, we are assuming that inductance of the inductor (L_{S1}) is very high that it is negligible. Also, this analysis assumes that the capacitance between the drain and the source terminal is small that it is negligible.

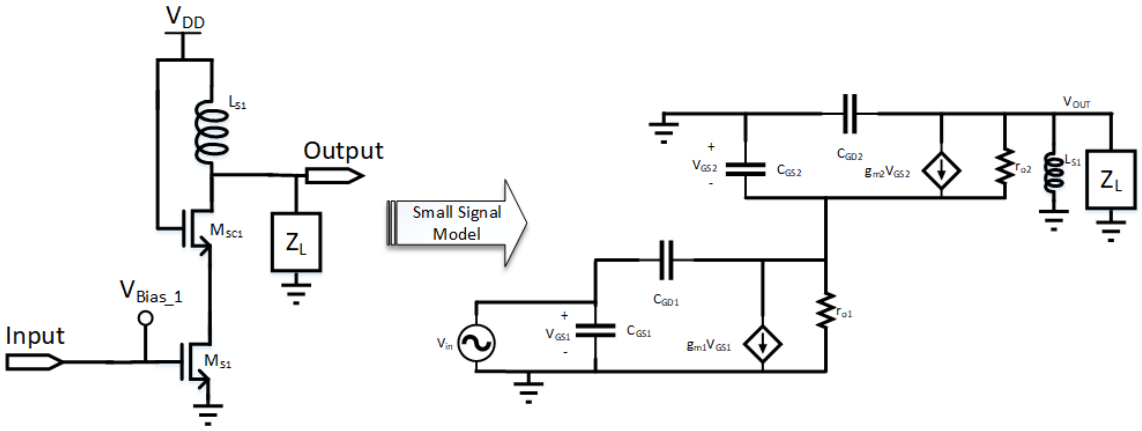


Figure 4.3: Small Signal Model of a Cascode Amplifier

$$G_{MAX} = {g_m}^2 r_0(r_0||R_L) \tag{4.2}$$

$$f_{3dB} = \frac{1}{2\pi(C_L + C_{gd})g_m r_0(r_0||R_L)} \tag{4.3}$$

$$f_t = \frac{g_m}{2\pi(C_L + C_{gd})} \tag{4.4}$$

As shown in equation (4.4), the unity-gain frequency of the common source amplifier and this cascode amplifier are the same. Thus, the analysis and sizing of the transistor done in the previous subsection is valid for the cascode amplifier design.

The width of the transistors was sized to increase the small signal output resistance while keeping the input resistance of the common-source transistor (M_{S1}) close to 50 Ω. Thus, for the first stage, a width of 52.5 μm was chosen for the transistors and for the second stage, a width of about 30 μm was chosen. The width of the common gate transistors were tuned to be slightly higher in order to minimize the drain-source voltage drop so that the common-source transistor can operate in the saturation region.

4.1.2 Stability

This low noise amplifier must be unconditionally stable over k-band (in specific from 19 GHz to 21 GHz). Stability equations shown in equation (4.5) and equation (4.6) are used at each frequency to determine if the circuit is unconditionally stable [24].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{4.5}$$

$$|\Delta| = |S_{11}S_{22} - S_{21}S_{12}| \tag{4.6}$$

K ≥ 1 and $\Delta < 1$ for the two port circuit to be unconditionally stable. These conditions must be satisfied at each stage in the low noise amplifier in order for the overall LNA to be unconditionally stable from 18 GHz to 21 GHz. Whenever the impedance looking into the circuit causes negative resistance, then that causes instability. The small signal analysis of the common gate transistor in the cascoded amplifier assumes that the inductance of the inductor (L_{S1}) is very high and the resistance of the transistor (r_0) is also very high that that are both negligible.

The common-source amplifier can be replaced with its equivalent impedance when looking into the drain terminal, which is its equivalent capacitance and resistance as shown in figure 4.4 and equation (4.7). By doing small signal impedance of the common-gate transistor as shown in figure 4.5, the resistance looking into the gate terminal of the common-gate transistor is negative, as shown in equation (4.8) [28].

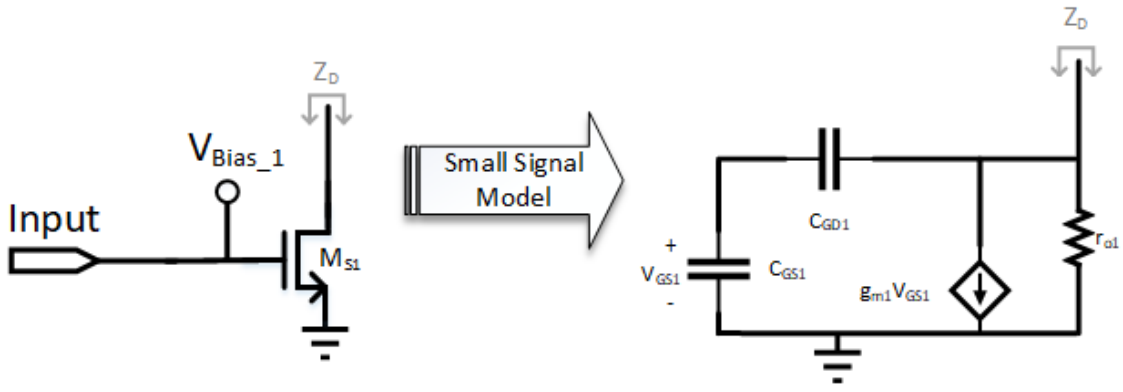


Figure 4.4: Impedance Looking into the Drain of the Common-Source Amplifier

$$Z_D = (r_0||(C_{GS1}||C_{GD1})) \tag{4.7}$$

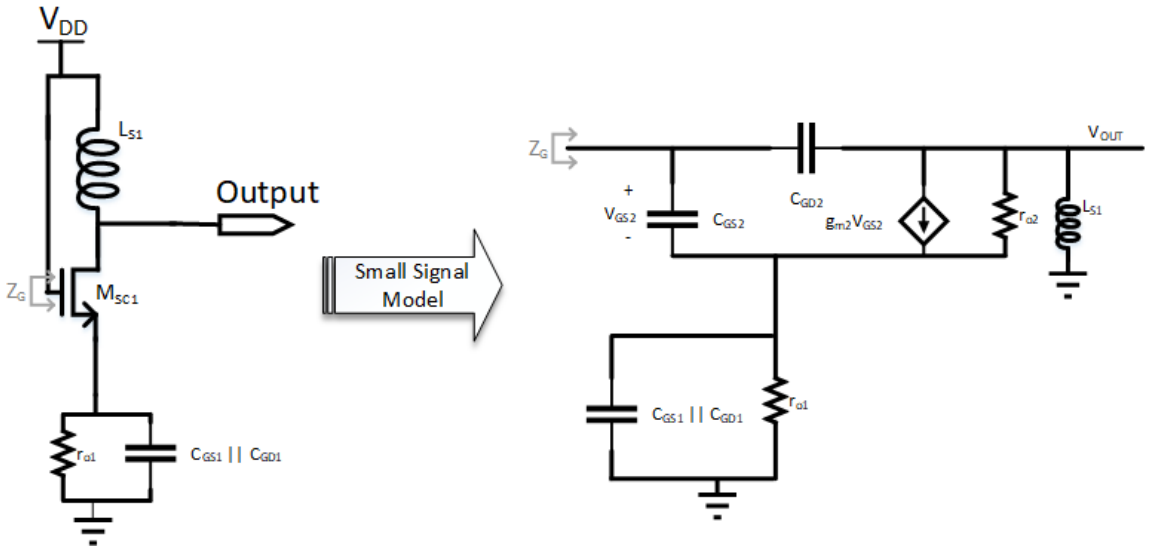


Figure 4.5: Impedance Looking into the Gate of the Common-Gate Amplifier

$$Real(Z_G) = \frac{-g_{m2}}{w^2(C_{GS1}||C_{GD1})C_{GS2}} \tag{4.8}$$

Furthermore, a long transmission line is needed to connect the gate terminal of the common-gate transistor to V_{DD}, which creates an equivalent inductance. Let L_{TL} represent the equivalent inductance of this transmission line. By doing small signal analysis of the circuit shown in figure 4.6, this inductor causes the resistance looking into the source terminal of the common gate transistor to be negative at very high frequencies, as shown in equation (4.9) [28].

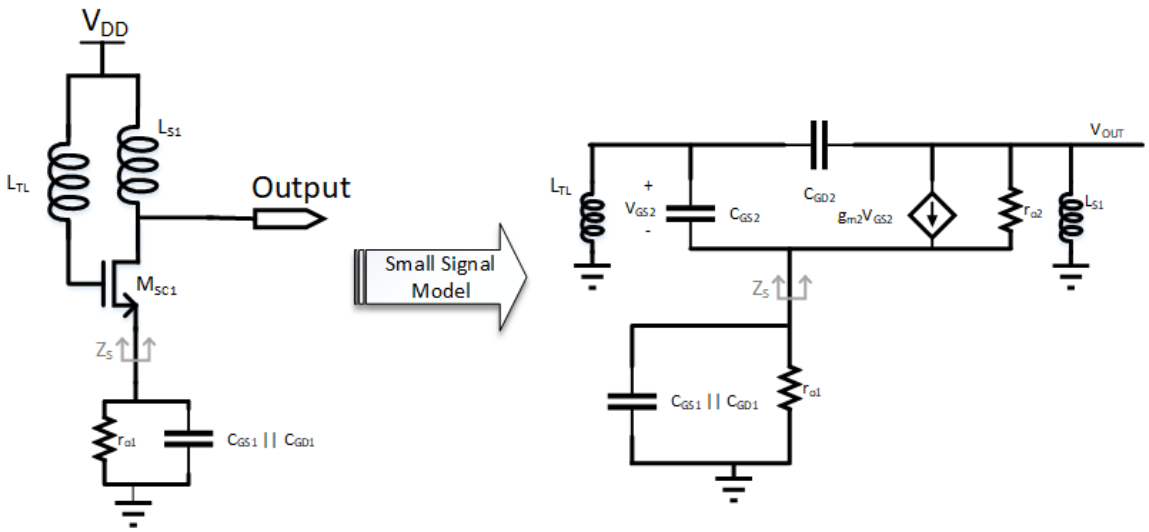


Figure 4.6: Impedance Looking into the Source of the Common-Gate Amplifier

$$Real(\frac{1}{Z_S}) = \frac{g_{m2}}{1 - wC_{GS2}L_{TL}} \tag{4.9}$$

High impedance series resistance are added in between V_{DD} and the gate terminal in order to push the instability to a much higher frequency higher frequency. In other words, series resistance is added to the gate in order to make the equivalent resistance looking into the gate to be positive and to make sure that the negative resistance looking into the source terminal of the common-gate transistor to a much higher frequency (away from k-band).

4.1.3 Matching Network

The input matching network was designed such that it transforms the source impedance (50 Ω) to the required impedance such that we get low noise figure and adequate gain. This is done using available power gain circles and noise circles.

Available power gain (G_A) is defined as the gain available to the network, assuming that the output impedance is matched ($\Gamma_L = \Gamma_{out}*$). The equation of the available gain and maximum available gain is shown in equations (4.10) and (**??**), where P_{AVN} represents the power available to the network and P_{AVS} represents the power available from the source [24].

$$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{1-|\Gamma_S|^2}{|1-s_{11}\Gamma_S|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{OUT}|^2} \tag{4.10}$$

$$g_a = \frac{G_A}{|S_{21}|^2} = \frac{1-|\Gamma_S|^2}{|1-s_{11}\Gamma_S|^2(1-|\Gamma_{OUT}|^2)} \tag{4.11}$$

From equation (4.10), you can see that an infinite number of source terminations can produce a specific available gain. This forms a circle on the smith chart. This circle can be calculated using equation (4.13) to locate the center of the available gain circle, and equation (4.12) calculates the radius of that circle [24]. Let g_a represent the ratio of the available gain with respect to the maximum gain (the formula is shown in equation (4.11)), K and Δ are the stability parameters.

$$R_a = \frac{[1-2K|S_{12}S_{21}|g_a + |S_{12}S_{21}|^2 g_a^2]^{0.5}}{1+g_a(|S_{11}|^2-|\Delta|^2)} \tag{4.12}$$

$$C_a = \frac{g_a(S_{11}-\Delta {S_{22}}^*)^*}{1+g_a(|S_{11}|^2-|\Delta|^2)} \tag{4.13}$$

Furthermore, as shown in equation (4.10), the source termination gets further away from 50 Ω then the smaller the gain

Similarly, noise circles can be drawn using a very similar procedure. A transistor noise performance is independent of the load termination. In fact, it is solely dependent on the inherent noise parameters of the transistor and the source termination. The noise factor of a transistor is shown in equation (4.14). F_{min}, r_n, and Γ_{opt} are the inherent noise parameters of the transistor. Note F_{min} or NF_{min} of the transistor was simulated in figure 4.1.

Equation (4.14) gives the noise factor value using the transistor's noise factor parameters.

$$F = F_{min} + \frac{4r_n|\Gamma_s-\Gamma_{opt}|^2}{(1-|\Gamma_s|^2)|1+\Gamma_{opt}|^2} \tag{4.14}$$

Noise factor degrades as the source termination ($Gamma_s$) gets further away from the optimal termination (Γ_{opt}). Similarly to the available gain circles, there are infinite possible source terminations that provides the same noise figure. This forms a circle on the smith

chart. The noise figure circle can be calculated using equation (4.17) to locate the center of the available gain circle, and equation (4.16) calculates the radius of that circle [24].

$$N_i = \frac{F_i - F_{min}}{4r_n}|1 + \Gamma_{opt}|^2 \tag{4.15}$$

$$R_{nf} = \frac{1}{1 + N_i}\sqrt{N_i^2 + N_i(1 - |\Gamma_{opt}|^2)} \tag{4.16}$$

$$C_{nf} = \frac{\Gamma_{opt}}{1 + N_i} \tag{4.17}$$

Typically, in any low noise amplifier design there is a trade off between gain and noise figure. The intersection point of the desired noise figure and available circles is the ideal source termination needed to achieve those parameters. This source impedance won't give the optimum noise of the maximum gain but it will give us something that will satisfy the specifications. If there is more than one intersection point between the noise figure and gain circles, then the source termination will be the one that is closest to 50 Ω for smaller trans-impedance ratio and thus wider bandwidth.

The noise figure and available gain circles for the first stage is shown in figure 4.7.

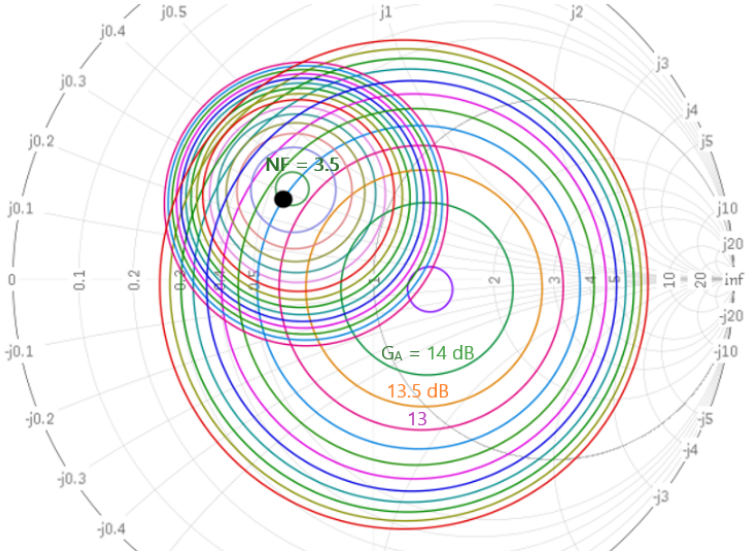


Figure 4.7: Available Gain and Noise Circles of the 1st Stage of the LNA

For this LNA design, the first stage was chosen to have a noise figure of 3.5 dB and an available gain of 12.5 dB. The ideal source termination for the first stage is shown with a solid black circle in figure 4.7.

Conjugate matching was done between the output of the first stage and the input of the second stage to provide maximum gain. In order to make the design as compact as possible, the RF choke and DC block capacitors of the first stage were tuned to provide the matching network needed between the two stages. Finally, the output of the last stage was matched to the 50 Ω termination for maximum gain. Similar to the intermediate matching network, the output matching network tunes the value of the RF choke and the DC block capacitor.

4.2 Final Design of LNA

The final circuit design of the low noise amplifier is shown in figure 4.8.

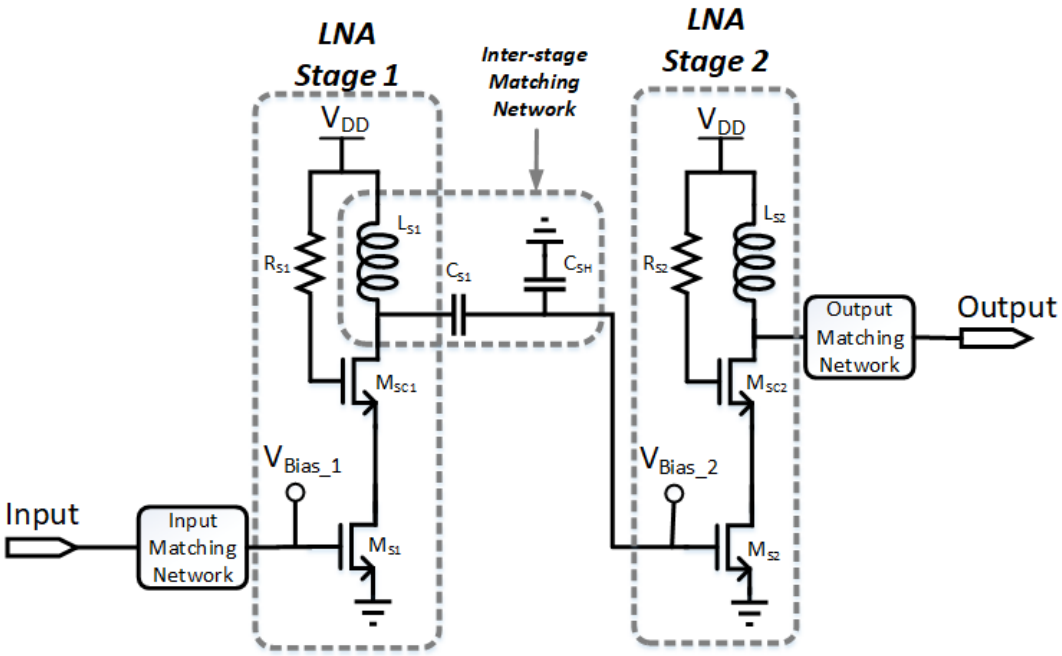


Figure 4.8: Schematic Diagram of a 2-Stage Low Noise Amplifier

The bias circuit of the LNA is shown in figure 4.9. Since the gate and drain terminals are

connected together, then this diode-connected transistor will always operate in saturation region. This topology converts current to the desired voltage.

The current going through the resistor is forced to be equal to the drain current of the transistor. By doing so, this induces a voltage drop across the resistor (R_1). The resistance of R_1 is tuned to provide the necessary voltage at the drain/gate terminal. For stage 1, we want the gate voltage to be biased at The resistance of R_2 is high enough in order to make sure no current goes to the LNA from the bias network and vice versa without affecting the input matching network of the LNA.

A bunch of high capacitance bypass capacitors are placed close to the DC pad and very close to the gate terminals of all transistors that are directly connected to the DC voltage of an external power supply. This is done in order to prevent any high frequency noise caused from the external environment (i.e. external power supply) from entering into the LNA design.

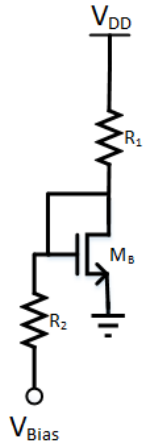
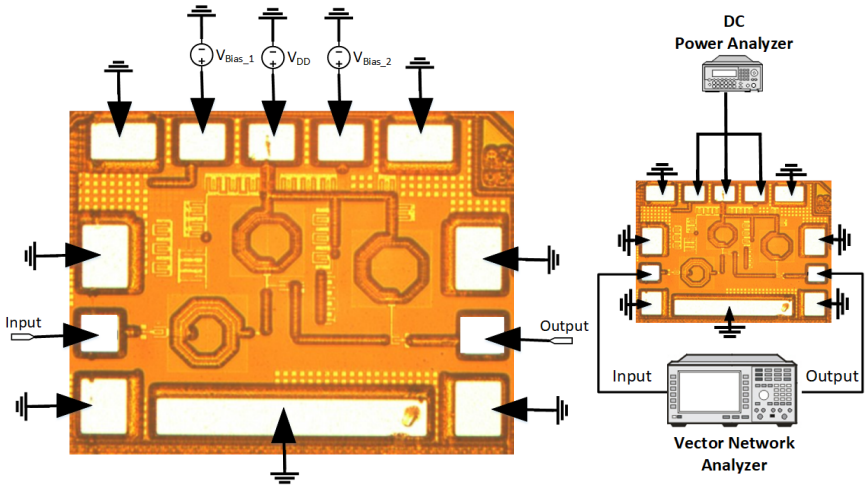


Figure 4.9: Schematic Diagram of the Bias Network used in the Low Noise Amplifier

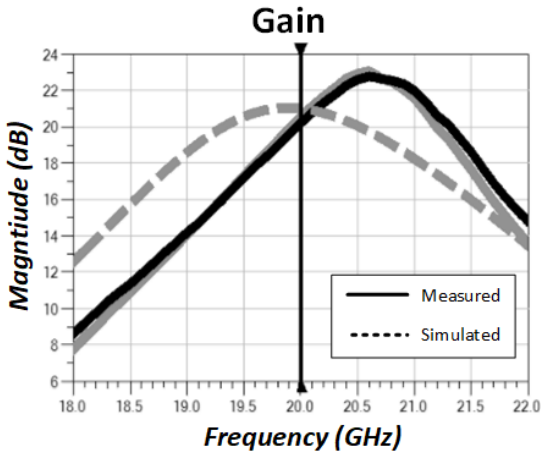
The test setup in order to measure the low noise amplifier is shown in figure 4.10.



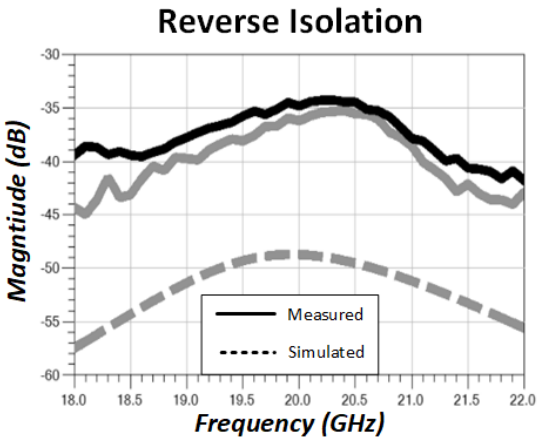
(a) Biasing the IC (b) Test Setup

Figure 4.10: Test Setup of the Low Noise Amplifier for Measurements

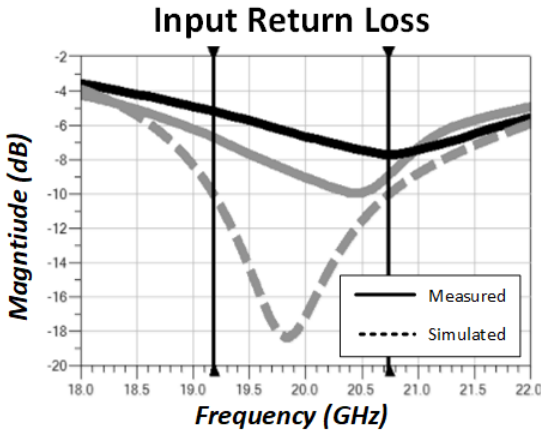
The fabricated circuit was measured using on-wafer probing. The measurement and simulation of this circuit is shown in figure 4.11. A gain of about 20.7 dB, was achieved with a return loss well below 10 dB from 19 - 21 GHz. The measured power consumption of the low noise amplifier is about 6.48 mW.



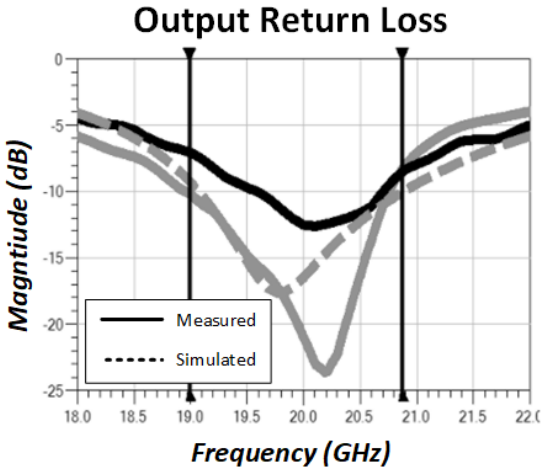
(a) Gain



(b) Reverse Isolation



(c) Input Return Loss



(d) Output Return Loss

Figure 4.11: Simulated and Measured Results of the 2-Stage On-Chip Low Noise Amplifier

The measured input return loss is lower than expected, due to the fact that the impedance of the RF pad of the input terminal was not considered in the simulation. The RF pad produces an equivalent shunt capacitance, which will effect the input matching network of the LNA. Thus, due to the poor input return loss and since we only have equipment that measures the noise figure assuming an ideal 50 Ω is presented at the input terminal. Then, figure 4.12 will only show the simulated noise figure.

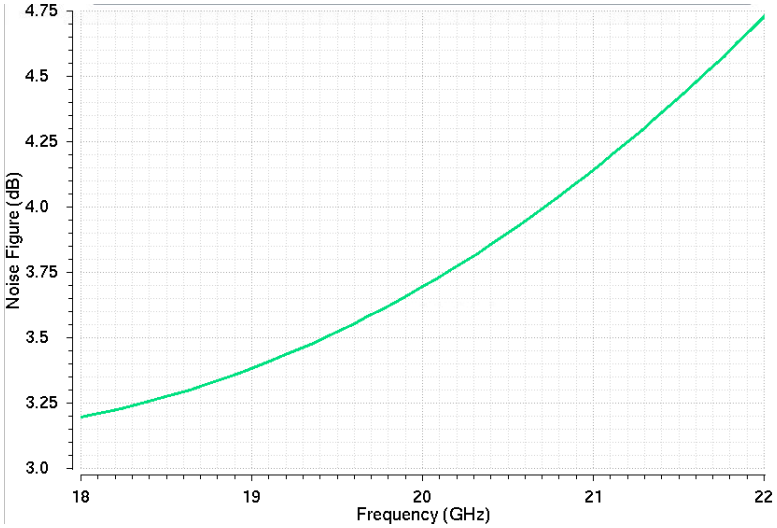


Figure 4.12: Simulated Noise Figure with Parasitic Extraction of On-Chip LNA Layout

Table 4.2: Summary of the Performance of the On-Chip Low Noise Amplifier

Feature	***Value***	
	Simulation	***Measurement***
Frequency (GHz)	20	
Technology	130-nm CMOS	
Gain (dB)	21.1	20.7
Noise Figure (dB)	3.7	N/A
Input Return Loss (dB)	17.5	>6.8
Output Return Loss (dB)	16.8	>13.4
Isolation (dB)	- 48.8	<- 36.5
1-dB Compression Point (dBm)	-24.7	- 25.2
Chip Size (mm^2)	0.785 X 0.640	

Chapter 5

Conclusion and Future Work

5.1 Phase Shifter

The cascaded phase shifter consumes no significant power, achieves a full 360° phase shift range and a reflection coefficient of around 10 dB or greater. However, the insertion loss is higher than what was required in this project. Furthermore, this cascaded phase shifter's optimal performance is at 29.75 GHz. If this phase shifter was to operate at 28 GHz, the insertion loss variation will be a bit more significant and the reflection coefficient will be lower than 10 dB. One way to overcome this problem is to design a compact broadband coupler, such as a transformer based hybrid coupler as shown in figure 5.1.

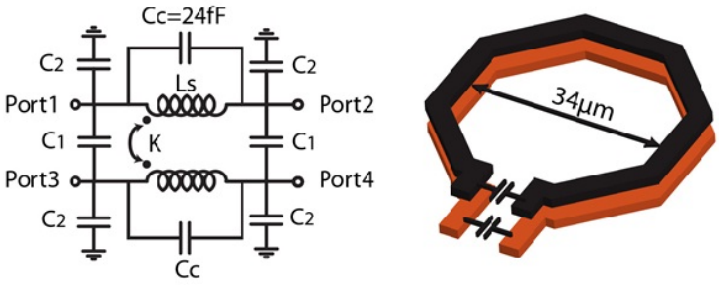


Figure 5.1: Schematic Diagram and Layout of Transformer Based Hybrid Coupler [29]

5.2 Low Noise Amplifier

The values for the off-chip LNA are known. Thus, using equations (1.19) and (1.20), we can compute the specifications for the off-chip LNA assuming an intermediate loss of about 2 dB between the two low noise amplifiers. For the off-chip amplifier we want to design it such that the noise figure is below 1.9 dB, the gain to be above 20 dB, while making sure that the 1 dB compression point is about -43.9 dBm or higher.

Designing a LNA with about 1.9 dB noise figure is going to be a challenge. A LNA with a reasonably low noise figure, high gain and reasonable power consumption must be designed. An example of a LNA with a noise figure of 1.9 dB and a gain of about 17 dB using 0.25μm SiGe BiCMOS technology is shown in [18].

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APPENDICES

Appendix A

Additional Plots

A.1 Simulation of Hybrid Coupler

The simulation of the hybrid coupler using in the reflective type phase shifter is shown in figure A.1.

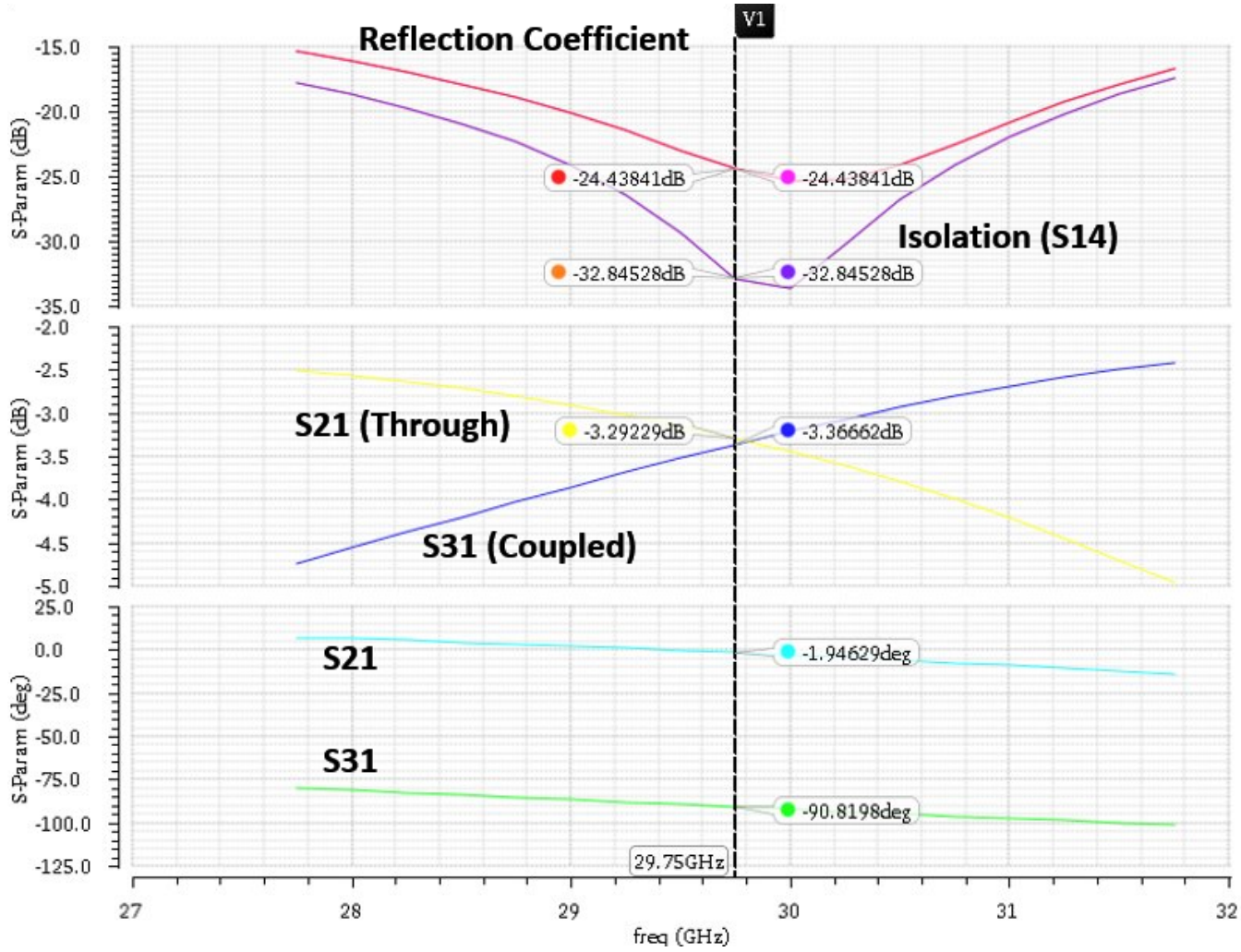

Figure A.1: Simulation of Hybrid Coupler in RTPS