Assessment of Germanane Field-Effect Transistors for CMOS Technology

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Abstract—**Using self-consistent atomistic quantum transport simulations, the device characteristics of n-type and p-type germanane (GeH) field-effect transistors (FETs) are evaluated. While both devices exhibit near-identical off-state characteristics, n-type GeH FET shows ~40% larger on current than the p-type counterpart, resulting in faster switching speed and lower power-delay product. Our benchmark of GeH FETs against similar devices based on 2D materials reveals that GeH outperforms MoS₂ and black phosphorus in terms of energy-delay product (EDP). In addition, the performance of GeH-based CMOS circuit is analyzed using an inverter chain. By engineering power supply voltage and threshold voltage simultaneously, we find the optimal operating condition of GeH FETs, minimizing EDP in the CMOS circuit. Our comprehensive study including material parameterization, device simulation, and circuit analyses demonstrates significant potential of GeH FETs for 2D-material CMOS circuit applications.**

Index Terms—**Germanane, Field-Effect Transistor, Quantum Transport, Device Simulation, CMOS Circuit**

I. Introduction

Two-dimensional (2D) semiconductors such as transition metal dichalcogenides and black phosphorus have been in the spotlight for electronic device components of next-generation complementary metal-oxide-semiconductor (CMOS) technology due to their intriguing electrical and mechanical properties [1], [2]. For instance, a microprocessor based on molybdenum disulfide (MoS_2) has been demonstrated, exhibiting significant potential of 2D semiconductors for integrated circuits [3]. Recently, a new family of 2D materials based on group-IV such as germanane (GeH) and silicene has emerged [4]–[6]. GeH is a light-effective-mass material ($m_e* < 0.1m_0$), and an exceptionally high carrier mobility (>18,000 cm²/V·s) is theoretically predicted [4], while measured mobility of GeH field-effect transistor (FET) is still limited to much lower values (30 cm²/V·s) [7]. With regard to device performance, promising characteristics of GeH FETs have been predicted for high-performance applications [8]–[10]. Although n-type GeH
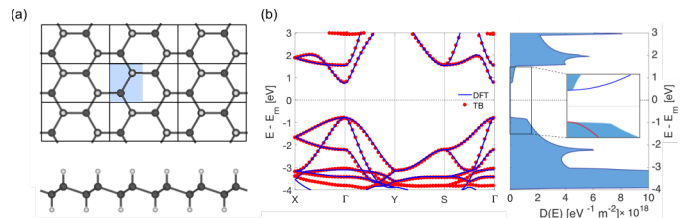
Fig. 1 (a) Top view (top panel) and side view (bottom panel) of GeH supercells chosen for NEGF simulation. Each supercell (black solid box) consists of two unit cells (blue shaded box). (b) (Left panel) Electronic band structure of the GeH supercell from DFT calculation (blue lines). Tight-binding (TB) bands are also shown (red dots), exhibiting excellent matching with the DFT bands. (Right panel) Density of states (DOS) of GeH, showing the significant difference of DOS in the conduction band (E_c) and the valence band (E_v). (Inset) A zoom-in plot of DOS near the band edges, where the velocity of electrons (blue line) and holes (red line) as a function of energy is also provided, showing significantly higher electron velocity.

FETs have been carefully investigated based on atomistic quantum transport simulations [8], in-depth understanding of p-type GeH device is currently absent from the field. Notably, GeH has heavy holes and light holes, which cannot be captured with semi-classical models [10]. Moreover, to assess the GeH-based CMOS circuit performance, the characteristics of both n-type and p-type transistors should be accurately evaluated using rigorous atomistic quantum transport simulations.

The overall goal and the key contribution of this study is to assess GeH-based CMOS technology through rigorous quantum transport simulations of both n-type GeH FET (NMOS) and p-type counterpart (PMOS). For this, first n-type and p-type GeH FETs are investigated individually using self-consistent atomistic quantum transport simulation with tight-binding (TB) parameters extracted from density functional theory (DFT) bands. Second, intrinsic device performance metrics such as intrinsic delay and power-delay product are evaluated and compared against other similar 2D material devices. Finally, circuit-level analyses are conducted to optimize the operating condition of GeH FETs by engineering power supply voltage (V_{DD}) and threshold voltage.

II. Simulation Methods

Electronic properties of GeH are described by TB parameters, which have been achieved through numerical fitting of the DFT band structure [8]. Transport properties are simulated based on the non-equilibrium Green's function (NEGF) method within a TB approximation, while self-consistent electrostatic potential is achieved by solving the Poisson's equation alongside the transport equation [11]. The following parameters are chosen for a nominal device: Monolayer GeH is used for the active material of the device. Channel length (L_{ch}) is 15 nm and source/drain extensions are
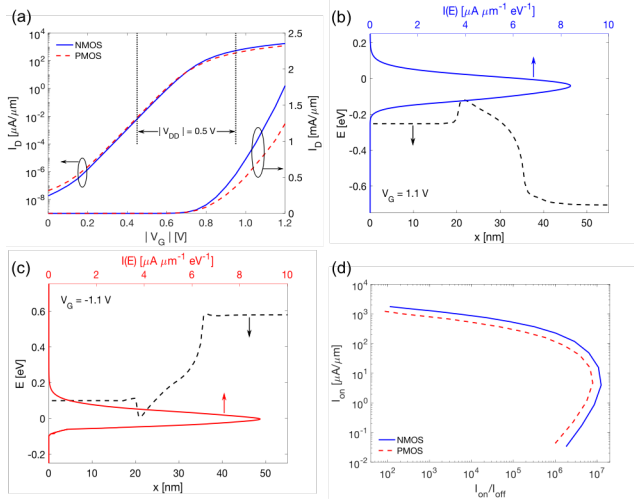
Fig. 2 Transfer characteristics of n-type and p-type monolayer GeH FETs. (a) I_D–$|V_G|$ curves at $|V_D|$ = 0.5 V. V_G and V_D are positive (negative) for the n-type (p-type) transistor. (b) and (c) are energy-resolved current spectrum of the n-type (blue solid line; top axis) and the p-type (red solid line; top axis) GeH FET, respectively, at $|V_G|$ = 1.1 V and $|V_D|$ = 0.5 V. E_c and E_v are also shown in (b) and (c), respectively, along the device (black dashed line; bottom axis). (d) I_{on} vs. I_{on}/I_{off} plotted by shifting the position of the V_{DD} window shown in (a). On (off) state is defined at the right (left) boundary of the V_{DD} window.

Fig. 3 Intrinsic device performance metrics. (a) Intrinsic delay (τ), (b) power-delay product (PDP; left axis) and $Q_{on} - Q_{off}$ (right axis) as a function of I_{on}/I_{off}. (c) PDP–τ relations. (d) Benchmark of GeH FETs against similar FETs based on MoS_2 and black phosphorus (BP). ITRS 2024 requirement (black square) is also shown. The gray dashed guideline represents EDP = 2×10^{-30} J·s/μm.

20 nm. 3.85-nm-thick Al_2O_3 (κ = 9) are used with a single-gate geometry. Source/drain doping concentration is 8.25×10^{12} cm^{-2} for the n-type device, whereas a higher doping concentration of 1.65×10^{13} cm^{-2} is used for p-type GeH considering its larger density of states (DOS). Ballistic transport is assumed due to the relatively short channel length considered in this study. A supercell, consisting of two unit cells [Fig. 1(a)], is chosen to construct a Hamiltonian matrix (H) for the NEGF simulation. The left panel of Fig. 1(b) presents the band structure of the GeH supercell based on both DFT and TB, exhibiting the accurate description of electronic states with TB parameters, which is inherently impossible in semi-classical models. The right panel of Fig. 1(b) shows the DOS of GeH, which reveals that the DOS near the valance band edge (E_v) is ~6× larger than that near the conduction band edge (E_c). In addition, the velocity of carriers is also plotted in the inset of Fig. 1(b), where it can be seen that electrons have significantly higher velocity than holes.

III. RESULTS

Figure 2(a) shows the transfer characteristics of n-type and p-type GeH FETs in both a logarithmic scale (left axis) and a linear scale (right axis). While both devices exhibit near-ideal switching characteristic (SS ~68 mV/dec), it is observed that NMOS has ~40% larger on current than PMOS. To understand this, energy-resolved current spectrum (solid line; top axis) is plotted for the n-type and p-type GeH FET in Figs. 2(b) and 2(c), respectively, along with potential profile (dashed line; bottom axis) in the on state ($|V_G|$ = 1.1 V). It is observed that NMOS has a wider current spectrum compared to PMOS due to the lower potential barrier at the same $|V_G|$. This is attributed mainly to the smaller DOS of n-type GeH, making the modulation of potential barrier by the gate easier. Although charge density in NMOS is limited by its small DOS, NMOS exhibits larger I_{on} than PMOS due to fact that the gain in the
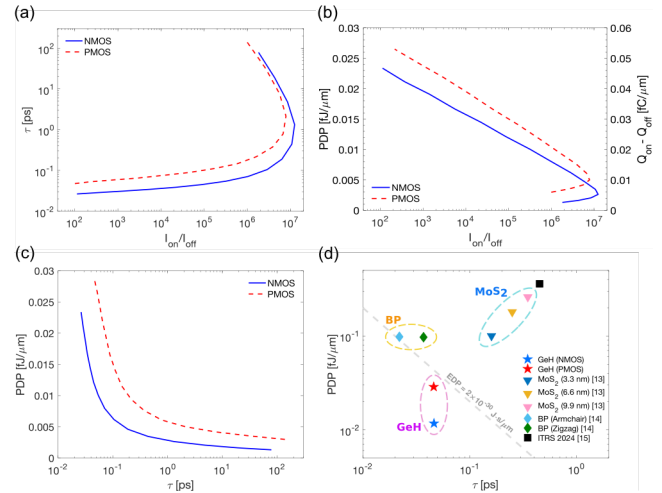
carrier velocity overcomes the loss in charge density [8]. Notably, high carrier velocity in NMOS is the result of both large injection velocity (as shown in the inset of Fig. 1(b)) and large energy window for current flow as explained above. To evaluate both on and off states simultaneously, we plot I_{on} vs. I_{on}/I_{off} in Fig. 2(d) by shifting the V_{DD} window [dotted lines in Fig. 2(a)], which exhibits that NMOS outperforms PMOS device. For the same I_{on} = 500 μA/μm, NMOS shows I_{on}/I_{off} = 1.2×10^5, which is larger than that of PMOS by ~1 order of magnitude.

It will be instructive to investigate the intrinsic performance of the individual GeH FET before circuit-level performance is discussed. Here we evaluate two important device performance metrics: intrinsic delay (τ) and power-delay product (PDP), which correspond to the intrinsic limitation of switching speed and the dynamic power dissipation, respectively. Utilizing the simulation results, the intrinsic device characteristics are evaluated as $\tau = (Q_{on} - Q_{off})/I_{on}$ and PDP = $(Q_{on} - Q_{off})V_{DD}$, where Q_{on} and Q_{off} are the charges at on and off state, respectively [12]. Figure 3(a) shows τ vs. I_{on}/I_{off} for NMOS and PMOS at a constant $|V_{DD}|$ = 0.5 V. Switching speed, or inverse of the delay, of both devices monotonically increases as the V_{DD} window shifts from the subthreshold to the super-threshold region. It should be noted that switching speed of NMOS is faster than that of PMOS at high gate voltages, which is mainly due to the larger on current of NMOS as shown in Fig. 2(a). PDP vs. I_{on}/I_{off} is shown for NMOS and PMOS in Fig. 3(b), where switching energy increases commonly for both NMOS and PMOS as the device switches at higher gate voltages. It was observed that NMOS needs less energy to be switched. It should be noted that the non-monotonic behaviors observed at large delay and small PDP in Figs. 3(a) and 3(b) are attributed to the tunneling component existing at low gate voltages as shown in Fig. 2(a), which is consistent with a previous report [8]. We also plotted PDP-delay trade-off curves in Fig. 3(c), which manifests the inverse relation of switching energy and delay. Energy-delay product (EDP) of transistor is a figure of merit for the intrinsic device performance. The optimal point
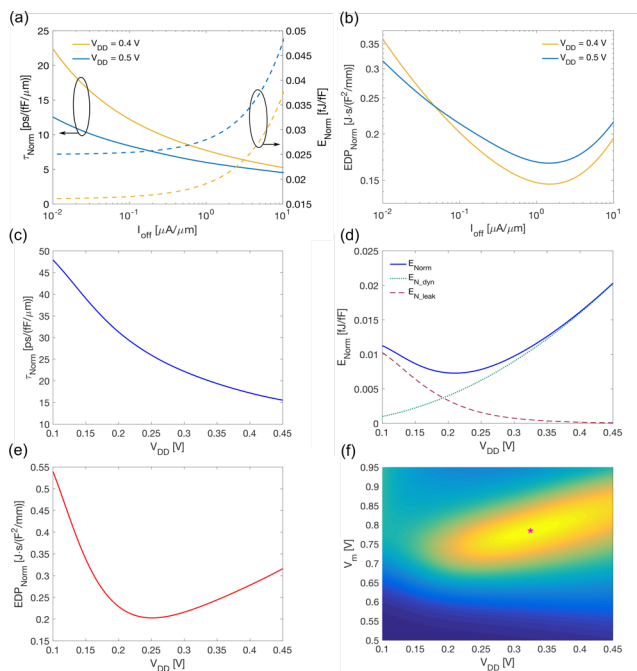
Fig. 4 Optimization of circuit-level figure-of-merits. (a) Normalized propagation delay (τ_{Norm}) and normalized energy (E_{Norm}), and (b) normalized energy-delay product (EDP$_{Norm}$) as a function of I_{off} at V_{DD} = 0.4 V and 0.5 V. (c) τ_{Norm}, (d) normalized total energy (solid line), dynamic energy (dotted line) and leakage energy (dashed line), and (e) EDP$_{Norm}$ as a function of V_{DD} with the mid-point of V_{DD} window fixed at V_m = 0.7 V. (f) Color map of 1/EDP$_{Norm}$ for various V_{DD} and V_m.

can be determined at τ = 46.3 fs and PDP = 11.7 aJ/µm for NMOS and at τ = 46.1 fs and PDP = 28.7 aJ/µm for PMOS, where a product of PDP and τ becomes minimum for each device. These optimal points of GeH-based NMOS and PMOS are plotted in Fig. 3(d), in which other similar 2D semiconductor devices, namely MoS$_2$ FETs [13] and black phosphorus (BP) FETs [14], are also included for comparison along with the ITRS 2024 requirement [15]. In general, 2D-material FETs have fast switching speed and low switching energy as compared to the ITRS 2024 requirement. Among them, GeH FETs exhibit the best performance with the lowest EDP (< 2×10^{-30} J·s/µm).

Next, we discuss the circuit-level performance of GeH FETs. We use normalized propagation delay (τ_{Norm}), normalized energy (E_{Norm}) and normalized energy-delay product (EDP$_{Norm}$) for the circuit-level figure-of-merits (FOMs), following the method used for a similar study [16], [17]. Those circuit-level metrics are evaluated by using a simplified CMOS circuit: 15-stage (L_d = 15), fan-out one (FO1) inverter chain with an average activity factor (α = 0.1) and balanced GeH FETs for NMOS and PMOS. First, we plot the normalized circuit-level FOMs as a function of I_{off} by changing the position of the V_{DD} window for a fixed V_{DD}. While τ_{Norm} can be decreased by increasing I_{off} (i.e., reducing threshold voltage), it comes with the cost of increasing E_{Norm} since the normalized leakage energy becomes dominant in the super-threshold region as shown in Fig. 4(a). Therefore, by considering τ_{Norm} and E_{Norm} simultaneously, the optimum point can be determined. Figure 4(b) presents the normalized energy-delay product as a function of I_{off}. For V_{DD} = 0.5 V, the minimum EDP$_{Norm}$ is 0.17 J·s/(F^2/mm), which is a 47% improvement as

compared to the maximum value observed at I_{off} = 10^{-2} µA/µm. Notably, the minimum EDP$_{Norm}$ can be further reduced by engineering power supply voltage. If V_{DD} = 0.4 V is used, EDP$_{Norm}$ decreases by 13% compared to that with V_{DD} = 0.5 V. This indicates that smaller V_{DD} should be taken into account for the global optimization of operating condition of GeH FETs for CMOS circuits. Therefore, next we investigate the effect of V_{DD}. Figures 4(c)-4(e) show τ_{Norm}, E_{Norm} and EDP$_{Norm}$ as a function of V_{DD}, where the mid-point of V_{DD} window [V_m = (V_{on} + V_{off}) / 2] is fixed at 0.7 V. We have observed a monotonic decrease of τ_{Norm} with increasing V_{DD}, which indicates that the increase of I_{on} is predominant over the increase of V_{DD}. On the other hand, normalized total energy does not exhibit a monotonic trend with V_{DD} since E_{N_dyn} and E_{N_leak} compete with each other as shown in Fig. 4(d). EDP$_{Norm}$ vs. V_{DD} is further plotted in Fig. 4(e), which shows the minimum value of 0.20 J·s/(F^2/mm) at V_{DD} = 0.25 V. Subsequently, we vary both V_{DD} and V_m to find the global optimum point for circuit-level performance of the GeH CMOS inverter chain. A color map of the inverse of EDP$_{Norm}$ in V_{DD} and V_m space is shown in Fig. 4(f). By performing computationally intensive device simulations for different power supply voltages and through careful circuit analyses, the minimum EDP$_{Norm}$ of 0.14 J·s/(F^2/mm) has been achieved at V_{DD} = 0.32 V and V_m = 0.78 V for the GeH-based CMOS inverter chain.

IV. CONCLUSION

In this work, monolayer GeH NMOS and PMOS are evaluated for CMOS technology, based on self-consistent atomistic quantum transport simulations. While both NMOS and PMOS have excellent switching characteristics (SS ~68 mV/dec), n-type GeH exhibits ~40% better on-state performance due to its high carrier velocity, compared to the p-type counterpart. We also calculated intrinsic delay and switching energy of GeH FETs and compared with similar 2D material FETs, exhibiting clear benefits of GeH over MoS$_2$ and BP in terms of energy-delay product. Furthermore, by engineering V_{DD} and threshold voltage, we identified the optimal operating condition of GeH FETs to minimize energy-delay product in CMOS circuits. Our comprehensive study covering material, device and circuit suggests that germanane can be a significant contender for electronic devices of next-generation CMOS technology.

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