Theoretical and Experimental Analysis of Resistor Networks for Use in Superconducting Analog-to-Digital Applications

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

Superconducting micro-electronics (SME) technology is capable of realizing extremely high speed digital receivers performing direct digitization of microwave signals with very low power consumption. SME technology uses integrated circuits based on Josephson junctions and rapid single-flux quantum (RSFQ) logic operating at 4°K. The analogue-to-digital converter (ADC) is a basic building block of such receivers. Quantization and sampling are two fundamental parts of ADCs. Flash ADCs are the fastest converters and consist of comparators and a resistor network.

This thesis investigates the use of a multi-layer niobium-based low-temperature superconducting process to implement a resistor network. Several configurations for resistors are investigated both electrically and thermally. The resistors are designed to maintain their values from DC to 50GHz. Floating metal structures are added and optimized to minimize the inductance of the structure in order to obtain frequency-independent resistors over a frequency range of 50GHz. Several resistors and R-2R ladder networks are fabricated in the same process and measured in an RF cryogenic probe station at the Centre for Integrated RF Engineering (CIRFE) Lab at the University of Waterloo. Theoretical thermal analysis, is also carried out for these resistors to investigate temperature variations through the structures when operating at different power levels. The investigation is important for making sure that the resistors' dissipated heat does not raise the local temperature above the transition temperature of niobium.

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Finally, I would like to express my appreciation to my parents and my beloved husband for their constant and loving motivation. Without their support, I would not have been able to achieve this stage of my life. In gratitude to my husband and parents, I dedicate this work to them.

Table of Contents

AUTHOR'S DECLARATION ii
Abstract iii
Acknowledgements iv
Table of Contents v
List of Figures vii
List of Tables x
Chapter 1 Introduction 1
1.1 Motivation 1
1.2 Objectives 2
1.3 Thesis outline 3
Chapter 2 Literature Survey 4
2.1 Superconductivity 4
2.2 Resistor network 8
2.3 Analog-to-Digital Converter (ADC) 9
2.4 Superconductor lumped elements 14
Chapter 3 Designs and Measurements of Broadband Resistors 17
3.1 MIT LL [17] superconductor technology 17
3.2 Design 19
3.2.1 Designing a coplanar waveguide 19
3.2.2 Designing resistors 21
3.3 R-2R ladder network 28
3.4 Measurements 34
3.4.1 Investigation of discrepancy between EM simulation and measurement results 45
Chapter 4 Thermal Analysis at Cryogenic Temperatures 48
4.1 Cryogenic cooling 48
4.2 Thermal analysis 48
4.2.1 Temperature distribution of 25Ohm resistor in 4K 52
4.2.2 Temperature distribution of 50Ohm resistor in 4K 54
4.2.3 R-2R thermal analysis in 4K 56
4.2.4 Room-temperature thermal analysis of 25Ohm resistor 60

Chapter 5 Conclusion..... 63
Bibliography 64

List of Figures

Figure 1.1. Comparison of digital-RF and conventional receiver architectures. 2
Figure 2.1. Circuit model for complex resistivity in superconductors [7]. 4
Figure 2.2. Surface resistance of a normal conductor campared to different superconductors vs frequency at 77K [7]. 7
Figure 2.3. Voltage division with a resistor network. 8
Figure 2.4. Resistor network: (a) Binary-weighted ladder; (b) R-2R ladder 9
Figure 2.5. Flash ADC: (a) 3-bit conventional Flash ADC; (b) 5-bit superconductor flash ADC. 10
Figure 2.6. Conventional non-clocked comparators: (a) Two-stage open-loop; (b) differential; and (c) threshold inverter quantizer [12]. 12
Figure 2.8. Schematic of quasi-one junction SQUID comparator [13]. 13
Figure 2.9. (a) 3-D model of conventional 50Ohm resistor (Design A), meander 50 Ω resistor (Design B), input resistor and reactance over 40GHz derived from EM simulation. (b) Measured results of a meander resistor with and without floating plate over 20GHz [15]. 16
Figure 3.1. Superconducting electronics scaling trend [18]. 17
Figure 3.2. Cross-section of MIT-LL process [19]. 19
Figure 3.3. 3D schematic of coplanar waveguide [20]. 20
Figure 3.4. (a) 3D schematic; (b) EM simulation of basic 50Ohm CPW in MIT-LL technology. 20
Figure 3.5. (a) 3D schematic; (b) EM simulation of a designed 50Ohm CPW in MIT-LL technology. 21
Figure 3.6. Equivalent π circuit. 22
Figure 3.7. 3D model and EM simulation of 25Ohm resistor: (a) rectangle-shaped resistor; (b) meander-shaped resistor; (c) meander-shaped resistor with floating metals. 23
Figure 3.8. 3D model and EM simulation of 1-port 25Ohm. 24
Figure 3.9. 3D model and EM simulation of (a) 1-port 37.5Ohm and (b) 2-port 37.5Ohm. 25
Figure 3.10. 3D model and EM simulation of (a) 1-port 50Ohm and (b) 2-port 50Ohm. 26
Figure 3.11. 3D model and EM simulation of improved 1-port 50Ohm. 27
Figure 3.12. 3D model and EM simulation of (a) 1-port 75Ohm and (b) 2-port 75Ohm. 28
Figure 3.13. 3D model and EM simulation of CPW T-junction using MIT-LL technology 29
Figure 3.14. 3D model and EM simulation of CPW 90-degree turn using MIT-LL technology. 30

Figure 3.15. a) Schematic and ideal simulations; b) 3D model and EM simulation of 1-bit R-2R ladder. 31
Figure 3.16. a) Schematic and ideal simulations; b) 3D model and EM simulation of 2-bit R-2R ladder. 32
Figure 3.17. a) Schematic and ideal simulations; b): 3D model and EM simulation of 4-bit R-2R ladder. 33
Figure 3.18. Schematic of stages of Lakeshore probe station chamber and temperatures [23]. 34
Figure 3.19. CPW taper used for measurements. 35
Figure 3.20. 3D schematic and EM simulation and measurement results of 2-port 25Ohm resistor with taper. 36
Figure 3.21. 3D schematic and EM simulation and measurement results of 1-port 25Ohm resistor with taper. 37
Figure 3.22. 3D schematic and EM simulation and measurement results of 2-port 37.5Ohm resistor with taper. 38
Figure 3.23. 3D schematic and EM simulation and measurement results of 1-port 37.5Ohm resistor with taper. 39
Figure 3.24. 3D schematic and EM simulation and measurement results of 2-port 50Ohm resistor with taper. 40
Figure 3.25. 3D schematic and EM simulation and measurement results of 1-port 50Ohm resistor with taper. 41
Figure 3.26. 3D schematic and EM simulation and measurement results of 2-port 75Ohm resistor with taper. 42
Figure 3.27. 3D schematic and EM simulation and measurement results of 1-port 75Ohm resistor with taper. 43
Figure 3.28. 3D schematic and EM simulation and measurement results of 1-bit R-2R ladder with taper. 44
Figure 3.29. 3D schematic of vias in a) fabrication and b) EM simulation. 46
Figure 3.30. Different box sizes in Sonnet. 47
Figure 3.31. S11 of two identical circuits with different box sizes in Sonnet. 47
Figure 4.1. Image of samples mounted on the chuck. 49
Figure 4.2. 3D model of 25Ohm resistor in COMSOL 50

Figure 4.3. 2D schematic of resistor in COMSOL showing electric current setting. 52
Figure 4.4. Temperature distribution through substrate and fabricated TL and 25Ohm resistor by applying 1 volt at cryogenic; maximum temperature 5.37K. 53
Figure 4.5. Temperature distribution through substrate and fabricated TL and 25Ohm resistor by applying 1.5 volts at cryogenic; maximum temperature 8.33K. 53
Figure 4.6. Temperature distribution through substrate and fabricated TL and 25Ohm resistor by applying 2 volts at cryogenic; maximum temperature 12.5K..... 54
Figure 4.7. Temperature distribution through substrate and fabricated TL and 50Ohm resistor by applying 1 volt at cryogenic; maximum temperature 3.79K. 55
Figure 4.8. Temperature distribution through substrate and fabricated TL and 50Ohm resistor by applying 2 volts at cryogenic; maximum temperature 6.16K..... 55
Figure 4.9. Temperature distribution through substrate and fabricated TL and 50Ohm resistor when applying 3 volts at cryogenic; maximum temperature 10.1K..... 56
Figure 4.10. Schematic of 1-bit R-2R ladder..... 56
Figure 4.11. Electric potential in an R-2R ladder by injecting a 0.06A current. 57
Figure 4.12. Temperature distribution in 1-bit R-2R structure when applying 1 volt at cryogenic; maximum temperature 3.51 K. 57
Figure 4.13. Temperature distribution in 1-bit R-2R structure when applying 2 volts at cryogenic; maximum temperature 5.05 K. 58
Figure 4.14. Temperature distribution in 1-bit R-2R structure when applying 3 volts at cryogenic; maximum temperature 7.61 K. 59
Figure 4.15. Temperature distribution in 1-bit R-2R structure when applying 3.5 volts at cryogenic; maximum temperature 9.27K. 60
Figure 4.16. Temperature distribution in 25Ohm resistor structure when applying 1 volt at room temperature; maximum temperature 295 K. 61
Figure 4.17. Temperature distribution in 25Ohm resistor structure when applying 1.5 volts at room temperature; maximum temperature 298 K. 62
Figure 4.18. Temperature distribution in 25Ohm resistor structure when applying 2 volts at room temperature; maximum temperature 303K. 62

List of Tables

Table 4-2. Material Properties of Silicon 51
Table 4-3. Material Properties of Silver 51

Chapter 1
Introduction

1.1 Motivation

The convenience and advantages of copying, processing, analyzing and storing in digital format necessitate using analog-to-digital conversion (ADC) methods. An enormous amount of information is currently available highlighting the importance of improving conversion between analog and digital domains. Specific benefits of using superconductor technology for data conversion applications include high speed switching, low power consumption, quantum precision, natural quantization of magnetic flux, and noise reduction of cryogenic superconductor circuits [1]. Unfortunately, however, the growth in convectional silicon technology does not allow for much improvement in data converters, especially with regard to recent advancements in the digital domain.

Rapid single-flux quantum (RSFQ) logic is the superconductor technology used in data converters. RSFQ circuits are based on superconductor quantum effects which have intrinsic digital logic. A current circulating in a superconducting loop generates a magnetic field that is quantized and leads to flux quantization. Fluxon or flux quantum, which is the unit of quantization, has a value of $\frac{h}{2e} = 2.07 * 10^{-15}$ Wb=2.07 mV.ps (h is the Planck constant and e is the electron charge) [2]. In RSFQ, quantized fluxons are the same as the quantized voltage in complementary metal-oxide semiconductor (CMOS) digital circuits, and bits are shown by either the presence or absence of fluxons rather than zero and one. Josephson junctions (JJs) are the basis of this technology as transistors in CMOS devices.

As wireless communication rapidly advanced in the 1990s, it faced several problems. The solution to those problems was to use a software-defined radio (SDR) concept. Having an ultra-fast and linear ADC with low noise, large dynamic range, and high sensitivity was the requirement for implementing a wideband SDR. Specific properties of superconductors make it feasible to design such ADCs. In digital-RF receivers, data conversion takes place at the RF, whereas in conventional receivers, the data conversion occurs in the baseband. In conventional architecture, RF signals pass through filters and down converters, after which they are digitized. These components are excluded in digital-RF architecture. A wideband digitized RF signal is applied to an RF digital signal processing (DSP) unit.

Figure 1.1 illustrates the differences between conventional and RF-digital receivers. RF DSP allows for the implementation of distinct functions as digital beamforming, digital signal combining, correlation-based digital filters, and adaptive active cancellation of transmission channels [3]. In 2004, HYPRES

[4] designed the first digital-RF receiver chip using the 1KA/cm^2 process. This chip was tested up to a clock rate of 20GHz [5].

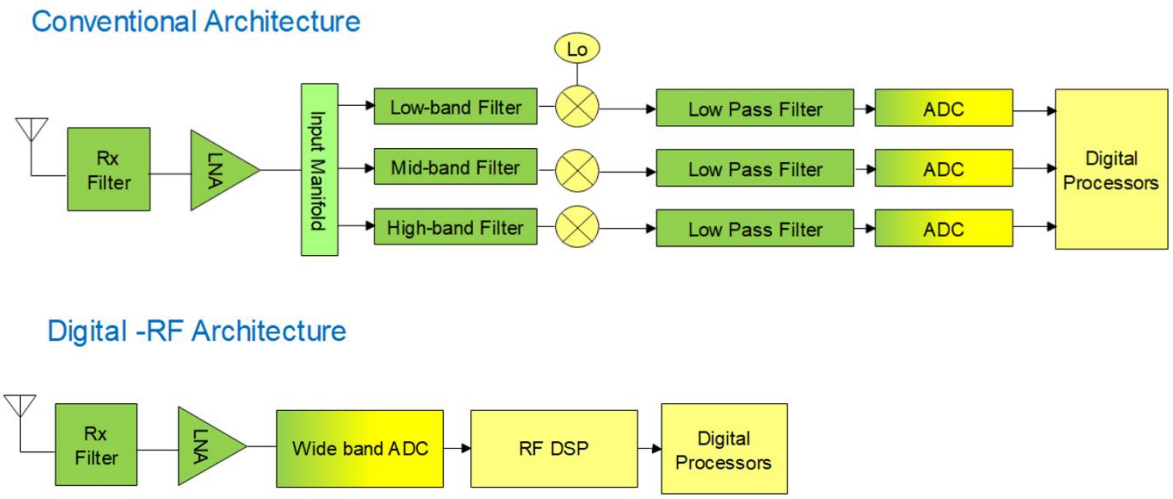


Figure 1.1. Comparison of digital-RF and conventional receiver architectures.

1.2 Objectives

The purpose of this thesis is to design a broadband multi-layer superconducting resistor network for superconducting analog-to-digital converters. Such ADCs include quantization and sampling, which are the two fundamental parts of each ADC. In superconducting ADCs, quantization is done through a resistor network to provide various reference voltages. Therefore, the performance of resistors is important in a resistor network to ensure accurate voltage levels.

Several 25, 50, 37.5, and 75 Ohm resistors are designed and fabricated. Fabrication was carried-out at the Massachusetts Institute of Technology Lincoln Laboratory (MIT-LL) in an 8-layer niobium-based process. MIT-LL's process allows for the use of a resistor layer to design miniaturized resistors. However, the challenge in this design is that resistors should maintain their values over a wide range of frequencies, which is difficult to accomplish as the frequency increases. Floating metals are added either on top or below the resistor layer to cancel out the inductance effect of the structure in order to obtain frequency-independent resistors over a 50GHz span and maintain their magnitude with a 1% error. The designed resistors are used in 1-bit, 2-bit, and 4-bit R-2R ladders and their performance is analyzed. The resistors and 1-bit R-2R ladder are all fabricated and measured in a cryogenic probe

station at the Centre for Integrated Radio Frequency Engineering (CIRFE) Lab at the University of Waterloo, Waterloo, Ontario, Canada.

In the second part of this thesis, thermal analyses are performed for the designed resistors and 1-bit R-2R ladder, to investigate how temperature is changed through the structure by applying different power levels. The heat dissipated in the resistor layer raises the local temperature in the structure above the critical temperature of niobium.

1.3 Thesis outline

Following the motivations and objectives sections in this chapter, some background information and a literature review are presented in Chapter 2. In that chapter, surveys are conducted on superconductors, resistor networks, and analog-to-digital converters.

In Chapter 3, multi-layer wideband resistors are designed based on a low-temperature superconducting process to implement resistor network. The process, which is offered by MIT-LL, is an 8-layer niobium-based fabrication method further described in Chapter 2. The designed resistors are implemented in 1-bit, 2-bit, and 4-bit R-2R ladder networks and the results analyzed. Several resistors and a 1-bit R-2R ladder are fabricated in the same process, with the measured results being presented in the chapter.

The focus of Chapter 4 is on thermal analyses of the designed resistors and 1-bit R-2R ladder network to investigate temperature distribution in different power levels at cryogenic temperatures.

Chapter 5 concludes the thesis and presents some suggestions for future work.

Chapter 2
Literature Survey

2.1 Superconductivity

The main difference between normal metals and superconductors is the carriers, which, in normal metals, are electrons and in superconductors are electron pairs (Cooper pairs). Cooper pairs conduct an electrical current with very small resistance (zero at DC and finite at microwave frequencies). According to Barden, Cooper, and Schrieffer's (BCS) theory, at the critical temperature (T_C), which is a specific temperature for every material, the number of normal electrons is decreased and they start pairing up into Cooper pairs. Cooper pairs do not exist at transition temperatures or at higher temperatures [6].

As shown in Equation 2.1, the conductivity σ of a superconductor is a complex quantity, which can be modeled as a parallel resistor and inductor (see Figure 2.1).

$$J = J_n + J_s = (\sigma_1 - j\sigma_2)E \qquad (2.1)$$

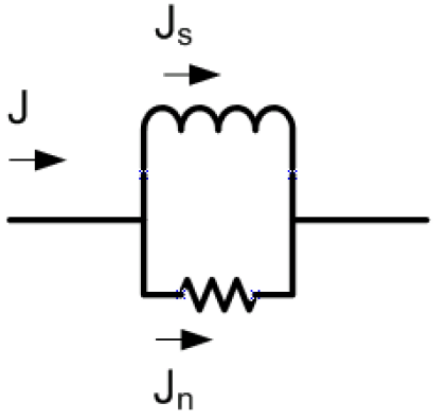


Figure 2.1. Circuit model for complex resistivity in superconductors [7].

At DC, the inductor has no resistivity and acts as a wire, so all the current goes through the inductor, which is lossless. At low frequencies, the inductor has lower impedance compared to the resistor, but

at high frequencies, the inductor has high impedance so the current travels through the resistor. Resistor values show a loss in superconductors at high frequencies.

By substituting the complex conductivity of superconductors in conventional equations for conductors, the propagation constant and intrinsic impedance of superconductors can be calculated from the following equations:

$$\gamma = \sqrt{j\omega\mu(\sigma_1 - j\sigma_2)} \tag{2.2}$$

$$Z_s = \sqrt{\frac{j\omega\mu}{\sigma_1 - j\sigma_2}} \tag{2.3}$$

where ω is the angular frequency and μ is the permeability of free space. Assuming that the superconductor is working below the critical temperature ($\sigma_2 \gg \sigma_1$), both the propagation constant and intrinsic impedance can be simplified as:

$$\gamma = \alpha + j\beta = \sqrt{\omega\mu\sigma_2}(1 + j\frac{\sigma_1}{2\sigma_2}) \tag{2.4}$$

$$Z_s = R_S + j\,X_s = \sqrt{\frac{\omega\mu}{\sigma_2}}(\frac{\sigma_1}{2\sigma_2} + j) \tag{2.5}$$

where α and β are attenuation and phase constants, respectively, and R_s and X_s are surface resistance and reactance, which can be formulated as a function of penetration depth (λ). R_s and X_s represent the resistor and inductor in a superconductor circuit model (shown in Figure 2.1), in which case they are called surface resistance and kinetic inductance, respectively. Penetration depth is similar to skin depth in a conductor and determines how far an electromagnetic wave can travel through a superconductor.

$$\lambda = \sqrt{\frac{1}{\omega\mu\sigma_2}} \tag{2.6}$$

$$\alpha = \sqrt{\omega\mu\sigma_2} = \frac{1}{\lambda} \tag{2.7}$$

$$\beta = \sqrt{\frac{\omega\mu\sigma_1^2}{4\sigma_2}} = \frac{\omega\mu\lambda\sigma_1}{2} \tag{2.8}$$

$$R_s = \frac{\omega^2\mu^2\sigma_1\lambda^3}{2} \tag{2.9}$$

$$X_s = \sqrt{\frac{\omega\mu}{\sigma_2}} = \omega\mu\lambda \tag{2.10}$$

Penetration depth, as opposed to skin depth, is independent of frequency, since σ_2 is inversely proportional to frequency $\left(\sigma_2 \propto \frac{1}{\omega}\right)$. As shown in Equation 2.9, surface resistance in a superconductor is proportional to f^2, whereas in a conductor, resistance varies with frequency, as in $\sqrt{f}$. Therefore, in high frequencies, superconductors can show more resistivity than conductors. Figure 2.2 depicts the surface resistance of various superconductors (Nb and YBCO) compared to a normal conductor (Cu) at 77°K versus frequency. It shows that the surface resistance of superconductors is smaller than that of the conductor up to 1THz, after which point their resistivity is higher than that of normal conductors [7].

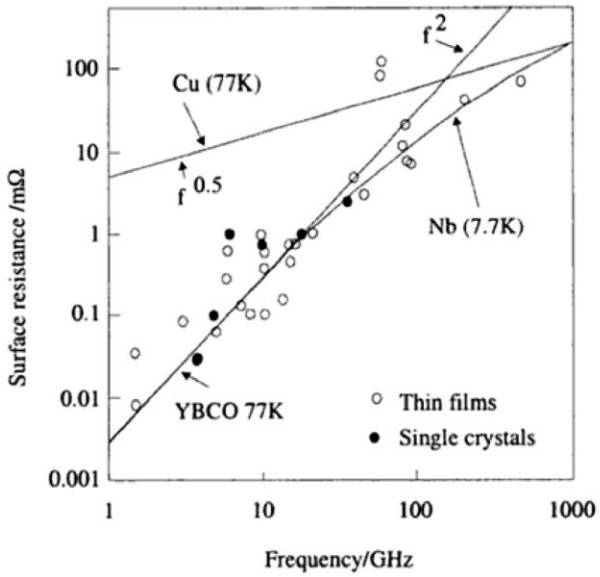


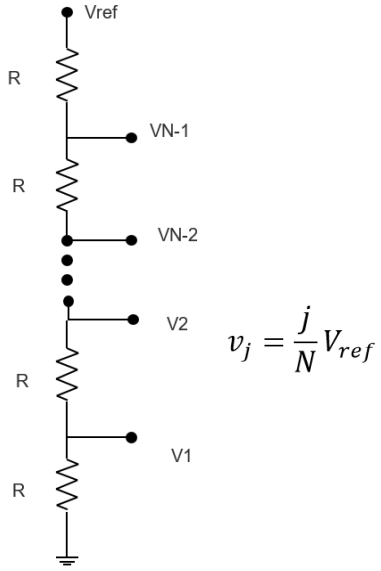
Figure 2.2. Surface resistance of a normal conductor campared to different superconductors vs frequency at 77K [7].

Superconductors are categorized as low-temperature or high-temperature according to their critical temperature. The critical temperature of low-temperature superconductors (LTS) is lower than 23°K while high-temperature superconductors (HTS) have a critical temperature as high as 161°K [8]. Although cooling of HTS is cheaper than LTS, their fabrication process is more complicated than LTS (such as niobium-based), which makes LTS more suitable for mass production.

The low insertion loss, light weight, low volume and small size of superconductors make it feasible to design lumped elements, in contrast to metallic microwave devices where miniaturization would deteriorate their performance. The Josephson junction is a weak link between superconductors that consists of an insulating barrier. According to Faraday's law ($v = \frac{d\phi}{dt}$), the voltage across the Josephson junction in a superconducting loop is a pulse known as a single-flux quantum (SFQ) pulse. SFQ pulses have a duration of 2ps and a magnitude of 1mv. An SFQ pulse is the basis for rapid SFQ logic, which makes the fastest digital circuits feasible. Superconductor Quantum Interference Devices (SQUID) are inductor loops containing one or more Josephson junction(s). They are highly sensitive to the magnetic field and thus are used as sensitive magnetometers [9].

2.2 Resistor network

The multiplication or division of voltages, currents, and charges are implemented through resistor ladders, current steering circuits and switched capacitors, respectively. In this thesis, the focus is on voltage division, as several voltage levels are required in designing an analog-to-digital converter. A resistor network is the most economical way to achieve voltage division. A given reference voltage can be divided into N equal segments using a ladder comprising N identical resistors (Figure 2.3). In this structure, small mismatches in resistors lead to nonlinearity in digital-to-analog conversion. Moreover, as the number of bits increases, the number of resistors grows exponentially (2^N resistors) and contributes to a long delay at the output. Consequently, other resistor ladder structures are introduced.

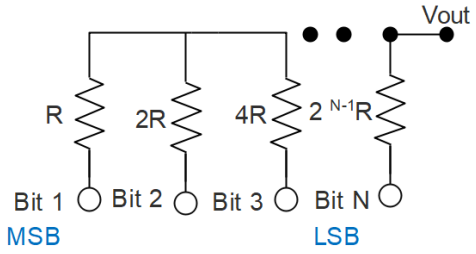


$$v_j = \frac{j}{N} V_{ref}$$

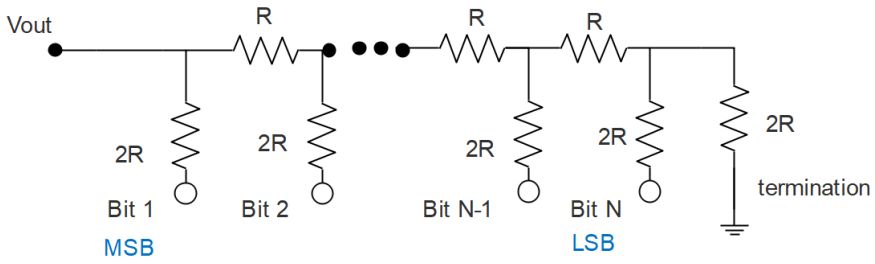
Figure 2.3. Voltage division with a resistor network.

Two popular resistor networks are binary-weighted and R-2R ladder. A binary-weighted resistor network, as shown in Figure 2.4 (a), is composed of N resistors which are double multiples of R. In this approach, the ratio between values of resitors increases as the number of bits grows. The challenge in this method is that it would be difficult to implement precise resistors for N>10 on a single chip, since there would be a great difference between the smallest and largest resistors (at a ratio of 2^{N-1}). On the other hand, an R-2R ladder has inherent accuracy, and since it only has R and 2R resistors, it relaxes the device scaling requirements. In an R-2R ladder network, there is a termination resistor which assures input impedance of the network to be R when all the bits are grounded. The resolution of an R-

2R ladder is determined by the number of bits. Because input bits are switched between the ground and a reference voltage (Vref) and Vout varies between 0 and Vref, 2^N combinations at the input of the ladder are possible. The resolution is the change in the LSB which marks the smallest change in the output given by $1/2^N$. Furthermore, the accuracy of the R-2R ladder is independent of the value of R and it is only crucial that the resistors be well-matched to achieve an accurate ladder. In fact, the voltage ratio between two consequent bits should be two to have an accurate ladder [10].



(a)



(b)

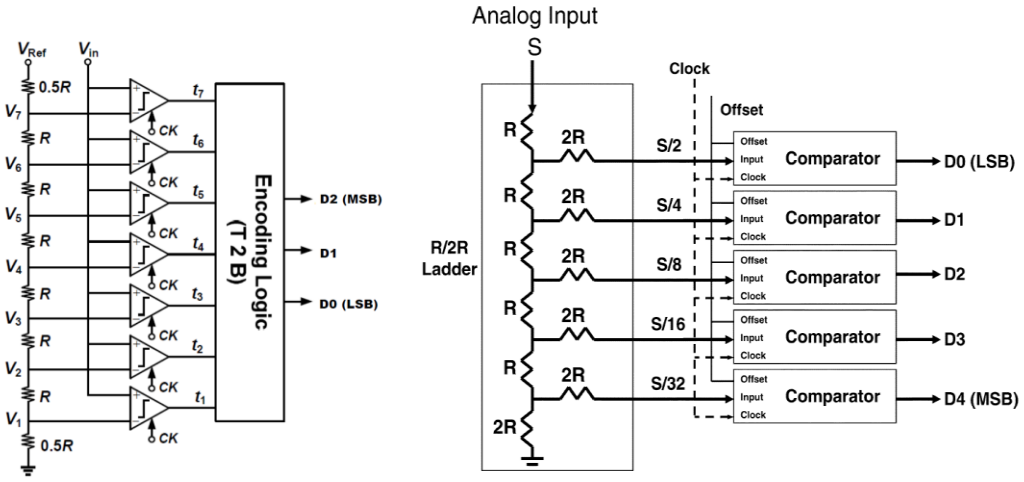
Figure 2.4. Resistor network: (a) Binary-weighted ladder; (b) R-2R ladder

2.3 Analog-to-Digital Converter (ADC)

An analog-to-digital converter (ADC) is a circuit which converts an analog signal (like a continuous voltage or current) to a digital signal at a specific rate (fs). It employs N binary bits, exploiting quantization (magnitude discretization) and sampling (time discretization). ADCs are categorized into two distinct classes according to their sampling frequencies: *Nyquist-sampling* and *oversampling* ADCs. A Nyquist ADC samples a limited bandwidth signal at $f_s = 2f_N$ using several separate quantizers. However, an oversampling ADC samples with a frequency of $f_s \gg 2f_N$ with a single quantizer. This thesis focuses on Nyquist-rate ADCs.

Flash ADC is a Nyquist-rate ADC in which sampling and quantization are performed simultaneously. This does not only make flash the fastest (1 clock cycle per conversion) ADC among all types of ADCs, but its fast conversion speed renders it an optimal converter in wideband applications. This ADC has a large number of quantizers (single-bit comparators) defining quantization levels. These quantization levels determine the accuracy of ADCs, which depends on the resistor values in resistor networks. The main drawback of flash ADCs is the number of comparators, $2^N - 1$, which exponentially grows as the number of bits increases. Hence, it is not applicable for a large number of bits, as the circuit then becomes too complicated. By using superconductors, however, this complexity is reduced and the number of comparators reduced to N [11].

Figure 2.5 illustrates the resistor network and comparators of a 3-bit conventional and 5-bit superconductor flash ADC. Figure 2.5 (a), which is a 3-bit semiconductor ADC, has 7 (2^N-1) comparators, while in Figure 2.5(b), a 5-bit superconductor ADC has only 5 (N) comparators. It is shown in Figure 2.5 (b) that the input signal travels through the resistor network and consecutively is divided by a factor of two. Thereafter, they are applied to single-bit comparators.



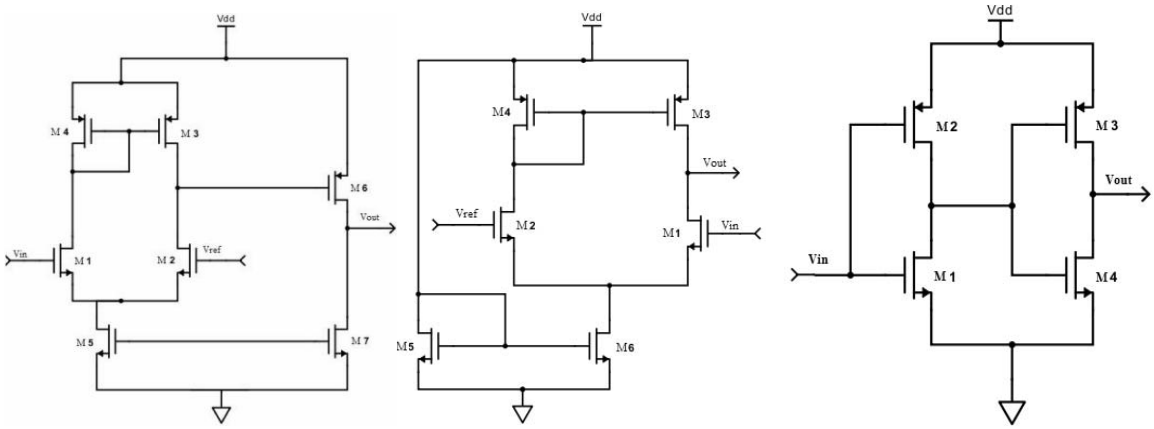
(a) (b)

Figure 2.5. Flash ADC: (a) 3-bit conventional Flash ADC; (b) 5-bit superconductor flash ADC.

A conventional flash ADC (Figure 2.5 (a)) consists of 2^N-1 comparators and a resistor ladder that includes 2^N resistors and generates a reference voltage for each comparator. There is one Least Significant Bit (LSB) difference between the two consequent comparators: When the input voltage is

greater than the reference voltage, the output of the comparator will be ‘1’; otherwise, it generates ‘0’. The thermometer code of the input signal is generated at the output of the comparators and afterwards is converted to binary code. There are numerous reports in the literature about decreasing the complexity, power, and area of CMOS flash ADCs while maintaining high speed and performance. The comparators are the main components which limit the performance of the flash ADC, with clocked and non-clocked comparators being used according to the specifications of the ADC. Clocked comparators are power-hungry and more complicated than non-clocked ones.

Two-stage open-loop, differential, and threshold inverter quantizers (TIQs) are examples of different non-clocked comparators. A two-stage open-loop comparator, as depicted in Figure 2.6 (a), includes two stages: the first has high gain and the second has high stability. The input stage consists of a differential pair and a current mirror and the output stage is a common source. There is a trade-off between gain and bandwidth, such that the greater the gain, the smaller the bandwidth. Moreover, the decision speed in a comparator relies on the bandwidth. A differential comparator includes two current mirrors and a differential pair. One current mirror provides the biasing voltage of the circuit and the other converts the current for the differential pair to output voltage (as shown in Figure 2.6 (b)). By increasing the length of transistors, gain will likewise increase, but it will also increase the power consumption and delay of the comparator. The threshold inverter quantizer comparator illustrated in Figure 2.6(c) is a single-ended circuit and has no external reference voltage. The W/L ratio of the transistors in the first stage determines an internal reference voltage, while the second stage provides the voltage gain [12].



(a) (b) (c)

Figure 2.6. Conventional non-clocked comparators: (a) Two-stage open-loop; (b) differential; and (c) threshold inverter quantizer [12].

In 1975, the idea of designing a flash ADC by using the periodic nature of SQUIDs was proposed by H. Zappe [13]. Using superconducting technology allows the number of comparators to be reduced to *N* rather than 2^N-1. This design demonstrates faster sampling as well as reduced circuit complexity. The pioneer flash ADC exploited the superconductor's natural magnetic flux quantization and high sensitivity of SQUIDs to magnetic fields. The first ADC design used different SQUID comparators, making its implementation relatively complicated.

Then, in 1979, R. Harris, C. Hamilton and F. Lloyd designed a 200 MS/s, 4-bit flash ADC using identical SQUIDs [13], as depicted in Figure 2.7. They later improved their design and presented a 6-bit flash ADC with a sampling rate of 4 GS/s. In 1988, an ADC with a sampling rate of 5GHz was implemented with a 3-um $Nb/AlO_x/Nb$ process in Fujitsu. That same year, a quasi-one junction SQUID (QOS) comparator (shown in Figure 2.8) was invented at UC Berkeley. This invention improved the analog bandwidth and sampling rate significantly (more than five-fold) [13]. The QOS comparator consists of a single junction SQUID (L and Jo) and a pair of Josephson junctions (J1 and J2), which are called the decision-making pair. Based on the input clock, one of the junctions switches to resistor when the current (I_{loop}) is clockwise; J2 is thus in a resistor state and pulls the digital output to "1". Meanwhile, with a counter-clockwise current, the output is pulled down to "0" through J2 [11].

Current ADC comparator design is based on a QOS comparator. In 1993, a 6-bit flash ADC with 4 and 3 effective numbers of bits, respectively, at 5 and 10GHz was proposed by HYPRES[4]. In this ADC,

an R-2R ladder delivers an input analog signal to 6 QOS comparators. Cryogenic packaging was designed for this flash ADC by HYPRES, which signifies the first superconducting digital and mixed-signal LTS-integrated circuit 4°K closed-cycle refrigerator [13].

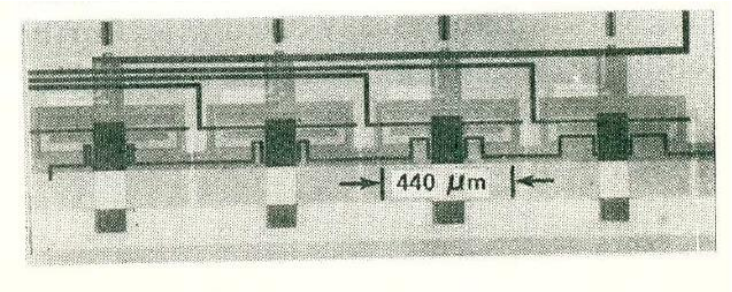


Figure 2.7. First superconducting 4-bit flash ADC in 1979 [13].

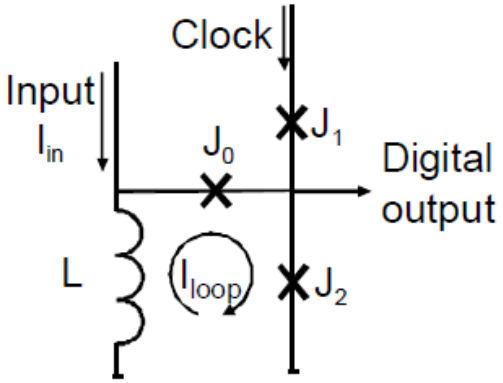


Figure 2.8. Schematic of quasi-one junction SQUID comparator [13].

Superconductor ADCs require a considerable number of Josephson junctions, which categorizes them as medium-sized integrated circuits. Even if a miniaturized ADC is designed, systems such as digital filters and demultiplexers include thousands of JJs, which makes the systems large. The majority of superconductor ADCs are LTS niobium-based, operating at 4°K. Reducing the size, power, and weight of cryogenic packaging is the main motivation for designing ADCs in high-temperature superconductors. Moreover, HTS ADCs are expected to show fast speed. However, the fabrication processes of HTS are so complex that despite major efforts, the progress in this area is slow. On the other hand, cryogenic packaging for 4°K is progressing swiftly, which can make LTS the leading technology for ADCs [13].

Research on designing an ADC with HTS technology has resulted in some progress in this field, including a 4-bit flash ADC based on a quasi-one junction SQUID comparator designed in 1997 by G. Gerritsma et al. [13], in which the comparator demonstrated low speed. In 2004, a high-speed QOS comparator based on HTS was designed by H. Sugiyama et al. This comparator demonstrated good performance at a clock frequency of 94 and 77GHz at 35 and 40K, respectively [13].

2.4 Superconductor lumped elements

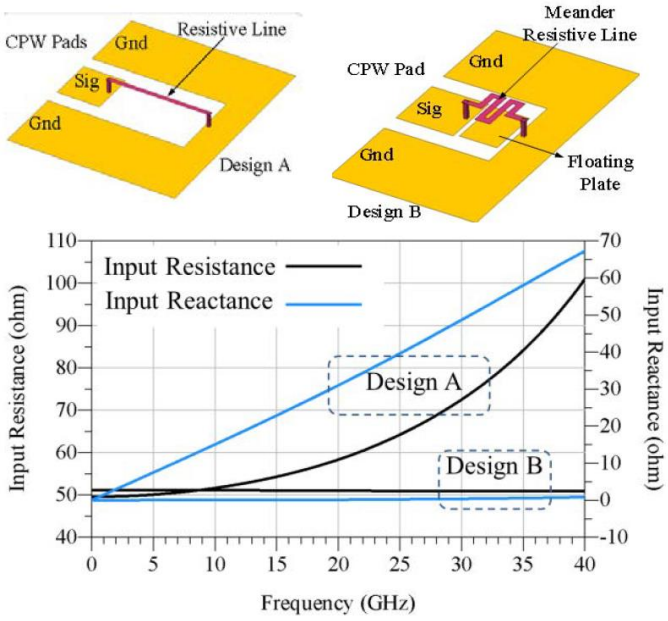
In lumped elements, the voltage and current through the conductors connecting the elements is the same and Ohm's law is applicable. At microwave frequencies, standard circuit theory fails to solve network problems and lumped elements cannot be used as easily. Lumped elements can, however, be exploited in Microwave Integrated Circuits (MIC), if their dimensions are smaller than operating wavelength such that there is no phase shift between input and output terminals. A good rule of thumb for lumped elements is to keep the dimensions smaller than $\frac{\lambda}{20}$, where λ is the wavelength. Although lumped elements exhibit more loss than distributed circuits, their small size and low cost make them a suitable option in MIC [14].

As the dimensions of microwave devices decrease, their performance, such as, insertion loss degrades. This issue can be solved by using superconductors. Furthermore, because superconductors have lower surface resistance than conventional conductors used in microwave devices, replacing metals such as copper and gold in microwave devices with superconductors reduces the insertion loss significantly. Therefore, superconducting lumped elements make it feasible to miniaturize microwave devices without degrading their performance.

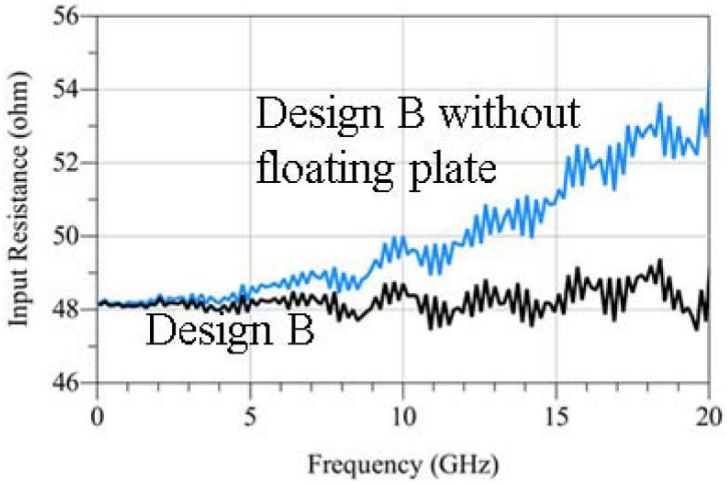
The drawback of using superconductors is the cryogenic packaging and their compatibility to other parts of the circuitry. Liquid nitrogen (77°K) and liquid helium (4°K) are used for cooling of HTS and LTS, respectively. Hence, the accuracy and complexity of cryogenic systems limit a superconductor's applications.

A broadband miniaturized LTS resistor is shown in Figure 2.9. The resistive metal layer existing in each technology has a sheet resistance, so a rectangle can be used to provide the required resistor at low frequencies, as shown in Design A. Due to parasitic inductance and capacitance at high frequencies, the values of resistors vary at high frequencies. A novel design is proposed in Design B to have a constant resistance over a wideband. A meander line is used rather than a straight line for the resistor. This topology minimizes the size and reactance of the structure. The opposite direction of the current

in adjacent legs of the meander resistor lowers the effects of inductance. A floating plate is added to the design to minimize variations over frequency. Floating metal can also be added on top of or below the meander resistor to add a capacitor to cancel out the structure's inductance. Simulation results of the proposed resistor in Figure 2.9 (a) show a frequency-independent impedance up to 40GHz. Measurement results depicted in Figure 2.9 (b) show an input resistance of the proposed resistor over 20GHz. Input resistance in the measured results starts from 48 Ohm and is caused by fabrication tolerances; otherwise, it shows reasonable results [15].



(a)



(b)

Figure 2.9. (a) 3-D model of conventional 50 Ohm resistor (Design A), meander 50 Ω resistor (Design B), input resistor and reactance over 40GHz derived from EM simulation. (b) Measured results of a meander resistor with and without floating plate over 20GHz [15].

Chapter 3
Designs and Measurements of Broadband Resistors

The sheet resistance of resistive metal layers for each fabrication is known according to the resistive material and the thickness of the layer. The conventional approach to designing a resistor with sheet resistance is to design a rectangle with proper L/W ratio. Using this approach, the design parameters are limited to the length and width of the rectangle. However, according to the application, the required current determines the width. In this thesis, the width of the resistor is set to 30um; therefore, taking the conventional approach, the only parameter to play with for designing different resistors is the length (L). In this chapter, a brief review of fabrication technology is conducted, after which the design procedure and results are elaborated. All of the structures are designed and simulated in Sonnet [16].

3.1 MIT LL [17] superconductor technology

In superconductor technology, the number of Josephson junctions (JJs) determines the performance of superconductor-integrated circuits as a transistor in CMOS technology. According to Figure 3.1, which shows the rate of JJs growing from 1990 to 2020, the number of JJs doubled every 4.5 years in an integrated circuit. However, according to Moore's law, the growth rate of transistors in integrated CMOS circuits is four times greater than superconductors and doubles every two years [18].

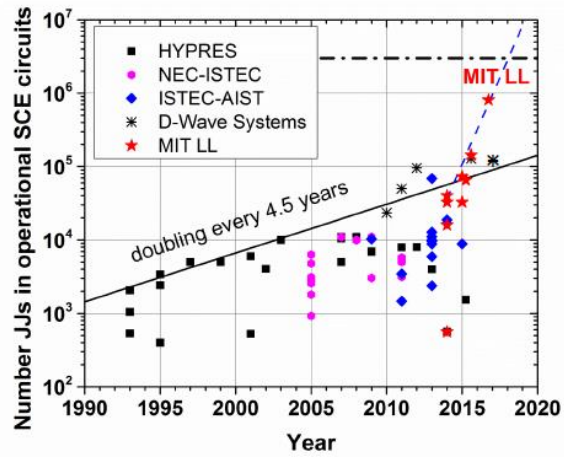


Figure 3.1. Superconducting electronics scaling trend [18].

The cross-section of a multi-layer niobium-based process offered by MIT Lincoln Laboratory (MIT-LL) is illustrated in Figure 3.2. As can be seen, there are 21 layers, including 8 superconducting layers, one gold layer on top, a resistive metal layer, Nb/Al-AlO_x /Nb[1] Josephson junctions, and insulating layers. The Josephson junctions are fabricated with a 10 KA/Cm^2 critical current density and minimum diameter of 500 nm, while J5 and M5 are the top and bottom electrodes of the Josephson junctions, respectively. M0-M4, M6, and M7 are niobium layers with a thickness of 200 nm. M5 is 135 nm thick, M8 is a gold layer used for a contact pad, and I0-I7 are 200 nm dielectric layers[2]. R5 is a molybdenum resistor layer with a thickness of 40 nm.

Chemical mechanical polishing (CMP) is used for the planarization of the dielectric and patterned layers of the Josephson junctions. This process allows having over $7*10^4$ Josephson junctions on a 5mm*5mm chip. A truncated 4-metal layer process of this procedure can be used for simplification, which employs a fabrication method and parameters of physical layers similar to those in the 8-layer set-up. In the truncated process, only the upper four niobium layers (M4-M7) are used [19]. In this thesis, the truncated process is utilized for EM simulation.

[1] Niobium-aluminum oxide-niobium
[2] Sio_2

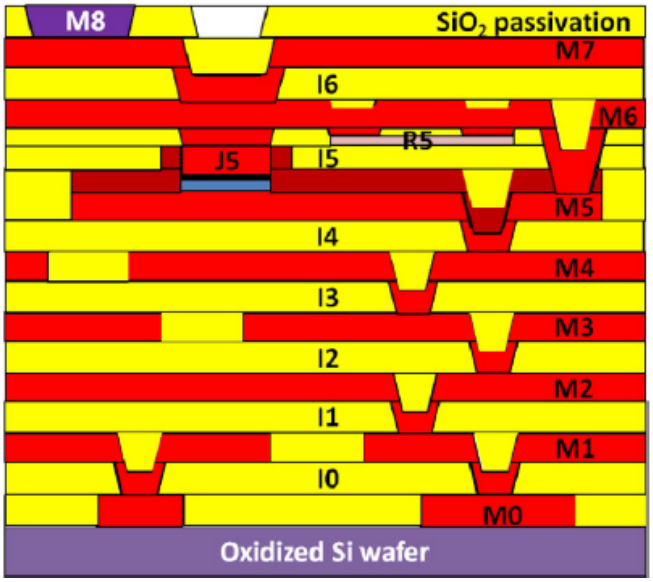


Figure 3.2. Cross-section of MIT-LL process [19].

3.2 Design

In this section, several different resistors are designed using the MIT-LL process and then are used in an R-2R ladder.

3.2.1 Designing a coplanar waveguide

A coplanar waveguide (CPW) is suitable for circuit miniaturization and broadband applications. A basic CPW consists of three conductors on top of a dielectric substrate, as shown in Figure 3.3. The conductor in the middle is the signal line and the other two are ground conductors. The signal line width (W) and the spacing between conductors (S) are the parameters determining the characteristic impedance of the transmission line [20]. The width of ground lines can be the same as the signal line (W) or larger (i.e., up to 3W). In designing a 50 Ohm Transmission line in MIT-LL, W and S are assumed to be 35um and 11um, respectively. The designed 50 Ohm CPW is simulated in Sonnet and the results are illustrated in Figure 3.4. CPW shows a good 50 Ohm match over 50GHz, with a return loss below 20dB.

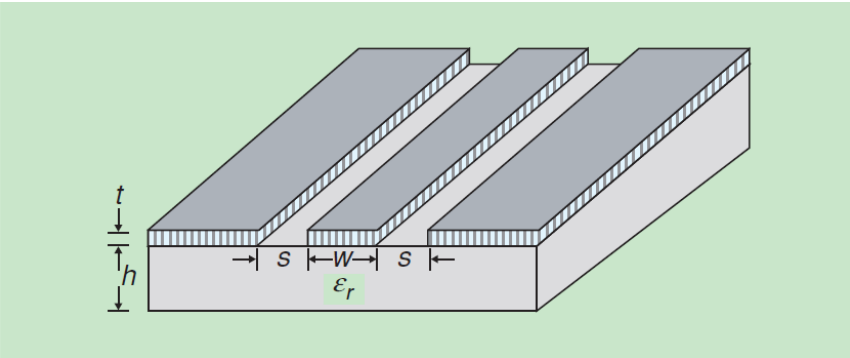


Figure 3.3. 3D schematic of coplanar waveguide [20].

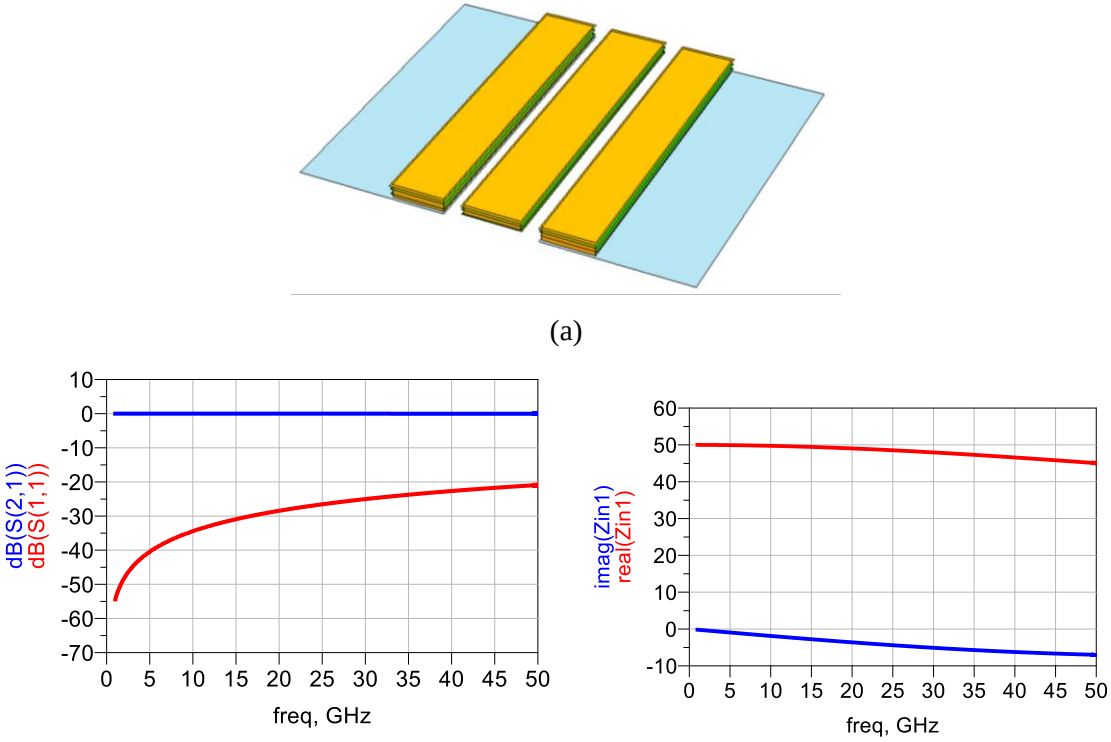
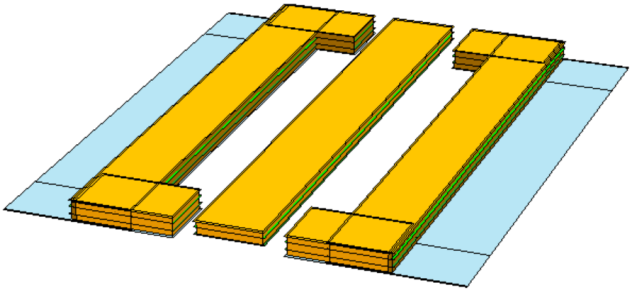


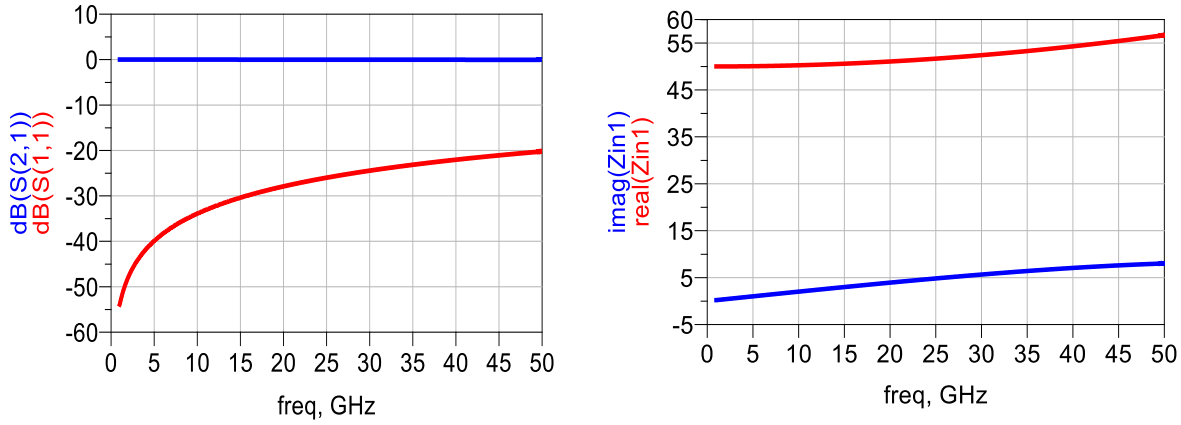
Figure 3.4. (a) 3D schematic; (b) EM simulation of basic 50 Ohm CPW in MIT-LL technology.

Designed structures for resistors cannot be fitted to the 50hm CPW shown in Figure 3.4. This is because designed resistors require a larger gap between the signal line and the ground, which would deteriorate its performance. Hence, the structure of this CPW is changed to make it suitable for the designed resistors while maintaining W and S. The new CPW structure and its EM simulation results are shown

in Figure 3.5. In comparing the results in Figure 3.4 and Figure 3.5, we can see that they both have almost the same performance. Changing the structure of the CPW does not have any significant effect on the results, as the modified CPW, S11 is below 20dB over 50GHz.



(a)



(b)

Figure 3.5. (a) 3D schematic; (b) EM simulation of a designed 50 Ohm CPW in MIT-LL technology.

3.2.2 Designing resistors

In the SFQ5ee process of MIT-LL, the resistivity of resistive metal layer, R5, is 2 Ohm per square. The number of squares in a rectangle specifies the resistance only at low frequencies. As the frequency varies, the resistance values change noticeably over a wide range of frequencies, which is caused by the parasitic capacitance and inductance of the ground and lines. 3D model and EM simulation results for a designed 25 Ohm resistor over 1GHz-50GHz are shown in Figure 3.7 (a). A simple rectangle L/W ratio of 12.5 is used with a coplanar waveguide to provide 25 Ohm at low frequencies. The structure is

modeled as a π model and the resistance is then given by $R = -real\left(\frac{1}{Y(2,1)}\right)$. It should be mentioned that the π model is a very simplified model that is applicable at very low frequency, a much involved model that includes parasitic effects must be used to accurately represent the resistor over a wide-band frequency range. The dimension of the structure, using a conventional approach, is 449 μm x 250 μm; however, the use of a meander [15], as depicted in Figure 3.7 (b), is a solution for decreasing dimensions to 300 μm x 250 μm.

Also, according to the results, using a meander line rather than a rectangular line decreases the phase mismatch in such a way that the equivalent resistor changes from 25 Ohm to 19 Ohm. If the gap between the legs of the meander is small enough, a large amount of the magnetic field of the adjacent legs would cancel each other out. The remaining magnetic field causes the resistor to exhibit inductance behavior that leads to phase mismatch. Floating metals are added either on top (M8 and M7) or beneath (M4 and M5) the meander to minimize the inductance effect by adding capacitance. Promising results are achieved through tuning the dimensions of floating metals. The input impedance of the structure with optimized dimensions for floating metals is shown in Figure 3.7 (c), varying from 24.95 to 25.25 Ohm, which introduces an error of less than ±1%.

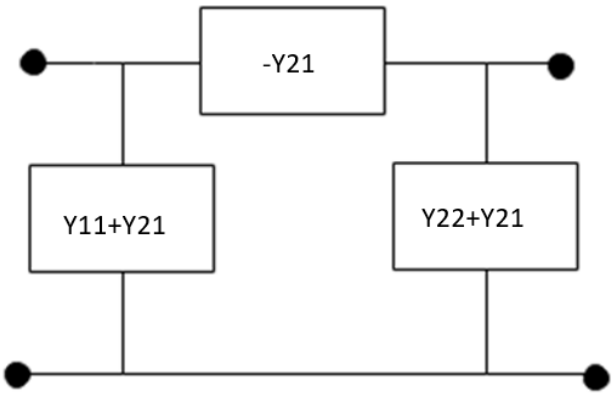
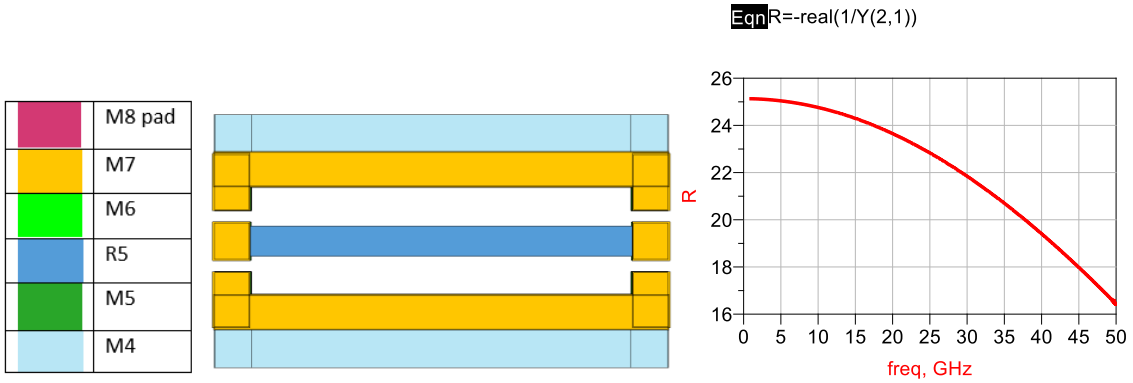
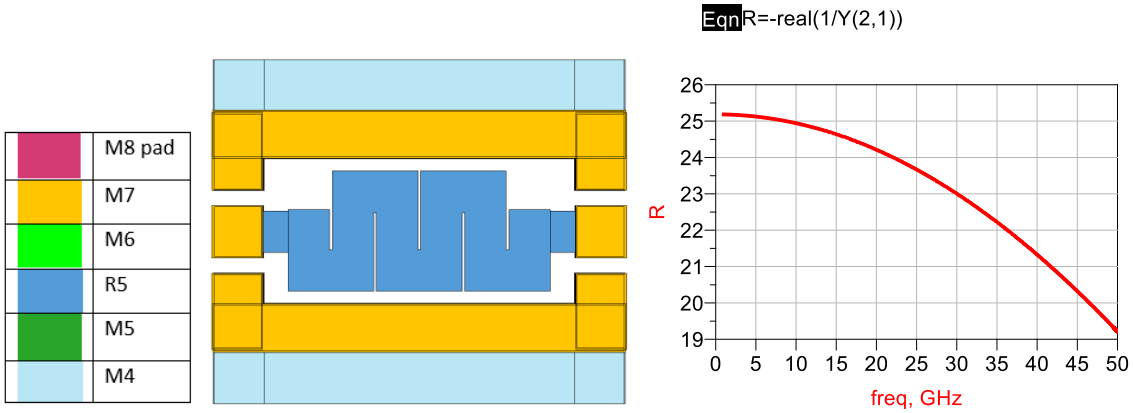


Figure 3.6. Equivalent π circuit.



(a)



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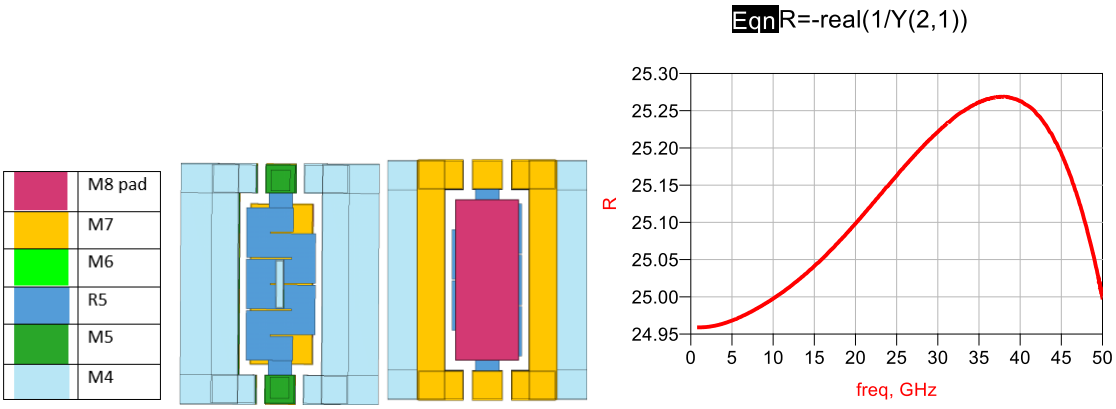


(c)

Figure 3.7. 3D model and EM simulation of 25 Ohm resistor: (a) rectangle-shaped resistor; (b) meander-shaped resistor; (c) meander-shaped resistor with floating metals.

A 1-port 25 Ohm resistor is designed with two floating metals at the top and bottom of the resistor, as illustrated in Figure 3.8. The input impedance changes from 24.5 to 26.4 Ohm, indicating an error of less than 6%.

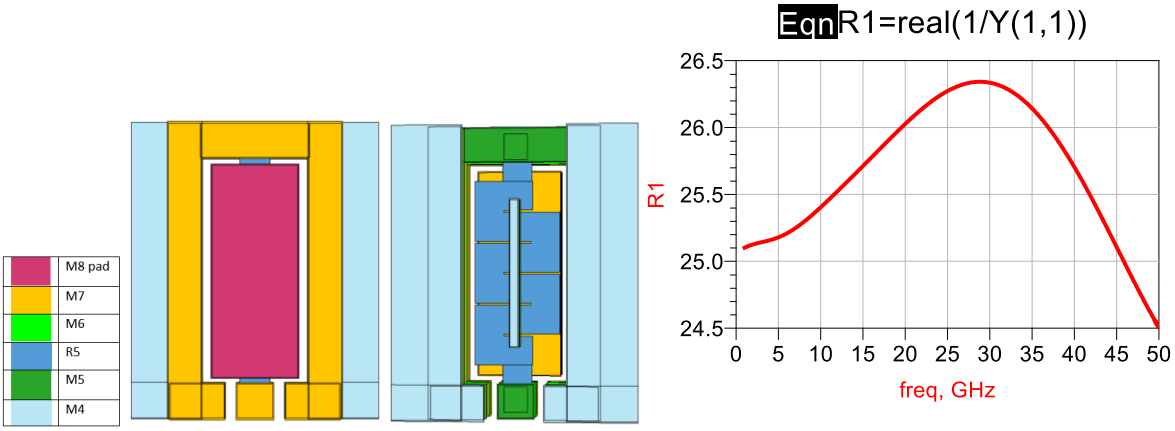


Figure 3.8. 3D model and EM simulation of 1-port 25 Ohm.

Using the same approach, 2-port and 1-port 37.5, 50, and 75 Ohm resistors are designed with a meander line as a resistor and floating metals optimized to minimize impedance variations over frequencies. A 3D model and EM simulations of the designed resistors are illustrated in Figure 3.9 to Figure 3.12.

As depicted in Figure 3.9, the designed 37.5 Ohm resistors only have one floating metal on top of the meander. The floating metals are on layers M8 and M7, which are connected through vias. In this case, one floating metal alleviates the inductance effect of the meander, leading to a less than 10% variation in input impedance of the structure over a frequency range of 50 GHz.

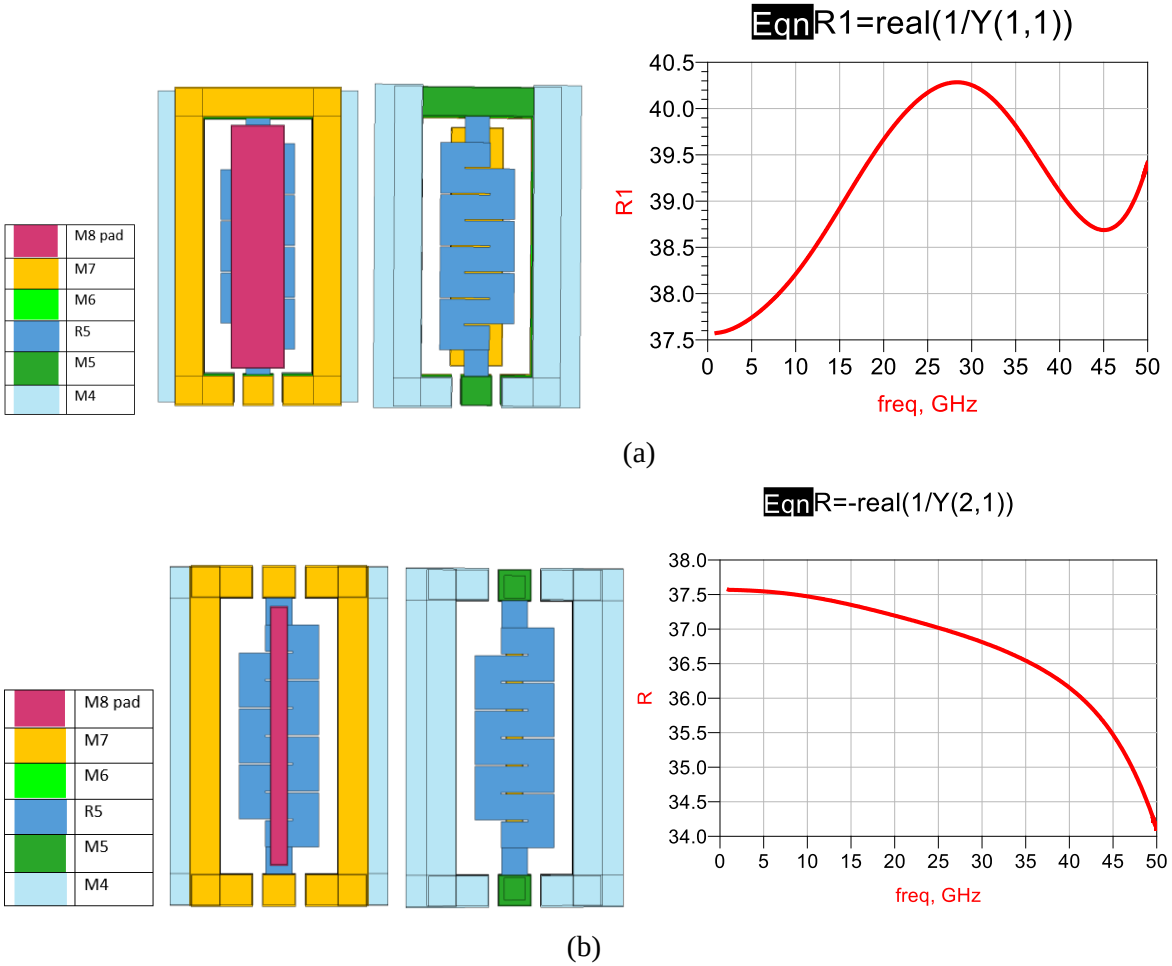


Figure 3.9. 3D model and EM simulation of (a) 1-port 37.5 Ohm and (b) 2-port 37.5 Ohm.

Designing 50 Ohm and 75 Ohm resistors is more challenging, since to achieve a higher value resistor, the number of turns in a meander line should increase, resulting in larger structures. Performing optimization to minimize the variations of a resistor over frequency becomes ever more difficult, because when the dimensions of the structure increase, the accuracy of the equivalent π model correspondingly decreases. In other words, lumped element assumptions are not as precise in high frequencies as the dimensions increase. For instance, the largest dimension in Figure 3.10 for designing 50Ohm is 415 μm ($\approx 0.7\lambda$), while the wavelength at 50GHz is 600 μm.

Figure 3.10 depicts the designed 1-port and 2-port 50 Ohm results, with errors of about 12% and 10%, respectively. In a 2-port structure, the inductance effect is only controlled by floating metals on layers M8 and M7, while in the grounded structure, another floating metal on layers M4 and M5 is exploited.

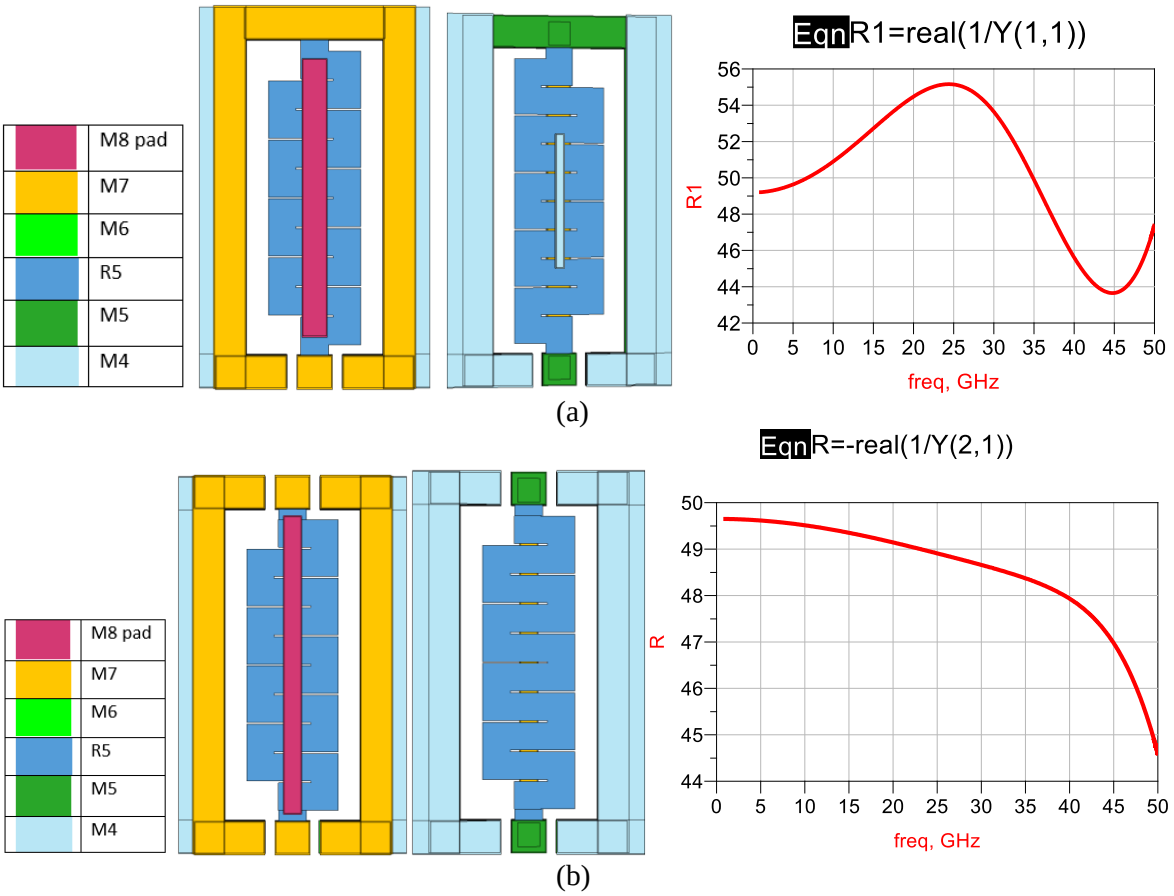


Figure 3.10. 3D model and EM simulation of (a) 1-port 50Ohm and (b) 2-port 50Ohm.

It is assumed that the width of the meander would be less than 100 µm in designing different resistors; thus, to achieve a higher value, the number of turns would be increased. Nevertheless, another version of 1-port 50 Ohm (greatest dimension is 300 µm) is designed in which meander width is set at 161 µm, while in the previous one it is 100 µm. As depicted in Figure 3.11, the new design gives better results, with only a 2.5 Ohm variation from 1GHz to 50GHz.

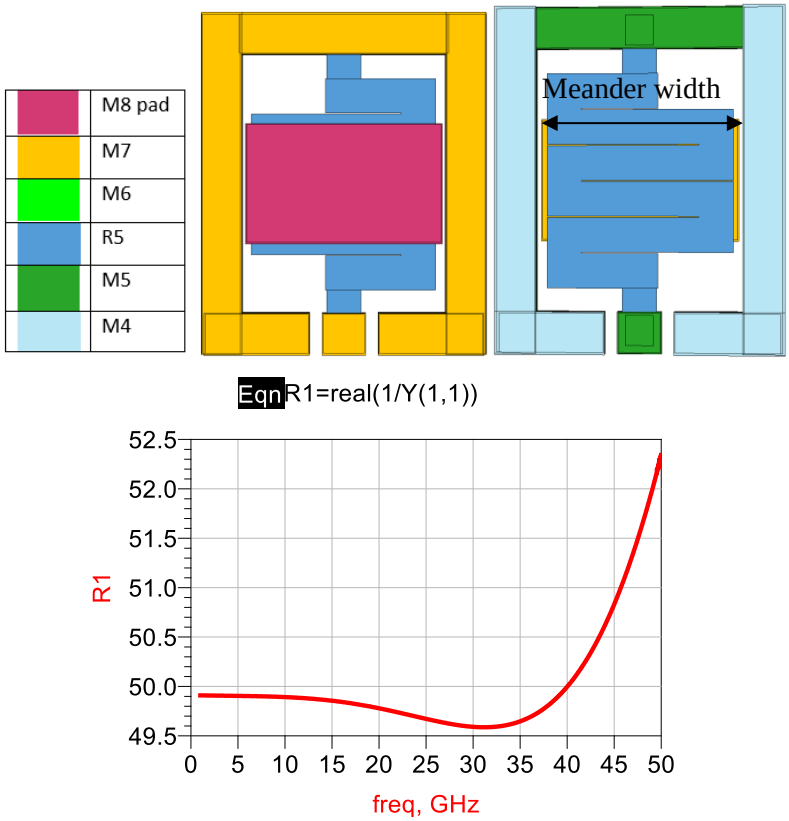


Figure 3.11. 3D model and EM simulation of improved 1-port 50 Ohm.

Figure 3.12 illustrates 1-port and 2-port 75 Ohm resistors. Two floating metals on either side of the meander are utilized to compensate the inductance behavior of the meander by adding capacitors. The 1-port resistor varies ±7 Ohm over a frequency range 50GHz, which is an error of less than ±10%. However, by optimizing floating metal dimensions, the best results achieved for a 2-port (Figure 3.12 (b)) show a greater than 15% variation over the 50GHz range, despite showing only a 6% error from 1GHz to 25GHz.

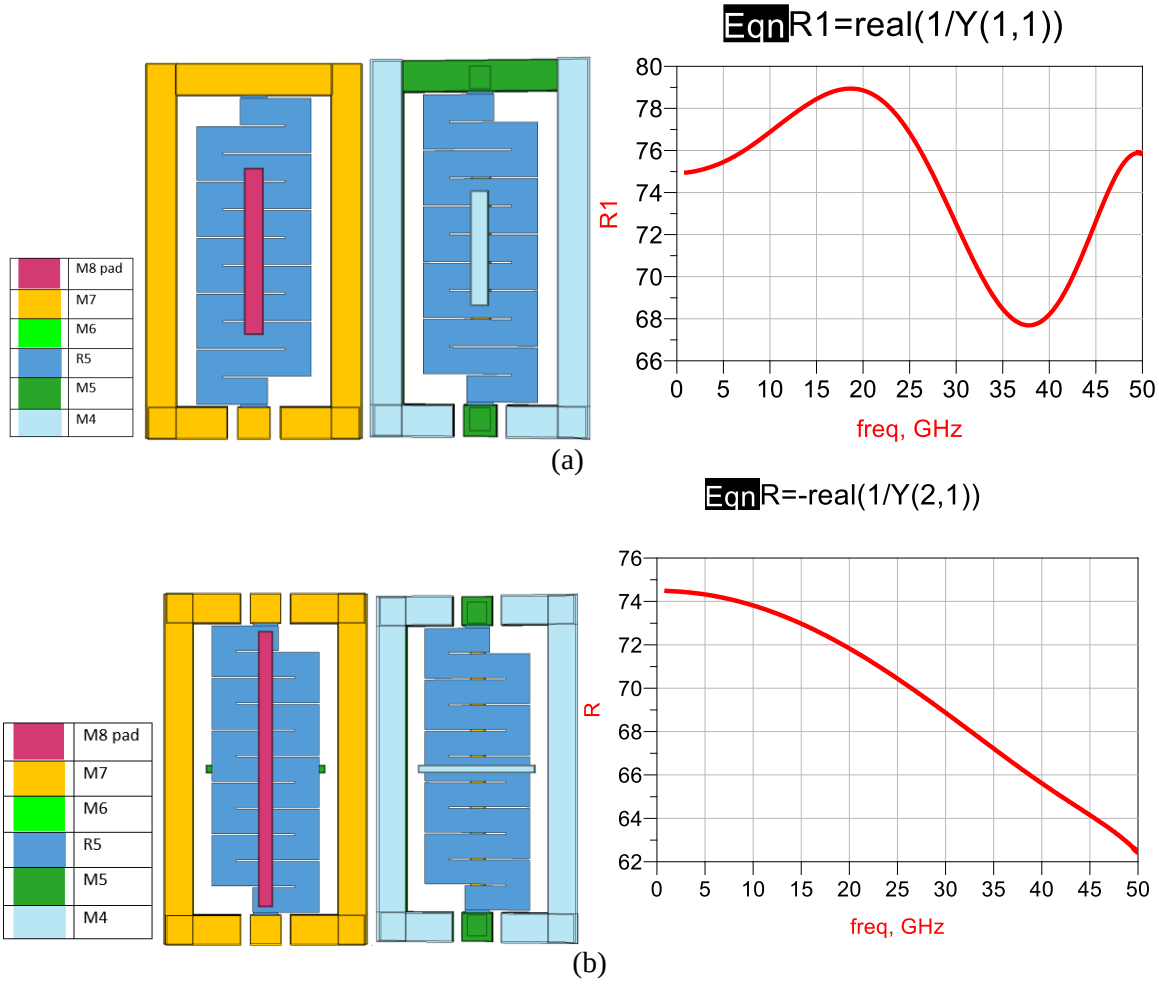


Figure 3.12. 3D model and EM simulation of (a) 1-port 75 Ohm and (b) 2-port 75 Ohm.

3.3 R-2R ladder network

In this section, a superconductor digitizer is designed and simulated using designed resistors in Sonnet. As well, 2-port 25 Ohm and 1-port 50 Ohm resistors are used as T-junctions and 90-degree turns in order to obtain an R-2R ladder. The T-junction, which is an equal power divider, is designed and simulated in Sonnet, as depicted in Figure 3.13. A basic analysis for a T-junction posits that it is assumed to be a lossless, reciprocal and symmetrical 3-port network. Hence, at very low frequencies the return loss and insertion loss of a T-junction would be as follows [21]:

$$|S_{11}| = |S_{22}| = |S_{33}| = \frac{1}{3}\ or - 9.54\ dB \tag{3.1}$$

$$|S_{21}| = |S_{31}| = |S_{32}| = \frac{2}{3}\ or - 3.52\ dB \qquad (3.2)$$

Figure 3.13 illustrates a 3D schematic and S-parameters of the designed T-junction simulated in Sonnet. According to EM simulation, |S31| and |S32| varies from -3.52dB to -3.98dB and |S21| changes between -3.54dB and -3.7dB over 1-50GHz. The return loss of the designed T-junction is the same as the theoretical value in low frequencies (1-5GHz) and changes 2dB in higher frequencies.

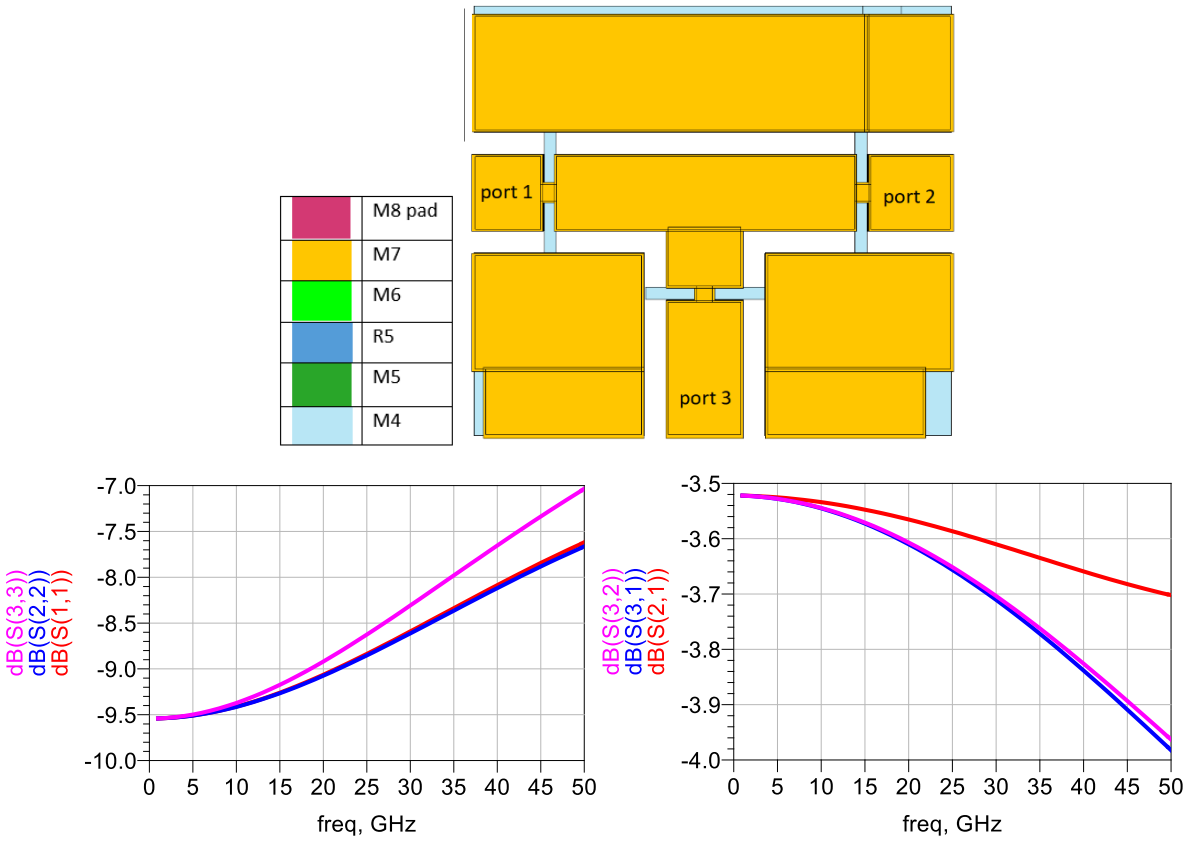


Figure 3.13. 3D model and EM simulation of CPW T-junction using MIT-LL technology.

A CPW 90-degree turn is designed and simulated in Sonnet, as illustrated in Figure 3.14. S-parameters display a good response over 50GHz. Its insertion loss is zero and |S11| is below -20dB over 50GHz.

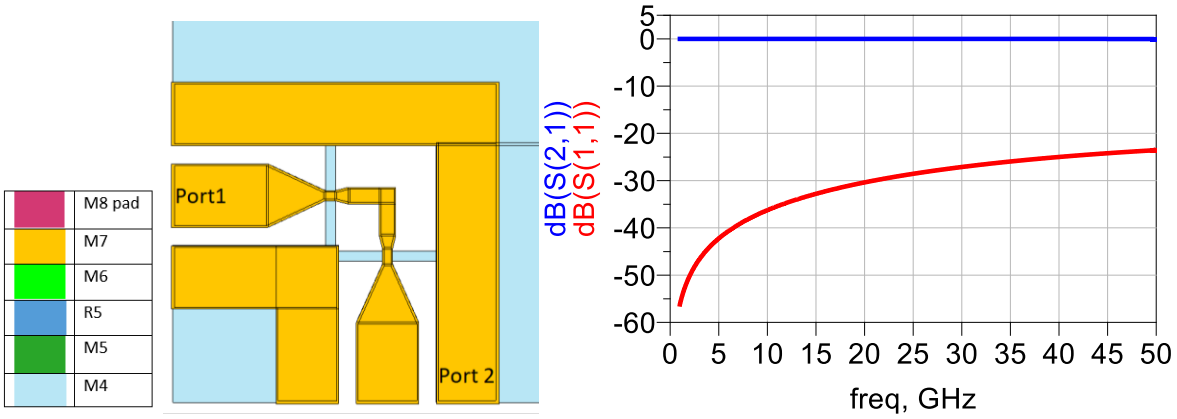
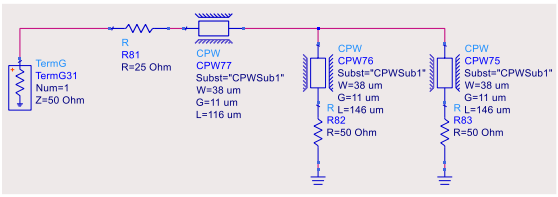
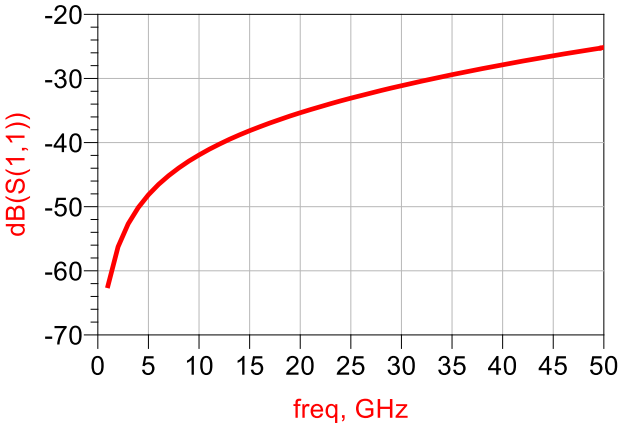


Figure 3.14. 3D model and EM simulation of CPW 90-degree turn using MIT-LL technology.

Next, 1-bit, 2-bit, and 4-bit R-2R ladders are designed and simulated in Sonnet by utilizing designed resistors, a T-junction and a 90-degree turn. The simulated results are compared with an ideal case simulated in the Advanced Design System (ADS). In the ideal simulations, ideal 25 Ohm and 50 Ohm resistors are used. CPW lines are also added with the same substrate used in MIT-LL technology and with the same length as the designed R-2R ladder in Sonnet. Ideal and EM simulations of 1-bit, 2-bit, and 4-bit R-2R ladders are illustrated in Figure 3.15, Figure 3.16 and Figure 3.17, respectively. In the ideal simulations, |S11| are all below -20dB over a 50GHz range, which means that there is a good match in the circuits, as is expected due to the use of ideal resistors. EM simulation results demonstrate promising results over a 50GHz range; |S11| are less than -15dB, supporting good designs for 25 Ohm and 50 Ohm resistors. This indicates that digitization is working well over the 50GHz range.





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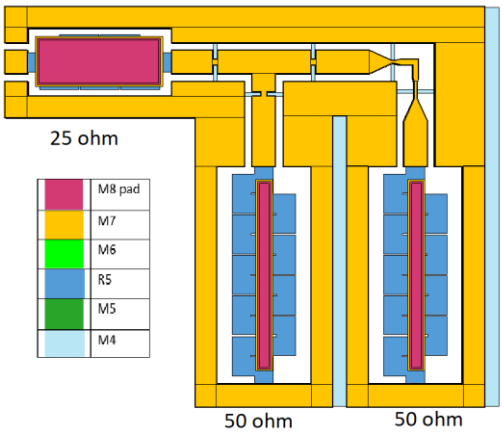
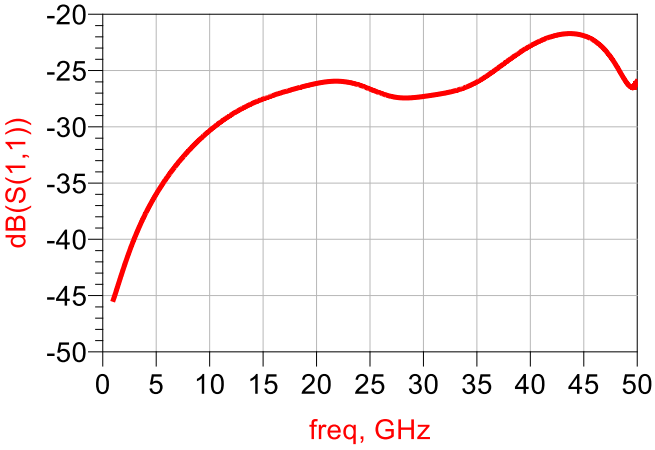
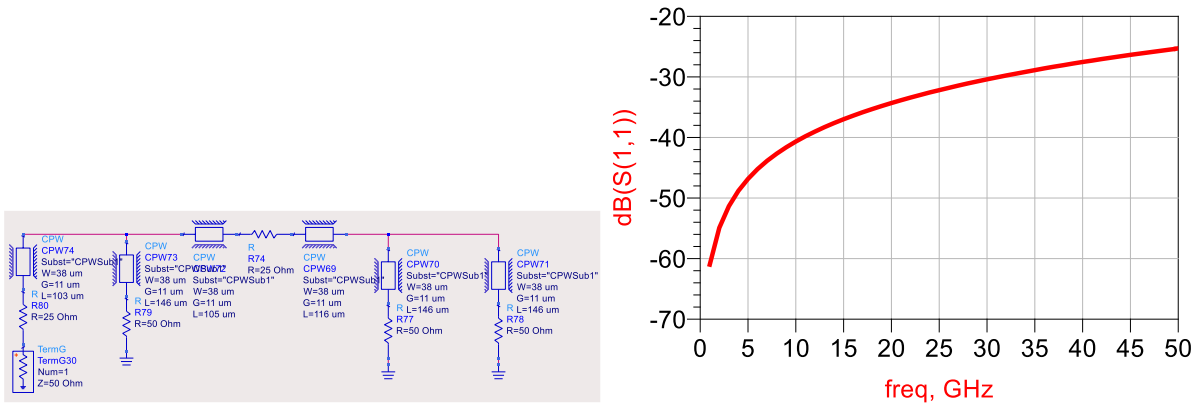


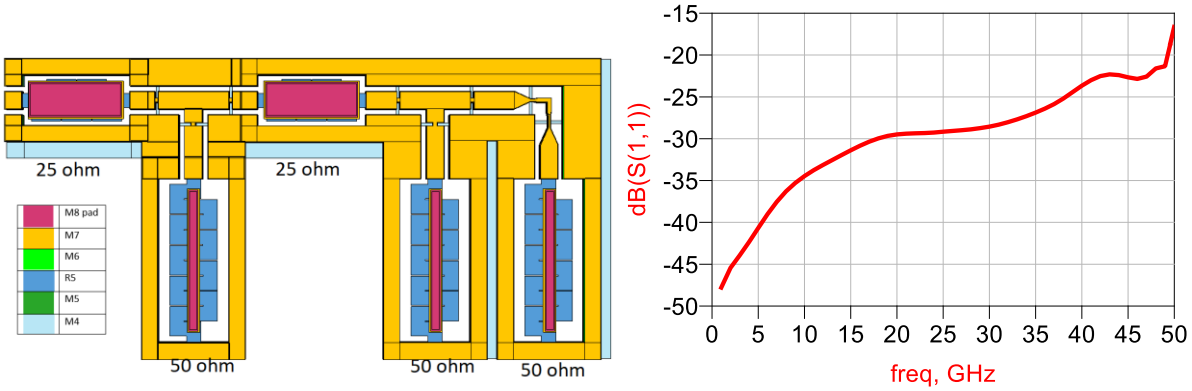


(b)

Figure 3.15. a) Schematic and ideal simulations; b) 3D model and EM simulation of 1-bit R-2R ladder.

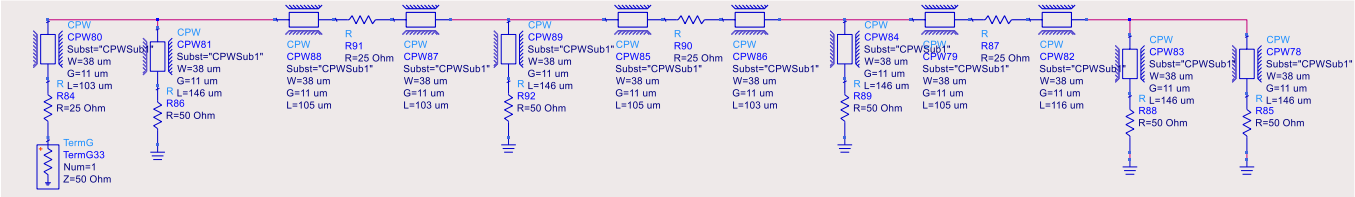


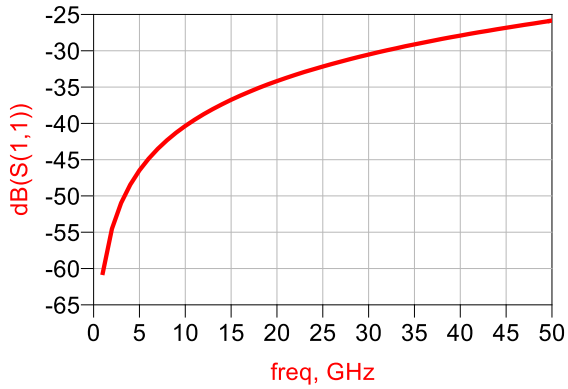
(a)



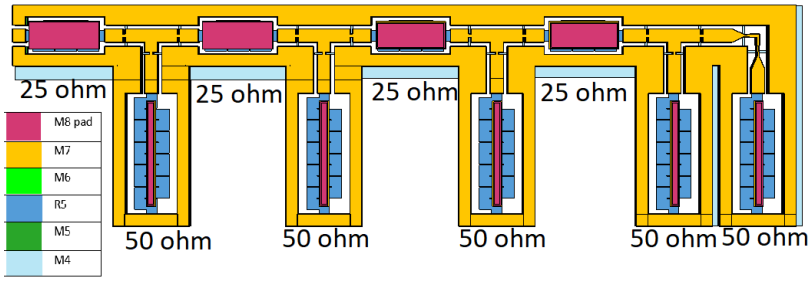
(b)

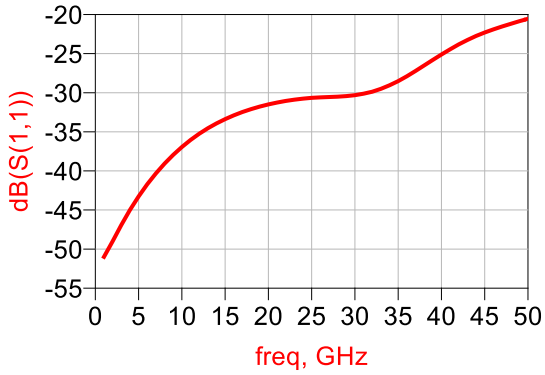
Figure 3.16. a) Schematic and ideal simulations; b) 3D model and EM simulation of 2-bit R-2R ladder.





(a)





(b)

Figure 3.17. a) Schematic and ideal simulations; b): 3D model and EM simulation of 4-bit R-2R ladder.

3.4 Measurements

All measurements for niobium-based low-temperature superconductor devices were done in the Lakeshore RF cryogenic probe station [23] of the CIRFE Lab [24]. As illustrated in Figure 3.18, the Lakeshore probe station has four different stages: the sample stage, the 4 °K shield stage, the radiation shield stage, and the second shield stage. There are five temperature sensors located in the four stages and one of the probe arms. Typical temperatures for these sensors when being cooled down by liquid Helium are 4.3 °K, 4.3°K, 15°K, 30°K and 15°K. However, the temperatures can be further decreased to 3°K, 4.2°K, 11°K, 22°K and 9°K by exploiting an external pump [7].

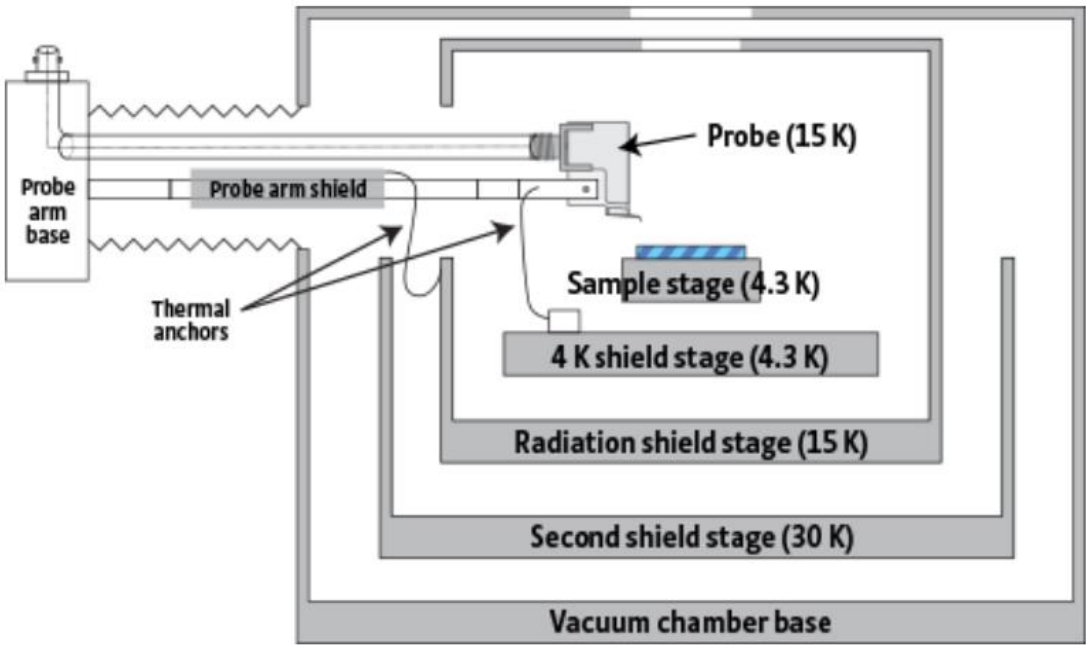


Figure 3.18. Schematic of stages of Lakeshore probe station chamber and temperatures [23].

Tapers are added to the designed resistors to extend the pads so that the probes can be landed on them and the measurements can be done. Although adding tapers changes the behavior of the resistors, it should be noted that designed resistors are used without tapers in real applications. Therefore, to obtain accurate evaluation of results, all of the designed resistors are simulated with tapers and their results compared with the measurement results. The taper is depicted in Figure 3.19. As can be seen, the ground

pads are 100 μm x 120μm and spaced at 55um,with the signal pad having a dimension of 100 μm x 70 μm.

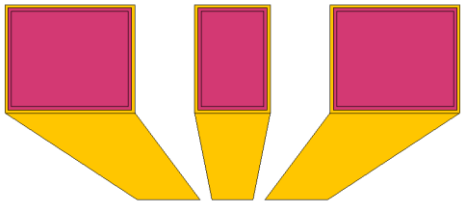
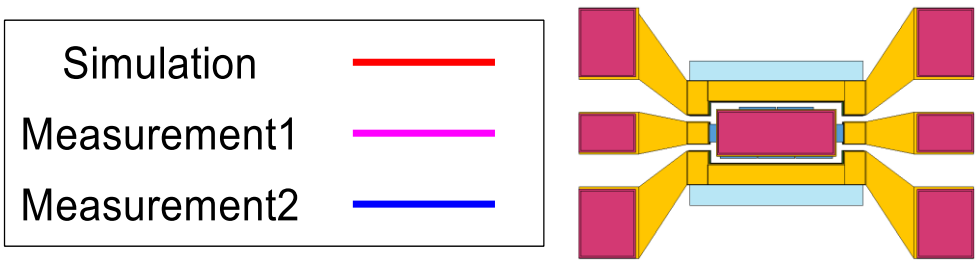


Figure 3.19. CPW taper used for measurements.

The operational frequency of the cables used for measurement is up to 27GHz, whereas devices are designed and simulated over a 50GHz range. Furthermore, because results are compared over the 50GHz range, any measurement results over 27GHz might not be valid. Measurements are repeated twice on two different chips and their results, along with taper simulations, are all plotted in a single figure. As can be seen, the measured results in low frequencies are not well-matched. Inconsistencies in the measurements at low frequency are being investigated. The measured and simulated results of the designed resistors are illustrated in Figure 3.20 to Figure 3.27.

Figure 3.20 shows a schematic of a 2-port 25 Ohm resistor with taper and a comparison of the results. As shown, the scattering parameters from the simulation and measurements are in good agreement. Other than for the S parameters, there are some mismatches between equivalent resistors.



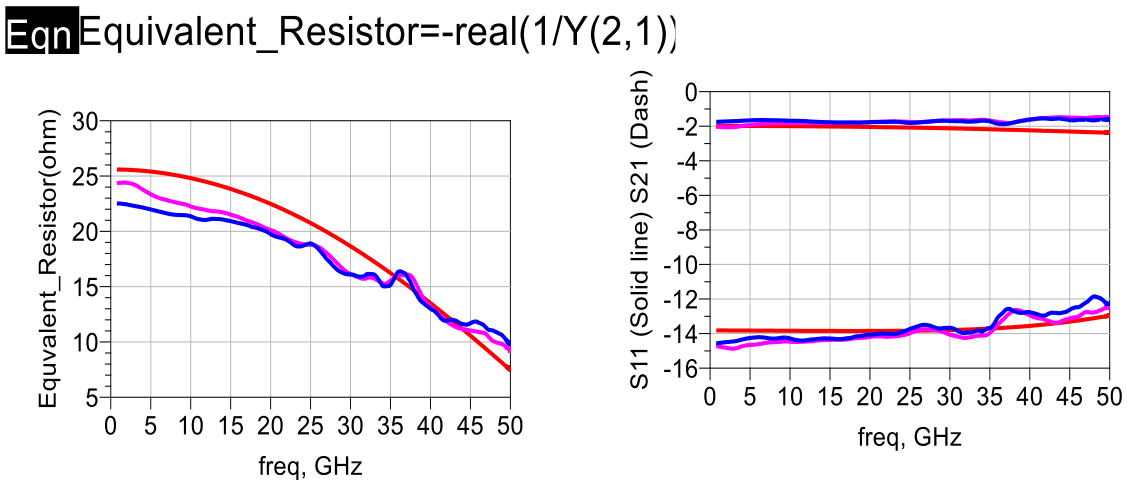


Figure 3.20. 3D schematic and EM simulation and measurement results of 2-port 25Ohm resistor with taper.

A 1-port 25 Ohm resistor is illustrated in Figure 3.21. These measurements appear to have better results compared to the EM simulation, as they have less variation in equivalent resistor over frequency.

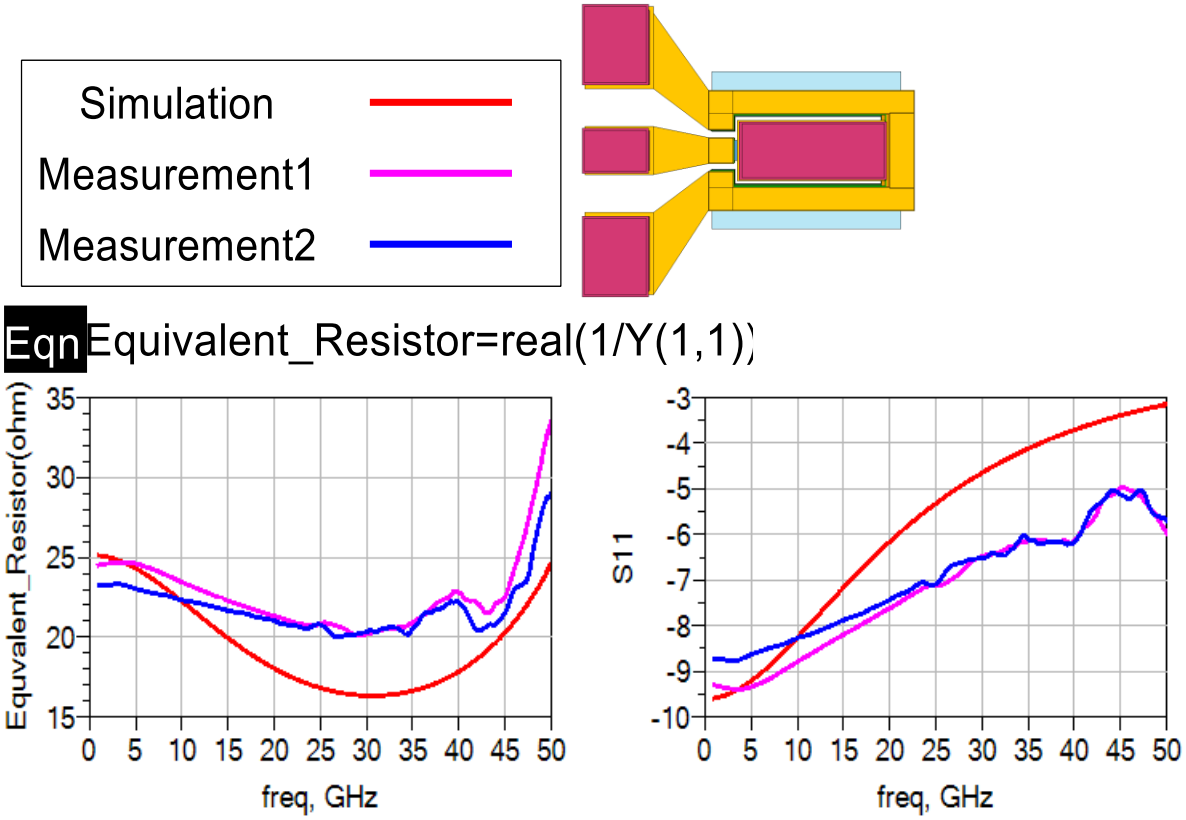


Figure 3.21. 3D schematic and EM simulation and measurement results of 1-port 25 Ohm resistor with taper.

Figure 3.22 and Figure 3.23 illustrate the schematic and results for 37.5 Ohm. In a 2-port structure, despite 1dB discrepancy between S_{11} measurements and simulation, equivalent resistors display good agreement between results, which is acceptable as there are discrepancies between measurements. In the 1-port structure, the same behavior as for 1-port 25 Ohm is seen, which shows consistency in simulation and measurement. Moreover, in the measurements, there is a less than 10 Ohm variation over 25GHz, while the variation in the simulation is around 15 Ohm.

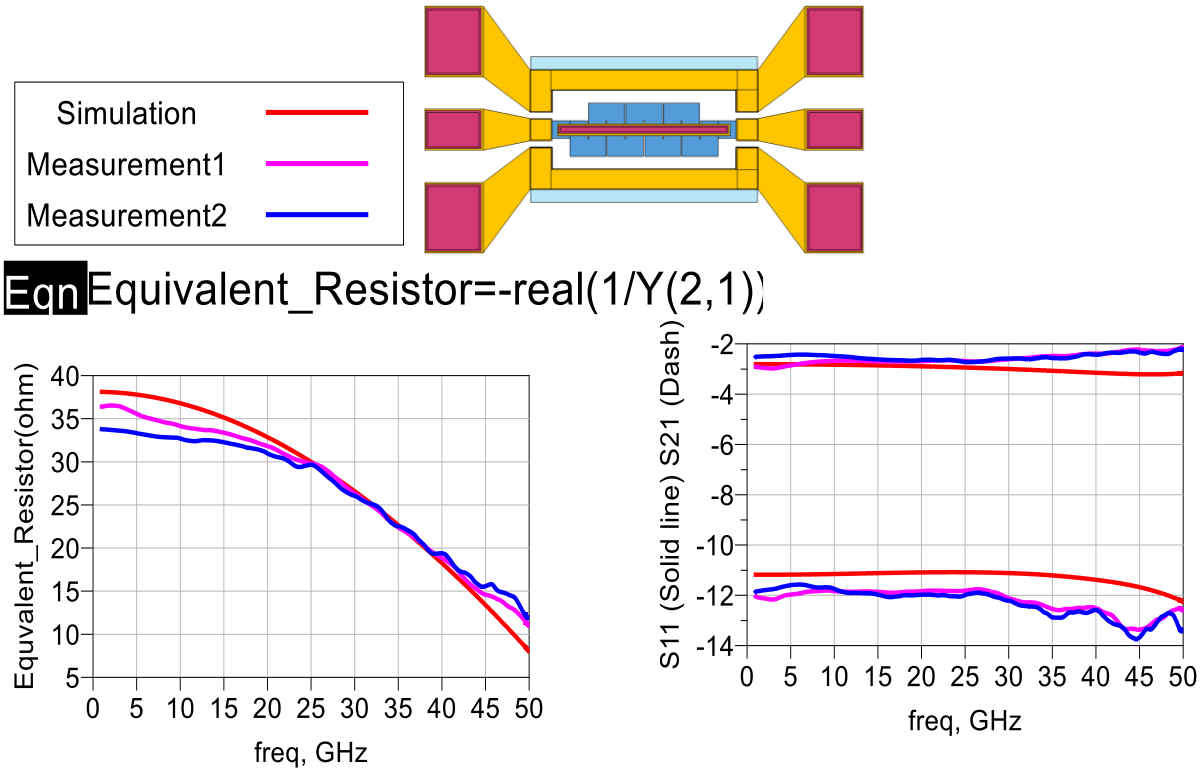


Figure 3.22. 3D schematic and EM simulation and measurement results of 2-port 37.5 Ohm resistor with taper.

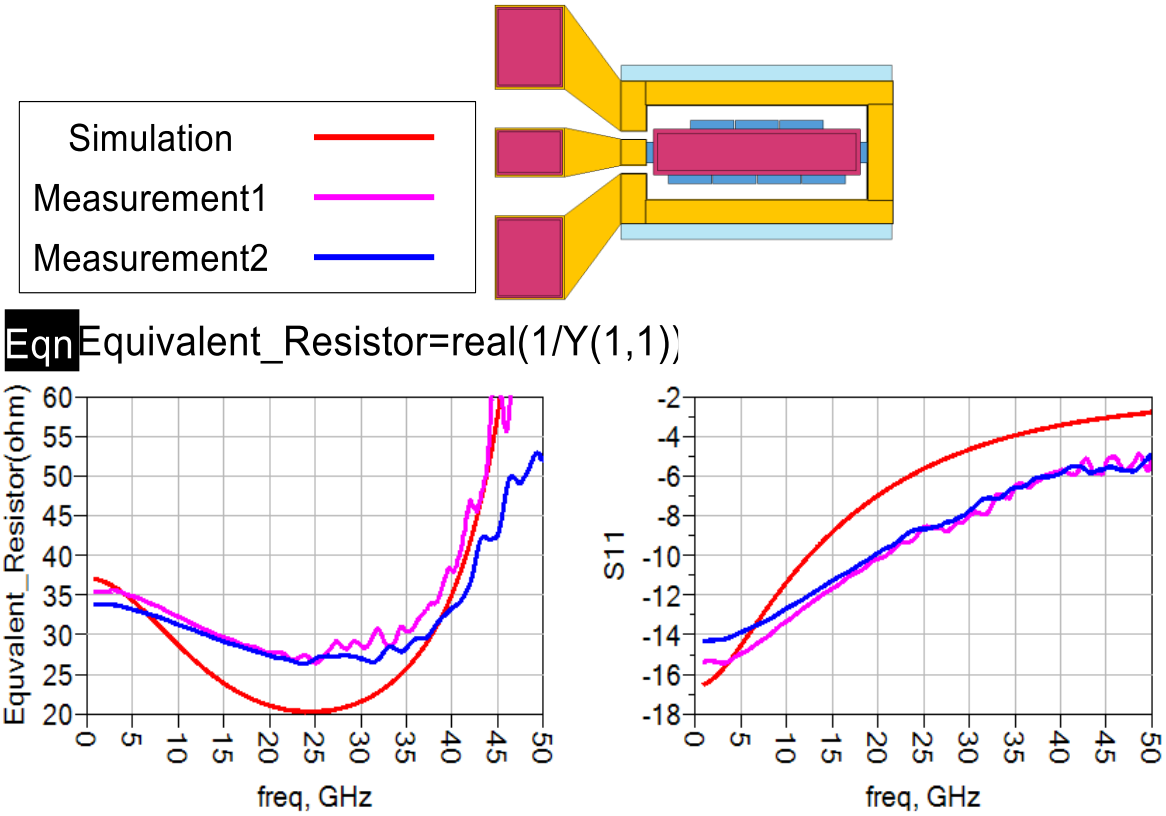


Figure 3.23. 3D schematic and EM simulation and measurement results of 1-port 37.5 Ohm resistor with taper.

Figure 3.24 and Figure 2.25, depict 2-port and 1-port results for 50 Ohm, respectively. The measured results of the 2-port structure are in compliance with EM simulation up to 30GHz, which is reasonable based on the frequency range of the cables used for the measurements. In the 1-port structure, the equivalent resistors both have the same behavior in simulation and measurements, although they show different values. This discrepancy is further investigated at the end of this chapter.

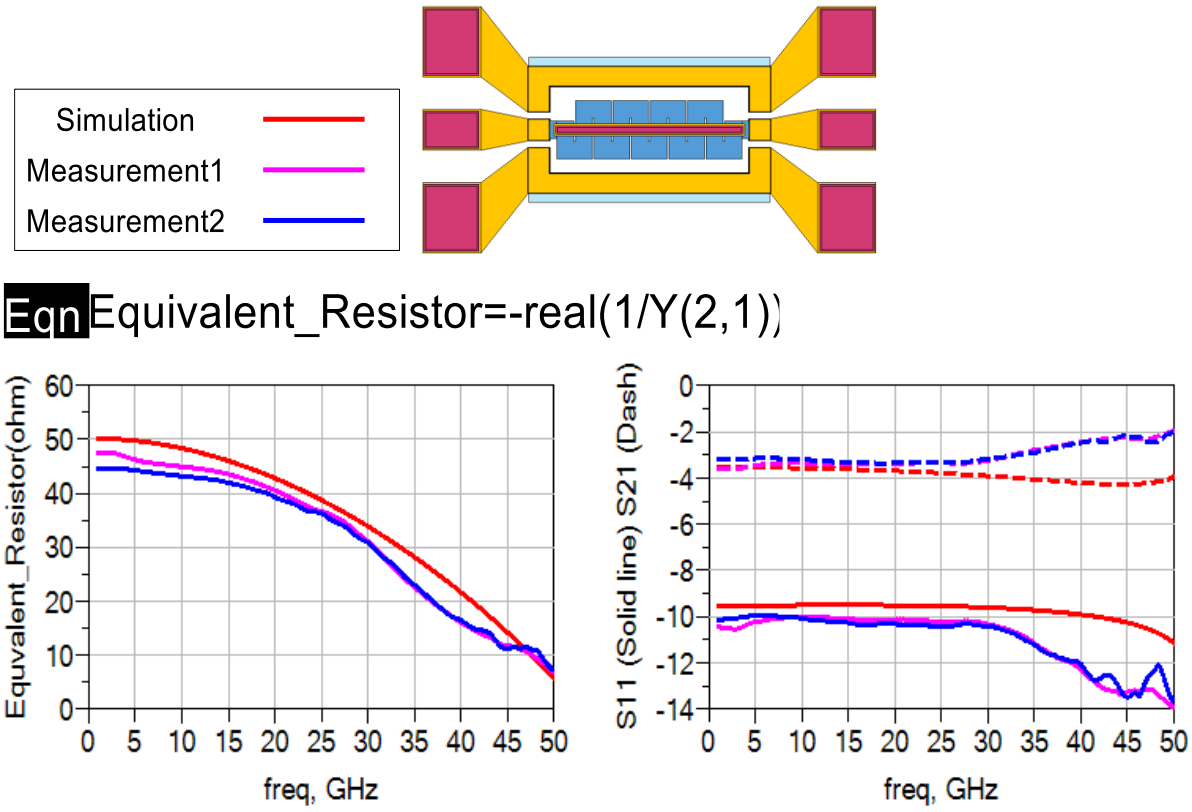


Figure 3.24. 3D schematic and EM simulation and measurement results of 2-port 50 Ohm resistor with taper.

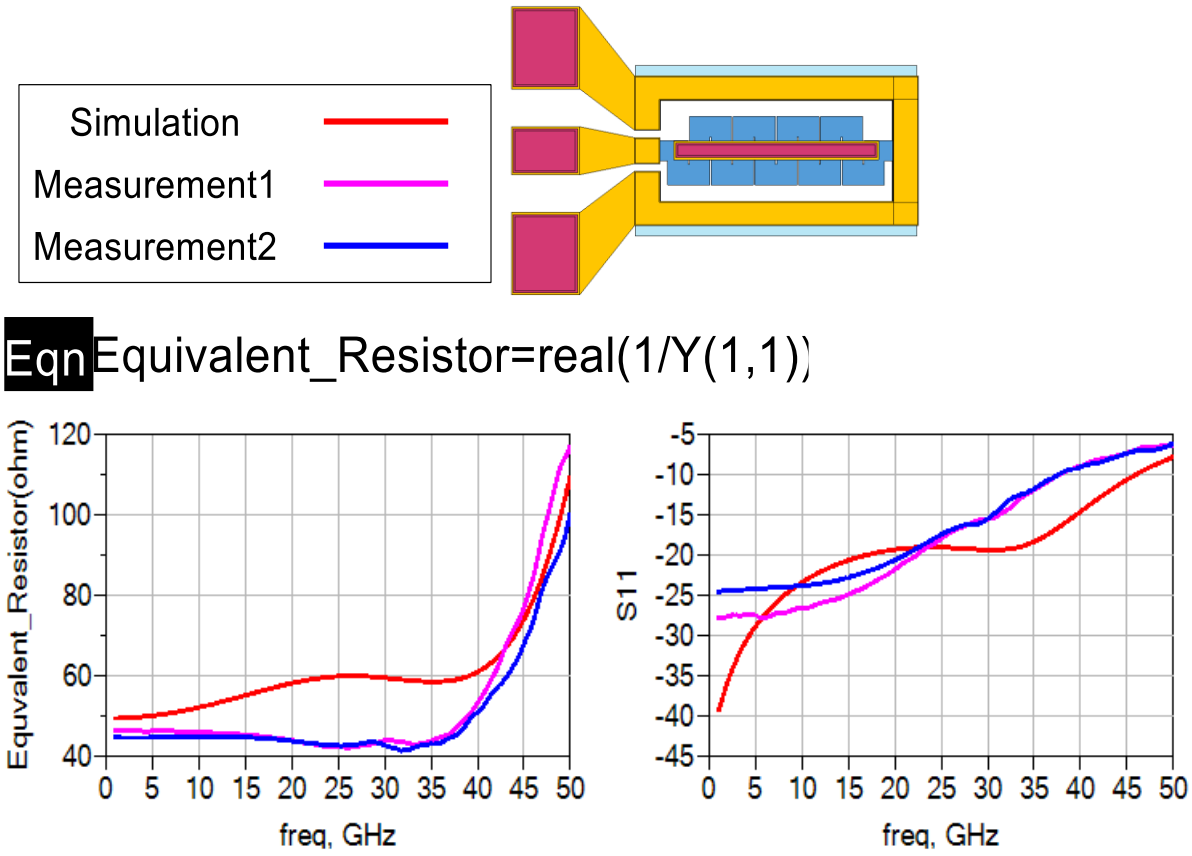


Figure 3.25. 3D schematic and EM simulation and measurement results of 1-port 50 Ohm resistor with taper.

Figure 3.26 and Figure 3.27 display 75 Ohm resistor results. In the 2-port structure, the S-parameters of the simulations and measurements are matched up to 25GHz but start deviating as the frequency increases. The operational frequency of the cables used for measurements explains this problem. In the 1-port structure, the equivalent resistor shows the same behavior in both the measurements and the EM simulations but their values are not the same. According to the distinction between the measurements done in two chips, slight differences in the properties of the material used for the fabrication likely led to such deviations, which clarifies the reason for the differences between the measurement and simulation results.

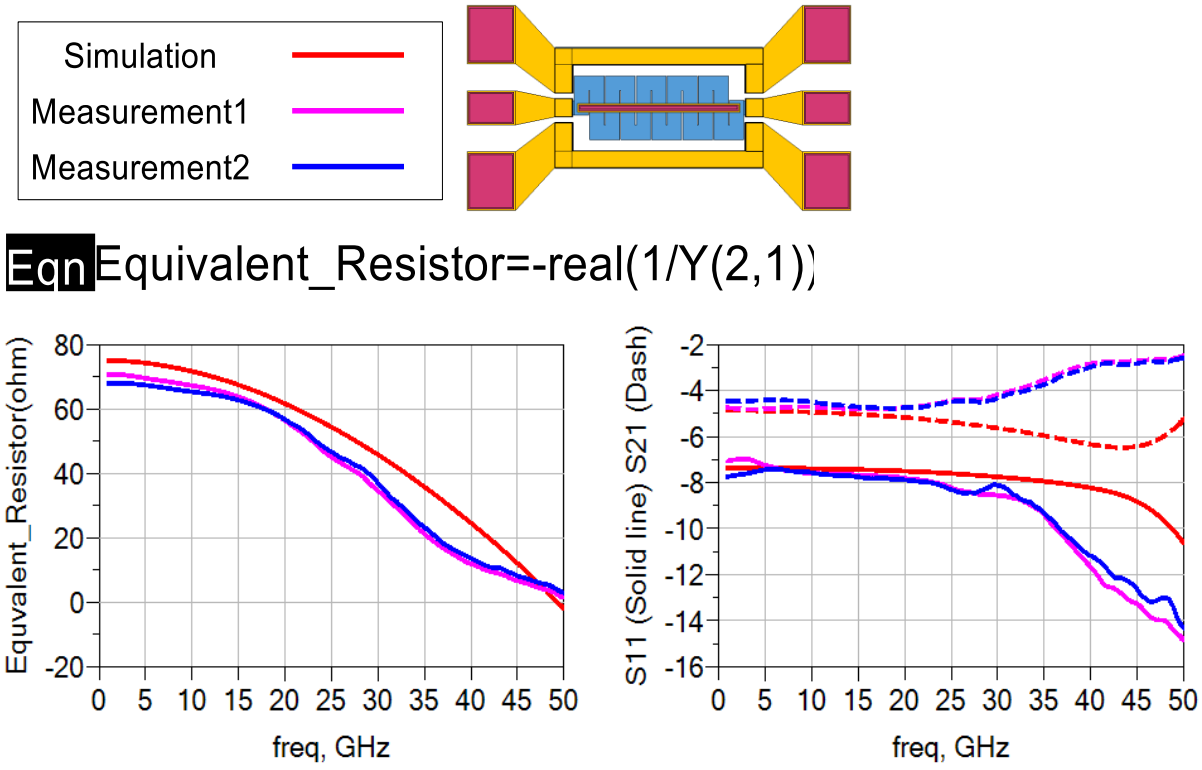


Figure 3.26. 3D schematic and EM simulation and measurement results of 2-port 75 Ohm resistor with taper.

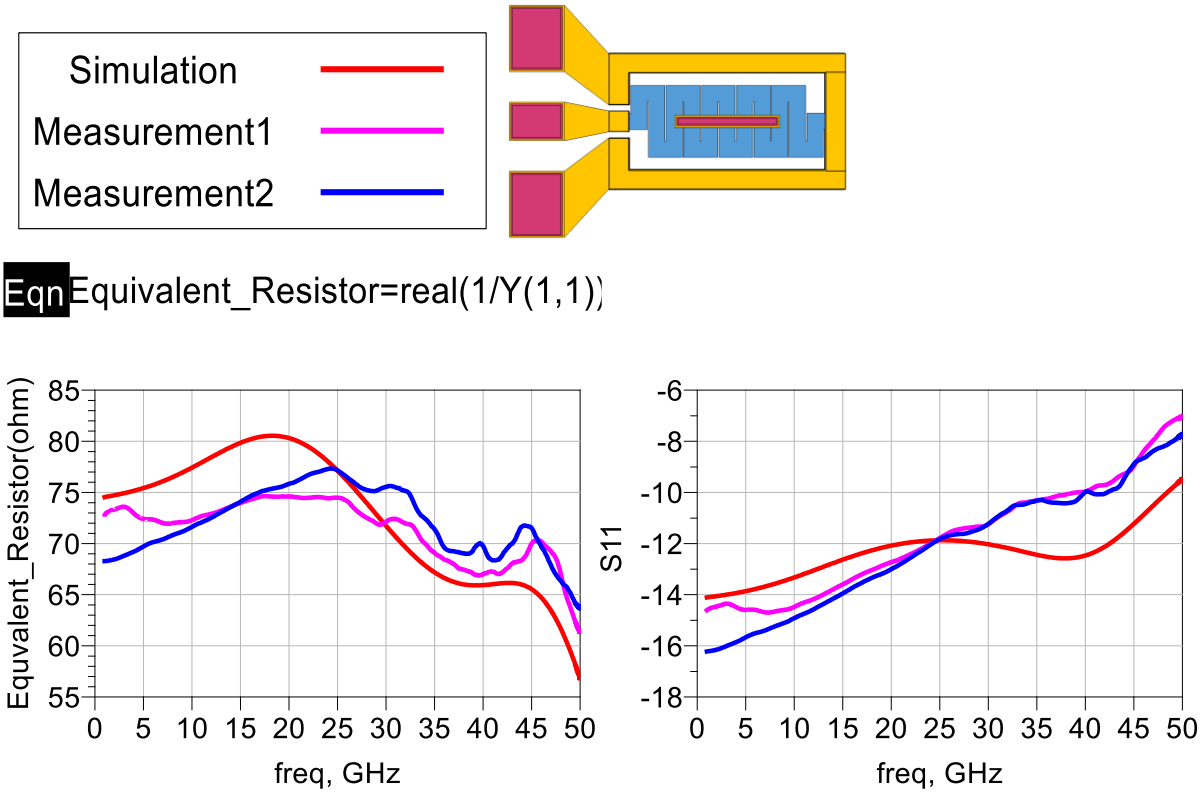


Figure 3.27. 3D schematic and EM simulation and measurement results of 1-port 75 Ohm resistor with taper.

The measured and simulated results of the fabricated 1-bit R-2R ladder are shown in Figure 3.28. The return loss (S_{11}) of the measurement results displays promising results over a 50GHz range (i.e., all below -10dB. In low frequencies up to 30GHz, there is a perfect match, as the return loss is below 24dB. In simulation result, return loss shows lower value which has the same perception as measurement, they are both showing good match.

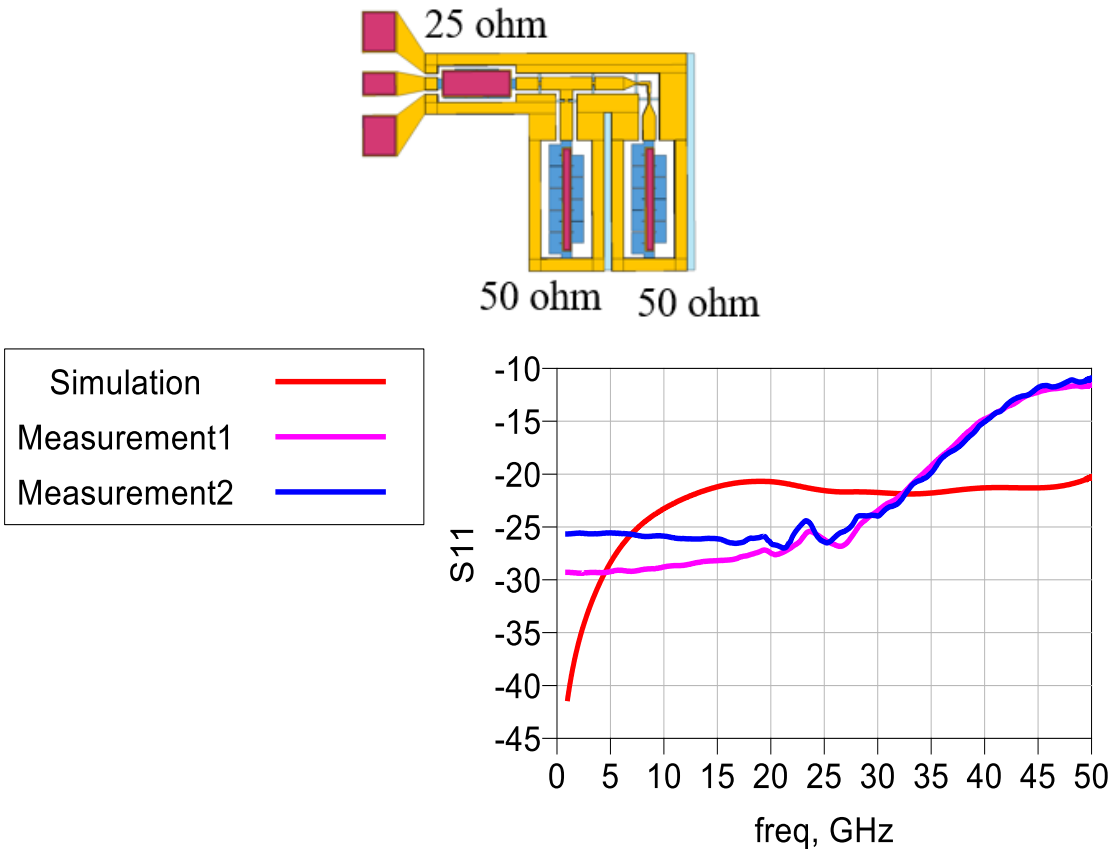


Figure 3.28. 3D schematic and EM simulation and measurement results of 1-bit R-2R ladder with taper.

In conclusion, the simulated and measured results both have almost the same behavior. However, there are discrepancies between results, which could be the outcome of various uncertainties both in measurements and simulation set-up. These are further investigated in the following section.

In 2-port structures, the insertion loss and return loss of measurements and simulations are well-matched and there is a 1dB difference between them over 25GHz. However, in 1-port structures, there are more variations between simulation and measurement results at some points. It is also worth noting that in the second measurements, equivalent resistors show smaller results than those from the initial measurements. Different temperatures in the chamber can lead to these differences.

3.4.1 Investigation of discrepancy between EM simulation and measurement results

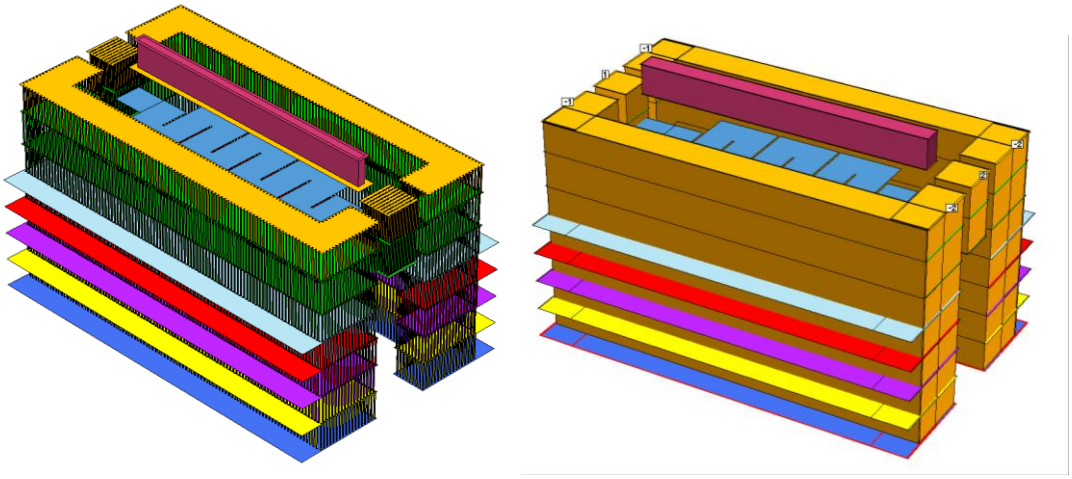
The potentioal sources of error are summarized as follows:

1. A resistor layer is used, which may add heat to the system and increase the temperature. In fact, the heat dissipated by the resistor layer increases the local temperature. The superconducting properties may vary by this slight change in temperature and also change the circuit's response.
2. The probes used for measurements only support 1-27GHz, whereas simulation results are from 1-50GHz. In other words, any results above 27GHz are not reliable. The fact that the results from two different measurements are not the same indicates that the cables used for the measurements are imperfect.
3. Uncertainty about the dielectric properties used for the simulations.
4. The vias used in the fabrication process are different from what is used in the simulation tests. Small vias, as illustrated in Figure 3.29 (a), can be used for fabrication, but performing EM simulations with small vias is not possible. Thus, in the EM simulations, the vias are modeled as a one-cell-width wall that is hollow in the middle, as shown in Figure 3.29 (b). Moreover, fabricated vias are niobium, but they are modeled as a lossless metal for simulation without including kinetic inductance. Kinetic inductance originates from the kinetic energy required by electrons or electron pairs. In this study, kinetic inductance is modeled as a surface inductance, which is calculated in Chapter 2 and formulated as follows:

$$L_s = \mu_0 \lambda_L(T)$$

$$\lambda_L(T) = \frac{\lambda_0}{\sqrt{1 - \left(\frac{T}{T_c}\right)^4}}$$

where μ_0 is $4\pi * 10^{-7}$ (H/m) and $\lambda_L(T)$ is the London depth at temperature T. According to the MIT-LL foundry, the London depth (λ_0) at T=0 is 90nm for all superconducting layers in the process. Therefore, kinetic inductance will be 0.115 pH per square at T=4°k.



(a) (b)

Figure 3.29. 3D schematic of vias in a) fabrication and b) EM simulation.

5. Uncertainty during measurements. If the process of landing probes on the pads takes too long, it could heat the circuit and change the temperature in such a way that the properties of the circuit material change.

6. In comparing 2-port and 1-port structures, 1-port structures show greater variations between measurements and simulation results. At mm-wave frequencies, box size in Sonnet can affect the entire circuit response. As shown in Figure 3.31, box size affects the response of the circuit significantly. For small box sizes, there is a resonance of around 38GHz, which is due to the capacitance effect between the box wall and the structure. This resonates with the circuit's inherent inductance effect. Simulation results are shown for larger box sizes as well, indicating that box size can still have some effect on results, which explains the discrepancies we see between the results.

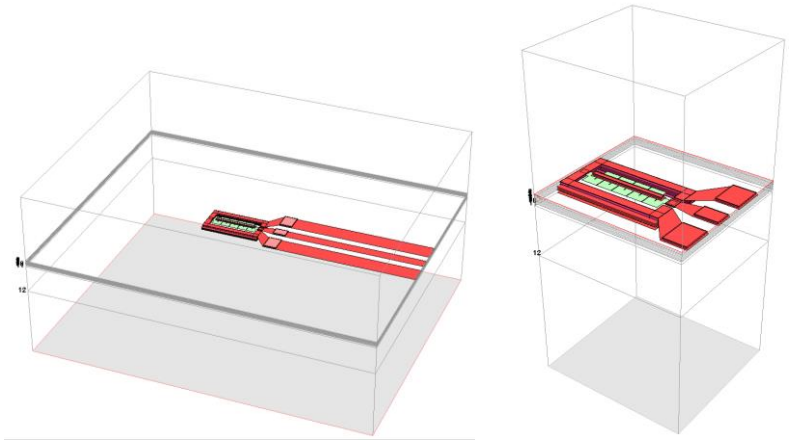


Figure 3.30. Different box sizes in Sonnet.

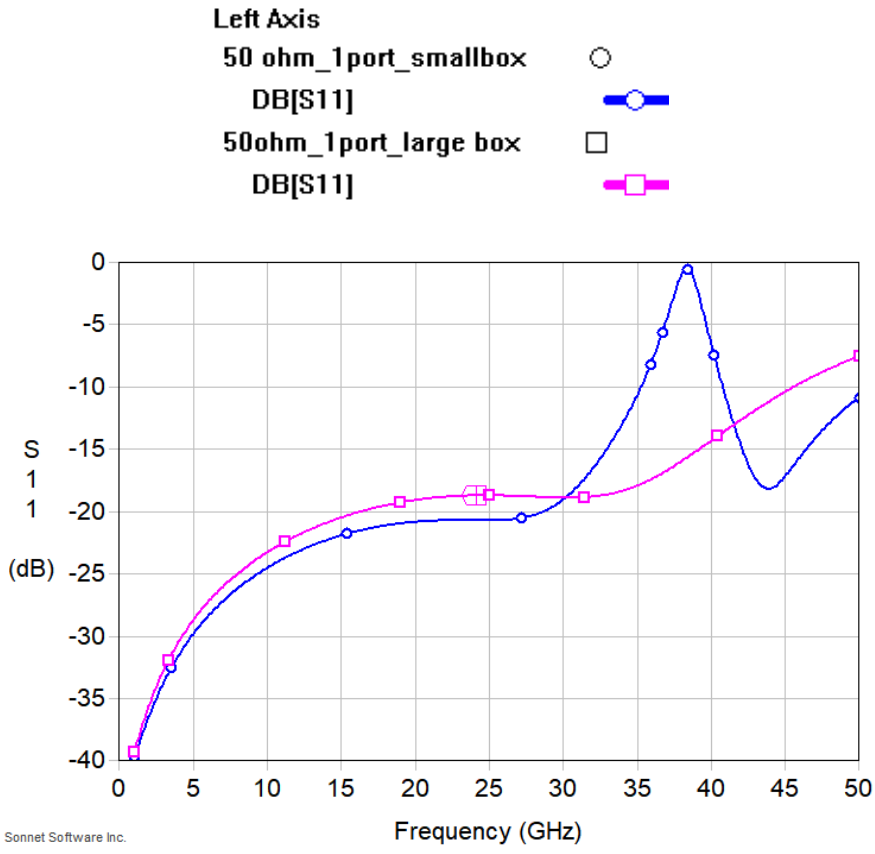


Figure 3.31. S_{11} of two identical circuits with different box sizes in Sonnet.

Chapter 4
Thermal Analysis at Cryogenic Temperatures

In this chapter, thermal analyses are conducted for some of the designed resistors in COMSOL [25]. The aim of this chapter is to analyze the impact of overheating the resistor layer at different power levels. It investigates how much the dissipated heat on the resistor layer raises the local temperature.

Different voltages are applied to the resistors, and temperature variations in different parts of the chip are studied. Additional thermal simulations are carried out in the R-2R ladder to see how heating a resistor affects other parts.

4.1 Cryogenic cooling

Each cooling system operates based on evaporation, conduction, radiation and convection, which are four fundamental processes for heat transfer. One of the challenges in designing cryogenic systems based on evaporation is a phenomenon known as vapor lock, whereby the flow of liquid is blocked. In fact, when liquid gas evaporates there is a tremendous increase in volume (in the order of 200). A technique to overcome this issue is to apply restrictions on the tube diameter [26].

Another aspect which should be considered to ensure favorable cooling is a vacuum. Thermal insulation, which is provided by a vacuum, is required for cryogenic refrigeration to cool the radiation shields and the sample. Moreover, a vacuum removes any air or minute particles which may contaminate the sample. The importance of a vacuum is highlighted, in that if any humidity exists during the cooling of the chamber, it would freeze and impede the process [23].

4.2 Thermal analysis

As mentioned in Chapter 3, there are five different temperature sensors in the Lakeshore cryogenic probe station showing the temperature of the probes during the sample stage, the 4°K shield stage, the radiation shield stage and the second shield stage. The lowest temperature that can be achieved for the sample stage is 3°K, while the critical temperature of niobium is 9.3°K. Therefore, temperature variations between the sample stages and the chips mounted in the chuck should be minimized to ensure that they remain well below critical temperature. There are a few different methods to mount samples on the chuck. The first approach is to use Apiezon-N grease, which is a typical adhesive for a vacuum

environment. The main drawback in using Apiezon-N grease is its low thermal conductivity (around 5mW/m.K) in cryogenic temperatures. The low thermal conductivity fails to maintain the sample's temperature close to the chuck's temperature. Another approach is to use silver paint, which has higher thermal conductivity compared to Apiezon-N grease at low temperatures [7]. Silver paste is used for mounting the device on the chuck, which guarantees good thermal conduction between the chuck and the sample.

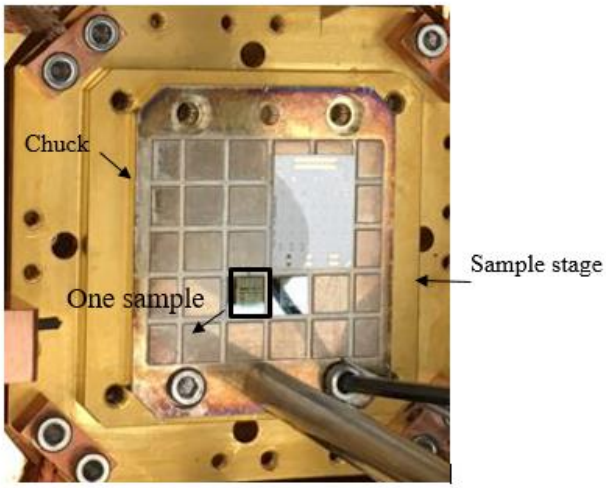


Figure 4.1. Image of samples mounted on the chuck.

To identify temperature variations over the structure when applying different voltages, 25 Ohm, 50 Ohm and a 1-bit R-2R ladder are modeled in COMSOL. Figure 4.2 illustrates the model for thermal analysis in COMSOL. As depicted, floating metals are not modeled for thermal analysis since simulations are done by applying DC voltage. Floating metals are exploited to compensate for variations at high frequencies. Figure 4.2 shows an adhesive layer and a silicon substrate with a thickness of 200 μm on top where the CPW transmission line, meander resistor, and RF probes are mounted with a thickness of 1 μm. The adhesive layer is assumed to be silver paint with a thickness of 150 μm. The properties of the materials used in the simulation are given in Table 4-1 to Table 4-3.

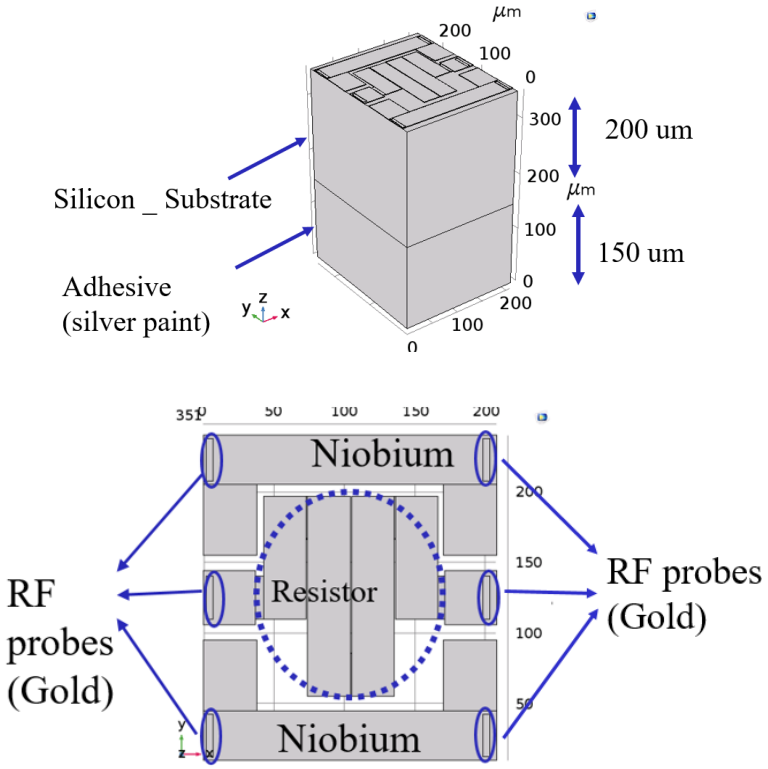


Figure 4.2. 3D model of 25Ohm resistor in COMSOL.

Table 4-1. Material Properties of Niobium

Properties	**Values**
Electrical conductivity	6.7e6 S/m
Heat capacity at constant pressure	265 J/kg.K
Density	8570 kg/m^3
Thermal conductivity	54 W/m.K
Coefficient of thermal expansion	7.3e-6 1/K
Young's modulus	200e9 Pa
Poisson's ratio	0.229

Table 4-2. Material Properties of Silicon

Properties	**Values**
Electrical conductivity	1e-12 S/m
Heat capacity at constant pressure	700 J/kg.K
Density	2329 kg/m^3
Thermal conductivity	150 W/m.K
Coefficient of thermal expansion	2.6e-6 1/K
Young's modulus	170e9 Pa
Poisson's ratio	0.38

Table 4-3. Material Properties of Silver

Properties	**Values**
Electrical conductivity	61.6e6
Heat capacity at constant pressure	235 J/kg.K
Density	10500 kg/m^3
Thermal conductivity	429 W/m.K
Coefficient of thermal expansion	18.9e-6 1/K
Young's modulus	83e9 Pa
Poisson's ratio	0.37

Conduction, convection and radiation are three different modes for transferring thermal energy in a process called heat transfer. Conduction refers to heat transfer between solids, while convection is heat transfer through fluids. Radiation is negligible in temperature lower than 400 °C [27].

In this simulation, the structure is in a chamber which is a vacuum, with temperatures below 10°K. Therefore, in this case, conduction is the leading mode for heat transfer. The backside of the adhesive layer which is in contact with the chuck is set to 3°K, as the temperature sensor displays. Figure 4.3 depicts the setting for the CPW transmission line. Different voltages are applied to terminal 1, while port 2 is set to 0 volts.

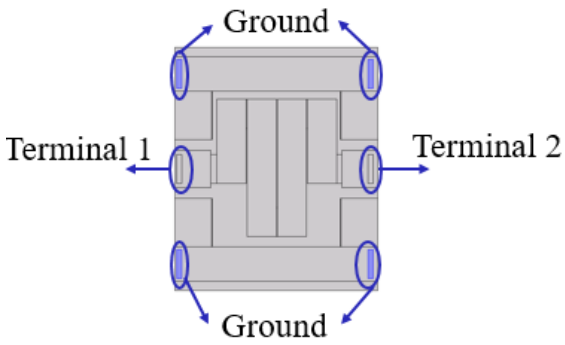


Figure 4.3. 2D schematic of resistor in COMSOL showing electric current setting.

4.2.1 Temperature distribution of 25 Ohm resistor in 4 °K

Figure 4.4 shows the simulation results when applying 1 volt. The device is designed to have a resistivity of 25 Ohm, so by applying 1 volt, the input power would be 0.04W or 16dBm. The temperature varies from 3 °K to 5.37 °K through the structure. The highest temperature in the transmission line is 4.64 °K. As the critical temperature of niobium is 9.3 °K, 4.64 °K is well below the critical temperature and thus assures a superconducting state.

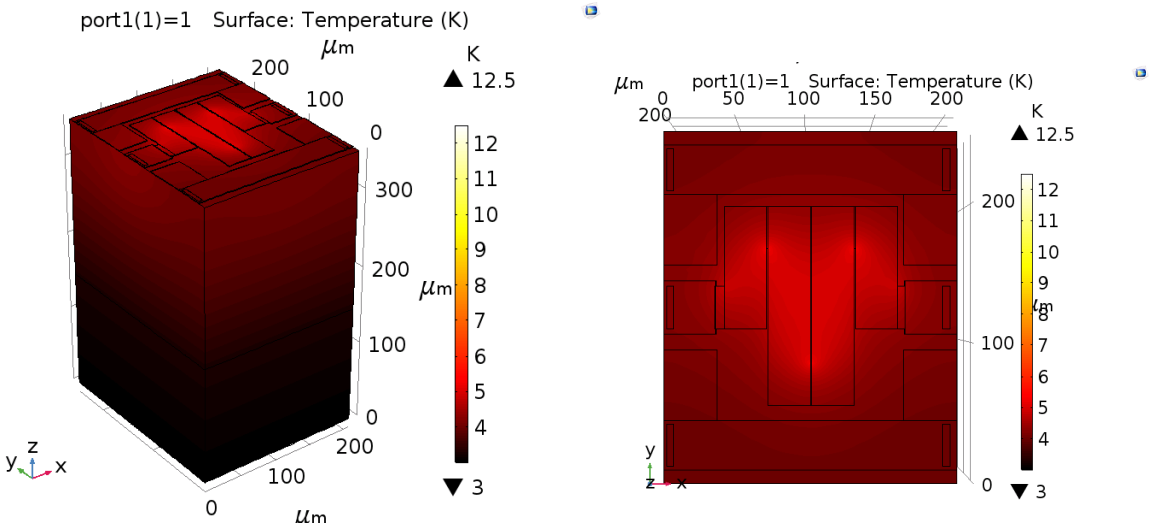


Figure 4.4. Temperature distribution through substrate and fabricated TL and 25 Ohm resistor by applying 1 volt at cryogenic; maximum temperature 5.37 °K.

Figure 4.5 shows the temperature variations when applying 1.5 volts. In this case, the input power is 19.54dBm and the temperature changes from 3 °K to 8.33 °K. The resistor is the most heated part. The temperature of the CPW TL is 6.70 °K at the hottest point, which is lower than the critical temperature of niobium. Although the temperature is well below 9.3°K, the difference may not be enough for superconducting.

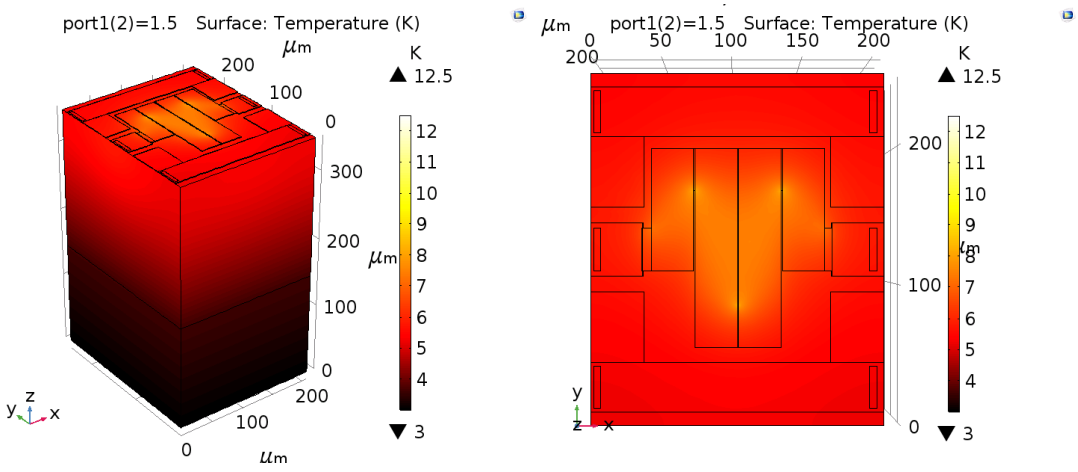


Figure 4.5. Temperature distribution through substrate and fabricated TL and 25 Ohm resistor by applying 1.5 volts at cryogenic; maximum temperature 8.33 °K.

According to the SFQ MIT-LL process, the maximum current of 0.066mA is recommended to be in a superconducting state. Therefore, in voltages higher than 1.65 volts, niobium-based transmission lines transit into a normal state. As illustrated in Figure 4.6, the input voltage is further increased to 2 volts and the temperature rises 12.5 °K in the device, reaching 9.59 °K at some points in the CPW TL.

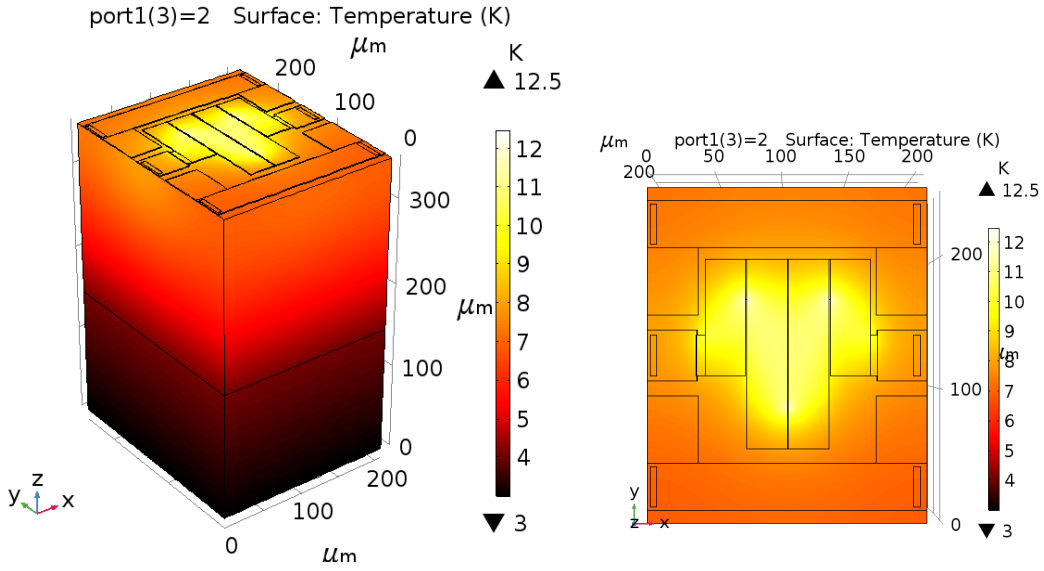


Figure 4.6. Temperature distribution through substrate and fabricated TL and 25 Ohm resistor by applying 2 volts at cryogenic; maximum temperature 12.5 °K.

4.2.2 Temperature distribution of 50 Ohm resistor in 4 °K

In this section, the temperature distribution in a 50Ohm resistor structure is investigated by applying different power levels, employing the same model as that used for the 25Ohm resistor.

Given a maximum current of (66mA) as proposed by MIT-LL, the corresponding voltage would be 3.3 volts for a 50 Ohm resistor. Increasing input voltage beyond 3.3 volts drives the transmission lines to a normal state. Figure 4.7 to Figure 4.9 display results for 1-volt, 2-volt, and 3-volt input levels. In the first figure, the temperatures vary from 3 to 3.79 °K and the highest temperature in the transmission line is 3.45 °K. Increasing the input to 2 volts increases the temperature in the resistor and transmission line to 6.16 °K and 4.76 °K, respectively. Further increasing the input to 3 volts raises the temperature in the resistor to 10.1 °K, while the temperature of the superconducting components is still 7 °K (i.e., two degrees lower than the critical temperature of niobium). Thus, by having an input of up to 3 volts or 22.5dBm, a 50 Ohm resistor would achieve acceptable performance in a superconducting state. On

the other hand, going beyond 22.5dBm, the superconductors would switch to normal state, as the temperature would not be adequate for superconducting. This is the expected result based on the maximum current in the process.

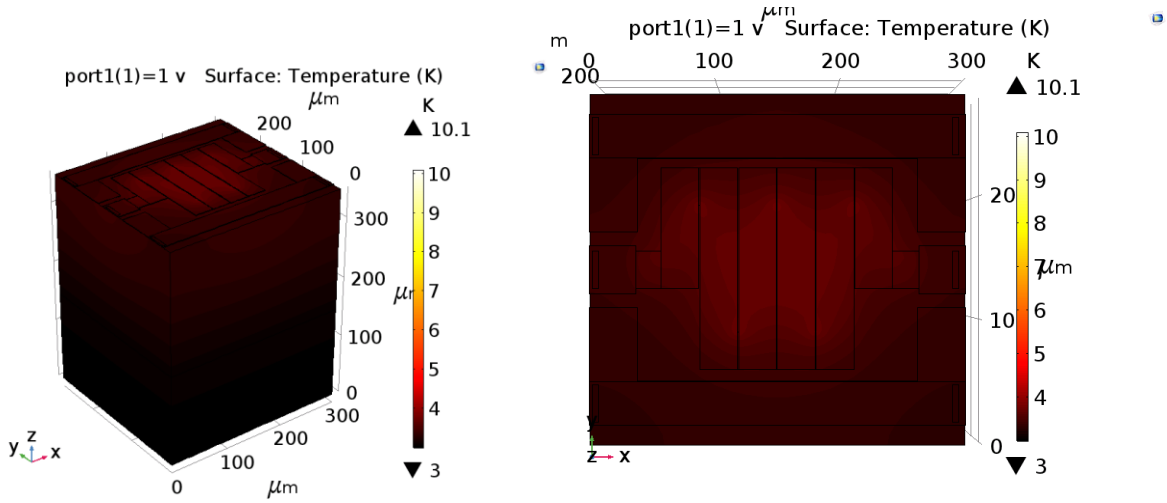


Figure 4.7. Temperature distribution through substrate and fabricated TL and 50 Ohm resistor by applying 1 volt at cryogenic; maximum temperature 3.79 °K.

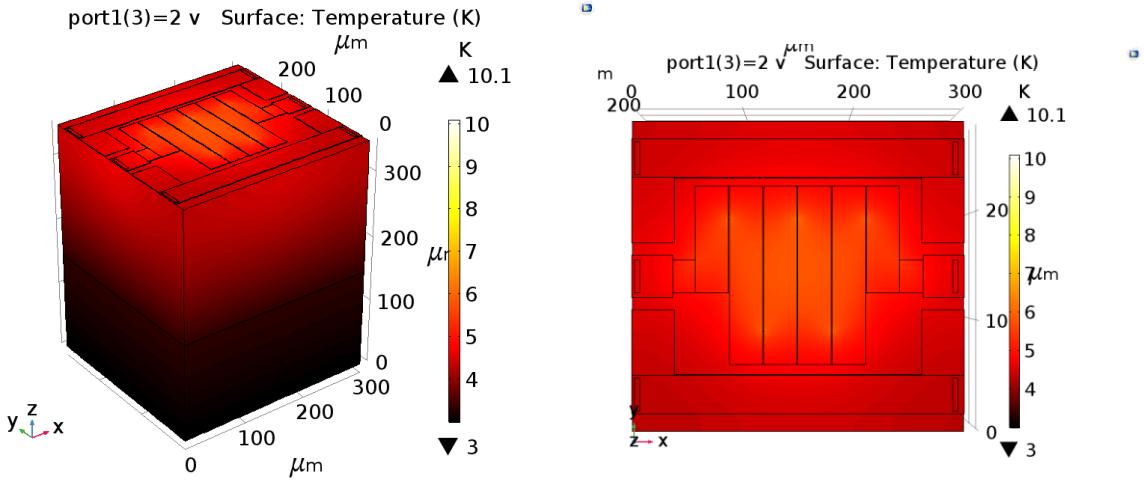


Figure 4.8. Temperature distribution through substrate and fabricated TL and 50 Ohm resistor by applying 2 volts at cryogenic; maximum temperature 6.16 °K.

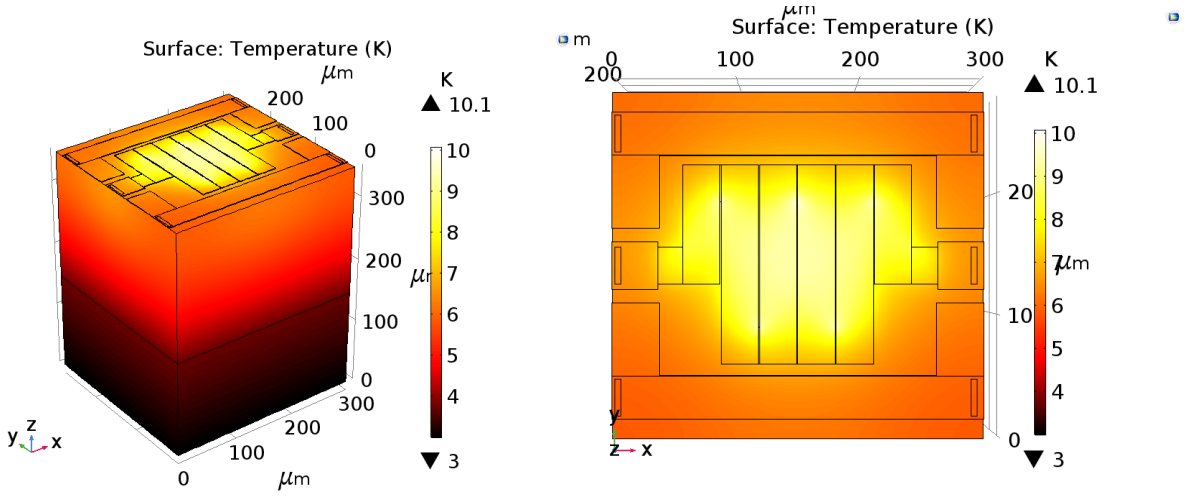


Figure 4.9. Temperature distribution through substrate and fabricated TL and 50 Ohm resistor when applying 3 volts at cryogenic; maximum temperature 10.1 °K.

4.2.3 R-2R thermal analysis in 4 °K

In this section, a 1-bit R-2R ladder, as depicted in Figure 4.10, is modeled in COMSOL and its temperature distribution is studied by applying different voltages.

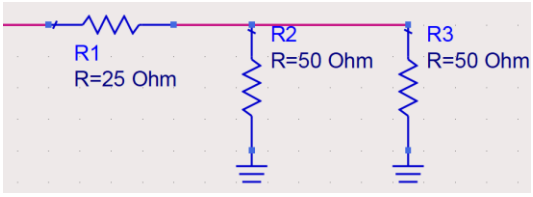


Figure 4.10. Schematic of 1-bit R-2R ladder.

A designed 25 Ohm resistor and 50 Ohm resistor in Sonnet are used to model a 1-bit R-2R ladder in COMSOL. The input impedance of the structure is assumed to be 50 Ohm. To validate the equivalent resistor, a 0.06A current is injected and the electrical potential distribution is plotted. Figure 4.11 shows the electrical potential which is in compliance with theory. As can be seen, 3 volts are the input, which is then divided into two branches.

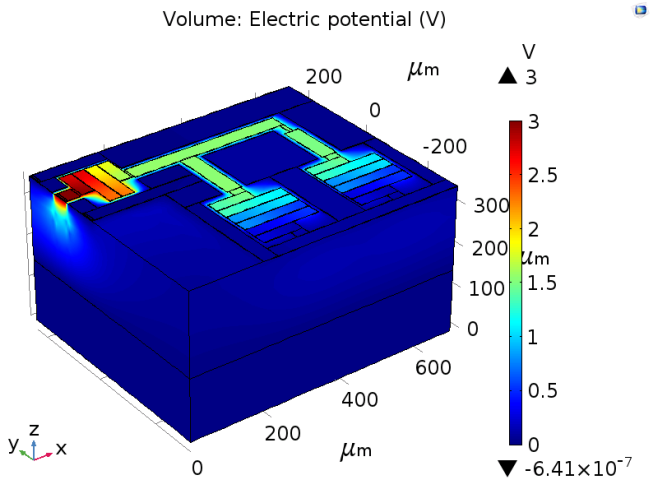


Figure 4.11. Electric potential in an R-2R ladder by injecting a 0.06A current.

Figure 4.12 depicts results when 1 volt is applied to the input. In this case, the hottest point (3.51 °K) is in the resistor layer, while the maximum temperature in the TL is 3.3344 °K. The CPW transmission lines remain in a superconducting state because the temperature is sufficiently low.

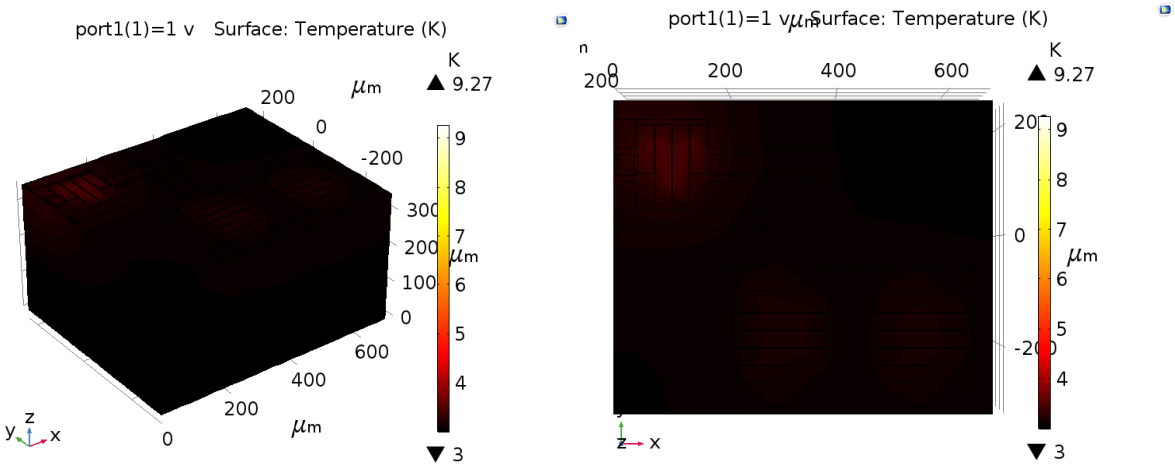


Figure 4.12. Temperature distribution in 1-bit R-2R structure when applying 1 volt at cryogenic; maximum temperature 3.51 °K.

As illustrated in Figure 4.13, by having 2 volts as the input, the temperature reaches 5.05 °K in the resistor, while the highest temperature in the transmission line is 4.33 °K. Under this condition, the device should have a good performance, as the temperature is low enough for superconducting.

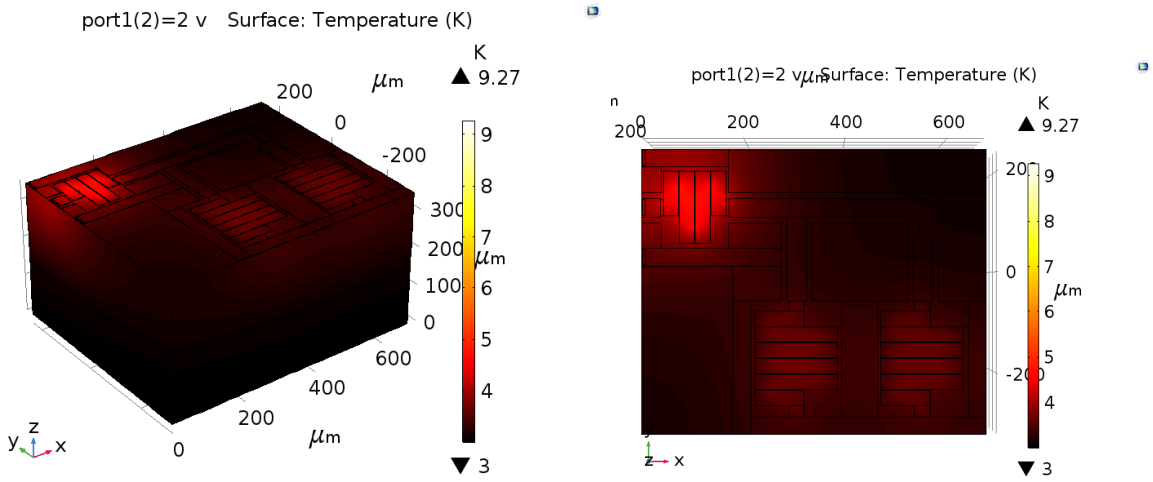


Figure 4.13. Temperature distribution in 1-bit R-2R structure when applying 2 volts at cryogenic; maximum temperature 5.05 K.

Figure 4.14 shows the results for an input with a value of 3 volts. The hottest point in the resistor layer and transmission line reaches 7.61 °K and 6.00 °K, respectively. The temperature of the superconductor parts remains 3 degrees below its critical temperature, thus securing the superconducting state without deteriorating the performance.

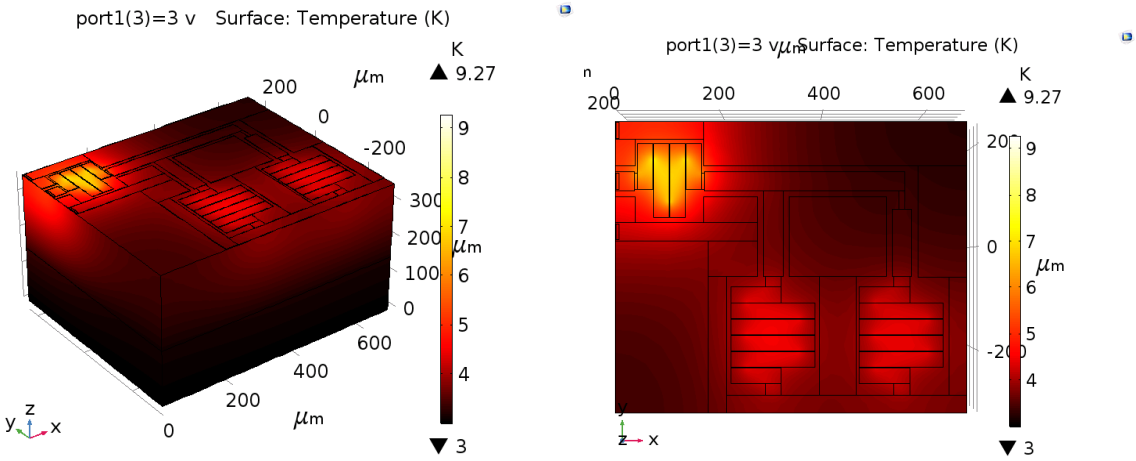


Figure 4.14. Temperature distribution in 1-bit R-2R structure when applying 3 volts at cryogenic; maximum temperature 7.61 °K.

Figure 4.15 demonstrates temperature distribution by having 3.5 volts as the input. According to the simulation, the highest temperature in the structure is 9.27 °K, which is located in the resistor layer. However, 7.09 °K is the highest temperature in the TL, and that is only 2 degrees less than the critical temperature of niobium. In this case, the voltage across the first resistor (25 Ohm) is 1.75 volts, which

is higher than the corresponding voltage for a maximum current of 66mA. Therefore, transition to a normal state is expected at this power level.

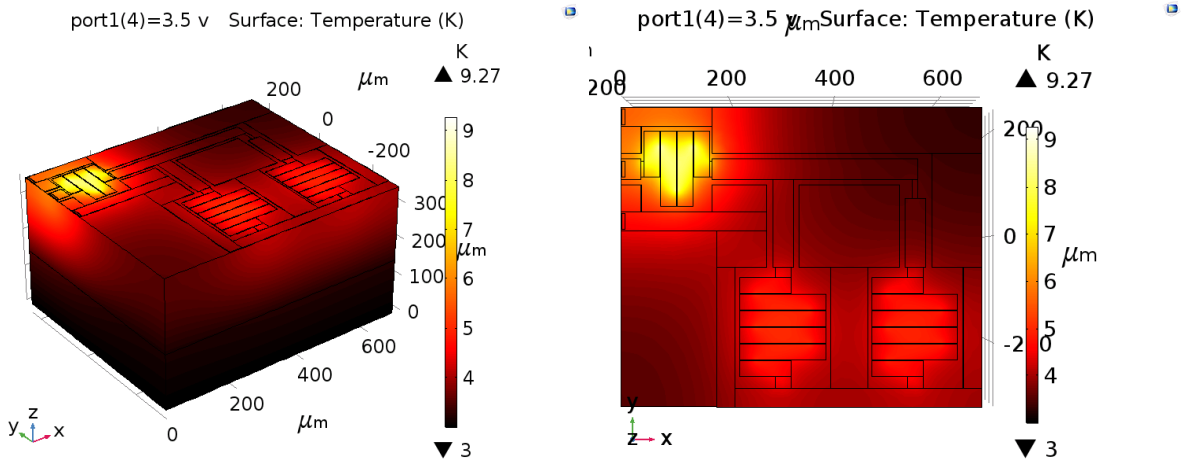


Figure 4.15. Temperature distribution in 1-bit R-2R structure when applying 3.5 volts at cryogenic; maximum temperature 9.27 °K.

4.2.4 Room-temperature thermal analysis of 25 Ohm resistor

Convection, conduction, and radiation are three types of transferring thermal energy. Radiation is only applicable in high temperatures, convection should be considered when there is a fluid in system, and conduction is for solid bodies. As shown in previous sections, conduction was the only way for heat transfer, owing to the fact that it was at cryogenic conditions and the temperature was not high enough for considering radiation. In this section, simulations are done at room temperature conditions and air comes in contact with the device. Therefore, convection and conduction are considered in the simulation.

Almost the same model as described in section 4.2 is used in this section, except that the structure is located in an air box to model convection heat transfer. The heat flux coefficient, which is the ratio between the heat flux density and the temperature variations between a solid body and a fluid, is an empirical value and is assumed to be $5 W/m^2K$ for convection in air. The boundary conditions are changed in such a way that initial temperature is assumed to be 293.15 °K (room temperature) and the bottom of the model, which is the outer side of adhesive layer, is set to 293.15 °K.

Figure 4.16 depicts the simulation results of a 25 Ohm resistor at room temperature by applying 1 volt as input. The temperature varies by 2 °K in the structure, which is similar to the simulation results at 4 °K.

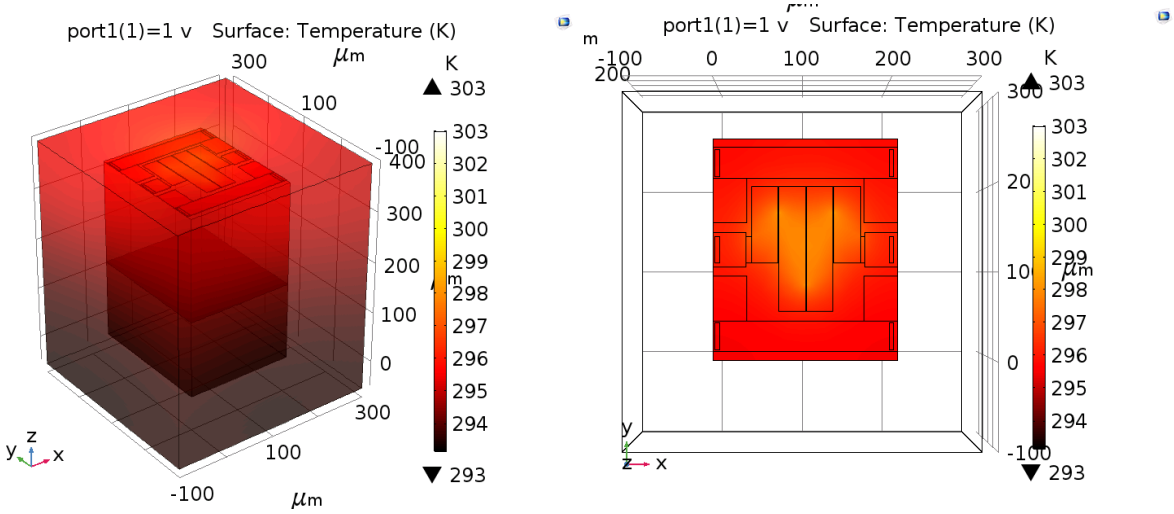


Figure 4.16. Temperature distribution in 25Ohm resistor structure when applying 1 volt at room temperature; maximum temperature 295 K.

Simulation results for a 1.5-volt input is shown in Figure 4.17. As shown, the temperature alters from 293.15 °K to 298 °K through the structure, which is about a 5 °K temperature difference. This is the same result as the temperature distribution at cryogenic temperature (5.33 °K difference in temperature through the structure).

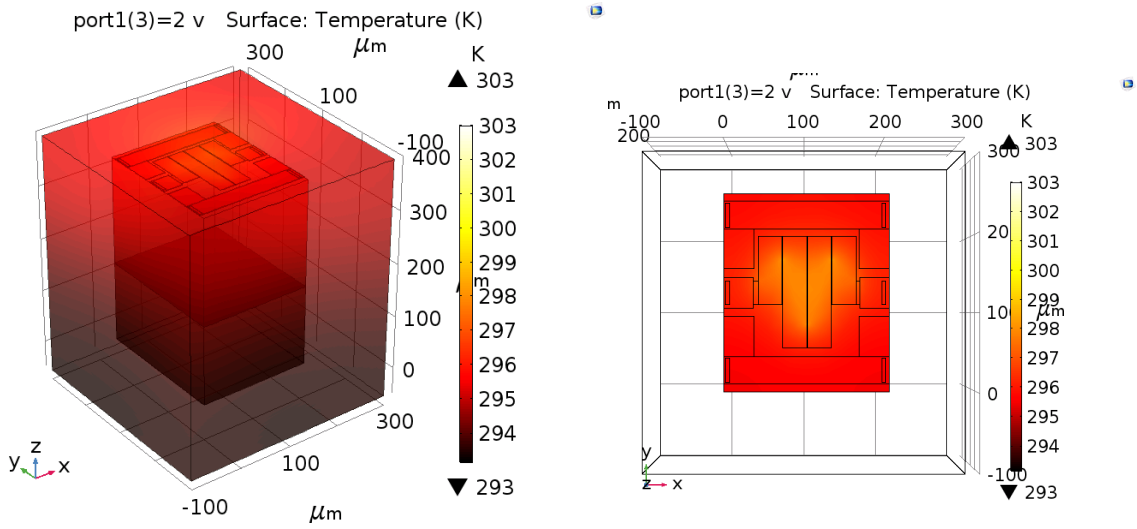


Figure 4.17. Temperature distribution in 25 Ohm resistor structure when applying 1.5 volts at room temperature; maximum temperature 298 °K.

Figure 4.18 depicts results for 2 volts. In this case, the temperature increases by 10 °K, roughly the same as the cryogenic case. .

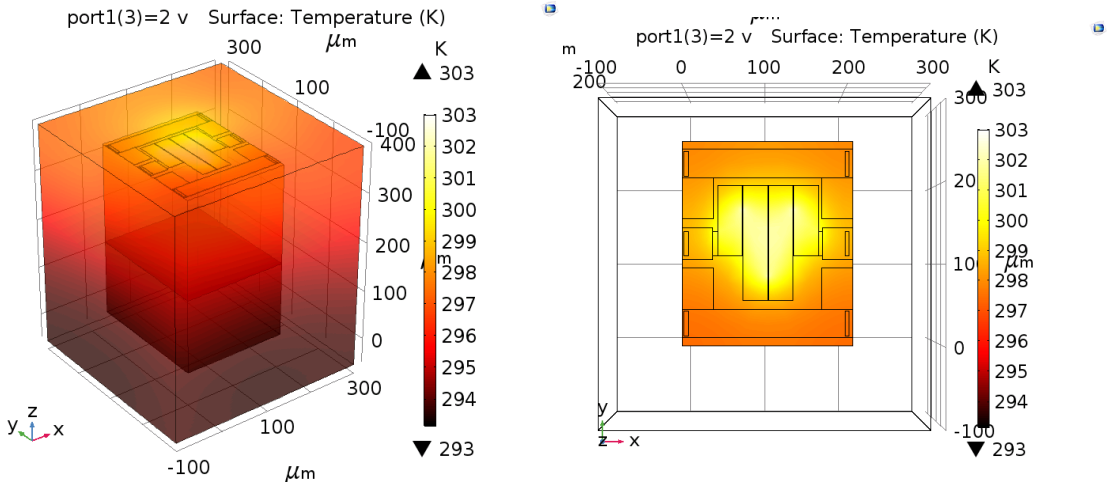


Figure 4.18. Temperature distribution in 25 Ohm resistor structure when applying 2 volts at room temperature; maximum temperature 303 °K.

Chapter 5
Conclusion

In this thesis, several wideband resistors impeded in multi-layer low-temperature superconducting circuits were designed, fabricated and tested. The dimensions of the designed resistors are all less than 440 μm x250 μm. The resistors were fabricated using the MIT-LL niobium process, which has eight niobium layers, with an extra gold layer on top for pads.

The resistors were designed to maintain their values from DC to 50GHz. In order to obtain frequency-independent resistors, floating metals were added to the structures and optimized to maximize the operating frequency range. The performance of designed resistors was analyzed both theoretically and experimentally. A 1-bit R-2R ladder was fabricated using the same process and measured at 4 °K in an RF cryogenic probe station.

The temperature distributions of some of the designed resistors were also investigated at cryogenic temperatures. Various power levels were applied to determine when the generated temperature exceeds the critical threshold temperature of niobium, which drives transmission lines into a normal state.

Future work could target various uncertainties both in simulations and measurements. The amount of heat generated by the resistor layer should be further studied, and the simulation results could be validated experimentally. Many other chips submitted for fabrication were not received prior to the publication deadline of this thesis. Therefore, measurements pertaining to those chips had to be left for future work.

Bibliography

1. Gupta, D., Inamdar, A. A., Kirichenko, D. E., Kadin, A. M., & Mukhanov, O. A. (2011, June). *Superconductor analog-to-digital converters and their applications*. In Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International (pp. 1-4). IEEE.

2. Cardwell, D. A., & Ginley, D. S. (2002). *Handbook of superconducting materials*. CRC Press.

3. Brock, D. K., Mukhanov, O. A., & Rosa, J. (2001). *Superconductor digital RF development for software radio*. IEEE Communications magazine, 39(2), 174-179.

4. www.HYPRES.com

5. Mukhanov, O. A. (2005). *Superconductor digital-RF electronics*. Update (Hypres Survey), 1, 11.

6. Sormeh Setoodeh (2011). *Superconducting Microwave Filters.* UWSpace. *http://hdl.handle.net/10012/5800*

7. Sara Sharifian Attar (2014). *Low Temperature Superconducting RF MEMS Devices.* UWSpace. *http://hdl.handle.net/10012/8888*

8. Mansour, R. R. (2002). *Microwave superconductivity*. IEEE transactions on microwave theory and techniques, 50(3), 750-759.

9. Mukhanov, O. A., Gupta, D., Kadin, A. M., & Semenov, V. K. (2004). *Superconductor analog-to-digital converters*. Proceedings of the IEEE, 92(10), 1564-1584.

10. Razavi, B. (1995). *Principles of data conversion system design* (Vol. 126). New York: IEEE press.

11. Mukhanov, O. A., Gupta, D., Kadin, A. M., & Semenov, V. K. (2004). *Superconductor analog-to-digital converters*. Proceedings of the IEEE, 92(10), 1564-1584.

12. Kalyani, N., & Monica, M. (2018, January). *Design and analysis of high speed and low power 6-bit flash ADC*. In 2018 2nd International Conference on Inventive Systems and Control (ICISC) (pp. 742-747). IEEE.

13. Mukhanov, O. A. (2011). History of Superconductor Analog-to-Digital Converters. *In 100 Years of Superconductivity*; Rogalla, H.; Kes, P., Eds.

14. Bahl, I. J. (2003). *Lumped elements for RF and microwave circuits*. Artech house.

15. Setoodeh, S., Mansour, R. R., & Gupta, D. (2013, June). *Multi-layer low temperature superconducting K-band filter and diplexer design*. In Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International (pp. 1-4). IEEE.

16. www.sonnetsoftware.com

17. https://www.ll.mit.edu/

18. Tolpygo, S. K., Bolkhovsky, V., Oates, D. E., Rastogi, R., Zarr, S., Day, A.L.,Weir, T.J., Wynn, A. L., Johnson, L. M. (2017). *Superconductor Electronics Fabrication Process with MoNx Kinetic Inductors and Self-Shunted Josephson Junctions*. 13th European Conferance on Applied superconductivity. Geneva, Switzerland.
19. Tolpygo, S. K., Bolkhovsky, V., Weir, T. J., Galbraith, C. J., Johnson, L. M., Gouker, M. A., & Semenov, V. K. (2015). *Inductance of circuit structures for MIT LL superconductor electronics fabrication process with 8 niobium layers*. IEEE Transactions on Applied Superconductivity, 25(3), 1-5.
20. Deal, W. R. (2008). *Coplanar waveguide basics for MMIC and PCB design*. *IEEE microwave magazine*, *9*(4), 120-133.
21. Villegas, M., Branner, G. R., Kumar, P. B., & Keese, W. (1993, August). *Analysis and design of microwave T-junction circuits for prescribed response characteristics*. In Circuits and Systems, 1993, Proceedings of the 36th Midwest Symposium on (pp. 604-607). IEEE.
22. http://www.keysight.com/
23. www.lakeshore.com
24. http://cirfe.uwaterloo.ca/
25. www.COMSOL.com
26. Ackermann, R. A., & Herd, K. G. (1996). *U.S. Patent No. 5,513,498*. Washington, DC: U.S. Patent and Trademark Office.
27. Kakoty, P., & Bhuyan, M. (2016) *Design and Electro-Thermal Analysis of a Meander Shaped Platinum Microheater for SnO2 Gas Sensors*. IEEE sponsored 3rd international conference on electronics and communication systems (ICECS).