SOI RF-MEMS Based Variable Attenuator for Millimeter-Wave Applications

by

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Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

The most-attractive feature of microelectromechanical systems (MEMS) technology is that it enables the integration of a whole system on a single chip, leading to positive effects on the performance, reliability and cost. MEMS has made it possible to design IC-compatible radio frequency (RF) devices for wireless and satellite communication systems. Recently, with the advent of 5G, there is a huge market pull towards millimeter-wave devices. Variable attenuators are widely employed for adjusting signal levels in high frequency equipments. RF circuits such as automatic gain control amplifiers, broadband vector modulators, full duplex wireless systems, and radar systems are some of the primary applications of variable attenuators.

This thesis describes the development of a millimeter-wave RF MEMS-based variable attenuator implemented by monolithically integrating Coplanar Waveguide (CPW) based hybrid couplers with lateral MEMS varactors on a Silicon–on–Insulator (SOI) substrate. The MEMS varactor features a Chevron type electrothermal actuator that controls the lateral movement of a thick plate, allowing precise change in the capacitive loading on a CPW line leading to a change in isolation between input and output. Electrothermal actuators have been employed in the design instead of electrostatic ones because they can generate relatively larger in-line deflection and force within a small footprint. They also provide the advantage of easy integration with other electrical microsystems on the same chip, since their fabrication process is compatible with general IC fabrication processes. The development of an efficient and reliable actuator has played an important role in the performance of the proposed design of MEMS variable attenuator. A Thermoreflectance (TR) imaging system is used to acquire the surface temperature profiles of the electrothermal actuator employed in the design, so as to study the temperature distribution, displacement and failure analysis of the Chevron actuator.

The 60 GHz variable attenuator was developed using a custom fabrication process on an SOI substrate with a device footprint of 3.8 mm $\times$ 3.1 mm. The fabrication process has a high yield due to the high-aspect-ratio single-crystal-silicon structures, which are free from warping, pre-deformation and sticking during the wet etching process. The SOI wafer used has a high resistivity (HR) silicon (Si) handle layer that provides an excellent substrate material for RF communication devices at microwave and millimeter wave frequencies. This low-cost fabrication process provides the flexibility to extend

this module and implement more complex RF signal conditioning functions. It is thus an appealing candidate for realizing a wide range of reconfigurable RF devices. The measured RF performance of the 60 GHz variable attenuator shows that the device exhibits attenuation levels ($| S_{21} |$) ranging from 10 dB to 25 dB over a bandwidth of 4 GHz and a return loss of better than 20 dB.

The thesis also presents the design and implementation of a MEMS-based impedance tuner on a Silicon-On-Insulator (SOI) substrate. The tuner is comprised of four varactors monolithically integrated with CPW lines. Chevron actuators control the lateral motion of capacitive thick plates used as contactless lateral MEMS varactors, achieving a capacitance range of 0.19 pF to 0.8 pF. The improvement of the Smith chart coverage is achieved by proper choice of the electrical lengths of the CPW lines and precise control of the lateral motion of the capacitive plates. The measured results demonstrate good impedance matching coverage, with an insertion loss of 2.9 dB.

The devices presented in this thesis provide repeatable and reliable operation due to their robust, thick-silicon structures. Therefore, they exhibit relatively low residual stress and are free from stiction and micro-welding problems.

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Dedication

To my loving husband Tejinder Singh

and my parents.

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Glossary

3G 3G is the third generation of wireless mobile telecommunications technology. 3G networks support services that provide an information transfer rate of at least 0.2 Mbit/s. Later 3G releases, often denoted 3.5G and 3.75G, also provide mobile broadband access of several Mbit/s to smartphones and mobile modems in laptop computers.

4G-LTE 4G is the fourth generation of broadband cellular network technology, succeeding 3G. 4G-LTE provides peak speed at 100 Mbit/s for high mobility communication and 1 Gbit/s for low mobility communication.

5G 5G is the latest generation of cellular mobile communications. 5G performance targets high data rate, reduced latency, energy saving, cost reduction, higher system capacity, and massive device connectivity. As per the ITU specifications, 5G demands speeds of up to 20 Gbit/s, achievable with wide channel bandwidths and massive MIMO (multiple-input and multiple-output) capabilities.

cut-off frequency a boundary in a system's frequency response at which energy flowing through the system begins to be reduced (attenuated or reflected) rather than passing through.

DC block component that prevents the flow of DC signals in to system, while allowing the high frequency RF signals to pass through. It is placed within a system to stop any signal with a frequency of 0 Hz from interfering with sensitive Rf components.

latching-switch a switch that maintains its state after being activated. A push-to-make, push-to-break switch would therefore be a latching switch - each time you actuate it, whichever state the switch is left in will persist until the switch is actuated again.

micro-fabrication the process of fabricating miniature structures of micrometre scales and smaller.

microstrip a type of electrical transmission line which can be fabricated using printed circuit board technology, and is used to convey microwave-frequency signals.

millimeter-wave the band of spectrum between 30 GHz and 300 GHz. Researchers are testing 5G wireless broadband technology on millimeter wave spectrum.

monolithic integrated circuit a set of electronic circuits etched or deposited on one small flat piece of semiconductor material that is normally silicon.

p-i-n diode a diode with a wide, undoped intrinsic semiconductor region between a p-type semiconductor and an n-type semiconductor region. The p-type and n-type regions are typically heavily doped because they are used for ohmic contacts.

parasitic capacitance an unavoidable and usually unwanted capacitance that exists between the parts of an electronic component or circuit simply because of their proximity to each other.

RF front-end modules RF front end is a generic term for all the circuitry between a receiver's antenna input up to and including the mixer stage. It consists of all the components in the receiver that process the signal at the original incoming RF, before it is converted to a lower intermediate frequency.

Single-Pole Single-Throw a switch that only has a single input and can connect only to one output. This means it only has one input terminal and only one output terminal and serves in circuits as on-off switches. When the switch is closed, the circuit is on. When the switch is open, the circuit is off.

Vanadium Oxide an inorganic compound, has a phase transition very close to room temperature (68 °C). Electrical resistivity and opacity of this material can change up several orders. Due to these properties, it has been widely used in surface coating, sensors, and imaging.

varactor a device that acts as a voltage dependent capacitor.

variable attenuators a tunable electronic device that reduces the power of a signal without appreciably distorting its waveform. An attenuator is effectively the opposite of an amplifier, though the two work by different methods. While an amplifier provides gain, an attenuator provides loss, or gain less than 1.

Abbreviations

Ar Argon

Au gold

BHF Buffered hydrofluoric acid

C_4F_8 octafluorocyclobutane

CCD charge coupled device

CIRFE Centre for Integrated RF Engineering

CMOS complementary metal-oxide-semiconductor

CPW co-planar waveguide

Cr chromium

DRIE deep reactive ion etching

FEM finite element modeling

FET field effect transistor

GaAs gallium arsenide

GHz gigahertz (1×10^9 Hz)

HF hydrofluoric acid

HfO_2 hafnium dioxide

HFSS High Frequency Structural Simulator

HR high resistivity

LED light emitting diode

LR low resistivity

MEMS microelectromechanical systems

MESFET metal semiconductor field effect transistor

MIM metal insulator metal

MMIC monolithic microwave integrated circuit

pHEMT pseudomorphic high electron mobility transistor

QNC Quantum Nano Centre

RF Radio frequency

RF-MEMS RF microelectromechanical systems

RIE reactive ion etching

SEM scanning electron microscope

SF_6 sulfur hexafluoride

SiO_2 silicon dioxide

SMD surface mount device

SOI silicon on insulator

THz terahertz (1×10^{12} Hz)

TR thermoreflectance

VNA vector network analyzer

VO_2 vanadium oxide

Chapter 1

Introduction

1.1 Motivation

Canada's wireless communication industry, an area of strategic national interest, is enjoying phenomenal growth with a market that remains fueled by the increased demands for multi-media services. RF devices represent a critical and substantive portion of any communication systems. Whereas third generation (3G) networks brought the internet everywhere and 4G LTE made it faster, 5G will vastly boost both the network capacity and speed by shifting towards the millimeter-wave range (30-80 GHz). Wireless networks operating at millimeter-wave frequencies will be capable of providing incredible data bandwidth and reduced latency between the devices they connect. Thus, 5G will not only allow users to send and receive nearly unfathomable amounts of data but can be employed in other applications like future autonomous vehicles.

The performance of future wireless systems critically depends on hardware capability. For 5G roll-out, affordable radio frequency (RF) devices are necessary to be implemented in RF front-end modules responsible for transmitting and receiving radio signals. Variable attenuators are highly in demand in high frequency equipment for adjusting signal level. They find applications in Radio Frequency (RF) circuits like automatic gain control amplifiers, broadband vector modulators and radar systems.

Currently available standard implementations of power attenuators are either based

on discrete components mounted on Printed Circuit Board (PCB) or use silicon-based CMOS processes for their implementation. PIN diodes and FETs are commonly used as variable resistors in attenuator circuits. However, the performance of such attenuators is degraded considerably at millimeter-wave frequencies and they exhibit limited power handling (typically up to few watts). Commercially available high-power variable attenuators usually employ mechanically tuning coaxial- or waveguide-based slow and bulky structures. Thus, there is a clear need to develop miniaturized variable attenuator that can deliver cost-effective and superior RF performance for 5G systems. RF-MEMS technology is seen as a potential solution to develop such passive devices and networks that can meet the demanding requirements posed by the upcoming 5G standards. The superior performance of RF-MEMS micro-relays, varactors, resonators and other passive devices in terms of high isolation, low insertion loss, high Q-factor and power handling capability has been widely reported in literature. Exploitation of the mechanical deformability in MEMS has allowed for adding tunability/reconfigurability in RF passive circuits like impedance tuners and variable attenuators. MEMS based microactuators have the potential to precisely control the large out-of-plane or in-plane motion of the attached structures, which can be successfully exploited to achieve controlled and wide tuning range.

In the modern-day smartphones, antenna integration with numerous other components has led to degradation in the quality of voice and data transmission. Currently, the key component that is used to address this problem is the reconfigurable impedance tuner. It can compensate for the input/output impedance variations between the different parts of RF-front-end circuit such as power amplifiers, antennas and low-noise amplifiers, hence allowing multi-band functionality. As we move towards higher frequencies with the increasing day to day consumer demands, there is a need to develop impedance tuners with large tunability, reduced hardware redundancy and power consumption. RF MEMS technology can be used to develop compact reconfigurable impedance tuner with improved tuning range, power handling capability, low insertion loss for high-power applications at microwave frequencies.

Most of the currently available high-aspect ratio lateral MEMS devices like RF single-pole single-throw switches, single-pole multiple-throw switches, varactors, phase shifters are fabricated using MetalMUMPs process, which is a thick nickel micromachining pro-

cess. There is a need to develop low-cost and simpler fabrication process for such high-aspect ratio structures. Over the past decades, there has been a significant advancement in microfabrication techniques like Si-Deep Reactive Ion Etching (DRIE), which needs to be explored for developing low-cost millimeter wave devices. The monolithic integration of all components on a single chip is an added advantage. Hence, the microdevices developed will serve as building blocks to further expand the structures for a wider range or integration with other modules to provide additional functionality.

1.2 Objectives

The purpose of this thesis is to investigate the feasibility of utilizing MEMS technology to implement innovative variable attenuator for millimeter-wave applications. A low-cost in-house fabrication process is adopted for fabricating the proposed design. The stages of this research include:

Development of a low-cost in-house fabrication process for high-aspect ratio lateral MEMS

A custom fabrication process for high-aspect ratio structures on SOI wafers is developed. It is particularly tuned to develop RF devices based on lateral MEMS. It is a low-cost process that involves single lithography step to co-fabricate the entire microsystem on chip. The sharp vertical structures are achieved using Si-DRIE. It is a high yield process and provides more reliable structures than surface micromachining processes.

Implementation of RF MEMS based variable attenuator

A millimeter-wave RF MEMS based variable attenuator is implemented by monolithically integrating CPW based hybrid couplers with lateral MEMS varactors on a SOI substrate. The varactor consists of a movable plate attached to the Chevron actuator. The variation of the gap between the movable plate and the signal line

with the applied voltage leads to a change in attenuation at the output. It is fabricated using the SOI MEMS fabrication process developed at University of Waterloo, hence it does not suffer from the dielectric charging, micro welding and stiction problems associated with RF MEMS devices realized using surface micromachining processes.

Detailed experimental thermal analysis of Chevron actuators

Thermoreflectance (TR) imaging is known for providing high-resolution and accurate thermal images of various (opto) electronic devices at the micro-scale. Thermal imaging microscopy was used for thermal characterisation of chevron actuator. It provided insights into temperature distribution, displacement and failure analysis of chevron actuator fabricated on SOI wafer, which can help in designing the microactuator with high-thermal uniformity and low power consumption.

Development, modeling and fabrication of novel RF MEMS impedance tuner

A novel RF-MEMS based impedance tuner is developed with a wide tuning range, good coverage on the Smith chart, compact size and high power handling capability. The tunability was achieved by using monolithically integrated contactless lateral MEMS varactors located strategically along a CPW line. These varactors are realized using laterally moving capacitive thick plates with their motion precisely controlled using Chevron actuators. This device is fabricated in-house using SOI MEMS process. It provides a reliable operation and is useful in high power applications, since it is constructed from lateral thick structures.

1.3 Thesis Outline

Following the motivation and objectives given in Chapter 1, Chapter 2 presents an overview of the different technologies available to realize variable attenuators with a focus on those operating at millimeter-wave frequencies. In Chapter 3, different types of MEMS actuators are investigated, particularly lateral electrothermal actuators. Additionally, the

fabrication process steps are discussed in detail. Chapter 4 investigates the use of thermoreflectance (TR) imaging to study temperature profiles of Chevron actuator. Chapter 5 presents the design and realization of monolithically integrated RF-MEMS based variable attenuator. RF MEMS-based impedance tuner is introduced in Chapter 6. Finally, a brief summary of the contributions of the thesis with an outline of the proposed future research are given in Chapter 7.

Chapter 2

Literature Review

Variable attenuators are highly in demand in high frequency equipment for adjusting signal level. They find applications in RF circuits like automatic gain control amplifiers, broadband vector modulators and radar systems. Variable attenuators have been implemented using various technologies; ranging from PIN diodes, FETs, and other CMOS based technologies to advanced materials like Graphene and VO_2 based variable attenuators. Their basic operating principles and performance are discussed in the following sections. RF MEMS-based variable attenuators are recently explored and are described in detail. The important design parameters of attenuator performance are attenuation range, bandwidth, return loss, power handling, flatness of attenuation, and circuit size/cost. Moreover, the linearity is also of utmost importance since the attenuator should not introduce non-linear distortion in the signal path.

2.1 Variable Attenuators Using Solid-State Devices

Semiconductor elements like PIN diodes or FETs are popularly used as the control element in variable attenuator circuits because of their speed and ease of design [1–4]. Such variable attenuators utilize the property of the semiconductor element that behaves like resistor at high frequencies. In the simplest form, variable attenuators can be implemented using a series connected or shunt connected p-i-n diode with a transmission line.

The major drawback of such approach is that the circuit's input and output impedance will vary with attenuation. To achieve a constant input and output impedance with the variation in attenuation, several types of variable attenuators circuits using PIN diodes and FETs have been presented: π attenuators, resistive line attenuators, bridged-T attenuators and hybrid coupled attenuators. The single hybrid coupled attenuator is used when reflected power must be minimized. However, double hybrid coupled attenuators are preferred in many applications due to its wider bandwidth, although it requires larger area than a single hybrid coupled attenuator [5, 6].

2.1.1 Single/Double Hybrid Coupler and Varactors

A single 3 dB quadrature coupler can be used to implement a variable attenuator by terminating its coupled ports with equal and variable terminations and the isolated port is used as output port as displayed in Fig. 2.1. The idea behind this circuit is that the isolated port of hybrid coupler presents infinite attenuation to the input signal when the coupled ports are terminated with reflection coefficients equal to zero [7]. Zero attenuation to the input signal is achieved when the coupled ports are equally terminated and entirely reflective (with reflection coefficient equal to one). This implies that when the termination resistance at the coupled ports is equal to the reference impedance of the coupler (e.g. 50 Ω), the insertion loss should theoretically, approach infinity. Between

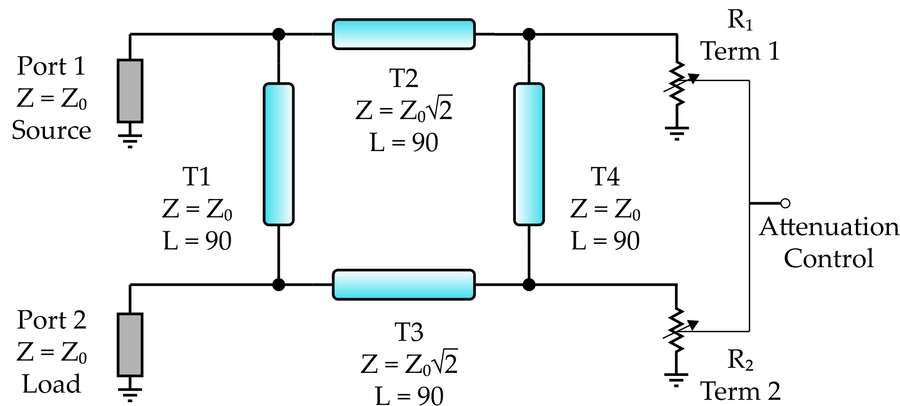


Figure 2.1: Schematic of a variable attenuator using 3-dB hybrid coupler

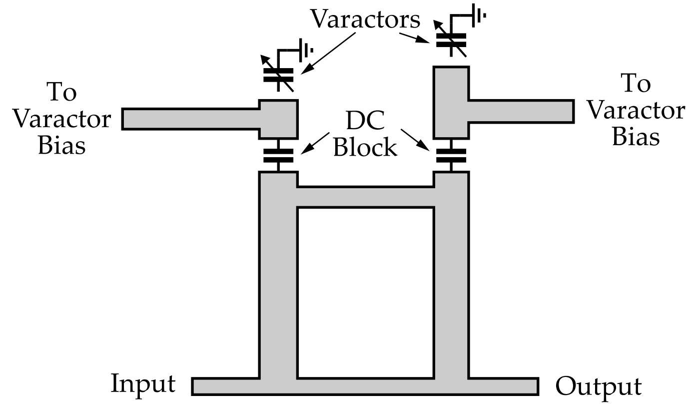


Figure 2.2: Reflection type variable attenuator with single hybrid coupler and two varactors.

these two extremes, the input port to the isolated port transmission is proportional to the magnitude of the reflection coefficient of the coupled ports.

One of the implementations of the above-mentioned idea can be seen in reflection type variable attenuators using a single hybrid coupler with two varactors [8]. As shown in Fig. 2.2, the completed circuit is a low-cost structure comprised of a microstrip quadrature coupler combined with integrated varactors to vary the attenuation from 2.2 dB to 17 dB over a 40% bandwidth for frequencies from 2.8 GHz to 4.2 GHz.

In reflection type variable attenuator, the signal present at the input of hybrid coupler is evenly split between the ports connected to the varactors, with a 90° phase difference between them. The signal entering each varactor is fully reflected into the coupler since

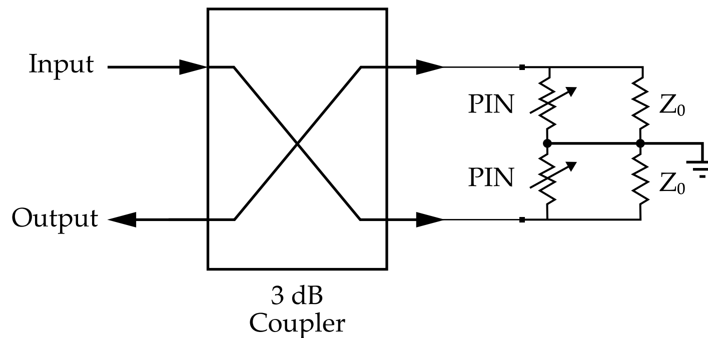


Figure 2.3: Variable attenuator using single hybrid coupler.

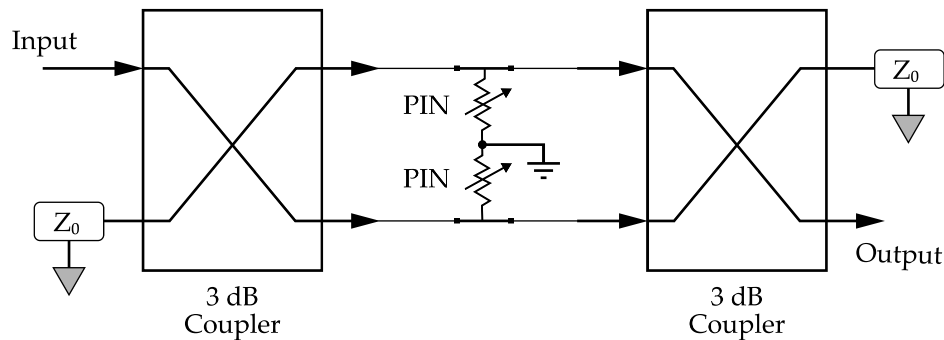
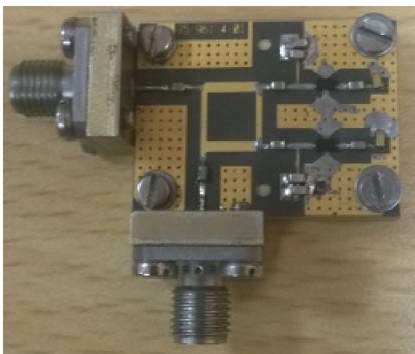


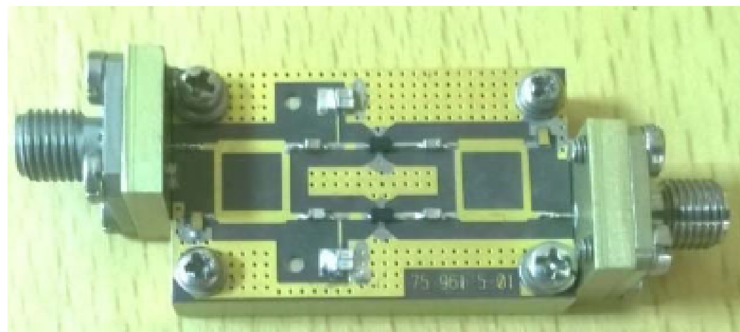
Figure 2.4: Variable attenuator using two hybrid couplers.

the varactors present a purely reactive load. The phase difference between the signals that are reflected from each varactor determines the amount of power present at the attenuator output and power reflected to the input. Chip capacitors are used as dc blocks in the circuit. Attenuation occurs because of destructive interference from input signal components that are reflected off each varactor. This implementation of attenuator can be improved by using thin film MIM capacitors instead of chip capacitors to get rid of the parasitics associated with them and replacing the varactor diodes with MEMS-type capacitor banks.

Another MESFET-based attenuator [10] is designed on the same principle with 3 dB quadrature directional coupler and two identical cold MESFETs, which act as voltage-



(**a**) Single hybrid coupler approach



(**b**) Double hybrid coupler approach

Figure 2.5: Variable attenuator fabricated on a PCB using single and double hybrid coupler approach [9].

controlled variable resistance reflection terminations. When zero gate bias voltage is applied, the drain-source channel resistance behaves as a short circuit and the insertion loss is at its minimum level. As the negative gate-bias potential is increased, the channel resistance increases, which results in a decrease in insertion loss.

The major advantage of using single hybrid coupler variable attenuator as shown in Fig. 2.3 is the simplified circuitry and good return loss performance. On the other hand, ripples can be seen in the high attenuation states due to directivity of the hybrid coupler. To eliminate this effect, another technique involves using two hybrid couplers as shown in Fig. 2.4 [9].

Fig. 2.5 shows the design implementation of variable attenuators using single vs double hybrid couplers and PIN diodes as the controllable resistances. A comparison of their performance is presented in [9]. The range of the diode resistance defines the dynamic range of the attenuator.

2.1.2 PIN Diodes and 0 dB Coupler

Due to the presence of intrinsic layer between its P-type and N-type layers, a PIN diode behaves as an ordinary PN junction diode at low frequencies and as a resistor at high frequencies whose value can be controlled by current. The high frequency equivalent circuit of PIN diode is shown in Fig. 2.6. At high frequencies, the PIN diode can be considered as a pure resistor.

A variable attenuator has been formed as shown in the schematic diagram in Fig. 2.7 by combining the PIN diode with a 0 dB branch line coupler [11]. It utilizes this resistive

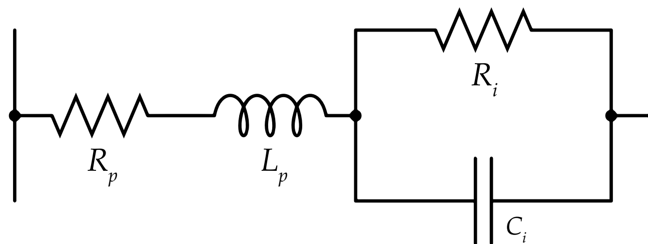


Figure 2.6: High frequency equivalent circuit of PIN diode.

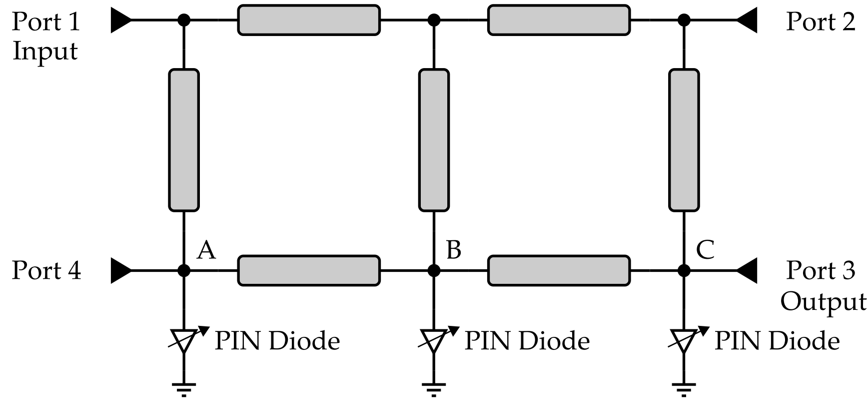


Figure 2.7: Schematic diagram of variable attenuator showing the PIN diodes and 0-dB coupler.

characteristic of PIN diodes. The 0 dB coupler is formed by 50 Ω quarter wavelength microstrip lines. The nodes A, B, and C can be floating or grounded depending on the resistance offered by the PIN diodes, which can be ideally varied from infinity to zero. When the PIN diodes have infinite resistance, the variable attenuator circuit acts as a 0-dB coupler alone, and the power incident at port 1 is transferred without any attenuation or reflection to port 3. Hence the current across the PIN diode acts as the controlling element for the output signal attenuation level. The PIN diodes are mounted through via holes on a thin board with the microstrip and the attenuation monotonically varies from 0.7 dB to 23 dB with the control voltage at the center frequency of 1.9 GHz.

However, the performance of such variable attenuators suffers from non-linearity issues precluding their use in applications where the signal level needs to be controlled without introducing intermodulation components. Moreover, the performance of semiconductor based attenuators is considerably degraded when operating at millimeter-wave frequencies. Variable attenuators that use diodes as variable resistors require dc blocks and bias circuits for operation. At the millimeter wave frequencies, this bias circuit becomes larger than the coupler itself, making it inefficient at higher frequencies.

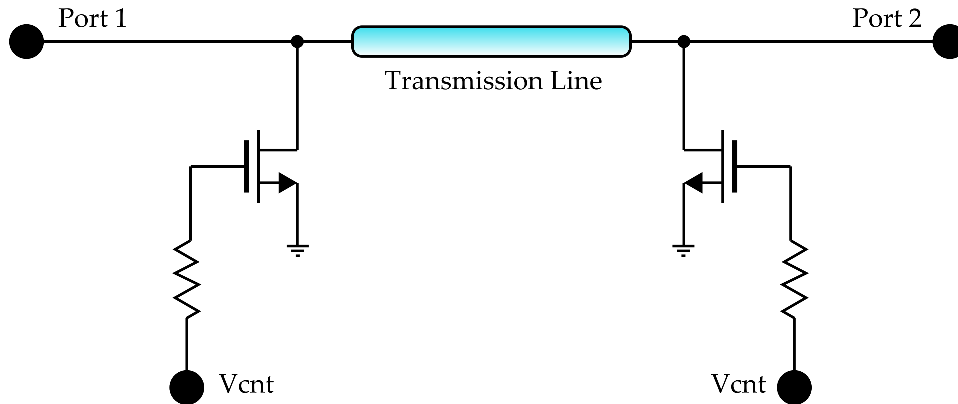


Figure 2.8: Variable attenuator π-configuration showing a transmission line and two shunt NMOS transistors.

2.1.3 Millimeter Wave CMOS-Based Variable Attenuator

Most of the analog type voltage-controlled attenuators use PIN diodes but these have some inherent drawbacks, such as high dc power consumption, narrow bandwidth, and integration limitations.

Conventional attenuator topologies can be categorized into T-, π- [12, 13], or Bridged-T [14–16] networks based on the arrangement of series and shunt branches. These consist of tunable components distributed in series and shunt between the input and output. The series components consist of the signal path and thus control the flow of passing signals, and the shunt tunable components connect the signal path to ground, thus divert the required amount of signal.

Fig. 2.8 shows the π-network used in designing variable attenuators comprising of a series transmission line and two shunt NMOS transistors connected from the signal path to ground. A continuous variable attenuator with wide bandwidth has been developed using 65 nm CMOS process [12]. The variable attenuator is designed using π-configuration with a series transmission line and three shunt FETs on one side of the transmission line. The amount of attenuation is determined by the impedance of the transistors, consisting of channel resistance and parasitic capacitance. Using three transistors in parallel with independent gate bias helps in achieving variable impedance, which expands the attenuation range. Hence, as the voltage bias is varied from 0 V to

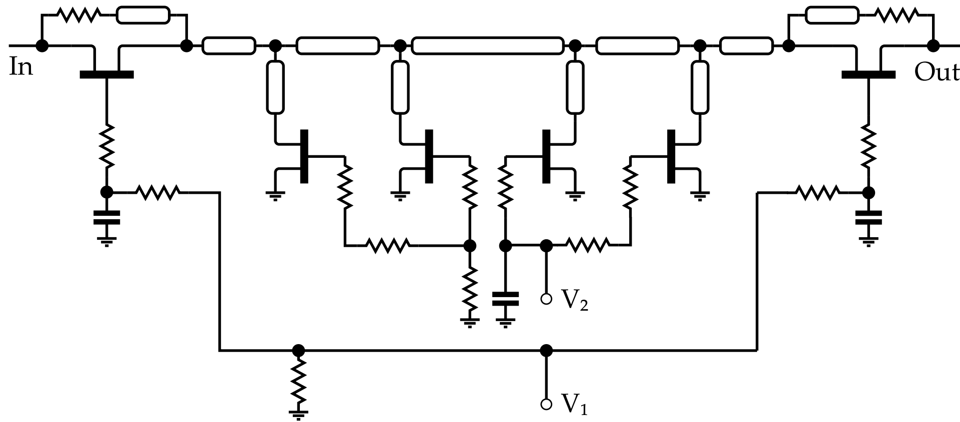


Figure 2.9: RF circuit schematic of the DC-50 GHz MMIC attenuator.

1.2 V, an attenuation range of more than 16 dB is achieved from DC–110 GHz.

The conventional GaAs MESFETs used as voltage-controlled variable resistors in the variable attenuator T- or π- topology suffer from performance degradation at high frequencies, basically limiting their operation beyond 20 GHz. This parasitic capacitance problem has been overcome by using a MMIC FETs based improved circuit techniques [17]. As shown in Fig. 2.9, this attenuator although being a T-type topology, distributed a shunt FET into four cells interconnected by a length of high impedance transmission lines. This attenuator demonstrated a 30 dB dynamic range of attenuation over a DC–50 GHz frequency band with a minimum insertion loss of 1.8 dB at 26.5 GHz and 2.6 dB at 40 GHz.

Another π-configuration can be seen in [13], where an adaptive bootstrapped body biasing technique is used to effectively reduce variations in transistor impedance resulting from large input signals. This improves the linearity of the attenuator significantly.

A compact DC–40 GHz variable attenuator MMIC has been developed by B. Lefebvre, et al., utilizing a standard T-configuration [18]. This configuration requires two control voltages for the series- and shunt transistors. The use of triple-gate transistors provides the advantage of achieving higher saturation levels in comparison to single gate transistors with minimal layout changes. Apart from FETs, Gallium Arsenide (GaAs) pseudomorphic high-electron mobility transistors (pHEMTs) were also utilized in fully integrated systems, but they face challenges in power handling capability and high-

Figure 2.10: GDTs with wire leads, no wire lead and surface mount packages. [21].

frequency performance [19].

Nevertheless, high-frequency performance is degraded due to resonance and parasitic effects. Recently, D. P. Nguyen, et al., reported a stacked-FET based voltage-controlled attenuator [20]. This topology not only enhances power handling capability, but also allows for wideband performance from 1.5 GHz to 45 GHz, low insertion loss (minimum insertion loss 1.9 dB) and large dynamic range of 26 dB. Moreover, the output power has excellent flatness over the entire frequency band.

2.2 Gas Discharge Tube-Based Variable Attenuator

Gas Discharge Tube (GDT)-based approach is particularly useful in emerging applications that involve high temperature and/or pressure and require high power and fast response times, where conventional techniques cannot be used [22]. A travelling electromagnetic (EM) wave exhibits reflection, attenuation and transmission coefficients when incident on a plasma region. These coefficients depend on the values of plasma oscillation and electromagnetic wave frequencies, i.e. ω_p and ω, respectively. Plasma frequency is decided by the electron number density (n_e) in the discharge area. High ω_p/ω ratio leads to high reflection. Since plasma can be turned on and off within a few nanoseconds, a very fast plasma-based RF switches and attenuators can be built on this principle. This work demonstrates the capability of low temperature plasma to be used as a tunable element in variable RF attenuator structures. As shown in Fig. 2.10, GDTs are available in no wire lead, wire lead and surface mount forms with two or three elec-

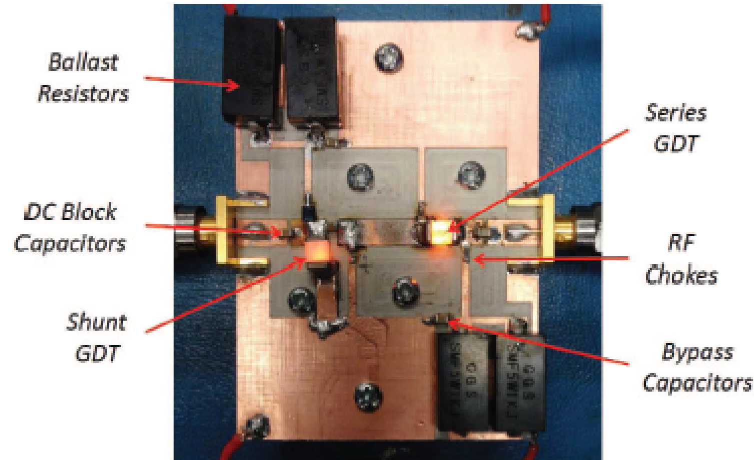


Figure 2.11: Fabricated GDT-based variable RF attenuator showing GDTs connected in series-shunt topology [22].

trodes in an enclosure filled with a non-radioactive rare gas e.g. argon, helium or neon.

Two independently controlled surface mount GDTs in a series-shunt configuration as shown in Fig. 2.11 result in a variable attenuator with maximum attenuation of 20 dB with 2 dB flatness over the 0.5 GHz to 1.2 GHz frequency range.

2.3 Graphene-Based Variable Attenuator

Other types of variable attenuators at microwave and millimeter wave frequencies are based on graphene based resistive elements [23, 24] have also been recently explored. They utilize the property that the graphene film can range from being a discrete conductor to a highly resistive material, depending on the externally applied voltage. A micrometric layer of graphene flakes is implemented in electronically tunable microstrip attenuator. As shown in the measurement setup in Fig. 2.12, the attenuator consists of a microstrip line with a gap that is filled with graphene nanoplatelets with the dimension in the order of 5 µm to 10 µm.

The measurements are performed with different values of dc voltage V_{dc} applied to the bias tees. Current I_{dc} increases with increasing V_{dc}, with suggests decreasing

resistance with applied voltage as shown in Fig. refgraphene-2.

The resistance of graphene changes with applied voltage, and the attenuator exhibits tunability of the insertion loss over the entire frequency range from 1 GHz to 20 GHz. A larger tuning range of 5.5 dB is obtained at lower frequency of 1 GHz and a smaller

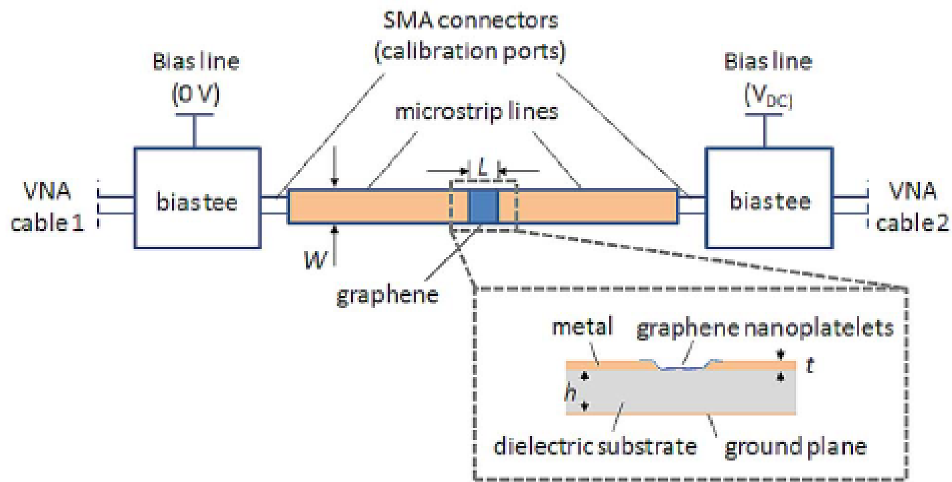


Figure 2.12: Measurement setup of the graphene-based microstrip attenuator [23].

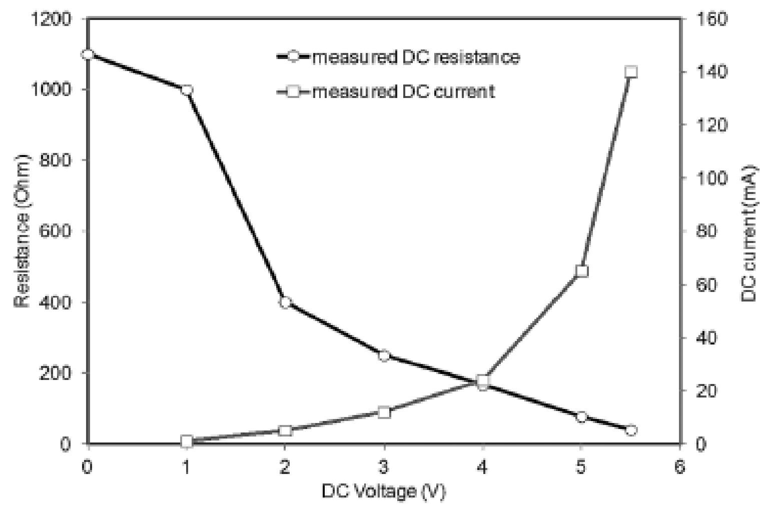


Figure 2.13: Measured dc current vs dc resistance of the graphene-based microstrip variable attenuator [23].

tuning range of 2.5 dB at 20 GHz.

2.4 Metal-Insulator Transition Material (VO_2) Based Variable Attenuator

Another alternative to PIN diodes has been provided by J. Jiang et al [25]. They have replaced PIN diodes with vanadium dioxide (VO_2)-based resistive film while using the 0-dB coupler as shown in Fig. 2.14 and 2.15.

Vanadium dioxide is a metal-insulator transition material that has the ability to switch between a metal state and an insulator state with the externally provided heat to the film. It undergoes a change in sheet resistance from 48 Ω/□ to 47 kΩ/□ when voltage is applied to the microheater.

This not only provides excellent performance at millimeter-wave frequencies but also provides monolithic integration of thin-film VO_2 with the 0-dB coupler and the bias heater circuit on a single chip.

The measurement results show that the device provides a continuous attenuation tuning range of 13 dB, and a return loss of 15 dB over the bandwidth of 5 GHz at 30 GHz as shown in Fig. 2.16.

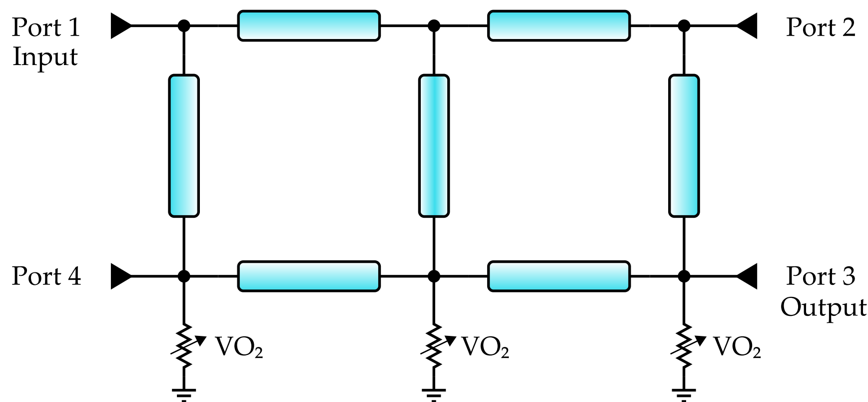


Figure 2.14: Schematic of the variable attenuator using VO2 variable resistor and 0-dB hybrid coupler.

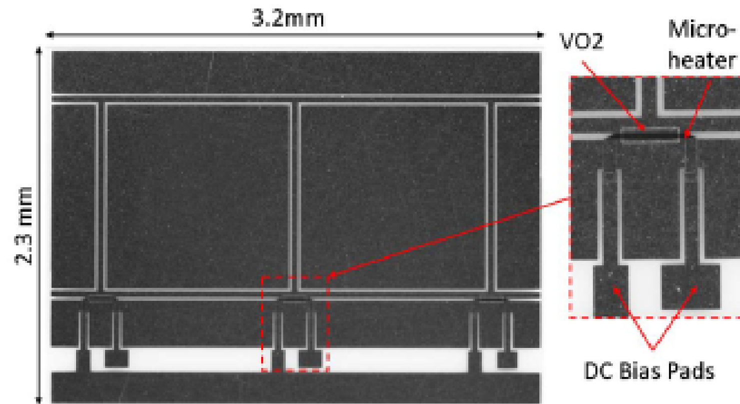
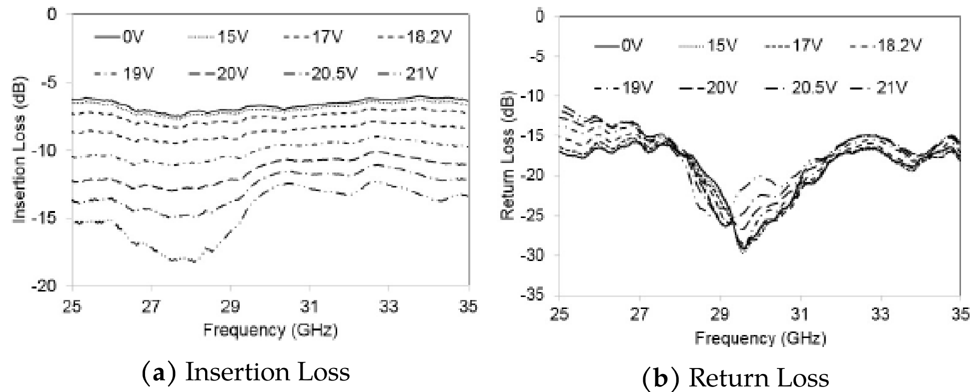


Figure 2.15: Optical micrograph of the fabricated variable attenuator showing micro-heater elements [25].



(**a**) Insertion Loss

(**b**) Return Loss

Figure 2.16: Measured RF performance of VO_2 based variable attenuator [25].

2.5 RF-MEMS Based Millimeter-Wave Variable Attenuators

The upcoming field of 5G demands RF devices that operate at high frequencies especially in millimeter wave range. RF-MEMS technology is capable of providing RF devices like impedance tuners and variable attenuators with boosted characteristics in terms of losses and flatness of attenuation. The flexibility to merge more signal conditioning functions on the same RF-MEMS device makes them even more appealing to 5G applications. For

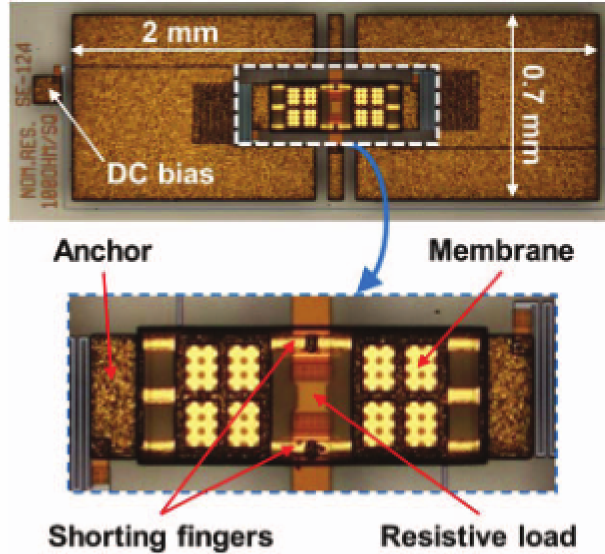


Figure 2.17: (Top image) The micrograph of the fabricated variable attenuator showing CPW lines and DC bias pads, (Bottom image) Close-up of the fabricated device showing electrostatically-controlled gold membranes, poly-Si resistive load, and shorting fingers [26].

example, merging the attenuation and phase shifting.

The first published attempt using this technology was by J. Iannacci et.al., who developed RF-MEMS based basic 2-state attenuator module [26, 27]. The device is fabricated using surface micromachining and consists of a series poly-Si Boron doped buried resistive load inserted on the RF line, which can be shorted by electrostatically actuating the suspended thin gold membranes above the resistor as shown in Fig. 2.17.

However, it has only two levels of attenuation. When the load is inserted, and gold membranes are in suspended rest position (no DC bias applied), a flat attenuation level (S_{21}) is observed over the whole range. When the gold membranes are pulled down by electrostatic actuation (DC bias greater than the pull-in voltage), the load is shorted as the RF signal finds a low-impedance path through the gold membrane and the module exhibits an insertion loss (S_{21}) better than 1.4 dB up to 50 GHz.

Another design variation has been proposed by J. Iannacci et. al. with the resistive load connected in series or shunt configuration on the RF line and the attenuation is ON/OFF switched by electrostatically driven MEMS micro-relays [27]. Hence, it oper-

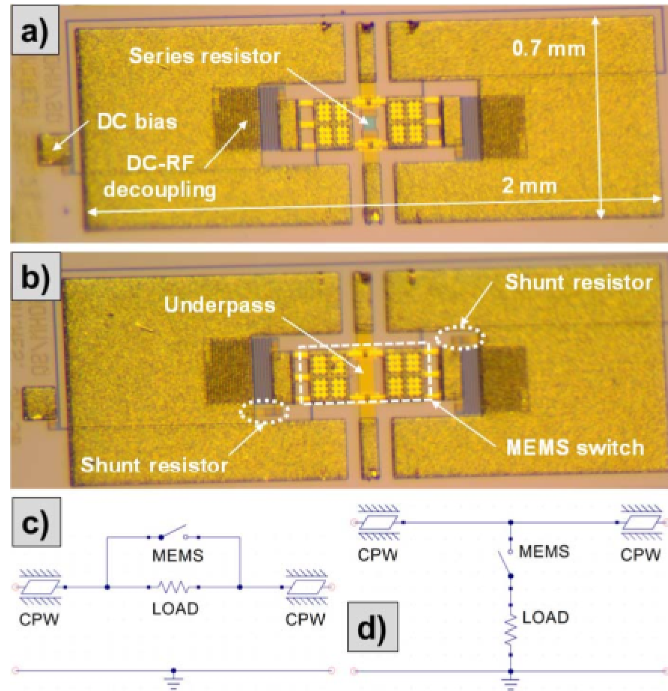


Figure 2.18: (a) Micrograph of the series design with an in-line poly-Si resistor; (b) Micrograph of the shunt design with two shunt-to-ground poly-Si resistors; (c) lumped-element model of series design; (d) lumped element model of the shunt attenuator [27].

ates on a similar principle as the one previously mentioned and provides a flat two step variable attenuation up to 110 GHz. As shown in the micrographs and lumped-element models in Fig. 2.18, in the series attenuator when the MEMS switch is actuated, it shorts the in-line resistive load. While in shunt configuration, when the MEMS switch is actuated, it inserts a shunt-to-ground resistive path.

X. Guo et. al. demonstrated a compact (2.45 mm $\times$ 4.34 mm $\times$ 0.5 mm) 3-bit microwave attenuator based on RF-MEMS single-pole double-throw (SPDT) switches and a resistive attenuation module [28]. As shown in Fig. 2.19, it is constructed by cascading three 1-bit attenuator units designed for 10-, 20- and 40 dB attenuation. The SPDT switches are used to toggle between each attenuation module path and a reference path to realize the target signal attenuation. The reference path is a fundamental CPW transmission line with a power consumption as low as possible. The attenuation path was

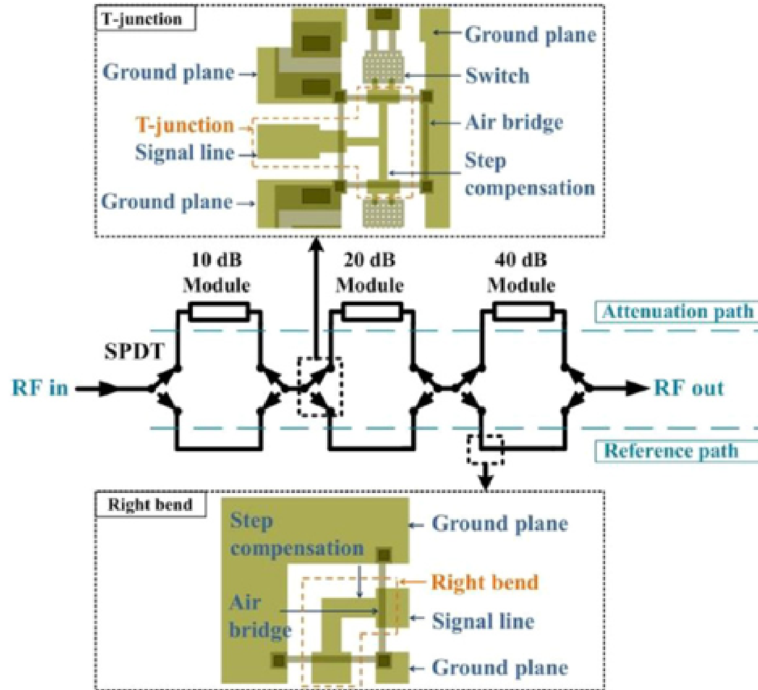
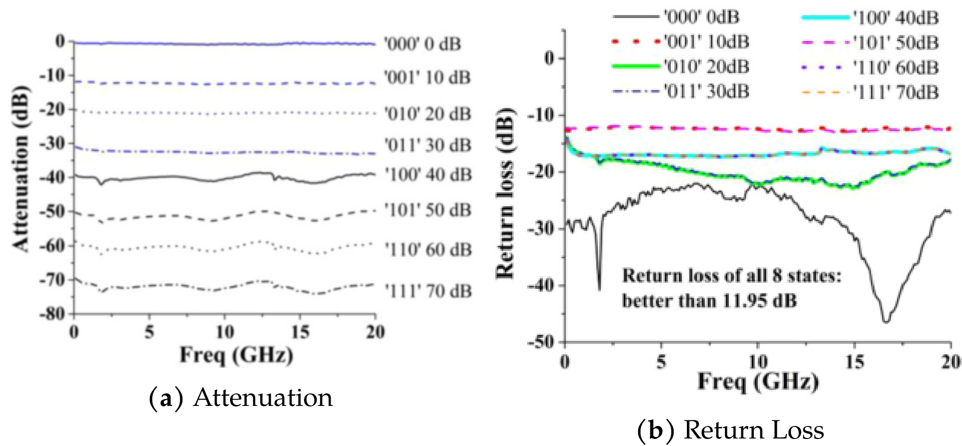


Figure 2.19: Overview of the 3-bit reconfigurable attenuator based on RF MEMS SPDT switches. [28]

the function module and absorbed signal power depending on the resistive network. By routing the signal through the selected transmission path using SPDT switches, attenuation performance of 10 dB to 70 dB in the frequency range 1 GHz to 20 GHz with an accuracy better than ±1.88 dB at 60 dB and error less than 2.22 dB at 10 dB is achieved as shown in Fig. 4.2.

Recently, 8-bit reconfigurable power attenuator up to 110 GHz has been developed using RF-MEMS technology available at CMM-FBK, in Italy [29]. The device (with a footprint of 3 mm × 1.95 mm) is based on CPW configuration and comprises eight cascaded stages (8-bit), thus implementing 256 different network configurations. As shown in Fig. 2.21(a), each of these stages has electrostatically actuated MEMS ohmic switches, independently controllable by applying DC bias to the pads. Depending on whether the micro-relay is in the rest position (OFF) or pulled-in (ON), the switches select or deselect a series of low-resistivity (LR) poly-Si resistors as shown in the equivalent network



(**a**) Attenuation

(**b**) Return Loss

Figure 2.20: RF performance of each state of the fabricated 3-bit MEMS attenuator [28]

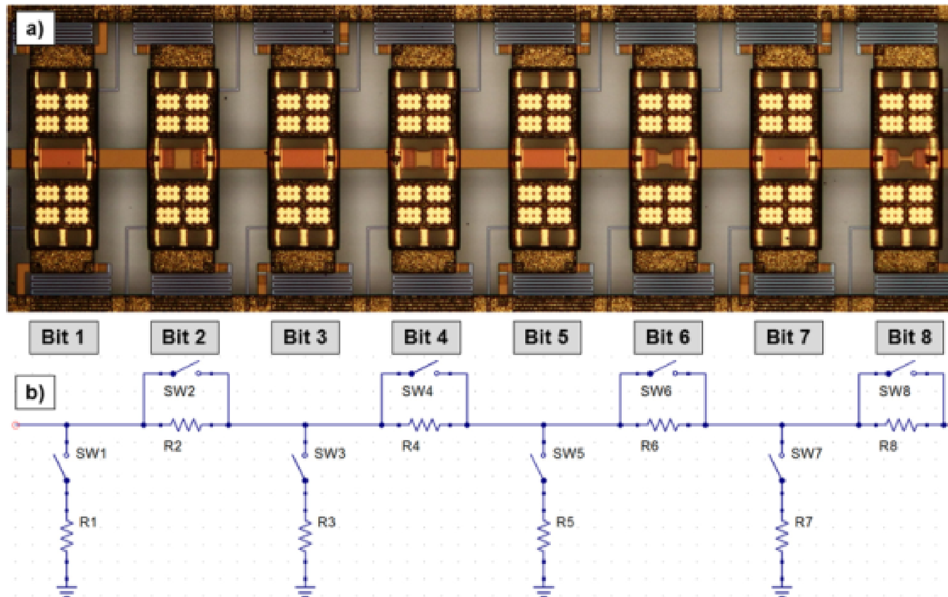


Figure 2.21: (a) Reconfigurable RF-MEMS attenuator showing the eight cascaded switching units; (b) Equivalent lumped element network of each stage of 8-bit attenuator, including the switches (SW1 to SW8) and the resistive loads (R1 to R8). [29]

in Fig. 2.21(b).

This device exhibits attenuation levels distributed in the range from 10 dB down to

60 dB, in the whole analysed frequency range i.e., from 10 MHz to 110 GHz. The flatness ranges from 3 dB to 5 dB at the low frequencies to around 15 dB over a 50 GHz span, but above 50 GHz the S_{21} traces show several ripples and markedly non-linear behavior.

Since all the above-mentioned approaches of MEMS based variable attenuators involve a CPW line and vertically moving thin membranes, they are still prone to the conventional MEMS reliability problems like stiction, micro-welding, and need high actuation voltages.

Chapter 3

Realization of High Aspect Ratio MEMS Actuators

3.1 MEMS Actuators

Over the last two decades, different microelectromechanical systems (MEMS) actuators such as magnetic [30, 31], electrostatic [32–34], piezoelectric [35, 36] and electrothermal actuators [37, 38] have been well documented. However, the most popular ones are electrostatic and electrothermal because of the larger displacements and forces generated by them. Microactuators with different driving mechanisms can be classified and studied based on the following categories:

3.1.1 Direction of Motion

Electrothermal actuation is a widely used driving mechanism and MEMS electrothermal actuators can be categorized into in-plane and out-of-plane based on their direction of motion. Most of the multi-morph designs provide out-of-plane motion since they rely on bending of the layer due to thermal mismatch as shown in Fig. 3.1 [39]. For in-plane

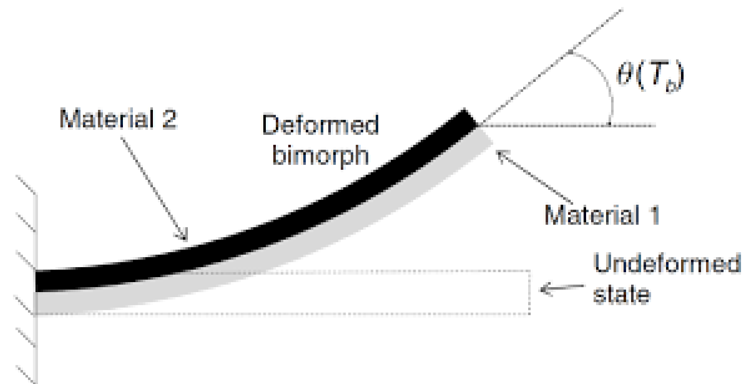


Figure 3.1: Bi-morph thermal actuator design for out-of-plane [40].

motion, uniform structural material with different widths of sections is utilized as shown in Fig. 3.2 [37, 38].

Since electrostatic actuators rely on the forces generated between two conducting electrodes when a voltage is applied, the most popular designs of electrostatic microactuators are parallel plate and comb drive structures. Parallel plate electrostatic actuators are usually used for out-of-plane motion [32, 33] and the comb-drive designs are popular for lateral (in-plane) motion (Fig. 3.3) [34].

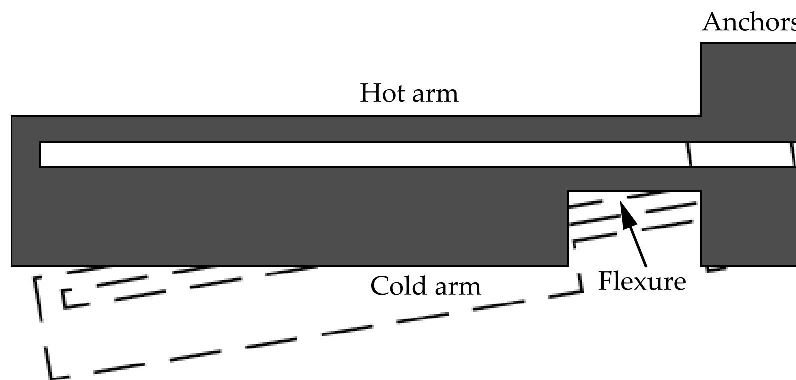


Figure 3.2: Thermal actuator design for in-plane motion.

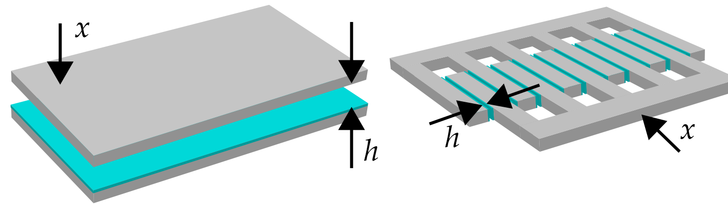


Figure 3.3: Electrostatic actuator configurations, (a) parallel plate actuator, (b) comb drive actuator. X denotes the direction of motion and h gives the capacitive gap between plates.

3.1.2 Operating Voltage/Power

Electrostatic actuators consume essentially zero dc power, but they require high operating voltages (usually >30 V), which makes them incompatible with microelectronic power supplies and integrated circuits. The reasons for this incompatibility are the dielectric oxide and junction breakdown at high voltages and the increased chip area required for larger depletion widths associated with elevated voltages. Moreover, such high electric fields on the surface of device increases the risk of arcing and make the device sensitive to ambient pressure and humidity, which is highly undesirable.

On the other hand, peak displacements of 1 μm to 15 μm can be achieved in the case of electrothermal actuators by using drive voltage of <15 V, enabling the use of electronic interfaces. The power consumed can be further reduced by implementing a locking mechanism as shown in Fig. 3.4 [41–43]. They provide the advantage of holding the mechanical position of the structure with no further electrical energy supplied unless a change in operation state is needed.

3.1.3 Materials

The transduction mechanisms utilized in the actuators include the use of magnetic materials, shape memory alloys, piezoelectric materials, or encapsulated fluids, but the use of such materials is prevented due to process constraints and difficulty in integration

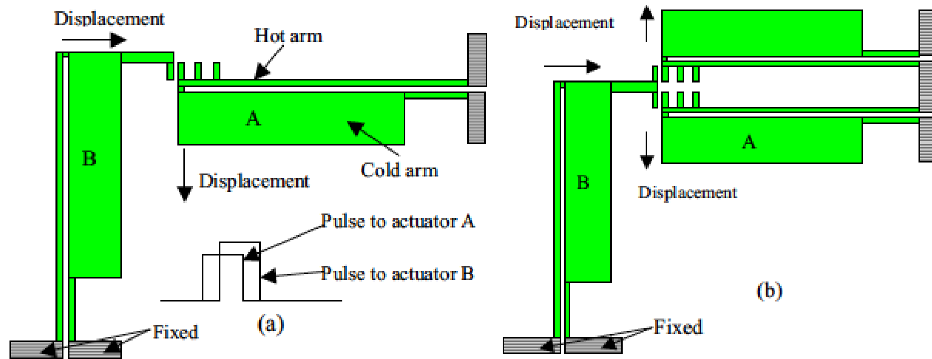


Figure 3.4: Locking mechanisms in thermal actuators [43].

with RF devices. Therefore, electrostatic or electrothermal transduction techniques are considered the best options for RF applications.

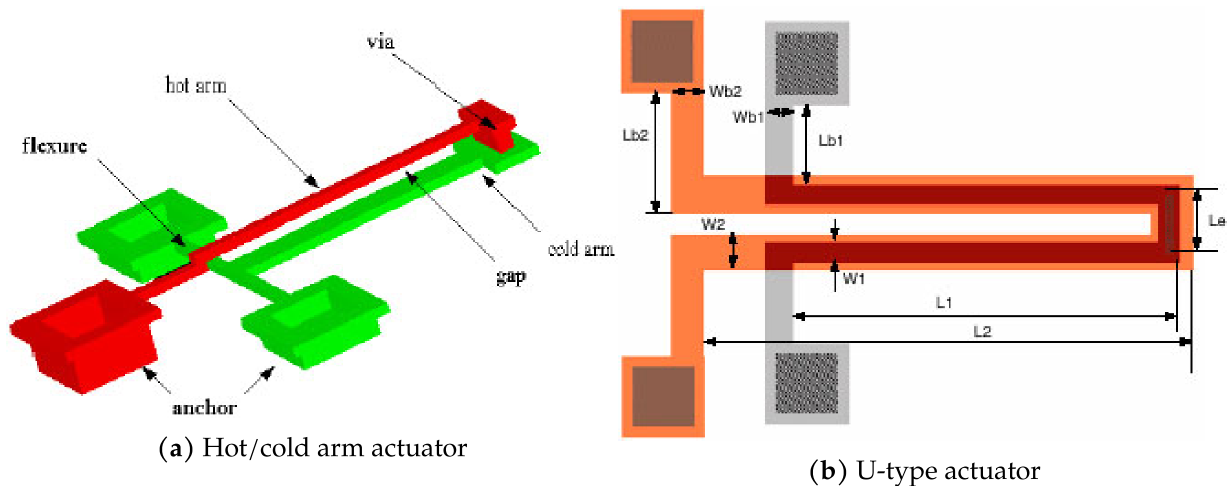
Undoubtedly, electrostatic actuators offer several advantages such as low temperature coefficient and zero dc power consumption, but they require high actuation voltages as discussed previously. Depending upon the choice of expansion materials, a wide range of displacements and forces can be achieved by using thermal expansion actuators. Electrothermal actuators can be designed with multi-morph or single-layer structures, where the latter design is more popular since they are more reliable and can provide rectilinear motion compared to the bending motion in the multi-morph designs. The most commonly used structural materials for electrothermal actuators are polysilicon, electroplated Ni, and silicon. Metal-based thermal actuators provide larger displacement at a much lower temperature than that of Si-based actuators [44, 45]. This is because the metals have higher thermal expansion coefficients than Si.

3.2 Electrothermal Actuators

Significant displacements and large forces can be generated by electrothermal actuators, which make them attractive for many space and radio frequency (RF) systems, especially in the tunable capacitors. Electrothermal actuation is generally based on heating two ad-

jacent materials with different expansion coefficients and creating a bending moment. This bimorph deflection is usually out-of-plane and is not rectilinear [39]. Another option is laying the bimorph materials side-by-side to achieve in-plane displacement, but this generally complicates the fabrication process and does not generate significant rectilinear displacement [46].

A popular technique to evade the use of dissimilar materials is the use of pseudo bimorph structures. This approach uses a single structural material with a uniform thermal expansion coefficient, but different parts experience different temperature changes because of the difference in width of arms of structure [37, 38]. The hot and cold arms structure can be used to achieve lateral or perpendicular motion to the substrate. In the thermal actuator shown in Fig. 3.5a, the hot arm is above the cold arm and is separated by an air gap [47]. The hot arm is thinner than the cold arm and are connected together with a via on one end. When the current is passes through the arms, the hot arm expands, and it drives the tip of the vertical actuator downward. However, the major limitation of this design is the power dissipated in the cold arm since it has no contribution towards the final motion of the actuator.



(a) Hot/cold arm actuator

(b) U-type actuator

Figure 3.5: Two-arm electrothermal actuators [47] [48]

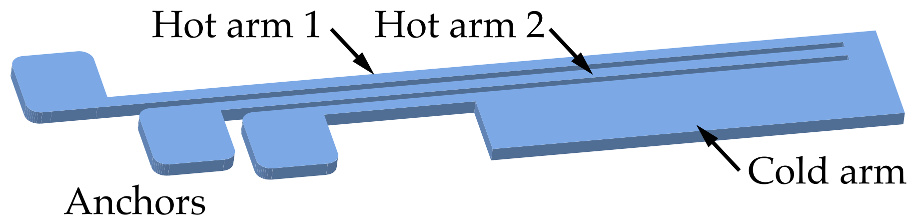


Figure 3.6: Three-arm electrothermal actuator

More electrically efficient designs are shown in Fig. 3.5b and in Fig. 3.6 where all electrical energy consumed contributes to the final deflection of actuator and no power is wasted in the cold arm. Electrothermal actuator shown in Fig. 3.5b uses two U-shaped beams in the top and bottom layer with a gap between them. The two beams are connected with a via at one end and are anchored separately on the substrate at the other end [48]. The actuator can bend upward or downward depending on which pair of anchors has been applied the voltage.

The two hot arm actuator design shown in Fig. 3.6 operates on the same principle as one hot arm actuator but in this case, the electrical current passes only through the outer and inner hot arms making it electrically more efficient than one-hot arm design.

The most popular structural materials for pseudo bimorphs are polysilicon and electroplated metals, however, the use of shape memory alloys has always been debated as they can provide significant linear displacement and forces, but it is challenging for process integration [49]. The thermal expansion coefficient of electroplated Ni is about four times that of Si. Although, this is highly desirable since it means larger displacement, but it also has some down sides. Since there is an expansion mismatch between the structural material Ni and the substrate material Si, the position of the apex may change with the ambient temperature. Moreover, there is a huge difference between the heat tolerance of these materials. While polysilicon structures can operate up to about 600 °C without any permanent deformation of the structures and Si structures can tolerate even higher temperatures [50], Ni structures have a maximum limit of 350 °C. Above this tempera-

ture, an irreversible darkening of the structures can be observed due to oxidation and it causes degradation of the actuation stroke.

To summarize, electrothermal actuators have the advantage of providing higher forces with low driving voltages, which allows the use of standard electronics interface, but they consume more power than electrostatic ones. The thermal time constant of these actuators is larger than the electrical and mechanical time constants of microstructures, making them slower than electrostatic actuators.

There are three important considerations in designing the thermal actuators:

- Thermal expansion of materials upon heating
- Mechanically amplifying the motion achieved by thermal expansion
- Deciding the direction of in-plane motion

It is well known that most materials undergo an increase in size when heated and decrease in size with decreasing temperature. The basic relation between structural elongation and thermal expansion coefficient α is given by:

$$\Delta L = \alpha L_0 \Delta T \tag{3.1}$$

where, L_0 is the initial length of object, ΔL is the change in the length, α is the coefficient of linear expansion in K^{-1} and ΔT is the change in temperature in K.

When voltage is applied to the electrical pads, current in the range of milliamps passes through the thin beams. This causes resistive heating and a temperature rise of several hundred degrees. The areas with maximum resistive heating undergo maximum expansion.

The amount of elongation possible from thermal expansion is limited by the linear thermal expansion coefficient and the melting point of the material. This thermal expansion achieved is small when compared to the overall dimensions of the device and

is not sufficient for effective actuation. Hence for larger deflections, it is necessary to amplify this motion by using geometrically constrained design. One of the techniques is to use dissimilarly shaped beams in parallel also called as bi-morphs. Another option is to use two beams bent at a slight angle to each other called as Chevron or V-shaped actuators as shown in Fig. 3.7. This can mechanically amplify the slight motion achieved from thermal expansion [51].

Various deflection modes are possible in thermal microactuators based on the geometry. In this case, the thickness of the structures is defined by the device layer thickness of the SOI wafers which is selected to be 20 μm. The width of all the thin beams is designed to be less than thickness to ensure that they deflect in-plane. To control the direction of in-plane motion, the thin beams are fabricated at a small angle with the central beam.

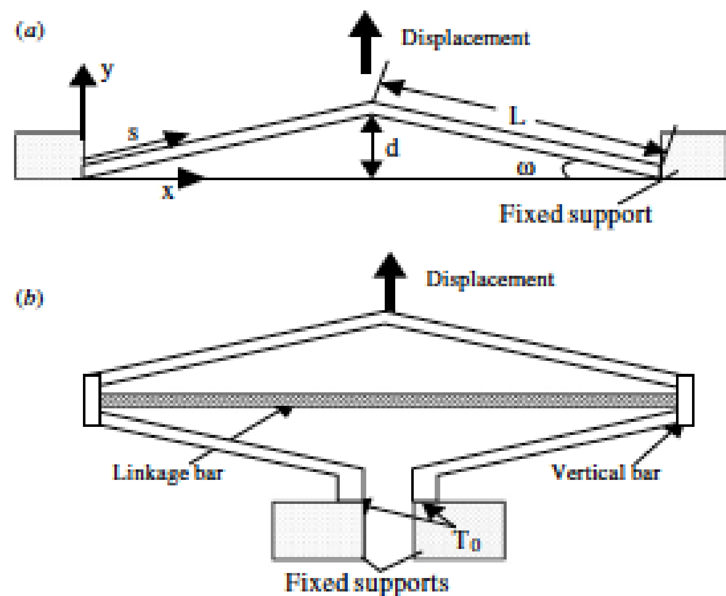


Figure 3.7: Geometrical constraints used to amplify the expansion motion (a) V-shaped beams (b) one-ring spring actuator with insulating beam as a constraint [51].

3.3 Design of Chevron Actuator

The traditional electro-thermal actuators are fabricated with different widths of hot and cold arms to provide high and low electrical resistance. Hence, when electrical current is applied to these arms, different magnitudes of thermal expansions are observed in hot and cold arms. This forces the tip of the device to bend.

By leveraging the deformations caused by localized thermal stresses, in-plane displacements and contact forces are generated in electrothermal microactuators. In Chevron actuators, an array of V-shaped beams is anchored at both ends [52]. When an electric current is passed through them, the apex is pushed forward due to a combination of thermal expansion in all the V-shaped beams caused by joule heating as shown in Fig. 3.8.

Chevron actuators produce more force compared to hot/cold arm actuators. Moreover, the net force produced can be increased by using multiple pairs of hot arms in parallel. Since, there is no cold arm to reduce the net expansion, Chevron actuators are more efficient that hot/cold arm actuators.

The basic Chevron type thermal actuator design has two electrical pads anchored to the substrate, a movable shuttle, and an array of thin beams. Due to the symmetry of the structure, when current passes through thin arms, the thermal expansion causes the

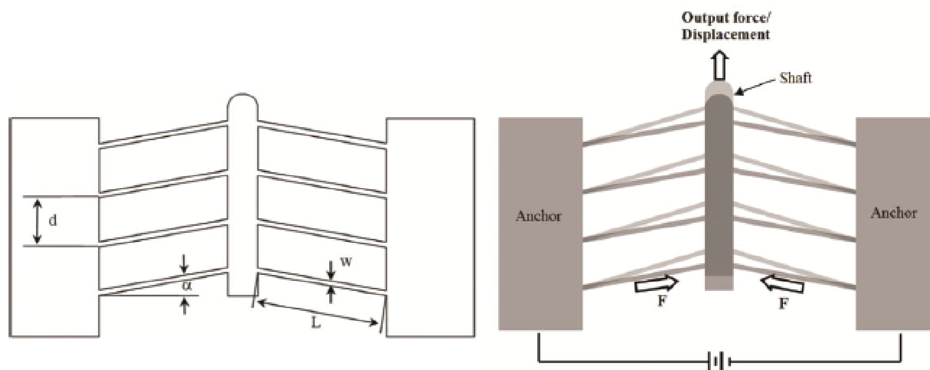


Figure 3.8: (a) Chevron actuator design (b) lateral displacement observed on application of voltage [52].

shuttle to undergo linear deflection.

The dimensions of the beams and their initial slope decide the final displacement of the apex. Hence, the performance of the actuator can be optimized by changing the geometry of the beam. An increased peak displacement can be achieved by using longer beams and reduced bending angle. However, shorter beams with larger bending angle generate higher peak force. Also, the output force is directly related to the thickness and width of the beams.

Linear displacements ranging from 1 μm to 15 μm can be achieved by Chevron actuator and the typical drive voltages required are $\leq$15 V. This allows the use of standard electronic interfaces which are inadequate for electrostatic actuators due to the higher levels of voltage required.

Chevron actuators do not require structural segments with different thermal expansion coefficients but can be fabricated with any material that is mechanically strong to serve as an actuator and is electrically conductive. We have selected Si as the structural material because the peak operating temperature of the Si structures is higher than Ni and there is no thermal mismatch between the structural material and the substrate, which provides the advantage of high reliability.

The Chevron actuator designed here consists of four thin hot arms on each side of a central beam forming a small angle θ with the central beam. This is done by slightly offsetting one end of each hot arm that is attached to the central beam by a few microns in the desired direction of lateral motion.

Here we present the design and performance of a horizontal electrothermal Chevron actuator fabricated by a single layer SOI MEMS process described in the following sections.

3.4 Simulated Results

3D model of the sole Chevron actuator is built in COMSOL Multiphysics [53] with a coupled physics model which consists of thermal expansion, structural mechanics and electric currents. The Young's modulus and thermal expansion coefficient of the structural material is selected precisely for accurate predictions. The tip displacement and heat distribution when the voltage is applied to the Chevron pads are predicted using finite element modelling (FEM) simulations, which helped in optimizing the dimensions of the actuator. It was found using simulations that structures with longer legs are capable of larger deflections since they undergo greater expansion for the same temperature difference. The advantage of the Chevron design is that the amount of deflection can be tailored to the application. Since our application demands 10 μm displacement, the dimensions of Chevron actuator were adjusted accordingly. FEM simulation of Chevron actuator for lateral displacement with the application of 9 V is shown in Fig. 3.9. Heat distribution throughout the structure is shown in Fig. 3.10 with the maximum heat generated in the array of bent beams on both sides of the central beam, hence undergoing maximum thermal expansion and pushing the central bem forward. Total displacement of the Chevron actuator with respect to linear sweep of dc voltage is shown in Fig. 3.11.

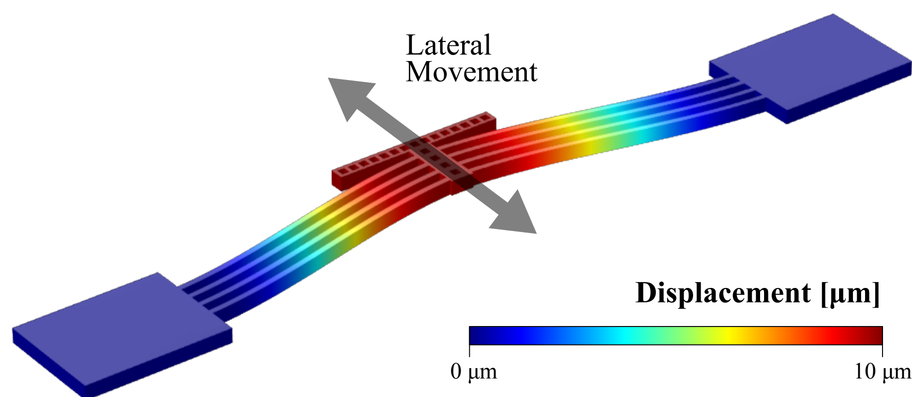


Figure 3.9: FEM simulation of Chevron actuator showing lateral displacement with the application of voltage.

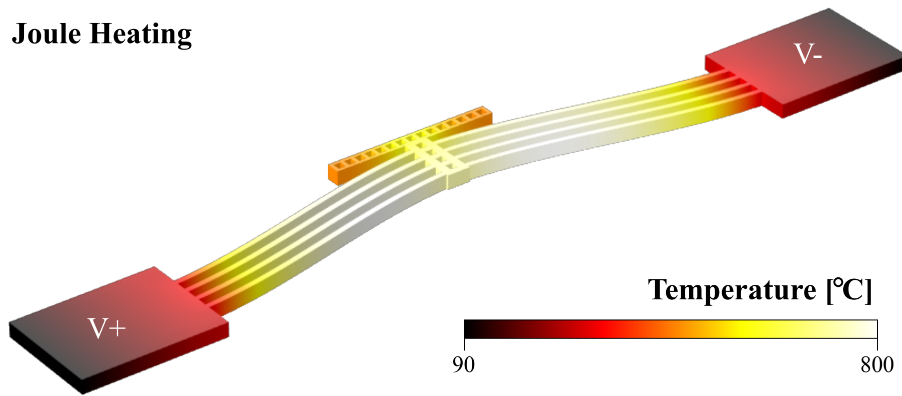


Figure 3.10: FEM simulation of heat distribution across the Chevron actuator with applied potential difference across the pads.

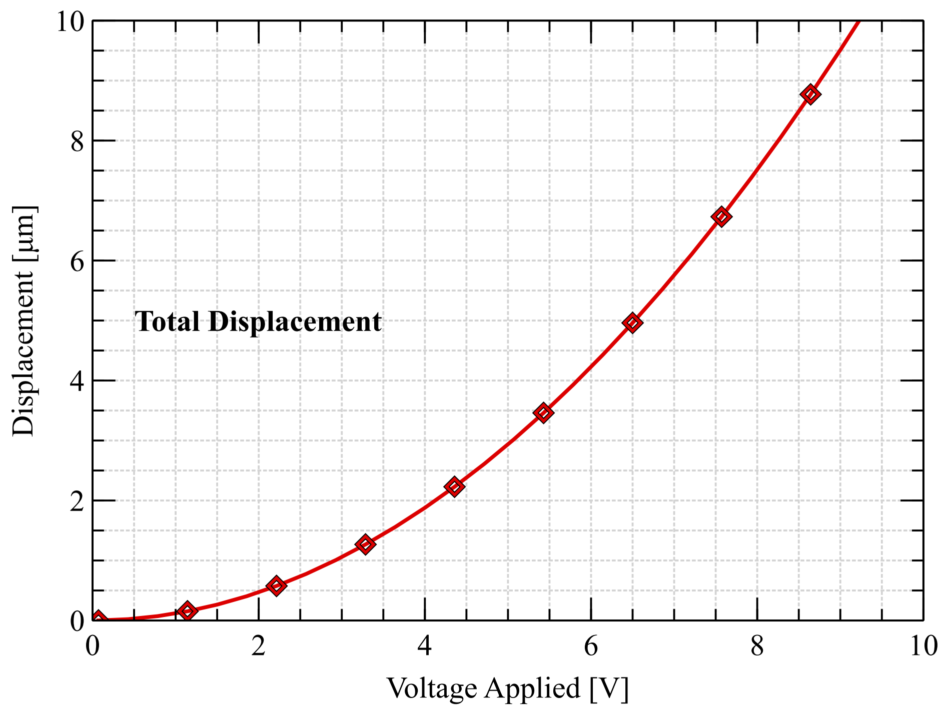


Figure 3.11: Simulated results for total displacement of the Chevron actuator versus linear sweep of dc voltage.

3.5 Fabrication Process

Many thermally actuated lateral RF MEMS switches with latching mechanism have been reported in literature [44, 45] fabricated using MetalMUMPS process [54] from MEMSCAP Inc. The process consists of two conducting structural layers of nickel and polysilicon, and two dielectric layers of silicon nitride on high resistive silicon substrate and provides the capability of having trench in the silicon substrate underneath. Hence, this Nickel micromachining process requires multiple fabrication steps and is overall complicated. So, we developed a custom fabrication process that is relatively simple and cost effective as it utilizes single lithography step to co-fabricate the Chevron actuator, RF CPW lines, bias pads and other supporting structures.

The 3″ SOI wafer as shown in Fig. 3.12 has the specifications: Device layer thickness: 20 μm; Device layer resistivity: $<0.003\,\Omega\cdot\text{cm}$; Handle layer thickness: 510 μm; Handle layer resistivity: $>10\,000\,\Omega\cdot\text{cm}$; Buried oxide layer thickness: 1 μm.

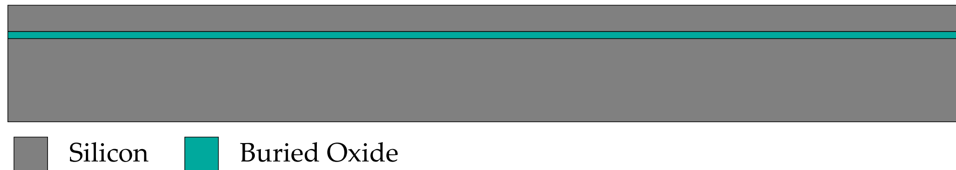


Figure 3.12: RCA cleaned bare SOI wafer showing the device layer, buried oxide and handle layer.

Metal Deposition

A 50 nm thick seed layer of chrome is deposited for proper adhesion of gold layer. This is achieved using E-beam deposition as shown in Fig. 3.13.

Then a 250 nm thick layer of gold is deposited using E-beam deposition, which is followed by another 30 nm thick layer of chrome forming a sandwich of metal layers as shown in Fig. 3.14. The top chrome layer acts as a protective layer for gold, since gold being a noble metal is not permitted as the top layer in RIE.

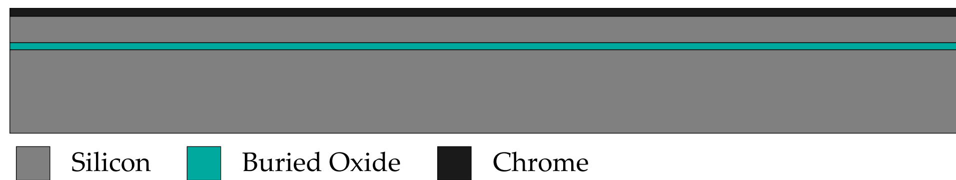


Figure 3.13: A 50 nm thick chrome seed layer on SOI wafer.

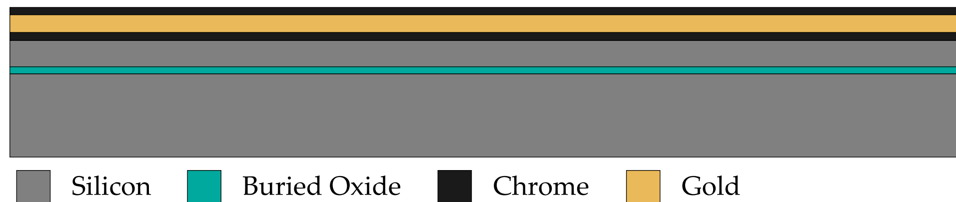


Figure 3.14: A 250nm thick gold layer, followed by another 30 nm chrome metal layer forming a stack of metal layers.

Patterning

The SOI wafers are spin-coated with UV-sensitive photoresist on the device layer as shown in Fig. 3.15

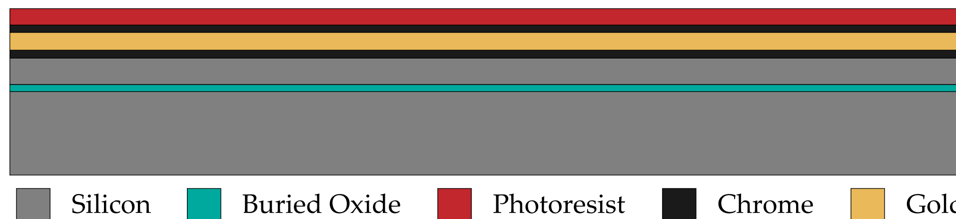


Figure 3.15: An even layer of photoresist spin-coated on the top of metal layer.

The photoresist layer is lithographically patterned by exposing to UV light using the GDSII layout file in Maskless aligner, and then developing it. This leaves us with a photoresist pattern as shown in Fig. 3.16.

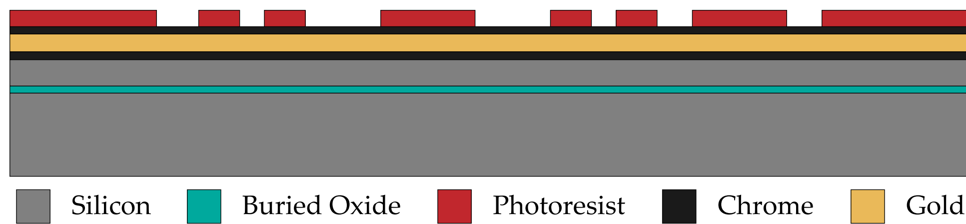


Figure 3.16: Patterns of photoresist formed on the top of metal layers after photolithography.

Metal Etching

Patterned photoresist acts as a mask for etching the stacked metal layers using ion milling as shown in Fig. 3.17. Ion milling should be done for smaller intervals of time successively since continuous bombardment of the substrate by ions for a longer period burns the photoresist layer and makes it hard to remove in the successive step. It is very important that the incident beam angle should be 90° with respect to substrate to obtain vertical edges of the etched structures. This step is followed by dicing the wafer into smaller chips. Dicing is done before the Si DRIE of device layer to avoid any damage to the thin structures with high aspect ratio due to vibrations generated during high speed cutting.

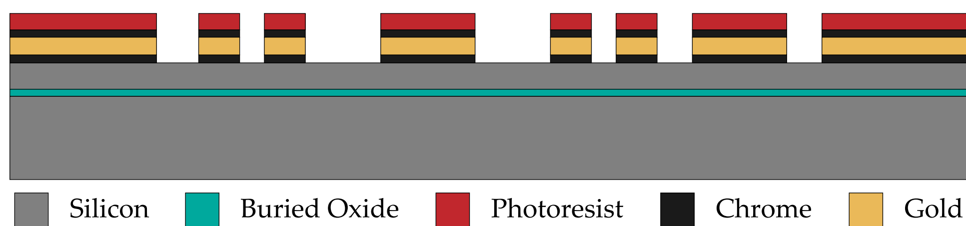


Figure 3.17: Etched metal layers after ion milling.

Photoresist Stripping

After the ion milling, the photoresist is partially removed by wet chemical stripping, which is followed by Plasma ashing to get rid of any remains of the photoresist as shown

in Fig. 3.18.

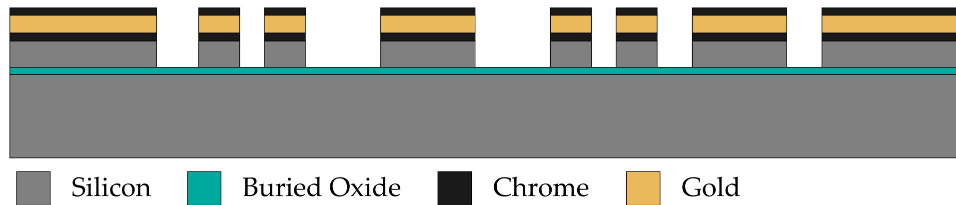


Figure 3.18: Exposed metal layers after removing the photoresist mask.

Si Deep Reactive Ion Etching

The patterned metal layers obtained in the previous step act as a hard mask for Si-DRIE. It is always preferable to use metal mask when the etching depth is large (which in this case is 20 μm), due to selectivity. Moreover, it is very tedious to get rid of the hardened photoresist after DRIE as shown in Fig. 3.19.

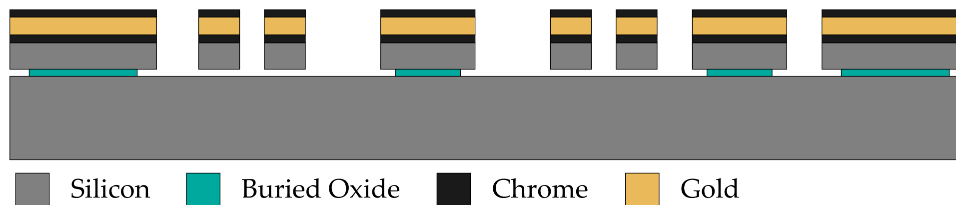


Figure 3.19: The high aspect ratio structures obtained after Si etching of the device layer.

Wet Etching of Oxide

After the deep etching of the device layer, the underlying oxide is exposed. This buried oxide needs to be removed from selected areas releasing the movable structures and leaving the anchors intact as shown in Fig. 3.20. Wet etching of oxide is obtained using Buffered Hydrofluoric acid (BHF) since it provides more control over the etching rate. The oxide layer in open areas and under the thin structures is removed completely. Slight

under-etch is observed in the oxide layer covered by larger structures while keeping them fixed to the substrate. This is followed by rinsing the chips three times in DI water. After this step, the chips are dipped in Isopropyl alcohol (IPA) to get rid of any surface tension on structures due to water. They are then transferred to the Critical Point dryer (CPD) to avoid any stiction of the released MEMS structures. Top chrome layer is removed by using chrome wet etchant.

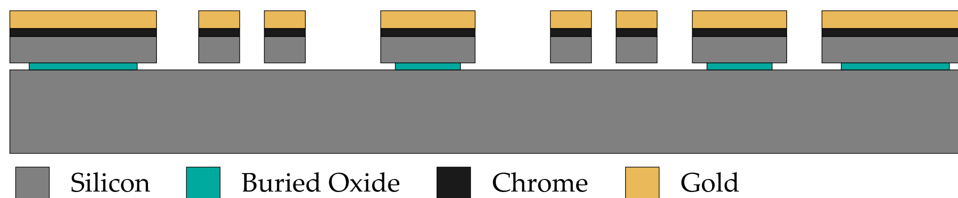


Figure 3.20: The released structures after controlled wet etching of oxide layer. Undercut can be observed under the anchor areas.

Wire Bonding and SMD Resistors Mounting

The cross-bonds on the top metal layer of structures are formed by using wire bonding in the desired areas as shown in Fig. 3.21. Surface mount resistors are then carefully bonded using silver epoxy adhesive.

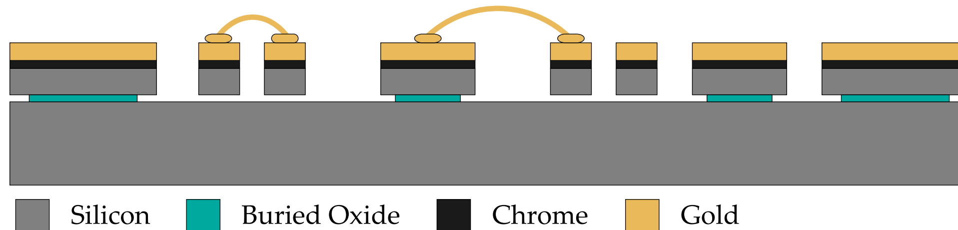


Figure 3.21: Wire-bonding on the gold layer of structures.

3.6 Deep Reactive Ion Etching (DRIE)

Cyclic Deep Reactive Ion Etching (c-DRIE) is an advanced RIE process and was originally developed in early 1990's by F. Laermer and A. Schilp, who were then employees of Robert Bosch GmbH. In 1996, the process was patented by the company [55] and became famous under the name 'Bosch-Process'. The process is mainly used to generate high aspect-ratio structures up to hundreds of microns in height to form MEMS sensor structures, electrostatic microactuators or holes for the so-called Through-Silicon-Vias (TSV) technology. This is a dry etching plasma process that anisotropically etches Si without dependence on the crystal orientation of Si. It offers better performance than RIE on all fronts: reduced damage by high energy ions, high aspect ratios (>100), high etch rates (>20 µm/ min), large etching depths (>500 µm), anisotropy, selectivity and process control.

The Bosch process consists of the cyclic isotropic etching and fluorocarbon-based protection film deposition by quick gas switching. The sulfur hexafluoride (SF_6) plasma cycle etches silicon, and the octafluorocyclobutane (C_4F_8) plasma cycle creates Teflon like protection layer. In both steps, Argon (Ar) can be added to dilute the reactive gases. Fig. 3.22 gives a schematic of the process sequence. During the first process step, a mask is created on the top surface of the substrate to be etched (Fig. 3.22a). A thin passivating film is isotropically deposited on the substrate, uniformly covering the structures (Fig. 3.22c). The subsequent etching is a combination of two steps (Fig. 3.22d). In the first step, directional sputtering of high energy ions leads to an anisotropic removal of the passivating film from the bottom horizontal surface of the trench and the second step involves etching the exposed surface by SF_6. This cyclic process is repeated depending on the depth of etch needed. The process consists of the steps described in Fig. 3.22 and their periodic cycling leads to the appearance of characteristic scallops on the sidewalls. A SEM image depicting these scallops on the sidewalls is shown in Fig. 3.23b. Slow-speed switching between the passivation and etching gases can result in large scallops and rough sidewalls, which might be problematic in some applications

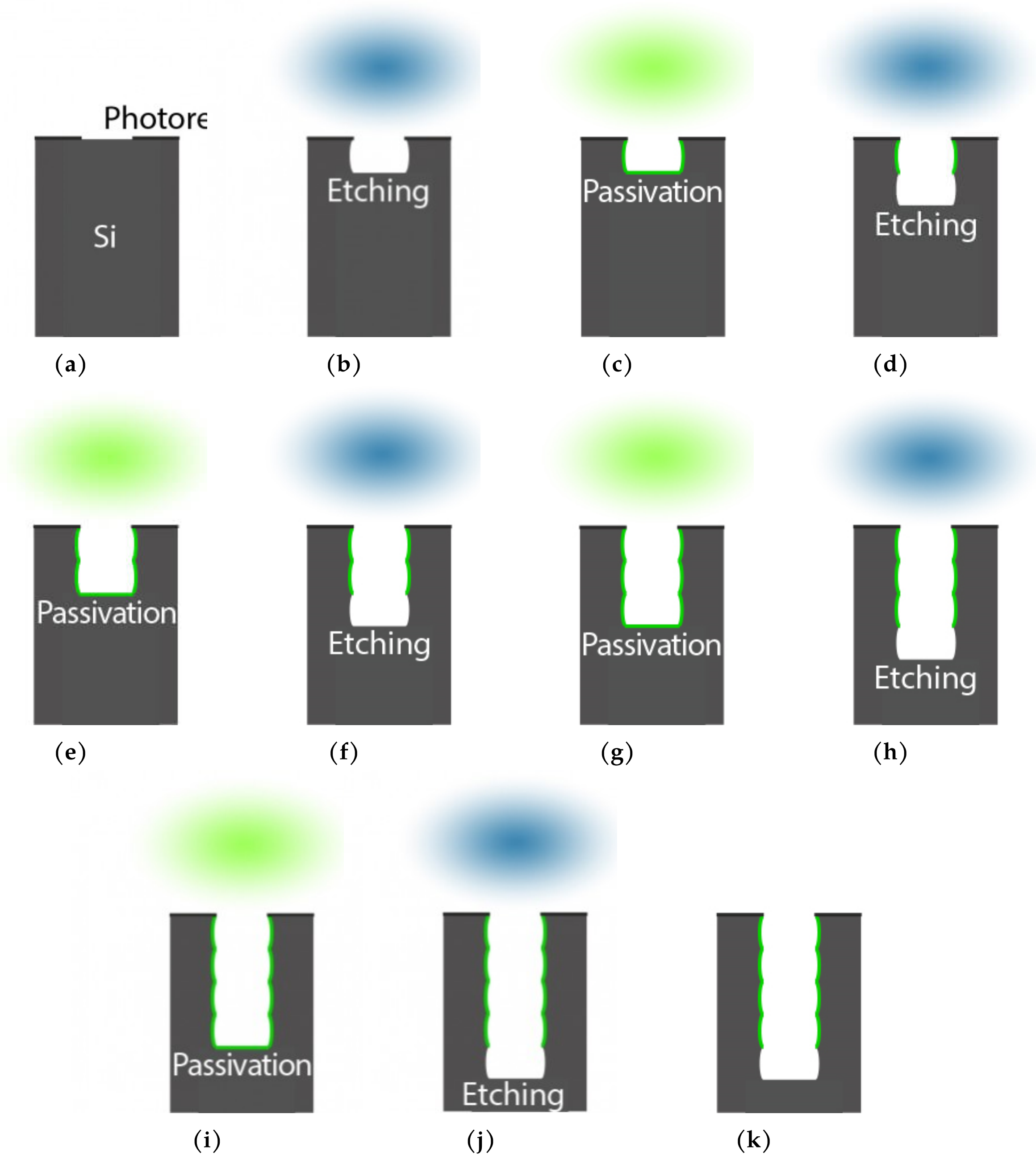
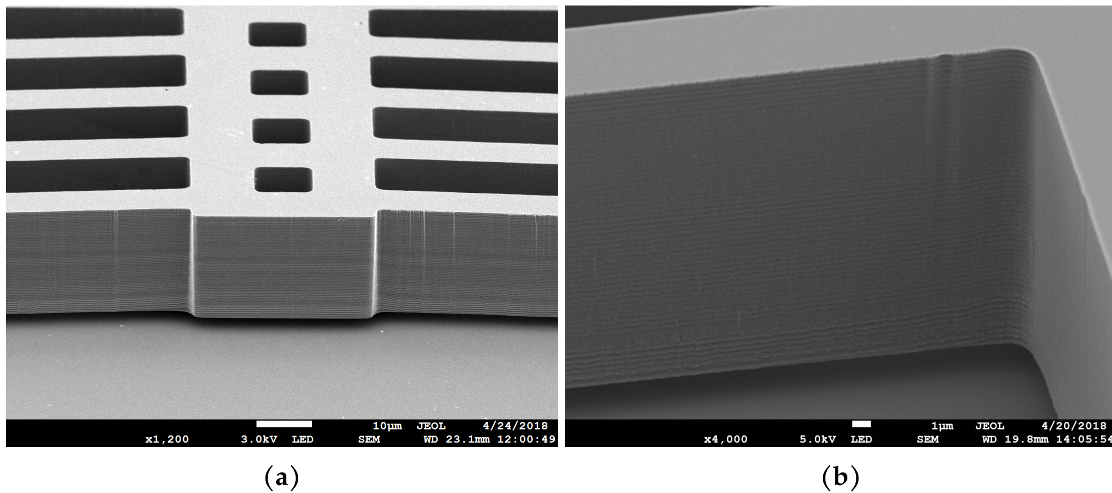


Figure 3.22: BOSCH Si DRIE process alternates between etching and passivation steps [56].

such as Through Silicon Vias (TSV) where delamination of copper film might occur due to sidewall roughness. Smooth sidewalls can be achieved by adequate process control [57]. The SF_6 plasma cycle and C_4F_8 plasma cycle need to be optimized to achieve deep silicon etching with high aspect ratio. The protection film deposited during C_4F_8 plasma cycle needs to be thick enough to withstand the SF_6 plasma cycle for highly anisotropic silicon etching.

There are several process parameters that can be optimized for particular applications to get the desired etch rate, anisotropy, sidewall angle, mask selectivity, substrate selectivity and etched surface quality. Hence, the Bosch process is unique for each structure in terms of the balance between the duration polymer deposition and duration of SF_6 etch. The following process parameters should be optimized during both the passivation cycle and etch cycle: Chamber pressure, Duration of cycle, Gas flow rate, Bias voltage and Gas composition.

The anisotropy of the etch is primarily controlled by the chamber pressure, which controls the amount of gas in the chamber for ionization. Increase in chamber pressure results in decrease in anisotropy. Etch duration needs to be optimized in such a way that it is long enough to remove the polymer at the bottom of the trench and reach desired etch depth, but not too long to start etching sidewall passivation leading to undercut in the structures. On the other hand, the duration of the passivation step controls how long the structure is exposed to the passivation gas. Longer duration of passivation step means thicker layer of polymer to protect the sidewalls. An increase in RF power during the etching step increases the density and energy of the free electrons in the plasma. However, RF power during passivation step affects the amount of polymer deposition. The potential between the plasma and the negatively charged electrode termed as "bias voltage" determines the directionality of the impeding ions. A high bias voltage directs the ions in a straighter line towards the electrode. Sharp vertical structures were achieved using Si DRIE as shown in Fig. 3.23a. Fig. 3.23b shows the scalloped sidewalls of the structures due to cyclic etching Bosch process.



(a) (b)

Figure 3.23: (a) High aspect ratio structures achieved using Si Deep Reactive Ion Etching; (b) Scalloped walls of the microstructures due to cycles of Bosch etch.

3.6.1 Mask Selection for DRIE

The mask for Si-DRIE is selected based on its accuracy to transfer patterns into silicon over the entire etching period. It is very important to determine which material to use as the mask since it interacts with the etching process parameters. Commonly used silicon etch masks are resist, oxides, and metal masks.

We tried using positive photoresist `S1811` as mask. Resist masks offer the simplicity of a single processing step and excellent selectivity. The patterns were sharp with vertical walls as shown in Fig. 3.24a and Fig. 3.24b, but the main drawback is that plasma etching makes the resist really hard and it is tedious and a prolonged process to remove the resist later. Moreover, for some applications in which a metal layer is required on the top of high aspect ratio Si structures, this method is not effective. On the other hand, some metals when used as mask undergo erosion at the edges of patterns during etching which can lead to undesirable slope and features on the sidewalls of the etched structures

as shown in Fig. 3.24c in comparison to the smooth sidewalls achieved using photoresist mask (Fig. 3.24a). This phenomenon is termed as mask induced roughness. Aluminium works perfectly as the metal mask with minimum erosion but the following fabrication step of removing the silicon dioxide layer with Hydrofluoric acid (HF) attacks the alu-

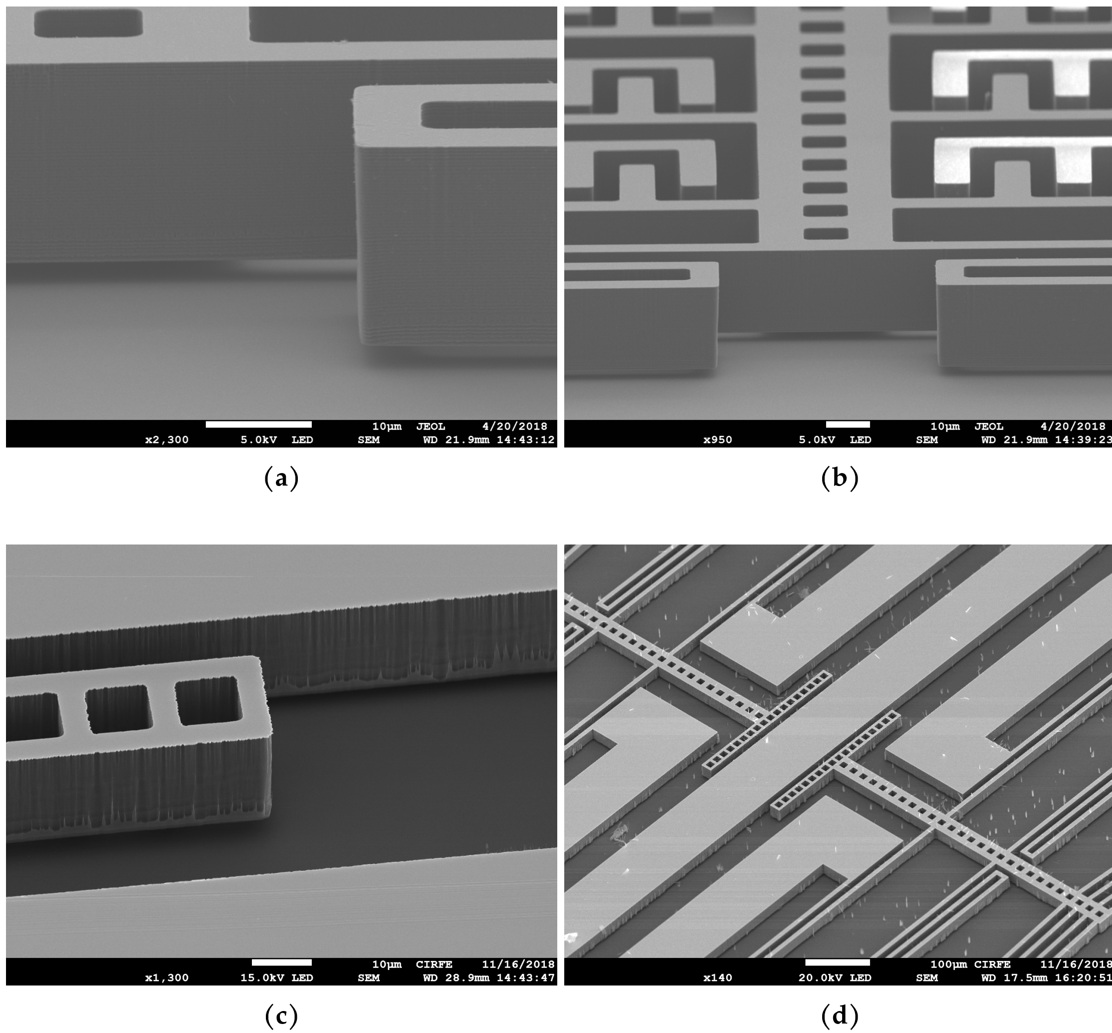


Figure 3.24: (a) Smooth sidewalls after Bosch etch; (b) Microstructures etched by Si-DRIE using photoresist mask; (c) Microstructures etched by Si-DRIE using hard mask; and (d) Micro-grass observed in the open areas of wafer due to micromasking.

minium layer and structures are left with barely any metal on the top layer after this step which leads to poor RF performance of the fabricated devices.

Another option is to use metals like gold, platinum, nickel which are not attacked by HF or chrome which is partially resistant to HF attack. Since gold and platinum are noble metals, they are forbidden in the ICP plasma Si-DRIE since the particles stay in the etching chamber forever. The exposure to gold mask can be avoided by using a thin protective layer of chrome on the top of gold. Another common problem is the sputtering of the metal mask due to high energy ions bombardment and this sputtered metal is redeposited in the unwanted areas on the surface and leads to micromasking and micrograss as shown in Fig. 3.24d.

Chapter 4

Thermal Analysis of Microactuator

4.1 Introduction

Over the last two decades, microelectromechanical systems (MEMS) based lateral thermal actuators, have aroused a considerable interest for a wide range of applications such as lateral latching RF switches. The major challenges involved in the design of such a structure are the requirements for high-thermal uniformity, low power consumption while realizing maximum displacement. It is thus of great interest to use methods that enable us to study the thermal behavior of such devices. Additionally, the study of temperature distribution and thermal characteristics of a device is very important for thermal management [58].

Several thermography techniques have been developed for temperature measurement of micrometer and sub-micrometer electronics and optoelectronic devices, such as, infrared (IR) thermometry, liquid crystal thermography (LCT), fluorescent microthermography (FMT), scanning thermal microscopy (SThM), acoustic thermography, and many others. The most popular among these is the infrared (IR) theromometry which uses infrared light with wavelengths of typically 3 μm to 5 μm. The spatial resolution achieved in this case is roughly 1.5 μm to 2.5 μm which is limited by diffraction

of light. The spatial resolution achieved with charged coupled device (CCD) based-thermoreflectance microscopy is at least one order of magnitude better than that obtained with conventional infrared thermography because visible optical wavelength is used in the illumination source. This can provide sub-micron spatial resolution between 250 nm to 400 nm [59, 60]. A better spatial resolution helps in achieving accurate measurements of peak temperatures [61].

Thermoreflectance imaging technique is well suited for thermal profiling and reliability analysis of MEMS devices and hence acts as a powerful tool to aid thermal and functional design of micro structures in comparison to the connectional techniques [62]. An extensive review of the principles of thermoreflectance microscopy and the various applications of the technique are reported in [63, 64]. The highly resolved and accurate 2D temperature field can be very helpful in identifying the areas which are getting excessively heated and can also help in diagnosing the performance of the device, if needed. Apart from the use of this technique in many advanced complex semiconductor devices and high-speed integrated circuits [65], its application in thermal analysis of high-power LEDs [66] and in identifying defects in photovoltaic solar cells has also been reported [67]. Theoretical and simulation-based studies have been carried out for designing various thermal MEMS devices [68], but to the best of our knowledge thermoreflectance based experimental analysis has not been studied for MEMS and this is the first report on the experimental thermal imaging of MEMS actuator that can be helpful in the analysis of reliability, hotspots, microdefects detection.

In this chapter, we present thermoreflectance imaging as a powerful, non-contact, non-destructive optical tool for thermal characterization of chevron actuators. Thermal imaging microscopy can provide accurate insights to heat distribution in the device and to conduct the failure analysis, which is extremely important in MEMS devices. Voltage applied to the chevron actuator under test leads to current flow due to Joule heating phenomenon, that results in modulation of the surface temperature and hence the reflectivity. The designed device is fabricated on SOI wafer and the performance predicted using finite element modeling is compared with experimental results.

4.2 Thermoreflectance Imaging

Thermoreflectance thermal imaging is an optical technique that measures the relative change in the surface reflectivity of the material with temperature. In this case, as the voltage is applied to the pads of the MEMS Chevron actuator, the current flow through the structure causes rise in surface temperature due to Joule heating effects. The surface displacement and thermomechanical stresses in Chevron structure can also be observed with the applied voltage. This change in temperature of the sample changes the refractive index, and hence reflectivity of the material's surface also changes, which is detected by the CCD camera. There exists a linear relationship between the change in reflectivity (R) and the change in temperature (T), given by:

$$\frac{\Delta R}{R} = \left(\frac{1}{R} \frac{\partial R}{\partial T} \Delta T = \kappa \Delta T \right) \tag{4.1}$$

where, κ is the Thermoreflectance coefficient.

Thus, if the relative change in reflectivity of the sample $(\Delta R/R)$ is known, and the accurate value of thermoreflectance coefficient (κ) is plugged-in, then the increase (or decrease) in the temperature of the sample (ΔT) can be discerned. Some of the main factors controlling the thermoreflectance coefficient are material temperature, illumination wavelength and material surface properties like roughness, porosity. The effect of each of these is described in [69]. The value of the thermoreflectance coefficient ranges from $10^{-2}\,\mathrm{K}^{-1}$ to $10^{-5}\,\mathrm{K}^{-1}$ for most metals and semiconductors.

This means to detect a temperature change of 1 °C in the sample, the reflectivity change of as small as 0.001 to 0.00001 should be detected by the CCD camera.

Table 4.1: Design specifications of MEMS Chevron actuator

Parameter	Value	Parameter	Value
l_{beam}	500 µm	l_{pad}	100 µm
w_{beam}	20 µm	w_{pad}	100 µm
a_{beam}	4°	g_{cont}	10 µm
l_{junc}	120 µm	t_{dev}	20 µm
w_{junc}	50 µm	g_{dev}	2 µm
l_{tip}	200 µm	l_{hole}	5 µm
w_{tip}	20 µm	w_{hole}	5 µm

4.3 Design and Fabrication of MEMS Chevron Actuator

Chevron actuator is fabricated on 20 µm thick device layer of silicon-on-insulator (SOI). The handle layer acts as a high-resistivity substrate, and the buried oxide layer is selectively removed to release only the movable parts of the actuator. Chevron electrothermal actuator is used because of its rectilinear displacement caused by resistive heating and the design simplicity and flexibility. It can be used in various applications as an actuator [70]. It is an array of four 400 µm × 8 µm silicon V-shaped beams (resistivity $<0.005\,\Omega \cdot$ cm, and a 4° pre-bent angle.

When voltage is applied to the anchors, the thermal expansion in the beams caused by ohmic heating, leads to motion of the central beam. The amount of motion of the central beam is determined by the pre-bent angle and the length of the beam. The voltage required for a 10 µm lateral motion of actuator is only 9 V. Top view and 3D view of Chevron actuator is shown in Fig. 4.1. Design specifications are given in Table. 4.1. SEM micrograph of Chevron actuator is shown in Fig. 4.2. The Chevron actuator is designed as a decoupled actuator that provides switching action to a subsequent flexure tied beam [70].

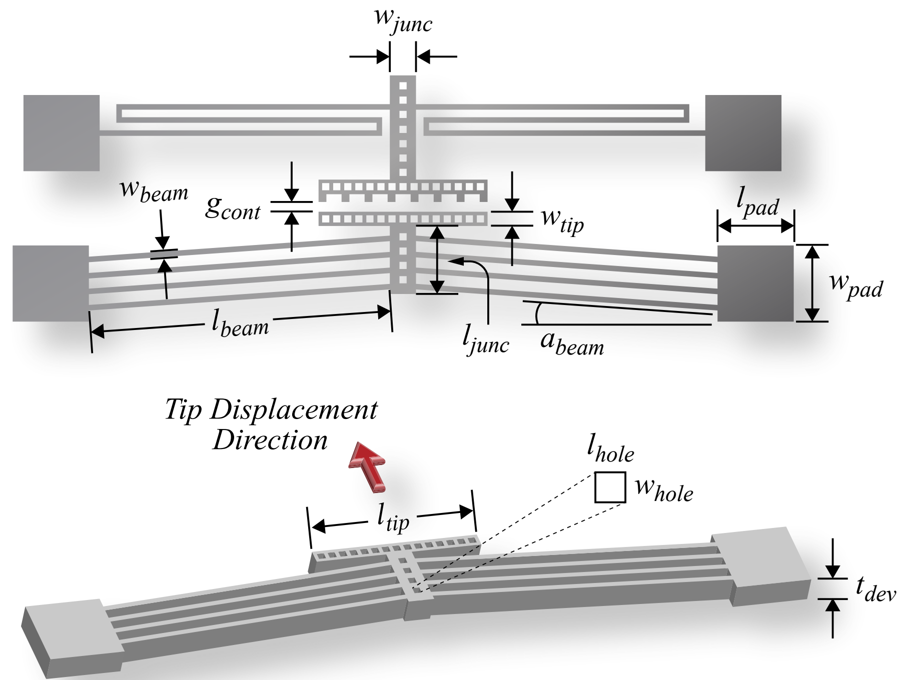
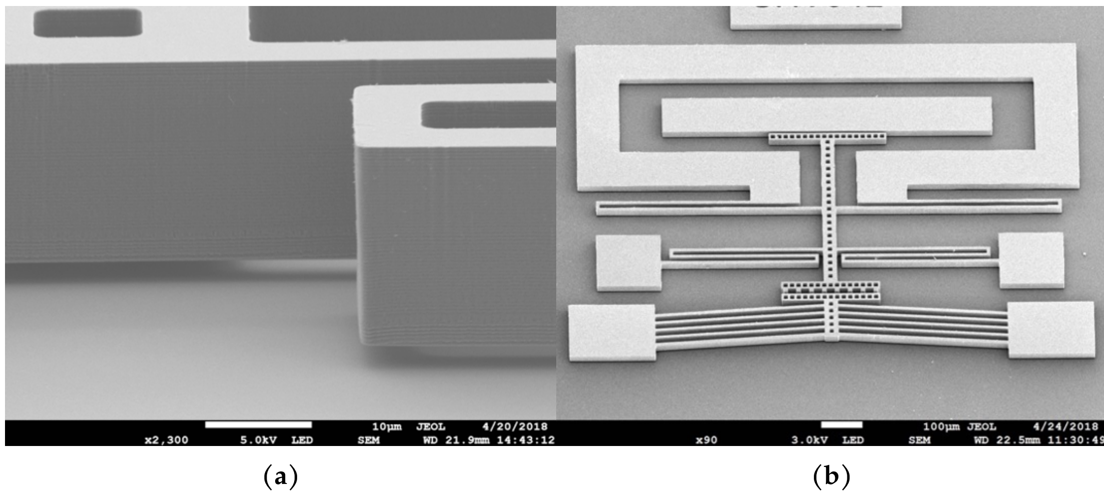


Figure 4.1: Design dimensions of Chevron actuator



(a) (b)

Figure 4.2: (a) SEM micrograph the device showing chevron actuator designed for displacement purpose. (b) SEM micrograph of the released free-standing structure.

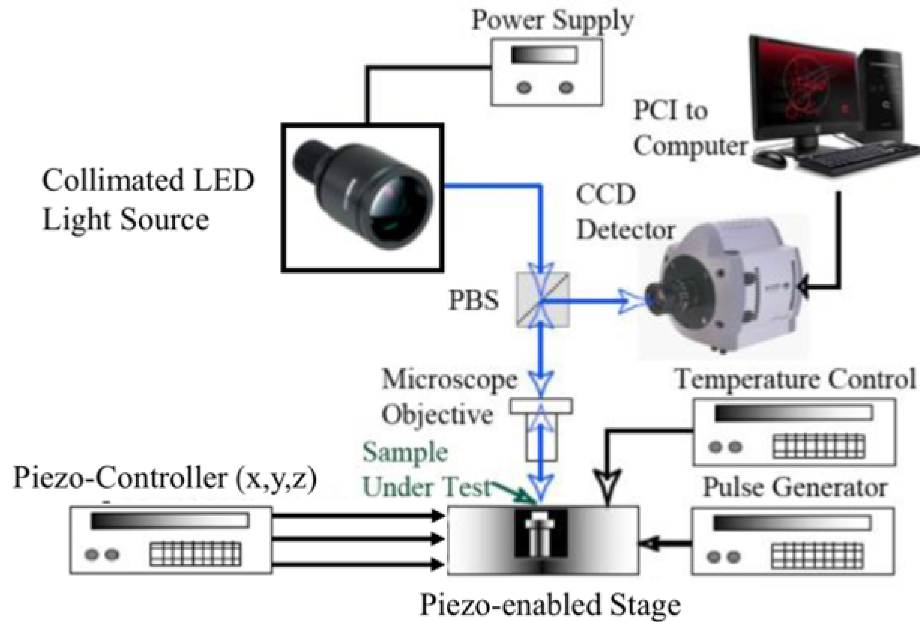


Figure 4.3: Illustration of experimental setup used for Thermoreflectance imaging [71].

4.4 Experimental Setup

The thermal imaging system is based on thermoreflectance physics and it uses a 4.4 µm × 4.4 µm pixel size CCD camera to measure the surface temperature field of activated microelectronic devices with sub-micron spatial resolution (0.29 µm with 470 nm LED) and 0.1 °C thermal sensitivity with temporal resolution of 100 nm. A highly sensitive lock-in technique that measures the change in a material's reflected light for each pixel is incorporated. Transient imaging module is used to generate timing signals for camera, LED, and device synchronization [71]. Function generator and temperature controller supplies the voltage potential and keep track of thermocouple mounted to read ambient and chuck temperature. A high-resolution CCD-based thermoreflectance imaging provides fast data acquisition times that can read thermal changes over a wide range of materials.

The basic experimental setup used for the thermal imaging is shown in Fig. 4.3. The

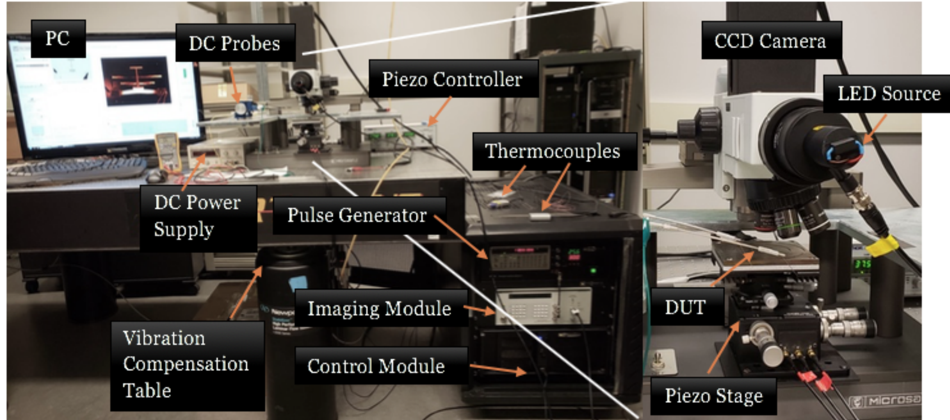


Figure 4.4: Experimental setup at University of Waterloo

setup consists of a visible light emitting diode (LED) as the source of probing light, which is focused onto the sample through the microscope objective. The light reflected back from the sample is captured by the charge-coupled-device (CCD) camera and is analyzed by the computer. This reflected light from the sample is modulated according to the variation in temperature of the sample, hence various modulation schemes can be used for detecting the relative change in reflectivity of the surface of DUT as mentioned in [63]. The setup is mounted on vibration compensated table, as vibrations can lead to focus offsets (Fig. 4.4).

The measurements were carried out using the blue LED (470 nm wavelength) as the illumination source and 20x objective lens. Although the thermoreflectance coefficient is a parameter dependent on material and illumination wavelength, but it is also affected by the magnification and numerical aperture (NA) of the microscope objective. Hence, the measurements were performed starting from a low NA and lower degree of magnification over a large area of sample surface. One of the reasons to not use high NA is that thermal expansion causes displacement of the Chevron tip and hence, can defocus the image seen by the lens. This highlights the need of piezo position controller for autofocusing during calibration [71], which is used for our measurements. Since most of the thermal imaging is done at ambient temperature, the calibration of the thermore-

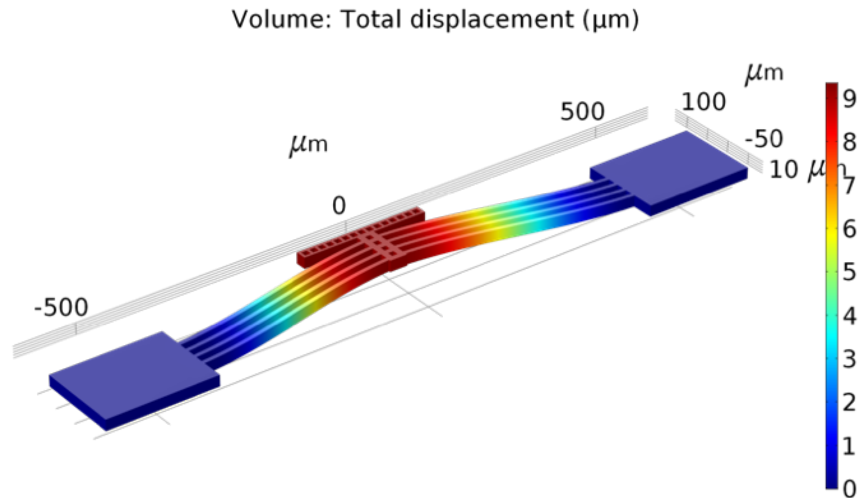


Figure 4.5: Total tip displacement at 11 V input voltage

flectance coefficient can be done by thermocouple-based calibration schemes.

4.5 Results and Discussion

The designed actuator has been simulated for displacement, stress and temperature distribution. Depending on the resistivity of silicon wafer, the device designed to provide 10 µm tip displacement with reasonable actuation voltage. The structure is simulated in COMSOL Multiphysics. Fig. 4.5 shows the total displacement of the Chevron actuator whereas Fig. 4.6 shows the von Mises stress distribution in the actuator. Heat distribution is shown in Fig. 4.7. It is important to design thermally driven actuator to provide desired displacement without going more than 2/3rd of the melting point of the material. Increasing temperature also affects the young's modulus of the material.

The actuator provides 10 um displacement at the application of 11 V and due to the resistivity of silicon layer, around 740 °C temperature is generated in the thin beams. Silicon can handle higher stresses, and the designed actuator due to its thickness shows

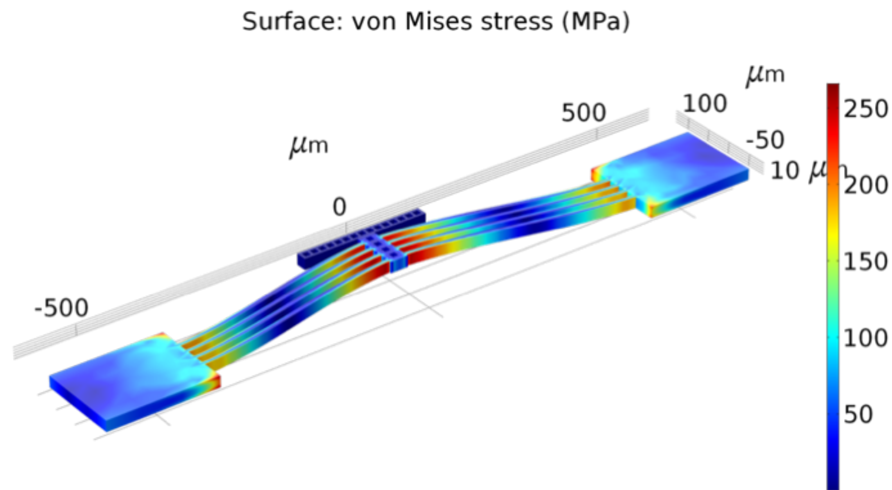


Figure 4.6: Stress distribution showing 250 MPa stress

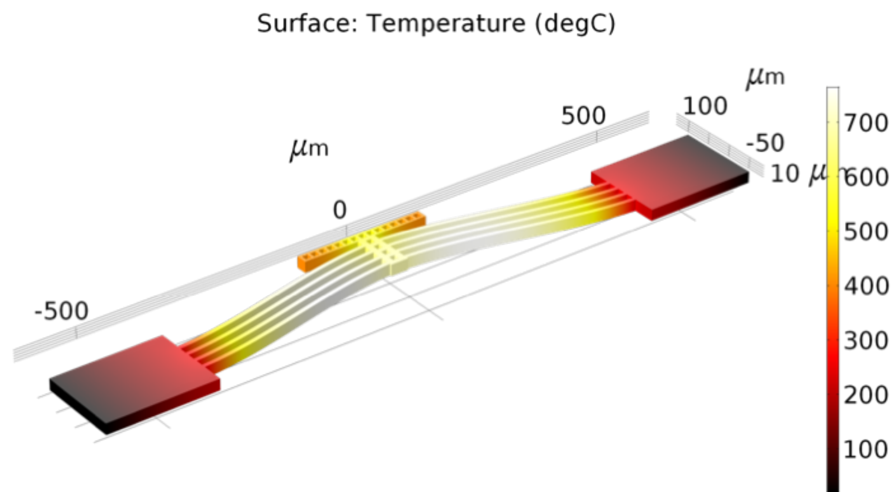


Figure 4.7: Temperature distribution in Chevron actuator. Maximum temperature reaches at 740 degC at 11 V

250 MPa stress.

Steady state thermal analysis was carried out experimentally using the CCD-based thermoreflectance technique. DC voltage is applied from 5 V to 13 V with ON pulse du-

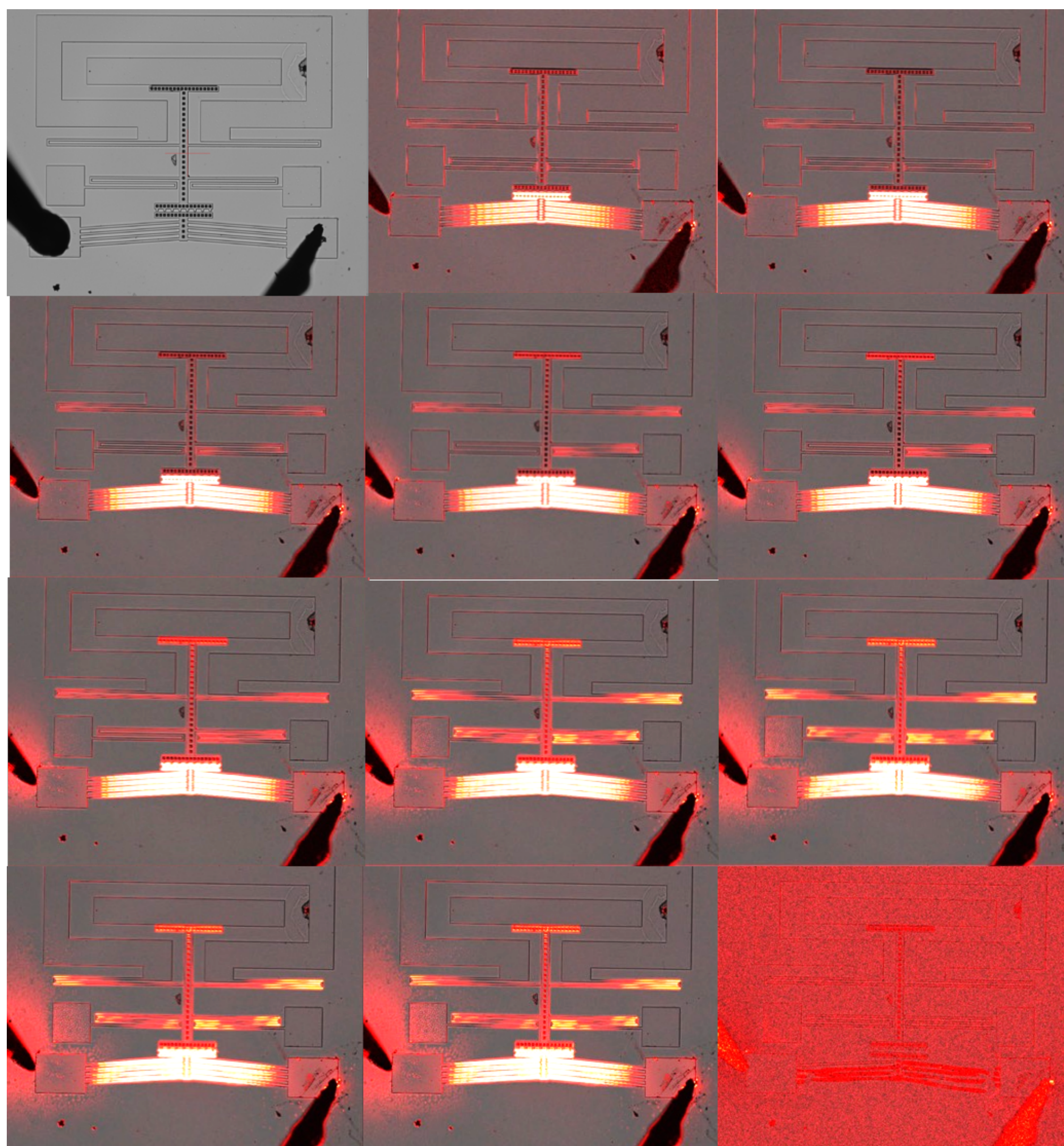


Figure 4.8: Thermal imaging microscopy of Chevron actuator. (Top left) CCD image of Chevron actuator, (Top mid to bottom right) Thermal image during voltage application of 5 V to 13 V.

ration of 10 sec and OFF pulse of 10 sec. ON pulse is the hot pulse while OFF pulse provides adequate time for cooling. All the measurements were averaged with minimum

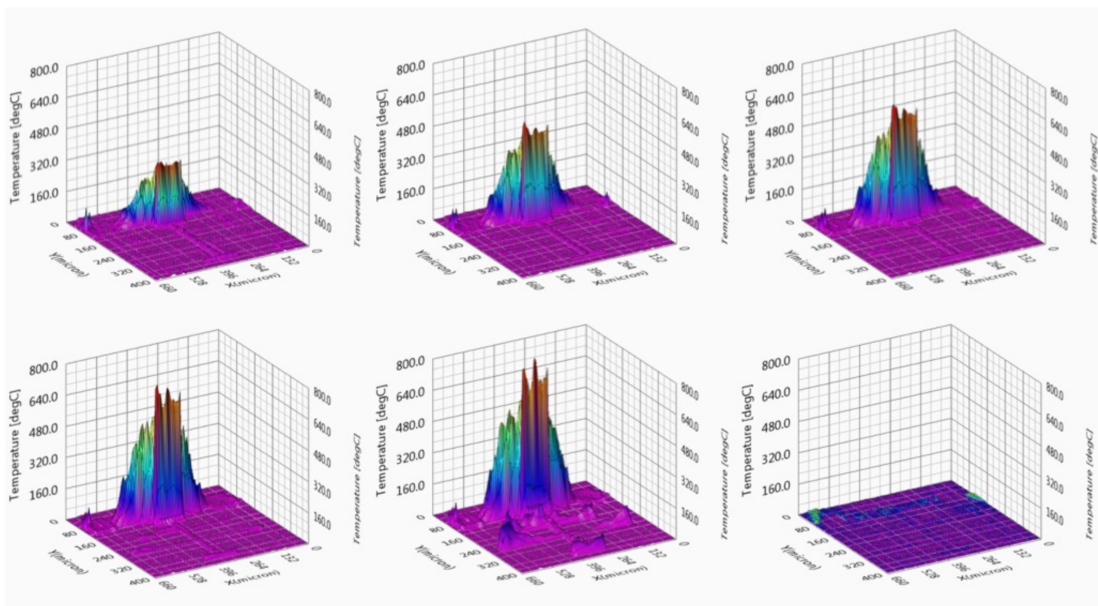


Figure 4.9: 3D heat profile of thermally driven Chevron actuator at (from left to right) 5V, 6V, 7V, 9V, 11V and 13 V potential applied across actuator.

5 cycles to rule out deviations as any artifacts and sudden temperature deviations can lead to deviation in output results. Chevron actuator shows 10 μm displacement and the maximum temperature reaches 810 °C at 11 V. Increasing voltage leads to breakage of a single beam, and temperature drops to 758 °C at 12 V and 711 °C at 12.5 V respectively. Applying 13 V leads to open circuit due to excessive heat generation.

Each temperature readout is averaged at-least at 5 times. Fig. 4.8 shows the thermal imaging microscopy images of Chevron actuator and Fig. 4.9 shows the 3D profile of the temperature distribution. CCD image of damaged Chevron actuator when 13 V is applied is shown in Fig. 4.10. From thermal imaging, it is observed that 10 V is enough to generate 10 μm displacement. Applying higher voltage leads to high contact force and higher displacement.

The experimental results match closely with the simulations. The difference in the simulation and experimental data is due to the substrate resistivity and specific heat con-

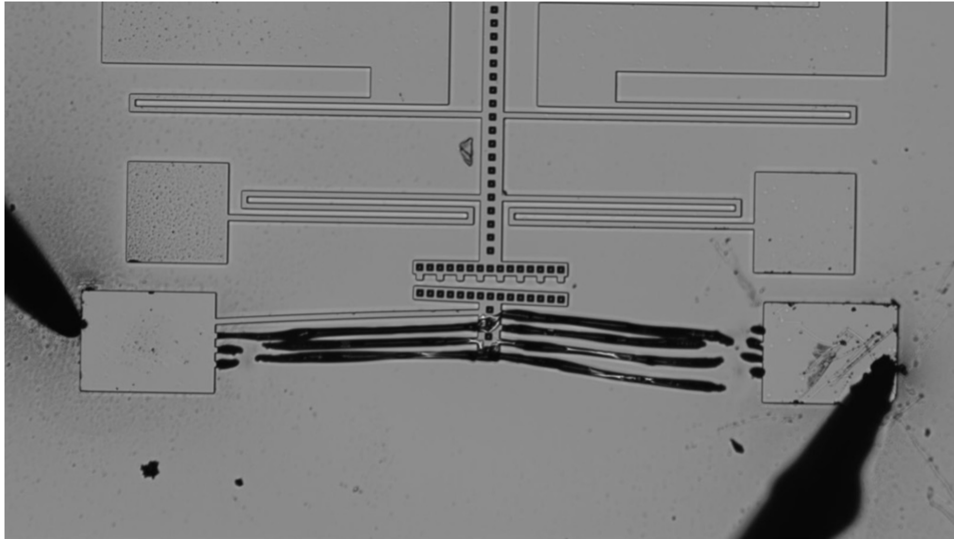


Figure 4.10: Optical CCD micrograph of broken Chevron actuator at 13V potential.

stant. Manufacturer states < 0.005 ohm.cm resistivity, thus we measured the resistivity using four-point probe and used the same value in our simulations. During microfabrication, lithography step including exposure or development phase can create some offset in gaps or visible features.

4.6 Summary

Thermoreflectance (TR) imaging is known for providing high-resolution and accurate thermal images of various electronic devices at the micro-scale. It is well-known for its sub-micron spatial resolution and excellent temperature resolution ($\sim$10 mK). In this chapter, we analysed the surface temperature profiles of microelectromechanical (MEMS) actuators using a charged coupled device (CCD)-based thermoreflectance non-contact and non-destructive imaging tool. TR imaging is used to study the temperature distribution, displacement and failure analysis of chevron actuator fabricated on a silicon-on-insulator (SOI) wafer. Results are compared with the finite-element mod-

Table 4.2: Temperature, resistance and current measured across MEMS Chevron actuator

Voltage Applied [V]	**Current Measured** [mA]	**Temperature Measured** [°C]	**Resistance Calculated** [Ω]
5	65	324.59	76.92
6	82	518.62	73.17
7	96	609.13	72.92
8	107	708.17	74.77
9	115	730.92	78.26
10	119	779.66	84.03
11	121	810.01	90.91
12	133	758.56	90.23
12.5	152	711.07	82.23
13	0	20.02	Open Ckt

elling predictions. The thermal analysis of such actuators can help in reducing dc power consumption and in enhancing reliability.

Chapter 5

Variable Attenuator for Millimeter-Wave Applications

5.1 Introduction

Variable attenuators find applications in radio frequency communication front end modules, network analyzers, frequency spectrometers for controlling and adjusting signal level. Variable attenuators are often realized using semiconductor elements such as PIN diodes [11, 12, 72–74], utilizing the property that the PIN diode behaves as an ordinary PN junction diode at low frequencies, but at high frequencies it behaves as a current-controlled resistor. However, their inherent high power consumption, limited power handling and low linearity degrades their performance and barring their use in advanced millimeter-wave systems that particularly demand a stringent linearity performance. Recently, graphene-based [23, 24] and VO_2 based variable attenuators have also been reported in [25, 75]. The RF Microelectromechanical systems (MEMS) technology is hugely popular in building several communication components such as phase shifters, reconfigurable impedance matching networks, and switch matrices [76–78]. The low insertion loss, superior isolation, linearity and power consumption properties of the

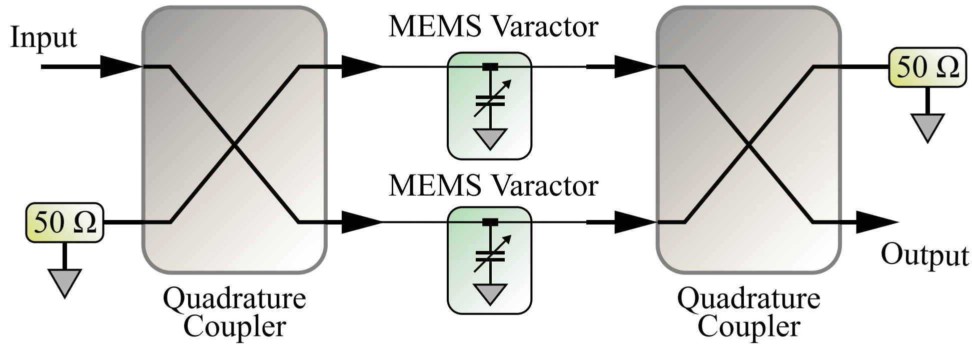


Figure 5.1: Schematic of proposed variable attenuator consisting of two 3 dB hybrid couplers and RF MEMS varactors

MEMS devices make them very promising candidates for such applications. However, there is not much literature that reports the implementations of RF power attenuators using this technology. Few attempts involving MEMS based ohmic switches electrostatically controlled to select/deselect the resistive loads that attenuate the RF signal at millimeter-wave frequencies have been recently explored [28, 29]. However, such devices employ mechanical movement in vertical direction of the electrostatically actuated suspended gold membranes, thus they are prone to reliability issues such as stiction, dielectric charging, micro-welding, etc.

A brief description of the concept of a 60 GHz MEMS-based variable attenuator, with limited measurement results, is given in [70]. In this chapter, we present details of design and fabrication of a monolithically integrated variable attenuator consisting of two lateral varactors integrated with two CPW 3 dB hybrid couplers realized on silicon-on-insulator (SOI) substrate. The proposed SOI-based fabrication process involves the use of gold as the metal layer, which requires additional steps to the aluminum-based process presented in [70]. Both theoretical and measurement results are presented for the proposed Chevron actuator design. Measured results are presented for individual components as well as for the fully integrated attenuator.

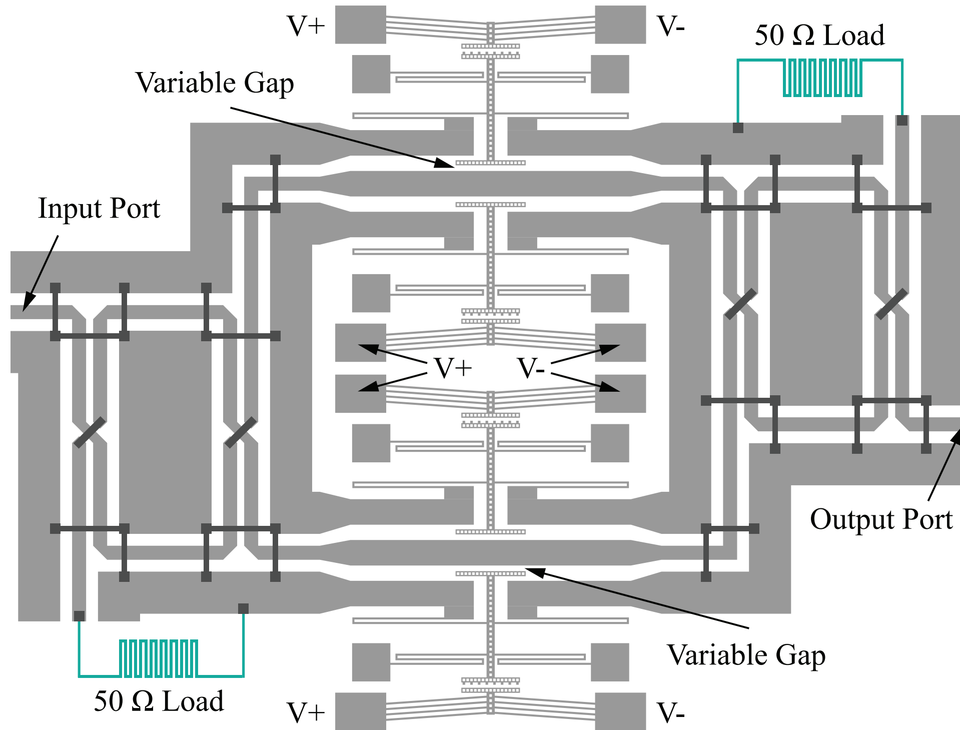


Figure 5.2: Layout of monolithically integrated RF MEMS-based variable attenuator displaying the variable gap between capacitive plates, input and output ports, and 50 Ω loads

5.2 Design and Operation Principle

Fig. 5.1 illustrates a schematic of the proposed attenuator concept. It consists of two hybrids and two varactors. The variation of capacitive loading to ground changes the insertion at the output. For very low values of capacitance, the insertion loss is basically the sum of the insertion loss of the two hybrids. As the capacitance is increased the insertion loss seen at the output increases gradually. Fig. 5.2 shows the layout of the fully integrated attenuator. The varactors used here operate on the principle of varying the gap between the signal line and a movable plate. The movable plate is connected to the Chevron actuator, which is responsible for providing lateral motion by the application of DC voltage as shown in Fig. 5.2. The amount of lateral displacement is controlled by the voltage applied to the Chevron actuator. The variation of the gap between the movable

plate and the signal line with the voltage leads to a change in capacitive coupling to the RF ground.

For a transmission line loaded with a shunt capacitor C, the S-parameters of the 2-port device depend on the loading effect of the capacitance and can be written as:

$$S_{11} = \frac{-j\omega C Z_0}{2 + j\omega C Z_0} \tag{5.1}$$

$$S_{21} = \frac{1}{1 + j\omega C Z_0/2} \tag{5.2}$$

where, S_{11} is the return loss and S_{21} is the insertion loss of the loaded RF transmission line. C is the capacitance that varies as the gap between the moving plate and the trans-

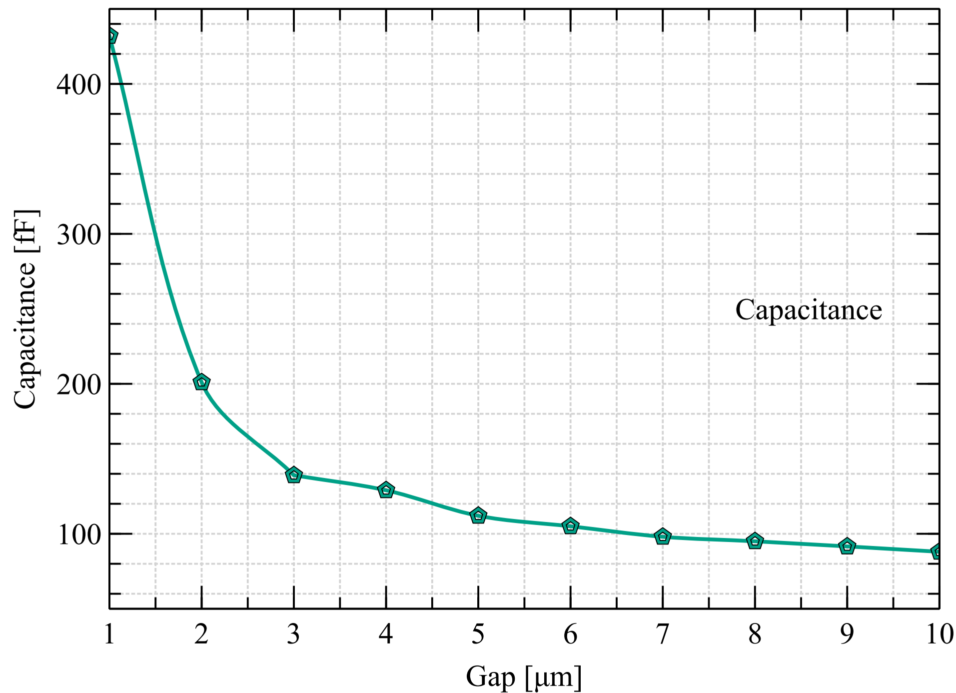


Figure 5.3: EM simulation of capacitance with a linear change in variable gap between signal line and actuator plates.

mission line is varied. Z_0 is the characteristic impedance of the RF signal line. There are two movable MEMS varactors in each RF branch. The capacitance values for different gaps between signal line and actuator plate is simulated using ANSYS HFSS as shown in Fig. 5.3.

The whole integrated attenuator has a footprint of 3.8 mm x 3.1 mm. All parts are co-fabricated on the 20 µm thick device layer of SOI wafer. The RF input is applied at the port 1 of the first hybrid, while its port 4 is terminated in a 50 Ω load. This input signal is split equally by the 90°hybrid between the two CPW lines with MEMS varactors. This is where the signal attenuation level is controlled, and the signal flows to the output hybrid coupler, which combines the two signals at the output port. The remaining port of the second hybrid coupler is terminated in a 50 Ω surface mount resistor.

This concept is very useful for millimeter-wave applications because even a small capacitance change to the ground can yield measurable isolation. Since the varactor involves lateral motion of 20 µm thick silicon structures, it eliminates the conventional MEMS reliability issues associated with MEMS varactors that use thin membranes.

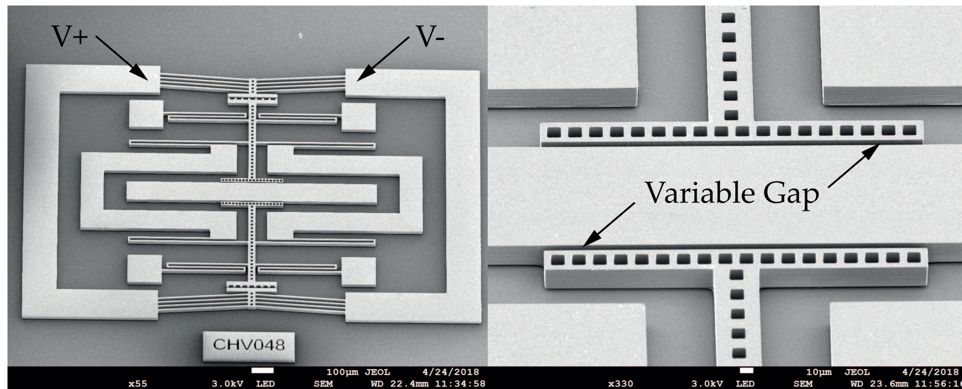


Figure 5.4: SEM micrograph of fabricated RF MEMS varactors with the tunable capacitive gap controlled by Chevron actuators and zoomed in view of movable plates on both sides of the signal line.

5.2.1 MEMS Varactors-Loaded CPW Line

Fig. 5.4 depicts details of the fabricated varactor-loaded CPW line. The operating principle involves applying dc voltage to the anchors of a Chevron actuator, which in-turn drives the central beam forward, hence closing the gap between the movable plate and the signal line. This changes the capacitive coupling to the ground leading to change in

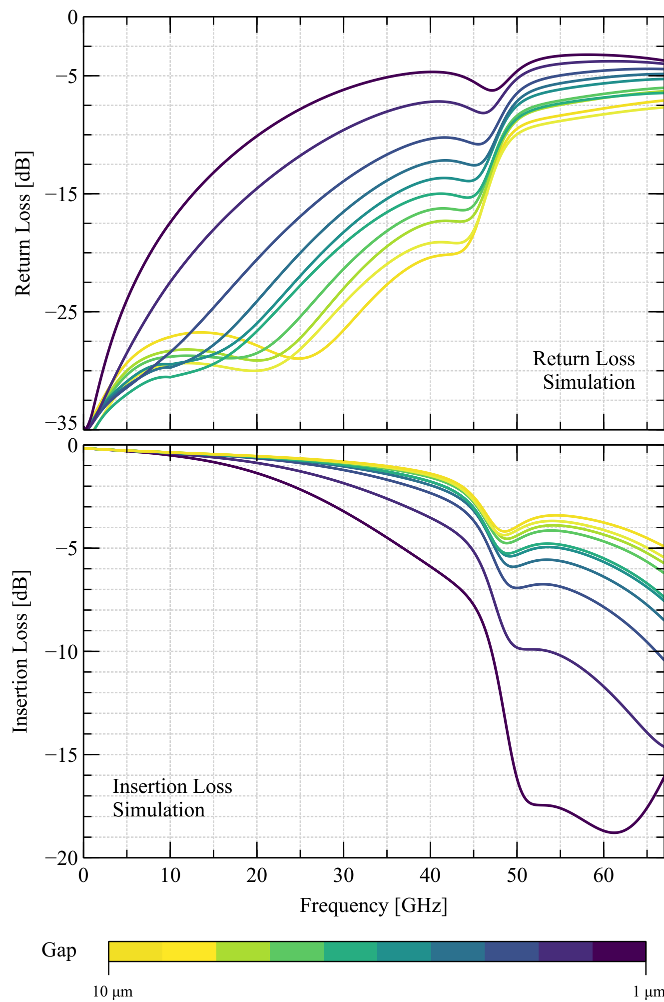


Figure 5.5: EM simulation of S-parameters: (top) Return loss and (bottom) Insertion loss of MEMS varactor from DC to 67 GHz with variation in gap from 10 µm to 1 µm.

isolation. Two movable capacitive plates on each side of the signal line were used, as it provides higher capacitance change, thus resulting in better isolation. The capacitance is shorted at one end to the RF ground through flexible arms. With no applied voltage to the electrothermal actuator, the gap between the movable plates and the signal line is relatively large (10 µm) leading to weak capacitive coupling to ground. Hence, the RF

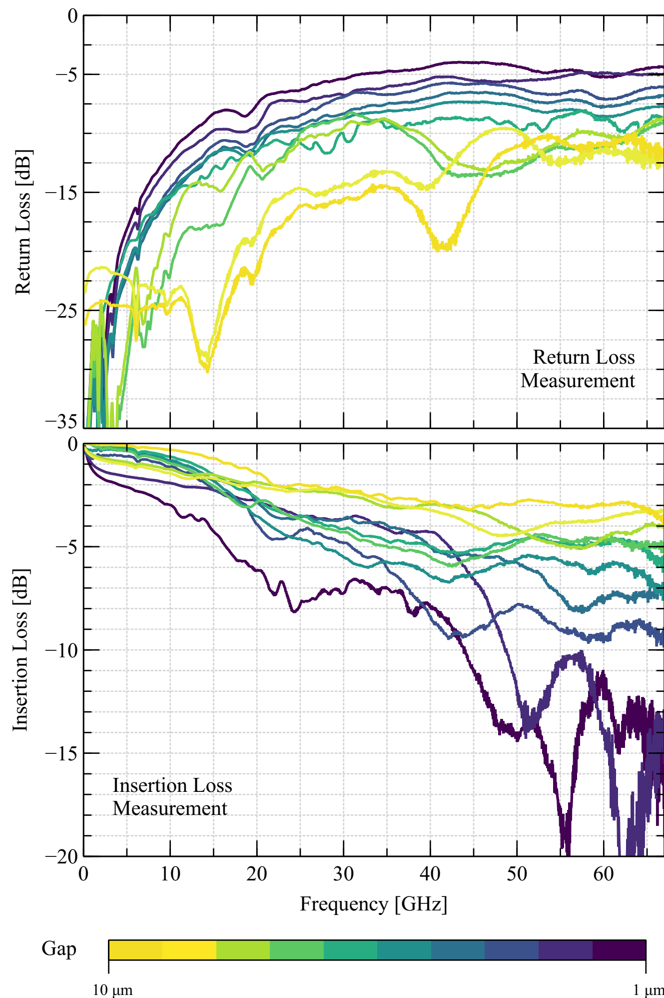


Figure 5.6: Experimental measurement of S-parameters from fabricated structure: (top) measured return loss and (bottom) measured insertion loss of the MEMS varactor from DC to 67 GHz with varying gap.

signal that transmits along the CPW line experiences a minimum attenuation. As the voltage is applied and the plates move closer to the signal line, the capacitive coupling increases, leading to an increase in isolation. The EM simulations of the MEMS varactor were done in ANSYS HFSS and are shown in Fig. 5.5. The insertion loss of the varactor varies from −4 dB to −19 dB at 60 GHz. It can be observed, that the effect of capacitive coupling and variation in insertion loss is better at higher frequencies than lower frequency ranges. The return loss also varies as the gap is tuned, with good return loss when the capacitive loading is low and it drops drastically when the capacitive loading gets larger.

A two-port measurement of the varactor-loaded CPW line was carried out using vector network analyzer (VNA) and the results are shown in Fig. 5.6. The isolation varies from −3 dB to −20 dB at 60 GHz as the applied voltage to the Chevron actuator is increased from 1 V to 9 V. The return loss also shows variation from −14 dB to −5 dB as the gap between the varactor plates closes successively till it reaches 1 μm.

5.2.2 Hybrid Coupler

Hybrid couplers are important passive components used in various microwave circuits such as mixers, balanced amplifiers and phase shifters. In the proposed variable attenuator circuit shown in Fig. 5.2, we have used hybrid couplers on both sides of the MEMS varactor-loaded CPW lines. CPW based tandem −3 dB hybrid coupler was used as it

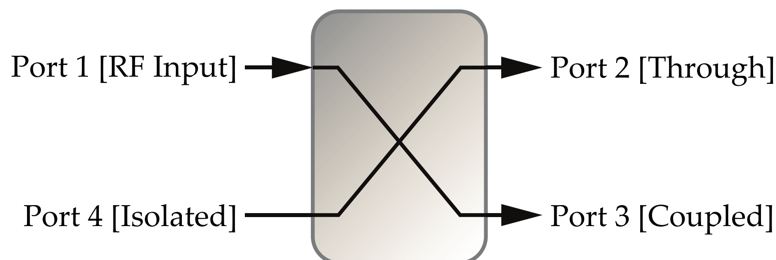


Figure 5.7: Schematic representation of quadrature coupler, highlighting RF port numbers.

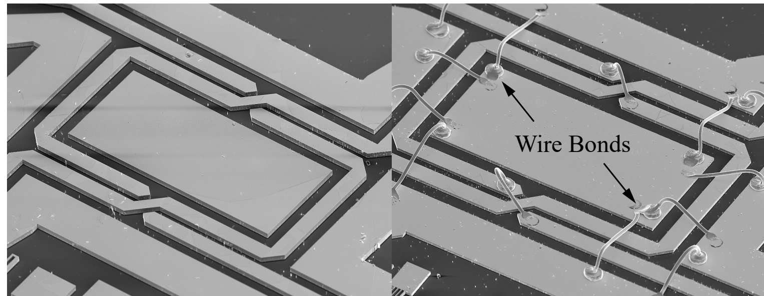


Figure 5.8: CPW based quadrature hybrid coupler: (left) before wire bonding (right) after wire bonding the ground planes and the signal lines

can be monolithically integrated with the laterally moving MEMS varactors. It has two-section CPW parallel-coupled lines and wire-bonded structures [79, 80]. The process tolerance and the minimum width and pitch required for wire bonding were considered while designing the coupler. The signal provided at input port 1 is split equally between the direct port 2 and the coupling port 3, while port 4 acts as the isolation port as shown

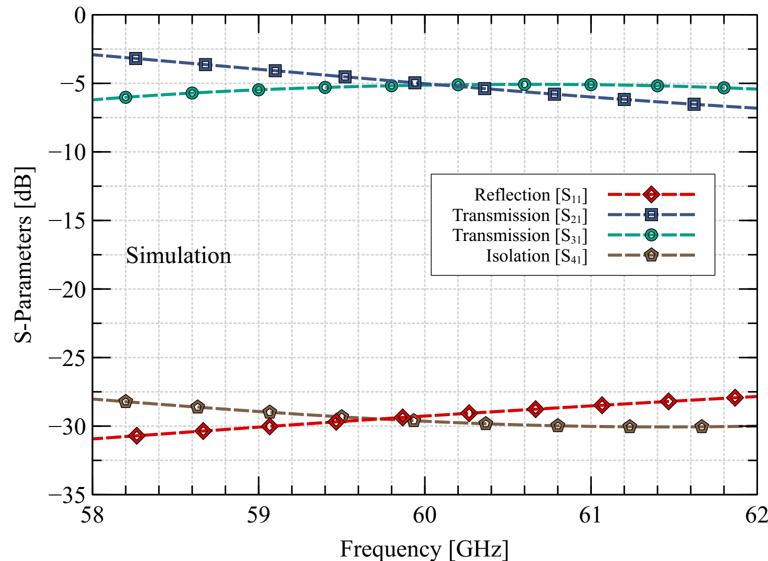


Figure 5.9: Simulated S-parameters of hybrid coupler for the range 58 GHz to 62 GHz showing a −5 dB coupling at 60 GHz between S_{21} and S_{31}, and the return loss at the input port (S_{11})and isolation port (S_{41})

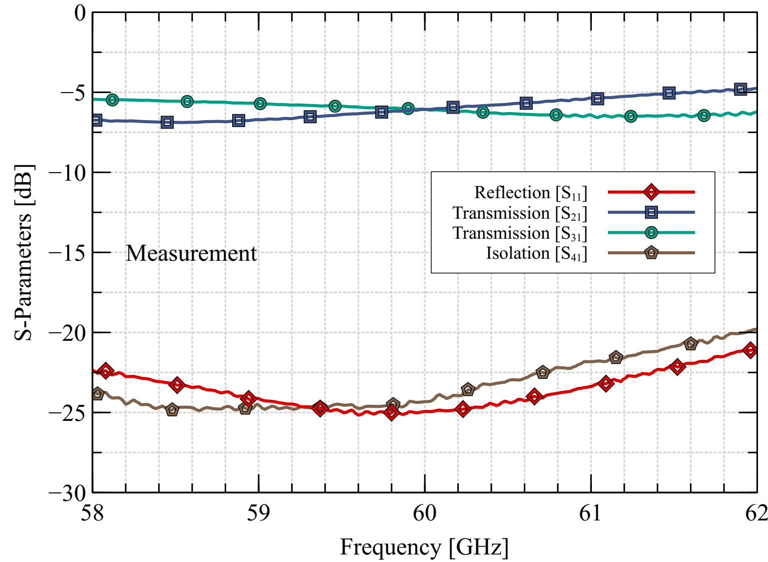


Figure 5.10: Measurement results of the RF performance of fabricated hybrid coupler module displaying −5.8 dB coupling at 60 GHz and the return loss at port 1 and port 4 for the 58 GHz to 62 GHz frequency range

in the schematic in Fig. 5.7. The individual coupling line lengths are smaller than $\lambda/4$ at 60 GHz to compensate for the broadside coupling effect generated by the wire bond crossovers. Wire bonds were used to provide the crossover connections between the two signal lines and between the ground planes as shown in Fig. 5.8. Although adding another metal layer to form an air bridge type structure for the crossover connections would have provided a more reliable operation at the millimeter wave frequencies than the wire-bonded structures, but wire bonding was done to keep the fabrication steps simple.

The structural dimensions were optimized for coupling at 60 GHz using ANSYS HFSS and Sonnet EM simulations. The width of the central ground plane was optimized for the lowest return loss and isolation at 60 GHz, however it doesn't have any significant effect on the coupling. The simulated results shown in Fig. 5.9 display an excellent equal coupling at the center frequency of 60 GHz with 4 GHz bandwidth for both (S_{21}) and

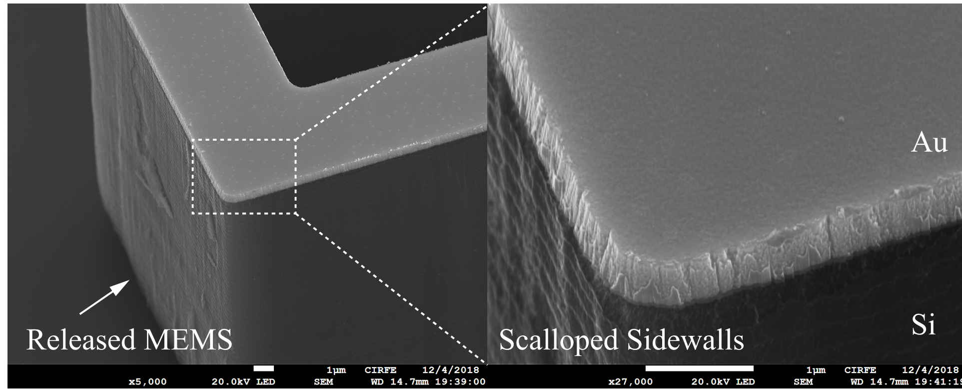


Figure 5.11: SEM micrograph of the fabricated structure: (left) sidewalls of the 20 μm thick device layer structures obtained after Si-DRIE, (right) a zoomed in view of the edge displaying the top metal coverage and scallops in the sidewalls

(S_{31}). The return loss better than −25 dB can be observed at the input port and an isolation of better than −27 dB was observed over the frequency range of 58 GHz to 62 GHz. To measure the four-port S-parameters of the fabricated coupler using a two-port vector network analyzer system, we used three different configurations for identically designed couplers, by successively terminating different sets of ports in matched load. The final measured results obtained by combining the three different configurations are shown in Fig. 5.10 and display fair agreement to the simulated results with the equal coupling around −6 dB and a return loss of better than −20 dB over a bandwidth of 4 GHz. It should be mentioned here that while the coupler exhibits a 3 dB of insertion loss, it is not an issue here since the device is used as an attenuator. Moreover, the insertion loss of the coupler can be improved by using a thicker gold layer as well as by using a high resistivity Si substrate for both the device layer and the handle layer.

Since the process requires sharp vertical structures/patterns with high-aspect ratio, Bosch process for Si-DRIE was employed in the fabrication process. The alternating plasma steps were used. The first step etches the silicon for a short period, then rapidly shuts off the gas and plasma, and the second step initiates a plasma that deposits an inhibitor film on the exposed surfaces. This alternating sequence continues as the etch

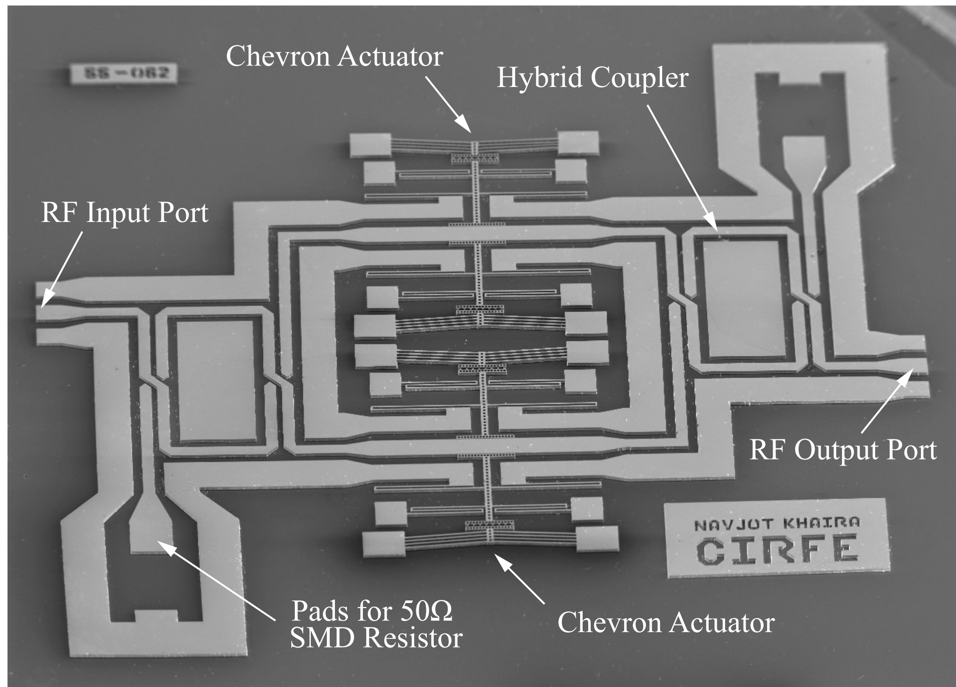


Figure 5.12: SEM micrograph of the fabricated variable attenuator module showing the RF input and output ports, hybrid couplers, MEMS varactors controlled by Chevron actuators and the pads where 50 Ω resistors are surface mounted

progresses and explains the scallops observed on the sidewalls as shown in Fig. 5.11. The duty cycle between the steps and the gas pressure is carefully controlled to achieve sharp vertical walls.

5.3 Results and Discussion

At first, we tested the DC behavior of different samples of MEMS varactor-loaded CPW lines fabricated on the same SOI wafer at different locations. All of them exhibited repeatable 10 μm lateral movement of switching plates by applying biasing voltage of 9.8 V. Then we tested three hybrids with loads located at different ports, to allow full characterization of the hybrid. As shown in Fig. 5.10, the measured results of the millimeter-wave

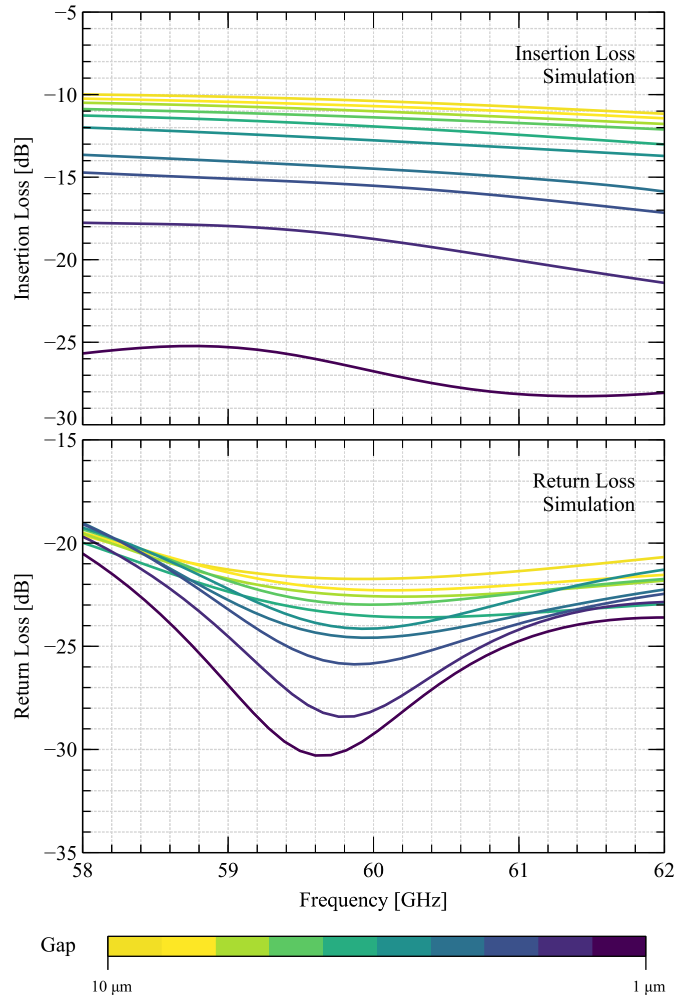


Figure 5.13: Simulated S-parameters of the variable attenuator module from 58 GHz to 62 GHz: (top) insertion loss variation with the gap displayed in the colour scale (bottom) return loss for different gap sizes

hybrid are in good agreement with simulation. The SEM micrograph of the fully integrated attenuator unit is shown in Fig. 5.12. The EM simulations were performed in ANSYS HFSS and the results are shown in Fig. 5.13. The insertion loss of the variable attenuator varies from −10 dB to −27 dB at 60 GHz as the capacitive gap is decreased from 10 µm to 1 µm. A return loss of better than −20 dB over the entire 4 GHz range for

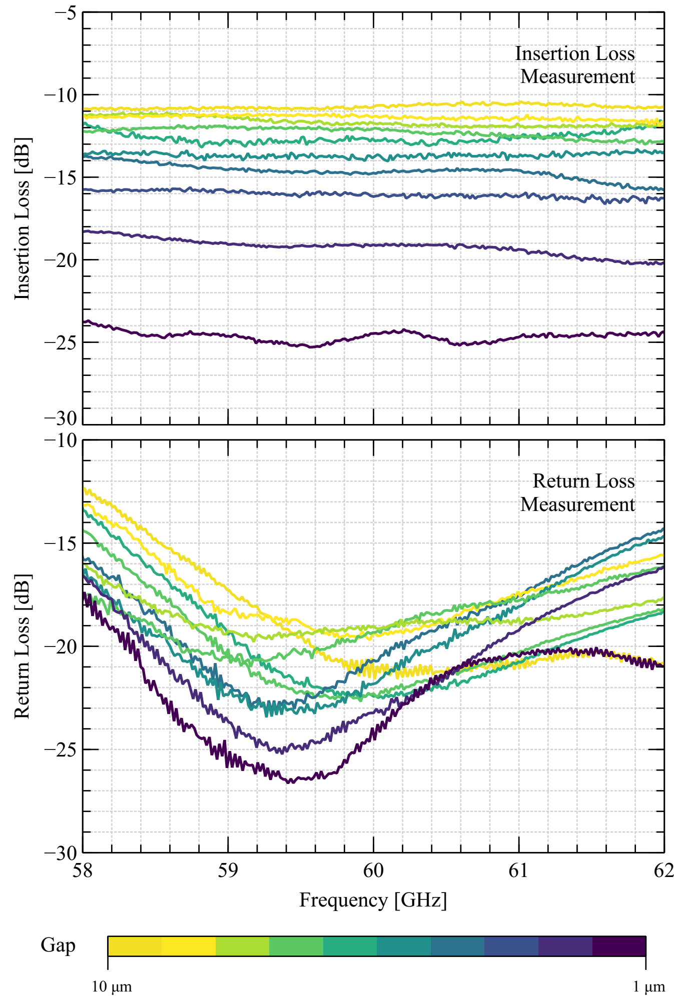


Figure 5.14: Measured S-parameters of the variable attenuator module from 58 GHz to 62 GHz: (top) insertion loss variation with the applied bias (bottom) return loss for different gap sizes

the different gap values is predicted by the simulations.

The S-parameters of the fully integrated variable attenuator are measured on a probe station using VNA. The measurements are conducted in air, under standard conditions of temperature and pressure. DC voltage was applied to the pads of the Chevron actuator using dc probes on the probe station. The insertion loss and return loss of the variable attenuator are measured while the gap between the signal line and movable

plate varies from 10 μm to 1 μm, as the applied voltage to the pads is increased from 0 V to 9.8 V. Fig. 5.14 shows that the measured insertion loss of the variable attenuator varies between −10.8 dB and increases up to −25 dB (i.e. a tunable attenuation range close to 15 dB) with the linear motion of the movable plates. The return loss also varies as the gap between the switching plate and signal line changes but maintains a value below −19 dB at 60 GHz. It can be noted that the HFSS model predicted the attenuator characteristics quite accurately, but the return loss was slightly worse in actual measurements than what was predicted by simulations. The difference between measured and simulated results is attributed to the slight variation in gap after the structures are released and also from other process variations. Overall, the measured results are in good agreement with the simulated results.

5.4 Summary

This chapter reports a millimeter-wave RF MEMS-based variable attenuator implemented by monolithically integrating CPW based hybrid couplers with lateral MEMS varactors on a SOI substrate. The MEMS varactor features a Chevron type electrothermal actuator that controls the lateral movement of a thick plate allowing precise change of capacitive loading on a CPW line leading to a change in isolation between input and output. The proposed variable attenuator is successfully fabricated on an SOI substrate with a device footprint of 3.8 mm to 3.1 mm. The fabrication process provides flexibility to extend this module and implement more complex RF signal conditioning functions, thus making it more appealing to realize a wide range of reconfigurable RF devices. The measured RF performance shows that the device exhibits attenuation levels (S_{21}) ranging from 10 dB to 25 dB, at the center frequency of 60 GHz with a bandwidth of 4 GHz and a return loss of better than 20 dB. The device involves laterally moving 20 μm thick structures, hence offers a reliable operation and eliminates MEMS problems like stiction, dielectric charging and micro-welding observed in surface micromachined thin membranes.

Chapter 6

Monolithically Integrated Impedance Tuner

6.1 Introduction

Over the past few decades, impedance tuners based on MEMS technology have attracted a great deal of interest as they have the potential to provide improved impedance tuning range, better linearity and power handling capability compared to the solid-state tuning elements utilizing electronic tuning [81, 82].

Such impedance tuners are currently employed in a wide range of commercial communication wireless devices and have an important role in realizing intelligent multi-band RF-front ends. Impedance tuners compensate for the antenna impedance variations that arise within an RF-front end due to switching of frequency band of operation. Such systems are useful not only in enabling more than one frequency band of operation but can also adapt dynamically with variations in temperature, output power levels and process deviations. They ensure optimum power transfer and highest system efficiency [83, 84].

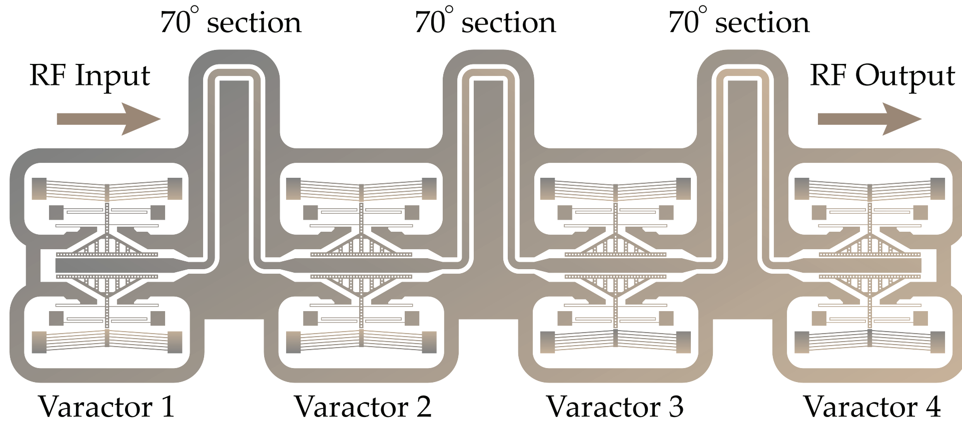


Figure 6.1: Layout of MEMS based impedance tuner, highlighting three 40 degree sections and four varactors.

Although many RF MEMS tuners have been reported with wide impedance coverage range [85], most are realized using hybrid integration by integrating MEMS switched-capacitors [86, 87] with PCB circuit or other lumped element components. Several attempts to achieve contact-less tuning have been made [88, 89]. The proposed impedance tuner is based on contact-less approach which does not suffer from any contact area wear and damage, poor power handling caused by the limited contact area or dielectric charging.

This chapter presents a monolithically integrated design that utilizes laterally moving plates located strategically along a CPW line to change its characteristics. The varactors can be tuned to certain capacitance range with the application of DC voltage. Varying the capacitance between the signal line and MEMS varactor, results in impedance tuning. As several combinations of capacitances can be achieved by controlling motion of the movable plate, it will generate more impedance points and a better coverage compared to the case where the switched capacitors are used.

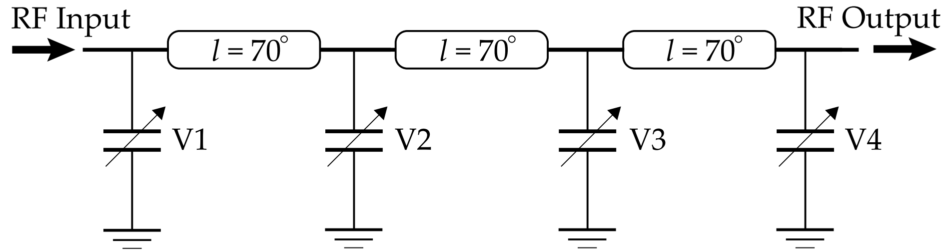


Figure 6.2: Schematic of impedance tuner using varactors and 40 degree sections

6.2 Principle of Operation

Fig. 6.1 illustrates the layout of the impedance tuner. It consists of three 70-degrees CPW transmission line sections and four variable capacitor units. Each variable capacitor unit has two movable plates, one on each side of the signal line as shown in Fig. 6.1. The schematic diagram of the circuit is given in Fig. 6.2. The lateral motion of these plates leads to a variation in the capacitance with the lowest being 0.19 pF with 10 μm gap and maximum 0.8 pF at 1 μm gap by linearly varying DC voltage from 4 V to 12 V. Capacitance ratio of 4.2:1 can be achieved using MEMS varactors utilized. The gap between the capacitive plates is precisely controlled by a Chevron actuators. The Chevron actuator has an array of four V-shaped beams attached to a central beam with a pre-bent angle of 4-degrees. The voltage applied to the Chevron actuator leads to Joule heating which pushes the tip of chevron actuator forward. The Chevron is designed to achieve a maximum of 10 μm motion with an applied voltage of 12 V. The selective lateral movement of these capacitive plates gives the impedance tuning and a good coverage on the Smith Chart.

6.3 Device Design and Fabrication

The impedance tuner is optimized to exhibit excellent impedance coverage at 6 GHz. The overall footprint of the impedance tuner with four varactors is 6.4 mm $\times$ 2.2 mm. The

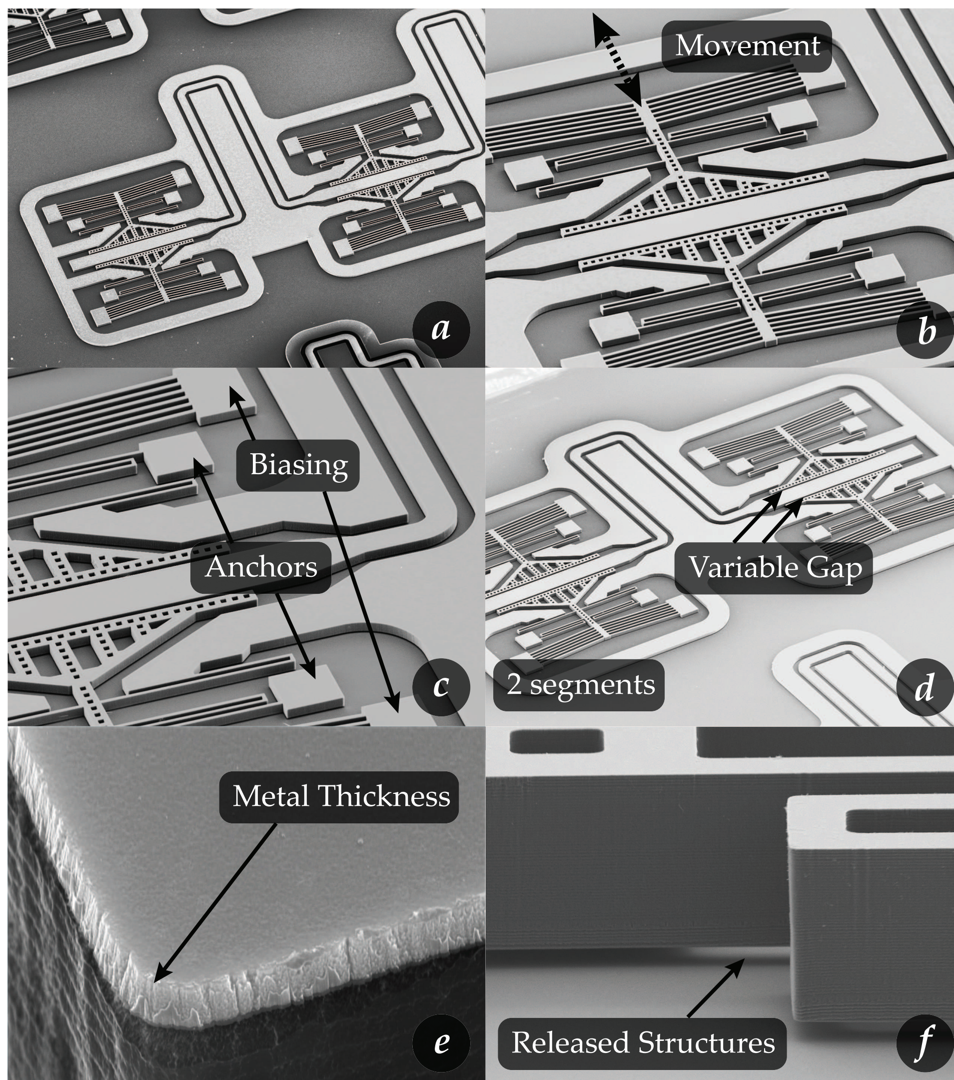


Figure 6.3: SEM micrograph of MEMS impedance tuner. a) overhead image of impedance tuner, b) close-up view of varactor unit, c) bias pads and anchors for movable varactors, d) highlighting variable gap of varactors, e). metal coverage on silicon device layer structures and f) close-up view of released structures.

device is fabricated using a micro-fabrication process on SOI wafer, that is cost effective and can be used to develop robust lateral MEMS devices using a single photolithography step. The fabricated impedance tuner is shown in Fig. 6.3. Fig. 6.3(a) shows the

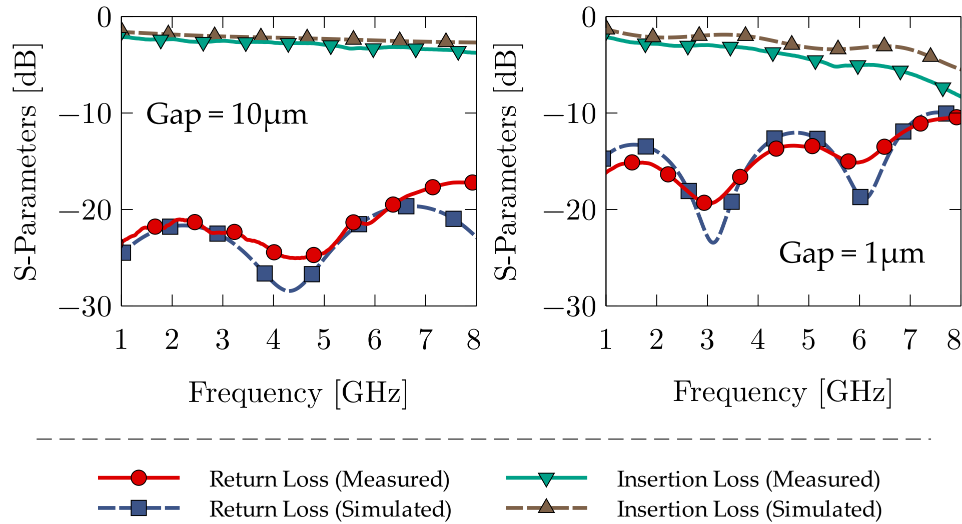


Figure 6.4: Simulation and measurement of impedance tuner (left) when all four varactors have minimum capacitance of 0.17 pF with 10 μm gap, and (right) when varactors have maximum capacitance of 0.8 pF with 1 μm and 12 V DC applied.

over head SEM micrograph, Fig. 6.3(b) highlights the direction of actuator movement for capacitive tuning. Fig. 6.3(c) shows the close up view of anchors and bias pads while Fig. 6.3(d) highlights the variable gap in varactors. Fig. 6.3(e) shows the metal thickness of gold on the device layer and Fig. 6.3(f) highlights the gap underneath the structures showing oxide been removed. Etch holes are designed on the beams for uniform etching of oxide layer. Due to the low resistivity of thick device layer, the transmission line sections are optimized for good RF matching. RF ground plane is connected through the outer boundary of the device to avoid wire bonding. The proposed device provides robust operation due to the utilization of thick silicon layer for movable structures. Lateral actuators offer a relatively large displacement and precise motion with the application of low DC voltage. This device is free from any reliability issues like contact micro-welding, dielectric charging and stiction.

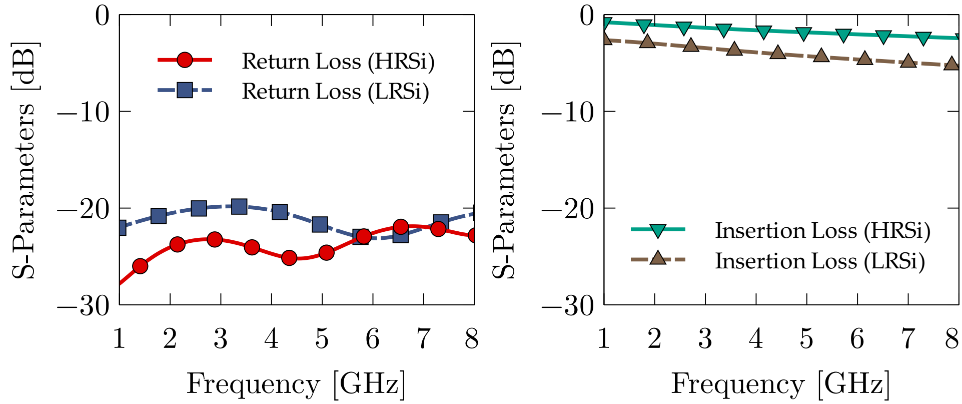


Figure 6.5: Comparison of simulated S-parameters of device utilizing low resistivity silicon (LRSi) and high resistivity silicon (HRSi) device layer.

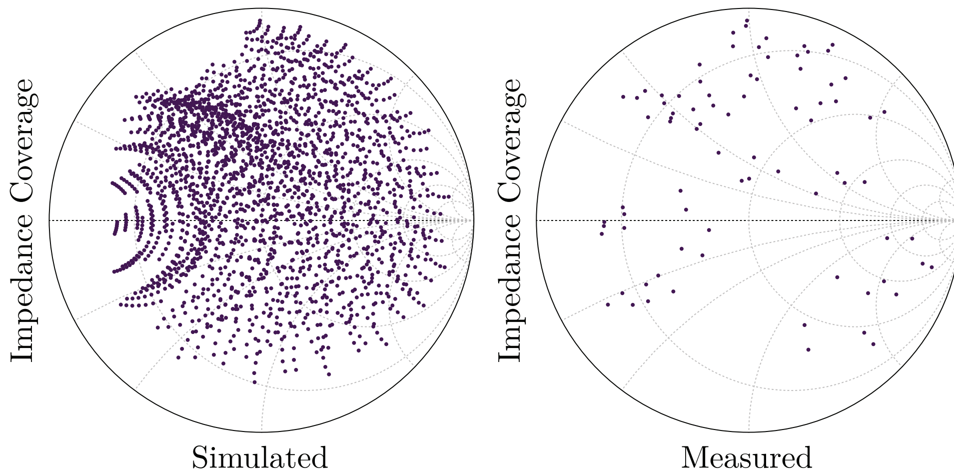


Figure 6.6: Simulated and measured impedance coverage at 6 GHz.

6.4 Results and Discussion

The measurement of the S-parameters of the fabricated impedance tuner was performed for the case when all the movable plates have a gap of 10 μm from the signal line and when the gap was reduced to 1 μm. The RF measurements were performed on-wafer using a vector network analyzer for the frequency ranging from 1 GHz to 8 GHz. As seen in Fig. 6.4, the circuit exhibits excellent RF performance with 2.9 dB measured insertion

loss at 6 GHz and a measured return loss of better than 20 dB when the gap between capacitive plates is 10 μm. When the capacitive plates are moved close to the signal lines to reduce the gap to 1 μm, the insertion loss of 4.6 dB and a return loss better than 16 dB is attained at 6 GHz. Very good agreement is observed between the measurement and EM simulation.

The Fig. 6.6 presents the simulated and measured impedance coverage at 6 GHz with 50 ohm output port termination. Since this is an analog tuner, it is impossible to measure all different configurations. The simulated data is presented for eight distinct capacitance values per varactor. About 80 experimental points were collected from the continuous range.

It should be mentioned that the high insertion loss is attributed to the use of a lower resistivity for the device layer of the SOI substrate and the use of a relatively thin gold layer of 600 nm. The insertion loss can be significantly improved by using a thicker gold layer and a high resistivity device layer. Fig. 6.5 shows a comparison of the simulated S-parameters of the circuit for the case when 20 μm thick device layer has low resistivity ($<$0.005 ohm·cm) and high resistivity ($>$10000 ohm·cm). Additional improvement of the insertion loss can be potentially achieved by backside etching of the silicon wafer. This leaves a scope of improvement for future work.

6.5 Summary

The design and implementation of a MEMS-based impedance tuner realized on a SOI substrate has been presented. Contactless lateral MEMS varactors were realized using laterally moving capacitive thick plates whose motion was precisely controlled using Chevron actuators. The voltage required for the maximum displacement is under 12 V. These varactors are monolithically integrated with CPW lines using a single mask fabrication process on SOI substrate. The implemented MEMS capacitive varactors exhibit a capacitance range of 0.19 pf to 0.8 pf. The improvement of the Smith chart coverage is

achieved by proper choice of the electrical lengths of the CPW lines and precise control of the lateral motion of the capacitive plates. The measured results demonstrate a good impedance matching coverage with an insertion loss of 2.9 dB. Details of the SOI-based fabrication process are presented along with discussions on techniques to improve the insertion loss of the device. The proposed design does not suffer from the dielectric charging, micro-welding and stiction problems associated with RF MEMS devices realized using surface micromachining processes. In addition, the device promises to be useful in high power applications, since it is constructed from lateral thick structures.

Chapter 7

Conclusion and Future Work

The main focus of this thesis is on the development of high performance variable attenuator and an impedance tuner using MEMS technology, which were fabricated in-house using a low-cost SOI based custom fabrication process that allows the monolithic integration of all microstructures on a single chip. The major contributions of this research are summarized below.

7.1 Contributions

The major contributions of this thesis are outlined as follows:

- A MEMS based 60 GHz variable attenuator has been presented with close to 15 dB of monotonically variable attenuation over a bandwidth of 4 GHz, making it suitable for a wide range of millimeter-wave applications. The device features two quadrature couplers integrated monolithically with MEMS varactors on an SOI substrate. A simple SOI-based fabrication process has been proposed that is flexible enough to allow monolithic integration of the variable attenuator with other RF devices. Both theoretical and experimental investigations have been presented

for the individual building blocks and the fully integrated attenuator. The device provides repeatable and reliable operation due to its robust structure that is made from thick silicon, hence has a much lower residual stresses and is free from any stiction or micro-welding problems. To out knowledge, the proposed concept is the first to be reported for the realization of MEMS-based millimeter-wave analog variable attenuators.

- Chevron actuator is studied for its displacement and heat distribution using thermoreflectance based thermal imaging system. Thermally driven Chevron actuator is designed and fabricated on SOI wafer and is investigated both experimentally and theoretically. Thermal imaging provides accurate picture of 2D temperature field which provides the ability to detect hot spots, diagnose performance, and assess reliability. In design and manufacturing of MEMS devices, thermoreflectance imaging has the potential to provide a rapid approach for analyzing the thermal behavior of complex structures, identify regions of excessive heat densities, and ultimately contribute to improved thermal designs, better device reliability, and shorter design cycle time.

- A MEMS based monolithically integrated impedance tuner is presented. The proposed device is developed utilizing the RF MEMS varactors on SOI substrate with high capacitance tuning ratio. The device exhibits wider impedance coverage. The insertion loss performance of the device can be improved significantly with the use of high-resistivity device and handle layer of SOI wafers and a thicker gold layer. The impedance tuner has been realized with a single mask fabrication process, hence reducing the overall cost of the device. It utilizes contact-less approach for capacitance tuning thus is free from any stiction, dielectric charging or micro-welding problems of conventional MEMS switches. The proposed device is one of the few MEMS-based impedance tuners that is applicable for use in high power applications.

In summary, the focus of this research has been on the development of monolithically

integrated RF devices using MEMS technology. The fabrication process proposed here enabled the low-cost implementation of variable attenuator and impedance tuner with improved performance and higher level of integration.

7.2 Future Work

There are several research problems related to SOI-based RF MEMS devices that can be possibly explored in the future.

The SOI based fabrication process developed here has a thin metal layer of gold 250 nm. The RF performance of the fabricated devices can be improved if a thickness $>2\,\mu$m can be achieved. This can be done either using gold electroplating or by E-beam deposition using a shadow mask. Moreover, a sidewall coverage of metal is highly desirable in this case. Another scope of improvement is by using a uniform coverage of high dielectric constant material like HfO_2 to achieve higher values of capacitance in the varactor. It will also provide electrical isolation between the dc and RF signal in case the varactor plates touch each other.

The flexibility of monolithic integration provides the possiblity of further expanding the functionality of proposed devices by adding other modules to build intelligent systems on the same chip.

Thesis List of Publications

(*as of April 2019*)

Journal Article

1 **N. K. Khaira**, T. Singh, and R. R. Mansour, "Monolithically Integrated RF MEMS Based Variable Attenuator for Millimeter-Wave Applications," *IEEE Transactions on Microwave Theory and Techniques*, pp. 1–9, 2018. (*under review*)

2 T. Singh, **N. K. Khaira**, and R. R. Mansour, "SOI RF-MEMS Based Monolithically Integrated Reconfigurable Phase Shifter and Impedance Tuner," *IEEE Transactions on Microwave Theory and Techniques*, pp. 1–7, 2019. (*submitted*)

Conference Papers

3 T. Singh, **N. Khaira**, and R. R. Mansour, "Monolithically Integrated Reconfigurable RF MEMS Based Impedance Tuner on SOI Substrate," *in 2019 IEEE MTT-S International Microwave Symposium* (*IMS*), Boston, MA, USA, June 02–07, 2019. pp. 1–3. (*to be presented*)

4 **N. K. Khaira**, T. Singh, and R. R. Mansour, "RF MEMS Based 60 GHz Variable Attenuator," *in Proceedings of the 2018 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications* (*IMWS-AMP*), Ann Arbor, MI, USA, July 16–18, 2018. pp. 1–3.

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