CMOS Electrochemical Camera for Biological Cell Impedance Imaging

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Many biomedical applications require observing the response of biological cells to various stimuli and conditions. Typical optical imaging systems for observing cells require labelling cells with fluorescent molecules. These systems have drawbacks such as limited luminescence time and light-induced damage. However, use of electrochemical based measurement methods overcome these issues. One method, which is label-free and non-invasive, is impedance spectroscopy (IS), which tracks impedance changes caused by variations in cell membrane properties.

This thesis describes the design and experimental characterization of a CMOS electrochemical camera for biological cell impedance imaging. The electrochemical camera is fabricated in a 0.18-μm CMOS technology, and is the first to implement a row-parallel architecture which improves upon spatial-readout efficiency compared to previously published work. Two integrated microelectrode arrays, one containing 17×11 40×40 μm^2 electrodes and the other containing 70×40 10×10 μm^2 electrodes, are implemented. Each array is connected to 84 integrated row-parallel lock-in amplifiers to measure the impedance of live cells on the electrode array surface. A novel lock-in amplifier design allows for an electrode pitch of only 20 μm. The design of a custom bench-top measurement system for characterizing the performance of the CMOS electrochemical camera is also described.

Experimental electronic characterization of the electrochemical camera shows that it can operate from 1 kHz to 1 MHz at a frame rate of 0.0117 Hz, which is sufficient for several cell imaging applications. The measured input-referred noise is 1.08 nA_{rms} with an applied input signal at 600 kHz. Compared to previously reported CMOS electrochemical sensor arrays, the presented work consumes the smallest channel area for the sensor readout electronics with integrated analog-to-digital converter, the lowest power consumption per channel for operating frequencies greater than 100 kHz, and the best area-readout figure of merit.

Acknowledgements

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Abbreviations

ADC analog-to-digital converter ix, xi, 11, 15, 16, 18, 20–22, 36, 39, 40, 42–45, 50, 54, 56, 58, 59, 61, 62, 65, 67–69, 71, 74, 87, 88, 90

BW bandwidth 10, 12–15, 17, 22, 23, 25–27, 29–31, 34, 36–38, 43, 45, 56, 88

CMOS complementary metal-oxide-semiconductor ix, x, 9–11, 14–19, 22, 53, 54, 89

DFF D flip-flop 41, 51, 54, 55

DNA deoxyribonucleic acid 15

DNL differential non-linearity 43

DR dynamic range 12–14, 16, 17, 23, 30, 31, 38, 39, 45, 88

DRAM dynamic random access memory 68

ESD electrostatic discharge 55

FIFO first-in, first-out 68

FOM figure-of-merit 16, 18, 61, 86–88

FPGA field-programmable gate array xii, 62, 64, 68

FSM finite-state machine 68

I/O input/output 49, 55

IC integrated circuit ix, xi, xii, 14, 43, 49, 50, 53–56, 59, 60, 62–65, 68, 69, 76, 80, 83, 88, 89

INL integral non-linearity 43

IS impedance spectroscopy x, 3, 4, 7, 10, 12, 14

LIA lock-in amplifier x–xiii, 11–17, 19–21, 33, 45, 53, 54, 56, 66, 67, 69, 71, 73–77, 80–82, 86, 88–90

LOD limit of detection 14–17, 22, 67, 89

LPF low-pass filter ix–xi, xiii, 13, 15, 16, 21, 26, 29, 31, 33, 36–39, 43–45, 58, 77, 89, 90

LSB least-significant bit 43, 67

MEA microelectrode array 49–51, 58

MIMCAP metal-insulator-metal capacitor 22, 26, 27, 31, 34, 55

MSB most-significant bit 55, 59

NMOS n-channel metal-oxide-semiconductor 26, 31, 32, 43, 54, 65

PCB printed circuit board xii, 62–64, 69, 71, 74, 75, 80, 83, 85, 90

PISO parallel-in serial-out 45, 49, 53, 54

PM phase margin 26, 27

PMOS p-channel metal-oxide-semiconductor xi, 21, 23, 26, 31, 34, 36–38, 43, 44, 54, 65, 90

PSD power spectral density x, xi, 29, 30, 36, 44, 45, 47, 69

SNR signal-to-noise ratio 14, 22

TIA transimpedance amplifier ix–xii, 12, 15–18, 20–30, 32, 34, 36, 38, 43–45, 56, 65, 66, 74, 87

USB Universal Serial Bus 62, 68

V_{LSB} voltage LSB 22, 39, 42, 45

Chapter 1

Background and Motivation

Many biomedical and life science research applications, such as drug screening, require observing biological cells under various stimuli and conditions. This thesis describes the design and experimental characterization of an electrical impedance camera for imaging cells.

1.1 Biological Cell Properties

There are two types of biological cells: eukaryotic and prokaryotic. Prokaryotic cells include bacteria and archaea which contain only ribosomes and a nucleoid. Eukaryotic cells include plants, animals, and fungi and contain multiple interior organelles such as the mitochondria, nucleus, and ribosomes. The typical range of diameter for eukaryotic cells is 10-100 μm, and for prokaryotic cells it is 1-5 μm [2]. For both tpyes of cells, the cell membrane regulates the flow of material into and out of the cell. The membrane is composed of a lipid bilayer and a large quantity of proteins which form channels embedded in the membrane. The thickness of the lipid bilayer is on the order of 7.5-10 nm [3] and the passage through a protein channel has a diameter of a few angstroms [4]. Figure 1.1 shows the physical structure of a cell membrane. The protein channels allow for inorganic ions, nutrients, and other molecules to enter and exit the cell. Additionally, the cell membrane maintains a potential

which provides energy so that ion channels can function. The interior of a cell contains cytoplasm and a nucleus as well as other organelles required for cell functionality [5]. The protein channels are often targeted to deliver drugs into the cell and are observed in drug screening applications. This requires characterizing and monitoring the cell membrane and the cell's internal environment [6].

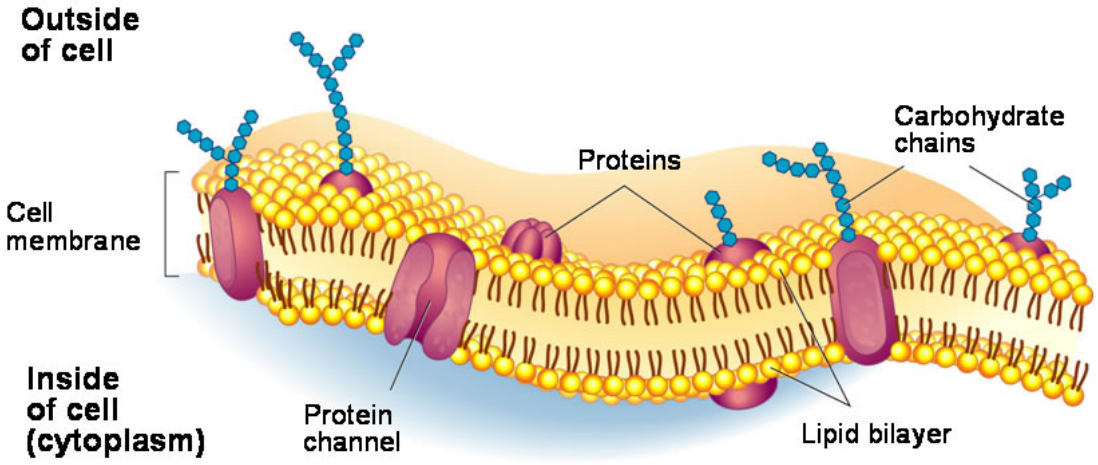


Figure 1.1: Physical structure of a cell membrane [1].

1.2 Optical Monitoring of Cells

Characterizing and monitoring biological cells are widely done not only to observe the effect of new drugs, but also to observe cancer progression, cell growth rate, apoptosis (programmed cell death), cell motility, cell adhesion, and to count cells [7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19]. Optical-based methods that are widely accepted and used for imaging biological cells require molecular labels (such as fluorescent molecules), which are not present in normal cell operation, to generate light when stimulated by a laser beam. The light emitted by the labels is then monitored using an optical setup [20]. One problem with fluorescent molecules is that they are subject to "photobleaching", which renders a flourescent molecule unable to fluoresce and limits the duration of imaging. Another

problem with using fluorescent labels is physical damage to the cell caused by incident light used to excite the labels, which is known as "phototoxicity" [21].

Some optical methods for observing cell apoptosis, such as flow cytometry, require setting up multiple experiments to observe cells at different times. The first set of cells is observed for a certain time period, then the cells are killed and another set of cells of the same type is used to continue the experiment. This type of experiment assumes that the behaviour of the cells in one set of measurements is very similar to cells in another set. This method requires multiple sets of cells and measurement equipment, which are costly and complex. In addition, the duration of any single experiment is limited.

Other optical-based cell measurement methods, such as phase contrast, differential interference constrast, and quantitative phase imaging, have been developed to avoid adding chemicals or excess light and allow for real-time monitoring. Although these techniques are "label-free", they are limited to measuring only thin materials and to observe whole-cell characteristics, such as in cell counting and cell motility measurements. In addition, these label-free methods are still prone to phototoxicity as significant optical power is required [22].

1.3 Electrical Impedance Monitoring of Cells

An alternative method that can characterize cell membrane properties, but does not use light, is electrochemical sensing. Electrochemical sensors characterize cells using electroanalytical techniques. One technique, impedance spectroscopy (IS), is a label-free approach, and, therefore, avoids the problems mentioned in Section 1.2 [23]. Although IS can affect the functionality of the cell when significant voltage potentials are applied across the membrane, when done within the breakdown potential of the membrane, IS is non-invasive [24, 25, 26].

IS measurements are made by applying a small-signal sinusoidal voltage to a reference electrode $V_{app}(t) = A_{app}sin(\omega t + \phi)$, where ω is the angular frequency, A_{app} is the small-signal voltage amplitude and ϕ is the input phase offset, which is often assumed to be zero. The current passing through the cell $I_{meas}(t)$ is captured at a sensing (or "working")

electrode and is given by $I_{meas}(t) = A_{meas}sin(\omega t + \theta)$, where θ is and arbitrary phase shift and A_{meas} is the amplitude [27]. To obtain the impedance $Z_{cell}(j\omega)$, the applied voltage phasor $V_{app} = |A_{app}|e^{j\phi}$ is divided by the measured current phasor $I_{meas} = |A_{meas}|e^{j\theta}$.

1.3.1 Cell Circuit Model

From the impedance spectrum of $Z_{cell}(j\omega)$, a passive electrical model of the cell can be fit to the spectrum. A simple model for characterizing the impedance of a cell uses three passive components as shown in Figure 1.2. The cell is contained in a bath which contains an electrolyte or solution with nutrients required for sustinence. The membrane with its protein channels, charge pumps, and membrane potential is modelled as a capacitor C_m in parallel with a resistor R_m. The cytoplasm and internal organelles are modelled simply as a resistor R_s [12]. Based on this cell model, $Z_{cell}(j\omega)$ is given by

$$Z_{cell}(j\omega) = \frac{V_{app}(j\omega)}{I_{meas}(j\omega)} = \frac{(R_s + R_m)\left(1 + j\omega C_m \left(\frac{R_m R_s}{R_s + R_m}\right)\right)}{1 + j\omega R_m C_m}. \tag{1.1}$$

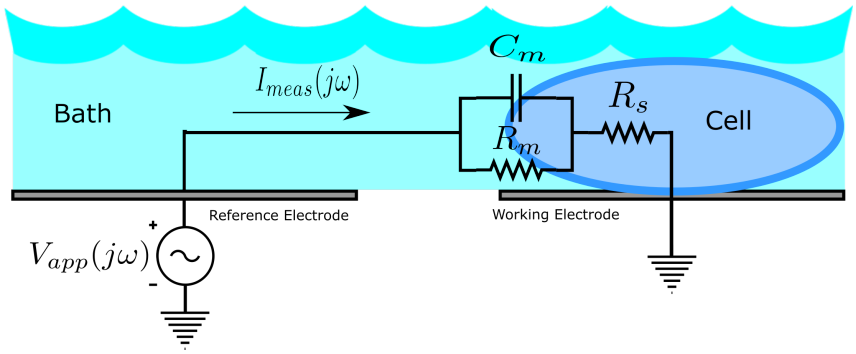


Figure 1.2: Cell IS measurement model.

As the applied voltage is swept across a range of frequencies ω_m, the Nyquist plot shown in Figure 1.3 is observed. The magnitude and phase plots corresponding to the Nyquist plot are shown in Figure 1.4 and 1.5, respectively.

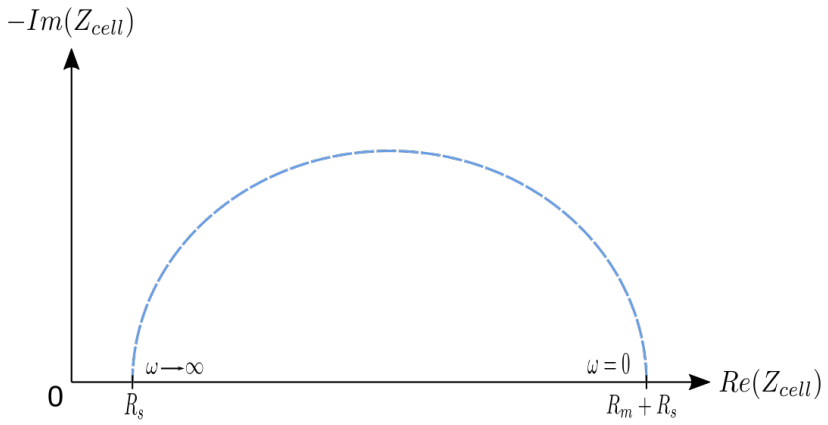


Figure 1.3: Nyquist plot of cell impedance Z_{cell}.

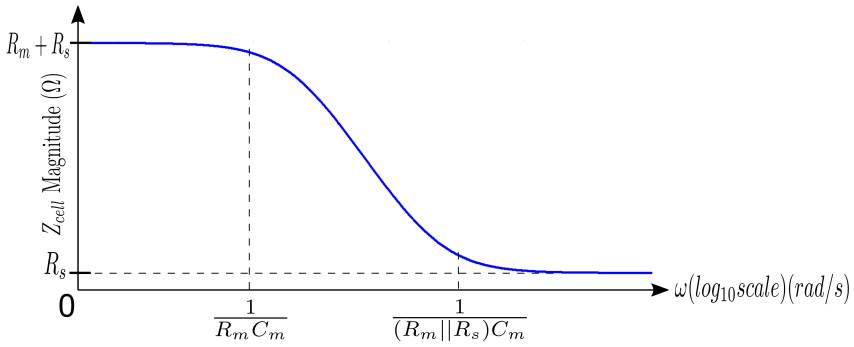


Figure 1.4: Magnitude response of cell impedance Z_{cell}.

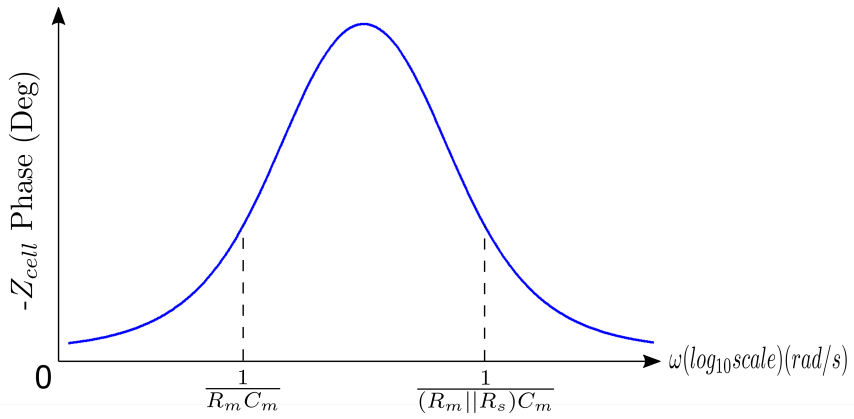


Figure 1.5: Phase response of cell impedance Z_{cell}.

From the Nyquist plot, the values of the electrical components in the cell model can be extracted. These extracted values can then be related to physical information about the cell under study.

Depending on the application, more sophisticated cell models have been developed to represent internal organelles, the membrane voltage, and ion channels. For simplicity, these models are not considered in this thesis [28].

1.3.2 Impedance Interface Model

Due to the measurement interface, the Nyquist plot will not typically match the impedance response shown in Figure 1.3. This is because the electrode-cell-electrode interface usually has some additional parasitics that need to be accounted for. Two major contributing parasitics are double-layer capacitance C_{dl}, electrolyte resistance R_{elec}, and charge transfer resistance R_p. Capacitance C_{dl} arises from the ions in the buffer solution forming a charge build up on the electrode, which can be modelled as a parallel-plate capacitor. Resistance R_{elec} is caused by dissolved ions in the electrolyte [27]. Resistance R_p arises from a leaky C_{dl}. The included parasitics are show in Figure 1.6, and based on this interface model, the total impedance $Z_{tot}(j\omega)$ is given by

$$Z_{tot}(j\omega) = R_s + R_{elec} + \frac{R_m}{j\omega R_m C_m + 1} + \frac{R_p}{j\omega R_p C_{dl} + 1}. \tag{1.2}$$

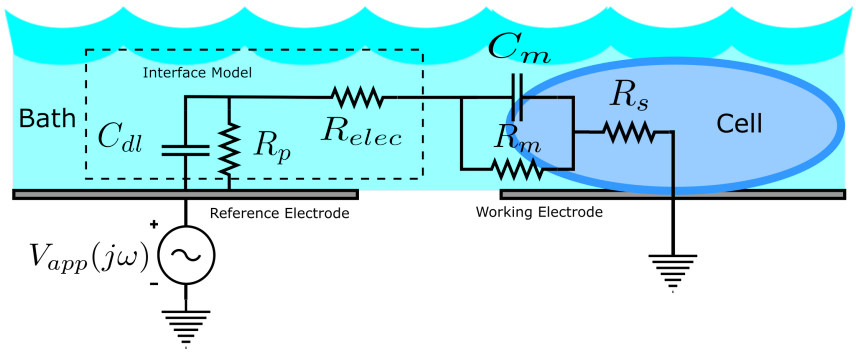


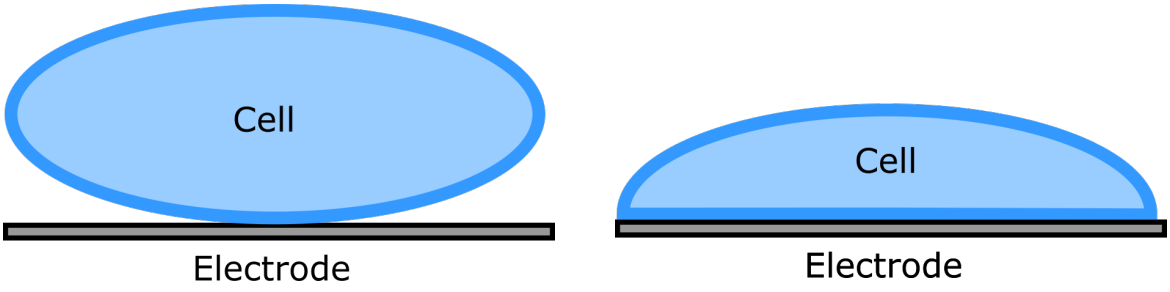
Figure 1.6: Complete cell IS measurement interface model.

There are additional parasitics, such as membrane-electrolyte capacitance and leakage current to other electrodes, that can be accounted for, but these are not considered in this thesis as they are typically insignificant [29]. The interface parasitics strongly depend on the type of interface designed, electrolyte, and platform being used.

1.4 Cell Impedance Measurement Applications

1.4.1 Cell Adhesion

One application of cell impedance measurment is in cell adhesion studies, which is shown in Figure 1.7, where a cell, initially floating in a bath (pre-adhesion), attaches to a physical structure such as an electrode (post-adhesion). Cell adhesion information can be used in cell migration studies, which is done to study cancer. Reference [10] demonstrates that cell adhesion can be monitored via impedance magnitude, and when cell detachment occurs, an impedance magnitude decrease on the order of a few hundred kΩ can be observed in as short a time as eight minutes. This is caused by the electrode not being fully covered by the cell which leads to a low-resistance path through the electrolyte.



(a) (b)

Figure 1.7: A cell (a) before adhesion to an electrode and (b) after adhesion.

1.4.2 Apoptosis

Another application is monitoring changes in cell membrane capacitance caused by induced apoptosis. Reference [30] has shown that changes in membrane capacitance from genistein induced apoptosis is on the order of 8 $\frac{nF}{mm^2}$. Typically, a change in the membrane capacitance can be observed after two hours.

1.4.3 Wound Healing and Cell Migration

To study cell migration a wound can be afflicted on to a plate of cells via mechanically induced damage. However, this approach does not produce a well controlled wound size. An alternative strategy is to use an electrical pulse to damage the cells via an electrode which results in a more controlled wound size. Additionally, the electrode interface can be used to monitor the cells as they migrate to close the wound [31]. In the case of reference [31], a change in impedance of 8 kΩ is observed over a period of several hours.

1.4.4 Drug Screening

Analysing the effects of drugs can also be done using impedance based measurements. In the study done in [32], the effect of various concentrations of the drug cisplatin was

observed over tens of hours, and a minimum impedance change of 20 kΩ was observed from a control.

1.5 Impedance Measurement Structures

Two types of measurement structures are typically chosen for characterizing cells with impedance sensors: integrated complementary metal-oxide-semiconductor (CMOS) sensor arrays and custom measurement structures.

1.5.1 Non-integrated Measurement Platforms

Non-integrated measurement platforms involve the design of unique micro/nano-scale structures and electrodes which utilize off-the-shelf impedance analyzers for signal processing [33]. This custom approach has the advantage of more design choices for the electrode-cell interface. The custom measurement structure reported in [34] uses electrodes to trap a cell and analyse its impedance. The design accomplishes this by using a set of electrodes (quadrupole) to manipulate and move the cell into a set of electrodes for impedance measurement.

Non-integrated designs can utilize common fabrication materials and processes for the sensor as they are not limited to a particular technology process. A disadvantage of this approach is that the signal processing circuits are located far from the electrode interface, which could result in higher interference coupling into the measured signal. Additionally, this platform is limited to simultaneously measuring only as many cells as there are unique measurement channels. Performing simultaneous measurements on multiple cells therefore becomes costly as the number of external measurement channels becomes impractically large.

1.5.2 CMOS Impedance Cameras

Analogous to optical digital cameras that measure light intensity using an integrated pixel sensor array, CMOS electrochemical cameras record electrochemical impedance changes sensed by an array of integrated electrodes. CMOS impedance cameras overcome the interference and simultaneous cell measurement problems characteristic of non-integrated measurement platforms by having the processing circuitry integrated on the same physical substrate as the electrodes. This allows for an amplifier to be placed physically closer to the electrode interface than an external amplifier, reducing parasitics which increases bandwidth (BW) and decreases external interference.

To read out impedance from multiple cells or electrodes quickly, the sensor array's architecture typically consists of an active area that contains the electrodes and additional processing circuitry (acquisition channel). These circuits reside within a column of an array of pixels to read out electrodes in the selected column. This architecture, shown in Figure 1.8, is similar to a CMOS visible-light imager camera and is also known as a "row-parallel architecture". It enables read out of multiple electrodes, and hence, multiple cells simultaneously without requiring external measurement equipment. The row-parallel architecture functions using an image capture method known as "raster scan" which works by reading out all rows in a single column and then scanning across each column to obtain the signal from all electrodes. This approach provides a high frame rate for the system, which allows for real-time monitoring. Typically, the acquisition channel layout is designed to fit within the vertical pitch (center-to-center spacing) of the electrodes, as shown in Figure 1.8. However, for small electrode sizes, it can be difficult to keep acquisition circuits within the given vertical pitch.

The cell-electrode interface is typically designed using the technology process with post-processing to make it compatible with the biological material. The electrodes are typically plated with a noble metal like gold to prevent them from oxidizing or reacting with the cells or electrolyte. With these advantages, CMOS electrochemical sensor arrays are being developed and researched for use in biological IS measurements [10, 27, 35, 36].

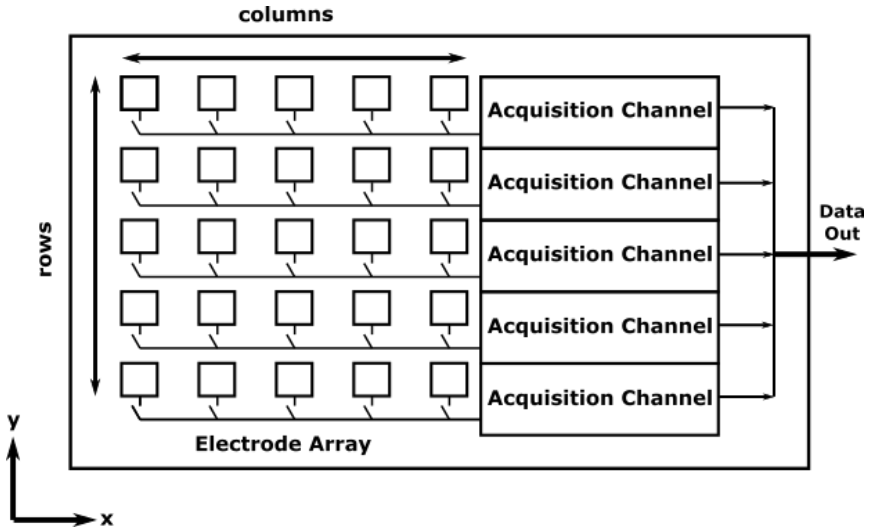


Figure 1.8: CMOS camera architecture.

1.6 CMOS Impedance Camera Circuits and Performance Parameters

Circuits and performance specifications for implementing CMOS electrochemical cameras for impedance sensing will now be described.

1.6.1 Lock-in Amplifier

A commonly used circuit for impedance measurement is the lock-in amplifier (LIA). An LIA is also referred to as a "direct-conversion receiver" [27] and, in its basic form, is built as shown in Figure 1.9. The analog output of the lock-in amplifier is captured by an analog-to-digital converter (ADC) so that it can be processed by a computer. In this case one ADC samples both the in-phase and quadrature components.

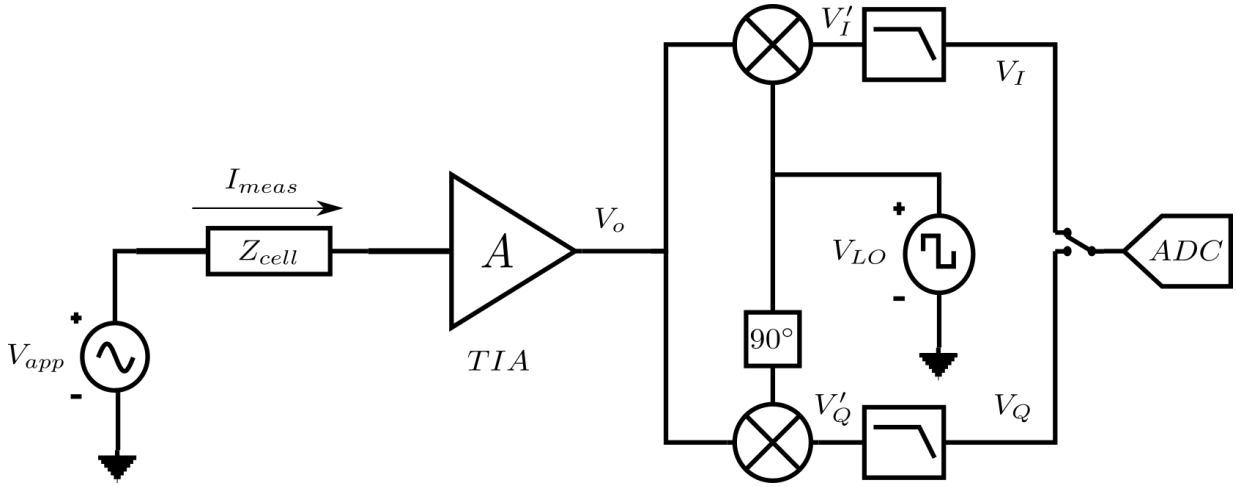


Figure 1.9: General LIA architecture.

This architecture yields high BW, low noise, and high dynamic range (DR). The operation of an LIA for IS is done by applying a wideband signal V_{app} across Z_{cell}. The resulting current I_{meas} is then amplified by a transimpedance amplifier (TIA) with gain A. The resulting output V_o is then multiplied by $V_{LO} = sin(\omega t)$, which has the same frequency and phase as V_{app} and unity amplitude. The result gives the in-phase (V_I') component of V_o. To get the quadrature (V_Q') component of the current through the cell, V_{LO} is shifted by 90° before being multiplied. Mathematically, the operation of the LIA is given by

$$V_I' = A_{meas} \cdot sin(\omega t + \theta) \cdot sin_{V_{LO}}(\omega t) = \frac{A_{meas}}{2} \cdot [cos(\theta) + cos(2\omega t + \theta)] \tag{1.3}$$

$$V_Q' = A_{meas} \cdot sin(\omega t + \theta) \cdot cos_{V_{LO}}(\omega t) = \frac{A_{meas}}{2} \cdot [sin(\theta) + sin(2\omega t + \theta)]\,, \tag{1.4}$$

where A_{meas} is the gain from I_{meas} to V_Q' and V_I'. As the equations show, V_I' and V_Q' have components at dc and at two times the frequency of the input. The output is also scaled by a factor $\frac{1}{2}$ and exhibits a phase shift θ, which is determined by Z_{cell}. In the case where V_{LO} is a square wave, the scaling factor $\frac{1}{2}$ becomes $\frac{2}{\pi}$ and additional higher order frequency components are introduced. The dc component of V_I' and V_Q' is obtained at the output of

the low-pass filter (LPF) in the LIA. The in-phase and quadrature filtered outputs V_I and V_Q, respectively, are only dependent on the phase of the signal as given by

$$V_I = A_{sys} \cdot cos(\theta) \tag{1.5}$$

$$V_Q = A_{sys} \cdot sin(\theta), \tag{1.6}$$

where A_{sys} is the gain from I_{meas} to V_Q or V_I. The magnitude of the cell impedance $|Z_{cell}|$ is given by

$$\mid Z_{cell}(j\omega) \mid = \frac{|V_{app}| \cdot |A_{sys}|}{\sqrt{V_I^2 + V_Q^2}}. \tag{1.7}$$

The phase of Z_{cell} is given by

$$\angle Z_{cell}(j\omega) = tan^{-1}\left(\frac{V_Q}{V_I}\right). \tag{1.8}$$

The high BW and DR of LIAs is a result of the amplifier and mixer front-end which exhibit these properties. Low noise is a result of being able to filter the incoming spectrum down to low frequencies, which attenuates noise [10, 27, 35, 36].

1.6.2 Performance Parameters

The key electrical specifications for the LIA and impedance camera are summarized in the following list. Each of these parameters arise from a biological or physical property of a cell.

- **Electrode Size** refers to the x and y dimensions of the electrodes. These determine the number of cells that reside on the electrode surface and in-between electrodes. In order to measure single cells, the electrode dimensions should be less than 10 μm [37].

- **Electrode Pitch** is the distance between adjacent electrode centres and determines the spatial resolution of the camera.
- **Array Size (Number of Electrodes):** determines the total number of cells that can be imaged.
- **Power Consumption** is related to heat dissipation of the camera integrated circuit (IC), which can affect the state of the cells but is not often addressed in the literature.
- **Dynamic Range (DR)** determines the impedance range that can be measured. A typical DR extends from about 1 kΩ to 10 MΩ (i.e, the DR is 80 dB [34, 38].
- **Bandwidth (BW)** refers to frequency range over which the LIA is operational. It therefore determines the smallest C_m and C_{dl} that can be measured. Typical C_{dl} densities are on the order of 20-40 $\frac{\mu F}{cm^2}$ and C_m densities are on the order of 1 $\frac{\mu F}{cm^2}$. Based on electrode sizes of tens of micrometers, the expected C_{dl} is on the order of tens of picofarads. For typical cell sizes of tens of micrometers in diameter, the expected C_m is on the order of nanofarads. C_{dl} is dependent on the electrolyte used and C_m on the cell type. [34, 17, 27, 38].
- **Limit of Detection (LOD)** determines the largest impedance (smallest I_{meas}) that can be measured at a signal-to-noise ratio (SNR) of 0 dB, which, for this application, is 10 MΩ [34, 38].
- **Frame Rate** is the rate at which all the electrodes in the CMOS camera can be read out. It determines the minimum period during which a cell physical property can change and be observed. Typical drug screening assays have observsation times from tens of minutes to hours [39].

Another parameter that is important to cell measurement is the maximum voltage that can be applied across a cell. This potential should be less than 200 mV_{pk} so that cell operation is affacted only negligibly [24, 25, 26]. The specifications for the IS camera that are most important are limit of detection (LOD) and BW as these determine the range of component values that can be detected.

1.7 Summary of Previous Work in CMOS Impedance Cameras

Previous CMOS electrochemical sensor arrays based on the LIA architecture have a broad range of applications. The list below highlights some of the advantages and disadvantages of previous work and the proposed work in this thesis.

- **Manickam et al., [27]:** In this work, a system is built to measure biological analytes (such as deoxyribonucleic acid (DNA)). It implements an analog front end which comprises of a TIA and mixer to capture in-phase and quadrature components. However, it does not include an integrated filter or ADC. The large external LPF capacitors yield low $\frac{kT}{C}$ noise and do not occupy chip area. Additionally, there is only one external ADC which is used to obtain samples from all electrodes. This yields a linear increase in system readout time versus the number of electrodes. Manickam also does not allow for simultaneous cell impedance measurements.

- **Liu et al. [35]:** This work implements a lock-in amplifier architecture with a counter to convert the analog in-phase and quadrature components. The lock-in amplifier is implemented with an analog multiplier and integrator. It has better performance than work in this thesis in terms of LOD and power. This, however, comes at a trade-off with BW which for this application is not sufficient. The target application of Liu's work does not require a high bandwidth.

- **Jafari et al. [36]:** This work implements a frequency response analysis algorithm to extract the in-phase and quadrature components. It does this by using a integrator and dual-slope multiplying ADCs. It has better performance compared to work in this thesis in terms of LOD and power. This, however, comes at a trade-off with BW. The target application of Jafari's work does not require a high bandwidth.

- **Chi et al. [10]:** This work shows few electronic characterization results, but uses an I/Q architecture, which is implemented as an integrator and double balanced mixer. Chi's work has experimental results which observes the adhesion of cells. It also does not describe an integrated ADC.

- **Viswam et al.** [40]**:** This work is the most advanced compared to the other four, and was published after the design in this thesis was in progress. It implements a lock-in amplifier using a multi-mode TIA and passive mixer. It also contains an on-chip delta-sigma ADC. This work has a high DR and low LOD. The high DR is only achieved through 2-mode operation where the gain of the TIA is varied and the power supply voltage is 3.3 V. One mode has 80 dB and another 40 dB. Additionally, a LPF filter capacitance of 10 pF would at least increase the input-referred noise of the channel to approximately 23 pA. Viswam's work can only read out 32 electrodes at one time, which is significantly lower than the number of rows in the system and yields a low frame rate.

1.8 Proposed Work

The objectives of the proposed work are to build a CMOS impedance camera with improved scalability and frame rate compared to existing work. A way to improve these parameters is to have one channel per row. This has better scalability when it comes to increasing the total number of electrodes in the camera. This architecture also helps to reduce the increase in frame rate as the number of electrodes increases. Additionally, having a small acquisition channel size to fit within a pixel pitch gives better area efficiency, as the electrodes occupy a higher percentage of the the overall chip area. The channel area is specified at 0.02 mm^2 to improve upon existing work. Because of these design considerations, this architecture results in a high area-readout figure-of-merit (FOM) compared to previous work, which is given by

$$FOM = \frac{d \cdot N_{chan}}{N_e}, \tag{1.9}$$

where d is the electrode density and $d^{-1} = P_x P_y$, where P_x and P_y is the electrode pitch in the x and y directions, respectively), and N_e and N_{chan} are the total number of imager electrodes and readout channels, respectively. A high FOM describes an imager with high spatial resolution (large d) and the ability to acquire signals from all electrodes simultaneously ($\frac{N_e}{N_{chan}} = 1$). The LIA design specifications are now summarized.

In order to get a starting design point for the LIA, a peak amplitude for the applied input signal voltage must first be chosen, which is less than 200 mV_{pk} to avoid causing damage to the cell. Therefore, a voltage of 10 mV_{pk} is selected to provide adequate margin. Using the largest $|Z_{cell}|$ of 10 MΩ, a current LOD of at least 1 nA is required. The smallest $|Z_{cell}|$ of 1 kΩ has a current of 10 μA, which yields a DR of 80 dB. To obtain the required BW, the smallest expected C_m needs to be considered. A 10x10 μm^2 electrode is the size required to obtain single cell resolution. Using this electrode size and adding some margin results in C_{dl} = 500 fF. The other expected capacitance and resistances are chosen based on values from literature: R_p = 5 GΩ, C_m = 500 pF, and $R_{elec} = R_m$ = 1 kΩ. Then the cell measurement interface model, which is given by (1.2), is used to obtain an impedance spectrum. After this, (1.2) is solved to find the required frequency to obtain enough samples to detect the pole of the impedance caused by $(R_m C_m)^{-1}$ for both real and imaginary components. This frequency is approximately 350 kHz for the given values. To give adequate margin, the BW of the TIA is selected to be 1 MHz.

The specification for the number of electrodes is determined by the physical space on the multi-project wafer provided by CMC Microsystems. The available targeted chip size is 3×2.5 mm^2, which results in 187 40×40 μm^2 electrodes, 2800 10×10 μm^2 electrodes and 84 acquisition channels. The frame rate should be on the order of 10 min or less to adequately capture cell behaviour. The CMOS technology chosen for this design is 0.18 μm. The final LIA specification, which is not clearly defined by cell properties, includes acquisition channel power. The targeted power per acqusition channel, is selected to be 300 μW in order to improve upon existing work. This improvement is obtained using the current consumption of [27] at a 1.8 V supply instead of 3.3 V. Table 1.1 summarizes the results of previous works on CMOS sensor arrays and the target specifications for this work.

Reference	Manickam [27]	Jafari [36]	Liu [35]	Chi [10]	Viswam [40]	Proposed Work
Architecture	TIA + Direct I/Q	SC TIA + Multiplying ADC	Lock-in + Counter	Direct I/Q	Lock-in + ΣΔ	Lock-in + Ramp ADC
On chip LPF + ADC	No	Yes	Yes	No	Yes	Yes
Frequency Range	10 Hz-50 MHz	0.1 Hz-10 kHz	1 mHz-10 kHz	500 kHz-4 MHz	1 Hz-1 MHz	1 kHz-1 MHz
Dynamic Range (dB)	97	140 (3 mode)	80 (multi mode)	-	102	80
Channel Power (μW)	726	42	5.2	-	412	300
Electrode Size (μm^2)	40×40	55×55	100 dia	80×100	3.5x7 & 605×605	10×10 & 40×40
Electrode pitch (μm)	100	300	-	-	13.5	20
No. of Electrodes	100	64	100	16	59760	2987
Input-Referred Noise	330 pA	320 fF	100 fA	-	6.4 pA	1 nA
Number of Channels	1	16	26	16	32	84
Channel Area (mm^2)	0.01	0.06	0.045	-	0.1	0.02
Die Size (mm)	2×2	1.05×1.6	3×3	2.2×2.0	12×8.9	3×2.5
Frame Rate(Hz)	0.9	-	-	-	0.000568	0.0117
Technology (μm)	0.35	0.13	0.5	0.13	0.18	0.18
FOM (mm^{-2})	1	2.8	-	-	2.9	36

Table 1.1: Previous published work in CMOS electrochemical cameras and target specification for work in this thesis.

1.9 Thesis Organization

This thesis describes a novel CMOS electrochemical camera for cell-impedance imaging and is organized as follows:

- **Chapter 2** begins by describing the design choices for the LIA used in the proposed CMOS impedance camera and then proceeds to describe the design, analysis, and optimization of the transistor level implementation.
- **Chapter 3** describes the physical layout and system architecture of the proposed CMOS impedance camera.
- **Chapter 4** describes the characterization setup and discusses the measured electronic performance of the proposed CMOS impedance camera.
- **Chapter 5** concludes the thesis with a brief summary and discusses future work.

Chapter 2

Lock-In Amplifier Design

This chapter focuses on the design of the acquisition channel containing the LIA. It begins by outlining the design choices for the LIA architecture. Then the design of the TIA, mixer, filter and ADC are explained. The chapter concludes with the LIA simulation results.

2.1 Implemented LIA Architecture

The LIA architecture shown in Figure 2.1 required several design decisions to meet the specifications. The differences between the architecture in Figure 2.1 and the one in Figure 1.9 is that the mixers are differential and two ADCs are used to sample the differential output.

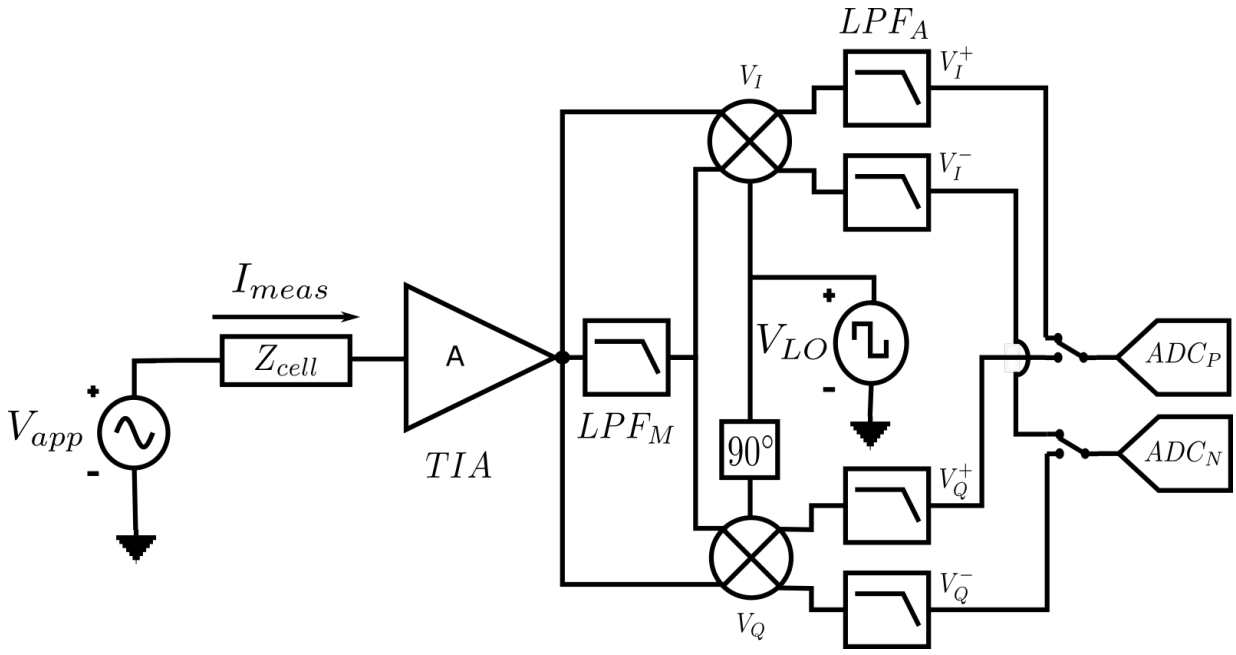


Figure 2.1: Implemented LIA architecture.

Having a differential TIA and electrodes would occupy significant space in an already small electrode pitch size, making routing next to impossible. As such, a single ended TIA is implemented. Using four ADCs (one each to sample V_Q^+, V_Q^-, V_I^+, and V_I^-) was considered to reduce read out time, but due to physical area constraints, only two were implemented. As a result, one ADC is dedicated to sampling V_Q^+ and V_I^+, and the other is dedicated to sampling V_Q^- and V_I^-. This design choice doubles the sampling time compared to the case where four ADCs are implemented. In addition, the ADC input can be switched between the mixer output and the output of LPF_A. This allows the mixer output can be directly characterized for test purposes.

To derive the design specifications for each circuit block, a few preliminary parameters must be known. The passive LPF_M and LPF_A circuits use a capacitor and weak-inversion p-channel metal-oxide-semiconductor (PMOS) transistors as resistors, which occupy little chip area compared to polysilicon resistors. The LPF_A capacitor C_f is an important design parameter because it impacts the input-referred noise current and area requirements of the LIA. It also affects the frame rate of the system as the filter requires sufficient time to

settle at each input frequency. Since metal-insulator-metal capacitor (MIMCAP) in the implemented CMOS process have densities of 1.06 $\frac{fF}{\mu m^2}$, we chose C_f = 1 pF so that four capacitors for each of the two mixers could fit in the LIA area allocation of 0.02 mm^2. The average noise voltage at the filter output is $\sqrt{\frac{kT}{C_f}} = 65\ \mu V_{rms}$, where k is Boltzmann's constant and T is absolute temperature, at T =300 K. A system single-ended gain of 65 kΩ is required to reduce the input-referred noise to 1 nA_{rms} as there is a capacitor at V_Q^+, V_Q^-, V_I^+, and V_I^-. For the calculated A_{sys}, the system output swing for a maximum input current of 10 μA_p is 1.28 V_{pp}. This is the required system gain, which is scaled by $\frac{2}{\pi}$ from the mixer output and would result in a required mixer output swing of 2 V_{pp}. This clearly is not feasible when using a 1.8 V supply. To mitigate this problem, sample averaging can be applied to reduce the noise which, in turn reduces the required transimpedance. The ADC can average the noise contribution from the capacitor and from a 1.8 V reference at a resolution of 16 bits, a voltage LSB (V_{LSB}) of 27.5 μV. The ADC quantization noise is $\frac{V_{LSB}}{\sqrt{12}}$ = 7.94 μV_{rms} [41]. Clearly the limiting factor is V_{LSB}, and hence, averaging is required to obtain a resolution of 27.5 μV. This approximately halves the A_{sys} gain requirement to about 30 kΩ and yields a maximum mixer output swing of 0.94 V_{pp}.

To be comparable to [27] and to meet the frame rate specification, the settling time of the filter for 16-bit settling accuracy is approximately 1.1 s with a filter BW of 10 Hz. Averaging increases the frame rate, but ideally scales the SNR by a factor of $\sqrt{N}$, where N is the number of samples averaged [42]. For an input current of 1 nA_p, the estimated SNR is -7.8 dB. To meet the LOD specification (A_{meas} at which SNR = 1 or 0 dB), the minimum number of samples required to average is five. In addition, the ADC sampling rate needs to be at least 20 Hz to capture frequencies within the filter BW.

A decision was also made to use an external signal generator for V_{app} and V_{LO} in order to allow for more flexibility in the signal parameters. The following sections describe the design of the TIA, mixer, filter, and ADC.

2.2 TIA Design

The TIA must be designed to meet the specifications shown in Table 2.1.

Parameter	Specification
Potential across the cell	<200 mV_p
DR	80 dB
BW	>50 MHz
R_{in}	<100 Ω
DC gain R_{TIA}	32 kΩ
Current consumption	<55 μA
Input-referred noise	<500 pA_{rms}

Table 2.1: TIA specifications.

To implement a controlled voltage for fixing the potential across a cell, a virtual ground must be established which requires at least a differential pair as the basis of the amplifier. The input resistance R_{in} to the amplifier must also be less than 100 Ω over the BW to capture the current passing through the cells. A single differential pair is insufficient to provide a low R_{in}. Therefore, a modified version of the circuit proposed in [27] is used instead. The circuit is shown in Figure 2.2 is a bootstrapped current buffer. The use of a current buffer keeps R_{in} of the TIA small.

To enhance output swing, a linear resistor R_{TIA} is used instead of a diode-connected PMOS as in [27]. Use of R_{TIA} also increases the linearity of the TIA. The drawback is that R_{TIA} could vary by ±10% from the pre-fabricated value. This, however, is not a problem in the proposed application as each channel can be calibrated. The actual transistor implementation of the circuit in Figure 2.2 is shown in Figure 2.3. Component geometries and bias points are shown in Table 2.2.

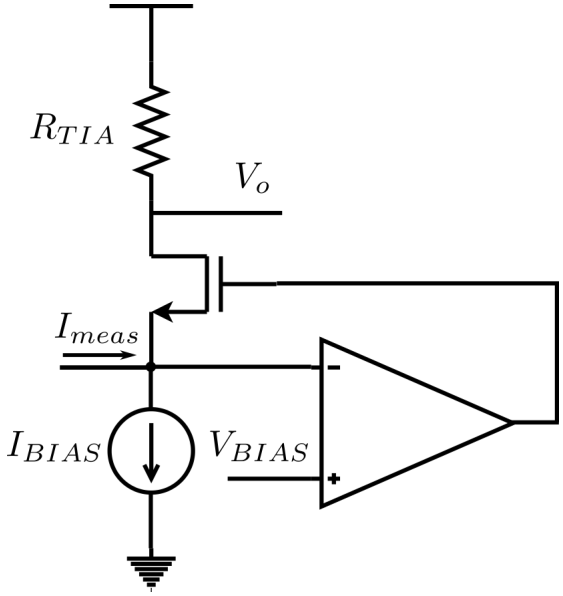


Figure 2.2: TIA architecture.

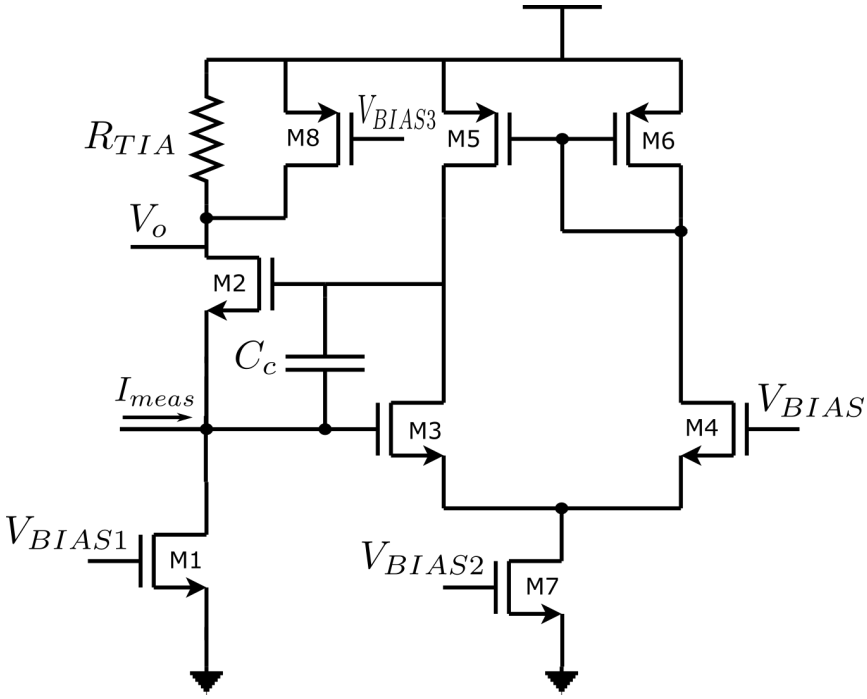


Figure 2.3: TIA circuit.

Component	W (μm)	L (nm)	$\lvert I_D \rvert$ (μA)	$\lvert V_{GS} \rvert$ (V)	Value
M1	100	720	13	0.405	-
M2	25	180	13	0.604	-
M3 & M4	30	540	20	0.530	-
M5 & M6	50	360	20	0.487	-
M7	40	540	40	0.500	-
M8	25	540	-	-	-
R_{TIA}	-	-	-	-	31.95 kΩ
C	-	-	-	-	326.9 fF

Table 2.2: Transistor geometries, component values, and bias points of the TIA.

The current buffer and bias devices, which are transistors M1 and M2, respectively, need to remain in saturation over the the specified BW and gain. Starting with an initial overdrive voltage of 0.175 V for the differential pair (diff pair), the resulting gate bias point for M3 is 0.75 V. The maximum input swing is 20 μA_{pp} at 1 kΩ source impedance and the maximum input swing is determined by the drain current of M1 (I_{D1}), as M2 will turn off when the amplitude of the input current exceeds I_{D1}. To give some margin, I_{D1} is designed to be 13 μA. This also leads to a maximum input current of 23 μA_p being passed through M2. To obtain a 1-V swing at the output, a maximum R_{TIA} value of 34.2 kΩ is allowed within a given tolerance of $\pm 10\%$. To provide some additional margin, R_{TIA} is selected to be 32 kΩ. R_{in} of the TIA is given approximately by

$$R_{in} \approx \frac{1}{|A_{diff}|} \left(\frac{1}{g_{m2}} + \frac{R_{TIA}}{g_{m2} r_{o2}} \right), \tag{2.1}$$

where A_{diff} is the dc gain of the diff pair, g_m is the small-signal transconductance of a transistor, and r_o is the output resistance of a transistor. Therefore, to keep R_{in} small, the channel length of the transistor must be minimized to make g_{m2} large. In addition, M2 has its input resistance reduced by the gain of the differential pair. As such, R_{in} of the current buffer without feedback can be set higher than required. To achieve $R_{in} = 1$ kΩ, a width of 25 μm for M2 is necessary. The differential pair with active load (transistors M5 and M6) was designed to meet an output dc operating point of 1.325 V and a gain of

$\sim$100 V/V to achieve an $R_{in} = 10\ \Omega$. This is much less than 100 Ω, or 10% of the smallest source resistance expected.

The diff pair design starts with determining the parameters for the gain specification, which is given by

$$|A_{diff}| = g_{m3}\left(r_{o3}//r_{o5}\right) = \frac{2I_{D3}}{V_{ov3}}\left(\frac{L_3}{\lambda_N I_{D3}}//\frac{L_5}{|\lambda_P| I_{D5}}\right), \tag{2.2}$$

where V_{ov} is the overdrive voltage, L is the transistor channel length, and λ_N and λ_P are the channel-length modulation parameters for n-channel metal-oxide-semiconductor (NMOS) and PMOS transistors, respectively. To get the design started, I_{D7} is chosen to be 42 μA to meet the estimated power requirements. Transconductance g_{m3} is then approximately 240 μS. To achieve A_{diff} of 100 V/V, the required $ro_3 \approx ro_5 = 830$ kΩ. Using the extracted λ values, the required L for M3 and M4 is 600 nm and for M5 and M6 is 390 nm. To keep the transistors in saturation, W of these devices are set to 30 μm and 50 μm, respectively, and the lengths are decreased to 540 nm and 360 nm, respectively. The resulting BW is 2 MHz and A_{diff} is 76.4 V/V. Although this is less than originally designed for, the result is $R_{in} = 70\Omega$ which still meets the R_{in} specification. Upon analysing the loop gain of the complete circuit, it was found that the phase margin (PM) was less than 60°. To compensate for this, a 326.7 fF MIMCAP C_c is placed between the gate of M3 and the input of the TIA. The MIMCAP value was determined by sweeping worst case MIMCAP value over corners.

The worst case noise of the TIA that falls within the output LPF BW is the flicker noise at 1 kHz and below. The most significant noise contributor is M1 as its 1/f and thermal noise currents are injected directly into the input node. The output noise of the diff pair is negligible comapred to M1, as it undergoes small gain when referred to the TIA input branch and M2 is a cascode transistor which also contributes insignificant noise [27]. The area of M1 is increased until the noise contribution from M1 is comparable with noise contribution from M3. Length L_1 is chosen to yield r_{o1} greater than 1 MΩ, so that less than 0.01% of I_{meas} is captured by M1.

2.2.1 TIA Simulation Results

All circuits presented in this thesis are simulated using the Cadence Spectre^{TM} simulator. The simulated -3 dB BW of the TIA is 56 MHz, which provides a phase shift of less than 1.7° at frequencies of 1 MHz and lower. Figure 2.4 shows the simulated TIA gain (magnitude response) versus frequency.

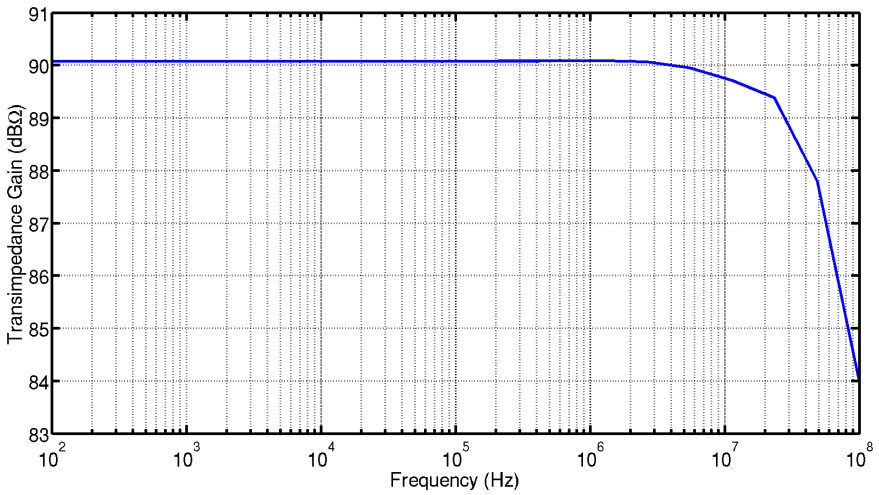


Figure 2.4: Simulated TIA gain versus frequency.

The simulated transimpedance gain versus source impedance is shown in Figure 2.5. As seen in the figure, the TIA maintains stable gain of approximately 90 dBΩ (32 kΩ) with less than 0.002 dB ripple over the range of impedances to be measured.

The simulated magnitude and phase response of the TIA loop transfer is shown in Figure 2.6. The PM is 71° for nominal MIMCAP value with an infinite source impedance. Adding a finite source impedance increases the PM. In the case of infinite source impedance, the dominant pole ω_p of the loop transfer is approximately given by

$$\omega_p \approx \frac{1}{r_{o3}//r_{o5}\left(C_c + C_{gs2} + C_{gd3} + C_{gd5}\right)}, \tag{2.3}$$

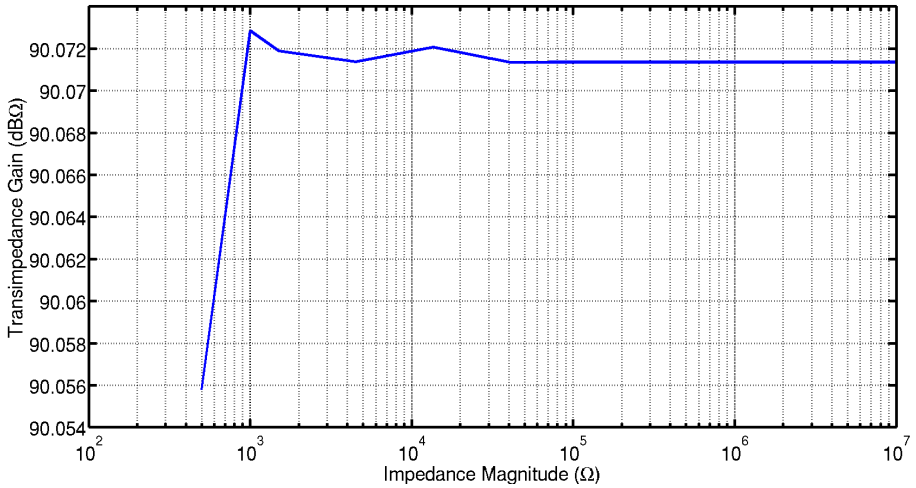


Figure 2.5: Simulated TIA gain versus source impedance magnitude.

where C_{gs} is transistor total gate-to-source capacitance and C_{gd} is total gate-to-drain capacitance.

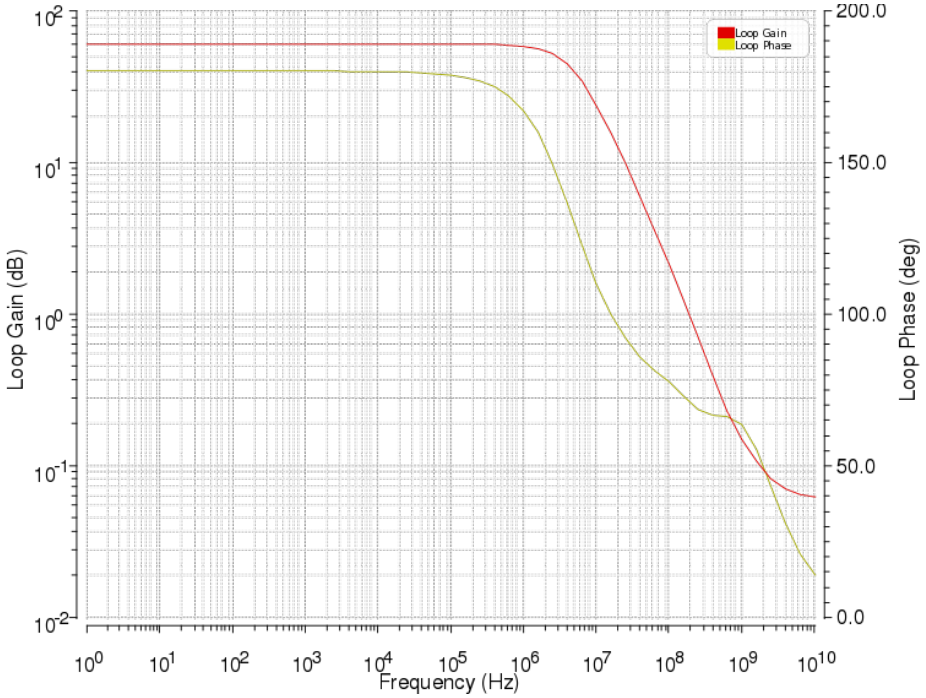


Figure 2.6: Simulated TIA loop transfer magnitude and phase.

The input-referred current noise power spectral density (PSD) of the TIA is shown in Figure 2.7. The average noise power is 326 pA_{rms} over a BW from 900 to 1100 Hz. This BW is the double side-band noise at the output of the LPF at the lowest input frequency, which is 1 kHz with an LPF_A BW of 100 Hz (the specification for the LPF_A BW is only 10 Hz, analysing noise at 100 Hz bandwidth gives some margin).

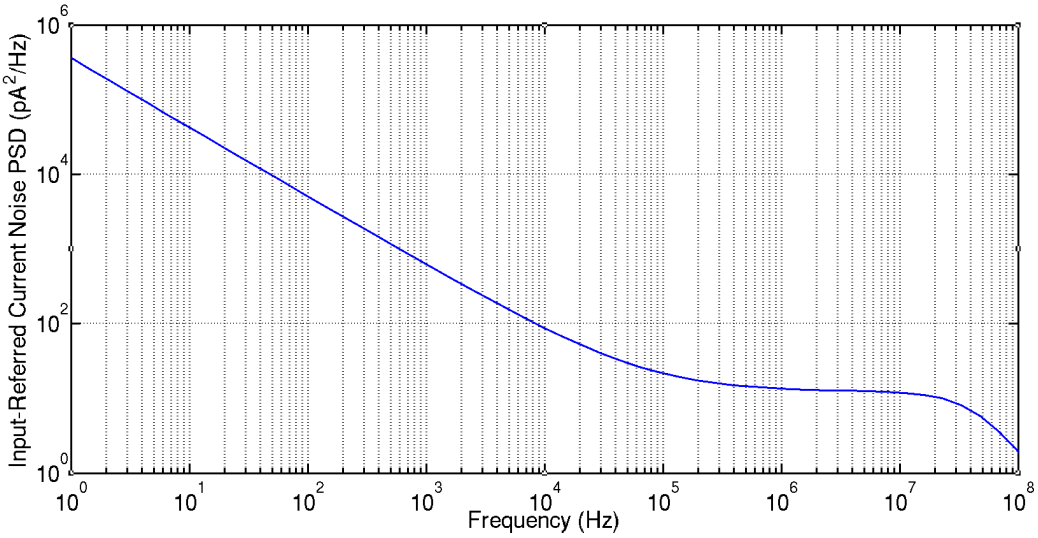


Figure 2.7: Simulated TIA input-referred current noise PSD.

The TIA simulation results are summarized in Table 2.3.

Parameter	Specification	Simulation Result
Potential across the cell	<200 mV_p	N/A
DR	80 dB	80 dB
BW	>50 MHz	56 MHz
R_{in}	<100 Ω	70 Ω
DC gain R_{TIA}	32 kΩ	32 kΩ
Current consumption	<55 μA	53 μA
Input-referred noise (900-1100 Hz BW)	<500 pA_{rms}	326 pA_{rms}

Table 2.3: Summary of TIA simulation results.

2.3 Mixer Design

The mixer and LPF_M must be designed to meet the specifications shown in Table 2.4.

Parameter	Specification
DR	80 dB
BW	>50 MHz
Gain	5.5 dB
LPF BW	<100 Hz
Current consumption	<27.5 μA
Input-referred noise at TIA input	<1 nA_{rms}

Table 2.4: Mixer specifications.

The LPF_M is implemented using weak-inversion PMOS transistors and a MIMCAP, as shown in Figure 2.8. Component geometries are shown in Table 2.5. Using PMOS devices is required as the body of NMOS devices are connected to the substrate in this technology. Because weak-inversion PMOS transistors are used instead of passive resistors, which allows for a large resistance to be integrated without occupying a large area. However, this resistance is non-linear with respect to frequency.

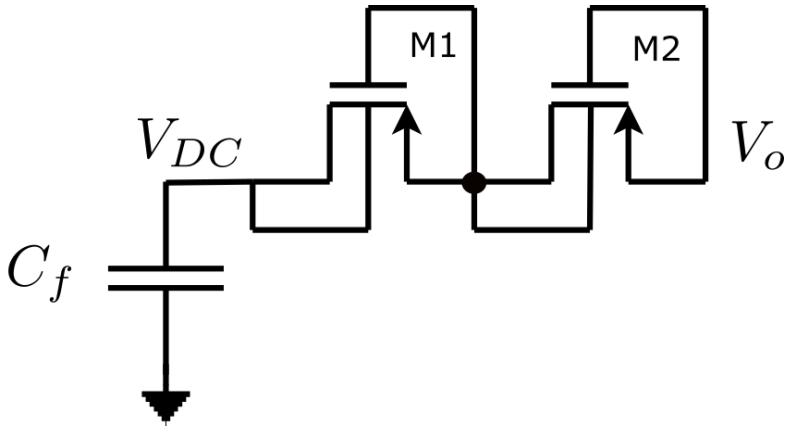


Figure 2.8: LPF used in the mixer (LPF_M).

Component	W (μm)	L (nm)	Value
M1 & M2	10	180	-
C_f	-	-	436.22 fF

Table 2.5: LPF_M transistor geometries and component values.

The mixer is implemented using a double-balanced topology [27], which is shown in Figure 2.9. Transistors geometries, bias points, and component values are shown in Table 2.6. This circuit has high port isolation and second-order harmonic suppression. For a double-balanced mixer the stage that contributes most to distortion is the mixing quad [43]. To handle the output range from the TIA, the LO and RF input ports are implemented using NMOS transistors. This mixer utilizes a diff pair input with the outputs being switched back and forth between the R_{mix} resistors. This allows for high input frequencies to be mixed down to lower frequencies, and for mixing up the low frequency 1/f noise.

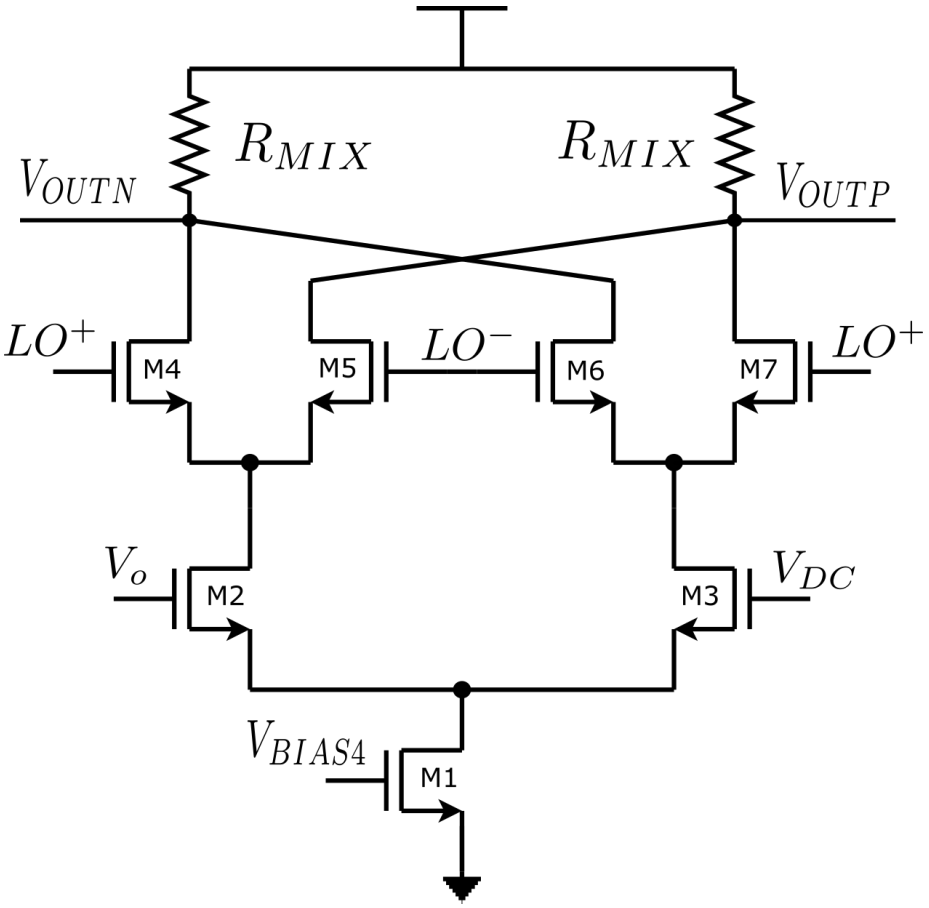


Figure 2.9: Double-balanced mixer used in the LIA.

Component	W (μm)	L (nm)	$\lvert I_D \rvert$ (μA)	$\lvert V_{GS} \rvert$ (V)	Value
M1	40	540	24	0.494	-
M2 & M3	0.750	720	12	0.883	-
M4 - M7	20	180	12.5	-	-
R_{mix}	-	-	-	-	42.85 kΩ

Table 2.6: Mixer transistor geometries and component values.

To reduce the input-referred current noise of the LPF to 1 nA_{rms}, the required single-

ended mixer dc gain A_{mix} is designed to be 0.94 V/V. A_{mix} is given by

$$A_{mix} = \frac{2}{\pi} \cdot g_{m2,3} \cdot R_{mix} // (g_{m4-7} r_{o,4-7}) r_{o2,3} = \frac{2}{\pi} \cdot \frac{2I_{D2,3}}{V_{ov2,3}} \cdot R_{mix} // \frac{L_{2,3}}{\lambda_{2,3} \cdot I_{D2,3}}. \tag{2.4}$$

The gain for $g_{m2,3} \cdot R_{mix} // r_{o2,3}$ is then required to be 1.48 V/V simply from the $\frac{2}{\pi}$ scaling factor. From the output of the TIA, the maximum signal amplitude is ∼0.35 V. This requires having a swing from the mixer output of ∼1 V. To meet the power requirements, bias current I_{D1} is selected as 25 μA. The required R_{mix} for maximum output swing is 40 kΩ. To avoid the case where the ±10% tolerance causes the output to clip at 1.8 V, R_{mix} is increased to 44 kΩ. This reduces the common-mode level to allow for a larger positive output swing. The design parameters $r_{o2,3}$ are chosen to be greater than 1.75 MΩ to keep the reduction of R_{mix} to less than 2.5%, which relaxes the requirement for $g_{m2,3}$. This also increases linearity, as a larger overdrive voltage is obtained and the gain is not as dependent on the output resistance of transistor devices. This yields $L_{2,3}$ = 754 nm. Transistor widths $W_{2,3}$ are then swept to obtain a gain of 1.48 V/V at the lowest expected resistance. Optimization of this process and BW consideration results in $L_{2,3}$ = 720 nm, R_{mix} = 43 kΩ, $W_{2,3}$ = 750 nm, a BW of 70 MHz, and a current consumption of 24 μA. The differential small-signal gain for the nominal load resistance is 3 V/V from Equation 2.4. The filter BW needs to be less 1 kHz to allow for the system to measure signals down to 1 kHz without causing attenuation. The largest possible MIMCAP for the given channel width of 20 μm is used (436 fF), and the PMOS device widths are chosen accordingly to give a BW of 100 Hz.

2.3.1 Mixer Simulation Results

Simulation of mixer differential gain versus frequency is shown in Figure 2.10. The mixer maintains a stable gain of 5.5 dB over the operating frequencies.

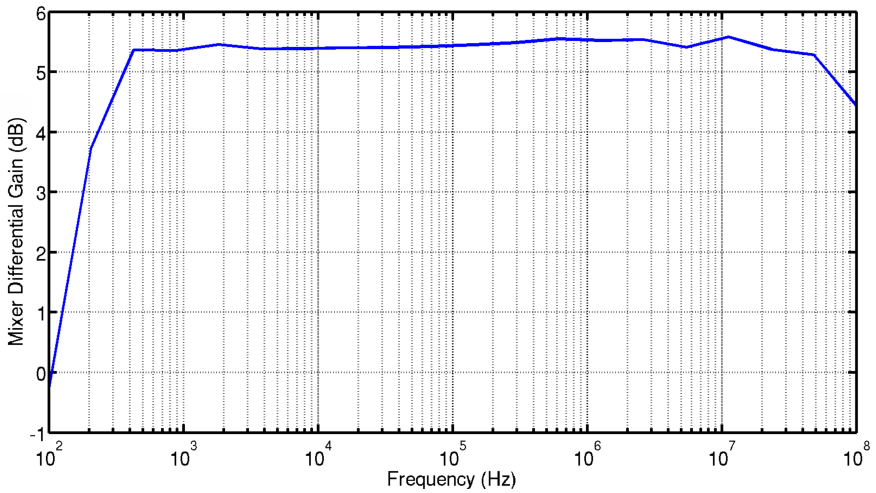


Figure 2.10: Mixer gain versus frequency.

Simulation results of mixer gain versus input voltage, shown in Figure 2.11, yields a 1 dB gain compression at an input amplitude of 10 μA_p, which is required for the maximum nominal input current. The on resistance of the electrode selection switches keeps the input swing to about 5 μA_p at a source impedance of 1 kΩ, which is well within the 1 dB gain compression point.

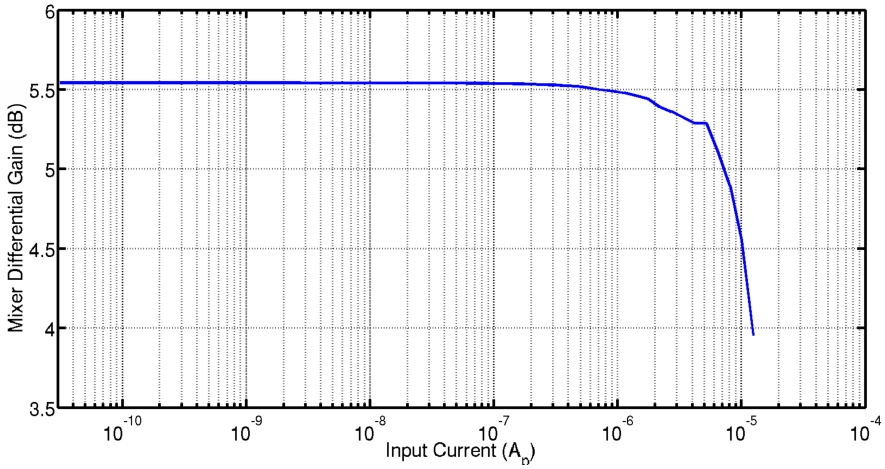


Figure 2.11: Simulated mixer gain versus input current.

The mixer noise PSD is simulated using harmonic balance in Spectre at a 1 kHz operating frequency. The input-referred noise current at the TIA input branch from a single-ended output is shown Figure 2.12. The average input-referred noise is 742 pA_{rms} over a BW from 980 Hz to 1020 Hz, which is the double side-band noise at the output of the filter at $2\pi\omega$= 1 kHz, with a filter BW of 20 Hz (which is a factor of two larger than the ADC LPF BW specification). The spikes at approximately 1.1 kHz and 3.5 kHz are caused by mixing fundamental frequency and second harmonic.

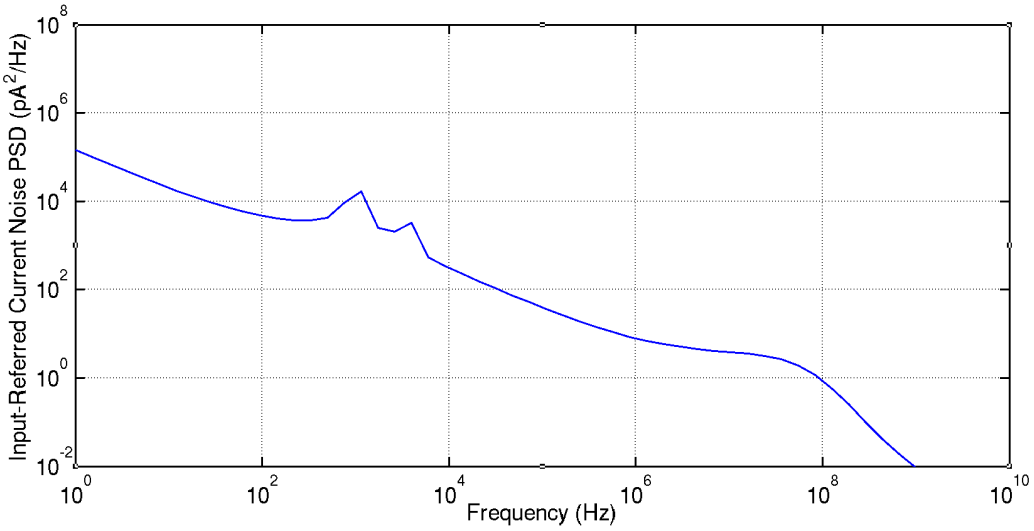


Figure 2.12: Simulated mixer input-referred noise PSD at TIA input.

The weak-inversion PMOS transistors used in the LPF in Figure 2.8 are simulated independently with no dc current and by applying a sinusoidal voltage at one side of the weak inversion transistors and measuring the resulting ac current. The result of impedance magnitude versus frequency is shown in Figure 2.13.

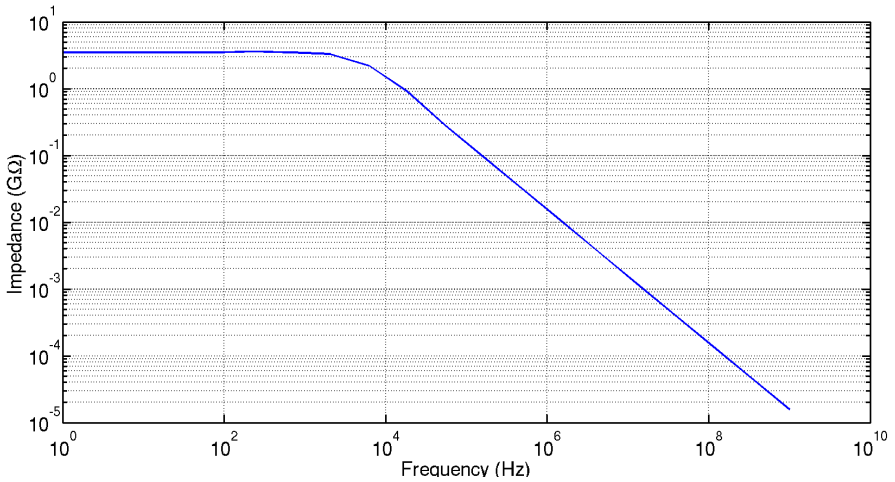


Figure 2.13: Simulated weak-inversion PMOS transistor impedance magnitude versus frequency for LPF_M.

At 6 kHz, the impedance magnitude starts to decrease at 20 dB per decade.

Results for impedance versus input amplitude are shown for 1 kHz and 1 MHz input signal frequencies in Figure 2.14. At 1 kHz, the impedance magnitude is about 3.5 GΩ and at 1 MHz, the impedance magnitude is about 10.6 MΩ. In both cases, the LPF BW is less than an order of magnitude below the operating frequency which is sufficient for passing the desired signal. The impedance drops at high input amplitudes due to the non-linearity of the parasitic capacitances in the weak-inversion PMOS transistors.

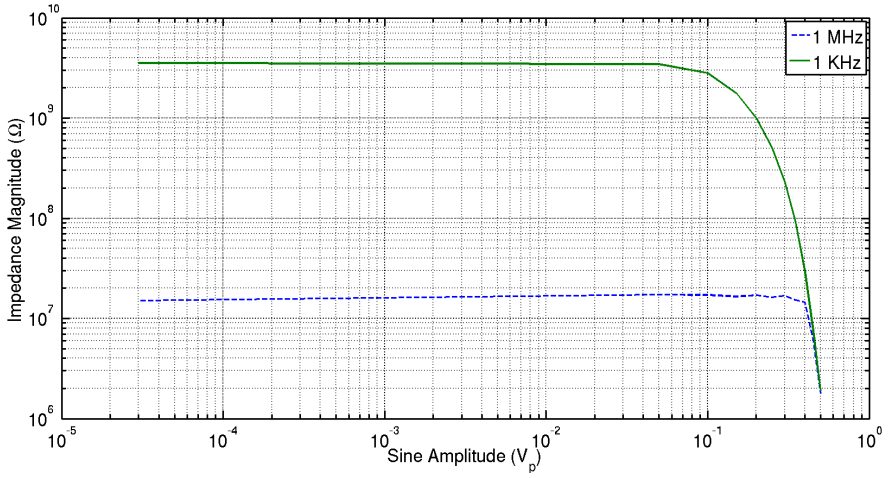


Figure 2.14: Simulated weak-inversion PMOS transistor impedance magnitude at 1 kHz and 1 MHz for LPF_M.

The mixer simulation results are summarized in Table 2.7.

Parameter	Specification	Simulation Results
DR	80 dB	80 dB
BW	>50 MHz	76 MHz
Gain	5.5 dB	5.5 dB
LPF BW	<100 Hz	100 Hz
Current consumption	<27.5 μA	24 μA
Input-referred noise at TIA input	<1 nA_{rms}	742 pA_{rms}

Table 2.7: Summary of mixer simulation results.

2.4 LPF_A Design

The LPF_A must be designed to meet a BW of 10 Hz. It is implemented using weak-inversion PMOS transistors and capacitors as shown in Figure 2.15. Device sizes are shown in Table 2.8.

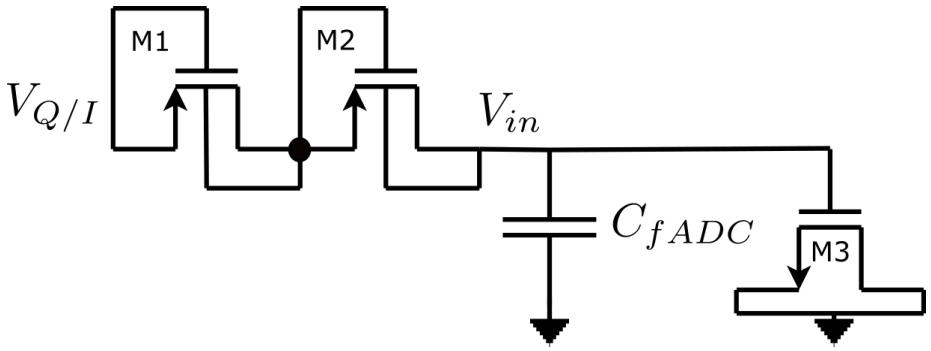


Figure 2.15: LPF$_A$ circuit.

Component	W (μm)	L (nm)	V$_{GS}$ (V)	Value
M1 & M2	10	180	0	-
M3	30	4000	>0.8	-
C_{fADC}	-	-	-	420.6 fF

Table 2.8: Transistors geometries and component values used in LPF$_A$

2.5 ADC Design

The ADC must be designed to meet the specifications shown in Table 2.9.

Parameter	Specification
DR	80 dB
Sampling Rate	>20 Hz
V$_{LSB}$	27.5 μV
Current consumption	<27.5 μA
Input-referred noise	<2.2 nA$_{rms}$

Table 2.9: ADC specifications.

A simple-ramp ADC topology was chosen, which is shown in Figure 2.16. This archi-

tecture has only comparator and a counter which reduces the area occupied by the ADC. When a voltage ramp V_{ramp} is compared to the signal input V_{in}, the counter increments when $V_{ramp} < V_{in}$. However, when $V_{ramp} \geq V_{in}$, the counter is disabled and the count value is held, providing a digital representation of V_{in}.

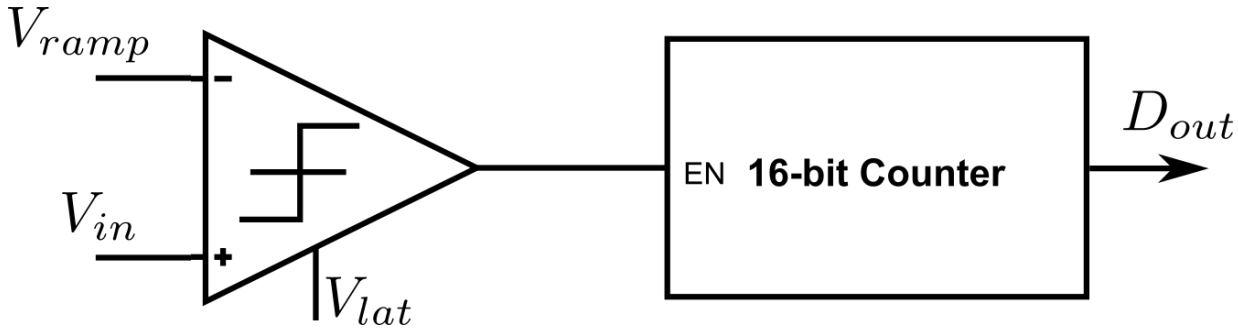


Figure 2.16: ADC architecture.

The comparator utilizes a diff pair and latch with enable signal (V_{lat}) to compare V_{ramp} and V_{in} as shown in Figure 2.17. Component geometries and biases are shown in Table 2.10. Transistors M8 and M9 in the latch turn on and off the positive feedback. Transistors M10 and M13 are used to reset the latch. M6 and M7 act as a buffer for the diff pair output which reduces the kickback from V_{lat} to the inputs. *Reset* is used to hold the outputs high.

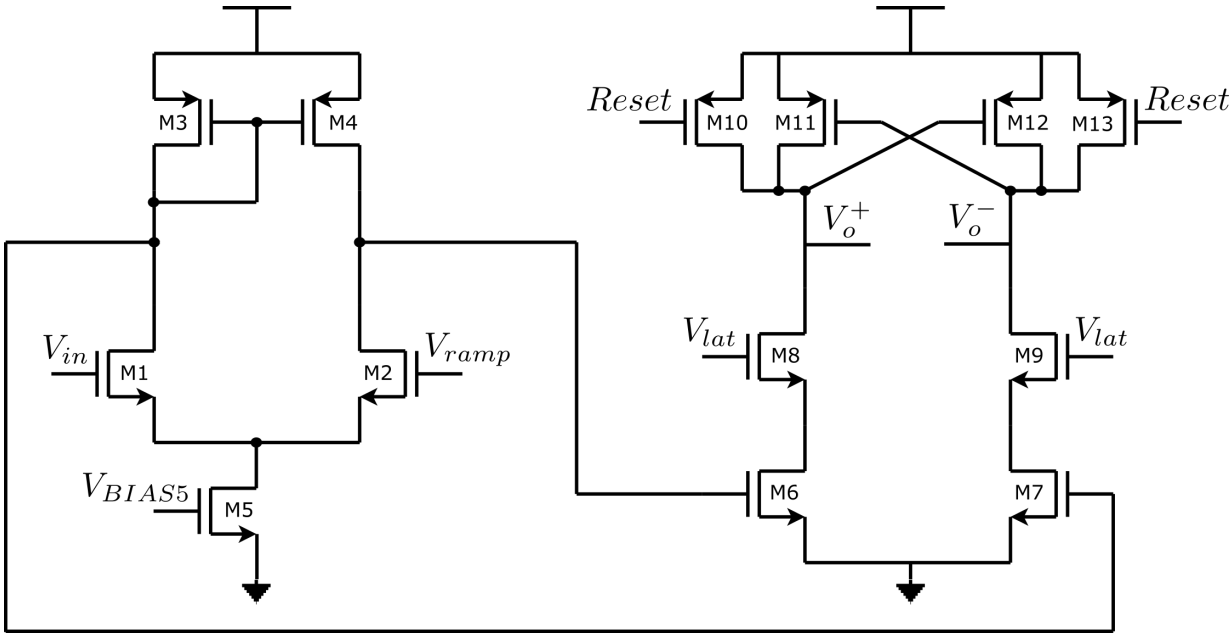


Figure 2.17: ADC comparator architecture.

Component	W (μm)	L (nm)	$\lvert I_D \rvert$ (μA)	$\lvert V_{GS} \rvert$ (V)
M1 & M2	50	540	15	0.519
M3 & M4	20	720	15	0.57
M5	40	540	30	0.487
M6 & M7	0.5	180	-	-
M8 & M9	0.5	180	-	-
M10 - M13	1.75	180	-	-

Table 2.10: Geometry and bias points of ADC comparator transistors.

The asynchronous 16-bit counter is implemented as a clock divider, shown in Figure 2.18, and some simple logic as shown in Figure 2.19. The counter clock (cclk) is gated. The system clock (clk) is used to control the D flip-flops (DFFs).

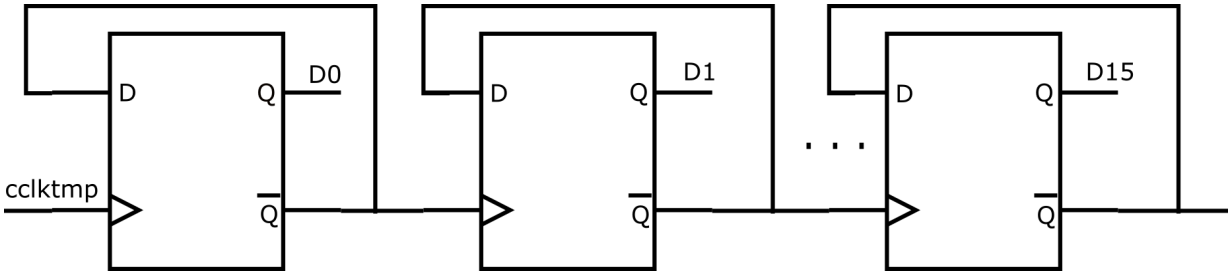


Figure 2.18: 16-bit ADC counter.

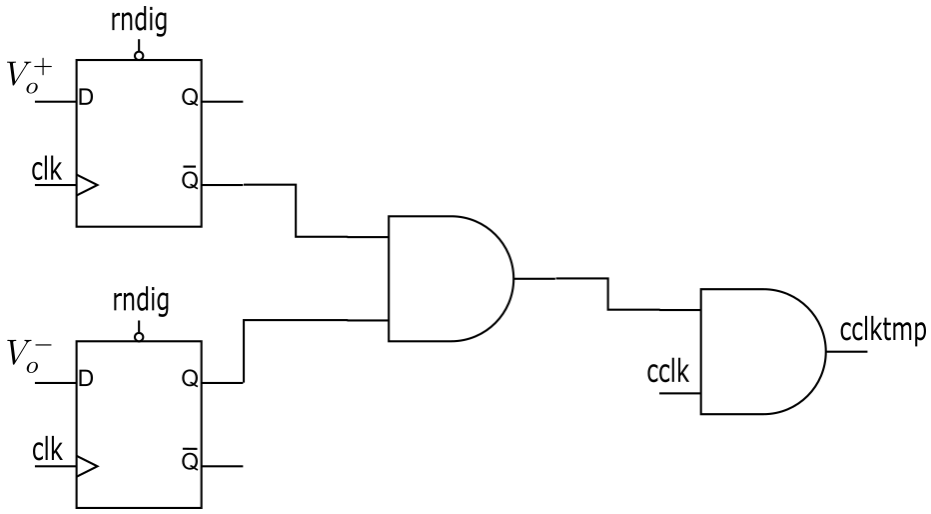


Figure 2.19: ADC counter stop logic.

The V_{LSB} of the ADC is given by

$$V_{LSB} = \frac{A_{ramp} \cdot f_{samp}}{f_{lat}}, \tag{2.5}$$

where f_{lat} is the frequency of V_{lat}, f_{samp} is the sampling frequency of the ADC, and A_{ramp} is the amplitude of V_{ramp}. For A_{ramp} of 1.8 V, the required f_{lat} is 1.31 MHz. This frequency is also the required counter frequency. As such, the asynchronous counter is verified at frequencies up to 2 MHz. The ramp amplitude can be reduced to 1 V (0.8 V to 1.8 V) which can then be used to decrease V_{LSB} or increase f_{samp}. The ADC comparator must settle to

within at least half an least-significant bit (LSB) in the period of V_{lat}. The relationship between comparator bandwidth f_{3dB}, the 16-bit relative error $\varepsilon_{16-bits}$ and f_{lat}, assuming a first-order response, is given by

$$\varepsilon_{16-bits} = e^{\frac{-\pi \cdot f_{3dB}}{f_{lat}}}. \tag{2.6}$$

Solving equation 2.6 yields a f_{3dB} of 4.38 MHz.

The comparator design uses the diff pair for the TIA as the starting point. Minimum sizes for the latch transistors reduce their parasitic capacitance, which also reduces kickback. The kickback amplitude at the output of the diff pair is ∼1.4 mV for the given topology. In order to be able to resolve 27.5 μV at the input, the gain must be at least 51 V/V. In the case where A_{ramp} is reduced to 1 V, the gain required becomes 91.7 V/V to resolve the new LSB.

The power requirement results in a total current consumption of 167 μA. The mixer and TIA use 101 μA which gives 65.7 μV for each of the two ADCs, resulting in 30 μA being selected as the bias. New values of $L_{3,4}$ for the PMOS transistors are computed to give a gain of a at least 100 V/V, which yields a length of ∼720 nm. Width $W_{3,4}$ is selected to give a dc operating point of approximately 1.24 V, which is the minimum voltage required at that node to keep the NMOS transistors in saturation over the range of expected input voltages. The LPF is designed to have a BW of approximately 10 Hz and the maximum equivalent capacitance per filter output is 1 pF. The equivalent BW for suppression of input frequencies below the detection limit is ∼14 Hz. V_{ramp} and V_{lat} are generated externally to the IC for flexibility.

2.5.1 ADC Simulation Results

The ADC differential non-linearity (DNL) and integral non-linearity (INL) are not simulated because to demonstrate a 16-bit resolution, the simulation time would be exceedingly long. Instead, a relatively small number of points are selected to verify the design. The simulation is run at f_{lat} of 40 Hz, f_{lat} frequency of 2.86 MHz, and a V_{LSB} of 14 μV from 0.8 to 1.68889 V. The results are shown in Figure 2.20. The filtered output can swing

from 1.6183 V down to 0.982 V. It is found that the ADC cannot resolve 27.5 μV at input voltages greater than 1.787 V as the gain of the comparator drops below the minimum value required. This is not an issue for the filtered output, but will limit the measurements from the mixer output as it could swing from 1.8 V down to 0.8 V.

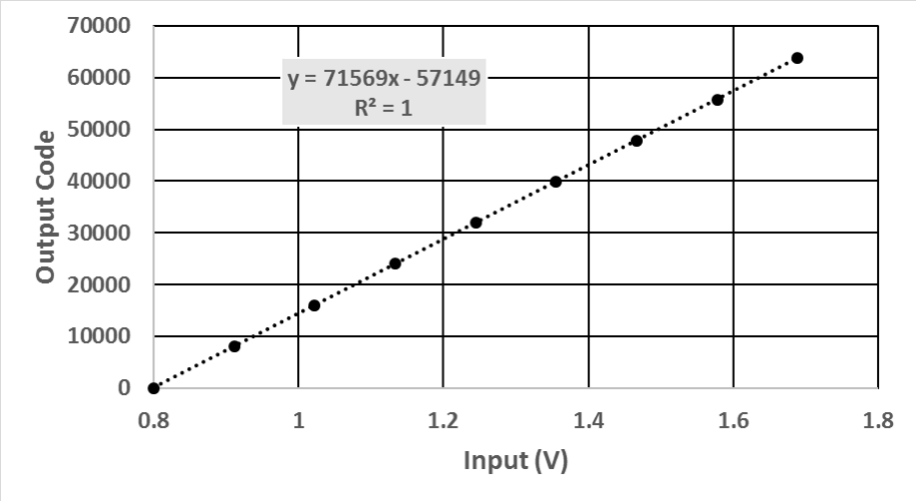


Figure 2.20: Simulated ADC output code vs. input.

The ADC noise current PSD, referred to the input of the TIA, is shown in Figure 2.21. The ADC has a total simulated input-referred noise of 1.8 nA_{rms} over the frequency range from 1 Hz to 5 MHz. This is lower than the estimated LPF $\sqrt{\frac{kT}{C}}$ noise of 65 μV, which when input-referred, is 2.2 nA_{rms}. This is probably due to the noise from the weak-inversion PMOS transistors not being modelled well.

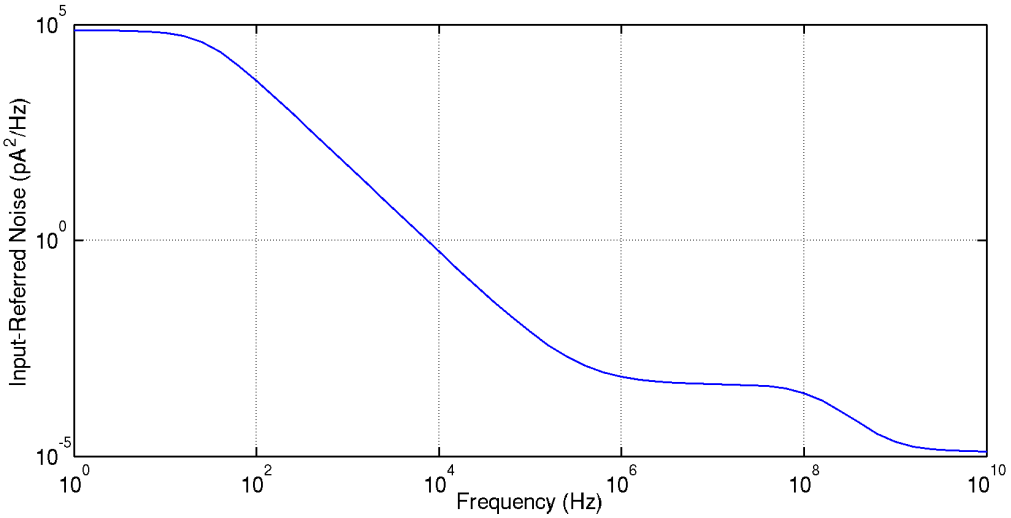


Figure 2.21: Simulated ADC noise current PSD referred to TIA input.

The ADC simulation results are summarized in Table 2.11.

Parameter	Specification	Simulation Results
DR	80 dB	80 dB
Sampling Rate	>20 Hz	40 Hz
V_{LSB}	27.5 μV	14 μV
LPF BW	10 Hz	14 Hz
Current consumption	<27.5 μA	30 μA
Noise (1 Hz - 5 MHz BW)	<2.2 nA_{rms}	1.8 nA_{rms}

Table 2.11: Summary of ADC simulation results.

2.6 Simulation of Acquisition Channel Performance

The LIA components are then laid out together to fit within the minimum electrode pitch (20 μm). The parallel-in serial-out (PISO) shift registers, which will be discussed in Chapter 3, are also placed within the given area specification. The layout of the entire channel is shown in Figure 2.22.

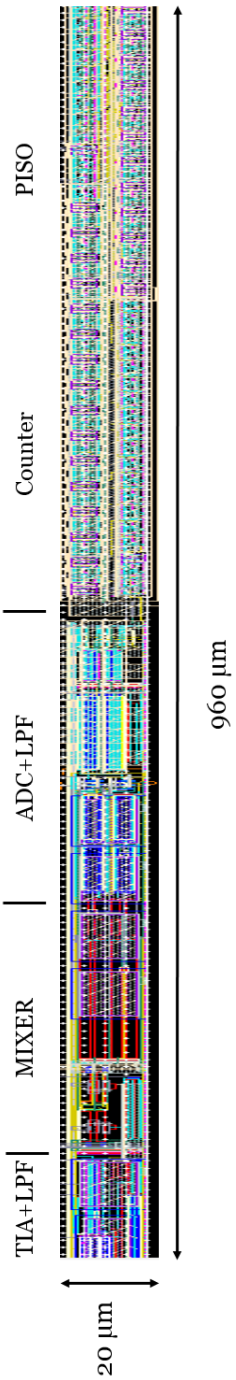


Figure 2.22: Acquisition channel layout.

The simulation results for extracted layout channel gain versus impedance magnitude at 10 kHz is shown in Figure 2.23. The 1-dB gain compression point is approximately 900 Ω.

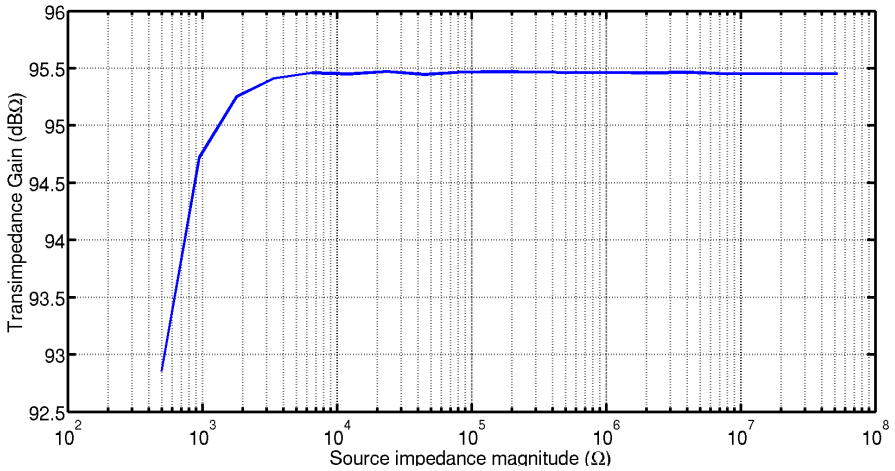


Figure 2.23: Simulated acquisition channel gain versus input impedance at 10 kHz.

The channel gain versus frequency for a purely real 100 kΩ input impedance is shown in Figure 2.24. Due to simulation runtime, frequencies only up to 1 MHz are simulated.

The acquisition channel input-referred noise PSD is shown in Figure **??**. The input-referred channel noise, as simulated with harmonic balance at 100 kHz, is 1.9 nA_{rms}.

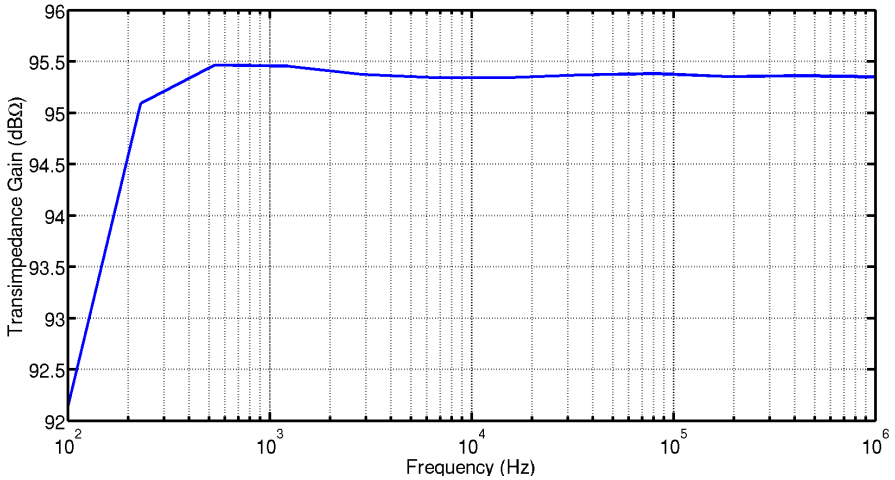


Figure 2.24: Simulated acquisition channel gain versus frequency with a purely real source impedance of 100 kΩ.

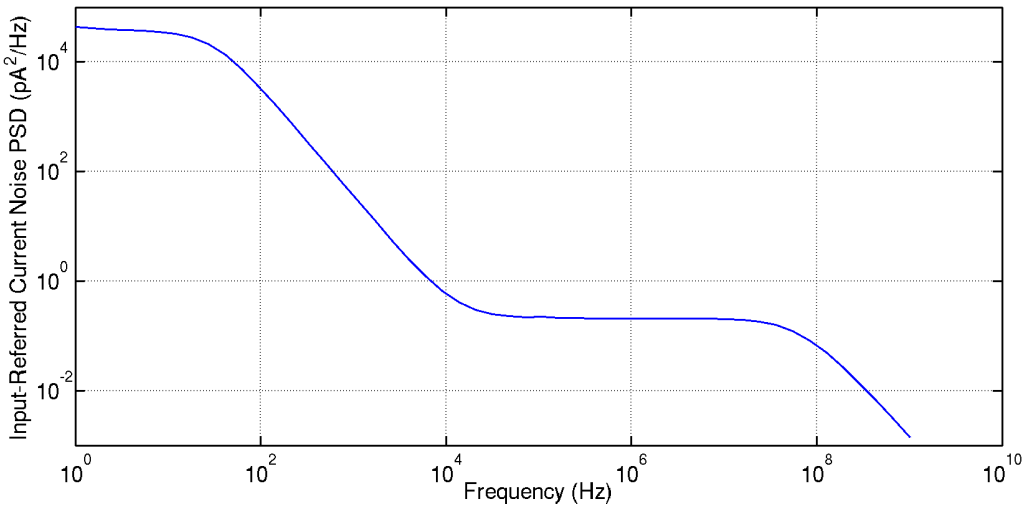


Figure 2.25: Simulated acquisition channel input-referred current noise PSD.

Chapter 3

Camera Architecture and Physical Design

This chapter starts by outlining the physical architecture of the camera and describing the design decisions made at the system level. Then the individual components of the architecture, including the electrode selection and interface circuits, power domains, clock domains, shift registers, PISO shift registers, input/output (I/O) pads, and test circuits are described. Next, an overview of the functional operation of the camera is given, and finally a performance summary from simulation is provided.

3.1 Camera Architecture

The camera floorplan, as shown in Figure 3.1, must accommodate electrode arrays, sensor electronics, and bond pads. The layout of the IC includes the microelectrode array (MEA) on one side of the chip and the sensor electronics for processing (acquisition channels) on the other. MEA1 has a 70×40 grid of electrodes, where each electrode has dimensions of 10×10 μm^2. MEA2 has a 17×11 grid of electrodes, where each electrode has dimensions of 40×40 μm^2.

The I/O bond pads are located along the perimeter of the IC. The electrode selection

scan chains are located at the bottom of the chip for columns and in-between the electrodes and acquisition channel for rows. Each row in MEA1 has its own acquisition channel to allow for multiple rows to be read out simultaneously. MEA2 has four acquisition channels per row. ADC data from each acquisition channel is converted from parallel-to-serial format using a parallel-in, serial-out shift register. System design decisions include having two V_{app} signals to allow for channel coupling measurements. Since only one is needed, the second acts as a fail-safe. Having two also enables an external impedance analyzer to be used as an alternative to the acquisition channels. As mentioned before, the ADC can sample either the mixer output or the filter output, which allows for independent characterization of the mixer output.

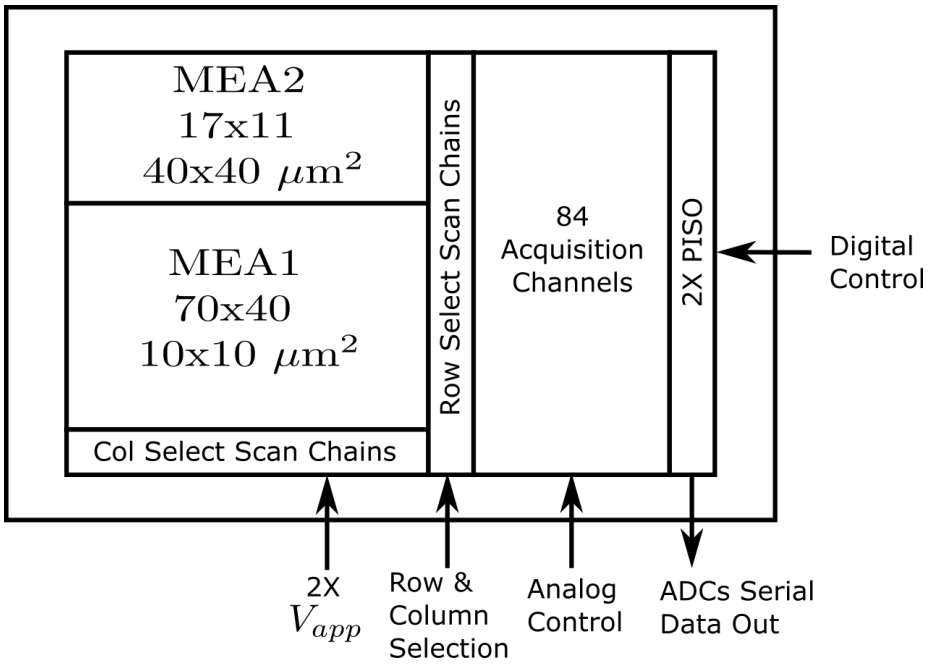


Figure 3.1: CMOS camera IC architecture.

3.1.1 Electrode Selection and Interface Design

The electrode selection is done with scan chains and switches. The switches are implemented with transmission gates which allow for rail to rail signals to pass through and

have reduced noise margin compared to single transistor switches. Scan chains are a series of DFFs which are serially loaded to turn the various electrode switches off or on. For the input to the acquisition channels and each of the two V_{app} signals, there are scan chains for both the rows and columns, yielding a total of six scan chains. Each output of a DFF in a row scan chain controls a switch to select a row. Similarly, each output from a column scan chain DFF controls all switches for each electrode in an entire column. A simple diagram in Figure 3.2 shows this functionality for a 2×2 block. Signals are in the form colxy and rowxy, where x is the row or column position and y is the scan chain identifier ($1 = V_{in}$, $2 = V_{app1}$, $3 = V_{app2}$).

Each electrode connects to each V_{app} signal through a row and column switch. The electrode also connects to an acquisition circuit through a row and column switch (V_{in}). It is found that the capacitive loading from the switches in MEA1 is high enough to cause significant leakage of input current at higher frequencies. To reduce the impact of loading, each row of an acquisition channel is split into three sections. This leads to three separate row switches for each acquisition channel input. Since there is limited space, the switch transistors are designed to have minimum length of 180 nm and widths of 5 μm. The switch's width is limited due to the electrode size and pitch. Since the signal V_{app} has to pass through four switches before reaching the acquisition channel input, each switch contributes an on resistance. The series on resistance combined by four switches between V_{in} and the acquisition channel input, is not an problem, as the resistance can be calibrated out from an impedance measurement. An additional feature added, as shown in Figure 3.3, is a load value (holdv) and a scan chain output selection (scoutsel). These controls allow all the switches to be set to the off position simultaneously when holdv=0 and scoutsel=1. As a result, for the scan chains can be loaded without activating any switches so that the cells are not disturbed due to transient effects.

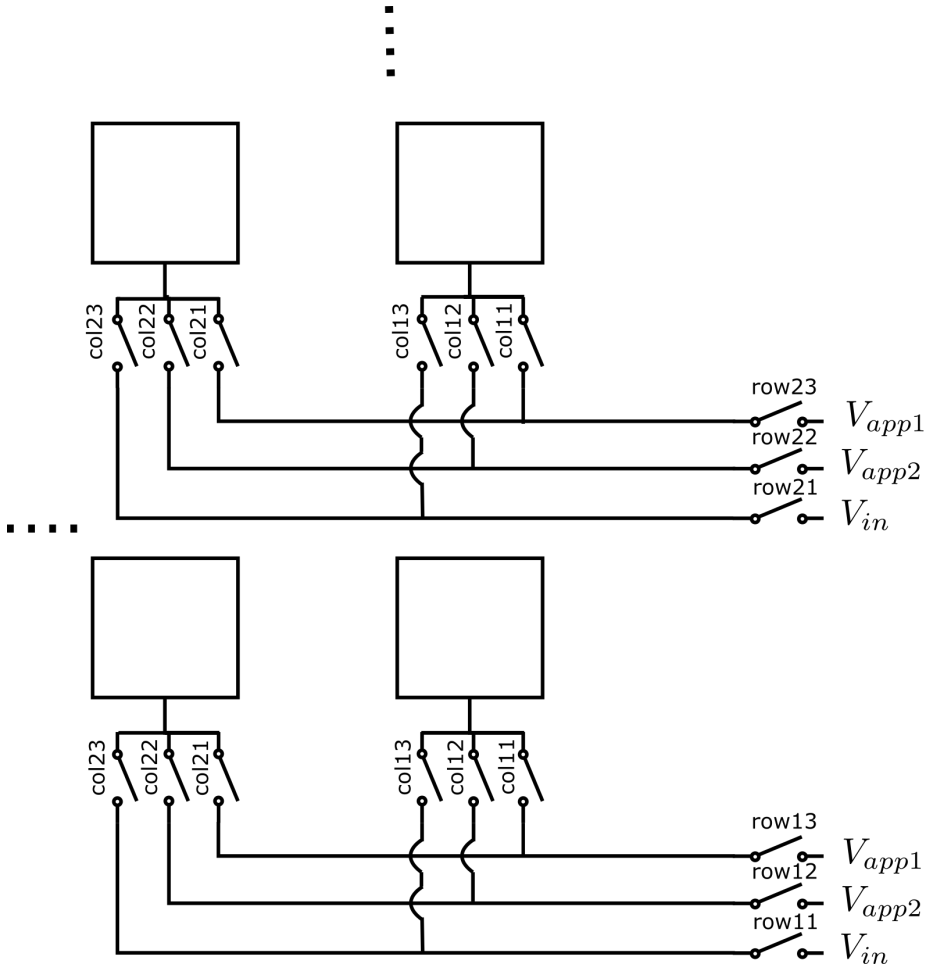


Figure 3.2: Electrode selection functional diagram.

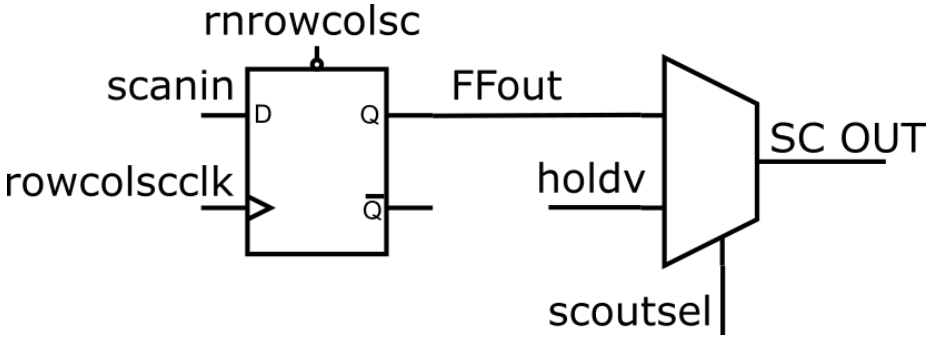


Figure 3.3: Shift register unit cell.

3.1.2 Electrode Fabrication

Each electrode is formed using the top aluminium metal layer of the CMOS process (metal 6). High density vias connect to the top metal layer to metal layers below, and eventually to the active devices in the silicon substrate. At the time of manufacture, the passivation above each electrode is removed so that the metal electrode is exposed. Because aluminium is electrochemically active and not compatible with live cells, two methods could be used to interface the electrodes to the cells and bath solution. The first involves wet etching away the top metal layer to expose the tungsten vias below, which then contacts the electrolyte and cell. The second method involves depositing gold on top of the aluminium (possibly by using an electro-less plating process), which would then contact the cell. Chip cross-sections before post processing and after the proposed gold deposition (not implemented in this thesis) are shown in Figure 3.4.

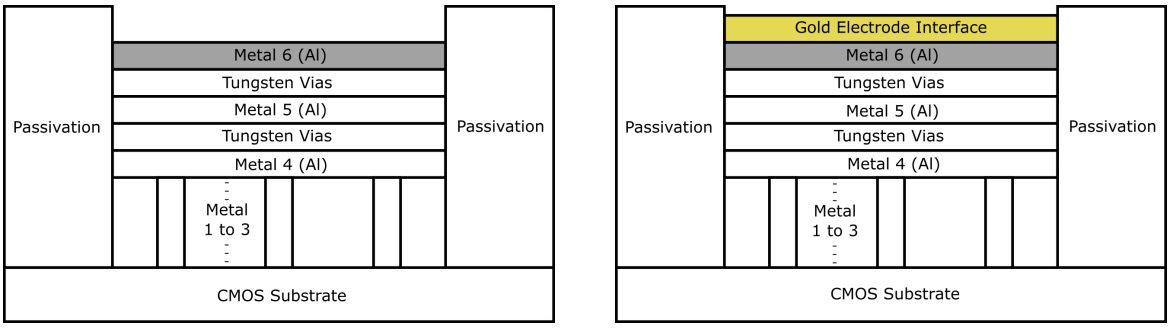


Figure 3.4: Chip cross-section (a) before post processing and (b) after the proposed gold deposition.

3.1.3 Power Domains

There are two power domains on the IC, analog VDD (AVDD) and digital VDD (DVDD), and both operate at 1.8 V. The LIA (with the exception of the digital logic) is powered by AVDD. The column and row select scan chains also powered using AVDD. The PISO and asynchronous counter are powered from the digital power supply. Interference from the

scan chain clock is insignificant as it is turned off when the LIA is operating. To isolate the substrate of the analog circuits and hence provide ground isolation, a guard ring consisting of a deep N-well is placed around the NMOS and PMOS transistors that are connected to digital ground (DVSS). This is the recommended procedure by the manufacturer of the CMOS process.

3.1.4 Clock Domains

The four clock domains on the IC are summarized in Table 3.1.

Clock Name	Description
clk	PISO and DFFs for logic
cclk	ADC counter
vlat	Latch
rowcolscclk	Scan chains

Table 3.1: Camera IC clock domains.

The reason for a separate scan chain clock is to allow for the digital components on the IC to run without generating switching interference near the electrode interface. The reason for separate counter and latch clocks is to add flexibility when setting the period between the time the latch settles and the time the counter increments. The remaining digital circuits also have their own clock.

3.1.5 Parallel-in Serial-out Shift Register

Each unit of the two PISOs is designed as shown in Figure 3.5. When signal w/s is high, the architecture behaves as a scan chain; when it is low, data is loaded from the counters. The PISO must transmit the ADC data from the IC within the sampling period of the ADC. The PISO contains 1344 DFFs, which for an ADC f_{samp} of 40 Hz (double the specification), sets the minimum PISO clock frequency of 50 kHz. However, to utilize only

one digital clock, the DFFs need to be able to run at f_{lat}, which is up to 2 MHz. The data is transmitted from the IC with most-significant bit (MSB) first.

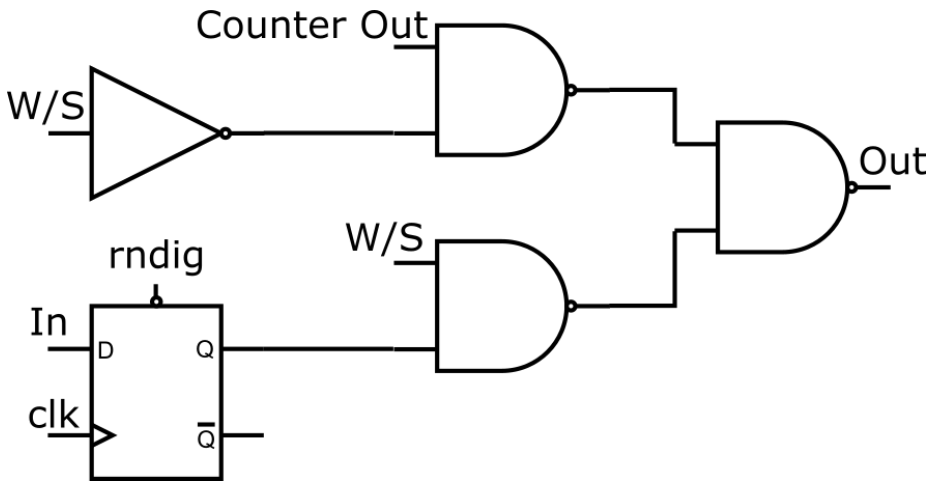


Figure 3.5: PISO unit circuit.

3.1.6 Global Bias Circuits

Each current mirror has a maximum size MIMCAP (30×30 μ m^2, 952 fF) connected to its gate to attenuate high-frequency interference. The total decoupling capacitance is 3.8 pF per current mirror.

3.1.7 I/O Pads

I/O pads based off work done in [44] were implemented for analog signals, digital signals, and power busses. The pads utilize diodes to provide electrostatic discharge (ESD) protection. To prevent large potentials from developing between different power domains, each domain is connected to the other by anti-parallel diodes.

3.1.8 On-chip Test Circuits

Two channels within the camera are dedicated to providing direct access to nodes within the LIA. The two channels selected are the first and last acquisition channels, which are at either end of the IC. The nodes that are brought out to pads on the IC for both test channels include: the TIA output, the output of the mixer filter, inputs to the two ADCs, the ADC comparator outputs, and the latch outputs. The only difference between the test circuits and the non-test circuits is the extra external capacitance connected to each of the internal nodes. This added capacitance reduces the BW and could result in additional interference coupling into the channel from external sources.

3.2 Camera Functional Operation

The proposed operation of the camera is outlined in Figure 3.6. Signals used in figures in this section are explained in more detail in the pin table in Appendix A. In step (1), the scan chains are loaded to select a working and reference electrode. At the same time the output of the scan chains are disabled which keeps all row and column select switches off until loaded. During the loading of the scan chains, the mixer or filter output for the real path of the LIA is selected. Once the scan chains are loaded, the outputs are enabled and the LIA outputs begin to settle. In step (2), once the LIA output has settled the ADC samples the output of the filter or mixer for the real path. In step (3), the data is transmitted off chip. After this, in step (4), the output of the filter or mixer for the imaginary path is sampled, then in step (5), the data is transmitted off chip. The process is repeated until all electrodes are read out.

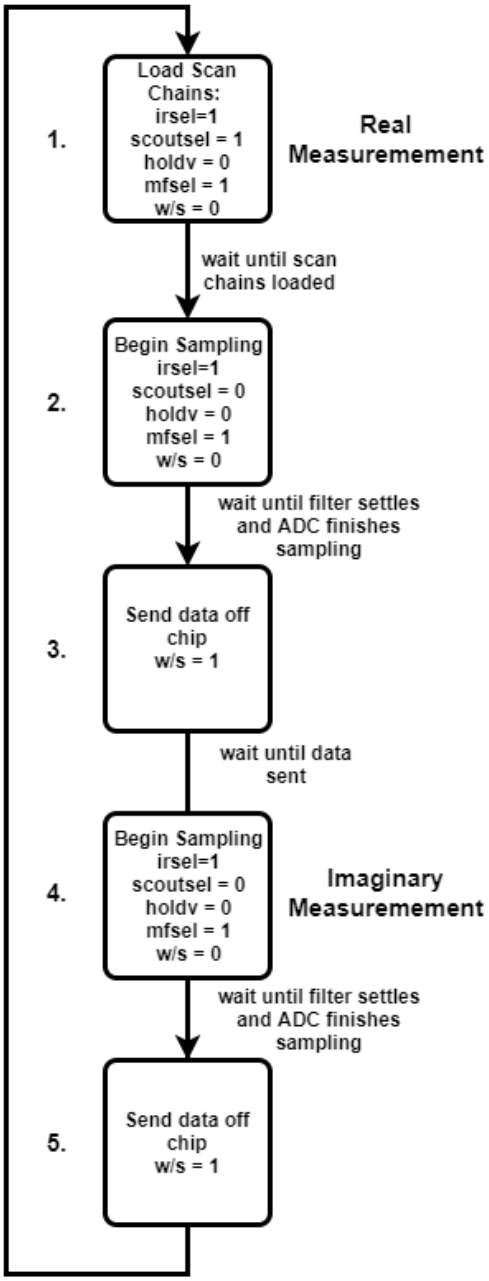


Figure 3.6: Flow graph of camera operation.

3.2.1 Camera Timing

For each of the core operations (loading scan chains, sampling, and sending data), a timing diagram is shown below to provide clarity on functionality. The timing digram for loading scan chain chains for V_{in} (vin) and V_{app1} (vsource) is shown in Figure 3.7. In this timing diagram, row 3 and column 4 are selected for vsource, and row 2 and column 5 for vin in MEA1. For loading the scan chains, the number of clock cycles needed is 164. The reason for this is that there are three scan chain units per V_{in} row within MEA1, which splits the columns into approximately three equal sections.

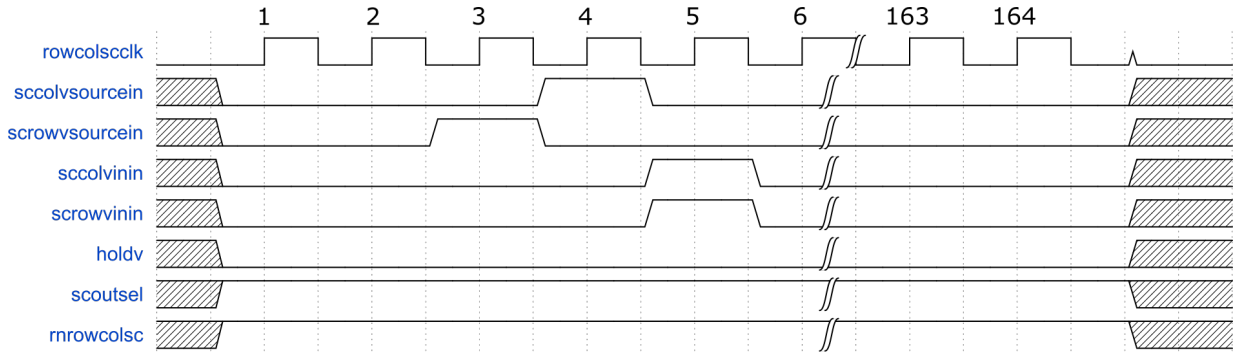


Figure 3.7: Timing diagram for loading scan chains.

The timing diagram to sample data for a filter output and real part of the signal is shown in Figure 3.8. N_{code} is the total number of codes for an N-bit ADC, where N is the number of bits. This timing diagram assumes that the LPF output has settled to within the value required by the ADC's resolution.

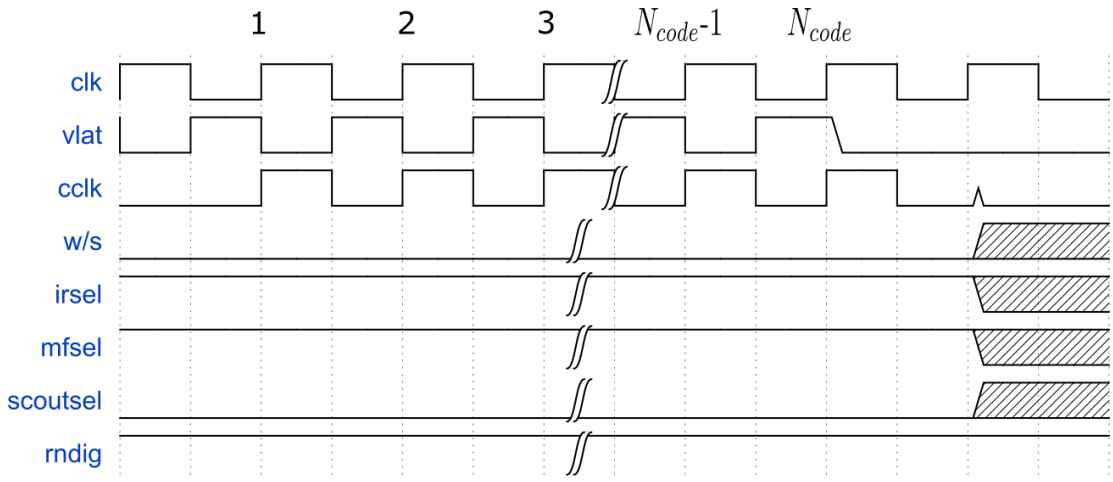


Figure 3.8: Timing diagram for sampling data.

The timing diagram to send the 16-bit data to an external controller with MSB first is shown in Figure 3.9. The scanoutp and scanoutn pins send the ADC data for row 1 first, then row 2, and this process continues sequentially until all 84 rows are sent. The whole process takes 1344 clock cycles.

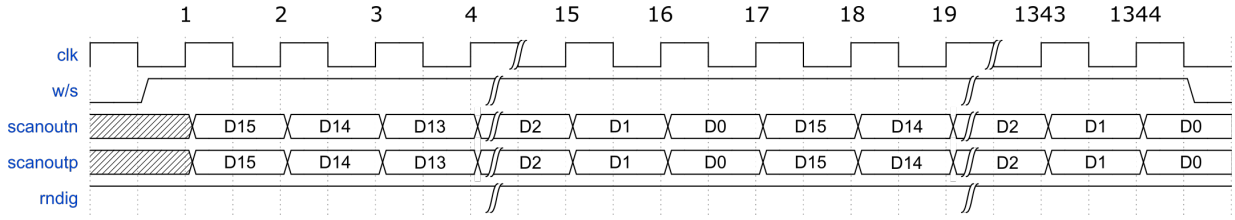


Figure 3.9: Timing diagram for transmitting data off chip.

3.3 System Performance Summary

The fabricated camera IC is shown in Figure 3.10. The simulated performance of the lock-in circuits and system are summarized in Table 3.2.

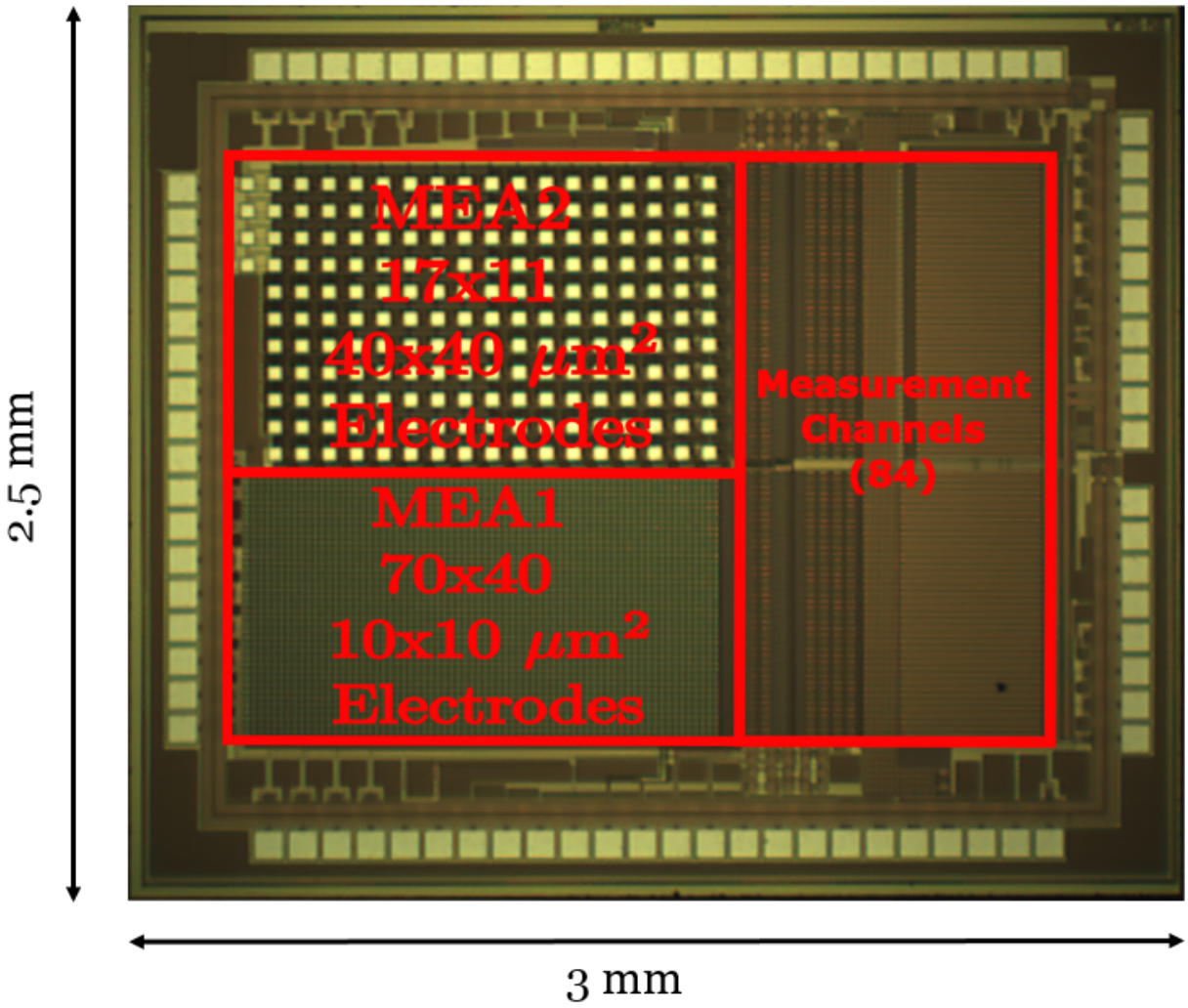


Figure 3.10: Camera IC.

Reference	Targeted Specification	Simulated Results
Topology	Lock-in + Ramp ADC	Lock-in + Ramp ADC
Frequency Range	1 kHz-1 MHz	1 kHz-1 MHz
Dynamic Range (dB)	80	80
Channel Power (μW)	300	300
Electrode Size (μm^2)	10×10 & 40×40	10×10 & 40×40
Electrode Pitch (μm)	20	20
No. of Electrodes	2987	2987
Input-Referred Noise	1 nA	1 nA (6 sample averaging)
Number of Channels	84	84
Channel Area (mm^2)	0.02	0.0192
Die Size (mm)	3×2.5	3×2.5
Frame Rate (Hz)	0.0117	0.0117
Technology (μm)	0.18	0.18
Area-readout FOM (mm^{-2})	36	36

Table 3.2: Camera target specifications and simulated performance.

Chapter 4

Experimental Results

This chapter outlines the printed circuit board (PCB) design and bench top characterization of the impedance camera IC. An overview of the complete system experimental setup is given first. Then, the PCB design and some of its key blocks are also described. The functionality of the RTL code used to operate the IC is discussed next. Following this, the camera is characterized and impedance measurements are summarized. Finally a summary and comparison of the measured camera performance is given.

4.1 Experimental Setup

The experimental test setup is shown in Figure 4.1. The system operates with the PC working as the master, which controls the PCB and the function generator using a C++ program. The experiments are run by setting field-programmable gate array (FPGA) parameters in software via a software library provided by the Opal Kelly company to operate the camera in various configurations. The Opal Kelly daughter board contains an FPGA and Universal Serial Bus (USB) interface which captures data and transfers it to the PC. The data is saved as binary files which are then imported into MATLAB for processing and analysis. This setup allows for flexibility in clock frequencies, ADC sampling rates, and camera operation through software control on a PC.

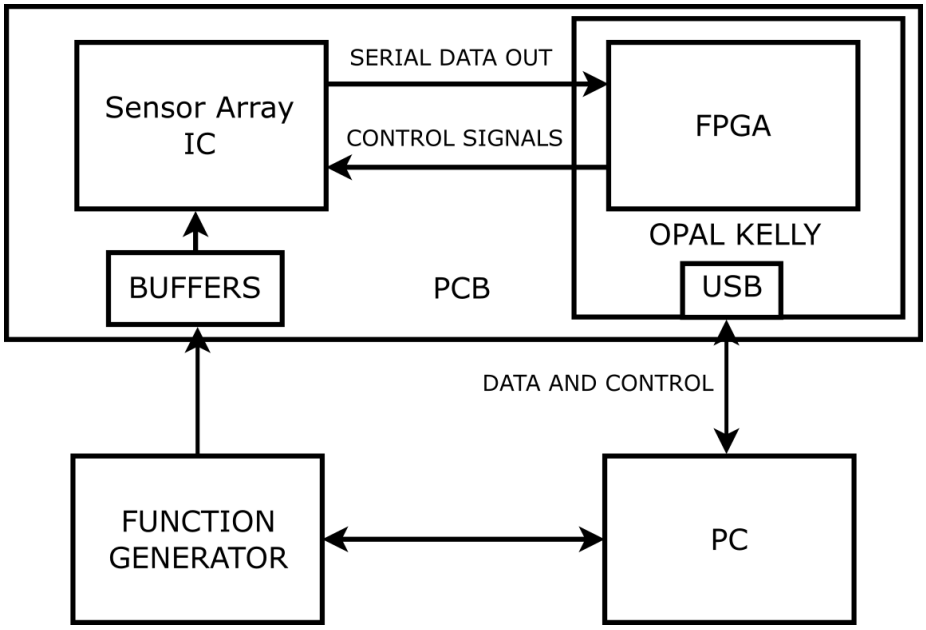


Figure 4.1: Experimental setup.

4.2 Printed Circuit Board Design

The PCB is designed and fabricated to operate the impedance camera IC and characterize its performance. Figure 4.2 shows the PCB used to characterize the camera IC.

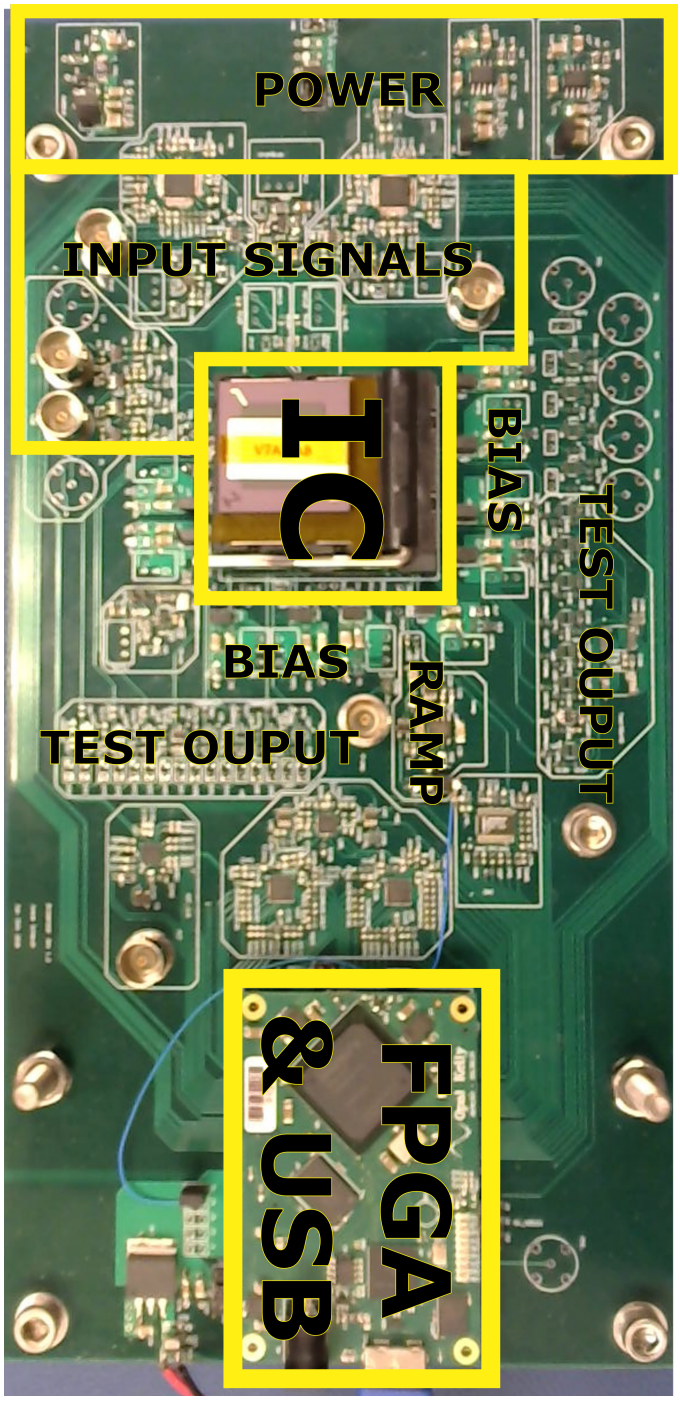


Figure 4.2: PCB showing camera, FPGA, biasing circuits and power ICs.

The board contains four layers: two for routing and one each for power and ground distribution. The following sections describe the design of bias circuits, ramp generator for the ADC, and signal buffers.

4.2.1 Bias Circuits

The impedance camera IC contains current mirrors for biasing the internal blocks. The current mirror biasing circuits for on-chip diode-connected NMOS and PMOS transistors are shown in Figure 4.3. An off-chip resistor R is used to generate the bias current for each device. To ensure low noise and interference, multiple decoupling capacitors C are inserted as shown.

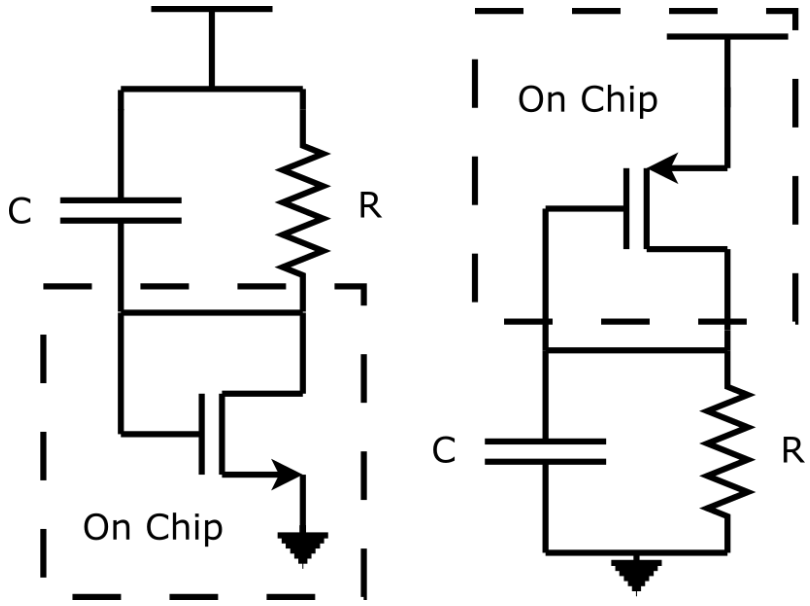


Figure 4.3: Current mirror biasing circuits with integrated transistors shown for clarity.

The off-chip bias circuit for the TIA reference voltage V_{BIAS} is shown in Figure 4.4. This circuit generates a reference voltage using a resistor divider, where R1 = 100 kΩ and R2 = 66.5 kΩ, a buffer, and filter capacitor C. The noise from the bias circuit is dominated by the op amp input-referred noise which is 1 μV_{rms}. This, when referred to the input of

the LIA is given by the expression $\frac{1\mu V}{|Z_{cell}|}$ and the magnitude of the input current is given by the expression $\frac{10mV}{|Z_{cell}|}$. From the two expressions, the input-referred noise will always be less than the input current magnitude by four orders of magnitude.

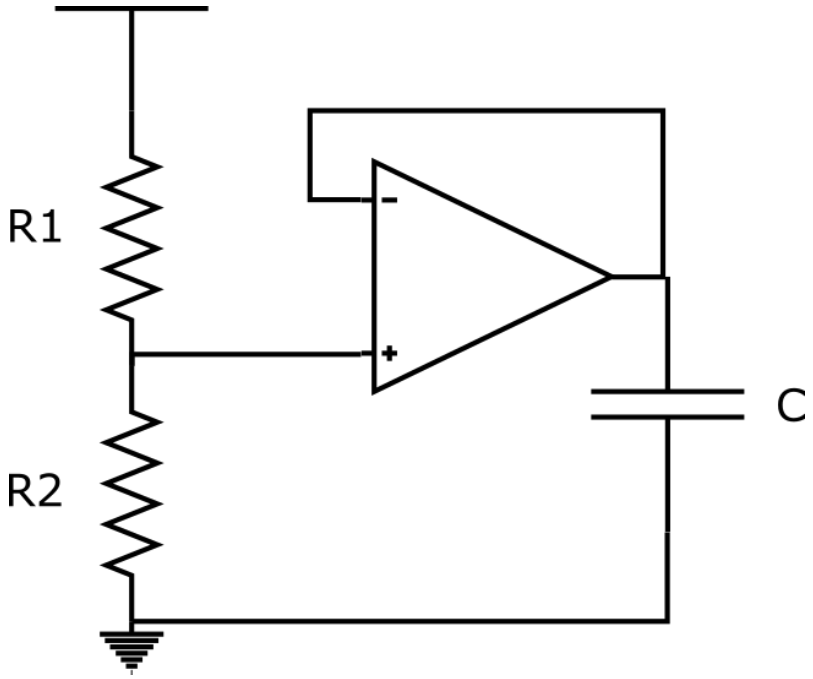


Figure 4.4: TIA reference voltage circuit.

4.2.2 Ramp Generator for ADC

The ramp generator circuit is shown in Figure 4.5.

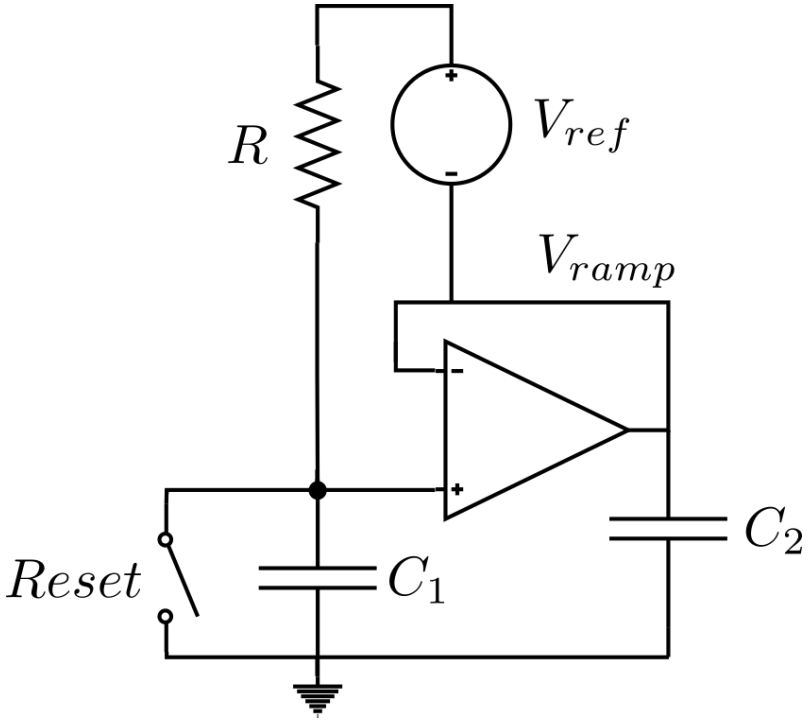


Figure 4.5: Ramp generator circuit.

The voltage reference V_{ref} generates a current though R which is fed into capacitor C_1 to generate a ramp voltage V_{ramp} with slope given by

$$\frac{dV_{ramp}}{dt} = \frac{V_{ref}}{C_1 \cdot R}. \tag{4.1}$$

The ramp is reset when the switch is closed (controlled by the FPGA) and the negative terminal is connected to the op amp output to maintain a fixed voltage across R. The ramp must exhibit low noise to meet the ADC LSB requirements. The total output noise is affected by the noise of the reference voltage, noise of the resistor, and noise of the op amp. The noise contribution from each component is summarized in Table 4.1. The total noise when referred to the LIA input is 280 pA_{rms}, which is significantly less than the LOD.

Component	Part # or value	Output-referred noise
Op amp	OPA322	1.4 μV_{rms}
V_{ref}	MAX6190	8.3 μV_{rms}
R	100 kΩ	40.6 nV_{rms}
Total	-	8.41 μV_{rms}

Table 4.1: Ramp generator components and noise contributions.

4.3 FPGA RTL Design

The FPGA is used to implement digital hardware to control the camera IC via a finite-state machine (FSM). The states implemented in the FSM are:

1. Reset: Resets all the digital circuits on the IC.
2. Load Scan Chains: Loads the row and column scan chains to enable individual electrodes to be selected as either the working or reference electrodes.
3. Sampling: Initializes the ADC to start sampling data.
4. Data Readout: Reads the ADC data from the IC.

The data path from the IC output to PC over USB involves a single first-in, first-out (FIFO) on the FPGA. Limitations in FIFO size imposed by the maximum FPGA memory size leads to a maximum of 189 16-bit ADC samples per acquisition channel. Obtaining a continuous time sampling size greater than 189 samples would require using the Opal Kelly's on board dynamic random access memory (DRAM) or a FPGA with more on-chip memory.

4.4 Camera Electrical Characterization

To characterize the electrical performance of the camera IC, an external source impedance Z_{cell} on the PCB is connected to V_{app} which sets a specific input current I_{in} into the LIA through the vsource pin. This default test setup is shown in Figure 4.6. As mentioned in Chapter 3, there are four switches that must be set to select electrodes. In this case, only one electrode needs to be selected (to provide a path from V_{app} to the LIA input), as there is no on-chip cell impedance being measured by the electrodes. Signal $mfsel$ selects whether the ADC samples either the filtered or unfiltered mixer output. Signal $irsel$, selects the real or imaginary mixer output.

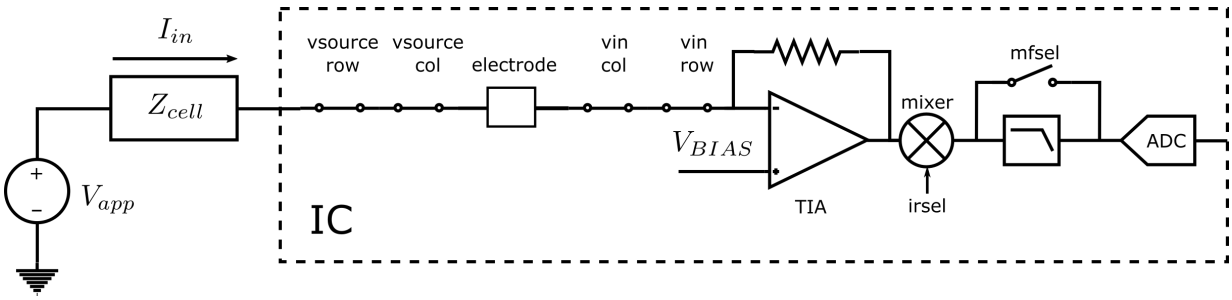


Figure 4.6: Default LIA test setup.

Electrical tests are run on the LIA in order to obtains the following results: (1) transfer characteristic at a fixed input sinusoidal frequency, (2) magnitude of the frequency response, (3) phase of the frequency response, (4) input-referred noise PSD, and (5) crosstalk. These tests are run on the 82 non-test channels, and in some cases, only the 39 non-test channels in $MEA1$. All channels operate simultaneously, but are individually tested unless otherwise specified.

4.4.1 Transfer Characteristic

The first test is plotting input current versus filtered output ADC code at a frequency of 10 kHz. This is done for both real and imaginary signals paths. The result for the I signal path is shown in Figure 4.7, and for the Q signal path is shown in Figure 4.8.

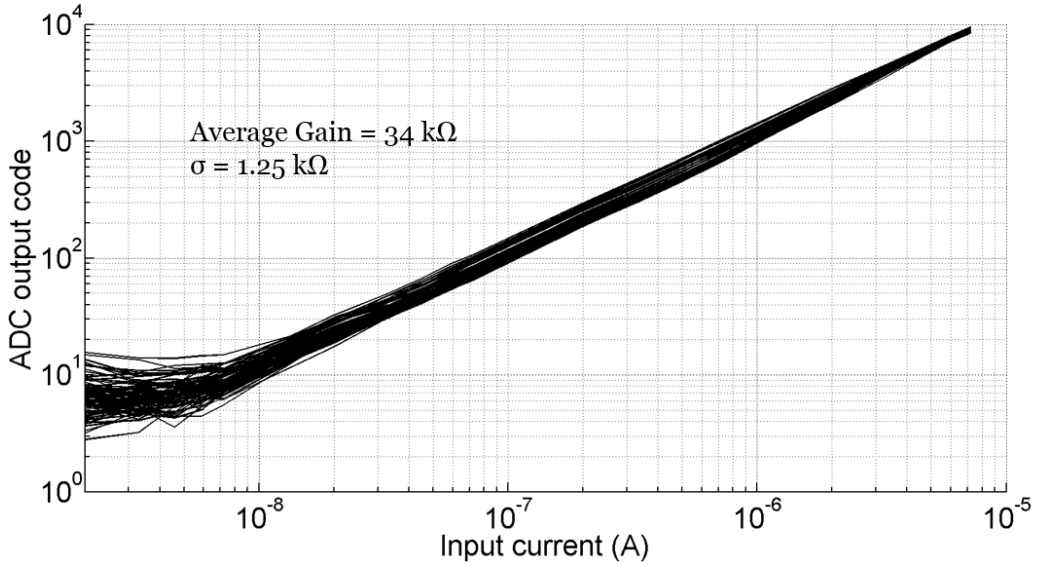


Figure 4.7: Measured real output versus input current at 10 kHz.

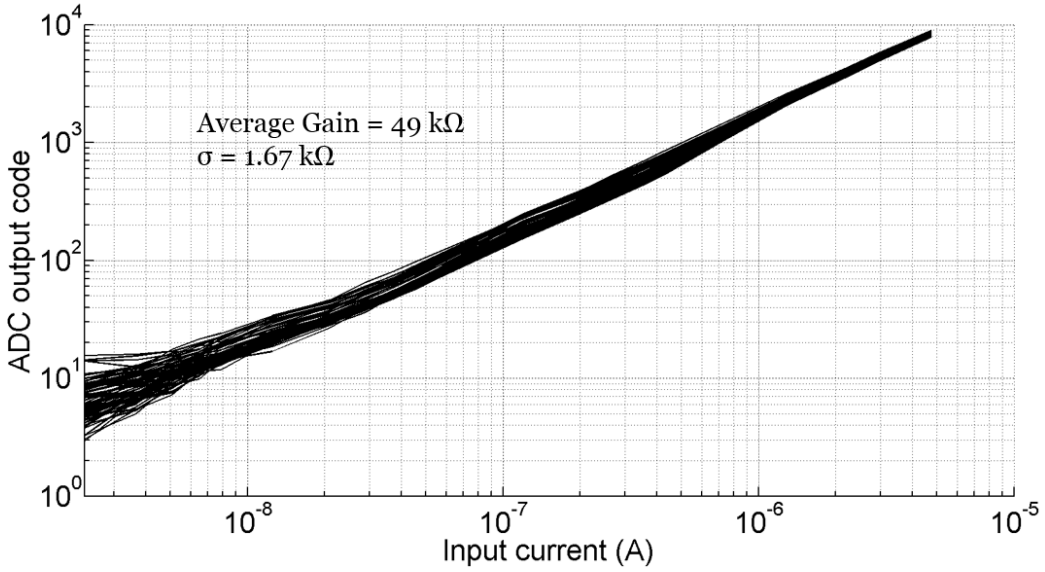


Figure 4.8: Measured imaginary output versus input current at 10 kHz.

The plots include input sinusoids having amplitudes of up to 7.2 μA_p, which covers a

cell impedance as small as 1.388 kΩ. As the switch resistance is significantly greater than 388 Ω, this verifies that a 1 kΩ impedance can be measured by the LIA. The range of input currents are obtained from selecting multiple impedance values (resistors or capacitors), as well as changing the amplitude of V_{app}. The low input saturation is caused by the attenuation of I_{in} from parasitic capacitors when large impedances >10 MΩ are placed on the PCB. From the plots it also observed that the average gain of 34 kΩ for the channels is lower than the designed value of 60 kΩ. The investigation of this reduced gain issue is described in Section 4.4.5. To characterize the linearity of the system the R^2 for each of the channels is computed and the average is taken over all channels from 7.2 nA to 7.2 μA. The average R^2 for the real and imaginary transfer curves are 0.9994 and 0.9996, respectively. These results give a percent error similar to a quantization error similar to that of a 11-bit ADC which is 0.0005. This low performance is due to the limited accuracy of V_{app} and tolerance on passive components (which are less than 16-bit accuracy). To obtain better characterization more accurate measurements need to be done.

4.4.2 Magnitude and Phase Response

In the next test, the filtered output magnitude and phase for real signals (at an I_{in} of 4.5 μA_p) is measured. The output magnitude versus frequency is shown in Figure 4.9 and the phase versus frequency is shown in Figure 4.10.

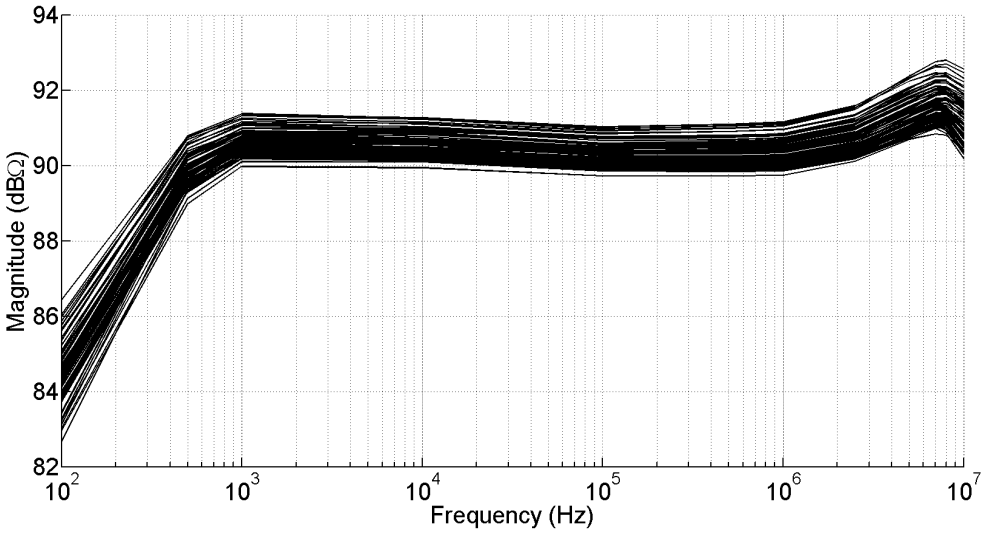


Figure 4.9: Measured filter output magnitude versus frequency at 4.5 μA_p.

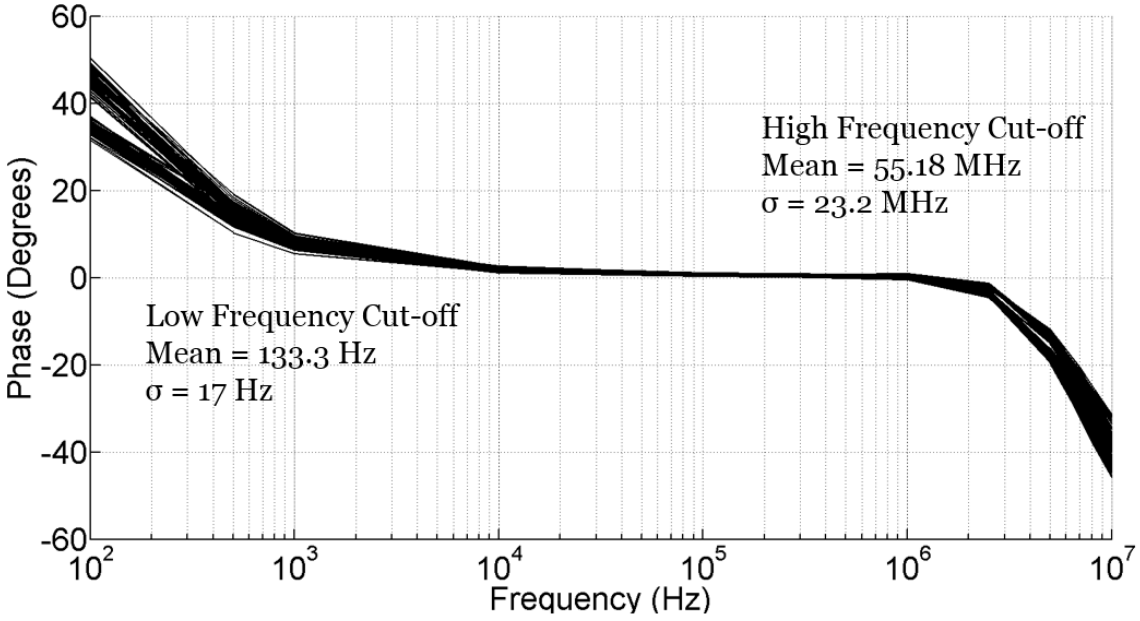


Figure 4.10: Measured filter output phase versus frequency at 4.5 μA_p.

The magnitude response over frequency also indicates that the gain is lower than expected, with a standard deviation of 1.217 kΩ across 82 channels at 10 kHz. To obtain the low-frequency and high-frequency cut-off, the phase at 1 kHz and 2.5 MHz, and a first-order approximation are used. The low-frequency cut-off is higher than expected by 33 Hz, but it is still adequate for having sufficient gain at the lowest operating frequency. The high-frequency cut-off estimate varies across channels more significantly than the lower cut-off frequency. This is likely caused by the coupling or feed-through which occurs at frequencies greater than 2 MHz, as seen by the significant change in output voltage in Figure 4.9.

4.4.3 Noise

The next test obtains the LIA input-referred current noise. The integrated input-referred noise is plotted versus mixing frequency for six-point averaging and without averaging for two different test setups. In the first setup, all selection switches are open, which leaves the inputs channels at high impedance as shown in Figure 4.11.

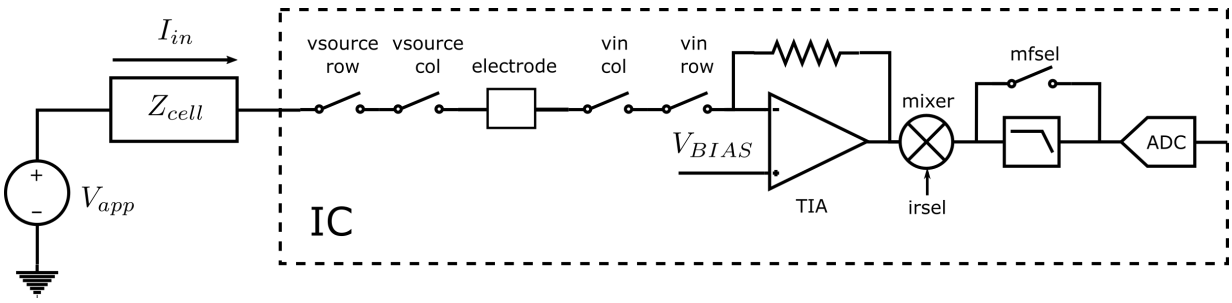
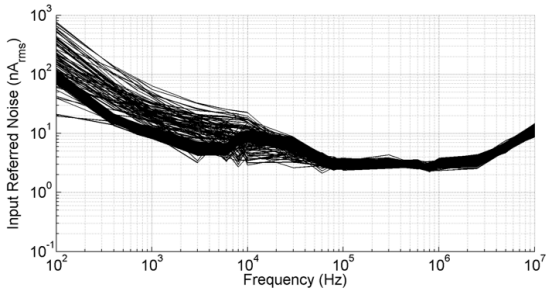
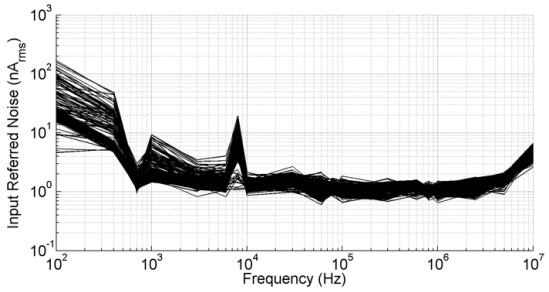


Figure 4.11: LIA noise test setup.

The results are shown in Figure 4.12 and capture any LIA noise and internal feed-through within the LIA itself. This result, as well as all other input-referred noise versus frequency results, are an integrated result versus frequency. This indicates that input-referred noise is either an up or down-converted noise from the input at a particular mixing frequency.



(a) Without averaging

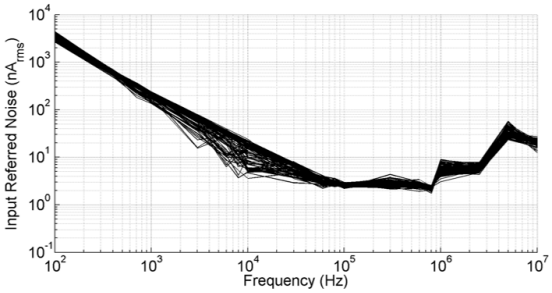


(b) 6 point averaging

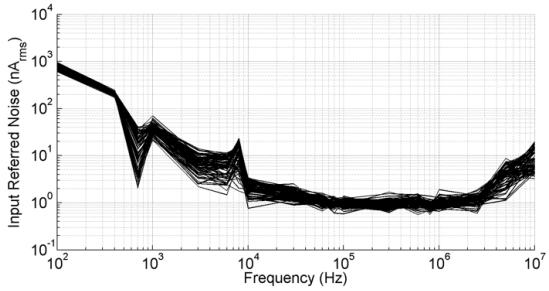
Figure 4.12: Measured LIA input-referred current noise versus mixing frequency for disconnected inputs.

As observed in Figure 4.12, the non-averaged input-referred noise is significantly higher than the averaged noise, especially over the 7 to 12 kHz range. When averaging is implemented, noise peaks at 1 kHz and 8 kHz are visible in Figure 4.12b. This could be caused by coupling into V_{ramp} for the ADC or V_{BIAS} for the TIA.

The second test setup uses the same default configuration as in Figure 4.11, which connects the LIA input to the PCB which contains a passive circuit with a dc level applied. The results are shown in Figure 4.13. These results include any noise, feed-through and coupling for both the LIA and the PCB and its components.



(a) Without averaging



(b) 6 point averaging

Figure 4.13: Measured LIA input-referred current noise versus mixing frequency for connected inputs.

The input-referred noise is higher at low mixing frequencies because the 1/f noise contribution is higher. This indicates that there is significant noise contribution from the components on the PCB or the function generator. There is still a peak in noise at 1 kHz and 8 kHz. A histogram of the LIA input-referred noise of each channel with 6 point averaging and no averaging is shown in Figure 4.14 at a mixing frequency of 600 kHz to show noise variation across the 82 non-test channels.

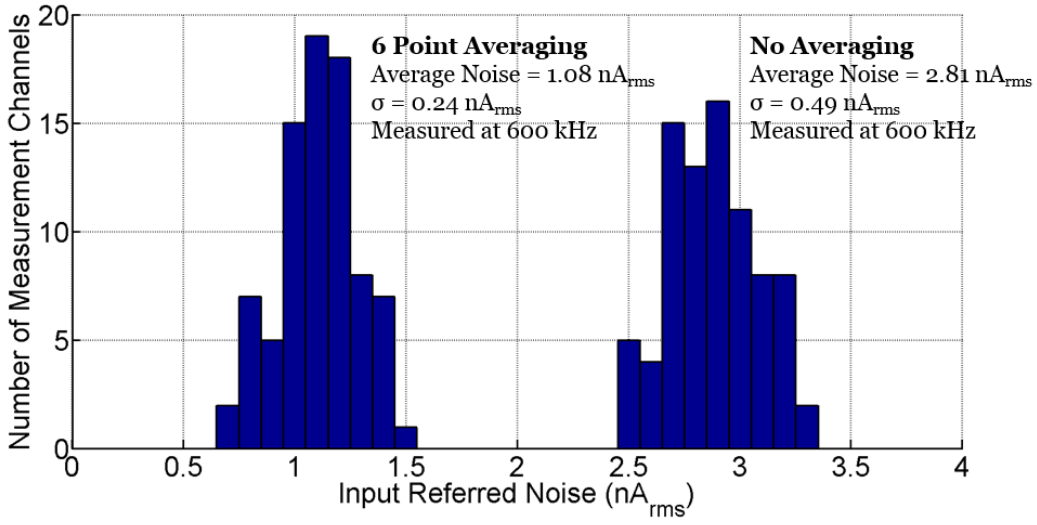


Figure 4.14: Measured LIA input-referred noise with 6 point averaging and no averaging measured at a mixing frequency of 600 kHz.

With 6-point averaging, the LIA input-referred noise has an average of 1.08 nA$_{rms}$ across channels at 600 kHz. To further reduce the noise of the system to reach noise levels below 1 nA$_{rms}$, additional averaging can be done at the cost of frame rate. For example, with 24-point averaging, the frame rate would become 0.0084 Hz, which results in only 5 frequency points being taken to meet the frame rate criteria. A histogram of the input-referred noise of each channel with 24-point averaging and no averaging is shown in Figure 4.15 at a mixing frequency of 600 kHz. This leads to an average noise of 0.618 nA$_{rms}$. The theoretical calculation for noise reduction results in an average noise of 0.574 nA$_{rms}$. Therefore, the 24-point averaging has an effective reduction of 21-point averaging. This discrepancy could be caused by the noise samples not being normally distributed or

correlation between samples.

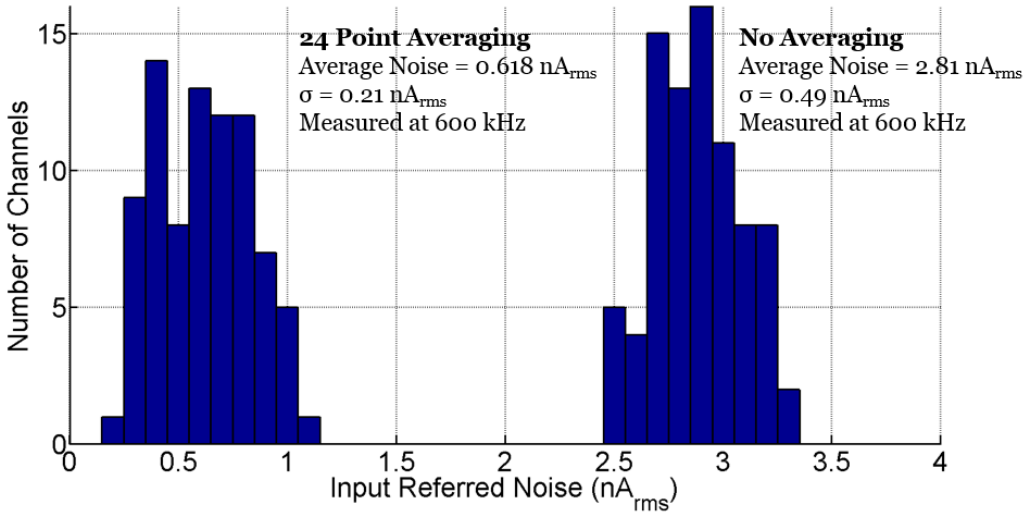
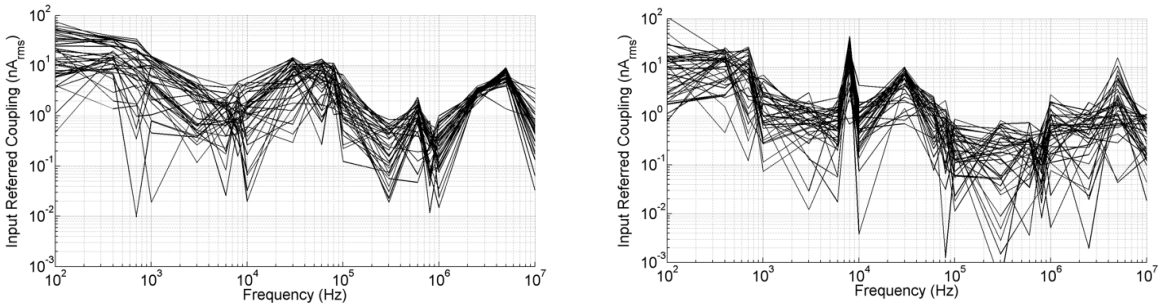


Figure 4.15: Measured LIA input-referred noise at 600 kHz with 24 point averaging.

4.4.4 Crosstalk

Since multiple channels operate simultaneously during normal operation of the camera IC, a crosstalk test is done to determine the extent of crosstalk between channels. To obtain channel crosstalk, an 8 μA$_p$ signal is applied to one channel (called the "aggressor channel"). This is higher than the expected I_{in} with a 1 kΩ source impedance. Using this value would indicate a possible worst-case coupling condition, in which there would be a near 0 Ω Z_{cell} impedance and the series switches would establish the current limit. A "victim" channel adjacent to the aggressor is set with its input floating. The extent of coupling is then measured by the victim channel. Since the LIA input-referred noise dominates over the coupling, noise is subtracted from the results to obtain the input-referred coupling. This method is subject to possible inconsistencies or variation as the noise measurement is taken separately from the coupling measurement. The 6 point averaging and no averaging result for 39 non-test channels in $MEA1$ are shown in Figure 4.16.



(a) Without averaging

(b) 6-point averaging

Figure 4.16: Measured LIA input-referred coupling from filtered output.

Similar to the input-referred noise measurements, the coupling exhibits a spike at 8 kHz which is the same case as the noise measurements. They also exhibit a spike at 12 kHz. With the exception of the 8 kHz spike, the maximum amount of coupling between channels over the intended operating frequency is 10 nA$_{rms}$.

4.4.5 Low-Gain Investigation

To investigate the low gain from the filtered output that was measured in Figure 4.17, the filter is bypassed as shown in Figure 4.17 and new measurements are made. In this setup, the dc component of the output signal sinusoid is obtained by sapling the output 188 times and then averaging.

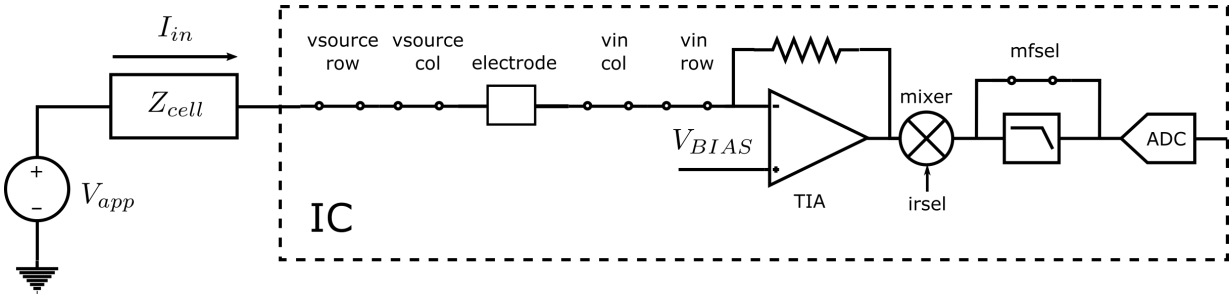


Figure 4.17: LIA with LPF bypassed test setup.

The mixer output magnitude versus frequency is shown in Figure 4.18 and the phase versus frequency is shown in Figure 4.19 at an input current of 4.5 μA_p.

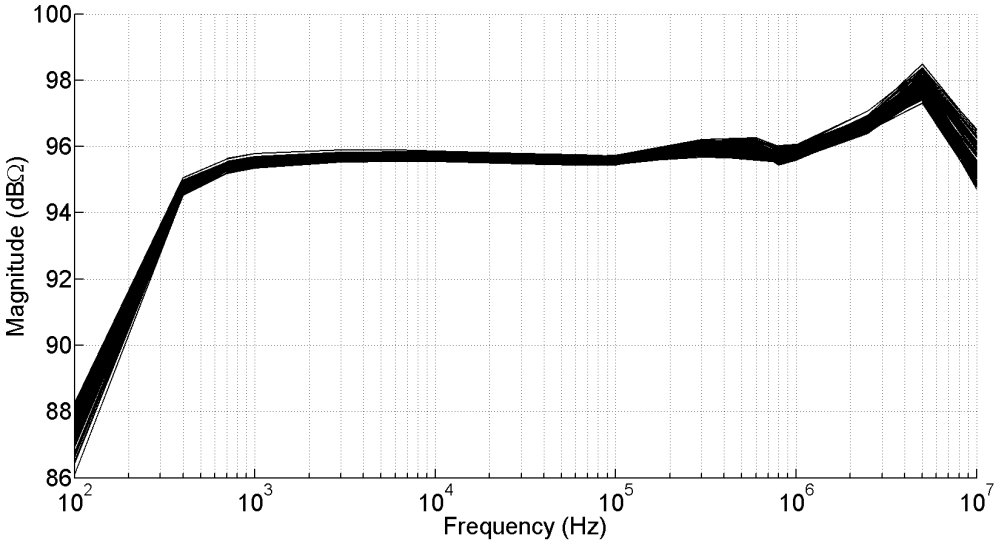


Figure 4.18: Measured mixer output magnitude versus frequency at an input current of 4.5 μA_p.

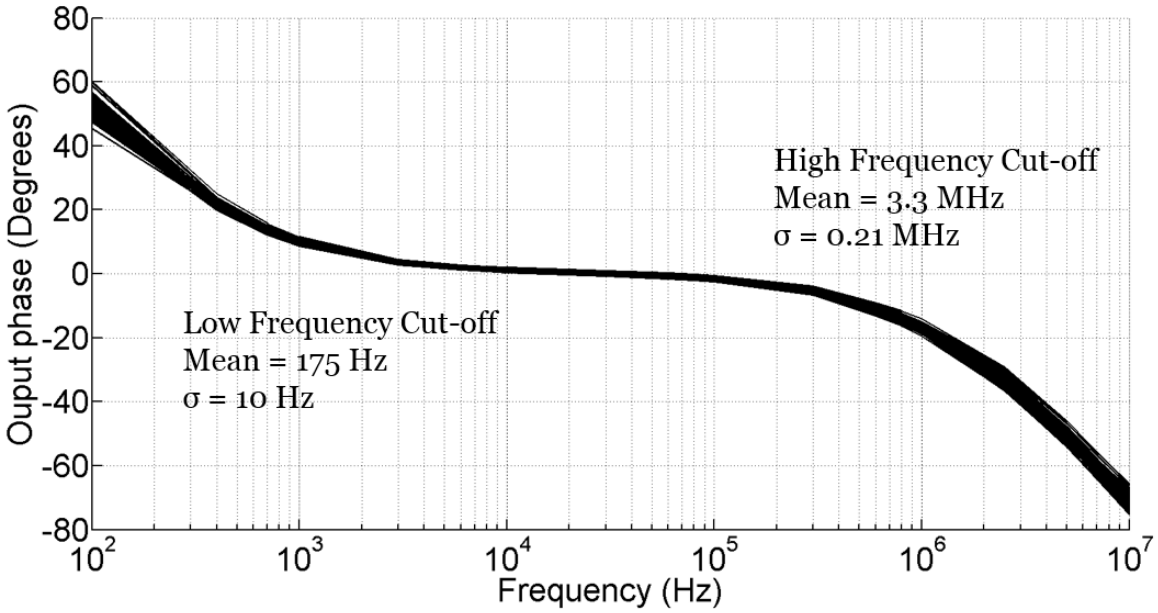
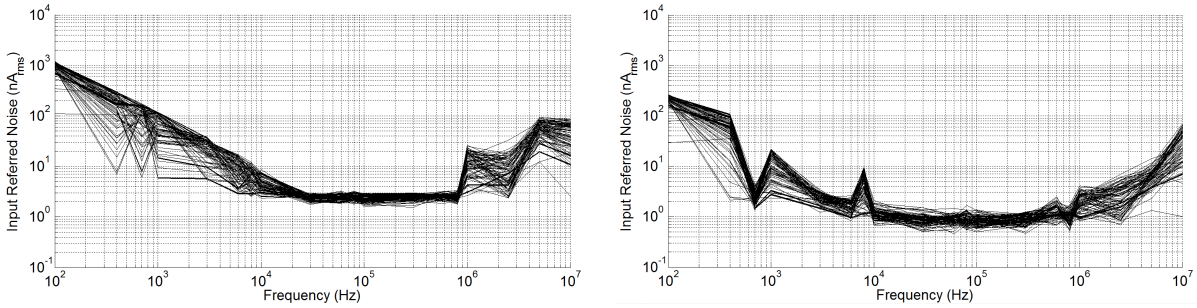


Figure 4.19: Measured mixer output phase versus frequency at an input current of 4.5 μA_p.

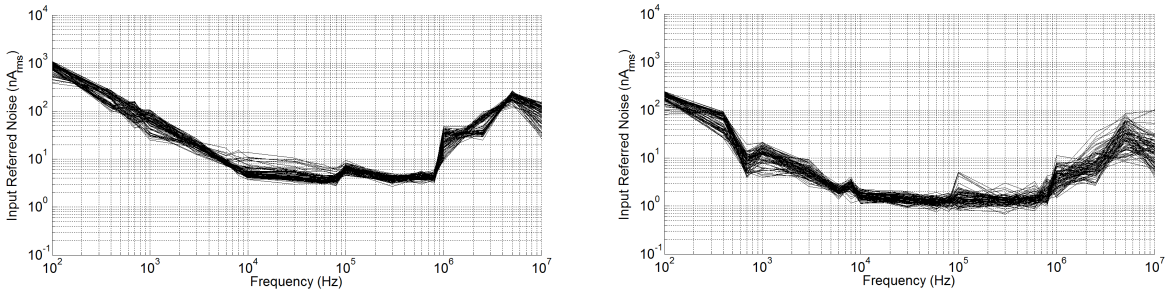
The average gain of the channels from the mixer output at 62.1 kΩ has an error of only 3.5% from the designed value. The between-channel gain deviation is also significantly less than the filtered output. This indicates that there is an attenuation that happens from filter input to output during normal operation with the filter activated. The input-referred noise from the mixer output is plotted against mixing frequency for 6 point averaging and no averaging using the test setup in Figure 4.6 with the mixer output selected. The results are shown in Figure 4.20. These results capture any channel noise and internal feed-through within the channel itself.



(a) No averaging (b) 6 point averaging

Figure 4.20: Measured LIA input-referred noise versus mixing frequency for disconnected inputs.

The noise is higher than the filtered output at frequencies less than 2 kHz and frequencies greater than 1 MHz. The second case test setup as in Figure 4.11 is used with no applied sinusoidal voltage. The results are shown in Figure 4.21. This result includes any noise, feed-through and coupling for both the internal IC input paths and the PCB.



(a) No averaging (b) 6 point averaging

Figure 4.21: Measured LIA input-referred noise versus mixing frequency for connected inputs.

The result from the mixer output in general has lower input-referred noise. This is largely due to the elimination of the filter $\frac{kT}{C}$ noise and increase in the channel gain. A histogram of the input-referred noise of the mixer output of each channel with 6 point averaging and no averaging is shown in Figure 4.22 at a mixing frequency of 600 kHz.

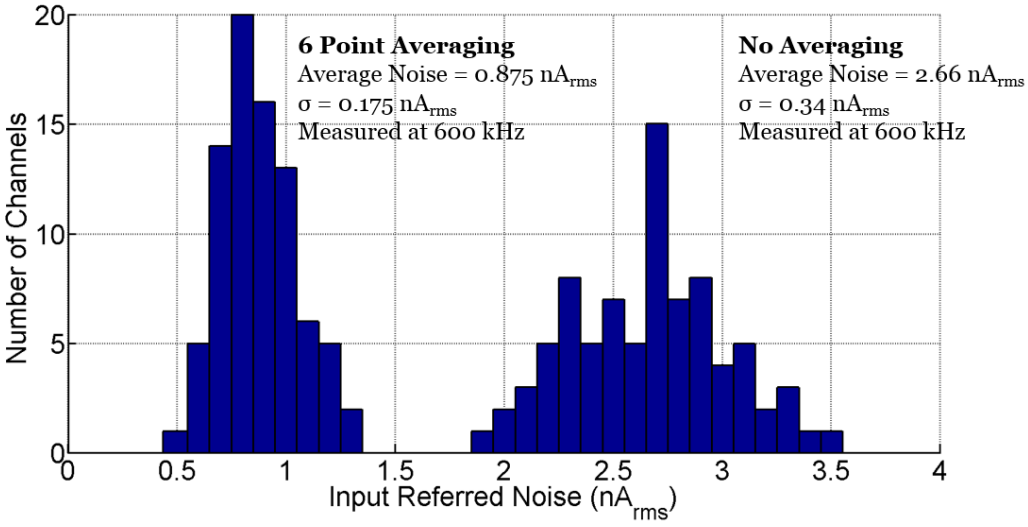


Figure 4.22: Measured LIA input-referred noise at 600 kHz input signal frequency with 6 point averaging.

As seen, the noise is significantly less than the filter output case. A histogram of the input-referred noise of each channel with 24 point averaging and no averaging is shown in Figure 4.23 at a mixing frequency of 600 kHz. Which again is significantly lower.

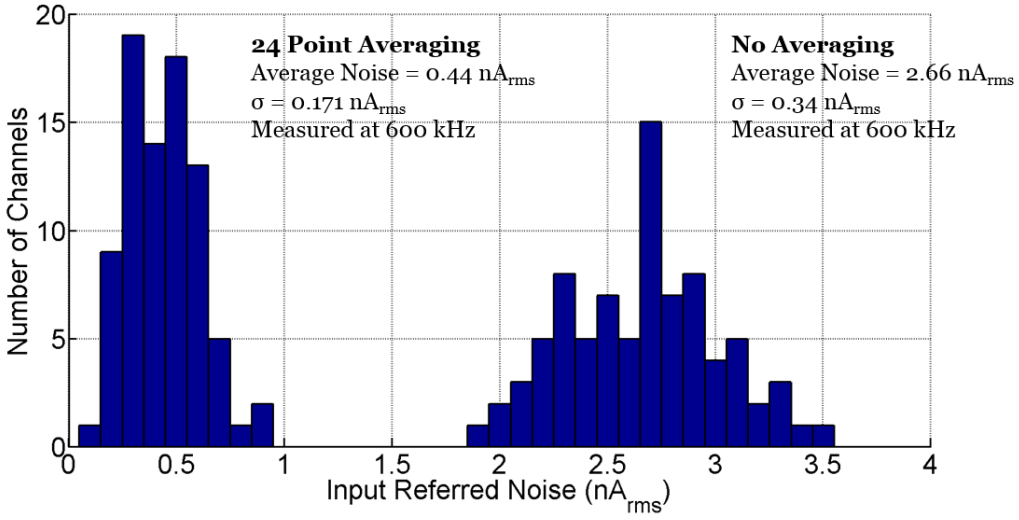
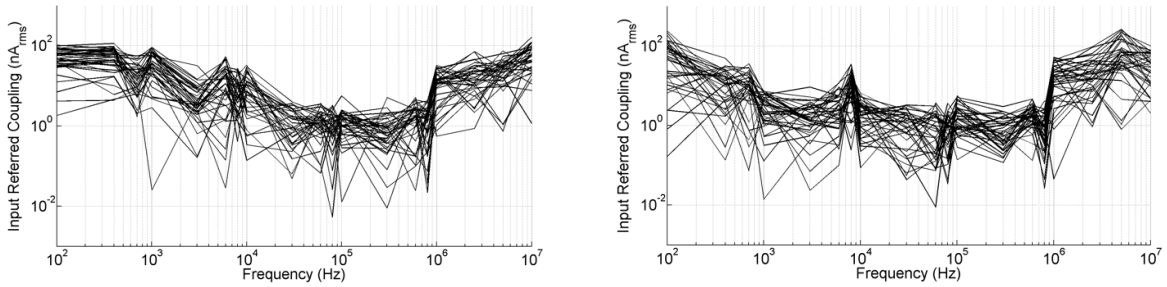


Figure 4.23: Measured LIA input-referred noise at 600 kHz input signal frequency with 24 point averaging.

The mixer output coupling result for the 39 non-test channels in $MEA1$ are shown in Figure 4.24 at a 8 μA_p signal. The coupling is similar to the filtered output which is as expected.



(a) No averaging

(b) 6 point averaging

Figure 4.24: Measured LIA input-referred coupling from mixer output.

To further examine the attenuation caused by the filter, the two on-chip test channels are examined. Both test channels have significantly lower cut-off frequency, which is expected due to the additional loading on internal circuit nodes. However, both channels

have a gain of approximately 54 kΩ with the filter active, which is much closer to the designed value. Further investigation such as investigating potential substrate voltage divider or observing the test channels with not external connection needs to be done to pinpoint the cause of attenuated gain on internal channels.

4.4.6 Cell Impedance Modelling

To simulate the camera response to a cell, a passive circuit model is made using resistors and capacitors on the PCB, as in Figure 1.2. The full interface model in Figure 1.6 is not used R_p and C_{dl} are large enough over the range of operating frequencies that it does not significantly affect the measurement result. In order to obtain an accurate result, the camera IC needs to be calibrated. To calibrate phase offset θ and gain mismatch x, additional terms are introduced into (1.8) and (1.7), as shown below:

$$\mid Z(j\omega) \mid = \frac{V_{app} \cdot A_{sys}}{\sqrt{V_I^2 + xV_Q^2}} \tag{4.2}$$

$$\angle Z(j\omega) = tan^{-1}(\frac{xV_Q}{V_I}) + \theta. \tag{4.3}$$

Variables A_{sys}, θ and x are quantified by applying an input sinusoid with known amplitude and phase. For 84 channels, the measured impedance for $R_m = 50$ kΩ, $R_s = 5$ kΩ, and $C_m = 200$ pF over the frequency range of 1 kHz to 1 MHz is shown as a Nyquist plot in Figure 4.25, and magnitude and phase in Figures 4.26 and 4.27, respectively.

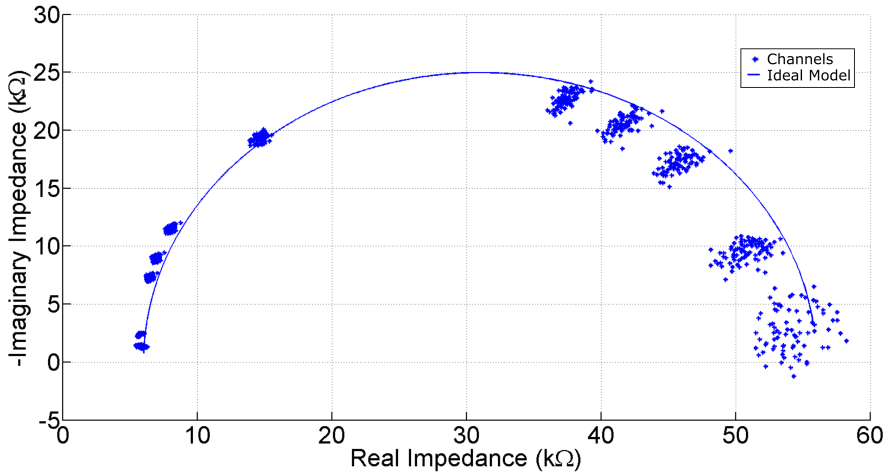


Figure 4.25: Measured and ideal cell model Nyquist plot for 82 channels.

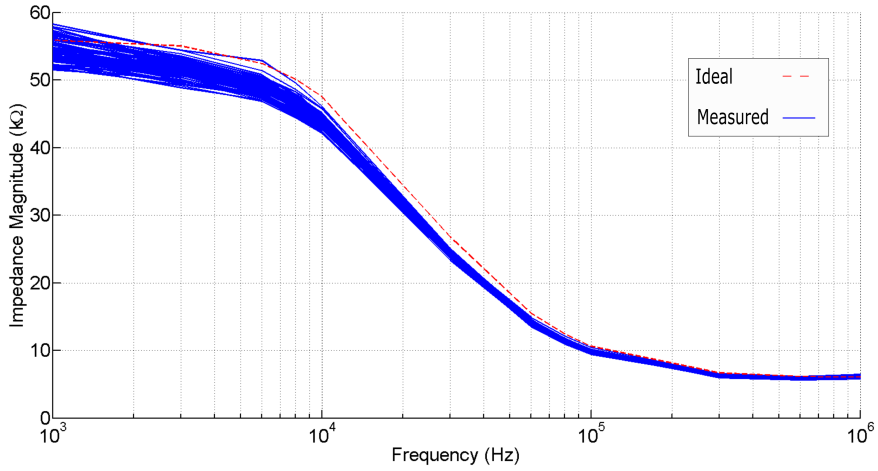


Figure 4.26: Measured and ideal cell model magnitude plot for 82 channels.

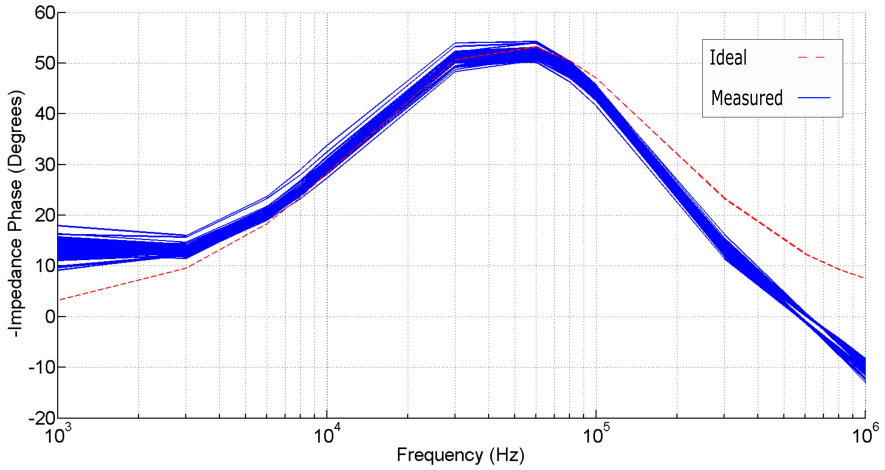


Figure 4.27: Measured and ideal cell model phase plot for 82 channels.

The maximum relative error in the magnitude response is 13% over 82 channels. The maximum relative error for phase is 170% at 1 kHz. This large relative phase error is expected as the noise is on the same order of magnitude as the imaginary input current and the tangent function is more sensitive to changes in phase close to zero. Similarly, at 1 MHz, the relative error is 77%. From 6 kHz to 600 kHz, the relative error is 20%.

To simulate simultaneous cell measurements, two adjacent channels are selected to measure two separate cell models on the PCB. For both models, $R_s = 10$ kΩ, $R_m = 50$ kΩ, and $C_m = 200$ pF. Figure 4.28 shows a Nyquist plot resulting from the test. The frequency is swept from 1 kHz to 1 MHz and obtains an accuracy better than 10.4% over the range.

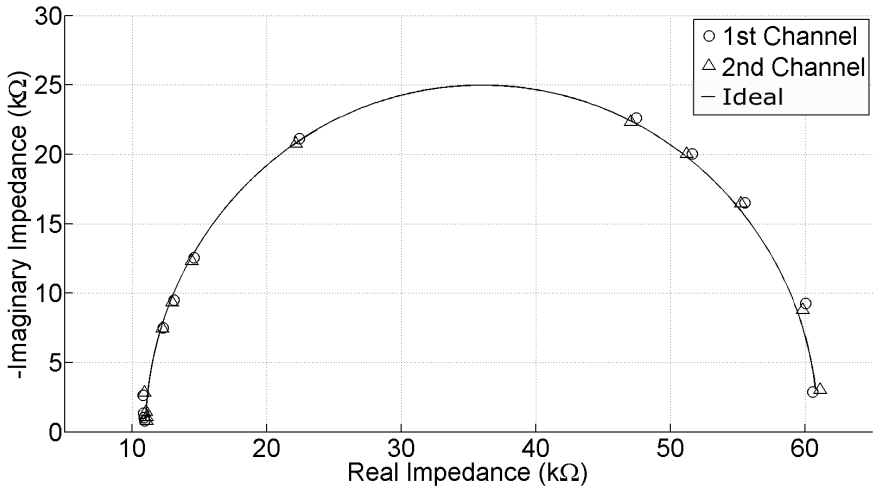


Figure 4.28: Measured and ideal cell model Nyquist plot for two adjacent channels.

4.5 Performance Summary

The camera's measured electrical performance is summarized and compared with previous work in Table 4.2. In addition to the area-readout FOM (FOM1), an additional LIA FOM (FOM2) is introduced to compare the LIA designed in this thesis with LIAs in previous work. FOM2 is given by $FOM2 = \frac{Power}{DR \cdot BW}$, where a lower value indicates better performance.

Reference	Manickam [27]	Jafari [36]	Liu [35]	Chi [10]	Viswam [40]	This Work
Architecture	TIA + Direct I/Q	SC TIA + Multiplying ADC	Lock-in + Counter	Direct I/Q	Lock-in + ΣΔ	Lock-in + Ramp ADC
On-chip LPF + ADC	No	Yes	Yes	No	Yes	Yes
Frequency Range	10 Hz-50 MHz	0.1 Hz-10 kHz	10 mHz-10 kHz	500 kHz-4 MHz	1 Hz-1 MHz	1 kHz-1 MHz
Dynamic Range (dB)	97	140 (3 mode)	80 (multi mode)	-	102	80
Channel Power (μW)	726	42	5.2	-	412	260
Electrode Size (μm^2)	40×40	55×55	100 dia	80×100	3.5×7 & 605×605	10×10 & 40×40
Electrode Pitch (μm)	100	300	-	-	13.5	20
No. of Electrodes	100	64	100	16	59760	2987
Input-Referred Noise	330 pA	320 fF	100 fA	-	6.4 pA	1.08 nA
Number of Channels	1	16	26	144	32	84
Channel Area (mm^2)	0.01	0.06	0.045	-	0.1	0.0192
Die Size (mm)	2×2	1.05×1.6	3×3	2.2×2.0	12×8.9	3×2.5
Frame Rate(Hz)	0.9	-	-	-	0.000568	0.0117
Technology (μm)	0.35	0.13	0.5	0.13	0.18	0.18
FOM1 (mm^{-2})	1	2.8	-	-	2.9	36
FOM2 ($\mu W/(dB \cdot Hz)$)	0.149	30	6.5	-	4.04	3.25

Table 4.2: Summary of measured camera performance and comparison to previous work.

The camera IC developed in this thesis achieves a significantly higher FOM1 compared to previous work, as well as the best FOM2 for LIAs with integrated ADC. These FOMs indicates a high spatial resolution and electrode readout efficiency with best LIA design. This is achieved by using a row-parallel architecture with an extremely compact LIA circuit. With the exception of [27], which does not contain an on-chip filter or ADC, this work's electronic circuits occupy the least amount of area. The camera IC developed in this work also achieves a significantly lower power consumption compared to other work at a similar BW. This is mainly because this work operates from a 1.8 V supply and other work operates from a 3.3 V supply. The noise and DR performance is not as good as the other work. Better DR and noise can be achieved at the cost of power and the maximum measurable input current being reduced. The simulation predicted the performance of the system specifications closely over most parameters. The exceptions to this are the reduced gain from output of the filter, external coupling, and noise being slightly worse than expected. Additional simulation could be done to observe the effect of off-chip signals coupling in to the ADC as well as providing an increased margin for noise performance to account for simulation inaccuracy.

Chapter 5

Conclusion and Future Work

This thesis presented a novel CMOS impedance camera IC for characterizing biological cells. It described the design of an LIA used in the acquisition channels in the camera IC and also described the experimental setup and characterization of the camera. The camera achieves a 1 kHz-to-1 MHz operating frequency and an input-referred noise of 1.08 nA_{rms} at 600 kHz with 6 point averaging. The camera meets all of the specifications, with exception of the system gain. The reduction in system gain from the LPF increases the LOD, from 0.46 nA_{rms} to 0.8 nA_{rms}. Since this is still below the targeted 1 nA_p LOD, it is not a major problem. This CMOS electrochemical impedance camera can also be used to obtain a impedance image of any sub-millimetre-diameter object to a 20 μm resolution.

5.1 Future Work

The following list summarizes the improvements that could be made in the next generation of CMOS camera:

- Investigate package pinout to make sure that sensitive analog signals, such as V_{app}, are not located close to switching signals such as V_{LO}. Additionally, add more on-chip shielding to reduce coupling between channels.

- Use an alternative to weak-inversion PMOS transistors as a source of resistance for the LPF. An alternative could be to use transistors with a controlled gate voltage.
- Implement a fully differential LIA to reduce noise and crosstalk.
- Using a high speed ADC instead of on-chip LPF could be implemented to increase frame rate.
- Add switches to test channels to disconnect the internal nodes from external capacitances. The effect of external capacitance on various nodes could then be examined.
- Redesign PCB to add additional shielding and filters to reduce coupling and noise.

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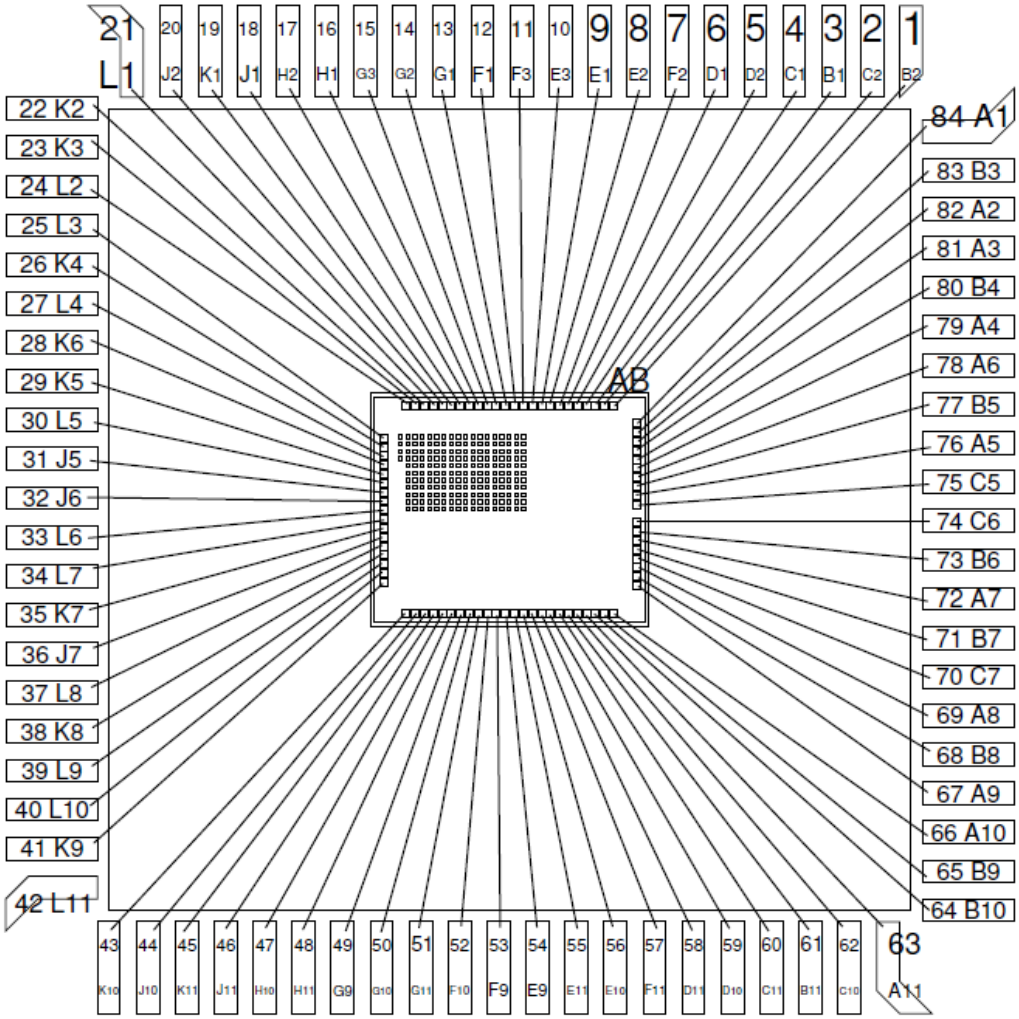
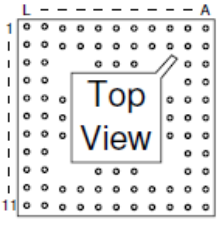
APPENDICES

Appendix A

Bonding Diagram and I/O Pin Descriptions



Qty: 5	V7AS-AB	PGA84M
	(96614)	
Customer Providing Diagram		
Minimum pad size: 85 x 85; minimum pad pitch: 100 um		
MOSIS	Design_name: WTLI1 - 1702CF	
	Customer Account: 244	
	Die Size: 3074 x 2604 um	
	Die Rotation in Cavity: None	
	Cavity Size: 8890 um x 8890 um	29-NOV-2017 10:05:08

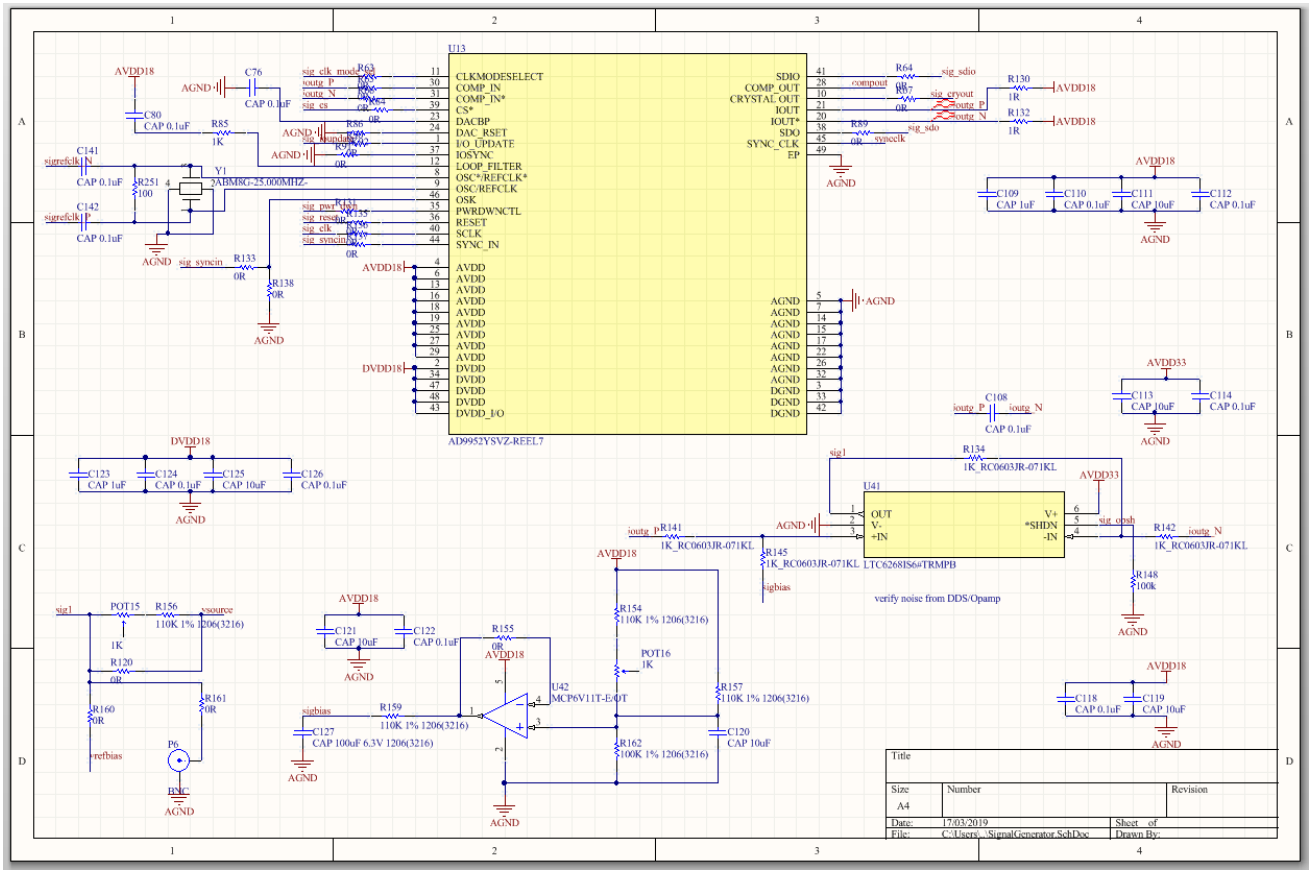


PIN	SIGNAL	ANA/ANA-DIG/DIG	I/O/PWR/GND	Description
1	voutp40	ANA	O	positive output of latch for 40x40 electrodes test channel
2	voutn40	ANA	O	negative output of latch for 40x40 electrodes test channel
3	compnin40	ANA	O	negative comparator input for 40x40 electrodes test channel
4	avdd	ANA	PWR	Analog Power 1.8 V
5	avdd	ANA	PWR	Analog Power 1.8 V
6	avss	ANA	GND	Analog Ground
7	avss	ANA	GND	Analog Ground
8	compbias40	ANA	I	Tail current for ADC comparators of 40x40 electrode channels, 0.472 V
9	mixbias40	ANA	I	Tail current for mixers of 40x40 electrode channels, 0.4756 V
10	diffbias40	ANA	I	Tail current for TIA diffpair of 40x40 electrode channels, 0.5144 V
11	curbufbias40	ANA	I	Tail current for TIA current buffer of 40x40 electrode channels, 0.405 V
12	voffset40	ANA	I	Tail current for TIA offset of 40x40 electrode channels, 1.8 V
13	vsource	ANA	I/O	Input for one of the Vapp signals
14	vref	ANA	I/O	Input for one of the Vapp signals
15	vtran40	ANA	O	output of TIA for 40x40 electrode test channel
16	mixin40	ANA	O	output of TIA filter for 40x40 electrode test channel
17	compnout40	ANA	O	negative output of comparator for 40x40 electrode test channel
18	comppout40	ANA	O	positive output of comparator for 40x40 electrode test channel
19	comppin40	ANA	O	positive input of comparator for 40x40 electrode test channel
20	scrowvinout	ANA-DIG	O	vin row scanchain output
21	scrowvsourceout	ANA-DIG	O	vsource row scanchain output
22	scrowvrefouT	ANA-DIG	O	vref row scanchain output
23	clktn	ANA	I	negative clock input for experimental electrodes
24	clkt	ANA	I	positive clock input for experimental electrodes
25	in1	ANA	I	input for experimental electrodes
26	out1	ANA	O	output for experimental electrodes
27	in2	ANA	I	input for experimental electrodes
28	out2	ANA	O	output for experimental electrodes
29	in3	ANA	I	input for experimental electrodes
30	out3	ANA	O	output for experimental electrodes
31	in4	ANA	I	input for experimental electrodes
32	out4	ANA	O	output for experimental electrodes
33	sccolvsourceout	ANA-DIG	O	vsource col scan chain output
34	sccolvrefout	ANA-DIG	O	vref col scanchain output
35	sccolvinout	ANA-DIG	O	vin col scanchain output
36	sccolvsourcein	ANA-DIG	I	vsource col scanchain input
37	sccolvrefin	ANA-DIG	I	vref col scanchain input
38	sccolvinin	ANA-DIG	I	vin col scanchain input
39	scrowvrefin	ANA-DIG	I	vref row scanchain input
40	scrowvsourcein	ANA-DIG	I	vsource row scanchain input
41	scrowvinin	ANA-DIG	I	vin row scanchain input
42	NC	ANA	N/A	No Connection

PIN	SIGNAL	ANA/ANA-DIG/DIG	I/O/PWR/GND	Description
43	holdv	ANA-DIG	I	state for all switches when scoutsel = 1, 1-on, 0-off
44	scoutsel	ANA-DIG	I	selection for switches states to be controlled by holdv or scanchains, 1-holdv, 0-scanchains
45	rnrowcolsc	ANA-DIG	I	active low reset for row and column select scanchains
46	rowcolscclk	ANA-DIG	I	row and column scanchains clock
47	vtran	ANA	O	output of TIA for 10x10 electrodes test channel
48	mixin	ANA	O	output of TIA filter for 10x10 electrodes test channel
49	comppin	ANA	O	poistive input of ADC comparator for 10x10 electrodes test channel
50	comppout	ANA	O	postive output of ADC comparator for 10x10 electrodes test channel
51	compnout	ANA	O	negative output of ADC comparator for 10x10 electrodes test channel
52	vbias	ANA	I	voltage bias for the TIA, 0.715 V
53	vref	ANA	I	Input for one of the Vapp signals
54	vsource	ANA	I	Input for one of the Vapp signals
55	voffset	ANA	I	Tail current for TIA offset of 10x10 electrode channels, 1.8 V
56	curbufbias	ANA	I	Tail current for TIA current buffer of 10x10 electrode channels, 0.406 V
57	diffbias	ANA	I	Tail current for TIA diffpair of 10x10 electrode channels, 0.5148 V
58	mixbias	ANA	I	Tail current for mixers of 10x10 electrode channels, 0.4756 V
59	compbias	ANA	I	Tail current for ADC comparators of 10x10 electrode channels, 0.473 V
60	avss	ANA	GND	Analog Ground
61	avss	ANA	GND	Analog Ground
62	avdd	ANA	PWR	Analog Power 1.8 V
63	avdd	ANA	PWR	Analog Power 1.8 V
64	compnin	ANA	O	negative input of ADC comparator for 10x10 electrodes test channel
65	vramp	ANA	I	Voltage ramp input
66	voutn	ANA	O	negative output of ADC latch for 10x10 electrodes test channel
67	voutp	ANA	O	positive output of ADC latch for 10x10 electrodes test channel
68	mfsel	ANA-DIG	I	selection for ADC to sample mixer output or filter output, 1-filter output, 0-mixer output
69	irsel	ANA-DIG	I	selection for ADC to sample real or imaginary outputs, 1-real output, 0-imaginary output
70	vlat	ANA-DIG	I	clock for latch
71	lopr	ANA	I	positive input for mixer switching devices of real path
72	lonr	ANA	I	negative input for mixer switching devices of real path
73	lopi	ANA	I	positive input for mixer switching devices of imaginary path
74	loni	ANA	I	negative input for mixer switching devices of imaginary path
75	dvss	DIG	GND	Digital Ground
76	dvdd	DIG	PWR	Digital Power 1.8 V
77	cclk	DIG	I	clock for counter
78	scanoutn	DIG	O	output of PISO for negative ADC output
79	scanoutp	DIG	O	output of PISO for positive ADC output
80	rndig	DIG	I	reset for digital circuits
81	scaninp	DIG	I	input of PISO for positive ADC output
82	scaninn	DIG	I	input of PISO for negative ADC output
83	clk	DIG	I	clock for digital blocks
84	ws	DIG	I	selection for PISO write or shift, 1-write, 0-shift

Appendix B

Schematics


U13
AD9952YSVZ-REEL7
CLKMODESELECT
COMP_IN
COMP_IN*
CS*
DACBP
DAC_RSET
I/O_UPDATE
IOSYNC
LOOP_FILTER
OSC*/REFCLK*
OSC/REFCLK
OSK
PWRDWNCTL
RESET
SCLK
SYNC_IN
AVDD
DVDD
DVDD_I/O
SDIO
COMP_OUT
CRYSTAL_OUT
IOUT
IOUT*
SDO
SYNC_CLK
EP
AGND
DGND
U41
LTC6268IS6#TRMPB
OUT
V-
+IN
V+
*SHDN
-IN
U42
MCP6V11T-E/OT
Y1
25ABM8G-25.000MHZ-
AVDD18
AVDD33
DVDD18
AGND
sig_clk_mode
sig_cs
sig_sdio
sig_sdo
sig_cryout
sig_pwr_dwn
sig_reset
sig_clk
sig_syncin
sigrefclk_N
sigrefclk_P
sig1
sigbias
ioutg_P
ioutg_N
verify noise from DDS/Opamp
Title
Size
A4
Number
Revision
Date:
17/03/2019
Sheet of
File:
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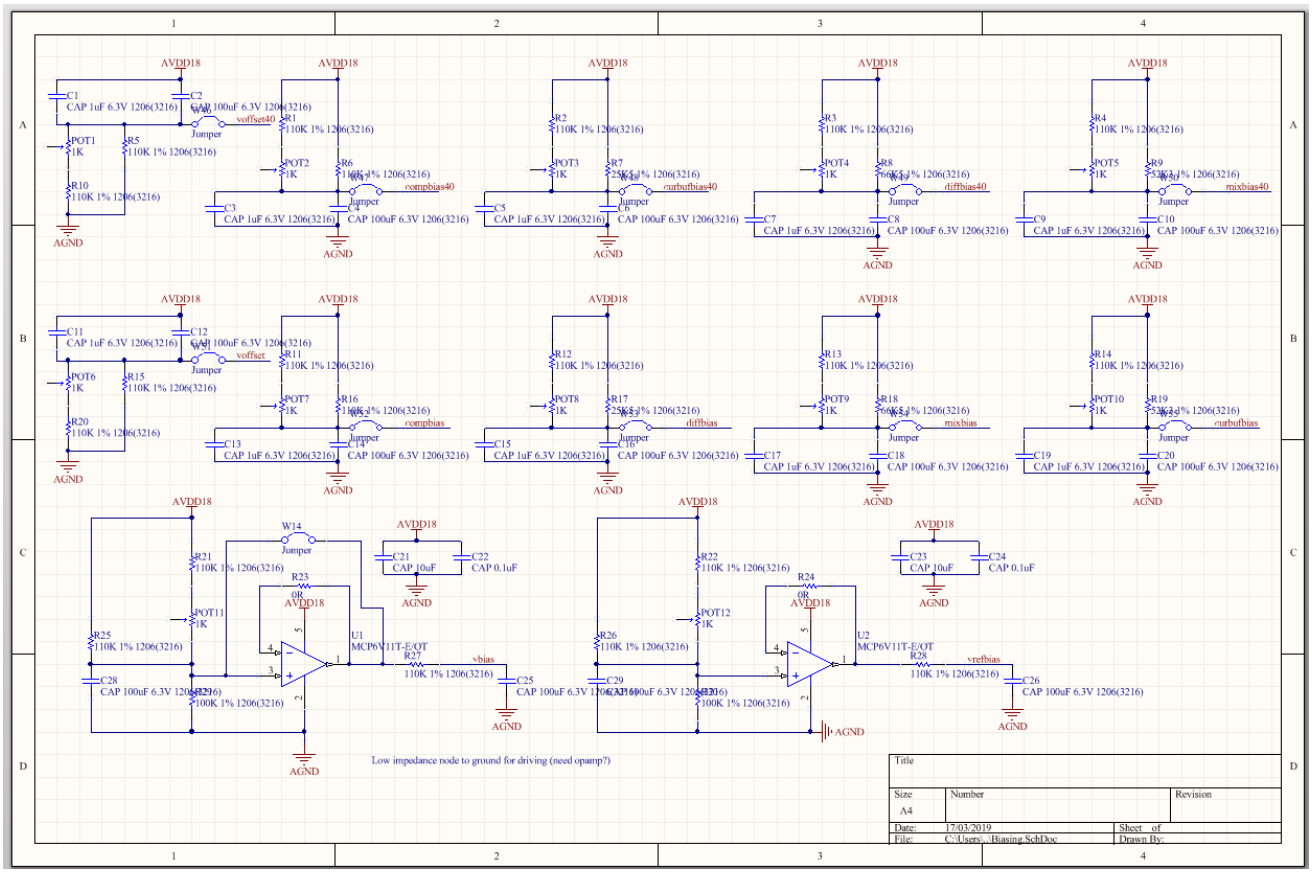
Drawn By:


AVDD18
AGND
C1
CAP 1uF 6.3V 1206(3216)
C2
CAP 100uF 6.3V 1206(3216)
W13
Jumper
voffset40
R1
110K 1% 1206(3216)
POT1
1K
R5
110K 1% 1206(3216)
R10
110K 1% 1206(3216)
POT2
1K
R6
110K 1% 1206(3216)
C3
CAP 1uF 6.3V 1206(3216)
C4
CAP 100uF 6.3V 1206(3216)
R2
110K 1% 1206(3216)
POT3
1K
R7
110K 1% 1206(3216)
C5
CAP 1uF 6.3V 1206(3216)
C6
CAP 100uF 6.3V 1206(3216)
R3
110K 1% 1206(3216)
POT4
1K
R8
110K 1% 1206(3216)
C7
CAP 1uF 6.3V 1206(3216)
C8
CAP 100uF 6.3V 1206(3216)
R4
110K 1% 1206(3216)
POT5
1K
R9
110K 1% 1206(3216)
C9
CAP 1uF 6.3V 1206(3216)
C10
CAP 100uF 6.3V 1206(3216)
C11
CAP 1uF 6.3V 1206(3216)
C12
CAP 100uF 6.3V 1206(3216)
W12
Jumper
voffset
R11
110K 1% 1206(3216)
POT6
1K
R15
110K 1% 1206(3216)
R20
110K 1% 1206(3216)
POT7
1K
R16
110K 1% 1206(3216)
C13
CAP 1uF 6.3V 1206(3216)
C14
CAP 100uF 6.3V 1206(3216)
R12
110K 1% 1206(3216)
POT8
1K
R17
110K 1% 1206(3216)
C15
CAP 1uF 6.3V 1206(3216)
C16
CAP 100uF 6.3V 1206(3216)
R13
110K 1% 1206(3216)
POT9
1K
R18
110K 1% 1206(3216)
C17
CAP 1uF 6.3V 1206(3216)
C18
CAP 100uF 6.3V 1206(3216)
R14
110K 1% 1206(3216)
POT10
1K
R19
110K 1% 1206(3216)
C19
CAP 1uF 6.3V 1206(3216)
C20
CAP 100uF 6.3V 1206(3216)
W14
Jumper
R21
110K 1% 1206(3216)
POT11
1K
R25
110K 1% 1206(3216)
C28
CAP 100uF 6.3V 1206(3216)
R23
0R
C21
CAP 10uF
C22
CAP 0.1uF
U1
MCP6V11T-E/OT
R27
110K 1% 1206(3216)
vbias
C25
CAP 100uF 6.3V 1206(3216)
R22
110K 1% 1206(3216)
POT12
1K
R26
110K 1% 1206(3216)
C29
CAP 100uF 6.3V 1206(3216)
R24
0R
C23
CAP 10uF
C24
CAP 0.1uF
U2
MCP6V11T-E/OT
R28
110K 1% 1206(3216)
vrefbias
C26
CAP 100uF 6.3V 1206(3216)
Low impedance node to ground for driving (need opamp?)
Title
Size
A4
Number
Revision
Date:
17/03/2019
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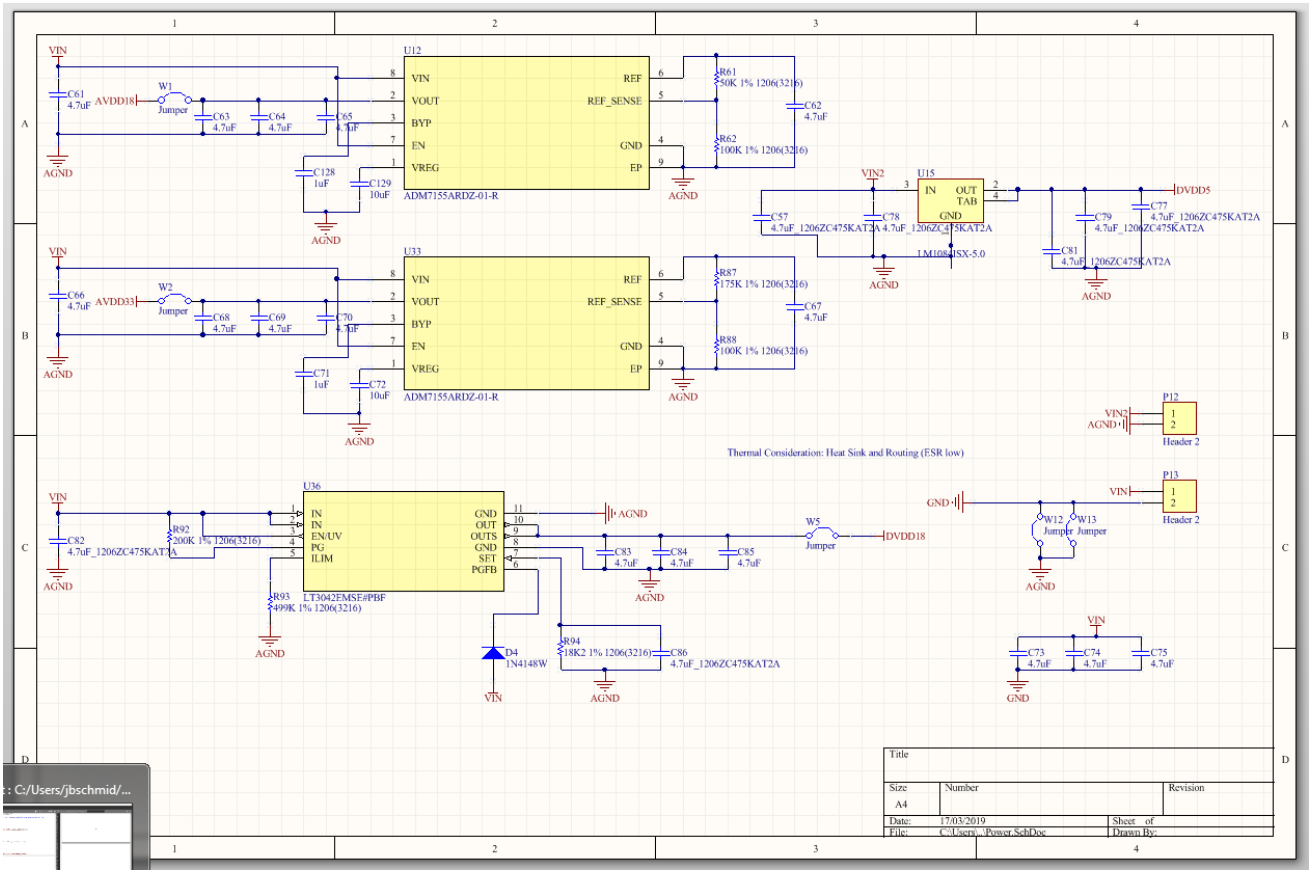
VIN
AVDD18
W1
Jumper
C61 4.7uF
C63 4.7uF
C64 4.7uF
C65 4.7uF
C128 1uF
C129 10uF
AGND
U12
ADM7155ARDZ-01-R
VIN
VOUT
BYP
EN
VREG
REF
REF_SENSE
GND
EP
R61 50K 1% 1206(3216)
R62 100K 1% 1206(3216)
C62 4.7uF
VIN2
U15
IN
OUT
TAB
GND
LM1084ISX-5.0
C57 4.7uF_1206ZC475KAT2A
C78 4.7uF_1206ZC475KAT2A
C79 4.7uF_1206ZC475KAT2A
C77 4.7uF_1206ZC475KAT2A
C81 4.7uF_1206ZC475KAT2A
DVDD5
AVDD33
W2
C66 4.7uF
C68 4.7uF
C69 4.7uF
C70 4.7uF
C71 1uF
C72 10uF
U33
R87 175K 1% 1206(3216)
R88 100K 1% 1206(3216)
C67 4.7uF
P12
Header 2
Thermal Consideration: Heat Sink and Routing (ESR low)
U36
LT3042EMSE#PBF
IN
EN/UV
PG
ILIM
GND
OUT
SET
PGFB
C82 4.7uF_1206ZC475KAT2A
R92 200K 1% 1206(3216)
R93 499K 1% 1206(3216)
C83 4.7uF
C84 4.7uF
C85 4.7uF
W5
Jumper
DVDD18
P13
W12
W13
Jumper
D4 1N4148W
R94 18K2 1% 1206(3216)
C86 4.7uF_1206ZC475KAT2A
C73 4.7uF
C74 4.7uF
C75 4.7uF
Title
Size
A4
Number
Revision
Date: 17/03/2019
File: C:\Users\...\Power.SchDoc
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Drawn By: