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A Low-Power Dynamic Comparator for Low-Offset Applications

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Abstract

In this paper, a low-power method for double-tail comparators is introduced. Using the proposed method, the power consumption of the pre-amplifier which is the dominant part is reduced considerably. Thanks to this method, the pre-amplifier is not able to draw more than required amount of power, therefore, the power is saved. Post layout and corner simulation results show the power consumption is reduced by about 40%. Moreover, several Monte-Carlo (M) simulations suggest the proposed method results in about 20% offset reduction at the cost of 5% area and 10% speed degradation.

Keywords: Dynamic Comparators; Low-power; Pre-amplifier;

Introduction:

these days, there are lots of battery-powered applications such as hand held devices, wearable electronics, and portable medical devices. In order to increase the battery lifetime, it is essential to reduce power consumption as much as possible. Comparators are essential parts of many mixed-mode circuits such as Analog to Digital Converters (ADC) as described in [1-3]. Therefore, the power consumption of comparators has a significant effect on the total power consumption [4-6]. Researchers have proposed several circuits and techniques to reduce the power consumption of the comparators [7]; some of the recent works are presented as follows.

In [8], a low-power low-offset comparator is presented. In that comparator, the pre-amplifier current tail is replaced with a positive feedback half latch circuit which considerably increases the number of transistors and area. Also, the half latch connected to the top of the pre-amplifier generates a significant differential kickback noise in the input nodes of the comparator. The kickback noise mechanism and the reduction techniques are properly explained in [9]. In [10], a bulk-tuned offset calibration is proposed to reduce the offset voltage, therefore, smaller transistors can be used resulting in a lower power consumption for a given offset voltage. This method significantly reduces the offset voltage; however, its area overhead (due to calibration capacitors) is also considerable. Moreover, the calibration circuitry increases the design area and implementation complexities. As another example, in [11], a double tail comparator is proposed using a current mirror to reduce the kickback noise and increase the speed. This method increases the power consumption, since the pre-amplifier is kept *on* during the entire pre-amplification process. The comparator reported in [12] with its special clock signals was proposed to reduce the power consumption although the low-power behavior is not effective for high resolution

applications. In fact, for a low offset voltage a big latch must charge and discharge the large parasitic capacitors of the large pre-amplifier input transistors causing significant power consumption and speed reduction. Moreover, generating special control signals requires especial circuitry which incurs area and power overheads. It is shown in [3] the power can be reduced by using another supply voltage for the pre-amplifier stage while the speed performance is enhanced. However, this method sacrifices the offset voltage. Also, generating the second supply voltage causes more power, area, and complexity to the design. In [13], a structure similar to the double tail comparator is introduced which works with delayed clock signals to reduce the power and enhance the speed performance. This comparator suffers from a large kickback noise, since the input transistors are directly connected to the latch internal nodes with a rail-to-rail differential swing. Moreover, in order to generate the delayed clock signals additional circuitry is required which increases power and area. A wise control scheme of the pre-amplifier could result in power/offset benefits as presented in [14-16]. The methods reported in [17, 18] are some of the most recent low-power methods. These methods are efficient in power reduction, however, their benefit is for ultra low-voltage applications.

In this paper, an efficient method is proposed to reduce the power consumption of the double tail dynamic comparators. Employing this method is easy and straight forward meaning that in its simplest form no design procedure is required. In fact, the proposed method is applied to a previously designed conventional comparator resulting in considerable power reduction. More than simplicity and effectiveness, the proposed method does not increase the kickback noise or offset voltage.

The Proposed Circuit

Fig. 1 presents the conventional dynamic comparator [19, 20]. In the reset phase (clk ="1", $\overline{clk}$ ="0"), the output nodes (O1+, O1-) of the pre-amplifier are discharged to *Vss* while the output nodes of the latch are charged to *Vdd*. When evaluation phase starts (clk ="1"→"0", $\overline{clk}$ ="0" →"1"), the pre-amplifier amplifies the difference between the input signals and a small differential voltage appears at the output nodes of the pre-amplifier [6, 21]. When the output common mode voltage of the pre-amplifier become larger than the voltage threshold of the latch input NMOS transistors (V_{thn}) the latch starts working and makes a decision (creates *Vdd* at one side and *Vss* at the other side) based on its input differential signal. In this circuit, the pre-amplifier continues consuming power even after the comparison is made until both of the outputs of the pre-amplifier goes to *Vdd*. Therefore, in each comparison, the pre-amplifier is wasting energy. In fact, when the output nodes of the pre-amplifier are more that V_{thn} (somewhere around 1.5 to 2 times of V_{thn}), the pre-amplifier strongly turns *on* the latch finishing the comparison, and there is no need to consume more energy after that.

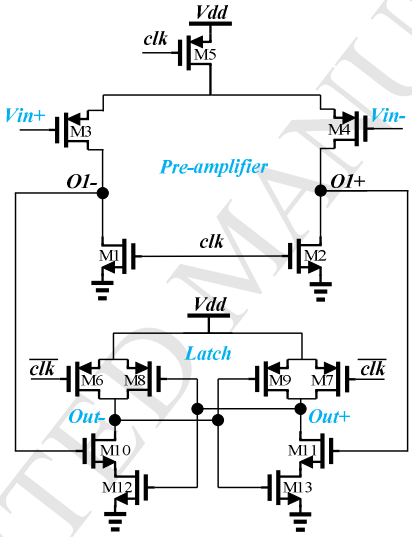

Fig. 1 **The circuit of the conventional dynamic comparator containing a latch and a pre-amplifier proposed in [19, 20].**

Fig. 2 presents the proposed method applied to the comparator of Fig. 1. The functionality of this circuit is the same as the comparator of Fig. 1. However, in this circuit the pre-amplifier is not able to waste a large amount of power. In fact, when the output voltages of the pre-amplifier go to a value close to Vdd-$|V_{thp}|$ the tail current approaches zero wasting no energy (V_{thp} is the threshold voltage of the PMOS transistors M14, M15). As discussed earlier, an output common mode voltage of 1.5 times to 2 times of V_{thn} is large enough to strongly activate the latch and finish the comparison. Assuming a nominal supply voltage of *Vdd* in a given technology, Vdd-$|V_{thp}|$ is higher than $1.5\times V_{thn}$; therefore, the proposed technique avoids wasting power after enough guard to the edge of $1.5\times V_{thn}$. This results in an efficient and safe power reduction method. The proposed method can be applied to double tail comparators. When employing the proposed method, the supply voltage should be large enough so that Vdd-$|V_{thp}|$ is sufficiently larger than V_{thn}, thus, the latch is activated strongly during the evaluation phase with no delay overhead. Therefore, the minimum appropriate supply voltage is about Vdd-($|V_{thp}|$+$1.5\times V_{thn}$).

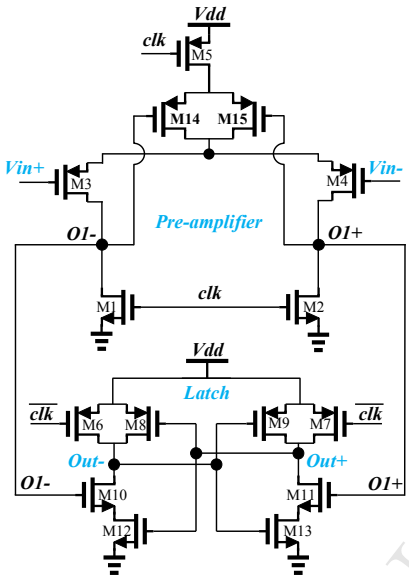

Fig. 2 **The proposed method applied on the conventional comparator.**

Fig. 3 presents the output voltages of the pre-amplifier of the proposed circuit compared to the conventional circuit presented in Fig 1. As seen, in the proposed comparator the output voltages goes from 0 to *Vdd*-$|V_{thp}|$ while in the other one it goes from to 0 to *Vdd*.

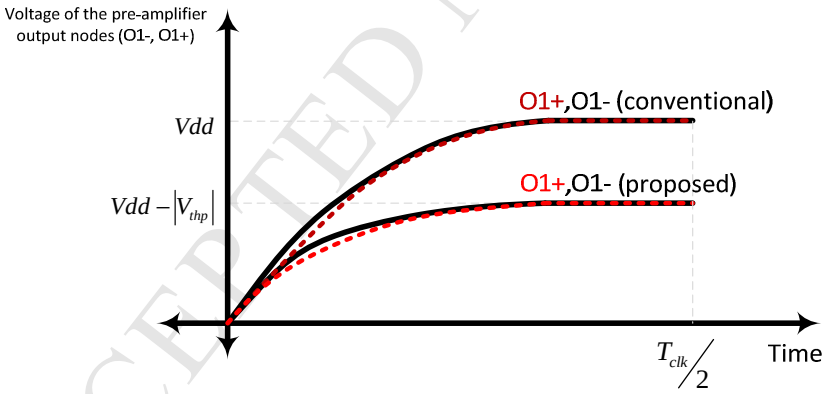

Fig. 3 **The voltage of the pre-amplifier outputs during the evaluation phase in the proposed and conventional comparators.**

Usually, especially in low offset comparators, the sizing of the pre-amplifier transistors is dominant to the sizing of the latch transistors. Therefore, the pre-amplifier consumes a large part of the total power dissipation (due to larger parasitic capacitors). As a result, reducing the power of the pre-amplifier noticeably reduces the total power of the comparator. The added tail transistors (M14, M15) are considerably smaller than the pre-amplifier input transistors (less than 10%). Therefore, their power overhead is negligible (due to small size and small voltage swing), and the proposed method is able to considerably reduce the total power consumption.

In the proposed circuit, it is essential that the connection from the output nodes of the pre-amplifier (O1-, O1+) to the tail current is done in a way that it does not add a term in the input referred offset voltage. In the circuit of Fig. 2, the output nodes affect the tail current which is seen as a common-mode value for the input transistors ($M_{3,4}$). Thus, the proposed method does not affect the input referred offset voltage, although the output nodes of the pre-amplifier has a differential term.

Analytical derivations

In this section, analytical derivations of the power consumption are presented. In the proposed comparator, the output nodes of the pre-amplifier are charged from *0* to *Vdd*-$|V_{thp}|$. If the output capacitor of the pre-amplifier is C at each side the power consumption of the pre-amplifier (which is dominant to the latch) is evaluated as follows:

$$P_{total} = \frac{1}{T_{clk}} \int Vdd(I_{tail}).dt = \frac{1}{T_{clk}} \int_0^{\frac{T_{clk}}{2}} Vdd(I_1 + I_2).dt \quad (1)$$

Where I_{tail} is the current of the tail transistor (M_5), I_1 and I_2 are presented in Fig. 4, and $T_{clk}/2$ is half of the clock period which is allocated for the evaluation phase (the other half is for the reset phase).

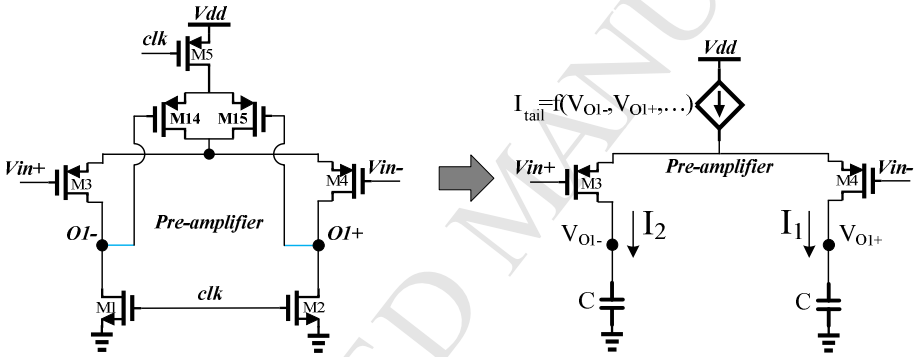

Fig. 4 **Modeling of I_1 and I_2 in the circuit of the proposed pre-amplifier.**

In a capacitor, the following equation holds.

$$I_C = C\frac{dv_c}{dt} \rightarrow I_C.dt = C.dv_c \quad (2)$$

Based on (2), (1) can be written as:

$$P_{total} = \frac{1}{T_{clk}} Vdd \int_0^{\frac{T_{clk}}{2}} (I_1 + I_2).dt = \frac{Vdd}{T_{clk}} \int_0^{V_{O1-}(\infty)} C.dV_{O1-} + \frac{Vdd}{T_{clk}} \int_0^{V_{O1+}(\infty)} C.dV_{O1+} \quad (3)$$

$$P_{total} = \frac{C}{T_{clk}} Vdd \left(\int_0^{V_{O1-}(\infty)} dV_{O1-} + \int_0^{V_{O1+}(\infty)} dV_{O1+} \right) \quad (4)$$

In the comparator, the output nodes of the pre-amplifier are charged from *0* to *Vdd*-$|V_{thp}|$. Therefore, the total power consumption is evaluated as presented in (5).

$$P_{total} = \frac{2C}{T_{clk}} Vdd\left(Vdd - |V_{thp}|\right) \quad (5)$$

The proposed derivations are independent of the linearity or operating region of the input/tail transistors, since the steady-state voltage variation is observed (as proved in (3)). The parasitic capacitors available at the pre-amplifier output nodes are mostly overlap capacitors which are almost constant during the operation. Therefore, (5) presents a good approximation of the pre-amplifier power consumption.

Similar to the mentioned derivations, it can be shown the power consumption of the conventional comparator of Fig. 1 is equivalent to:

$$P_{total} = \frac{2C}{T_{clk}} Vdd \times Vdd = \frac{2C}{T_{clk}} Vdd^2 \quad (6)$$

As discussed earlier, in low-offset comparators, the power consumption of the latch is negligible compared to the power consumption of the pre-amplifier. Therefore, the percentage of the power reduction is calculated as follows.

$$Power\ Reduction\ (\%) = 100 \times \left(1 - \frac{P_{proposed}}{P_{conventional}}\right) = 100 \times \frac{|V_{thp}|}{Vdd} \quad (7)$$

Considering the average of typical values in $0.18\mu m$ CMOS technology, the power reduction is about 36%. Using *hvt* transistors with a larger value of $|V_{thp}|$ in the proposed comparator results in about 50% power reduction while it reduces the speed of the comparator.

Totally, the proposed method is able to reduce the power consumption by about 30%-50%. As a benefit of the proposed method, there is no need to redesign the circuit and few components are added to the circuit ($M_{14,15}$). In fact, first the comparator (*e.g.*, the one presented in Fig. 1) is designed, then, two transistors are added to the circuit as presented in Fig. 2. Therefore, without changing the initial transistor sizing the proposed method is applied to the conventional circuit.

Simulation Results

In this section, the simulation results of a typical comparator before and after using the proposed method is presented. First, the comparator proposed in Fig. 1 was designed in $0.18\mu m$ CMOS technology with *Vdd=1.8V* for an offset voltage of about *2.5mV* at V_{cm}=*Vdd/2* (V_{cm}=*0.5*(V_{in+}-V_{in-})), a clock frequency of *0.5GHz*, and power consumption of less than *500uW*. This comparator is a good candidate for a 10bit high speed differential ADC where LSB is about 3.5.mV. Then, the proposed method is applied to the comparator. In order to do so, the following sizing (shown in Fig. 5) and replacement is applied to the tail transistor and the rest of the comparator remains untouched.

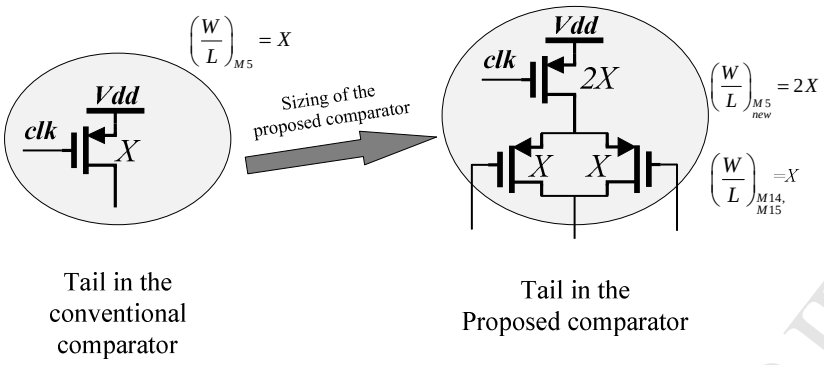

Fig. 5 **The sizing of the tail transistor in the proposed comparator based on the conventional comparator.**

In the designed comparator, the size of the tail transistor is about 3.7% of the total size, therefore, the sizing illustrated in Fig. 5 increases the area by a maximum of about 11% (4X-X=3X=3*3.7). In the layout section, it is shown the area overhead of the proposed method in this design is about 5% compared to the conventional comparator.

It is noteworthy that after applying the proposed method, it is possible to make a refinement into the sizing of the other transistors for a better improvement. However, we did not do that to see how much the proposed method is effective in the worst case meaning when minimum design effort is made (keeping the rest of the comparator exactly the same).

Fig. 6 presents the output of the pre-amplifier in the proposed and conventional comparators for different V_{cm}'s ranging from *0V* to *1V* with the steps of *0.1V*. As expected, in the proposed circuit, the voltage goes to $Vdd-|V_{thp}|$ while in the other circuit it goes to *Vdd* wasting power.

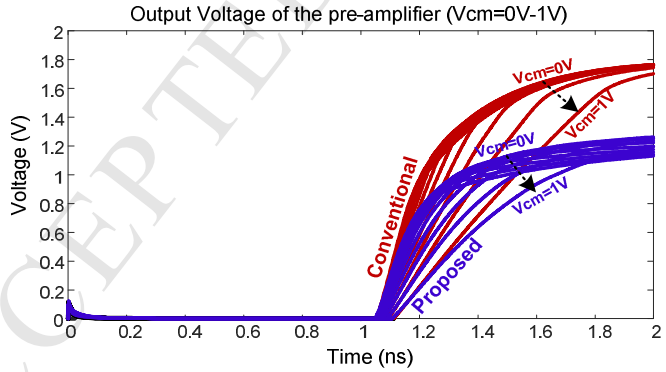

Fig. 6 **The output voltage of the pre-amplifier in the proposed and conventional comparators during the evaluation phase. Vcm is changed from 0V to 1V to create different figures.**

In the proposed comparator, the pre-amplifier output voltage goes from somewhere between *1.1V* to *1.25V*. Therefore based on (7), the power reduction of the pre-amplifier is about *30%-40%*. As a result, we expect the total power reduction to be about *35%*.

Fig. 7 presents the power consumption at *0.5GHz* clock frequency versus input V_{cm} of the comparator. As seen, for different values of V_{cm} the power reduction is about *35%*. For example, for $V_{cm}=0V$ the power reduction is about *40%* and for $V_{cm}=0.9$ the power reduction is about 33%. The average power consumption of the proposed and conventional comparators over the operating range of V_{cm} is about

347uW and *556uW*, respectively. Therefore, the proposed method reduces the total power consumption by about *37%*.

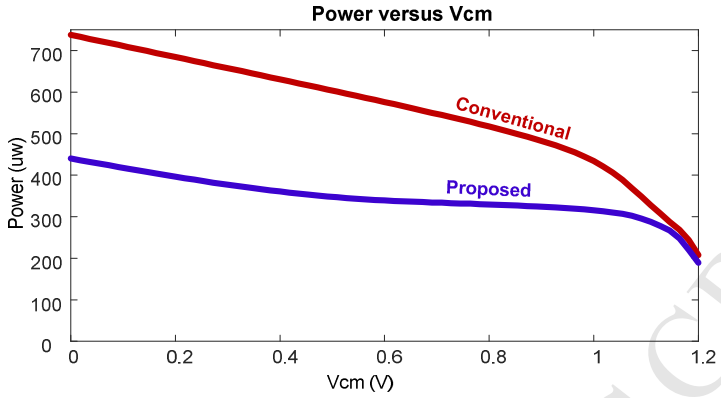

Fig. 7 **Power consumption of the proposed and conventional comparators versus input Vcm at 0.5GHz clock frequency.**

Fig. 8 presents the dynamic behavior of the comparators. In this figure, the delay of the proposed and conventional comparators versus input V_{id} and V_{cm} are presented. Both the figures suggests that the delay of the proposed and conventional comparators are comparable. The delay of the proposed comparator is larger, since the pre-amplifier tail current is reduced. The delay degradation is about 10%.

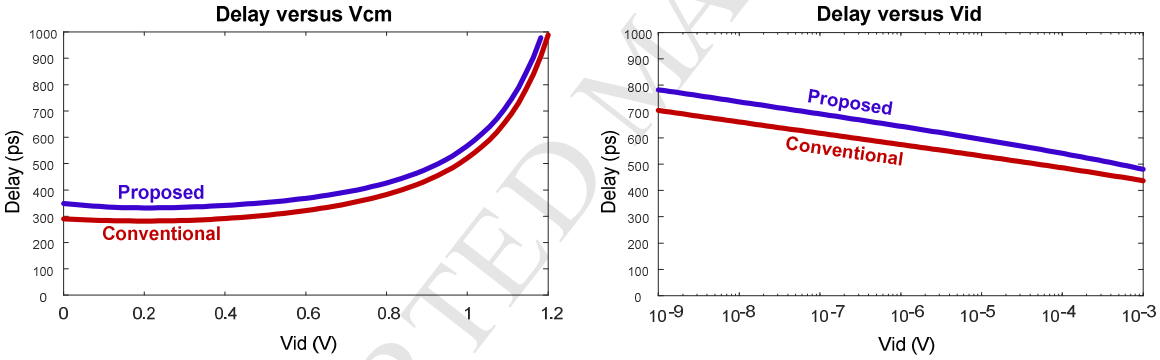

Fig. 8 **Delay versus Vcm (V_{id}=1mV) and versus Vid (V_{cm}=0.9V) of the proposed and conventional comparators.**

In recently proposed capacitive DACs of SAR ADCs such as the ones reported in [22-24], it is important that the comparator is able to work in the V_{cm} range of *0.25Vdd-0.75Vdd*. The proposed method does not have a noticeable bad effect in the mentioned range, thus, this method is an acceptable low-power candidate for SAR ADCs. It is noteworthy that in some other capacitive DACs of SAR ADCs the required V_{cm} range is one point which is usually equal to 0.5*Vdd. For example, the output *Vcm* range of DACs reported in [25, 26] is 0.5*Vdd or very close to it like the method presented in [27].

To evaluate the offset voltage, 1k-point Monte-Carlo simulations were performed for each V_{cm} value (*e.g.*, V_{cm}=0.5V) in the input V_{cm} range of the comparator. The statistical behavior of the comparators originated from several Monte-Carlo simulations is depicted in Fig. 9. In this figure, the standard deviation of the input referred offset voltage versus input V_{cm} is presented. Generally, the input referred offset voltage of the proposed comparator is better by 20%. The proposed method reduces the tail current of the pre-amplifier enhancing the gain so the effect of the latch on the offset voltage is reduced. This offset voltage reduction is achieved with the overhead of speed reduction as the results presented in Fig. 8 reveals.

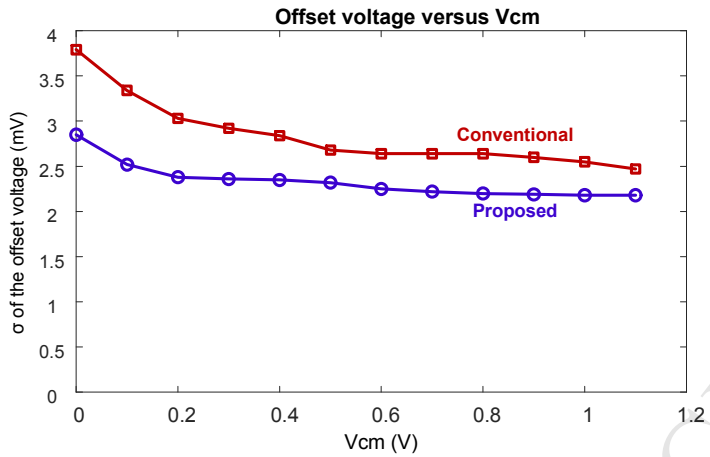

Fig. 9 **Offset voltage of the proposed and conventional comparators. Each point represents several Monte-Carlo simulations.**

Corner Simulations

In this section, corner simulations are presented to confirm the effectiveness of the proposed method in different corners. Extreme PVT corners were considered for simulations. First, the circuit was simulated for slow-slow (ss) process at T=75^{o}C, and Vdd=1.6V. The results are presented in Fig. 10(a). The delay of the proposed comparator is larger than the conventional comparator while still 40% power reduction is achieved. Next, the circuit was simulated for typical-typical (ss) process at T=25^{o}C, and Vdd=1.8V. Also in this case, 36% power reduction is achieved while the speed reduction is negligible as shown in Fig. 10(b). Finally, the comparators were simulated for fast-fast (ff) process at T=-25^{o}C, and Vdd=2.0V as the results are depicted in Fig. 10(c). Again in this case, the power reduction is 38% which is a considerable value. In this corner, the delay of the proposed and conventional comparators are almost the same. As a conclusion, corner simulations show the proposed method is able to considerably reduce the power in different corners. The delay degradation of the proposed method is large in extreme slow corner while in extreme fast corner the delay is almost equal to the conventional comparator.

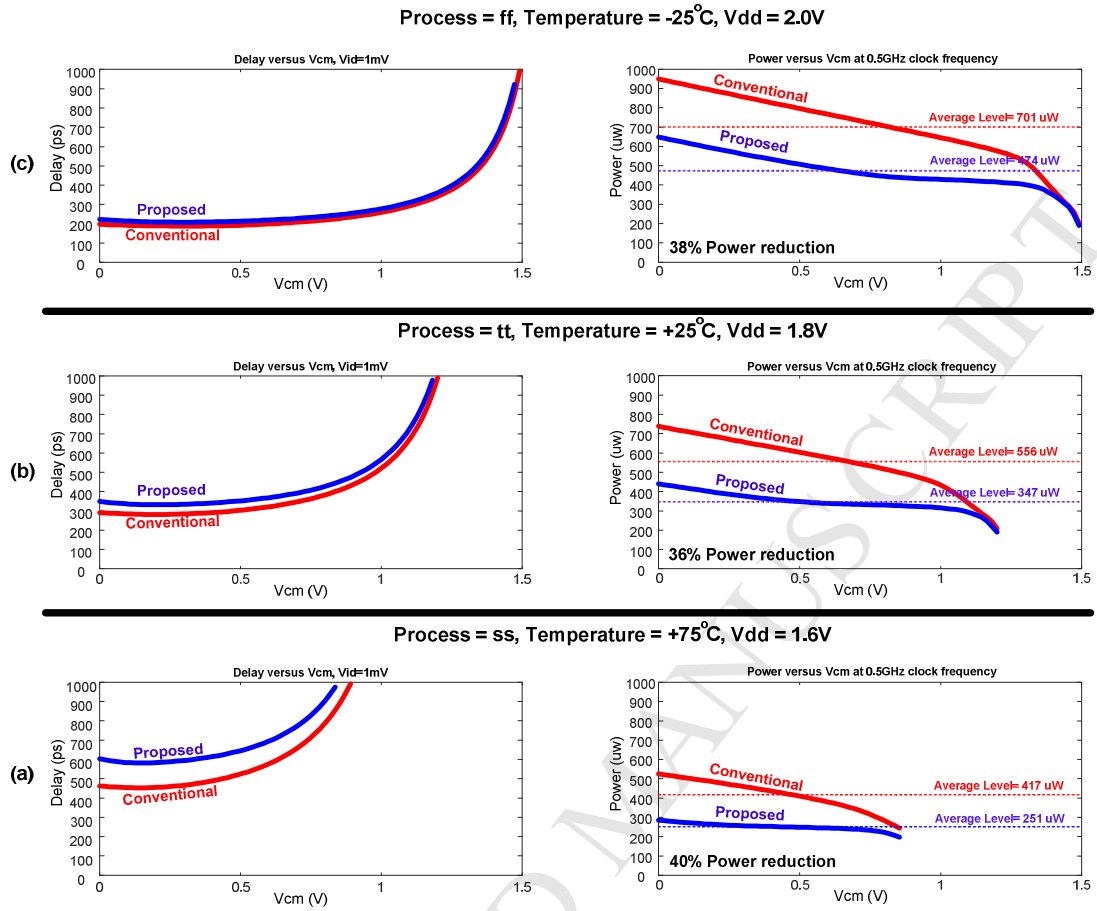

Fig. 10 **Corner simulations: (a) Process=ss, Temperature=75°C, and Vdd=1.6V, (b) Process=tt, Temperature=25°C, and Vdd=1.8V, (c) Process=ff, Temperature=25°C, and Vdd=2.0V .**

Layout and Post Layout Simulation

In order to further confirm the low-power behavior of the proposed comparator, a symmetric layout was created then Fig. 7 simulation was repeated for the extracted circuit. Fig. 11 presents the layout and the schematic of the proposed and conventional comparators. The labels of the transistors have been written using white color on the layout image. As seen, the size of the proposed comparator is 19um by 19um and almost equal to the conventional comparator. The only difference is the lack of M14 and M15 in the layout of the conventional comparator; the area of this part ($14 \times 1.3\ um^2$) is about 5% of the total area of the comparators ($19 \times 19\ um^2$). Therefore, the area overhead of the proposed comparator is negligible compared to the total area.

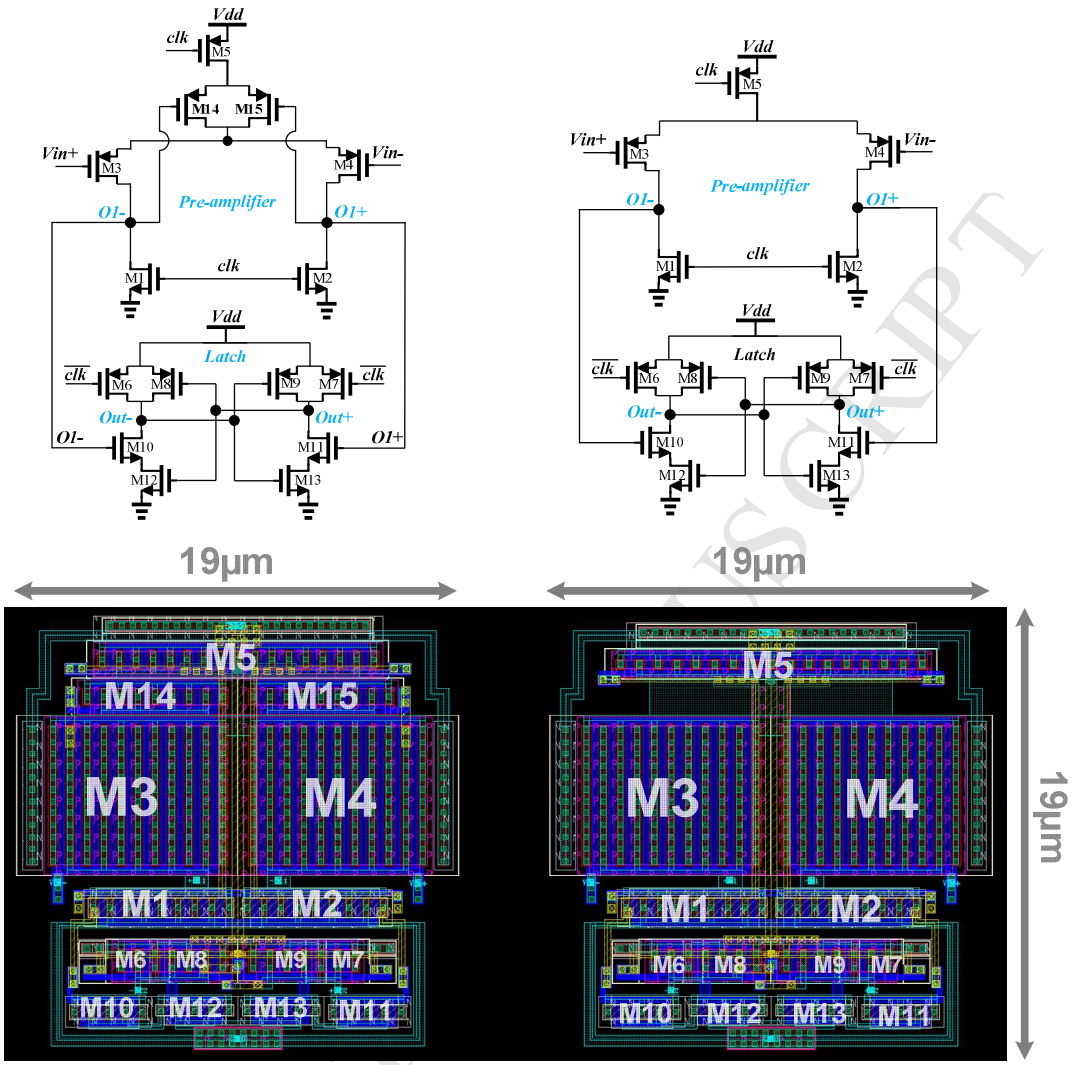

Fig. 11 **Layout structure and schematic of the proposed and conventional comparators compared to each other. The label of the transistors is placed on the layout image using white color.**

Fig. 12 presents post layout and schematic simulation results of the power consumption versus input V_{cm} range of the comparators.

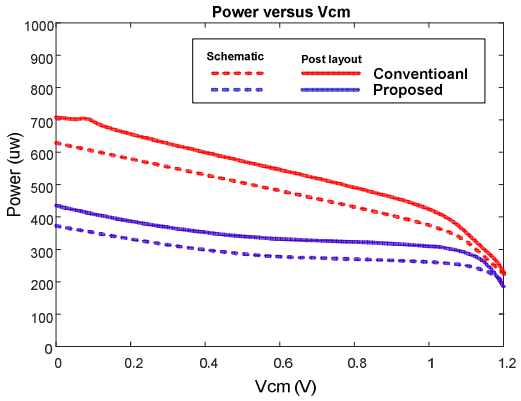

Fig. 12 **Post layout versus schematic simulation of the power consumption of the proposed and conventional comparators.**

Fig. 12 confirms the proposed comparator is able reduce the total power consumption. Parasitic components has led to about 10% and 15% increase in total power consumption of the proposed and conventional comparators.

Comparison and Discussion

Schematic simulations, analytical derivations, and post layout simulations show the proposed method is effective in reduction of the power consumption in different PVT corners. However, power reduction is achieved with some advantages and disadvantages. Table I presents a comparison between the proposed and conventional comparator. As discussed earlier, the current proposed method is the simplest version which is achieved with no design effort (explained in Fig. 5). Therefore, if this version of the proposed method is effective in power reduction, sizing refinement will further improves its benefits.

Table I COMPARISON BETWEEN THE PROPOSED AND CONVENTIONAL COMPARATORS

	Average Power consumption @0.5GHz	Input referred offset voltage @ V_{cm}=0.9V	Speed @ V_{cm}=0.9V	Layout Area
Conventional	556 μW	2.6 mV	1.16 GHz	343 μm^2
Proposed	347 μW	2.19 mV	1.05 GHz	361 μm^2
relative	+37.6 %	+15.8 %	- 9.5 %	- 5 %

Based on Table I, the proposed method reduces the power by *37.6%* and the input referred offset voltage by *15.8%* while speed and area are degraded by about *10%* and *5%*, respectively.

Table II presents a comparison between the proposed and some recently proposed comparators.

Table II COMPARISON BETWEEN THE PROPSOED AND SOME OTHER COMPARATORS

	Average Power	offset voltage	Operating Frequency	Vdd	Area	Technology	Measurement /Simulation
[13]	600 μW	7.78 mV	–	1.2 V	–	130 nm	Simulation
[10]	766 μW	0.056 mV	100 kHz	5.0 V	64000 μm^2	0.5 μm	Measurement
[11]	–	5.62 mV	1 GHz	1.2 V	–	90 nm	Measurement
[12]	51 μW	16.5 mV	0.9 GHz	1 V	260 μm^2	90 nm	Simulation
[28]	252 μW	5.8 mV	2.5 GHz	1.2 V	–	65 nm	Simulation
[3]	420 μW	2.5 mV	0.5 GHz	1.8 V	453 μm^2	0.18 μm	Simulation
conventional	556 μW	2.65 mV	0.5 GHz	1.8 V	343 μm^2	0.18 μm	Simulation
Proposed	347 μW	2.19 mV	0.5 GHz	1.8 V	361 μm^2	0.18 μm	Simulation

As seen in Table II, the proposed method offers a low-power and a low-offset with 1.8V in 0.18μm technology. Also, applying the proposed method to a given double-tail comparator is simple compared to the other ones where a new design procedure or additional circuitry are required. As a result, the proposed method is an effective and easy to use way of power reduction suitable for low-offset low-power applications.

Conclusion

This paper presents a method to reduce the power consumption in dynamic comparators. The proposed method is easy to implement and does not require an extra design procedure. First a comparator is designed then the proposed method is applied to the tail transistor of the pre-amplifier using a simple sizing. Simulation results confirm the proposed method is able to reduce the power consumption by about 40% and offset voltage by 20% while area is increased by 5% and speed is reduced by about 10%. Analytical derivations as well as PVT corner and post layout simulation validate the low-power behavior of the proposed method.

References

[1] H.-K. Hong *et al.*, "26.7 A 2.6 b/cycle-architecture-based 10b 1 JGS/s 15.4 mW 4×-time-interleaved SAR ADC with a multistep hardware-retirement technique," in *Solid-State Circuits Conference-(ISSCC), 2015 IEEE International*, 2015: IEEE, pp. 1-3.

[2] K. Ragab, L. Chen, A. Sanyal, and N. Sun, "Digital Background Calibration for Pipelined ADCs Based on Comparator Decision Time Quantization," *IEEE Trans. on Circuits and Systems*, vol. 62, no. 5, pp. 456-460, 2015.

[3] A. Khorami and M. Sharifkhani, "High-speed low-power comparator for analog to digital converters," *AEU-International Journal of Electronics and Communications*, vol. 70, no. 7, pp. 886-894, 2016.

[4] H. Nasiri and A. Nabavi, "A 1.8 V 3 GS/s 7-bit time-interleaved Quasi C-2C SAR ADC using voltage-comparator time-information," *AEU-International Journal of Electronics and Communications*, vol. 83, pp. 138-149, 2018.

[5] D. Del Corso and C. Passerone, "A taxonomy of ADC architectures for ICT engineering curricula," *AEU-International Journal of Electronics and Communications*, vol. 84, pp. 394-402, 2018.

[6] B. Razavi and B. A. Wooley, "Design techniques for high-speed, high-resolution comparators," *IEEE journal of solid-state circuits*, vol. 27, no. 12, pp. 1916-1926, 1992.

[7] S. Babayan-Mashhadi, M. Daliri, and R. Lotfi, "Analysis of power in dynamic comparators," in *Electrical Engineering (ICEE), 2013 21st Iranian Conference on*, 2013: IEEE, pp. 1-4.

[8] Y. Jung, S. Lee, J. Chae, and G. Temes, "Low-power and low-offset comparator using latch load," *Electronics Letters*, vol. 47, no. 3, pp. 167-168, 2011.

[9] P. M. Figueiredo and J. C. Vital, "Kickback noise reduction techniques for CMOS latched comparators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 7, pp. 541-545, 2006.

[10] J. Lu and J. Holleman, "A low-power high-precision comparator with time-domain bulk-tuned offset cancellation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1158-1167, 2013.

[11] S. D'Amico, G. Cocciolo, A. Spagnolo, M. De Matteis, and A. Baschirotto, "A 7.65-mW 5-bit 90-nm 1-Gs/s folded interpolated ADC without calibration," *IEEE transactions on instrumentation and measurement*, vol. 63, no. 2, pp. 295-303, 2014.

[12] M. Hassanpourghadi, M. Zamani, and M. Sharifkhani, "A low-power low-offset dynamic comparator for analog to digital converters," *Microelectronics Journal*, vol. 45, no. 2, pp. 256-262, 2014.

[13] J. Gao, G. Li, and Q. Li, "High-speed low-power common-mode insensitive dynamic comparator," *Electronics Letters*, vol. 51, no. 2, pp. 134-136, 2015.

[14] A. Khorami and M. Sharifkhani, "Low-power technique for dynamic comparators," *Electronics Letters*, vol. 52, no. 7, pp. 509-511, 2016.

[15] A. Khorami and M. Sharifkhani, "A Low-Power High-Speed Comparator for Precise Applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, no. 99, pp. 1-12, 2018.

[16] A. Khorami and M. Sharifkhani, "Excess power elimination in high-resolution dynamic comparators," *Microelectronics journal*, vol. 64, pp. 45-52, 2017.

[17] Y.-H. Hwang and D.-K. Jeong, "Ultra-low-voltage low-power dynamic comparator with forward body bias scheme for SAR ADC," *Electronics Letters*, vol. 54, no. 24, pp. 1370-1372, 2018.

[18] X. Xin, J. Cai, R. Xie, and P. Wang, "Ultra-low power comparator with dynamic offset cancellation for SAR ADC," *Electronics Letters*, vol. 53, no. 24, pp. 1572-1574, 2017.

[19] M. Van Elzakker, E. Van Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, "A 1.9 μW 4.4 fJ/conversion-step 10b 1 MS/s charge-redistribution ADC," in *2008 IEEE International Solid-State Circuits Conference-Digest of Technical Papers*, 2008: IEEE, pp. 244-610.

[20] M. Van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. A. Klumperink, and B. Nauta, "A 10-bit Charge-Redistribution ADC Consuming 1.9 μW at 1 MS/s," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 5, pp. 1007-1015, 2010.

[21] T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE journal of solid-state circuits*, vol. 30, no. 3, pp. 166-172, 1995.

[22] J. Zhao, N. Mei, Z. Zhang, and L. Meng, "V aq-based tri-level switching scheme for SAR ADC," *Electronics Letters*, vol. 54, no. 2, pp. 66-68, 2017.

[23] B. Yazdani, A. Khorami, and M. Sharifkhani, "Low power DAC with single capacitor sampling method for SAR ADCs," *Electronics Letters*, vol. 52, no. 14, pp. 1209-1210, 2016.

[24] L. Xie, J. Su, J. Liu, and G. Wen, "Energy-efficient capacitor-splitting DAC scheme with high accuracy for SAR ADCs," *Electronics Letters*, vol. 51, no. 6, pp. 460-462, 2015.

[25] A. Khorami, R. Saeidi, and M. Sharifkhani, "An ultra low-power DAC with fixed output common mode voltage," *AEU-International Journal of Electronics and Communications*, vol. 96, pp. 279-293, 2018.

[26] B. Ginsburg and A. Chandrakasan, "A 500MS/s 5b ADC in 65nm CMOS," in *VLSI Circuits, 2006. Digest of Technical Papers. 2006 Symposium on*, 2006: IEEE, pp. 140-141.

[27] E. Rahimi and M. Yavari, "Energy-efficient high-accuracy switching method for SAR ADCs," *Electronics Letters*, vol. 50, no. 7, pp. 499-501, 2014.

[28] D. Xu, S. Xu, and G. Chen, "High-speed low-power and low-power supply voltage dynamic comparator," *Electronics Letters*, vol. 51, no. 23, pp. 1914-1916, 2015.

In dynamic comparators, the pre-amplifier amplifies the input differential signal to some extent then the latch finalizes the comparison. After some moment from the latch activation, the pre-amplifier is wasting power and sometimes reduces the gain worsening the power consumption and offset voltage. The aim of the proposed comparator is to overcome this issue. In low-offset comparators, the sizing of the input transistors of the pre-amplifier is chosen large for matching purposes so that the pre-amplifier consumes the dominant part of the total power consumption making it a good candidate to work on for low-power applications. In this paper, a low power method for dynamic comparators is presented using which the power consumption of the pre-amplifier is controlled in a proper way. Therefore, not only the power is saved but also the input referred offset voltage is improved.

In the paper, analytical derivations are presented to quantify the amount of power saving. Simulations showed the derivations are consistent with the circuit. The proposed method is able to reduce the power consumption by about 30%-40% and the offset voltage by about 20%. Post layout simulation of the RC-CC extracted circuit confirms the benefits of the proposed comparator.

The proposed method is applicable to different types of the double tail comparators. This method is simple yet effective in power reduction.