High-Efficiency Millimeter-Wave Front-Ends for Large Phased-Array Transmitters

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

The ever-increasing demand for wireless broadband connectivity requires infrastructure capable of supporting data transfer rates at multi-Gbps. To accommodate such heavy traffic, the channel capacity for the given spectrum must be utilized as efficiently as possible. Wideband millimeter-wave phased-array systems can enhance the capacity of the channel by providing multiple steerable directional beams. However the cost, complexity, and high power consumption of phased-array systems are key barriers to the commercialization of such technology. Silicon-based beam-former chips and scalable phased-array technology offer promising solutions to lower the cost of phased-array systems. However, the implementation of low-power phased-array architectures is still a challenge. Millimeter-wave power generation in silicon beam-formers suffers from low efficiency. The stringent linearity requirements for multi-beam wideband arrays further limits the achievable efficiency. In scalable phased-arrays, each module consists of an antenna sub-array and a beam-former chip that feeds the antenna elements. To improve efficiency, a design methodology that considers the beam-former chip and the antenna array as one entity is necessary. In this thesis, power-efficient solutions for a millimeter-wave phased-array transmitter are studied and different high-efficiency power amplifier structures for broadband applications are proposed.

Initially, the design of a novel 27-30 GHz RF front-end consisting of a variable gain amplifier, a 360 degree phase shifter, and a two-stage linear power amplifier with output power of 12 dBm is described. It is fabricated using 0.13 μm SiGe technology. This chip serves as the RF core of a beam-former chip with eight outputs for feeding a 2×2 dual-feed sub-array. Such sub-arrays are used as part of large phased-arrays for SATCOM infrastructure. Measurement results show 26.7 % total efficiency for the designed chip. The chip achieves the highest efficiency among Ka-band phased-array transmitters reported in the literature.

In addition, original transformer-based output matching structures are proposed for harmonic-tuned power amplifiers. Harmonic-tuned power amplifiers have high peak-efficiency but their complicated output matching structure can limit their use in beam-former RF front-ends. The proposed output matching structures have the layout footprint of a transformer, making their use in beam-former chips feasible. A 26-38 GHz power amplifier based on a non-inverting 1:1 transformer is fabricated. A measured efficiency of more than 27 % is achieved across the band with an output power of 12 dBm. Furthermore, two continuous class F^{-1} power amplifiers using 1:1 inverting transformers are described. Simulation results show a peak-efficiency of 35 % and output power of 12 dBm from 24 to 30 GHz. A common-base power amplifier with inverting transformer output matching

is also demonstrated. This amplifier achieves a peak-efficiency of 42 % and peak output power of 16 dBm.

Finally, a low-loss Ka-band re-configurable output matching structure based on tunable lines is proposed and implemented. A double-stub matching structure with three tunable segments is proposed to maximize the impedance matching coverage. This structure can potentially compensate for the antenna impedance variation in phased-array antennas.

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Dedication

This thesis is dedicated to my beloved parents Sohrab and Parvin Rasti Boroujeni.

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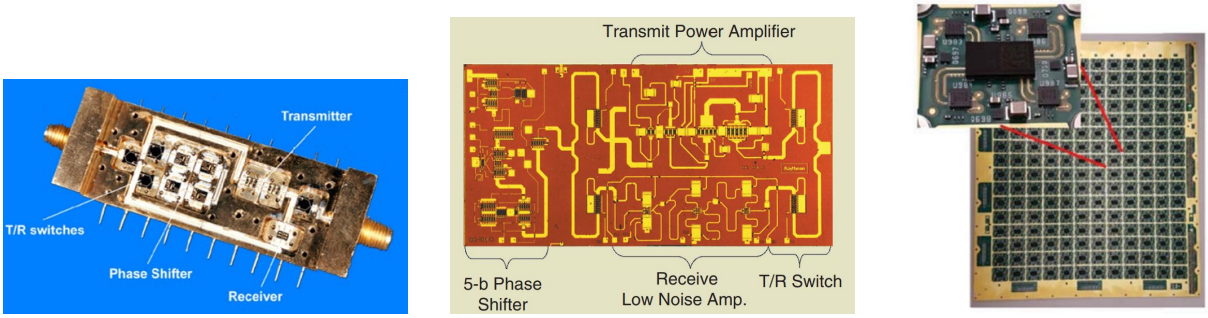
Chapter 1

Introduction

The increasing number of users with high-speed connections and the growing need for higher data rates both demand larger bandwidths and more effective use of channel capacity for the allocated spectrum bandwidths [12]. In addition, advances in 4G and 5G technologies necessitate the advent of infrastructure that can support large volumes of data traffic. The large bandwidth and steerable directional links offered by millimeter-wave (mm-wave) phased-arrays could be harnessed to cover the transmission of data over different layers of such networks [12–14]. Pico-cells and base stations for 5G networks, and mm-wave point-to-point links for back-hauls, are examples that demonstrate the potentials of mm-wave phased-arrays. These 5G networks can support a greater number of users by generating multiple beams [13]. Mm-wave phased-arrays for satellite communication at the Ku and Ka bands represent another emergent technology that aims to provide data access to users/places that cannot easily be covered by terrestrial networks [15–17]. Several digital and RF beam-forming architectures are currently being developed, each appropriate for specific applications [18]. In phased-array antennas, beam-forming happens by feeding an array of antenna elements with the correct phase and amplitude [19]. Among the beam-former architectures, baseband and RF phase-shifting have attracted the most interest; usually a combination of these techniques being employed [20].

Fig. 1.1 shows the historical development of RF beam-forming circuitry. Phased-array antennas were initially developed for radar systems. Each antenna was fed by a Transmit/Receive (TRX) module. Each module was implemented by a separate discrete phase-shifter, TRX switch, transmitter, and a receiver. The cost and complexity of assembling a high number of components in each TRX module were the main motivations behind developing a monolithic microwave integrated circuit that has all the components of a TRX module in one chip, as shown in Fig. 1.1(b). The advancement of silicon technology and



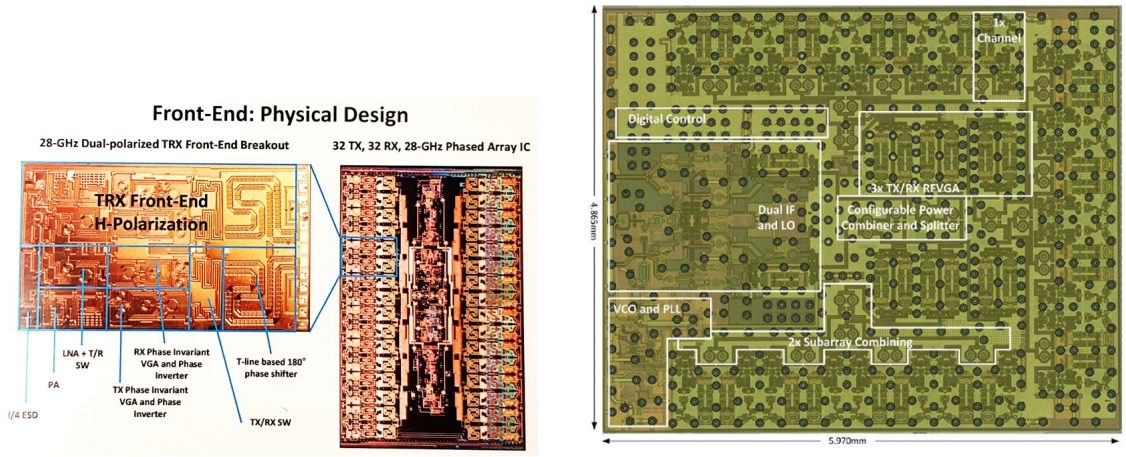
(a) (b) (c)

Figure 1.1: Historical development of active phased-arrays. (a) The first TRX module consisted of MMICs [1]. (b) First fully integrated TRX module operating at X-band [1] (c) 768-element phased-array radar using silicon as beam-former and Gallium-Arsenide (GaAS) technology Power Amplifier (PA) and receiver [2].

availability of transistors with f_t of more than 250 GHz [21] paved the way for lower-cost beam-former chips [22]. The combination of digital control and superior RF performance in the same chip make the implementation, test, and debugging cost of phased-arrays more affordable for commercial applications [23, 24].

The output power of silicon chips is limited due to the low breakdown voltage in advanced silicon technologies. Therefore, in applications that need high Effective Isotropic Radiated Power (EIRP), the use of silicon beam-former chips integrated with GaAs PAs has been reported [2, 25, 26] but at the expense of higher implementation and test costs. Fig. 1.1(c) shows an example of these phased-arrays. For a given EIRP, as the number of elements in an array increases, the radiated power per element decreases. For large phased-arrays, the radiated power of each antenna is in the range of power that is feasible by PAs in silicon technology. Implementation of all the RF and control circuitry in one silicon die reduces the cost of these systems significantly. Therefore, [3, 27–29] reported all-silicon phased-arrays for 5G base stations as a potential application. A comprehensive review of all-silicon phased-array antennas is presented in [18]. Fig. 1.2 shows two examples of silicon-based multi-channel phased-array chips. Due to the large number of elements in an antenna array, the power consumption of these chips is a key factor that can make the thermal dissipation of these transmitters a challenge.

Satellite communications (SATCOM) systems are currently being developed to provide low-latency and high data throughput connectivity around the globe. The satellites orbiting in Low, Geostationary, and Medium Earth Orbits (LEO, GEO, and MEO) are expected

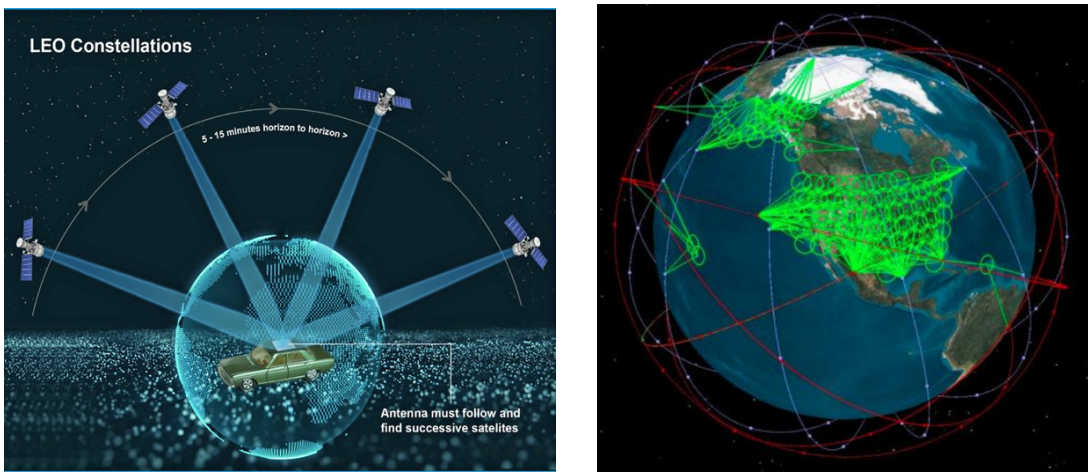


(a) (b)

Figure 1.2: Two examples of all silicon phased-array TRX chips for 28 GHz 5G. (a) 32-channels TRX chip with channel area of 5.2 mm^2 [3]. (b) 24-channel phased-array chip with channel area of 1.16 mm^2 [4].

to provide reliable internet connection through High Throughput Satellites (HTS) [30] systems. Broadband internet to ground subscribers, maritime connectivity, and in-flight internet access are some examples of potential uses for this technology. These Satellite Communication On The Move (SOTM) systems need to point the main beam of their antenna toward the satellite, which can look to the fixed ground terminal either stationary for GEO or in motion for LEO and MEO satellites. Fig. 1.3(a) shows a graphical application of SOTM and Fig. 1.3(b) shows the cluster of satellites in space to support this communication. Therefore an affordable antenna system with agile beam steering capability is needed for users to connect to HTS systems [2, 13]. Fig. 1.4(a) shows a reflector antenna optimized for this application.

Low profile, power consumption, and cost are the key requirements for these antennas. Fig. 1.4 shows the main trend in the development of these antennas. Several solutions have been proposed for high gain low profile antenna systems during the past decades. In [31] a mechanical system called Variable Inclination Continuous Transverse Stub Array (VICTS) has been proposed where the phase adjustments of the radiating elements are realized by three rotating plates of antenna, feed, and polarizer. One commercial example of this antenna is shown in Fig. 1.4(b). In [32] another flat panel based on near field transformation with a rotating meta-surface is proposed. The main disadvantage of these mechanical systems is their response time due to its mechanical nature and their large



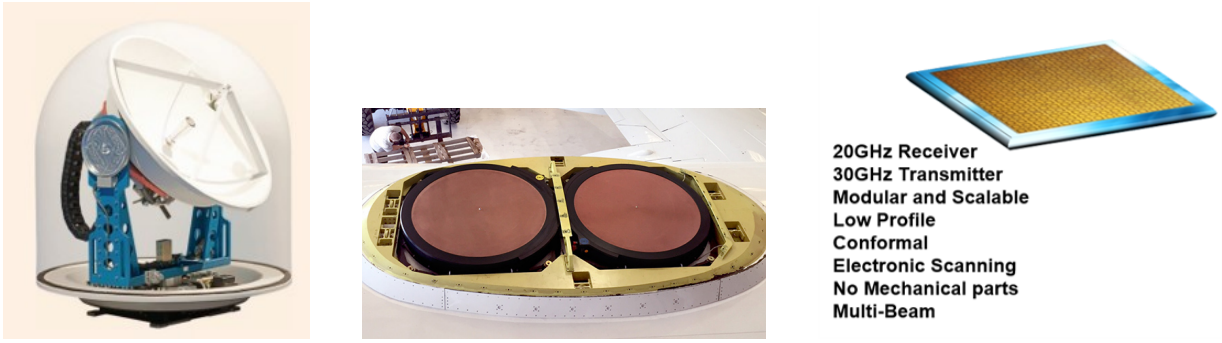
(a) (b)

Figure 1.3: (a) Mobile SATCOM conceptual use case for a car [5]. (b) Graphical cluster of satellites at LEO (Courtesy of Via-Sat).

weight. Using holographic switchable meta-surface [33] is also another solution that has a moderate bandwidth. All three mentioned systems need a high power amplifier. To compensate the feeding loss and the loss associated with the beam-forming mechanism, the amplifier should deliver higher output power. This reduces system reliability and necessitates a complex heat management system. Furthermore, there is no side-lobe and polarization control mechanism over the scan angle and at different temperatures in these systems.

Active phased-array antennas have attracted tremendous interest during the past decade [18, 34]. Digital, RF, and hybrid beamforming architectures have been proposed and implemented [35–37] using CMOS technology. In digital phased-array chips, the RF signal is down (up)-converted to (from) base-band and the signal combining is performed in the digital domain [37]. Although combining signals in the base-band simplifies the RF-feeding network and enables the digital processing capabilities but the chip complexity increases significantly. One mixer and analog to digital converter are required per each antenna element. Each beam-former chip may require an RF phase-locked loop or synthesizer to generate the required LO signals. Furthermore, the high power consumption of these solutions makes thermal dissipation a challenge.

RF beam-forming solutions implemented using advanced SiGe or SOI technologies enable superb RF performance with a noise figure of less than 2 dB on package [38] and PA

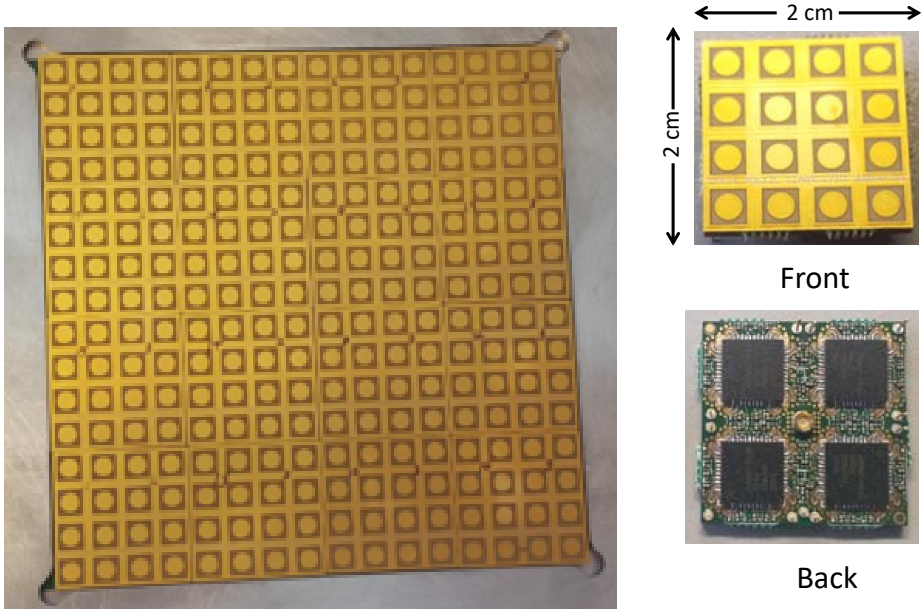


(a) (b) (c)

Figure 1.4: (a) A Ka-band reflector antenna developed for mobile SATCOM [6]. (b) A low-profile antenna developed using VICTS technology [7]. (c) A flat panel active phased array antenna.

peak efficiency of higher than 30 % [39, 40]. In transmitter RF front-ends, each chip has N RF-inputs (usually 1) and M (usually 4 or 8) RF-outputs. The RF signal goes through a phase shifter, variable gain control, and a PA which drives the antenna element. The digital control, storage, and processing capability of these chips offer the unique feature of self-test and self-characterization of RF-channels [41, 42]. Furthermore, the gain and phase control states can be stored in each chip for ultra-fast beam-forming algorithm implementation. Phased-array antennas with RF beam-forming require a large RF feeding network with low loss RF substrates which adds to the cost of the system. However, the advancement and maturity of multi-layer laminate and Printed-Circuit-Board (PCB) technologies [43, 44], is dropping the cost of the RF feed network.

Active phased-arrays with hundreds to thousands of antenna elements are needed for SATCOM. These antenna arrays are implemented on either one or multiple PCB batches [2]. This approach requires very accurate PCB manufacturing on large scales and increases the manufacturing cost. To avoid this issue, a modular and scalable architecture based on 4×4 active antenna sub-arrays has been developed to implement these massive antenna arrays [8] as shown in Fig. 1.5. The very small sub-array size in this technique significantly reduces the test and maintenance cost of these large phased-array systems. In active phased-array antennas, the generated heat is distributed across the antenna aperture. This relaxes the heat dissipation system. Furthermore, by employing a modular architecture, failure in one or some of the PAs does not severely affect the communication link performance. This results in higher reliability compared with other low profile antenna systems [31, 33]. The power consumption of RF-beamforming architecture is much lower

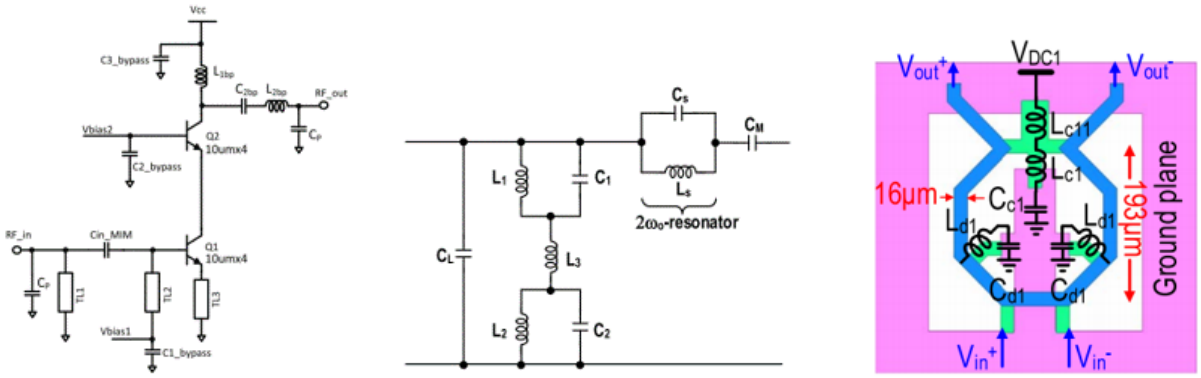


(a) (b)

Figure 1.5: (a) A Large 256 elements phased array transmitter antenna. (b) A 4 × 4 active-antenna sub-array [8].

than digital beam-forming architectures and makes it an affordable solution for mobile applications. Several silicon-based Ku and Ka-band SATCOM beam-former chips have been reported in the academia [45] and industry [46–48]. However, the high cost and power consumption of these chips limit the maximum size of the array due to DC power budget limitations on mobile platforms and heat dissipation challenges. The focus of this thesis research is to find power-efficient solutions for large phased-array transmitters. The main application of these transmitters is ground terminals for satellite communications [2, 49, 50] and sub-arrays for MIMO transceivers in 5G networks [3, 25, 27, 51, 52].

Wideband mm-wave large phased-array systems are the key element of emerging communication systems for enhancing the capacity of the channel by providing multi-band, multiple steerable directional beams [2–4, 53]. These phased-array systems will be used in the 5G network as a base station antenna, Customer Premises Equipment (CPE), mobile user terminals to connect to the satellite, and in satellites on the space side of the link. Several frequency bands including 24, 28, 38, and 39 GHz have been allocated for a 5G net-



(a) (b) (c)

Figure 1.6: Schematic diagram of various harmonic-tuned PAs proposed in the literature. (a) A 28 GHz continuous class-AB PA [9] (b) A 28 GHz class F^{-1} PA [10]. (c) A fully-differential 24-38 GHz continuous mode PA [11]

work in different regions [54]. In addition, Ku (10.7-12.75 GHz / 14-14.5 GHz) and K/Ka (17.5-20.2 GHz / 27-30 GHz) bands are the specified bands for SATCOM with several research and development efforts and significant interest for electronic beam-steering antenna systems [2, 8]. Therefore, a broadband front-end that can support multi-bands/standards is highly desired.

In 5G standards, signals with high-order modulation (e.g., 256 or 1024 Quadrature Amplitude Modulation (QAM)) are proposed to use the allocated spectrum efficiently and deliver Gb/s data rates [55]. Therefore, the PA for the 5G application needs to be highly linear. Furthermore, in existing SATCOM systems, lower complexity modulation schemes such as Quadrature Phase Shift Keying (QPSK) are being used in the transmitter side and the PA can operate in saturation mode to achieve higher efficiency [15]. However, emerging SATCOM applications are also expected to use more complex modulations to increase the data rate [56]. Therefore, wide bandwidth, high efficiency, and linearity are the key requirements and challenges in a mm-wave PA that need to be addressed.

Numerous silicon-based PAs have been recently reported [9, 10, 57–68]. Switching mode amplifiers like class E [57, 59] have narrow bandwidth and suffer from poor linearity and lower efficiency at mm-wave. Harmonic-tuned amplifiers like class-AB [9, 60–65, 69], F [66] or F^{-1} [10, 66, 67, 70–73] have been shown to offer good linearity and high peak-efficiency (>40%). However, creating short or open-circuit at the harmonics, limits the bandwidth and increases the layout area [9, 10, 66, 67, 70, 71]. This prohibits their application in

the beam-former MMICs or MIMO systems. Fig. 1.6 shows some examples of proposed harmonic-tuned PAs. The complex output matching structure in these PAs limit their application in a phased array chip.

Continuous-mode PAs offer high efficiency over a wide bandwidth [11,70,72,74]. These amplifiers are the generalized form of class-AB, F or F^{-1}. The harmonics are terminated by reactive impedances instead of short or open-circuits and therefore, the narrow-band harmonic traps can be eliminated. In [9] a 28 GHz continuous-mode PA with a complex output matching network is reported which has only 10% bandwidth. In [11] a broadband fully differential continuous-mode PA with a compact layout is introduced which is shown in Fig. 1.6(c). An efficiency greater than 40% is reported. This can be attributed to the output matching simplicity, higher quality factor of on-chip transformers in differential-mode [75], and using neutralized transistors. However, a differential output is not desirable in a phased-array integrated circuit (IC) as it increases the number of output pads and can potentially double the size of the die. Furthermore, since the antenna element input in phased-arrays is usually single-ended, an on-chip or off-chip Balun is required to convert the differential output to single-ended. This results in 0.7 to 1 dB extra loss at Ka-band [75,76] which contradicts the lower loss of a differential output matching. In addition, in large phased-array terminals for SATCOM, the average radiated power of each antenna is usually low and is in the range of 6-8 dBm. The R_{opt} of a single transistor in CMOS or BiCMOS technology at this power is close to 50 Ω. The differential PA is not desirable for low output power levels as it doubles the impedance transformation ratio and increases the output matching loss and reduces the bandwidth. Therefore, in this thesis, single-ended PA structures are investigated.

1.1 Statement of Problem and Thesis Structure

In large phased-array antennas, the need for hundreds to thousands of active-antenna elements results in the co-operation of many PAs with low output power. The associated total power consumption and thermal dissipation challenges require the design of power-efficient beam-former chips. Furthermore, since the cost of active components in a phased-array is the main barrier toward the commercialization of this technology, the design of novel structures with a small layout area is a must.

In this thesis, power-efficient techniques to enhance the efficiency of large phased-array transmitter antennas are presented. The structure of the thesis can be divided into three parts:

In the first part which is presented in Chapter 2, the system-level requirements of a beam-former chip are investigated first and a power-efficient front-end solution for Ka-band SATCOM active phased-array transmitters is proposed. The front-end architecture is optimized for minimum DC power consumption and simple amplitude and phase control.

In this work, a single-channel power-efficient beam-former chip is developed for mobile SATCOM. The chip is designed to deliver 10 dBm output power. This is based on the system-level requirements of implementing an array with 13250 elements and EIRP of 48.5 dBW. Our developed chip achieves the lowest reported DC power consumption at 30 GHz for 10 dBm output power. Furthermore, the phase resolution of existing SATCOM chips was limited to 5.6°. This limits the achievable beam-pointing accuracy, cross-polarization, and maximum sidelobe level. Therefore, a continuous phase shifter that will be controlled by a 10-bit Digital to Analog Converter (DAC) is implemented in this work.

In an active antenna array, to reduce the amplitude of radiation side lobes to the desired level, the antenna amplitudes are tapered by more than 12 dB. This will cause more than half of the array elements to operate at deep back-off and this degrades the efficiency of the system further. The adaptive supply voltage is employed to enhance the efficiency of the chip at power back-off.

Following our goal of developing power-efficient beam-former chip solutions, in the second part of the thesis, Chapter 3 and 4 focus on PAs which are the most power-hungry elements in a beam-former front-end. In these chapters, high efficiency and broadband PAs with a compact layout area are presented. These PA solutions offer high efficiency with a compact layout area which results in integrating more number of channels for the given die area. By investigating the properties of a 1:1 transformer, novel output matching structures for harmonic tuned PAs is proposed and validated by measurement and simulation.

In the third part of the thesis, Chapter 5 the antenna impedance in active arrays is investigated and a solution to compensate the antenna impedance variation is proposed. A low-loss off-chip re-configurable matching network is presented that can compensate for the antenna impedance variation.

Chapter 2

A Power Efficient BiCMOS Ka-Band Transmitter Front-End for SATCOM Phased-Arrays[1]

2.1 Introduction

As part of the thesis work, a single-channel power-efficient beam-former chip was developed for mobile SATCOM. The chip was designed to deliver 10 dBm output power. This value was determined based on the system-level requirements of implementing an array with 13,250 elements and an EIRP of 48.5 dBW. The chip is designed for for 10 dBm output power at 30 GHz. Furthermore, the phase resolution of currently existing SATCOM chips is limited to 5.6°. This limits the achievable beam-pointing accuracy, cross-polarization, and maximum sidelobe level. Therefore, a continuous phase shifter controlled by a 10-bit DAC was implemented as part of the designed chip.

[1]This work was carried out with the help of Dr. Mohammad-Hossein Mazaheri (for phase shifter design) and Aneta Wyrzykowska (for variable attenuator design). The measurement results reported in this chapter are included in the paper accepted for IMS 2020, "A Power Efficient BiCMOS Ka-Band Transmitter Front-End for SATCOM Phased- Arrays", S. Rasti Boroujeni, et. al.

2.2 System Level Specification

To determine the target specifications of an RF beam-former chip, it is necessary to conduct a system-level analysis. Based on this analysis, the main parameters of a phased-array chip for a use-case of a user-terminal communication link with GEO orbit satellite were analyzed. The phased-array antenna was assumed to have the same EIRP of 48.4 dBW as a commercial Ka-band reflector antenna [77] at 30 GHz. The operating frequency considered for this active array is 27 to 30 GHz.

Array size and EIRP

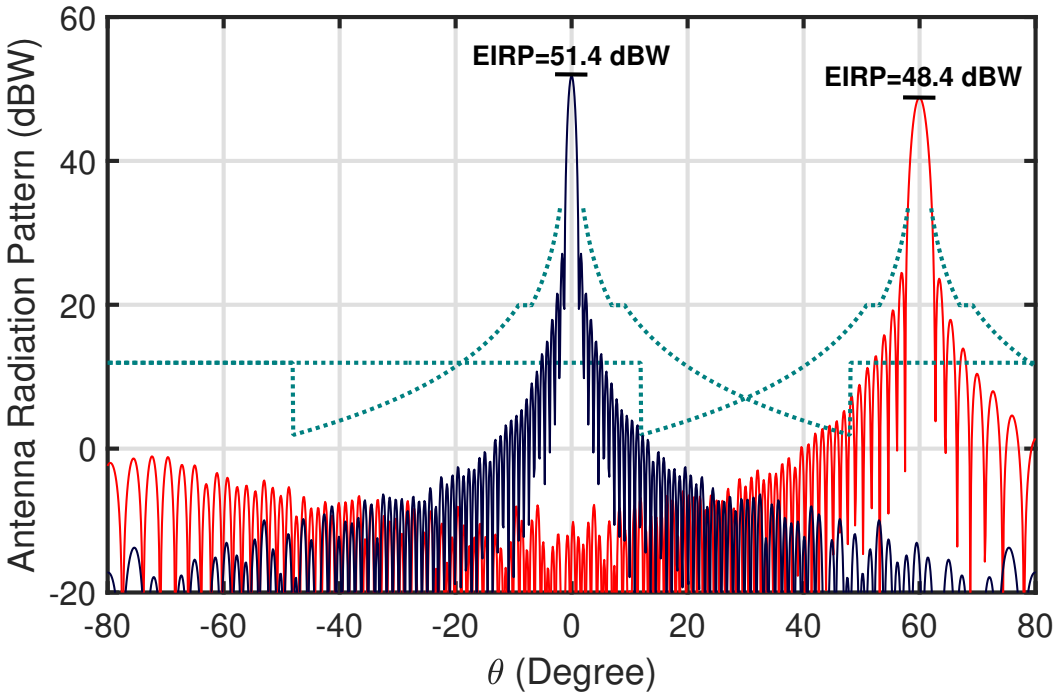
The size of an array is mainly determined by the required peak-EIRP and the FCC emission regulation [78], shown in Fig. 2.1 by a dotted line. The antenna array radiated power should not exceed this limit at any scan angle. The FCC radiation mask imposes a radiation limit of 33.4 dBW at $\theta = \theta_0 \pm 2^\circ$ and the satellite communication link requires an EIRP of 48.4 dBW at θ_0 =60°. For a circularly truncated rectangular array, the minimum number of antenna elements that would meet these two conditions is 13,250. The antenna's radiated power would be 0.8 mW. The array size and output power are found by array optimization for a required EIRP and beam-width. For an array this size, the required 15 dB radiation drop occurs at ±2° offset from the main beam angle. Fig. 2.1 shows the radiation pattern of this array at 0 and 60°. A 10 dB Gaussian tapering has been applied to keep the generated side-lobes below the radiation mask. This results in a tapering loss (L_{TL}) of 4.5 dB.

PA Output power

The required output power of the PA can be calculated by considering the loss factors in the array's operation. The PA average output power is given by

$$P_{out} = P_E + L_{FL} + L_{PM} + L_{AS} + LM \tag{2.1}$$

where P_E is the antenna radiated power of the center element in dBW (the element with the highest output power), L_{FL} is the feed loss, L_{PM} is the polarization mismatch loss, L_{AS} is the impedance mismatch loss due to active scan impedance at the scan angle [79] and LM is the communication link margin. For this analysis, we assumed a constant antenna radiated power of 0.8 mW (−1 dBm), as described in the previous section. Table 2.1 lists the loss factors and the PA average output power at different scan angles. At $\theta_0 = 60^\circ$, the PA has an average power of 2.5 dBm. For a modulated signal of QPSK or 16-QAM,



(a)

Figure 2.1: Radiation pattern of 13,250-element array at bore-sight and $\theta_0 = 60^\circ$. The FCC radiation mask for a signal bandwidth of 6.25 MHz is plotted at both angles by a dotted line.

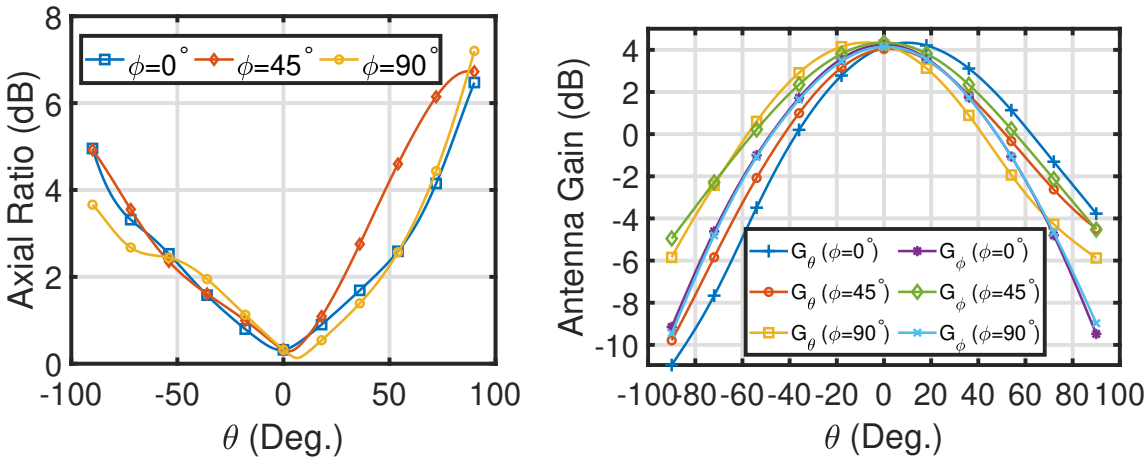
Table 2.1: Summary of Loss Factors and PA Average P_{out} at Different Scan Angles

θ_0	P_E (dBm)	L_{FL} (dB)	L_{PM} (dB)	L_{AS} (dB)	$P_{out,avg}$ (dBm)
0	-1	1	0	0	0
30	-1	1	0.5	0.5	1
60	-1	1	1	1.5	2.5

the signal has a Peak to Average Power Ratio (PAPR) of about 4 dB. Considering the communication link margin of 4 dB, the PA requires a linear response up to 10.5 dBm to generate 48.4 dBW at $\theta_0 = 60^\circ$. The EIRP increases to 51.4 dBW at bore-sight due to a 3 dB lower scan loss.

Gain Control

To control the radiated power, side-lobe level (SLL), and polarization of the antenna array, the amplitude of the RF signal needs to be adjustable. An amplitude tapering of about 10 dB over the array aperture is required to reduce the radiation SLL. The other factor to consider is the Insertion Loss Variation (ILV) of the phase shifter. The reported silicon-based continuous phase shifters usually have 2-5 dB ILV to achieve 360° phase shift [80,81]. Since we have a 200° continuous phase shift in our design, a 3 dB ILV was considered sufficient for our gain variation budget analysis. Degradation of the antenna's Axial Ratio (AR) by scan angle is the third parameter that determines the total gain variation. A circularly polarized patch antenna will only provide 0 dB AR at bore-sight angle, with the AR degrading as θ increases. Dual-polarized antenna elements are usually employed to adjust the phase and amplitude of each feed and correct the AR at other angles. An amplitude adjustment of up to 3 dB for each feed is usually needed [82] to generate a circularly polarized radiation pattern. Fig. 2.2 shows the G_θ, G_ϕ and AR of a dual feed patch antenna over different angles. There is 2-3 dB gain difference and 30° phase error at $\theta = 60^\circ$, that needs to be adjusted to achieve circular polarization. Considering all of the above mentioned factors, a gain control of up to 16 dB was targeted in our design.



(a) (b)

Figure 2.2: Simulation results for a dual-feed single rectangular patch antenna over different angles. The inputs are excited by equal amplitude and 90° phase differences. (a) AR. (b) G_θ and G_ϕ over different angles.

Phase Range and Phase Shifting Accuracy

In phased-arrays for SATCOM, a beam steering range of up to ±60° is required. This will translate to an inter-element phase difference of 156° (at 30 GHz and assuming $\frac{\lambda_0}{2}$ element spacing). Therefore, considering a large phased-array covering ± 60°, the full phase shift range of 360° is required. For our design specifications, we targeted a 400° phase range to compensate for the process, voltage and temperature variation.

The continuous phase shifter will be controlled by a digital control unit. The digital circuit controlling the phase shifter introduces a phase quantization error. This error does not affect the main beam but increases the SLL of the array. The phase quantization generates undesired grating lobes in the antenna pattern as shown in Fig. 2.3. According to this analysis, at least 7 bits are needed for quantization of the 360° phase range to avoid violating the radiation mask, as shown in Fig. 2.3. In this work, we used a 10-bit external DAC to generate the analog control voltage for our chip characterization.

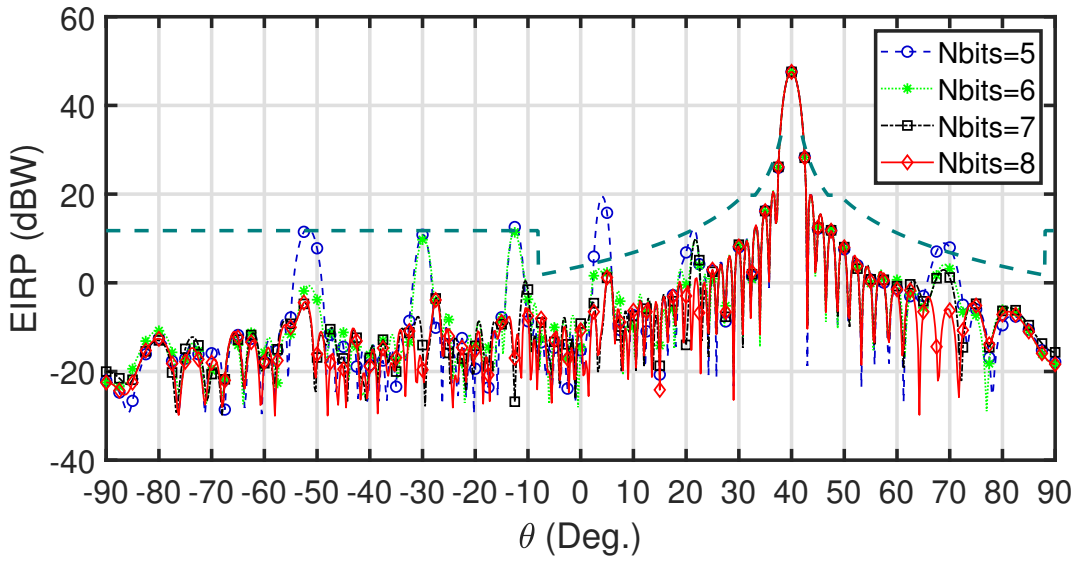
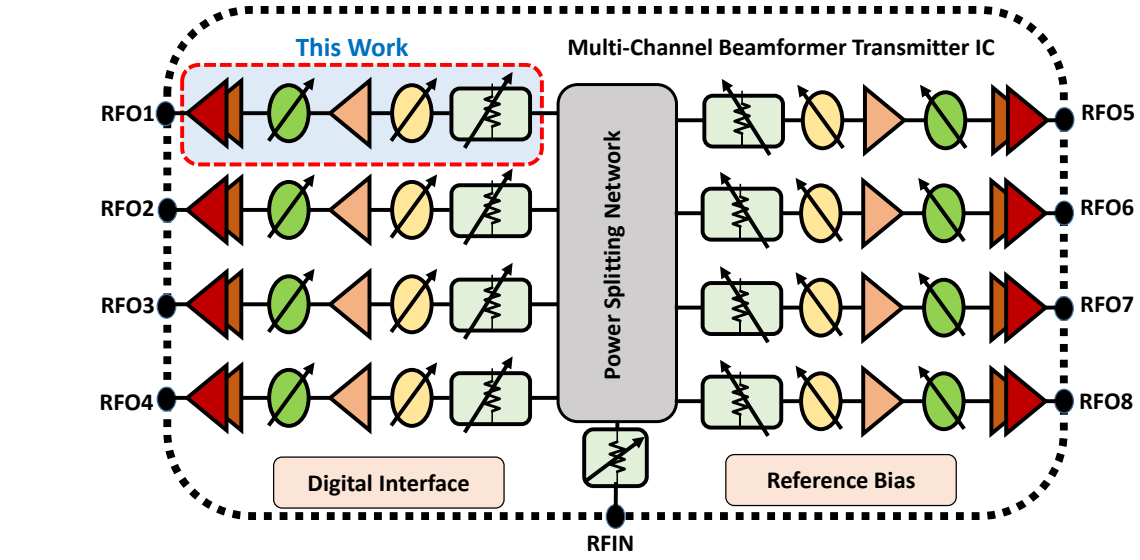


Figure 2.3: Effect of phase-shifter resolution on phased-array antenna pattern.

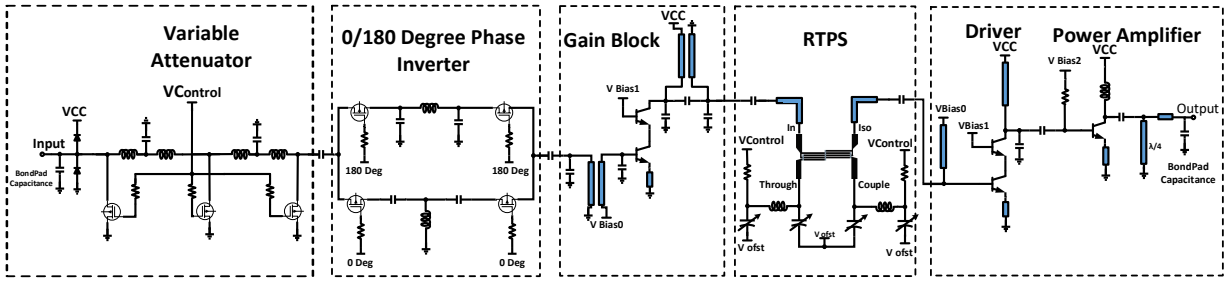
2.3 Building-Block Design and Characterization

The architecture of the implemented chip is shown in Fig. 2.4(a). The proposed RF front-end was fabricated using Global-Foundries' 0.13μm BiCMOS SiGe-8XP technology with f_T/f_{max} of 250/340 GHz. This process has three RF metal layers (AM, LY and MQ) and four thinner copper layers (M1 to M4) for digital circuitry and other purposes. The high breakdown voltage of HBT transistors in this process enables high-efficiency PA design. According to the analysis in Section 2.2, the chip was designed to have a 360° phase range, 16 dB gain control and OP_{1dB} of 12 dBm. A wide-band passive variable attenuator was used along with a fixed gain stage to control the gain. Lower power consumption can be achieved by using this technique compared to using active variable gain amplifiers [3,83]. A phase shift of 400° was achieved through a combination of a continuous 220° Reflective-Type Phase Shifter (RTPS) and a one bit 0/180° phase shifter. Although 360° phase shifters have been reported in the literature, they have large ILV and need two control voltages and extensive tests for calibration [80,84]. Therefore, we decided to limit the phase range of the RTPS phase shifter to 220° to simplify the array calibration.

Below, the simulation and measurement results of the five building blocks are presented, shown in Fig. 2.4, followed by the simulation and measurement results of the single channel.

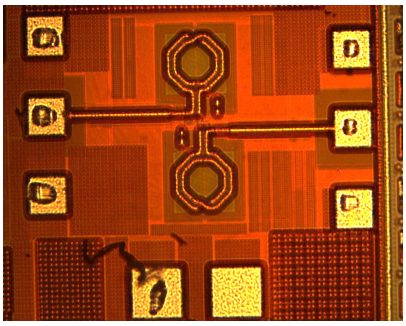


(a)

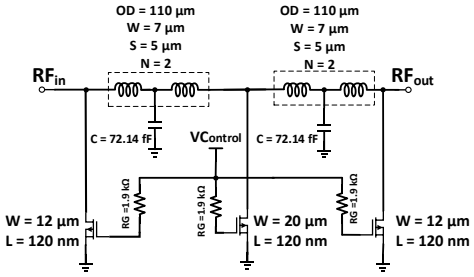


(b)

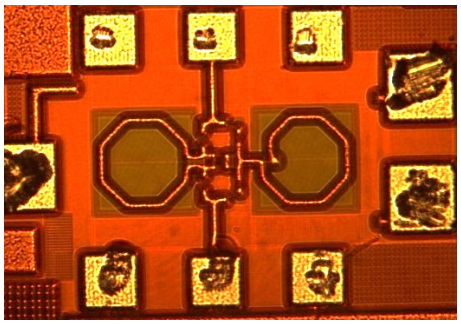
Figure 2.4: (a) Block diagram of 8-channel beam-former chip for SATCOM phased-array transmitters. (b) Schematic diagram of RF-core of 8-Channel TX beam-former chip.



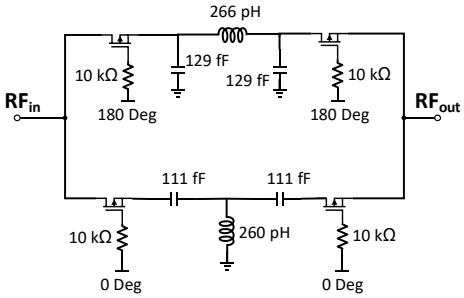
(a)



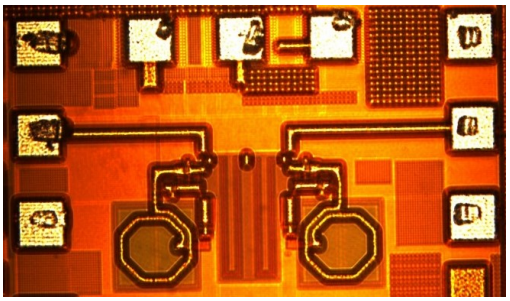
(b)



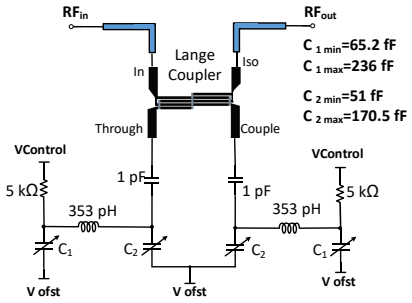
(c)



(d)



(e)



(f)

Figure 2.5: Micro-graphs and schematic diagrams of fabricated chip blocks: (a,b) variable attenuator, (c,d) phase inverter, and (e,f) RTPS.

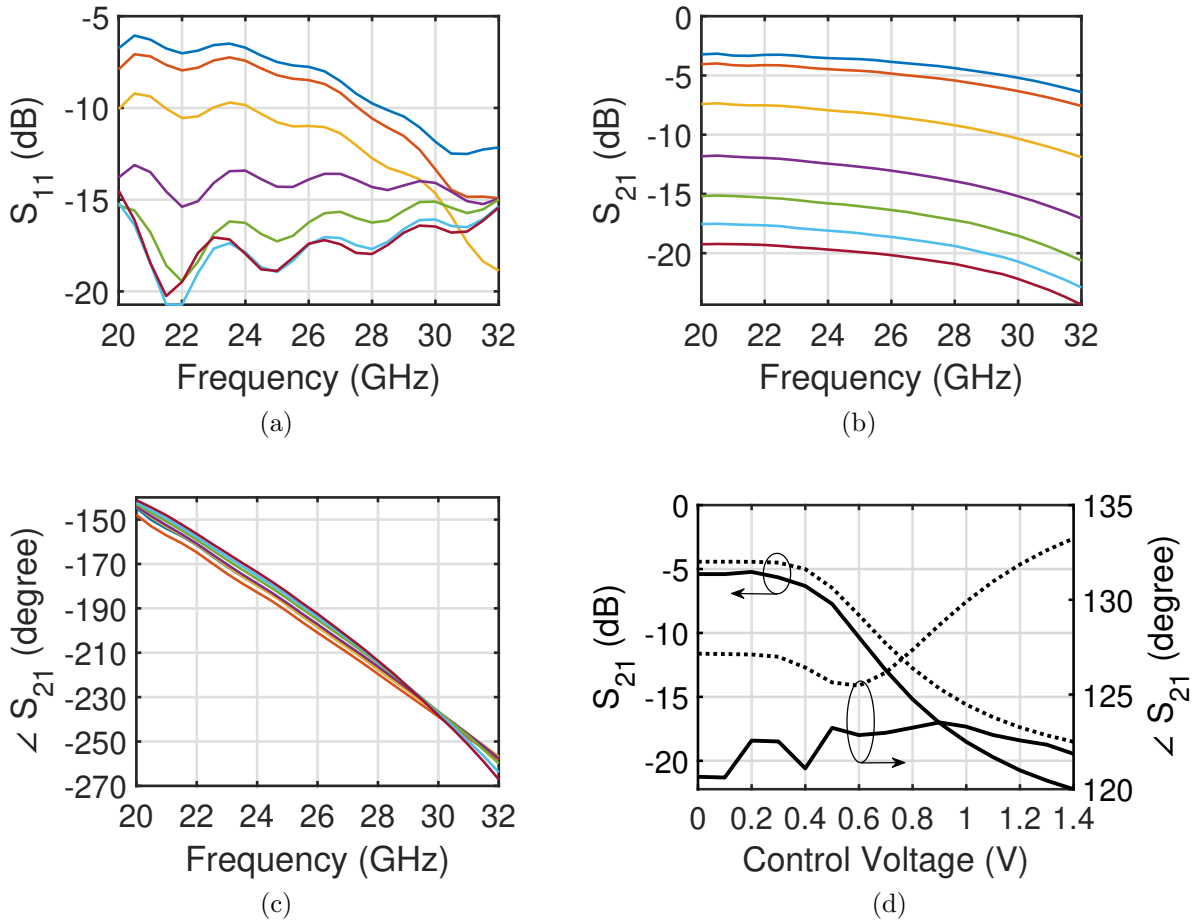


Figure 2.6: Variable attenuator simulation and measurement results. (a,b) measured S_{11} and S_{21} vs control voltage. (c) S_{21} phase variation with control voltage. (d) Comparison of measurement (solid line) and simulation (dotted line) of S_{21} phase and amplitude variation with control voltage at 30 GHz.

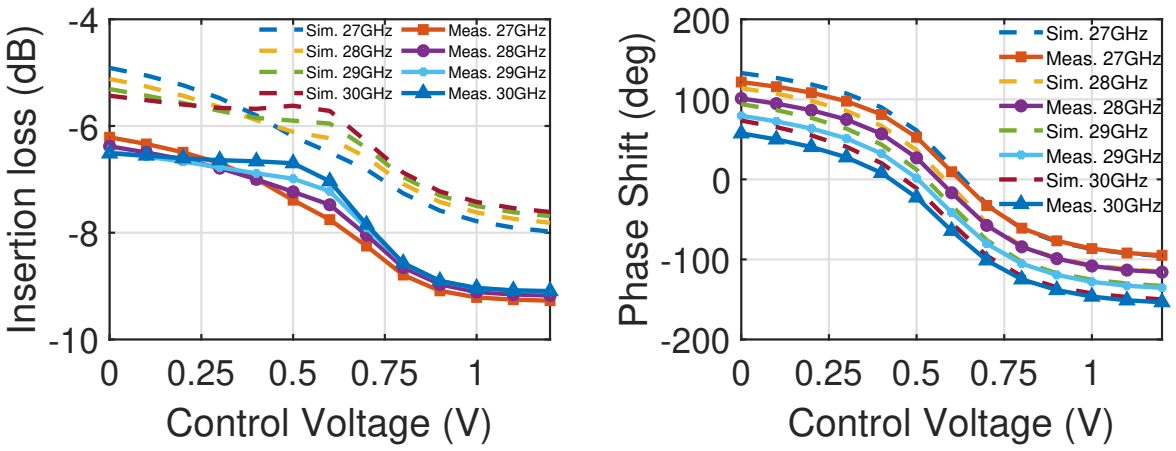
2.3.1 Variable Attenuator

As described in Section 2.2, 16 dB of gain variation is required for adjusting the antenna amplitudes. The amplitude variation should have minimal impact on the phase of the RF signal to simplify the chip and array calibrations [3]. In this work, the variable attenuator was built by cascading two identical variable attenuator units [85]. Each unit is a π network which consists of a 50 Ω quarter wavelength line and two shunt Field Effect Transistors (FET). The transistors are biased in the triode region and act as variable resistors. Each section provides 8 dB of attenuation with good matching performance and minimum phase variation over a wide bandwidth. The quarter wavelength line is implemented with lumped elements to reduce the layout area. To further minimize the interconnect and layout area, the two inner transistors have been combined into a single FET of twice the size. A single voltage is used to control the bias of the transistors. The design is optimized for minimum phase variation over the gain control range. Fig. 2.5(a) shows the fabricated die for block characterization and Fig. 2.5(b) shows the schematic diagram of the block. Measurement results are shown in Fig. 2.6. The measured minimum insertion loss is -5 dB and the phase variation is $\pm 3^{\circ}$ at 30 GHz. The measured S_{21} is about 3 dB higher than the simulated loss. The measurement results show the wide-band response of 16 dB amplitude variation from 20 to 32 GHz. In addition, the phase error is minimum at 30 GHz and increases to $\pm 5^{\circ}$ within the operating bandwidth.

2.3.2 Phase Shifter Blocks

RTPS

As mentioned in Section 2.2, the phase shifter must provide 400° phase shift in the desired band. Accordingly, an RTPS was designed to provide 220° phase shift along with a 1-bit 180° phase shifter to cover the desired phase range. As illustrated in Fig. 2.5(f), the RTPS is implemented using a Lange-coupler terminated with variable reflective C-L-C loads at its coupling and through ports. By changing the varactor values, the phase of the output signal changes. The varactor sizes are optimized to achieve the desired phase shift of 220° with less than 2 dB ILV. Fig. 2.7 illustrates the performance of the RTPS phase shifter and compares it with the simulation predictions. As indicated, the measured phase shift is the same as the simulate shift, however, the measured insertion loss is slightly higher. This is mainly due to the metal roughness and metal fillings required for the fabrication process.



(a) (b)

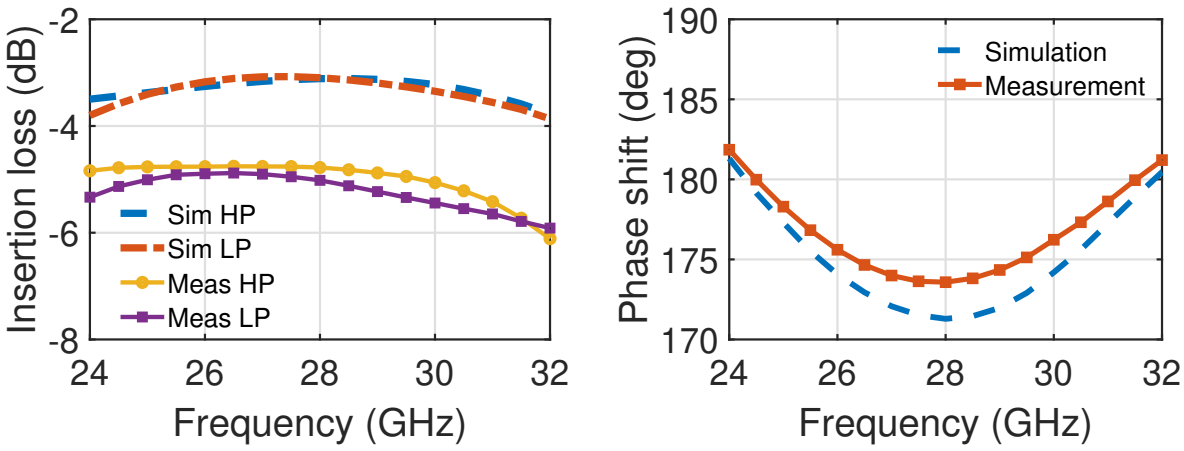
Figure 2.7: Comparison of full-chip EM simulation results with measurements of the RTPS: (a) ILV, and (b) phase variation at different frequencies.

Phase Inverter

In the phase inverter stage, by employing the Low-Pass/High-Pass (LP/HP) configuration shown in Fig. 2.5(e), the circuit switches between 0° and 180° phase shifts. In an LP/HP configuration, two filters with HP and LP responses are designed in two parallel branches. These filters have 180° phase difference to each other and equal amplitude responses. Accordingly, by employing triple-well FET switches, one branch is selected at a time to implement the desired phase shift. The simulation and measurement results are shown in Fig. 2.8. An insertion loss of -5 ± 0.3 dB and phase shift of $175\pm5°$ was achieved from 24 to 30 GHz.

2.3.3 Gain-Block

As indicated in Fig. 2.4, a cascode amplifier stage drives the RTPS phase shifter. This gain stage compensates for the loss of the preceding passive blocks. The schematic is shown in Fig. 2.9 and the die micro-graph of the fabricated block is shown in Fig. 2.10(a). The input and output matching are implemented with coupled Coplanar-Waveguide-Lines (CPW). The CPW coupled lines and the metal-insulator-metal capacitors C_1 to C_4 are optimized for minimum layout area and loss. The cascode transistors Q_1 and Q_2 are



(a) (b)

Figure 2.8: Comparison of full-chip EM simulation results with measurements of the phase inverter: (a) ILV, and (b) phase variation over bandwidth.

biased at 0.5 $mA/\mu m$ current density. Furthermore, the confinement of the EM fields in the CPW structure minimizes the risk of oscillation at higher gains. Fig. 2.11(a) shows the simulation and measurement results for this block. The simulation and measurement results are in good agreement. The measured gain (17 dB) was 1 dB lower than the simulated projection. The output power measurement in Fig. 2.11(b) shows an OP_{1dB} of 3 dBm at 28 GHz.

2.3.4 High-Efficiency Two-Stage PA

The designed two-stage PA is shown in Fig. 2.12. The last stage is implemented using a common emitter amplifier for its higher Power Added Efficiency (PAE) and better output matching compared to cascode amplifiers at VCC of 1.8 V. The transistor is biased in class-AB mode. All the transistors are biased at 0.28 $mA/\mu m$ current density. The output matching is a shunt inductor with a series capacitor and a quarter wavelength transmission line. This topology was chosen for its low-loss impedance transformation from 50 Ω load to the optimum impedance of 73+j38 Ω obtained from load-pull simulations. The output matching loss is less than 0.7 dB over the operating bandwidth; 0.2 dB of this loss is due to the quarter-wavelength line. The inductive degeneration at the output stage provides unconditional stability at the cost of lower gain. The output stage is optimized for high

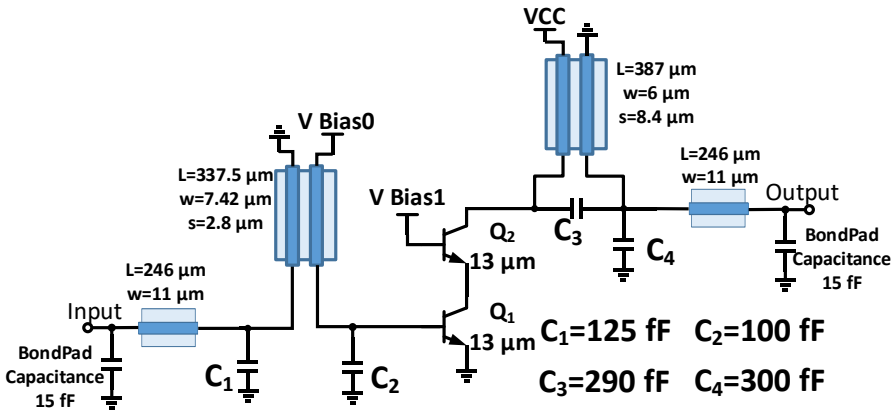


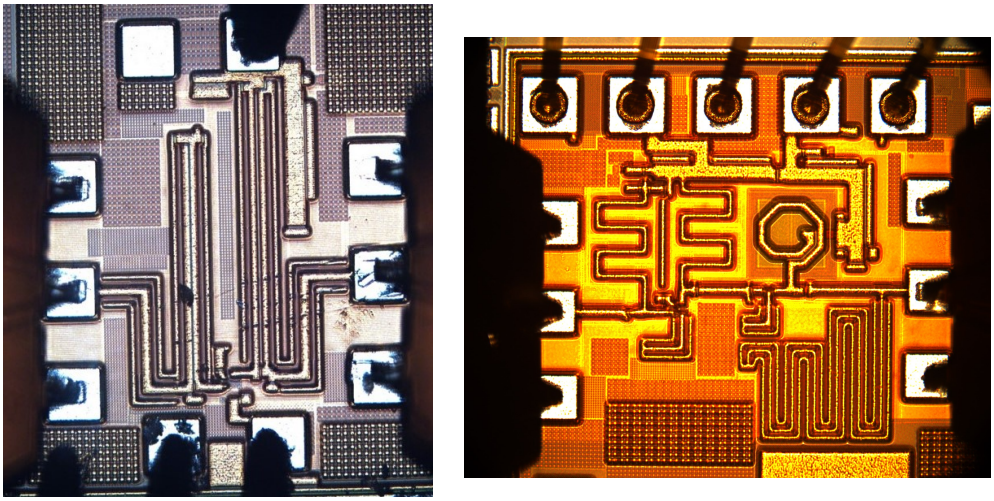
Figure 2.9: Schematic diagram of proposed gain stage.

peak-efficiency and the input stage provides the desired gain.

The driver stage is a cascode amplifier that offers higher gain and more isolation compared to common a emitter structure. Moreover, the inter-stage matching is implemented using microstrip meandered lines. The cascode transistor is degenerated to improve the stability and input matching. Furthermore, the quarter wavelength transmission line at the output provides an electrostatic discharge path as well as a second harmonic short. This minimizes the leakage of the second harmonic current in the output as well. The PA is intended to operate in a large phased-array where the operating temperature may be as high as 50-70 °C. Therefore, both the driver and output stages are biased through a 1:10 current mirror to avoid thermal runaway as shown in Fig. 2.12.

The chip has a compact layout area of 0.3 mm^2 when excluding the pads, as shown in Fig. 2.10(b). The simulated and measured small signal S-parameters of the chip are shown in Fig. 2.14; they are in good agreement. The measured gain is 1.5 dB lower than the simulated estimate which may be due to higher metal loss. The amplifier has 1 dB and 3 dB small signal bandwidths of 4 GHz and 7.6 GHz respectively. Fig. 2.15. shows the measured small signal μ factor of the PA is above one. Furthermore, the PA is unconditionally stable, and no stability issues were observed during the measurements.

Figure 2.16 shows the large signal response of the PA at 28 GHz. The measured OP_{1dB} is 0.8 dB higher than anticipated by simulation. This could be due to model inaccuracy. The measured peak-efficiency is 36 % at 28 GHz, including the current consumption of the bias circuitry. Table 2.2 summarizes the large signal performance of this chip over various frequencies.



(a) (b)

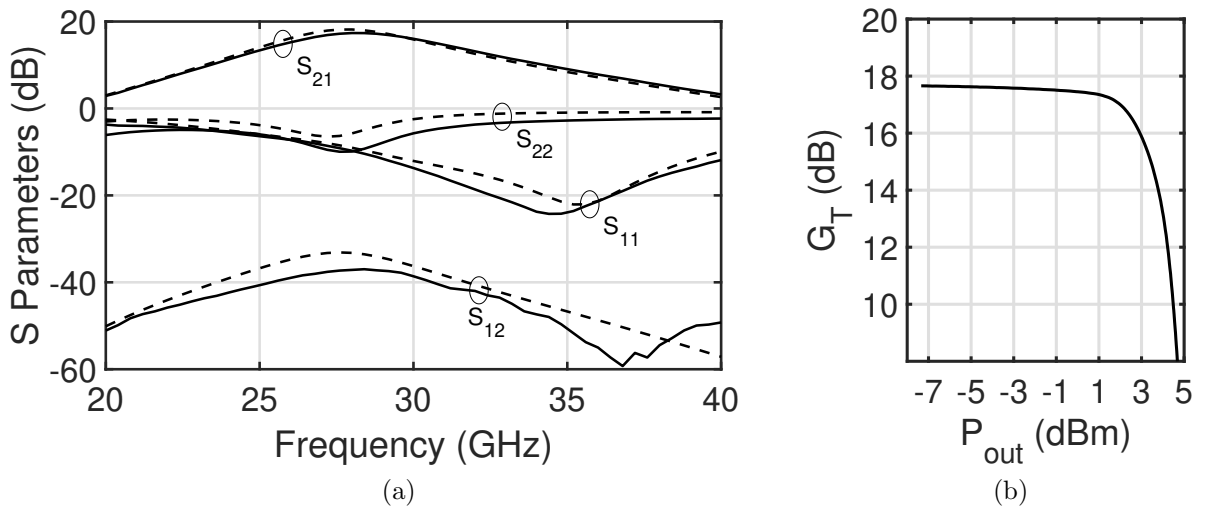
Figure 2.10: (a) Micro-graph of fabricated chip gain block. (b) Micro-graph of fabricated chip two-stage PA. Die size is 570 $\mu m \times 520 \mu m$ (pads excluded).

2.3.5 Modulated Signal Performance

The modulated signal performance of the PA was measured with a 400 MHz 64-QAM signal generated by a Keysight M8190 arbitrary waveform generator which was up-converted to 30 GHz by a Keysight E8267D signal generator. The error vector magnitude (EVM) was measured using Keysight VSA 89600 software installed on an N9041B Keysight signal analyzer. The measured EVM was 4.3 % for an average output power of 7.5 dBm at 30 GHz and 26 mW DC power consumption.

At VCC=1.8 V and an output power close to P_{sat}, we observed a sudden change in the Q_3 bias current. The bias current jumps from 9 mA to 25 mA. This is due to a Q_3 transistor breakdown which only happens at large signals under load impedance mismatch. We were not able to capture such an effect in simulation for a 50 Ω load with impedance mismatch up to -5 dB at VCC=1.8 V but we were able to observe this phenomenon at VCC=1.9 V in simulation. The breakdown does not happen for lower VCC biases. For VCC=1.7 V, we did not observe large signal breakdown in the measurement even in the case of removing the Ground-Signal-Ground (GSG) probes from the output.

Table 2.3 compares the performance of this PA with some state of the art PAs reported in the literature. This work achieves the highest reported gain with high efficiency, linearity



(a) (b)

Figure 2.11: Comparison of simulation (dashed line) and measurement (solid line) results for gain block stage: (a) small signal S-parameters, (b) transducer gain versus output power at 28 GHz.

and wide bandwidth. The PA has output electrostatic discharge (ESD) protection and can be employed in phased-array chips.

2.4 Transmitter Channel Measurement Results

In this section, the measurement results of the transmit-channel shown in Fig. 2.4 are presented. Fig. 2.19 shows the fabricated die. The die area of this chip is 1.9 mm × 0.6 mm excluding the pads. On-die measurement was performed and a short-open-load-through calibration routine was used to calibrate the network analyzer up to the probe tips. The chip was epoxy bounded on an FR4 carrier with wire bonds providing the DC bias and control voltages.

The simulated and measured small-signal S-parameters are shown in Fig. 2.20. The measured S_{21} is 5-6 dB smaller than the simulated figure. This is expected as all the measurements in Section 2.3 have approximately 1 dB lower gain in the measurement compared to previously run simulations. The transmit-channel has a gain of 23 dB at 30 GHz.

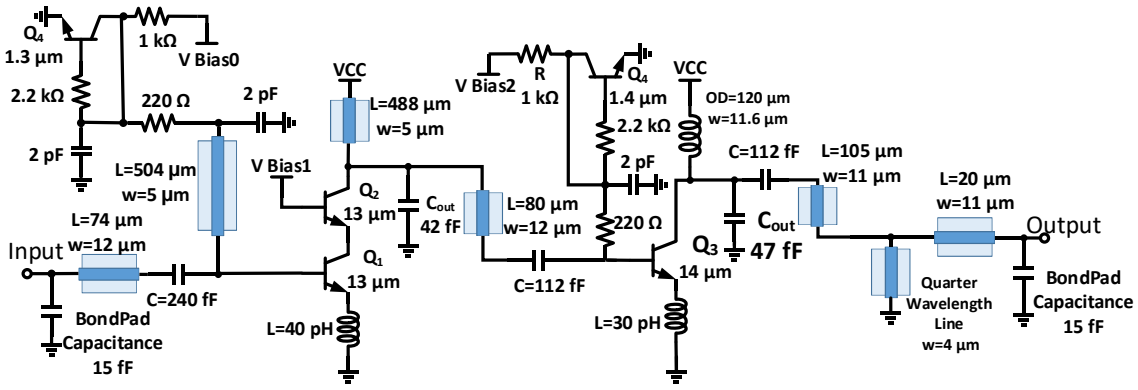


Figure 2.12: Schematic diagram of implemented two-stage PA.

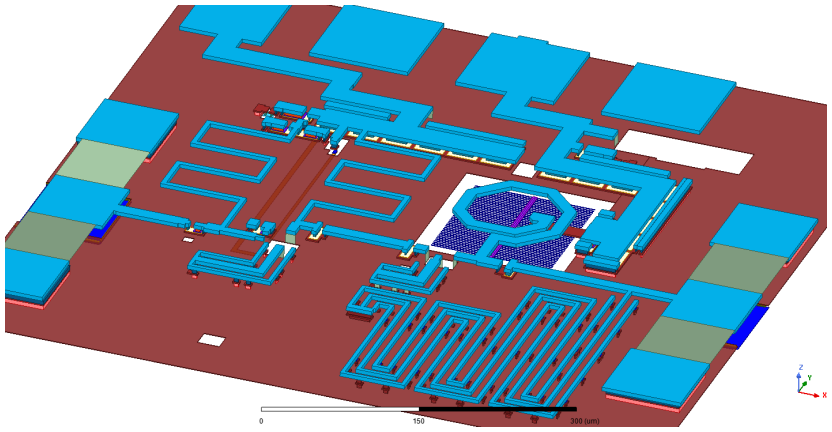


Figure 2.13: Three dimensional layout of designed PA in ANSYS HFSS.

2.4.1 Small Signal Phase and Amplitude Control

Fig. 2.17(a) shows the measured amplitude variation as a function of control voltage. A maximum gain of 23 dB is achieved. The gain variation of the transmitter channel is 16 dB; similar to the block-level measurements. However, the phase error has increased from $\pm 3^{\circ}$ to $\pm 5^{\circ}$, as shown in Fig. 2.17(b). Furthermore, Fig. 2.17(a) illustrates the input matching of the chip which at some attenuation levels becomes close to -6 dB. This is mainly due to the ESD protection diodes loading the input impedance of the attenuator. Note that the input matching of the attenuator block, presented in Fig. 2.6(a), is better

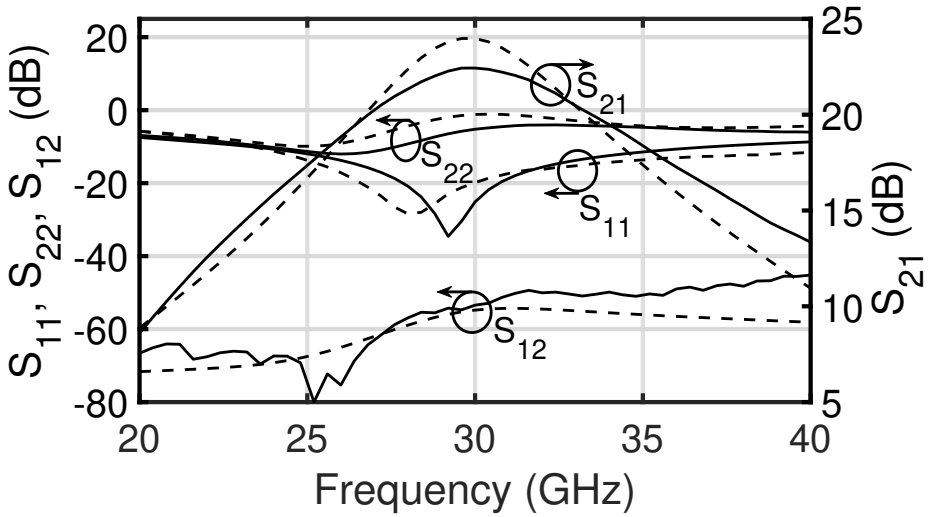


Figure 2.14: Comparison of measurement (solid line) and simulation (dashed line) of small signal S-Parameters.

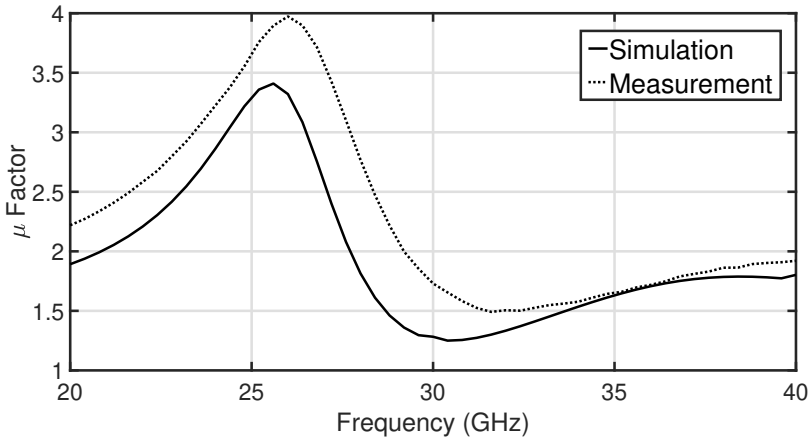
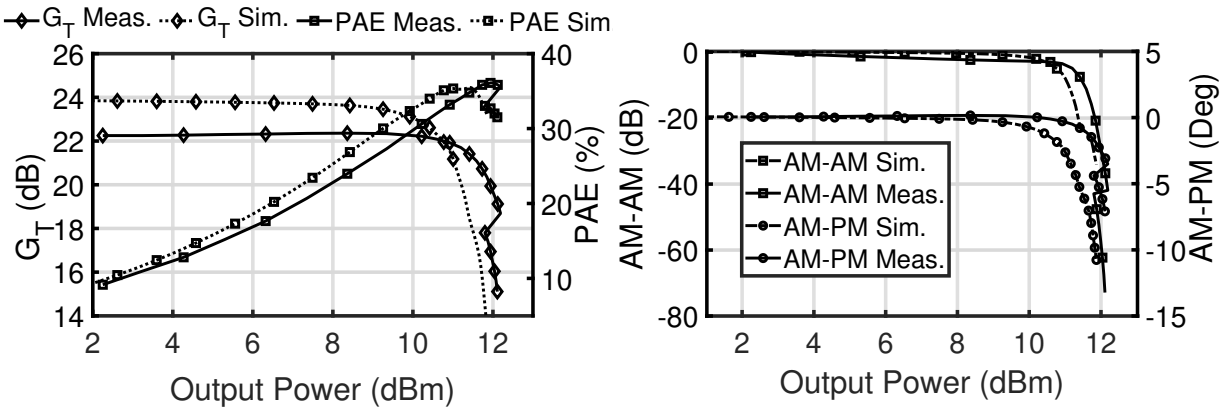


Figure 2.15: Comparison of simulation (solid line) and measurement (dashed line) results for small signal μ stability factor.

than -9 dB in the desired band.

The RTPS block provides more than 220° phase shift, as shown in Fig. 2.17(c). The RTPS shows ± 1.5 dB ILV as illustrated in Fig. 2.17(d), which is almost identical to the RTPS block measurement. Fig. 2.18 shows the measured phase and amplitude states of



(a) (b)

Figure 2.16: Comparison of simulation and measurement results for implemented PA at 28 GHz: (a) PAE and transducer gain, (b) AM-AM and AM-PM distortion.

the chip at 28 and 30 GHz. The two analog control voltages of this chip are varied together for this measurement. It can be seen that there is no blind region in our amplitude-phase coverage.

2.4.2 Large Signal Measurements

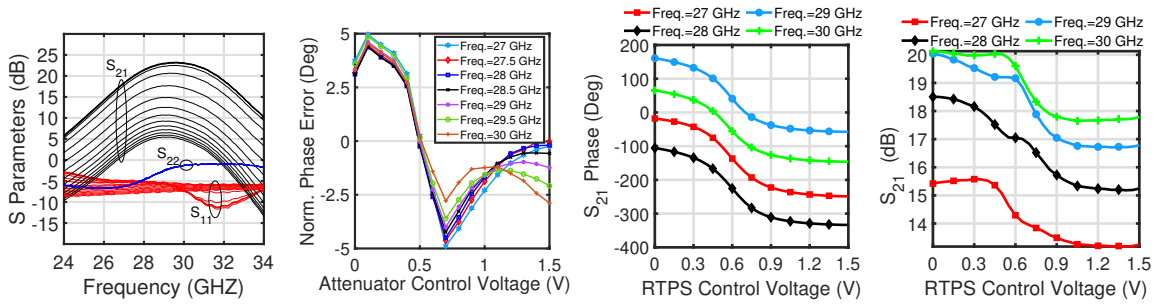
Single-tone and modulated signals were used to characterize the large-signal performance of the fabricated chip. Fig. 2.21 shows the experimental results for the large-signal performance of the fabricated die at 30 GHz. The PA has a P_{1dB} of above 10.8 dBm over the operating bandwidth of 27 to 30 GHz. The break in VCC=1.8 V lines in Fig. 2.21 (a) and (c) is due to the breakdown of the collector-base junction of the PA RF transistor as described in Section 2.3.

The large signal parameters are provided in Fig. 2.21 for various VCC supply voltage levels. Changing the supply voltage level from 1.4 V to 1.8 V results in a 25 % improvement in the power consumption at 6 dB back-off, as shown in 2.21(a). This is very beneficial for large phased-arrays used in SATCOM since a large number of elements are operating at deep back-off. Fig 2.21(c) and (d) show the effect of changing VCC on phase and gain response versus output power. The variation in VCC introduces less than 1 dB gain variation and less than 5° phase error which can be calibrated out.

The chip is tested using a 300 MS/s 64-QAM signal with the roll-off factor of 0.35

Table 2.2: Summary of PA Large Signal Performance

Frequency (GHz)	27	28	29	30	31
P_{sat} (dBm)	11.7	12	12	11.5	11.6
OP_{1dB} (dBm)	10.2	11.5	11.2	10.9	11.1
Peak PAE (%)	33	36	35	34	34.5
PAE 1 dB (%)	31	34	34	33.2	33
PAE 6 dB backoff (%)	16	16.5	16.7	15.6	17



(a) (b) (c) (d)

Figure 2.17: Small signal measurement results: (a) gain variation and input matching, (b) normalized phase error over gain control, (c) RTPS phase shift with control voltage, and (d) gain variation versus phase shift.

generated by Keysight M8190 arbitrary waveform generator and up-converted to 30 GHz by Keysight E8267D signal generator. The error vector magnitude (EVM) is measured using Keysight VSA 89600 software installed on N9041B Keysight signal analyzer. The signal analyzer has a built-in channel equalizer to estimate the channel response. The measured error vector magnitude (EVM) is better than -29 dB for average output power of 5.7 dBm at 30 GHz and 31 mW DC power consumption. VCC was set to 1.8 V in the EVM measurements. The measured average efficiency is 12% for this EVM level. Fig. 2.22 shows the demodulated 64-QAM constellation and the measured Adjacent Channel Leakage Ratio of 31 dB.

TABLE 2.3
PERFORMANCE COMPARISON OF PROPOSED PA TO SI-BASED LINEAR PAS IN THE LITERATURE

	This work	[61]	[9]	[74]
Frequency (GHz)	30	30	28	28
P_{sat} BW (GHz)	27-31	27-31	27-29	26-32
P_{sat} (dBm)	12	14	18.6	15.6
OP_{1dB} (dBm)	11.5	13.2	15.5	14
G_T (dB)	22.5	15.7	15.3	15.8
Peak PAE (%)	35.6	35.5	35.3	41
PAE_{1dB}(%)	34	34.3	31.5	34.7
PAE @ $P_{sat} - 6$ dB	16.5	17.5	11.5	16
EVM (dB)	-29 64-QAM	-25 64-QAM OFDM	-	-26.4
PAE @ EVM (%)	16.1	9	-	18.2
P_{out} @ EVM (dBm)	6.4	4.2	-	9.8
Technology	130nm SiGe	28nm CMOS	130nm SiGe	65nm CMOS
Topology	2-Stg Class-AB	2 Stg. Class AB, DB*	1 Stg.Cont. Class-AB	2-Stg. Cont. Class-F
Core Size mm^2	0.3	0.16	0.27	0.24

* DB = Differential structure with output Balun.

TABLE 2.4
PERFORMANCE COMPARISON OF THIS CHIP WITH REPORTED PHASED-ARRAY CHIPS

Ref.	Technology	Number of Channels	Freq. (GHz)	P_{1dB}/P_{Sat} (dBm)	Gain(dB)	$P_{DC}/Ch.$ (mW)	PAE at P_{1dB}(%)	Gain Control (dB)	Phase Resolution
This work.	130nm SiGe	1-TX	27-30	10.8 / 12	23	45	26.7	16	continuous
[47][1]	-	8-TX	27.5-31	8 / -	20[4]	-	-	32×0.5	6 bits
[46][2]	-	8-TX	27.5-30	12 / -	22[4]	112.4	14	15.5	5 bits
[48][2]	-	8-TX	27-31	13 / -	25[4]	200	10	35	6 bits
[45]	250nm SiGe	4TX-2RX	29.5-30.8	4.19 / -	9.47	85	3	8	8 bits
[83][3]	40nm CMOS	1-TRX	27-30	14.6 / 15	12.4	137	21	9×1	3 bits
[3][3]	130nm SiGe	32-TRX	27.2-28.7	13.6 / 16	30	143.8	15.9	8×1	5 bits
[86][3]	180nm SiGe	4-TRX	28-32	11 / 13	19	220	5.7	20	6 bits
[4][3]	28nm CMOS	24-TRX	26.5-29.5	12 / 14	44	122	13	8×1	3 bits
[87][3]	45nm SOI	1-TRX	24-30	8 / 13	16.5	100	6	16×0.5	6 bits

[1] WLCSP package. [2] QFN package. [3] Includes TX/RX switch loss.
[4] Includes splitting loss.

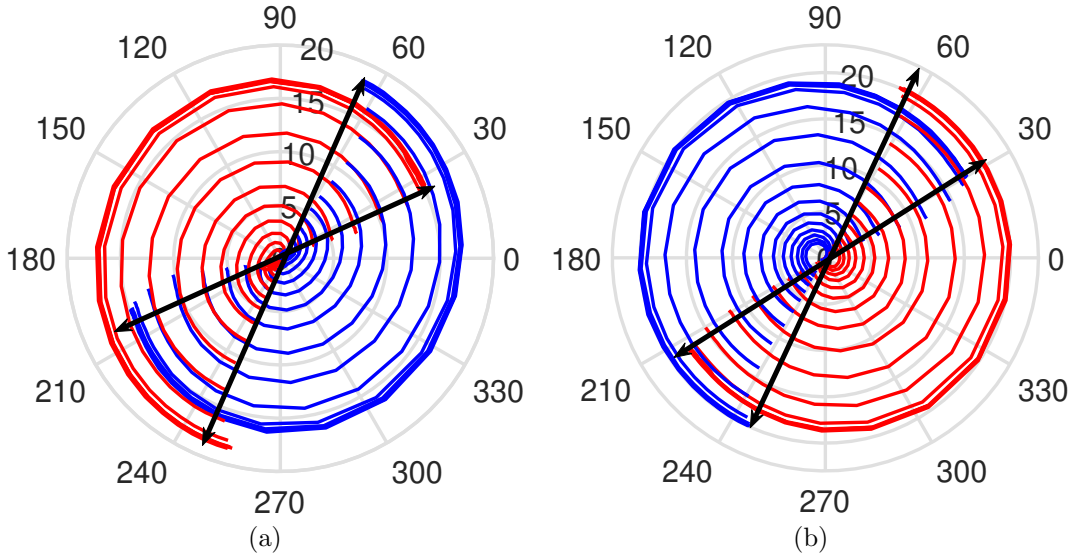


Figure 2.18: Measured S_{21} in polar coordinate system at (a) 28 GHz and (b) 30 GHz. The attenuator and RTPS control voltages are independently varied.

2.4.3 Performance Comparison

Table 2.4 compares the performance of this work with the latest reported transmitter solutions for 5G and SATCOM. There are very few academic reports [45] on Ka-band SATCOM so the work must be compared with commercially-packaged SATCOM beamformer chips [46–48]. Therefore, to make a fair comparison, a package loss of about 1-2 dB should be considered for these chips. Considering this loss, the total efficiency of our front-end at OP_{1dB} outperforms the SATCOM chips in [46], [47] and [48]. In addition, 28 GHz 5G transceiver chips are also included in Table 2.4. On-die measurements for 5G chips have been reported [3, 4, 83, 86] but the T/R switch loss (about 1 dB) at the output of this chips should be de-embedded for a fair comparison. Considering 1 dB loss for this switch, the T/R in [86] has similar output power compared to our work but with much higher DC power consumption. Furthermore, the proposed front-end's PAE is comparable with that reported for the chip in [83]. That chip has the highest reported efficiency among 5G chips. Finally, the gain achieved for the proposed device is 10 dB higher than [83] with lower DC power consumption. Our continuous phase shifter allows for control of the phase with high resolution.

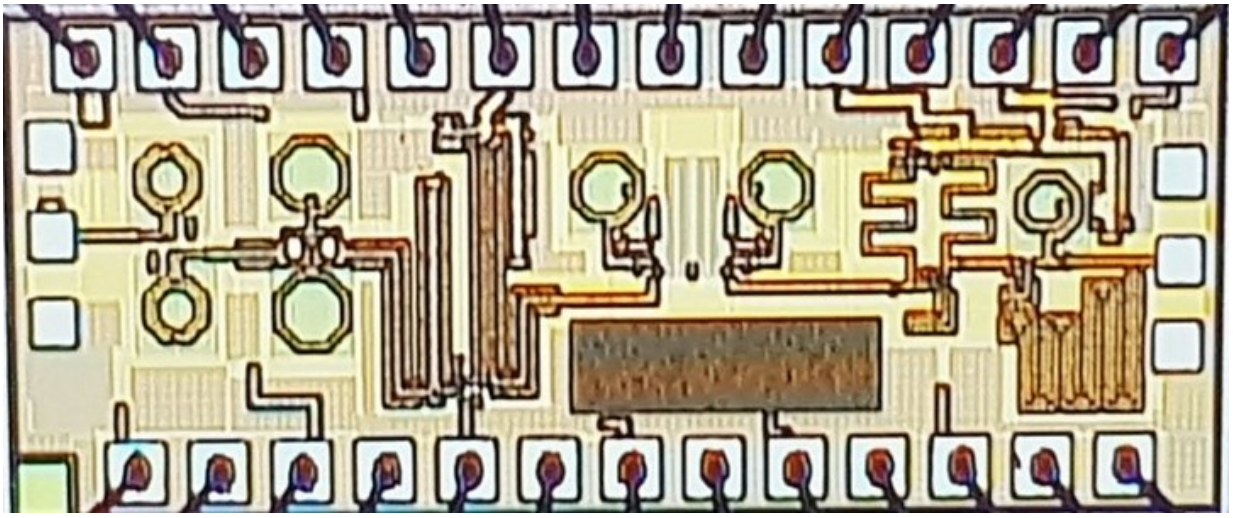


Figure 2.19: Micro-graph of implemented transmit-channel.

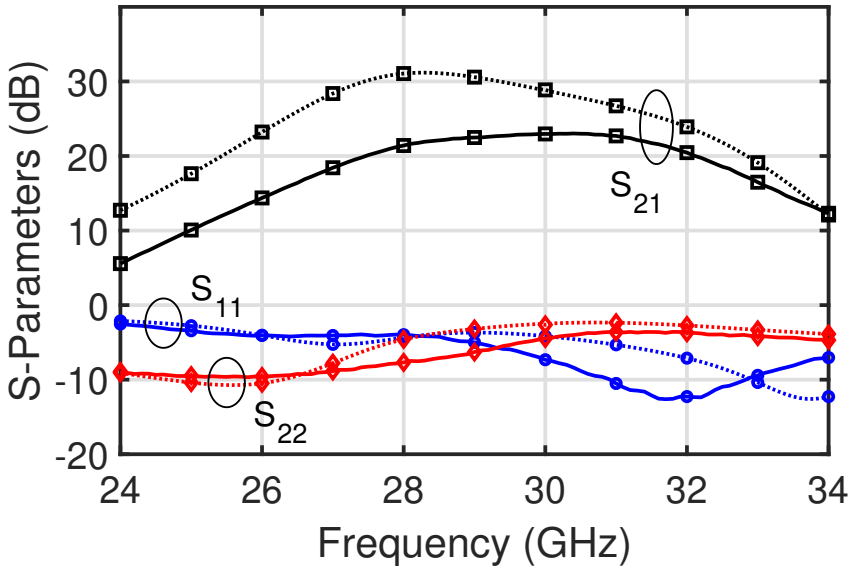
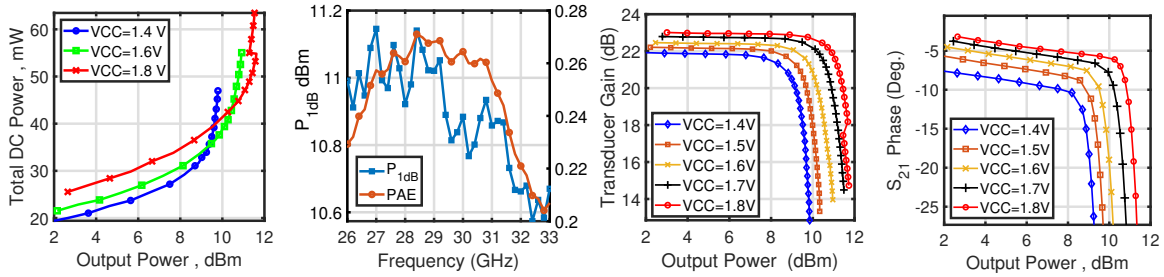
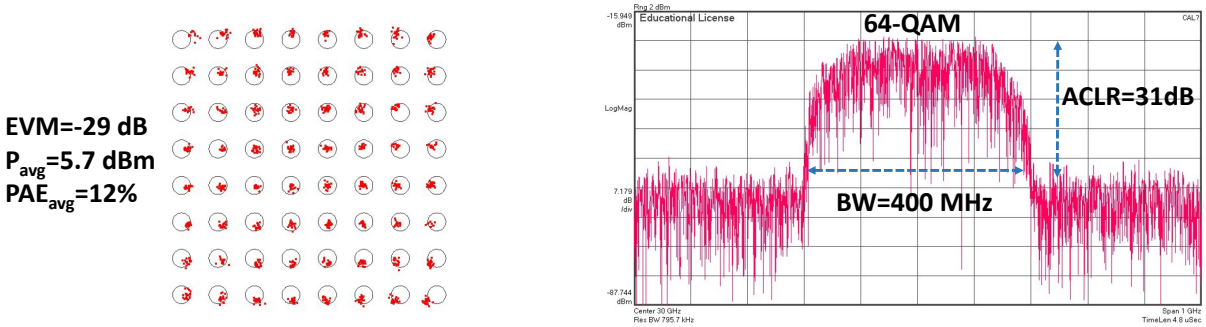


Figure 2.20: Comparison of simulation (solid line) and measurement (dotted line) results for small signal S-parameters of transmitter channel.



(a) (b) (c) (d)

Figure 2.21: Large signal measurement results: (a) measured total DC power consumption at 30 GHz over various VCC, (b) output P_{1dB} over frequency, (c) transducer gain compression with output power at different VCC at 30 GHz, and (d) phase variation with output power and VCC at 30 GHz.



(a) (b)

Figure 2.22: Modulated signal measurement results. (a) Measured constellation and (b) spectrum of a 300 MS/s 64-QAM signal at an average output power of 5.7 dBm for DC power consumption of 31 mW.

2.5 Conclusion

This chapter presented an integrated BiCMOS Ka-band RF front-end for SATCOM phased-array transmitter user terminals. Passive phase shifters and attenuators are used to achieve a 400° phase shift and 16 dB amplitude control. OP_{1dB} of higher than 10.8 dBm is measured from 26 to 30 GHz. The PA, gain, phase shifter, and variable attenuator blocks were separately simulated and verified by measurements. This work achieved the highest PAE (26.7

%) among the reported SATCOM phased-array chips by using passive beam-forming and employing a high-efficiency PA and fixed gain stage. The continuous phase control facilitates array calibration for stringent SATCOM polarization purity, SLL, and beam pointing accuracy. For a 400 MHz 64-QAM modulated signal, the TX-channel average efficiency of 12 % is measured at $P_{out,avg}$ of 5.7 dBm. This will facilitate the implementation of large phased-arrays with affordable power consumption for mobile SATCOM applications.

The main contributions of this work are as follows:

1- This work achieved the highest efficiency among the reported SATCOM chips. This is mainly due to its passive amplitude and phase control architecture and the design of a high-efficiency PA.

2- The architecture is designed for easy control of both the amplitude and phase of the RF signal. One analog control voltage is required for control of either amplitude or phase. This significantly reduces the complexity of the calibration routine in large phased-array antennas. Furthermore, the architecture is designed for orthogonal amplitude and phase control. By properly designing the proposed architecture, an amplitude error of less than 1 dB and a phase error of less than 5° can be realized.

3- The good agreement between simulations and measurement results shows the validity of the design flow.

4- This work is the RF-core of an eight-channel SATCOM phased-array transmitter. Our ability to design the phased-array chip and the antenna element together can result in more freedom and less constraint in designing an active phased-array system.

Chapter 3

A Broadband High-Efficiency Continuous Class-AB Power Amplifier for Millimeter-Wave 5G and SATCOM Phased-Array Transmitters[1]

3.1 Introduction

In this chapter, a single-ended continuous class-AB PA with broadband peak-efficiency and compact layout is introduced to address the aforementioned challenges. A non-inverting transformer is used as the output matching network of the PA. The output matching is optimized to achieve high efficiency at 28 and 38 GHz bands. Section 3.2 describes the proposed transformer based PA architecture. Load-pull analysis and design of broadband output matching are presented in Section 3.3. Experimental results and comparisons of measurements and simulations are provided in Section 3.4.

[1]The results presented in this chapter are published in the paper: S. R. Boroujeni, A. Basaligheh, S. Ituah, M. Nezhad-Ahmadi and S. Safavi-Naeini, "A Broadband High-Efficiency Continuous Class-AB Power Amplifier for Millimeter-Wave 5G and SATCOM Phased-Array Transmitters," in IEEE Transactions on Microwave Theory and Techniques, vol. 68, no. 7, pp. 3159-3171, July 2020, doi: 10.1109/TMTT.2020.2983703.

3.2 Proposed PA Architecture

Figure 3.1(a) shows the circuit diagram of the proposed PA and Fig. 3.1(b) shows the 3D layout. The amplifier core is a single-ended cascode topology in Global-Foundries 0.13μm BiCMOS SiGe-8XP technology, with f_T/f_{max} of 250/340 GHz. Fig. 3.1(c) shows the metal layers and substrate parameters. A 1:1 non-inverting transformer provides the supply and acts as the output matching for the transistor. C_{12} is a first order equivalent model of the distributed inter-turn capacitance of the transformer.

3.2.1 System Level Analysis

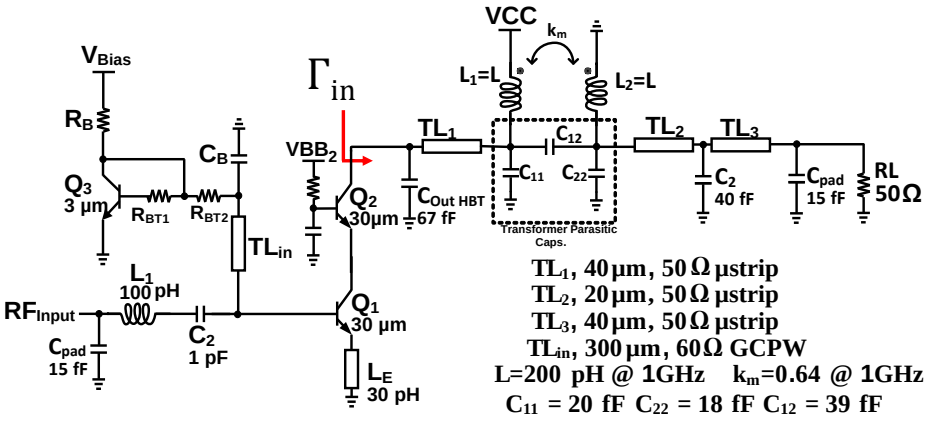
One of the emerging applications of mm-wave silicon-based phased-array is the Ka-band satellite user terminals for fixed or mobile SATCOM [2, 88]. In this application, a large and bulky dish antenna is replaced with an active phased-array. The phased-array antenna has thousands of elements whose amplitudes and phases need to be accurately controlled by phased-array front-end ICs. For example, a Ka-band phased-array with 64×64 antenna elements requires 1024 beam-former MMICs, where each MMIC feeds a 2×2 dual-feed antenna array element [8]. The phased-array antenna for GEO satellites needs to generate 48 dBW EIRP. In order to generate this power at boresight ($\theta = 0^\circ$), the average radiated power of each antenna element is given by [82]

$$\begin{aligned} P_T\ (\text{dBm}) &= EIRP\ \text{dBm} - G_T\ (\text{dB}) - 20\log N + TF \\ &= 78\ \text{dBm} - 6\ \text{dB} - 20\log(64\times 64)\ \text{dB} + 6.3\ \text{dB} \\ &= 6.05\ \text{dBm}. \end{aligned} \tag{3.1}$$

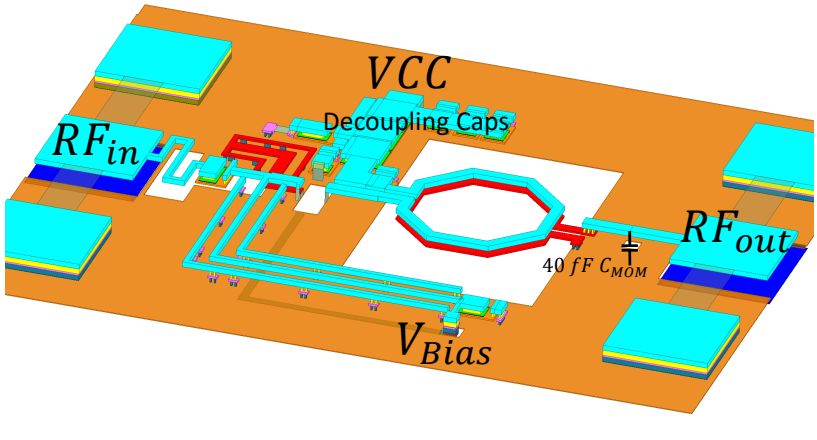
Where G_T is the gain of the antenna element, N is the total number of elements, and TF is the effect of amplitude tapering to achieve -30 dB side lobe level for a 2D Taylor tapering [82]. Considering a QPSK signal with 4 dB peak to average power ratio and 1 dB feed loss, the PA needs to deliver 11.05 dBm of linear power. Therefore, a peak output power of 13 dBm is targeted to generate 11 dBm linear power and to allow for design margin. This PA is mainly developed for Ka-Band SATCOM active phased array application with the purpose of delivering 11 dBm linear power from 27-30 GHz.

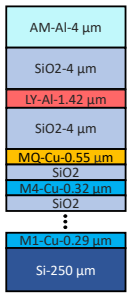
3.2.2 Circuit Model of Non-Inverting Transformers

In a transformer, the electric and magnetic coupling between the turns transfers power. These coupling mechanisms can cancel or add together in the transmission band. In a



(a)





(b) (c)

Figure 3.1: (a) Schematic of proposed transformer-based PA. (b) 3D layout in HFSS. (c) cross section of 0.13 μm Bi-CMOS SiGe-8XP back end of lines metal stack-up.

non-inverting transformer, they cancel each other at a specific frequency and this results in a notch in the transmission band [75]. As an example, Fig. 3.2(a) shows the full-wave frequency response of a non-inverting 1:1 transformer. The non-inverting transformer has a narrow-band transmission notch and two wide pass-bands. The transformer loss is defined as G_{max} in Fig. 3.2(a) which is the loss of transformer for conjugate input and output matching. The G_{max} at the first pass-band (20 GHz to 50 GHz) is -0.6 to -0.7 dB and -0.3 dB at the second pass-band (70 GHz to 90 GHz). Fig. 3.3(a) and (b) show the output matching and its simplified circuit model respectively. C_{22}, C_2, and C_{pad} are lumped into C_{out} and C_{11}, TL_1 and $C_{out,HBT}$ are lumped into C_{in}. The transmission lines were neglected in this analysis due to their very short electrical length. A π equivalent model with the following parameters is used for the transformer in Fig. 3.3(b)

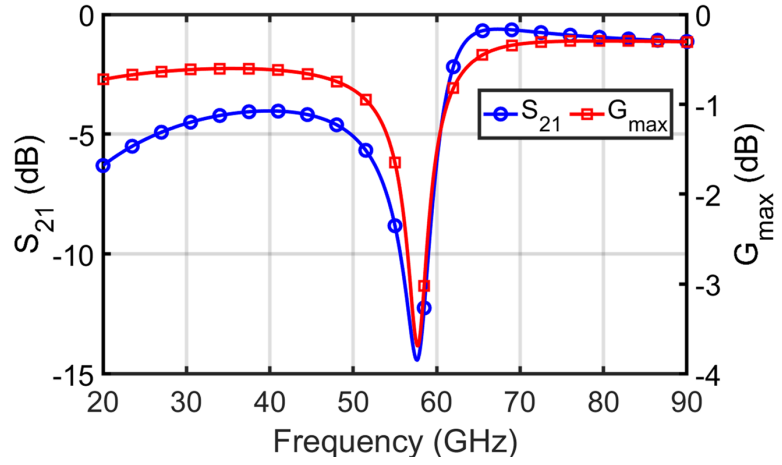
$$\begin{aligned} L_{11} &= (1+k_m)L \\ L_{22} &= (1+k_m)L \\ L_{12} &= \frac{1-k_m^2}{k_m}L \end{aligned} \tag{3.2}$$

where k_m is the magnetic coupling coefficient between the turns and L is the self-inductance of the primary and secondary turns. We have assumed equal self-inductance for the primary and secondary turns to simplify the analysis.

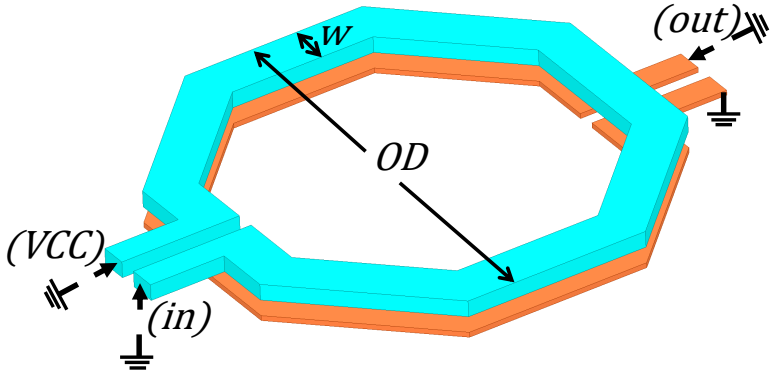
Figure 3.3(c) shows the impedance transformation of a 50 Ω load through the transformer and its associated parasitic capacitances at the fundamental-harmonic. The resonant frequency of $L_{11}-C_{in}$ and $L_{22}-C_{out}$ tanks is considered to be above the fundamental-harmonic frequency. Low C_{in} and high C_{in} values map the 50 Ω load into $\Re Z_{in} < 50$ Ω and $\Re Z_{in} > 50$ Ω regions respectively. The value of C_{in} is determined mainly by the output power level and size of the transistor. The parallel LC tank formed by L_{12} and C_{12} is the power transmission path from input to output. A second-harmonic trap can be created by setting the resonance frequency of this tank at the second-harmonic

$$2\omega_0 = \frac{1}{L_{12}C_{12}}. \tag{3.3}$$

This tank isolates the input and output at the second-harmonic by providing a high impedance in the power transmission path. The desired impedance at second-harmonic can be obtained by properly setting L_{11} and C_{in} as indicated in Fig. 3.3(d)



(a)



(b)

Figure 3.2: (a) Frequency response of a 1:1 non-inverting transformer with OD=140 μm and w=8 μm. (b) The non-inverting transformer model in HFSS and the design parameters, AM and LY layers are used for the transformer. The ground is shown in Fig. 3.1(b) and it is omitted here for clarity.

$$\begin{aligned} Z_{2nd} &= j2\omega_0 L_{11} \parallel \frac{1}{j2\omega_0 C_{in}} \parallel Z_{tank} \\ &\approx j2\omega_0 L_{11} \parallel \frac{1}{j2\omega_0 (C_{11} + C_{out,HBT})} \end{aligned} \tag{3.4}$$

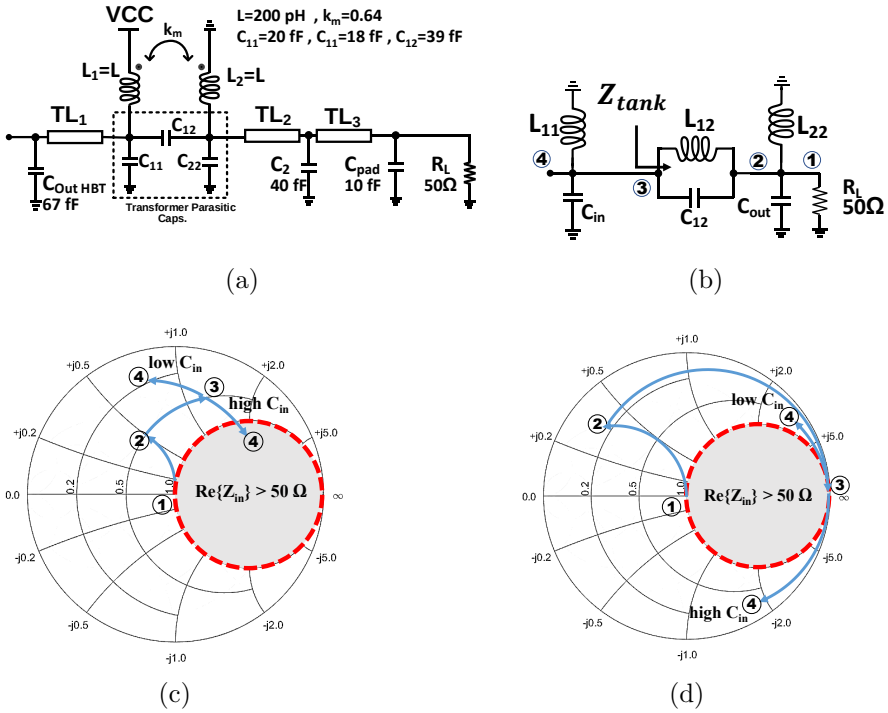


Figure 3.3: (a) Output matching with π equivalent circuit of the transformer at fundamental-harmonic. (b) Simplified model of output matching. (c) Impedance transformation at fundamental-harmonic. (d) Impedance transformation at second-harmonic.

where Z_{tank} is defined in Fig. 3.3(b).

In order to validate the simplified circuit model, a 1:1 non-inverting transformer is simulated with ANSYS-HFSS and the parameters of the model in Fig. 3.3(b) are extracted from the full-wave solution. Fig. 3.4 compares the response of this circuit model with the full-wave solution. The circuit model predicts the transmission zero at the second-harmonic but fails to follow the input impedance trajectory of the full-wave solution above the transmission zero frequency. As the length of the turns become closer to a quarter of a wavelength, the lumped element model is no longer valid. The coupling between the primary and secondary increases significantly after the notch frequency, and a low-loss transmission response is observed in the full-wave solution in Fig. 3.4. According to EM simulation results, a 1:1 non-inverting transformer has one narrow stop-band and two wide pass-bands as illustrated in Fig. 3.2(a). In the pass-bands the G_{max} of transformer is better than -1 dB. In the second pass-band, the optimum load impedance is close to 50 Ω and S_{21}

and G_{max} are approximately the same. However, at the first pass-band, the transformer needs a certain load impedance at the input and output to achieve an insertion loss close to G_{max}. Fig. 3.3(a) shows our matching circuit for this purpose.

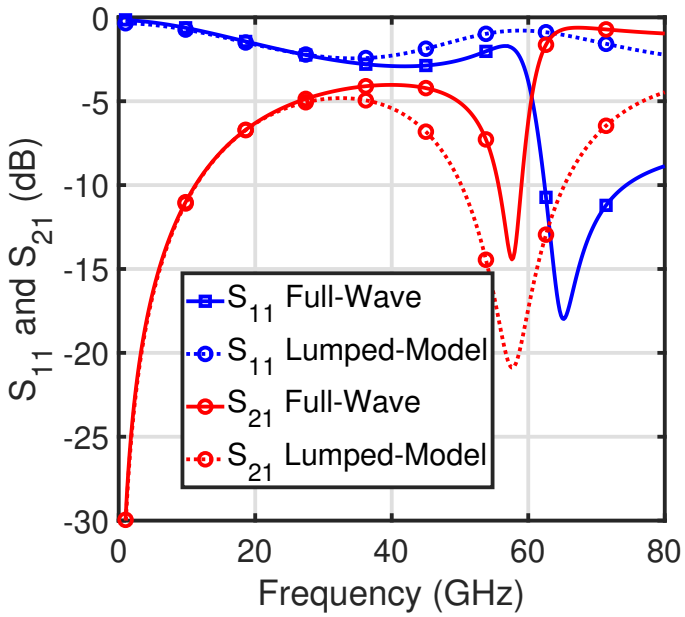


Figure 3.4: Comparison of the lumped-element circuit model and full-wave HFSS model for a non-inverting 1:1 transformer.

3.2.3 Transformer Design for Class F^{-1} and Continuous Class-AB

A non-inverting transformer with a notch in its frequency response can be employed as a filter in harmonic tuned PAs. As discussed in the previous section, the $L_{12} - C_{12}$ parallel tank can be designed to resonate at the second-harmonic, leading to a reactive impedance at the collector node.

Output Matching Design for Class F^{-1} PA

Assuming $L_{12} - C_{12}$ resonates at the second-harmonic, the impedance at the collector node is given by (3.4). By setting C_1 and L_1 to resonate at the second-harmonic, we can create

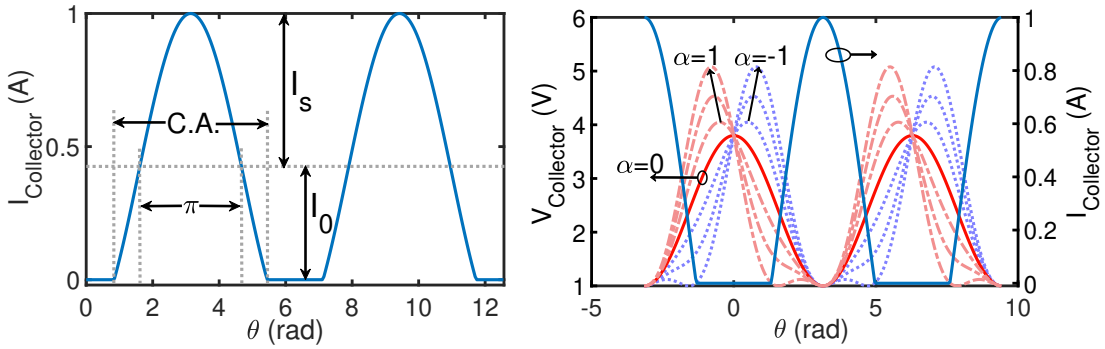


Figure 3.5: Continuous class-AB ideal voltage and normalized current waveforms. (a) Ideal class-AB collector current waveform. I_s and I_0 define the parameters in (3.6) and C.A. stands for conduction angle. (b) Collector voltage for continuous class-AB PA for different α values. The collector voltage is calculated according to (3.8) with VCC=2.4 V and V_k=1 V and $\theta = \omega_0 t$.

an open circuit at the collector node. These two tanks present an inductive impedance with $\Re Z_{in} < 50\ \Omega$ at the fundamental-harmonic as shown in Fig. 3.3(c). This mode is most suitable for the PAs with small R_{opt} and narrow bandwidth.

Output Matching Design for Continuous Class-AB PA

Designing the proposed output matching for class F^{-1} mode puts some limitations on the output power and bandwidth of the amplifier. By designing the parallel tank of $L_{11}-C_{in}$ to have a finite reactive impedance, we can overcome the limitations of power and bandwidth in class F^{-1} mode. In continuous class-AB PAs, the optimum impedance at each harmonic is given by [89]

$$\begin{aligned} Z_1 &= R_{opt} + j\alpha R_{opt} \\ Z_2 &= -j\frac{3\pi}{8}\alpha R_{opt} \\ Z_{n\geqslant 3} &= 0 \\ -1 \leqslant &\alpha \leqslant 1 \end{aligned} \tag{3.5}$$

where R_{opt} is given by

$$\begin{aligned} R_{opt} &= \frac{2P_{out}}{{I_s}^2}\frac{1}{\left(1-\frac{\theta_0}{\pi}+\frac{\sin 2\theta_0}{2\pi}\right)^2} \\ \theta_0 &= \arccos\frac{I_0}{I_s} = \pi - \frac{C.A.}{2}. \end{aligned} \tag{3.6}$$

The I_s, I_0 and, C.A. (conduction angle) are defined in Fig. 3.5(a). The collector current is defined by

$$I_C(t) = \begin{cases} I_0 - I_s\cos\omega_0 t & \cos\omega_0 t \leqslant \frac{I_0}{I_S} \\ 0 & \cos\omega_0 t > \frac{I_0}{I_S}. \end{cases} \tag{3.7}$$

In the proposed output matching, the fundamental-harmonic is usually inductive and the second-harmonic is capacitive as illustrated in Fig. 3.3(c) and (d). According to our parametric study, for all the possible 1:1 transformer dimensions that have a notch at 56 GHz, a 65 fF transistor output capacitance results in a capacitive impedance at the collector node. Therefore, $0 \leqslant \alpha \leqslant 1$ in the continuous class-AB design space should be selected according to (3.5). The collector voltage is given by [89]

$$V_C = V_k + (VCC - V_k)(1-\cos\omega_0 t)(1+\alpha\sin\omega_0 t). \tag{3.8}$$

In (3.8), the minimum collector voltage is V_k and the maximum collector voltage varies by α. Fig. 3.5(b) illustrates how the collector voltage changes with α for V_k=1 V and VCC=2.4 V. For $0 \leqslant \alpha \leqslant 1$, V_C is an increasing function of α. Therefore, the maximum collector voltage happens at $\alpha = 1$ and is given by

$$\begin{aligned} V_{C,max} &= V_k + (VCC - V_k)\left(1+\frac{1}{\sqrt{2}}\right)^2 \\ &\approx V_k + 2.91(VCC - V_k). \end{aligned} \tag{3.9}$$

The breakdown voltage for HBT transistors in the cascode structure is determined by the BV_{CBO} parameter which has a nominal value of 5.8 V in 0.13 μm SiGe-8XP technology [90]. For VBB_2=1.6 V, the maximum allowed collector voltage in this technology is 7.4 V. In our design, the $\alpha = 1$ and the maximum collector voltage can be calculated from (3.9). For VCC=2.4 V and V_k=1 V the $V_{C,max}$ =5.07 V. Therefore, we have 2.33 V margin to the breakdown region.

3.3 Load-Pull Analysis and Output Matching Design For Broadband Operation

In order to design the proposed output matching network to operate at 28 and 38 GHz, we first load-pull the transistor at both of these bands. By finding the optimum impedances, we design the output matching to achieve high efficiency over a wide bandwidth.

3.3.1 Transistor Load-Pull for Continuous Class-AB

According to the analysis in Section 3.2, the targeted output power for this PA is 13 dBm. Assuming a realistic output matching loss of 1 dB, the transistor should deliver at least 14 dBm. A cascode transistor structure is chosen for its higher gain and better stability as shown in Fig. 3.1(a). Additionally, cascode structures can operate at higher collector voltages compared to common-emitter transistors due to the AC short circuit that exists at the base of the top transistor [91]. The supply voltage is set to 2.4 V and the bias voltage for base of Q_2 is 1.6 V. These values do not result in transistor breakdown as explained in Section 3.2-C. The transistor is biased at the current density of 0.2 $mA/\mu m$ for a flat 13 dB gain and minimum AM/AM distortion. The HBT transistor emitter length is 3×10 μm in 0.13 μm SiGe-8XP technology. The extracted transistor has 65 fF output capacitance ($C_{out,HBT}$ in Fig. 3.1(a)) found by Y-parameter extraction. The employed SiGe-8XP process offers seven metal layers with three top thick RF-layers (AM, LY, and MQ) and four routing layers (M_1 to M_4) shown in Fig. 3.1(c). Momentum EM-solver is used to characterize the inductance and capacitance of the transistor interconnects from M_1 to AM layer. Emitter degeneration is implemented by a 50 μm grounded CPW line which consists of MQ and LY layers. The inductive degeneration at the emitter has little effect on the effective output capacitance. It also increases the resistive part of the base input impedance and simplifies the input matching design. The base of Q_2 is AC-grounded by a 1 pF Metal-Insulator-Metal (MIM) capacitor to avoid instability.

The inductively degenerated transistor is load-pulled for the fundamental and second-harmonics. The higher harmonics are shorted due to their negligible effect on power added efficiency (PAE). The transistor output capacitance is de-embedded and considered as part of the output matching network.

Transistor Load-Pull at 28 GHz

By setting the maximum collector current to 60 mA and the quiescent current to 9 mA, the fundamental impedance for a classic class-AB design is given by (3.5) when α is zero. By setting I_s to 51 mA and I_0 to 9 mA (see Fig. 3.5(a)), the R_L will be 38.5 Ω for 14 dBm output power. Using this starting point, we swept the reactive part of the first and second-harmonics according to (3.5) as tabulated in Table 3.1. The PAE and output power increases by 6.2 % and 0.9 dB respectively as α varies from 0 to 1. This can not be predicted by the ideal analysis of continuous class-AB PA where the output power is constant with α. The variation of output power with α is due to transistor non-linearities. These non-linearities include variation of transistor output capacitance (Q_2, C_{bc}) with output power and the uncertainty in the true V_k in the preliminary calculations [9, 92]. As a result, we target the second-harmonic impedance to be –j45 Ω. However, a pure reactive impedance is not possible due to presence of loss in output matching. Considering $\Gamma_{2^{nd}} = 0.85$, we have 0.15 dB output power degradation as listed in Table 3.1.

For further optimization, we performed a load-pull for the fundamental impedance and set Z_2=-j45 Ω. Fig. 3.6 shows the final load-pull results for output power of 14 dBm at 28 GHz. The optimum impedance is 70+j40 Ω for the peak PAE of 44%. The operating mode of the PA for this impedance is similar to continuous class F^{-1} [11]. Despite its higher peak-efficiency, we preferred not to target this impedance to avoid narrow-band output matching and increase the efficiency of the PA at 38 GHz. We target the fundamental impedance of 40+j40 Ω which has a PAE of 40 % according to our load-pull analysis.

Transistor Load-Pull at 38 GHz

The transistor gain is lower at 38 GHz compared to 28 GHz. Therefore, the load-pull simulation was done for 13 dBm output power (1 dB lower compared to the 28 GHz band). As briefly discussed in Section 3.2, the second-harmonic of 38 GHz lies within the second pass-band of the transformer and the impedance at the second-harmonic of this band is not well controlled. However, it is mostly capacitive due to transistor output capacitance and parasitic capacitance of transformer. Therefore, we load-pulled only the fundamental-harmonic and terminated the second-harmonic by $\Gamma_{2^{nd}} = 0.4\angle\frac{3\pi}{2}rad$. We found this value by experimenting with the final output matching. Fig. 3.6 shows the load-pull contours for 38 GHz. The maximum PAE is 42% for a load impedance of 54+j23 Ω. However, we selected a load impedance of 71+j23 Ω which lies on the 40 % PAE contour. This will help in our output matching design for both 28 GHz and 38 GHz. Since Γ_{in} travels clock-wise

in the Smith-Chart with increasing the frequency, we chose the optimum load impedance at 28 and 38 GHz to align with the output matching impedance trajectory.

In order to further investigate the effect of loss in the second-harmonic, we swept the magnitude and phase of reflection coefficient at 76 GHz. Fig. 3.7 shows the result. The reflection coefficient at the second-harmonic is defined by

$$\Gamma_2^{nd} = \rho \exp\left(j\pi\gamma_{2nd}\right) \tag{3.10}$$

where ρ and $\pi\gamma_{2nd}$ are the magnitude and angle of reflection coefficient at second-harmonic. The peak-efficiency is degraded by 2 % by changing ρ from 1 to 0.4. The peak-efficiency occurs in the capacitive region of the Smith-Chart. Fig. 3.7(b) shows that even with the presence of loss in the second-harmonic, operating the PA in continuous class-AB is beneficial and results in 3.5 % higher PAE compared to class-AB where $\gamma_{2nd} = 1$. The same behaviour is observed for the effect of ρ on PAE and P_{out} at the second-harmonic of 28 GHz band.

3.3.2 Input and Output Matching Design

The output matching network is shown in Fig. 3.3(a). In order to design this output matching, we first performed a parametric study to find the transformer dimensions that create a notch at 56 GHz. The transformer is implemented with the two top thick layers (AM and LY) and the MQ layer is used as the ground plane as shown in Fig. 3.1(b). The main design parameters of the transformer are width (w) and output diameter (OD) as defined in Fig. 3.2(b). Fig. 3.8 shows the result. For a certain width, increasing OD results in higher inter-turn capacitance and higher mutual inductance and therefore the frequency of the notch decreases as shown in Fig. 3.8(a). Furthermore, for each output diameter, increasing the width results in higher inter-turn capacitance and decreases the frequency of the notch as shown in Fig. 3.8(b). The quality factor of transformer turns increases by increasing OD due to its higher inductance and this reduces the loss.

The transformer L_{11} and transistor output capacitance determine Γ_{in} according to (3.7). L_{11} should be large enough so that the second-harmonic of the collector current shunts through the transistor output capacitance.

Finding the transformer design-space for a notch at 56 GHz, we select the transformer dimensions, C_2 and TL_1 such that the load trajectory of Γ_{in} passes through the targeted impedances at 28 and 38 GHz as shown in Fig. 3.6. Fig. 3.9 shows the realized intrinsic collector impedance of the final output matching. The $\Im Z_{in}$ is almost constant over the

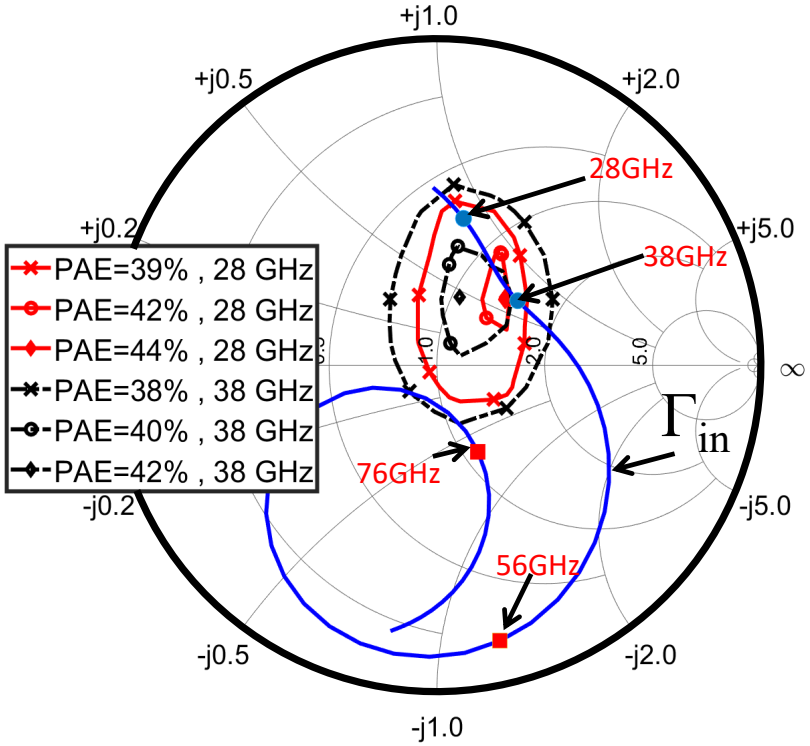


Figure 3.6: Constant output power Load-Pull contours. Red solid contours are for 14 dBm output power at 28 GHz. Black dashed contours are for 13 dBm output power at 38 GHz. Blue solid-line is impedance trajectory of the output matching network.

operating bandwidth and the $\Re Z_{in}$ increases with frequency. This explains the broadband high-PAE behaviour of the proposed output matching. The optimum load impedances at 28 and 38 GHz are selected based on this impedance response in an iterative selection of load-impedance and output matching component values.

The MIM cap available in our process had a Q-factor of 27 at 28 GHz, and 22 at 39 GHz. In order to lower the output matching loss, a high-Q Metal-Oxide-Metal (MOM) capacitor is formed by M_1 to M_4 layers to implement the 40 fF C_{out} as shown in Fig. 3.10(a). The bottom layer of the capacitor (M_1) is connected to ground (MQ layer) and the top layer is connected with an array of via to the top AM layer. Fig. 3.10(b) shows the simulated Q-factor and capacitance. The Q-factor is above 150 in the operating bandwidth.

Figure 3.11 compares the power gain of entire output matching with the stand alone transformer. The load of transformer is considered the same as in the output matching

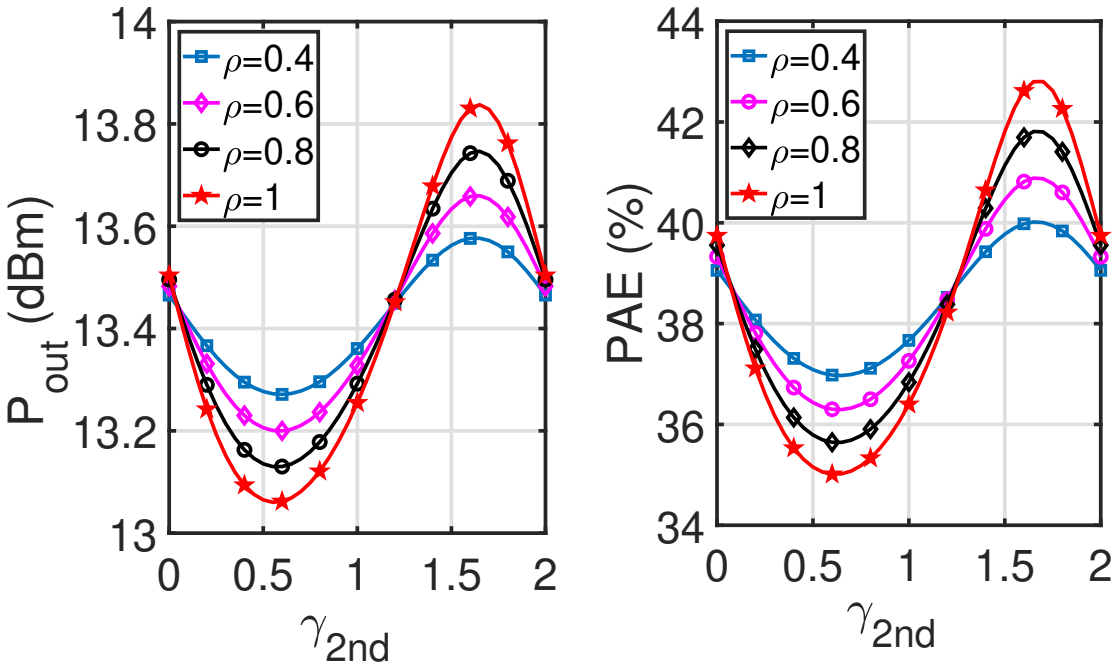


Figure 3.7: Effect of presence of loss on the second-harmonic termination at 38 GHz (a) P_{out} (b) PAE.

circuit however, the loss of $TL_{2,3}$, C_2 and C_{pad} is set to zero. The output matching has 0.9 dB and 1.2 dB loss at 28 and 38 GHz respectively. The excessive loss of 0.2-0.3 dB is due to the finite impedance of supply decoupling network and loss of other parts of circuit e.g. bond pad, MOM capacitor and transmission line. Fig. 3.2(a) shows the frequency response of the stand-alone implemented transformer. The transformer has a G_{max} of 0.65 dB at 28 GHz for the implemented dimensions of $OD = 140\ \mu m$ and $w = 8\ \mu m$.

The input matching consists of a shunt inductor implemented by transmission line and a series inductor. The inductor is implemented by a meandered line as shown in Fig. 3.1(b) to reduce the layout area. The simulated S_{11} of the amplifier is -14 dB at 28 GHz and -8 dB at 38 GHz. The proposed PA has a single-ended topology which is sensitive to modeling inaccuracies and the parasitic elements may change the frequency response. Therefore, we performed full-chip EM simulation of the layout in Fig. 3.1(b) and re-optimized our input and output matching circuits. We included the supply path and VCC decoupling caps in our EM simulation to capture the supply impedance and their de-tuning effects.

Table 3.1
Large Signal Load-Pull Results For Continuous Class-AB at 28 GHz Band

α	$Z_L@f_0$ (Ω)	Z_{2nd} (Ω)	G_T (dB)	OP_{1dB} (dBm)	PAE_{1dB} (%)
0	38.5	0	14.5	13.1	31
0.2	38.5+j7.7	-j9	14.6	13.4	32.3
0.4	38.5+j15.4	-j18	14.8	13.5	33.5
0.6	38.5+j23.1	-j27	14.9	13.6	33.9
0.8	38.5+j30.8	-j36	15	13.7	35.5
1	38.5+j38.5	-j45	15.1	14	37.2
1	38.5+j38.5	7-j45	15.1	13.85	36.5

Figure 3.12 shows the large signal simulation results of the chip at P_{1dB} and 6 dB back-off. PAE of larger than 30 % is obtained from 28 to 38 GHz at P_{1dB}. The simulated output power is 13 dBm at 28 GHz and 11.5 dBm at 38 GHz. The broadband response of the power amplifier is due to proper selection of the optimum load impedance at 28 GHz and 38 GHz.

3.3.3 Class of Operation

The realized fundamental-harmonic impedance is 40+j44 Ω at 28 GHz and 86+j38 Ω at 38 GHz. The imaginary part of the fundamental impedance is fairly constant. However, the real part of the impedance increases with frequency as shown in Fig. 3.9. This compensates the reduction of transistor gain and improves the gain flatness over frequency.

At the second-harmonic, the reflection coefficient is capacitive and its magnitude is higher than 0.7 from 52 GHz to 62 GHz. Therefore, from 26 to 31 GHz we can assume that the operating class of the PA is continuous class-AB with $\alpha > 0$. From 62 GHz to 76 GHz, the Γ_{in} trajectory gradually moves to the center of Smith-Chart which results in smaller reflection coefficient for the second-harmonic as illustrated in Fig. 3.6. However,

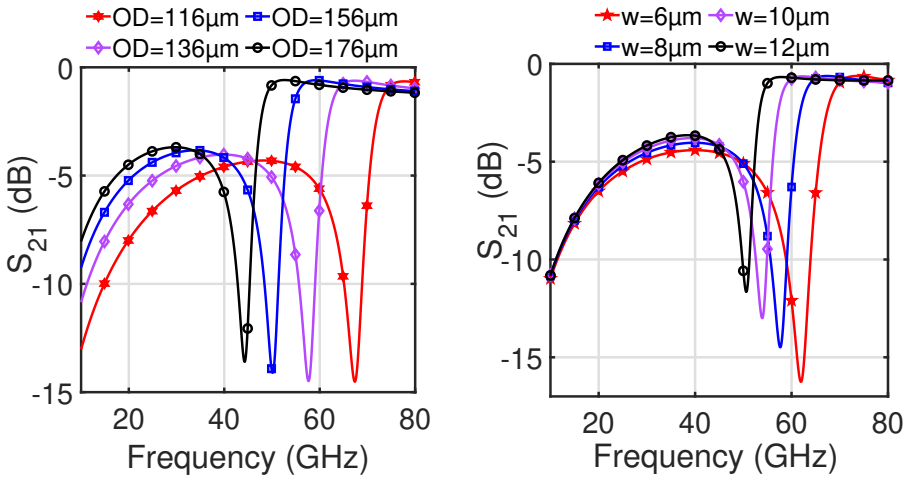


Figure 3.8: Frequency response of a 1:1 transformer. (a) varying OD, $w = 8\ \mu m$. (b) varying w, $OD = 136\ \mu m$.

as shown in Fig. 3.7(b), the efficiency is 4.5 % higher for this second-harmonic impedance compared to an ideal short circuit at 76 GHz. The operating class of the PA in this region cannot be fully described by (3.5) due to presence of significant resistive part at the second-harmonic. However, it can still be considered as an extension of continuous class-AB with resistive second-harmonic termination [72].

3.3.4 Effect of Carrier and Die Size

The transformer's electromagnetic fields are not shielded and interact with the substrate and the PCB carrier. In transformers, the currents in the primary and secondary turns flow in opposite directions in the transmission bands and this confines the magnetic field. Therefore, there is a small interaction with the carrier and the die and the performance of the amplifier at the fundamental-harmonic is not affected. However, at the second-harmonic (transformer stop-band), the second-harmonic trap stops the flow of current in secondary turn, so the transformer's magnetic fields are not confined and can interact with the substrate. If the chip is attached to the carrier by a conductive paste, it creates a parallel plate cavity, consisting of chip-ground, silicon, and the carrier. This cavity is another transmission path from the input to the output of the transformer and degrades the depth of the notch. To investigate this phenomena further, the layout in Fig. 3.1(b)

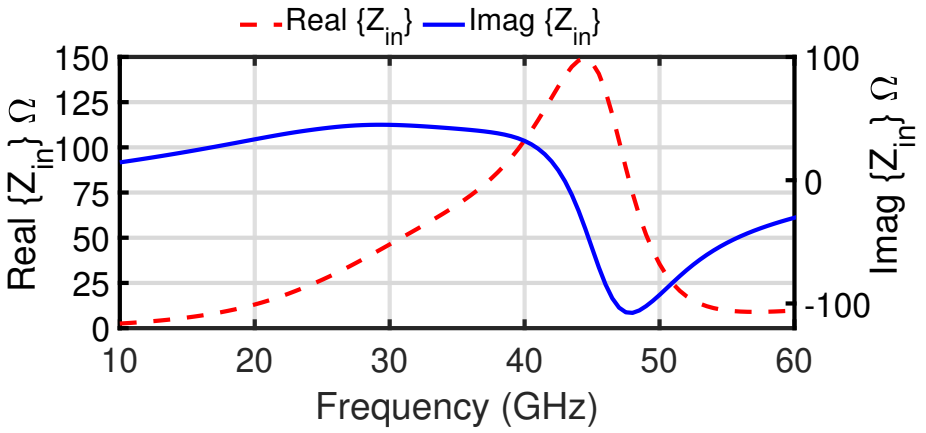


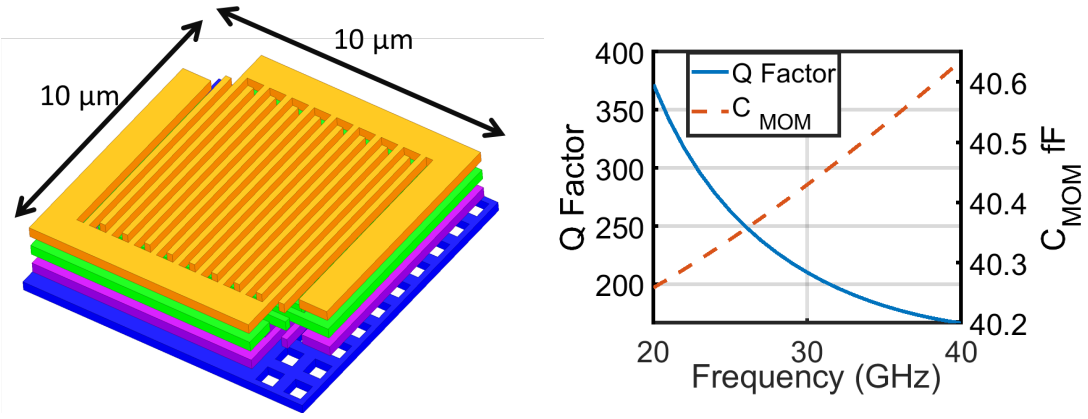
Figure 3.9: Realized intrinsic collector impedance for the proposed output matching.

is simulated using ANSYS-HFSS for substrate sizes of 500 μm ×500 μm (our design) and 2 mm by 2 mm (our fabricated die size). Both dies were simulated with and without a conductive paste at the silicon back (250 μm height). Fig. 3.13(a) shows the result. The fundamental-harmonic response is the same for all cases as expected. The presence of conductive paste and size of the die have no effect on the transformer Q-factor and S_{21} of the PA as shown in Fig. 3.13(a). However, the depth of the notch is degraded by 4 dB with the presence of conductive paste in the 2 mm × 2 mm and 2 dB in 500 μm × 500 μm die. This clearly shows the effect of presence of a parallel-plate cavity. In our design, we had not considered a conductive plane at the bottom of silicon and we realized this issue during measurement of the fabricated samples. Our design was fabricated on a 2 mm × 2 mm die which was shared with other designs.

The interaction of chip with PCB has very little effect on the transformer loss and the output power performance of the chip. Fig. 3.13(b) shows the magnitude of reflection coefficient of the output matching for each case. The magnitude of reflection coefficient is degraded from 0.85 to 0.75 which degrades the efficiency by less than 0.5 % according to Fig. 3.7.

3.3.5 Effect of Process Variation

The resonant frequency of the non-inverting transformer that results in second-harmonic notch is a function of the inter-winding capacitance and inter-winding mutual inductance.



(a) (b)

Figure 3.10: (a) The 3D structure of implemented MOM capacitor. (b) simulated Q-factor and capacitance.

The inter-winding inductance is fairly stable as it depends on the geometrical dimensions of the transformer and are determined by lithography accuracy. The inter-winding capacitance is determined by the dimensions of transformer and SiO_2 dielectric thickness and permittivity. The inter layer dielectric thickness in a CMOS process is well controlled with a precision of better than 10 nm through chemical-mechanical polishing (CMP) and using Plasma Enhanced Chemical Vapor Deposition (PECVD). The permittivity of the SiO_2 is also controlled in the fabrication process. Therefore, the frequency response of the transformer is fairly stable due to process variation [93]. This way of implementing a second-harmonic notch filter is more stable over process variation as compared to LC tanks implemented by MIM caps [9] which have 10 % variation over process corners. Furthermore, Fig. 3.7 shows how the magnitude and angle of second-harmonic impedance affects the PA performance. A 10-20 % variation in ρ or γ_{2nd} results in less than 0.1 dB output power variation. Therefore, process variation has negligible effect on the performance of the proposed PA.

3.3.6 Output ESD Protection

In order to use the PA in an active-antenna application, the output of the PA should have ESD protection to avoid permanent damage during the packaging process. An effective and low-loss technique for ESD protection of the PA output is to have a DC short circuit

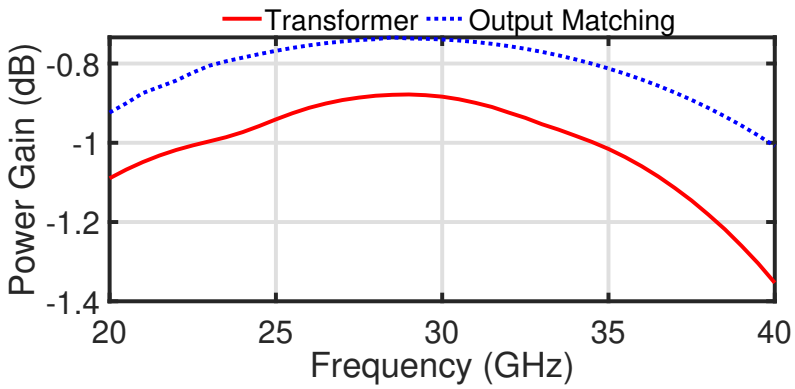
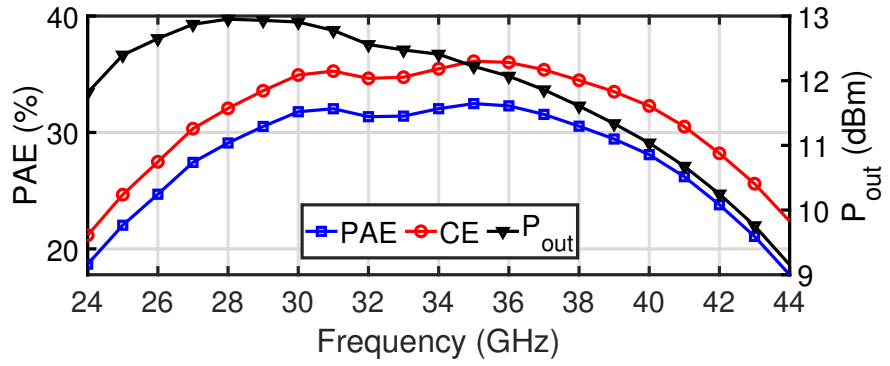


Figure 3.11: Comparison of transformer power gain with the whole output matching.

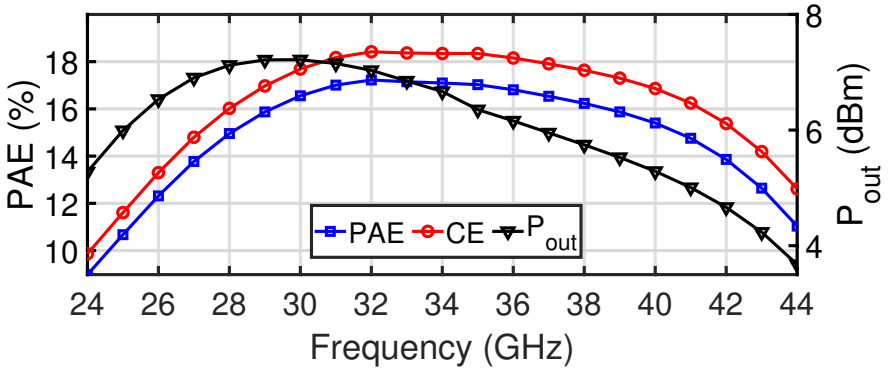
(open at RF) at the output. This can be realized by including either a quarter-wavelength line [3] or a shunt-inductor [94] in the output, at the expense of 0.2-0.4 dB higher loss. The addition of ESD network can limit the bandwidth and increase the layout area of the PA and its effect should be considered in the PA output matching design. In ESD circuits based on quarter-wavelength lines or tuned-LC tanks, the bandwidth is limited to around 10 %. In the proposed transformer-based output matching circuit, the secondary turn of the transformer is shunted to ground and operates as ESD protection. Therefore, the ESD network is part of the output matching circuit and does not limit the bandwidth or add extra loss and layout area to the circuit.

3.4 Experimental Results

Figure 3.14 shows the die micrograph. The layout area is 0.14 mm^2 excluding the pads. The measurement is performed using the Keysight 67 GHz 5227A PNA-X and 67 GHz on-wafer probes. The PNA is calibrated using the SOLT calibration routine. The die is attached on the PCB with silver epoxy. The bias pads are wire-bonded to a PCB and are decoupled to ground with 100 nF capacitor. Fig. 3.15 compares the measurement and simulation of the small signal S-parameters for the fabricated PA up to 67 GHz. The small signal measurements are done at VCC=2.4 V and a bias current of 7 mA. The transistor is biased with a 1 to 10 current mirror through Q_3,R_{bt1} and R_{bt2} to avoid thermal run-away. The base of Q_2 is decoupled with a 1 pF MIM capacitor and connects through a 1 $k\Omega$ resistor to a DC pad and the bias voltage is 1.6 V. There is good agreement between the



(a)

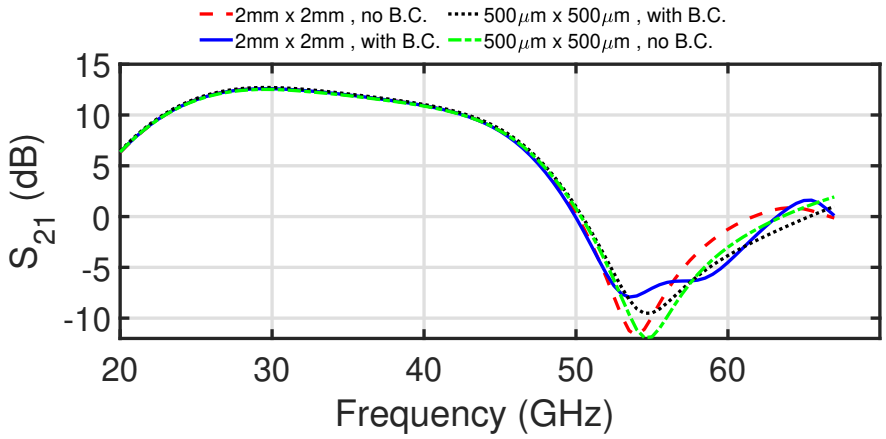


(b)

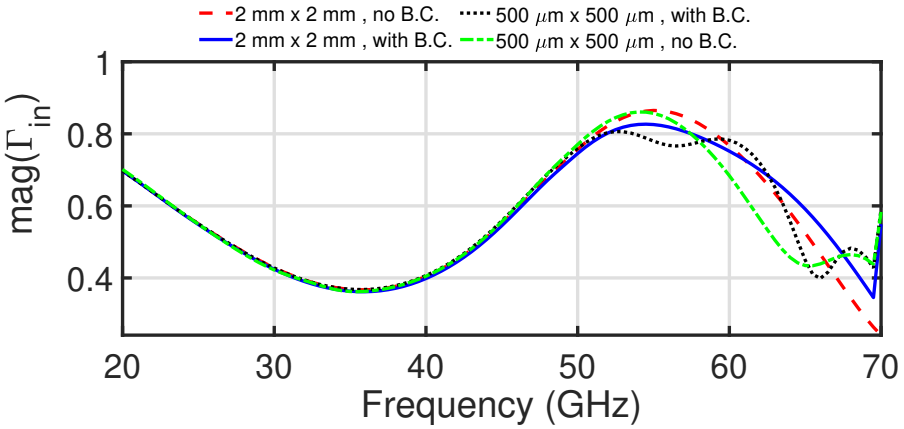
Figure 3.12: Full-chip EM-simulation results for large signal parameters. (a) at P_{1dB}. (b) at 6 dB back-off.

measurement and the EM simulation. The EM-simulation is performed up to 150 GHz for the entire chip layout using ANSYS-HFSS for a 2 mm × 2 mm chip substrate with a conductive plane at the back. The amplifier has the S_{21} of 12±0.05 dB from 27 to 39 GHz. The designed second-harmonic transmission notch for the transformer is measured at the same frequency as the simulation but with a lower depth. This can be attributed to the higher loss in the transformer and the resonance that occurs between the chip and PCB grounds as explained in Section 3.3. The PA is unconditionally stable over the entire operating bandwidth and no instability issue was observed during the measurements.

Figure 3.17(a) and (b) show the measured and simulated transducer gain and PAE over the output power. Our measured P_{1dB} is 12 dBm at 28 GHz and 11 dBm at 38 GHz which



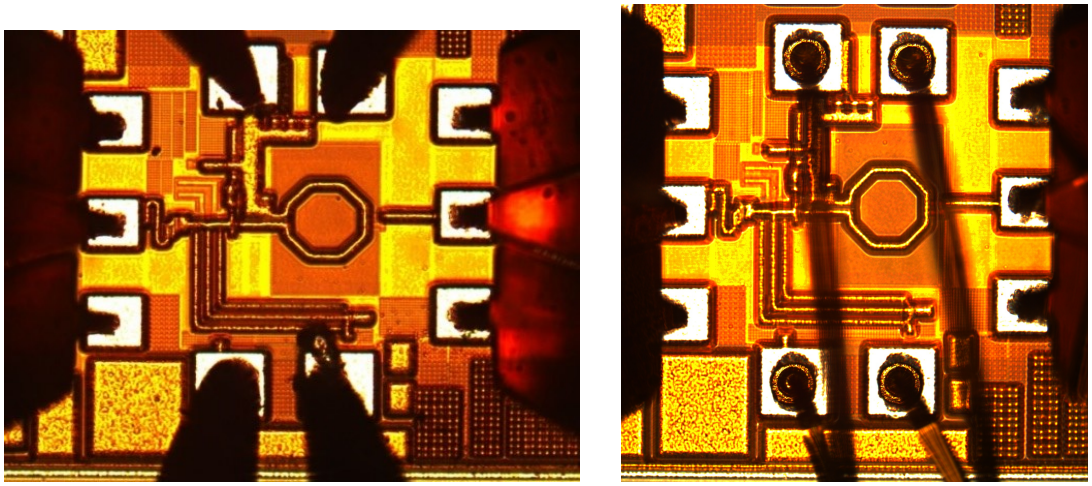
(a)



(b)

Figure 3.13: Full-chip EM simulation results or the effect of die size and interaction of conductive epoxy at the back of silicon. (a) Simulated S_{21} of power amplifier. (b) Magnitude of Γ_{in} (defined in Fig. 3.1(a)). B.C. stands for Back Conductive paste.

satisfy our goal of 11 dBm linear power from 27 to 30 GHz. The peak PAE of 25 % at 28 GHz and 26.7 % at 38 GHz is measured. The peak output power of 14 dBm and 13 dBm is measured at 28 and 38 GHz respectively as shown in Fig. 3.17(c). Fig. 3.17(d) shows the measured P_{1dB} of the amplifier. The measured P_{1dB} is above 11 dBm from 25 to 38 GHz and the measured PAE at P_{1dB} is higher than 25 % from 27 to 39 GHz. The measured collector efficiency at P_{1dB} is higher than 30 % from 30 to 38 GHz.



(a) (b)

Figure 3.14: Chip micro-graph. Chip size is 350 μm × 400 μm (pads excluded). (a) Chip measured with DC-probes for small signal measurements. (b) Wire-bounded chip for EVM measurement. Wire-bounds are far enough from the die to avoid de-tuning effect.

The PA is tested by broadband 64-QAM signal to evaluate its behaviour under modulated signals. Fig. 3.16 shows our EVM and ACLR measurement setup. A 64-QAM, 400 MHz bandwidth signal is generated by Keysight M8190 and up-converted to the desired carrier frequency by Keysight E8267D. The roll-off factor for the raised cosine filter is set to 0.35. The EVM is measured by Keysight VSA 89600 software installed on N9041B Keysight signal analyzer. The receiver span of our signal analyzer was limited to 1 GHz and we could successfully demodulate 64-QAM signals with maximum symbol rate of 800 MS/s with the EVM of less than 5 % at 28 and 38 GHz. However, we present the result for a 300MS/s signal so that we can measure the adjacent channel leakage ratio (ACLR). We observed that the average efficiency is independent of the signal bandwidth. We measured the modulated large signal parameters of the chip at 28, 30, 38 and, 42 GHz. These are the main frequency bands for 5G and SATCOM. Fig. 3.19 shows the results. PAE of 17±1 % at 8.4±0.2 % dBm average output power is achieved for 64-QAM signal. We measured the average power by integrating the spectrum of the signal. Our average power measurement has ±0.2 dB error which results in ±1 % inaccuracy in PAE measurement. Our signal generator had a residual EVM of less than 1 %. The measured EVM is better than -25 dB for average output power of 8.4 and 7.4 dBm at 28 and 38 GHz respectively.

Figure 3.18 (a) and (b) shows the measurement results for AM-AM and AM-PM at

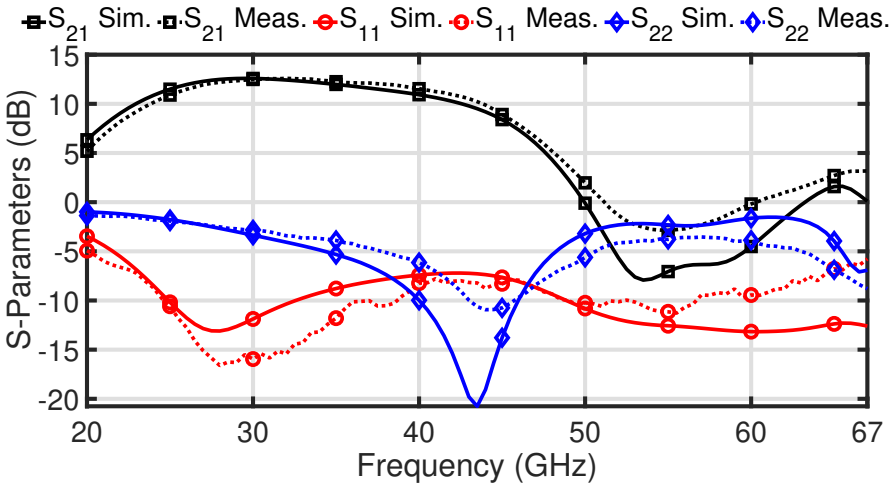


Figure 3.15: Comparison of measurement and simulation of small signal S-Parameters. Die size of 2 $mm \times 2\ mm$ with conductive plane at the back is considered for simulation.

both the 28 and 38 GHz bands. AM-PM of 2 °/dB and 3 3°/dB is achieved at P_{1dB} at 28 and 38 GHz respectively. The measured IM_3 is shown in Fig. 3.18 (c) and (d). The tone spacing is set to 400 MHz to evaluate the non-linearity of amplifier for wideband signals. The IM_3 of -16 dBc and -37 dBc is measured at 28 GHz for P_{1dB} and 6 dB back-off respectively. The dip in the IM_3 curve is due to class-AB biasing of the amplifier [65]. The IM_3 at 38 GHz band is -22 and -40 dBc at P_{1dB} and 6 dB back-off powers.

Table 3.2 compares the performance of our proposed design with the existing linear PAs in the literature. This work is the first reported PA with compact area, broadband relatively high efficiency response, and electrostatic discharge (ESD) protection. The proposed PA can cover all the 5G and Ka-band SATCOM bands and can be integrated in a phased-array beam-forming front-end.

3.4.1 Discussion on The Peak-Efficiency

In this chapter, a compact and broadband single-ended PA is presented with the main application of SATCOM beam-former chips. The single-ended input of the antenna elements necessitate the use of single-ended PA architectures. In [11] a broadband fully-differential PA with a transformer-based output matching is presented and an efficiency of above 40 % is reported. However, this efficiency drops to 30-35 % with the presence of output Balun in a active phased-array application as discussed.

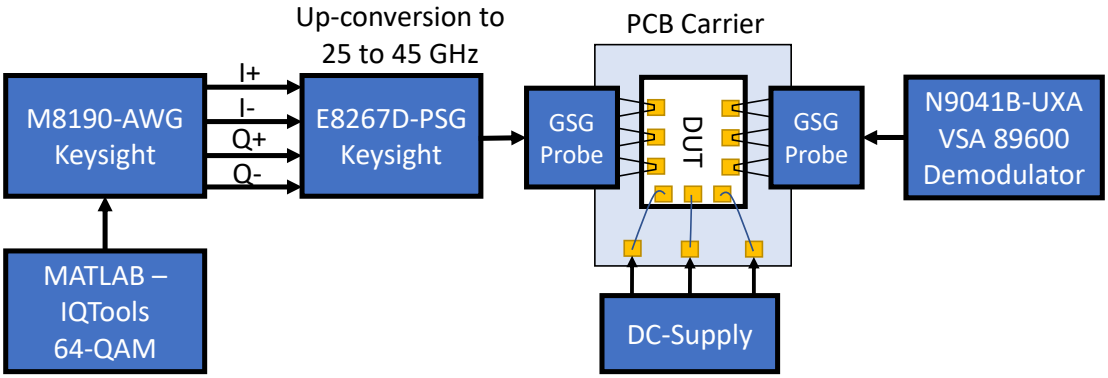


Figure 3.16: EVM and ACLR measurement setup.

Furthermore, the peak-efficiency of a PA is proportional to the supply voltage. In [10] and [11] the supply voltage of 2.4 V and 1.9 V are used for a common-emitter transistor, and in [9] and [95] VCC of 3.6 V and 4 V are used for a cascode structure. The peak-efficiency of 35% to 43% are reported in these works. However, all these PAs are operating very close to the HBT breakdown region [91] and some impedance mis-match at the output can cause transistor breakdown. Furthermore, in phased-array antennas, the antenna input impedance varies by scan angle and the return loss of the load for the PA can be as high as -5 dB [79]. A large VSWR at the output can enter the transistor into breakdown region and causes severe reliability issues for the phased-array system. Therefore, we chose a lower supply voltage of 2.4 V to have 2.33 V design margin (as calculated in Section 3.2) for the cascode structure. Our penalty for this choice is lower peak-PAE compared to other state-of-the-art works.

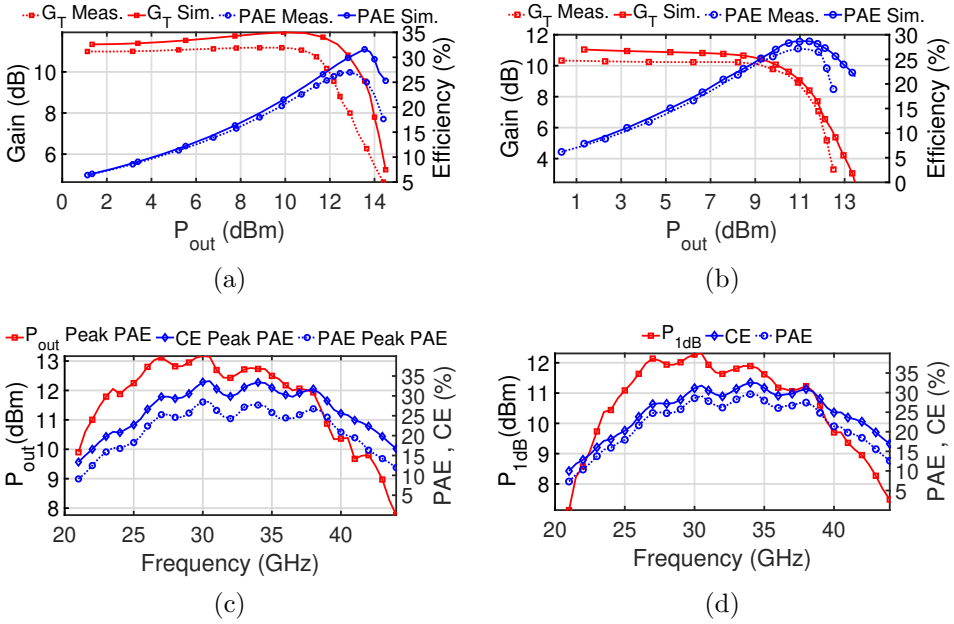


Figure 3.17: Measurement and simulation of transducer gain and PAE vs output power at (a) 28 GHz (b) 38 GHz. Measurement of peak-efficiency and the corresponding output power over frequency (c). Measurement of efficiency at P_{1dB} over frequency(d).

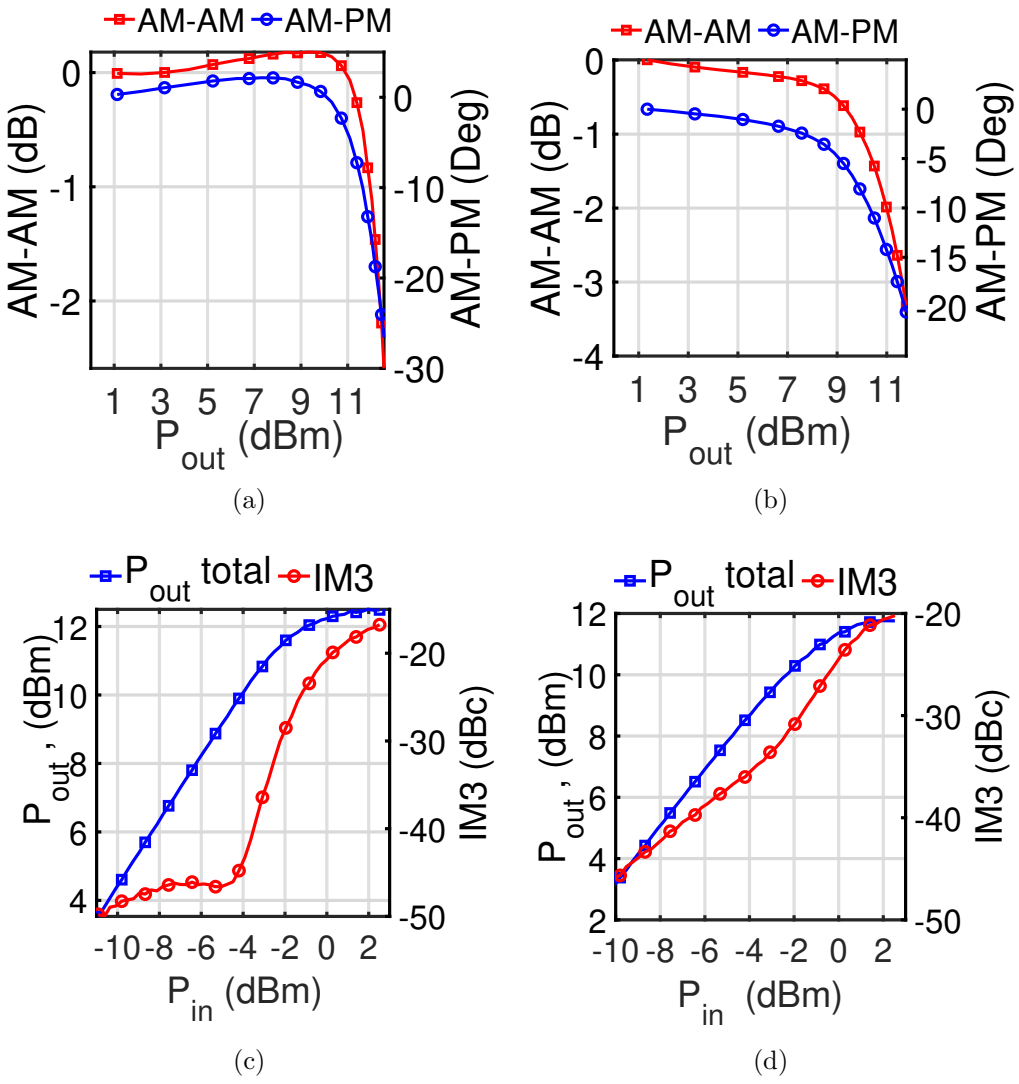


Figure 3.18: AM-AM and AM-PM measurements of the PA (a) 28 GHz (b) 38 GHz. IM_3 measurement of the PA at tone spacing of 400 MHz at (c) 28 GHz (d) 38 GHz.

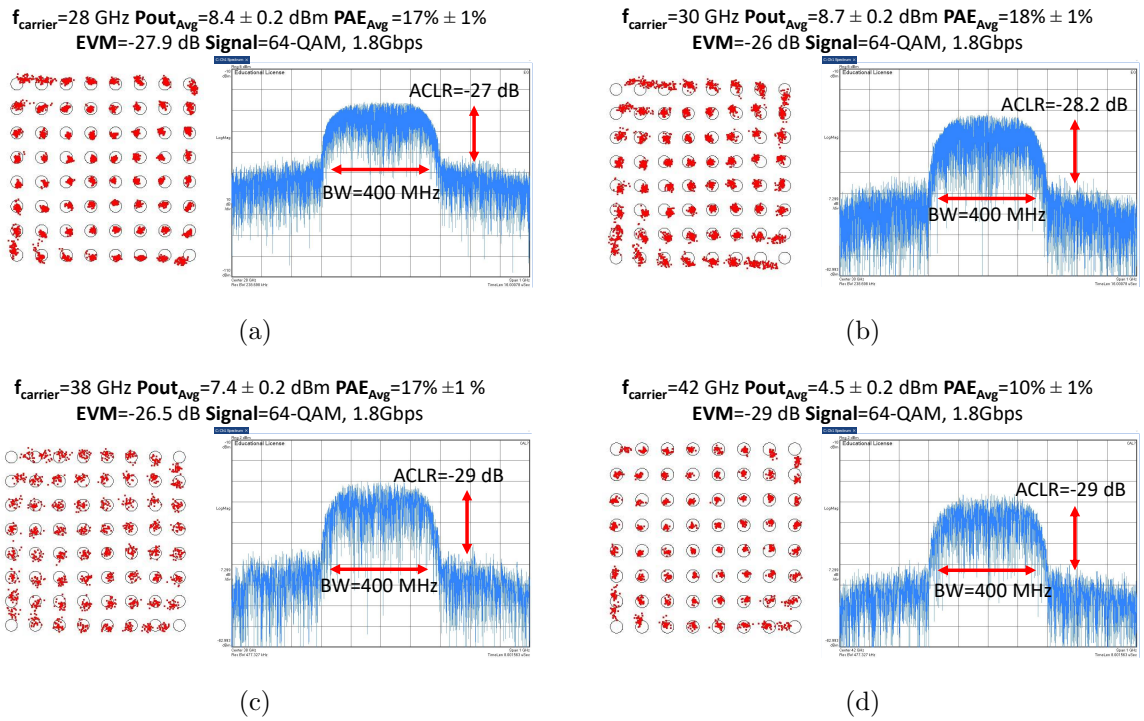


Figure 3.19: Measured constellation, PAE_{Avg}, EVM and, ACLR of a 64-QAM 300MS/s signal at different carrier frequencies. (a) 28 GHz (b) 30 GHz (c) 38 GHz (d) 42 GHz.

TABLE 3.2
CW AND MODULATED SIGNAL PERFORMANCE COMPARISON WITH EXISTING SILICON-BASED LINEAR PAS

	Operating Frequency (GHz)	f_0(GHz)	OP_{1dB} (dBm)	P_{sat} (dBm)	Peak PAE (%)	G_T (dB)	EVM(dB) Mod. - BitRate (Gbps)	PAE at EVM (%)	P_{out} at EVM (dBm)	Supply (V)	ESD Protection	Topology	Process	Core Size (mm^2)
This work	24-38	28 38	12 11	14 13	25 26.7	11.2 10.2	-28 -26 64-QAM / 1.8-4.8	17±1 17±1	8.4±0.2 7.4±0.2	2.4	Yes	1-Stg , Cont. Class-AB / SE*	130 nm SiGe	0.14
[11]	19-29.5	28.5	15.2	17	43.5	20	-25 64-QAM / 18	18.4	9.8	1.9	Yes	2-Stg, Cont. Class-F^{-1} / FD**	130 nm SiGe	0.29
[11]	23-40.5	28 39	16.9 17.4	18.9 18.9	45.7 41.2	18.7 15.6	-28.1 -28.1 64-QAM / 3	13.1 10.2	10.3 11	2	Yes	1-Stg, Cont. Class-F-1/F / FD**	45 nm SOI	0.14
[9]	27-30	28	15.5	18.6	35.3	15.3	-22 16-QAM OFDM / 3.2	11.5	12.6	3.6	No	1-Stg. Cont. Class-AB / FD**	130 nm SiGe	0.27
[10]	36-39.5	38	15	16.5	38.5	16	-26 64-QAM OFDM / 3.2	20	13.5	2.4	No	2-Stg, Class-F-1 /SE*	130 nm SiGe	0.5
[63]	27-31	28	14.3	15.3	36.6	16.3	-25 64-QAM OFDM / 1.5	9.6	5.3	1.15	Yes	2-stg. Class-AB / DB***	28 nm CMOS	0.16
[64]	26-33	28	27	15.1	33.7	22.4	-25 64-QAM OFDM / 4.8	11	6.7	1.1	Yes	3-stg. Class-AB / DB***	40 nm CMOS	0.23
[96]	26-34	28	13.2	14.75	46.4	10	-	-	-	1.1	No	Cont. Class-F / SE*	65 nm CMOS	0.12
[74]	27-30	28	14	15.6	41	15.8	-25.6 64-QAM OFDM / 2	19.3	10.4	1.1	No	2-Stg. Class-F / SE*	65 nm CMOS	0.24

* SE = Single-Ended output. ** FD = Fully-Differential PA. *** DB = Differential structure with output Balun.

3.5 Conclusion

A broadband, high efficiency, single-ended PA with linear output power 1 dB bandwidth of 25 to 38 GHz has been presented. A collector efficiency of more than 30 % is achieved from 30 to 39 GHz. An average PAE and output power of 17±1 % and 8.4/7.4±0.2 dBm are measured for a 400 MHz 64-QAM signal at 28/38 GHz. A non-inverting transformer is used for the output matching of the first and second-harmonics, which minimizes the layout area and operate as broadband ESD protection. The proposed amplifier demonstrates the realization of one of the key blocks in a multi-band mm-wave phased-array transmitter with relatively high efficiency and compact area and high reliability.

The main contributions of this work are as follows:

1- A transformer-based output matching structure is introduced that can be used in harmonic-tuned PAs. The compact layout of the proposed structure makes the use of harmonic-tuned PAs in phased array chips feasible and enhances their peak-efficiency.

2- The proposed output matching provides the second-harmonic trap, broadband operation and ESD protection in the layout footprint of a single transformer. This results in significant area reduction and make integration of more number of PAs in one die feasible.

3- The interaction of on-chip transformer with silicon bulk is investigated more carefully. It is shown that the size of the chip die can affect the response of the transformer at the second harmonic.

Chapter 4

A Compact and High-Efficiency Continuous Class-F^{-1} Power Amplifier for Millimeter-Wave 5G and SATCOM Phased-Array Transmitters

As demonstrated in Chapter 3, harmonic-tuned PAs can be used as the output stage of a beam-former chip due to their high peak-efficiency and high linearity at back-off. In Chapter 3, we used a non-inverting transformer in designing the output matching network of the PA. However, due to the narrow-band second harmonic suppression of this structure, we had to trade off the efficiency with the bandwidth. In this chapter, essentially an extension of Chapter 3, a 1:1 inverting transformer is studied and it is shown that it provides a relatively broadband second-harmonic filtering. Based on this structure, two PA examples from the continuous class-F^{-1} are presented. The first PA operates from 24-30 GHz and has a PAE of higher than 35 % over the bandwidth. The second PA, which is a class-F^{-1} PA based on the common-base structure, has a peak-efficiency of 42 % at 26 GHz and an output power of 16 dBm from 25 to 28 GHz.

In this chapter, a brief review of the continuous class-F^{-1} PA principle of operation is presented, followed by an investigation of the inverting transformer structure. The structure's broadband behavior is compared to that of a non-inverting transformer. Following these sections, the designs of the aforementioned PAs are presented. The chapter concludes

with a comparison of the back-off performance of these two amplifiers, demonstrating the superior performance of the common-base structure over the cascode structure.

4.1 Millimeter-Wave Harmonic-Tuned Power Amplifiers

In single-ended mm-wave PAs, the third harmonic component of the collector current is mostly absorbed by the transistor output capacitance. Tuning out this capacitance at the third harmonic reduces the bandwidth significantly and increases the output matching complexity. Therefore, it seems wise to consider a short circuit termination at the third harmonic for the transistor; however, this limits the possible operating classes of a harmonic-tuned mm-wave PA to classes A, AB, C, F^{-1} and their generalized continuous classes. In these classes of operations, the second harmonic impedance determines the class of operation. As continuous class-AB PA theory was discussed in Chapter 3, here only the continuous mode class F^{-1} PA theory is reviewed.

4.1.1 Continuous Mode Power Amplifier Theory

Harmonic-tuned PAs are based on short or open circuits at the even or odd harmonics. Continuous mode PAs are a generalized form of these classes where the harmonics are terminated by a reactive impedance. The collector (drain) current and voltage are given by [72, 97]

$$v_{F^{-1}}(\theta) = VCC\left[1+\sqrt{2}\left(1-\frac{V_{knee}}{VCC}\right)\cos\theta+\frac{1}{2}\left(1-\frac{V_{knee}}{VCC}\right)\cos 2\theta\right] \tag{4.1}$$

$$i_{CF^{-1}}(\theta) = i_{DC}(1-\frac{2}{\sqrt{3}}\cos\theta+\frac{1}{3\sqrt{3}}\cos 3\theta)\times(1-\xi\sin\theta) \tag{4.2}$$

the multiplying term of $(1-\xi\sin\theta)$ in (4.2) generalizes the collector current of a conventional class-F^{-1} into a a more general class of waveforms. The parameter ξ can vary only from -1 to 1 to avoid a negative collector current.

The load impedances for these harmonics can be calculated from $Z_n = -\frac{V_n}{I_n}$ and are given by the following equations

$$Y_{1,F^{-1}} = \sqrt{\frac{2}{3}}\frac{i_{DC}}{VCC-V_k}-\frac{j\xi}{\sqrt{2}}\frac{i_{DC}}{VCC-V_k} \tag{4.3}$$

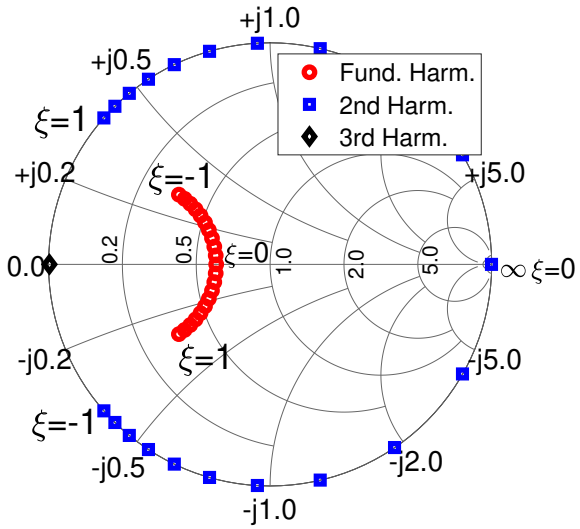


Figure 4.1: Ideal harmonic impedances of a continuous class-F^{-1} PA. $R_{opt} = 50\ \Omega$.

$$Y_{2,F^{-1}} = j\frac{7\xi}{3\sqrt{3}}\frac{i_{DC}}{VCC - V_k} \tag{4.4}$$

$$Y_{3,F^{-1}} = \infty. \tag{4.5}$$

The output power of a class F^{-1} PA can be calculated by

$$P_{out} = \frac{1}{2}\Re V_1 I_1^* = \sqrt{\frac{2}{3}}(VCC - V_k)i_{DC}. \tag{4.6}$$

Fig. 4.1 shows the fundamental, second and third harmonic impedance trajectories with ξ in the Smith-chart.

The peak-efficiency of a continuous class-F^{-1} is the same as that of a conventional class-F^{-1}, and is given by

$$\eta_{C,max} = \frac{P_{out}}{P_{DC}} = \frac{\sqrt{\frac{2}{3}}(VCC - V_k)i_{DC}}{VCC \times i_{DC}} = 0.82 \times \left(1 - \frac{V_{knee}}{VCC}\right) \tag{4.7}$$

Assuming that the maximum collector voltage is limited by the device breakdown voltage of V_{BK}, it can be shown [10] that the maximum collector efficiency is slightly less than (4.8) and is given by

$$\eta_{C,max,BK} = 0.28 \times \frac{V_{BK}}{VCC} \times \left(1 - \frac{V_{knee}}{V_{BK}}\right). \tag{4.8}$$

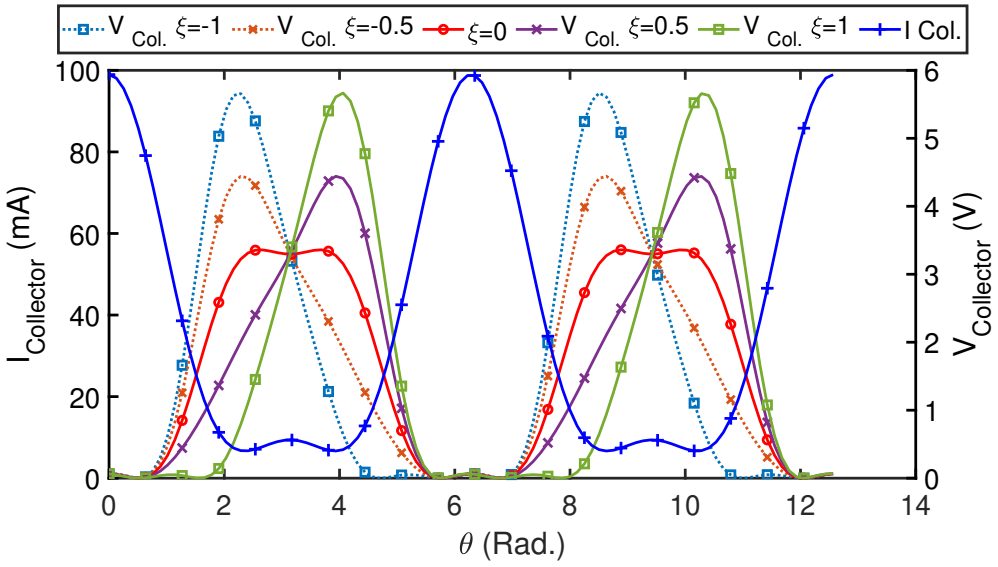


Figure 4.2: Collector current and voltage waveforms of an ideal class-F^{-1} PA for VCC=2.3 V and $I_{DC} = 28$ mA and $V_k = 0.4$ V.

For $VCC = 2.4$ V and $V_K = 0.4$ V and $V_{BK} = 5.6$ V, the peak-efficiency of a continuous class-F^{-1} PA is 60.6 %.

4.2 Inverting Transformer Properties

Figure 4.3(a) shows an inverting transformer, and Fig. 4.3(b) shows a simplified lumped circuit model for this same transformer. In this model, which can only be used at low frequencies, $k_m < 0$ and therefore the parallel LC tank formed by L_{12} and C_{12} creates a low impedance path from the input to the output. Therefore, at the primary and secondary self-resonance frequencies where $L_{11} - C_1$ and $L_{22} - C_2$ resonate at f_0, we can have low-loss transmission from the input to the output. Fig. 4.3(c) shows the frequency response of a 1:1 inverting transformer implemented in 0.13 μm Bi-CMOS technology (see Fig. 3.1(c)). At the self-resonance frequencies of the primary and secondary turns, where Z_{11} and Z_{22} show high impedance, the transformer shows a low-loss transmission response in which $S_{21} = 0.51$ dB. Therefore, the full-wave solution confirms the intuitive analysis obtained from the circuit model. However, this circuit model cannot predict the broadband behavior of an inverting transformer. Broad-side coupled lines can be used for more accurate modeling of a 1:1 transformer. Fig. 4.5 shows the circuit model of an inverting transformer that

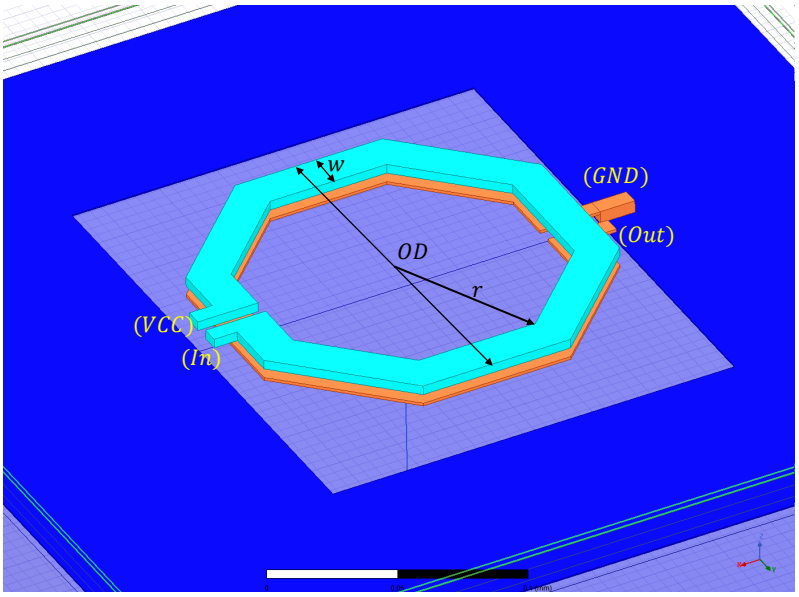
uses coupled-lines. Fig. 4.3(a) and (b) show two coupled-line structures modeled in HFSS, and Fig. 4.3(c) shows the transformer structure. AM and LY metals form the coupled lines, and the MQ metal layer forms the ground return path. Fig. 4.4 compares the full-wave solution of the rectangular transformer, shown in Fig. 4.6(c), with the circuit model solution obtained from simulating the full-wave solution of straight coupled lines [Fig. 4.6(a)] and a transformer half-turn [Fig. 4.6(b)]. It can be seen that the solution obtained from the transformer half-turn fits the full-wave solution of a rectangular transformer over the entire bandwidth. The solution obtained from a straight coupled line [Fig. 4.6(a)] deviates from the full-wave solution, but it can predict the transmission notch frequency accurately.

In inverting transformers, the electric and magnetic couplings between the turns add together, resulting in a low-loss transmission response in the fundamental harmonic. Fig. 4.7(a,b) compares the G_{Max} of a 1:1 transformer at the various configurations shown in Fig. 4.7(c). An inverting transformer has lower transmission loss and a deeper transmission notch in its frequency response compared to a non-inverting transformer. For the chosen dimensions, an inverting transformer with single-ended excitation has a transmission loss that is almost equal to the loss found for a deferentially excited transformer [Fig. 4.7(c), item (3)]. This property makes an inverting transformer an interesting structure for implementing a compact, high-efficiency PA at mm-wave frequencies.

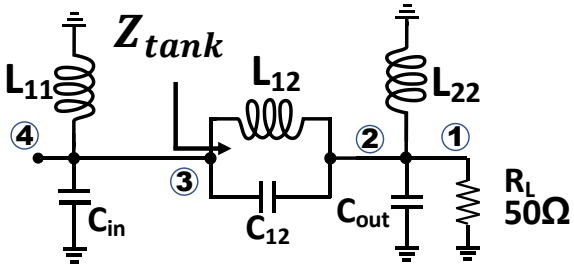
4.2.1 Parametric Study of an Inverting 1:1 Transformer

For more accurate analysis of an inverting transformer, a parametric analysis was performed with ANSYS-HFSS. Fig. 4.8 shows the results. Fig. 4.8(a,c) shows the magnitude of the reflection coefficient at the primary input when the secondary turn output is terminated to a 50 Ω load. The magnitude of the reflection coefficient is 0.9 at the frequency of the notch; this is higher than the achieved reflection coefficient of the non-inverting transformer studied in Chapter 3. The higher reflection coefficient at the second-harmonic results in higher peak-efficiency.

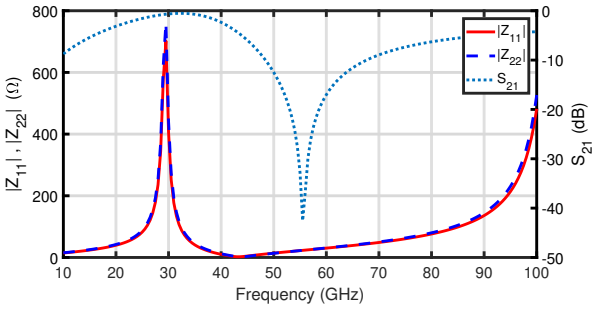
The parametric study shows that the radius and width of the transformer have little effect on its transmission loss. However, the transmission notch frequency increases as the width of the transformer is reduced. Increasing the output diameter decreases the transmission notch frequency. We used the results of this parametric study to determine the proposed output matching design. The output diameter and width of the transformer were chosen based on the frequency of the second harmonic. Furthermore, the required current handling capability puts a minimum on the transformer width for reliable operation of the PA.



(a)



(b)



(c)

Figure 4.3: (a) Geometry of an inverting transformer. (b) Simplified low frequency circuit model of an inverting transformer. (c) Frequency response of a 1:1 inverting transformer implemented in Bi-CMOS 8xp metal stackup. $r = 64\ \mu m$, $w = 14\ \mu m$. The maximum of S_{21} is at 31 GHz and equals -0.51 dB.

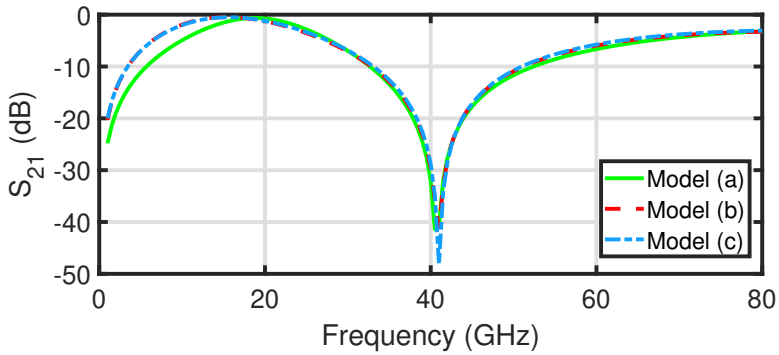


Figure 4.4: Comparison of S_{21} responses generated from models shown in Fig. 4.6 for modeling an inverting transformer.

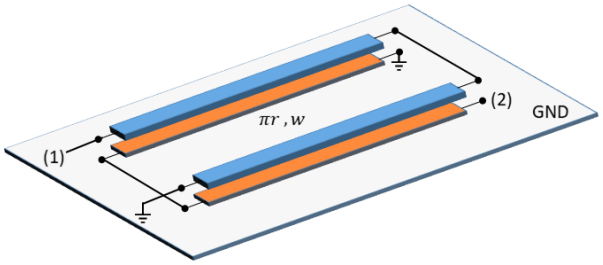
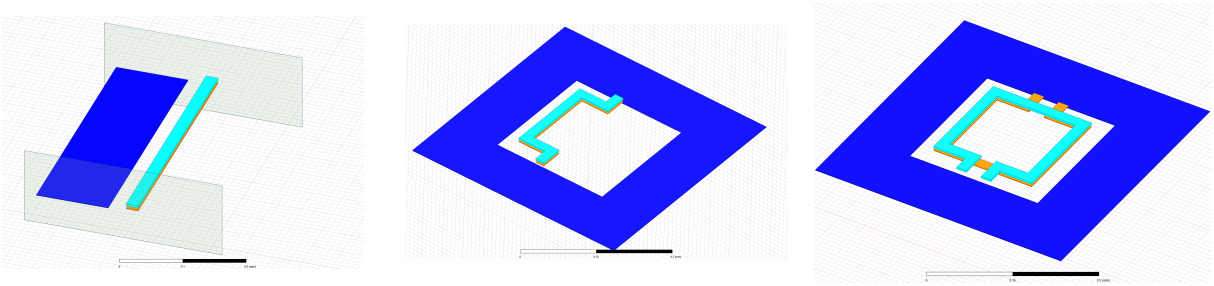


Figure 4.5: Modeling a 1:1 inverting transformer with coupled lines. Each half turn of the transformer is modeled by a straight line that is half the length of the turn perimeter.

The low-loss transmission and high rejection in an inverting transformer make it a preferable choice for harmonic-tuned PAs. Below, the design of a wide-band harmonic-tuned PA with OP_{1dB} of 11.5 dBm from 24-30 GHz and a narrow-band class-F^{-1} PA with 16 dBm output power is presented.

4.3 Harmonic-Tuned PA Design Using Inverting Transformer in the Output Matching

As explained in the previous section, a 1:1 inverting transformer can operate as the output matching network of a harmonic-tuned PA as it has very low-loss transmission in the



(a) (b) (c)

Figure 4.6: HFSS models: (a) broadside coupled line modeled, (b) half-turn of a transformer, and (c) rectangular inverting 1:1 transformer. (Substrate stack-up is not shown for clarity.)

band-pass and a very deep rejection in its stop-band response. By employing an inverting transformer in the output matching of a PA, we can realize a low-loss and compact output matching network for a class-F^{-1} and a continuous class-F^{-1} PA. Furthermore, transformers can be used as the input and inter-stage matching networks to achieve wide-band low-loss matching over a compact area.

4.3.1 Designing Output Matching Network for Wide-Band Operation

Our full-wave solution of an inverting 1:1 transformer shows that it provides a wide rejection band and a wide and low-loss transmission band. In the rejection band, the input impedance of the transformer has an inductive response with a very small resistive part. The wide transmission and rejection response of the inverting-transformer makes the design of a wide-band harmonic-tuned PA possible. Fig. 4.9 shows the input impedance of the transformer. It can be seen that from 48 to 60 GHz, the input impedance of the transformer is mostly inductive. Furthermore, it creates a wide-band harmonic trap that can be used to control the angle of the reflection coefficient at the second-harmonic to enhance the peak-efficiency. A 20 μm HBT transistor was used in a cascode structure for this PA and the transistor layout parasitics were extracted using the RC-extraction method. A CBE transistor structure available in the BiCMOS technology was chosen due to its smaller interconnect parasitics. The supply voltage is set to 2.4 V. A load-pull simulation at f_0 = 24 GHz, f_0 =27 GHz, and f_0 =30 GHz was performed for the extracted transistor.

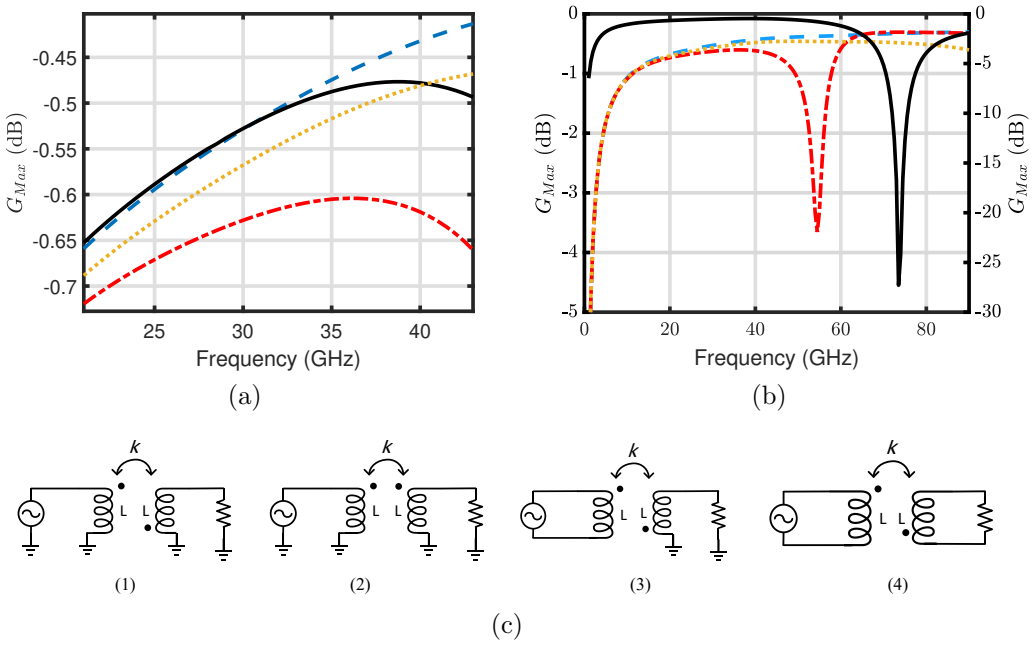


Figure 4.7: Comparison of different excitations on the G_{Max} of a 1:1 transformer. Inverting (solid line) and non-inverting (dot-dash line) transformer with single-ended input and output. Fully differential transformer (dashed line). Balun structure (differential input and single-ended output, dotted line). (a) Bandpass response. (b) Broadband response. (c) Different transformer excitations.

Fig. 4.10 shows the results. The second harmonic is terminated to an open-circuit in this load-pull simulation. The load-pull results show that the efficiency contours at these frequencies are almost identical. If we can design our matching network in a way that realizes an impedance close to the 60+j60 Ω region, we can achieve a peak efficiency of higher than 50 % and an output power of higher than 12 dBm. Fig. 4.11 shows the effect of second-harmonic termination impedance on the output power and efficiency of the transistor at 28 GHz. The second harmonic reflection coefficient is set to $0.9 \exp j\alpha_{2nd}\pi$. It can be seen that there is a wide design space for controlling the second harmonic impedance. The PAE remains above 48 % for $1 < \alpha_{2nd} < 2$ and $0 < \alpha_{2nd} < 0.15$. By designing the output matching network with second harmonic impedance in this region, we can achieve high efficiency over a wide bandwidth. It should be mentioned that the result in Fig. 4.11 is almost the same for the other frequencies examined: 24, 27, and 30 GHz.

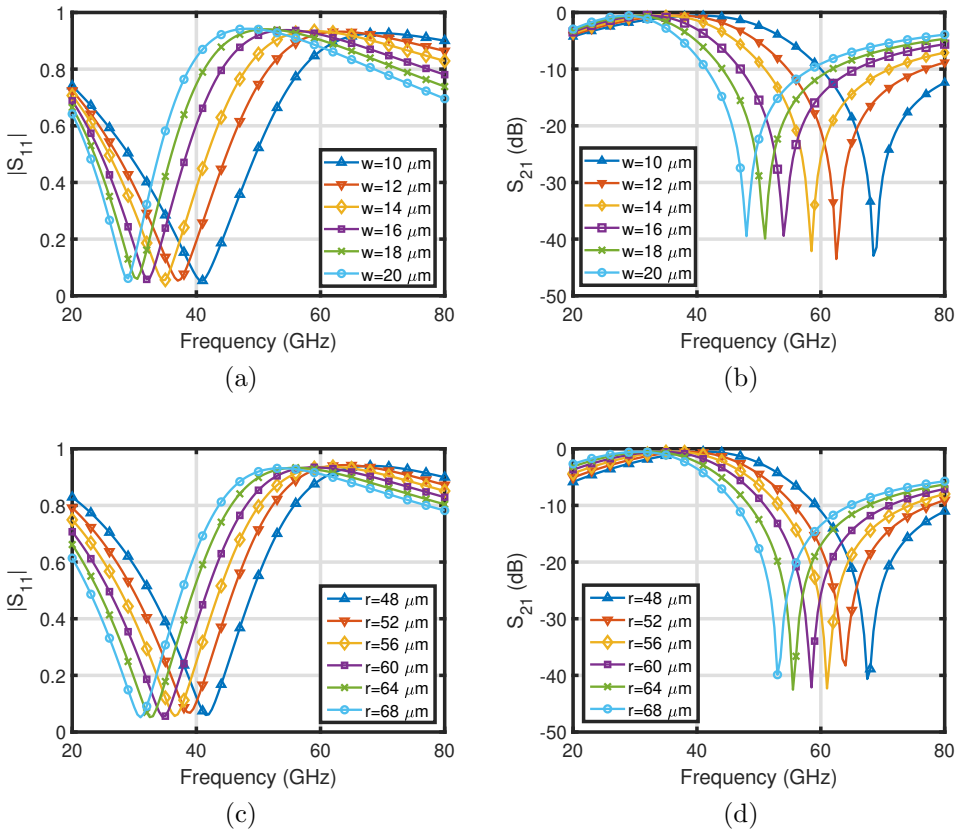
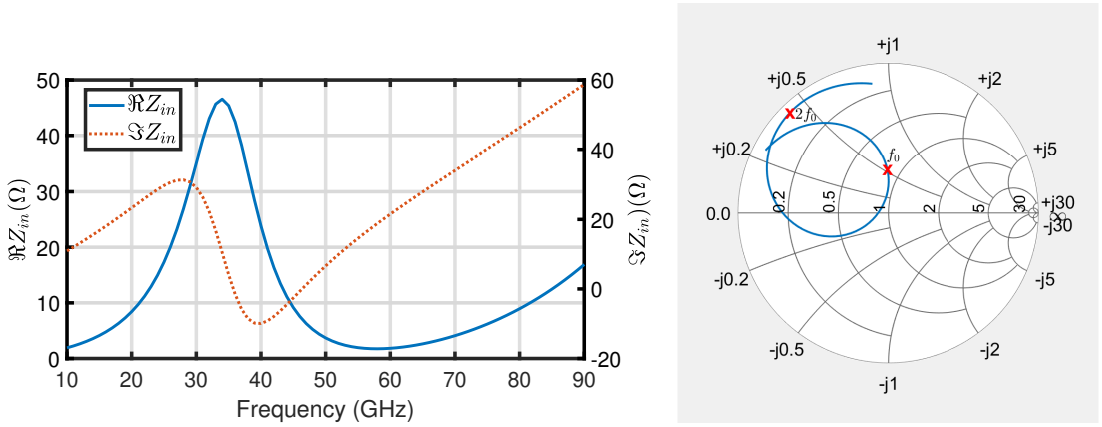


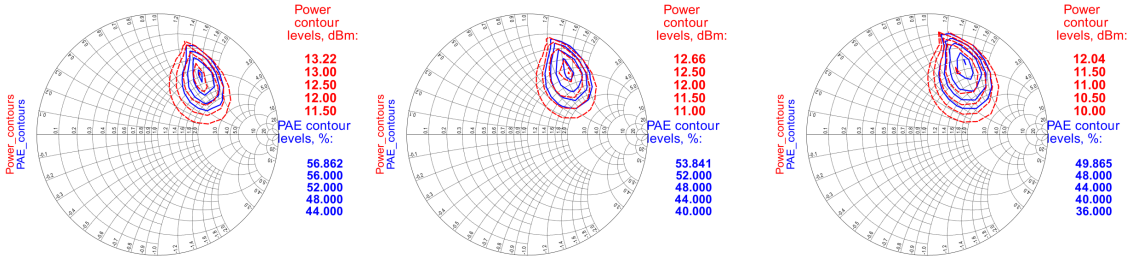
Figure 4.8: Parametric study of the 1:1 inverting transformer shown in Fig. 4.3(a).

Following the fundamental and second harmonic impedance analysis, the output matching was designed, as shown in Fig. 4.12(a). A series inductor is used to increase the inverting transformer reactance at the second harmonic that also provides a broadband match to the $Z_{opt} = 60 + j60\ \Omega$. Fig. 4.12(a) and (b) show the equivalent circuit of the output matching network at the fundamental and second harmonics, respectively. C_{p1}, C_{p2}, and C_{12} are the parasitic capacitances of the series inductor and inter-turn capacitance of the transformer. The input and output parasitic capacitances of the transformer can be absorbed by C_{p2} and C_1 and are not shown in the figure. Fig. 4.13(a) shows the realized intrinsic and extrinsic impedance of the designed output matching network. It can be seen that the extrinsic impedance rotates around the $Z_{opt} = 60 + j60\ \Omega$, and the second harmonic impedance lies in the desired region as well. Fig. 4.13(b) shows the input impedance of the realized output matching network. The real part of the input impedance



(a) (b)

Figure 4.9: Wide-band response of inverting transformer with output terminated to 50 Ω. (a) Input impedance. (b) Reflection coefficient at the primary turn in Smith-chart.



$f_0 = 24\ GHz$ $f_0 = 27\ GHz$ $f_0 = 30\ GHz$

Figure 4.10: Load pull results for extracted transistor at various frequencies.

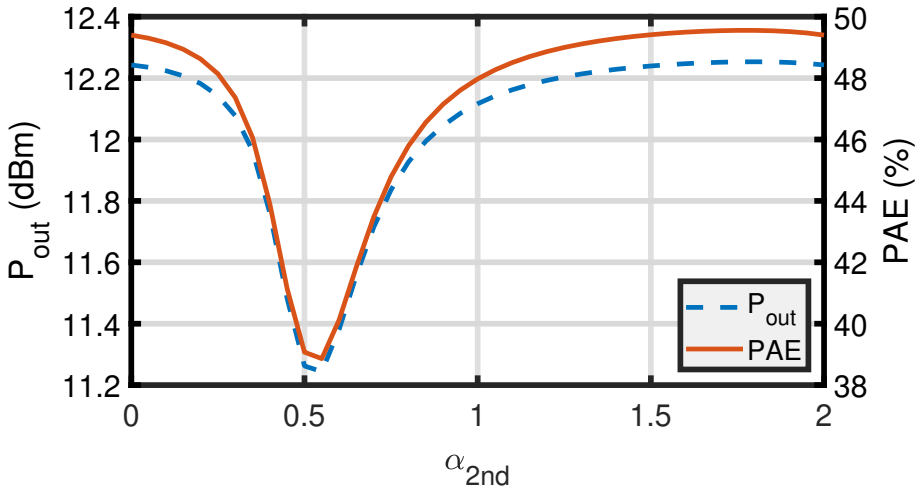
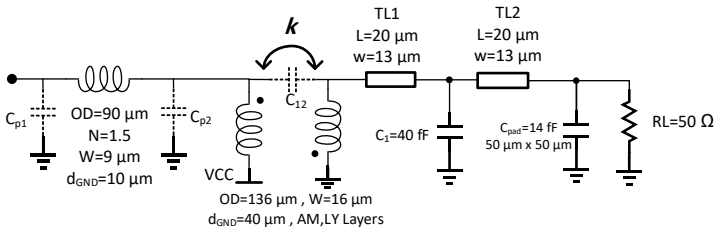
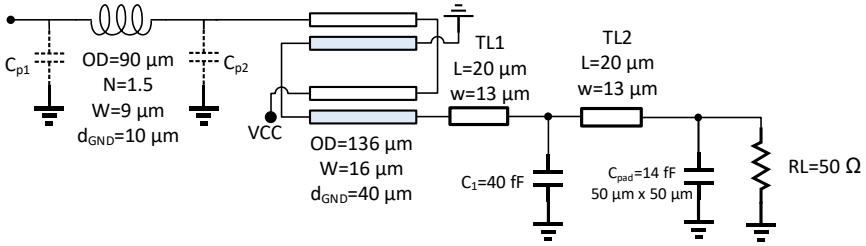


Figure 4.11: Effect of second-harmonic reflection angle on output power and efficiency of an extracted transistor. The fundamental harmonic impedance is set to $Z_L = 60 + j60\ \Omega$.

is close to 100 Ω and the imaginary part is close to zero Ω over the operating bandwidth. This provides a broadband match at the fundamental harmonic. Fig. 4.14 shows the power gain of the final output matching network. The blue dot-dash line shows the response of the circuit shown in Fig. 4.12 with an ideal DC supply source. The VCC node here is connected to an ideal voltage source. The output matching loss, in this case, is −0.7 dB at 24 GHz and −0.65 dB at 30 GHz. However, by including the actual DC decoupling network in the EM simulation, the output matching loss drops to −0.85 dB at 24 GHz and −0.95 dB at 30 GHz. There is a notch in the output matching response at 15 GHz which is due to the resonance of DC decoupling caps with the partial inductance of the interconnects. It is possible to avoid this resonance in the band of operation of interest by using an artificial quarter-wavelength line that creates a short-circuit at the middle of the operating band, at node VCC in Fig. 4.12 (a). Fig. 4.12(c) shows the complete proposed output matching structure with the artificial quarter-wavelength line. The structure of the artificial quarter wavelength line can be seen in Fig. 4.15(a). It includes an open-ended transmission line loaded by four metal-insulator-metal (MiM) capacitors. Fig. 4.15(b) shows the effect of MiM capacitor width on the resonance frequency of this line. A supply impedance of less than 1 Ω in the band of operation can be achieved as shown in Fig. 4.15(b) for $w_{MiM} = 25\ \mu m$. By using this method, we make sure the supply impedance at the band of operation is well controlled. An array of MiM capacitors and low-Q MOS (Metal-Oxide-Semiconductor) capacitors are also used to maintain low impedance level for



(a)



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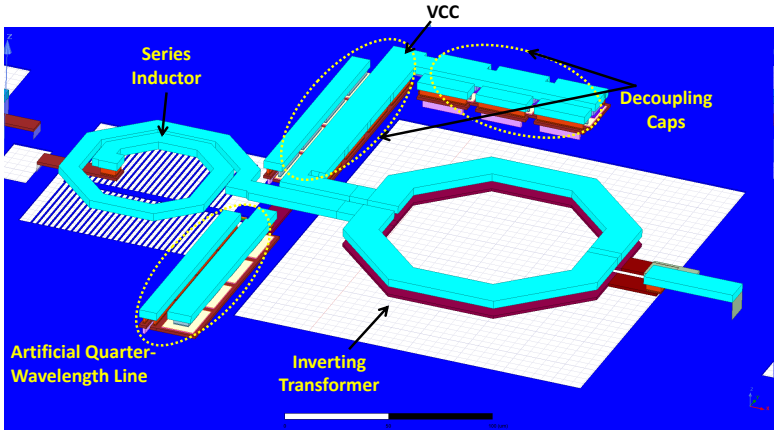
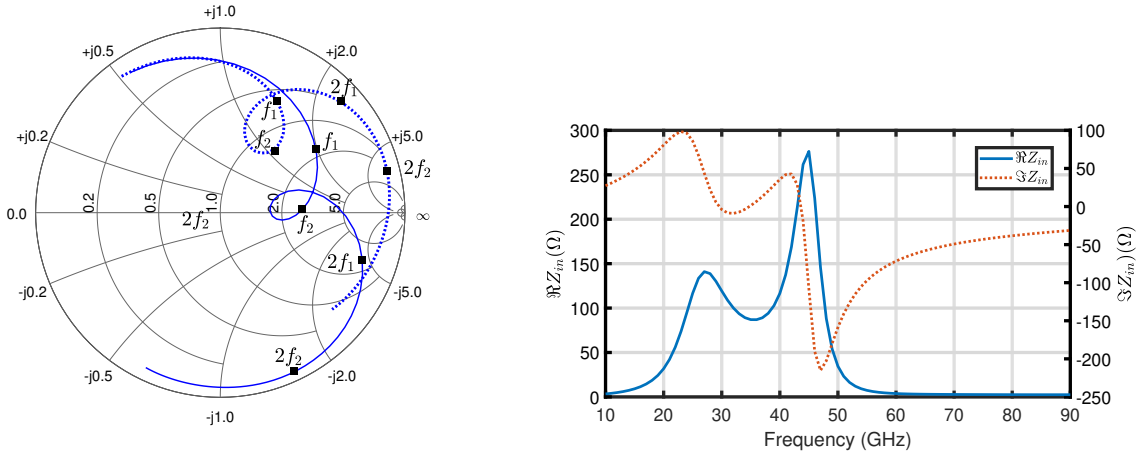


(c)

Figure 4.12: Output matching network: (a) equivalent circuit model at fundamental harmonic, (b) equivalent circuit model at second harmonic, and (c) three dimensional model of implemented output matching network.



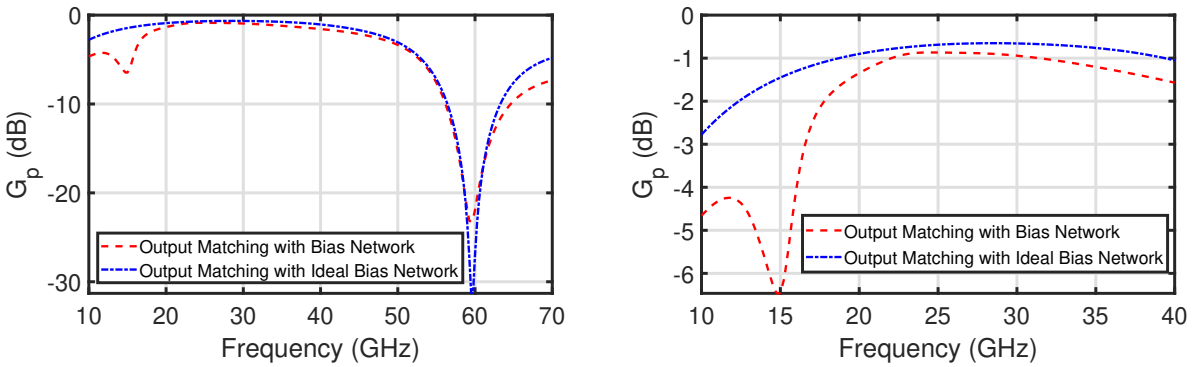
(a) (b)

Figure 4.13: (a) Load trajectory of designed output matching (solid line) and intrinsic collector impedance of the extracted $2\times10\mu m$ HBT at f_0 =28.5 GHz. (b) Realized intrinsic collector impedance.

the VCC node.

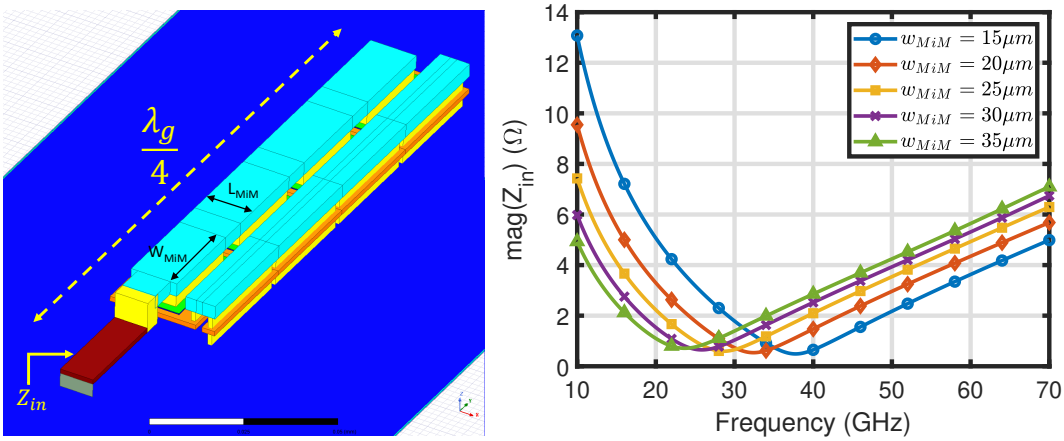
4.3.2 Class of Operation

To find the operating class of the PA, the intrinsic collector impedance is calculated. Fig. 4.13 shows the realized impedance of the output matching network, the dotted curve showing the intrinsic impedance. The intrinsic impedance determines the operating class of the amplifier. At f_0 = 24 GHz, the fundamental and second harmonic impedances resemble the continuous class-AB and at f_0 =30 GHz, the operating class is similar to a class-F^{-1} PA. Fig. 4.16 shows the intrinsic collector current and voltage waveforms of the designed PA. It can be seen that at 24 GHz, the current and voltage waveforms are similar to a continuous mode PA (class-F^{-1}). The collector voltage rises to 6 V as is typical when ξ in (4.2) reaches 1. The waveforms at 30 GHz are similar to a conventional class-F^{-1} PA.



(a) (b)

Figure 4.14: Power gain of output matching network. (a) Broadband response showing second harmonic trap. (b) Fundamental harmonic response showing output matching loss and effect of non-ideal supply decoupling in a single-ended PA.



(a) (b)

Figure 4.15: Implemented artificial quarter-wavelength line made with array of MiM capacitors. L_{MiM} is 18 μm. (a) three dimensional view of the structure in ANSYS-HFSS. (b) Magnitude of input impedance for various MiM cap sizes.

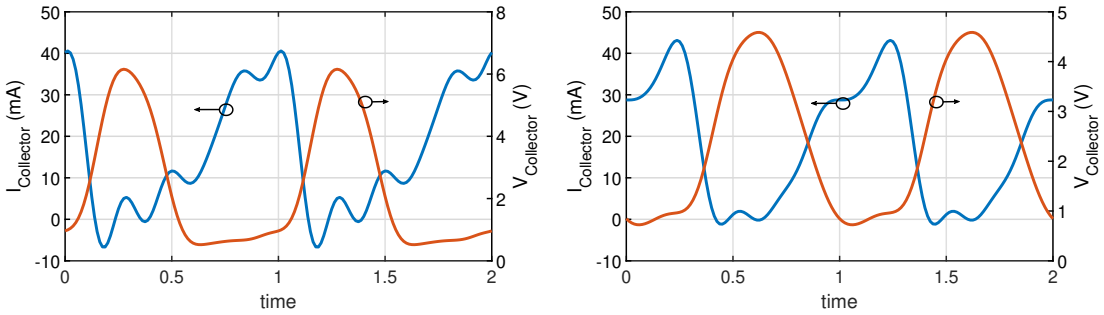


Figure 4.16: Intrinsic collector current and voltage waveforms at (a) 24 GHz and (b) 30 GHz.

4.3.3 Driver Design

The driver was designed as a cascode stage to enhance the gain. It was designed to have a wide-band frequency response for the amplifier. The efficiency of the driver does not affect the total PAE of the amplifier due to the large gain of the output stage. A transformer is used for the input and inter-stage matching networks. A transformer in the inter-stage matching network provides biasing for the driver and the output stage in a compact layout. The input and inter-stage matching networks are implemented with a 2:1 transformer. The dimensions of these transformers are optimized for a flat gain response over frequency. Fig. 4.18(a) shows the small-signal S-parameters of the final implemented PA. The entire chip was simulated in ANSYS-HFSS to capture all the unwanted couplings. The inter-stage matching dimensions were optimized to obtain a flat gain over the operating bandwidth. The maximum gain is 27.4 dB at 24 GHz, and the 1dB bandwidth is from 21.2 GHz to 28 GHz. The amplifier is unconditionally stable. Fig. 4.18(b) shows the total PAE and gain of the PA over the operating bandwidth. The peak PAE of 35 % is achieved at 24 GHz. Fig. 4.18 (c), (d) show OP_{1dB} and the corresponding PAE at different frequencies.

4.4 Design of a Two-Stage Common-Base Class-F^{-1} Power Amplifier with Peak Efficiency of 42 %

In this section, the design of a two-stage PA based on a common-base structure is presented. We use the same output matching structure as in Fig. 4.12, based on an inverting

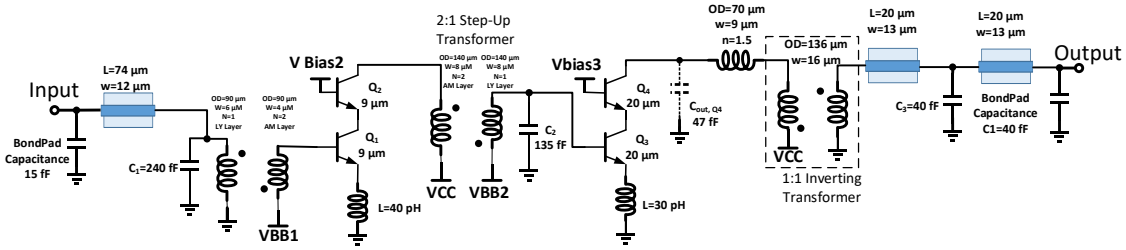


Figure 4.17: Schematic diagram of implemented two-stage PA.

transformer.

4.4.1 Common-Base Amplifier Properties

Most of the PAs implemented in this thesis so far have been based on a cascode structure. A cascode structure has high gain, however, it needs a higher supply voltage to achieve efficiencies higher than 40 %. Furthermore, its higher V_k compared to the common-emitter (CE) structure, limits its peak PAE. Therefore, for applications where the supply voltage is below 2 V, cascode PAs suffer from low peak efficiency.

In CE amplifiers, the maximum supply voltage is limited to $V_{CER} = 1.6$ V, whereas in common-base structures, the supply voltage is limited by $V_{CBO} = 5.6$ V. The latter is much higher than V_{CER}. Therefore, the supply voltage of a common-base amplifier can be set to a higher value compared to a CE structure. This results in higher peak efficiency in common-base structures compared to CE or cascode structures [98].

In common-base structures, the AC-grounded base isolates the input and output by removing the Miller effect. Therefore, a higher gain can be achieved for the same bias current in a common-base versus a CE structure. Furthermore, the input impedance of a common-base is mostly resistive and is given by

$$Z_{in} = \frac{1}{g_m} || C_\pi \approx \frac{1}{g_m} \tag{4.9}$$

where g_m is the transistor trans-conductance and C_π is the base-emitter capacitance. This results in broadband input matching. However, the input impedance of a common-base transistor is usually low for large transistors and this makes the design of the input-matching (or inter-stage) network challenging. In PAs for phased-array applications, the

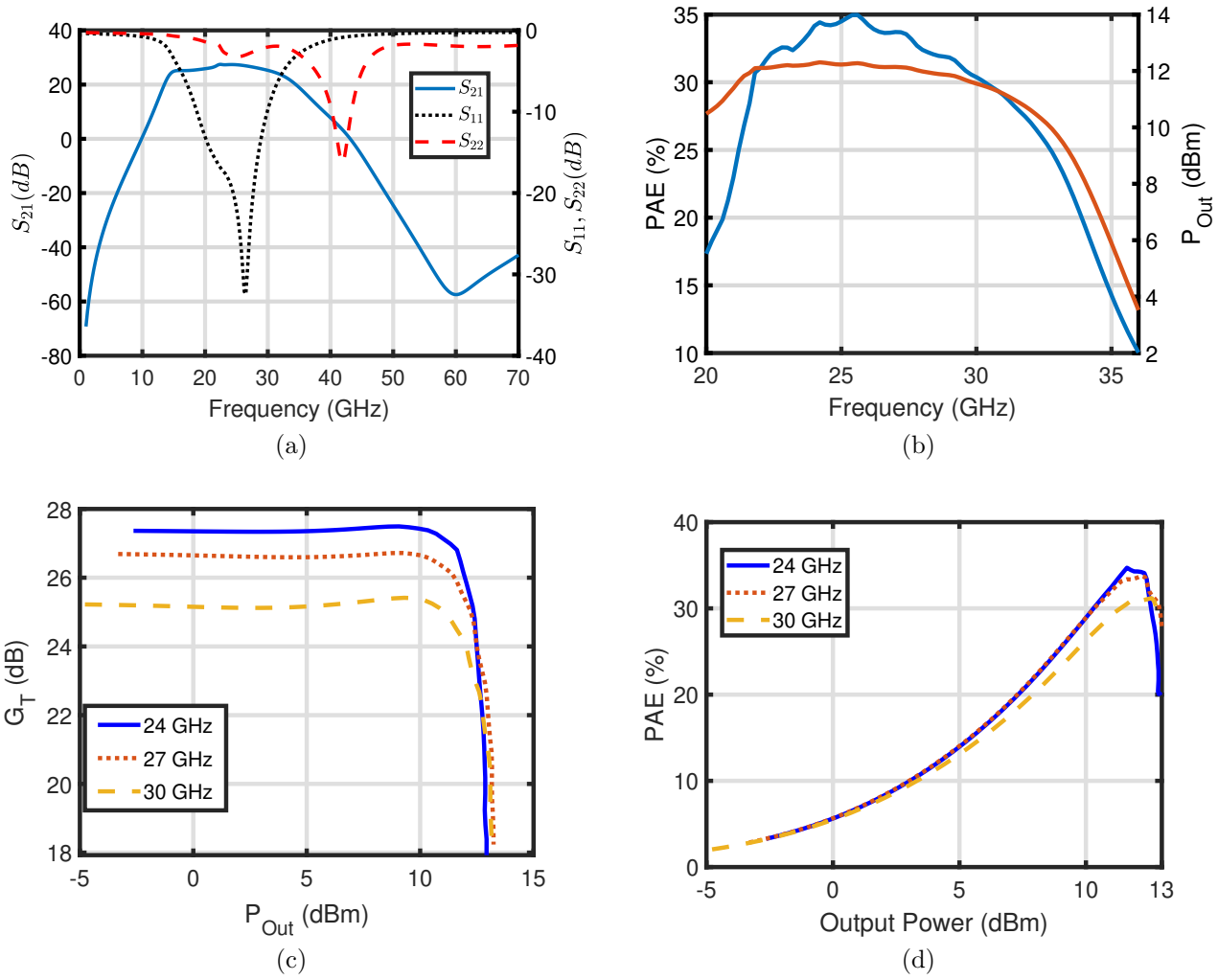


Figure 4.18: Post-layout small and large signal responses of designed PA. (a) Small signal S-parameters of two-stage PA. (b) Output power and efficiency over frequency. (c) Gain compression of PA at 24, 27 and 30 GHz. (d) PAE versus output power at 24, 27 and 30 GHz.

maximum output power is in the range of 10-15 dBm. For this output power level, transistor size is not very large and the emitter input impedance is in the range of 5-20 Ω. This simplifies the design of the input matching network and makes a common-base PA a good candidate for large phased-array applications.

In this section, we first perform a load-pull analysis for a common-base transistor and investigate the effects of a second-harmonic termination on the efficiency and output power. Then, input and output matching networks are designed for this PA. The inter-stage matching network is based on a 2:1 transformer which has a high coupling coefficient; the output matching is based on an inverting transformer.

To have a better understanding of the common-base structure, the DC I-V curves of such a structure were studied and compared with those of a cascode structure. Fig. 4.19(a), (b), and (c) show the DC I-V curves of a $3\times10\mu m$ HBT for three different configurations. In Fig. 4.19(a), the maximum collector voltage is determined by BV_{CER}, where R=0 and BV_{CER} is a function of the bias current. For low bias currents, this value can be as high as 4 V; for high bias currents it drops to 2 V. However, if we bias an HBT with a current source at the emitter, as shown in Fig. 4.19(b), the breakdown due to collector voltage is moved to very high voltages. This is mainly because the collector current is forced to be constant by the current source and the generated holes in the breakdown of the collector-base junction are absorbed by the voltage source connected to the base. This explains the very high breakdown voltage seen for the cascode structure shown in Fig. 4.19(c). In a cascode structure, the bottom transistor operates as a current source, and therefore the collector breakdown voltage is determined by BV_{CBO}.

A common-base PA's large-signal behavior is mostly similar to Fig. 4.19(b) where the current source has a finite inductance as shown in Fig. 4.19(d) [98]. However, the DC behavior of a common-base PA is similar to Fig. 4.19(a). The maximum supply voltage for a common-base PA is determined by these curves as opposed to in the cascode structure where it is possible to have a larger DC supply voltage as shown in Fig. 4.19(b).

4.4.2 Load-Pull Analysis of a Common-Base PA

As mentioned in the introduction of the chapter, the proposed design is intended for 16 dBm output power. Assuming 1 dB loss for the output matching network, the transistor should deliver 17 dBm. The maximum collector voltage can be calculated from (4.1) and is given by

$$V_{C,max} = (1.5 + \sqrt{2})VCC - (0.5 + \sqrt{2})V_k \tag{4.10}$$

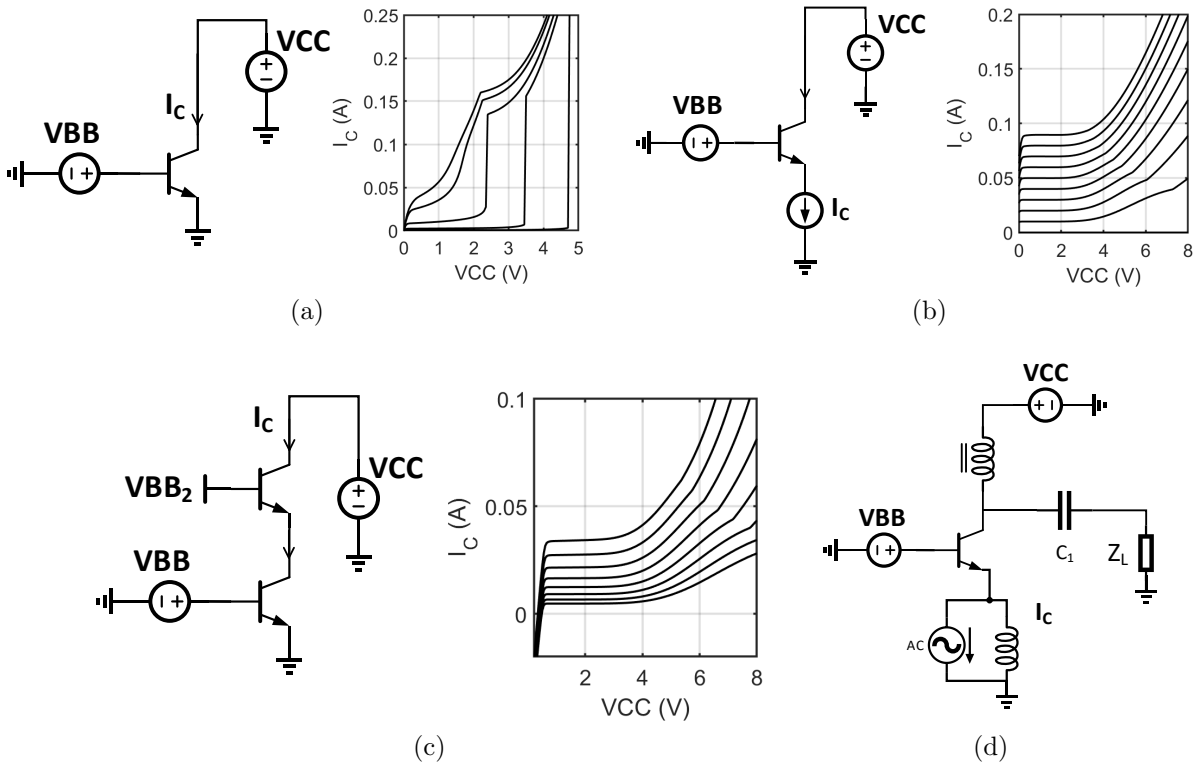
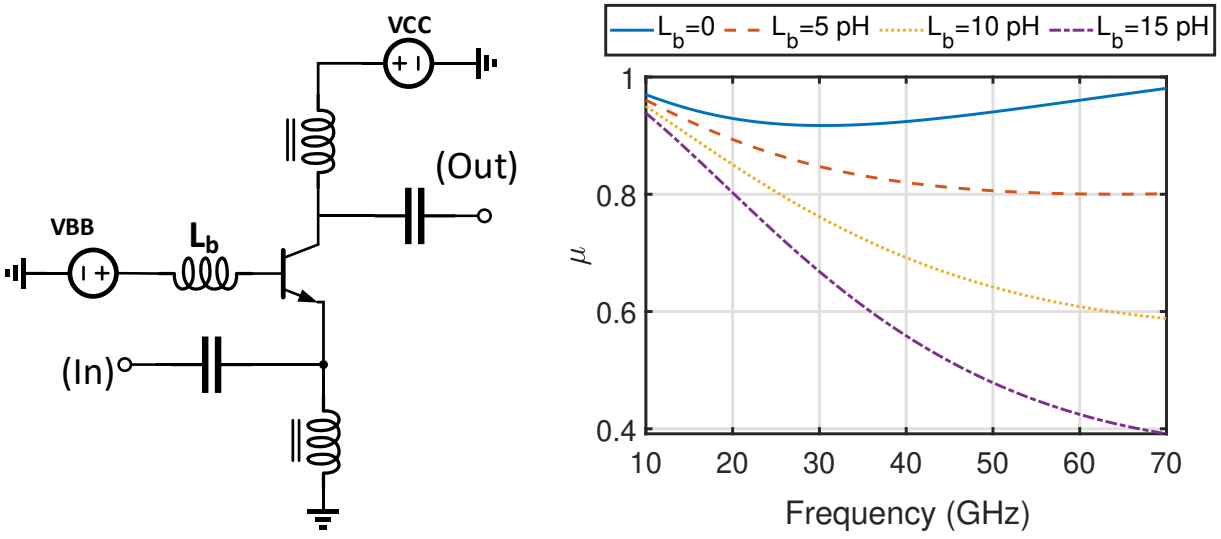


Figure 4.19: $3{\times}10\mu m$ HBT DC IV curves: (a) common emitter, (b) common-base biased by a current source, and (c) cascode structure. For all structures, VBB is swept from 0.75 V to 0.9 V with 50 mV step. (d) Simplified model of common-base PA. Norton equivalent circuit model has been used for the input excitation.

For a maximum collector voltage of 6 V with $V_k = 0.4$ V, the supply voltage becomes 2.3 V. The transistor peak current can be found from the output power for a class-F^{-1} PA

$$P_{Out} = \frac{(V_{Peak} - V_K) \times I_{Peak}}{2\pi}. \tag{4.11}$$

Therefore, the peak current becomes 56 mA. Since the current waveform of a class-F^{-1} PA is rectangular, the DC bias current at maximum power is 28 mA. A 30 μm HBT was chosen to provide this peak current. This results in 11 dB of power gain at 28 GHz. Three parallel 10 μm CBE-npn transistors were used to implement the 30 μm transistor. By extracting the output capacitance at zero bias current, the $C_{out} = 66\ fF$ is calculated. It is 15 fF of the output capacitance due to the interconnect parasitic capacitance.



(a) (b)

Figure 4.20: Effect of base parasitic inductance on stability. (a) Model schematic. (b) μ-stability factor for various base inductances.

In a common-base structure, a few pH of inductance at the base creates stability problems. Fig. 4.20 shows the μ factor for different base inductances. This problem becomes more severe at higher output powers where the base of the transistor can carry up to 40 mA. Therefore, the proposed designed utilizes a 1 pF metal-oxide-metal capacitor very close to the base contact (added at the M4 metal layer) and two 2 pF MiM capacitors are (added at both sides of the AM interconnect) as shown in Fig. 4.27(a). Therefore, we can have a low impedance RF decoupling at the base of the transistor. Two artificial quarter wavelength lines are also used to create a short circuit very close to the transistor base at the carrier frequency.

Following our choice of peak voltage and output power, the R_{opt} can be calculated from 4.3 for $\xi = 0$ to be 72 Ω

$$R_{opt} = 2\frac{(VCC - V_k)^2}{P_{out}} = 2\frac{2.3V - 0.4V}{50mW} = 72\ \Omega. \tag{4.12}$$

Based on these initial calculations, we performed load-pull simulation on the extracted transistor in the class-F^{-1} design space. For the extracted transistor, the optimum impedances

for the first and second harmonics are given by

$$Z_{fund} = 40 + j40\ \Omega \tag{4.13}$$

$$\Gamma_{2nd} = 0.9 \exp j0.5\pi. \tag{4.14}$$

For a 66 fF output capacitance, the optimum intrinsic impedance was found to be 80 Ω and the second harmonic impedance to be 380-j180 Ω. The difference in the optimum 80 Ω simulated R_{opt} and the theoretical 72 Ω is due to uncertainty in V_k and C_{bc} estimation. The intrinsic collector current and voltage are shown in Fig. 4.21 (a) and (b). These waveforms are similar to the class-F^{-1} waveforms in (4.2) where $\xi = 0$.

Fig. 4.21(c) shows the PAE, collector efficiency and transducer gain versus input power at 28 GHz. A peak PAE of 61 % has been achieved at OP_{1dB}. The small signal bias current is set to 6 mA. Fig. 4.21(d) shows the AM/AM and AM/PM results at the optimum load-pull point.The driver should provide a maximum of 7 dBm output power to saturate the output stage.

4.4.3 Output Matching Design

Given the optimum impedances for the first and second harmonics, an output matching network based on an inverting transformer was implemented. Fig. 4.22(a) shows the output matching schematic. A series transmission line is added to match the Z_1 =40+j10 Ω impedance, seen at the input of the transformer, to the required 40+j40 Ω impedance for the extracted transistor. The transformer notch frequency is set to $2f_0$ =56 GHz, resulting in j20 Ω. The output matching was designed to create an open circuit at the second harmonic at the intrinsic collector node of Q_3. Fig.4.23(a,b) show the targeted impedances and the response of the proposed output matching in the Smith-chart. Fig. 4.23(c) shows the loss of the output matching network. The designed output matching achieved 85 % efficiency and provided the targeted impedances obtained from load-pull simulation. Fig. 4.24 shows the intrinsic collector current and voltage waveforms for the implemented output matching network. The rectangular current and half sinusoidal voltage confirm the class-F^{-1} operation of this PA.

4.4.4 Driver Design

Based on the load-pull analysis presented in the previous section, the transistor in the output stage needs 6-7 dBm input power to get to the nonlinear region and achieve the

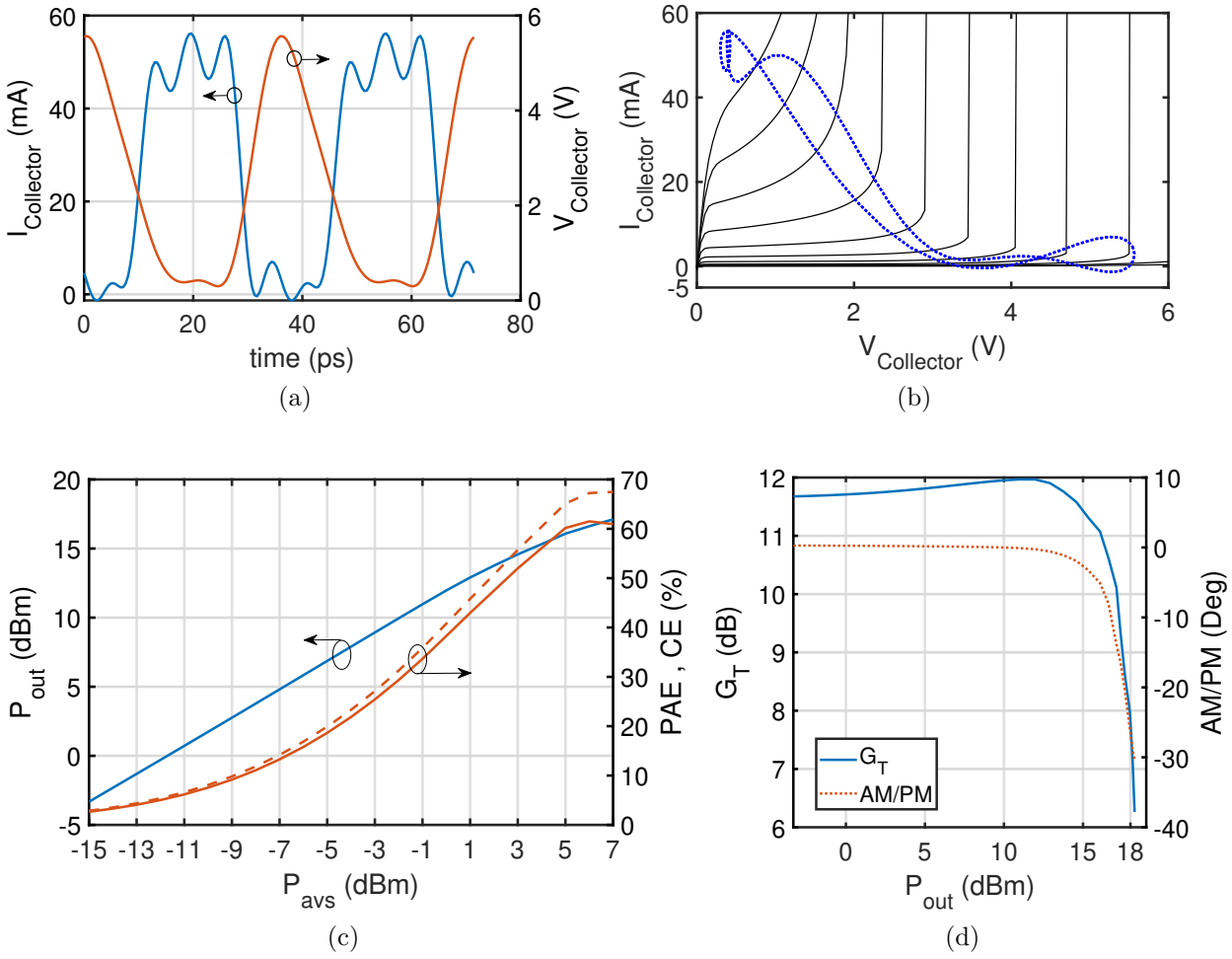
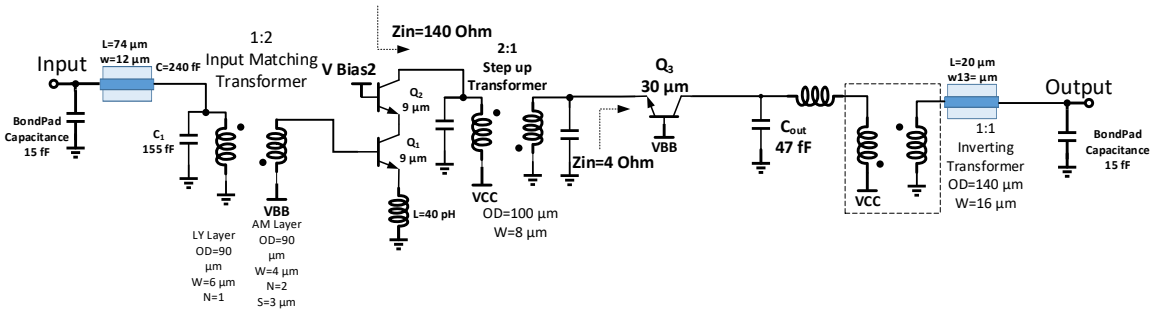
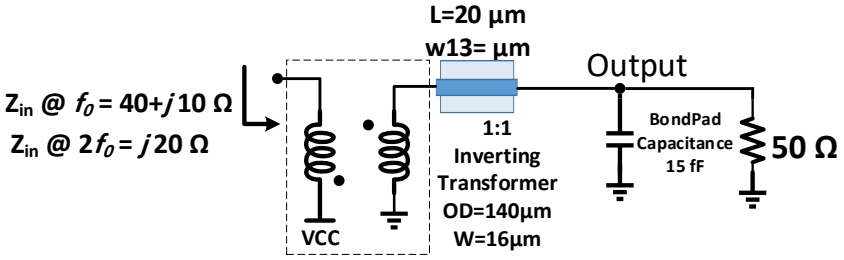


Figure 4.21: (a,b) Intrinsic collector voltage and current waveforms at OP_{1dB} at 28 GHz. (c) PAE, CE and P_{out} versus input power at optimum load-pull point for class-F^{-1} PA. (d) Amplitude and phase non-linearity responses at optimum load-pull point.

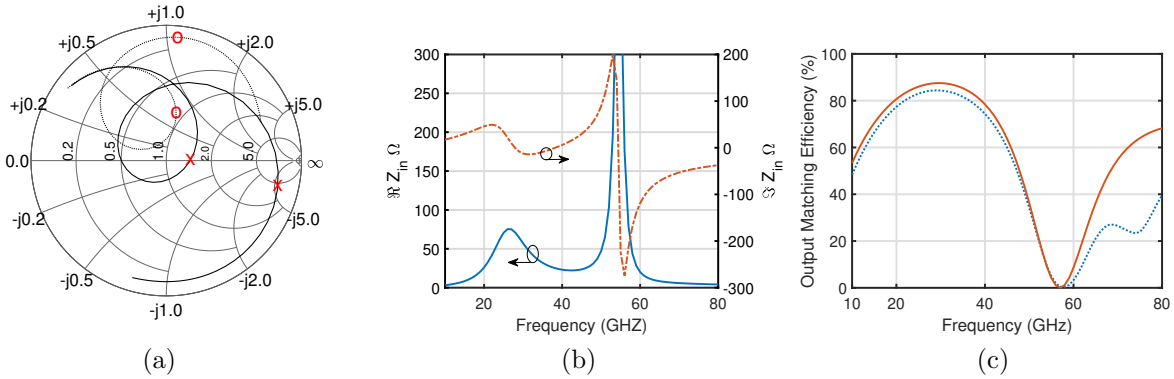


(a)



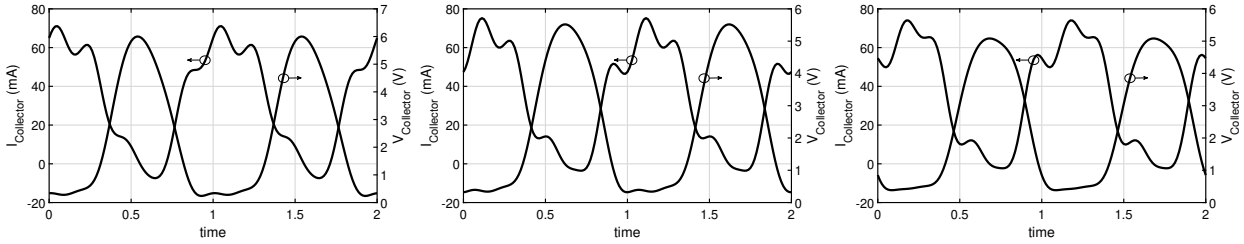
(b)

Figure 4.22: (a) Schematic diagram of two-stage PA with common-base output stage. (b) Input impedance seen from transformer.



(a) (b) (c)

Figure 4.23: Frequency response of designed output matching network. (a) Intrinsic (solid line) and extrinsic (dotted-line) impedances. (b) Intrinsic impedance showing fundamental and second harmonic impedances. (c) Output matching efficiency. The solid line is with ideal bias circuit and dotted line includes extra loss for the VCC decoupling.



(a) (b) (c)

Figure 4.24: Intrinsic collector current and voltage waveforms at: (a) 26 GHz, (b) 27 GHz, and (c) 28 GHz.

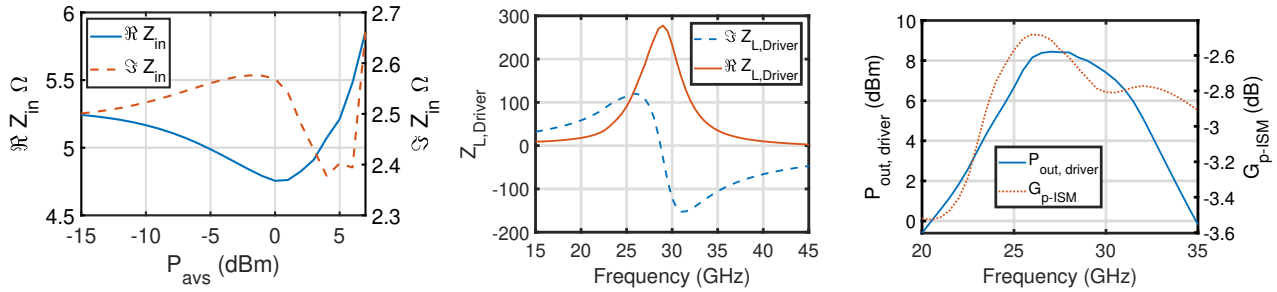
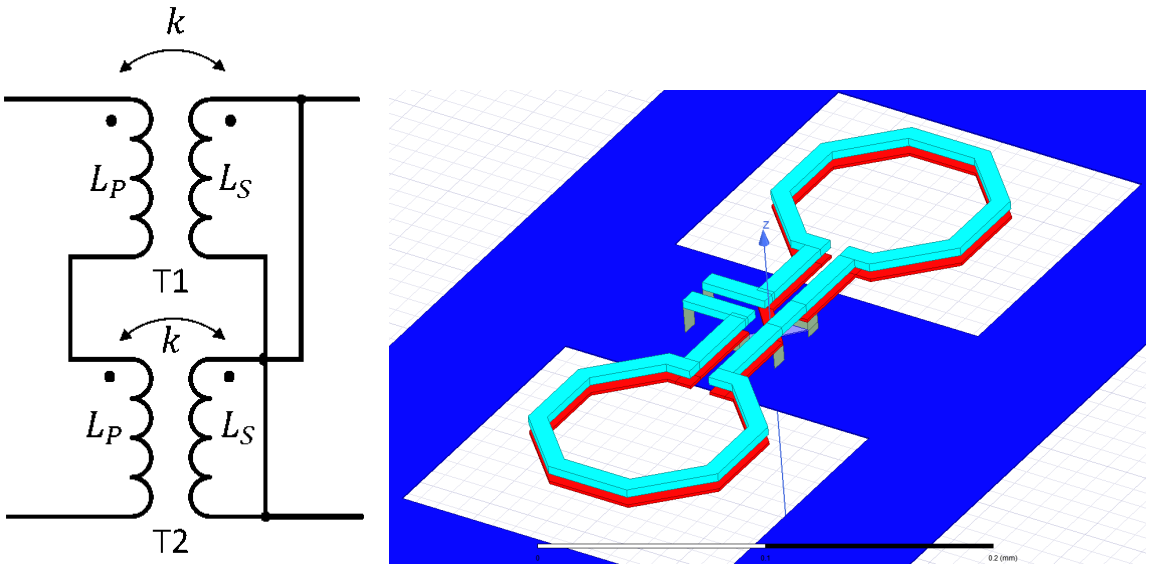


Figure 4.25: (a) Large signal impedance seen at emitter. (b) Realized impedance at driver transistor. (c) Output power of driver transistor and inter-stage matching insertion loss.

highest possible efficiency. The large signal input impedance of the emitter is shown in Fig.4.25(a). Therefore, the driver should drive a relatively low impedance of 5 Ω and deliver 7 dBm to it. Since the output stage has enough gain (11 dB), the efficiency of the driver can be compromised to achieve a higher gain. A cascode structure was chosen given its higher gain. Due to the high impedance transformation ratio needed for the driver, 3 dB loss was assumed for the inter-stage matching network. An eight-shaped 2:1 transformer was used to implement the inter-stage matching network. This type of transformer has a high coupling coefficient of 0.65. It consists of two 1:1 transformer where the primary is connected in series and the secondary is connected in parallel, as shown in Fig. 4.26. A 2:1 transformer with a high coupling coefficient helps to improve the impedance matching bandwidth and reduces the loss of the overall structure. The inter-turn capacitance increases the step-up transformation ratio. Fig. 4.22 shows the two-stage PA schematic and Fig. 4.25(b) shows the realized impedance for the cascode structure. The 5 Ω impedance of the emitter has increased to 250Ω at the collector of the $Q2$. Fig. 4.25(c) shows the power gain of the inter-stage matching. An insertion loss of 2.5 dB has been achieved using the proposed inter-stage matching network for an impedance matching of 5 Ω to 250 Ω.

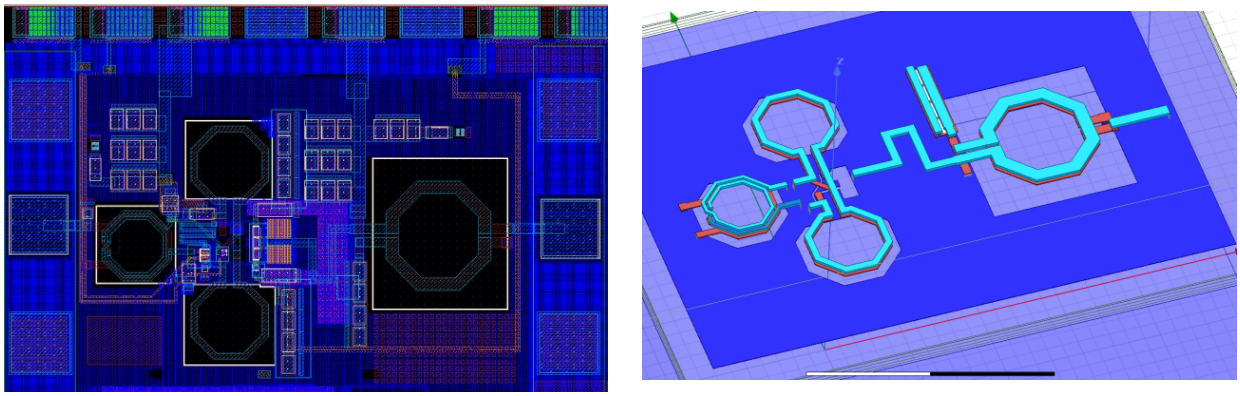
Fig. 4.22 shows the complete schematic for the common-base two stage PA, and Fig. 4.27 shows the submitted chip layout. The input matching is designed with a transformer to reduce the layout area. Fig. 4.28 (a) shows the small signal S-parameters, and Fig. 4.28 (b) shows the large signal parameters, of this PA.

As mentioned in previous chapters, the majority of antenna elements in a large phased-array antenna operate at deep back-off. Reducing the supply level is a simple and effective method to enhance the efficiency of the PAs. Fig. 4.29 shows the efficiency of the PAs



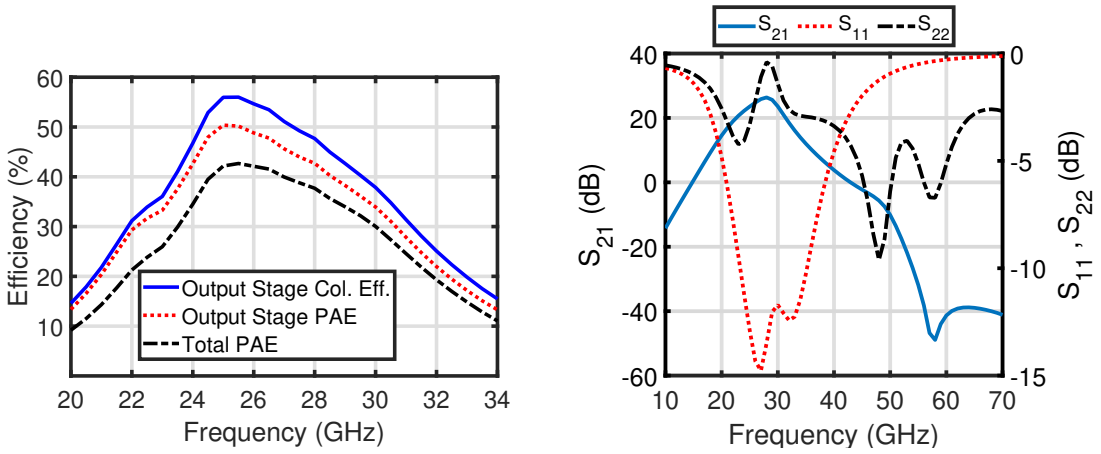
(a) (b)

Figure 4.26: Implemented 2:1 transformer as inter-stage matching network. $OD = 100$ μm and $w = 8$ μm (a) Simplified schematic model. (b) Three dimensional model in ANSYS-HFSS.



(a) (b)

Figure 4.27: (a) Submitted chip layout.(b) Three dimensional model of layout in ANSYS-HFSS.



(a) (b)

Figure 4.28: Frequency response of two-stage common-base PA: (a) small signal, and (b) large signal.

proposed in this chapter for different supply voltages. Both amplifiers were designed for a peak supply voltage of 2.4 V. The peak efficiency of a PA is proportional to $1-\frac{V_k}{VCC}$. In the PA based on a common-base structure, V_k =0.4 V. In the PA based on a cascode structure, V_k =1 V. The smaller V_k in the common-base PA results in higher peak-efficiency and also higher efficiency at 10 dB backoff compared to the cascode structure. In the common-base structure, reducing the supply voltage from 2.4 V to 1.2 V results in an efficiency improvement from 10 % to 24 %. However, in a cascode structure, the efficiency improves only from 8 % to 14 %. Therefore, a common-base PA has higher efficiency compared to a cascode version, and is a better choice for PAs to be used in beam-former chips.

4.5 Conclusion

In this chapter, harmonic-tuned PAs based on a 1:1 inverting transformer were presented. An inverting transformer was proposed as a compact output matching for harmonic-tuned PAs. The low-loss transmission and high rejection for the second harmonic in an inverting transformer result in higher peak efficiencies in Ka-band PAs. Two examples of PAs were presented to show the applicability of an inverting transformer. A high gain 12 dBm PA with a cascode-based output stage was presented for large phased-arrays. It achieved a peak efficiency of higher than 35 % from 24 to 30 GHz.

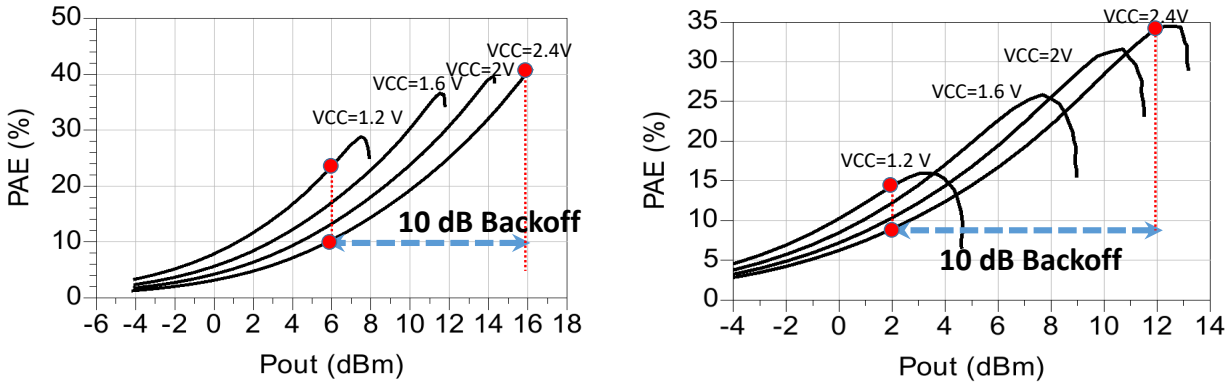


Figure 4.29: Comparison of proposed PA efficiencies versus output power at different supply voltages: (a) PA based on common-base structure, and (b) PA based on cascodestructure.

A PA based on a common-base structure was also demonstrated using an inverting transformer. The common-base structure has high isolation, high breakdown voltage, low V_k, and high peak efficiency. Furthermore, due to the large breakdown voltage, it is more robust to breakdown in the presence of a large RF signal and output mismatch. This makes it an ideal candidate for the output stage PA of a large phased-array antenna.

The main contributions of this chapter are as follows:

1- The full-wave behavior of a 1:1 inverting transformer was investigated and it was shown that an inverting transformer provides ultra-low loss in its transmission band and a wide-band rejection in its stop-band. These properties make it an ideal choice for a wide-band harmonic-tuned PA.

2- A 12 dBm 24-30 GHz high-gain two-stage continuous class-F^{-1} PA was implemented in 0.13 μm Bi-CMOS process and achieved a peak efficiency of 35 %. An inverting transformer was used for broadband impedance matching and second harmonic tuning. This work targeted architectures to be employed in 5G and SATCOM phased-array chips.

3- The common-base structure was investigated for the output stage of a linear or harmonic-tuned PA. A common-base PA has low V_k, high breakdown voltage, and high isolation. This results in higher peak efficiency compared to other output-stage structures. Using an inverting transformer in the output matching structure, a 16 dBm class F^{-1} PA with peak efficiency of 42 % was implemented. The proposed common-base PA demonstrated high efficiency at power back-off.

Chapter 5

A Low Loss Ka-Band Re-configurable Impedance Matching Network for Active Scan Impedance Compensation

In phased-array antennas, due to the finite mutual coupling between antenna elements, the input impedance of an antenna element in the array is different from that of an isolated antenna in free space [99, 100]. This so-called active scan impedance is a function of scan angle and the array's amplitude distribution. Fig. 5.1 represents an N-element array that is excited with N voltage sources with internal impedance of $R_0 = 50\ \Omega$. For the applied currents given in (5.1), the input voltages can be found by (5.2) where $[Z]_{N\times N}$ is the impedance matrix of the array and $[U]_{N\times N}$ is a unitary matrix.

$$I_m = I(m_1, n_1) = I_0 \exp(-jk_0(n_1 - 1)d_x \sin\theta_i \cos\phi_i) \times \exp(-jk_0(m_1 - 1)d_y \sin\theta_i \sin\phi_i) \tag{5.1}$$

$$[V_i]_{N\times 1} = [[Z]_{N\times N} + Z_0[U]_{N\times N}]\,[I_{in}]_{N\times 1} \tag{5.2}$$

Therefore, the active scan impedance of each antenna element can be calculated by

$$Z_{in} = Z_{i,i} + \sum_{n=1,\neq i}^{N^2} Z_{n,i}\frac{I_n}{I_i}. \tag{5.3}$$

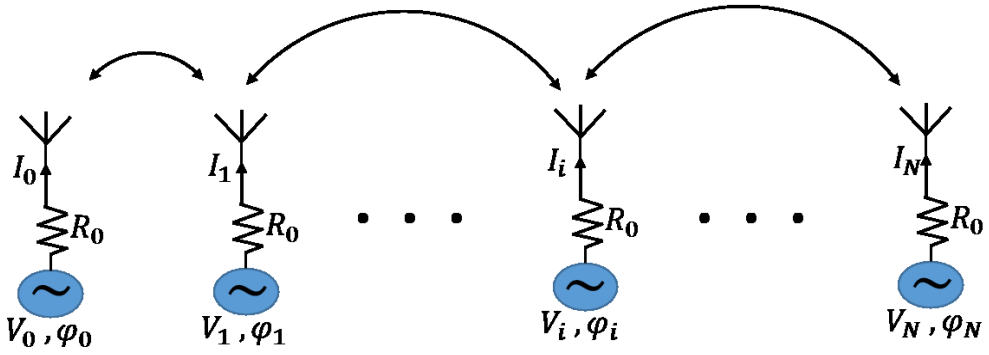


Figure 5.1: Active phased-array antenna with coupling.

The active input impedance defined in (5.3) is a function of other elements' excitation. For a 3×3 uniformly excited array, (5.3) simplifies to

$$Z_{in} = Z_{11} + 2Z_{d1}\cos(\beta_X + \beta_Y) + 2Z_{d2}\cos(\beta_X - \beta_Y) + 2Z_H\cos\beta_Y + 2Z_V\cos\beta_X \tag{5.4}$$

$$\begin{aligned} \beta_X &= -k_0 d\sin\theta\cos\phi \\ \beta_Y &= -k_0 d\sin\theta\sin\phi \end{aligned} \tag{5.5}$$

where Z_V, Z_H, Z_{d1} and Z_{d2} are the mutual impedances of the centre element with its adjacent elements in the same column, row and diagonals respectively. For two special cases of $\phi = 0$ and $\phi = \pi/2$ we have

$$\phi = 0 \rightarrow Z_{in} = Z_{11} + 2Z_H + (4Z_{d1} + 2Z_V)\cos(\pi\sin\theta) \tag{5.6}$$

$$\phi = \frac{\pi}{2} \rightarrow Z_{in} = Z_{11} + 2Z_V + (4Z_{d1} + 2Z_H)\cos(\pi\sin\theta) \tag{5.7}$$

As observed in (5.6), for small θ the $\cos(\pi\sin\theta)$ term is almost constant and the active impedance does not change substantially for small elevation scan angles. However, for large scan angles, the active impedance can cause strong impedance mismatch. Fig. 5.2 shows the active scan reflection coefficient of an antenna element in an infinite array [79]. The antenna element is designed for a large phased-array antenna [101]. The active refection coefficient reaches up to −5 dB for scan angles of higher than 60°.

5.1 Active Impedance Compensation Techniques

Depending on the level of mutual coupling between the antenna elements, and the size of the array, the active impedance can vary significantly over the scan angle. In some cases,

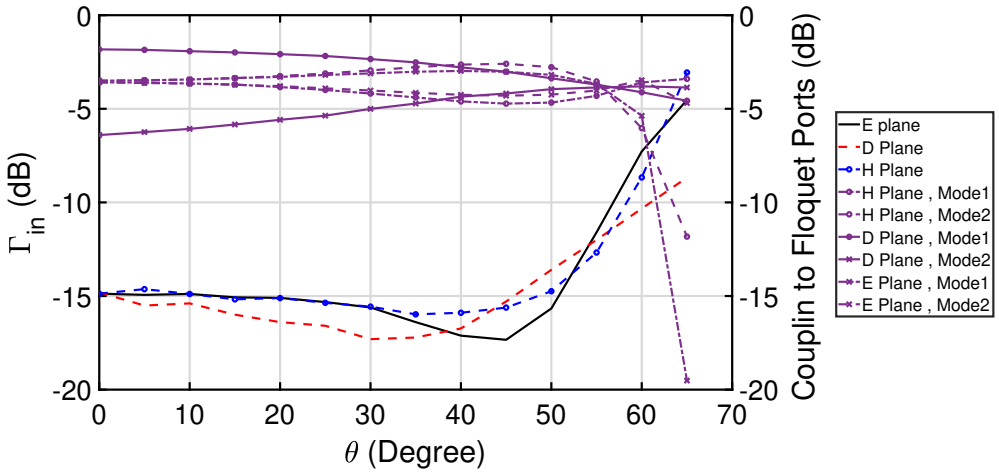


Figure 5.2: Reflection coefficient of antenna element in infinite array for different scan angles at 29.75 GHz.

the scan impedance becomes completely reactive, rendering the array completely blind for some scan angles [102]. For planar patch antennas, this phenomenon is more pronounced in elevation scan angles of larger than 50°. This change in impedance can directly affect the output power and efficiency of the PA in the transmitter array and the noise figure of the low noise amplifier at the receiver [103]. The radiated power of each antenna element also reduces due to coupling losses.

In this section, we review coupling reduction and impedance compensation methods reported in the literature, and investigate their applicability to large phased-array antennas. There are two general trends in the literature to solve antenna input impedance variation: passive methods and active methods.

Passive Methods

Two well-studied techniques used to improve isolation between antenna elements are i) to reduce the EM interaction between the antenna elements (without changing the feed line) [104], and ii) to provide a cancellation path in the antenna feed to cancel the mutual coupling [105]. Both of these approaches are usually narrow-band and add further complexities to the antenna package. While these techniques improve the impedance matching of the antenna over the scan angle, they do so at the cost of some additional loss. The mutual coupling between two adjacent antennas mainly consists of coupling through the air, the

antenna substrate, and the antenna ground [106]. Several methods have been proposed in the literature to minimize each mutual coupling component. In [106], by optimizing the antenna element, truncating the antenna substrate and ground, and using decoupling metal walls as a shield between the elements, isolation of up to 40 dB and elevation scan angle of up to 60° have been reported. The use of a shielding ring and via fence around each antenna element is also reported in [107] for a 28 GHz phased-array, but it reports a very small isolation improvement. Shielding the antenna elements by putting them in a cavity is another effective technique, reported by [108, 109]. Introducing bandgap structures or using a defected ground plane between the antenna elements have also been used to suppress coupling, through the substrate and ground respectively [110–113]. However, there is no report of applying these decoupling techniques for a phased-array antenna due to the limited inter-element spacing in mm-wave phased-arrays.

Non-structural approaches, such as reducing the coupling by providing a cancellation signal with the proper phase and amplitude have also been reported [105, 114, 115]. These techniques usually suffer from relatively narrow bandwidth and add more loss and complexity to the feeding network of the array. In [105], a linear array that can scan the beam up to 66 degrees is implemented using this technique with 3% bandwidth.

Active Methods

The second general approach is to make the amplifier re-configurable so that it can adapt itself to the new impedance. This can be accomplished either by making the output matching re-configurable [**?**, 23] or by using active load-pulling of the amplifier through an amplitude- and phase-controlled auxiliary amplifier [116, 117]. However, these methods increase the layout area significantly, are not well suited for modular structures, and they increase the cost of the chip. Furthermore, on-chip re-configurable output matching has high loss [23] and there is not much improvement in the output power of the amplifier.

The approach taken in this thesis toward solving this problem consists of applying mutual coupling reduction at both the circuit and antenna levels. At the antenna side, all the techniques above should be practiced to minimize the mutual coupling between the elements. In addition, and what constitutes the focus on this chapter, at the circuit level a low-loss off-chip re-configurable matching network should be implemented. The proposed approach will be explained in the next section.

5.2 A Low-Cost Ka-Band Tuner for Re-configurable Output Matching Networks

As explained in the previous section, in active antenna arrays the antenna impedance varies by the scan angle due to the active loading effect of adjacent antenna elements [82]. Therefore, the PA that drives the antenna element observes a variable impedance. This impedance variation can result in output power degradation or oscillation. In large mm-wave phased-arrays, the antenna impedance can increase up to -5 dB [79]. By employing a re-configurable output matching network (tuner) between the PA and the antenna, we can compensate for this impedance variation and avoid possible damage from a large Voltage Standing-Wave Ratio (VSWR) at the output of the amplifier.

Several works have reported the development of compact tuners [118–120] but they were all limited to RF frequencies. In the current work, a low-cost solution for a Ka-band tuner is proposed. We use a π-network with three tunable transmission lines to cover the entire Smith-chart over a wide bandwidth. The proposed system can potentially cover the Smith-chart with $|\Gamma_L| < 0.8$.

5.2.1 Proposed Tuner

Figure 5.3 shows the proposed tuner. A double-stub matching network is used to maximize the transformation ratio. By changing the electrical length of TL1 and TL3, we can transform the 50 Ω load to any desired point in the Smith-chart. The TL2 in Fig. 5.3 is also tunable to cover a wider area of the Smith-chart at a wider bandwidth.

The tunable line is made of a Grounded Co-Planar Waveguide (GCPW) line which is loaded with a high permittivity dielectric slab. The effective electrical length of each stub changes by changing the gap between the line and the slab [121].

5.2.2 Tunable-Line Characteristic

Figure 5.4 shows a GCPW line with a dielectric slab with $\epsilon_r = 100$ placed on top of it. The bottom surface of the slab operates as a Perfect Magnetic Conductor (PMC) wall; changing the gap (Δz) results in a change in the propagation constant of the transmission line. This structure is comprehensively analyzed in [121] and employed as a low-loss phase shifter.

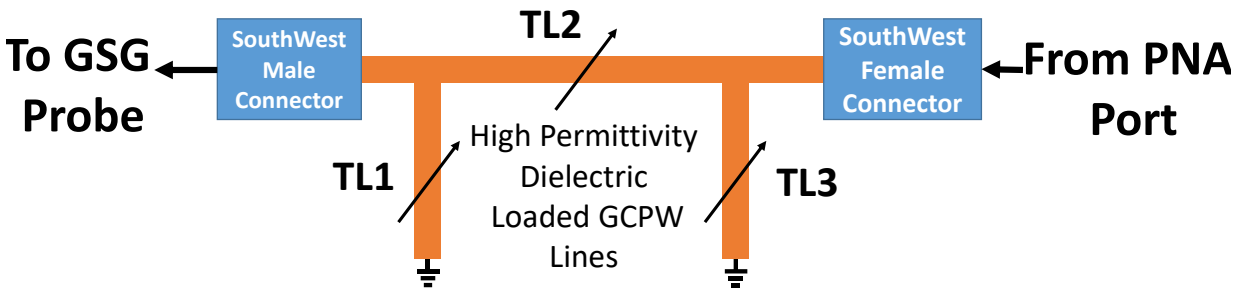
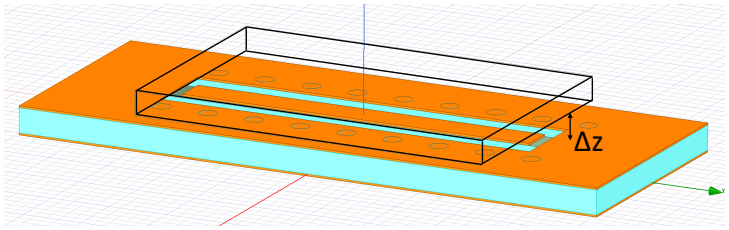
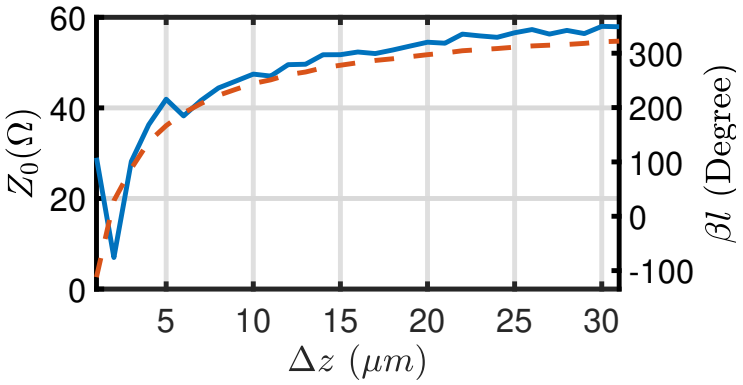


Figure 5.3: Conceptual diagram of proposed tuner.

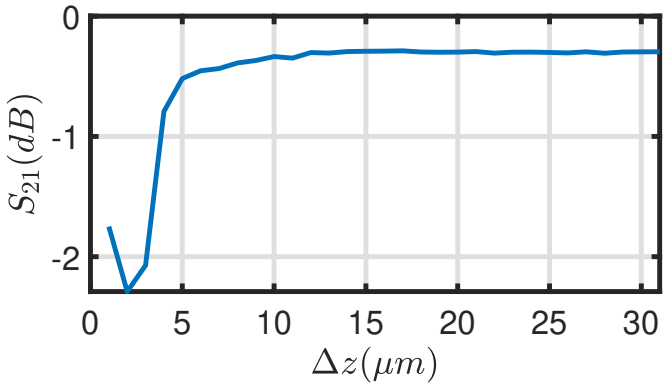
Figure 5.4(a) shows the structure as analyzed in ANSYS-HFSS and Fig. 5.4(b) shows the characteristic impedance and electrical length variations for $\Delta z = 1\mu m$ to $\Delta z = 30$ μm at 30 GHz. It can be seen that for the gap variation from 5 μm to 30 μm, the electrical length of the line varies from 160° to 322° and the Z_0 of the line remains relatively constant. Fig. 5.4(c) shows the insertion loss of the this 7 mm line. The S_{21} is -0.5 dB for the gap from 5 μm to 30 μm at 30 GHz.



(a)



(b)



(c)

Figure 5.4: Structure of proposed tunable line. (a) A 50 Ω 7mm GCPW line loaded with a high permittivity ($\epsilon_r = 100$) slab in ANSYS HFSS. (b) Electrical length and characteristic impedance of the line over various gap heights. (c) S_{21} of the line for various gap heights.

5.2.3 Tunable Double-Stub Matching Circuit

A double-stub matching circuit can ideally transform a 50 Ω load into any desired point in the Smith-chart. This can be achieved by changing the electrical length of the stubs. In this work, two 6 mm long grounded stubs were used. The stubs were loaded stubs with high permittivity dielectric with $\epsilon_r = 100$ and the gap for each slab varied from 5 μm to 30 μm. The transmission line substrate was RO4350 with $\epsilon_r = 6.15$ and $\tan\delta = 0.003$. Fig. 5.5 (a) shows the response at 30 GHz when TL1 and TL3 are tunable and TL2 is a straight unloaded GCPW line. We can see that the coverage of the Smith-chart, in this case, is limited and there are certain blind spots. This is due to a fundamental problem with double-stub tuners: all the loads cannot be matched for a fixed stub spacing. This problem can be solved by using a tunable line for TL2.

In order to maximize the coverage, the structure in Fig. 5.3 was simulated with a tunable TL2. Fig. 5.5 (b), (c) and, (d) show the estimated reflection coefficient at 20, 30 and, 40 GHz respectively. Broad Smith-chart coverage of $|\Gamma_{in}| < 0.8$ is achieved over a wide bandwidth. The substrate and ohmic loss of the line limit the maximum achievable reflection coefficient.

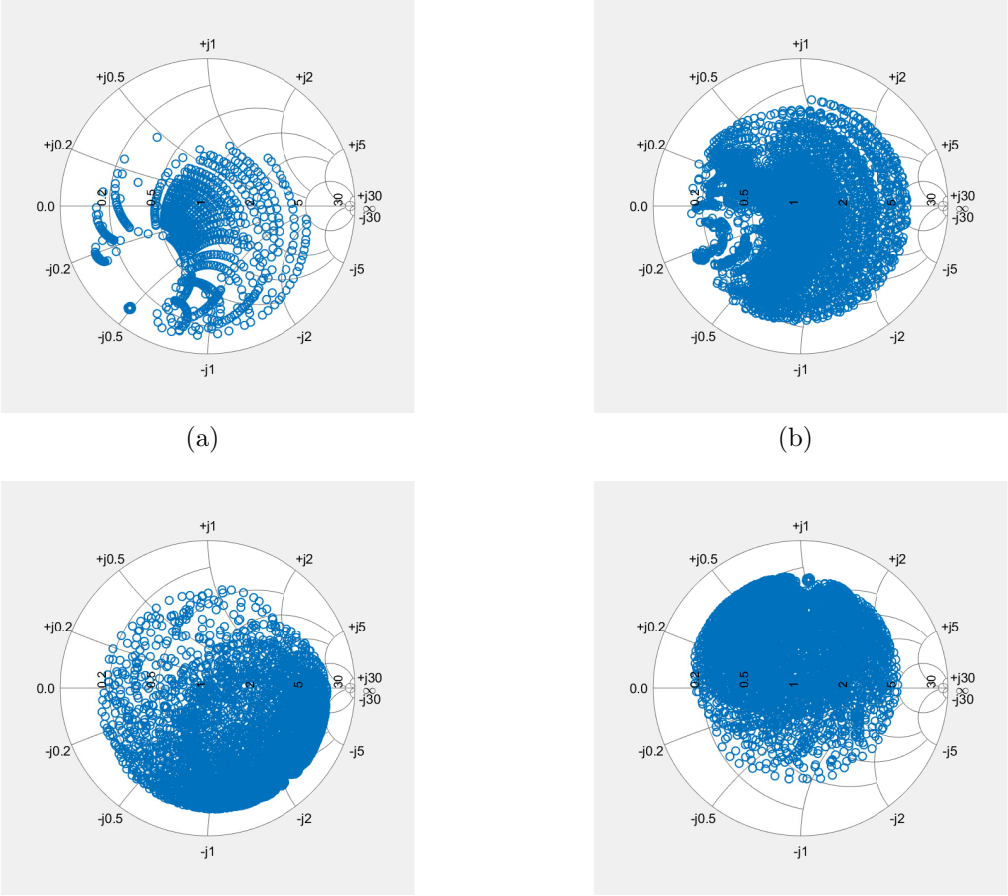


Figure 5.5: Simulation results for structure outlined in Fig. 5.3 (connector and GSG probe loss not included). Impedance coverage of Smith-chart when (a) TL1 and TL3 are tunable and TL2 is a constant 50 Ω line, and when TL1,2,3 are tunable at (b) 20 GHz, (c) 30 GHz, and (d) 40 GHz.

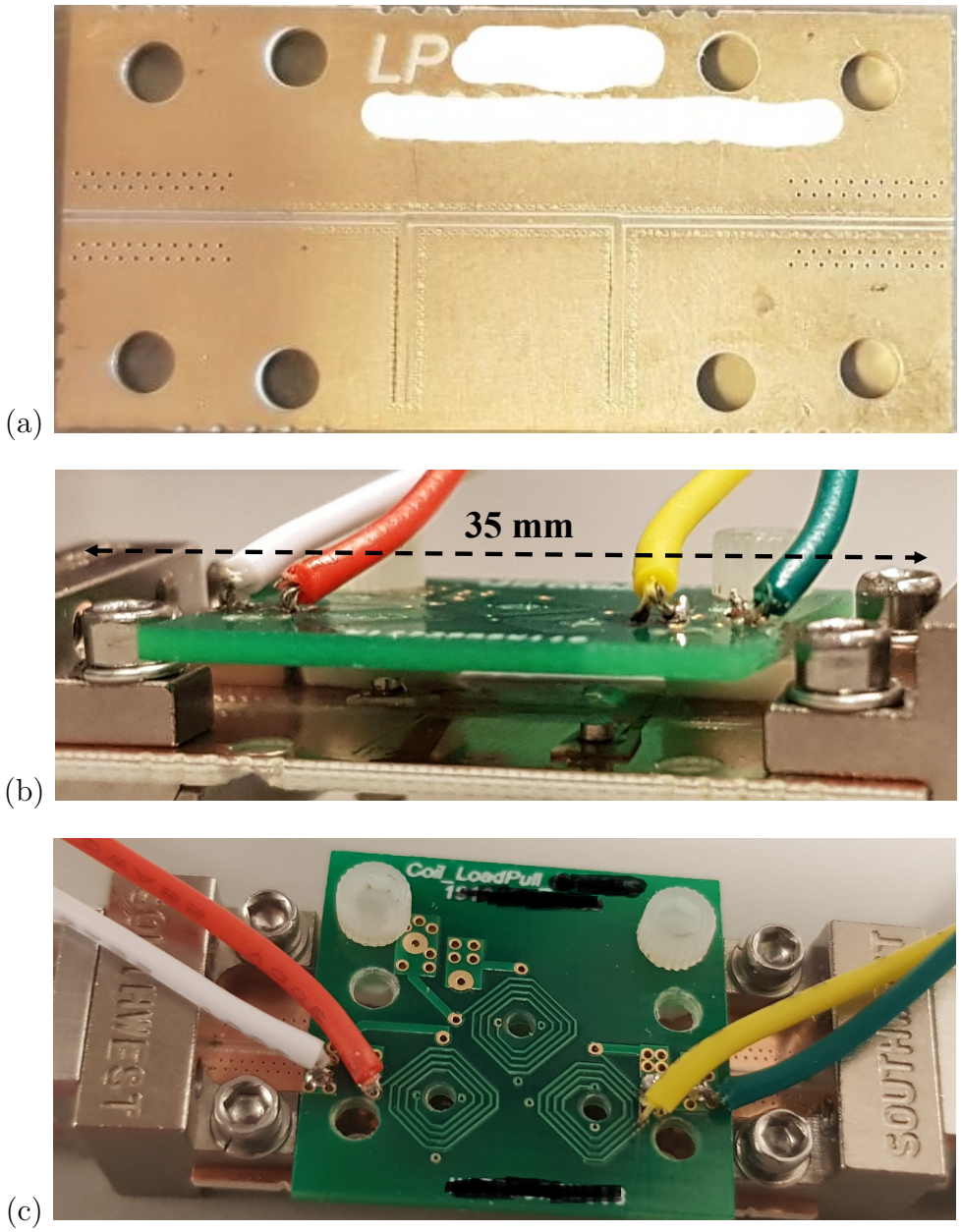


Figure 5.6: Proposed compact Ka-Band tuner. (a) Double-stub Grounded-CPW line. (b) Actuation mechanism (the right dielectric sits on the line; the left dielectric is raised up 4 mm). (c) Coils for magnetic actuation.

5.2.4 Measurement Results

To verify the feasibility of the proposed tuner, we fabricated a double-stub matching network on the RO4360 substrate as shown in Fig. 5.6 (a). The whole structure has a length of 35 mm and can directly connect to the GSG probe and operate as a tuner. A magnetic actuator is used to move the high permittivity dielectric up and down as shown in Fig. 5.6 (b) and (c). By changing the current in the coils, the distance of the dielectric from the GCPW-line surface can be adjusted. Originally, the plan was to have three actuators (one for each of the three dielectric slabs) but unfortunately, the actuator could not be installed for the middle line (TL2). Therefore, it was possible to test the tuner with only two tunable lines. A two-part test was conducted on the fabricated tuner and the bias current was changed for the actuators. Fig. 5.7 shows the measured S_{11} at various frequencies. A maximum $|\Gamma|$ of 0.71 is measured at 24.6 GHz, as shown in Fig. 5.7 (a). The $|\Gamma| = 0.35$ is fully covered at 35 GHz as illustrated in Fig. 5.7 (c), and a resistive impedance of 15 Ω to 250 Ω is achieved at 40 GHz.

Our coverage was limited to a $|\Gamma|$ of 0.7. We could not achieve the same coverage as in simulation because of the higher loss and the restriction of using only two tunable lines. The higher loss of the conductor was due to surface roughness, and alignment inaccuracy when moving the dielectrics limited our coverage further. However, the main purpose of this work was to demonstrate the concept of using a dielectric-loaded GCPW line as a tuner. Achieving more coverage requires a GCPW-line with a lower-loss substrate, a conductor with less surface roughness, and a carefully optimized design. The proposed tuner can be used for preliminary mismatch tests of a phased-array transmitter chip.

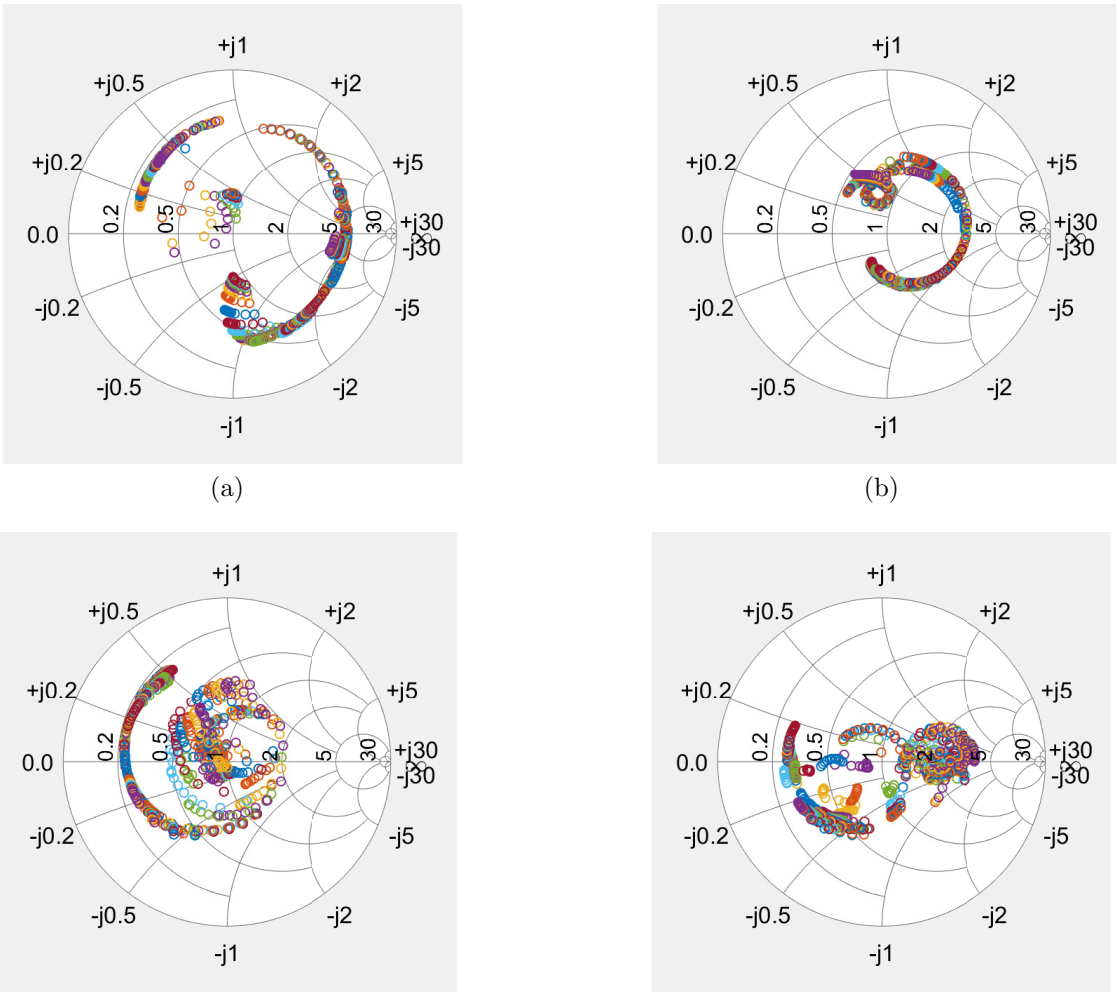
5.3 Using the Proposed Tuner as a Re-configurable Output Matching Network

The proposed tuner has the potential to be used as a re-configurable output matching network. However, the current circuit implementation can be used only for linear arrays where there is enough space between the PA and the antenna. To implement this technique in a two-dimensional 30 GHz array, a few issues would need to be solved. The antenna spacing is 5 mm and the dimensions of the matching circuit should be approximately less than $1mm \times 1mm$ to be able to fit between the phased-array chip and the antenna feed. This would require further research and the exploration of other technologies to achieve such a level of integration.

Table 5.1
Measured insertion loss and impedance variation compensation of fabricated tuner at 30 GHz.

Z Antenna	Measured Tuner IL	Mismatch Loss	Compensated S11 seen by the chip
50 Ω	-1.2 dB	0 dB	-Inf
150 Ω	-2.2 dB	-1.2 dB	-14 dB
150+j100 Ω	-2.7 dB	-2.2 dB	-20 dB

However, to demonstrate the potential of this technique for compensating the impedance variation, the measured S-parameters of the tuner were applied for a few impedance points to investigate the measured insertion loss and matching. Table 5.1 summarizes the results. Our tuner has an extra loss of 1.2 dB for a 50 Ω load. Despite the extra loss, the considered impedance mismatches are compensated to below -14 dB for the studied cases.



(a) (b)

(c) (d)

Figure 5.7: Measured reflection coefficient for different dielectric states: (a) 26.4 GHz, (b) 30 GHz, (c) 35 GHz, and (d) 40 GHz.

5.4 Conclusion

A low-cost and compact tuner made of a double-stub matching network with three tunable lines was presented. The proposed tuner can potentially cover the Smith-chart with $|\Gamma < 0.8$ over a wide bandwidth. Reflection coefficients of 0.7 (VSWR=5.6) and 0.6 (VSWR=4) were measured at 24.6 GHz and 40 GHz, respectively. The proposed tuner can be used for testing a phased-array transmitter chip under impedance mismatch conditions. The proposed structure was designed to connect directly to a GSG probe. This omits the extra 3-4 dB cable loss of existing load-pull tuner systems.

The main contributions of the work detailed in this chapter are as follows:

1- A low-loss Ka-band tuner with the potential to be integrated into the feed network of an antenna element and compensate for the antenna active-impedance variation was developed.

2- The proposed tuner is a compact solution for a passive load-pull tuner system. This system can be used in characterizing a mm-wave PA under impedance mismatch conditions.

Chapter 6

Conclusion and Future Works

With the advance of silicon technology and further progress in packaging and multi-layer PCB techniques, active phased arrays are going to be a feasible solution in near-future communication and radar technologies. SATCOM, 5G, radar, and mm-wave sensing are potential examples of this flourishing technology.

In this thesis, power-efficient solutions for integrated phased array transmitters are proposed. Large phased array antennas for Ka-band SATCOM and 5G are the main application for these solutions. A large phased array antenna consists of hundreds to thousands of antenna elements, requiring hundreds to thousands of active chips with small to medium output power. This technology brings opportunities and challenges in the large scale integration of active RF components. Among these RF components, power amplifiers are the most power-hungry element in a phased array chip. This thesis's focus is mostly on Ka-band high-efficiency power amplifiers and proposes novel structures for harmonic-tuned power amplifiers that achieve high peak efficiency with a compact layout form factor.

The main contributions of this thesis that have been verified either by simulation or experiment are as follows:

1- A power-efficient beam-former chip that operates from 27 to 31 GHz with an output power of 11 dBm and total efficiency of 25%. The implemented chip was developed for large phased array terminals for GEO orbit satellite communication. A phase shift range of 400◦ and amplitude variation of 16 dB was achieved with the goal of minimum phase-amplitude correlation and a simplified calibration routine. This chip is the RF-core of an eight-channel Ka-band beam-former chip that is currently under development in the CIARS group. This work achieved the highest efficiency among the reported SATCOM chips at the time of this publication.

2- A broadband harmonic-tuned power amplifier with an output power of 12 dBm and peak-efficiency of 30% from 25 to 39 GHz. This proposed PA uses a non-inverting transformer and its parasitic capacitance for matching the fundamental harmonic and controlling the phase of second harmonic impedance. The output matching also operates as an ESD protection. Furthermore, as an extension of this work, the properties of a 1:1 transformer when implemented as an inverting transformer have been studied. The results show that an inverting transformer has a very small loss in its transmission response and very high rejection in its rejection-band. We used an inverting transformer in the output matching network of two power amplifiers to show its application. The first example was a 12 dBm PA operating from 24 to 30 GHz with a peak-efficiency of higher than 35%. The second example was a common-base PA with an output power of 16 dBm. The common-base PA has unique properties that are very beneficial in low to medium output power PAs: high peak-efficiency and higher efficiency at 10 dB back-off compared to other linear amplifier structures. These results are mainly for its lower V_k and its high breakdown voltage. To the best of author's knowledge, this work is the first harmonic-tuned PA implemented using common-base structure.

The common property of all these PAs is the small form factor that is essential for large scale integration of these amplifiers. The focus of this work was in developing high efficiency PAs with low output powers with a compact layout and wide bandwidth. The proposed novel inverting transformer based PA, enables wide-band harmonic tuning.

3- A low cost and potentially low loss re-configurable tuner is proposed, to be used as a passive mm-wave tuner and re-configurable output matching network. By implementing a double-stub matching network with tunable lines developed in CIARS, we demonstrated Smith-Chart coverage of up to $|\Gamma_L| = 0.6$. The proposed tuner, achieves one of the smallest form factors in the literature and can potentially be used in on-wafer load-pull tuners.

6.1 Future Work

Active phased arrays are an emerging technology that is rapidly progressing, and we may see its widespread deployment in the near future. However, a few challenges facing this technology still need to be addressed. Thermal dissipation for these large arrays remains a challenge and needs further innovations in multiple fields. In this thesis, we have only been able to address the development of power amplifiers with high peak-efficiency. Due to limited research time, we could not investigate efficiency enhancement techniques deeply. It should be mentioned that to the best of the author's knowledge, the reported PAs with enhanced back-off efficiency like Doherty [122, 123] or Outphasing [124] architectures have

led to marginal improvements in the overall efficiency but added a lot of complexity and layout overhead that makes the integration of these PAs in a multi-output beam-former chip a challenge. However, there are still opportunities to enhance the efficiency of an antenna array as follows:

1- The output stage transistor is usually large, and in a phased array antenna where the majority of the elements operate in back-off, we can implement the output stage PA with a multi-segment transistor. Therefore, we can change the peak current of the transistor based on the required peak output power. Doing so results in an adaptive bias current based on the output power and enhances the efficiency in low output powers. Furthermore, in large arrays where the edge elements operate at deep back-off, we can provide a higher impedance by adding extra impedance matching at the PCB. However, implementing these techniques needs a relatively accurate flip-chip package model.

2- In SATCOM phased array communication, the bandwidth of the signal is approximately 6 MHz, but this signal can be anywhere in the spectrum from 27 to 30 GHz. Furthermore, as demonstrated in Chapter 4, common-base PAs maintain their peak-efficiency even at lower supply voltages. The narrow signal bandwidth and the high peak-efficiency of common-base PAs make envelope tracking architecture a feasible approach in enhancing the efficiency of mm-wave PAs for SATCOM. The reported supply modulators have a tracking bandwidth of up to 100 MHz, which is higher than the required tracking bandwidth ($5 \times BW_{signal}$) of SATCOM modulation signals.

3- This thesis has introduced and demonstrated a narrow-band RF front-end specifically designed for Ka-Band SATCOM. By designing broadband phase shifters and variable gain amplifiers and using the proposed broadband power amplifiers, we can use one beam-former chip for different bands, thereby significantly reducing costs.

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