Silicon Nanowire Networks as a Printable Semiconductor

by

Tianqi Li

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Printed flexible electronics is gaining in popularity and is used in applications such as flexible displays, wearable medical devices and the internet of things [1]. Compared to traditional silicon device manufacturing technologies, printed flexible electronics overcomes the limitations of mechanical rigidity, as well as imposes advantages such as simplified manufacturing requirements, less material consumption, lower fabrication costs, and lighter-weight devices. Satisfactory printable dielectrics and conductors exist, but printable semiconductors remain a challenge. Most often printable semiconductors are organic based, but these materials suffer from low mobility and short lifetime. Inorganic materials have much better electronic properties and higher stability but are typically not printable. Nanowires, which can be synthesized as single crystals on one substrate then dispersed in an ink, provides a solution to print inorganic semiconductors, including silicon. In this thesis, solution-processed silicon nanowire networks are evaluated for printed electronics. A nanowire network is a mesh of randomly oriented nanowires, for which no alignment is needed and thus fabrication is simple. Since nanowires are much longer than nanoparticles, there are less junctions in a nanowire network compared to a nanoparticle film, ideally resulting in less scattering and better electrical performance.

To fabricate silicon nanowire networks, the first step is to synthesize silicon nanowires and metal-assisted chemical etching was chosen for its solution compatibility, high quality nanowires, simplicity and cost effectiveness [2]. Various parameters in metal deposition and chemical etching were explored and silicon nanowires with homogeneous diameters of 100 nm and lengths of up to 62 μm were successfully obtained. Dispersion of these silicon

nanowires in a solution was examined next through ultrasonication. To minimize nanowire agglomeration, a simple method was demonstrated for the first time whereby the nanowires on the growth substrate were transferred directly to the dispersion solvent from the etching solution. This avoids the capillary forces at the liquid-vapor interface during drying. Different dispersing factors were individually tested to maximize the length and minimize the agglomeration of silicon nanowires in solution.

Three printing techniques were explored to print networks of silicon nanowires: drop casting, rod coating and transfer printing through vacuum filtration and membrane dissolution. This represents the first time silicon nanowire networks were rod coated and this method was found to be a feasible approach to print silicon nanowires that is compatible with the large-scale roll-to-roll printing needs in industry. However, one limitation was observed, which is the need of formulating a higher concentration silicon nanowire ink while maintaining minimal agglomeration. After printing silicon nanowires networks, they are further processed and incorporated into a thin film transistor (TFT) for electrical characterization. Annealing treatments on the nanowire networks at different temperatures were explored, with 400 ˚C for 1 min yielding the best electrical performance. An I_{ON}/I_{OFF} ratio of ~10^5 was obtained for the transistors. Overall, the synthesis and printing of the nanowires was successful and compatible with the needs of printed, flexible electronics. The field effect mobility of the nanowire networks was poor however, which is attributed to the oxide existing at the nanowire junctions and between the nanowires and the metal contact as well. Strategies to control and remove this oxide is outlined and discussed as future work.

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Dedication

I hereby dedicate this thesis to my parents and my fiancé.

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Chapter 1
Introduction

1.1 Printed Flexible Electronics

The fabrication of conventional silicon electronics involves hundreds of complicated steps including lithography, etching and packaging, some of which require vacuum, high temperatures and very expensive equipment. Furthermore, the electronics are deposited on silicon wafers which are rigid and thus not appropriate for up-and-coming large-area mechanically flexible devices [1]. To address these issues, the area of printed flexible electronics has emerged where devices are instead manufactured by printing techniques on flexible substrates [1]. The term 'Printed flexible electronics' can be defined in two parts. 'Printed' means that functional ink (usually demonstrating conductive, semiconductive, dielectric or optoelectronic properties) are simply printed or deposited in an additive fashion usually using high-throughput continuous methods that are compatible with so-called roll-to-roll manufacturing processes. Deposition can be low-cost, take place in ambient atmosphere, occur at low temperatures to be compatible with flexible substrates, and be done over large areas. Therefore, compared to traditional silicon integrated circuit manufacturing, the manufacturing of printed flexible electronics is simpler, cheaper, more adaptable and consumes less material [3]. 'Flexible' means the electronics are made on bendable and sometimes even stretchable substrates such as plastic [4], paper [5], textile [6] and thin sheet of metal or glass [1]. Application areas of printed, flexible electronics include flexible displays [7], smart packaging [8], robotics [9], wearable electronics [10], biomedical sensing [11] and healthcare

monitoring [12]. Printed flexible electronics is an emerging and developing field [3] that has attracted increasing research interest in the last decade [1].

Various printing techniques for flexible electronics have been introduced. They can be classified into two broad categories: contact and non-contact printing. A typical contact printing process involves physical contact between a pre-patterned surface and the receiving substrate to fulfill the transfer of the functional ink on the specific targeted areas [3]. Popular techniques under the contact printing category include gravure printing [13], gravure-offset printing [14], flexographic printing [15] and micro-contact printing [16]. In non-contact printing, the ink solution is usually sprayed through a nozzle or dispensed from the openings of a module above the substrate and includes techniques such as inkjet printing [17] and slot-die coating [18]. Non-contact printing is becoming more preferable than traditional contact-printing methods due to characteristics such as faster speed, lower cost and greater versatility to different application requirements [3].

1.2 Printable Semiconductors

Semiconductors are an essential component in most electronic devices. In traditional electronics, Si has been dominant for the past several decades [19]. This is attributed to its electrical performance, excellent oxide quality, stability and natural abundance. The ability to easily purify and grow Si as a defect-free single crystal contributes to its excellent electrical properties [20]. However, the wafer-based form of Si is not mechanically flexible, and single crystalline silicon cannot be deposited as films on flexible substrates since the required

deposition temperatures temperature, 1000 °C or higher [21], far exceeds the thermal budget of flexible substrates.

There has been tremendous effort devoted to solving these problems and finding other alternatives to satisfy the market demand. One popular area of research is organic semiconductors [22]. Organic semiconductors can be dissolved in organic solvents then printed. They are mechanically flexible and can be manufactured at low temperatures that align within the thermal budget of most flexible substrates. Example materials include poly(3-hexylthiophene) (P3HT), poly (triarylamine), poly(3,3-didodecyl quaterthiophene) (PQT), poly(2,5-bis(3-tetradecyllthiophen-2-yl) and thieno[3,2-b] thiophene) (PBTTT) [23] [24]. However, there are two large challenges of most organic semiconductor materials. Firstly, their poor environmental stability and thus shortened lifetime [22]. Secondly, their charge carrier mobilities are usually in the range of 10^{-4} to 1 cm^2/Vs [1], which is far lower compared to their inorganic counterparts (for example, the mobility of single-crystal silicon is on the order of 10^2 - 10^3 cm^2/Vs [1]) [25]. This is a problem since low mobilities lead to lower conductivities and thus worse electrical performance. For example, a transistor with low carrier mobility cannot switch as fast at a given electric field [1].

Apart from organic semiconductors, efforts have also been made to explore printable inorganic and carbon-based semiconductors. These materials have inherently high charge mobility and are more stable in an ambient environment. To make such semiconductors printable, they are typically synthesized in nanostructure form such as nanoparticles (NPs), nanowires (NWs) or 2D nanosheets and then dispersed in a solution to form printable inks.

Some examples are summarized in Table 1-1, along with their printing methods, device substrates and field effect mobilities. The major material categories are discussed below.

Table 1-1: Examples of printable nanostructured inorganic and carbon-based semiconductors along with their respective printing method, device substrate and field effect mobility.

Semiconductor	Printing Technique	Substrate	Field-effect mobility (cm^2/Vs)	Ref
Si NPs	Screen printing	Paper	0.3~0.7	[26]
ZnO NPs	Spin coating	Plastic	0.066	[27]
In_2O_3 NPs	Inkjet printing	Plastic	0.26~0.8	[28]
CNTs (aligned)	Spray coating	Plastic	98	[29]
CNTs (random network)	Gravure printing	Plastic	~9	[30]
Graphene sheets	Wet transfer	Plastic	230	[31]
MoS_2 nanosheets	Inkjet printing	Plastic	0.08 – 0.22	[32]
WSe_2 nanosheets				

1.2.1 Inorganic Nanoparticles

Inorganic nanoparticles are the nano-particulate form of its bulk inorganic constituent. Among the different printable inorganic nanoparticles, Si nanoparticles (SiNPs) are one of the most popular candidates because of the prevalence of Si in traditional electronics. SiNPs have advantageous properties such as high mobility, good environmental stability, controllable luminescence, size-dependent band gap and non-toxicity [33]. They are usually synthesized through physical (such as pulsed laser ablation [34] and high energy mechanical milling [26]), chemical [35] or electrochemical etching [36] processes. Their solution processibility makes them compatible with different printing methods and thus they are well suited for many printable electronics applications. However, films composed of NPs are polycrystalline in nature; the boundaries between NPs causes electron scattering which limits their electrical properties such as their charge carrier mobility. High temperature treatments such as post-deposition anneals on the NP films, which are otherwise commonly adopted to improve the crystallinity of the films, are prohibited on flexible substrates. A mobility of only 0.3 to 0.7 cm^2/Vs has been reported for a thin film transistor based on the screen printing of SiNPs on paper [26]. Apart from SiNPs, metal oxide nanoparticles such as ZnO NPs [27] and In_2O_3 NPs [28] is another popular category, but their mobilities are no greater than SiNPs. Metal oxide NP films, like SiNPs, suffer from charge carrier scattering at NP junctions and the inability to employ high temperature treatments when incorporated onto flexible substrates. Furthermore, another possible reason is the use of precursors or stabilizers in the synthesis process of these metal oxide nanoparticle based inorganic inks. These precursors or stabilizers often cause

fraction in deposited films and induce charge traps that deteriorate the charge transport properties [37].

1.2.2 Carbon Nanotubes

The superior charge transport properties of carbon nanotubes (CNTs) have attracted great research interests. For example, field effect transistors based on an individual single-walled semiconducting CNTs have reported a mobility of 10^5 cm^2/Vs [38]. CNTs are usually synthesized using chemical vapor deposition (CVD), arc discharge or laser ablation [1]. To make CNTs printable as a film, they are usually dispersed in organic solvents and surfactants are widely used to facilitate better dispersion [1]. However, due to the synthesis process of CNTs, they generally demonstrate a mixture of metallic and semiconducting properties, and therefore need to be further sorted before their incorporation in devices which is an expensive, impractical process [39]. In addition to proper sorting, these CNTs need to be either aligned or printed in the form of a random network. However, the former is challenging to scale up and adapt to a fully printable scope [37], and the distance between contacts cannot be larger than the length of one CNT, which is limiting for larger-area sensors and long channel devices. In the case of a random network/mesh, the mobility is significantly compromised due to carrier hopping at nanotube-nanotube junctions in the loosely arranged CNT networks [37]. These points of overlapping CNTs cannot be sintered like in traditional metals and inorganic semiconductors.

1.2.3 Graphene

Graphene is a two-dimensional semiconductor with zero band gap whose lattice is composed of a flat sheet of hexagonally arranged carbon atoms [1] [37]. Single-crystalline graphene can have very high mobility of 2.5 x 10^5 cm^2/Vs [40]. The simplest method to synthesize graphene is through mechanical exfoliation using a scotch tape [41], however it is neither printable nor scalable [42]. Chemical synthesis offers the ability to mass-produce graphene through the oxidation of graphite into graphene oxide (GO), which can then be converted back to graphene at the very end through chemical reduction or thermal annealing [43]. Compared to graphene, GO can facilitate the dispersion of the flakes in solvents such as water [42] due to the stronger oxygenated content that enhances its hydrophilicity [44]. However, the oxidation-reduction process significantly degrades the electrical properties of graphene [42] and in cases where the GO is reduced using high temperature annealing instead of chemical methods, a temperature of 1000 ˚C or higher in required, which prohibits its incorporation onto flexible substrates. For example, an electron mobility of 281 cm^2/Vs was obtained on such chemically synthesized, solution-processed graphene on rigid (Si/SiO_2) substrate, where an annealing temperature of 1000 ˚C was applied [45]. Another popular method to produce high-quality graphene is through chemical vapor deposition, where transition metals such as Ni, Cu and Pt are used to catalytically decompose hydrocarbon and graphene is formed on the surface of the metals [42]. However, very high temperatures (~1000 ˚C) are involved, and the metals need to be chemically etched away so that the graphene can be released and transferred onto another substrate in the form of a graphene film [42]. This can be scalable but is expensive and not solution-processible. The mobility of graphene films is on

the order of 10^1s [46] to10^2s [31] cm^2/Vs for devices directly transferred on flexible substrates, which is several orders of magnitude lower than single-crystalline graphene. The mobility reduction is possibly because of electron scattering when moving from one flake to another at the flake edges, and due to the presence of impurities in the flakes [37]. Another problem with graphene is that is does not have a band gap, which leads to poor switching performance in transistors (i.e. low I_{ON}/I_{OFF} ratios) [37].

1.2.4 Metal Dichalcogenides

To overcome the issue of graphene having no band gap, other 2D materials are currently being explored, particularly metal dichalcogenides such as Molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2) [37]. These materials, like graphene, can also be exfoliated as flakes and deposited as a film. However, although they have appreciable band gaps and demonstrate semiconducting properties, their carrier mobility when incorporated into films is relatively low as can be seen in Table 1-1. Apart from carrier scattering at the flake edges or junctions (similar to the issue with graphene flakes), this low mobility can also be attributed to the vulnerability of metal dichalcogenides to surface contamination and uncontrollable doping which occurs during its synthesis process [32]. In addition, transistors made from these materials have issues of poor environmental stability; the drain current decreases dramatically by up to two orders of magnitude upon exposure to ambient conditions due to the chemisorption of oxygen and water in the defect sites [47], which makes it challenging for reliable applications.

In this thesis, I focus on SiNWs. They have the same advantages of SiNPs described above, i.e. high mobility, good stability, the prevalence of Si in existing electronics and non-toxicity. However, the problem of scattering at the nanoparticle interfaces is lessened in nanowire films compared to nanoparticles, as will be explained in section 1.3. This in turn may increase film mobility as will be investigated in this thesis.

1.3 Silicon Nanowires for Printed Electronics

A nanowire (NW) is a cylindrically shaped 1D nanostructure with a diameter typically less than 100 nm and a length of several microns or more. Although nanowires of many materials have been synthesized and explored, the most attention has been given to silicon nanowires (SiNWs) because of the dominance of silicon in conventional electronics. Simple and cost-effective methods have been developed to obtain single-crystalline, defect-free SiNWs. These nanowires have been shown to have mobilities up to 300 cm^2/Vs [48], which is almost two orders of magnitude larger than most organic semiconductors [49]. In addition, they also demonstrate good environmental stability, which is one of the common advantages of inorganic nanomaterials [1]. Compared to Si thin-films, SiNWs can be fabricated on one substrate (which can, for example, tolerate high temperatures or provide a template for epitaxy), then easily transferred to an arbitrary substrate including plastic. One convenient way to do this is to disperse the NWs in a solvent then print them using standard solution-deposition techniques. Because the NWs are very thin, they are mechanically flexible and at low areal densities can even be transparent [50]. All these features make SiNWs a promising printable semiconductor.

SiNWs have been successfully incorporated into flexible electronics, some using printable techniques. For instance, flexible chemical sensors with highly ordered arrays of SiNWs transfer-printed on plastic substrates have been reported with a hole mobility of 100 cm^2/Vs [51]. Periodic crossed SiNW arrays treated with orthogonally fluidic flow-directed alignment have been used to fabricate flexible light emitting diodes [52]. Large-scale and well-aligned SiNW arrays assembled using the bubble-blown technique have been utilized for field effect transistors on plastic substrates [53]. Contact printing has also been used to deposit aligned SiNWs directly from the substrate upon which the SiNWs are grown (i.e. no need for dispersion in a solvent) by sliding the donor substrate across Kapton. In this manner, flexible diodes based on such parallel arrays of SiNWs have been fabricated [54].

Despite the successful incorporation of SiNWs in printed flexible electronics such as the aforementioned examples, almost all of them rely on the assembly of regularly aligned SiNWs arrays using techniques such as flow-assisted alignment treatment [52], bubble blown treatment [53], contact/roll transfer printing [54] [55], Langmuir-Blodgett [56] and electric field-assisted orientation [57]. None of these are the simple printing techniques used in typical printed electronics manufacturing and the need for alignment increases fabrication complexity and cost. They may also induce impurities that are challenging to remove, such as the use of surfactant in the Langmuir-Blodgett technique [58]. And some techniques can only print over small areas (eg. flow-assisted and electric-field assisted techniques) and/or have limits on the density of NWs that can be printed (eg. bubble blown technique). Secondly, the active areas of all devices are limited in size since contacts can be no more than one nanowire length (i.e. usually a few 1s to 10s of micrometers) apart. This small area is not appropriate for some

applications such as long channel devices and sensors. And depositing metal contacts with these small spacings is challenging with printing techniques.

1.4 Nanowire Networks

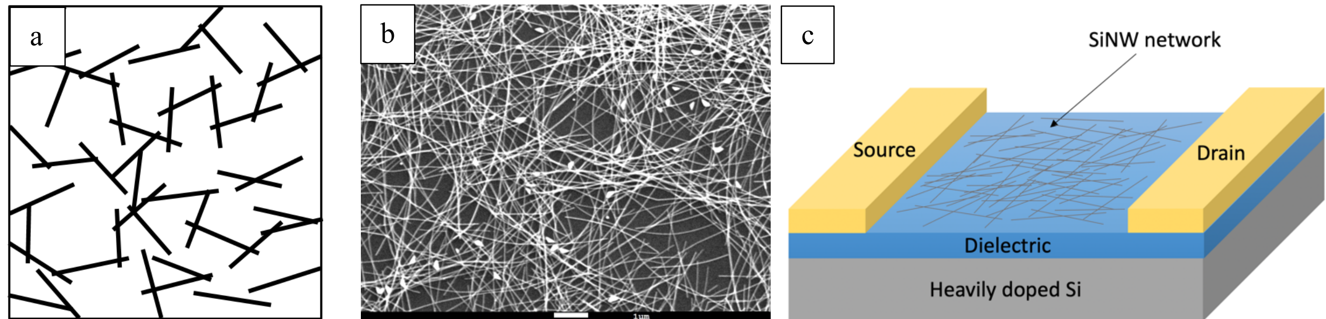

Figure 1-1: a) Schematic of a NW network structure, where the black sticks refer to the NWs. b) SEM image of a silver NW network. The scale bar is 1 µm. c) Schematic of a SiNW network as the channel material in a transistor.

Instead of employing aligned NWs, in this work I propose instead to print the SiNWs as a nanowire network. A nanowire network, which has also been termed a nanonet, refers to a nanostructured system or film which is composed of randomly oriented nanowires (Figure 1-1(a) and 1-1(b)). When the density of NWs in a network is high enough, a connected path exists from one side to another and current can conduct. The smallest NW density required to achieve measurable conductivity is called the percolation threshold [59]. Compared to films of SiNPs, the charge carriers travel further along a crystalline path (the SiNWs are crystalline) before encountering a junction. Thus, there are less junctions overall in the film compared to NPs and the mobility of SiNW networks should be higher than SiNP films.

Unlike the devices reviewed in chapter 1.3, nanowire networks can be deposited using much simpler methods such as spray coating [60], rod coating [61], spin coating [62], drop casting [63] and inkjet printing [64] [65] and are compatible with large scale manufacturing.

Specifically, rod coating and inkjet printing in particular are common printing techniques used in printed electronic manufacturing. Secondly, no NW alignment is needed which simplifies printing. Thirdly, most SiNW synthesis methods result in a lot of variation in properties between NWs, including those synthesized in the same batch (eg. there is variation in their diameters). Therefore, devices based on one or a few NWs themselves also have variation from one device to another. On the other hand, because the electrical performance of nanowire networks arises from the average over many NWs, this should decrease variation between devices [66]. Fourthly, using nanowire networks allows contacts to be spaced further apart, which is desirable for some applications and allows the metal contacts to be printed as well.

Silver nanowire networks have been widely used in the past decade to create transparent electrodes [63] [67]. Because the spaces between the NWs is larger than the wavelength of visible light, these networks are transparent. Simple processing techniques such as sintering or mechanical pressing [61] are used to lower the resistance at the NW junctions (the points where NWs overlap) so that conductivity can be achieved. Although the melting point of silver is > 950 °C, NWs can melt at much lower temperatures which can be explained by the Gibbs Thomson theory [68]. Specifically, the free energy of the NWs is inversely proportional to the diameter of the NWs. This means that compared to the bulk form, the atoms in the NWs will gain the thermal energy required for diffusing rapidly onto other NWs more easily. Therefore, a heat treatment at much lower temperatures is able to provide enough thermal energy to sinter a thin NWs compared to its bulk form [68]. For silver nanowires with average diameters of 35 nm, a 150 °C anneal for 30 minutes is enough to sinter the junctions which lowers the junction resistances, and in turn leads to a network with high conductivity [69].

Networks of semiconducting nanowires have received far less attention than metal nanowire networks and has mostly focused on metal oxide NWs such as ZnO [70] [71] or SnO_2 [72] [73]. Only a few examples of Si NW networks exist [74]; SiNW networks have been used to make a thermoelectric generator [75] and photodetectors [76]. However, the use of SiNW networks for printed flexible electronics has not been explicitly explored. There are no reports in the literature of SiNW networks which have been deposited using common or scalable printable techniques. And there has been little characterization of the electrical performance of these networks, including no characterization of their performance metrics as a transistor channel material. This may be because it has been assumed that the junction resistance of overlapping SiNWs is very high due to the existence of native oxide at the interface between NWs, and/or the high temperature that would be required to sinter the junctions (silicon's melting point is > 1400 °C [77]). However, the Ternon group showed recently that SiNW junctions can sinter at 400 °C due to their nanoscale dimensions, which in turn increased the network's conductance by two orders of magnitude [74]. This temperature is compatible with polyimide substrates, a flexible plastic, thus opening the possibility of using SiNW networks in flexible electronics. Furthermore, because the melting temperatures of nanowires is known to decrease with decreasing diameter [68], thinner SiNWs would likely sinter at even lower temperatures which would permit other substrate possibilities. Combining a moderate processing temperature with the fact that NW networks can be easily printed through several methods without the need for alignment (as shown for silver NWs [69]), the possibility exists for SiNWs to be an attractive option for "printable silicon". The purpose of this thesis is to explore the possibility of semiconductor inks based on SiNWs that are compatible with various

printing techniques, while still maintaining the superior electrical properties inherited from the single crystallinity of Si.

1.5 Silicon Nanowire Synthesis

1.5.1 Review of synthesis methods

To research the possibility of SiNW printable inks, an appropriate SiNW synthesis method must be chosen. There exist many methods, the most common ones are briefly summarized here.

SiNWs can be synthesized using either bottom-up or top-down approaches [2]. The most widely used bottom-up approach is vapor-liquid-solid (VLS) growth [78]. Most commonly chemical vapor deposition (CVD) is used though other techniques such as laser ablation are used as well. A gaseous phase of Si such as silane (SiH_4) or silicon tetrachloride ($SiCl_4$) acts as a Si precursor and certain metals, most commonly gold, are used as a catalyst. When the temperature is heated above the eutectic point of the Si-metal system (such as 363 °C for Au-Si [79]), a liquid Si-metal alloy is formed. When enough gas precursor dissolves into the metal, supersaturation occurs, and a silicon nanowire will precipitate from underneath the Si-metal alloy and continue to grow as long as the precursor gas is supplied.

The advantages of using the VLS method to grow SiNWs is that it can have excellent control of the nanowire diameter (which is controlled by the size of the metal catalyst), the NWs have smooth side-walls which leads to less electron scattering and thus higher mobilities, and vertically standing NWs can be obtained [78]. However, when gold is used as the metal

catalyst, it can create electronic traps which deteriorate the NW electronic performance [80]. More importantly for the application of printed, flexible electronics, which is typically used for large-area low-cost devices, the manufacturing costs and complexity are high.

An alternative approach of SiNW synthesis that has attracted growing interest in recent decades is a top-down approach where NWs are etched from a Si wafer [2]. This approach has large-scale processing capability and can be performed in ambient conditions [49] which brings down fabrication costs extensively. Both these attributes are important for printed electronics.

The most popular methods to etch SiNWs from wafers are reactive ion etching (RIE) and metal-assisted chemical etching (MacEtch) [81]. Reactive ion etching (RIE) is typically a dry etching process which often works in combination with lithography for the successful fabrication of SiNWs [81]. With the help of a bias on the substrate holder, a gaseous source becomes ionized and accelerates towards the substrate. The Si substrate undergoes a chemical reaction with the ions and becomes etched to form SiNWs. The etching process is usually highly directional, which can result in nanowire structures that have a high aspect ratio, smooth sidewalls, and are very well aligned with the substrate and each other [81]. The independence of a metal catalyst is another advantage [82]. However, the downside of this method is that the crystalline quality of SiNWs is compromised because of defect formation in areas close to the etched surface during the dry etching process [2]. Additionally, the scalloping phenomenon which results from the undercuts during sequential etching and deposition steps in RIE remains

challenging for optimization, and it hinders the fabrication of NWs that have a diameter larger than 200 nm [81].

Metal-assisted chemical etching (MacEtch) is another popular top-down approach, but it is fundamentally a wet etching process. A metal catalyst is firstly deposited on a Si substrate, after which the substrate is immersed in an etching solution containing hydrogen fluoride (HF) and an oxidizing agent. Then anisotropic chemical etching occurs at the interface between metal and Si, leading to the fabrication of NWs with a high aspect ratio [81]. Unlike RIE, the synthesis process occurs at room temperature and ambient atmosphere, without the need for a furnace or special equipment. This makes manufacturing simple and inexpensive. SiNWs can be obtained over large area wafers. It allows good control of NW diameter, length, doping type and doping level, all of which are important parameters of the NWs when used in a device [2]. The NWs are not as well aligned as in RIE, but this is unimportant for solution-processable printed electronics applications since the NWs will be harvested off the substrate to be dispersed in an ink. The NWs etched from the single crystalline Si wafer also have excellent crystalline quality as these NWs could inherit the superior electronic properties from the wafer [2]. For these reasons, I chose MacEtch as the preferable method to synthesize SiNWs for my research. Details of the MacEtch process are outlined in the next section.

1.5.2 Metal-assisted chemical etching

1.5.2.1 Overview

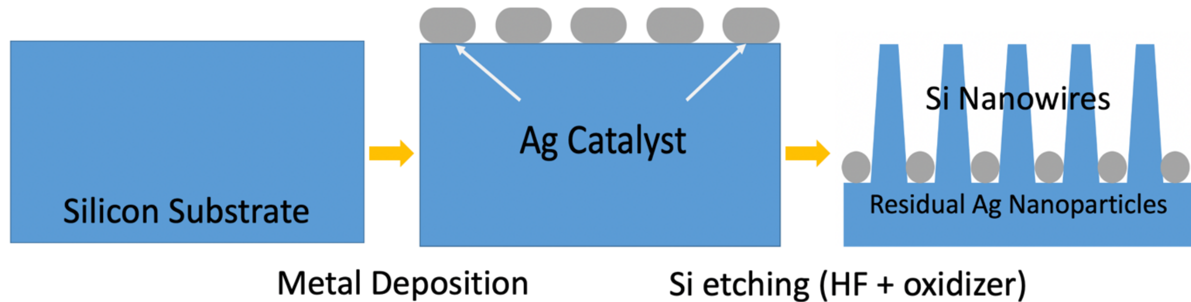

Figure 1-2: Schematic of a typical MacEtch process.

As illustrated above in Figure 1-2, the standard process and basic mechanism of this method is that, through simple deposition of metals on a Si substrate followed by immersing the substrate in a solution containing HF as well as an oxidizing agent, local oxidation reaction takes place at regions covered by the metal. Consequently, Si dissolves anisotropically, leaving nanowire structures on the substrate [2]. The anisotropy results from the preferential movement of metal particles along the crystallographic direction of Si, and the metal acts like a catalyst to speed up the chemical etching reaction [83]. The doping type and level of the SiNWs are the same as that of the source wafer, and the crystal axis of the NWs is the same as the normal crystallographic direction of the wafer [2]. Apart from the metal catalyst deposition through physical process (i.e. sputtering or electron beam evaporation), the remainder of the fabrication process can be conducted in any chemical lab at room temperature and ambient atmosphere, without the need for a furnace or special equipment [2].

Table 1-2 shows some examples of state-of-the-art research regarding the growth of SiNWs with MacEtch, together with a list of the metals used, how the metal is deposited onto the Si

substrate, the etchant composition and the resulting dimensions of the SiNWs [84] [85] [86] [87] [88] [89] [90] [91] [92].

Table 1-2: Examples of SiNWs synthesized using the MacEtch method with different noble metal catalysts, methods of deposition, etchant composition and concentrations, and the resulting NW dimensions. Below L refers to length, while D refers to the average diameter of the SiNWs reported.

Metal catalyst	Deposition method	Etchant composition	NW dimensions	Ref.
Ag	PVD	HF: H_2O_2: ethanol = 30:1:1	L: ~ 1 µm D: 60~80 nm	[84]
Ag	Sputtering	HF: H_2O_2: H_2O = 10:5:35 (v:v:v)	L: N\A D: 8 nm	[85]
Ag	Electroless plating	4.6M HF 0.02M $AgNO_3$	L: 2 µm D: 30 nm	[86]
Ag	Thermal evaporation	4.6M HF 0.44M H_2O_2	L: 1.3 ~ 5.3 µm D: 230 ~ 270 nm	[87]
Au	E-beam lithography	HF: H_2O_2: H_2O = 10 wt%: 1.5 wt%	L: N\A D: 19-22 nm	[88]
Au	Electroless plating	0.4 mM $HAuCl_4$	L: N\A	[89]

		HF: H_2O_2 : H_2O = 1:5:2 (v:v:v)	D: N\A	
Fe	Electroless plating	4.6M HF 0.135M $Fe(NO_3)_3$	L: varies by etching time D: 150 – 250 nm	[90]
Pt	Sputtering	HF (49%): H_2O_2 (30%): methanol = 1:1:2 (v:v:v)	L: N\A D: large variation, ~10 nm (middle of Pt-covered area) and 1~5 µm (at the edge of the coated area)	[91]
Cu	Electroless plating	0.01M $CuSO_4$ 10% HF and 1.2% H_2O_2 in H_2O	L: ~3 µm D: 30~50 and ~75 nm	[92]

There are two main steps in MacEtch that have a determining effect on the quality and morphology of the final SiNWs: metal deposition and the chemical etching reaction [2]. The main parameters within these steps are discussed in the following subsections. It was observed that the morphology of the noble metal film directly relates to the diameter of the SiNWs, as the area covered by the noble metal will sink into the substrate which leaves the standing SiNWs structure. The composition of etchant also has a significant influence as it dictates the morphology of the NW sidewalls [2] [81] [93]. In the following sub-sections, we will further

discuss the main parameters that affect the quality and morphology of the SiNWs fabricated from the MacEtch technique.

1.5.2.2 Metal deposition parameters

Type of metal

The most commonly used metals in the etching process via MacEtch for SiNW synthesis are Au, Ag and Pt [94]. Straight pores form if Au or Ag particles are used to catalyze the chemical etching of Si wafer. However, for the case of Pt, it was found that the Pt particles moved randomly during the etching process, which led to curvy pores generated in the silicon substrate [2]. Since straight pores lead to a smoother sidewall profile of the etched SiNW structure, which in turn should lead to higher NW mobilities, Ag or Au is preferable from this regard.

Thickness of metal

Optimization of the metal layer thickness is critical to successfully fabricate NWs [2] [95] [93]. If it is too thin, such as what was shown by Huang *et al* with the use of a 5 nm thick Ag film, fine pores rather than NWs are formed [2]. However, when the thickness of the Ag film was between 20 nm and 50 nm under otherwise identical conditions, nanowire structures formed [2]. Ideally, a continuous metal film with pores is preferred rather than isolated islands. If the film is too thick, the oxidizing agent will not be able to diffuse into the metal/Si contact and chemical etching reactions will not occur [93]. In Chapter 2, the effect of thickness on the morphology and etching profile of SiNWs will be further explored experimentally.

Method of metal deposition

The third parameter is the method of metal deposition. The metal can be deposited on Si wafers via physical deposition or solution processing techniques [2] [93]. Specifically, physical deposition includes thermal evaporation [96] [87], sputtering [85] and electron beam evaporation [88], while solution process usually refers to electroless plating [90] [97] or spin coating [98]. In order to achieve SiNWs with more controlled morphologies, physical deposition is usually more favorable as the metals can be deposited in a more controlled manner with pre-defined shapes and separation [2]. Studies also found that the adhesion between metals and the silicon wafer was stronger when the metal film was deposited using sputtering compared to solution-based techniques [93]. This may be because the sputtered metal has higher ionic energy after being accelerated in the plasma, which enhances the adhesion between the coating material and the receiving substrate [99], whereas no such bombardment occurs in solution-based methods. When the metal adheres well enough to the surface of the silicon wafer during the entire etching process, a very high aspect ratio (length: diameter around 100) with a diameter of ~ 200 nm and nanowire length of ~ 20 μm can be fabricated [93]. However, physical vapor deposition process usually involves a vacuum environment and high manufacturing temperature, therefore, it often incurs higher fabrication expenses compared to solution-based techniques [2].

1.5.2.3 Etching reaction parameters

After the metal is deposited on the silicon wafer, the wafer is then immersed in an etching solution consisting of hydrofluoric acid (HF) and an oxidizing agent such as hydrogen peroxide

(H_2O_2) [2]. Two of the important parameters in the chemical etching step are discussed below in more detail.

Type of oxidizing agent

The most commonly used oxidizer is H_2O_2 which successfully produces SiNWs with good uniformity and is thus reported in literatures extensively [2] [56] [66]. Other oxidizing agents which serve as potential candidates of etchants include $AgNO_3$ [102], HNO_3 [103], $KMnO_4$ [104], $Na_2S_2O_8$ [105] or O_2 bubbles (i.e. O_2 dissolved in H_2O) [106]. However, the use of H_2O_2 is generally the primary choice because of the avoidance of ionic metal by-products which is usually challenging to get rid of [2].

Concentration of etching solution

Apart from the choice of oxidizing agent, the concentration of the etching solution is of importance as well. Researchers [2] have observed that straight pores, and thus NWs with a cylindrical shape, are generated when the concentration of H_2O_2 is low ([HF]/([HF]+[H_2O_2]) between 0.7 and 1.0), while cone-shaped pores gradually form as the concentration of H_2O_2 increases further ([HF]/([HF]+[H_2O_2]) smaller than 0.7). NWs with a uniform diameter along their axes would lead to more uniform electrical performance when assembled into networks, and thus a lower concentration of H_2O_2 was adopted in my project.

More experimental details will be covered in Chapter 2.

1.6 Thesis organization

For SiNWs to be suitable for printed flexible electronic devices, an inexpensive, large-volume synthesis method is required, and the NWs, once dispersed in an ink, should ideally be

printable using a cost-effective and scalable technique. In Chapter 2, the optimal experimental parameters found for the MacEtch method is presented, followed by a summary of the experiments to disperse SiNWs in an aqueous medium with minimal agglomeration and breakage, then lastly the fabrication of a SiNW network through different printing techniques is described. In Chapter 3, the SiNW networks are electrically characterized. The optimal annealing temperature to reduce the overlapping NW junctions is determined, and the SiNW network is incorporated into a transistor to assess its mobility and I_{ON}/I_{OFF} ratio. Chapter 4 is a departure from SiNWs in which 2D graphene oxide flakes are rod-coated onto plastic substrates. This is relevant for printable semiconducting inks since 2D flakes are another semiconducting nanostructure, and rod-coating is an underexplored but promising method for their deposition due to its suitability for large-area, continuous and cost-effective printing. Finally, Chapter 5 concludes the thesis and outlines future work.

Chapter 2
Synthesis, Dispersion and Printing of Silicon Nanowires

2.1 Synthesis of silicon nanowires

2.1.1 Introduction

As mentioned in Chapter 1.5, metal-assisted chemical etching (MacEtch) has been selected as the optimal method for this project, as single-crystalline SiNWs can be synthesized in large volumes at a relatively low cost, and the resulting NWs are compatible with various solution-based printing methods [2]. The following subsections will focus on the specific procedures and parameters within this method.

The goal of synthesis for this particular project is to obtain Si NWs that:

- Are as long as possible. This is because the NWs will be deposited in a network, and fewer NWs are required to reach the percolation threshold when they are longer [107]. Furthermore, networks assembled from longer NWs tend to exhibit better electrical performance [59] because networks of longer NWs have a lower number of overlapping NW junctions where high resistance is incurred. Thus, long NWs should lead to films with higher mobility than networks of shorter NWs.
- Are well separated from one another. NWs which are touching one another (bundling) make it more difficult to disperse individual NWs in a solution.
- Have a uniform diameter along their length so that the properties are constant along its length.

- Have homogeneous diameters (the diameters of the NWs are similar to one another) so that the properties across the printed NW network are similar across its area.

The synthesis of the SiNWs will be described and discussed into three main categories: substrate preparation (section 2.1.2), metal deposition (section 2.1.3) and chemical etching (section 2.1.4).

2.1.2 Substrate preparation

One-side-polished single crystalline <100> p-type boron doped Si wafers with a resistivity of 10 - 20 Ω·cm, thickness of 500 – 550 μm and diameter of 100 mm were used. Lightly doped wafers were chosen since the resulting lightly doped SiNWs will have higher mobility than more heavily doped ones. The wafers were sonicated in acetone, isopropyl alcohol (IPA) and deionized (DI) water for 5 min each, which cleans the surface of undesired impurities and residues from manufacturing that can be detrimental to the device performance [108]. After ultrasonic cleaning, the wafers were then blown dry with nitrogen gas and subsequently cleaved into 1 x 1, 1 x 2 and 0.7 x 0.7 cm^2 samples using a Disco automatic dicing saw (DAD3240), with the choice of size depending on the application needs.

2.1.3 Metal deposition

Silver was chosen as the metal to assist the chemical etching because, as mentioned in section 1.5.1, it can produce straight holes (i.e. vertical sidewall profiles of SiNWs) during the etching step [2] [93] [101] and is less expensive than gold. As mentioned in section 1.5.1 also, physical vapour deposition is preferable compared to solution-based techniques as it allows better adhesion between the deposited metal film and the substrate [2]. More importantly, it is

able to deposit metals in a more controlled manner with the desired 'anti-dot' morphology [93]: a porous structure with uncovered nano-scaled dots. The uncovered dots will form the NW structure, while the parts covered by the metal will sink into the substrate. These properties are crucial for the success of MacEtch. The deposition was carried out by sputtering (AJA Orion twin chamber magnetron sputter system) Ag film (source: Kurt J. Lesker, 2.00'' in diameter and 0.250'' in thickness) with an average thickness of 10 nm on a 1 x 1 cm^2 Si substrate. A standard recipe preset in the sputter system was followed during the sputtering process. The speed of Ag deposition was calibrated to be roughly 0.97 nm/s with a Dektak 150 surface profilometer (Veeco Instruments Inc).

Atomic force microscopy (AFM) (Bruker Fastscan/Icon atomic force microscopy, ScanAsyst mode) was performed, where the bright parts in Figure 2-1 correspond to the area covered by Ag and the darker background is the bare Si substrate. It can be observed that the desired porous structure was obtained.

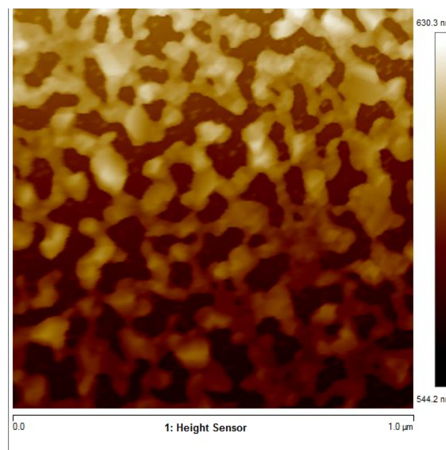

Figure 2-1: AFM results of the 'anti-dot' morphology of Ag sputtered on Si. The righter areas correspond to the area covered by Ag and the darker areas are bare Si.

It was experimentally determined after chemical etching that a deposition thickness of 10 – 20 nm of Ag generates the most desirable porous structure that leads to the successful growth of SiNWs. When the thickness was increased to 25 nm, a non-uniform porous structure instead of 1D NW structures formed after etching (Figure 2-2b). A similar observation was reported in the literature [96], where a 20 nm thick Ag resulted in the formation of SiNWs with more homogeneous diameters after chemical etching, whereas a further increase in thickness to 50 nm under otherwise identical conditions led to nonhomogeneous nano-structures of Si. This phenomena was attributed to the insufficient presence of gaps in the thick Ag film coverage, which made it difficult for the etching solution to properly make contact with the Si beneath the thick Ag film [96].

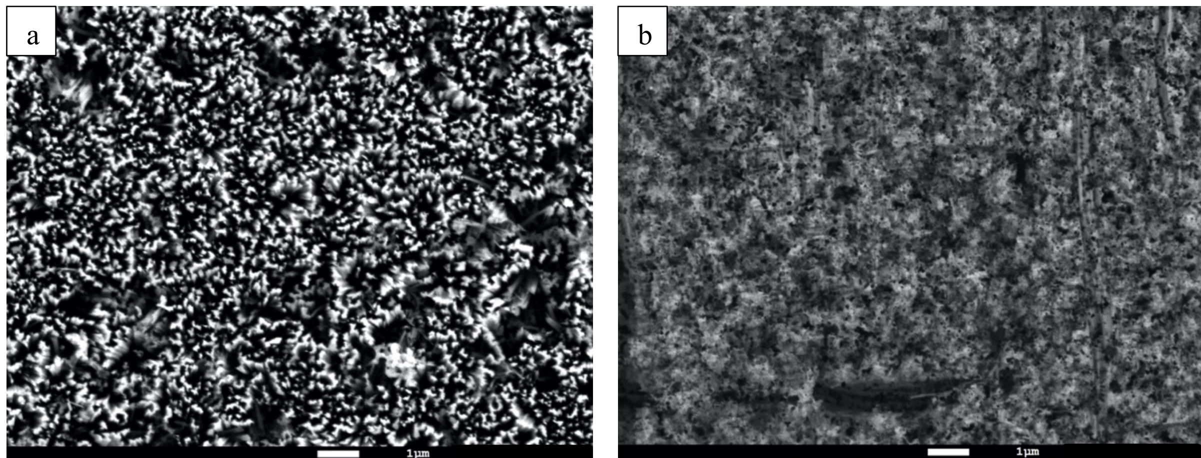

Figure 2-2: SEM images comparing the top-down profiles of the etched structures. a) 15 nm of Ag was deposited and SiNWs were successfully obtained. b) 25 nm of Ag was deposited and a porous mesh structure with no NWs was observed. The scale bars are 1 µm.

2.1.4 Chemical etching

For the reasons described in section 1.5.2, H_2O_2 was chosen as the oxidizing agent in the etchant. As discussed in Chapter 1.5.2, the concentration of etchant has a determining effect on both the quality of the etching profile as well as the etching rate [2]. In order to achieve

anisotropic etching at an acceptable etching rate, an etching solution containing HF (49%), H_2O_2 (30%) and deionized water with a volume ratio of 10:1:8 was selected which generated SiNWs as desired, and the SEM characterization (shown below in Figure 2.3) demonstrated that these NWs were similar to what was reported in other work [2] [101] [109] as well. The NWs showed good uniformity and homogeneity, with an average diameter of 100 nm.

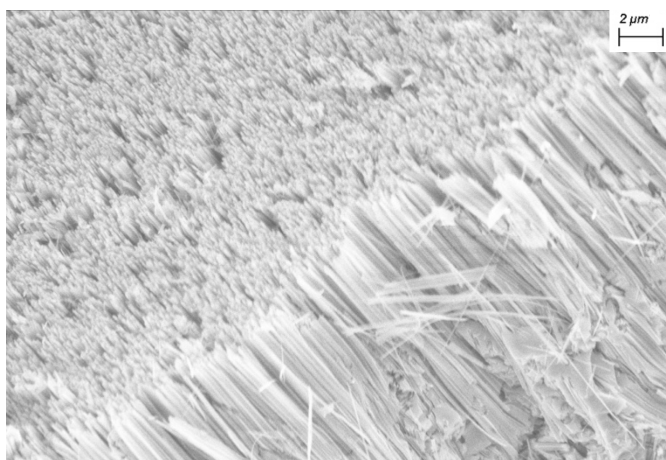

Figure 2-3: 45˚ tilted SEM characterization of SiNWs after chemical etching and without any specific treatment. The scale bar is 2 μm.

The Ag-coated Si pieces were immersed in the etching solution and the etching was carried out for a duration of 3 min, 20 min, 80 min, 120 min and 210 min. After 3 min of etching, the NW length was negligible as observed in the SEM and hard to measure. After 20 min of etching, the average length of NWs increased to roughly 17 μm, while further increases in duration led to further increases in the average NW length (Table 2-1). However, the growth rate slowed gradually as the duration was increased, which might be due to the increased difficulty of the etchants penetrating deeply to the bottom of the NW forest as the NWs grew longer with etching. Therefore, although longer NWs are desired, one may need to take into account the excessive time required to achieve very long lengths.

Table 2-1: Average SiNW lengths with respect to the different etching durations.

	Etching Duration (min)				
	3	20	80	120	210
Average NW length (μm)	N\A	~17	~32	~48	~62

2.1.5 Post-etching surface treatment

A common problem that occurred after chemical etching was the agglomeration of SiNWs into bundles (as seen in Figure 2-4a and 2-4b below). The bundling effect is an inherent limitation of the MacEtch method itself because of the unavoidable dependence on the liquid medium in the chemical etching step [86]. The causes of the agglomeration can be attributed to van der Waals forces between NWs [110] [111] [112] and the capillary forces due to the surface tension when the solvent evaporates [113] [114] [115]. Avoiding or minimizing bundling is desired so that individual NWs, rather than bundles of NWs, can be dispersed in the ink and thus networks of individual NWs can be printed. This will result in better electrical and optical performance of the networks.

Typical post-surface treatment for minimizing bundling effect include freeze drying [116] or critical point drying (CPD) [117]. In freeze drying, the solvent is directly sublimated from the liquid state to the vapor state [86]. Similarly, in CPD, the liquid is directly transformed to the gaseous state by means of the critical phase transformation (the temperature and pressure conditions where liquid and gaseous states coexist). Liquid carbon dioxide is often used due to its low critical point and pressure. The capillary force is minimized throughout the process

because of the limiting presence of liquid-vapor interfaces as the supercritical carbon dioxide evaporates [118]. As explained earlier, the capillary force is one of the critical reasons why coalescence of NWs occurs, therefore, minimizing this force by restricting the formation of a liquid-vapor phase boundary throughout the drying process would be beneficial in reducing the agglomeration effect.

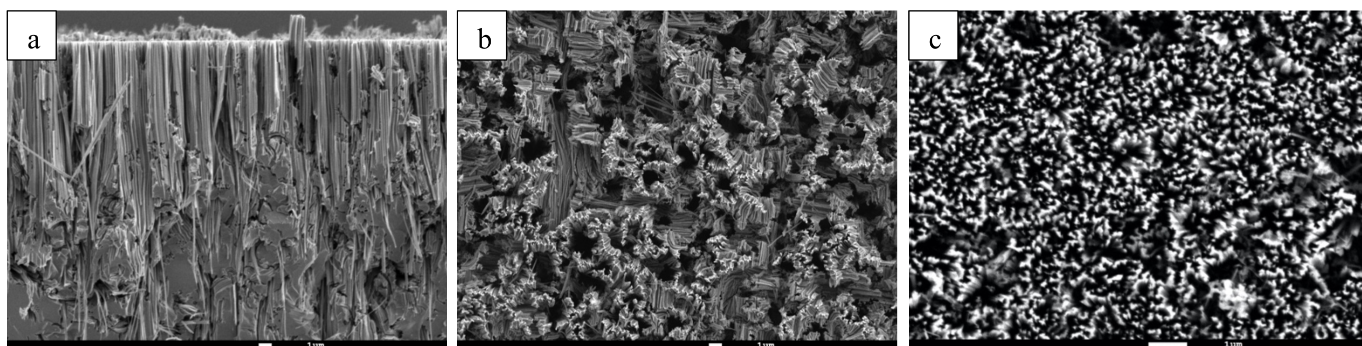

Figure 2-4: SEM images of SiNWs (a), (b) without and (c) with the use of critical point drying. Less bundles are present in (c). The scale bars are 1 µm.

The reasons above form the basis of why CPD was first employed in this work to minimize the bundling effect of SiNWs. After chemical etching, CPD (Tousimis Critical Point Dryer Autosamdri-815B, Series C) treatment with supercritical carbon dioxide was performed on the SiNWs on silicon wafer right after the chemical etching. There was a slight decrease in the bundling phenomenon after the CPD treatment (Figure 2-4c compared to Figure 2-4a and 2-4b). However, bundles are still present, and furthermore, the additional step of CPD deteriorated the yield during the dispersion of SiNWs in the solvent, which is discussed in more detail in the next section. Apart from CPD, a new method was developed for the first time where after the chemical etching step, the SiNWs were directly immersed and stored in IPA without going through any drying process to limit its contact with air. This contributed to

fewer large bundles after dispersion and printing of SiNWs, which will be further discussed and presented in the following sections in more detail.

2.2 Dispersion of Silicon Nanowires

2.2.1 Introduction

To be able to be printed, the SiNWs need to be harvested off the Si wafer and dispersed in a solvent. It is preferable if the detachment of SiNWs occurs closer to their roots to maintain their length, since longer NWs will lead to networks with better electronic properties as described in section 2.1.1.

Various methods have been developed to remove the SiNWs from a substrate [119]. Common examples include physical scraping with mechanical bending fracture [120] or a razor blade [121], stamping with an elastomer material such as polydimethylsiloxane [122] and ultrasonication bathing [123] [124] [125] where the detached SiNWs are sonicated then dispersed in an aqueous medium such as deionized water (DI) [126], ethanol [109] or isopropyl alcohol (IPA) [127]. In physical scraping, it is hard to control precisely as it is difficult to quantitatively adjust the direction and strength of forces during the detaching process [119]. Similarly, the difficulty in completely removing the residual elastomer remains a limitation of the stamping method, which raises concerns of possible contamination that may deteriorate device performance. In addition, pre-treatment is often required to soften the contact areas for easier transferring with the elastomer, which adds additional complexity [119]. On the other hand, since ultrasonication is easy to set up and allows precise control over multiple parameters

such as sonication power, duration, temperature and volume, it was chosen as the method for dispersion.

The goal for the dispersion of SiNWs is to maximize the number of NWs that are removed from the substrate to maximize the NW density in the solvent, maintain long NW length, and minimize agglomeration and precipitation out of the solution. The optimization process focused primarily on four parameters: surface treatment (section 2.2.2), sonication power (section 2.2.3) and sonication duration (section 2.2.4).

2.2.2 Surface Treatment

As mentioned in subchapter 2.1.5, agglomeration occurred among the SiNWs after being chemically etched. Critical point drying (CPD) only moderately reduced bundles. In addition, as the samples with CPD treatment showed a much poorer yield when the NWs were dispersed in DI water compared with the samples that did not go through CPD treatment. The lower yield was evidenced by a much clearer solution color as seen in Figure 2-5 (two vials on the right), compared to a brownish color observed for samples that did not undergo such CPD treatment (two vials on the left).

Therefore, I designed a different route never discussed in the literature. The drying step was skipped entirely to avoid the capillary force exerted by the solution phase at the liquid-vapor interface during the process of drying. After etching, the Si substrate (with SiNWs on top) was moved directly from the etching solution into a different beaker of IPA with minimal contact with air. Through this method, the presence of agglomeration in the solution decreased dramatically while the yield, or SiNW density, remained similar to the samples without any

special treatment, as indicated by a similarly brownish color after sonication to that of the left two vials in Figure 2-5. Quantitative data showing this will be covered in the next section where comparisons will be made after printing SiNW inks with and without such surface treatment.

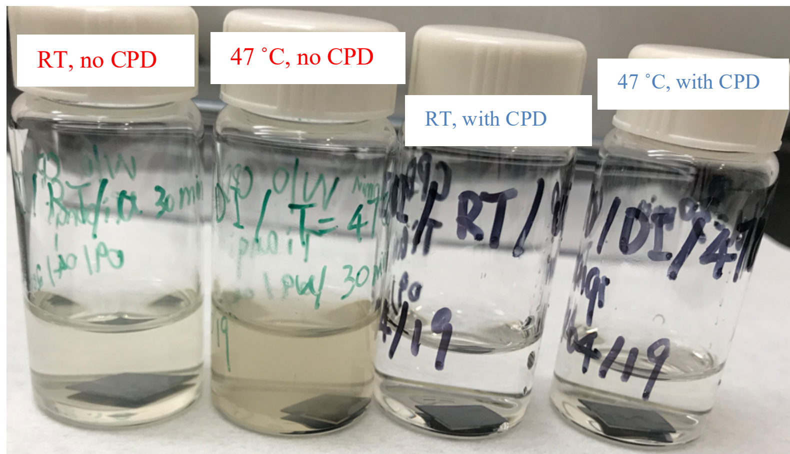

Figure 2-5: SiNW solution after sonication. The two vials on the left did not undergo CPD treatment and the right two vials underwent CPD treatment. In addition, the sonication bath used for the first and third vial was at room temperature (RT), whereas it was 47 ˚C for the second and fourth vials.

2.2.3 Type and volume of solution

It was intensively reported in the literature that dispersion of SiNWs in deionized (DI) water [126] and IPA [127] achieved complete dissolution, while precipitation occurred when dispersing SiNWs in toluene, xylene and chloroform [127]. The different solubility behavior of the SiNWs is attributed to the polarity of the solvent as well as the surface hydrophilicity of the NWs [127]. Since the SiNWs synthesized through MacEtch are covered with a SiO_2 shell which creates a hydrophilic surface, these NWs therefore dissolve more easily in polar solvents such as DI and IPA [127]. As such, these were chosen as the initial dispersing medium of the SiNWs.

Before sonication, 1 x 1 cm^2 Si substrates with SiNWs grown on one side were placed on the bottom of a clear 20 mL glass vial (cone-lined cap) containing the dispersing solution of various volume ranging from 1 to 20 mL.

Although no NW precipitation took place after sonication in either DI water or IPA, it was found that the yield was higher in IPA as indicated by a more brownish solution color. This difference may be attributed to the combined effect of the polarity and surface hydrophilicity of IPA that better facilitates the dissolution of SiNWs. Therefore, IPA proved to be a better and more promising dispersing solvent medium candidate than DI water for the case of SiNWs synthesized using the parameters discussed in Chapter 2.1.

The optimal volume in which SiNWs are dispersed depends on the printing method to be used. As will be described in the following subchapter 2.3, two main methods were tested to print the SiNW inks – rod coating and vacuum filtration. The volume of solution that can be rod coated is limited, whereas with vacuum filtration a large amount of solution can be used to deposit on a small area. This means that the density of NWs in an ink to be rod-coated needs to be much higher than an ink that is vacuum filtered. For rod-coating, 1 x 1 cm^2 Si wafer chips with SiNWs on top were dispersed in volumes of 1, 2, 5, 10 and 20 mL. For inks that were vacuum filtered, the volume used was 15 mL.

2.2.4 Sonication power and duration

Sonication power and duration are the main parameters which manipulate the intensity of the mechanical force acting on the SiNWs to facilitate the detachment from the Si wafer [119]. Fine optimization needs to be performed to properly disperse the SiNWs while preserving their length. This is because, when either the sonication intensity or duration is high to break more NWs off the substrate, these NWs also have a higher probability to be fragmented into shorter pieces [59] [127]. Consequently, the parameters need to be well explored to maximize the yield of SiNWs while still preserving their longest length possible.

Sonication duration was varied first while keeping the sonication intensity to half of its maximum value. After sonication, the NWs in solution were drop-cast on a Si substrate and observed in the SEM to determine the density of NWs, their length and spatial distribution. As summarized in Table 2-2, for durations of 10, 30, 60 and 90s, the yield increased gradually and reached maximum concentration at 90s. After a further increase to 120s, small NW bundles started to form and when reaching 180s, more broken NW pieces was observed.

Table 2-2: Summary of the quality of SiNWs dispersed with respect to duration of ultrasonic bathing. Other parameters were set the same, including mid power (half of maximum intensity achievable), a bath temperature of 70 ℃, and DI water as the dispersion solvent.

Ultrasound duration	10s	30s	60s	90s	120s	180s
Mid power, 70 ˚C in DI water, drop casting	Lowest yield	Low yield	Moderate yield	Highest yield	High yield, small bundles formed & mild fragmentation	High yield, small bundles & more fragmentation

The combination of sonication duration and intensity on the quality of SiNWs was then tested. Durations of 90s, 120s and 180s were selected because they generated the highest SiNW density, while one half and one quarter of maximum intensity settings were chosen because a lower power setting might reduce fragmentation. However, as summarized below in Table 2-3, the lower intensity of ultrasonic bathing provided limited improvement on the preservation of intactness and length of the SiNWs. At the same time, the yield was lower as the mechanical force is not strong enough to separate the NWs from the Si substrate.

Table 2-3: Summary of the quality of SiNWs dispersed with respect to the different durations and intensity settings of ultrasonic bathing. Other parameters were kept the same, including a bath temperature of 70 °C and DI water as the dispersion solvent.

	Mid Power (1 / 2 P_{max})			Low power (1 / 4 of P_{max})		
Duration	90s	120s	180s	90s	120s	180s
70 ˚C in DI water	High yield	High yield but with bundles & little fragmentation	High yield but with bundles & mild fragmentation	Moderate yield	Moderate yield, mild fragmentation	Low yield, more presence of fragmentation

In conclusion, among the matrix of sonication power and duration, the combination of half of maximum ultrasound intensity for a duration of 90s generated the highest yield while limiting bundling and fragmentation.

2.3 Printing of Silicon Nanowires

2.3.1 Introduction

Once the NWs are dispersed in solution, the next step is to print these SiNWs as networks onto various substrates ranging from a rigid Si substrate to flexible platforms including Kapton and polyethylene terephthalate (PET). For randomly interconnected SiNWs, a homogenous

distribution is preferable [74] [128]. There are various methods for printing solution-based NWs onto substrates including drop casting [129] [130] [131], Mayer rod coating [132] [133] [134], vacuum filtration [74] [128] [66], elastomer assisted transfer printing [51] [135] and spray coating [136] [137]. In this work, the first three methods were tested. Elastomer assisted transfer printing was not employed because it is not a method used in printed electronics; it is complex, there are contamination issues with the elastomer, metal contacts are poor because of poor metal adhesion, and the peeling step of the elastomer causes breakage of 80-85% of the NWs [135]. Spray coating was avoided as well because the length of NWs that can be printed is limited due to clogging of the nozzle, and the nozzle causes the printed NWs to be curved rather than straight, which leads to worse electrical performance of the networks [138].

2.3.2 Drop casting

Drop casting simply involves dispensing a volume of NW suspension onto a substrate. It benefits greatly from simplicity and low fabrication cost. It can be applied to any receiving platform. However, this method has limited control on coating homogeneity, which significantly affects the quality of the NW network that would be formed after deposition.

The dispersed SiNWs used for drop casting were obtained by immersing one 1 x 1 cm^2 Si substrate with etched SiNWs in 2 mL of IPA, and then sonicating for 60s at mid power. Then the glass vial containing the SiNW solution was shaken for 1 min. Afterwards, 500 µL of the SiNW solution was drop casted in the middle of a clean Si substrate and the substrate was then air dried before scanning electron microscopy (SEM) imaging. The coffee ring effect noticeably appeared after drop casting and drying (Figure 2-6). The SiNWs tended to

accumulate on the circumference and in the middle of the droplets after drop casting, which originated from the minimizing of surface tension during the evaporation of liquid.

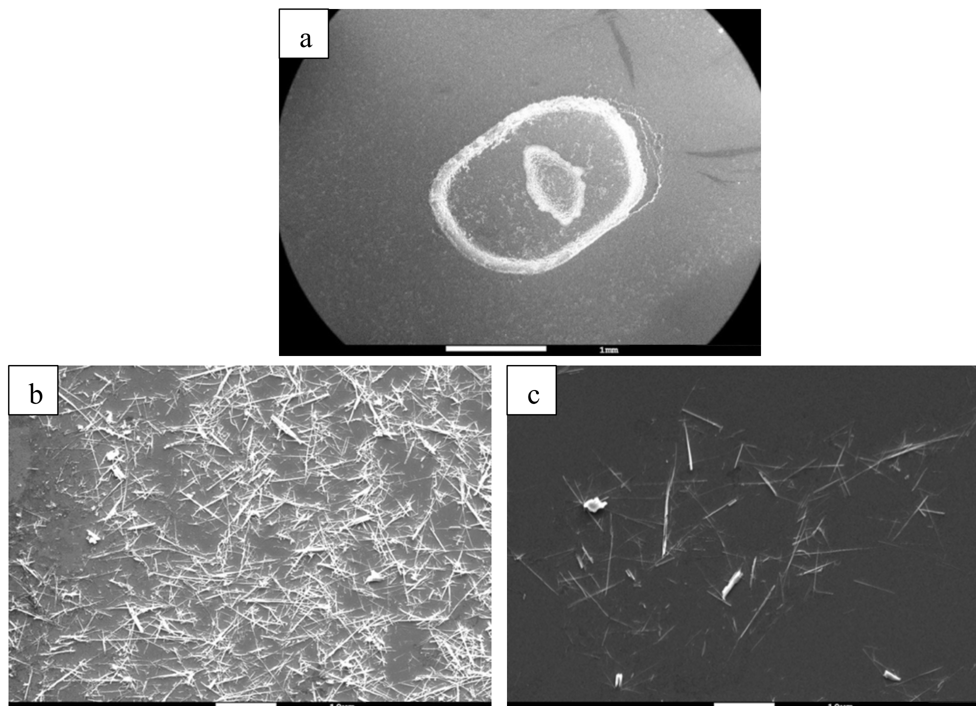

Figure 2-6: SEM characterization of SiNWs drop casted on a Si wafer. a) The presence of a coffee ring deposition pattern at low magnification. The scale bar is 1 mm; b) The circumference of the ring where SiNWs accumulate; c) The inner portion of the droplet, away from the middle, where much fewer SiNWs are observed. The scale bar is 10 µm in both b) and c).

The non-uniform distribution of SiNWs on the substrate is problematic as the network would have very different properties in some parts compared to others and would be completely non-conductive where the SiNWs are sparse. Therefore, the method of drop casting was not explored further.

2.3.3 Mayer rod coating

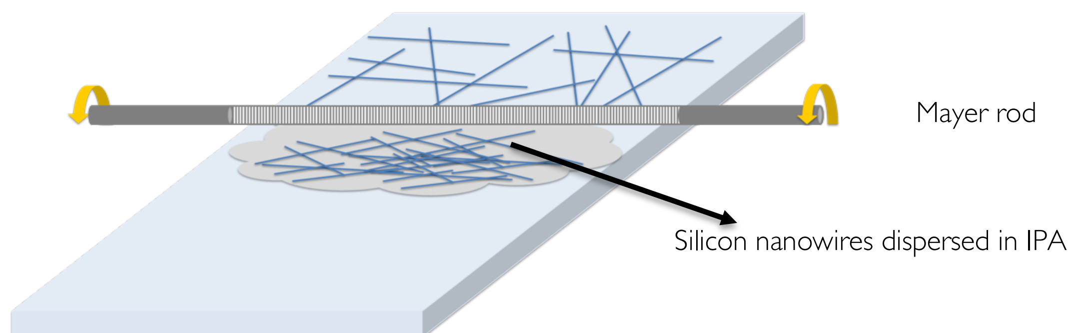

Figure 2-7: Schematic of the Mayer rod coating process.

In Mayer rod coating, as demonstrated in Figure 2-7, NW ink is first drop casted at one end of the substrate, then the Mayer rod is rolled or pulled along the substrate to draw the solution from one end to the other. The Mayer rod itself has a wire wound around the rod, and the diameter of this wire determines the thickness of the film that gets deposited. Mayer rod, or very similar coating methods such as knife coating or doctor blading, is commonly used in industrial-scale printing because it is scalable to metre scales and compatible with high-throughput roll-to-roll methods. It is simple and inexpensive, offers precise control on the thickness of the solution printed and is compatible with deposition onto various substrates. For these reasons, and because rod coating can solve the non-homogeneity problem of drop casted SiNWs, it was explored as a printing method.

For all rod coating experiments, the SiNWs were sonicated for 90s at mid-power. Initially, one 1 x 1 cm^2 Si substrate immersed in 2 mL of IPA was used in the vial during sonication. An RDS #10 rod (RD Specialties) was used to deposit four coats onto a clean Si substrate, with each coat being in each of the four orthogonal directions to contribute to a more homogenous distribution of printed NWs. As expected, the distribution of SiNWs was more uniform over

the entire surface (Figure 2-8) compared to drop casting. However, the areal density was too low to reach the percolation threshold and thus a functional network of SiNWs was not obtained. Therefore, the next step was to increase the density of the SiNWs deposited on the substrate.

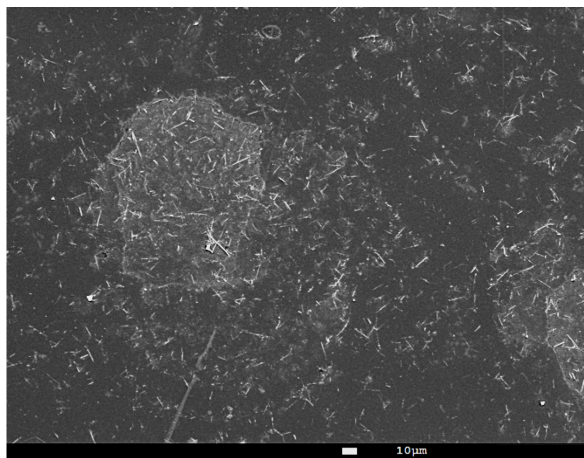

Figure 2-8: SEM characterization of the initial trial of Mayer rod coated SiNWs on Si using RDS #10 with 4 coats. The scale bar is 10 μm.

In order to increase the areal density of SiNWs, an RDS #20 rod was adopted next as it was able to deposit a thicker film of solution with the same number of coats. However, a new problem arose as the SiNWs tended to accumulate in circular shapes rather than uniformly spread across the entire substrate (Figure 2-9). At higher magnification (Figure 2-9c), it was seen that a coffee ring effect was observed within the circles, with a higher density of SiNWs on the circumference of the circles. Also, the concentration of SiNWs for samples with 8 coats (Figure 2-9b) was a little higher than those with 4 coats (Figure 2-9a) but not doubling. This might be due to more SiNWs remaining on the rod as the number of coats increased.

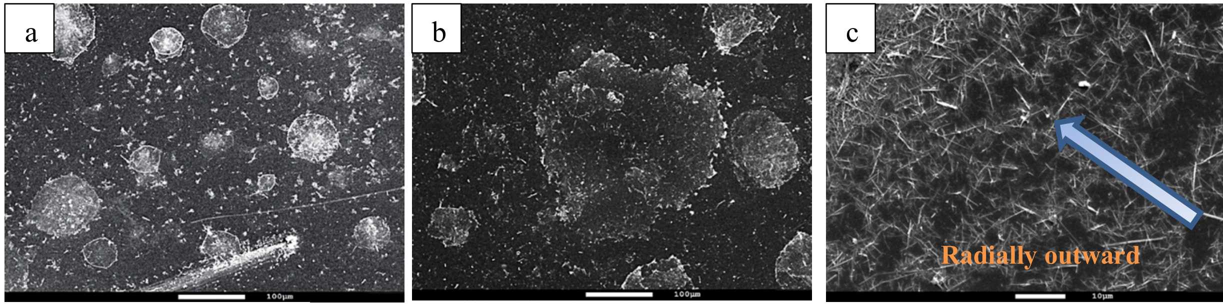

Figure 2-9: SEM characterization of NWs deposited by Mayer rod coating using an RDS #20 rod. a) 4 coats have been applied; b) 8 coats have been applied. The scale bar is 100 µm in both SEM images. c) A magnified view of the circumference of a circle. The scale bar is 10 µm.

Non-homogeneous drying patterns were also observed when a higher density of SiNWs were deposited, this time using an RDS#60 rod with 8 coats. The drying patterns were linear instead of circular (Figure 2-10).

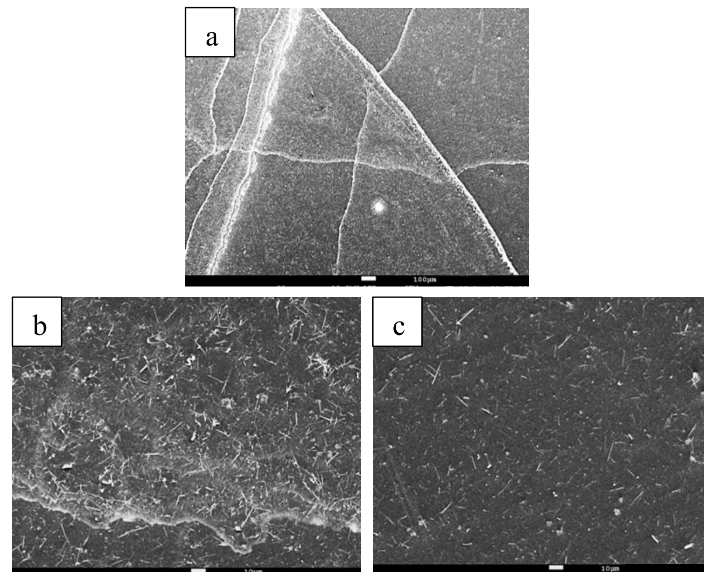

Figure 2-10: SEM characterization on the samples prepared by Mayer rod coating of SiNWs onto a Si substrate using an RDS #60 rod for 8 coats. a) The clear presence of linear drying patterns spanning across the entire substrate. The scale bar is 100 µm; A location further away from the drying lines with much fewer SiNWs present. The scale bar is 10 µm.

To solve the non-uniform dying problem, a surface treatment was used to make the Si substrate surface more hydrophilic to increase its wettability [139] [140]. This was achieved by pre-spraying the Si substrate with IPA [139] or performing the oxygen plasma treatment on

the surface where coating was performed [140], or a combination of both. As demonstrated below in Figure 2-11a), it can be observed that when Si substrate was pre-treated with IPA, then dried with the N_2 gun, before Mayer rod coating, the coffee-ring effect was greatly suppressed and the coating was much more uniform, as compared to samples without such pre-treatment (Figure 2-10). However, the oxygen plasma pre-treatment on the Si substrate worsened the printing results as the linear drying patterns remain as before (Figure 2-11b). Moreover, the density of printed SiNWs was also much lower compared to Figure 2-11a. The combination of oxygen plasma and IPA pre-treatment also did not mitigate the non-homogeneity issue at all (Figure 2-11c), as it also exhibited similar patterns as the samples with oxygen plasma surface treatment alone.

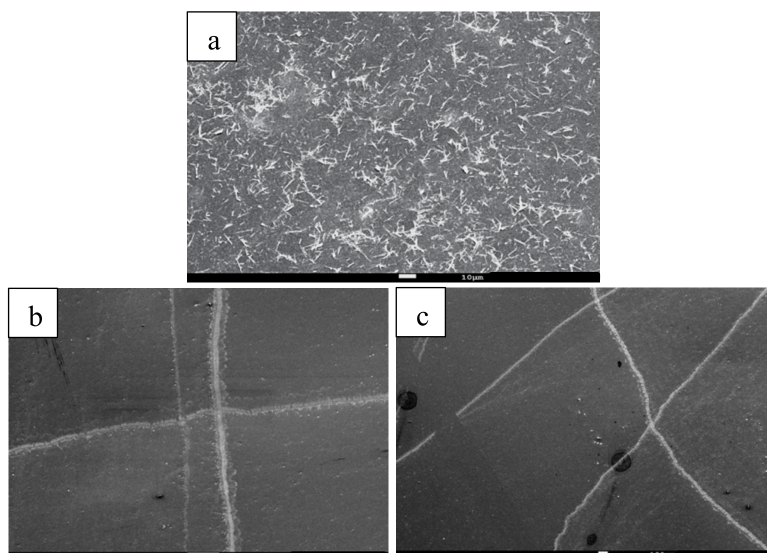

Figure 2-11: SEM characterization on the samples prepared by Mayer rod coating of SiNWs onto a Si substrate using an RDS #60 rod for 8 coats. a) The surface was pre-treating spraying IPA before Mayer rod coating. The scale bar is 10 µm; b) A surface pre-treatment of oxygen plasma is applied right before Mayer rod coating. The scale bar is 100 µm; c) The combination of oxygen plasma and IPA spraying pre-treatment is applied right before Mayer rod coating. The scale bar is 100 µm.

Since the density of SiNWs in Figure 2-11a was still not high enough for forming a connected SiNW network, a thicker film deposition was still required. Consequently, 8 coats

using a RDS #95 rod, which is the highest rod number available from RD Specialties, were applied (Figure 2-12). In addition, SiNWs etched for 120 min was used (rather than the 80 min etch time used for all the rod coated samples presented in Figure 2.7-2.11). This results in a longer NW length which in turn can achieve percolation (a connected network) at lower densities. After dispersion (room temperature ultrasonic bath for 90s at mid power in 2 mL of IPA using one 1 x 1 cm^2 Si substrate), the average NW length was approximately 15 µm, with the longest NW being around 40 µm.

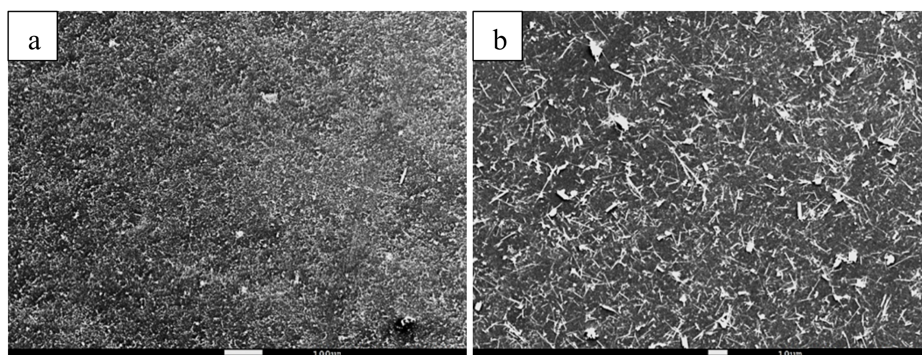

Figure 2-12: SEM characterization on the samples prepared by Mayer rod coating of SiNWs onto a clean Si substrate by using a RDS #95 rod for 8 coats. a) The scale bar is 100 µm; b) The scale bar is 10 µm.

It can be observed that the density of Mayer rod coated SiNWs using RDS #95 for 8 coats (Figure 2-12) increased compared to using a RDS #60 rod. However, it was still not high enough to form an interconnected network of SiNWs. Therefore, efforts were devoted to increase the density of SiNWs in solution. This was done by using only 1 mL of IPA rather than 2 mL. Also, putting 2 etched Si chips in the vial during sonication (Figure 2-13b) was tested and compared to the use of one etched Si piece (Figure 2-13a), where both were sonicated in 1 mL of IPA. Although a darker color was observed in the vial after sonication compared with the use of 1 etched Si chip, there was unexpectedly no discernable increase in SiNW density after printing. However, there was more NW agglomeration. This suggests that

NWs agglomerate if their density in solution is too high. There also may be issues with the 2 Si chips striking on another in the vial during sonication.

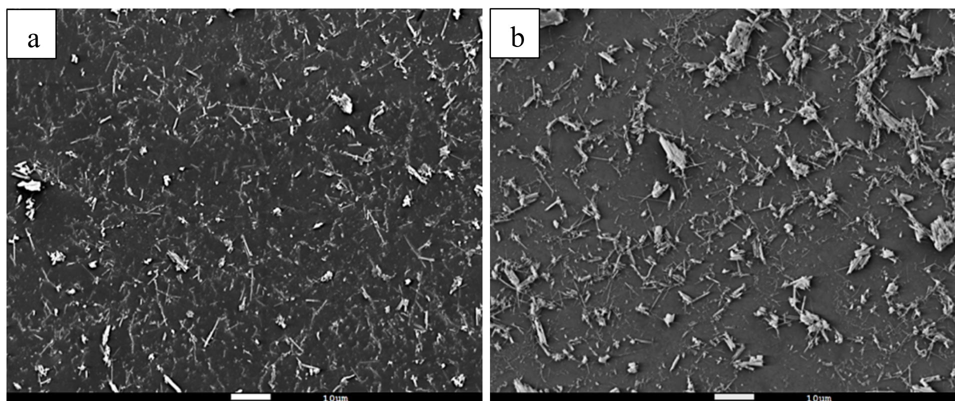

Figure 2-13: SEM characterization of SiNWs rod coatedon Si using a RDS #95 rod for 8 coats and sonicated in 1 mL of IPA. The scale bars are 10 μm. a) One etched Si piece is immersed in IPA during dispersion; b) Two etched Si pieces are immersed in IPA during dispersion. The latter had more agglomeration.

In conclusion, a bottleneck was reached for how dense of a SiNW network could be printed using the method of Mayer rod coating. A connected NW network could not be obtained. The density of NWs in solution could not be increased because it was not feasible to use a lower volume of IPA than 1 mL during sonication, nor was it feasible to use more Si chips together in the vial. Furthermore, results suggested that even if higher concentrations of NWs in solution are obtained, it leads to undesirable agglomeration. The deposition of more than 8 coats is unwieldy and Mayor rods that deposit thicker films of solution are not commonly used. As a result, a third method of vacuum filtration was used to deposit a functional SiNW network with a higher NW density.

2.3.4 Vacuum filtration

As mentioned earlier in Chapter 2.3.1, vacuum filtration is a commonly used method to obtain interconnected films of NWs [66] [74] [128]. In this method, solution containing dispersed NWs is filtered through a membrane. With the help of the vacuum environment

beneath the filter, the liquid flows through the pores of the membrane while the NWs remain on the surface of the filter membrane in a randomly oriented NWs [128]. The pore size is an important parameter: if it is too small, unwanted non-nanowire particles will be included in the film, and if it is too big less NWs will be collected. Vacuum filtration can result in a higher NW density than rod coating because a large volume of solution can be used - it is able to retain and concentrate the NWs to a limited area on the filter membrane. However, the NW network on the filter needs to be transferred to another receiving substrate, which brings processing complexity and raises concerns of lowered NW densities and organic or polymer residuals from the membrane.

Two different types of filter medium were selected. The first was a filter paper with a diameter of 42.5 mm and a pore size of 2 µm. The second was a mixed cellulose ester (MCE) membrane with a diameter of 25 mm and a pore size of 1.2 µm. All of the dispersed SiNWs for vacuum filtration were sonicated at mid power for 90s with 15 mL of IPA, and two such samples (i.e. a total of 30 mL) were used for each run of vacuum filtration.

Figure 2-14: SiNWs retained on the paper filter after vacuum filtration.

The paper filter was used in the initial trial for vacuum filtration. From the immediate presence of brownish color on the filter after filtration (Figure 2-14), it was evidenced that a

sufficient amount of SiNWs were retained. Then, in terms of the transference, peeling off by mechanical means was implemented first as it was the easiest to implement and it was reported as a successful means of transferring NW network to another substrate for further processing [141]. The use of a flat mechanical press was first used to transfer the NWs onto a Si substrate (the substrate was chosen for easier SEM characterization). However, only very few SiNWs came off even when the pressure gauge was set at its maximum value. Pressing at elevated temperature (100 and 120 ˚C) for 1 hour was tested, but still only very few NWs got transferred.

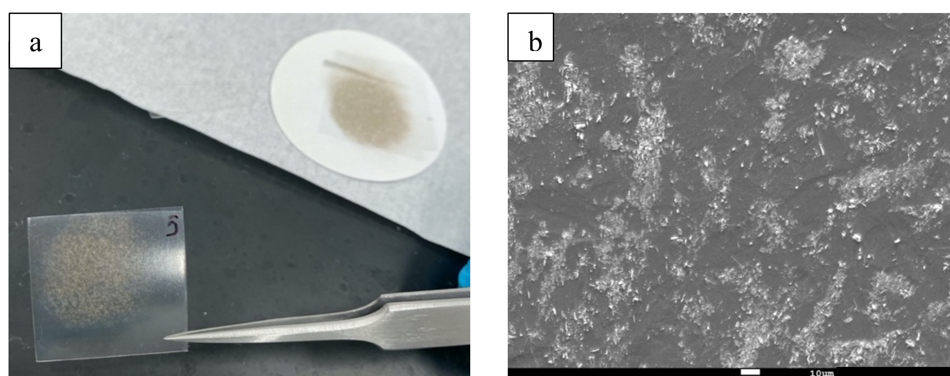

Figure 2-15: Demonstration of the transferring of SiNWs from the paper filter onto the PET substrate through the use of hot-rolling. a) The macroscopic picture showing the successful transfer, where the presence of SiNWs is indicated by the brownish color on the transparent PET substrate; b) The SEM characterization of the transferred networks of SiNWs. The scale bar is 10 µm.

A hot roller (MSK-HRP-01, MTI Corporation) was then experimented with where a polyethylene terephthalate (PET) substrate was selected because hot rolling is only compatible with flexible and soft substrates. 5 rolls at 75 ˚C proved to be a successful initial trial temperature where an adequate amount of SiNWs were successfully transferred from the paper filter onto the PET substrate, as demonstrated below with the apparent brownish color on the transparent PET platform in Figure 2-15a. The SEM characterization in Figure 2-15b also proved the transfer of SiNWs onto the PET substrate where iridium was coated on top of the

PET substrate to allow for better SEM imaging. However, although a significant amount of SiNWs get transferred onto the PET substrate, the density of SiNWs was not high enough to achieve a connected network. Therefore, more rolls using the same hot roller at the same temperature was tied. However, the NWs became permanently stuck on the filter and there was little increase of the NWs transferred to the substrate.

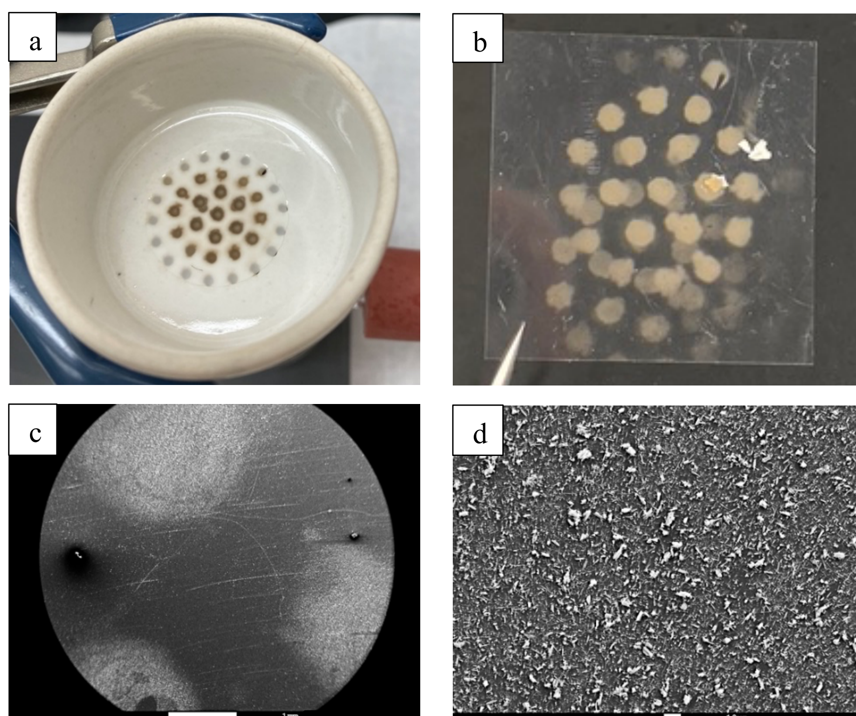

Figure 2-16: a) The successful retaining of SiNWs on the MCE membrane after vacuum filtration; b) Successful transferring from the MCE membrane onto the PET substrate through the use of hot rolling; c) SEM characterization of the PET substrate after transferring the SiNWs. The circular bright parts correspond to the most concentrated circular areas, similar to the example in b). The scale bar is 1 mm; d) A higher magnification SEM image of a circular bright part from c). The scale bar is 10 µm.

The MCE membrane was tested next as it is a common filter membrane used for vacuum filtration especially for transferring networks of NWs onto PET substrates [142] [143]. Hot rolling was used for transfer, with the rollers at 75 ˚C since it is the maximum temperature tolerated by the MCE membrane. As demonstrated in Figure 2-16a, the transfer worked well, and the SEM characterization shows that the density of SiNWs on the PET was a lot higher

than the optimal result using Mayer rod coating. However, Figure 2-16 a-c show that most NWs accumulated on the places corresponding to the position of holes on the funnel, which is undesirable for subsequent device integration.

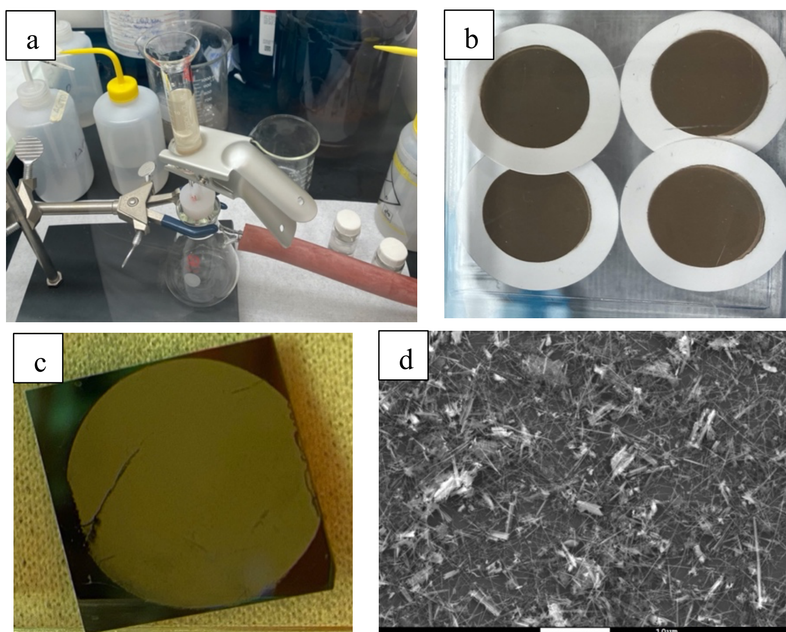

Figure 2-17: a) Demonstration of the updated vacuum filtration setup; b) The uniform distribution of SiNWs across the filtrated area with excellent repeatability; c) The transferred network of SiNWs on a Si wafer chip after membrane dissolution; d) SEM characterization showing the high density of SiNWs transferred. The scale bar is 10 µm.

In an effort to get rid of the circular dense areas distributed across the filter medium, a new vacuum filtration setup was used where the traditional Buchner funnel was replaced by a cylinder tube with openings on both ends and the membrane was placed in between the stopper and funnel (Figure 2-17a). It can be seen in Figure 2-17b that the NWs were deposited uniformly across the inner area of the filter. Secondly, since the SiNW transferring process did not generate a uniform coating over the substrate, a different method of transfer was used: membrane dissolution. In this method, I filtered the SiNWs onto a dissolvable membrane, in this case a porous nitrocellulose membrane which can be dissolved in acetone [74]. The membrane is subsequently placed on the receiving substrate (in this case a Si wafer chip), then

dissolved in an acetone bath treatment leaving only the SiNWs on the receiving substrate. Specifically, the membranes were soaked in an acetone bath overnight where the side with SiNWs is faced down on the surface of the final substrate. After the membrane was fully dissolved, the samples were immersed in IPA and DI water baths for 1 min sequentially in order to clean up the residual organic solvents that may remain on the surface. This procedure was successful; Figure 2-17c) and 2-17d) show that a dense and fairly uniform network of SiNWs was transferred over to a Si wafer chip.

In addition, one-side-polished single crystalline <100> p-type boron doped Si wafers with a resistivity of 0.001 – 0.005 Ω·cm, thickness of 500 μm and diameter of 100 mm were also used to fabricate heavily doped SiNWs with the same metal deposition and chemical compositions as mentioned in subchapter 2.1 and 2.2 for a duration of 210 min, and the same process of dispersion and vacuum filtration was adopted. However, the transfer process failed as the adhesion between the heavily doped SiNW network and the substrate was too weak, which caused the NW network to slide over onto other undesired areas during the membrane dissolution. Future surface modification to enhance the adhesion between NW network and the substrate will be detailed in Chapter 5 as future work.

2.3.5 Printing summary

In conclusion, a combination of vacuum filtration to collect the SiNWs from its solution form and membrane dissolution to transfer the retained SiNWs from the membrane to the final substrate proved to be optimal in constructing a network of SiNWs with high density and good uniformity. The quality outperformed those obtained by transferring through hot rolling or

pressing, as well as printed through drop casting or Mayer rod coating. This is the procedure used to print the SiNWs for electrical characterization in the next Chapter. The method is compatible with flexible substrates such as PET and Kapton, but unfortunately is not scalable. Future work, as discussed in Chapter 5, includes developing a scalable, high-throughput method to deposit the NW networks. Although it didn't work here, I believe Mayer rod coating would still be a good option as it is used in industry to deposit dense networks of silver nanowires. To work, a method to increase the SiNW concentration in solution would be needed, and the surface of the NWs could be treated to prevent agglomeration as is done in many other dispersions of nanoparticles and nanowires.

Chapter 3
Electrical Characterization of Silicon Nanowire Networks

3.1 Device fabrication

After a dense and uniform network of SiNWs was obtained using vacuum filtration and membrane dissolution as discussed in Chapter 2.3, contacts were deposited to characterize the electrical properties of the networks. Both two-terminal and three-terminal configurations were fabricated. For the latter, the SiNW network was the channel material in a thin-film transistor (TFT) which is a back-gated metal oxide semiconductor field effect transistor (MOSFET), as illustrated in Figure 3-1. The TFT configuration permits the measurement of mobility and assesses the NW network as a possible transistor channel material.

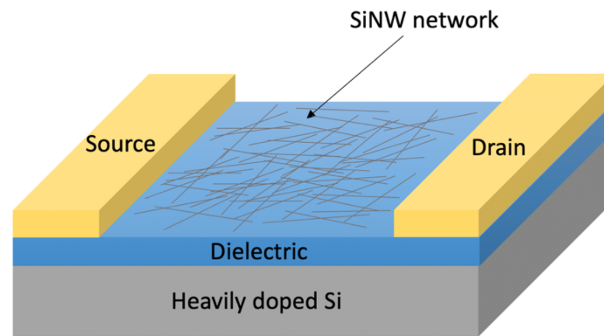

Figure 3-1: Schematic of a thin-film transistor where the SiNW network is the channel material.

The initial fabrication plan is listed below:

Step 1. *Cleave substrate and clean pieces*

For the two-terminal measurements, lightly doped p-type Si substrates with 322 nm thick thermally grown silicon dioxide on top were used. For the TFT devices, heavily doped p-type

Si substrates with 100 nm of silicon nitride, deposited on top using low pressure chemical vapor deposition, were used (purchased from University Wafer). In both cases, the substrates were cleaved into 1.7 cm * 1.7 cm pieces using a dicing saw. These pieces were then cleaned by ultrasonication successively in acetone, IPA and DI water baths respectively for 1 min each, then dried with nitrogen.

Step 2. *SiNW transfer*

Vacuum-filtrated SiNW networks were transferred onto the surface of the diced wafer pieces using the process described in subchapter 2.3.4. The SiNWs used were etched from a Si wafer that was lightly p-type with a resistivity of 10-20 Ω·cm. The NWs had an average diameter of 100 nm.

Step 3. *HF dip*

To remove the native oxide on the outer shell of the SiNWs, the networks were dipped in buffered oxide etchant (1:10) for 30s then dried with N_2.

Step 4. *NW networks anneal*

To lower the resistance at the overlapping NW junctions, the networks were annealed (Allwin21 AW610 Rapid Thermal Processor) at 350 ˚C, 400 ˚C, 450 ˚C, 500 ˚C and 550 ˚C under nitrogen for 1 min respectively.

Step 5. *Second HF dip*

The purpose of this HF dip is to remove any native oxide that forms during step 4 so that the NWs can make good electrical contact with the metal contacts.

Step 6. *Sputter metal electrodes*

120 nm thick aluminum (Al) pads were deposited using sputtering because Al forms an Ohmic contact with p-type Si [144]. Since lightly doped SiNWs are used, the channel conductivity is low and thus switching will still be possible in a transistor with an Ohmic source and drain (i.e. Schottky contacts are not needed). This being the case, Ohmic contacts are preferred to reduce contact resistance. A shadow mask was used (Angstrom Engineering). The channel length ranged from 50 μm to 200 μm (in steps of 50 μm) and had a constant width of 1400 μm. The design sketch of the 50 μm channel length is shown in Figure 3-2, where the two larger pads are designed for easier contact with the probe tips during electrical characterization. The channel length (such as 50 in Figure 3-2) is labelled beside the pad.

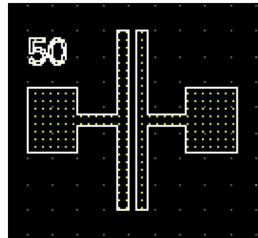

Figure 3-2: Shadow mask design of source and drain electrodes with channel length (L) of 50 μm and channel width (W) of 1400 μm.

Step 7. *Metal/NW contact anneal*

To improve the contact between the Al pads and the NWs, the device was annealed at 400 ˚C for 1 min in nitrogen atmosphere.

A few issues were encountered when carrying out the above steps. Firstly, the HF dip was conducted by immersing the SiNW networks in diluted HF using buffered oxide etchant (BOE, volume ratio of 1:10) for 30s, followed by rinsing 3 times in DI water baths (which is a requirement for any process that uses HF in the Quantum-Nano Fabrication and Characterization Facility (QNFCF)). However, all the NWs were lost during the HF dipping and the following DI water bath rinsing, as shown in Figure 3-3.

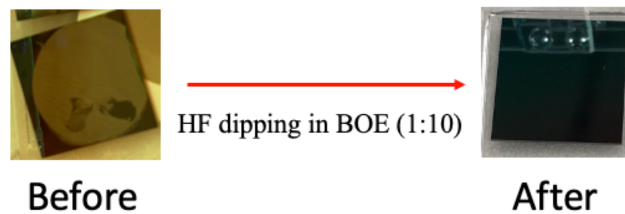

Figure 3-3: Comparison of the substrate before and after dipping in BOE (1:10) for 30s and dried with N_2 gun. The brownish circular-like regions are the locations where there are dense NWs.

There are three possible reasons to account for the loss of NWs. Firstly, for the first devices the dielectric on top of the silicon substrate was SiO_2 and the surface of the oxide layer would have been consumed during the HF dipping. This could have released the NWs that were originally on top of the dielectric surface. Secondly, it is possible that the removal of the oxide around the NWs could lead to the NWs floating and thus easily removed, as illustrated in Figure 3-4. Thirdly, the attraction between the NW network and the substrate was weak, and thus the flow of solution (both the BOE and DI water baths) likely flushed the NWs away from the dielectric surface.

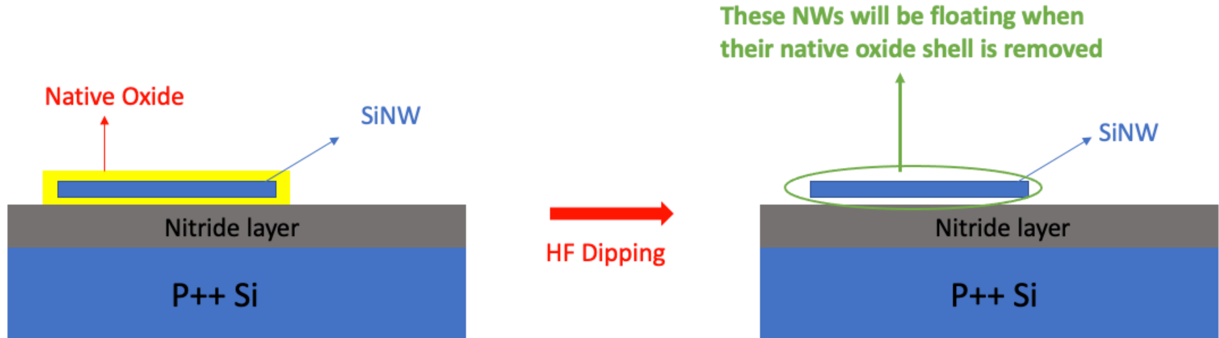

Figure 3-4: One possible failure mechanism explaining the loss of NWs during HF dipping.

Many optimization steps were taken to better preserve more SiNWs on the substrate, which included:

i) Silicon substrates with a Si_3N_4 dielectric layer rather than a SiO_2 layer were used instead since low pressure chemical vapor deposited silicon nitride does not etch in BOE (1:10) [145]. However, 30s of dipping in BOE (1:10) still caused the majority of the SiNWs (~70-80%) to be lost.

ii) The BOE (1:10) dipping time was reduced from 30s to 15s so that the NWs might still be loosely attached to the substrate due to their native oxide shell not being entirely removed. Although this significantly improved the ratio of NWs retained on the nitride surface (Figure 3-5), the NW density was still reduced, and there were

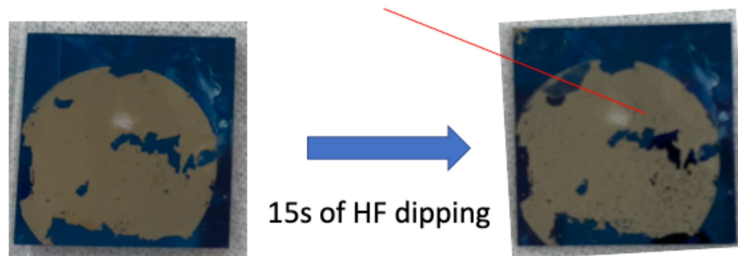

Figure 3-5: Comparison of the same substrate before (left) and after (right) a 15s HF dip.

also many small bare areas (holes) on the substrate where fewer NWs remained. Therefore, the shorter dipping time was still not sufficient.

iii) Using a clipper instead of a dipper (Figure 3-6) to transport the substrate into the BOE. When a dipper was used, a longer initial setup time (15-20s) prior to the 30s dip caused a longer actual dipping duration for certain parts of the sample. This is because the entire substrate was not initially fully immersed in the BOE (1:10). On the other hand, when a clipper was used instead, the above issues were solved easily. However, the downside was that there was BOE (1:10) trapped within the two clips that was hard to remove during DI water baths, which caused continuous etching until the BOE is dried.

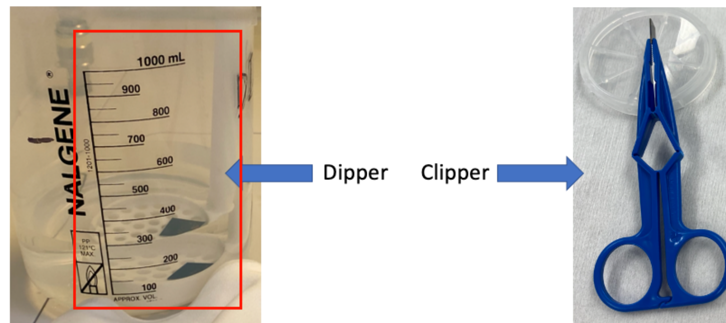

Figure 3-6: Demonstration of a dipper (left) and a clipper (right) to handle the HF dipping (BOE, 1:10) of the sample.

iv) During the drying process with the N_2 gun, a gentle flow was used, and the flow was directed inward (from the surface of the substrate towards the clipper) to prevent water (on the clipper) from reaching the substrate again by accident.

Ultimately, these steps did not lead to enough SiNWs remaining on the substrate. A different method to etch the oxide from the SiNWs, such as using HF vapor (which is not

available at the University of Waterloo), would be needed. Unfortunately, there was not the time nor the resources in this MASc project to properly carry out a better method and thus the HF dipping was skipped entirely. In Chapter 5, a discussion of how the HF steps might be successfully carried out will be presented as future work.

In addition to the problems with the HF dip, it was found out that when the Al contacts were sputtered, there was significant variation between the patterns on the shadow mask and the actual deposited electrodes. In particular, the distance between the deposited electrodes varied from one set of contacts to another, and the average distance between the metal pads was quite a bit smaller than the pattern on the mask. The variation and smaller distances are because of the high energy and short mean free path of the sputtered atoms after they hit the substrate, which causes the movement and random re-deposition of the sputtered atoms into the channel region between the two electrodes. A summary of the deviation of the channel length between the mask and deposited contacts is presented below in Table 3-1.

Table 3-1: Summary of the deviation between the planned and actual device channel length for electrodes deposited using sputtering.

Designed Channel Length (μm)	50	100	150	200
Average Actual Channel Length* (μm)	0	33	106	133
Percentage Deviation	100%	67%	30%	33%

*The calculation is based on the average channel length of 5 devices.

Because of these issues with sputtering, electron beam evaporation (Angstrom Engineering Amod Electron Beam Evaporator) was used to deposit the Al instead. Due to the lower energy and longer mean free path of the evaporated atoms, the deposited electrodes matched well with

the designed shadow mask with only a 1% deviation from the expected channel length (calculated based on the average percentage deviation of 3 devices) and a much smaller variation as well.

The revised fabrication steps for the final devices, with modifications from the initial plan, are listed below:

Step 1. *Cleave substrate and clean pieces*

Step 2. *SiNW transfer*

~~Step 3. *HF dip*~~

Step ~~4.~~ 3. *NW networks anneal*

~~Step 5. *Second HF dip*~~

Step ~~6.~~ 4. ~~*Sputter*~~ *E-beam evaporate metal electrodes*

Step ~~7.~~ 5. *Metal/NW contact anneal*

3.2 Two-terminal measurements

Electrical characterization was performed using a 4200A-SCS Parameter Analyzer and Everbeing Probe Station under dark conditions in air. Two terminal characterization was conducted first, where a voltage bias was applied between the source and drain electrodes on the devices made on a lightly doped Si substrate with SiO_2 on top. Firstly, the effect of annealing on the SiNW network was investigated. For the samples where the Al electrodes

were deposited using sputtering, initial comparison was made between devices with and without an annealing treatment of 500 ˚C for 1 min in N_2. As shown in Figure 3-7, such annealing treatment improved the channel conductivity by doubling the current under the same voltage bias as compared to the samples without such annealing treatment. This is possibly due to the lowering of junction resistance at the overlapping NW junctions. In addition, the current increases as the channel length decreases from 200 μm, 150 μm to 100 μm due to the lower resistance of a shorter channel.

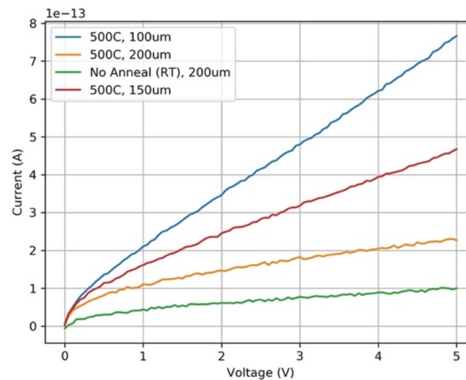

Figure 3-7: Two-terminal characterization showing that a 500 ˚C anneal improves the SiNW network conductivity, and that the conductivity of the channel is higher for smaller channel lengths.

Afterwards, the effect of annealing temperature was investigated, where in this case the Al electrodes were deposited by electron beam evaporation for better accuracy and enhanced batch-to-batch consistency. The two-terminal current-voltage (I-V) plots are shown in Figure 3-8 for NW networks spanning electrodes that are 50 μm apart, each annealed at a different temperature between 350 and 550 ˚C in steps of 50 ˚C. It was found out that devices annealed at 400 ˚C had the highest conductivity compared to the devices annealed at other temperatures under otherwise identical conditions. The annealing temperatures, in order of those which lead to the highest to lowest conductivity, are: 400 ˚C > 350 ˚C > 550 ˚C > 500 ˚C > 450 ˚C > no anneal. Similar I-V characterization was done for NW networks spanning contacts that were

100 µm apart. The annealing temperatures in order of those which lead to the highest to lowest conductivity was the same as for the 50 µm wide networks.

I hypothesize that annealing the NW network increases its conductivity by lowering the resistance of the overlapping NW junctions through sintering, as shown by Ternon *et al* [74]. The annealing treatment on the NW network was performed before metal deposition, which ruled out the possibility of conductivity improvement through the formation of a silicide from alloying metal electrodes and NWs at their contact. The optimal annealing temperature of 400 ˚C is much lower than the melting point of bulk Si (1414 ˚C). This may be explained by the Gibbs Thompson effect which states that an inversely proportional relationship exists between the free energy of the NWs and their diameters. By taking advantage of the nanoscale dimensions (average of ~100 nm in diameter) in such NW structures, the energy barrier for the atoms in the NWs to diffuse onto other NWs can be reduced significantly. As a result, a much lower temperature is able to offer sufficient thermal energy required for NW sintering than its bulk counterpart [68]. Remarkably, the optimal annealing temperature of 400 °C is the same optimal temperature found by Ternon *et al* [74]. The average diameter of the SiNWs in this work, 100 nm, is similar to the diameters used in Ternon's work (which is stated as ranging between 50 and 120 nm). However, there were also many differences. There was a different synthesis mechanism (MacEtch versus VLS), different doping type (p-type, boron doped versus n-type, phosphorous doped) and doping level (light versus heavy), and the presence of

oxide (exists versus removed). More investigation is required for a better understanding of the mechanisms of how annealing influences the NW network conductivity.

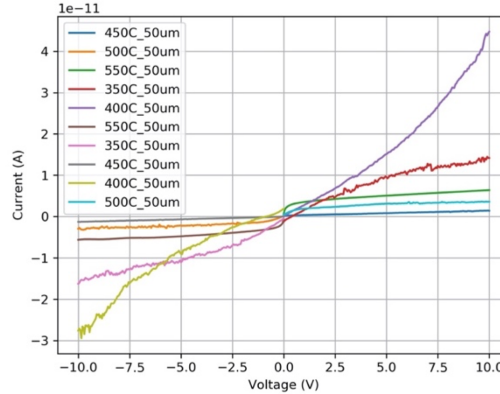

Figure 3-8: Two-terminal I-V characterization comparing NW networks annealed at different temperatures.

In the I-V curves of Figure 3-8, the voltage was swept from -10 to + 10 V, and these curves showed good symmetry around V = 0 which is as expected because the device structure is symmetrical. The shape of the curves doesn't match Ohmic nor Schottky behavior. Clearly, good quality contacts were not obtained, which is expected due to the presence of oxide between the NWs and the metal contacts. The NW/metal contacts have large resistance which played a role in limiting current flow across the semiconductor channel.

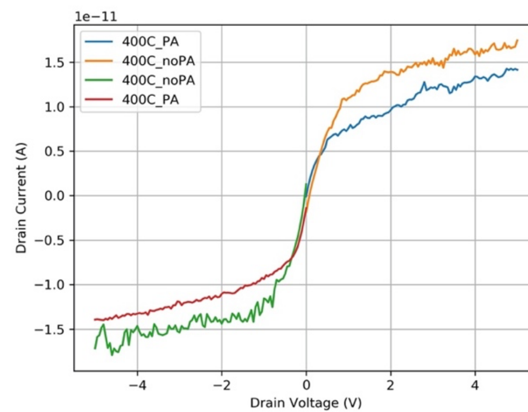

Figure 3-9: 2-terminal I-V characteristic comparing the channel conductivity with and without an annealing after metal contact deposition. "PA" stands for post annealing in the legend.

The effect of the annealing treatment after metal deposition, step # 5 on the revised fabrication list in section 3.1, was also investigated. A rapid thermal processing step at 400 ˚C for 1 min under N_2 was performed on the devices, which is commonly adopted by others as a method to promote better contact between the semiconductor and the metal contact by forming silicide [74]. In Figure 3-9 the I-V curve of a sample with and without a post-metal anneal are shown. The anneal did not have a significant impact on the electrical characteristics of the samples, likely because of the native oxide shell surrounding the SiNWs prevented the formation of silicide.

3.3 Three-terminal measurements

For 3-terminal measurements, an area uncovered by the NW network was used to connect to the gate. The 100 nm thick nitride layer was scratched to expose the heavily doped Si substrate beneath for contact with the probe tip. First the transfer curves were collected (i.e. drain current (I_D) versus gate voltage (V_G) curves). To do this, the source electrode was grounded, and a constant bias was added on the drain while a linear voltage sweep was applied on the gate electrodes to plot the transfer curve of the device. To electrically isolate the heavily doped Si substrate away from the metal probe station, a glass substrate was placed on the probe station first, on top of which the sample was fixed.

The resulting curve is shown below in Figure 3-10. Because the source and drain contacts are not Schottky, current flowed between the contacts at both positive and negative values of V_G – the transistor exhibits ambipolar transfer characteristics. However, as mentioned earlier, decent switching behavior is still obtained because of the low initial conductivity of the channel

which could be significantly increased with the field effect induced by the gate voltage. At negative gate bias, more holes are attracted to the channel, which increases the hole concentration in the p-type channel. At positive gate bias, the channel is in inversion and the I-V has the shape more typical of a MOSFET. I_{ON}/I_{OFF} ratios of 10^3-10^4 were obtained. The shift of the transfer curves at adjacent drain bias conditions is possibly due to the discharging of the trapped charges in defects within the SiNW network and/or the semiconductor-dielectric interface when the gate voltages were continuously swept at different drain biases.

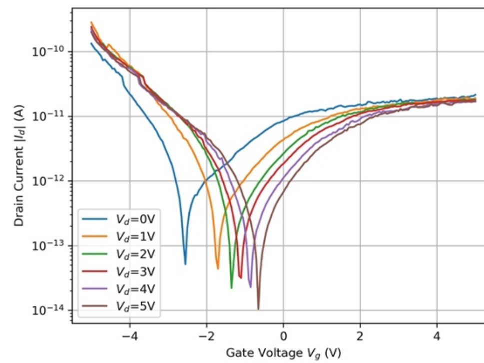

Figure 3-10: Transfer characteristics of TFTs whose channel region was composed of lightly doped p-type SiNW networks. The channel length is 50 µm and an annealing treatment of 500 ˚C was applied on the SiNW network.

Because of the ambipolar transistor behavior, both the electron and hole field effect mobilities were calculated from the drain current (I_D) versus gate voltage (V_G) curve at a chosen drain voltage (V_D) of 0.5 V. To extract hole field effect mobility, the gradual channel approximation was adopted where the square root of I_D versus V_G was plotted, and a linear fit was applied in the region of $-5 \text{ V} < V_G < -2 \text{ V}$ (Figure 3-11a). For the electron mobility, it is the region above $V_G = -2$ V that is relevant. The transistor at these values of V_G is in the linear regime when $V_D = 0.5$ V so a fit was applied to the linear I_D versus V_G curve (Figure 3-11b). The electron and hole mobilities were then calculated from the slope of these curve using

equations (1) and (2) which corresponds to the MOSFET I-V equation in the linear and saturation regime respectively.

$$I_D = \frac{W}{L} C_{ox} \mu \left(V_G - V_T - \frac{V_D}{2} \right) V_D, \qquad V_D < V_G - V_T \qquad (1)$$

$$I_{D_{sat}} = \frac{W}{2L} C_{ox} \mu_{sat} (V_G - V_T)^2, \qquad V_D > V_G - V_T \qquad (2)$$

An average hole field effect mobility of 2.57 x 10^{-5} cm^2/Vs and electron field effect mobility of 3.46 x 10^{-5} cm^2/Vs was obtained. However, the calculated field effect mobilities here do not represent the mobility of the NW network itself, because the semiconductor film is not continuous like in a traditional MOSFET. Rather the current only goes through the thin NW pathways. To calculate mobility more accurately, the effective channel width should be the diameter of one NW multiplied by the number of NW pathways formed between the electrodes, which is roughly estimated to be 280 µm (2800 * 0.1 µm) based on the SEM image in Figure 2-17d, which is one fifth of the channel width (1400 µm). Also, the gate capacitance was calculated based on the parallel plate model, which is an overestimation in this case because the areal coverage of the NW network is less than for a continuous film. This underestimates the actual mobility value, as similarly observed in the characterization of the mobility of an ambipolar field effect transistor with random networks of carbon nanotubes as the channel. This study reported a 50% and ~25% increase in their hole and electron mobility calculation respectively after using a modified model to better evaluate the capacitance of the gate dielectric [146]. Thirdly, the network deposited was sparse. Higher currents would be obtained by using a network with a higher NW density, which is expected to result in a much

higher calculated channel mobility as observed for both the case of Si nanoparticle [147] and carbon nanotube [148] TFTs. Even accounting for all these factors, the network mobility is still very poor. This is likely due to the existence of native oxide that was not removed.

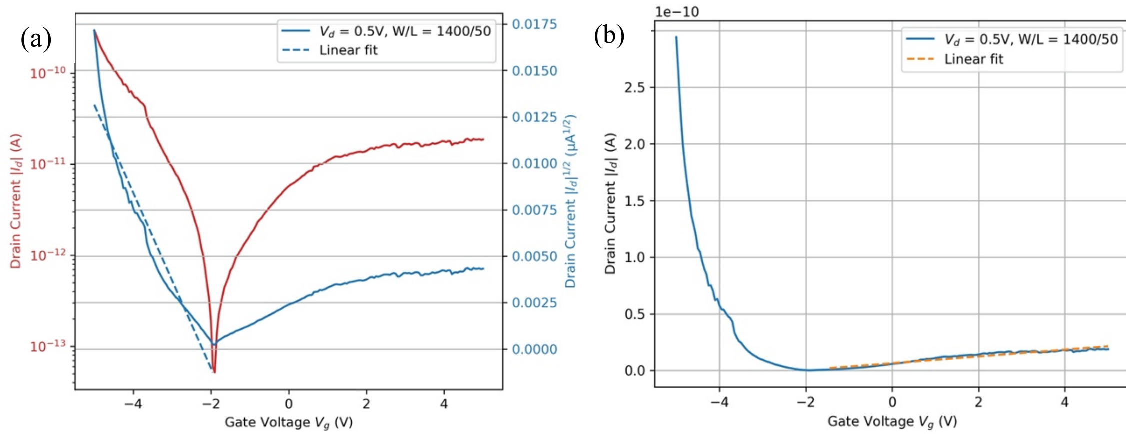

Figure 3-11: Transfer characteristics of lightly doped p-type SiNW TFTs at V_D = 0.5 V. (a) Transfer characteristics plotted in logarithmic scale (left axis) and square root (right axis) and hole mobility is extracted from the accumulation region. (b) Transfer characteristics plotted in linear scale to extract the electron mobility from the inversion region. The channel length is 50 µm and an annealing treatment of 500 ˚C for 1 min under N_2 was applied on the lightly doped p-type SiNW network.

To improve the electrical results, the following two steps were added to subsequent samples. First, the entire vacuum filtration step was moved from our own lab to the Quantum Nano Fab so that air exposure of the samples could be limited between the vacuum filtration of the SiNWs and the membrane dissolution step, for the purpose of reducing native oxide formation surrounding the SiNWs. In order to pursue identical parameters to match the original setting in our own lab, the vacuum intensity for vacuum filtration was adjusted to the same level (24’’ psi) as measured by the pressure gauge, and additional connecting tubes, an adjustable switch as well as a tightening ring was added, as depicted in Figure 3-12.

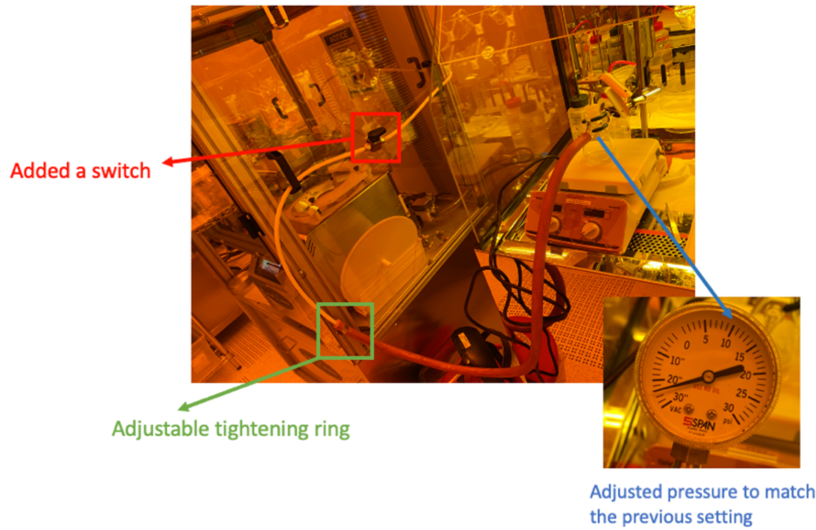

Figure 3-12: Photo of the vacuum filtration setup within the Quantum Nano Fab.

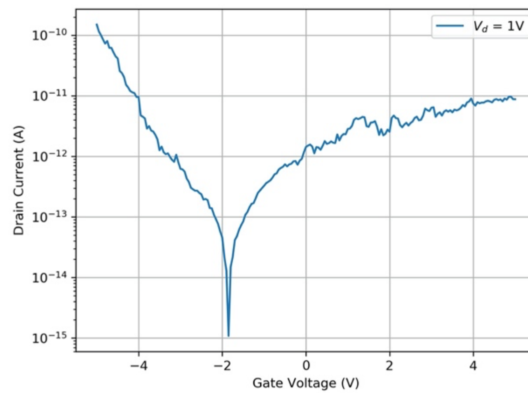

Figure 3-13: Transfer characteristics of lightly doped p-type SiNW TFTs at V_D = 1V plotted in logarithmic scale. The channel length is 50 µm and an annealing treatment at 400 ℃ for 1 min under N_2 was applied on the lightly doped p-type SiNW network.

By shortening the duration of sample's air exposure through this method and employed an annealing treatment at 400 ˚C for 1 min under N_2, a further improvement on the I_{ON}/I_{OFF} ratio of ~10^5 was achieved at V_D of 1V, which is presented below in Figure 3-13. This ratio is higher than TFTs whose channel was composed of randomly oriented carbon nanotubes, such as an

I_{ON}/I_{OFF} ratio of ~100 reported in Snow *et al*'s work [149], and an inkjet-printed organic thin film transistor ($I_{ON}/I_{OFF} = 10^4$) [150].

3.4 Conclusion

Although a large I_{ON}/I_{OFF} ratio of ~10^5 can be achieved, the mobility of the SiNW network is poor. The low mobility is attributed to the presence of the native oxide shell surrounding the SiNWs as well as oxide existing between the NWs and the metal contacts, which limits the current flow and deteriorates the channel conductivity. Suggestions of surface modification and the use of photolithography to possibly incorporate HF dipping while preserving the SiNWs from getting flushed away from the surface will be discussed in Chapter 5 as future work.

Chapter 4
Rod coating of graphene oxide

4.1 Introduction

In this chapter a project on the rod coating of graphene oxide (GO) flakes is covered. This was a side project during my MASc studies and is a departure from the main goal of this thesis. However, the work is still briefly included here because 2D flakes are a potential alternative printed semiconductor to silicon nanowires. As discussed in Chapter 1, graphene and metal dichalcogenides such as MoS_2 are being explored by others as a printable semiconductor. Many methods for the deposition of graphene and other 2D flakes into films have been explored including spin coating [151], the Langmuir-Blodgett technique [152], inkjet printing [32] and vacuum filtration [153]. However, none of these methods meet all the deposition requirements of printed, flexible electronics including large-area, high-throughput continuous deposition, simplicity, and low cost [154]. A review article by Wang and Liu [154] state that solution-processed 2D materials have high promise for electronic and optoelectronic applications because of their diverse electrical (demonstrating metallic, semiconducting or dielectric behavior) and optical properties (showing transparency or non-transparency) while can be mass produced at the same time, but the authors identify the need for better film assembly techniques as a key challenge [154]. Rod coating meets all the criteria listed above but has been under-explored for the assembly of 2D-flake films. Through this project, I show that it is a promising method for printing films of 2D flakes.

This project is a collaboration with Dr. Marika Schleberger's research group from the University of Duisburg-Essen in Germany. The motivation for the project is not for printed,

flexible electronics, however the target goals of the deposition is very similar to what is needed for printed electronics: to print a thin film of 2D flakes on plastic with high uniformity. The application of this particular project is to use graphene as a nano-porous membrane. Such graphene membranes have become a promising candidate for biomedical and environmental applications such as artificial kidneys [155] and water desalination [156]. This is because graphene demonstrates superior mechanical strength with a single layer thickness as thin as 0.3 nm, and nano-porous graphene has high permeability to water and gases, which is ideal for thin membrane devices [155]. Previously, the fabrication of such functional membranes by Dr. Marika Schleberger's group fabricated nano-porous graphene membranes on polymer supports by irradiating graphene films with ions to create atomic-sized pores. However, the graphene films were obtained on polyethylene terephthalate (PET) by transferring CVD-grown graphene layers from a copper substrate, which is expensive and not scalable. Thus, because our group has extensive experience with the Mayer rod printing technique, Dr. Schleberger asked us to rod-coat graphene flakes as a simpler, cheaper and more scalable method to deposit these membranes. The goal of my deposition was to rod-coat a film of graphene oxide flakes on PET that had a high surface coverage of 98 – 99.9%, while being as thin as possible so that size-controllable pores could still be created through the swift heavy ions in the film [155]. I explored the optimal parameters that could lead to this, while Dr. Schleberger's group will continue with the reduction of GO, then create the nanopores.

The experimental parameters include the concentration of the GO, the rod number and number of coats which dictate the thickness of the solution that is deposited onto the substrate,

different receiving substrates as well as surface treatments. Discussions will be presented in the following subsections.

4.2 Experimental procedures

The setup of the Mayer rod coating process was very similar to what was demonstrated earlier in Chapter 2.3.3 on the Mayer rod coating of SiNWs. The GO flake solution shipped from Dr. Marika Schleberger's group was used as the starting solution and as the reference for the concentration after dilution. For example, a concentration of 0.1 mL/mL means a dilution to one tenth of its original concentration, which was obtained by mixing 1 mL of the original GO with 9 mL of DI water.

The process of the Mayer rod coating went as follows. First, 10 mL of homogeneous GO solution with a concentration of 0.1 mL/mL was transferred to a glass vial for easier handling and further processing. Then, the glass vial was shaken for 3 min by hand to help distribute the GO flakes in the solution. Afterwards, 25 µL of such solution was drop casted along one side of a Si substrate (1 x 1 cm^2) which was then drawn across the entire surface from top to bottom using the Mayer rod. Initially, RDS #10 (RD Specialties) with a wire diameter of 0.25 mm was selected and 4 coats were performed along each side of the Si square substrate. Here the Si substrate was chosen instead of PET in the first trial for easier imaging with SEM. Figure 4-1 showed the result of SEM characterization under such conditions.

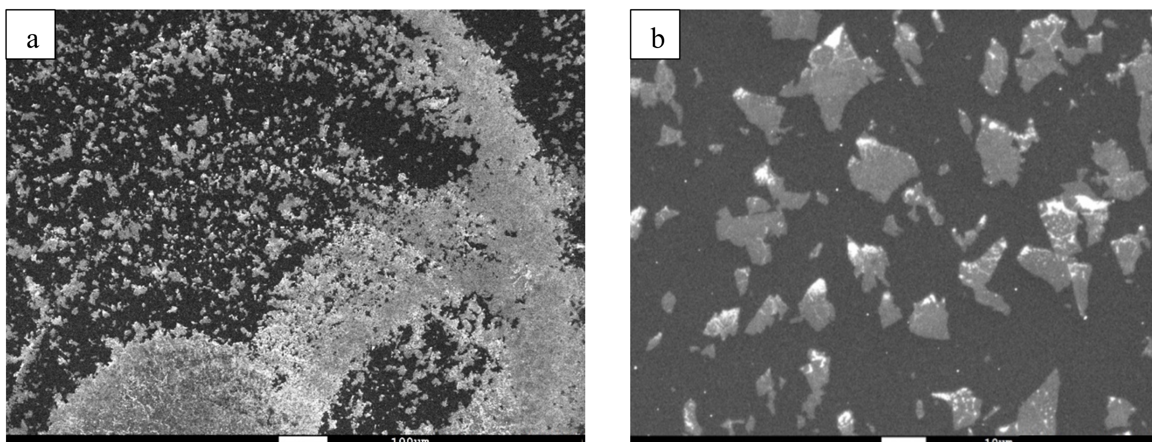

Figure 4-1: SEM characterization of rod-coated GO solution on Si substrate using RDS #10 with 4 coats at two different magnifications. a) scale bar is 100 µm; b) scale bar is 10 µm.

As is demonstrated above in Figure 4-1, a continuous film with high coverage ratio was observed in some regions of the substrate, while in other regions the density was still low. The overall uniformity was good but could be improved. To achieve better uniformity, the vial containing the GO solution was subjected to an additional treatment of an ultrasonic bath for 1 min before the hand shaking of the diluted solution and subsequent Mayer rod coating. The corresponding SEM characterization is shown below in Figure 4.2. It can be noticeably observed that the additional ultrasonic bathing treatment contributed to a much more uniform distribution of GO over the entire Si substrate, with no appearance of flake damage (eg. flakes remained the same size). Therefore, ultrasonic bathing of 1 min was added prior to the Mayer rod coating for all the following runs of experiments.

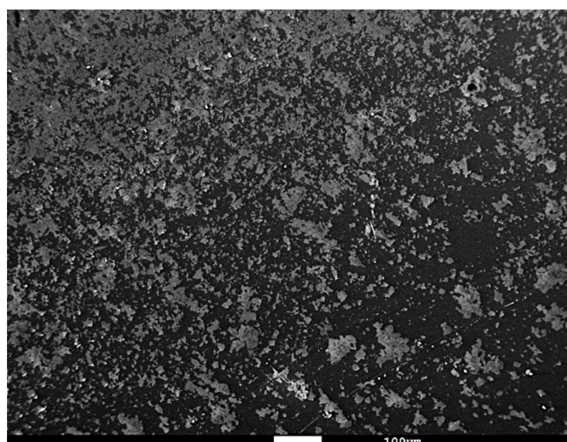

Figure 4-2: A comparison of the SEM characterization of rod coated GO solution on a 1 x 1 cm2 Si substrate using RDS #10 with 4 coats. Scale bar is 100 µm. The additional ultrasonic bath of 1 min was added prior to the Mayer rod coating.

The other problem that needed to be dealt with was the surface coverage, which was much lower than the required 98% and above. To tackle this problem, a wire rod with a larger wire diameter (which corresponds to the printing of a thicker film) was adopted. In particular, rod numbers 60 and 95 were used along with 4 coats applied on each of the four side of the Si substrate. It can be concluded from the SEM characterization in Figure 4.3 that, as the film thickness increased with a higher rod number, the surface coverage ratio increased further as well. Also, the GO film on the Si substrate was more uniform for samples deposited with RDS #95 compared to RDS #60, indicating that a thicker film suffered less from agglomeration and non-uniformity.

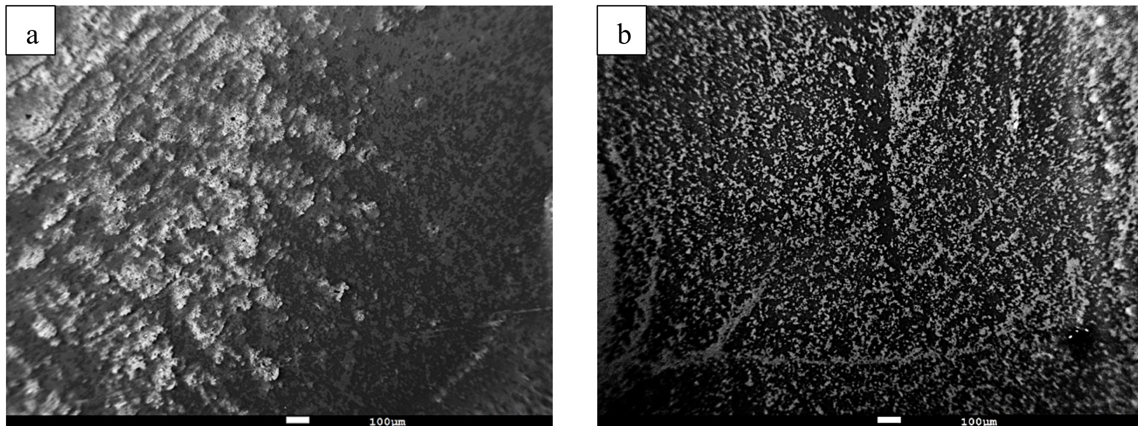

Figure 4-3: A comparison of the SEM characterization of rod-coated GO flakes on Si with 4 coats. Scale bar is 100 μm. a) The Mayer rod #65 was used; b) The Mayer rod #95 was used.

Since the surface coverage ratio still did not meet the goals of 98% or above, a higher concentration of GO was made in an effort to further increase the coverage ratio. After a 4X increase in the concentration of GO (obtained by well mixing 4 mL of the original GO with 6 mL of DI water) while maintaining the rest of the parameters the same (ultrasonic bathing for 1 min before the hand shaking and 4 Mayer rod coats with rod #95 on a Si substrate), a surface coverage of 85.95% was obtained (coverage ratio calculated using ImageJ), and the uniformity was simultaneously maintained well. The SEM characterization of the coating result is shown below in Figure 4-4.

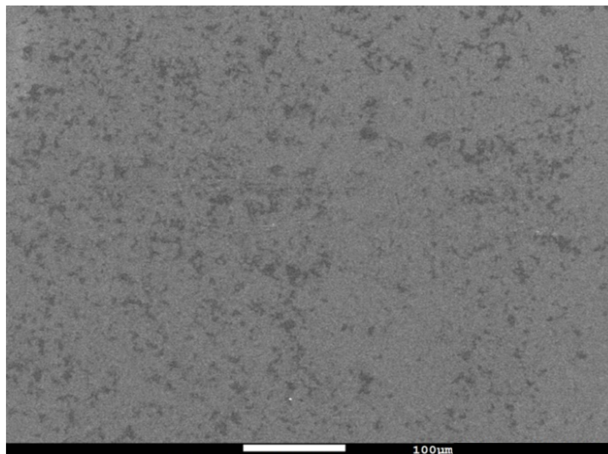

Figure 4-4: The SEM characterization of rod-coated GO solution with a relative concentration of 0.4 mL/mL on a Si substrate with 4 coats. Scale bar is 100 μm.

Then, to further increase the surface coverage ratio, relative concentrations of 0.4, 0.5, 0.6, 0.7, 0.8 mL/mL were prepared to investigate the optimal concentrations that would lead to the best results in terms of uniformity and coverage ratio. The coverage ratio increased gradually as expected, with the highest coverage ratio reaching 96% at 0.8 mL/mL of concentration for four coats on Si substrate, as shown below in Figure 4-5. A further (but small) increase above 0.8 mL/mL is expected to raise the coverage ratio to >= 98% with the same rod number and number of rod coats.

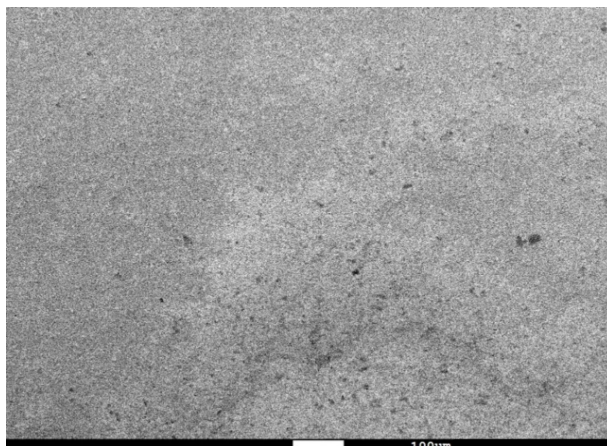

Figure 4-5: The SEM characterization of rod-coated GO solution with 96% surface coverage, obtained using a relative concentration of 0.8 mL/mL on a Si substrate with 4 coats. Scale bar is 100 µm.

I did not characterize the thicknesses of the deposited films as Dr. Schleberger’s group will do this. Thickness can be assessed with atomic force microscopy (AFM). However, the SEM images at increasing flake densities imply that for the highest surface coverage of films I obtained (96%), most of the film was only one or two monolayers, and the rod-coated film demonstrated very good uniformity across the entire surface, which satisfies the goals of printing 2D graphene flakes for nano-porous membranes. As the film coverage ratio increases further (>96%), imaging become harder as there is less open space within the GO film for proper contrast as per needed by SEM characterization.

Similar observations were found on PET substrates. The surface of PET was pre-treated with ultrasonication for 1 min in acetone, IPA and DI water before oxygen plasma cleaning to increase the hydrophilicity of the surface to facilitate easier coating.

4.3 Conclusion

The best set of parameters which led to 96% surface coverage with excellent uniformity and maintaining a thin film was to rod coat with an RDS #95 rod for 8 coats using the relative concentration of 0.8 mL/mL. The thicknesses of these films will be measured by Dr. Schleberger's group, after which time they will tell us what target in the 98 – 99.9% coverage range is desired. There is a trade-off: at the higher end of surface coverage there will be more locations with 2 or more flakes stacked on top of one another.

More generally, it was found that rod coating is a very simple way of obtaining very thin, uniform films of 2D flakes. Agglomeration of flakes was an issue that was very easily overcome by better dispersing the flakes in solution using ultrasonic treatment. The fact that rod coating is cost-effective, simple, and compatible with large-area and continuous assembly makes it an excellent candidate for the printing of 2D flake-based semiconducting films. Future work on post-deposition processing and testing of the electrical (and optical) properties of rod-coated 2D-flake films is recommended.

Chapter 5
Conclusion and Future work

5.1 Summary

In this thesis, SiNWs were synthesized through a wet chemical method – metal assisted chemical etching. NWs with homogeneous diameters averaging 100 nm and lengths of up to 62 µm were successfully fabricated under room temperature and ambient atmosphere. This is a relatively simple, inexpensive method to fabricate large batches of SiNWs with single crystallinity and is thus a fitting method for NWs to be used in printed electronics. The etched SiNWs were then harvested off the source substrate and dispersed in IPA using ultrasonication with minimal agglomeration, thereby rendering the NWs 'printable'. A combination of vacuum filtration and transfer printing was used to successfully deposit SiNW networks. The Mayer rod coating method was also studied, which represents the first time in the literature rod coating has been used to print SiNWs. With this method, NW networks with sufficient density were not obtained due to the low concentration of SiNWs in the ink. However, there are likely methods to increase the concentration of SiNWs in solution. Also, to avoid agglomeration, proper ink formulation would be needed which would likely include a surface treatment on the NWs to prevent agglomeration.

Thin film transistors based on such networks of SiNWs were fabricated, where the as-transferred SiNW networks act as the channel between source and drain electrodes. The effect of post-processing annealing was studied, and an annealing treatment at 400 ˚C on the SiNW network for 1 min under N_2 can improve the channel conductivity by more than double compared to samples without such post-annealing treatments. An I_{ON}/I_{OFF} ratio of $\sim10^5$ was

obtained. However, the mobility of the SiNW networks is poor. It was found that the typical method of removing oxide from the Si – dipping the Si in diluted liquid HF or buffered oxide etchant – was not compatible with SiNWs on a substrate because the NWs were removed from the substrate. Thus, the native oxide shell surrounding the NWs as well as the oxide present between the NW and metal contacts was not removed, leading to the poor mobility. Suggestions on compatible strategies of oxide removal is discussed in the next subchapter. Overall, it was shown that using SiNWs to enable printable silicon shows some promise, but more research needs to be done to properly evaluate their potential.

5.2 Future work

The most important future work would be to find a method to make NW oxide removal compatible with the SiNW network. I have a few suggested strategies to pursue.

Firstly, it would be worth a consideration to remove the oxide surrounding NWs using HF vapor, as shown in Ternon's work [74].

A second approach could be to implement a surface treatment on the dielectric layer and/or the surface of the SiNWs to enhance the adhesion between the NWs and the substrate. If the adhesion is strong enough, the SiNWs would not be removed with the post-HF DI water rinses. For instance, Heo *et al*'s showed that coating SiNWs with amine-terminated aminopropyltriethoxysilane (APTES) can enhance their adsorption onto substrates with a carboxyl-terminated self-assembled monolayer [157]. This adsorption results from the electrostatic charge interaction between the treated NWs and the treated surface. Then the APTES coating as well as the native oxide of the NWs can be removed in a buffered oxide

etching process. As an additional advantage, such amine-functionalized NWs treated with APTES also exhibits better dispersions in DI water. Similarly, another study by Chryssikos *et al* [147] functionalized a SiO_2 surface with 1,10-decyldiphosphonic acid molecules which improved the attraction between the surface and silicon nanoparticles.

A third suggestion is to use photolithography to deposit the metal contacts instead of a shadow mask with advantages as listed below. Firstly, if an HF dip is employed after the photoresist is deposited and before metal deposition (Figure 5-1a), the native oxide on the exposed ends of NWs beneath the metal deposition regions will be removed without the NWs being rinsed away since they are anchored by the photoresist. Then, after metal deposition and removal of the photoresist, the second HF dipping can be applied to remove the native oxide on the NWs in the channel region (Figure 5-1b). The ends of the NW network beneath the metal electrodes can potentially help anchor the SiNW network and prevent them from being rinsed off in the DI water bath.

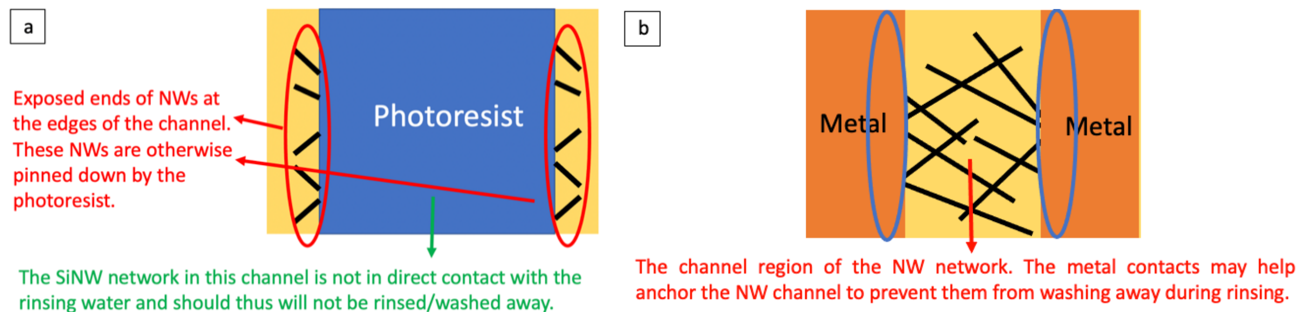

Figure 5-1: Schematic diagram showing the structure of the device before the first (left) and second (right) HF dipping.

A fourth suggestion would be to develop a plasma etching recipe that can selectively etch and remove the oxide shell surrounding the NWs without damaging the NWs or the dielectric surface.

Other than developing a method to remove the native oxide from the NWs, below is a list of suggested future work:

- Establish a scalable method to print the SiNW networks. Rod coating may be a good method. The SiNW concentration in the ink needs to be increased beyond what was achieved in this work, and the ink would need to be properly formulated to prevent NW agglomeration.
- Explore how the optimal annealing temperature of the NW network depends on NW diameter, and in particular see if thinner diameter NWs can lower this optimal temperature.
- Print and fabricate SiNW network-based devices on flexible substrates such as Kapton.
- Characterize the electrical properties of printed SiNW networks made from VLS-grown SiNWs and compare their performance to that of MacEtched SiNW networks.
- More study is needed on the metal contacts to the SiNW networks such as choice of metal, the electrical properties of the contact, and optimal processing methods.
- Test the impact of NW density on the performance and properties of thin-film transistors.
- Test the mechanical flexibility of printed SiNW networks and the impact of bending and stretching on the network's electrical properties.

- Test the electrical lifetime SiNW networks.
- Evaluate device-to-device variance of SiNW transistors.

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