Investigation on performance enhancement of micro-sized IR photodetectors

by

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A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Master of Science
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2021

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

As an Infrared detector with high responsivity, high transmission speed, and low dark current, InP/InGaAs p-i-n photodetectors (PD) have been used as a promising technology for many applications, including optical communication and various imaging applications, for over two decades.

In the following optoelectronic devices scaling down, such as micro-sized light-emitting diodes (LEDs), the integration of PDs in micro-sizes may find a more important position in the near future. Device size shrinkage would be essential to achieve a low dark current and a low depletion capacitance. However, the biggest technical challenge with the conventional micro-size p-i-n detector is producing a significant dark current due to surface recombination. The increased surface area to volume ratio leads to a high carrier surface recombination rate, which significantly degrades the performance of InP-InGaAs micro-sized PDs, including the responsivity and detectivity.

In this case, the most important parameter affecting device performance is the surface recombination velocity (SRV), reflecting the impact of surface recombination rate, depending majorly on the etching process and the passivation layer quality.

This thesis investigates the size-dependent properties of the micro-sized PDs, such as dark current, capacitance, and responsivity. In this work, the simulation tool Atlas SILVACO is employed to simulate the optoelectrical properties of the devices and Finite Difference Time Domain (FDTD) for the optical simulation.

The simulation results show that the responsivity of micro-sized PDs decreases from 80% to 15% when the size shrinks down from 100 μm to 10 μm. To suppress this performance degradation, we went through two different investigation routes.

First of all, we studied two different top surface configurations to couple more light into the micro-sized PDs. Both optical and optoelectrical simulations showed that the configuration with one-sided contact improves the generation rate, reflectivity, and responsivity by ~33%.

Secondly, we scrutinized the enhancement of the gating technique in the performance of the micro-sized PDs. By changing the surface potential and electron concentration at sidewalls, this technique helps to decrease the dark current density in reverse gate biases. The increment of this method for external quantum efficiency (EQE) was ~18%.

Acknowledgments

I would like to thank my supervisor, Prof. Dayan Ban, for his patience and encouragement throughout my Master's studies. This work would not have been possible without his support and guidance.

I want to express my gratitude to the readers of this thesis, Professor Bo Cui and Professor Guoxing Miao.

My deepest gratitude goes to Dr. David Hwang and Dr. Shazzad Rassel for sharing their research experience with me.

I would like to thank my friend Sina, Nani, and Martins for their encouragement and company.

This work would not have been finished without the help and support of my colleagues. I would like to express my gratitude to Jian, Boyu, Masud, Fahim, Siyi, Asif, and Burak for their company and interesting discussions during my Master's studies. It is my pleasure to work with them, and I really enjoy it.

Finally, I must express my profound gratitude to my wife for all the mental support throughout all those years. This accomplishment would not have been possible without the support from my family. Thank you.

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Table 4.1. The main parameters used in the SILVACO Atlas simulation

List of abbreviation

IR	Infrared
NIR	Near Infrared
SWIR	Short wave IR
MIS	Metal-insulator-semiconductor
CV	Capacitance-voltage
DC	Direct current
NDC	Negative differential capacitance
FPA	Focal plane arrays
EQE	External quantum efficiency
DD	Drift-Diffusion
SRH	Shockley-Read-Hall
TAT	Trap-assisted tunneling
BTB	Band-to-band tunneling
RT	Ray tracing
TMM	Transfer matrix method
FDTD	Finite difference time domain
PECVD	Plasma-enhanced chemical vapor deposition
G-R	Generation-recombination
ICP	Inductively Coupled Plasma
LED	Light-emitting diode
OLED	Organic Light-emitting diode
PD	Photodetector
SRV	Surface recombination velocity

Chapter 1 Introduction

1.1 Background and motivation

Sir William Herschel discovered infrared radiation in 1800. He used a prism to separate the spectral components of sunlight. Then he used a thermometer to measure the energy distribution of different colored rays in the spectrum of sunlight. He noticed an interesting phenomenon: the temperature increased beyond the visible spectrum's red end. He discovered that the spectrum of light contains some form of invisible rays in this way.[1]

The electromagnetic spectrum's infrared (IR) spectral region is depicted in Fig. 1.1. The IR region begins where the human eye stops seeing. Near IR (NIR) or Short Wave IR is the first IR region (SWIR).

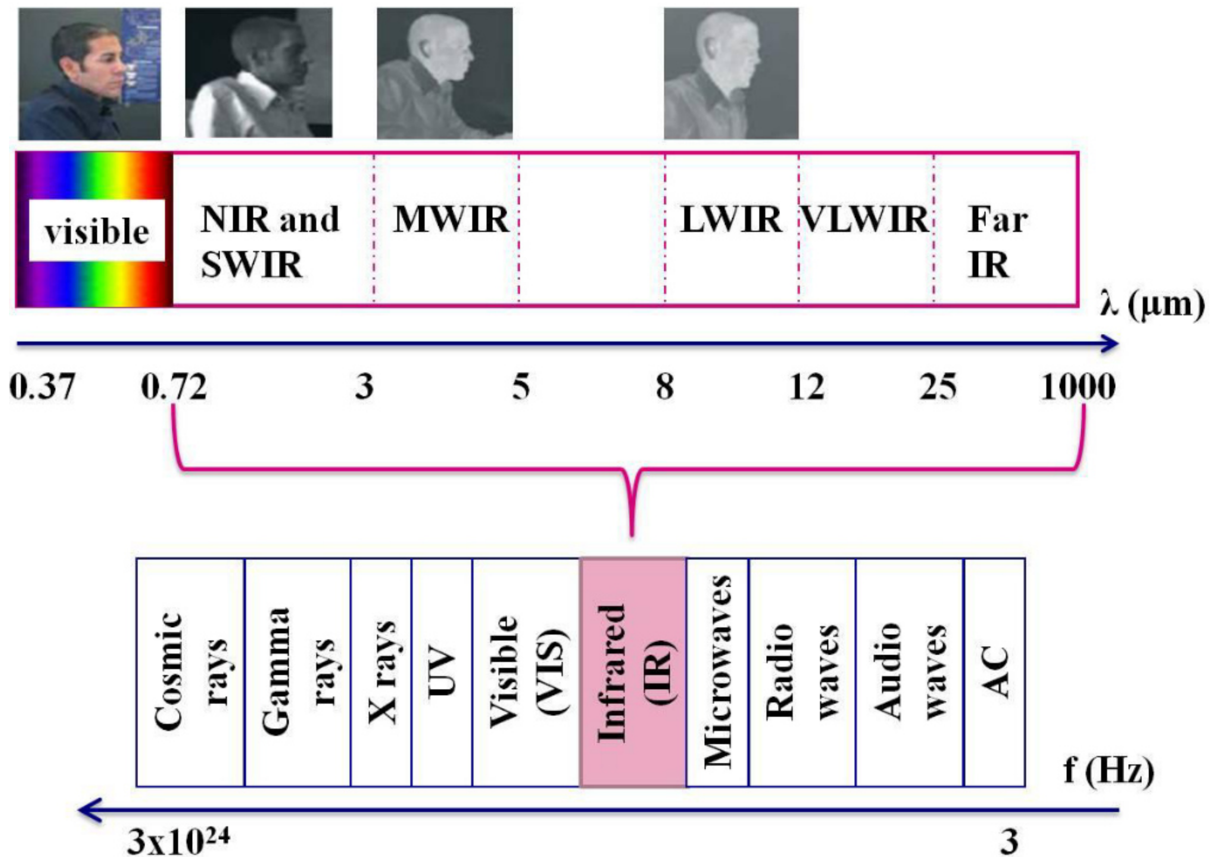

Figure 3.1 IR and visible ranges in the electromagnetic spectrum [1]

In photon detectors, incident photons interact with electrons that are either bound to lattice atoms, impurity atoms, or free electrons, absorbing IR radiation. Figure 1.2 [1] depicts these mechanisms. Photon detectors have a high detectivity as well as a short response time, and their responsiveness is wavelength-dependent. Photon detectors are intrinsic, extrinsic, free carriers, and quantum well detectors based on the nature of the electron-photon interaction. Photon detectors can also be classified based on their electrical output, such as photoconductive, photovoltaic, capacitance, and photoelectromagnetic.

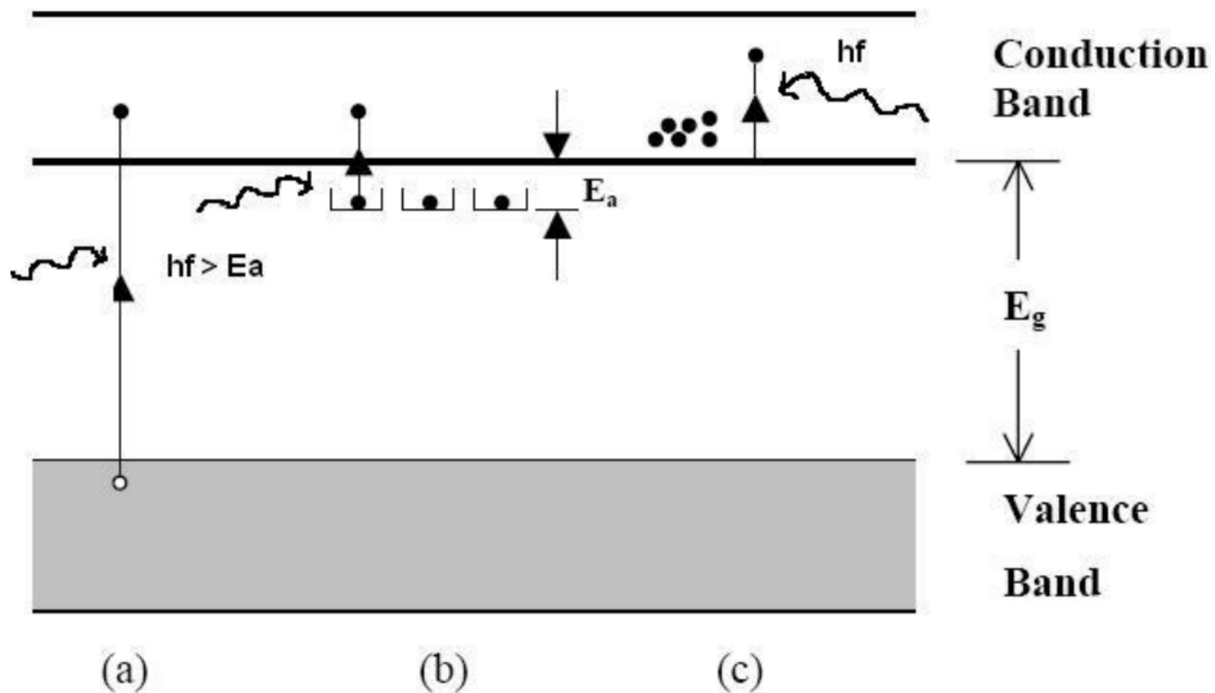

Figure 1.4 Basic optical excitation processes in the semiconductors: (a) intrinsic absorption, (b) extrinsic absorption, and (c) free carrier absorption [2].

Photovoltaic detectors are the most common. They have a built-in electric field and an internal potential barrier. P-n or p-i-n diodes, heterostructure diodes, Schottky barrier diodes, and metal-insulator-semiconductor (MIS) photo-capacitor devices are the most common photovoltaic detectors. The geometry and operation of a simple photodiode are shown in Fig. 1.3. In p and n-type regions, incident radiation produces electron-hole pairs. The strong electric field of the depletion region sweeps these electrons and holes to the opposite side as they diffuse towards the junction.

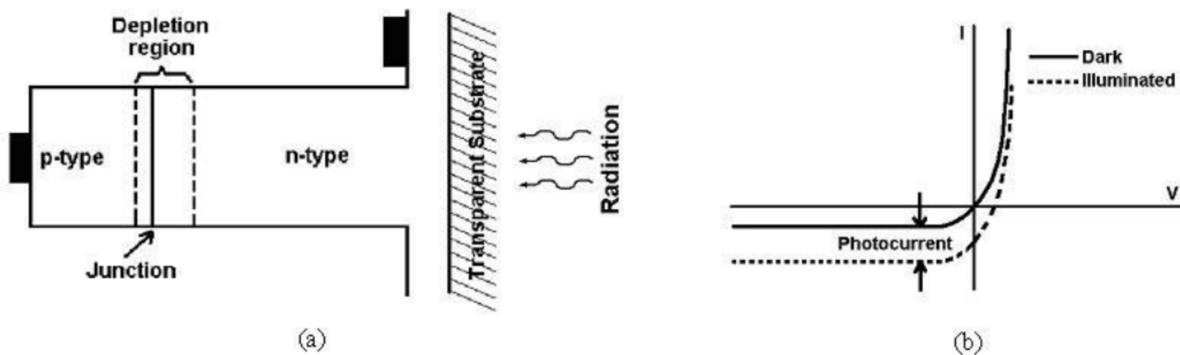

Figure 1.3 Geometry (a), and I-V curve (b) of a photovoltaic p-n diode [13]

InP/InGaAs p-i-n detectors have been used widely in optical communication and various imaging due to high responsivity at 1.3 µm and 1.5 µm, high transmission speed, and low dark current [3]. The sensitivity range for regular InGaAs of 500 nm to 1700 nm and – in increments – up to 2600 nm for extended InGaAs. Scaling down of these photodetectors is essential to achieve a low dark current and a low depletion capacitance. On the other hand, carrier recombination at the exposed mesa surface produces a significant dark current component in a typical small-size mesa structured p-i-n detector, reducing the responsivity and detectivity [4].

This thesis examines how recombination current density affects the dark current, capacitance, and responsivity performance of size-dependent InP/InGaAs p-i-n detectors and investigates some strategies to improve the aforementioned figure of merits.

1.2 Literatura review

1.2.1 InGaAs/InP p-i-n photodetector operation principle

The p-i-n denotes a semiconductor device with the structure p^+-intrinsic-n^+, as shown schematically in Figure 1.4 (a). Depending on the application, the intrinsic layer has much less doping than the p+- and n+-regions, which is much wider than these regions. In an InGaAs/InP p-i-n photodetector, the n^+ layer normally is the InP layer. The intrinsic layer would be i-InGaAs, and the p+ layer is InGaAs or, in some cases InP. When the structure is first formed, holes from the p^+- and electrons from the n^+- sides diffuse

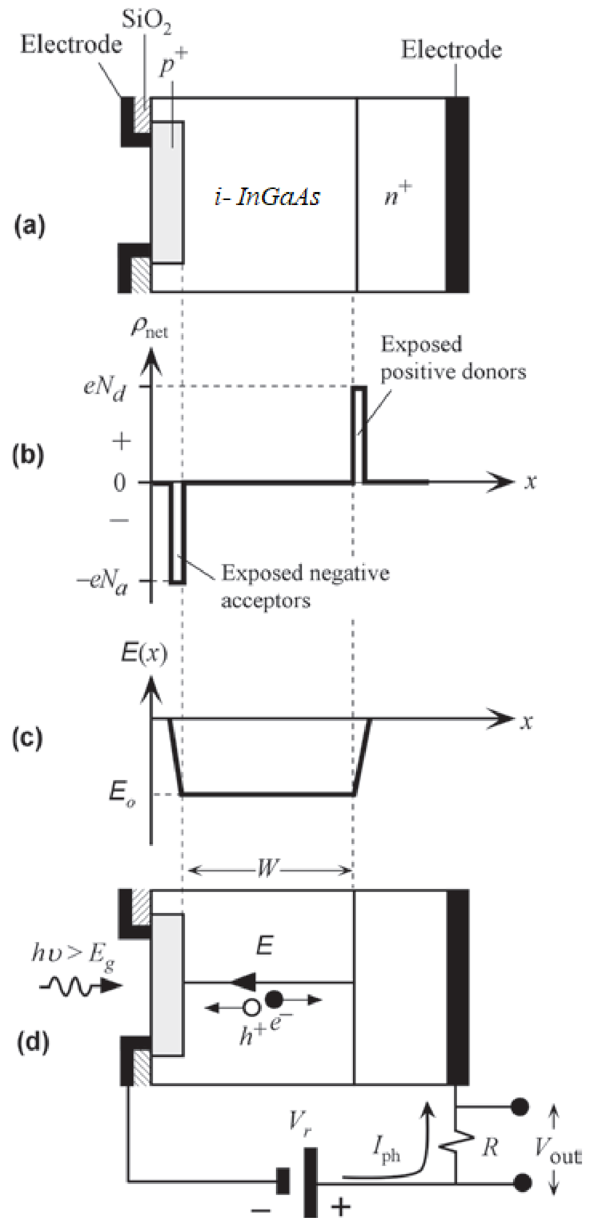

Figure 1.4 (a) the schematic structure of an idealized *p-i-n* photodiode. (b) The net space charge density across the photodiode. (c) The built-in field across the diode. (d) The *p-i-n* photodiode reverse biased for photodetection [5].

-into the intrinsic layer, where they recombine and vanish. As can be seen in Figure 1.4 (b), this leaves a thin layer of exposed negatively charged acceptor ions on the p^+ side and a thin layer of exposed positively charged donor ions on the n^+ side. The intrinsic layer separates the two charges. Figure 1.4 (c) shows that the intrinsic layer has a uniform built-in field from exposed positive ions to exposed negative ions. The built-in field maintains equilibrium when no bias is applied, preventing further diffusion of majority carriers into the intrinsic layer. Photon absorption occurs over the intrinsic layer thanks to the p-i-n structure. As shown in Figure 1.4 (d), the photogenerated electron-hole pairs in the

intrinsic layer are separated by the field and drift toward the n^+- and p^+-sides, respectively. The photogenerated carriers, on the other hand, as they pass through the intrinsic layer, generate an external photocurrent that is detected as a voltage. The p-i-n photodiode has the distinct advantage of allowing a wider spectral range to be absorbed in the space charge layer where photogeneration occurs.

1.2.2 Photodetector characteristic parameters

In the design of photodetectors, speed, power, dark current, and responsivity are four major performance characteristics, which should be considered carefully. Since this thesis aimed to investigate the size-dependent properties of dark current, capacitance, and responsivity of the detectors, we introduce these parameters more in detail.

1.2.2.1 Dark current

The dark current is the sum of the diffusion current, tunneling current, and generation current in the bulk, surface, and heterointerface. The components of the dark current are analyzed as follows:

A. Diffusion current

The diffusion current of the p-i-n photodiode due to thermally generated minority carriers diffusing into the depletion region is given by [6]

$$I_{\text{diff}} = I_s\{1 - \exp(-qV_R/kT)\} \quad (1.1)$$

Where q is the electronic charge, k Boltzmann's constant, T the junction temperature, and I_s is the saturation current. The saturation current I_s is:

$$I_s = qn_i^2(D_n/\tau_d)^{1/2}A/N_A \quad (1.2)$$

Where τ_d is the minority-carrier diffusion lifetime, A the area of the depletion boundary in the p-InGaAs region, N_A is the doping density, and D, the minority-carrier diffusion constant in the p-region.

The diffusion current due to carriers generated in the n-region can be neglected because the minority-carrier density in the n-InP layer is 10^{-10} times that in the n-1nGaAs layer.

B. Bulk and surface generation current

The generation current dominates at low temperatures. The current due to the generation of hole-electron pairs in the depletion region of the InGaAs bulk is

$$I_{\text{gen (bulk)}} = (qn_i AW/\tau_{\text{eff}})\{1 - \exp(-qV_R/2kT)\} \quad (1.3)$$

Where τ_{eff} is effective lifetime. Here, W is the depletion region width, which for an abrupt junction is written as

$$W = \{(2\epsilon_s/qN_D)(V_R + V_{bi})\}^{1/2} \quad (1.4)$$

Where V_{bi} is the built-in potential, N_D the carrier density is the of the InGaAs, and which for a one-sided abrupt junction is given by

$$qV_{bi} = E_g + kT \ln(N_A N_D/n_i^2) \quad (1.5)$$

C. Heterointerface generation

The heterointerface generation current can be expressed by the simplified form

$$I_{\text{gen (hetero)}} \simeq q\sigma v_{th} N_t n_i A/2 \quad (1.6)$$

Where N_t is the trap density at the heterointerface, σ the capture cross-section of the carrier, and υ_{th} the carrier thermal velocity. The heterointerface generation current is estimated from the temperature dependence on the dark current at V= -10 V by subtracting the diffusion and bulk generation components.

D. Tunneling Current

The tunneling current dominates the dark current at higher voltages and is given for band-to-band tunneling through a triangular barrier by

$$I_{\text{tun}} = \{(2m_e)^{1/2} q^3 E_m V_R / 4\pi^2 \hbar^2 E_g^{1/2}\}$$
$$\cdot A \exp\{-4(2m_e)^{1/2} E_g^{3/2}/3qE_m\hbar\} \quad (1.7)$$

Where h is Planck's constant divided by 2π and E $_m$, the maximum electric field. The dark currents differ from the calculated values at lower temperatures. It is considered that the carrier density N_D of the n-InGaAs layer varies with the temperature.

1.2.2.2 EQE and responsivity

The quantum efficiency η of a photodiode indicates the photodiode's ability to convert optical energy into electrical energy, which is defined as:

$$\eta = \frac{number\ of\ electron\ and\ hole\ pairs\ contributing\ to\ the\ photo-induced\ current}{number\ of\ incident\ photons} \quad (1.8)$$

$$\eta = \frac{I_{ph}\ /\ q}{P_{inc}\ /\ h\nu} \times 100\ \% \quad (1.9)$$

Where I_{ph} is the photo-induced current, P_{inc} is the incident optical power, q is the elementary charge, h is the Planck's constant, and ν is the frequency. Instead of the quantum efficiency η, the responsivity R (A/W) is often used.

$$R = \frac{I_{ph}}{P_{inc}} = \frac{q\eta}{h\nu} \quad (1.10)$$

1.2.2.3 Capacitance

In heterojunction devices, the capacitance-voltage (CV) technique is a powerful tool for estimating band offsets and interface charges. Under direct current (DC) biased AC impedance measurements, the capacitance of a semiconductor device is usually extracted from the imaginary part of the complex impedance.

To achieve a faster response speed in p-i-n PDs, the device's capacitance should be as low as possible. The junction capacitance C_J, bond-pad capacitance C_{BP}, and space-charge (depletion) capacitance C_{SD} form the capacitance of a p-i-n PD. The junction capacitance C_J is proportional to the diffusion window area and inversely proportional to the absorption layer thickness. Reduced responsivity results from reducing the diffusion window area while increased carrier transit time and, thus, the reduced operation speed results from increasing the absorption layer thickness. It should be considered that the applied bias has little effect on C_{BP} and C_J.

In the p-i-n photodetector structure, the p-i interface can be considered a p+-n junction, while the i-n interface is an n-n+ junction. Both interfaces form injection barriers under bias, and a large number of electrons accumulate at the p-i interface. In contrast, holes accumulate at the i-n interface, shown in the device band structure profile, Figure 1.5 [7].

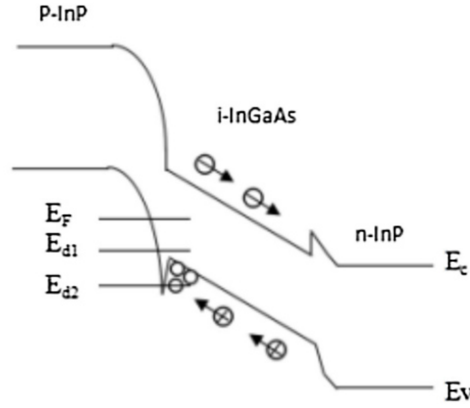

Figure 1.5 Band profile of p-i-n InP/InGaAs/InP photodetector [7]

The p-i interface is more important than the i-n interface because the electron mobility is greater than holes [8]. At the p-i interface, a potential well exists, and some carriers have accumulated there. This heterostructure's capacitance consists of the three-dimensional bulk capacitance caused by the electron distribution around the depletion region and the diffusion capacitance caused by the interface state effect [9]. When measuring the capacitance of the p-i-n diode, a small AC signal upon the DC bias is applied.

$$V = V_0 + v(t) = V_0 + v_0 \sin(2\pi f t) \quad (1.11)$$

The testing signal is υ (t), and the frequency is f. The depletion capacitance (C_T) is calculated as follows:

$$C_T = \frac{\varepsilon_0 \varepsilon_r}{w} \quad (1.12)$$

$$w = \left[\frac{2\varepsilon_0 \varepsilon_r (V_{bi} - V)}{eN_d}\right]^{1/2} \quad (1.13)$$

In the p-i interface state, the V_{bi} is the barrier height. The interface state effect is the main cause of diffusion capacitance. A few electrons accumulate in the interface state when the bias is applied. The external AC signal affects the carriers in the interface state, allowing them to escape the interface and contribute to the excess capacitance. When some charges in the interface have a capture/escape time of less than $1/f$, they are unable to follow the external AC signal. On the other hand, charges with a longer lifetime can easily follow the external AC signal and produce excess capacitance. This phenomenon is thought to be a carrier transport delay. We account for the presence of the diffusion capacitance C_D [7] due to the carrier confinement effect:

$$C_D = e\frac{dn_{d2}}{dV} \quad (1.14)$$

The electron concentration accumulating in the interface state (n_d) can be defined as:

$$n_d(V) = \frac{\eta}{1 + \exp\left(\alpha(E_F - E_d - eV)/kT\right)} \quad (1.15)$$

The η is the effective density of states in the ground state E_d, the α is the delay factor related to the E_d and applied frequency [10]. As a result, the overall capacitance is:

$$\begin{aligned} C &= C_D + C_T \\ &= \frac{e^2\eta_2\alpha}{kT}\left(\frac{1}{1+\exp(\alpha(E_F - E_d - eV)/kT)}\right)^2 \exp(\alpha(E_F - E_d - eV)/kT) \\ &\quad + \left[\frac{e\varepsilon_0\varepsilon_r N_d}{2(V_{bi} - V)}\right]^{1/2} \end{aligned} \quad (1.16)$$

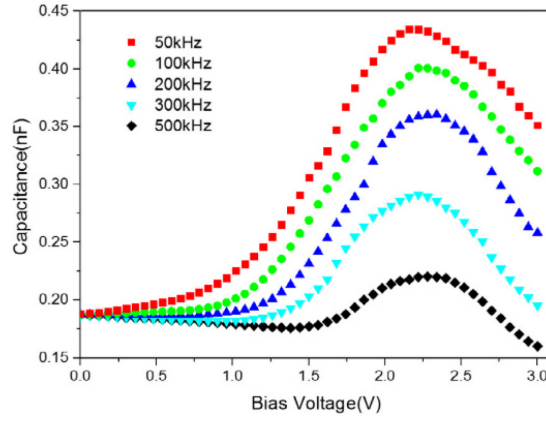

Figure 1.6 The C-V curves measured at room temperature at various frequencies [7].

Figure 1.6 shows a C-V plot of a conventional InGaAs/InP PD from [7] that can be divided into three regions: inversion, accumulation, and depletion. In the entire measured frequency range, the value of capacitance increases very slowly in the inversion region, increases sharply in the accumulation region, increases very sharply, showing a peak in the depletion region, and decreases with applied bias. In these curves, we can find that the capacitance value and the magnitude of the peaks increase with decreasing frequency. A few charges at the interface trap can follow the external AC signal at high frequencies. However, at low frequencies, these charges with varying lifetimes can easily trail the external AC signal, resulting in an excess capacitance. Because at the p-InP/i-InGaAs hetero-interface, a potential well forms, as the Fermi energy approaches the potential well with increasing voltage, some charges will accumulate in the potential well, resulting in an additional capacitance. The C-V characteristics

are influenced by deep-level defects [11]. The recombination and emission centers caused by deep level defects will affect the carrier transport in the accumulation region, resulting in an excess capacitance.

The negative differential capacitance (NDC) phenomenon becomes more apparent with decreasing frequency, as shown in Figure 1.6. The response rate of semiconductor devices is affected by this phenomenon, and the carrier confinement of the interface trap and deep level defects caused by the fast charging-discharging process are the main causes of NDC [12]. Capacitance with negative values is obtained from the device under test when the transient current caused by the small modulation signal lags behind the modulation voltage.

1.2.3 IR photodetectors applications

IR imaging is widely used both in civil and military areas. Civil applications include driver vision enhancement, security systems, industrial process control, fire alarms, medical imaging, and satellite instruments. Military applications cover land, airborne and marine thermal sight systems, mine detection, search and track, reconnaissance, IR guided missiles, and fire control systems. Some civil and military applications are presented in Figs. 1.5 and 1.6.

Figure 1.7 Civil applications of thermal imaging [13]

Firefighting: IR imaging can be used for fighting against forest fires. It is impossible to see hot spots or flames from the air in a normally visible region due to the dense smoke above the region. However, smoke is transparent to the IR light, and firefighters can see and concentrate on the critical points on the fire region [13].

Medicine: IR imaging is an alternative technique for screening and diagnosing purposes in medicine. Medical trials using an IR imager have been discussed by Fauci et al. [14]. In medical applications, desired features are high sensitivity, a small number of dead pixels, high thermal and spatial resolution,

short acquisition time, compatibility with large focal depth optics, and low-cost focal plane arrays (FPAs) [15].

Defense: In military applications, the temperature of the target and background may vary drastically. Highly sensitive FPAs are required to discriminate the target from the background when warm targets with high background irradiance are observed. The need for very high performance, multispectral, uniform, and high yield FPAs becomes more significant when strategic applications are considered. Degraded or dead pixels may cause a target to be missed completely. Missile seeker systems need higher operating temperatures and lower cool-down times.

Figure 1.8 Military land applications of thermal imaging [16].

1.3 Research objective

Performance of small IR photodetectors drops dramatically as size shrinks, according to the previous research. This thesis aims to investigate the size-dependent properties of micro-sized PDs and, using simulation results to find the possible ways to enhance this performance degradation effectively.

1.4 Thesis overview

This thesis focuses on the simulation and analysis of the InP/InGaAs based micro-sized photodetectors. Moreover, new designs are introduced to improve the performance of the devices.

Chapter 2 introduces the physics-based device simulation fundamentals. This chapter discussed the main physics behind our modeling and the various simulators we have been used to investigate the micro-sized photodetectors. These simulators are softwares such as Atlas SILVACO for the electrical and optoelectrical simulations and the FDTD solutions applied for the precise optical simulations.

Chapter 3 describes the size-dependent properties of the photodetectors and the mechanisms affecting their performance. In more detail, the dark current density, responsivity, and the C-V characteristics of the devices in various sizes will be discussed more specifically.

Chapter 4 investigates the performance enhancement strategies in micro-sized IR photodetectors. Firstly, we optimized the top surface window opening for the light illumination of the detectors, which is becoming more critical in small size devices. Second, we studied the effects of gating on the performance of the micro-sized photodetectors, revealing to be as effective as what we expected from the literature.

In summary, a comprehensive study of InP/InGaAs based micro-sized PDs, which entails the theoretical principles, model derivation, and reliable simulation is reported in this thesis. Besides, this thesis exhibits how various strategies impact the improvement of the performance of the micro-sized PDs.

Chapter 2 Physics-based device simulation

2.1 Introduction to semiconductor modeling and simulation

Semiconductor modeling and simulation can be classified into three different branches, which are interrelated: process, device, and circuit simulation, as in Fig. 2.1 [17]. In device modeling/simulation, we usually solve a set of fundamental physics equations to derive the device's electrical, optical, or thermal properties [17]. Using these device simulations, compact models for the devices can be created [17].

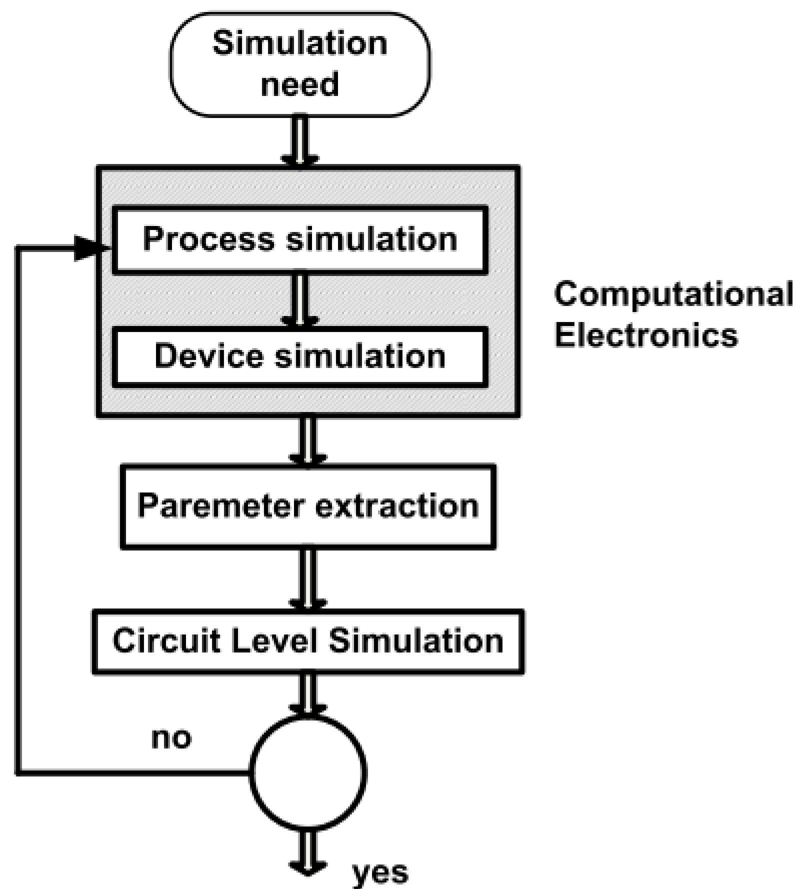

Figure 2.1 Design sequence to achieve simulation need [17].

Fig. 2.2 shows the main components of semiconductor device simulation at any level [17]. There are two main parts that must be solved self-consistently: the transport equations governing charge flow and the fields driving charge flow [17]. These are coupled strongly to one another and must be solved simultaneously [17]. The fields originate from external sources, as well as the charge and current

densities which act as sources for the time-varying electric and magnetic fields obtained from the solution of Maxwell "s equations [17]. Under appropriate conditions, only the quasi-static electric fields arising from the solution of Poisson "s equation is necessary [17].

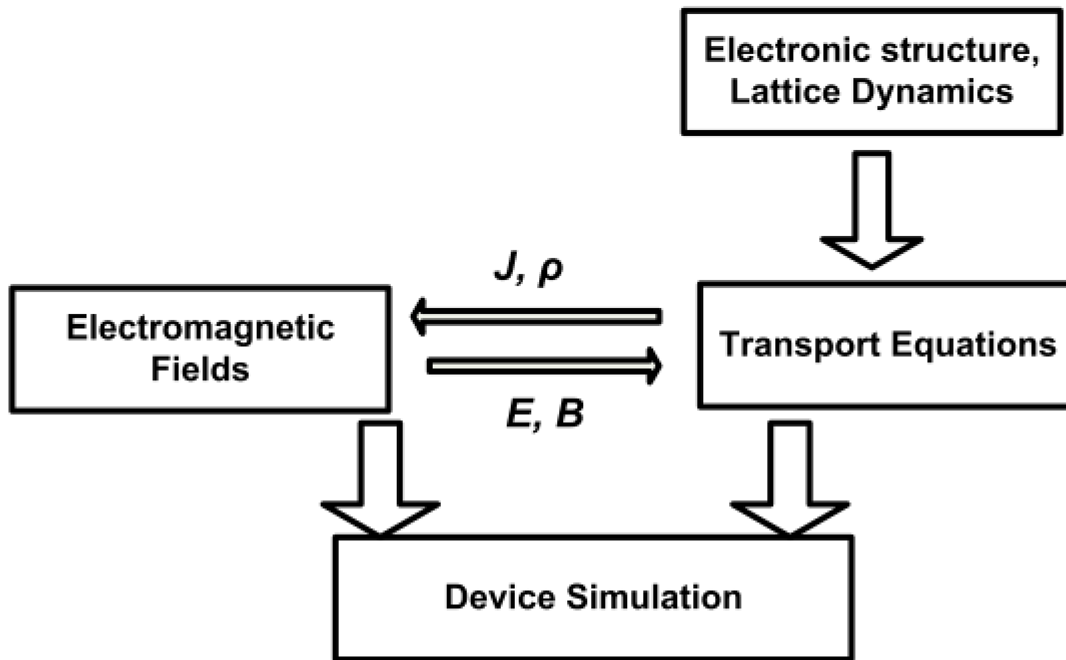

Figure 2.2 Description of the device simulation sequence [17]

SILVACO Atlas is a fully numerical simulator that calculates using a set of fundamental equations within the simulation domain. Poisson's equation, the continuity equations, and the transport equations are the equations that connect the electrostatic potential and carrier densities. Variations in the electrostatic potential are related to local charge densities using Poisson's equation. As described by the continuity and transport equations, the electron and hole densities evolve in detail due to transport processes, generation processes, and recombination processes.

2.2 Electrical simulation fundamentals

2.2.1 Drift-Diffusion (DD) Model

Drift-diffusion (DD) model is widely used for the simulation of carrier transport in semiconductors. The complete drift-diffusion model is based on the following set of equations in 3-dimensional space and time.

2.2.2 Recombination-generation mechanisms

R (x) is the total net recombination rate in continuity equations, and G (x) is the total net generation rate. Applying recombination-generation processes in InGaAs/InP p-n structure include Shockley-Read Hall (SRH), trap-assisted tunneling (TAT), and photogeneration. Description and mathematical modeling of these processes are introduced as follows.

2.2.3 SRH recombination-generation

The Shockley-Read-Hall (SRH) recombination mechanism emerges from the recombination of electron-hole pairs via defect levels within the energy bandgap of the material. Therefore, SRH is not an intrinsic process. The excess energy is released via phonon emission. Such defect levels in InGaAs and InP could be a result of vacancies, substitutional impurities, interstitial impurities, dislocations, or grain boundaries [18]. They can be generated during growth, post-growth annealing treatments, or during device processing [19]. This mechanism can affect all of the merits of the detector, such as noise and detectivity.

The SRH model uses non–degenerate statistics and assumes a single localized recombination center located at an energy level E_t with the trap density N_t (cm^{-3}) [19]. The basic mechanisms are shown in Fig. 2.3 [20]. Four possible transitions may occur via the localized recombination center by which electrons and holes can be captured and emitted [21]. The localized trap state could either be empty or full. When it is empty, it can either capture an electron from the conduction band, as shown in Fig. 2.3 (a), or emit a hole to the valence band, as shown in Fig. 2.3 (d). When it is filled, there exist two possibilities. It can either emit the electron to the conduction band with an emission rate, as is shown in Fig. 2.3 (b) or capture a hole from the valence band, as is shown in Fig. 2.3 (c)

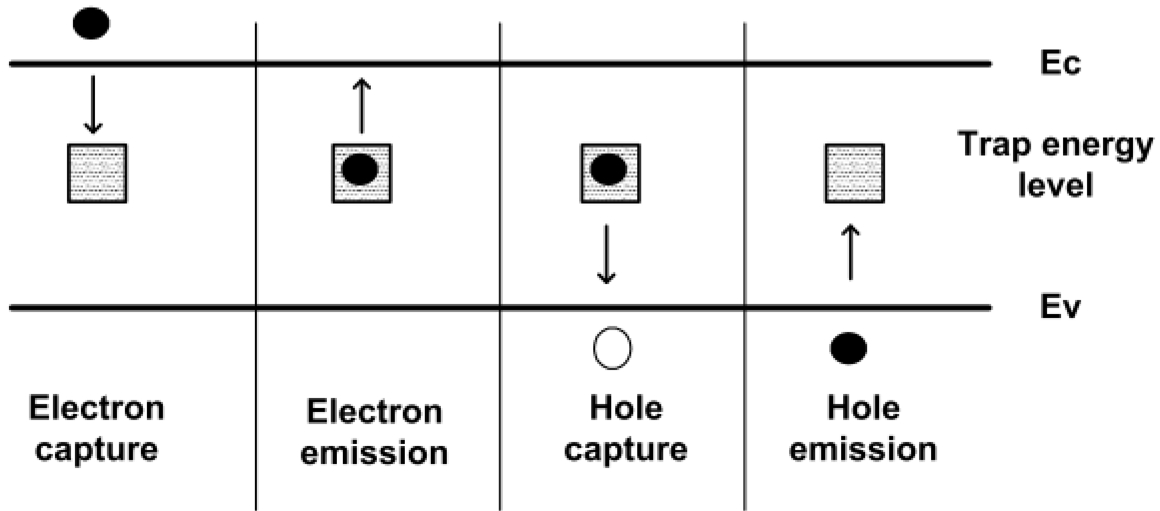

Figure 2.3 Schematic of SRH recombination [20]

The net SRH recombination rate is given by [22]

$$R_{SRH}(x) = \frac{\left[n.p - n_i^2\right]}{\left[\tau_p\left[n+n_1\right]+\tau_n\left[p+p_1\right]\right]} \quad (2.1)$$

Where τ_n and τ_p are minority carrier lifetimes due only to SRH processes. Also, n_1 and p_1 are the electrons and the hole concentrations respectively when the Fermi level is coincident with the trap level as follows

$$p_1 = N_v \exp\left[-E_t / kT\right],$$
$$n_1 = N_c \exp\left[-\left[E_g - E_t\right]/kT\right] \quad (2.2)$$

E_t is measured from the top of the valence band. N_c is the density of states of electrons in the conduction band, and N_v is the density of states of heavy holes in the valence band [23].

2.2.4 Surface recombination-generation

In addition to generation-recombination within the bulk of the semiconductor, electrons or holes may recombine or be generated at interfaces. The rate of surface recombination may be even greater than within the bulk. The standard method is to model interface recombination similarly as the bulk generation-recombination rate [24] where:

$$R_{surf} = \frac{pn - n_{ie}^2}{\tau_p^{eff}\left[n + n_{ie} exp\left(\frac{\mathrm{ETRAP}}{kT_L}\right)\right] + \tau_n^{eff}\left[p + n_{ie} exp\left(\frac{-\mathrm{ETRAP}}{kT_L}\right)\right]} \quad (2.3)$$

Here:

$$\frac{1}{\tau_n^{eff}} = \frac{1}{\tau_n^i} + \frac{d_i}{A_i}\mathrm{S.N} \quad (2.4)$$

$$\frac{1}{\tau_p^{eff}} = \frac{1}{\tau_p^i} + \frac{d_i}{A_i}\mathrm{S.P} \quad (2.5)$$

τ^i_n is the bulk lifetime calculated at node *i* along with the interface, which may also be a function of the impurity concentration. The d_i and A_i parameters are the length and area of the interface for node *i*. The S.N and S.P parameters are the recombination velocities for electrons and holes, respectively.

2.2.5 Mathematical modeling of trap assisted tunneling (TAT)

Traps in the depletion region play an important role in degrading low-bandgap detector performance. As shown in Fig. 2.4, an electric field in the depletion region causes two non-thermal (horizontal) transitions: tunneling electrons from the valence band to the traps and tunneling from the traps to the conduction band.

Tunneling from the valence band to the conduction band is called direct or band-to-band tunneling (BTB), which is dominant in large reverse bias voltages [26]. In low and moderate reverse-bias, we omitted BTB in our model. Trap-assisted tunneling (TAT), shown in green in Fig. 2.4, is the dominant dark current mechanism under large and moderately large reverse bias voltages [27]. Since there is a correlation between TAT current and 1/f noise, even negligible TAT current due to traps may degrade detector performance [28]. Therefore, modeling the TAT rate is extremely important.

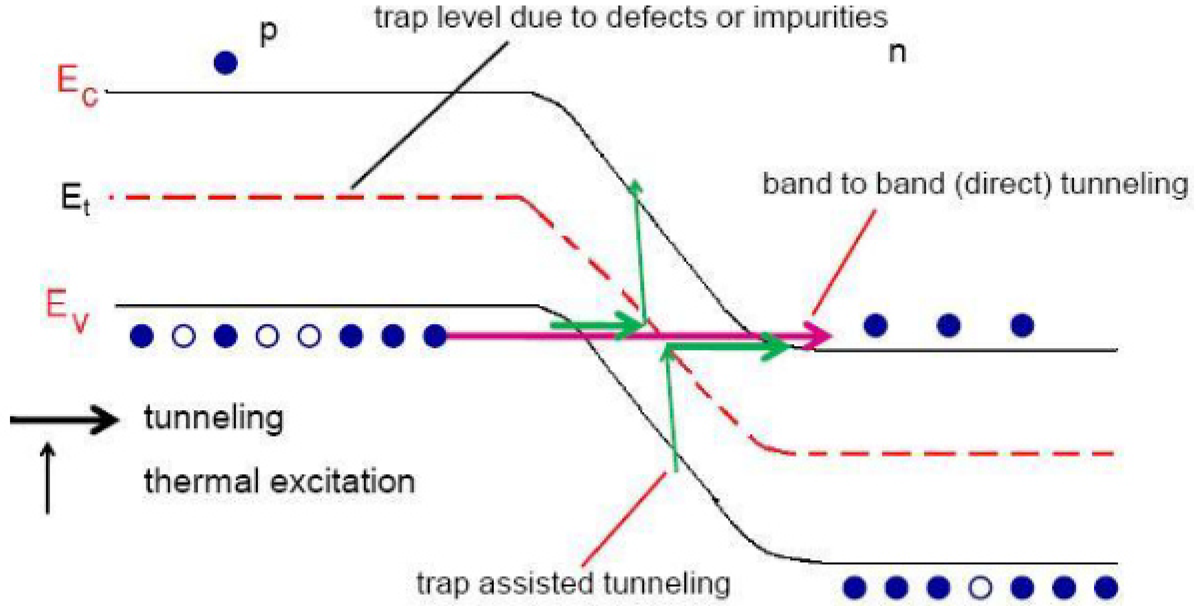

Figure 2.4 Schematic of tunneling mechanisms [25].

In the literature, [29] and [23] have been performed for detailed mathematical modeling of the TAT rate, embedded into the continuity equations for numerical analysis. We adapt following expressions for TAT rate [29], [23], and [28]

$$R_2 = N_t\left[n.p - n_i^2\right]\left[W_v.W_c.e^{E_g/kT} + W_c.\gamma_v.e^{(E_g-E_t)/kT} + W_v.\gamma_c.e^{E_t/kT} + \gamma_c.\gamma_v\right] \quad (2.6)$$

$$R_3 = \left[p(x) + p_1\right].\gamma_v + \left[n(x) + n_1\right].\gamma_c$$
$$+\left[n(x)e^{(E_g-E_t)/kT} + N_c\right].W_c + \left[p_{lh}(x)e^{E_t/kT} + N_{vlh}\right].W_v \quad (2.7)$$

$$R_{TAT} = \frac{R_2}{R_3} \quad (2.8)$$

Where N_{vlh} is the density of states of light holes in the valence band (cm^{-3}), which is taken approximately equal to N_c [29]. E_t is the trap energy measured from the valence band in eV. N_t is the trap density. $p=p_{hh}+p_{lh}$ (hh: heavy hole, lh: light hole). Light holes are responsible for tunneling since the mass of the light hole is small, and the tunneling rate is large. In our study, p_{lh} is taken approximately to be (N_{vlh}/N_{vhh}) p.

Tunnel capture constants are given by [28]

$$W_c = \frac{6x10^5 E}{N_c(E_g - E_t)}.exp\left[\frac{-1.7x10^7 E_g^{1/2}(E_g - E_t)^{3/2}}{E}\right] \quad (2.9)$$

$$W_v = \frac{6x10^5 E}{N_v E_t}.exp\left[\frac{-1.7x10^7 E_g^{1/2}.E_t^{3/2}}{E}\right] \quad (2.10)$$

Thermal capture constants are expressed as [23]

$$\gamma_c = \frac{1}{\tau_n N_t}$$

$$\gamma_v = \frac{1}{\tau_p N_t} \quad (2.11)$$

2.2.6 Lifetime modeling

Minority carrier lifetime is an important parameter for InGaAs/InP detector modeling and simulation. In our study, lifetime is incorporated into the SRH and TAT (recombination-generation) R-G expressions. Electron (hole) lifetime is modeled as follows [30]

$$\tau_{n(p)} = \frac{1}{\gamma_{n(p)} N_t} \quad (2.12)$$

$$c_{n(p)} \text{ or } \gamma_{n(p)} = \sigma_{n(p)} v_{th,e(p)} \quad (2.13)$$

$$v_{th,e(p)} = \sqrt{\frac{3kT}{m^*_{e(h)}}} \quad (2.14)$$

Where N_t is the trap density, c_n is the electron capture coefficient, c_p is the hole capture coefficient, υ_{th} is the electron/hole thermal velocity, and σ_n and σ_p are the electron and hole capture cross-sections.

2.3 Optical simulation

2.3.1 Mathematical modeling of photogeneration rate

The photogeneration rate is given by [18]

$$G_f(x) = F_f \alpha \eta e^{-\alpha x} \quad \left[\# \text{of } EHP / (cm^3.s)\right] \quad (2.15)$$

Where x is the distance, F_f is the incident photon flux, α is the absorption coefficient, and η is the quantum efficiency [18].

2.3.2 Luminous: optoelectronic simulator

Luminous is a general-purpose program for light propagation and absorption, which is integrated into SILVACO Atlas. Luminous calculates optical intensity profiles within the semiconductor device, and the intensity profiles are then converted into photogeneration rates. This unique feature allows users to simulate electrical responses to optical signals for various optical detectors. In Luminous, there are four physical models for light propagation, including ray tracing (RT), the transfer matrix method (TMM), the beam propagation method (BPM), and the finite difference time domain (FDTD) method. Ray tracing is used in the following SILVACO Atlas simulations. Optoelectronic device simulation can be split into two distinct models used to calculate simultaneously at each DC bias point [31].

1. Ray tracing model uses the refractive index's real part to calculate the optical intensity at each grid point.

2. Absorption or photogeneration model using the imaginary part of the refractive index to calculate the carrier concentration at each grid point.

Then, an electrical simulation is performed to calculate the terminal currents. The schematic for ray tracing in 2D device simulation is shown in Figure 2.5. An optical beam is specified using the BEAM statement. The origin of the beam is defined by parameters X.ORIGIN and Y.ORIGIN. The ANGLE parameter specifies the propagation direction of the beam. MIN.WINDOW and MAX.WINDOW parameters define the illumination window. As shown in Figure 2.5, the illumination Window is automatically clipped to the edge of the device. The beam is automatically split into a series of rays so that all of the rays cover the entire width of the illumination window.

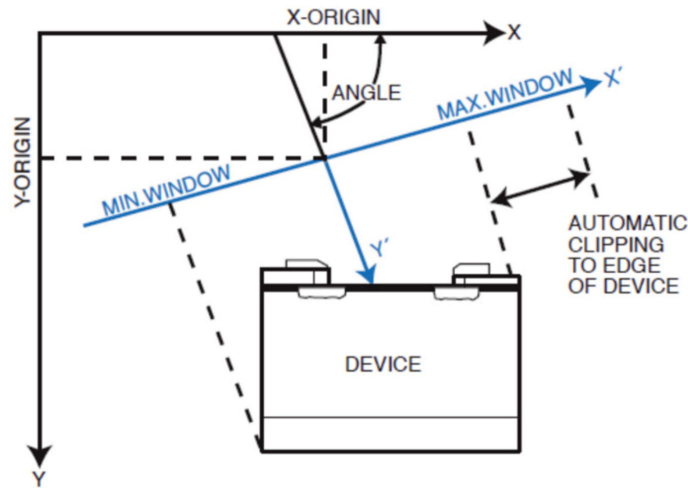

Figure 2-5 Schematic of the ray tracing in 2D [31].

2.3.3 FDTD solution fundamentals

FDTD is the gold standard for modeling Nanophotonic devices, processes, and materials. This finely-tuned implementation of the FDTD method delivers reliable, robust, and scalable solver performance over a broad spectrum of applications. The integrated design environment provides scripting capability, advanced post-processing, and optimization routines, focusing on design.

The finite-difference time-domain (FDTD) method is used to solve Maxwell's equations in the time domain. The equations are solved numerically on a discrete grid in both space and time, and derivatives are handled with finite differences. It does not make any approximations or assumptions about the system, and, as a result, it is highly versatile and accurate. It is a fully vectorial simulation method since it solves for all vector components of the electric and magnetic fields. Because it is a time-domain method, FDTD can be used to calculate broadband results from a single simulation. FDTD is typically used when the feature size is on the order of the wavelength. This wavelength scale regime where diffraction, interference, coherence, and other similar effects play a critical role is called wave optics. FDTD can handle arbitrarily complex geometries and makes no assumptions about, for example, the direction of light propagation. It has no approximations other than the finite-sized mesh and finite-sized time step; therefore, it is accurate. FDTD can address a wide range of applications. These include photonic crystals, plasmonics, CMOS image sensors, nanoparticle scattering and absorption, nano-patterned solar cells, OLEDs and LEDs, gratings, lithography, metamaterials, and integrated optics, to name just a few.

Chapter 3 Simulation-based investigation of micro-sized IR photodetectors in various sizes

3.1 Introduction

Miro-sized photodetectors applicable in any part of the light spectrum could be useful in various applications, such as micro-LEDs industries, lab-on-chip, and related miniature instrumentation.

On the other hand, micro-sized devices become extremely sensitive to device sidewall quality because surface roughness or residual byproducts cause significant surface leakage. Surface leakage not only degrades device performance and interferes with detector array uniformity, but it also overwhelms important bulk dark current mechanisms. The abrupt termination of the periodic crystalline structure, contamination from processing (dry etching), and fixed charges within the passivation layer, which can cause band bending on mesa-sidewalls, are thought to be the sources of surface leakage. This band-bending results in electron accumulation or type inversion at sidewall surfaces, forming a conduction channel along the sidewalls [32], [33]. In addition, crystallographic defects, impurities, and dangling bonds on the etched surface create trap states within the bandgap that act as recombination centers [34] and [35].

At this time, sidewall passivation with dielectric materials has been proven to be an effective method for PDs to reduce the impact of sidewall defects. However, different methods of sidewall passivation have different effects on PD photoresponse properties. The traditional method of sidewall passivation is plasma-enhanced chemical vapor deposition (PECVD), which provides a fast deposition rate but poor film quality [36], making the investigation of micro-sized photodetectors more crucial. The micro-sized design of the devices will be introduced in the following sections, and their electrical and photoresponse characteristics will be thoroughly investigated.

3.2 Device structure and simulation

Micro photodetectors in different sizes, such as 100, 50, 40, 30, 20, and 10 μm diameter, were designed. All of the devices consists of a 0.5 μm heavily doped n-type InP buffer layer (5×10^{18} cm^{-3}), a 2 μm lightly doped n-type InGaAs absorption layer (1×10^{15} cm^{-3}), a 0.1 μm heavily doped p-type InGaAs layer (1×10^{19} cm^{-3}) as an ohmic contact layer. More details about the depth of the etch, top surface contact configuration, and the gate structures could be seen in Figure 3.1. In the simulation settings, we

introduced surface recombination velocity for the micro-sized consideration analysis purposes. All of the parameters used in the simulation are bought in Table 3.1.

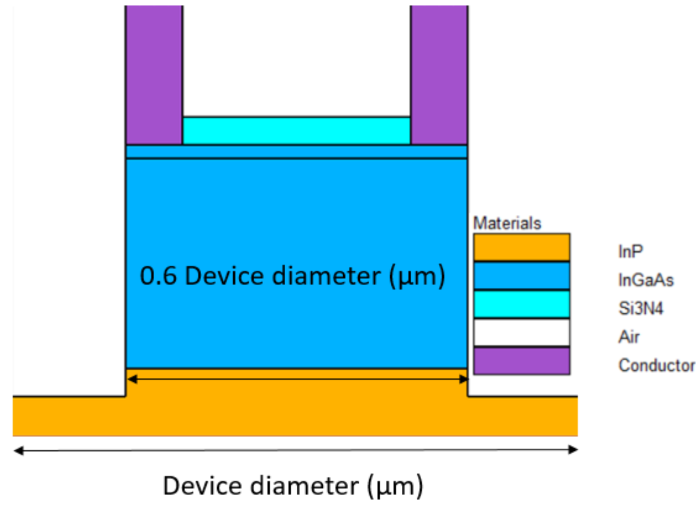

Figure 3.1- The cross-section of the micro-sized photo detectors in various diameters

Table 3.1. The main parameters used in the SILVACO Atlas simulation

Parameters	Unit	InGaAs	InP
Band gap	eV	0.78	1.34
Effective conduction band density of states	cm^{-3}	7.62×10^{18}	5.66×10^{17}
Effective valence band density of states	cm^{-3}	7.62×10^{18}	2.03×10^{19}
Electron lifetime	s	1×10^{-7}	1×10^{-9}
Hole lifetime	s	1×10^{-7}	1×10^{-9}
Electron mobility	cm^2/Vs	12,000	4730
Hole mobility	cm^2/Vs	450	151
Bulk trap density	cm^{-3}	3.5×10^{13}	-
Surface recombination velocity	cm^{-2}	5×10^3	-
Ref.		[10]	[10]

3.3 Results and discussion

To do the size-dependent simulations for each of the optoelectrical properties of the detectors, we needed to find the parameters changing in any of the sizes. One of the essential parameters, changing by the device's size, is effective carrier lifetime [37]. According to the literature, the size-dependency of this parameter follows the equation 3.1:

$$\frac{1}{\tau} = \frac{1}{\tau_b} + \frac{2S}{R} \quad (3.1)$$

In which, τ_b is the carrier lifetime in the bulk section of the semiconductor, S is the surface recombination velocity, and R is the radius of the photodetector. Based on this formula, we introduce the effective carrier lifetime for each size of the device as it comes in Table 3.2.

Table 3.2 effective carrier lifetimes in various sizes

Size (μm)	Effective carrier lifetime(s)
100	10^{-6}
50	10^{-7}
40	9.4×10^{-8}
30	8.6×10^{-8}
20	7.35×10^{-8}
10	5.1×10^{-8}

We ran electrical and optoelectrical simulations based on the assumptions in this table to investigate the size-dependent properties of the devices.

3.3.1 Dark current

The size-dependent properties of the micro photodetectors' dark current will be discussed in Figure 3.2 (a, b). According to the literature, the dark current of InP/InGaAs photodetectors consists of three main components [38]: SRH generation (bulk and surface), trap assisted tunneling, and the diffusion current. In the preceding sections, these elements were thoroughly examined. The diffusion current in our devices was negligible because it was on the order of 1^{-12} Ampere[38]. The dark current density vs. reverse bias voltage is usually divided into two parts. The first part is in low voltages (usually V= -2V), indicating that the SRH generation current is increasing as the absorption region depletes. The second part is the one in which dark current due to the trap-assisted tunneling is more critical in intermediate

voltages. The sign of this part of the dark current is its linear behavior depending on the tunneling effective mass of the carries as the slope of that line. Figure 3.2 (a) shows that the dark current density increases with the decrease in the size of devices. More deeply observing the dark current curve, it could be seen that the SRH generation component increases with the decrease of the size. Since this component consists of bulk and surface parts and the bulk parts are equal for any of the sizes, it could be concluded that the increase of the dark current density is mainly related to the surface SRH generation part. This phenomenon occurred because, in smaller devices, the sidewall dry etch damage or the sidewall interface traps play a more critical role in the degradation of the device's performance owing to the higher ratio of sidewall perimeter to mesa area. Figure 3.2 (b) exhibits the correlation between the dark current density and the P/A parameter. Here P is the perimeter, and A is the area of the device. The linear dependence of the dark current density to the P/A parameter proves that in devices with higher P/A (smaller devices), we have a larger current density. According to the literature, the slope of this curve would be the value of the surface recombination velocity and comparing the value coming out of the curve with the value we put in our simulation settings validate our size-dependent simulation

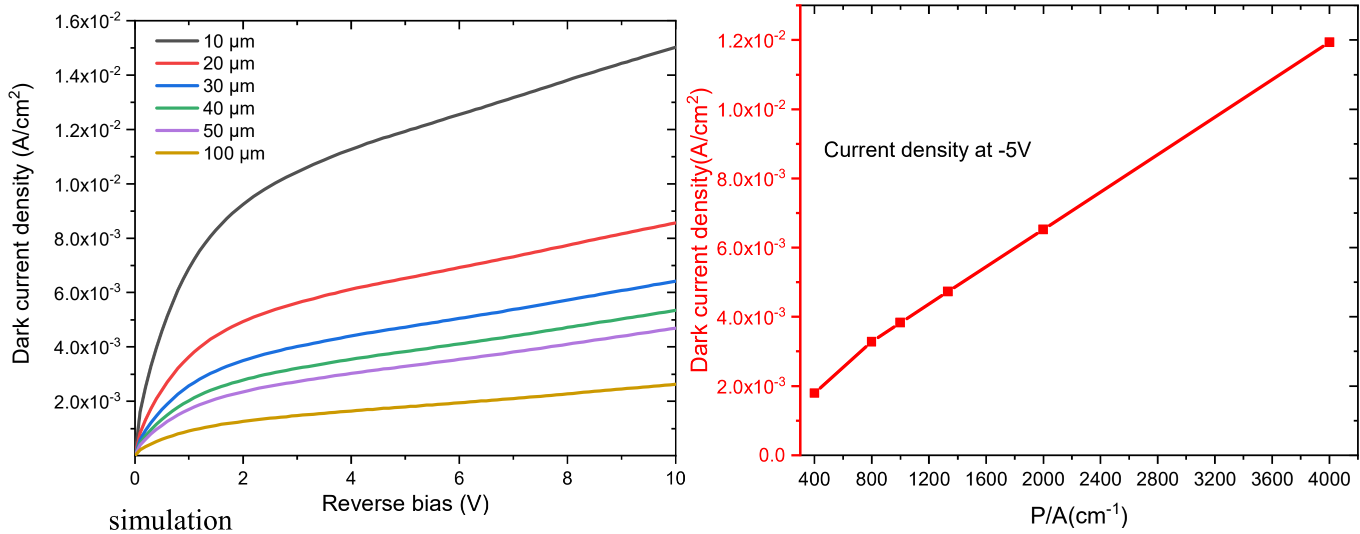

Figure 3.2 (a) Dark current density vs. Reverse bias in various sizes, (b) the correlation of the dark current density with P/A parameter of various photodetectors.

results.

3.3.2 Capacitance

Following our discussion of the theoretical concepts of photodetector capacitance, we will present capacitance simulations of our device in various sizes. A small-signal AC impedance technique was

used to simulate the capacitance of the micro-sized photodetectors between -5 and 5 V DC bias. The C–V characteristics of photodetectors for various diode diameters are shown in Figure 3.3 (a). The capacitance of all devices, regardless of size, follows a similar pattern: the value of capacitance is positive under reverse bias, then increases to a peak with forward bias, then decreases with increasing forward bias to a negative value. In traditional broad-area photodetector devices, similar trends have been observed [7], demonstrating that no matter the size or format of the device, the device's capacitance is dominated by the same physical mechanism. This increase in capacitance with increasing bias can be explained in the following way. The width of the depletion region and the carrier concentration in the depletion region change with the applied bias under reverse bias, and the depletion capacitance dominates the device capacitance. Because a large number of carriers pass through the depletion region under forward bias, the depletion approximation is no longer applicable. The carriers stored in either the n-type or p-type diffusion region change with the applied bias in this case. The forward capacitance should increase exponentially with bias voltage according to conventional p-n junction theory [7]. However, the experimental results are in direct opposition to those predicted by Shockley's theory, as a capacitance peak is observed, followed by a drop to a negative value. As a result, an NC mechanism should increase much faster with forward bias and has the opposite trend as diffusion capacitance. NC is caused by the nonmonotonic or positive-valued behavior of the time-derivative of the transient current in response to a small voltage step, according to Ershov et al. [39], who interpreted the NC effect based on the measuring principle. This interpretation is persuasive when it comes to numerically describing the appearance of NC, but it is less insightful when it comes to clarifying the underlying physical mechanism, which is particularly important for NC research.

Figure 3.3 (b) shows that both depletion and diffusion capacitances are proportional to the device junction area. The larger diameter photodetectors have a higher capacitance in both the depletion and diffusion regimes: the device's depletion capacitance and diffusion capacitance scale linearly with its size in the lower voltages. However, unlike conventional depletion and diffusion capacitance, size-dependent NC exhibits a deviation from linearity as applied bias increases. To better understand this strange relationship between NC and device size, we looked at the normalized capacitance per device area as a function of bias for various photodetector devices. Figure. 3.3 (c) shows the characteristics of normalized capacitance versus bias voltage of different photodetector devices. This NC represents the effect of the defect densities originating from the microfabrication process, according to the theory developed by Basal et al. [40] and experimental results reported by Yang et al. [41] (primarily due to Inductively Coupled Plasma (ICP) etching). The findings suggest that the higher NC in smaller

diameter photodetectors is due to the effect of the sidewall fabrication process settings, which may cause sub-band-gap defects on the sidewalls. In our simulations, we used the same surface recombination velocity for various sizes of the devices, which impact the normalized capacitance of the smaller devices due to larger surface-to-volume ratios. The largest NCs are found in 10 μm photodetectors, and the smallest in 100 μm photodetectors, validating our simulations with the experimental results in [41].

3.3.3 Responsivity

Responsivity, as discussed in Section 1.2.2.2, is one of the most important characteristics of a photodetector. The responsivity is defined as the ratio of photocurrent to the total radiation power. To analyze the size-dependent properties of the photodetectors` responsivity, the effects of sidewall defects on the photocurrent should be considered. According to the literature [42], the photocurrent density of a photodetector is as follows:

$$J_{photo} = J_{bulk} - J_{p-n} - J_S \qquad (3.2)$$

$$J_{p-n} = \frac{1}{2} e \frac{n_i}{\tau_{0p-n}} W \qquad (3.3)$$

$$J_S = \frac{1}{2} e n_i S_0 d \left(\frac{P}{A}\right) \qquad (3.4)$$

As shown in Eq. (3.2), the photocurrent density (J_{photon}) consists of the following three components: photocurrent density generated in bulk (J_{bulk}), the recombination current density within the depletion region of the p-n junction (J_{p-n}), and the surface recombination current density (J_S). To describe more the Eq. (3.3) and (3.4), n_i is the intrinsic carrier concentration, W is the bulk depletion width, τ_{0p-n} is the carrier lifetime in bulk, d is the mesa depth, s_0 is surface recombination velocity, and q is the electron charge, P is the device periphery, and A is the device area. Based on these formulas, we can predict that as the recombination current density types increase, the photocurrent and, as a result, the device's responsivity will decrease. Also, because the P/A is larger for smaller devices, it follows from Eq. 3.4 that smaller devices will have higher J_s and thus lower responsivity.

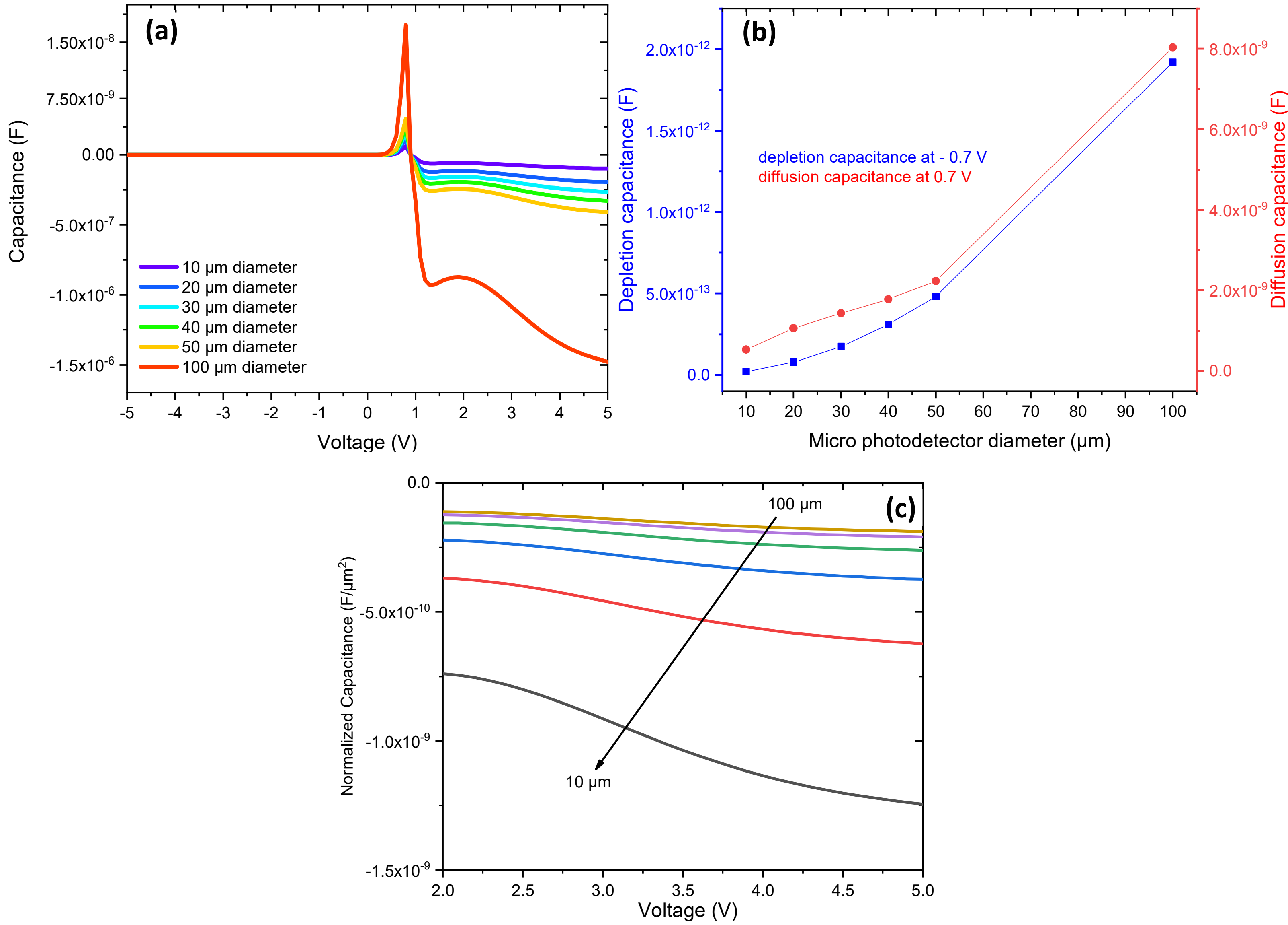

Figure 3.3 (a) Diameter-dependence of the photodetectors' C–V characteristics measured at 100 KHz. (b) Depletion and diffusion capacitances of various diameter photodetectors simulated at −0.7 V and +0.7 V DC bias, respectively. (c) The normalized negative capacitance of photodetectors driven from +2 to +5 V, 100 kHz AC signal.

Figure 3.4 shows the simulation results for photodetectors of various sizes in terms of responsivity vs. wavelength at V= -1 V. The responsivity of the 100 μm diameter shows an excellent agreement with the literature values [3]. Moreover, the simulation results vividly exhibit the size-dependent properties of responsivity in the photodetectors. Simulation results show that the device with 100 μm diameter has the highest value for the responsivity, even though the device with 10 μm diameter has the lowest

value. This phenomenon happens since decreasing the size of the devices will increase the importance of sidewall defects in small devices. Another variation is observable between the responsivity reductions of devices in each size reduction. For example, the responsivity reduction differs between 50 to 40 µm device and 20 to 10 µm device. Figure 3.4 (b) shows that the responsivity reduction increases in the greater P/A changes (among smaller devices). This trend proves that recombination current densities play a more dominant role in reducing the photogenerated current and, therefore, the responsivity in smaller devices.

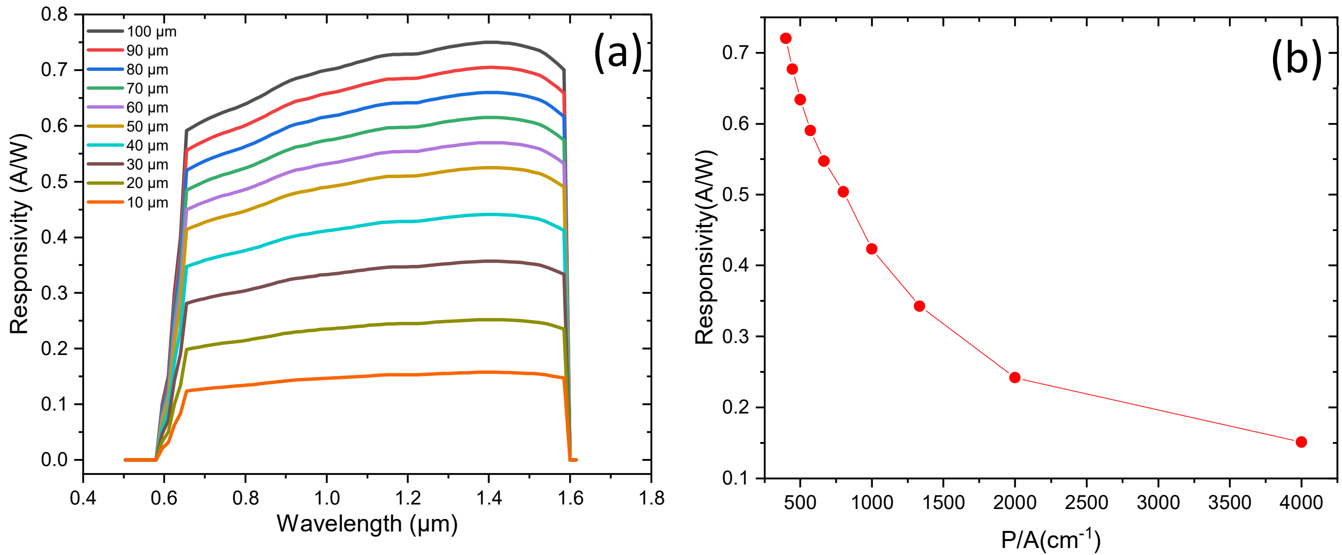

Figure 3.4 (a) spectral responsivity vs. wavelength of various photodetectors in different sizes, (b) Responsivity vs. P/A changes.

3.4 Conclusions

To summarize, we used optoelectrical simulation with SILVACO software to investigate the various size-dependent characteristics of micro-sized photodetectors in this chapter. Electrical properties and responsivity were the two main categories of this investigation. We introduced our simulation setup in section 3.2 and the parameters that should be considered for size-dependent investigations, such as effective carrier lifetime and surface recombination velocity, which former varies depending on device size. In section 3.3.1, we studied the size-dependent dark current of the micro photodetectors. Our investigation revealed that, as we expected from the literature, surface SRH generation current density is the key factor in increasing the dark current density in smaller devices. This trend was due to the sidewall dry etch damage or the sidewall interface traps due to the higher ratio of sidewall perimeter to

the mesa area. In section 3.3.2, we investigated the size-dependency of the micro-sized photodetectors. First of all, we mentioned the theoretical fundamentals of the capacitance of a photodetector and then specifically discussed the capacitance of the InGaAs/InP photodetector. Finally, we presented our capacitance simulation results in the -5 to 5 V range. The depletion and diffusion capacitance shows size-dependent properties, and they increase with the increase of the device size. Since, according to the literature, InGaAs/InP photodetectors show the NC feature like GaN photodetectors, we studied the size dependency of this characteristic in more detail. NC happens when the transient current caused by the small modulation signal lags behind the modulation voltage. The simulated normalized capacitance of the photodetectors was in complete agreement with the experimental expectation for the GaN photodetectors. The higher NC in smaller diameter photodetectors is due to the effect of sidewall fabrication process settings, which may cause sub-band-gap defects on the sidewalls. In section 3.3.3, we evaluated the simulation results of size-dependency in the responsivity of the micro-sized detectors. In the investigation, it is becoming evident that smaller devices show lower responsivity due to the higher importance of the sidewall defects. This parameter influences the surface recombination current density of Eq.3.1. Also, it was observed that in size reduction with greater P/A changes (among smaller devices), the responsivity reduction percentages increase.

Chapter 4 Investigations on performance enhancement in micro-sized IR photodetectors

4.1 Performance enhancement of micro-sized IR photodetectors with different top surface window configurations

4.1.1 Introduction

The first place where photons of the light coupled with devices are the opening layer of any photodetectors. As the size of the devices shrinks, the quality and configuration of this layer will become more important since due to the fabrication limitations in micro fabrication processes, in small devices, the metal contacts cover more percentage of the top surface which leads to a higher reflection. Higher reflection, according to the literature, reduces the transmission of light inside the device and therefore reduces the responsivity. The quality of anti-reflection layer includes the absorption layer size and thickness, which influences the number of photons absorbed before reaching the absorption layer, where they will be converted to an electrical signal.

In the following section, we will compare the optical and electrical performance of the micro-sized photodetectors with two different top surface window configurations.

4.1.2 Device structure and simulation

The micro photodetectors with 10 μm diameter were designed in 2 with two different top surface window configurations. The epitaxial layers of devices with top surface window configuration were the same as previous devices. On the other hand, the devices with a second top surface window configuration have a one-sided contact area.

The schematic cross-section of different device configurations is shown in Fig. 4.1 (a, b), respectively.

4.1.3 Results and discussion

The finite-difference time-domain (FDTD) method was used to simulate the photodetector's optical properties including, carrier generation rate and the surface reflection profile.

Optical absorbed power can be used to calculate the local generation rate of electron-hole pairs. When each absorbed photon excites an electron-hole pair, the photon absorption rate is equivalent to the (frequency-dependent) generation rate, as follows.

$$P_{abs}(\mathrm{r},\omega) = -\frac{1}{2}\omega|\mathrm{E}(\mathrm{r},\omega)|^2\Im\{\epsilon(\mathrm{r},\omega)\} \qquad (4.1)$$

$$g(\mathrm{r},\omega) = \frac{P_{abs}(\mathrm{r},\omega)}{\hbar\omega} = -\frac{\pi}{h}|\mathrm{E}(\mathrm{r},\omega)|^2\Im\{\epsilon(\mathrm{r},\omega)\} \qquad (4.2)$$

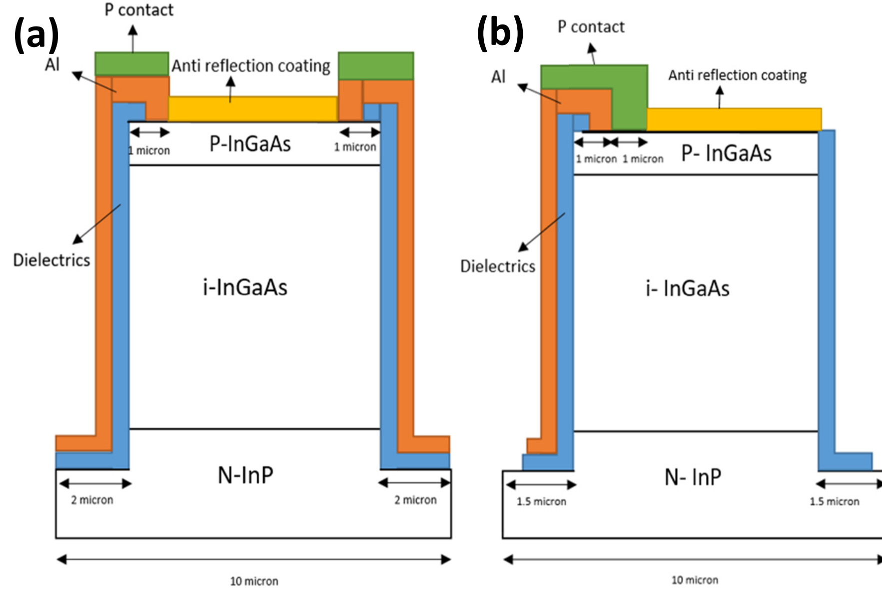

Figure 4.1 (a) The cross-section of the devices with first top window configuration, (b) the cross-section of the devices with second top window configuration.

Figure 4.2 (a, b) and Figure 4.3 (a, b) show the results of optical simulations, including carrier generation rate and surface reflection profile. We can compare the photoresponse generation rates of the devices in Figure 4.2 (a, b). The devices with the first top surface window configuration generate slower than those with the second. By comparing the surface reflection power profiles of different configurations, we could determine what was causing this phenomenon. The second configuration, with a smaller metal contact area, showed lower reflectivity, as expected, as shown by the contours in Figure 4.3 (a, b). The percentage of reflectivity drops from 55 to 33 by switching from the device with the first configuration to the device with the second configuration.

To make our findings more quantitative, we used SILVACO software to run optoelectrical simulations to compare their dark current density and device responsivity, as shown in Figure 4.4 (a, b). Figure 4.4 (a) shows that devices with the first top surface window configuration have a lower dark current density than devices with the second top surface window configuration because the contact area in the first

device is larger. As a result, the diode's rectification behavior improves. Figure 4.4 (b) also shows that devices with the second top surface window configuration have higher responsivity in each wavelength than devices with the first top surface window configuration. As expected, the second configuration's device devices have higher EQE and responsivity due to lower top surface reflectivity.

For photons with a wavelength of 1.55 µm, this variation increases by around 33.33 percent, which could significantly improve.

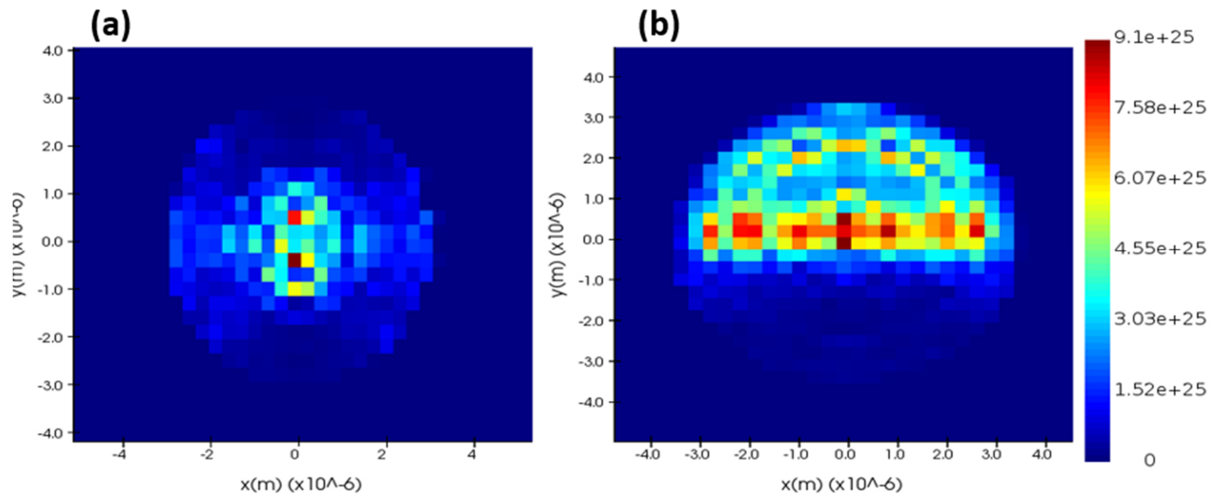

Figure 4.2 (a) generation rate contour of the device with first top surface configuration, (b) generation rate contour of the device with second top surface configuration.

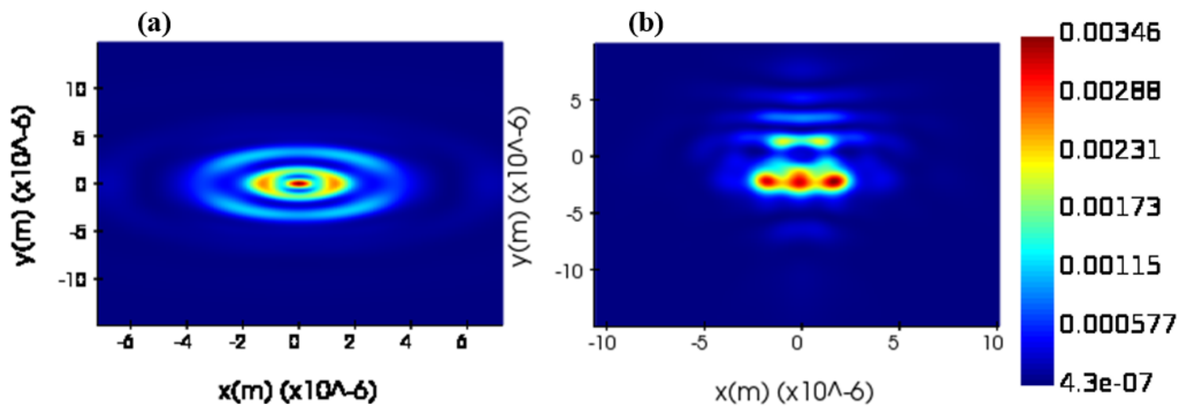

Figure 4.3 (a) surface reflection power profile contour of the device with first top surface configuration, (b) surface reflection power profile contour of the device with second top surface configuration.

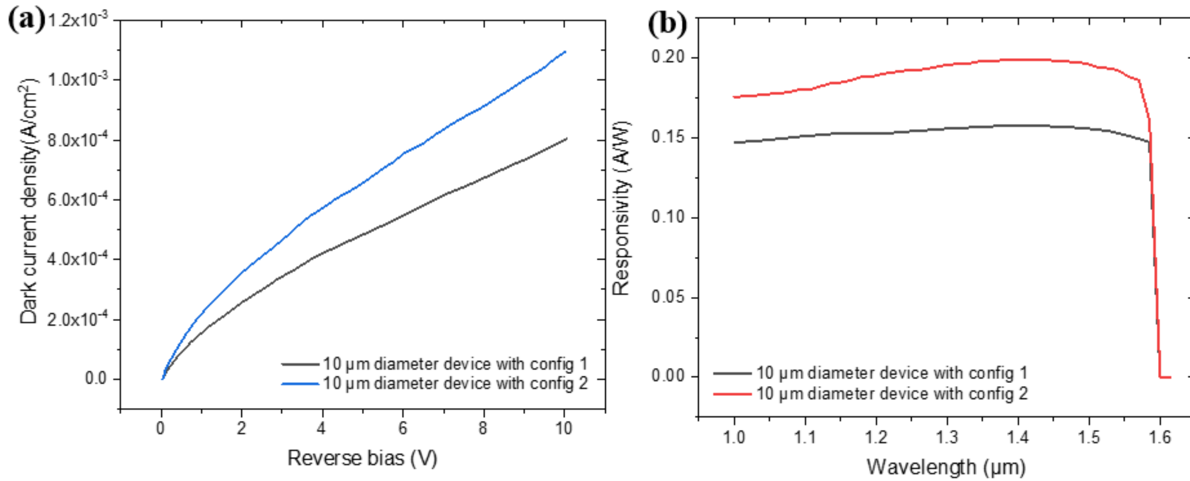

Figure 4.4 (a) dark current density comparison between devices with different top surface window configuration, (b) Responsivity comparison between devices with different top surface window configuration.

4.2 Performance enhancement in micro-sized IR photodetectors by side gate engineering

4.2.1 Side-gated structures background

Several attempts have been made to understand the mesa sidewall's surface and reduce surface leakage in infrared photodiodes. The use of various passivation, as well as the use of double heterostructure[43] and hybrid graded doping profile [43] in detector designs, have all been used in the past to suppress this phenomenon [44], [45], [46] and [47]. The current physical understanding of surface leakage current, on the other hand, does not allow for adequate control of its effect.

The gating technique has recently been shown to remove surface leakage [48] in mid-wavelength and long-wavelength infrared photodetectors. This technique can actively control sidewall surface band bending by forming a metal-insulator-semiconductor (MIS) structure on the mesa sidewall. Because of a significantly lower leakage current at a high gate bias, gated diodes demonstrated higher detectivity. The band bending on mesa-sidewalls is thought to be the cause of surface leakage. This band-bending leads to electron accumulation or type inversion at sidewall surfaces, forming a conduction channel along the sidewalls [48] and [45].

When no gate bias is applied, electrons accumulate on the insulator/Semiconductor interface, resulting in a conducting channel and surface leakage. Negative charges are stored at the metal-insulator interface

when the negative gate bias is applied, repelling accumulated electrons away from the insulator/semiconductor interface. As a result, flat band conditions can be created, as shown in Figure 4.5.

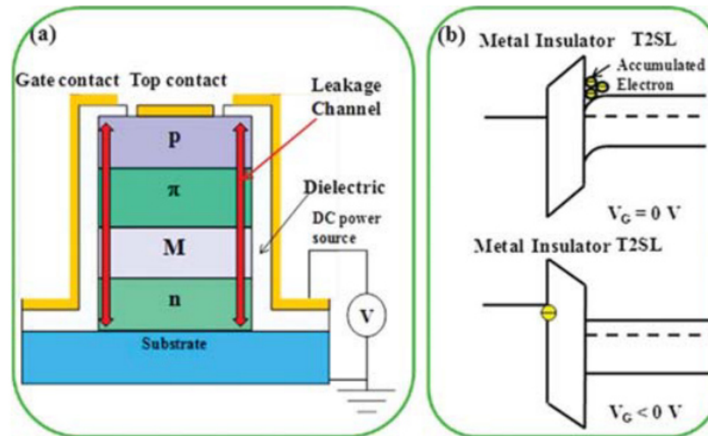

Figure 4.5 (a) Schematic diagram of a gated diode. (b) Surface band diagram of gated diode at zero and negative gate bias. [32]

However, this technique requires very high gate biases to be applied when the gate bias is less than or equal to saturated negative gate bias ($V_{G} < V_{sat}$) and not sufficient to generate a distinct field-induced depletion region at the absorption layer surface, holes accumulate at the surface, and the space charge region (SCR) remains primarily at the metallurgical junction.

The surface leakage current is eliminated because there is no significant change in the surface's SCR region or type inversion. As a result, when $V_{G} <= V_{sat}$, the dark current density is identical to the bulk dark current and remains unchanged concerning the gate bias.

Fixed charges at the absorption-passivation interface or within the passivation layer attract electrons when the gate bias is greater than V_{sat} but less than the threshold voltage of inversion ($V_{sat} < V_G < V_T$), leaving an SCR of uncompensated ionized acceptor ions near the p-region surface.

The surface generation-recombination (G-R) current associated with the surface depletion region is related to the surface field-induced depletion width, x_{sd}. When the mesa surface is depleted, the surface field-induced depletion width and hence surface G-R current increases with increasing gate bias, [49], resulting in a rising reverse dark current.

There are two options for reducing the high saturated gate bias: Reduce the dielectric layer's thickness or use a high-k dielectric material. The parallel capacitance formula can be used to calculate gate bias.

$$\sigma = \varepsilon\varepsilon_0 \mathrm{V}/\mathrm{d} \quad (4.3)$$

ε_0 is the permittivity in vacuum, ε is the passivation layer dielectric constant, σ is the surface charge density, and d is the dielectric thickness.

Understanding of the photodiode response performance when it is in gated condition needs to consider several analytical equations. The measured photocurrent density (J_{photon}) is made up of one or more of the four components shown in Eq. (4.4):

$$J_{photon} = J_{bulk} - J_{p-n} - J_{SDR} - J_S \quad (4.4)$$

J_{bulk} is the photocurrent density generated in bulk, J_{p-n} is the recombination current density within the p-n junction's depletion region, J_{SDR} is the recombination current density within the surface depletion region, and J_s is the surface recombination current density (J_S).

J_{SDR} and J_S do not contribute to the recombination of the photocurrent when the sidewall surface is accumulated or in flat band condition [50]. On the other hand, Both J_{SDR} and J_S contribute to the recombination of the photocurrent when the sidewall surface is depleted. The magnitude of J_{SDR} depends on V_G because the surface depletion width changes with V_G, and the magnitude of J_S is strongly related to the interface trap density of the absorption layer and the passivation layer. J_S no longer contributes to photocurrent recombination when the surface is inverted because all interface traps are filled, meaning they are not activated and can no longer act as recombination-generation centers.

The recombination in the surface depletion region (J_{SDR}) becomes maximal in this case because the surface depletion width is at its maximum value, which is determined by the applied anode voltage [50].

We will investigate the effects of gated structures on the performance of micro-sized photodiodes based on the observed improvement in the performance of mid and long-wavelength IR photodiodes.

4.2.2 Device structure and simulation

The micro photodetectors with a photosensitive area of 20 µm diameter were designed with 3 different passivation layer thicknesses (150 nm, 300 nm, and 600 nm). All of the devices consists of a 0.5 µm heavily doped n-type InP buffer layer (5×10^{18} cm^{-3}), a 2 µm lightly doped n-type InGaAs absorption layer (1×10^{15} cm^{-3}), a 0.1 µm heavily doped p-type InGaAs layer (1×10^{19} cm^{-3}) as an ohmic contact layer. More details about the depth of the etch, top surface contact configuration, and the gate structures could be seen in Figure 4.6.

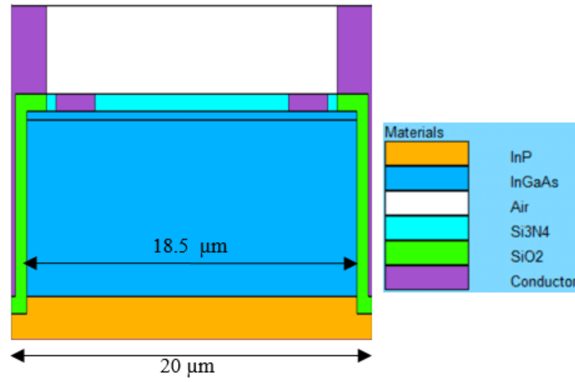

Figure 4.6 The cross section of gated micro-sized IR

We introduced surface recombination velocity and negative charge density for the micro-sized consideration and gated diode analysis purposes in the simulation settings. All of the parameters used in the simulation are bought in Table 4.1.

Table 4.1. The main parameters used in the SILVACO Atlas simulation

Parameters	Unit	InGaAs	InP
Band gap	eV	0.78	1.34
Effective conduction band density of states	cm^{-3}	7.62×10^{18}	5.66×10^{17}
Effective valence band density of states	cm^{-3}	7.62×10^{18}	2.03×10^{19}
Electron lifetime	s	1×10^{-7}	1×10^{-9}
Hole lifetime	s	1×10^{-7}	1×10^{-9}
Electron mobility	cm^2/Vs	12,000	4730
Hole mobility	cm^2/Vs	450	151
Bulk trap density	cm^{-3}	3.5×10^{13}	-
Surface recombination velocity	cm^{-2}	5×10^{3}	-
Negative charge density	cm^{-2}	2×10^{11}	
Ref.		[10]	[10]

4.2.3 Results and discussion

This section discussed improving the gated micro-sized photodetectors' performance via the investigation of gate effects on dark current and the EQE. Figure 4.7 shows the current-voltage characteristics of the gated photodetectors in various bias conditions. When no gate bias is applied, the dark current values are related to the anode voltage and increase with its values. In addition, in this condition, the surface depletion width is thought to be at its maximum. The surface G-R current will not change with gate bias in this scenario, and the mesa surface will be inverted and form a leakage

channel, resulting in the high tunneling leakage current. The reverse dark current density decreases as gate bias approach -10 V, indicating that the mesa surface is becoming less depleted. The decrease in dark current seen does not come from bulk current because the diode operation bias is fixed for each curve; however, the dominant dark current mechanism in this region, the surface G-R current, is decreasing. When the dark currents of the two curves are compared at the same gate bias, the surface G-R current at higher applied anode voltage is found to be greater, which is due to an increased surface depletion width at higher diode reverse operation bias, as described in [49]. When the gate bias exceeds gate saturation voltage ($V_{gs=}$-8V), the reverse dark current is dependent on the operation bias rather than gate bias, implying that the surface leakage current is eliminated and the mesa surface is accumulating.

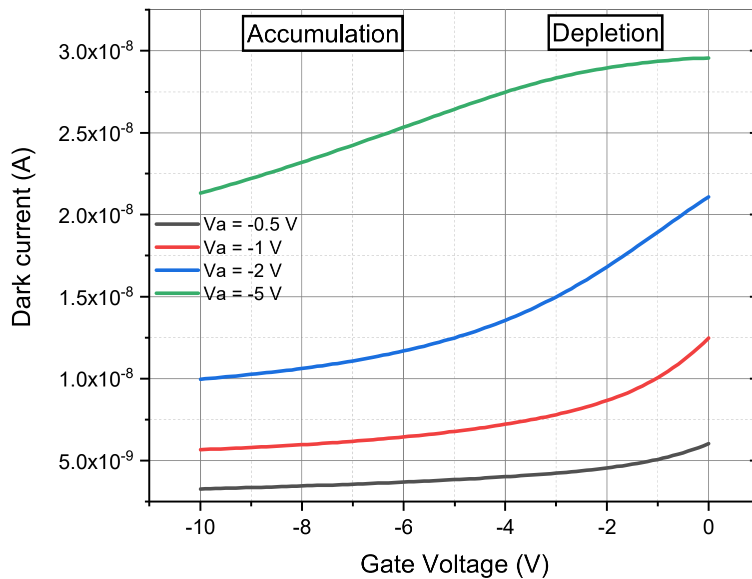

Figure 4.7 The correlation between the dark current and gate bias at various diode operation biases.

We plot the electron concentration, electric field, and SRH contours in 500 nm from the sidewall to the bulk area for various gate voltages to better understand the effect of the gate voltage on the condition of the diode sidewall. Figure 4.8 shows the electron concentration contours as the main photogenerated carriers in the absorption layer. With the increase of gate voltage, as we expected, the concentration of electrons has been reduced due to electron repelling to the bulk area because of the band bending occurring.

This phenomenon is obvious in the contours by considering the enlargement of the light orange areas with lower electron concentration, proving the decrease of the electron concentration in the sidewalls.

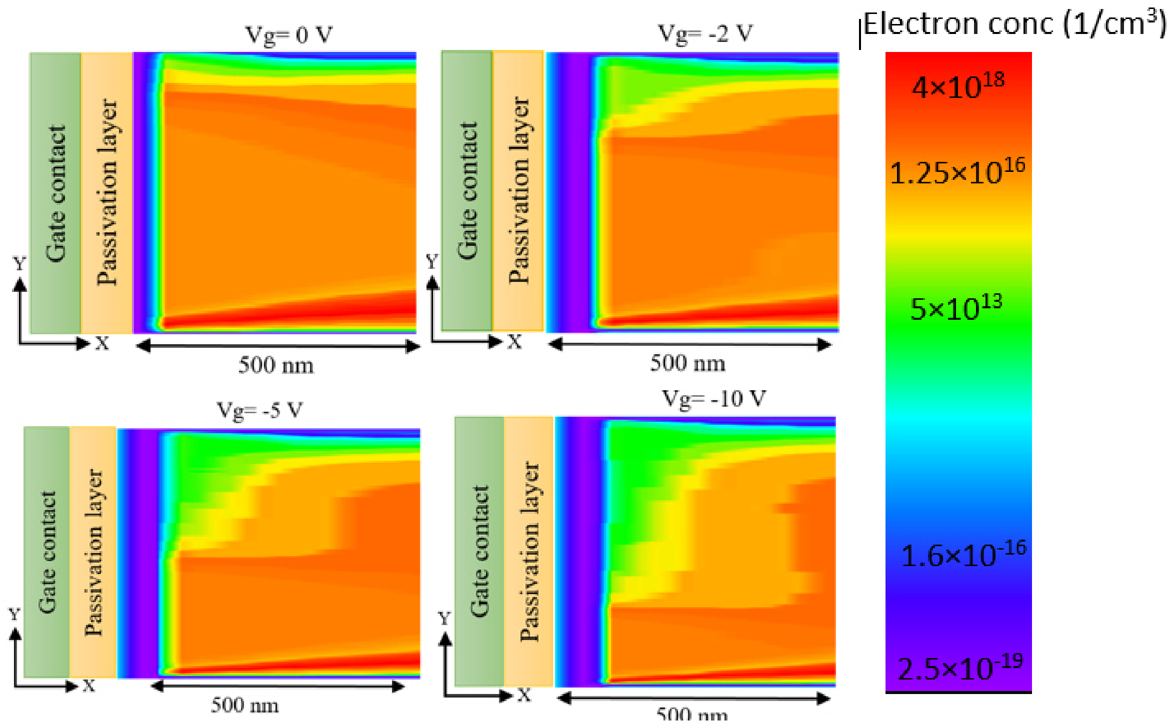

Figure 4.8 Electron concentration contours for various gate voltages in the sidewall

The electric field in the sidewalls can also be used to investigate the condition of electron concentration in greater depth. Figure 4.9 exhibits the electric field contours near the absorption layer's sidewalls. The effects of electron repelling could also be seen here, as the electric field close to the sidewalls was increased as the gate voltages were increased. Because of the increased emptiness of the sidewalls from electron carriers, this effect can increase dark red areas in the sidewalls.

Finally, in Figure 4.10, the SRH rate contour at the sidewalls was used to examine the generation-recombination condition. The SRH recombination decreased as the gate voltage was increased, as shown in these contours. Because the SRH rate is related to electron concentration, this phenomenon could be explained by decreasing electron concentration. In addition, the increase in the size of the yellow area with a lower SRH rate with the increase in the applied gate voltages indicated a decrease in the SRH rate in the contours.

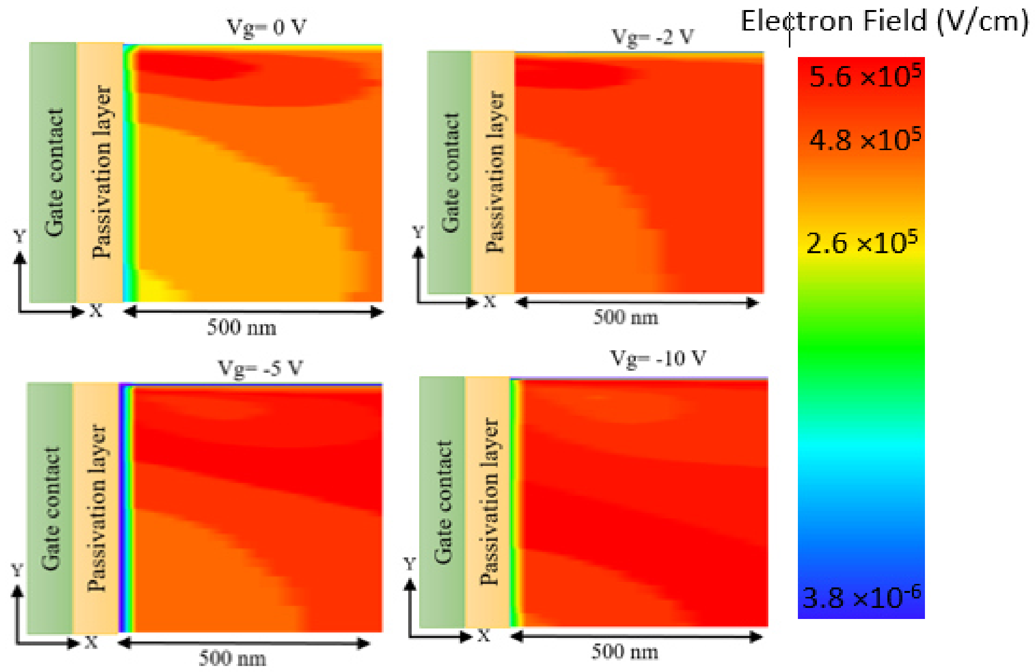

Figure 4.9 Electric field contours for various gate voltages in the sidewall area.

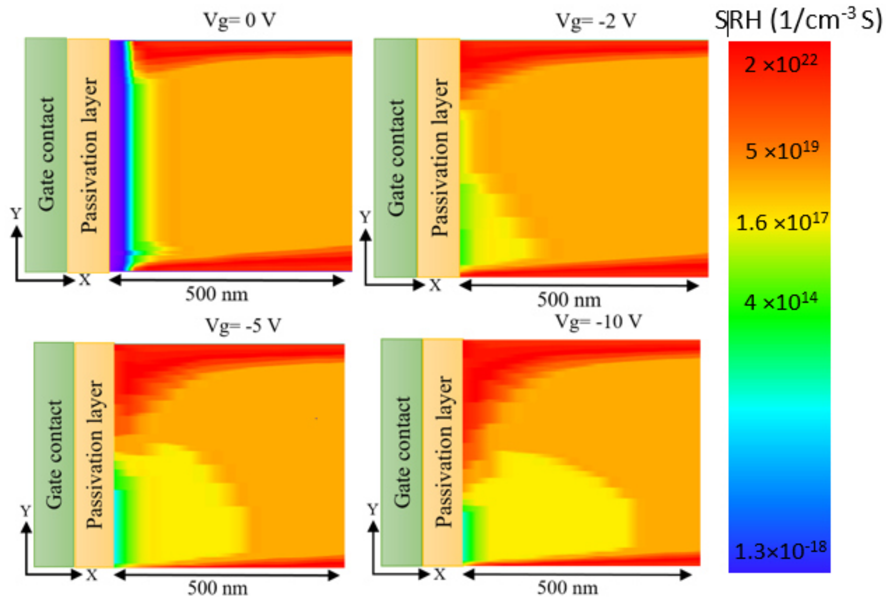

Figure 4.10 SRH rate contours for various gate voltages in the sidewall area.

In another investigation direction, we studied the effects of various passivation layer thicknesses on the gating effects. Figure 4.11 (a, b) shows the effects of a different passivation layer on the dark current and the EQE of the gated photodetectors. Figure 4.11 (a) shows that the micro-sized photodetector with lower thickness has a better gating effect on the dark current, according to the theory about the relationship between the gate saturation voltage and the passivation layer thickness mentioned in section 4.2.1. In addition, at the same gating voltage, the device with a thicker passivation layer has a higher dark current, indicating that the gating is less effective due to the higher fixed charge density and less effective charge transport performance.

The correlation between the reverse gate bias and the EQE of 1.55µm illumination for gated photodetectors in various passivation layer thicknesses is depicted in Figure 4.11 (b).

Each curve shows that as the gate voltage was increased, the EQE increased due to the suppression of surface recombination [51]. In addition, when comparing the EQE of photodetectors with different passivation layer thicknesses, as expected, the gating setting with a thinner passivation layer improves the device response more effectively than the devices with a thicker passivation layer due to the mentioned reasons for the dark current. This EQE increment for the 150 nm passivation layer was 18% in Vg=-10 V, which is comparable to the improvement for the mid-wavelength IR gated photodetectors. To better understand the effect of passivation layer thickness on the condition of the gating of the diode sidewall, we plot the electron concentration and SRH contours in 500 nm from the sidewall to the bulk area for devices with various passivation layer thicknesses. Figure 4.12 shows the electron concentration contours close to the absorption layer surface. With the decrease of the passivation layer, as we expected, the concentration of electrons has been reduced due to more effective electron repelling

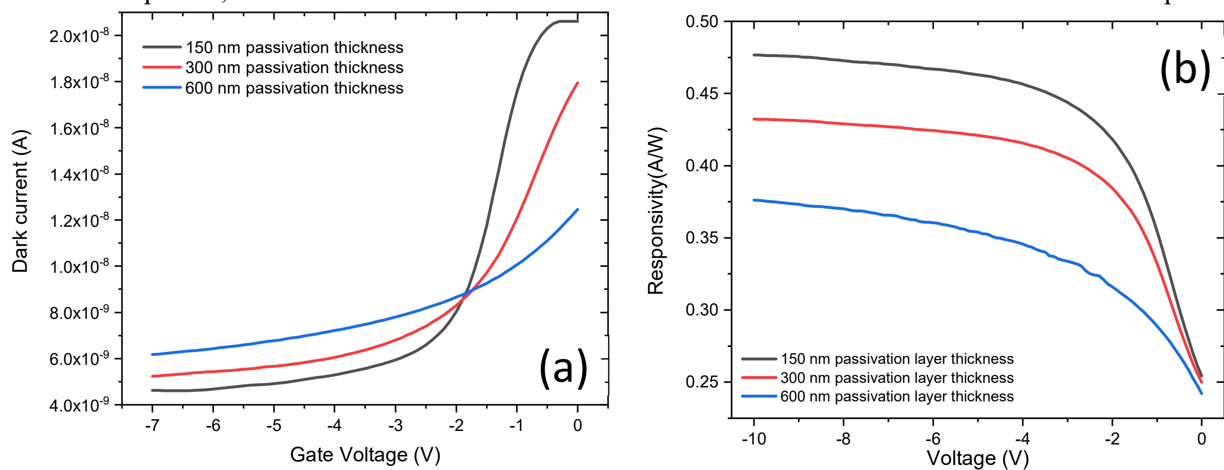

Figure 4.11 (a) The correlation between the dark current and gate bias at various passivation layer thickness, (b) The correlation between the EQE of 1.55µm illumination and gate bias at various passivation layer thickness.

to the bulk area occurring because of the lower gate saturation voltage and easier charge transport. This phenomenon is evident in the contours by considering the enlargement of the light orange areas with lower electron concentration, proving the decrease of the electron concentration average in the sidewalls.

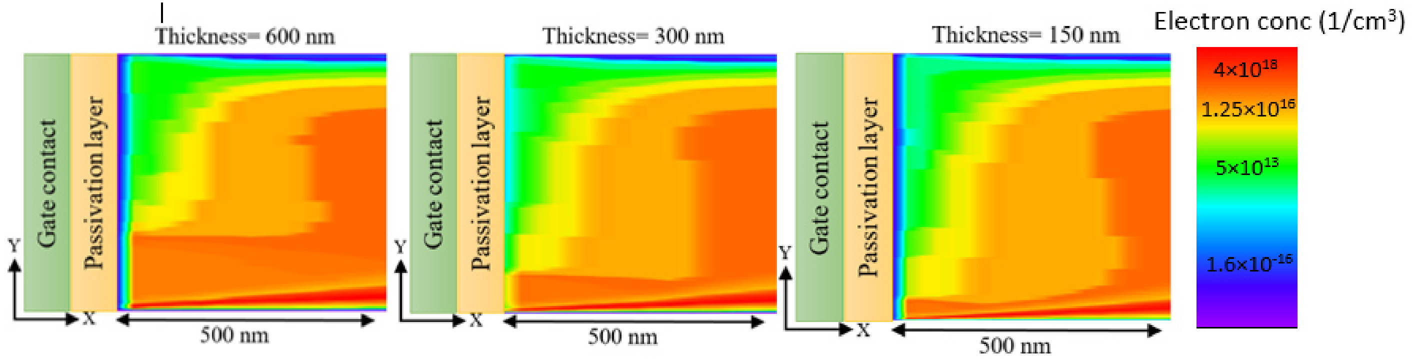

Figure 4.12 Electron concentration contours for devices with various passivation layer in the sidewall area.

The generation-recombination condition was also investigated using the SRH rate contour at the sidewalls for devices with various passivation layer thicknesses in figure 4.13. As the passivation layer thickness was decreased, the SRH recombination decreased, as shown in these contours. Because the SRH rate is linked to electron concentration, a drop in electron concentration could explain this phenomenon. The size of the yellow area with a lower SRH rate grew larger, indicating a decrease in the SRH rate in the contours corresponding to the devices with a thinner passivation layer.

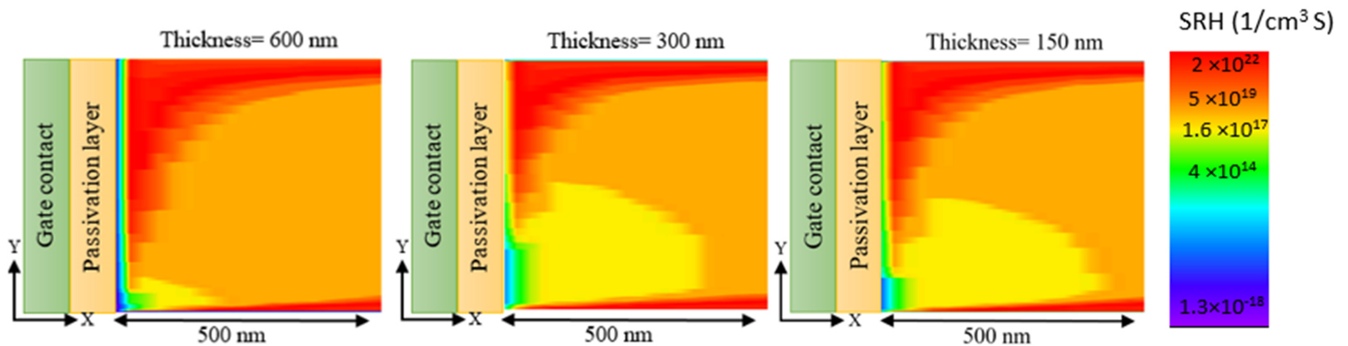

Figure 4.13 SRH rate contours for devices with various passivation layer in the sidewall area.

4.3 Conclusions

In this chapter, we looked into some of the possible strategies for improving the performance of micro-sized IR photodetectors.

First, because the top window layer's size shrinks as the photodetectors' size shrinks, optimizing this layer for better light-device coupling becomes more critical. FDTD solutions and SILVACO softwares were used to compare two top surface window layer configurations optically and optoelectrical. Because the second configuration has a smaller metal contact area, it has less top surface reflectivity and better light-device coupling. As a result of the optoelectrical simulations, it was determined that the 10 µm diameter photodetector's responsivity has improved by 33.33 percent.

Second, we attempted to cancel out the size-dependent effects of the performance of micro-sized photodetectors in another section of this chapter. We investigated the impact of the gating technique on both the electrical and optical characteristics of devices in this regard. According to the literature, the gating technique aids in repelling photogenerated electrons from absorption layer sidewalls by causing a change in surface potential due to the reverse bias voltages. We looked at a 20 µm diameter device to see how the gating affected its performance. According to the optoelectrical simulation results, the dark current and EQE of the devices improved with different gate voltages and passivation layer thicknesses. The best improvement was an 18 percent increase in the EQE of the 20 µm diameter device, which is a very high value for this parameter. We also plot the electron concentration, electric field, and SRH rate contours at the sidewalls to better understand the sidewalls' condition in ungated and gated situations, confirming the same results as optoelectrical investigations.

Chapter 5 Conclusions and Future Work

This thesis reports a comprehensive study on InP/InGaAs micro-sized photodetectors. The SILVACO simulation software and FDTD solutions were used to simulate the optoelectrical and optical properties of the micro-sized devices. The mechanisms that affect the dark current and photoresponse performance of the InP/InGaAs photodetectors were explained. With the reduction of device size, the surface recombination rate plays a more critical role in the performance drop due to the device's high surface area to volume ratio.

Various strategies have been studied to suppress the surface recombination effect and improve the dark current density and the EQE or the photoresponse performance of the micro-sized photodetectors. These strategies consist of optimizing the top surface light entrance of the devices, which could be more important in the small-sized devices, and the investigation of the gating effects. Each of them can improve the performance of the micro-sized IR photodetectors for at least 18 percentages by optimizing the applying gate voltage and the passivation layer thickness.

In conclusion, a comprehensive study of InP/InGaAs micro-sized PDs is reported in this thesis, in which new device work mechanisms and simulation results are presented. A newly designed micro-sized PD with optimized top surface opening window and the gated PD is demonstrated.

There are some clear future works:

1. Further examination of the working mechanism of micro-sized PDs with a new design should be conducted. Based on their experimental grown, fabricated, and tested devices.

2. Various device characterization such as temperature-dependent, polarization-dependent, and so on should be investigated to understand better the device's performance and more detailed physical perspective.

3. Smaller devices should be investigated to make a theoretical foundation for the devices, including arrays of pixels instead of single-pixel photodetectors.

4. More materials-based characterizations like carrier lifetime investigations and interface trap densities investigations should be done to understand better the device's essential aspects in a

micro-scale.

5. Last but not least, to enhance the responsivity of the small devices, application of light trapping structures on top of the device should be investigated to reduce the reflection.

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