Characterization of gate oxides and microwave resonators for silicon spin qubit devices

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Silicon quantum dots present themselves as a promising implementation for quantum information processing due to the fact that they possess a small chip foot-print, yield high coherence times and are able to leverage the semiconductor industry. These nanoscopic devices rely on forming an electrostatic confinement for individual electrons. To accomplish this, an overlapping metallic gate geometry is implemented. The overlapping metallic gates are typically electrically isolated from one another by an insulating asher oxide layer. Due to unreliable processes during quantum dot fabrication, we substitute the asher oxide for a more robust and reliable oxide. For this, gate-oxide test structures are fabricated to simulate the overlapping gate geometry while various oxides are grown and deposited. It is found that oxides, grown by either ashing or hotplate in tandem with atomic layer deposited Al_2O_3, yield substantially higher breakdown voltages than conventional methods.

One issue single electron spin qubits face is noise generated by charge traps. Charge traps appear at the Si/Oxide interface and seriously impedes many aspects of a quantum processor such as qubit coherence times, electrostatic screening effects and two-qubit gate fidelities. Here, we characterize the density of interface traps on a multitude of oxides found in the Quantum Nano-Fabrication and Characterization Facility. These oxides include plasma enhanced chemical vapour deposition (PECVD) SiO_2, Tystar dry oxidation, commercial thermal SiO_2, atomic layer deposition (ALD) Al_2O_3 and ALD HfO_2. We find that each of these oxides is plagued by a high density of fixed charge and interface traps. We also implement forming gas anneals at high temperature to help passivate the charge traps. It is found that a forming gas anneal at 400C for 10 minutes reduces the number of interface traps by several orders of magnitude and that PECVD SiO_2 and ALD Al_2O_3 host the smallest interface trap density of approximately 10^{10} eV^{-1} cm^{-2}.

A major issue facing this implementation of quantum computing is the ability to scale-up. Current methods of single qubit rotation are electron spin resonance and electron dipole spin resonance. In either method, a high frequency (HF) transmission line is placed nearby the quantum dots. For a large scale quantum computer, hundreds to thousands of transmission lines and therefore HF interconnects will be necessary, dramatically increasing the complexity of the device and reducing the qubit packing density. In this thesis, we present an elegant solution, dramatically reducing the need for many interconnects. A superconducting microresonator sits directly above the quantum processor providing an oscillatory magnetic field to perform single qubit rotations over an area of 1 mm^2. With a modest quantum dot pitch of 100 nm, approximately 40 million qubits can fit within this region. The resonator possess a unique shape to minimize the electric field component while maximizing the magnetic field 'felt' by the qubits. Electrons are tuned on and off of

resonance by electrostatic tuning of the electron g-factor. We fabricate and characterize a prototype resonator's transmission coefficient to determine its resonant frequency at room temperature and at 1.4K. Both measurements agree with simulations with a resonance frequency of approximately 16 GHz.

Acknowledgements

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Life in Waterloo would not have been what it is without Kira and Eisen by my side. You have both been supportive of me through this process and have helped me grow as a person. I am forever grateful that you two are in my life. I would like to thank my family, Mark, Lesley and Jack for their love and endless support. Thank you for being there for me from beginning to end. This would not have been possible without you all.

Dedication

To my parents.

Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

Today, a plethora of research is being accomplished in the field of quantum computation. It has been shown that a quantum computer is advantageous over a classical computer for unordered searches [18], simulations of chemical systems [17], prime number factorization [42], and machine learning [32]. A classical computer performs many operations (electrical switches) on bits of information (0 and 1 states) to complete a task. On the other hand, a quantum computer leverages the unique properties of the quantum world to complete select tasks. Quantum superposition allows quantum bits (qubits) of information to be described as a combination of 0 and 1 states. Moreover, a quantum computer's fast calculation speed derives from more quantum mechanical phenomena such as entanglement and interference. Currently, quantum computers are small with the largest being only 53 qubits [20] and are prone to errors. These existing devices are often called "Noisy Intermediate-Scale Quantum" (NISQ) computers. Implementing the aforementioned algorithms will require millions of physical qubits while additionally requiring many more to implement error correction protocols. We are far from a fault-tolerant quantum computer. Despite this, Shor's algorithm (prime number factorization) amongst others has been demonstrated and tremendous progress towards large-scale quantum computers is being achieved [46].

In 2000, DiVincenzo introduced five requirements for physical qubits to meet [13]:

1. A physical implementation of a qubit.
2. The ability to initialize the qubit into some known state.
3. The coherence time of the qubit is long.
4. Universal set of quantum gates.

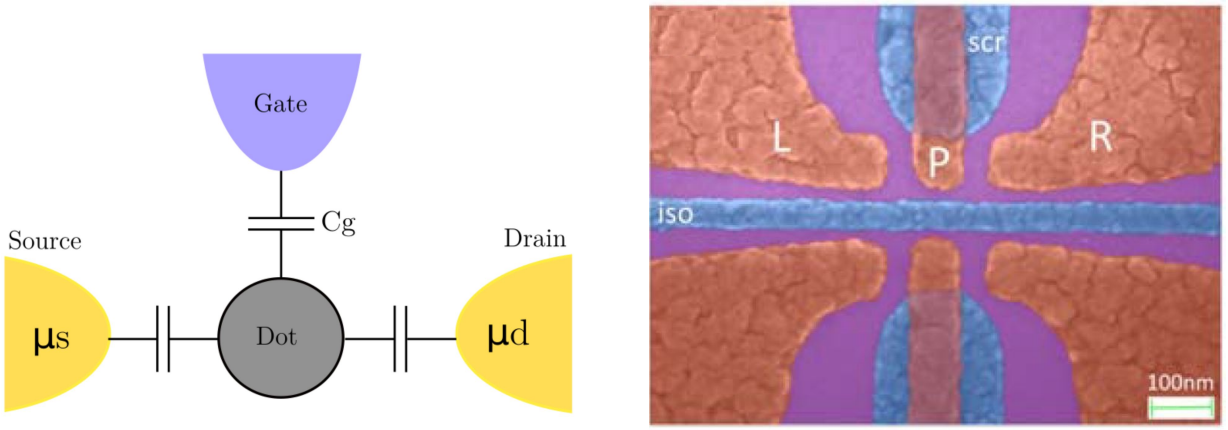
5. The ability to readout the state of the qubit.

In the next 20 years, the field of quantum computing has progressed to the point where there exists a myriad of platforms and material systems which follow the above requirements. These include nuclear magnetic resonance [11], superconducting circuits [9], diamond nitrogen vacancies [7], ion traps [8] and quantum dots [29]. Each of these platforms has their own advantages and disadvantages. One of the first architectures, proposed by Loss and DiVincenzo, were electron spins in semiconductor quantum dots. Quantum dots are regions of electrostatic confinement, often generated by metallic gating, which trap electrons or holes. Quantum dots are an attractive implementation for a quantum computer for several reasons, namely electronic states form a natural two-level system under the influence of an external magnetic field. Secondly, quantum dots fabricated on semiconductors can leverage the semiconductor industry which has seen unbounded growth in the past few decades. Finally, entangled states, a necessary ingredient in a universal quantum computer, can be generated by the exchange interaction between two adjacent electrons. The work presented within this thesis focuses on improving the material properties and fabrication methods relevant to silicon quantum dots. While quantum dots are not utilized here, it is necessary to discuss basic quantum dot theory within the context of improving and optimizing them.

1.1 Single quantum dot transport

Electron spin qubits in silicon quantum dots present themselves as a promising candidate for scalable quantum computation. This is owing to their addressability and electrical control but also the intrinsic properties of silicon. Isotopic purification of silicon allows for a 'nuclear vacuum', further increasing coherence times of qubits. In this chapter, the transport and spin physics of quantum dots and electron spins, respectively, will be discussed.

A quantum dot is a region of space which is used to confine or trap individual electrons (or holes). Electrically tuneable gates are patterned on the surface of a Si substrate to define a potential landscape. Figure 1.1a shows a schematic of a quantum dot coupled to source and drain leads whereas figure 1.1b shows a single quantum dot fabricated on a silicon substrate. The leads are a two-dimensional electron gas (2DEG) at the Si/SiO_2 interface, which is generated by additional metallic gates known as accumulation gates. When the voltage on these gates reaches a certain threshold voltage, V_{th}, a 2DEG is formed where electrons are confined in 2-dimensions. The accumulation gates extend from the area where



(a) (b)

Figure 1.1: (a) Schematic of a single quantum dot between two leads. The dot is capacitively coupled to the source, drain and the top gate. (b) [Reproduced] from [37]] Colourized SEM image of a single quantum dot which is labelled by the metallic gates, L, P, R and SCR. Here, P is the plunger top gate and L and R accumulate a 2DEG nearby the dot.

the dot is formed to a highly doped region which acts as an ohmic contact. The ohmic contacts supply carriers to the 2DEG. The source and drain leads are capacitively coupled to the dot forming tunnel barriers. Furthermore, the source and drain are the reservoir for electrons to tunnel into and out of the quantum dot. Often, a tunnel barrier gate is used to tune the tunnel rate of electrons. The reservoirs are used both in the initialization and readout of the spin states. A metallic top gate is also capacitively coupled to the quantum dot with capacitance C_g. The voltage of this top gate, V_g, allows for the control of electron occupancy within the dot. Due to the lateral confinement of the quantum dot, quantized electron orbitals are formed. An electron within a quantum dot is often compared to that of a 3D particle in a box, whose energy levels are $E = \frac{h^2}{8m^*}(\frac{n_x^2}{L_x^2} + \frac{n_y^2}{L_y^2} + \frac{n_z^2}{L_z^2})$, where m^* is the effective mass of the electron, n_x, n_y, n_z, are three quantum numbers which describe the state and L_x, L_y, L_z are the three spatial lengths of the box. For a quantum dot, if $L_z << L_x$,L_y, the result is effectively a 2D system.

In the leads, electrons will occupy states up to the chemical potential of the source and drain, μ_s and μ_d, respectively. When the chemical potential of the source and drain are different, for example, $\mu_s > \mu_d$, then a bias is being applied across the dot. When the energy levels of the quantum dot lie within this "bias window", a current can be measured as electrons can tunnel from the source to the available state within the dot, then tunnel

to the drain. When there is no energy level between the bias window of the leads, current is suppressed. This configuration is known as Coulomb blockade (Fig. 1.2a). Coulomb blockade is an important feature of quantum dots as it forces the electron occupation of the dot to be fixed within each blockaded region, i.e. each Coulomb diamond. It can be found that current blockaded regions occur over a range of bias voltages V_{bias}, resulting in the formation of diamond shaped regions of zero current. The Coulomb diamonds are shown in figure 1.2b. As the gate voltage increases, each new diamond indicates the addition of an electron tunnelling onto the quantum dot. Useful information about the quantum dot can be extracted from this measurement. The width of the Coulomb diamond directly tells us the charging energy, E_c, the amount of energy required to add an electron to the quantum dot. Furthermore, the slope of the edges of the diamond is related to the capacitance between the quantum dot and the source and drain leads. When the number of electrons decrease on the dot, the current through the dot decreases. This is because as V_g decreases, the dot becomes smaller and the barrier potential height between the dot and source/drain leads tends to become more opaque. For small electron occupancies of the dot, the current is often too small to directly measure. In this case, a charge sensor is used to determine electron occupancy. A charge sensor is typically another quantum dot or single electron transistor (SET) located nearby the dot. The charge sensor dot is close enough to be capacitively coupled to the dot of interest. The charge sensor is tuned to a regime where the sensor current, I_{sensor}, is measured. In other words, the sensor dot is tuned along the edge of a Coulomb peak. When this occurs, because the charge sensor is capacitively coupled to the dot of interest, it becomes sensitive to electrostatic fluctuations in the surrounding area. When the electron occupancy of the dot of interest changes, the charge sensor is perturbed and a measurable change in sensor current is observed. This allows for monitoring of the electron occupancy down to the last electron. This method is often used, in conjunction with spin-to-charge conversion, for spin read out [35].

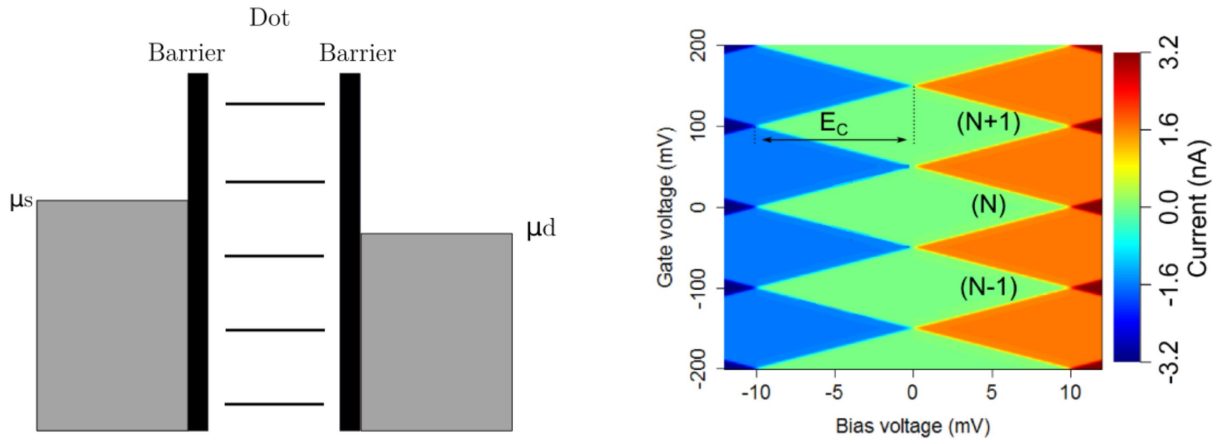


Figure 1.2: (a) Energy level diagram of a quantum dot in a Coulomb blockaded regime. No energy level within the dot lies between the chemical potential of the source of drain. (b) [Reproduced from [19]] Current as a function of bias voltage and gate voltage showing a Coulomb diamond structure. The green diamond regions indicates zero current through the dot and a fixed number of electrons (N-1, N, N+1) on the device.

1.2 Double quantum dots

Double quantum dots are merely an extension of single quantum dots. That is, instead of having one conducting island between a left and right lead, there are now two conducting islands in series. However, a double dot system allows us to perform two-qubit gates, an essential ingredient in developing a quantum computer. A schematic of a double quantum dot is found in figure 1.3. The double dot system now requires two metallic plunger gates to control the chemical potential of each dot. For now, it is assumed that the metallic gate of one dot does not affect the chemical potential of the other dot. Only the case where the bias is small is considered.

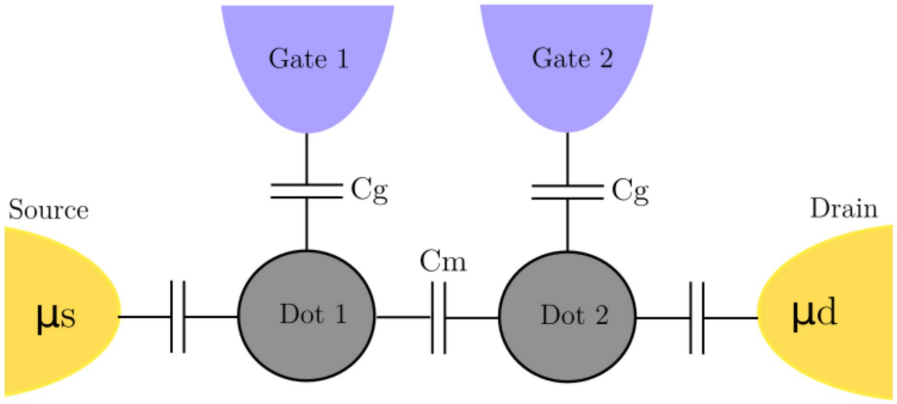
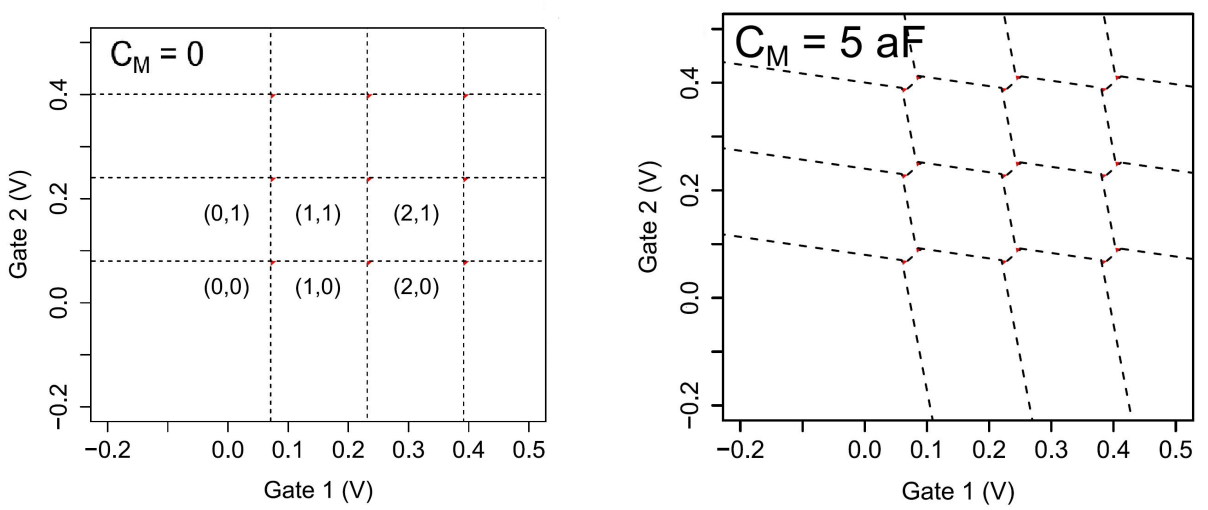


Figure 1.3: A schematic of a double quantum dot between two leads. Each dot is capacitively coupled to a local plunger gate.

Knowing how current can pass through a double dot is crucial as it leads to the formation of stability diagrams. The charge stability diagram is a fundamental tool in characterizing gate defined double quantum dots as it reveals information about the charge occupation in each dot at any given gate voltages, V_{g1} and V_{g2}. The current through the double dot can be determined using a similar manner as that of the single quantum dot. That is, focusing on the chemical potentials of the leads, μ_s, μ_d, and the dots, μ_1, μ_2. If a very small bias is applied, that is, $\mu_s \geq \mu_d$, the current will only be non-zero when a charge state in both dots is aligned with the leads. When the current is plotted as a function of V_{g1} and V_{g2}, a square pattern is observed, as seen in figure 1.4a. The dashed lines indicate areas of fixed charges on both dots. The fixed charges in these dashed lines are considered stable as they do not change until a dashed line is crossed, hence the name, charge stability diagram. In the case where the dots are not coupled to each other, the dots behave as if they are two single dots. When one gate voltage is held constant and the other varies, only one dots' occupation will change. This example is useful to consider but it is not realistic as the dots are spatially close enough to be capacitively coupled to one another. In real systems, there is a capacitive coupling between the two dots, C_m, as the number of electrons on one dot affects the chemical potential of the other dot. With respect to the charge stability diagram, this results in a skew in the dashed lines indicating each dots occupation but also, the points of current split into two points. Each of these points is called a triple point because they correspond to 3 different electron occupation configurations. A typical charge stability configuration can be seen in figure 1.4b. The skew to the dashed lines and the triple points results in hexagons dictating electron configuration. Another variable to consider is the capacitive coupling from the first metallic gate to the second dot and vice

versa. This cross capacitance shifts the location of triple points, further skewing the charge stability diagram.



(a) (b)

Figure 1.4: [Reproduced from [19]](a) Stability diagram for a pair of uncoupled ($C_M = 0$) double quantum dots as a function of both top gate voltages. (b) Stability diagram for two coupled ($C_M = 5$ aF) as a function of gate voltages. Dotted lines separate regions of differing charge occupation for a double dot system.

1.3 Electron spins as qubits

There are several ways to implement electron spins as qubits within quantum dots, such as a single-spin qubit with one electron in one quantum dot, or a singlet-triplet qubit with two quantum dots each with one electron [33]. Additionally, hybrid-qubits with two quantum dots with two electrons in one dot and one electron in another [23], and more recently, dressed spins with a single electron within one quantum dot but dressed by a constant oscillating magnetic field [28]. Each realization of a qubit has its own advantages and disadvantages. For example, singlet-triplet and hybrid qubits, have relatively fast manipulation times but relatively short coherence times. Single electron spins as qubits, however, have the advantage of longer coherence times and provide one qubit per quantum dot. On the other hand, they require coupling to an oscillating magnetic field and qubit rotations

are relatively slow. In this thesis, only single electron spin qubits will be considered as it was the first realization proposed by Loss and DiVincenzo [29]. The first step is to define two distinct states to represent qubits. Earlier, it was described that an electron within a quantum dot was like an electron in a 3D box. This is studied extensively in undergraduate physics courses so only the fundamental concepts will be addressed. When solving the Schrödinger equation for any given potential, the spin of the electron is decoupled from the spatial part of the wavefunction. Kramer's theorem states that each energy eigenstate is doubly degenerate for a spin-1/2 particle. With doubly degenerate spin states there are no mechanism to manipulate their superposition or to read out their state. This degeneracy can be broken by applying an external perturbation in the form of a static external magnetic field, B_0. B_0 lifts the spin degeneracy forming a two-level qubit system. The rest of this chapter provides an introduction to utilizing a single spin in a quantum dot. The areas covered are qubit initialization, single-qubit rotations, two-qubit rotations, and qubit measurement.

1.4 Initialization

As previously stated, the external magnetic field results in an energy splitting of the qubit states. This energy splitting is referred to as Zeeman splitting and the magnitude is often represented by $E_z = g\mu_B B_0$, where g is the g-factor of an electron (g$\sim$2) and μ_B is the Bohr magneton. Spin qubits are typically operated with an external magnetic field ($|B_0|$) on the order of a few hundred mT. In order to initialize a spin-up $|\uparrow\rangle$ state, we consider a single quantum dot adjacent to an electron reservoir. A quantum dot is formed by applying a gate voltage to the metallic top gate leaving unoccupied spin states within the dot. The chemical potential of the adjacent lead is then tuned to fall between the Zeeman split spin states. Because the energy of the ground state qubit ($|\uparrow\rangle$) is below the chemical potential of the lead, it is energetically preferential for an electron to tunnel from the lead to this state. If using an external magnetic field $|B_0| = 500$ mT, then $E_z \approx 55$ μeV. If the temperature of the system is too high, electrons will be able to tunnel into the excited state of the dot. Reducing the temperature of the system as much as possible maximizes the probability of loading in a ground state electron. If an electron tunnels into the excited state, waiting $5\mathrm{T}_1$ allows the electron to relax into the ground state. Typically, experiments are performed in a dilution refrigerator where temperatures can reach 100 mK or below.

1.5 Single-qubit gates

Quantum computing relies on being able to perform quantum operations on qubits. Moreover, it is crucial that these operations be fast (compared to qubit decoherence time) and have high fidelity. There are two types of operations to discuss: single-qubit operations and two-qubit operations. We begin by discussing single-qubit operations on electron spins in quantum dots. The underlying mechanics of single qubit operations are nearly identical to that of NMR quantum computing. Electron spins are manipulated by electron spin resonance (ESR). The applied static magnetic field, B_0, is produced by large superconducting magnets in the cryostat and sets the Zeeman energy splitting and therefore the frequency of the qubits (Larmor Frequency). This Zeeman splitting is mediated by the magnetic moment of the electron, $\tilde{\mu} = -\frac{1}{2}\hbar\gamma\tilde{\sigma}$, where γ is the gyro-magnetic ratio and σ_z is a Pauli operator. Applying oscillatory magnetic field pulses, $B_1(t)$, at the Larmor frequency and orthogonal to the static field will cause a transition between the two spin states (spin-up and spin-down) and determines the qubit transition frequency (Rabi Frequency). The Larmor frequency tends to be on the order of 10s of GHz while the Rabi frequency is typically of the order MHz. The microwave pulses can be implemented via superconducting microstrip lines placed within a few hundred nanometres of the quantum dots. Recent methods of implementing microwaves pulses utilize resonant cavities, whereby a coaxial loop couples to a dielectric resonator to produce a global magnetic field. Microstrip transmission lines have been widely used and demonstrate high fidelity single-qubit operations F > 0.999 [48]. These transmission lines, however, take up valuable chip space and the number of transmission lines scales with the number of qubits. Furthermore, many high-frequency coaxial cables would be needed to deliver microwave pulses into the cryostat. Another possible concern is that large currents running through numerous transmission lines could raise the temperature of the chip.

An alternative method for local spin control is electric dipole spin resonance (EDSR). EDSR requires large micromagnets in the vicinity of the quantum dots to produce a magnetic field gradient. This method was originally shown by Pioro-Ladriere et al [34]. The micromagnets are magnetized in the direction of the external magnetic field, B_0, to create a magnetic field gradient within the quantum dot region. The magnets tend to be significantly larger (on the order of microns) than the quantum dots. Next, a microwave is applied to a nearby terminated transmission line. The goal of the microwave electric field is to displace the electrons wavefunction within the quantum dot. In the presence of the magnetic field gradient, the displaced electron wavefunction 'feels' an effective oscillatory magnetic field which induces transitions between spin states. This only occurs when the microwave frequency equals the Larmor frequency. In the same vein as the ESR trans-

mission line, EDSR suffers from similar issues. However, now micromagnets take up even more precious chip space. Scaling up with this method proves difficult as the gradient field lines from the micromagnets can shift the Larmor frequency of the qubits. Another promising method of inducing spin rotations is utilizing a global RF magnetic field. Resonant cavity is a good example of creating a global magnetic field. It is a device that leaves no chip footprint and drastically reduces the number of interconnects when scaling up to multiple qubits. Scaling up to hundreds or thousands of qubits yields other issues when implementing global magnetic fields such as targeting individual qubits for rotations. This can be achieved by modulating the g-factor locally via the Stark shift, which will be further discussed in Chapter 4.

1.6 Two-Qubit gates

Much like single-qubit gates, the two-qubit gate is also crucial to be able to implement with high-fidelity as it is necessary for universal quantum computation. Furthermore, since quantum computing takes advantage of superposition and entanglement, two-qubit gates are essential for generating Bell states [49]. Two-spin quantum gates are mediated via the exchange interaction. The exchange interaction is a function of the atomic orbital overlap of two electrons within two separate quantum dots. The strength of the exchange interaction can be modulated by increasing or decreasing this overlap. Implementing a two-qubit gate requires only local gate control to allow the electrons to interact with one another. Therefore, enabling the exchange interaction results can result in a root SWAP gate operation [30]. One particular implementation of a CNOT gate requires a magnetic field gradient across the double quantum dot system, creating a different Zeeman energy splitting for each electron. In the presence of a magnetic field gradient the exchange interaction reduces the energy of the antiparallel spin states relative to the $|\uparrow\uparrow\rangle$ and $|\downarrow\downarrow\rangle$ spin states. This results in the transition frequency of the left qubit being dependent on the state of the right qubit, and vice versa. In this situation, the left qubit will be the control qubit [49].

1.7 Qubit Readout

Nuclear magnetic resonance (NMR) quantum computing determines the spin state by measuring the net magnetization of the bulk sample. This, however, is not possible when working with single spins as the individual magnetic moment is too tiny to measure. Early

methods of spin readout were based on a method first demonstrated by Elzerman et al. [15]. This method is implemented by having a quantum point contact (QPC), or SET, in proximity (100 nm's) of a quantum dot. The QPC is used to measure fluctuations in the charge configuration of the dot. The dot, which is adjacent to an electron reservoir, is tuned in such a way that the chemical potential of the reservoir lies between the two qubit states, spin-up and spin-down. If the electron is in the ground state, $|\uparrow\rangle$, it cannot tunnel out of the dot. Since the charge occupation of the quantum dot remains constant, the QPC's sensor current, I_{sensor}, also remains unchanged. If the electron is in the excited state, $|\downarrow\rangle$, the electron can now tunnel out of the dot and into the reservoir. The sensor current will show a response to the change in charge occupation as there has been a change in the electrostatic environment. A new electron can tunnel into the dot and occupy the ground state, therefore returning the sensor current to normal. This method is destructive, as the qubit is lost when the electron tunnels into the reservior.

Another widely used method of spin state readout is Pauli spin blockade (PSB) [26]. This method is advantageous as the spin state is not lost to the leads, like in Elzerman's readout which destroys the spin state. Two electrons in a double quantum dot system will either form a singlet state or one of three triplet states which correspond to different values of spin component, m_s = -1, 0, +1. The transport of electrons from one dot to the next, becomes dependent on the spin state due to the Pauli exclusion principle. The transport can be completely blocked if the two electrons form a triplet state. If the spins form a singlet state, then transport is not forbidden, and the electrons can form a different charge configuration. The variation in charge configuration is typically detected by a nearby charge sensor device.

Finally, the last method of spin readout to be covered here will be SET reflectometry [10]. This method utilizes a SET placed nearby a quantum dot system. The SET is made to be part of an LC tank circuit connected via one of the accumulation gates. The SET is tuned to a Coulomb peak and behaves like a charge sensor. Charge transitions in the nearby quantum dots change the electrostatic environment and therefore the conductance through the SET. The response is observed by variations in the transmission coefficient through the tank circuit. SET reflectometry can reach higher fidelities than dc charge sensing, with integration times being on the order of 800 ns with $>$ 98% fidelity [10].

1.8 Silicon quantum dots

There are three standard materials when fabricating quantum dots: GaAs, Si/SiO_2 and Si/Ge. GaAs has been the workhorse in the field as a lot of early research occurred on GaAs

quantum dot devices. Their early success has come from the fact that they are larger (≈ 100 nm) and easier to fabricate. A drawback of using GaAs as a substrate is the materials large hyperfine interaction which drastically reduces the qubits coherence time ($T_2^* \sim 40$ ns) [3]. This can be avoided by moving to Si, and using ^{28}Si isotope which has zero spin component, significantly increasing coherence times ($T_2^* \sim 120$ us) [47]. As fabrication techniques have advanced, so have the sizes of silicon metal-oxide-semiconductor (SiMOS) quantum dots which, today, can be as small as 50 nm. The need for smaller dots in Si is dictated by the fact that electrons in Si have an effective mass ≈ 5 times larger than that of GaAs. The g-factor of electrons in silicon is also approximately 5 times larger than GaAs, allowing for smaller external magnetic fields for the same Zeeman energy. This also translates to having Rabi oscillations 5 times faster in Si, given the same strength of drive field. Additionally, the dependence of the g-factor on vertical electric field strength (known as the Stark shift) allows for more alternatives for large scale quantum computation, allowing for global magnetic fields and qubits to be brought on and off resonance by modulating the g-factor. Si/Ge devices, on the other hand, tend to be less noisy as the electrons are buried in a heterostructure. Despite this, Si/Ge is more expensive and it is difficult to obtain high quality heterostructure materials. The silicon is strained due to a lattice mismatched with germanium, making wafer development and fabrication more challenging. SiMOS devices (Fig. 1.5), however, are not perfect. Devices tend to posses significant amounts of noise as a result of charge traps at the Si/Oxide interface, due to the amorphous nature of the oxide. This can be corrected to an extent by forming gas anneals as seen in Chapter 3. Furthermore, an overlapping gate geometry can have nanoscopic 'pinholes' in the oxide between them, compromising the electric isolation between the two gates. Chapter 2 studies various oxides in depth to determine and optimize the level of electrical isolation. The work in this thesis is accomplished with only SiMOS devices in mind as they are comparatively easier to fabricate.

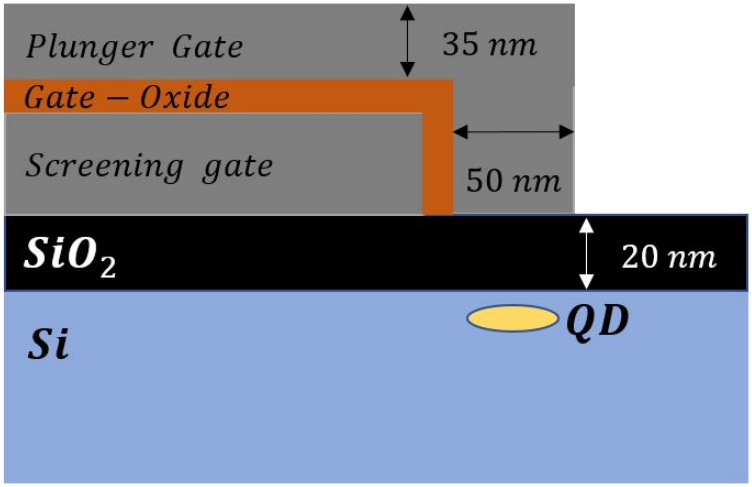


Figure 1.5: Side view schematic of an overlapping gate geometry quantum dot. The plunger gate defines the electrostatic confinement for the qubits. The gate-oxide ($\approx$ 10 nm thick) is an insulating layer between the plunger gate and screening gate. The screening gate ensures the quantum dot is generated only at the tip of the plunger gate and is also 35 nm in thickness. QD represents the quantum dot region in the silicon substrate.

Chapter 2

Gate-Oxide characterization

2.1 Motivation

Gate-based quantum dots are nanoscopic devices which rely on an overlapping metallic gate geometry for the confinement of individual electrons. Due to its high quality grown oxide, aluminum has been the workhorse in the field for the past 20 years. Aluminum oxide (depending on how it is grown/deposited) boasts a large band gap energy $E_g = 9.2$ eV and large dielectric constant K: approximately 9. The aluminum oxide between any two layers must be completely electrically isolating to avoid shorting to one another. Depending on the geometry of the quantum dot device, electrically short circuited gate layers can render the device useless as less control will be had in confinement of the electrons. In this chapter, oxide test structures are fabricated in order to test various oxide growth conditions between two layers of aluminum.

The oxide test structures must be as similar to the gate defined quantum dots as possible. In the quantum dot devices, the area of overlap between two aluminum layers can be as small as 360 nm^2. Therefore in order to obtain the most accurate results, the test structures overlap must be as small as possible. The test structures are fabricated to have an overlap area of approximately 5 $microns^2$. This is about as small of an overlap area that is possible due to the limitations of the Heidelberg MLA150 Maskless Aligner system (photolithography). Each test structure consists of 4 bond pads made of 20 nm and 80 nm of titanium and palladium, respectively. The oxide test structures are fabricated via a bilayer method which involves an initial layer of HMDS followed by a layer of S1811 and PMGI-SF7. They are then exposed via photolithography and subsequently developed in MF-319. An O_2 plasma descum is performed before 35 nm of aluminum is deposited

via the Angstrom Engineering E-beam deposition system. The first layer of aluminum is left in PG-remover overnight for lift-off. After lift-off, the first layer of aluminum has an oxide grown/deposited immediately. For the second layer, a slightly different process must be implemented as the photoresist developer MF-319 is known to etch aluminum and therefore aluminum oxide. First, a bilayer of MMA and S1811 is spun on the silicon pieces. The bilayer is then exposed via photolithography and developed in MF-319. The MMA provides a protective coating for the first aluminum layer and will not be etched away. Afterwards, the sample is hard baked to create a pseudo mask out of the developed S1811. The pieces are then flood exposed in the UV Ozone system for 20 minutes at room temperature. Following this, development in a solution of IPA and water (7:3 ratio) occurs before another O_2 plasma descum. Finally, the second 35 nm layer of aluminum is deposited. The final design can be seen in Fig. 2.1. The red colour are the bond pads and the blue and brown are the first and second layers of aluminum, respectively. Each silicon chip has 28 of these structures.

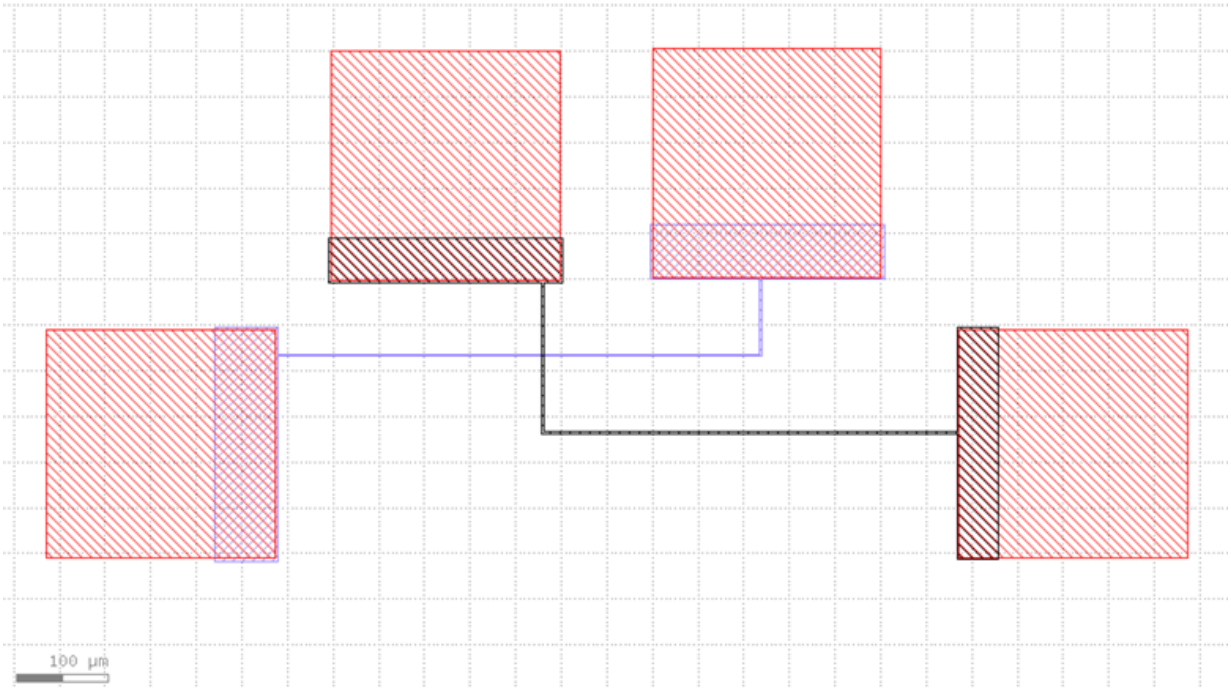


Figure 2.1: Klayout schematic of the oxide test structures. The red represents the bond pads for 2-point probe characterization, while the blue and brown represent the first and second layer of aluminum, respectively.

2.2 Results

Various methods of oxide growth are utilized in fabricating the test structures. A common oxide growth technique used to fabricate gate based silicon quantum dots is an Asher Oxide. The Asher oxidation has the advantage that the dielectric layer is grown directly on the aluminum layers, rather than depositing an insulating layer over the entire substrate. In this process, the sample is heated to 150C and exposed to an oxygen plasma. A thermal dry oxide is grown by simply applying heat to the aluminum at a high temperature to increase the rate of diffusion of oxygen. Each process is not perfect at growing an oxide and will have a given defect density. We attempt to 'fill-in' these defects by annealing the aluminum devices in O_2 at various temperatures and times.

After fabrication, each layer of aluminum is tested for continuity via 2-probe characterization. The probe tips are connected to opposite sides of the same aluminum layer and an electrical short is measured if the aluminum layer is continuous. If the layer is not continuous, a large resistance is measured. After each layer has been tested, each device is forming gas (FG) anneal at 300C for 10 minutes to see if the quality of the aluminum or aluminum/palladium interface decays. This is done to further simulate actual quantum dot devices. A list of tested oxides and their respective continuity is found in Table 2.1. The devices with FG anneals are indicated by a *. Results are presented as a ratio of devices being continuous out of all devices on the chip.

After the continuity test, there were clear outliers as to which process yielded better devices. Devices with the 400C O_2 anneal show no continuous first layers implying that the temperature was too high. Every other device showed a reasonable success rate when taking processing variability into account. Chips which have less than 28 devices had severe lift-off issues. This issue is expected to be fixed with a longer deep UV exposure time.

The oxide test structures are now tested for leakage voltage, V_{leak}, and breakdown voltage, $V_{breakdown}$. One probe tip is placed on one of the bond pads connected to the first aluminum layer and another probe tip is placed on a bond pad connected with the second aluminum layer. The only way that a current can successfully pass from one probe tip to another is by breaking down the grown oxide where the two layers overlap. This occurs when the voltage difference between two layer becomes larger than the dielectric strength of the oxide; this occurs at $V_{breakdown}$. Once the dielectric begins to leak, the leakage current increases exponentially until breakdown. A device is said to be 'leaking' when the leakage current, $I_{leakage}$ surpasses 0.3 nA. At this value, the leakage current can be distinguished from noise in the measurement set-up. Before the dielectric breakdown, the layers were first tested for electrical continuity. A list of tested oxides and their respective leakage

Test / **Oxide**	1^{st} layer continuity	2^{nd} layer continuity	1^{st} layer continuity*	2^{nd} layer continuity*
Asher Oxide	28/28	27/28	27/28	25/28
2 x Asher Oxide	27/28	25/28	27/28	25/28
Hotplate (200C, 5 minutes) Oxide	28/28	28/28	28/28	28/28
Asher Oxide + O_2 anneal (150C, 2 minutes)	28/28	28/28	28/28	28/28
Asher Oxide + O_2 anneal (250C, 2 minutes)	27/28	12/12	27/28	12/12
Asher Oxide + O_2 anneal (350C, 2 minutes)	28/28	1/1	27/28	1/1
Asher Oxide + 4 nm ALD Al_2O_3	27/28	20/25	27/28	20/25
Hotplate (200C, 5 minutes) Oxide + 4 nm ALD Al_2O_3	28/28	18/18	28/28	18/18
Asher Oxide + O_2 anneal (150C, 30 minutes)	24/28	18/18	24/28	18/18
Asher Oxide + O_2 anneal (250C, 30 minutes)	28/28	26/28	28/28	26/28
Asher Oxide + 4 nm ALD Al_2O_3 + O_2 anneal (400C, 30 minutes)	0/28	28/28	0/28	28/28
Hotplate (200C, 5 minutes) Oxide + 4 nm ALD Al_2O_3 + O_2 anneal (400C, 30 minutes)	0/28	28/28	0/28	28/28

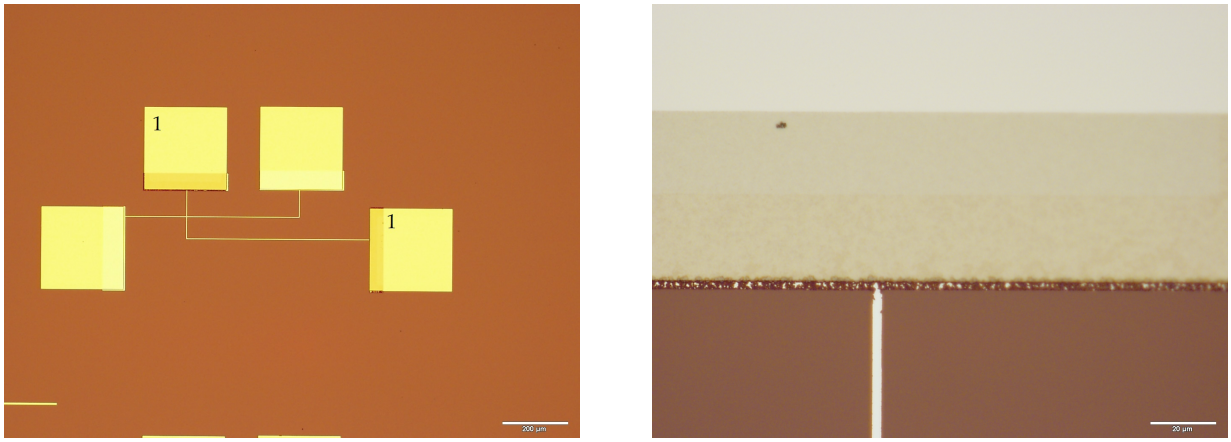
Table 2.1: The ratio of electrically continuous devices to total devices is reported. A forming gas anneal at 300C for 10 minutes is implemented to observe its effects (denoted by *). A 400C anneal appears to be too high in temperature for the test structures.

voltage, V_{leak}, and breakdown voltage, $V_{breakdown}$, is found in Table 2.2. Once each device has been measured, a forming gas anneal is employed.

Test / **Oxide**	Avg. V_{leak} [V]	Avg. $V_{breakdown}$ [V]	Avg. V_{leak}* [V]	Avg $V_{breakdown}$* [V]
Asher Oxide	2.32 ± 0.03	3.15 ± 0.09	2.05 ± 0.07	3.38 ± 0.10
2 x Asher Oxide	2.37 ± 0.05	3.12 ± 0.09	1.80 ± 0.40	2.55 ± 0.95
Hotplate (200C, 5 minutes) Oxide	1.97 ± 0.05	3.0 ± 0.1	1.66 ± 0.05	3.53 ± 0.22
Asher Oxide + O_2 anneal (150C, 2 minutes)	2.25 ± 0.04	3.10 ± 0.03	1.94 ± 0.03	3.32 ± 0.06
Asher Oxide + O_2 anneal (250C, 2 minutes)	2.48 ± 0.22	3.10 ± 0.08	2.03 ± 0.08	3.37 ± 0.03
Asher Oxide + O_2 anneal (350C, 2 minutes)	2.41	3.09	Unknown	Unknown
Asher Oxide + 4 nm ALD Al_2O_3	5.25 ± 0.70	5.52 ± 0.33	4.50 ± 0.30	5.61 ± 0.23
Hotplate (200C, 5 minutes) Oxide + 4 nm ALD Al_2O_3	3.78 ± 0.41	4.92 ± 0.27	3.82 ± 0.34	5.46 ± 0.21
Asher Oxide + O_2 anneal (150C, 30 minutes)	2.25 ± 0.18	3.07 ± 0.21	2.20 ± 0.12	3.49 ± 0.14
Asher Oxide + O_2 anneal (250C, 30 minutes)	2.20 ± 0.11	3.19 ± 0.10	2.13 ± 0.13	3.43 ± 0.18
Asher Oxide + 4 nm ALD Al_2O_3 + O_2 anneal (400C, 30 minutes)	Unknown	Unknown	Unknown	Unknown
Hotplate (200C, 5 minutes) Oxide + 4 nm ALD Al_2O_3 + O_2 anneal (400C, 30 minutes)	Unknown	Unknown	Unknown	Unknown

Table 2.2: The average leakage voltage and average breakdown voltage is shown for various gate oxides with and without a forming gas anneal at 300C for 10 minutes (denoted by *). It can be seen that the forming anneal improves the breakdown voltage but decreases the leakage voltage.

Following the voltage breakdown test, several interesting results appeared. First, the forming gas anneal resulted in a lower average leakage voltage and a higher average breakdown voltage amongst the oxides. The second important result is the improvement 4 nm of ALD Al_2O_3 yields.For the Asher oxide and hotplate oxide, the additional ALD almost



(a) (b)

Figure 2.2: Images of an oxide test structure where the first layer has been exposed to 400C O_2 anneal. (a) an overview is showing the first layer (labelled '1') with a dark outline. (b) a zoomed image of the dark outline surrounding the Ti/Pd bond pad.

doubles the average leakage voltages. The ALD likely is filling-in many of the defects developed in the previous oxide growth providing better results.

Previous results indicate that an O_2 anneal at 400C is too high in temperature. The test structures labelled 'Asher Oxide', '2 x Asher Oxide', 'Hotplate (200C, 5 minutes) Oxide', 'Asher Oxide + O_2 anneal (150C, 2 minutes)' and Asher Oxide + O_2 anneal (150C, 2 minutes)' undergo a forming gas anneal at 400C for 10 minutes in order to determine whether the temperature or the gas used is causing the structures to be discontinuous. It was found that all 5 of the above oxides had 100 % of the first and second layer electrically discontinuous. This shows that the temperature is too high for these structures. Imaging the aluminum layers post FG anneal shows small cracks (Fig. 2.2).

It is hypothesized that the dark outline is an oxide formed by the reaction between the aluminum and the palladium, similar to the reaction between aluminum and gold. Improvements (Fig. 2.3) were made to the original test structures to be able to withstand a 400C anneal, namely the aluminum layers overlapped the bond pads significantly more in order to increase the area for current to pass through. Furthermore, smaller probe pads were added in the 'arms' of the aluminum layer as nanoscopic cracks in the aluminum were also suspected to be the issue. These probe pads allow for us to determine where the nanoscopic cracks exist. This issue was also present in our quantum dot processing.

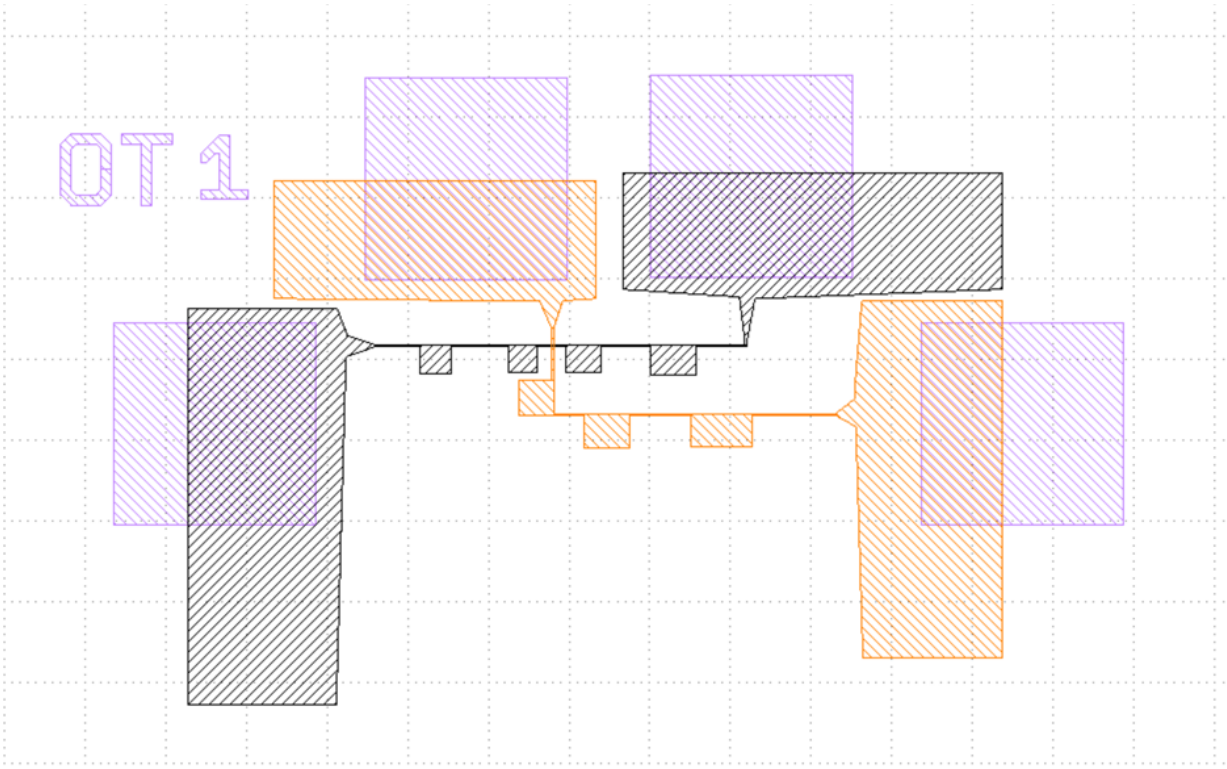


Figure 2.3: Klayout schematic of the oxide test structures. Purple is the Ti/Pd bond pad, orange is the first aluminum layer and black is the second aluminum layer. The design features large aluminum/Pd over laps and small probe pads.

With the new pattern, more test structures were fabricated and exposed to a 400C forming gas anneal for 10 minutes. Test structures featured an Asher oxide, a 2 x Asher oxide and a hotplate (200C, 5 minutes) oxide. With each chip having 28 of these patterns, each layer was tested for continuity and it was found that both the first and second layer were continuous on all devices on each chip: a 100% yield.

Aluminum has been used as a metallic gate in quantum dots for many years due to it's ability to grow a high quality oxide with a large dielectric constant. More recently, palladium has been used with great success [4]. Palladium offers a smaller grain size which allows for smaller quantum dot regions to be formed. Furthermore, aluminum and silicon posses wildly different thermal expansion coefficients, which can lead to mechanical stress leading to variations in electrochemical potential [43]. Aluminum oxide is subsequently deposited via ALD on the palladium to form a dielectric between layers. A down side

Test / Oxide	1^{st} layer continuity	2^{nd} layer continuity	1^{st} layer continuity*	2^{nd} layer continuity*
7 nm ALD Al_2O_3	28/28	28/28	28/28	28/28
10 nm ALD Al_2O_3	28/28	28/28	28/28	28/28
13 nm ALD Al_2O_3	28/28	28/28	28/28	28/28
10 nm ALD Al_2O_3 + O_2 anneal (400C, 30 minutes)	28/28	28/28	28/28	28/28

Table 2.3: Test structures fabricated with Pd gates and ALD Al_2O_3. The ratio of electrically continuous devices to total devices is reported. A forming gas anneal at 400C for 10 minutes is implemented to observe it's effects (denoted by *). There is no change in continuity with after performing a FG anneal at 400C.

to palladium is that the ALD aluminum oxide is deposited across the wafer resulting in necessary buffered-oxide-etching and additional processing.

Test structures with their first and second layer are fabricated with 5 nm of titanium and 25 nm of palladium. The titanium behaves as an adhesive layer to the SiO_2 to ensure that delamination of palladium does not occur. Three thicknesses of ALD Al_2O_3 are tested: 7 nm, 10 nm and 13 nm. An additional device was fabricated with 10 nm of ALD Al_2O_3 and an O_2 anneal at 400C for 30 minutes. The devices are again tested for their continuity and for their V_{leak} and $V_{breakdown}$. Following these tests, a FG anneal at 400C is implemented. The results of these tests are seen in Table 2.3 and Table 2.4. The continuity test resulted in each layer on each device being 100% continuous: a slight improvement over the aluminum gate. The voltage breakdown test yielded more improved results over aluminum. The ideal thickness for the ALD Al_2O_3 is thought to be 10 nm, as it is not too thin where it would break down too early but also not too thick, resulting in a smaller lever arm (the value which converts the top gate voltage to the change in the electrochemical potential of a quantum dot). Comparing with the 'best' device with aluminum gates, the device with an oxide comprised of Asher oxide + 4 nm ALD Al_2O_3 has similar breakdown voltages, just with less variation. This is evidence of palladium's high reproducibility and low variation. Finally, the average leakage and average breakdown for the different Al_2O_3 thicknesses is shown in Fig. 2.4. The average leakage and average breakdown appear to be nearly linear in relation, however, more tests are needed to confirm this.

Test / Oxide	Avg. V_{leak} [V]	Avg. $V_{breakdown}$ [V]	Avg. V_{leak}* [V]	Avg $V_{breakdown}$* [V]
7 nm ALD Al_2O_3	2.52 ± 0.63	3.30 ± 0.70	2.65 ± 0.72	3.29 ± 0.82
10 nm ALD Al_2O_3	5.85 ± 0.25	6.70 ± 0.20	6.16 ± 0.20	6.84 ± 0.19
13 nm ALD Al_2O_3	8.71 ± 0.27	9.25 ± 0.15	8.95 ± 0.35	9.32 ± 0.41
10 nm ALD Al_2O_3 + O_2 anneal (400C, 30 minutes)	4.93 ± 0.47	6.48 ± 0.34	5.12 ± 0.39	6.59 ± 0.41

Table 2.4: Test structures fabricated with Pd gates and ALD Al_2O_3. The average leakage voltage and average breakdown voltage is shown with and without a FG anneal at 400C for 10 minutes (denoted by *). Only the device with 10 nm of aluminum oxide shows a clear improvement post FG anneal.

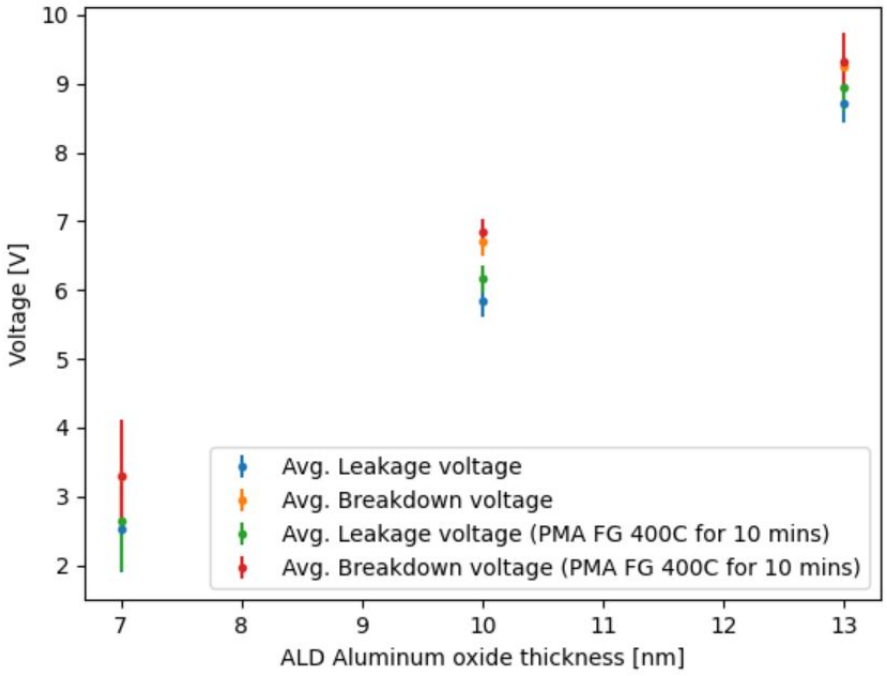


Figure 2.4: Plot of the voltage difference between two Pd layers as a function of ALD Al_2O_3 thickness.

2.3 Conclusions

In summary, with aluminum gates, the Asher oxide, which was standard in the fabrication process of our quantum dots, presents a low leakage voltage. Leakage between overlapping layers compromises the spatial confinement of the electron. This process does not generate a high quality oxide. Utilizing either an Asher oxide or a hotplate oxide, in combination with a thin film such as ALD Al_2O_3, increases the average leakage voltage, average breakdown voltage and therefore the quality of oxide. Performing a high temperature anneal of the test structures provided insight to how the leakage and breakdown voltages changed in a thermal cycle. It was found that for every oxide, the average leakage voltage decreased while the average breakdown voltage increased slightly. Despite this, a hotplate oxide with 4nm of ALD Al_2O_3 should provide a sufficient level of isolation between plunger and screening gate in a quantum dot device. Palladium gates were also studied with a high quality Al_2O_3 film. Test structures with 10 nm of Al_2O_3 showed promising results and could be used as an alternative instead of aluminum gates. This thickness was not too thin to allow leakage and not too thick to significantly decrease the lever arm of the gate. Contrasting the aluminum layers, both the average leakage voltage and breakdown voltage increased following a forming gas anneal.

Chapter 3

CV measurements/Charge noise characterization

In this chapter, we characterize various oxides and the semiconductor-insulator interface for density of interface traps. First, we will discuss the theoretical background needed of a metal-oxide-semiconductor capacitor (MOSCAP) and then CV (capacitance/voltage) measurements. A well characterized density of interface traps is essential for improving silicon quantum dots as, charge traps can directly interfere with many aspects of quantum dot spin qubits, namely the detuning potential, g-factor, coherence times and two-qubit fidelity.

The MOSCAP consists of 3 distinct layers: a conductive metal layer, an insulating oxide layer and a semiconductor layer (Fig. 3.5). As it is a significant component of most electronic devices, the MOSCAP has been studied for the past 50 years and because of this, the conventional semiconductor utilized in their fabrication is silicon. It follows that SiO_2 is typically utilized as the oxide layer as it is readily formed on silicon surfaces. More recently, the electronics industry has seen a transition to other insulating materials such as hafnium oxide (HfO_2) and aluminum oxide (Al_2O_3) due to their high dielectric constants.

3.1 The MOS capacitor

As previously mentioned, the MOS capacitor consists of three layers. The metallic top layer gate is separated from the doped silicon substrate by a thin oxide layer. The MOS capacitor behaves similarly to the parallel plate capacitor in the sense that there are two

terminals: the metallic top gate and the back side of the silicon substrate. Moreover, the oxide layer must provide electrical isolation between the metallic gate and the silicon substrate. The workings of the MOS capacitor are best understood using the band theory of solids, whereby the overlap of electronic orbitals in crystal structures results in allowed and forbidden energy bands: the electronic band structure. The most important features of a material's band structure are the band gap energy E_g, the conduction band, and the valence band. The band gap energy is a range of energy where electronic states are forbidden. It is also the minimum energy necessary to promote an electron from a state in the valence band to the conduction band. The valence band is the set of electron orbitals which are tightly bond around atoms within the crystal. Finally, the conduction band is the set of orbitals where electrons can move freely within the crystalline structure and can be used for electrical conduction in the material.

The MOS capacitor utilizes three materials which each have differing electrical properties and thus, differing electronic band structures. The first layer, the metallic gate, is a metal. Materials which are metals have no band gap, meaning electrons can move almost freely between a valence state and conduction state. Next, the oxide layer responsible for electrical isolation between top gate and substrate, is an insulator. Insulators are poor electrical conductors and thus have large band gap energies. For example, SiO_2 has a band gap energy of around 9 eV. Finally, the silicon substrate is a semiconductor. Semiconductors are better electrical conductors than insulators but worse than metals. There are two types of semiconductors: intrinsic and extrinsic. Previously described is an intrinsic semiconductor, and for silicon, the band gap energy is approximately 1.2 eV. An extrinsic semiconductor is a semiconductor whose electrical properties have been modified with the addition of impurity donors or acceptor atoms, making them n-type or p-type, respectively. To n-type dope silicon, an atom from Group V of the periodic table is introduced. A Group V dopant has 5 valence electrons whereas silicon only has 4. Similarly, to p-type dope silicon, an atom from Group III is introduced. Elements from Group III will have only 3 valence electrons. In the n-type silicon, electrons are the majority charge carriers as an extra one is introduced, while holes (the absence of electrons) are the minority charge carriers. It is the opposite in p-type silicon; holes are now the majority charge carriers and electrons are the minority carriers. With respect to the band structure of the semiconductor, the Fermi energy E_f is shifted depending on the type of dopant. N-type silicon will have a Fermi energy which is near the conduction band edge (with respect to the intrinsic silicon's E_f), increasing the likelihood of electrons being in states within the conduction band. The p-type dopant in silicon results in a higher likelihood of holes in the valence band which lowers the Fermi energy to near the valence band edge.

Band diagrams are a useful way of understanding how MOS capacitors function. The

electron energy levels are plotted against the vertical position of each material. When different materials are combined with one another, their energy bands will affect each other. This is the result of charge imbalances at the interfaces and depends on the Fermi energy of the materials forming the interfaces. When a voltage, V_g, is applied to the metal top gate, the Fermi energy can then be modulated resulting in varying degrees of band bending. The differences in band bending results in the different operational modes of the MOS capacitor: accumulation, depletion and inversion. Depending on whether the semiconductor is p-type or n-type, the modes of operation change slightly. The MOSCAPs investigated in this thesis involve p-type silicon, but the characterization of the oxide interface traps will also apply to the undoped or low-doped silicon used for qubit devices.

3.1.1 Flat band voltage

Before going into detail about the modes of operation where the bands are bending, we must first describe the case where there is no charge imbalance at the interface. When there is no charge imbalance at the interface, the Fermi energy of the metal and semiconductor are aligned and the bands remain flat, resulting in no charge accumulation (Fig. 3.1). This occurs at the flat band voltage V_{FB}, which for a MOS capacitor comprised of aluminum and silicon, is approximately $V_{FB} = -0.8V$ [31]. It should be noted that the bands can bend while the Fermi energy of the metal and the Fermi energy of the semiconductor are aligned.

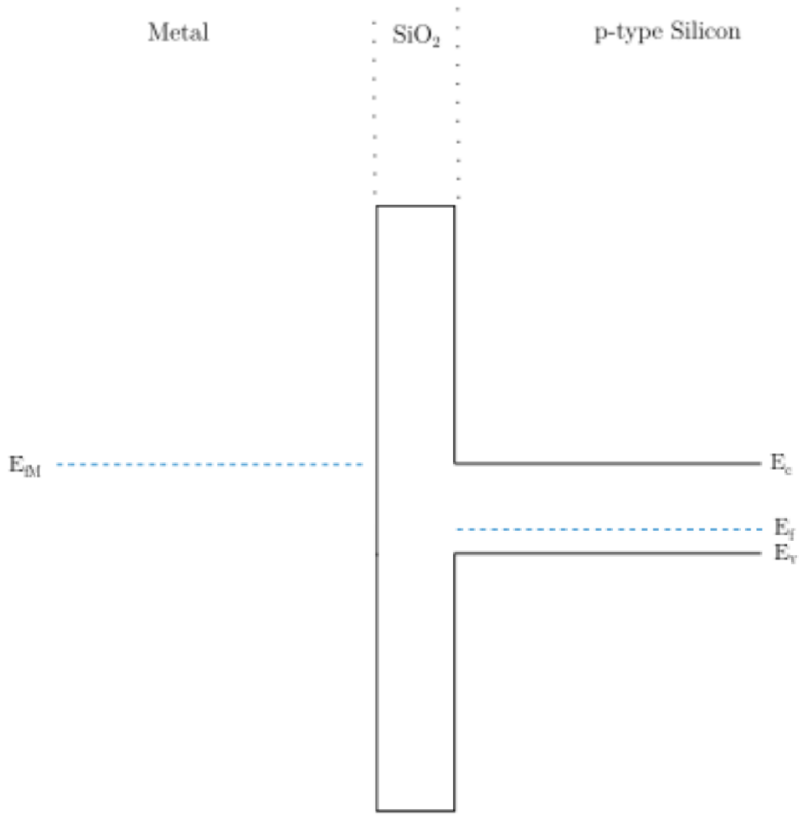


Figure 3.1: Energy band diagram for a MOS capacitor at the flat band voltage with a top gate voltage of V_g = -0.8V. The top band labelled E_c is the bottom of the conduction band. The bottom band labelled E_v is the top of the valence band, E_f is the Fermi energy in the silicon and E_{fM} is the Fermi energy in the metal. When E_{fM} is at this configuration, the bands in the semiconductor remain flat.

3.1.2 Accumulation

When the p-type MOS capacitor is in accumulation mode, the applied V_g is more negative than the flat band voltage. This results in holes gathering at the SiO_2/Oxide interface. The negative V_g causes the top gates Fermi level to increase. The larger relative Fermi energy of the metal causes the silicon's bands to bend upwards. Moreover, the electric field

within the SiO_2 is directed from the silicon substrate to the top gate, yielding an upward slope in the oxides band diagram as seen in Fig. 3.2.

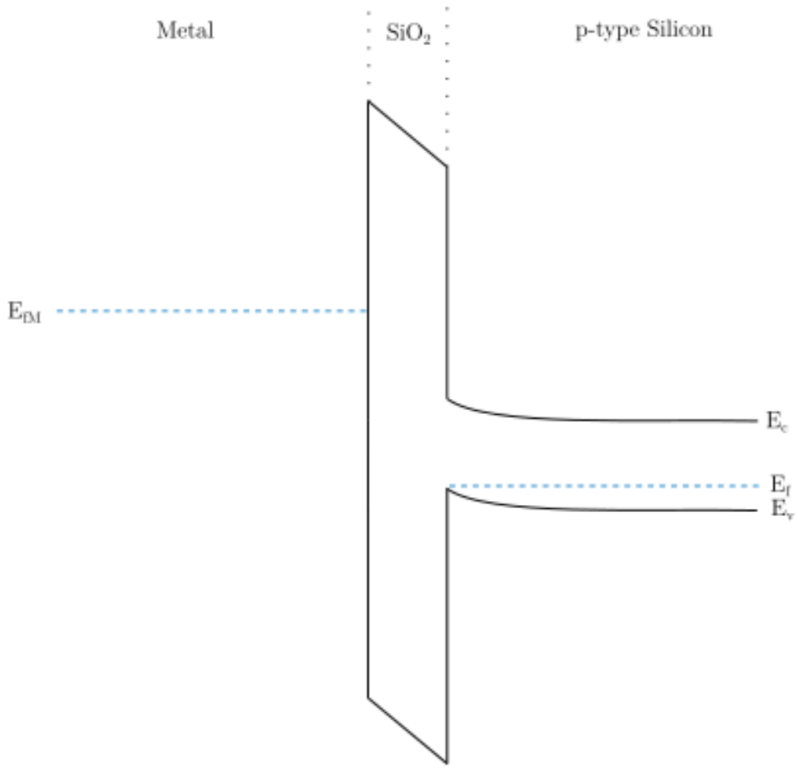


Figure 3.2: Energy band diagram for a MOS capacitor in the accumulation mode. The more negative V_g increases the Fermi energy of the metal which in turn bends the bands of both the oxide and the silicon substrate upward.

3.1.3 Depletion

When the p-type MOS capacitor is in depletion mode, the applied V_g is slightly more positive than the flat band voltage. The positive top gate voltage causes the metal's Fermi energy to decrease, so the smaller relative Fermi energy of the metal causes the silicon's bands to bend downwards and a region with no holes is formed: the depletion region. The width of the depletion layer will increase to balance the positive charge added to the top

gate. At the SiO_2/Si interface, the silicon's Fermi energy is further away from the valence band indicating that there is no longer a collection of mobile holes there. The electric field within the SiO_2 is directed from the top gate to the substrate, resulting in a downward slope in the oxides band diagrams as seen in Fig. 3.3.

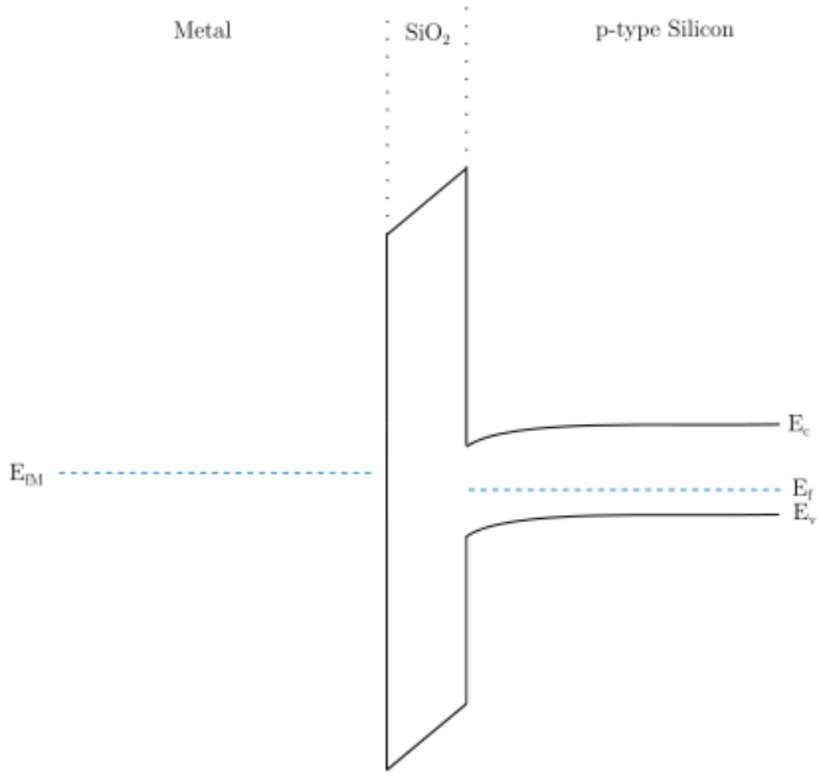


Figure 3.3: Energy band diagram for a MOS capacitor in the depletion mode. Here, V_g is becoming more positive. The Fermi energy of the metal decreases causing the bands of both the oxide and the silicon substrate downwards.

3.1.4 Inversion

If we push the top gate voltage to be even more positive, past depletion, the MOS capacitor will change modes from depletion to inversion. This occurs at a threshold voltage, V_{Th}. In inversion, the silicon bands bend so much that the conduction band is near or below the

Fermi energy (Fig. 3.4). Here, a thin layer of minority carriers (electrons) collect at the oxide/semiconductor interface.

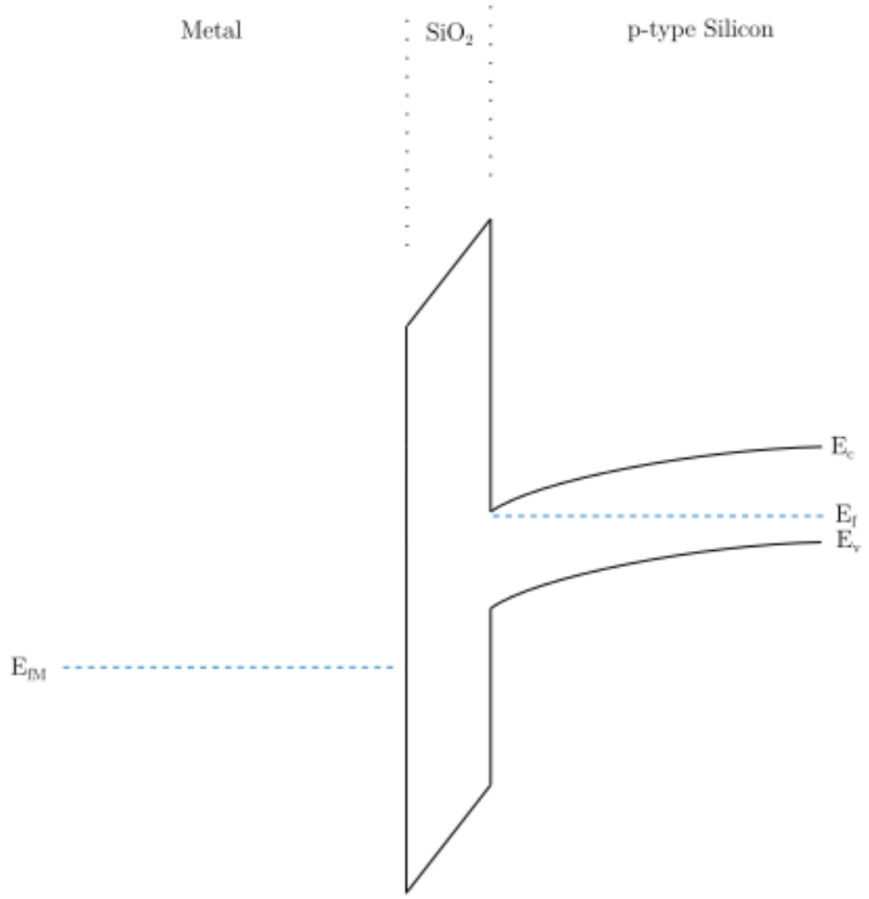


Figure 3.4: Energy band diagram for a MOS capacitor in inversion mode. Here, V_g becomes increasingly positive. The Fermi energy of the metal decreases causing the bands of both the oxide and the silicon substrate to bend downwards. The bands have bent so much now that E_c is near E_f

3.1.5 MOS capacitor characteristics

For a better understanding of the 3 operational modes of the MOS capacitor, it is useful to think about the capacitance as a function of the applied top gate voltage. These

measurements are often referred to as CV curves or measurements. For these measurements, the DC top gate voltage is modulated with a small AC signal which, depending on the frequency, will drastically effect the measured capacitance because different charge carriers react differently with the oscillating signal. When the p-type MOS capacitor is in the accumulation mode, a large density of majority carriers (holes) is present at the Si/Oxide interface as seen in Fig. 3.5. Any negative charge added or subtracted to the gate is balanced by the charges in the accumulation layer. Therefore, the accumulation mode capacitance will always be equal to the oxide capacitance, C_{OX}. As the top gate voltage becomes more positive, the device moves into the depletion mode and the large accumulation layer decreases as the majority carriers move away from the interface. As a result of this charge movement, the measured capacitance decreases (Fig. 3.6). Further increasing the top gate voltage, the device moves to the inversion mode (Fig. 3.4). Here, the frequency of the applied signal plays a significant role. At low frequencies, 0.1 KHz or less, the capacitance increases back to the oxide capacitance because any additional positive charges added or subtracted to the top gate is balanced by negative charges added to the inversion layer. At high frequencies (1MHz), the capacitance remains low in inversion. This is due to the generation-recombination process not being able to supply or eliminate the minority carriers in response to the AC signal; therefore the capacitance remains low.

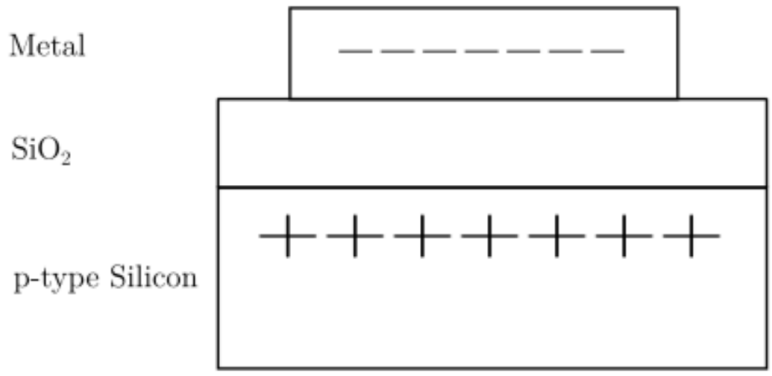


Figure 3.5: Cross section of MOS capacitor in accumulation mode. In accumulation, the top gate voltage is negative which generates a large density of majority carriers (holes) at the SiO_2/Silicon interface.

The capacitance measured in accumulation does not depend on the frequency of the

AC signal. Therefore,

$$C_{HF} = C_{LF} = C_{OX} \tag{3.1}$$

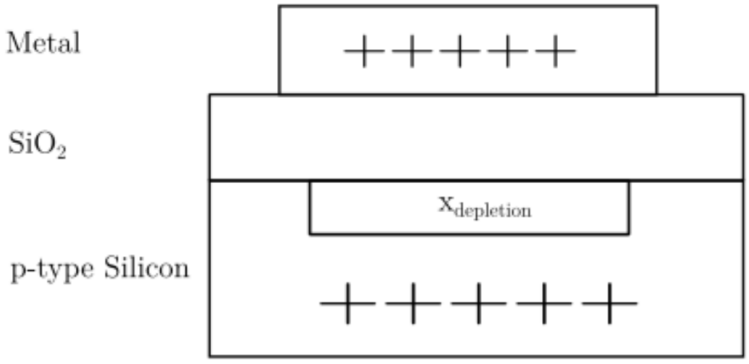


Figure 3.6: Cross section of MOS capacitor in depletion mode. In depletion, the top gate voltage becomes positive and the density of majority carriers decreases at the interface. A small depletion region (x_d) now appears.

The depletion mode capacitance is simply the oxide capacitance and depletion region capacitance (C_d). They are added in series to obtain:

$$\frac{1}{C} = \frac{1}{C_{OX}} + \frac{1}{C_d} \tag{3.2}$$

$$C_{HF} = C_{LF} = \frac{1}{\frac{1}{C_{OX}} + \frac{x_d}{\epsilon_s}}, \tag{3.3}$$

where x_d is the thickness of the depletion region and ϵ_s is the dielectric permittivity of silicon (1.04e-12 Fcm^{-1}).

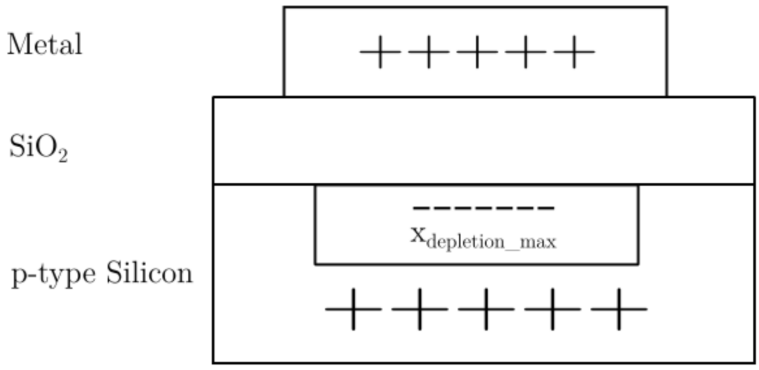


Figure 3.7: Energy band diagram for a MOS capacitor in the inversion mode. Here, V_g becomes increasingly positive and so the Fermi energy of the metal decreases causing the bands of both the oxide and the silicon substrate downwards.

The frequency plays a significant role in the inversion mode. The capacitances in inversion are:

$$C_{LF} = C_{OX} \tag{3.4}$$

$$C_{HF} = \frac{1}{\frac{1}{C_{OX}} + \frac{x_{d-max}}{\epsilon_s}}, \tag{3.5}$$

where, x_{d-max} is the maximal thickness of the depletion region. Majority carrier cannot decrease any more and now minority carrier (electrons) begin to contribute to the capacitance.

3.1.6 MOS capacitor defects

The MOS capacitor is frequently used to characterize the electrical quality of dielectrics. There are four distinct types of defects found in the MOS capacitor which reduces its quality: trapped oxide charges, fixed oxide charges, mobile ions, and interface traps (Fig. 3.8). First, the trapped oxide charges are either holes or electrons within the oxide, often created by ionizing radiation. Fixed oxide charges are found near the Si/Oxide interface and typically originate if the substrate underwent a dry oxidation process. Traces of water

during the oxidation process can be absorbed into the oxide, and can form a positive fixed charge known as hydronium (H_3O+). Next, mobile ions which are positively charged, can move freely throughout the oxide under the presence of an electric field [14]. Mobile ions are often the result of using processing tools which are contaminated with alkali metals such as lithium, potassium and sodium. Finally, interface traps, also known as charge traps, appear where the amorphous structure of the oxide meets the crystal structure of Si. At the interface, a mismatch of the atomic structure can cause electron orbitals to remain unbound and results in dangling bonds. In silicon quantum dots, unbound electrons will interact with the qubits resulting in unwanted charge noise.

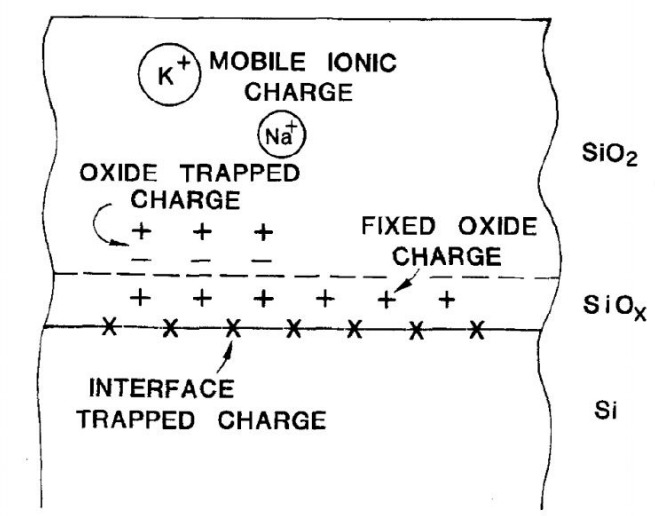


Figure 3.8: Schematic of the four types of defects in a SiO_2/Silicon stack: trapped oxide charges, fixed oxide traps, mobile ionic charges and interface charge traps. (from B.E. Deal, "Standardized Terminology for Oxide Charges Associated with Thermally Oxidized Silicon," J. Electrochem. Soc. Vol 127, No. 4 (April 1980) pp. 979-981)

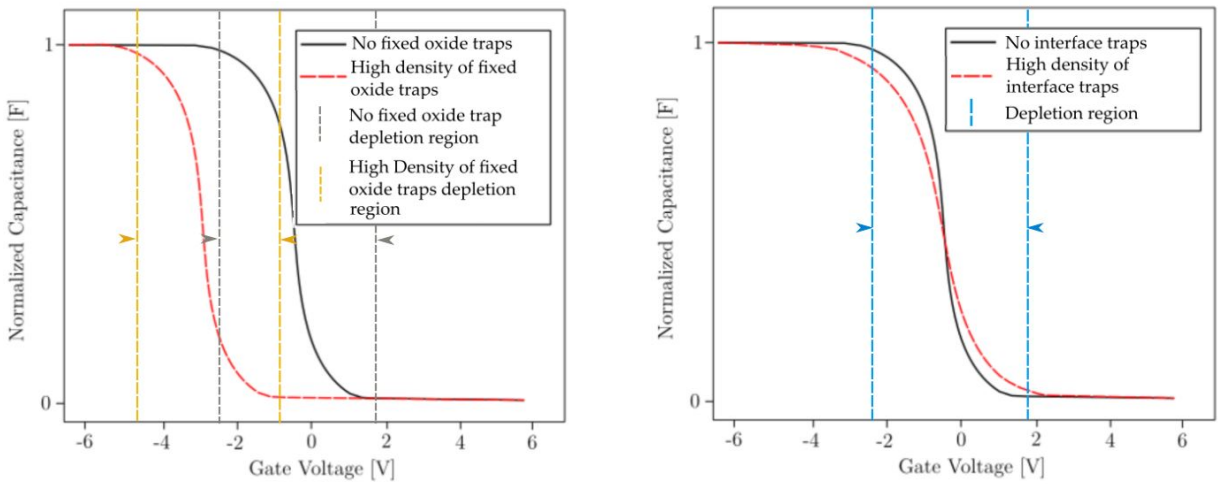
3.1.7 Fixed oxide traps

Fixed oxide traps typically occur when traces of water appear in the oxidation process. The water forms a positively charged fixed oxide trap called hydronium (H3O+) which will shift the CV curve to the left slightly (Fig. 3.9a). The positive charges act as an additional

gate voltage which will need to be cancelled out with the applied gate voltage [14].

3.1.8 Interface traps

The interface traps are surface states and therefore manifest within the bandgap of the semiconductor. It is important to note that the charge trap polarity can be either positive, negative or neutral, meaning that holes, electrons or both can be trapped. The positive charge traps are situated in the bottom half of the band gap and are considered “acceptor-like traps" and the negative charge traps, situated in the top half of the band gap and are considered “donor-like traps" [41]. To better understand how the charge traps affect the CV measurement, we must understand how these charge traps are filled when the Fermi energy of the metal varies. At top gate voltages more negative than the flat band voltage, the MOS capacitor is in accumulation mode: the semiconductor bands are bending upward. In this state, the donor-like traps above the semiconductors Fermi energy are empty and neutrally charged while acceptor-like state, also above the semiconductors Fermi energy, are also empty and therefore positively charged. This additional positive charge reduces the total charge of the accumulation layer and appears to shift the CV curve left slightly (Fig. 3.9b). Next, at the flat band energy, the donor-like states are empty as they lay above the Fermi energy and are neutrally charged while the acceptor-like states are filled below the Fermi energy and thus neutral, meaning near this top gate voltage, the CV measurement looks ideal. Finally, in inversion the bands are bending downwards. Therefore, the acceptor-like states are neutral because they are below the semiconductors Fermi energy and filled and the donor-like states are also below the semiconductors Fermi energy and filled, leaving an overall negative charge. An overview of the band bending and charge trap occupation is seen in Fig 3.10. This additional negative charge appears to shift the CV curve right slightly (Fig. 3.9b).



(a) (b)

Figure 3.9: Comparison of high frequency CV measurements with and without (a) fixed oxide traps and (b) interface traps. Additionally, the depletion region for each CV curve is indicated. Devices with different flat band voltages will undergo depletion in a different voltage range.

3.1.9 Capacitance-Voltage measurements

All of the CV measurements were performed on an Everbeing C-8 Probe Station. The probe station is completely surrounded by a Faraday cage to minimize electromagnetic noise. The MOS capacitor characterization was accomplished using the Keithley 4200A-SCS Parameter Analyzer which facilitates the CV measurements by measuring the conductance and capacitance of the device. The high frequency measurements were performed using a swept DC voltage and a small AC voltage at 1MHz, unless otherwise stated, to observe the response of the interface traps. In the measurement set-up, series resistances can generate due to the probes contact with the top gate and the silicon back contact so it can be necessary to compensate for them [14]. The corrected capacitance and conductance are given from the following equations:

$$C_{corr} = \frac{(G^2 + (2\pi f C)^2)C}{(a_r^2 + (2\pi f C)^2)} \tag{3.6}$$

(a) (b)

Figure 3.10: The band gap of silicon in (a) accumulation and (b) inversion. In accumulation the bands bend upward and the occupancy of the acceptor-like traps and donor-like traps are filled and empty, respectively. The filled acceptor-like traps are positively charge while the empty donor-like traps are neutrally charge. In inversion, the bands bend downwards and the occupancy of the acceptor-like traps and donor-like traps are empty and filled, respectively. The filled states yield a net negative charge while the empty states are neutral. Note that in (a) and (b) the Fermi energy E_f does not change value when the top gate voltage is modulated from accumulation to inversion but rather only the bands bend.

$$G_{corr} = \frac{(G^2 + (2\pi fC)^2)a_r}{(a_r^2 + (2\pi fC)^2)} \tag{3.7}$$

with,

$$a_r = G - (G^2 + (2\pi fC)^2)R_s \tag{3.8}$$

$$R_s = \frac{G_{acc}}{G_{acc}^2 + \omega C_{acc}^2} \tag{3.9}$$

where G is the measured conductance, C is the measured capacitance, ω is the angular frequency G_{acc} is the conductance value when the device under test (DUT) is in strong accumulation and C_{acc} is the capacitance value when the DUT is in strong accumulation. After the series resistance correction, the oxide capacitance value can be determined in order to extract the dielectric constant of the oxide, which is calculated from:

$$\epsilon_r = \frac{C_{OX} t_{OX}}{A\epsilon_o} \tag{3.10}$$

where, t_{OX} is the thickness of the deposited oxide (in cm), A is the area of the top gate (in cm^2), and ϵ_o is the vacuum permittivity (8.854e-12 F*cm^-1).

3.1.10 Low frequency measurements

The low frequency measurements are performed in a similar manner albeit at a low frequency (less than 0.1KHz). The top gate voltage is now essentially DC which, in inversion, allows for the slow minority carriers to contribute to the capacitance. The minority carrier generation-recombination time is much longer than the majority carriers. The low frequency measurements are also necessary to see the effects of interface traps to be observed, as their response time is also long. The low frequency, or quasi-static measurement is completed by slowly sweeping the DC voltage and measuring the current across the MOS capacitor using source-measure units (SMUs). Therefore, the capacitance can be determined by the following expressions:

$$C = \frac{dQ}{dV} \tag{3.11}$$

using,

$$I = \frac{dQ}{dt} \tag{3.12}$$

we observe that,

$$C = \frac{I}{\frac{dV}{dt}} \tag{3.13}$$

where Q is the charge of the capacitor in coulombs, I is the current across the MOS capacitor in amperes, V is the top gate voltage V_g and finally, t is the time in seconds.

3.1.11 Density of interface traps calculation

The measurement of interface density, D_{it}, is particularly useful as a qualitative measure of the quality of the Si/Oxide interface. The technique to determine D_{it}, was accomplished by Castagne and Vapaille and involves combining both the high and low frequency measurements [6]. In the high frequency measurement, the generation-recombination time of the charge traps is long enough that their capacitance contribution is absent. However, at low frequencies they do contribute to the capacitance. The difference between the low frequency and high frequency CV measurements in depletion allows us to determine the capacitance of the interface traps:

$$C_{it} = C_{LF} - C_{HF} \tag{3.14}$$

where,

$$C_{LF} = (\frac{1}{C_{LFm}} - \frac{1}{C_{OX}})^{-1} \tag{3.15}$$

and,

$$C_{HF} = (\frac{1}{C_{HFm}} - \frac{1}{C_{OX}})^{-1} \tag{3.16}$$

which leads to,

$$D_{it} = \frac{C_{it}}{qA} \tag{3.17}$$

Above, C_{LFm} and C_{HFm} are the capacitances obtained by measuring at a low frequency and a high frequency, respectively, q is the charge of the electron (1.6e-19 C) and A is the area of the capacitor in cm^2. The interface trap density is typically reported as $eV^{-1}cm^{-2}$. It should also be noted that this analytical method only gives accurate information when $C_{OX} > C_{LF}$ and when $C_{LF} > C_{HF}$. In other words, when the MOS capacitor is in deep accumulation or deep inversion, equations 3.15 and 3.16 approach infinite which is not

a physical value. Therefore, these region are ultra sensitive to changes in the sample capacitance and will appear to be noisy.

3.1.12 Fabrication of MOS capacitors

The MOS capacitors were fabricated on boron doped p-type silicon. The wafers were 4 inches in diameter, $\langle 100 \rangle$ oriented and grown using the CZ method. The electrical resistivity was reported to be 10-20 Ohm*cm (unless otherwise stated). Small 1cm x 1cm pieces of the 4 inch wafer were cleaved for processing. The pieces had approximately 300 nm of thermally grown SiO_2 from the manufacturer which needed to be removed. To remove the native oxide, the pieces were submerged in a solution of HF (10:1 NH4F:HF) which etches at a rate of approximately 0.85 nm/second. Etching the pieces for 7 minutes guaranteed no oxide would remain. Thin layers of SiO_2, Al_2O_3 oxide, and HfO_2 were then grown or deposited by thermal oxidation, plasma enhanced chemical vapour deposition (PECVD) or atomic layer deposition (ALD), respectively. After the oxide was grown, the thickness is verified by ellipsometry. The samples were then coated in Hexamethyldisilazane (HMDS) primer before being spin coated with PMGI-S7 and S1811. The samples were then exposed via photolithography using a Heidelberg MLA150 Maskless Aligner and subsequently developed in MF-319. Before the metal deposition, a room temperature O_2 plasma descum ensured a clean surface. Aluminum contacts with a thickness of 100 nm were then deposited in an Angstrom E-Beam deposition system before leaving the samples to lift-off in PG remover over night. Further processing is needed for the back contact of the substrate. The back of the silicon substrate was lightly scratched with a diamond scribe to remove the native oxide. Immediately following this, Indium-Gallium eutectic alloy was applied to the scratched region to form an ohmic contact. It was found that applying a silver epoxy does not form an ohmic contact and is therefore not utilized [31]. A conductive silver paste is liberally applied to a 3 cm x 3 cm glass slide to which the MOS capacitor is then mounted on with the Indium-Gallium alloy in contact with the silver paste. The sample is left to dry for 30 minutes before 2-probe characterization.

3.2 CV Results and Discussion

3.2.1 Charge trap passivation

Interface traps arise when the amorphous structure of the oxide meets the crystal structure of the silicon substrate. They are also thought to arise during various processing steps in

the MOS capacitors fabrication. For example, X-rays generated in the electron beam deposition can damage the sample, increasing the density of charge traps. An O_2 plasma descum is also thought to contribute to the density of charge traps.

Before the results of the 2-probe characterization, a method of device improvement and charge trap passivation should be discussed. Following the metallization of the MOS capacitor, a post metallization anneal (PMA) is performed. The PMA is theoretically expected to reduce the quantity of both fixed oxide charges and charge traps [14]. PMA's were implemented using N_2 gas, O_2 gas or a mixture of H_2 and N_2 known as forming gas. Heated H_2 in the forming gas diffuses into the oxide and passivates the dangling bonds at the Si/Oxide interface and therefore reduces the quantity of charge traps [1]. The temperature and length of the PMA directly affects the quantity of charge traps. The temperature must be high enough such that the hydrogen molecules have enough energy to diffuse through the dielectric. The higher the temperature then the faster the diffusion process will be. If the temperature is too high, hydrogen bonds can become thermally de-passivated [14]. The standard temperature used for a PMA with forming gas is approximately 400C [43].

Plasma enhanced chemical vapour deposition SiO_2

SiO_2 is the standard oxide utilized in quantum dot devices. We deposit 100 nm of SiO_2 via plasma enhanced chemical vapour deposition (PECVD) in the QNFCF Oxford Cluster and perform a series of anneals (H_2 and O_2) at various temperatures for 10 minutes. While thinner oxides provide better signal-to-noise ratio than thicker oxides, PECVD films are often more robust to leakage when thicker. Devices are fabricated with both post-oxidation anneals (POA) and post-metallization anneals (PMA). The flat band voltage and experimental dielectric constant of each device are found in Table 3.1. The control device (no POA or PMA) posses a flat band voltage of $V_{FB} \approx$ -15V which deviates significantly from the ideal MOS capacitor indicating that the PECVD process generates a large density of fixed oxide charges. Each device where a POA was implemented was also shifted from the theoretical V_{FB} of -0.8V. The flat band voltage can be determined from the minimum of the density of interface traps curve. Only the device which had a PMA at 400C in FG showed a convincing reduction in fixed charge traps. Futhermore, this device also exhibits a dielectric constant which is within uncertainty of the theoretical value ($\epsilon = 3.9$). The two devices with only POA (POA in O_2 at 500C, and a POA in FG at 400C) yielded similar results to the control. Theoretically, the POA FG should passivate charge traps produced by the PECVD process, because this CV curve remains stretched and shifted, which indicates that the metallization procedure (E-beam deposition) contributes to the

generation of charge traps, too. Note than the control and POA samples have no reported dielectric constant due to leakage current skewing the oxide capacitance in accumulation.

Device	**Flat band voltage [V]**	**Dielectric constant: K**
Control	-15 ± 2	Unknown
POA 500C O_2	-15 ± 2	Unknown
POA 400C FG	-16 ± 1.75	Unknown
POA 500C O_2, PMA 400C FG	-0.45 ± 0.11	4.24 ± 0.34
POA 400C FG, PMA 400C FG	-0.50± 0.17	4.11 ± 0.25
POA 400C O_2, PMA 400C FG	-0.05 ± 0.21	4.23 ± 0.27
PMA 400C FG	-0.75 ± 0.13	4.03 ± 0.19

Table 3.1: Table depicting the flat band voltages and dielectric constants K extracted from each device fabricated with PECVD SiO_2. The ideal flat band voltage and dielectric constant for SiO_2 is V_{FB} = -0.8V and, K = 3.9, respectively.

We can infer from Table 3.1 that the PMA in FG dramatically reduces the number of interface charge traps. This is seen in Fig. 3.11 with the quantitative density of interface trap calculation. The control D_{it} curve along with the POA only devices is not seen, as the results are skewed by the device leaking at large top gate voltages in accumulation. Furthermore, complete oxide breakdown was observed at approximately V_g = -19V. Each device shows a small decrease in interface traps density at approximately V_g = 4V. This is most evident in the device labelled 'POA 400C O_2, PMA 400C FG'. This is possibly due to deep impurities behaving as recombination sites resulting in a decreased lifetime of charge carriers [1]. The most accurate D_{it} information is found in the depletion region. The depletion region is centered around the flat band voltage and can be estimated to be over the range where the D_{it} curve remains flat or 'not noisy' but is more accurately found in the raw CV measurements as seen in Fig. 3.9a and Fig. 3.9b. Outside of this range (accumulation and inversion), the C_{LF} and C_{HF} can approach C_{OX}. Here, small variations in C_{LF} and C_{HF} can cause large, fictitious changes in interface capacitance and therefore D_{it}.

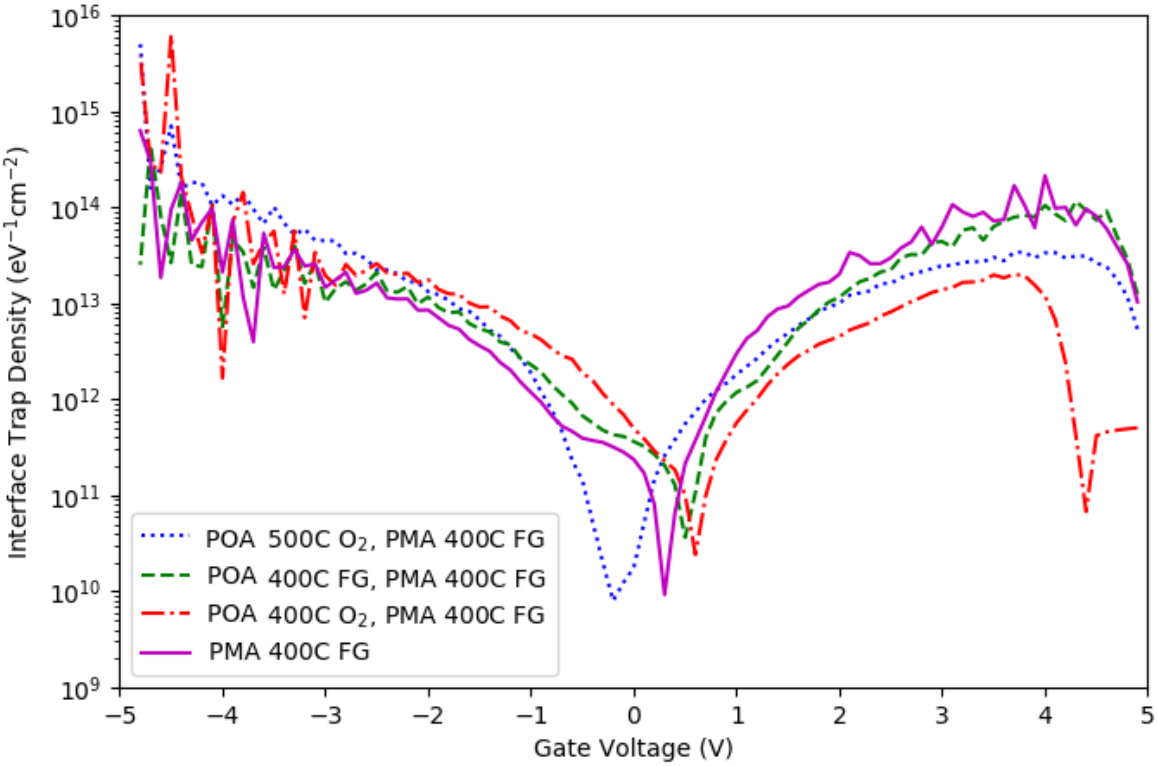


Figure 3.11: Density of interface trap calculation for PECVD SiO_2. The two optimal devices are those labelled 'POA 500C O_2, PMA 400C FG' and 'PMA 400C FG' with an interface trap density less than 10^{10} eV^{-1}cm^{-2}. The different minima indicate the flat band voltage for that device. In deep accumulation and deep inversion, noise is seen due to the limitations of the analytic method. The device labelled 'POA 400C O_2, PMA 400C FG' shows a sharp drop in inversion, possibly due to deep level impurities.

Tystar SiO_2

MOS capacitors were also fabricated using an oxide grown in the Tystar furnace (QNC Nanofab facility). Silicon pieces approximately 1 cm x 1 cm were etched of their native thermal oxide via buffered oxide echant (BOE) before the oxide growth. The Tystar oxidation furnace is used to grow thermal oxides in an O_2 rich atmosphere at 1000 C°for 12 minutes. Following the growth procedure, a standard 20 minute anneal in N_2 at 1000 C°was performed in the Tystar furnace. Following this, ellipsometry was performed and

the devices were found to have 50 nm of grown SiO_2. The Tystar oxide is a dry oxidation process which is thought be better than PECVD because of its slow growth rate which allows for much more uniformity and control in thin-films. The control MOS capacitor remains dramatically horizontally shifted and stretched much like the PECVD SiO_2 control (Table 3.2). In fact, the results are quite similar to those of PECVD SiO_2; the series of POA and PMA tend to improve the quality of the oxide over the control. The device labelled 'POA 600C FG, PMA 400C FG' shows the depletion region and the flat band voltage shifted more negatively than the other devices showing that the 600C PMA in FG may have introduced fixed oxide traps (Fig. 3.12). While performing the high-frequency CV measurement on this device, the capacitance value increased when inversion mode is reached. The ideal MOS capacitor should display an increase in capacitance in this mode in only quasi-static conditions. This indicates that the device has a longer minority carrier generation-recombination lifetime than the other devices, despite being fabricated from the same wafer at the same time. This variation in inversion capacitance, and therefore minority carrier lifetime, may be due to non-uniform fast generation-recombination surface states within the band gap [40]. Furthermore, it is thought that contaminations in the silicon substrate could also cause this to occur [39].

Device	**Flat band voltage [V]**	**Dielectric constant: K**
Control	-9.05 ± 0.47	Unknown
POA 400C FG, PMA 400C FG	-0.80 ± 0.07	3.60 ± 0.23
POA 500C FG, PMA 400C FG	-0.80± 0.09	3.45 ± 0.38
POA 600C FG, PMA 400C FG	-1.49 ± 0.16	3.43 ± 0.48
PMA 400C FG	-0.75 ± 0.11	3.69 ± 0.21

Table 3.2: Table depicting the flat band voltages and dielectric constants extracted from each device fabricated with Tystar SiO_2. The three devices which appear to be optimal are 'POA 400C FG, PMA 400C FG', 'POA 500C FG, PMA 400C FG', and 'PMA 400C FG' with flat band voltages -0.80V, -0.80V and -0.75V, respectively and dielectric constants 3.60, 3.45 and, 3.69, respectively.

One area where the contamination could have arisen is the carrier wafer used in the PMA or the beaker for lift-off. Remnants of other III-V materials and metals could be left behind by other members of the group. This phenomenon was common amongst devices. A higher frequency (greater than 1MHz) can be utilize to decrease the inversion

capacitance. Despite having the most optimal V_{FB} = -0.75V and dielectric constant K = 3.69, the presence of interface traps persists in the PMA 400C FG device. This is seen as the plateau in the density of interface traps curve. For Tystar oxide, the device with the minimal amount of interface traps is the device labelled 'POA 600C FG, PMA 400C FG'. However, the quality of oxide is misleading due to a number of fixed oxide charges. Between the other MOS capacitors, there is very little difference in terms of the minimal value of interface traps; this makes sense as they all experienced the same PMA FG anneal.

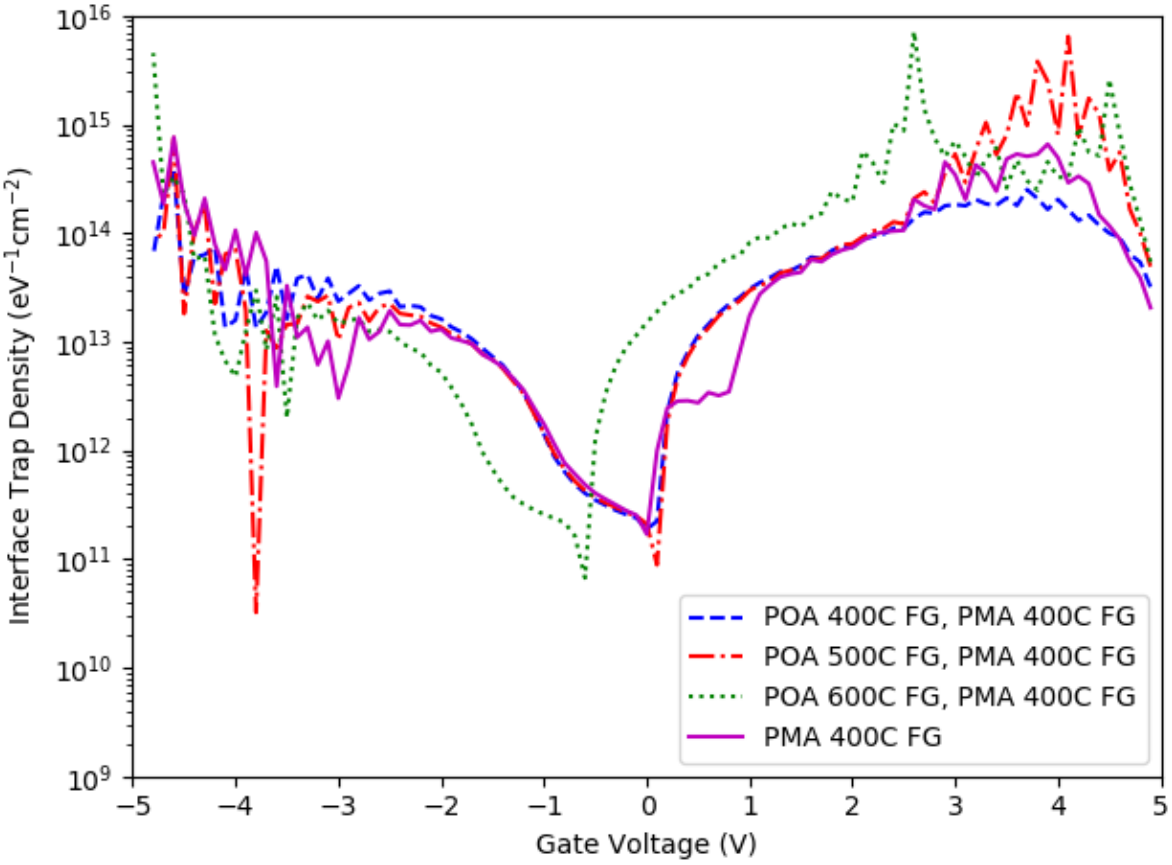


Figure 3.12: Density of interface trap calculation for Tystar SiO_2. Devices have similar interface trap densities as they all received the same PMA in FG. The device labelled 'PMA 400C FG' shows a plateau near V_{top} = 0.5V indicating a region of low interface traps.

Commercial Thermal SiO_2

Wafers that are purchased often come with a grown oxide of their own known as a commercial thermal oxide. A wafer of resistivity 10-20 Ωcm was diced and etched with a buffered oxide echant down to a thickness of 50 nm. This was verified via ellipsometry directly after. Wafer suppliers often try to reduce the number of mobile ions by introducing a small percent of hydrochloric acid (HCL). In theory, this should provide a higher quality oxide than those made via deposition. Table 3.3 shows the control sample having fewer fixed oxide charges than the other grown SiO_2 control devices. All MOS capacitors showed an increase in inversion capacitance in the high-frequency measurement. Aside from the control, the POA and PMA seemed to have little variation in capacitance, flat band voltage and dielectric constant. The QSCV measurements painted a similar picture: the devices with POA/PMA treatment show little variation amongst each other, and showed significant improvement over the control sample. Each of the devices never reached their 'true' oxide capacitance as the accumulation capacitance never flattened, therefore the reported dielectric constants are not optimized. To obtain better results, devices should be pushed to more negative gate voltages.

Figure 3.13 shows the results of the density of interface trap calculations. Quantitatively, each device shows a similar density of interface traps in the depletion region; this is the region where the bands bend to empty and fill the trap states. Outside of the depletion region, 'POA 400C FG, PMA 400C FG' shows signs of non-optimal QSCV measurement indicated by the flat plateaus and larger than expected D_{it}.

Device	**Flat band voltage [V]**	**Dielectric constant: K**
Control	-5.10 ± 0.31	Unknown
POA 400C FG, PMA 400C FG	-0.80 ± 0.04	3.98 ± 0.14
POA 500C FG, PMA 400C FG	-0.85± 0.09	3.88 ± 0.05
POA 600C FG, PMA 400C FG	-0.90 ± 0.13	4.25 ± 0.22
PMA 400C FG	-0.74 ± 0.24	3.88 ± 0.07

Table 3.3: Table depicting the flat band voltages and dielectric constants extracted from each device fabricated with commercial thermal SiO_2. Each device appears to be very similar to the theoretical values of V_{FB} and dielectric constant.

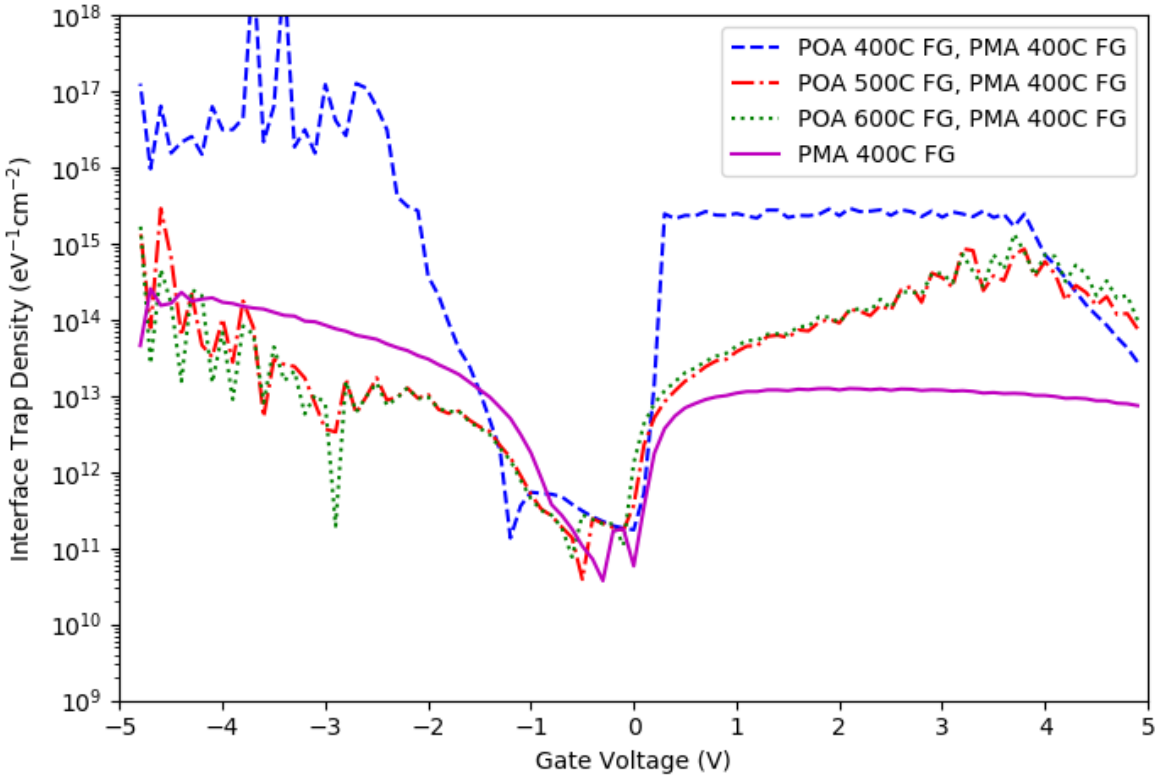


Figure 3.13: Density of interface trap calculation for commercial thermal SiO_2. Each device behaves similar in the depletion regime. The device labelled 'POA 400C FG, PMA 400C FG' shows signs of non-optimal QSCV measurement indicated by the large plateaus and larger than expected D_{it} in accumulation and inversion.

Atomic layer deposition Al_2O_3

Atomic layer deposition (ALD) is a process of developing very thin and conformal films. Wafers are first etched in a buffered oxide echant solution to remove the commercial thermal oxide. The substrate is then processed in the Oxford Cluster to deposit a thin film of Al_2O_3. The film was determined to be 40 nm thick via ellipsometry measurements. The control MOS capacitor qualitatively shows fewer fixed oxide charges than both PEVCD and the Tystar oxide as seen in Table 3.4. This is evidence for the ALD process contributing fewer of this type of charge trap in the oxides growth. Both a PMA in FG and O_2 were performed and both yielded a similar result: similar flat band voltages and dielectric

Device	**Flat band voltage [V]**	**Dielectric constant: K**
Control	0.89 ± 0.32	6.85 ± 0.43
PMA 400C O_2	1.95 ± 0.87	7.95 ± 0.24
PMA 400C FG	1.90 ± 0.85	7.50 ± 0.31

Table 3.4: Table depicting the flat band voltages and dielectric constants extracted from each device fabricated with ALD Al_2O_3. The flat band voltage for devices fabricated with ALD Al_2O_3 appears to become worse after PMA due to possible contamination. The dielectric constants appear to be near the theoretical value of 7.8.

constants. Additionally, hysteresis in the CV measurements was not seen in any either PMA devices, further indicating a decrease in interface traps. The extracted dielectric constants are 7.95 and 7.50 for the PMA 400C O_2 device and PMA 400C FG device, respectively. The expected theoretical dielectric constant for the control device is approximately 8 and after PMA in FG is expected to be approximately 9 [21]. It should be noted that during the QSCV measurement, a sharp drop in capacitance during the DC voltage sweep in inversion occurred and is observed in Figure 3.14 as a sharp drop in interface trap density at a gate voltage of $V_g = 3.5$V. This could be the result of deep level impurities. The control MOS capacitor showed no obvious capacitance decrease in depletion mode, only when the PMA are performed does this appear. This indicates high levels of interface traps. Furthermore, the QSCV curves did not flatten in the accumulation mode which indicates current leakage within the device showing that the electrical isolation of this material is poor. The density of interface traps is seen in Fig. 3.14. It is clear that the PMA causes the interface trap density to reduce by approximately an order of magnitude in the depletion region. Furthermore, we see that the PMA caused the flat band voltages to shift more positively meaning that the rapid thermal processor (RTP) responsible for annealing, could be contaminated.

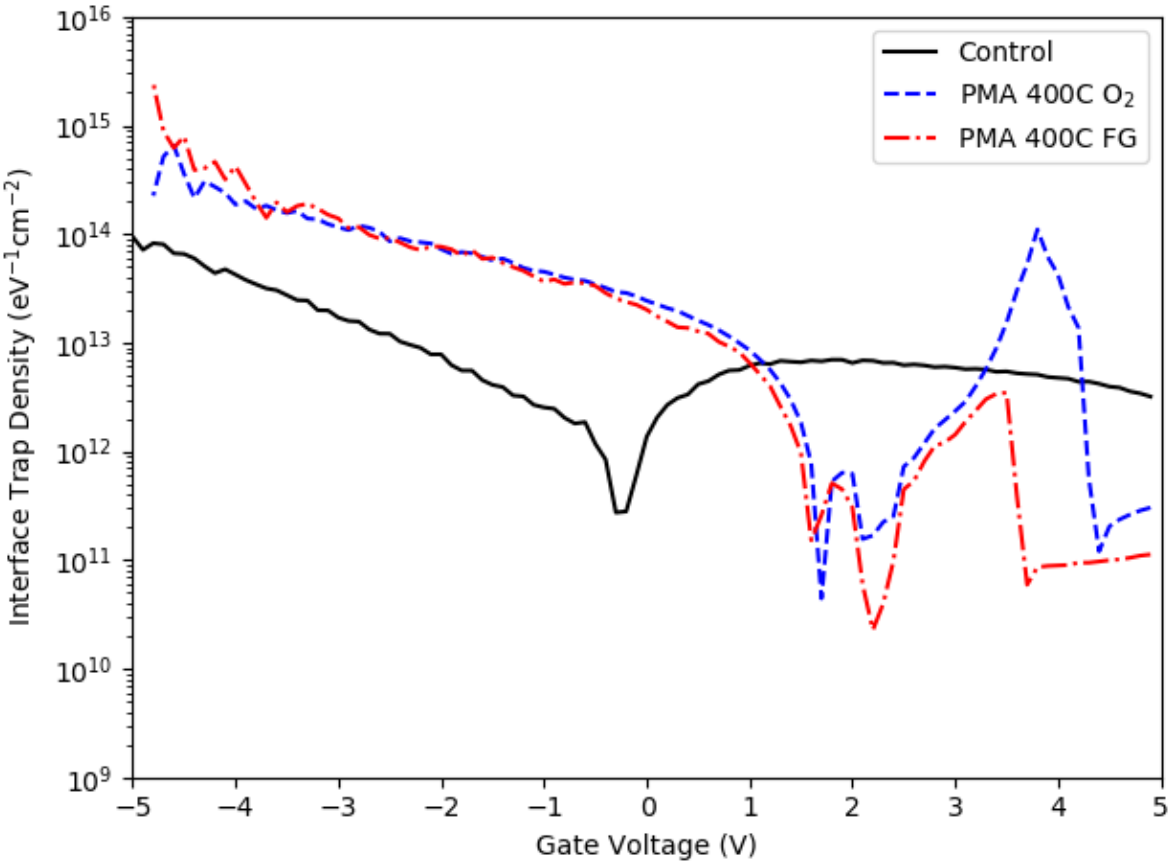


Figure 3.14: Density of interface trap calculation for ALD Al_2O_3. oxide. Devices with a PMA show an order of magnitude less in interface trap density over the control. Additionally, PMA devices have a large shift in flat band voltage and an unexpected decrease in D_{it} in inversion. This is most-likely the result of contamination during the PMA process and deep-level impurities, respectively.

ALD HfO_2

In recent years, large companies such as Intel have been making the switch from SiO_2 to HfO_2 as a dielectric. HfO_2 has the advantage of a high dielectric constant which can be 4-6 times larger than that of SiO_2. Additionally, HfO_2 is typically deposited via ALD, providing thin and uniform thin-films. Silicon pieces diced from a wafer of resistivity 10-20 Ωcm had their native commercial oxide etched in a buffered oxide echant followed by

atomic layer deposition of HfO_2. Ellipsometry was performed to confirm a thickness of 20 nm. A smaller oxide thickness allows for a larger signal-to-noise ratio. Preliminary results from the control device showed that there were few fixed oxide charges but there were a large density of interface charge traps as indicated by the shoulder just as the device enters depletion. PMA were performed at both 300C and 400C in FG. The removal of the shoulder in the PMA devices indicates that some interface traps were alleviated.

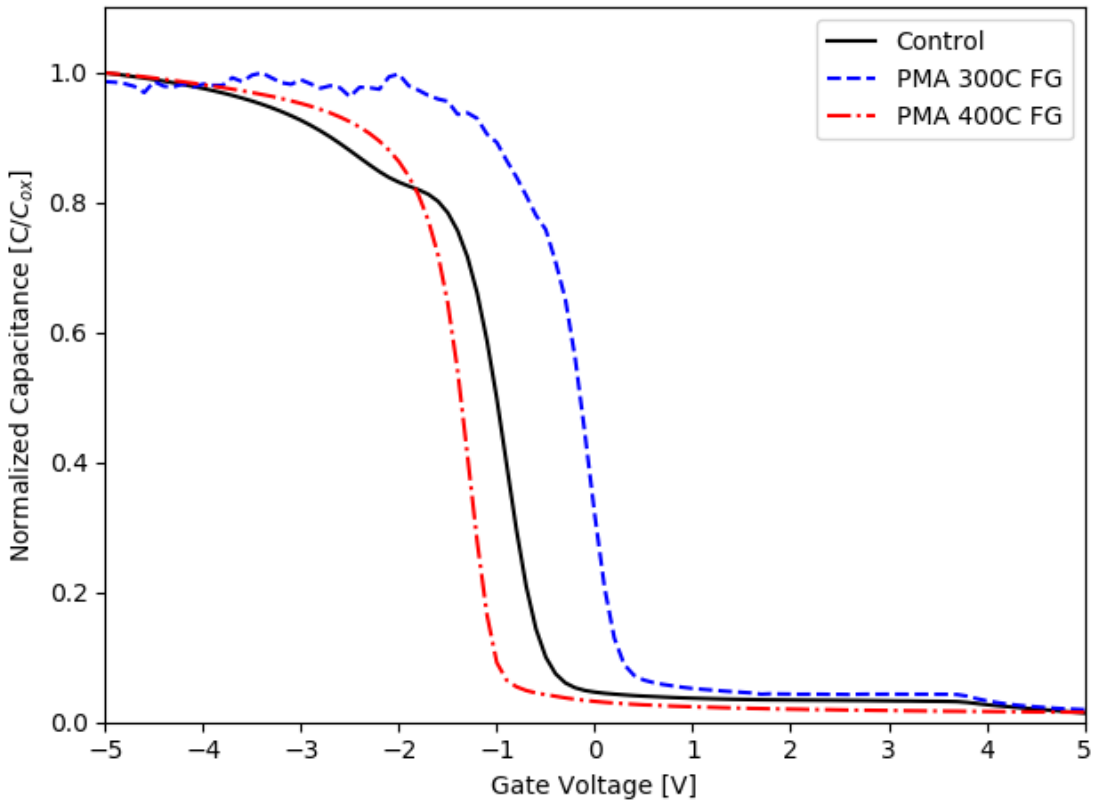


Figure 3.15: High frequency CV measurements for MOS capacitors fabricated via ALD HfO_2. The control device shows a low density of fixed oxide charges but a high density of interface charge traps due to the shoulder seen near depletion. Upon PMA of the devices, the O_2 anneal seemed to introduce fixed oxide charges but reduced the interface trap density while the FG anneal seemed to reduce both fixed oxide charges and interface traps.

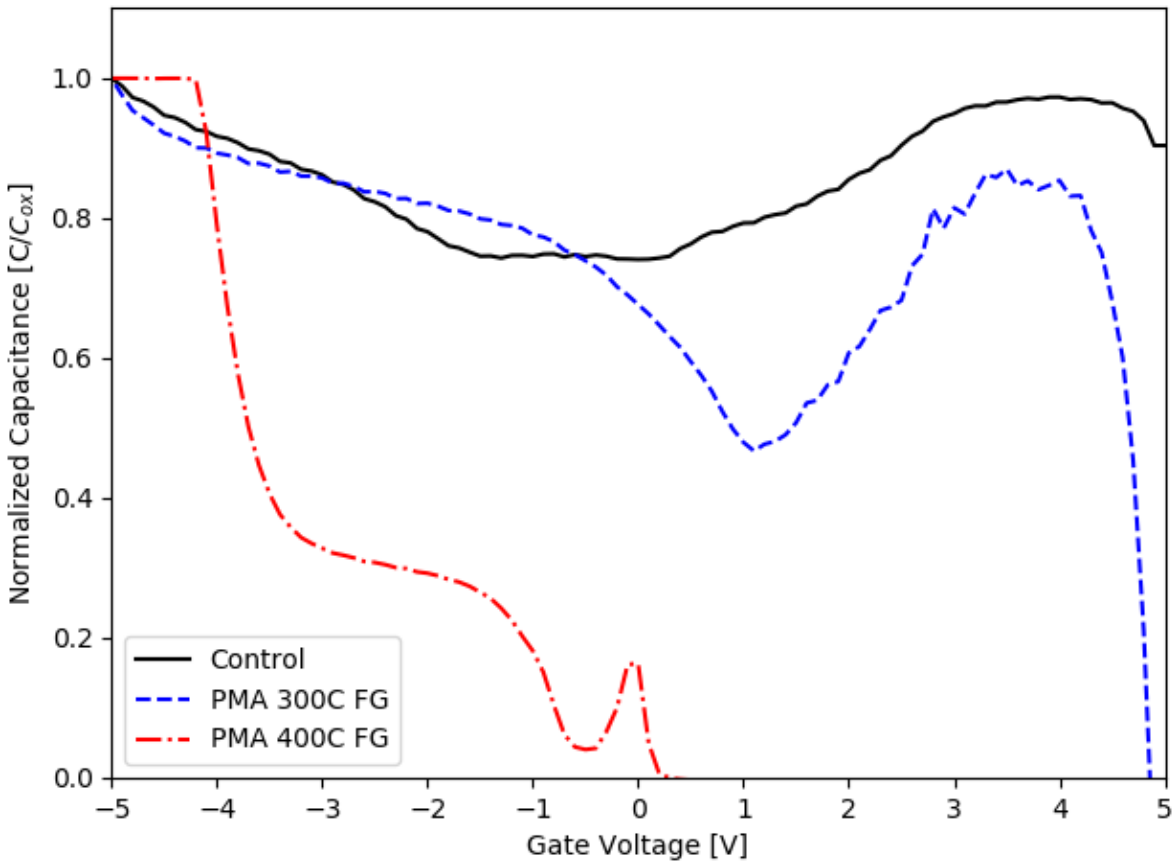


Figure 3.16: QSCV measurements for MOS capacitors fabricated via ALD HfO_2. The control HfO_2 shows no decrease in depletion mode capacitance and does not exhibit a flattening of the accumulation mode capacitance. These are a result of interface traps and oxide leakage, respectively. Annealing the devices after metallization appears to reduce the interface trap density, indicated by the decrease in depletion capacitance but also seens to further degrade the oxide electrically. The PMA 400C FG sample shows oxide breakdown at V_g = -4V.

Performing the QSCV measurements provided a lot of useful information about the quality of the ALD HfO_2. The first observation is that in accumulation, all of the fabricated devices posses an upward curve due to gate leakage. This becomes more pronounced with the PMA devices. The control sample also lacks a deep depletion due to a large density of interface traps. Following the PMA, the depletion region deepens proving that the forming

gas anneal does improve the quality of the oxide with respect to interface traps. It should be noted, however, that electrical isolation deteriorates following the PMA as indicated by the stronger gate leakage within accumulation. The PMA annealed samples also show sudden decreases in inversion capacitance. Finally, the higher temperature 400C FG anneal shows oxide breakdown at approximately V_g = -4V.

3.3 Conclusions

In this chapter, we explored interface traps at the Si/Oxide interface. We first discussed the working mechanisms of MOSCAPs and then discussed how they can be used to characterize the density of interface traps in silicon quantum dot devices. Next, we introduced how a forming gas anneal can theoretically reduce the density of interface traps. It was observed that devices which had no forming gas anneal had a large density of interface traps to the point where the flat band voltage was significantly shifted: up to -15V in some cases (PECVD, Tystar dry oxide). Afterwards, a series of high temperature anneals were performed on the devices. Devices with POA showed no improvement from the control devices, only when a PMA was implemented did we observe a significant reduction in the number of charge traps. This occurred most notably in devices with only a forming gas anneal. Because the POA yieled no change from the control, it is thought that processes which generate high energy X-rays, such as E-beam deposition and E-beam lithography, generate interface traps. Following the PMA (400C for 10 minutes), some devices (ALD Al_2O_3) showed a reduction in the density of interface traps but still had a flat band voltage which was shifted from the theoretical value. This is thought to be due to contamination during either the lift-off procedure or the annealing process. Finally, we found HfO_2 to be a poor insulator both before and after PMA. After the FG anneal, the electrical properties of HfO_2 deteriorated quicker than the HfO_2 control MOSCAP despite having a smaller density of interface traps. For future quantum dots, the data show that, in terms of minimizing the density of interface traps, PECVD SiO_2 and ALD Al_2O_3 are optimal with a density of interface traps on the order of 10^{10} $eV^{-1}cm^{-2}$. This value is in agreement with similarly processed chip which have POA and PMA in FG at 400C for 15 minutes [22, 27].

Chapter 4

Microwave resonator for single qubit operations

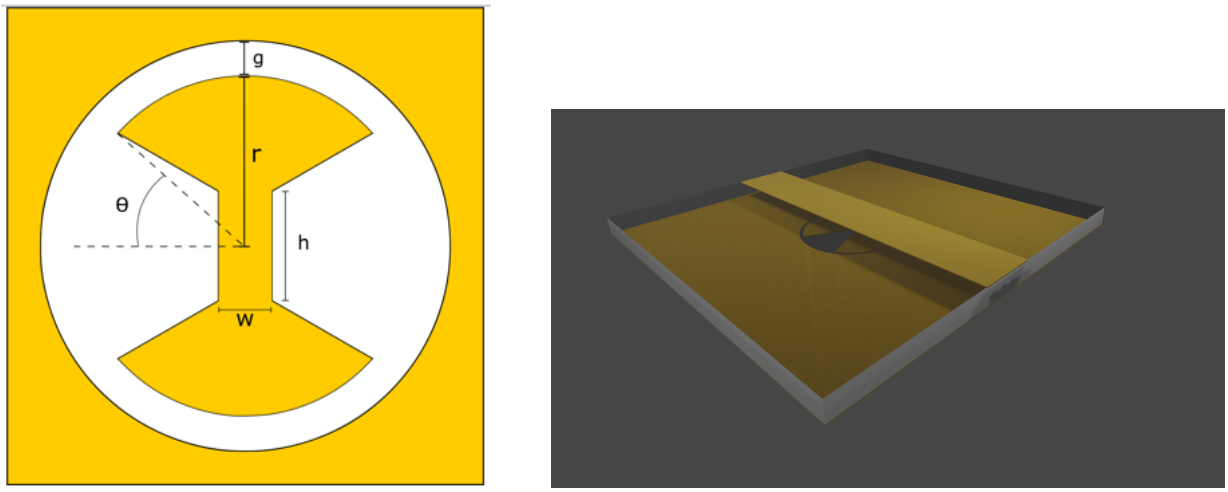
In this chapter, we discuss methods of implementing single qubit rotations in silicon spin qubits. We then provide a method of performing single qubit rotations utilizing a global magnetic field generated by a microwave resonator situated above the quantum dot device. We also present preliminary results from prototype devices and then discuss the design and operation of the resonator.

4.1 Microwave resonator

Electron spins confined to quantum dots are a promising platform for scalable quantum computation. They have shown long coherence times and have the potential to leverage the semiconductor industry to fabricate devices in mass. Advances in high fidelity single-qubit and two-qubit gates has allowed a plethora of research to be performed on developing a large-scale quantum processor. A lot of work in optimizing quantum architectures has occurred. Superconducting strip lines for single-qubit control are bulky (1>micron) and take up valuable on-chip space reducing qubit packing densities. Furthermore, large arrays of qubits would need an immense amount of transmission lines, complicating connectivity within the cryostat [24]. EDSR shows similar faults. Micromagnets and strip lines will also take up on-chip real-estate [5]. Micromagnets make things worse as stray, uncontrolled field lines can cause decoherence effects to nearby shuttling electrons. An elegant solution to this problem is providing the entire qubit array with a single uniform magnetic field.

Conventional ESR spectroscopy involves placing a sample within a large cavity or magnetic coil. This poses problems such as large oscillating electric fields, which can have large negative effects on the metallic top gates.

We provide a design for a microwave resonator which sits atop of a silicon quantum dot device showing high uniformity over a large area. The resonator is adapted and repurposed from Nir Dayan et al [12]. Prototype resonators are fabricated by depositing a thin (2 μm) copper layer on a high permittivity substrate ($\epsilon \approx 11.9$), (500 μm thick) single crystal SiO_2. Single crystal SiO_2 has the advantage of no background signal (it doesn't behave as a dielectric resonator). The bow tie shaped resonator is coupled to a microstrip line on the other side of the quartz substrate (Fig. 4.1b). The magnetic and electric field distribution of the resonator was calculated by Ph.D student Stephen Harrigan in the finite element software HFSS and are seen in Fig. 4.2. The bow tie resonator features low electric field strength in the center of the design while maximizing the magnetic field. This is critical for single qubit operation as the quantum dot array sits below the center of the resonator. With 1W of input power into the strip line, a magnetic field strength of ≈ 1.75 mT is 'felt' over an area of 1 mm^2. Assuming a modest quantum dot pitch of 100 nm, approximately 40 million qubits can fit within this region. In the original literature, the length (long axis) of the resonator was 750 μm and had a resonant frequency of 36 GHz. We scaled the size of the resonator to ≈ 3.5 mm in length to decrease the resonance frequency to approximately 16 GHz. For the photon's energy to equal to the Zeeman splitting, an external magnetic field, B_0, of approximately 0.57T must be applied. Furthermore, the quality factor (Q-factor) extracted from the simulations is approximately $Q = 10$.



(a) (b)

Figure 4.1: (a) Schematic of resonator with the various design parameters. (b) 3D rendering of the resonator, showing the strip line used to couple to the resonator. The quantum dot device layer is below the resonator.

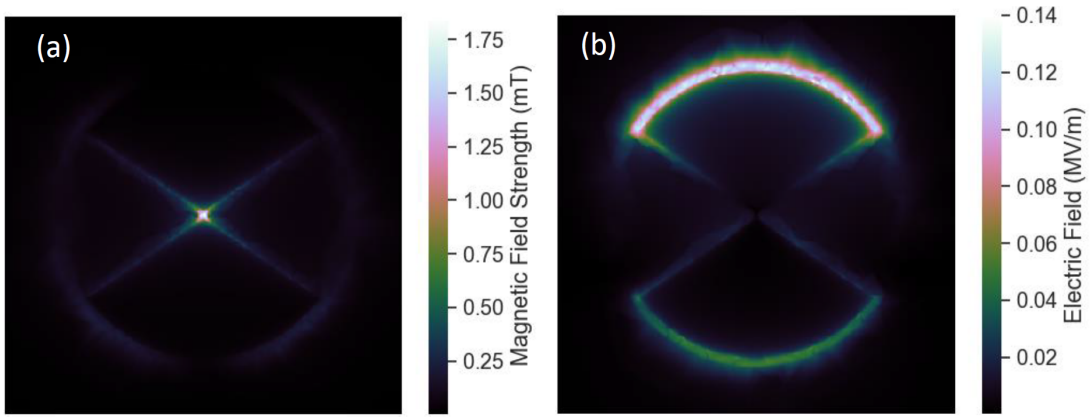


Figure 4.2: Simulated (a) magnetic field and (b) electric field of resonator (design 1) with input power of 1 W. (a) The magnetic field is found to be homogeneous and situated at the center of the resonator. (b) The electric field is found on the outside of the resonator, far away from quantum dot devices.

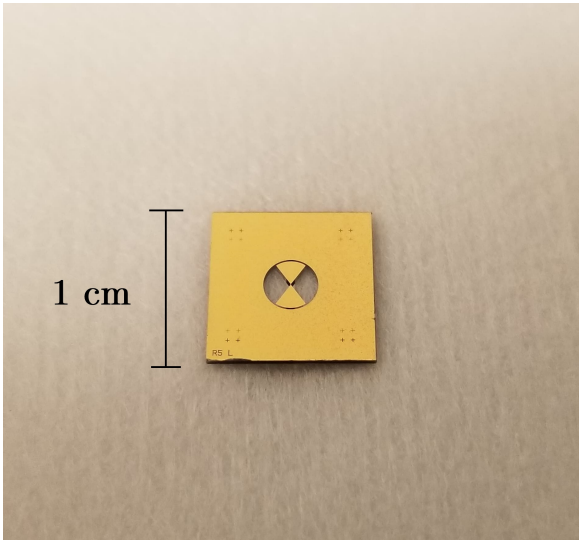
Design	θ [deg]	r [μm]	g [μm]	w [μm]	h [μm]	Theor. f_{res} [GHz]	Exp. f_{res} [GHz]
1	35	1525	100	30	70	16.1	15.5
2	45	1525	100	30	70	16.7	16.4
3	55	1525	100	30	70	17.1	16.9

Table 4.1: Table containing design parameters for 3 groups of resonators as well as theoretical and experimental resonant frequencies.

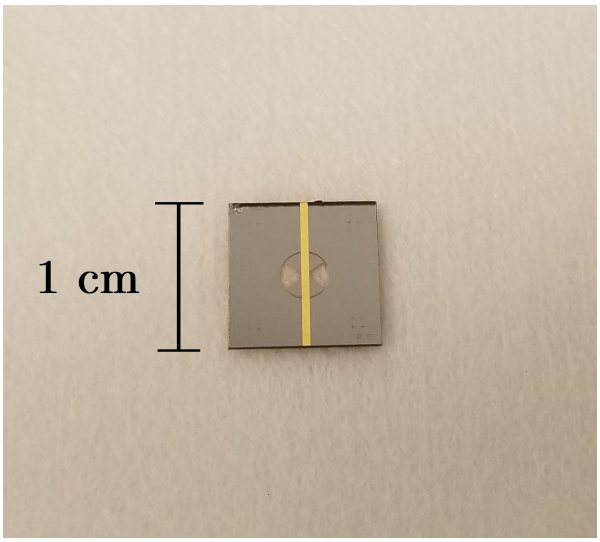
4.2 Results

The resonators were fabricated according to the procedure described in Appendix A.1 (Fig. 4.3a and 4.3b). In total, nine devices were fabricated. The nine devices were separated into groups of 3 which had slightly varying design parameters (Fig. 4.1a). Post fabrication, the resonators were characterized for their resonant frequency and Q-factor using a vector network analyzer (Keysight VNA N5225B). The design parameters and resonant frequencies are seen in Table 4.1. While the substrate had a microstrip line, it was thought that the coupling to the resonator was too poor and therefore it was not utilized in the following experiment. Instead, a high frequency (HF) SMA cable spanned between the two ports of the VNA. At the halfway point between the ports, there is an exposed strip line used to couple to the bow tie resonator (Fig. 4.3c). The exposed strip line is then moved near the bow tie and the transmission (S21) through the SMA cable is measured. This method of testing is preferred as it does not require long cables or adapters that can cause unnecessary losses in signal. Furthermore, there is more control on how close the sample is from the exposed strip line. The transmission coefficient for design 1 is seen in orange in Figure 4.3d. Experimental results from the transmission test yielded a resonance frequency of approximately 15.5 GHz with a quality factor, Q = 10. This is in good agreement with the simulations, however, it is thought that differences in material parameters such as the conductivity of copper and dielectric constant of quartz caused the slight discrepancy between experiment and theory. The observed signal strength was strongly dependent on the orientation and proximity of the exposed strip line.

A series of bow tie resonators were fabricated with superconducting Nb, following the recipe described in Appendix A.1. A substrate thickness of 200 μm was used for these devices. The aim of these measurements was to characterize the frequency response of the resonator at low temperatures when the material is superconducting. A special printed circuit board (PCB) was designed to impedance match to the microstrip on the resonator.



(a)



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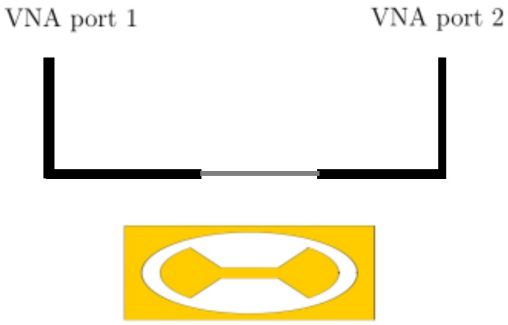

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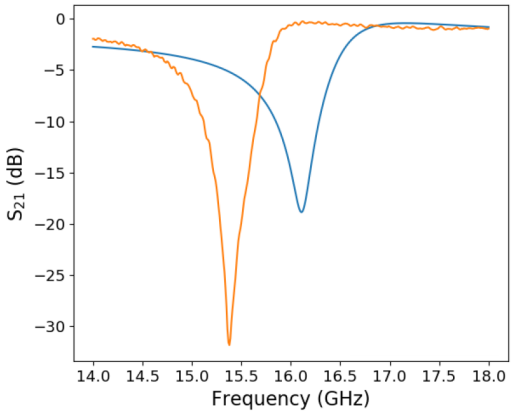
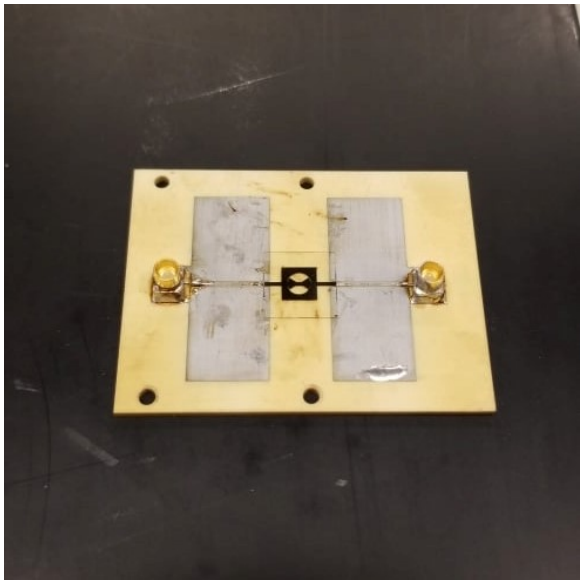


(d)

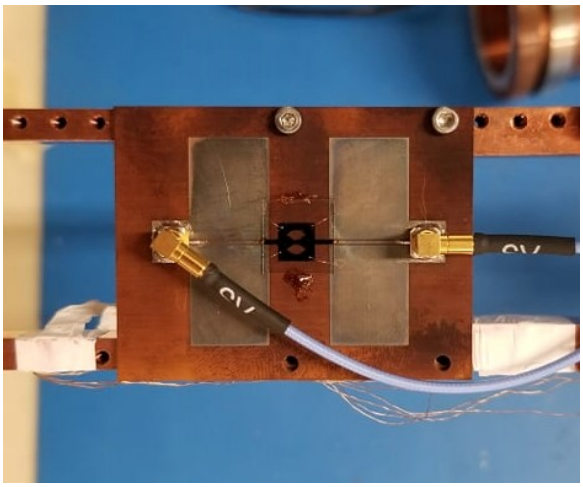
Figure 4.3: (a-b) Front and back of copper resonator, respectively. (c) Shows the resonator transmission test apparatus. A cable is BNC cable is connected from port 1 to port 2 of a VNA. A small section of the cable has been stripped away and the strip-line exposed. The resonator is then brought near the exposed strip-line which behaves as an antenna, triggering a response in the resonator. (d) Transmission S_{21} measured (orange) and simulated (blue) through a coupling strip-line when the resonator is near. A clear resonance is seen in the measured S_{21} near 15.5 GHz.

The radiation pattern of the resonator is easily influenced by the dielectric constant and conductivity of nearby objects. Therefore, the bow tie resonator sits face up, away from the PCB (Fig. 4.4a). Impedance matching is crucial to maximize the power transferred to the resonator. When components in the circuit are not impedance matched, reflections occur, reducing power transfer and minimizing the response in the resonator's transmission function, making it harder to observe and less efficient. The coplanar strip lines on the PCB and the strip line on the resonator chip have all been impedance matched to 50 Ohms. Solder paste is applied lightly to the ends of the coplanar strip lines with a needle. The microstrip line is then placed between the two coplanar strip lines such that the solder paste connects to it. The PCB is then placed in an oven following the standard reflow process (300C for 5 minutes) for tin lead solder. It is noted that solder does not wet Nb at all. To circumvent this, a thin layer (70 nm) of gold was deposited at each end of the microstrip to be able to form the electrical connection. After, Rosenberger Mini-SMP connectors are soldered to the PCB to be able to observe the frequency response of the resonator. Because the microstrip line is in contact with the PCB, the resonator and ground plane are 'face-up'. This allows for wire bonding to the ground plane to form a transmission line.

The resonator and PCB is fixed into Janis probe 5 as seen in Figure 4.4b and is then cooled down to 1.4K. The transmission coefficient is then measured using a vector network analyzer (HP-VNA2). SMA cables are fixed from the VNA ports to the SMA connectors on the probe and the transmission coefficient is observed. The temperature of the niobium resonator is then increased until it is no longer superconducting (near 9K). As the resonator changes from superconducting to non-superconducting, a change in the transmission coefficient and quality factor should be observed. When non-superconducting, the resonator should show a smaller absolute transmission coefficient and quality factor than when it is superconducting, as they are functions of the materials resistance. Figure 4.5 shows the measured transmission function. While there are two peaks observed in this figure, only one is thought to result from the resonator. The other peak is thought to be a resonance associated with the two coplanar strip lines and Nb stripline system. When non-superconducting, the resonator shows a clear response at approximately 16.39 GHz. The extracted transmission coefficient is S_{12} = -80.3 dB and the quality factor is Q = 97.5. When superconducting, the resonator shows a larger dip in transmission at S_{12} = -92.1 dB, while the quality factor nearly doubled to 182.7. These resonances are the only two to change when the Nb changes from superconducting to non-superconducting indicating that they are strictly due to the strip line and resonator. This S_{12} coefficient is the port-to-port transmission. Subtracting the losses from the SMA cable connecting to port 2 of the VNA (-20dB at 16 GHz), and one of the high frequency lines of Janis probe 5 (-24dB at 16GHz) and the losses due to connections to the PCB (-5dB), we can determine the transmission



(a)



(b)

Figure 4.4: (a) Niobium resonator spanning between two coplanar strip lines. (b) PCB placed inside Janis probe 5 connected to two HF cables. The cables are then connected to an external VNA for transmission measurements. The ground plane on the Nb resonator is wire bonded twice to each coplanar stripline's ground plane.

coefficient at the resonator strip line to be S_{12} = -43.1 dB. Furthermore, the relation between the B_1 field generated by the resonator and the applied microwave power is $B_1 = C\sqrt{P_{MW}}$. Using Fig. 4.2 we can determine that C = 1.75 mT/$\sqrt{W}$. Therefore, with -5 dBm applied from port 1 of the VNA, the power incident at the resonator strip line is -48.1 dB ($20\mu W$). This microwave power generates a magnetic field strength of $B_1 = 7.8\ \mu T$. At this field strength, the Rabi frequency would be ω_{Rabi} = 219 kHz. This field strength is comparable to off-chip dielectric resonators ($B_1 = 42\ \mu T$), yet substantially lower than on-chip methods of generating oscillatory fields (B_1= 1.5 mT) [45, 25]. The resonators field strength can be improved by further impedance matching. Additionally, using a Rohde & Schwarz microwave generator, which is capable of applying an output power of +20 dBm, would substantially increase the generated field strength ($B_1 = 122\ \mu T$, $\omega_{Rabi} = 3.42$ MHz). Additional simulations were performed by Ph.D student Zach Merino utilizing a substrate thickness of 200 μm and show a theoretical quality factor of approximately 300. While the experimental results do not match exactly, they indicate that the resonators design operates at an expected frequency of nearly 16 GHz while demonstrating a stark increase in the quality factor when superconducting. The difference between theoretical Q-factor and experimental Q-factor is thought to be due to inferior coupling of the strip line to the resonator. This could be the result of variations in the thickness of the quartz substrate which can vary up to $\pm$ 10%. Additionally, the PCB which the strip line is in contact with alters the geometry of the electromagnetic field lines radiating out from it, which could further reduce coupling to the resonator. To further characterize the frequency response of the resonator, more testing is necessary with quantum dot devices.

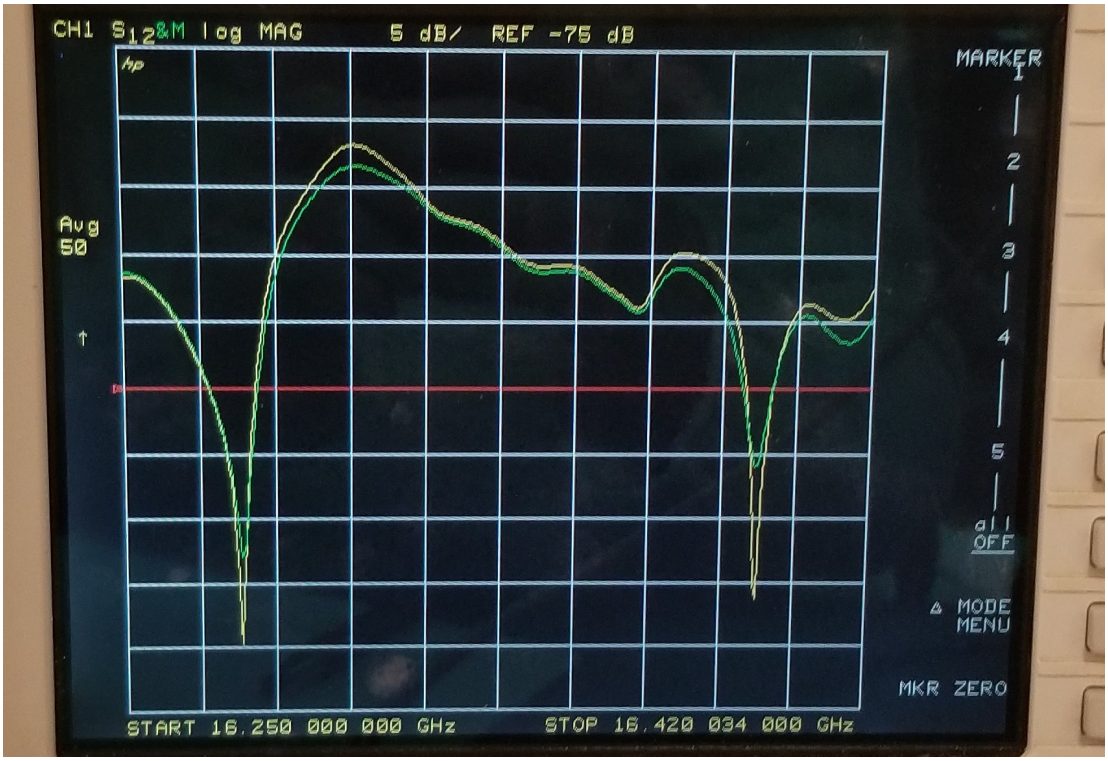


Figure 4.5: Transmission response of superconducting (Yellow) and non-superconducting (Green) niobium resonator. Two peaks are observed: one at $f = 16.27$ GHz and one at $f = 16.39$ GHz. Both appear to be related to the Nb on the PCB as they both increase in transmission when the resonator turns superconducting. However, the resonance dip at $f = 16.39$ GHz is expected to result from the resonator itself as the Q-factor also changes.

Chapter 5

Conclusions

Single electron spins confined to silicon quantum dots are a favourable semiconductor device for spin-based quantum computing due to their small chip foot print, scalability and long coherence times resulting from a spin-free Si 28 nucleus. Chapter 1 provides an introduction to quantum dots from an electron transport perspective. The chapter then discusses how electron spins can behave as qubits covering ideas such as qubit initialization, single qubit gates, two-qubit gates and spin readout. Finally, the rationale for using silicon versus Si/Ge or GaAs is briefly covered.

Chapter 2 focuses on developing and characterizing test structures to test the quality of the inter-gate oxide. In quantum dots, overlapping gates must be completely electrically isolated, otherwise perfect control over the qubit is compromised. Two sets of test structures are fabricated. The first set uses overlapping aluminum layers while the second set focuses on overlapping palladium layers. Aluminum allows for simpler fabrication as a natural native oxide forms on top of it, whereas palladium is a more modern approach allowing for potentially smaller devices. However, palladium does not oxidize naturally. It is found that the optimal oxide used with aluminum is a hotplate grown oxide with 4 nm of ALD Al_2O_3. The breakdown voltage was determined to be 4.92 ± 0.27 V. For palladium, breakdown voltage is studied as a function of ALD Al_2O_3 thickness. Afterwards, forming gas anneals at 300C for 10 minutes are performed. After this anneal, the breakdown voltage appears to increase, while the leakage voltage decreases. It was also found that too high of an anneal temperature can compromise the quality of the aluminum layers.

Chapter 3 is concerned with the quality of the grown/deposited oxide above the silicon substrate. At the interface of the Si substrate and the oxide, interface traps can appear due to the oxides amorphous structure. The interface traps are electrons or holes which can

interfere with the qubits within quantum dots. MOS capacitors are fabricated and characterized using a silicon substrate and various oxides, including, PECVD SiO_2, TYSTAR dry oxide, commercial thermal SiO2, ALD Al_2O_3 and ALD HfO_2. The density of interface traps is characterized by measuring the capacitance at high and low modulation voltage frequency. Prior to a forming gas anneal, the oxide quality is poor and electrically breaks down before a quantitative density of interface traps is found. However, interface traps can be qualitatively observed in the high modulation voltage frequency as a large shift in the flat band voltage. The forming gas anneals show a reduction in the value of interface traps with the optimal oxides (PECVD SiO_2 and ALD Al_2O_3) having a $D_{it} = 10^{10}$ $eV^{-1}cm^{-2}$. It is also found that various processes during fabrication introduce interface traps and fixed oxide traps. Processes involving electron beams (E-beam deposition, E-beam lithography), often generate X-rays damaging the Si/Oxide interface. Furthermore, communal processes, such as Rapid Thermal Process (RTP) annealers and the Oxford cluster, can contain contaminants, further reducing the quality of the oxides.

Finally, Chapter 4 presents an alternative method for single qubit rotation. The bow tie resonator sits directly above a quantum dot device, generating a uniform oscillating magnetic field to drive spin rotations. This methods allows for scalability due to the sharp reduction in the amount of high frequency interconnects necessary when compared to conventional methods. Simulations performed by Ph.D students Stephen Harrigan and Zach Merino show that a superconducting resonator has a resonance frequency of $f = 16.5$ GHz, while hosting a quality factor of 10 and 300 when the substrate thickness is 500 μm and 200 μm, respectively. Furthermore, the design minimizes the electric field and maximizes the magnetic field 'felt' by the quantum dots, thereby reducing the probability of photon assisted tunneling. After, two prototype devices were fabricated, one made of copper for testing at room temperature and one made of superconducting niobium for testing at 1.4K. In response to a transmission excitation the copper resonator shows a clear response at a frequency of $f = 15.5$ GHz, with a quality factor of nearly 10, agreeing with the simulations. To test the niobium resonator, a PCB with two impedance matched coplanar striplines was developed. At 1.4K, the niobium shows a clear resonance dip at $f = 16.39$ GHz. When the device turns from non-superconducting to superconducting, the transmission response increases as the resistance decreases, as expected. The quality factor at 1.4K is only 182.7 whereas simulations expect a value of nearly 300. It is expected that the coupling strength between the Nb strip line and resonator is worse than theoretically shown as a result of variations in wafer thickness and changes in the field lines emanating from the strip line due to the PCB.

5.1 Outlook

The work in this thesis aims to develop, characterize and optimize the quality of quantum dots for quantum information processing. With that in mind, more work in optimization can be achieved with respect to the tests performed in Chapter 2 and Chapter 3. For both tests, various parameters can be further studied such as the length of anneal, temperature of anneal and thickness of oxide. More interestingly however, is the type of oxide that can be used. Currently, the ability to deposit SiO_2 via ALD is being implemented in the Oxford Cluster in the QNFCF, allowing for further development and characterization. ALD provides much finer quality films than PECVD. Therefore it is expected that the interface trap density would be reduced. Furthermore, it would allow for a high quality, thin SiO_2 film to behave as the inter-gate oxide.

Both successful fabrication and characterization of superconducting resonators has been demonstrated in Chapter 3. However, difficulties in fabrication prevented testing the resonator with functional quantum dot devices. Much work still lies ahead to test the resonator in tandem with functional quantum dots. As stated before, the resonator lies directly above the quantum dot device. There are two different methods of attaching the resonator to the top of a quantum dot device. The first is depositing an oxide cladding on top of the quantum dot device as to not short the gates to the resonator or ground plane. To ground the ground plane, metal must then be deposited on the oxide cladding which can then be wire bonded to. Finally, the quartz substrate with resonator and strip-line is placed directly on top of the quantum dot device and held in place with GE varnish. This method excels in quick characterization. However, it doesn't ensure the ground plane will be electrically grounded. The second method is fabricating the resonator directly on top of a finished quantum dot which provides a lot more control in processing and will ensure the ground plane can be grounded effectively.

We have seen that prototype microwave resonators made of copper have a resonance dip in their transmission spectrum at a frequency near 15.5 GHz and with a quality factor of $Q = 10$. We have also observed the frequency response of the resonator fabricated with superconducting niobium. The next step in testing is to perform photon assisted tunneling (PAT) in a quantum dot or SET device. In brief, the resonator generates a high frequency magnetic field which is utilized for single qubit rotations. A high frequency electric field is also generated which can excite electrons into higher energy orbitals or to the electron reservoirs nearby. By tuning a quantum dot to a coulomb peak and applying a high power RF signal, the current through the device will decrease because additional energy levels are attainable via PAT. This results in a lower probability of the electron state situated between the chemical of the left and right reservoir being occupied and reduce the coulomb

peak height.

Lastly, the bow tie resonator is an elegant solution to the issues that current methods of single qubit implementations face regarding scalability. With a network of many quantum dots, a single resonator can provide a uniform magnetic for spin rotations. The resonator is designed to operate at a single high frequency which can be altered by varying the size of the resonator. The larger the resonator is, the lower the resonant frequency. Reducing the size of the resonator increases the resonant frequency. With many quantum dots 'feeling' the same magnetic field at a certain frequency, single qubit operations must be implemented by tuning the g-factor of non-target qubits off resonance. This is achieved by varying the electric field experienced by non-target qubits and is implemented via changes in electrostatic gate voltage. Tuning the g-factor of the electron shifts the Zeeman splitting of electrons such that they are off resonance with the frequency of the resonator allowing only targeted qubits to rotate.

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APPENDICES

Appendix A

Fabrication

In fabrication, small variations during processing can have drastic effects on the outcome of ones device. Therefore it is crucial that each step in the process is recorded and understood. Below are the recipes in detail for devices which were fabricated during this thesis.

A.1 Microwave resonator

This section will cover the process of fabricating the microwave resonators. For the microwave resonator, both sides of a quartz wafer is fabricated. The fabrication process is identical for each side, only the pattern is different. The microwave resonator side is processed first. Note that this recipe is for the prototype devices. For the actual devices, 250 nm of Nb or NbN will be utilized and the fabrication process will be a bi-layer process (similar to the MOS capacitor process).

1. Cleave 4 inch quartz water such that there are 9 equally sized pieces
2. Acetone rinse for 60 seconds followed by IPA for 60 seconds. Blow dry with N2 gun until dry
3. Spin coat nLOF 2035 (negative resist) at 2000 rpm for 60 seconds
4. Soft bake at 110C for 60 seconds
5. Photolithography exposure. Dose/Defoc = 450/-2. Wavelength = 375 nm

6. Post exposure bake at 110C for 60 seconds
7. Develop in AZ300 for 60 seconds
8. Moderate descum in the Asher (required for thick resists such as nLOF)
9. Deposition of Ti/Cu/Au, 20 nm/2000 nm/100 nm. (Use pocket 4 in the IntelVac for the copper deposition and deposit at a rate of 5 A/s)
10. Lift-off in PG remover overnight

A.2 MOS capacitors

The fabrication process for the MOS capacitors is a bi-layer process.

1. Take approximately 1 cm x 1 cm pieces of a silicon wafer you want to study
2. Acetone rinse for 60 seconds followed by IPA for 60 seconds. Blow dry with N2 gun until dry
3. Coat with HMDS
4. Spin coat PMGI-SF7 (positive resist) at 5000 rpm for 60 seconds
5. Bake at 150C for 5 minutes
6. Spin coat S1805 (positive resist) at 5000 rpm for 60 seconds
7. Bake at 120C for 90 seconds
8. Photolithography exposure. Dose/Defoc = 100/0. Wavelength = 405 nm
9. Develop in MF-319 for 60 seconds
10. Light descum in the Asher
11. Deposition of aluminum for the top gate (100 nm)
12. Lift-off in PG remover overnight
13. Remove native oxide from the back of the small piece with a diamond scribe. Be careful not to damage the processed side

14. Remove any debris from the scratched side with a small amount of IPA
15. Using swabs, carefully apply Indium-Gallium paste to the area you previously scratched (special permission from fab-staff is required to use the Indium-Gallium paste)
16. Cut a glass slide in half and apply silver epoxy to one of the halves
17. Carefully press the silicon piece such that the Indium-Gallium paste makes contact with the silver epoxy
18. Leave device to dry for 30 minutes

A.3 Gate-oxide test structures

The process for the gate-oxide test structures is described below. The first layer follows a standard bi-layer while the second layer utilizes an E-beam resist because MF-319 will etch aluminum and aluminum oxide.

Beginning with the first aluminum layer.

1. Take approximately 1 cm x 1 cm pieces from a silicon wafer
2. Acetone rinse for 60 seconds followed by IPA for 60 seconds. Blow dry with N2 gun until dry
3. Coat with HMDS
4. Spin coat PMGI-SF7 (positive resist) at 5000 rpm for 60 seconds
5. Bake at 150C for 5 minutes
6. Spin coat S1805 (positive resist) at 5000 rpm for 60 seconds
7. Bake at 120C for 90 seconds
8. Photolithography exposure. Dose/Defoc = 100/0. Wavelength = 405 nm
9. Develop in MF-319 for 60 seconds
10. Light descum in the Asher

11. Deposition of aluminum for the top gate (35 nm)
12. Lift-off in PG remover overnight
13. Deposit/grow oxide immediately after removing it from the PG remover

The second aluminum layer process is listed below.

1. Spin coat MMA (positive E-beam resist) at 5000 rpm for 60 seconds
2. Bake at 180C for 5 minutes
3. Spin coat S1811 (positive resist) at 5000 rpm for 60 seconds
4. Bake at 120C for 90 seconds
5. Photolithography exposure. Dose/Defoc = 100/0. Wavelength = 405 nm
6. Develop in MF-319 for 60 seconds
7. Bake for 5 minutes at 150C to hard bake S1811
8. Flood exposure in UV Ozone machine (20 minutes. Longer is better. Stage height set to 9cm. Temperature set to 0C (room temperature)
9. Develop in IPA:Water (7:3) [35 mLs IPA: 15 mLs water] for 2 minutes and 15 seconds. If residue is observed in the pattern, this is a sign that the MMA was under exposed. At this step, the sample can be further exposed and subsequently developed until it is removed
10. Deposition of aluminum for the top gate (35 nm)
11. Lift-off in PG remover overnight