FPGA Based Ultrasonic Non-Destructive Testing

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

In this research, a prototype of an ultrasonic testing device was developed based on a field-programmable gate array for ultrasonic testing. Ultrasound is a mechanical wave that is generated by a vibrating object and propagates through a medium. Ultrasonic testing is one of the most used nondestructive testing (NDT) techniques in industries. Various types of ultrasonic devices are used for ultrasonic testing to detect cracks, defects, and fractures. Despite being a well-known technique, the commercially available ultrasonic NDT equipment requires skilled personnel for conducting the inspection and has limited access to the raw data. The training of these inspectors requires a lot of time and resources. Testing of equipment by human inspectors becomes a tedious and difficult process when many components must be inspected. For automated inline inspections in industries access to raw data is essential for the onboard algorithms to understand and adjust effectively. To improve the efficiency of NDT and to aid the transition from labor-intensive manufacturing to the upcoming "Industry 4.0" that aims at total industrial automation it is required to automate the inline inspection process in industries. To facilitate this transition an affordable, compact, and versatile prototype system based on a field-programmable gate array was developed, tested, and optimized. Various experiments were conducted on different specimens with artificially induced defects to study the behavior of the system. The prototype displayed excellent capabilities for signal generation, acquisition, and processing. It exhibited proficiency in NDT applications and successfully detected mm-level defects in steel and aluminum specimens. A comparison between the prototype system and commercially available NDT systems was carried out to examine the performance of the prototype to guide future developments.

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I would first like to thank my supervisor Prof. Hyock Ju Kwon for his guidance and dedicated involvement in every step throughout my MASc study. Without his support, encouragement, and valuable advice this thesis would have never been accomplished. I sincerely thank him for providing me with this inimitable opportunity of pursuing a MASc study in the field of Engineering.

My sincere thanks to my colleague and friend Yanjun Qian for his efforts and continuous support during my studies at the University of Waterloo.

I would like to thank my parents for the true love and support that they gave me throughout my life. I extend my gratitude to Yasmin Shabeer for her never-ending support and encouragement.

Dedication

This thesis is dedicated to my parents and family members.

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Chapter 1
Introduction

1.1 Thesis Outline

This thesis consists of 5 chapters. The first chapter focuses on the background, modern technologies, and the objective of this project. Chapter two discusses the methodology used to find a solution for the problems. Chapter three focuses on the development of FPGA based Ultrasonic NDT system for industrial applications. Chapter four discusses the results obtained from the experiments conducted and provides a comparison between the prototype and commercial NDT devices. Finally, chapter five provides the conclusions and details for future work.

1.2 Backgrounds

1.2.1 Non-Destructive testing

Non-destructive testing is a method that identifies and characterizes the defects on the interior and surface of the materials without altering or damaging the material and its applications [1]. Ultrasonic NDT systems that are commercially available provide highly sensitive flaw detection capabilities when shorter distances and physical access to the material are provided [2]. The major disadvantages of ultrasonic NDT are that it requires trained personnel for the interpretation of acquired data and reduced reliability due to human errors. The key components of NDT are a clear-cut procedure to conduct the testing, advanced NDT tools and trained personnel for following the procedure and successful interpretation of data [3]. The training of these personnel requires a significant amount of time and resources involved. Testing carried out by human inspectors would become a tedious and difficult job when many components must be inspected [4]. As humans are prone to boredom and fatigue the reliability of the results is affected. Hence to reduce the cost of the NDT and improve the inspection quality it is required to automate the inspection process [5]. Integrating the automated process of inspection into the manufacturing sector aids the transition from labour-intensive manufacturing to the upcoming “Industry 4.0” which aims at total industrial automation [6].

1.3 Literature Review

1.3.1 Ultrasonic Testing (UT)

The sound that is audible to humans is ranging between 20Hz to 20KHz frequencies [7]. Sound waves having a frequency higher than 20 kHz are referred to as ultrasound which a human ear cannot detect or hear. Sound waves in the high-frequency range of 0.15 to 15 MHz are being used in ultrasound testing (UT). Like a sound wave that propagates through air, ultrasonic waves can propagate through materials and when they encounter any defects or abnormalities, they get reflected which can be captured and used to identify the defects. Ultrasonic waves cannot be transmitted through the air; thus, if there is an air gap between the ultrasonic transducer and the tested metals, ultrasonic testing cannot be well conducted. To overcome the difficulty of transmitting waves to metals, water, or gel couplant is applied to the material to be tested to act as conductive medium between the transducer and the material being tested [8]. The two common ultrasonic testing methods are pulse-echo and through-transmission. The various components of pulse-echo testing are transducer, pulser/ receiver, and a display. The pulser/receiver is a device that can produce high voltage electrical signals. Transducers are devices that are driven by the high voltage signals from the pulser/receiver to produce high-frequency ultrasonic waves. The waves produced by the transducer are then introduced to the material to be tested. When the waves encounter a defect part of it is reflected and captured by the transducer. The reflected wave signal is then converted to electric signals and displayed on the screen. By knowing the velocity of waves in that material, the size, location, and orientation of the defects can be obtained [9].

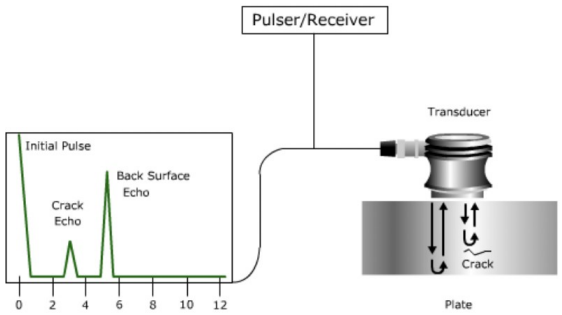


Figure 1.1: Pulse-echo ultrasonic testing system [10]

In solids, based on the oscillation of wave particles, there are four principal modes in which the sound wave can propagate. They are longitudinal, shear, plate, and surface waves. Longitudinal and shear waves are predominantly used in ultrasound testing. Longitudinal waves are also called compression waves because compression and expansion forces are active on them. The wave particles oscillate along the wave propagation's direction. Longitudinal waves can be produced in gases, liquids, as well as solids as the energy, travels in a series of expansion and compression movements through the atomic structure. In shear waves, the oscillation is at 90 degrees to the wave propagation direction. Shear waves require solids to propagate and their propagation through liquids and gases is less effective compared to solids. Compared with compression waves, shear waves are weak in nature [8]. Surface waves or Rayleigh waves are waves that travel through the surface of the material and penetrate through them to a depth of one wavelength. It has an elliptical motion due to longitudinal and transverse motions. These are used to inspect materials with intricate round featured surfaces. Plate or Lamb waves are like Rayleigh waves, but they only occur in plates with small thickness. They can travel significant distances within the material and are useful in scanning wires, plates, and tubes [11].

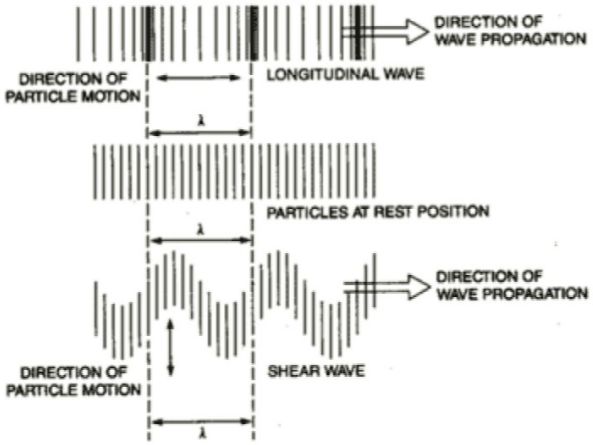


Figure 1.2: Wave propagation of longitudinal and shear waves [12]

Detecting the irregularities in specimens having complex shapes and design is difficult with the conventional UT. Hence to improve the inspection quality, phased array ultrasonic testing (PAUT), guided wave technology, laser ultrasonic testing technology and electromagnetic ultrasonic testing methods are proposed [13]. The shortcomings of conventional UT can be solved by PAUT by providing the ability to focus and steer the signals at desired locations and angles. Using a phased array transducer with a series of ultrasonic elements provides the chance to activate individual elements in a sequence that is programmable [14]. Guided wave ultrasonic testing (GWUT) is used to monitor the structural health of composites having complex designs and shapes [15]. GWUT has the potential for long-range inspections of pipelines and corroded structures. As it works using low frequency and energy attenuation this method is cost effective [16]. Shear horizontal guided waves can travel circumferentially while the transducer moves along the axis of a given pipe. The operation of SH waves is preferred to other systems for pipe inspections as it can be applied to the exterior pipe without the necessity to cover the total circumference and its ability to scan coatings as thin as 1mm [17]. Laser ultrasonic testing technology (LUTT) was able to successfully identify holes with a small diameter (0.8mm) on an additive manufactured (AM) Ti-6Al-4V part. LUTT achieved a high resolution and has shown capabilities to be used as a non-destructive testing technology for AM parts [18].

1.3.2 Field Programmable Gate Array (FPGA)

Field Programmable Gate Arrays (FPGAs) are integrated circuits that can be reprogrammed electrically into any desired digital circuit system [19]. The development of ICs in the 1960s has paved the path for the origin of FPGAs. In 1967 the first FPGA (static memory-based) commonly known as SRAM-based FPGA was developed by Wahlstrom [20].This architecture used a line of configuration bits to achieve both interconnection and logic configurations. Even though SRAM-based FPGAs were versatile and offered re- programmability in devices they required a large area per programmable switch which waslater resolved when the cost of transistors was lowered resulting in the commercialization of FPGA in the 1980s. It was in 1984 the first modern-era FPGA was released by Xilinx [21]. When compared to the first FPGA which had sixty-four logic blocks and 58 I/Os the modern era FPGA has become hugely complex systems with about 0.3 million logic blocks andthousand I/Os [22].

Every FPGA must depend on a particular technology that controls its programmable switches to achieve programmability. The programmable logic architecture depends on these programming technologies. The basis of SRAM-based FPGA is the static memory cells, and it can be found in devices manufactured by Xilinx, Altera, and Lattice [19]. The primary functions of SRAM cells are to store data in the look-up tables (LUTs) to im- implement logic functions and to be used to drive inter-connect signals by setting the select lines to the multiplexer. LUT is typically a truth table that provides the O/Ps for different combinations of inputs. The main advantage of SRAM FPGA is its versatile nature that can be re-programmed an infinite number of times. But it is volatile meaning that it requires external sources to store data permanently as they will lose all the data once they are powered down. On the other hand, Flash/EEPROM Programming Technologyis non-volatile; they can hold the data even if they are turned OFF. It was made possible using a technology called floating gate where charges were inducedin the gate that floats above the transistor. The problem with EEPROM technology as it cannot be reprogrammed an infinite number of times. The reason behind this was that thecharge build-up in the oxide made it difficult to erase and program the device [23]. Anotherprogramming technology that used flash storage along with the SRAM programming was used to provide non-volatile storage for the SRAM cells.

This overcame the problems suchas the volatile nature of SRAMs and the necessity to make a choice between infinite timesof reprogramming or permanent storage of configuration data. Since this flash-based technology is based on pure SRAM technology it is like SRAM in working but requires more area to operate.

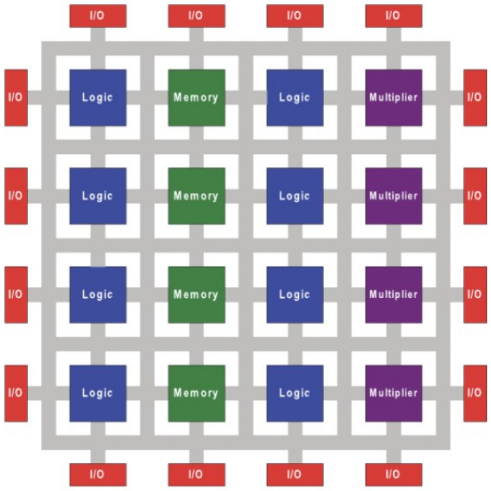


Figure 1.3: Basic Structure of FPGA [1]

Anti-fuse programming technology uses anti-fuses, and as the name suggests it works in a way opposite to that of fuses. These elements are used in transmitting FPGA signals. Un- like, SRAM these are not re-programmable, and they can be programmed only once in their lifetime. There are two approaches to implement anti-fuses. One among them is dielectric anti-fuses, in which a dielectric made of oxide-nitride-oxide is placed between polysilicon and N+ diffusion [24]. When a source of high voltage is applied the dielectric eventually breakdown paving a new conductive link that offers a resistance of 100-600 Ohms. The dielectrics were replaced by metal-metal anti-fuses in which an insulating material made up of silicon oxide [25] or amorphous silicon [26] is placed between to metal layers. The advantage of these metal-metal anti-fuses is they have a resistance of 20-100 Ohms. The main disadvantage of anti-fuse technology is that it is not re-programmable which makes it not suitable for systems requiring constant configuration changes. Comparing the above-mentioned technologies SRAM is dominating FPGA manufacturing. Not all technologies satisfy all the requirements but the key reason for SRAM dominance is that it uses standard CMOS technology for production. The table 1.1 shows the summary of the properties of the programming technology [19].

Table 1.1: Summary of the properties of the programming technology

Properties	SRAM	FLASH	ANTI-FUSE
Volatile	Yes	No	No
Re-programmable	Yes	Yes	No
Storage area required	High	Intermediate	Low
Manufacturing Method	CMOS	FLASH	Requires special development

In the early 80s, Application-specific integrated circuits (ASICS) were manufactured by many companies and had fierce competition on the market due to their high speed and high performance for a comparatively low cost. Though FPGAs were relatively poor compared to these advantages of ASICs they have thrived in the market to date. The reasons behind this were the fact that ASICs required a high up-front non-recurring engineering cost compared to FPGA at some specific level of volumes. The other advantages of FPGA over ASICs were that they were readily available in the market and low failure rate. Despite thorough simulations, it was nearly impossible to make an ASIC work on the first try. On the other hand, FPGA can be reworked easily and there was no need for extensive simulations [27]. FPGAs provide the possibility of working independently as they can be tailored exactly to your project requirements. With FPGAs, the development of prototypes can be faster as troubleshooting can be done along with development. It is common to use software implementations with high-speed processors, but FPGA provides a cost-effective method via parallelization and adaption to the use. It also provides a comparatively good speed advantage over processor-based solutions. Due to the flexibility of FPGA, it requires a shorter time to carry out complicated calculations. Finally, with the advancement in engineering, the amount of data to be processed is increasing steadily, and with the help of parallel processing of data provided by FPGA it can be made possible and carried out in a shorter period.

1.3.3 Ultrasonic Transducers

A device that can convert one form of energy to another is known as a transducer. Ultrasonic transducers can convert electrical energy into mechanical energy inthe form of sound waves and vice versa. A typical ultrasonic transducer consists of active elements, wear plates and backing. Active elements are made up of piezoelectric materials and can convert electrical signals produced by a pulser device into ultrasonic sound energy and vice versa. The purpose of adding a wear plate is to protect the transducer elements from various environmental conditions. Wear plates used in contact transducers should be wear-resistant as they will be used against hard materials such as steels, etc. Wear plates also act as an acoustic transformer in immersion, delay line and anglebeam transducers to equal the large acoustic impedance of the transducer active elementand the small acoustic impedance of the water, delay line or the wedge. The transducer vibration is controlled by grasping the energy radiated from the backside of the active element by the backing which is made of high-density material [28].

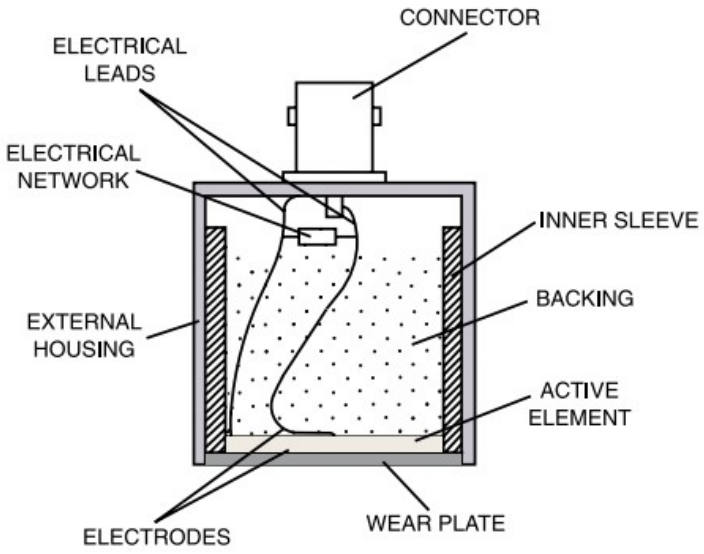


Figure 1.4: Main components of Ultrasonic transducers [29]

Transducers can be classified into 2 types based on their applications. For direct contact inspections, contact type transducers are used which are hand manipulated. A rugged casing is used to cover and protect the active elements of the transducer to withstand the sliding contact with various materials. The ergonomic design of these transducers provides the ease to handle and slide it along the surface of the materials to be inspected. To increase the lifetime of these transducers wears plates are designed to be replaced periodically depending on the amount of wear. The air gap between the transducer and the testing material is eliminated using couplants such as water, grease, or commercially available materials etc. Another type of transducers is the immersion transducers which do not have any direct contact with the materials to be tested. Their connections are well sealedas they are made to work in a liquid environment. As mentioned earlier these transducers must wear plates that act as the impedance matching layer to facilitate large amount of sound energy entering the water, in turn, more into the material being tested. Immersion transducers are available in 3 different configurations, namely flat or unfocused, spherical,and cylindrical. Focusing is achieved by using a lens or by designing the element in a curved shape. Flat immersion transducers are commonly used in inspections of thick materials. To improve the detection of small flaws spherically focused immersion transducers are used and cylindrical focusing is used in tubing inspections [29].

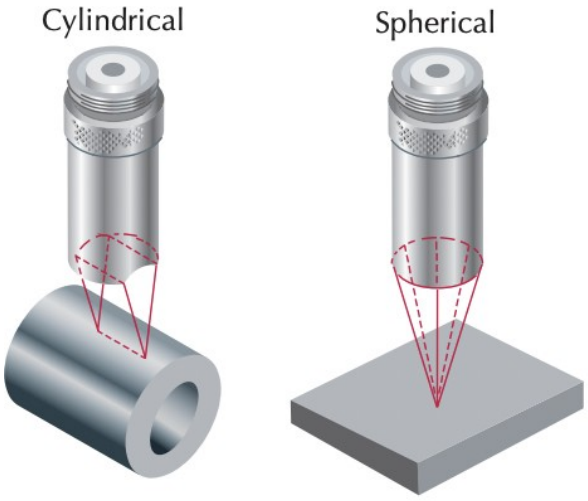
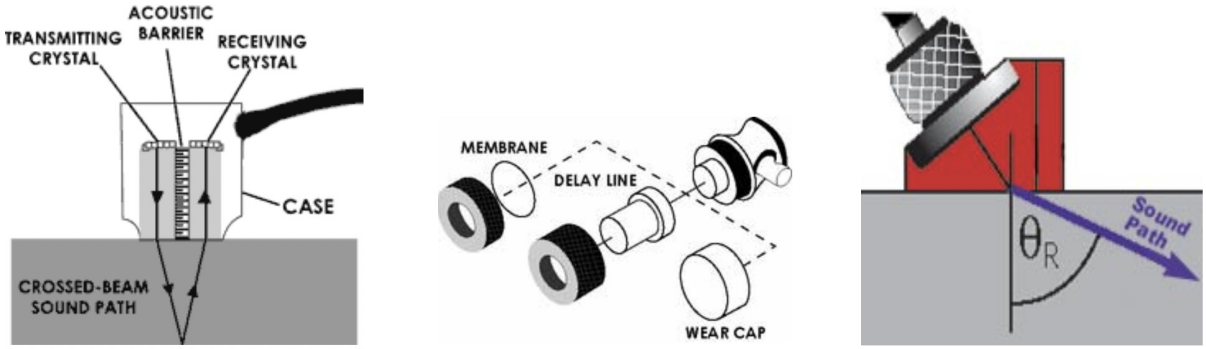


Figure 1.5: Types of Immersion Transducers [29]

Contact transducers are available in different configurations for various applications. Dual element transducers have two different elements for transmitting and receiving ultrasonic signals. These transducers have a crossed-beam path of sound waves which is achieved by positioning the dual elements at an angle to each other. This type of contact transducer is used to measure the thickness of thin materials and to find the near-surface defects. Delay line transducers can make a single transducer effective for various applications. The main function of this type is to provide a time signal between the transmitted sound wave and the received signal. This helps in achieving improved surface resolution and these types of transducers are used in measuring the thickness of thin materials and in composite materials for de-lamination checks. Since it can provide some protection to the active element from the heat it can be used in high-temperature applications. Angle beam transducers are used to introduce refracted shear waves into the test material by using the principles of refraction and mode conversion. These transducers are used to find the flaws that are situated non-parallel to the test surface (i.e., welded joints) [10].



(a) (b) (c)

Figure 1.6: Different types of contact Transducers – (a) Dual Element Transducer, (b) Delay line Transducer, (c) Angle beam Transducer [10]

As mentioned earlier UT introduces high-frequency mechanical waves into the specimen to gather data about the object without altering it. The time of flight and the amplitude of the reflected wave are two basic quantities measured in UT. The thickness of the material (T) can be calculated with the velocity (c) and the round-trip time (t) taken by the sound wave to travel through the material [30].

$$T = (c * t)/2 \tag{1.1}$$

The sound field of a transducer can be divided into the near field and the far-field. The sound produced by a piezoelectric element does not start at an individual point but forms from a large area of the active element. The sound wave intensity is affected by a series of constructive interference and destructive interference which in turn leads to extensive fluctuations in the intensity of the ultrasonic wave produced by the transducer near the origin and this region is known as the near field. The far-field is the region beyond the near field where the ultrasonic waves emanated by the transducer are relatively uniform. The natural focus is the distance at which the change between near and far-fields takes place. The near field distance can be calculated using the formula [29].

$$N = (D^2 * f)/(4 * V) \tag{1.2}$$

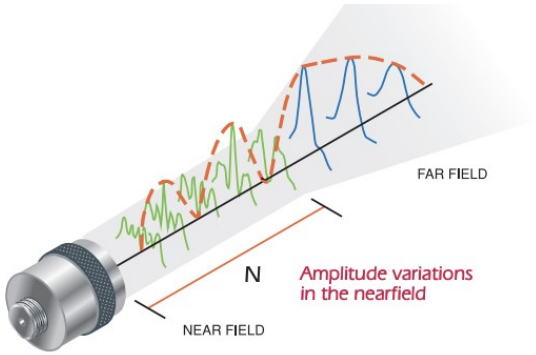


Figure 1.7: Sound Field of an Ultrasonic Transducer [29]

All ultrasonic beams diverge. In other words, ultrasonic beams undergo beam spread. It is the measure of the angle of the beam in the far-field from side to side and beam divergence is the measure of the angle between the center axis of the beam and one side of the beam in the far-field. Also, the beam spread is twice the value of beam divergence. Beam spread is affected by the diameter and the frequency of the ultrasonic transducer. For a flat transducer, beam divergence angle theta can be calculated by

$$Sin\ A = (1.2 * V)/(D * f) \tag{1.3}$$

where V is the material sound velocity, f is the transducer frequency and D is the diameter of the transducer [30].

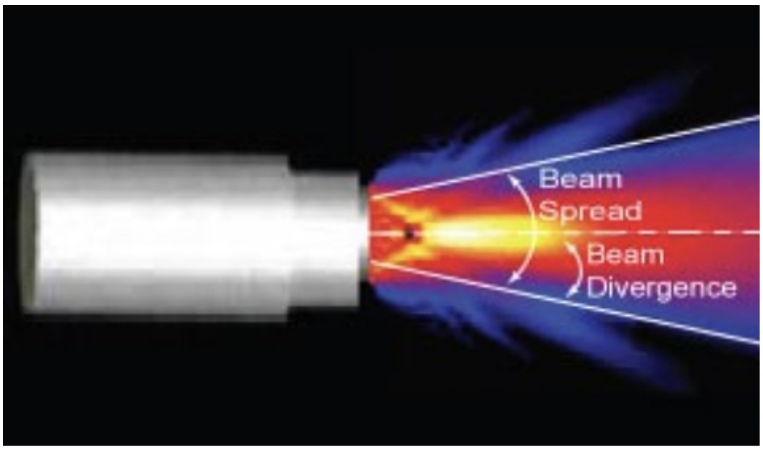
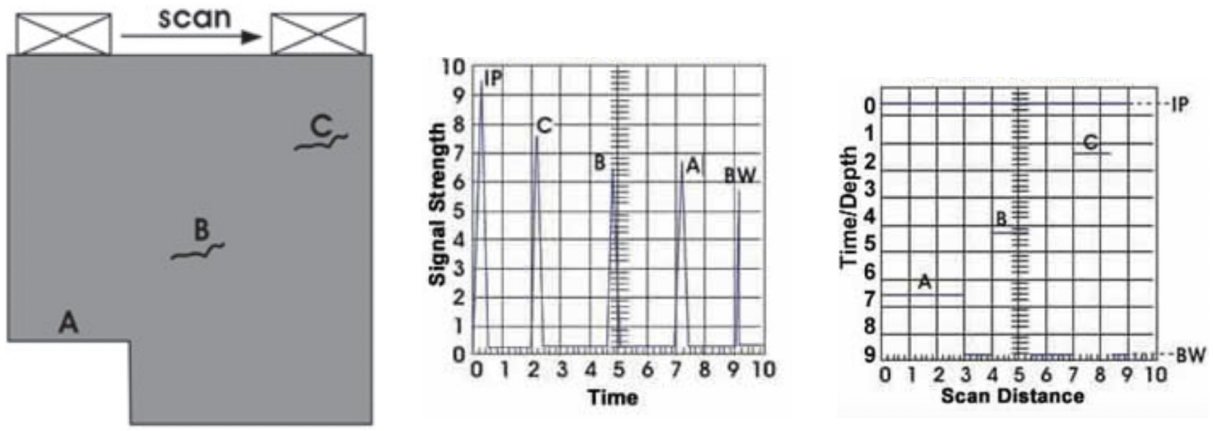


Figure 1.8: Beam spread and Beam divergence of a transducer [10]

1.3.4 Data Representation

There are several formats to display the collected ultrasonic data. The most common formats are A-scan, B-scan, and C-scan respectively. Each presentation provides a unique way to look at and evaluate the material being tested. A-scan is a plot between time and the amount of ultrasonic energy received. The ultrasonic energy received is plotted on theY-axis and the time is plotted along the X-axis. Most of the commercial devices display thereceived signal in its natural radio frequency (RF) form, RF fully rectified signal, also the negative or positive half of the RF signal. The figure shows an example of an A-scan. The IP represents the initial pulse at the start of inspection. When the transducer is positionedon the far-left side only the Initial pulse and the reflected signal from A will be visible in the A-scan. As moved along the surface towards the right side, BW, the signal from the back wall will be visible later in the time scale showing that the sound has travelled a longdistance. On moving forward, signal B is visible in the time scale between IP and BW. AsIP represents the front surface it can be concluded that flaw B is present halfway betweenthe front and back walls. When moved over point C, signal C will appear sooner as it isnear to the front surface and the sound wave has travelled a shorter distance [10].



(a) (b) (c)

Figure 1.9: Data representations of UT – (a) Testing component, (b) A-Scan, (c) B-Scan [10]

To have a cross-sectional view of the material B-scans are used. Along the vertical axis, the travel time of the wave is plotted, and the transducer's linear position is plotted along the horizontal axis. With the help of the B-scan, the linear dimensions of the defect along the direction of the transducer and the vertical distance from the front surface can be identified. By producing a trigger gate on A-scan the presentation of B-scan is produced. Whenever the gate is triggered by a high-intensity signal, a point is plotted in the B-scan. Also, the triggering of gate happens due to the sound waves reflected from the back wall and produces lines that are like the size of the flaws B and C. Similarly, C-type scans can provide a plan-type visualization of the size and location of the flaws. An automated data acquisition system is required to produce C-scans. A gate for collecting data is provided on the A-scan and the amplitude is noted when the transducer is moved along the specimen at regular intervals. The recorded amplitude signal is presented as a shade of grey or a different color for the positions at which the data was gathered. These are the three different presentations used widely in NDT [30].

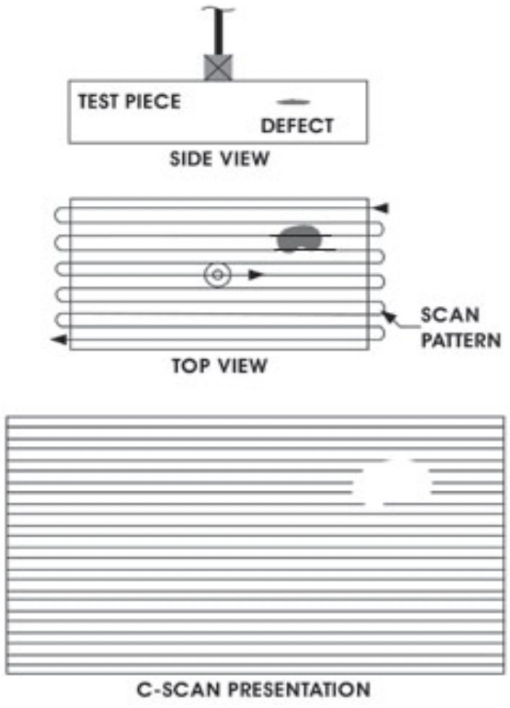


Figure 1.10: C-Scan Representation [10]

1.3.5 Commercially Available Ultrasonic NDT systems

There are many commercial ultrasonic testing systems available today. Olympus a Japanese company is one such manufacturer of Ultrasonic systems. They have a variety of systems namely, OMNISCAN X3, EPOCH 650, EPOCH 6LT, OMNISCAN SX and OMNISCAN SX2 [12]. The OMNISCAN series is supported by Pulse-echo ultrasonic testing and phased-array testing. It is a complete phased array toolbox with high image quality to conduct inspections on-site. It has a hard drive capacity of 64 GB extendable using a USB drive. Four UT connectors are available in the system of which two are pulser-receivers. It also has one PA connector. The system has a TFT LCD with a resistive touch screen of size 10.6 inches and 1280x768 pixels resolution. In remote locations, it is powered by a 93W lithium-ion battery with a life of 5 hours using 2 batteries. The EPOCH 650 has a large VGA display for vivid clarity in any lighting conditions. For ease of usage and portability,it has been designed to be lightweight and has a 4-point harness connection for chest straps.It has a dimension of 236 mm x 167 mm x 70 mm with a lightweight of 1.6 kg including a lithium-ion battery. It uses a single lithium-ion rechargeable battery with a running time of 15 to 16 hours. It provides a stable A-scan representation of the inspection using a highdynamic range receiver. The price of these devices is not found on the Olympus site but the cost of a re-furbished OMNISCAN X3 is 50000 USD as of February 2022 [31].

Figure 1.11 Olympus OMNISCAN X3 [12]

Figure 1.12: Olympus EPOCH 650 [12]

An alternative to the expensive ultrasonic devices from Olympus is SIUI from Shantou, China. The SIUI sync scan is a conventional ultrasonic flaw detector that comes in various configurations. The one that is available in Dr. Kwon's AI lab was purchased in 2017 and cost around 5000 Canadian dollars which included a 16-channel phased array transducer. It has an 8.4-inch LCD with a 600x800 pixels resolution touch screen display. It can handle many basic and advanced functions such as angle calibration, A-scan mode, auto freeze, wave screenshot, wave filling and wave comparing. It is also capable of B-scan, crack height measurement, thickness measurement, as well as calibration wizard to facilitate a step-by-step menu for improved accuracy and speed of calibration in phased array testing. It uses a rechargeable lithium-ion battery with a life of 4 hours for phased-array UT applications and 5 hours for pulse-echo UT applications [32].

Figure 1.13: SIUI SYNCSCAN [32]

Figure 1.14: DPR 300 by JSR Ultrasonics [33]

DPR 300 is a commercial-grade ultrasonic pulser/receiver device manufactured by JSR Ultrasonics, a division of Imaginant, New York, USA. The DPR 300 present in the lab can be controlled using a PC. The DPR 300 pulser produces a high voltage electrical pulse which is applied to the T/R connector of the instrument. From the T/R connector through a 50- ohm coaxial cable an ultrasonic transducer is connected to convert this electrical signal into an ultrasonic signal. For a pulse-echo mode of operation, the reflected signal from defects is converted into electrical signals by the ultrasound transducer which then is presented to the T/R connector. These electrical signals are amplified by the receiver of DPR 300 and passed through low and high pass filters.

The DPR 300 can also be used with oscilloscopes in which a synchronization pulse is applied to the trig/sync connector of the DPR to trigger the pulser when it is in external trigger mode. In the

case of internal trigger mode, a short pulse is generated in sync/trig connector in parallel to the high voltage electric signals [33].

1.4 Problem Statement and Research scope

Manufacturing of transducers requires advanced facilities for controlling the process accurately to obtain precision at the sub-micron level. Considering the resources available for the project, the manufacturing of transducers is not feasible. Hence, ultrasonic transducers that are available commercially from SIUI are used for this project. The industrial UT systems are accurate but require trained professionals to interpret the obtained data and itis not a good fit for research. Modifications to the existing commercial devices are expensive and not adjustable. Hence, a new research platform should be developed to overcome these problems.

The advancement in FPGA technology over the decades has facilitated hardware algorithms that can be made more efficient than software realization. The hardware integration has become more effective due to SoC FPGA. Previous studies on FPGA had used it as a multiplexer rather than a processor [6]. The first step towards in-line NDT is the building of high potential FPGA-based research platform.

The objectives of the projects are:

1. Conduct ultrasound testing experiments on the prototype.
2. Compare the test results of the prototype with commercial devices.
3. Optimize the design to improve its functionality.
4. Provide references of the design to the lab for future development.

Chapter 2

Methodology

2.1 Procedure for PCB development

The Analog Front End (AFE) of the Ultrasound testing system developed for this project is made using Printed Circuit Boards (PCB). To develop a PCB from scratch the schematics must be drawn and converted to a PCB layout. This procedure can be done using Ki CAD which is an open-source software tool for developing schematic diagrams and PCB layouts. The workflow of Ki CAD has two major tasks creating the Schematics and laying out the PCB. To Achieve this, it has an inbuilt component library and footprint library. The procedure to develop AFE using Ki CAD is as follows.

1. Creating a new project and organizing all the files in a single folder.

Table 2.1 shows various file extensions available in Ki CAD that are used in this project.

Table 2.1: Various file extensions available in Ki CAD

File Extension	Description
*.pro	Ki CAD project file
*.sch	Eeschema Schematic file
*.net	Eeschema Netlist file
*. kicad_pcb _	PCBnew circuit board editor file
*.gbr	PCBnew circuit board Gerber file

2. Creating a schematic file.

The Schematic file comprises the electronic circuit diagram of the AFE is created using the Eeschema tool. Components can be added from the component library available in Ki CAD. Being an open-source software, many component libraries are available online and Ki CAD also has tools to draw new ones.

3. Generation of Netlist.

To generate the netlist all the components must be annotated in Eeschema. Checking circuit connections, unassigned pins and drivers that are missing can be done using electrical rule checking tool available in Ki CAD.

4. Assigning components with correct footprints.

In an Electronic board, footprints are the patterns that are exactly in the shape and size of the component to be soldered. Footprints of components can be found in the footprint library available in Ki CAD or can be drawn using footprint tools. To draw a footprint of a component its design features can be obtained from the datasheet of the corresponding component. Footprints represent the actual dimensions and pin configurations of a com- ponent like ICs. Incorrect selection of footprints can cause electrical shorting in the PCB making it useless. Hence, a designer needs to be careful while assigning a footprint in Ki CAD.

5. Layout Printed Circuit Boards.

Ki CAD tool PCBnew is used for laying out the PCB. The netlist generated is imported in PCBnew and the components will appear on the workspace. The PCBnew file. Kicadpcb is saved and provided to the manufacturer along with the Gerber files for manufacturing [34].

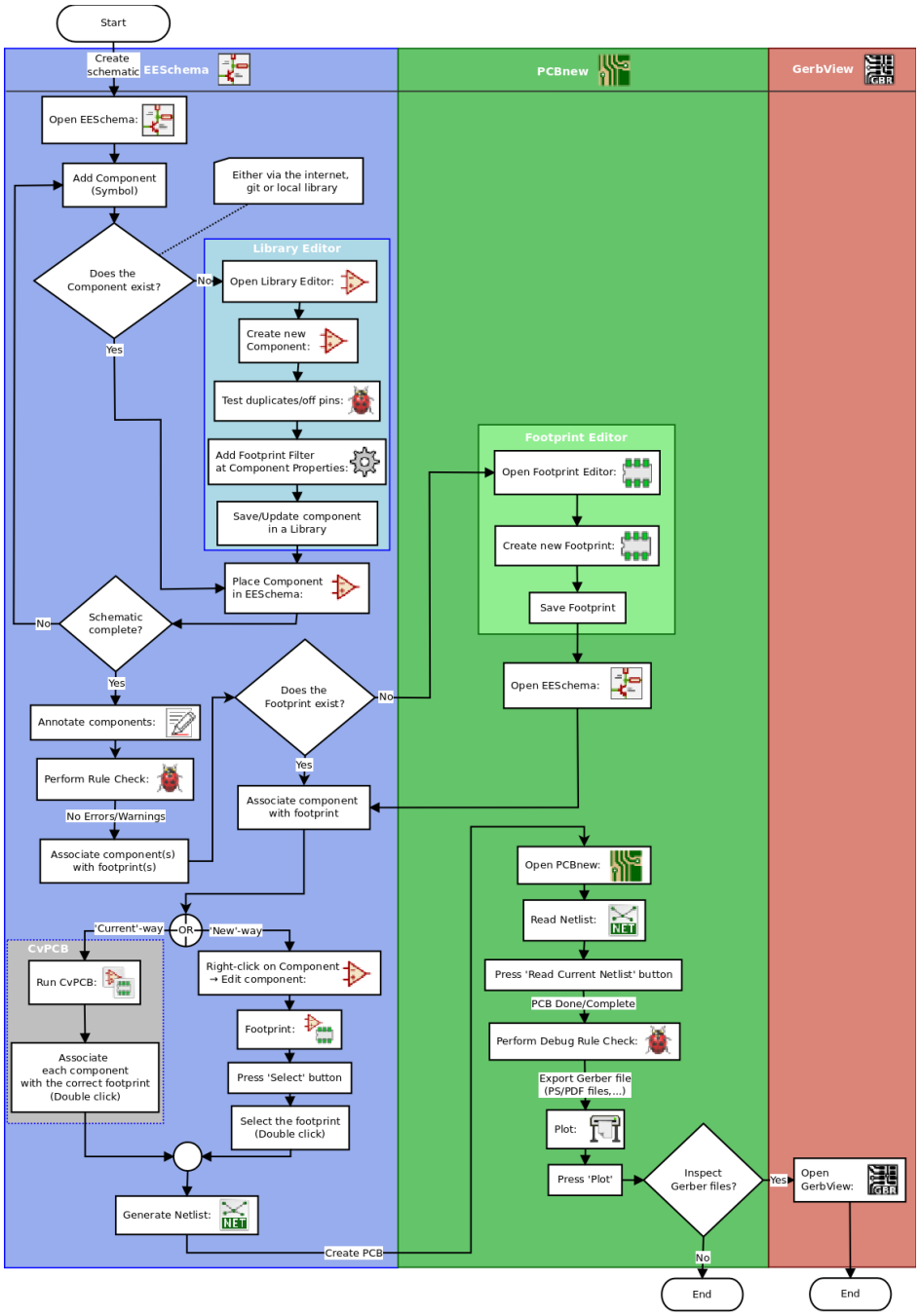


Figure 2.1: Ki CAD Workflow

2.2 Procedure for FPGA development

In this project, a chip manufactured by INTEL named Cyclone V SoC is used. The FPGA development software for INTEL chips is Quartus Prime. Quartus prime has 3 editions namely

pro, standard, and lite. Quartus Prime Pro and Standard versions require paid license whereas the lite edition is free, and no license is required. The Cyclone V chip is compatible with the lite edition and hence it is used in this project. The interface of Quartus Prime lite edition (version 18.1) is shown in the Figure 2.2.

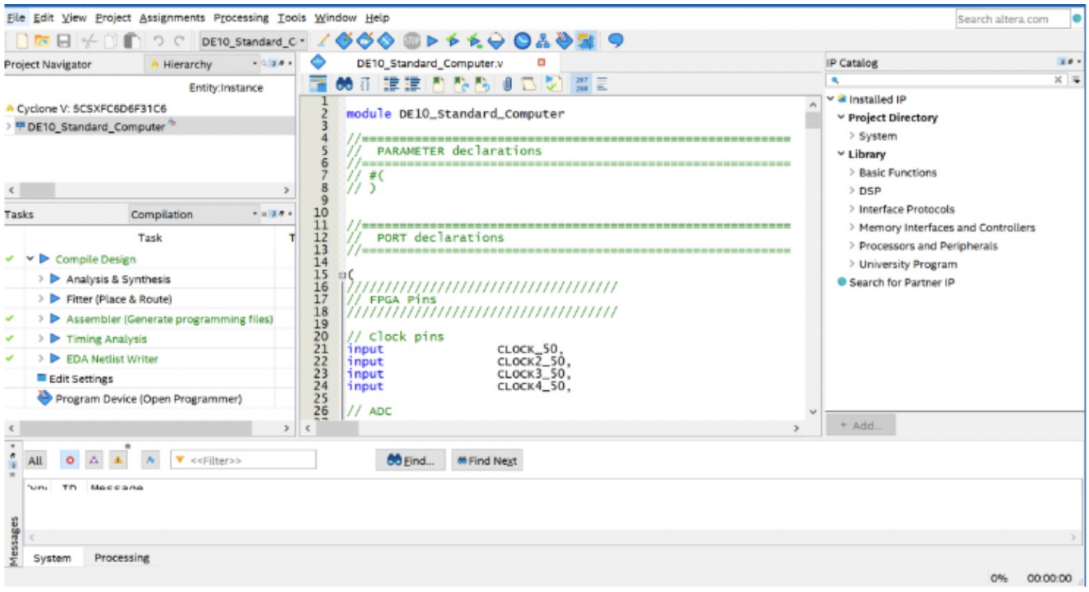


Figure 2.2: User Interface of Quartus Prime

Quartus Prime helps in organizing the design files and connecting the HDL designs to the required I/O pins, in this case, we used the system builder tool to automatically generate the pin assignments. The compiler compiles the design then circuit and timing constraint optimizations are conducted. The step-by-step procedure for using the software is as follows:

1. Creating a project file and selecting cyclone V chip from the settings.

2. Adding the required HDL files to the project.

3. Establishing a connection between Hard Processor System and FPGA using Platform Designer. Generating Top-level HDL template and adding it to the top-level module.

4. Compile the design and start to debug from the error messages displayed. Figure 2.3 shows the Quartus Prime design flow [35].

5. Load the .sof file generated after compilation by the assembler module to the FPGA hardware using the Programmer tool. Table 2.2 shows various design file extensions used in Quartus Prime [36].

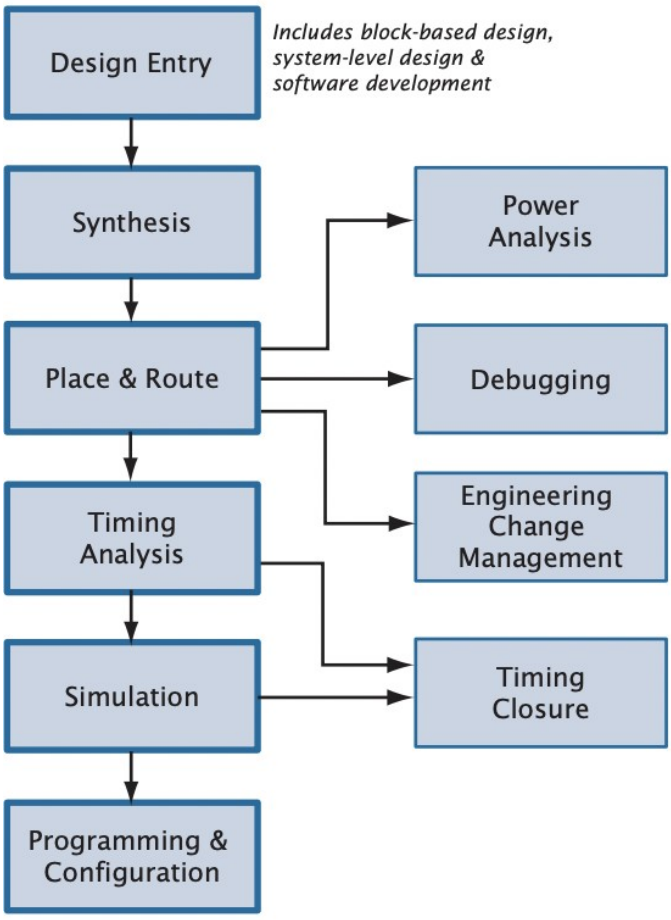


Figure 2.3: Quartus Prime design flow

Table 2.2: Various file extensions available in Quartus Prime

File Extension	Description
. v or .vhd	Verilog or VHDL file
. qpf	Project File
. sdc	Synopsis Design Constraints file
. sof	SRAM object file
. htm	Pin assignment

Chapter 3

FPGA based Ultrasonic Testing

3.1 Introduction

The two main objectives in developing FPGA-based UT are hardware engineering and software development. There are 4 key components in hardware engineering. The ultra- sound probe, the Analog Front End (AFE), AD/DA interface and the FPGA controller are the four key components in the hardware engineering part of this project. These four components are further divided into analog and digital parts, where probe and AFE fall under analog parts of the system. The system requires probes that work with specified frequencies, hence commercially available SIUI probes(P10-10L) are used in this system. The AFE was built from scratch, starting from creating electronic diagrams in Eeschema to laying out the board in pcbnew tool provided by KICAD software. The corresponding *. kicad_pcb file can be sent to the manufacturer for manufacturing the PCB. It is important to mention that the ultrasound FPGA project developed by Y Qian [6] from Dr. Kwon's lab was very inspiring in the initial stages of designing. The final version of the PCB is presented in the thesis and was manufactured by Bittele Electronics, Ontario.

The digital parts of the system include the DE10 standard board carrying the SoC FPGA, and its daughter card AD/DA interface THDB-ADA are used. They are commercially available and manufactured by Terasic (China). The great advantage of FPGAs is that they can be reprogrammed. Hence the digital circuit was programmed using Verilog HDL. An algorithm developed by Y Qian [6] for pulse detection was implemented in this project in the FPGA to access the direct data from the Ultrasonic system. In the software system, C language is used to code the system. It can provide a user interface, display details about the pulser frequencies and provides data saving options to the user. It runs on Linux installed on the SoC that is supplied with power by the ARM processor of the system.

3.2 Digital parts of the hardware system

The digital parts include DE10 Standard, and THDB-ADA manufactured by Terasic Technologies (China). The DE10 standard development board is a part of the University program organized by Intel hence it comes with many tutorials and guides for beginners. It also includes educational videos on the FPGA development platform Quartus Prime which helped in developing the system for this ultrasound project.

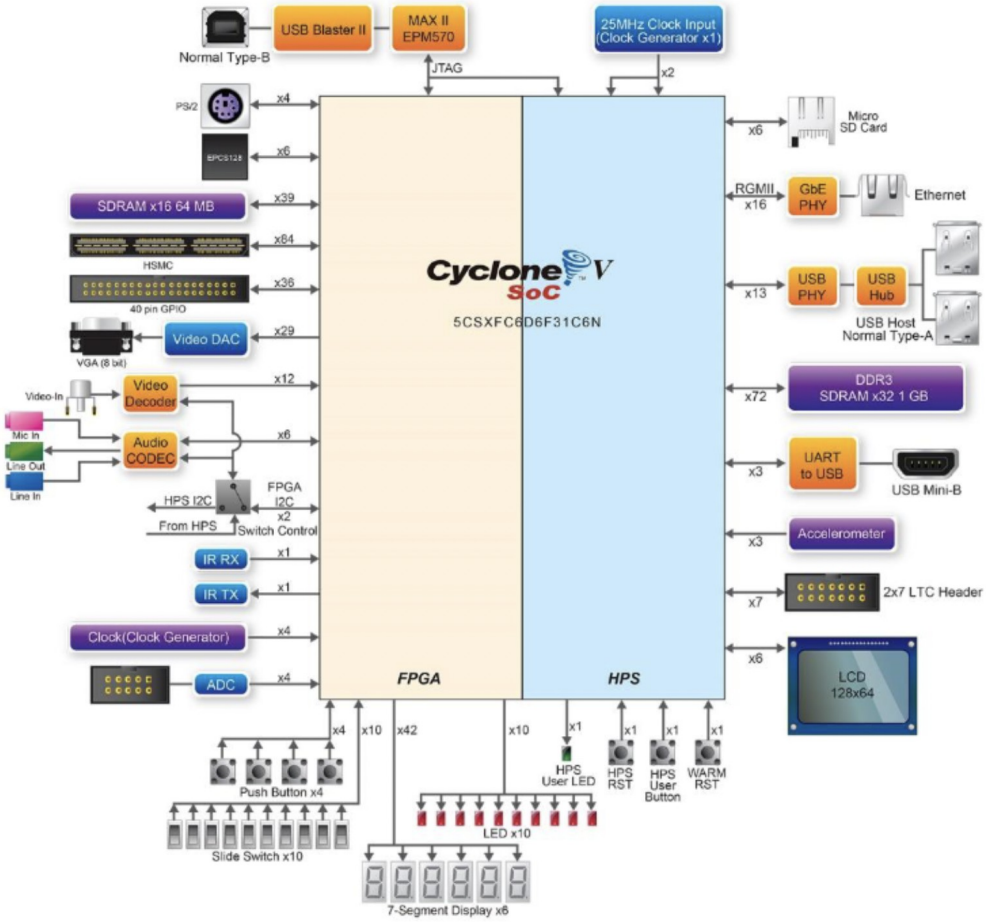


Figure 3.1: DE10 Standard block diagram [36]

The DE10 standard development board has many features that allow the users to create both simple and complex multimedia projects. Intel Cyclone V SoC is the core of the DE10 development board. Along with the SoC, it also provides the dual-core A9 ARM cortex processor. The chip's core is split into HPS and FPGA which are connected through high bandwidth interconnect backbone. The board includes hardware such as video and audio capabilities, high-speed DDR3 memory, Ethernet networking, and a lot more. Figure 3.1 shows the block diagram of the board.

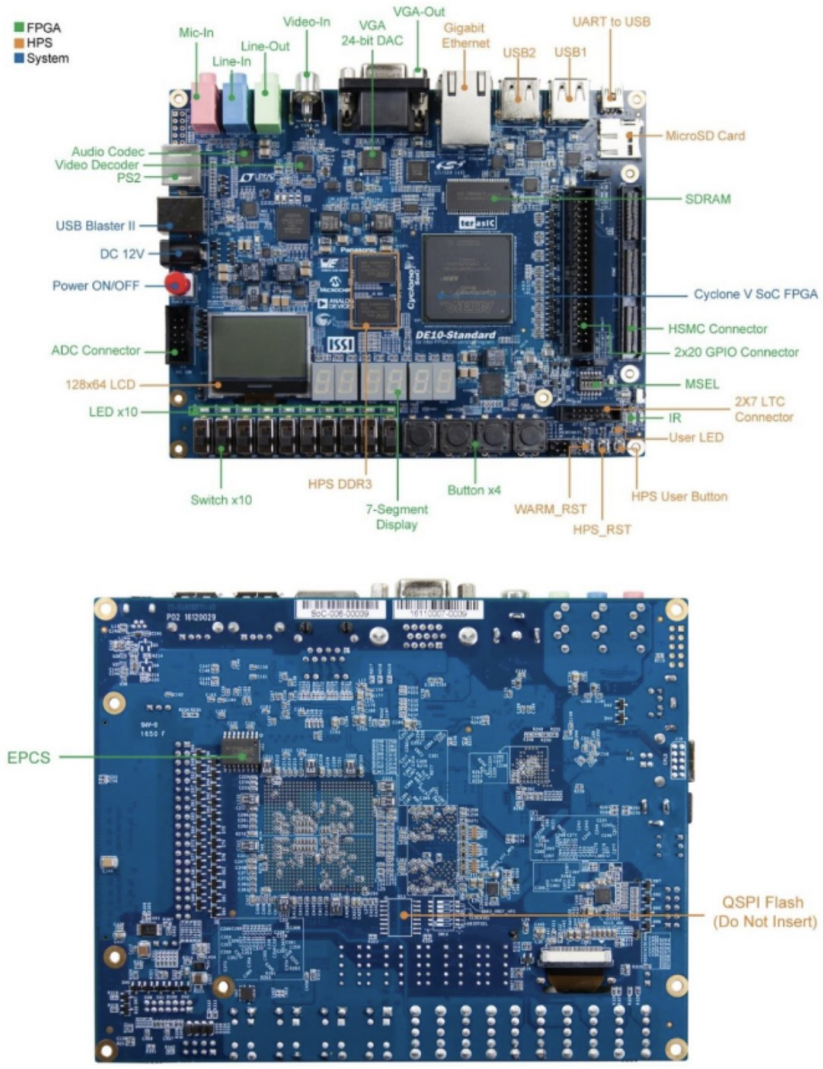


Figure 3.2: DE10 Standard Board Top and Bottom View [36]

In Figure 3.2 the layout of the development board is shown [36]. It can be noted that the DE10 standard board has a High-Speed Mezzanine Card (HSMC) connector through which the THDB-ADA AD/DA interface is connected to the board.

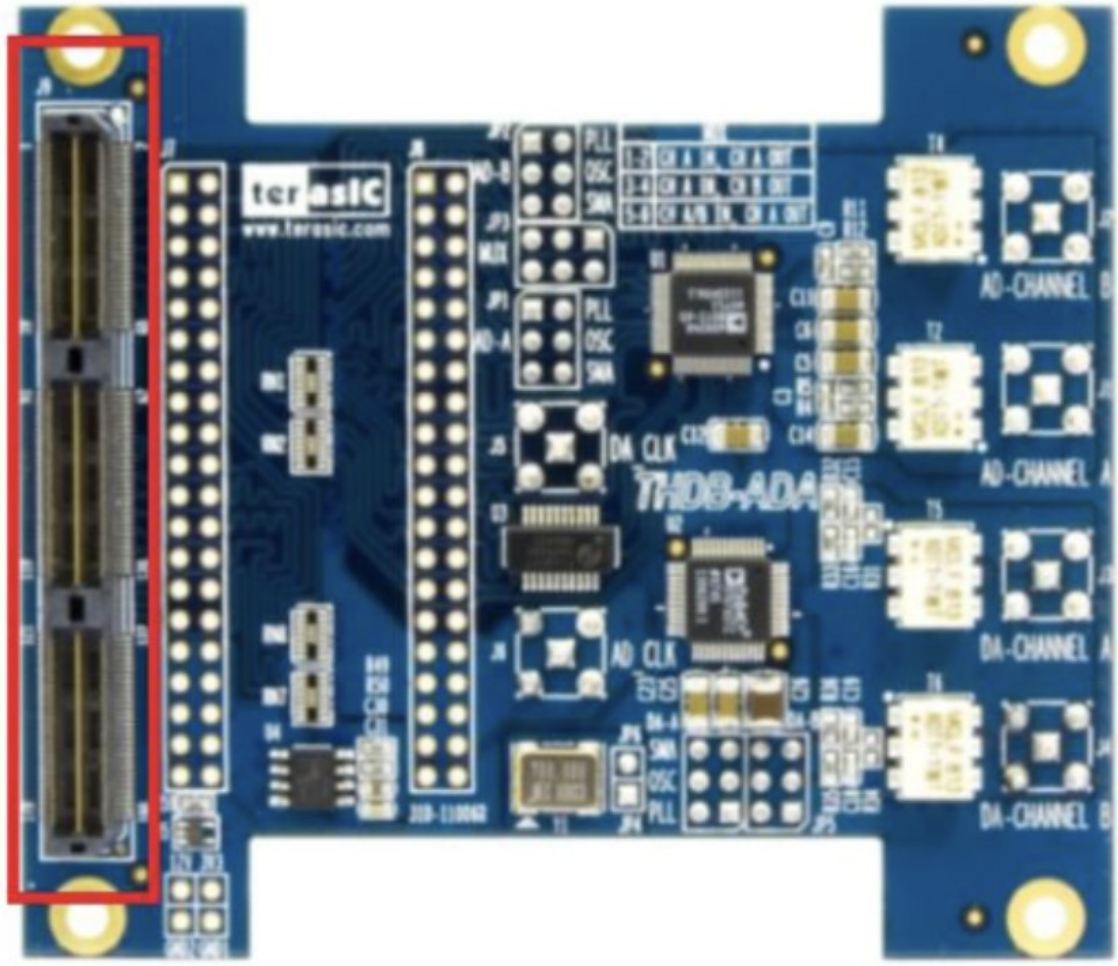


Figure 3.3: THDB-ADA AD/DA interface with HSMC connector marked in red color [37]

Though the DE10 board has its own 8 ADC channels with 12-bit precision it has a low sampling rate of 500 Ksamples/s. Whereas THDB-ADA has dual AD/DA channels with fourteen-bit precision and a sampling rate of 65 MSPS. Hence THDB-ADA is used in the ultrasonic system to achieve higher sampling rates.

To make the pin assignment step in the Quartus Prime software, a board-specific system builder tool is provided by Terasic. Figure 3.4 shows the interface of the DE 10 standard system builder interface. From the figure, it can be noted that the GPIO and the HSMC reader are included in the pin assignment. GPIO and HSMC are selected to send pulse signals to the analog front end and to connect the THDB-ADA with the board respectively. A .qsf file will be generated with the corresponding pin assignments and a timing constraint file with the. sdc extension is also generated.

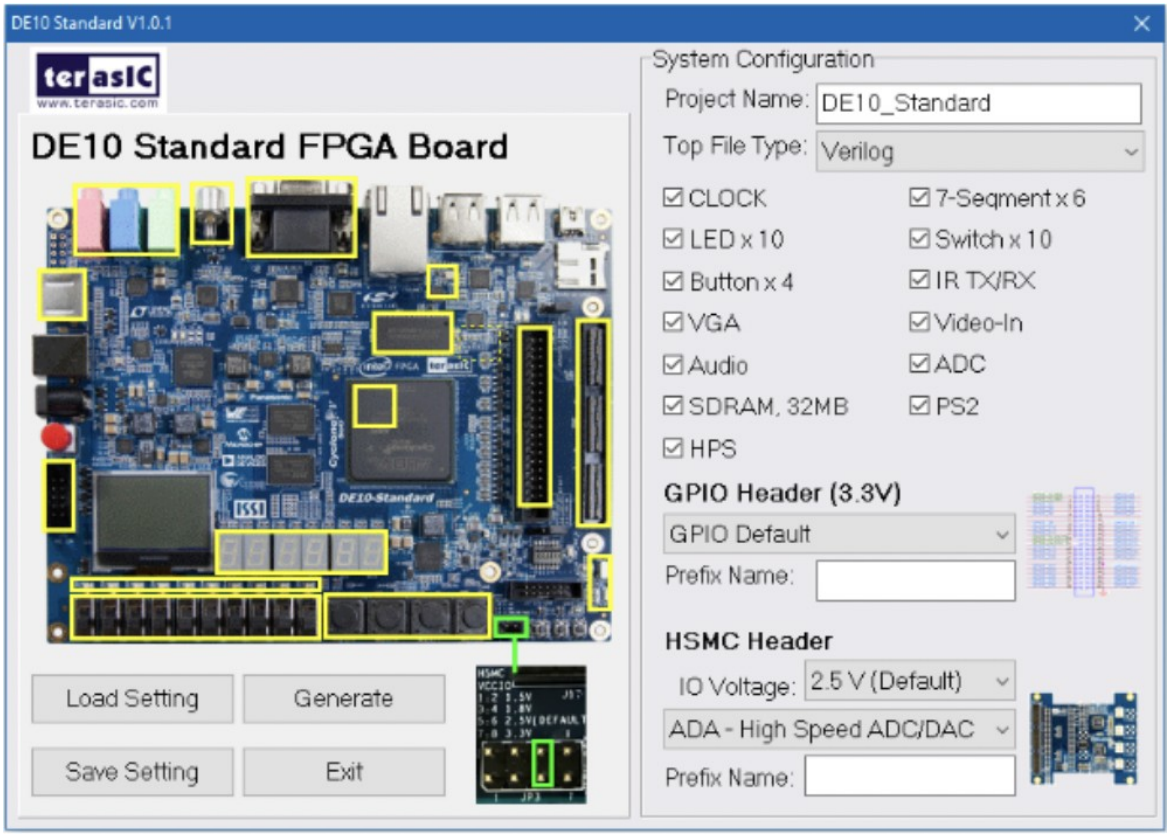


Figure 3.4: System Builder User Interface

3.3 Analog Front End

The initial design of the Analog front end was adopted from Y Qian [6] and improvised for this project. The electrical circuit was created using the Eeschema tool provided by Ki- CAD. The design files were sent to Bittele Electronics for manufacturing the PCB including all the components being soldered on the board. The analog front end of the system is very important as it directly affects the quality of the signal generated. The circuit design and the components used in the design will be explained in this section and data sheets are available for each component to refer to their technical specifications.

3.3.1 24V to 12V Conversion Circuit

The main power supply for the PCB is 24V DC and this 24V is converted to 12V to power the development board. The 24V to 12V conversion circuit is shown in figure 3.5. The 24V DC voltage source is supplied to TPS40170RGY which is a controller used to step down the 24V input to 12V. The design for this conversion circuit was inspired by the datasheet of TPS40170RGY [38]. The 12V is supplied to a voltage regulator UA7505CKTTR to obtain a 5V voltage source to supply power to the remaining circuits.

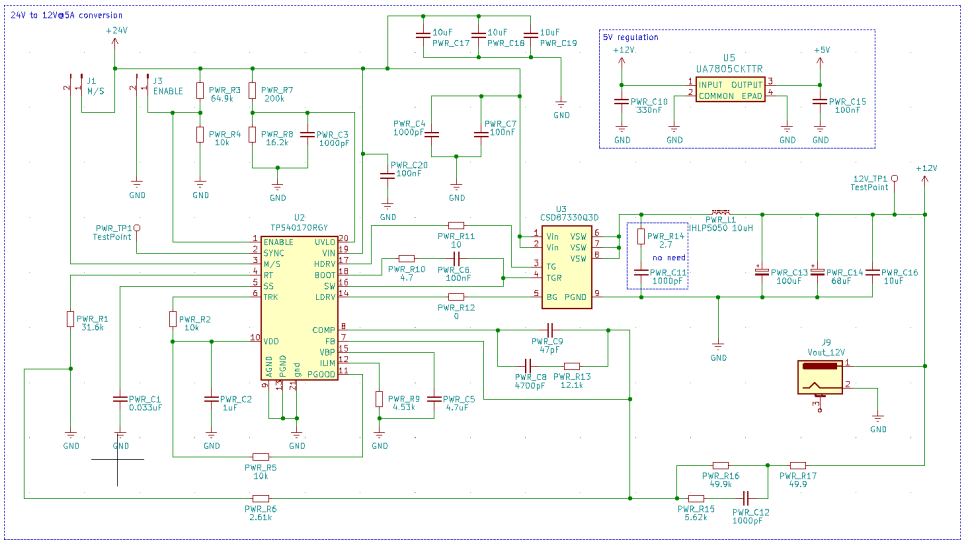


Figure 3.5: 24V to 12V conversion circuit

3.3.1 High Voltage Generation Circuit

The conversion of 24V to 100V is done by the high voltage generation circuit to send high voltage pulses to the transducer as they are known to provide excellent results with high voltage pulses. The main component of the circuit is the LM3481 high-efficiency controller for boost converters. A boost converter requires a low-side N-FET as its primary switch. LM3481 is capable of being operated at high switching frequencies between 100KHz to 1MHz [39]. A low-cost operational amplifier TLV171DBVR is used in this circuit that has a working range of 2.7V to 36V [40]. 100 nF capacitor is placed close to the power supply pins to prevent errors due to the impedance from high power supplies.

A transformer from Wurth electronics is used which can convert 24V to +100V and -100V. The transformer has a turn ratio of 5.5:1 for converting 24V to 100V at 125 mV [41]. From the transformer, the high voltage positive and negative signals are sent to the pulse generation circuit for generating the required high voltage pulse with the help of MOSFET gates which is explained in section 3.2.3. Since the transformer is not a Surface mount device it was hand soldered by placing it at its footprint having 10 pin slots and soldering it to the bottom of the PCB.

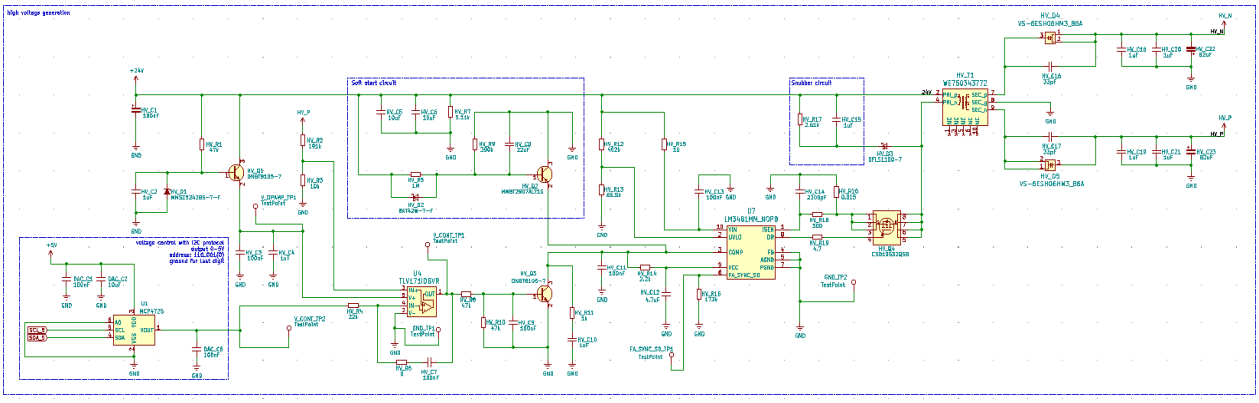


Figure 3.6: High Voltage Generation Circuit

3.3.2 Pulse Generation Circuit

The pulser generation circuit is shown in figure 3.6. Pulsing is achieved using a MOSFET gate in this AFE design. The high voltage pulses can be produced by activating the MOSFET gates at certain frequencies. In this design MD1213, a high-speed dual MOSFET driver is implemented that has its operating conditions between 0.5V to 13.5V with a 6 ns rise and fall time with a load of 1000 pF [42]. The FPGA through its GPIO pins provides the initial pulses to the AFE. For a digital high FPGA, GPIO works at 3.3V and it falls inside the rated voltage range of the MOSFET driver used.

The positive and negative pulses are sent to MD1213 through the GPIO pins by the FPGA at correct intervals, but MOSFET gates are required to give bipolar signals. The reference design suggested in datasheet [42] of MD1213 required to use TC6320 MOSFET gate. TC6320 MOSFET gate has its main application in high voltage pulsers and has a drain to source breakdown voltage of 200V. Hence the recommended pulse generation voltage cannot exceed 200V. The purpose of 2 diode rectifiers BAV23A and BAV23C are to isolate the +Ve and -Ve voltage signals.

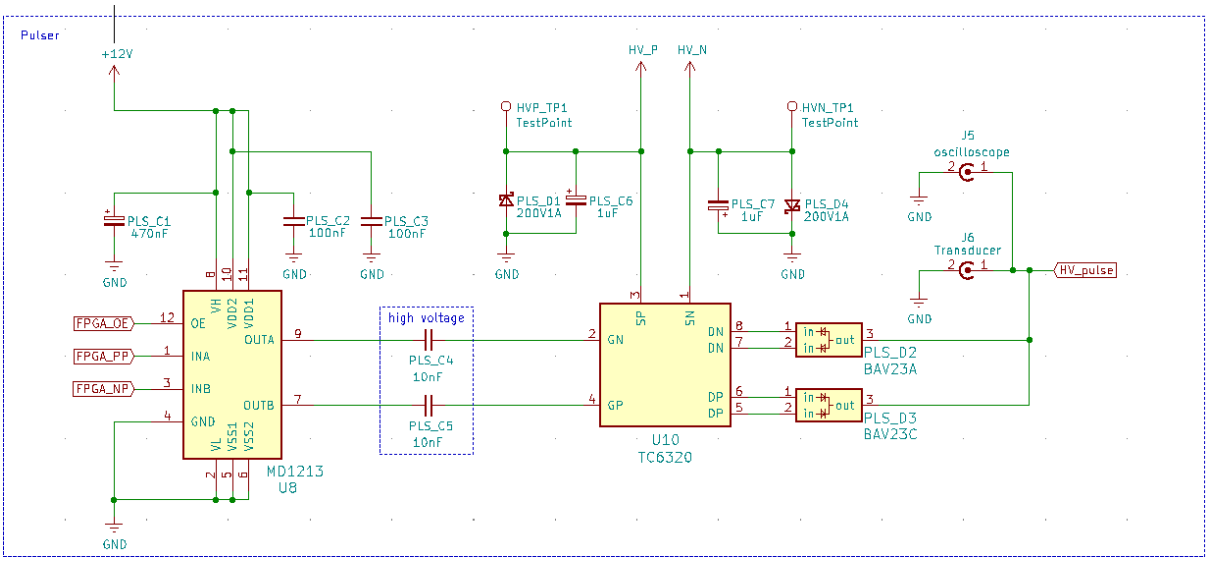


Figure 3.7: Pulse generation circuit

3.3.3 Low noise and variable gain amplifier

The magnitude of high voltage pulses given to the probe is around 100V, but the echo signals are low voltage pulses of magnitude 0.01V. To isolate the high and low voltage pulses a T/R switch was implemented. MD0100 a single/dual channel high voltage protection T/R switch that has a 100V input voltage protection is used in this design [43]. The high voltage pulse was sent to the ultrasound transducer through a BNC connector and the received echo pulses pass through MD0100. Before sending the pulse for amplification it is sent through two oppositely connected diodes BAS16 that acts as a voltage clipper that permits a maximum voltage value of 1.25V to pass through it to protect the remaining components. The amplification is carried out by using AD8331 ultra low variable gain amplifier. By activating maximum gain setting provided by the chip a gain of 55 dB can be achieved [44]. It is important that the amplified signal reaches the receiver end with the same voltage value. To achieve this a RF transformer T1-6T-KK81+ is used for impedance matching and has a wide band of 0.015 to 300 MHz [45].

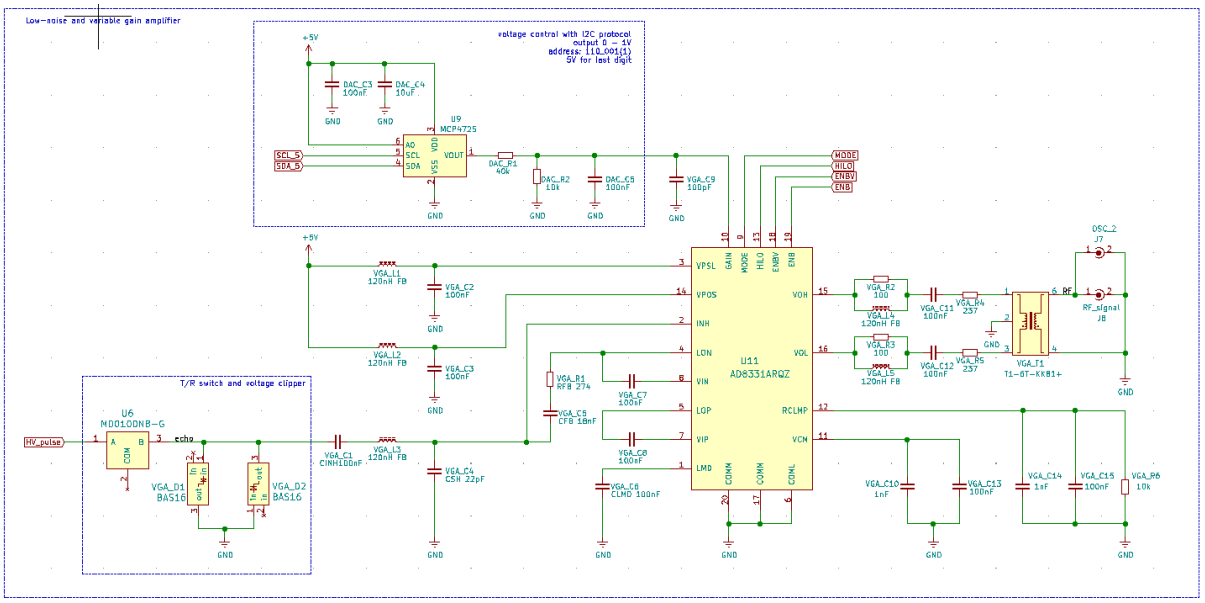
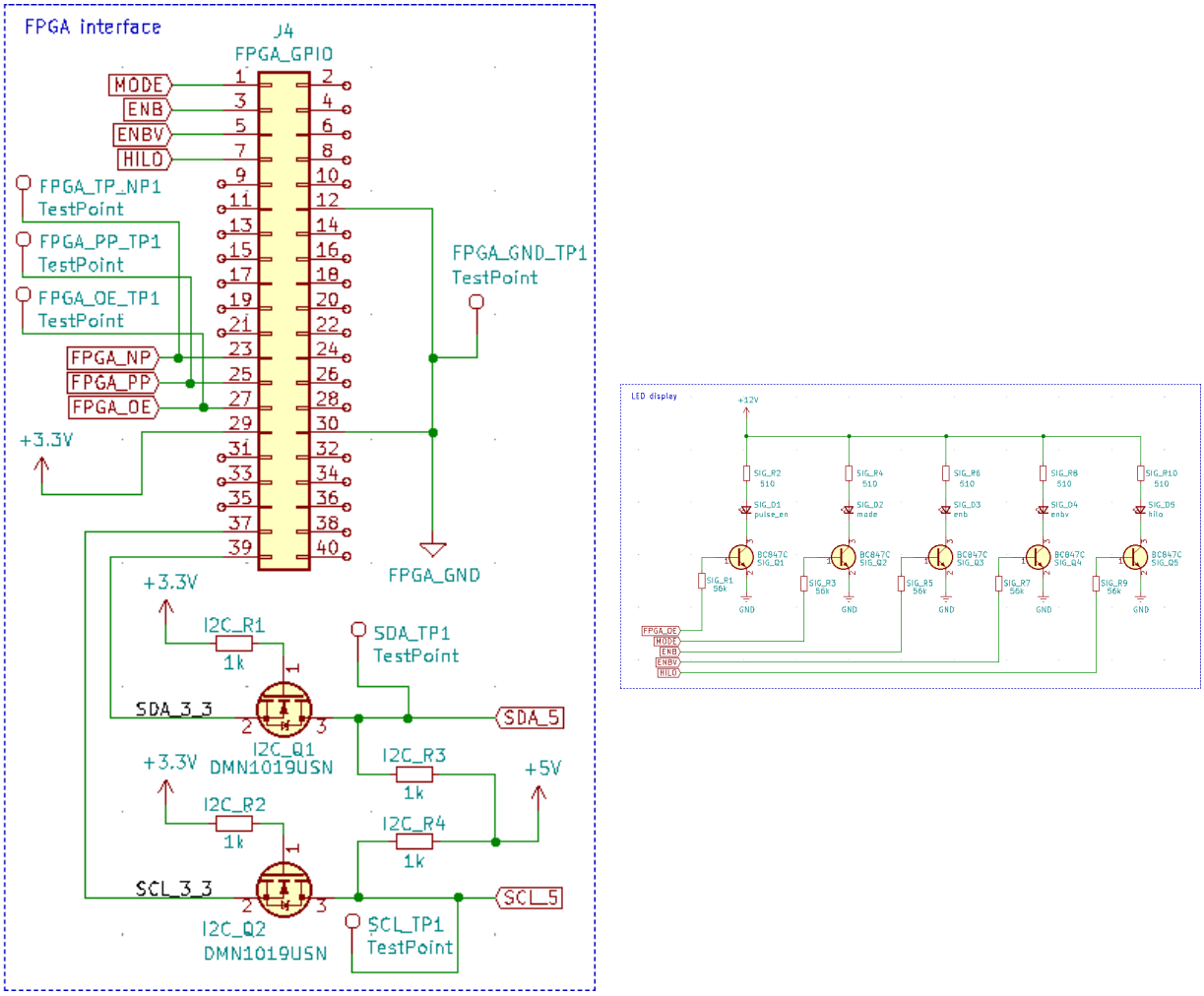


Figure 3.8: Low noise and variable gain amplifier circuit

3.3.4 FPGA Interface and LED Display

Figure 3.9 (a) shows the FPGA GPIO pins connector interface in which a 40-pin position connector header is used in the AFE to connect the FPGA. Figure 3.9 (b) shows an LED display having 5 LEDs that indicate the power supply to 1,3,7,9 and 27 pin positions of the FPGA GPIO pins by lighting up when the power supply is turned ON.



(a) (b)

Figure 3.9: (a) FPGA Interface Circuit, (b) LED Display Circuit

3.4 PCB Layout

After completing the schematic of the AFE using the pcbnew tool provided by Ki CAD the PCB layout was made. Once it was arranged in the most efficient way it was sent to the manufacturer. Bittele electronics in Markham, Ontario manufactured the PCB and soldered all the components onto the board. Since the components were soldered by the manufacturer the shortcomings of hand soldering were eliminated. Most of the components used were Surface Mount Devices that make the board compact. The board was designed to be fitted over the FPGA development board for portability. A protector glass for the components was screwed to the development board. Slots were designed at 4 corners of the PCB to fit the screw slots available on the board. The PCB was placed right above the protector glass and screwed to board along with the protector glass. Since the protector glass was designed in a way to give access to all the switches, buttons and ports placing the PCB caused no trouble in accessing the peripherals of the board.

The manufacturing process includes sending the Gerber files and drill files to the manufacturer. These files are sufficient for the manufacturer to manufacture the board. For the components to be soldered, a bill of materials must be generated and sent to the manufacturer. Each component to be solder has its footprints which can be found in the footprint library provided by Ki CAD, or many online libraries are available for the unavailable footprints. Since the component to be soldered must be physically placed over these footprints, incorrect footprints can cause electrical shorting to the board which makes the board practically unusable. To avoid this the footprints of each component, must be verified multiple times before proceeding to manufacture. For a few components footprint won't be available in any libraries in that case Ki CAD provides a drawing tool to draw the footprints on our own. The footprint of these components will be available in their datasheets that are available online. Figure 3.10 shows the front and the bottom view of the PCB prototype manufactured for this project.

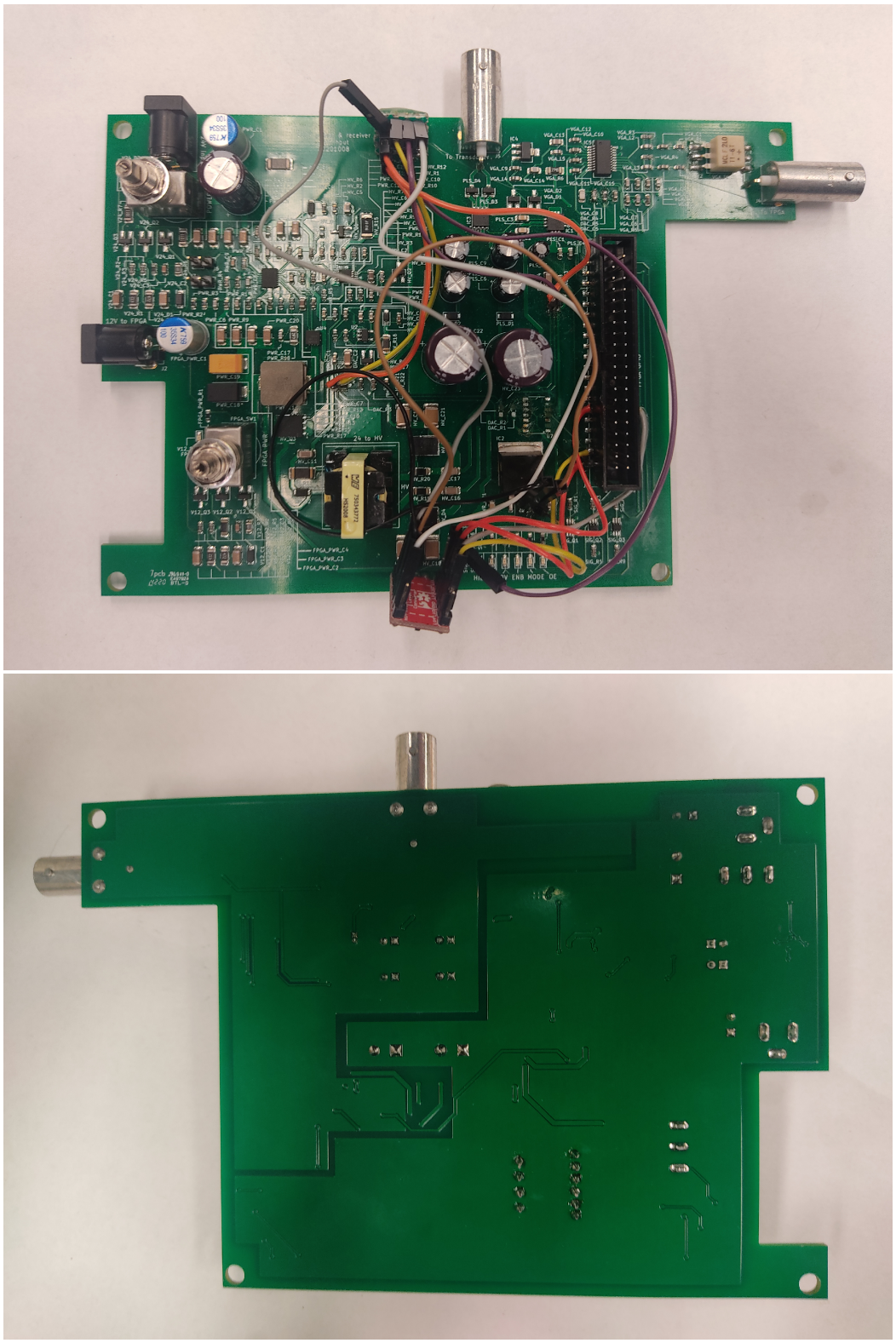


Figure 3.10: PCB manufactured by Bittele (a) Front View, (b) Bottom View

3.5 FPGA based Signal Generation and Processing

DE10 allows its users to program the FPGA using a connector called USB Blaster II through the QP's programmer tool or using binary files by having a micro-SD card with ARM based Linux system. Since Linux is used in software development, the Linux approach of programming the FPGA is preferred for this project. Linux is installed on the SoC part of the chip, HPS. HPS has FPGA as a peripheral in this configuration. To program the FPGA through HPS the setup procedure explained in the DE1 tutorial document is followed. In which the MSEL switch on the development board should be configured as shown in figure 3.5 to permit the hard processor system to program the FPGA.

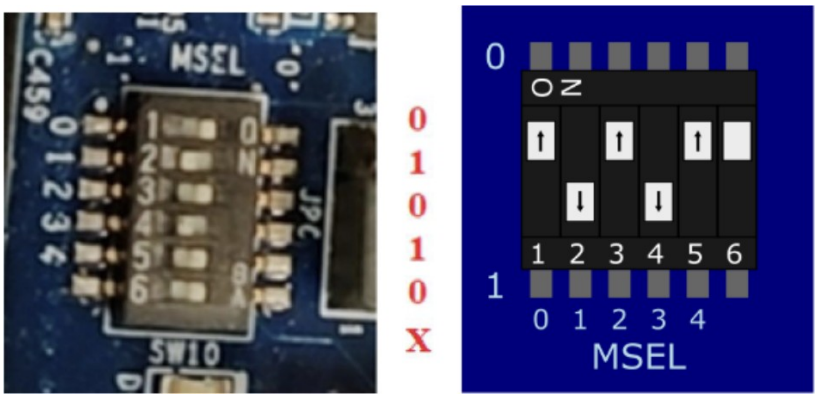


Figure 3.11: MSEL Switch Configuration [6]

To boot the ARM-based HPS with Linux, a micro-SD card with suitable Linux distribution is required. Once Linux is booted after the card is inserted in the Micro SD cardslot command-line instructions are used to program the FPGA. A freeware called Puttyis used to obtain grants to the Command line of Linux from the host computer. The USB mini-B port on the HPS side of the board is connected to the computer through the USB port of the host computer. The UART serial communication should have a Baud rate of 115200 bits per second and 8 data bit is required. The figure shows the Putty configurationinterface. The figure 3.7 provides a full image on the working of the Ultrasonic system.

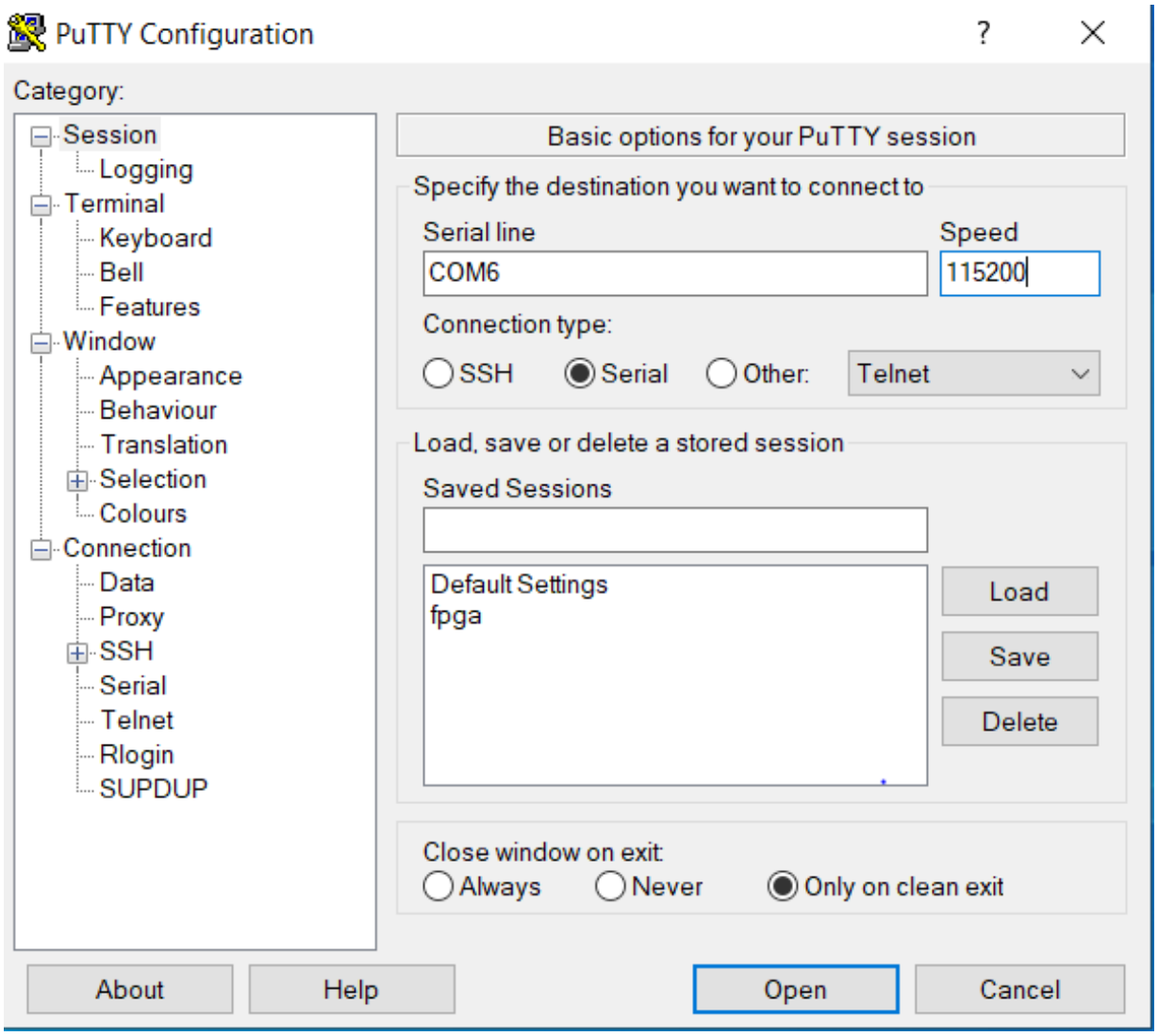


Figure 3.12: Putty Configuration

The signals shown in figure 3.7 can be explained as follows.

1. Activation pulses are sent to AFE from the Pulser block of the FPGA.

2. High Voltage pulses are sent to the probe by the AFE.

3. When the high voltage pulses strike the piezoelectric material on the probe it deforms and produces mechanical waves which are then sent to the testing specimen.

4. The echo signals from the specimen are collected by the probe and converted intoelectrical signals.

5. The echo signals from the probe are amplified to a 55db gain by the AFE.

6. The ADC converts the amplified echo signals to digital signals with 15-bit precision at 65 Msamples/s.

7. From ADC using the HSMC connector the digitized signals are sent to the FPGA.

8. The control block write of the FPGA writes the contents to the FIFO buffer.

9. From the FIFO buffer the read control block gathers the data.

10. The gathered data is then sent to the smart detection block and on-chip RAM for storage purposes.

11. Once the data is examined by the smart detection block it is then transferred to the HPS.

12. The HPS will examine the memory once sufficient data points are collected.

13. Finally, the HPS converts the data into display information that can be seen on a VGA display and can be stored into an SD card upon request which can be later transferred to the host computer.

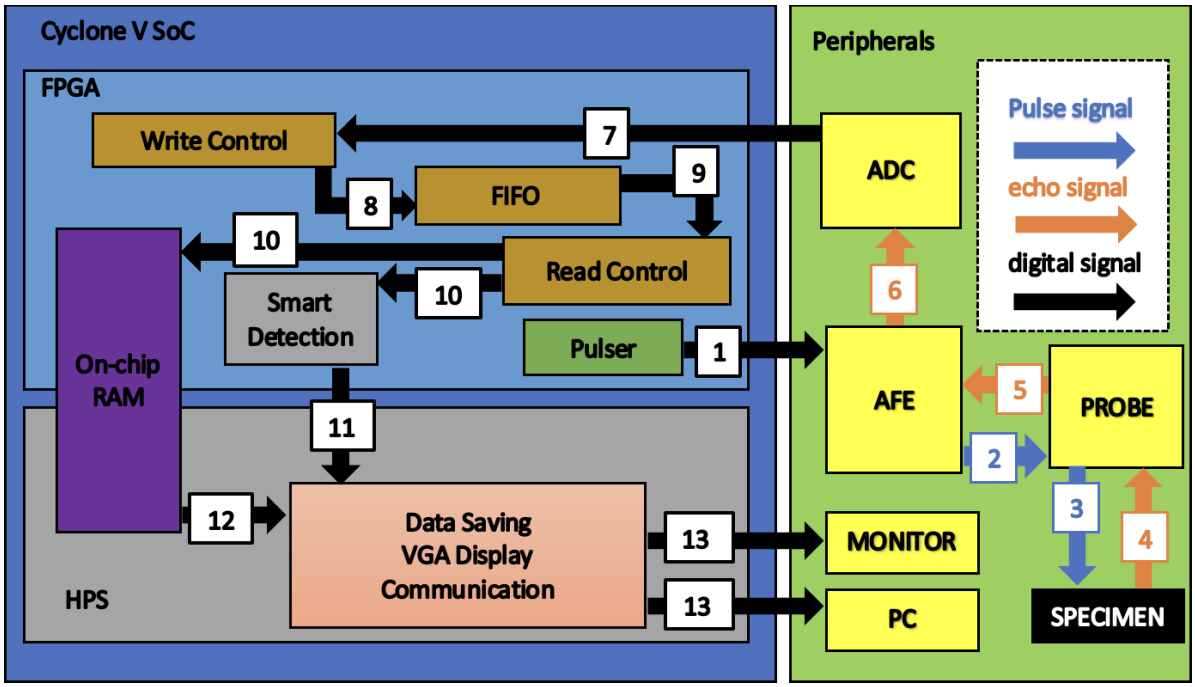


Figure 3.13: Ultrasonic System Block Diagram

Individual function blocks have been developed with Verilog HDL for carrying out the functions mentioned above. Explanation of these codes is a tedious process hence the function of each block can be explained. Pulser block has 3 states that include 10 MHz, 2.5MHz and an OFF state. The pulse repetition frequency of the pulser block is set to be 1 kHz. Switch 9 of the DE10 board is assigned to be an ON/OFF button. Hence the pulser's output signal depends on the switch's position as well as the pulse enable signal. The data from ADC should be sent directly to the on-chip RAM. But ADC and RAM have different clock domains hence for data preservation and clock domain crossing a dual clock FIFO is used. The working of the FIFO block commences when its reset state is lifted. The FIFO operation will terminate automatically when the write block that is programmed to take 4096 samples writes all of them. From FIFO the data will be absorbed by the read control and eventually the process of reading will stop.

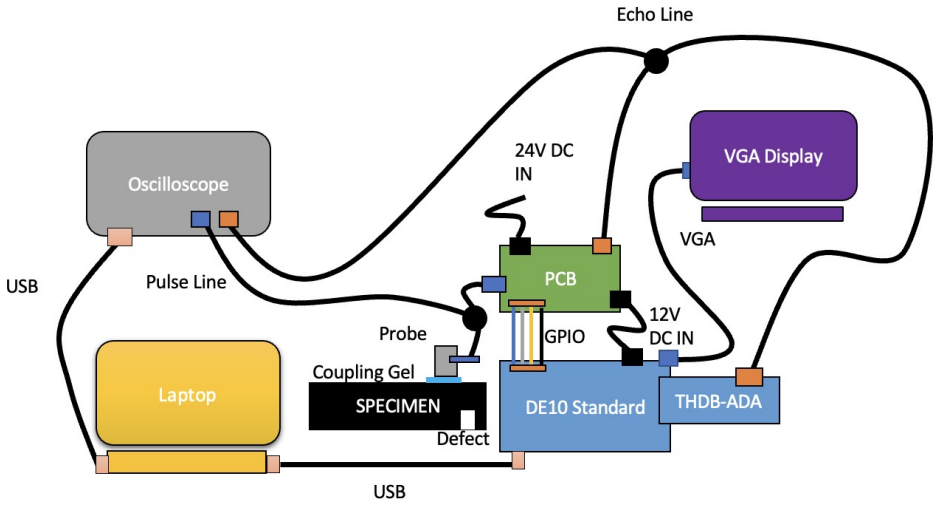
As the name suggests the smart detection block detects large fluctuations disregarding smaller ones by setting a trigger level. This block filters the signal and eliminates high- frequency components leaving behind distortions that provide valuable information. The smart detection block has four states along with the reset state. The IDLE state of smart detection block starting

values are fixed and the HPS is prevented from taking data from the shared memory. The TAKE DATA state of smart detection is triggered when the read control reads the specified number of words. Once the encountered echo position is recorded the information of pulse detection is forwarded to the HPS, and the smart detection block changes its state to PROC DATA. In the state of PROC DATA, the pulse information is examined, and the current pulse position is stored as a reference for the upcoming cycle and comparing the reference signal and a new signal if there is a premature reflection from a defect it can be easily determined. The smart detection block will change to a DONE state once all the words are read by the read control block. Key 1 of the development board acts as the reset button and erases all the previous pulse positions. The software development of the FPGA-based Ultrasonic system uses Linux in the ARM core for executing the codes. C language is used to code the software development and converted to binary files to run on Linux.

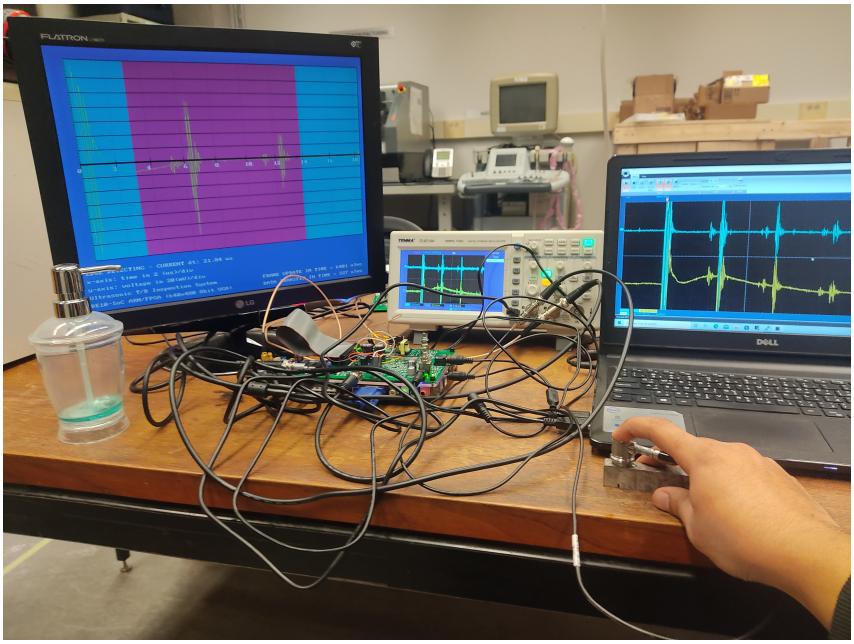
Chapter 4
Experimental Results

4.1 Specimens and Experimental Setups

The experiment aims at confirming the ability of the prototype to perform signal acquisition. A comparison between the prototype and TENMA 72-8710A oscilloscope is given in this chapter. The oscilloscope provides information that is used as the benchmark data to evaluate the prototype's data. In this experiment, the data is acquired from the oscilloscope and the prototype simultaneously. The real setup and its corresponding schematic are given in Figure 4.1. The pulse signal from AFE is given to channel 1 of the oscilloscope and the transducer probe using a T-connector. In the same way, using a T-connector the echo signal from AFE is split between channel 2 of the oscilloscope and the ADC channel 1 (THDB-ADA). A coupling gel is used between the specimen and the transducer since in this experiment a contact type transducer SIUI P10-10L is used. The prototype was controlled by a laptop through serial connections using Putty software. The data stored in the SD card is sent to the laptop using FileZilla through an ethernet connection. The contents from the oscilloscope are transmitted to the laptop using a program provided by TENMA named DSO monitor Controller. The DSO monitor controller stores the data in .wav form which is then converted into .csv format in the same software.

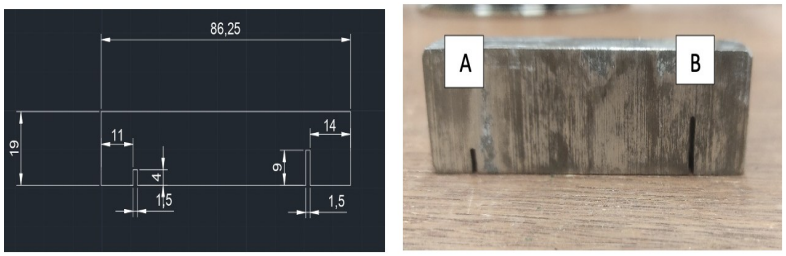


(a)

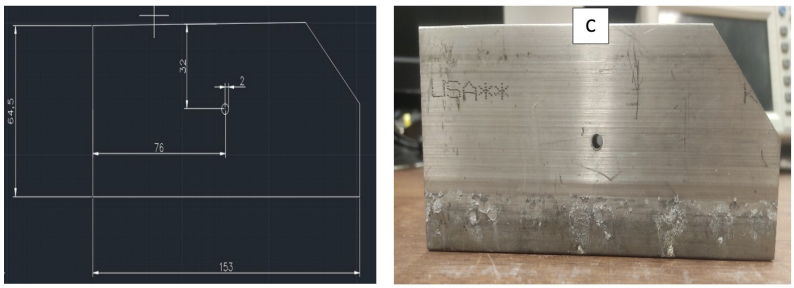


(b)

Figure 4.1: Validation Experiment Setup – (a) Schematic, (b) Actual



(a)



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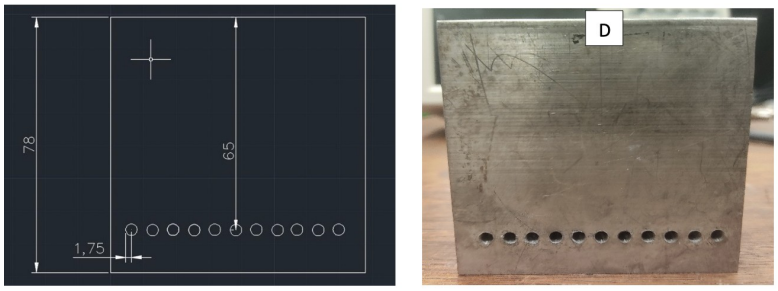


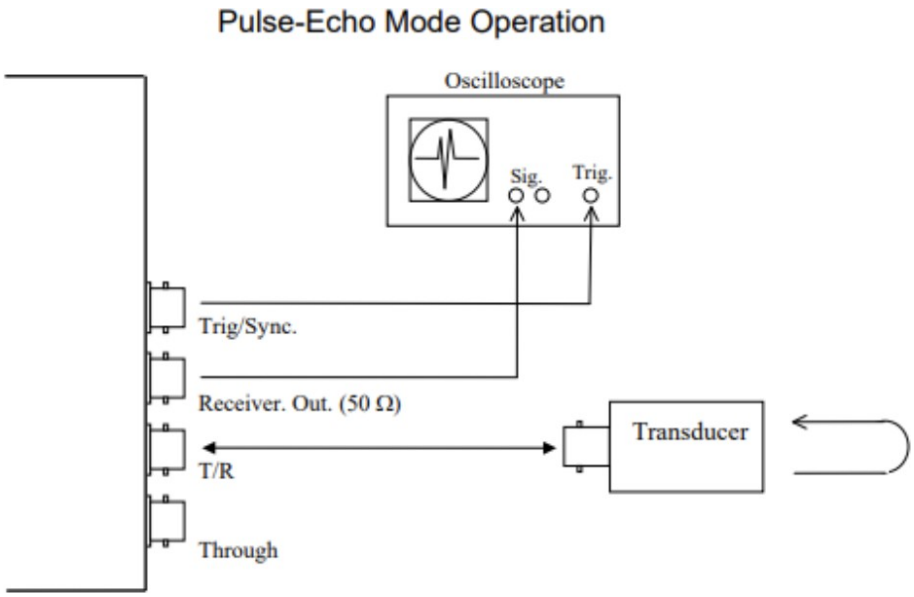
(c)

Figure 4.2: Dimensions and Test Points – (a) Specimen 1, (b) Specimen 2, (c) specimen 3

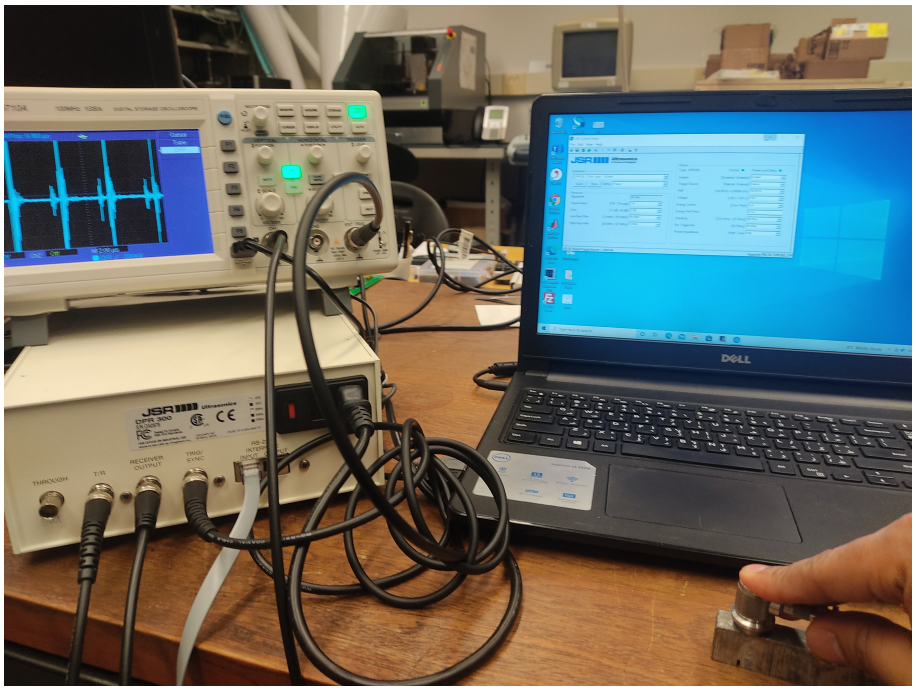
Specimens shown in the Figure 4.2 were prepared for the experiment. Specimen 1 is made up of aluminum and has 2 slots of 1.5 mm width. Specimen 2 has 11 drill which are present at 63.5 mm from the top of the specimen. Specimen 3 is made of steel and has a drill hole approximately at its center (29.75 mm when measured from the top). Four test points are selected from the three

specimens. Point A in specimen 1 was selected right above the slot of depth 4 mm and width 1.5 mm. Point B of specimen 1 is selected right above the slot of depth 9 mm and width 1.5 mm approximately. Specimen 2 has 11 drill holes and the center drill hole with a hole diameter of 4mm is taken into consideration and Point C is marked right above it. Finally, Point D in specimen 3 is right above the drill hole which is approximately present in the center of the specimen.

The benchmark experiment for this project was conducted using DPR 300 manufactured by JSR Ultrasonics. DPR 300 pulser/receiver unit is commercially available and capable of conducting T/R ultrasonic testing. It can be connected to the laptop through the JSR control panel software provided by JSR Ultrasonics in which the frequency, PRF and triggering of the pulse signal can be controlled. Figure 4.3 shows the schematic and the real setup of the DPR 300 unit. The output of the transducer from DPR 300 is connected to the TENMA oscilloscope to obtain the data.



(a)



(b)

Figure 4.3: Benchmark Experiment Setup – (a) Schematic [33], (b) Actual

Figure 4.4 shows the parameters that were set to conduct the benchmark experiment in the JSR control panel.

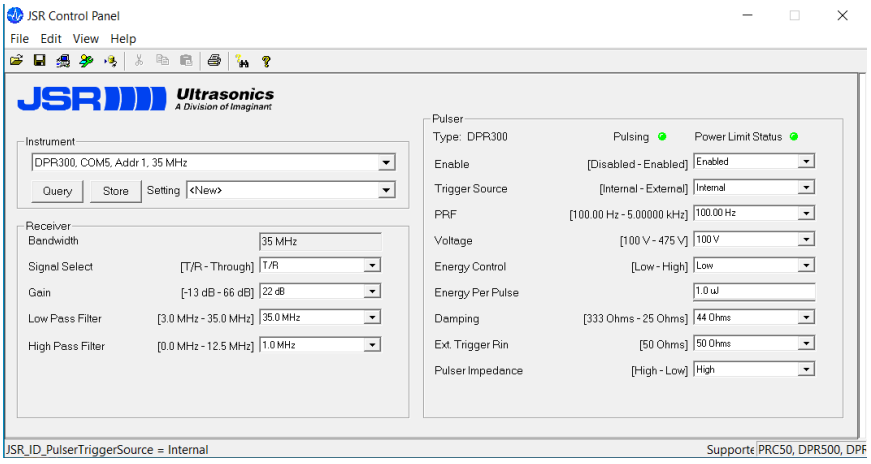
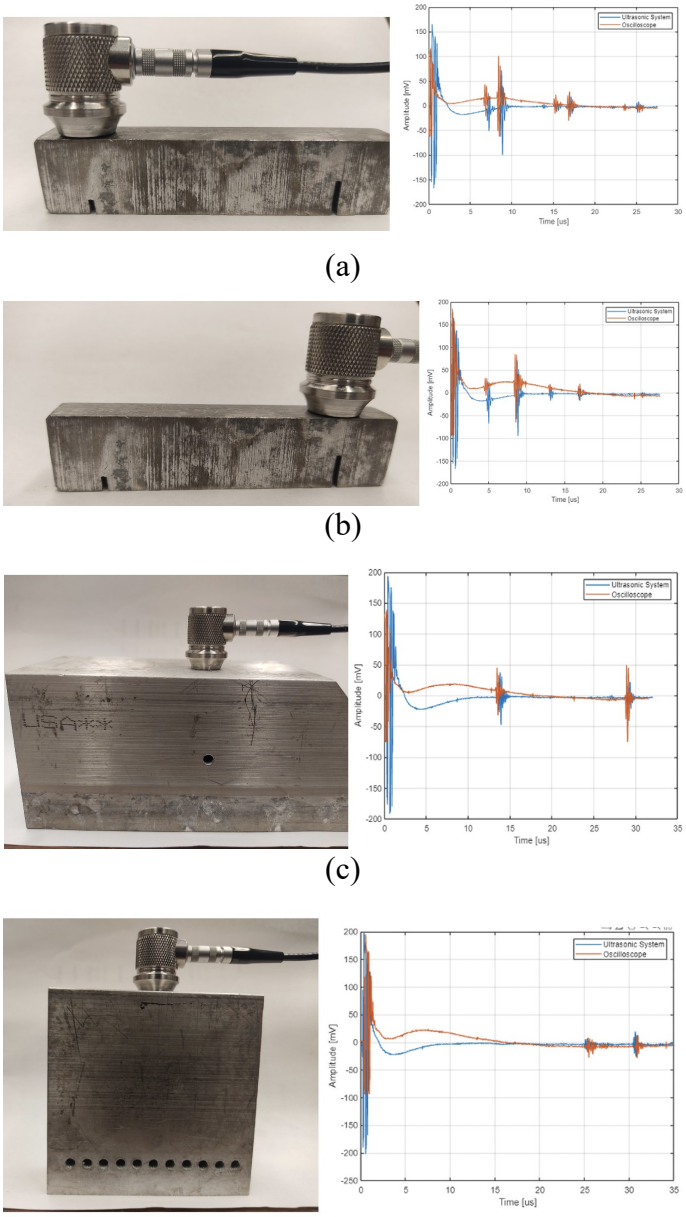


Figure 4.4: JSR Control Panel

4.2 Experimental Results

The results from the prototype system and the oscilloscope are presented in this section.



(a)

(b)

(c)

(d)

Figure 4.5: Validation Test Results – (a) Test Point A, (b) Test Point B, (c) Test Point C, (d) Test Point D

From the results plotted in Figure 4.5, the data from the model system has some disturbance in its base trend when compared to the oscilloscope. This can be due to the cable connections which

have to take a longer route to reach the FPGA than the oscilloscope. Since the RF signals are known as sparse vectors, the signals with large amplitude are considered to have useful information at the pulse locations. When comparing the pulse amplitude obtained from the prototype and the oscilloscope there is a ten to twenty percent difference in them. But both systems have a similar trend in the pulse magnitude. The reflection from the artificial defects and the boundaries can be seen easily in Figures 4.5 (a) to (d).

The results acquired from the DPR 300 pulser/receiver and prototype system are compared below. The DPR 300 has low and high pass filters applied hence it doesn't have any distortions in its base trend.

From figure 4.6 it can be seen that the pulse picked by the prototype is similar to the DPR 300 pulser/receiver. The prototype system is capable of mm to cm level thickness detection or detecting mm level defects as shown in the test results in figure 4.5 and figure 4.6. The system requires high voltage levels to detect micron level defects which can be developed in the upcoming design improvements.

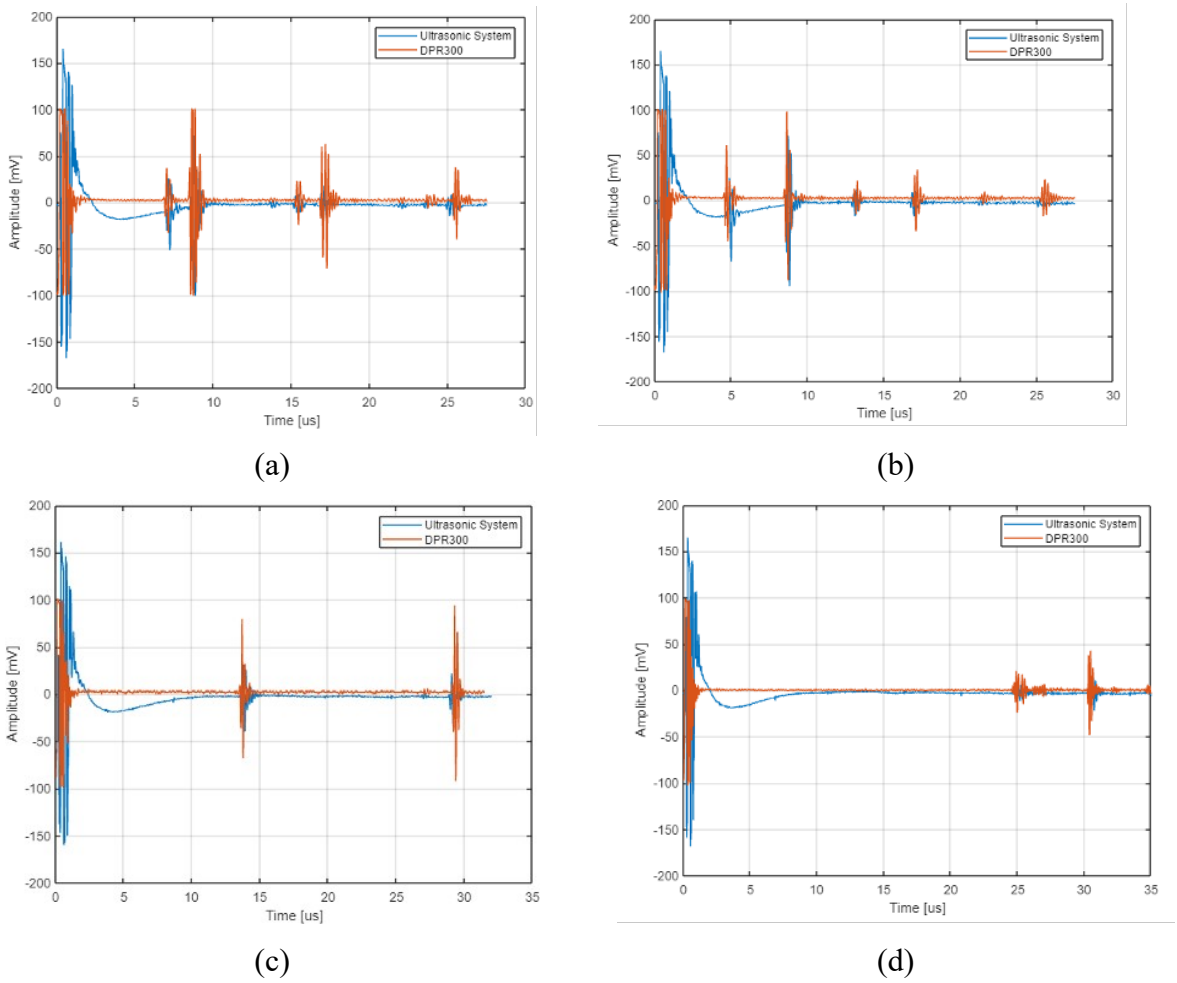


Figure 4.6: Comparison of Test Results obtained from DPR 300 and the Prototype system – (a) Test Point A, (b) Test Point B, (c) Test Point C, (d) Test Point D

Figure 4.7 shows the plots from which the distance of the defects from the top surface can be measured.

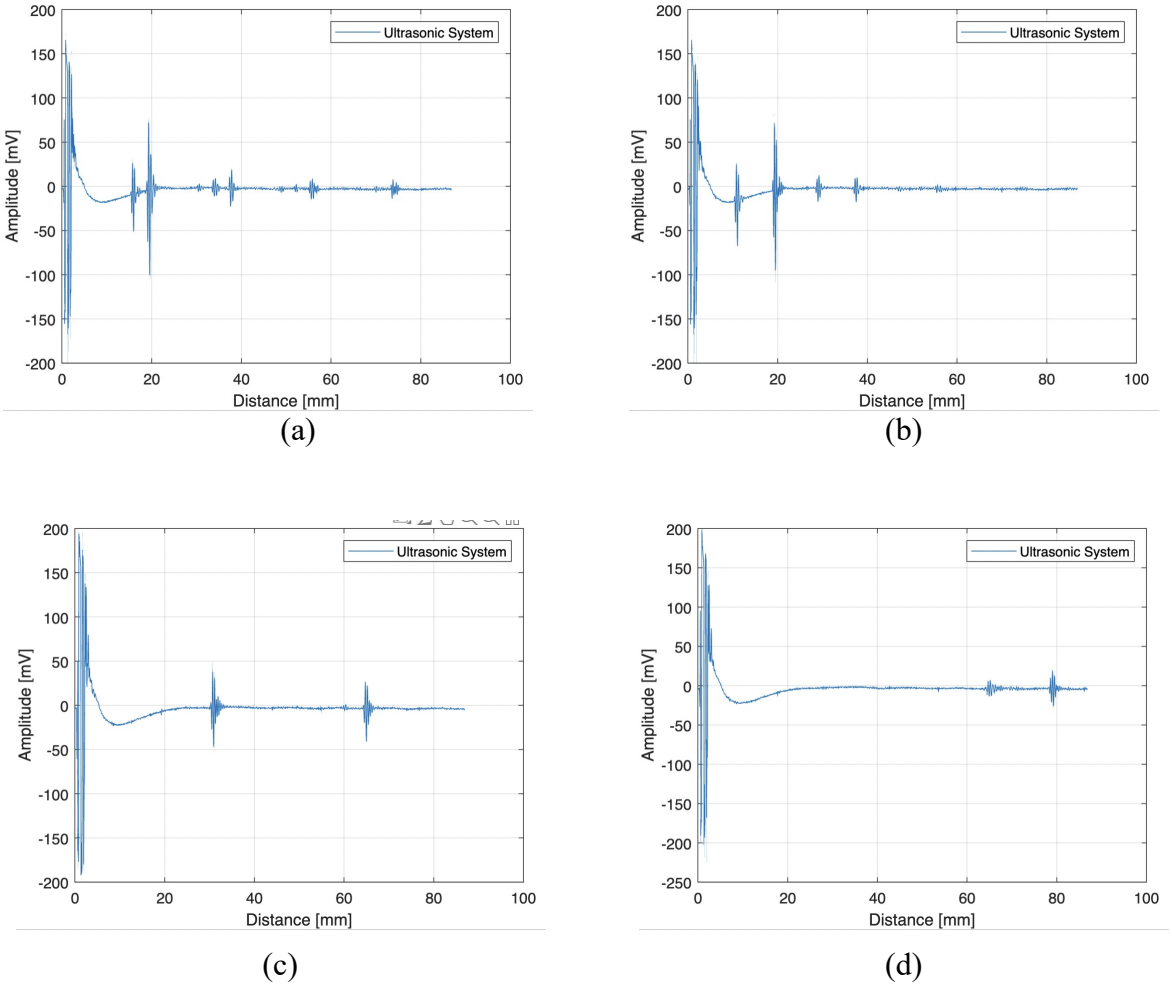


Figure 4.7: Distance of the defects from the top surface – (a) Test Point A, (b) Test Point B, (c) Test Point C, (d) Test Point D

Specimen 1 has 2 artificial defects of dimensions 4mm*1.5 mm at test point A and 9mm*1.5mm at test point B. From Figure 4.7 (a) the boundary reflections occur at 19mm approximately which is the thickness of specimen A. Also, the 1st premature reflection is seen at the 15mm mark approximately from which it can be inferred that there is a defect in the specimen 15 mm from the top surface or at 4mm when measured from the bottom surface. Similarly, from Figure 4.7 (b), the premature reflections are seen at 10 mm which means there is a defect 9mm from the bottom surface. For specimen 2 the center of the drill hole with a diameter of 4 mm is located at 32mm from the top surface and the reflection is seen at the 30mm mark indicating that the circumference

of the defect surface is at 30mm. Finally, for specimen 3 the prototype is capable of capturing the reflections from the boundary which at 78mm from the top surface and the center of the drill hole is 65mm from the top surface. The data shows that the prototype captured the pulse signals at 63mm indicating the premature reflections from the surface of the hole. From this, it can be concluded that the prototype system can be used in thickness measurement applications for mm-to-cm level thickness specimens.

The raw data from the prototype system was smoothed using Savitzky-Golay filter pro- vided by MATLAB [46]. There are many filters available in MATLAB that can aid in data de-noising and smoothing. It is a trail to use the Savizky-Golay filter as it tends to preserve the peak height and width of the signal. Figure 4.8 (a) to (d) shows the noisy and smooth signals of the 4-test points A, B, C and D. From these plots the smoothing seems fine but further smoothing is required to get rid of the initial spikes in the waveform. One way to do that is by using neural networks to filter out each segment of data separately. The ability to smooth the signal obtained from the prototype system indicates the capability of performing post-processing of data. As seen in DPR 300 which has both low and high pass filters provides the required de-noising and smoothing to the signals. In the upcoming improvements including these types of filters to the signal obtained from the prototype system are considered.

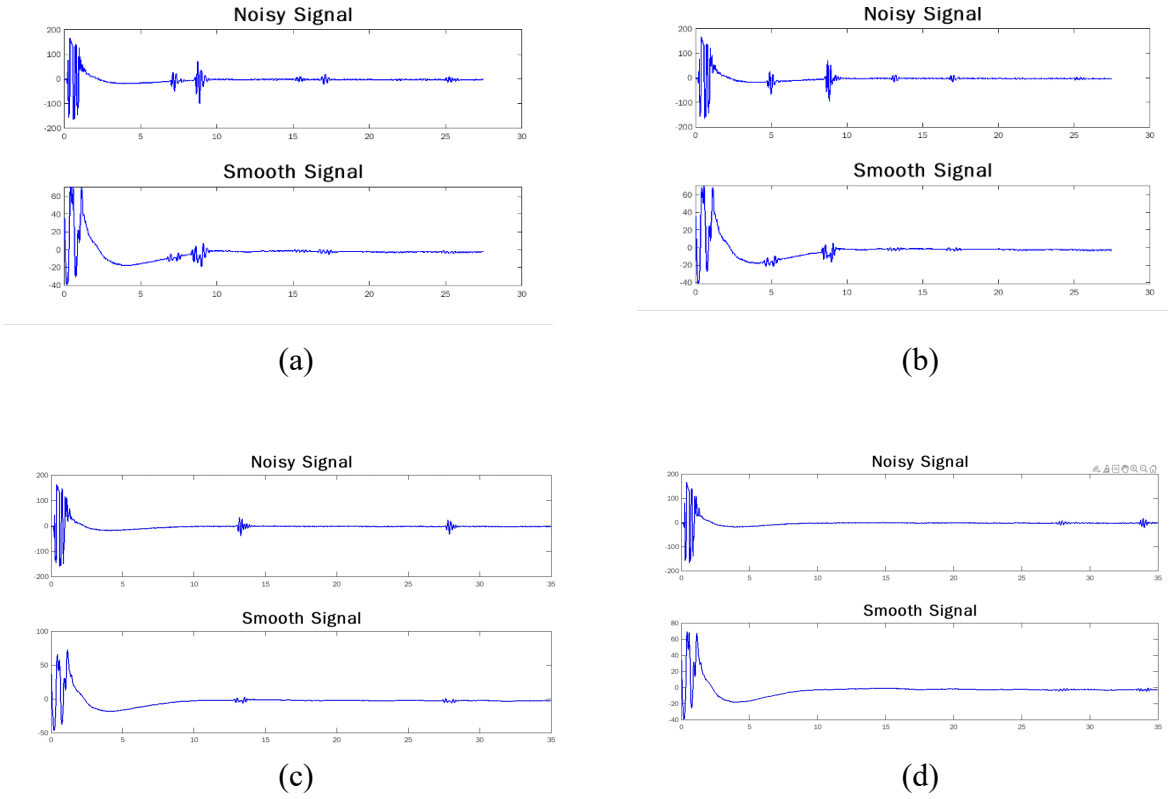


Figure 4.8: Noisy and Smooth Signals - (a) Test Point A, (b) Test Point B, (c) Test Point C, (d) Test Point D

4.3 Summary

The prototype system has shown good results for mm-level defect detection. For micro-level detection, high voltage input signals are required which can be developed in the upcoming systems. As in commercial UT equipment, the next design consideration should include battery packs to power up the prototype for the portability of the system.

As discussed in section 4.2 there are background noises in the data gathered by the prototype system. Though post-processing of acquired data can be done using MATLAB filters next design should include filtering techniques that de-noise and smooths the signal beforehand thus reducing the need for post-processing. Also, the problem of initial voltage fluctuation in the AFE as discussed in the section has to be rectified and the onboard connections have to be properly secured and protected with good shielding to be used in hazardous environments and portable applications.

Currently, the prototype is saving 2048 data points which last about 31.5 microseconds and has a sampling rate of 65 MHz. In the next prototype, the sampling rate should be increased making it suitable to be used on larger objects. To store a large amount of data we can use the board's 64 MB SDRAM or the HPS side's 1GB DDR3 RAM storage. The VGA drawing is a software-driven display that was adopted from Y Qian [6]. Hence it is relatively slow and cannot display a large number of data points. In the next design, a GPU processor could be coded on the FPGA side making the total system faster and more efficient. Using a GPU system can improve the resolution, display of VGA display which currently works with 640x480 pixels and data transfer can become more efficient as it removes the need to transfer data between two fabrics in the system.

Chapter 5
Conclusions and Future Work

The FPGA-based Ultrasonic Non-destructive testing system developed is field programmable and easy to set up. The prototype includes conversions like analog to digital and digital to analog, voltage amplification, software development, acquisition of signal and data processing. Currently, the system supports detection of single channel, but the components required for multi-channel detection (i.e., Phased Array) has been included in the design.

The Analog front end adopted from the previous designs has been improvised, the TENMA lab power source has been eliminated by including Voltage amplification in the design. The next design should be designed to be capable of providing higher voltage signals for minute defects detection. As discussed earlier the signal from the prototype has some background noises which can be eliminated using filtering techniques in the upcoming design changes. Initial power fluctuations on the board have to be resolved in the next design. The board has been designed to be mounted on the DE10 board making the system portable as a single unit. Further developments such as having a compact high-resolution display like modern UT equipment can be included in the future to the prototype system.

The prototype developed is capable of signal acquisition and processing but requires a few updates such as including a high-resolution display rather than the 640x480 pixel VGA display. THDB-ADA can be eliminated by including channels having high precision and sampling rates to make the system more compact. More advanced algorithms can be implemented to incorporate the prototype with robotics to make the automated inline inspection possible. Nonetheless, a working prototype has been developed and the main concepts of detecting defects, acquiring signals, processing the data, and displaying them have been done successfully.

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