Monolithic Integrated Reconfigurable RF-MEMS Phase Shifters

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

Micro-electro-mechanical systems (MEMS) actuators are a key technology that have been utilized in many real-world applications. This thesis investigates the application of MEMS technology in the design of RF components and reconfigurable phase shifters for use at fifth generation (5G) cellular network mid-band frequencies. The key benefits that MEMS technology offers are very attractive for use in RF applications. RF-MEMS switches provide the advantage of low loss, low power consumption, and high isolation, with the disadvantage of having slow switching speeds, reliability concerns of physical moving structures, and difficult fabrication.

This thesis presents the design, simulation, microfabrication, and testing of RF-MEMS devices for use in the 5G mid-band spectrum. This includes monolithic integrated single and multiport RF-MEMS switches, which go on to serve as the foundational components for further complicated RF devices. These switches are implemented to design switched-capacitor banks using metal-insulator-metal (MIM) capacitors and capacitors realized using co-planar waveguide (CPW) stubs. The aforementioned components are then incorporated into a 40° reconfigurable digital RF phase shifter design over the frequency range of 3.4 to 3.8 GHz, and feature enough bits and states to achieve near analog phase shift resolution. A switched-line RF phase shifter is designed using multiport RF-MEMS switches, capable of a true-time-delay (TTD) phase shift of 0° to 320°, in increments of 40°. These two phase shifters are then combined to design a monolithic integrated full range 360° reconfigurable RF-MEMS phase shifter.

Acknowledgements

I would like to express my sincere feelings of gratitude first and foremost to Professor Raafat Mansour, without whom none of this would be possible. His support and guidance has continued to help me find direction in my work and research in the exciting field of RF.

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Finally, I would like to thank my family, friends, and loved ones for their support in my academic journey. I am forever grateful to my parents, and especially thankful to my girlfriend, Annika Kjerulf, for their endless support and encouragement throughout the duration of my graduate degree.

Dedication

To my family, friends, and loved ones. Your support is forever appreciated.

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Chapter 1

Introduction

1.1 Motivation

In the current era of fifth-generation technology standard for broadband cellular networks (5G), phased array antennas are one of the most critical devices, vital in the performance and operation of 5G systems. They are used in radar applications, satellite communications, and telecommunications applications. RF phase shifters are key components for use in phased arrays. Phased array antennas are arrays of unit elements that can adjust the direction of the propagating beams without physical movement. RF phase shifters are critical in phased array antennas, as they provide relative phase shift and propagation delay amongst array elements to allow for beam steering.

In today's industry, the points of interest for phased array antennas are low insertion loss, low driving power, and low cost of production. Traditional phased arrays are usually associated with high fabrication, assembly, and integration cost, as well as high power consumption.

The motivation to use MEMS based RF switches is from the high isolation, low insertion loss, and low DC drive power consumption characteristics they offer.

Phased array antennas typically employ a large number of phase shifters. Each phase shifter uses several switches, thus MEMS-based phase shifters offer very low power consumption when implemented in phased arrays. MEMS phase shifters can be fabricated fully monolithic and integrated with the other components in antenna elements, on substrates. This results in low-cost phased arrays. Generally, MEMS switching speed is relatively slow, which limits the application of RF-MEMS based phased arrays to only slow scanning arrays.

1.2 Objective

The objective of this thesis is to explore the design, fabrication, and performance of fully monolithic integrated RF-MEMS based reconfigurable phase shifters at 3.4 to 3.8 GHz, a common frequency range allocated for use in 5G applications.

The research tasks involve the development and design of a single pole single throw (SPST) MEMS switch and incorporating this component into more complex RF devices that are vital for the design of a reconfigurable phase shifter. These components include multi-port RF-MEMS switches, and MEMS-based switched-capacitor banks.

Specifically, the objective is to design a 40° reconfigurable RF-MEMS based phase shifter. With this phase shifter, a switched-line phase shifter is also incorporated to extend the phase shift range to 360°.

1.3 Outline of Thesis

Following the motivation, objective, and outline provided in chapter 1, chapter 2 of this thesis gives an overview of MEMS technology and its application in RF switch devices. Chapter 2 also goes over a literature review on RF phase shifters and distributed MEMS transmission lines (DMTL). In chapter 3, the microfabrication process used to realize the RF-MEMS devices is reported. The measurement setup for the RF devices is also discussed in this chapter. Chapter 4 goes over the design of a series contact RF-MEMS switch, and presents more complex multi-port switch configurations. This chapter also presents the design of RF-MEMS based switched-capacitor banks using either metal-insulator-metal (MIM) capacitors or open circuit co-planar waveguide (CPW) stubs. Chapter 5 presents the design of a reconfigurable 40° phase shifter using the previously listed components, and the integration of switched-line phase shifters into the 40° phase shifter to design a full range 360° phase shifter at the target frequency of 3.6 GHz. Chapter 6 reviews the presented designs and results of the thesis, and proposes future work for performance improvement.

Chapter 2

Literature Review

2.1 Overview

RF switches are vital components in a variety of commercial and industrial applications, including wireless communications systems, aerospace, and radar systems. Traditional solid state RF switches (GaAs FET and PIN diode) offer fast switching speeds and are low cost. However, they suffer from high power consumption and non-linear effects at higher frequencies.

RF-MEMS switches on the other hand offer advantages in performance including low insertion loss, high isolation, high linearity, and low power consumption. For this advantage, they suffer from slow switching speeds, are difficult to fabricate, and have the reliability concerns regarding physical mechanical movement. This chapter presents a brief review on the topic of MEMS actuators and their application in RF-MEMS devices.

2.2 MEMS Actuators

Microelectromechanical systems (MEMS) actuators are micrometer scale devices that convert applied electrical power into physical motion [1]. There are a large variety of uses for MEMS devices. An example is the design of an ethanol vapor sensor by applying of a polymeric sensing material onto a MEMS cantilever [2]. A mass adsorbed onto the detecting material increases the mass of the MEMS cantilever, changes the displacement or resonant behaviour of the structure. A scanning electron microscope (SEM) image of the MEMS gas sensor can be seen in Figure 2.1.

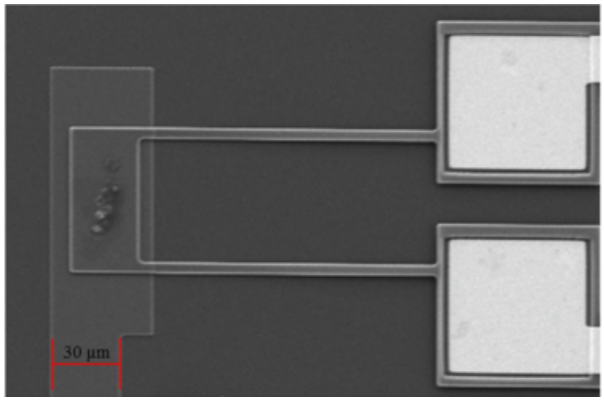

Figure 2.1: SEM image of a MEMS cantilever ethanol gas sensor [2].

MEMS actuators can be categorized based on their method of actuation, typically grouped into electostatic, electrothermal, piezoelectric, and magnetic MEMS actuators. Within these classifications, the MEMS categories can be broken down even further, as seen in Table 2.1 [3].

Of the four classifications, electrostatic and electrothermal actuators are the most common. A simple electrostatic actuators typically consist of a fixed and movable electrode

Table 2.1: Families and classes of mechanical MEMS actuators [3].

Electrostatic	**Piezoelectric**	**Thermal**	**Magnetic**
Comb drive	Bimorph	Bimorph	Electromagnetic
Scratch drive	Expansion	Solid expansion	Magnetostrictive
Parallel plate		Topology optimized	External field
Inchworm		Shape memory alloy	Magnetic relay
Impact		Fluid expansion	
Distributed		State change	
Repulsive force		Thermal relay	
Curved electrode			
S-shaped			
Electrostatic relay			

plates, anchored at one or both ends. An applied voltage bias between the two electrodes creates an attractive electrostatic force, opposing the spring force of the movable upper electrode plate. The two forces oppose each other, and come to a steady state. As the bias increases, so does the attractive force, causing displacement of the movable electrode plate. Once the applied voltage reaches a threshold and the gap between the electrode plates reduces enough, the increased electrostatic force causes the system of equilibrium between the two forces to collapse due to a positive feedback. This effect is called the pull-in effect. This typically occurs when the displacement reduces the gap to a third of its original value. A lumped parameter model of a parallel-plate actuator can be seen in Figure 2.2 [4].

Electrothermal actuators operate by converting electrical energy into heat. They have been used in a wide variety of applications. Figure 2.3 presents a thermal actuator used

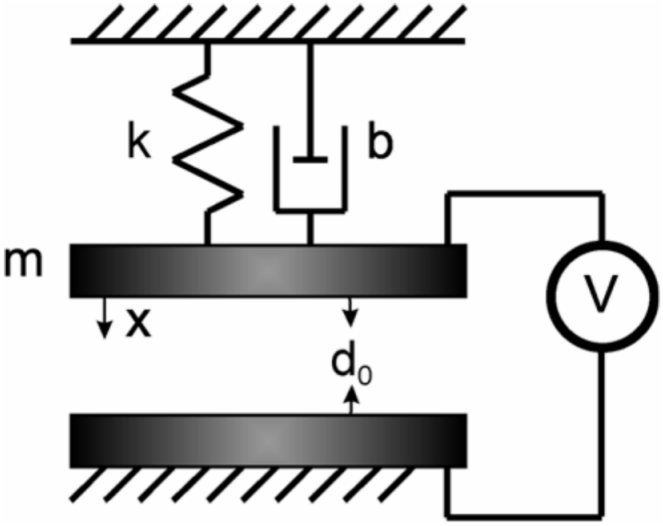

Figure 2.2: Lumped parameter model of a parallel-plate actuator [4].

in optical switching devices, by the Southwest Research Institute [5].

The most basic of these is an electrothermal bimorph actuator, an actuator that consists of thin layers of two materials with different coefficients of thermal expansion. When a voltage bias is applied, a current flows through and heat is generated in the actuator through joule heating. Because of the different in thermal expansion, the two thin films expand at different rates, causing the MEMS device to actuate.

Another example of electrothermal actuators is a hot-and-cold arm actuator. This type of actuator uses the same material, but changes the width of the metal, effectively increasing or decreasing the resistance of the metal line. With higher resistance, the temperature increases due to joule heating. With different arms of different thickness, a hot arm that expands more, and a cold arm that expands less can be achieved, resulting in lateral actuation. A typical model of a hot-and-cold arm can be seen in Figure 2.4 [5].

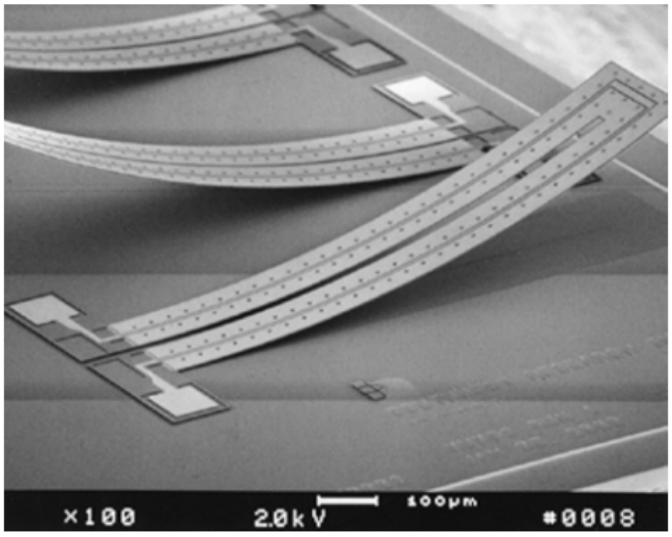

Figure 2.3: Thermal actuator SEM image by the Southwest Research Institute [5].

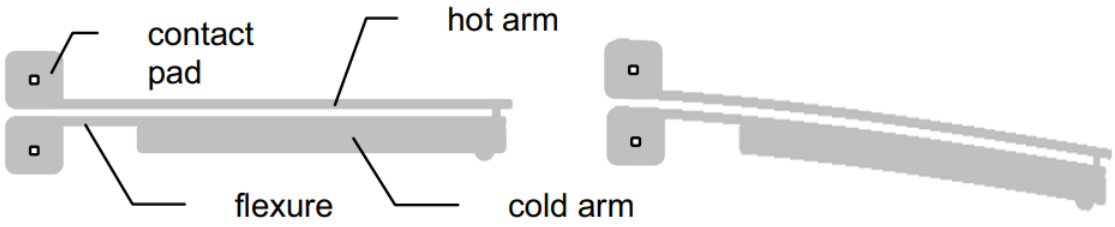

Figure 2.4: Hot-and-cold arm therma actuator model: a) Not actuated, b) Actuation after an applied bias [5].

2.3 RF-MEMS Switches

Using the aforementioned MEMS actuators, RF switches can be designed. An RF-switch is capable of turning on or off the flow of the RF signal in a conducting line. An electrostatic actuator can be used to realize both series and shunt RF-MEMS switches.

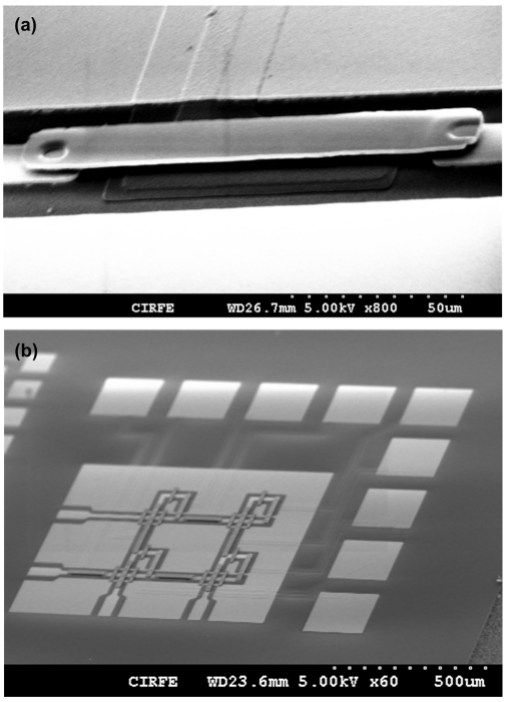

Figure 2.5: SEM image of a) a series contact cantilever beam switch and b) a 2 by 2 switch matrix [6].

A series RF switch is a contact switch that uses physical contact in the ON state to pass RF signals along the switch. This is typically achieved using a series electrostatic MEMS switch that is anchored on one end, and free on the other. By applying a large bias between an isolated bottom electrode and the upper electrode of the switch, the series switch will

actuate and make physical contact with the transmission line on the other side, completing the RF connection. A low loss dielectric layer is used to isolate the bottom electrode, to prevent the upper electrode from making contact and short circuiting. Switch matrices can be designed using individual series contact switches [6]. An example of a series switch fabricated at CIRFE is presented in Figure 2.5 [6].

Electrostatic MEMS switches draw almost no current and result in a very low power consumption, which is ideal for RF switches. RF-MEMS switches use high conductivity metals and dielectrics with low RF loss to yield an impressive low RF loss. However, RF-MEMS switches suffer from a high actuation voltage requirement, sometimes reaching over 50V. Because of this, MEMS devices often need step-up converters to reach the required voltages for pull-in.

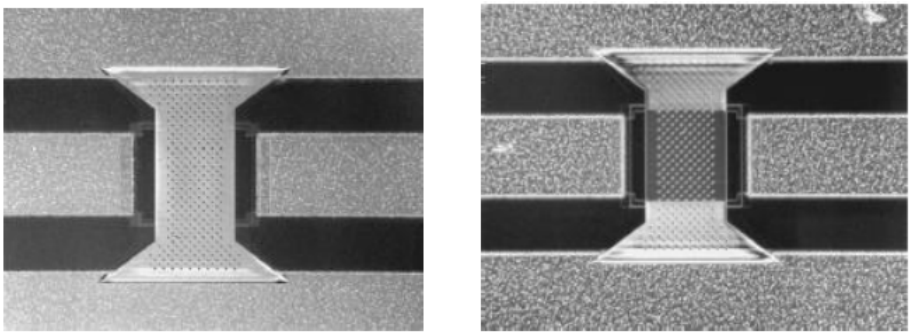

Figure 2.6: SEM of a Raytheon shunt switch in the a) ON state, b) OFF state (actuated) [7].

A shunt RF switch is typically a electrostatic RF switch that does not rely on physical contact. Instead, it is in the ON state without any applied bias. This is achieved by an electrostatic MEMS bridge actuator, anchored at both sides, and anchored on the ground planes. This bridge structure is over the signal line of a transmission line. An isolating

dielectric layer is placed above the signal line to prevent direct contact during actuation. By actuating the switch, the upper electrode moves closer to proximity with the signal line. When this occurs, the RF signal will flow through the bridge and be shorted to ground.

Examples of RF-MEMS switches can be found in literature, realized using CMOS technology [8], or even an in house custom fabrication process [6]. Using the basic single pole single throw (SPST) RF-MEMS switch, more complex multi-port switch matrices can be developed. In the past, multiport switches for satellite applications were realized using RF-MEMS technology [9] [10]. An example of a thermally actuated latching RF-MEMS switches that was previously demonstrated in literature can be seen in Figure 2.7 [11]. Further exploration into RF-MEMS switches will be presented in Chapter 4.

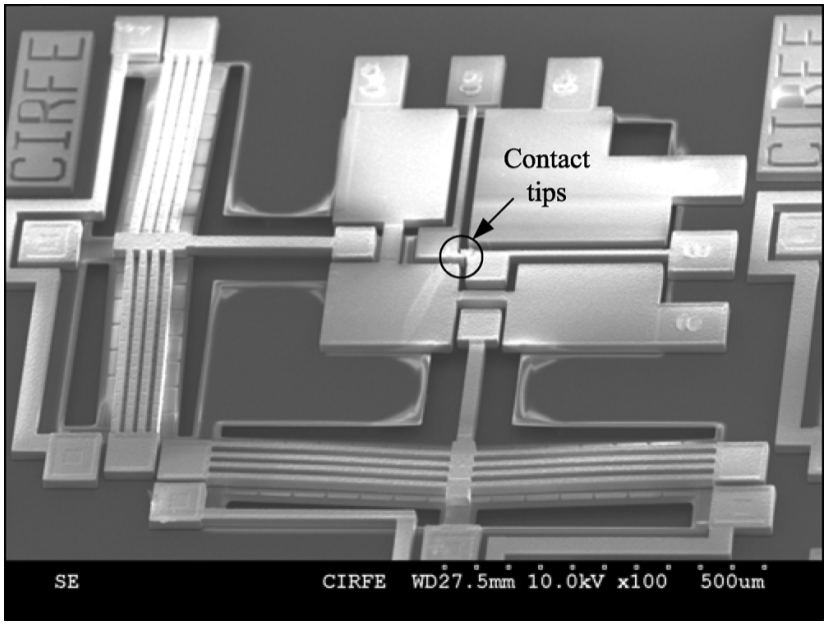

Figure 2.7: SEM image of a fabricated thermally actuated latching RF-MEMS switch by CIRFE [11].

2.4 RF-MEMS Phase Shifters

Complex devices such as RF phase shifter can be designed using the aforementioned RF-MEMS switches as a foundation. Switched-line phase shifters use multiport switches to switch between two or more transmission line paths with different electrical lengths, to achieve a true time delay phase shift from a reference RF path [1]. The insertion loss of a switched-line phase shifter is primarily determined by the losses from the switches used, as well as the transmission line losses if the lengths are really long, for very large phase shifts at lower frequencies.

Switched-line RF phase shifters using RF-MEMS switches have been demonstrated previously in literature [12]. Figure 2.8 shows a fabricated switched-line phase shifter using SP4T RF-MEMS switches, designed for use at 60 GHz [12]. This design consists of a reference line and 3 other RF paths with different electrical lengths to achieve a phase shift of 90° 180° and 270° respective to the reference line.

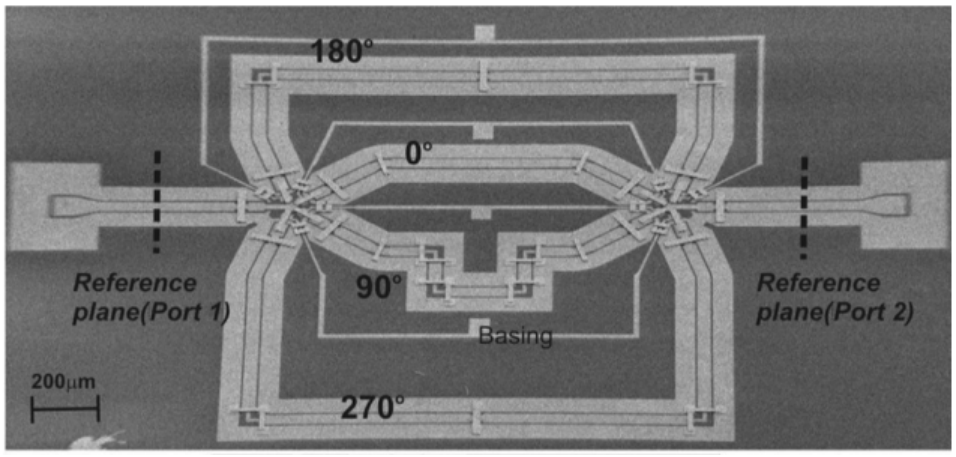

Figure 2.8: SEM image oof a 2-bit switched-line phase shifter [12].

A greater number of bits used in such a phase shifter results in smaller precision in phase shift steps, as well as a greater number of states [13]. An SEM image of a 4-bit RF-MEMS phase shifter design using SPDT switches can be seen in Figure 2.9.

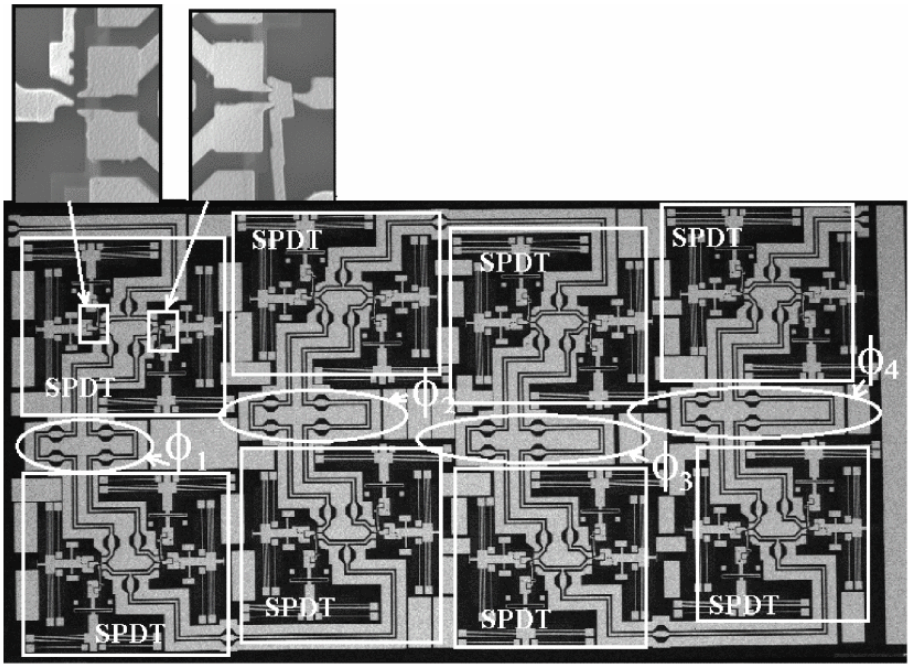

Figure 2.9: SEM image of a 4-bit RF-MEMS phase shifter using SPDT switches [13].

Distributed transmission lines can be used as phase shifters by adding a periodic switchable capacitance along a high impedance line [14]. By increasing the capacitance per unit length of the transmission line, the phase velocity decreases, resulting in a phase delay. As a consequence of the increased capacitance, the characteristic impedance of the line is decreased, so the high impedance line is used to compensate for this effect and bring the impedance closer to 50 Ω during operation [14]. Nagra et al. [14] presents a phase shifter design realized using a CPW line periodically loaded with varactor diodes.

An RF-MEMS based phase shifter has also been demonstrated using distributed MEMS (DMTL) transmission lines [15]. Figure 2.10 presents a 1-bit RF-MEMS DMTL phase shifter using 11 shunt MEMS switches [15]. Unfortunately, shunt MEMS switches can only provide small capacitance changes from OFF to ON state. To account for this, the design by Borgioli et al. uses 11 total shunt MEMS switches to increase the capacitance change. However, this elongates the transmission line and the total design length.

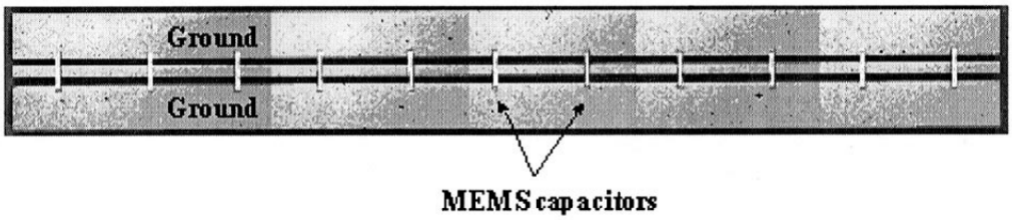

Figure 2.10: Image of a 1-bit RF-MEMS DMTL phase shifter using 11 shunt MEMS switches [15].

Alternatively, MEMS capacitor banks can be used to load the transmission line to increase the number of possible states rather than a binary MEMS capacitor. With a larger number of states and bits, a digital phase shifter with smaller resolution and precision can be attained. Examples of MEMS capacitor banks with multiple states with progressively increasing capacitance have previously been presented in literature. Aziz et al. presents a CMOS based 4-bit RF-MEMS switched-capacitor bank capable of exhibiting 16 operational states over a range of 0.15-1.2pF with an operational frequency range of 3-10GHz [16], and Bakri-Kassem et al. presents a 4-bit RF-MEMS switched-capacitor bank with a capacitance range of 0.7-20pF capable of higher power applications up to 30W [17].

A digital RF-MEMS phase shifter with sufficiently small resolution and numerous operation states would be able to achieve tuning with analog-like phase resolution. A smaller

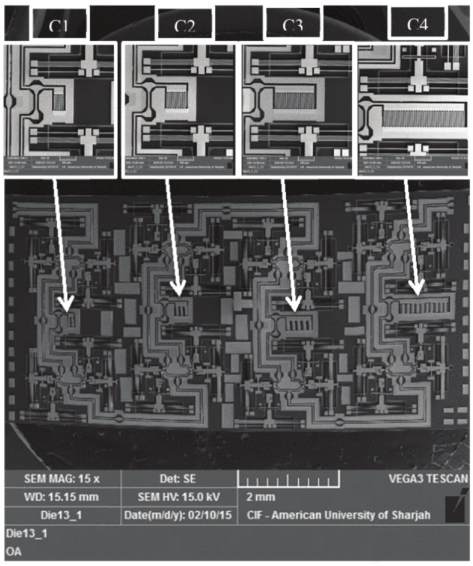

Figure 2.11: SEM image of a high power 4-bit RF-MEMS switched-capacitor bank [17].

resolution would result in much more accurate beam control when it comes to applying RF phase shifters for phased array antennas.

A reconfigurable digital 360° RF-MEMS phase shifter with near analog precision has never been demonstrated before in literature. The goal of this thesis it to propose one such design capable of achieving full 360° range with very small analog-like phase resolution relying on RF-MEMS switch technology.

Chapter 3

Fabrication and Testing of RF MEMS Devices

3.1 Microfabrication Process

With any form of thin film device technology, the design aspect is confined by the fabrication methods and the limitations set by the microfabrication tolerances. Factors such as thickness, minimum feature size, and material characteristics must be taken into consideration when designing devices. The fabrication process steps and layers for the RF-MEMS devices presented in this thesis are described below. The microfabrication process for the RF devices is a modified version of the University of Waterloo MicroElectroMechanical Systems (UW-MEMS) process developed in the Centre for Integrated RF Engineering (CIRFE) [18]. The UW-MEMS process is a seven mask surface micromachining microfabrication process developed for gold-based RF circuits and MEMS devices, as shown in Fig. 3.1.

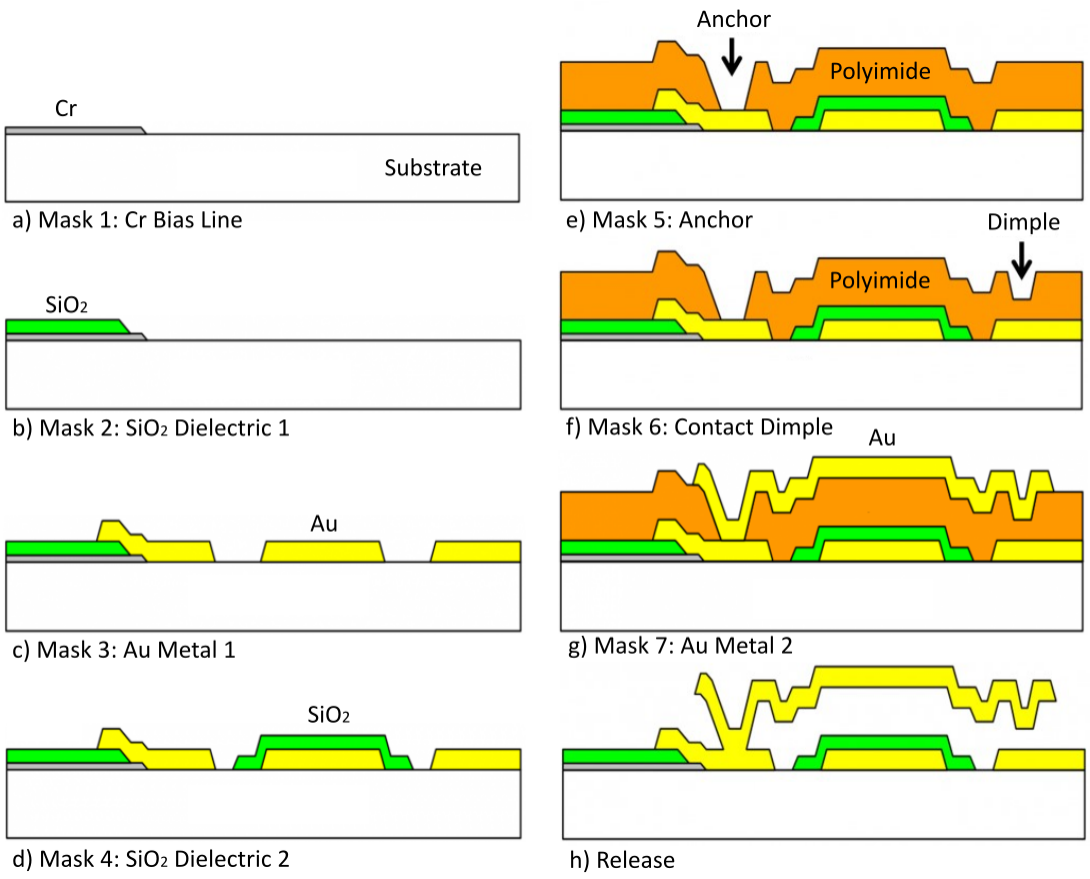

Figure 3.1: UW-MEMS microfabrication process steps for monolithic integrated RF-MEMS devices.

Alumina substrates are used for their low loss properties, with a size of 2.5" x 2.5". The substrate is cleaned using RCA1 cleaning. A 50 nm thick layer of chromium (Cr) is deposited using e-beam evaporation and patterned using wet etching. This Cr layer serves to form routing and biasing lines for the MEMS devices. Figure 3.2a shows the Cr pattern of a bias line and on-chip resistor used to bias a single port single throw (SPST) MEMS switch.

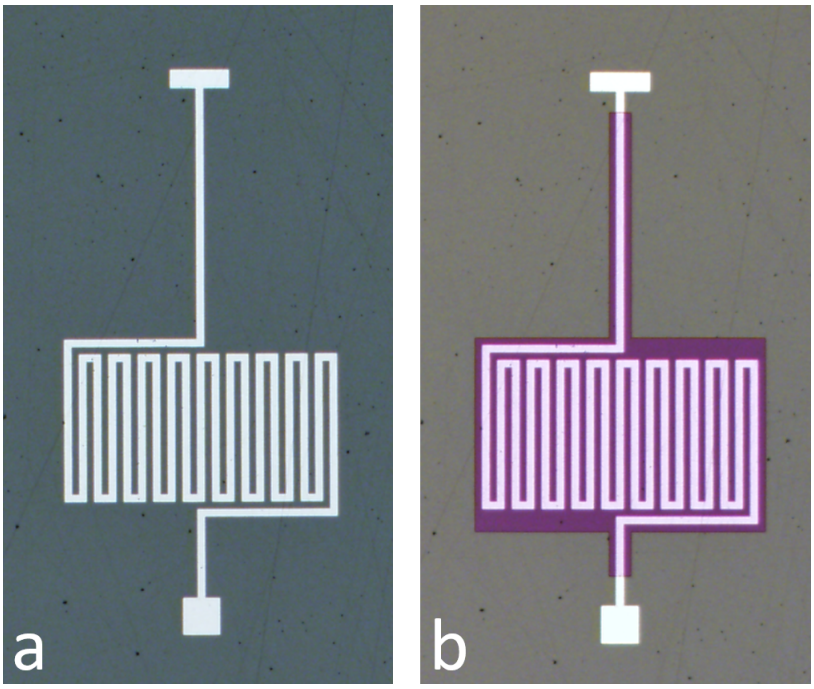

Figure 3.2: MEMS Switch Fabrication: a) Layer 1 (Cr) b) Layer 2 (SiO_2).

The sheet resistance of the Cr layer is vital for designing bias lines and on-chip resistors to place in series with the bias lines to decouple RF and DC signals. The sheet resistance is given by R_s $[\Omega/sq]$ in equation 3.1

$$R_s = \frac{\rho}{t} \tag{3.1}$$

where ρ is the resistivity of the material $[\Omega m]$, and t is the thickness of the material $[m]$. The precision of the layer thickness is vital as it determines the sheet resistance of the layer. Using a 4 point probe, the sheet resistance of the Cr layer throughout 12 points on the alumina wafer was found as shown in Fig. 3.3. The average sheet resistance was found to be 34 Ω/sq, with the standard deviation at 7.540%. The Cr layer can also be used as bottom electrodes for electrostatic MEMS actuation, however it will not be used as such in this work.

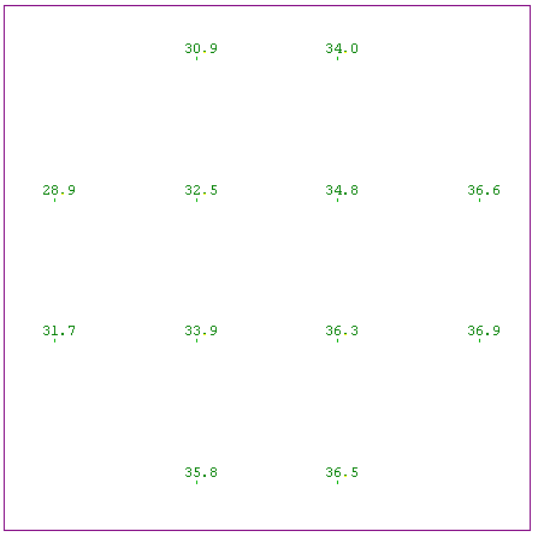

Figure 3.3: Sheet resistance distribution of e-beam Cr film on wafer.

A layer of 0.65 μm thick silicon dioxide (SiO_2) is then deposited using plasma enhanced chemical vapor deposition (PECVD) and patterned using reactive ion etching (RIE). The purpose of this layer is to electrically isolate the Cr layer (layer 1) from the first gold (Au)

layer (layer 3) in any overlapping area between the two layers and prevent shorts. It is also used to protect the Cr bias and routing lines from any future microfabrication process steps and outside exposure. Fig. 3.2b shows the SiO_2 layer of a MEMS switch, used to protect the Cr bias line.

This layer also serves as the dielectric layer for metal-insulator-metal (MIM) capacitors, between the 1st Cr and 3rd Au layer. Once patterning of this layer is complete, the thickness is carefully characterized to resimulate and design the capacitors using the measured thickness. The dimensions of the 3rd layer (first gold layer) were adjusted, so that the realized capacitors matched the capacitance values used for designing devices. The frequency dependant dielectric constant of the SiO_2 was found to be 4.0 at 3.6 GHz using test MIM capacitor structures (shown in Fig. 3.4) of varying overlapping area on a previous wafer and measured using an RF probe. It should be noted that due to fabrication tolerances and thickness variation throughout the wafer, the dielectric constant may vary.

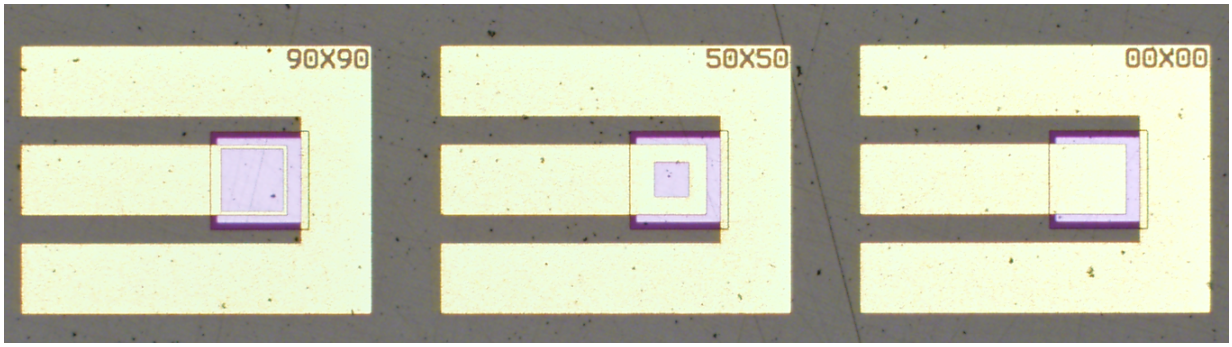

Figure 3.4: Test MIM capacitors for SiO_2 characterization.

The first gold layer is then deposited and patterned as the main metal layer for the RF circuits and co-planar waveguides (CPW), as seen for an SPST device in Fig. 3.5a. A 30/150 nm thick bilayer of Cr/Au is deposited using e-beam evaporation to serve as the

adhesion layer and seed layer. A sufficient thickness is necessary for step coverage over the previous SiO_2 layer. The gold layer is then patterned and electroplated to the final thickness. A thick gold layer is necessary because a gold thickness close to the skin depth will result in RF losses, however cannot be greater than the thickness of the photoresist used to electrolate the gold into. Equation 3.2 gives the skin depth thickness (δ) as

$$\delta = \sqrt{\frac{\rho}{\pi f_o \mu_r \mu_o}} \tag{3.2}$$

where ρ is the bulk resistivity $[\Omega m]$ of the material, f_o is the frequency $[Hz]$, μ_r is the relative permeability, and μ_o is the permeability constant.

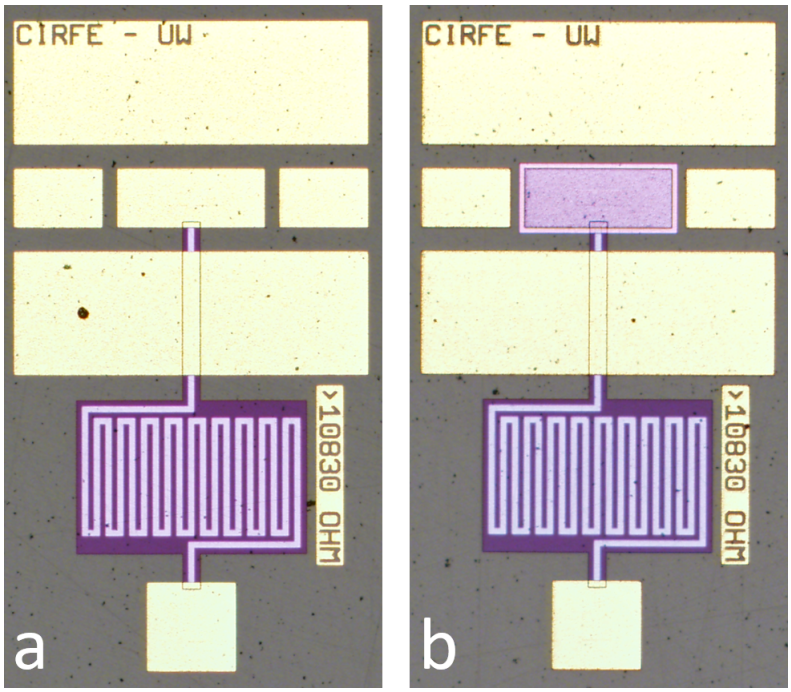

Figure 3.5: MEMS Switch Fabrication: a) Layer 3 (Au) b) Layer 4 (SiO_2).

For the targeted frequency of the phase shifter designs, the lower end of the frequency

range is 3.4 GHz. The corresponding skin depth of gold at 3.4 GHz is 1.3 μm. Therefore, a thick gold layer is necessary to avoid losses at a low frequency, and 2 μm was chosen as the final thickness of gold for the 1st metal layer. At higher frequencies, a thickness of 1 μm would suffice for good RF performance.

Next, a 30 nm Cr adhesion layer and a 0.65 μm SiO_2 layer were deposited using e-beam evaporation and PECVD respectively, to serve as the isolation layer for the bottom electrode of the MEMS structures. The SiO_2 was patterned using RIE and the Cr layer with wet etching. Fig. 3.5b demonstrates this process step used to isolate the bottom electrode for an SPST.

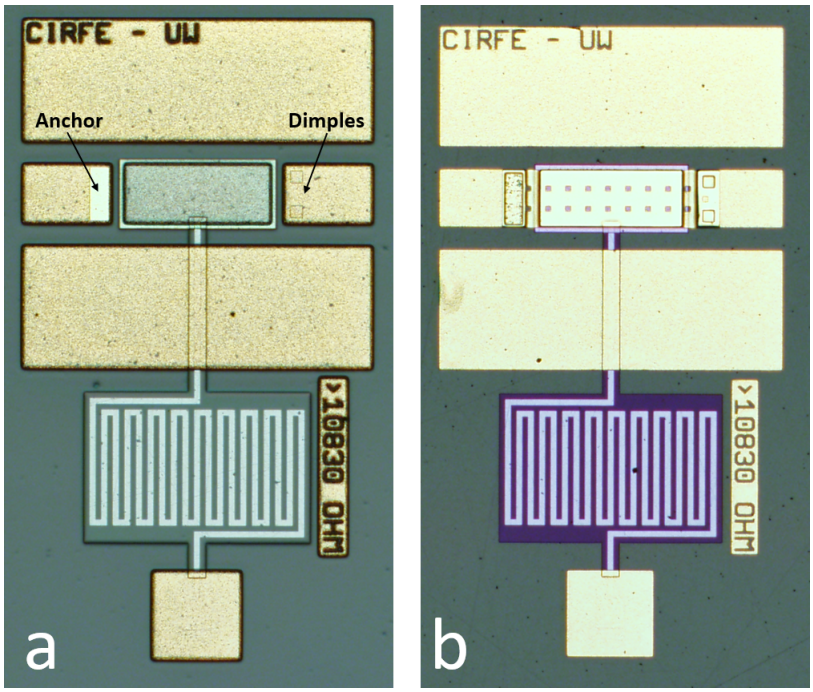

Figure 3.6: MEMS Switch Fabrication: a) Layer 5 & 6 (Dimples/Anchor) b) Layer 7 (Au).

After patterning and characterizing the first four layers of the process, a polyimide

sacrificial layer is spin coated onto the substrate. The polyimide used is PI 2555, and the spin coating and curing recipe is finely tuned to achieve a sacrificial layer thickness of 2.4 μm. An aluminum mask was then used to partially etch into the polyimide 1 μm deep using oxygen plasma dry etching. This 5th mask was used to pattern the contact dimples for the MEMS switches to make Au-Au contact with the first metal layer. This process step was repeated to completely etch the polyimide through the 6th mask and pattern the MEMS anchors and expose the first metal Au layer through them. The resulting anchor and dimple patterns etched into the polyimide sacrificial layer can be seen for an SPST device in Fig. 3.6a.

To form the structural layer for the MEMS switches and the air bridges, a 2 μm layer of gold was deposited and patterned. This was accomplished using a sputtered Au seed layer of 150 nm thickness. Sputtering was used because of its high pressure (random angled delivery) and high energy (improved surface mobility) deposition, allowing for better step coverage of Au of the anchors. The gold was then electroplated through the photoresist mold to the final thickness of 2 μm. Fig. 3.6b presents the fully patterned structural layer for an SPST MEMS switch. Finally, the sacrificial layer was wet etched with EKC 365 and loaded into a critical point dryer (CPD) to be released. The CPD is critical to release the MEMS structures without stiction failure.

3.2 Microfabrication Issues

A few issues arose during the microfabrication process that negatively impacted the yield of the RF-MEMS devices. The chromium layer of the process was damaged during the process. This chromium layer was used for the bias lines to actuate the RF-MEMS switches, as well as the bottom electrode for any MIM capacitors used in the devices. Once the

microfabrication was complete, and the resulting devices characterized, it was found that this chromium layer was damaged. This resulted in a low yield from damage of the bias lines and MIM capacitors not operating with the desired capacitance they were designed for.

Upon further investigation, this was likely due to the etching of the chromium thin film under high power, high temperature oxygen plasma ashing, under the mechanism proposed in [19].

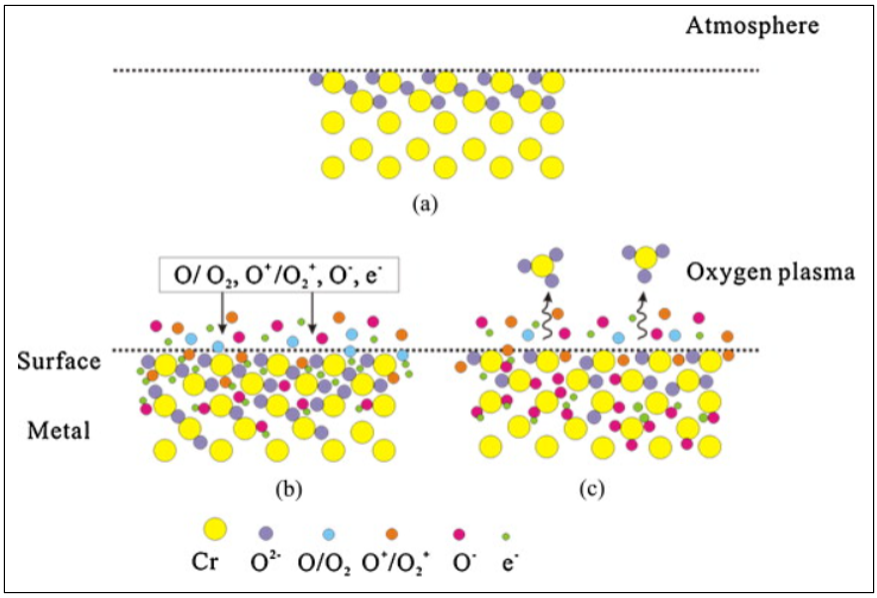

Figure 3.7: Cr etch mechanism by oxygen plasma ashing, a) in atmosphere, b) with power $<$ 200 W, c) when power $>$ 200 W [19].

The patterning of 0.7 μm SiO_2 in layer 2 for the isolation of the bias lines and dielectric for the MIM capacitors, and layer 4 for the isolation of the layer 3 Au (MEMS) bottom electrode) and layer 7 Au (RF-MEMS switch upper electrode), was conducted with high power reactive ion etching (RIE) with C_4F_8 through positive photoresist AZ-3330F as a

mask. The high power oxygen plasma hardened the photoresist and made it difficult the remove. To remove the baked on photoresist, a high power oxygen plasma ashing was conducted using a YES CV-200RFS photoresist asher with a power of 500 W, pressure of 300 mTorr, and temperature of 180°C, until no photoresist residue remained. This was done for both dielectric layers, and was likely the cause of the damage to the chromium layer.

The mechanism of the Cr etching can be seen in Figure 3.7 [19]. During oxygen plasma ashing, Wei et al found that oxygen ions transport through the native chromium oxide to oxidize the Cr [19]. When power is below 200 W, the plasma was found to not have enough energy to dissociate the stable Cr_2O_3, and a limiting thickness of oxide was reached. At room temperature, when higher than 200 W, the Cr_2O_3 was found to dissociate to unstable and volatile forms such as CrO, CrO_2, and CrO_3. Energetic oxygen ions would transport to the Cr layers underneath and further oxidize them, resulting in more etching. It should be noted that power density depends on the size of the asher chamber, and is a more crucial metric than total power.

It is likely that during the two times that ashing were used to descum the photoresist residues from RIE in the microfabrication process, the oxygen ions diffused through the protective SiO_2 layers, and etched the Cr layer underneath. Wei et al found that at when the substrate was heated to 100°C, even 100 W of power was enough to fully remove their Cr film. The adhesive Cr layers used in Cr/Au bilayers were found to be much more resistaive to oxygem plasma etching of Cr, but still found to occur with power $>$ 400 W and temperature $>$ 100°C [19].

The ashing conducted in the fabrication process used power and temperature greater than these values. It is likely that the Cr layer damage during the fabrication was caused by the oxygen plasma ashing step. Future fabrication runs should use alternative methods

to removing the hard baked photoresist residues caused by the RIE.

Another issue that occurred was the outgassing of the polyimide sacrificial layer during the liftoff step for the final gold layer in the fabrication process. A 30 nm Cr layer was deposited onto the final gold layer using e-beam evaporation and patterned using liftoff to serve as protection from wet etching of the seed layer used to pattern the layer 7 gold metal layer.

The liftoff was conducted using a solution of remover PG, heated to 75°C. The solution was heated to aid with the removal of the photoresist layer for liftoff, but due to the high temperature, outgassing of the polyimide sacrificial layer occured. From the high heat, gas escaped from the polyimide, with nowhere to go because of the gold layer covering the substrate. This caused the gold layer to bubble, both visually scarring the polyimide and first gold layer (layer 3) underneath the polyimide, as well as lifting up and warping some structures patterned in the second gold layer (layer 7). The warping of the structures patterned in layer 7 include warping the upper electrodes of the SPST switches, as well as the air bridges. This also affected the yield, and caused some of the released devices to not operate as intended. To address this issue, a lower temperature and longer liftoff process is recommended. If the low temperature remover PG is ineffective in the liftoff process in removing the photoresist, then an alternative solution should be used.

3.3 Testing Setup

In the following chapters, the simulated performance of the fabricated RF-MEMS devices will be compared to the measured results in various testing states. The testing setup to measure the S-parameters of the devices is discussed here.

Fig. 3.8 presents the complete testing setup for the RF devices presented in this thesis. On-wafer RF measurements were conducted using an analytical probe station. The device under test (DUT) was probed using 2 ground-signal-ground (GSG) MPI RF probes, with a pitch of 150 μm and rated for measurements up to 26 GHz. These probes were connected to a Keysight PNA Network Analyzer (N5227B) using phase stable RF cables rated up to 40 GHz, to provide extremely stable device phase characteristics over broad frequency ranges. The cables were connected to ports 1 and 2 of the network analyzer through bias tees (SHF BT45A-HV200) to protect the network analyzer. The bias tees are rated for measurements up to 45 GHz, and a voltage/current limit of 200V/0.4A.

The testing setup was SOLT calibrated using the MPI AC-2 calibration substrate from a range of 10 MHz to 25 GHz. Some measurements were taken up to 40 GHz to observe the response patterns of certain devices at higher frequencies, but it should be noted these measurements are at frequencies above the recommended frequency of the GSG probes of 26GHz. Thus the results are not reliable above 26 GHz. The measurements were conducted at an RF power level of 0 dBm.

To actuated the RF devices to specific states, 100 μm tungsten tip DC probes were used to make contact with the actuation pads and apply bias. A DC power supply was used to apply a voltage bias to actuate the devices, the positive terminal was applied to the signal line of the port 1 GSG probe through the bias tee, whereas the negative terminal was applied through the DC probes onto the MEMS bias pads. The probe and bias placement can be seen in Fig. 3.9.

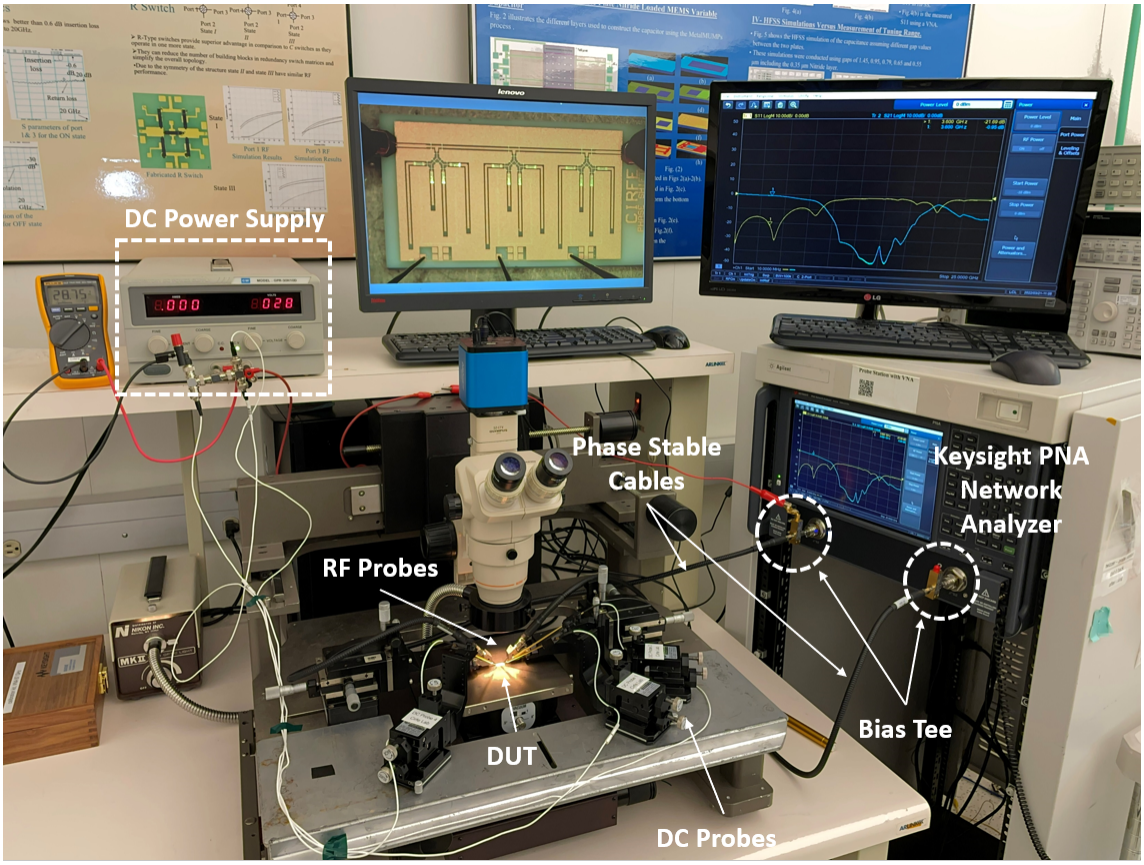

Figure 3.8: RF device testing setup.

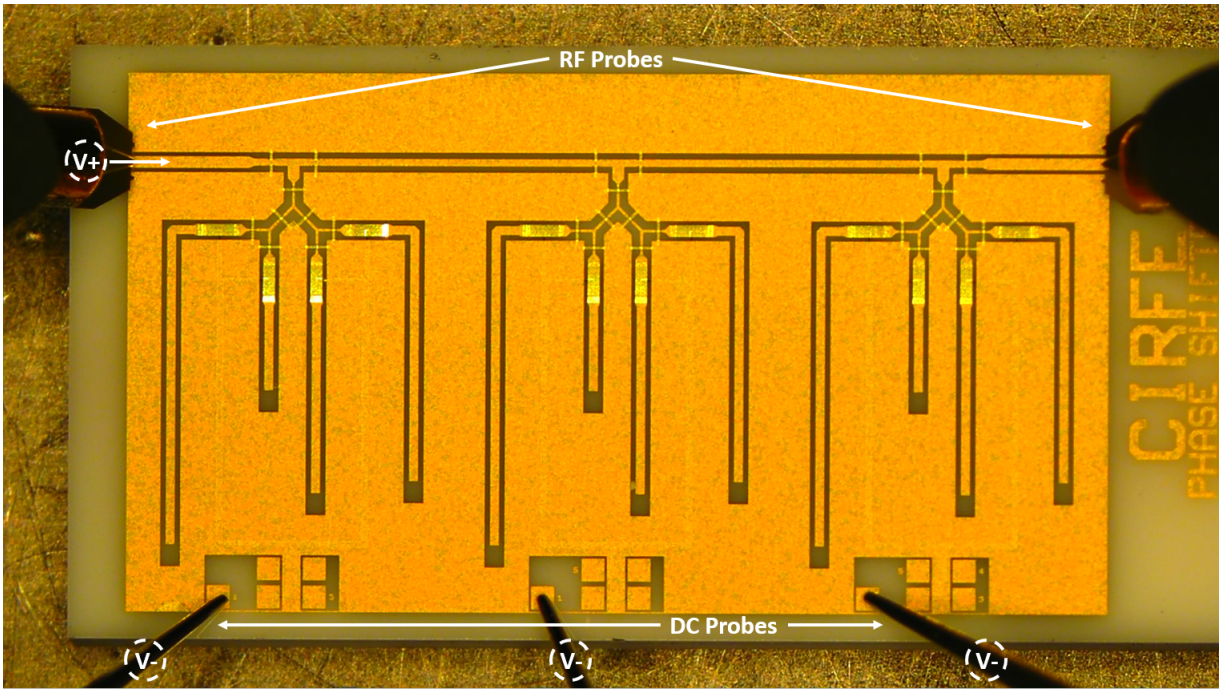

Figure 3.9: On-chip testing bias and probe placement.

Chapter 4

Design and Performance of RF-MEMS Components

RF switches are essential components that make up the foundation of any RF circuit. RF-MEMS switches have the advantage of a high isolation as well as low insertion loss. This chapter goes over the use of metal contact series RF-MEMS switches and their role in designing more complex RF components, such as capacitor banks. For this purpose, a single pole single throw (SPST) RF-MEMS switch was designed, fabricated, tested, and incorporated into more advanced switching components such as the single pole four throw (SP4T) and single pole triple throw (SP3T) RF-MEMS switches.

4.1 Single Port Single Throw (SPST) Switches

The SPST switch is a basic element that was used to design all the more complex switches presented in the later half of this chapter. Therefore, the reliability and performance of this

component was critical in ensuring the success of later switch designs. The SPST switch needed to be reliable, have a low likelihood of failing, and offer great RF performance. Figure 4.1 presents the EM model of the SPST design. The switch was incorporated into a 50 Ω co-planar waveguide (CPW) transmission line, with a signal line width of 100 μm and a CPW gap of 41 μm. One end of the switch is anchored to the signal line, while the other is a free end, with contact dimples patterned into it.

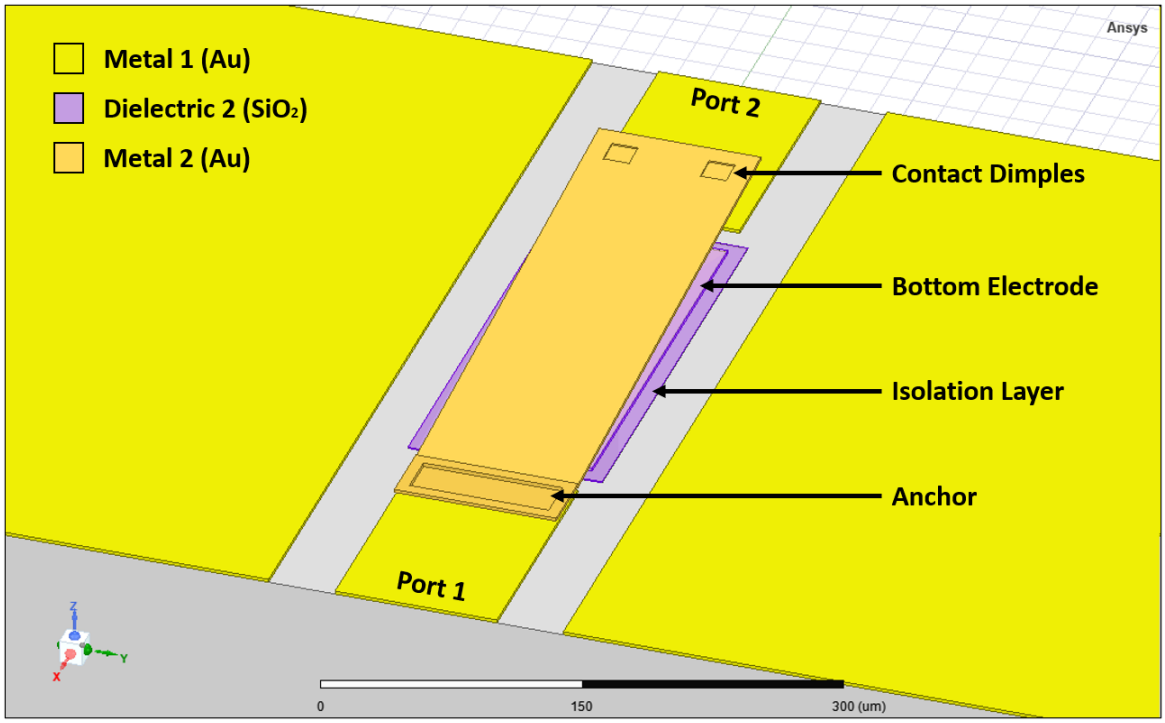

Figure 4.1: EM model of a single pole single throw (SPST) switch.

The operation of the SPST switch involves applying a voltage difference between the upper electrode of the switch (the signal line) and the bottom electrode of the switch. After a certain threshold voltage, the resulting attractive electrostatic force pulls the upper beam of the MEMS switch from its OFF (up) state, to its ON (down) state, shown in Figure

4.2. When the electrostatic force of the voltage difference overcomes the opposing spring force of the MEMS cantilever structure, the switch collapses onto the substrate, achieving 'pull-in'. When the SPST is in the ON state, the RF signal can flow freely from one end of the switch to the other. A layer of dielectric, in this case silicon dioxide (SiO_2), isolates the bottom electrode metal layer and prevents contact between the two electrodes, preventing any DC current from flowing.

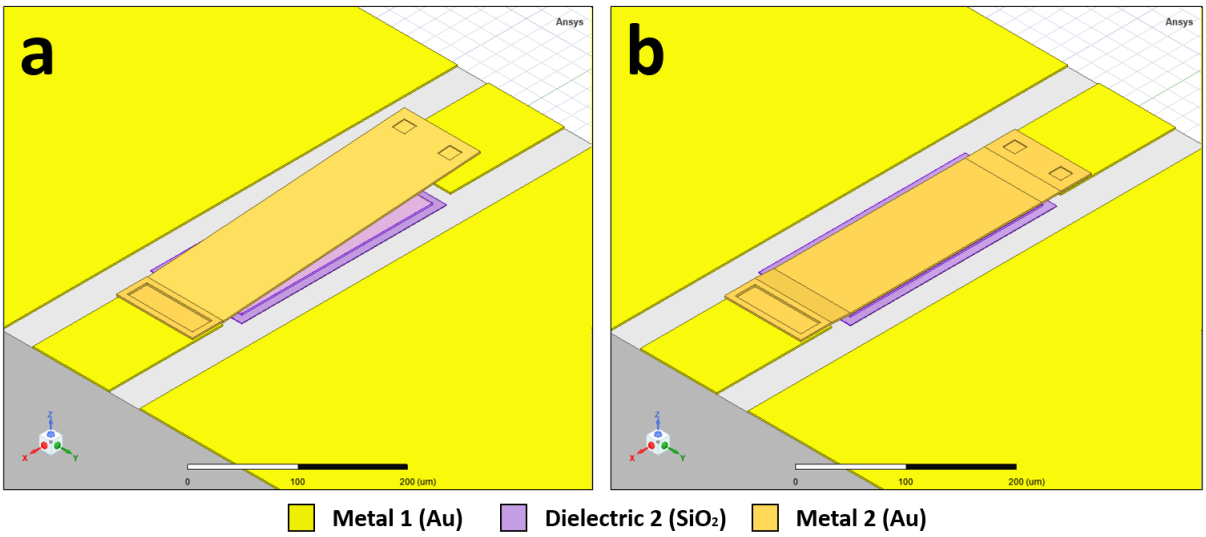

Figure 4.2: SPST states a) OFF b) ON

The SPST switch was carefully designed while considering both the pull-in voltage of the design, and the breakdown voltage of the dielectric material used. In the case where the pull-in voltage is greater than the breakdown voltage of the isolating layer, the applied voltage will exceed the breakdown voltage before ever reaching pull-in. When this occurs, a portion of the dielectric becomes electrically conductive, effectively shorting the device [20]. This results in a DC current flowing through the switch that may either burn out the device, as well as damage the testing equipment.

A dielectric with high breakdown voltage is used to combat this. A study by Bartzsch et al [21] found that the breakdown field for SiO_2 was 5.6 MV/cm as opposed to 2.4 MV/cm for Si_2N_3. Aluminum nitride (AlN) films were found to have a breakdown field at 2.1 MV/cm [22]. Very thin films under 100 nm may experience partial conductivity due to an electron tunneling effect. A 0.65 μm thick layer of SiO_2 was used for the isolation layer.

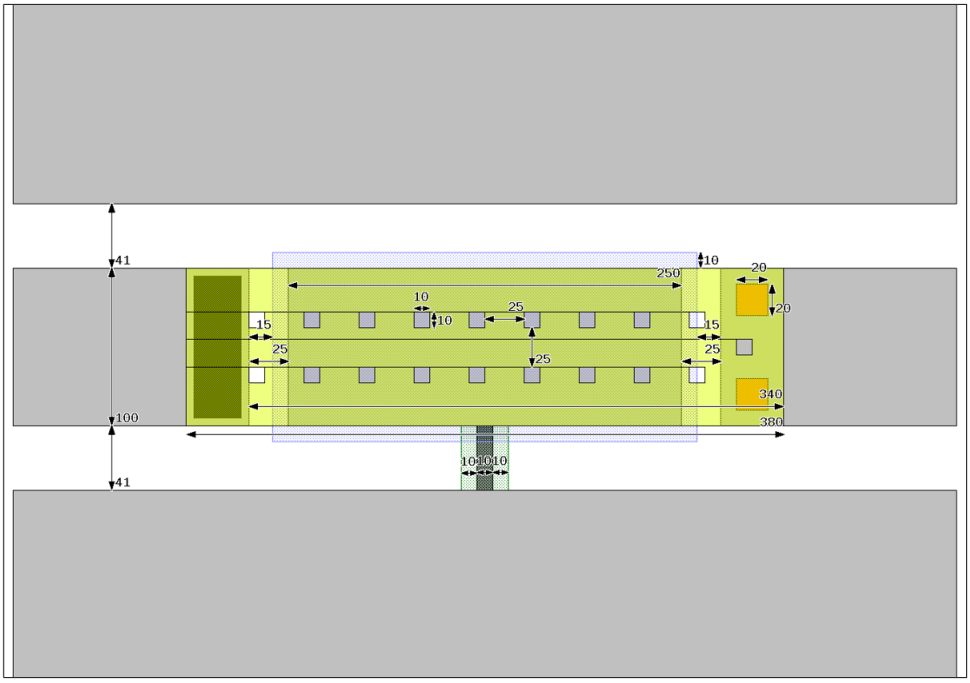

Figure 4.3: SPST dimensions.

A MEMS switch design featuring a low pull-in voltage can also be used to combat this issue. However, a low pull-in voltage means that the upper electrode cantilever must be closer to the bottom electrode and signal line. This would result in a lower RF isolation in the OFF state for the SPST switch. Therefore, a balance between the pull-in and breakdown voltage must be met when designing the SPST RF-MEMS switch. The SPST

dimensions can be seen in Figure 4.3 and Table 4.1.

Table 4.1: SPST Dimensions.

Parameter	**Value** (μm)
Actuation Gap	2.5
Anchor Length	90
Anchor Width	30
Bottom Electrode Length	250
Bottom Electrode Width	100
Cantilever Length	340
Cantilever Width	100
Contact Dimple Width	20
CPW Gap	41
CPW Width	100
Release Hole Spacing	25
Release Hole Width	10

Using insight gathered from previous microfabrication runs and device iterations, the cantilever beam of the SPST is expected to bend up due to material film stress. This effect directly correlates to a higher device pull-in voltage, but also improves the RF isolation in the OFF state. A modified version of the SPST is designed to mitigate this bending and reduce the required applied voltage to reach pull-in.

The value of pull-in voltage between two electrodes in a MEMS cantilever is given by Eq. (4.1):

$$V_{PI} = \sqrt{\frac{8Kg^3}{27\varepsilon_o A}} \tag{4.1}$$

where K is the effective spring constant of the cantilever, g is the actuation gap between the upper cantilever and bottom electrode, ε_o is the permittivity of free space, and A is the total overlapping electrode area. Pull-in voltage is proportional to the root of the spring constant. It has been previously reported in literature that variations of support beams in cantilevers can be used to reduce the effective spring constant in MEMS devices, thereby lowering the pull-in voltage requirement of the capacitive MEMS switch [1].

Figure 4.4 compares the original and modified variation of the SPST switch. The interface between the cantilever and the anchor is modified in the variation such that a gap of 10 x 45 μm is added where previously there were only two release holes of 10 x 10 μm. This is expected to reduce the effective spring constant of the cantilever, reduce the amount that the cantilever bends up, and decrease the pull-in voltage of the structure.

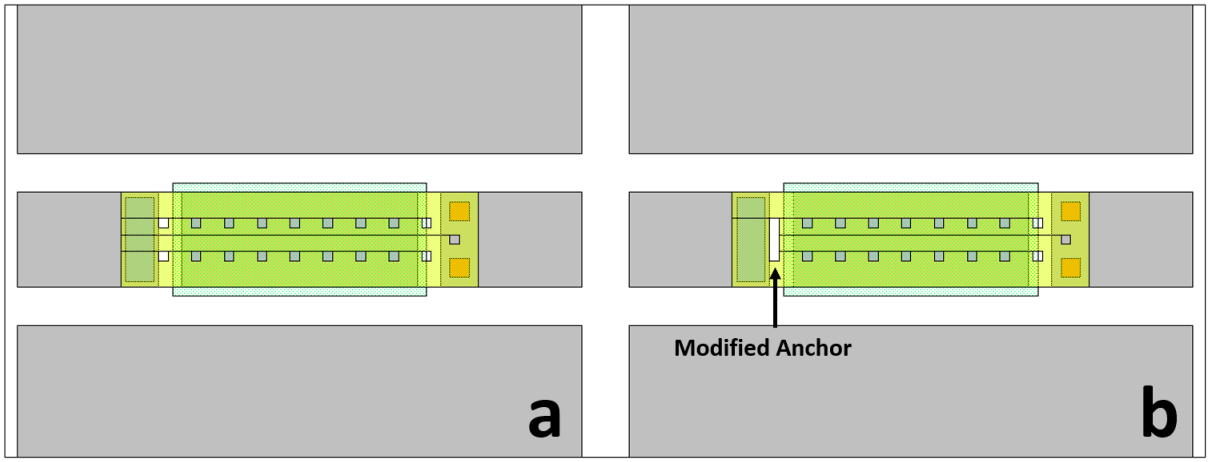

Figure 4.4: Comparing (a) initial and (b) modified SPST designs.

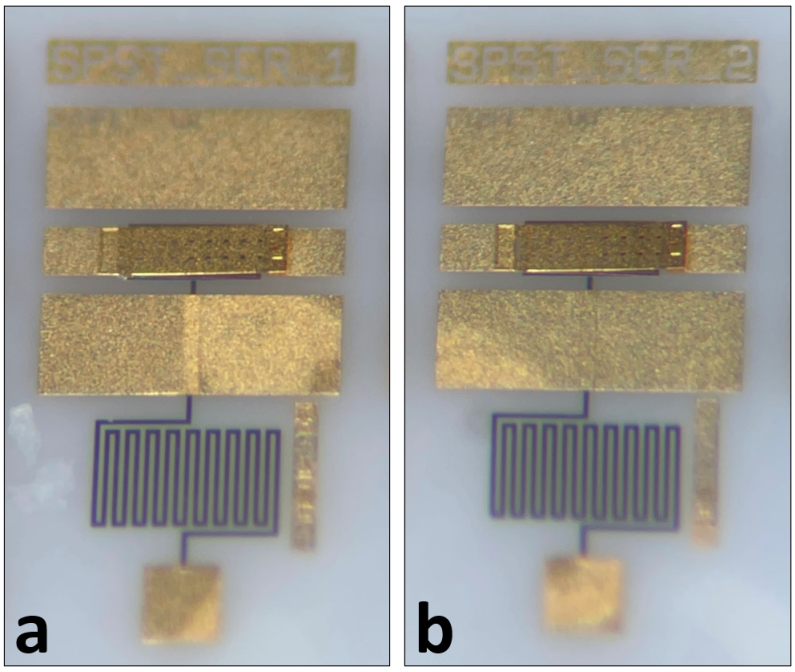

Figure 4.5: Microfabricated (a) initial and (b) modified SPST RF-MEMS switch.

Once the two SPST switch designs were fabricated and released, an optical profilometer was used to measure the profile of their cantilevers. Figure 4.6 displays the profile of the initial SPST device after release. The switch warps up as expected due to the film stress, with an effective angle calculated at 3.9°. The total warping in the Z-axis is determined using the difference in height between the MEMS anchor and the tip of the free end, and is found to be 22.55 μm.

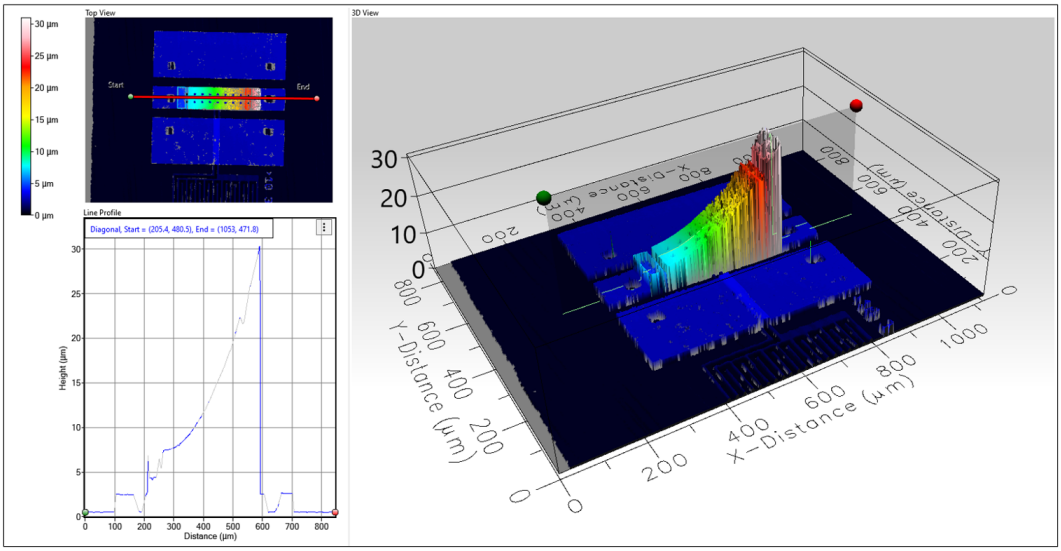

Figure 4.6: SPST profilometry scan.

The optical profilometry scan of the modified SPST device with smaller anchor contact can be seen in Figure 4.7. From the profilometer scan, the modified SPST is measured to have a lower effective angle at 3.55°, and a total warping displacement in the Z-axis measured at 20.5 μm.

Both initial and modified designs of the SPST RF-MEMS switch were released, tested, and found to have an average pull-in voltage of 55 V and 50 V respectively, varying slightly device to device. This shows that changing the anchor improved the pull-in voltage and

reduced the bending of the cantilever. There is a likelihood of this modification having a negative impact on the reliability and lifetime of the switch. With continuous actuation, the switch may fail sooner due to a lower amount of contact length from the anchor to the beam.

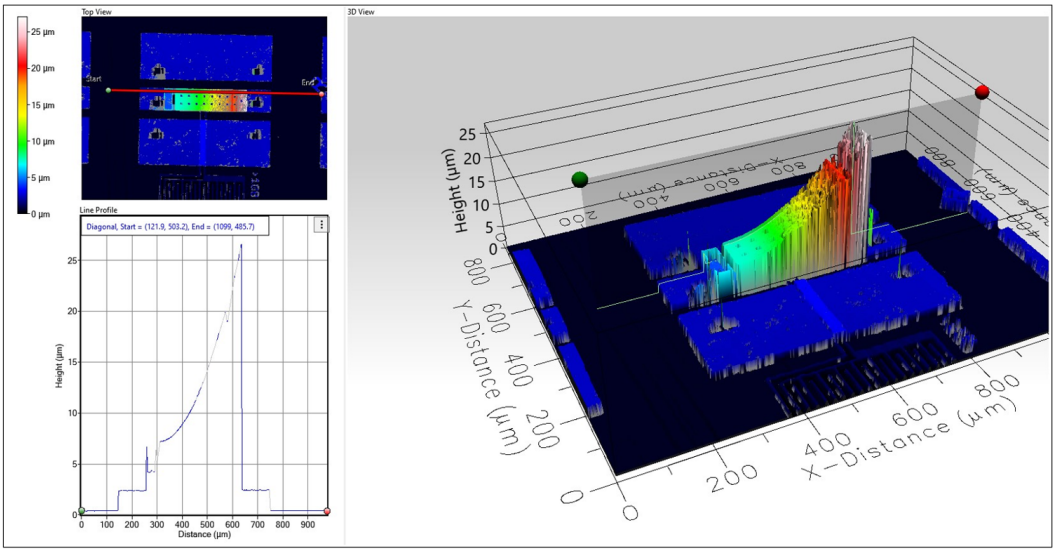

Figure 4.7: SPST version 2 profilometry scan.

Figure 4.8 plots the measured RF performance of the MEMS SPST switch in the OFF state, and compares it to the corresponding EM simulated performance. The two plots exhibit a good match between the measured and simulated performance, with the measurement results following the profile of the simulation closely. The isolation of the switch in the OFF state was simulated to be better than 20 dB from DC to 22 GHz, and the measurement results show the same amount of isolation up to 20 GHz. The EM simulation expected the return loss in the OFF state to be better than 0.2 dB for a frequency range of DC to 25 GHz, but the measurement results have the return loss performing worse, going as bad as 0.4 dB at 25 GHz.

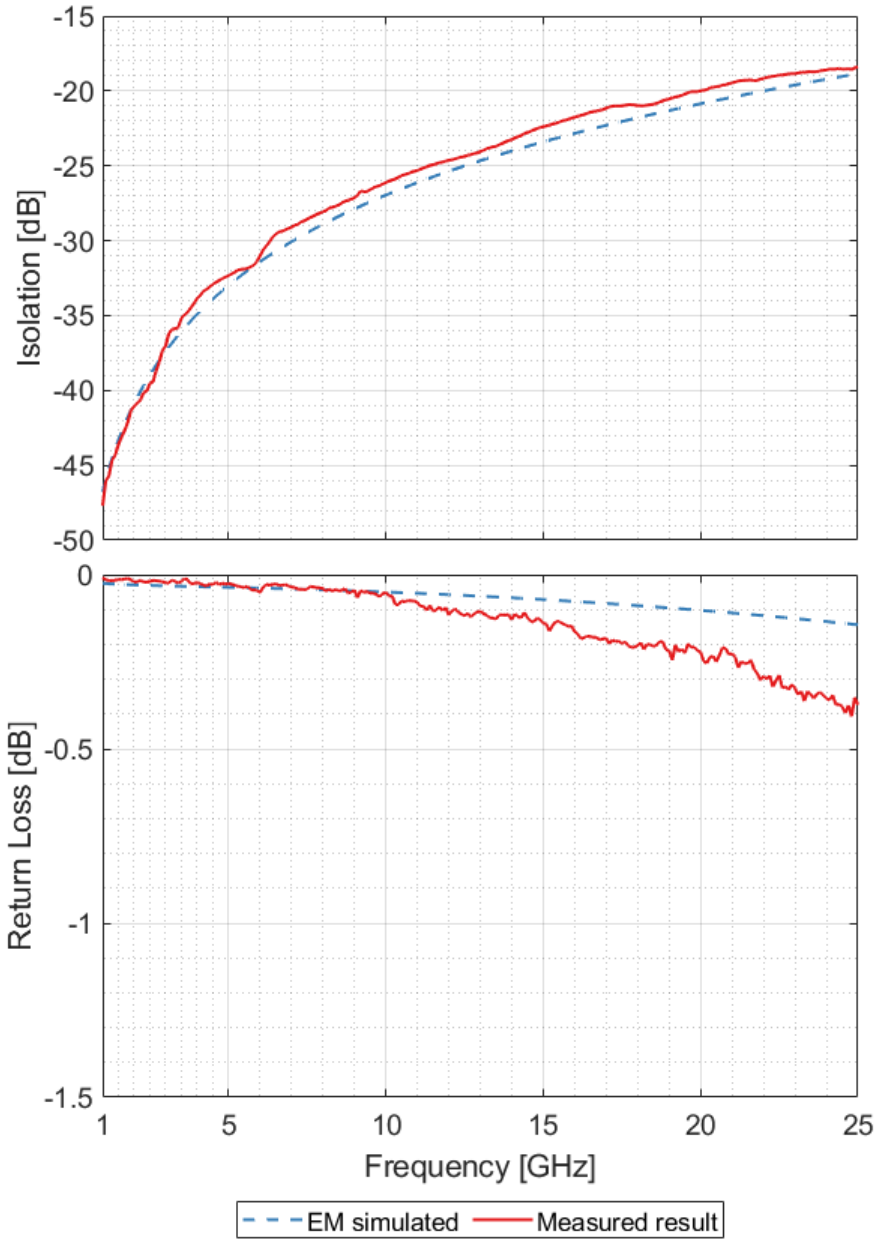

Figure 4.8: Measured and simulated RF performance of the released RF-MEMS SPST switch in the OFF state.

The RF performance of the released MEMS SPST switch in the ON state is compared with its EM simulation counterpart in Figure 4.9. The shapes of the measured and simulated RF performance do not match as closely as in the OFF state presented above. However, the shapes and profiles of the curves are still similar. The insertion loss of the SPST in the ON state was simulated to perform better than 0.5 dB from DC to 25 GHz. The measured response shows that the insertion loss went as low as 0.65 dB for the same frequency range.

The SPST return loss in the ON state was simulated to be better than 27 dB from DC to 25 GHz, but was measured to be much worse. The performance is still acceptable, with return loss better than 20 dB from DC to 25 GHz. The profiles of both curves resemble each other, but the measured response performs worse.

The measured RF performance of the released RF-MEMS SPST switches correlates well with the EM simulation results, in both OFF and ON states. The performance of the switches at low frequencies was especially good, which is great since the target frequency for the more complicated RF devices is also at lower frequencies (around 3.6 GHz), and the SPST switches were used as fundamental building blocks for the more complicated designs.

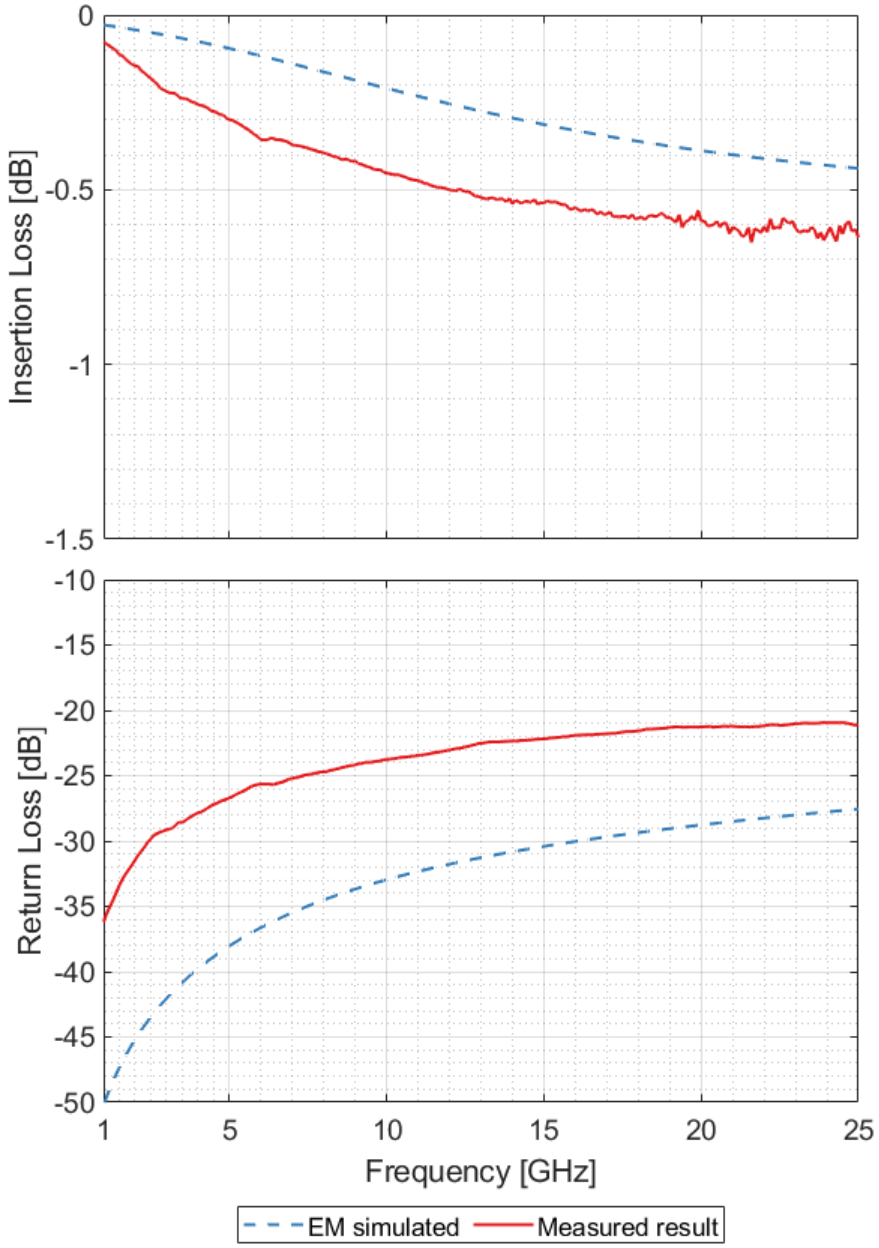

Figure 4.9: Measured and simulated RF performance of the released RF-MEMS SPST switch in the ON state.

4.2 Air Bridges

In the following RF-MEMS component designs presented later, air bridges were included at transmission line and design discontinuities. Air bridges are typically used in RF CPW circuits to connect ground planes together, as well as suppress the parasitic coupled slot line modes caused by said discontinuities [23]. An L-turn discontinuity in a CPW circuit is shown in Figure 4.10 [24].

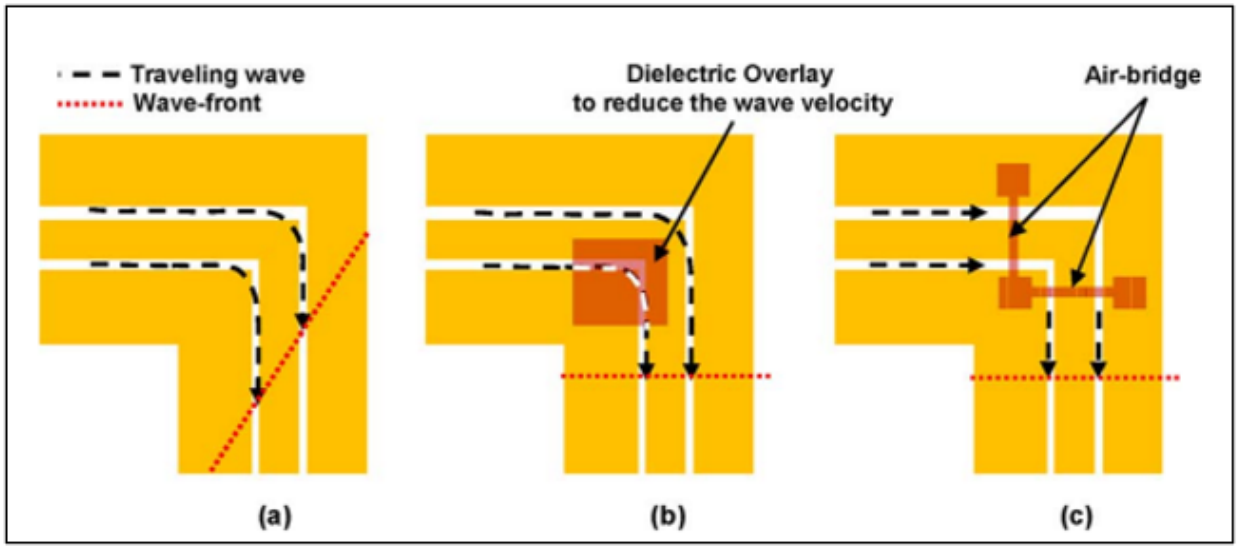

Figure 4.10: CPW L-turn discontinuity showing (a) discontinuity from difference in traveling path length, (b) solution using dielectric slab, and (c) solution using air bridges [24].

Figure 4.10 a) shows the outer ground conductor has a longer travel path for the RF signal than the inner ground conductor. This imbalance of phase occurs at discontinuities such as T-junctions, L-turns, and U-turns, causing a degradation in RF performance (insertion loss and return loss) of CPW circuits [24].

To address this issue and remedy the mismatch of phase of the wavefronts and minimize radiating slot modes, examples of dielectric slabs (Figure 4.10b) [25], air bridges (Figure 4.10c) [26], and wire bonds [27] have been utilized in literature. Each of these approaches adds local parasitics to the transmission line, changing the characteristic impedance and impacting performance.

Using air bridges rather than wire bonds to address the phase mismatch and slot line modes was predicted to have better RF performance due to the smaller footprint of air bridges [27]. However, a disadvantage of air bridges was the complicated fabrication method for realizing them, as opposed to the simple implementation of wire bonds. Air bridges were realized in this work very easily, using the same fabrication method as the RF-MEMS structures to realize the air bridges which were essentially metal cantilevers fixed at both ends.

Even though the footprint of the air bridges was small, a local parasitic capacitance would be introduced when including them in RF devices, effectively decreasing the characteristic impedance of the transmission line. This would negatively impact the line performance metrics such as return and insertion loss. Derived using the telegrapher's equations, Eq. (4.2) represents the general expression for the characteristic impedance of a transmission line.

$$Z_o = \sqrt{\frac{Z'}{Y'}} = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}} \tag{4.2}$$

where Z_o is the characteristic impedance of the transmission line, ω is the angular frequency, and Z' is the series impedance, Y' is the shunt admittance, R' is the resistance, L' is the inductance, G' is the conductance, and C' is the capacitance of the transmission line per unit length.

For lossless transmission lines, resistance and conductance become very small and can be approximated using the relation below.

$$G' << j\omega C'$$

$$R' << j\omega L'$$

Ignoring the resistance and conductance contribution from the equation, the characteristic impedance of the transmission line reduces to Eq. (4.3).

$$Z_o \approx \sqrt{\frac{L'}{C'}} \tag{4.3}$$

From Eq. (4.3), the relation shows that the increase in capacitance originating from adding an air bridge to the CPW decreases the localized characteristic impedance of a transmission line. This leads to a mismatch of line impedance and negatively impacts performance. An EM simulation was conducted to verify this conclusion, where line performance was found to decrease with the addition of air bridges to a co-planar waveguide.

To address this unwanted change in characteristic impedance, the inductance of the transmission line can be locally increased. This can be accomplished by reducing the width of the signal line under the air bridge [28]. By increasing the line inductance per unit length, the characteristic impedance of the CPW near the air bridge can be brought up to 50 Ω, mitigating the effect of adding the air bridge somewhat. An EM model of an air bridge, and the air bridge compensation applied to the transmission line, can be seen in Figure 4.11.

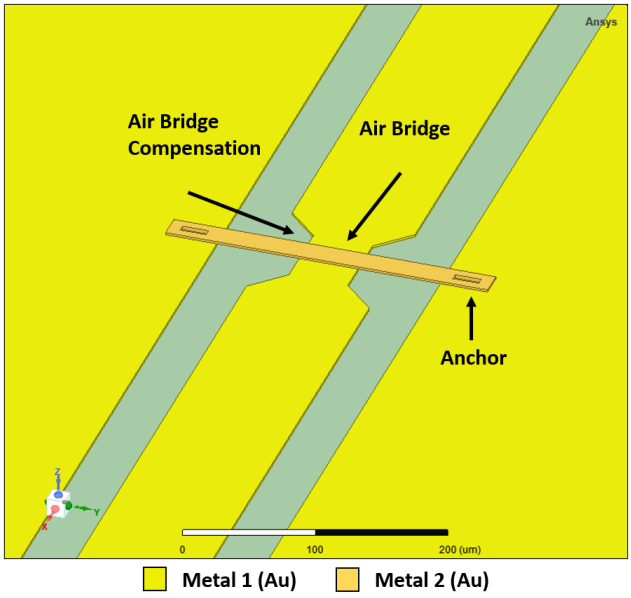

Figure 4.11: EM air bridge model.

The parameters and dimensions of the air bridge and CPW line can be seen in Table 4.2 and Figure 4.12. The CPW was designed with with a constant total ground to ground plane width of 182 μm, with the characteristic impedance of the CPW determined by the width of the signal line. For a value of 50 Ω, the corresponding CPW width for this setup was 100 μm. The CPW thickness was the same as the metal 1 thickness presented earlier, at 2 μm. Likewise, the air bridge thickness was the same value as the metal 2 thickness presented earlier, at 2.5 μm.

The length of the air bridge compensation was fixed at 60 μm, centered under the air bridge. The width and length of the air bridge compensation transition is listed as X μm in Table 4.2. An EM simulation was conducted to find the optimal relation between CPW width and air bridge compensation width, for the given microfabrication process specifications and dimensions.

Table 4.2: Air bridge and CPW dimensions.

Parameter	**Value** (μm)
Air Bridge Length	262
Air Bridge Width	20
Air Bridge Gap	2.5
Air Bridge Metal Thickness	2.5
Air Bridge Compensation Length	60
Air Bridge Compensation Width	X
Anchor Length	25
Anchor Width	10
CPW Gap	(182-Width)/2
CPW Width	Width
CPW Metal Thickness	2

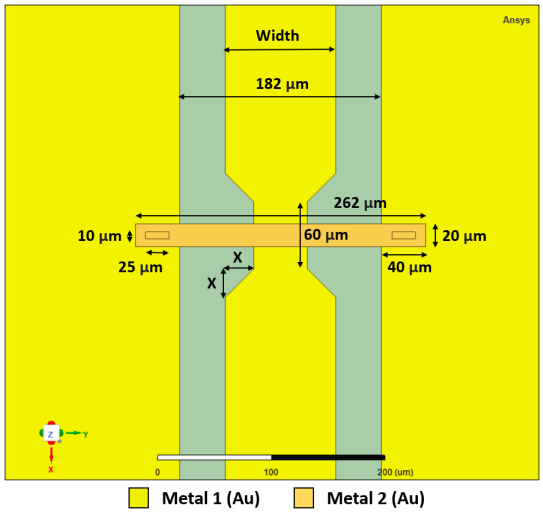

Figure 4.12: Air bridge dimensions

For CPW signal line widths of 20 to 100 μm, a parametric sweep of the air bridge compensation width X was conducted to find the best performing values of X, from DC to 40 GHz. These compensation widths were then plotted and used to find the equation for the best fit, relating air bridge compensation width to the width of the CPW signal line.

From the EM simulation, the relation for the optimal value for air bridge compensation width X with regards to CPW signal line width was found to be

$$X = \frac{\text{CPW Width}}{4} + 1\mu\text{m} \tag{4.4}$$

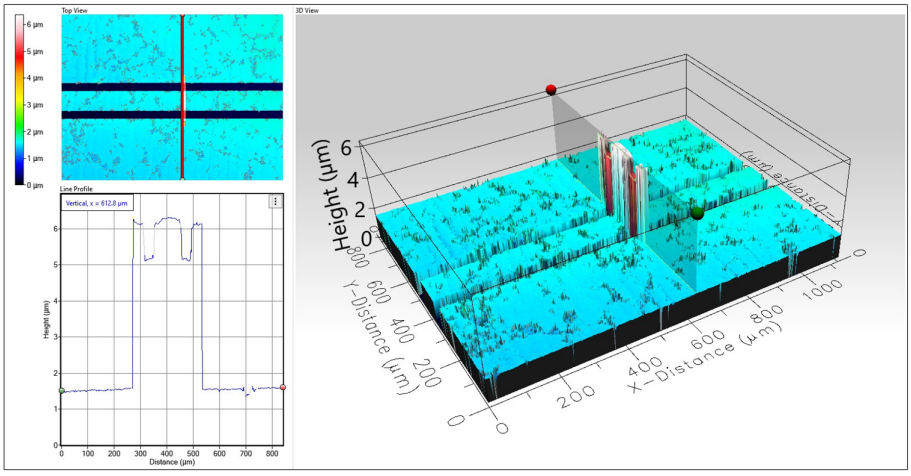

Figure 4.13: Air bridge profilometry scan.

Figure 4.14 shows the results of the EM simulation sweeping for CPW widths from 20 to 100 μm, showing the performance of a CPW line with an air bridge with a) no compensation, and b) air bridge compensation according to the Eq. (4.4). After applying the air bridge compensation, it is clear that the performance of the CPW line at higher frequencies was improved, showing a much better return loss. Figure 4.13 shows the optical profilometry scan of a released air bridge structure on a CPW line.

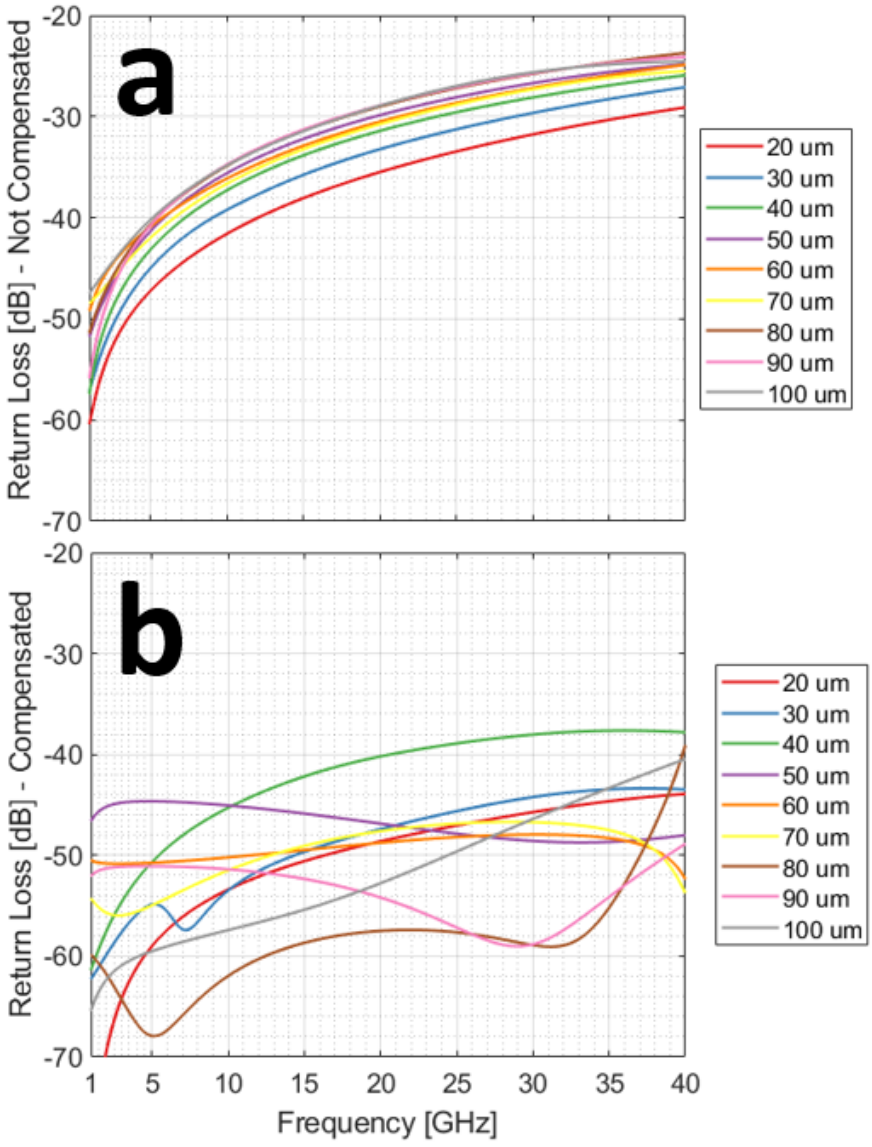

Figure 4.14: Return loss of CPW line with air bridge with, a) no compensation, and b) air bridge compensation according to Eq. (4.4), with increasing signal line width.

4.3 Single Port Four Throw (SP4T) Switches

A single port four throw (SP4T) switch was designed using the previously reported RF-MEMS based SPST switch and air bridge as components. The design features an input port that exits into four ports, controlled by four individual SPST switches that control the path of the RF signal. A CPW junction was used to connect the four SPST switches in parallel. This CPW junction was carefully designed to create a good match and simulated response for when the switch was in the OFF and ON states.

The design of the junction was achieved using EM simulations, keeping the CPW lengths fixed while adjusting the width of the connecting junction CPW lines and keeping the ground to ground width constant. Air bridges were used in this design to connect the ground planes as well as for phase matching. The EM model for the SP4T design can be seen in Figure 4.15.

Symmetry was maintained between all four ports throughout this SP4T design. This provided the advantage of keeping the loading from each of the SPSTs and ports identical, making the design of this switch, and subsequent components that used this switch in their design, very straightforward. Thanks to this, the optimization of the junction was simplified, and conducted for the case when only one SPST switch was actuated. Because of symmetry, this was the equivalent of optimizing the design for all ports, since there is no difference from any case when a single switch was actuated. The SP4T CPW junction width was adjusted for the scenario of only one ON switch (ex. port 3 ON, ports 2, 4, 5 OFF), and extrapolated for the ON state for all other ports.

Figure 4.16 displays the EM simulated RF performance of the SP4T switch in the OFF state, with a parametric sweep for the CPW junction width from 20 to 60 μm. As CPW junction width increases, the isolation of the switch in the OFF state at higher frequencies

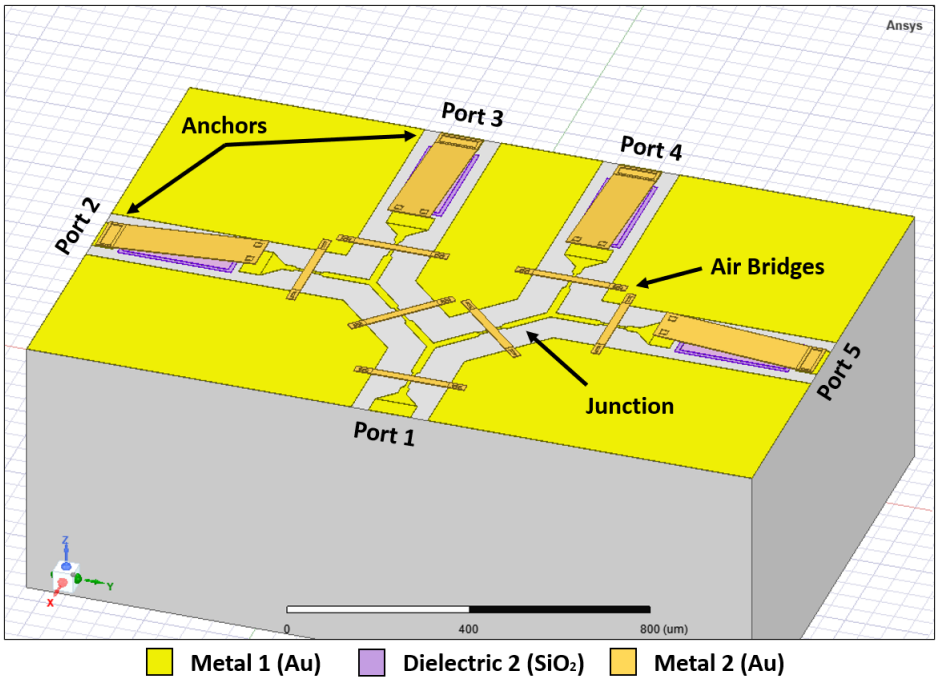

Figure 4.15: EM SP4T model.

suffers slightly, while the return loss of the switch improves. The return loss improves from 0.5 dB to around 0.3 dB with increasing width from 20 to 60 μm.

The RF performance of the EM simulation of the SP4T switch in the ON state is shown in Figure 4.17, with the same parametric sweep in junction CPW width. The return loss of the SP4T in the ON state is clearly the limiting parameter, with the smallest acceptable performance frequency ranges. From a width value of 20 to 60 μm, the frequency at which simulated return loss is better than 20 dB decreases from 16 GHz to 8 GHz. The best performing variation, 20 μm, was used for the final design of the SP4T device, to achieve the greatest bandwidth of acceptable performance.

While the trend is clear that lower width values will yield better results, the width of the CPW junction was limited to 20 μm. This is because the CPW signal line width after applying the air bridge compensation must be taken into consideration. For a signal line width of 20 μm, the total width of the CPW signal line under the air bridge would be 6 μm. A smaller CPW width would reduce the actual width value after compensation even further, approaching a very small feature size that might be too unrealistic for the microfabrication process. A 6 μm width leaves room from the minimum feature size realizable from the microfabrication process, where even with the process tolerances, will still result in a reliable amount of gold left for an RF signal to flow through.

The SP4T switch designs were fabricated, released, and tested. Figure 4.19 plots the measured RF performance of the realized RF-MEMS SP4T switch in the OFF state, and compares it to the corresponding simulated RF performance. RF probes were landed on ports 1 and 3 of the device, and all SPST switches were left unactuated. The measurement results match up well with the simulated response. The isolation of the measured SP4T switch shows a response better than 20 dB from DC to 20 GHz, and a return loss better than 1 dB from DC to 22 GHz. The SP4T device shows great performance especially at

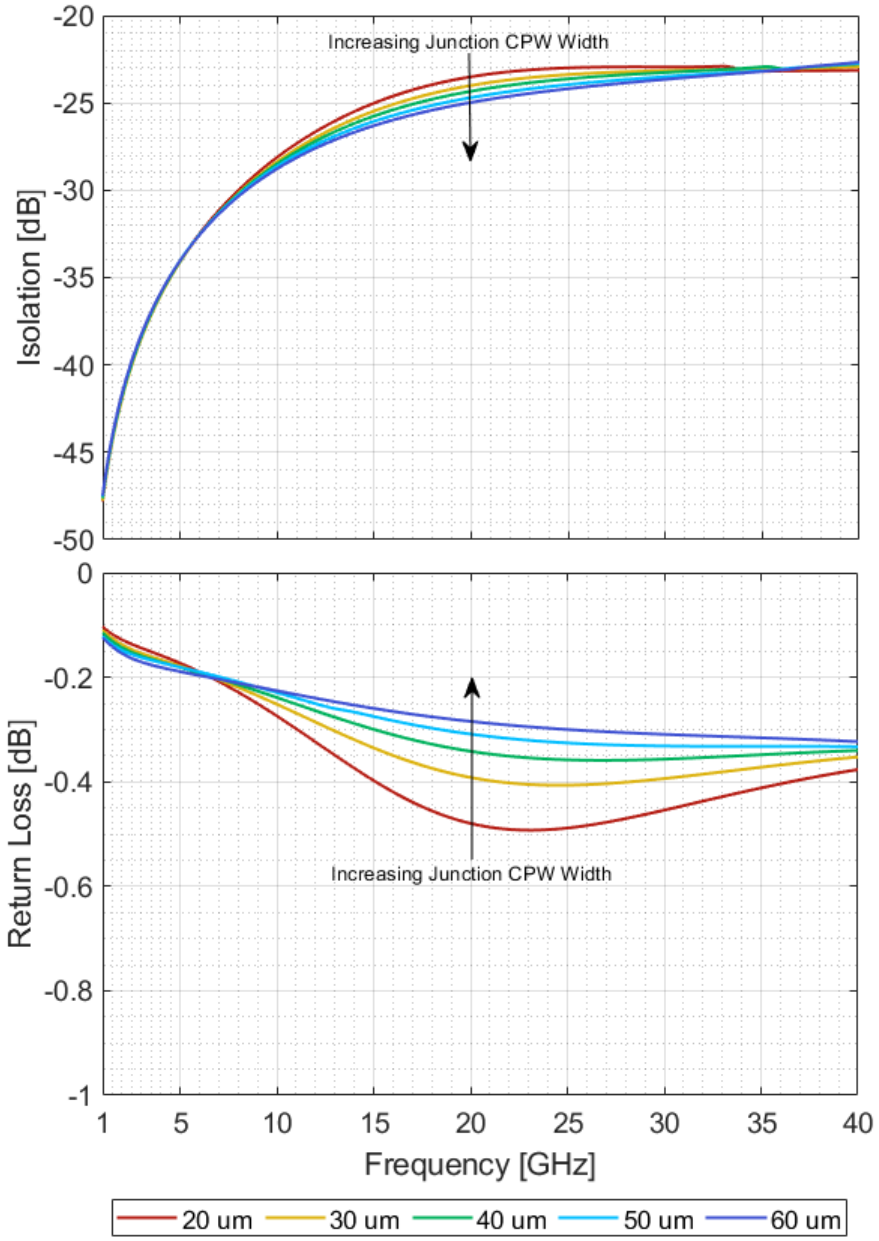

Figure 4.16: EM simulated RF performance of the SP4T switch in the OFF state, with junction CPW width swept from 20 to 60 μm.

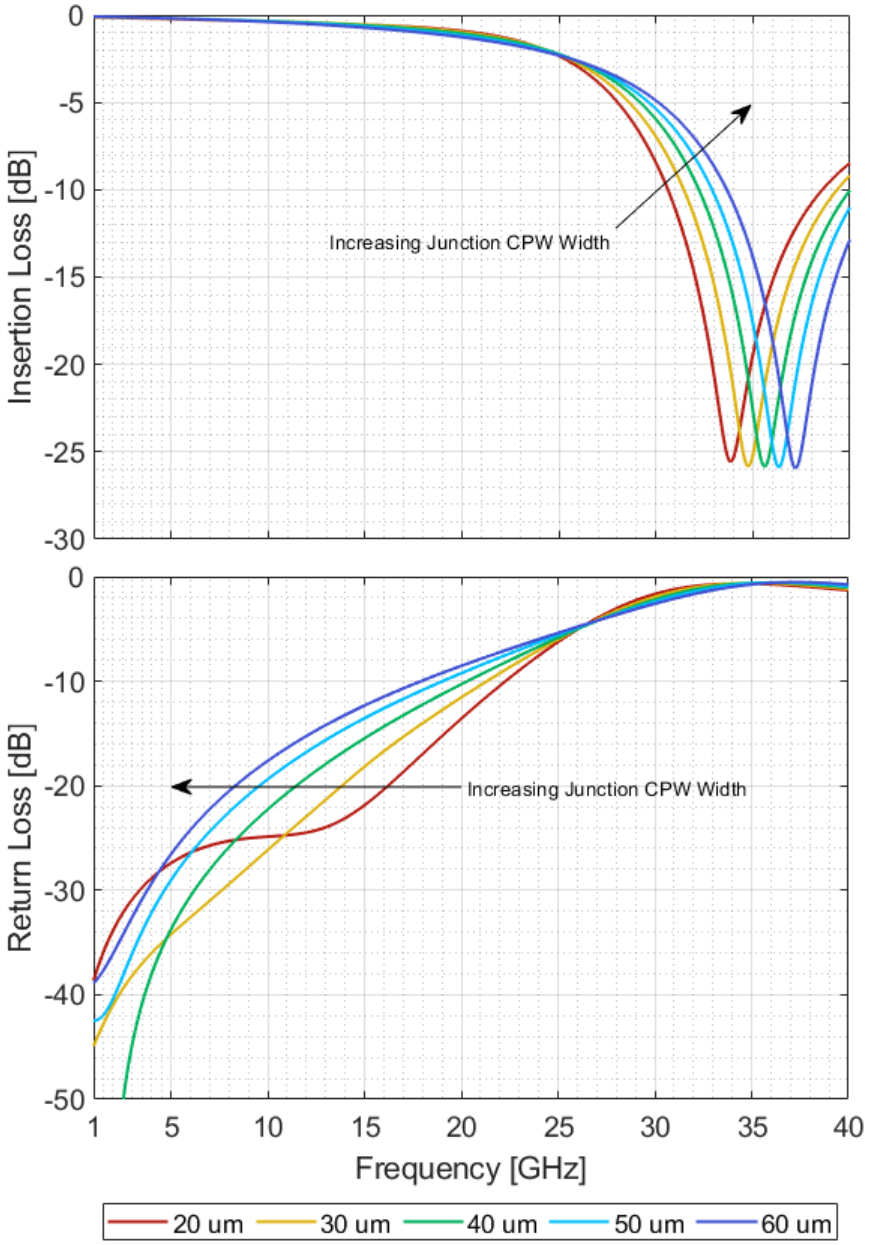

Figure 4.17: EM simulated RF performance of the SP4T switch in the ON state, with junction CPW width swept from 20 to 60 μm.

lower frequencies. Because of symmetry in the SP4T design, these OFF state results can be extrapolated for ports 2, 4, and 5. The maximum frequency for reliable measurements that the RF probes used were rated for is 225 GHz, and should be taken into consideration when viewing test results. Measured behaviour of the device beyond this range is not as reliable and should only be used to roughly visualize the performance at higher frequencies.

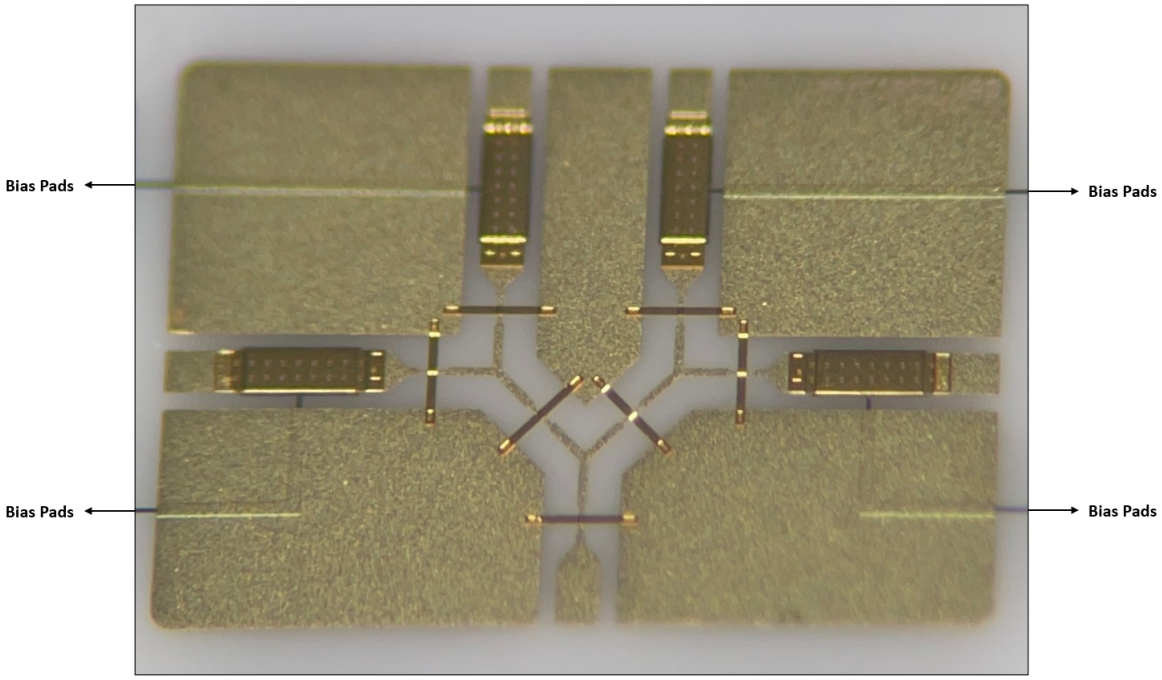

Figure 4.18: Microfabricated SP4T RF-MEMS switch.

The RF performance of the released SP4T switch was measured in the ON state, where the probes were landed in ports 1 and 3. The SPST corresponding to port 3 was actuated using a DC probe, which allowed the RF signal to flow between the two ports. Figure 4.20 shows the measured and simulated RF performance of the SP4T switch in the ON state, where port 3 is ON and ports 2, 4, and 5 are in the OFF state.

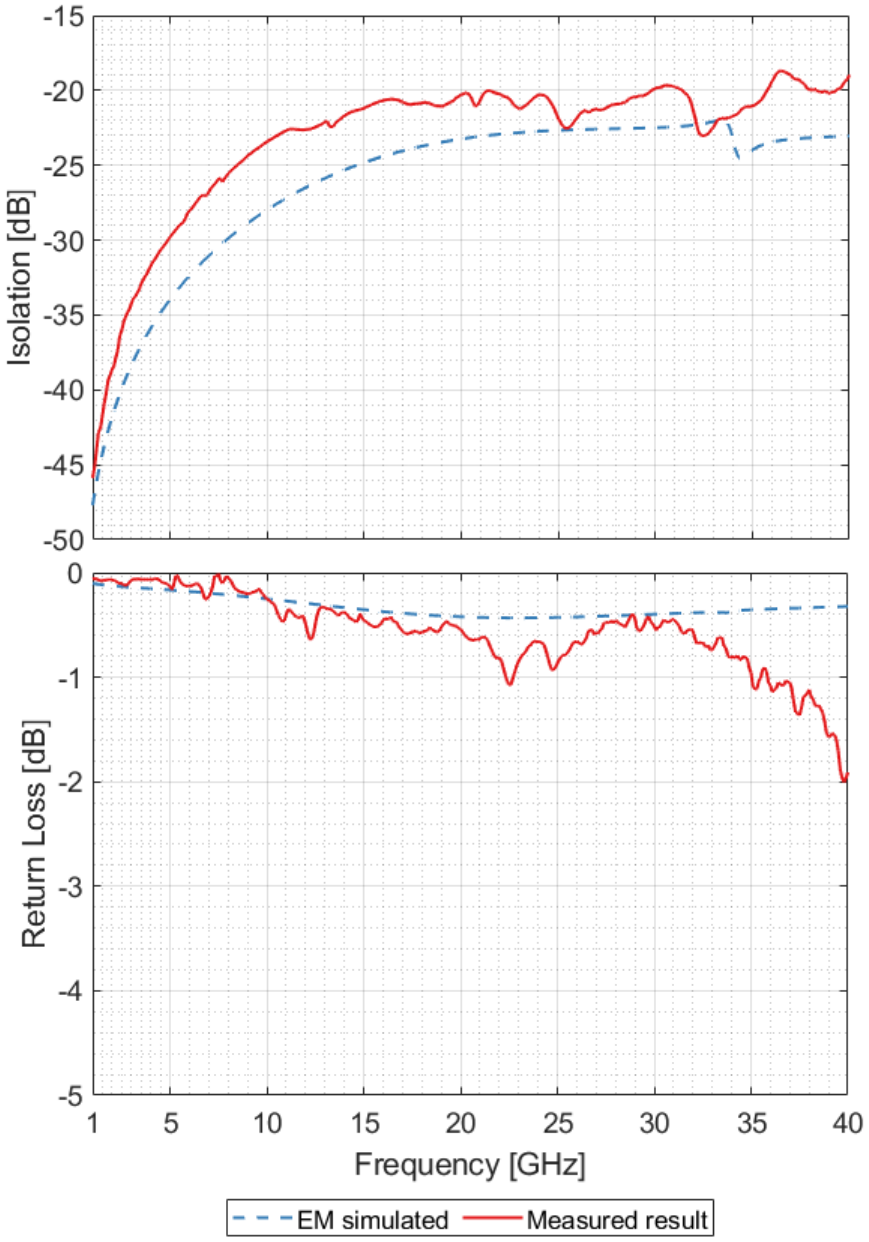

Figure 4.19: Measured and simulated RF performance of the released RF-MEMS SP4T switch in the OFF state.

The measured switch performance greatly mimics the expected performance from the EM simulation. The insertion loss performs almost identical to its EM simulated counterpart, with the response after 25 GHz deviating slightly. The measured return loss of the SP4T performs even better than expected, showing great performance at low frequencies. However, this plot deviates from the EM simulation results at the lower frequencies, likely due to microfabrication tolerances causing a deviation in feature dimensions at the CPW junction signal line width. Looking back at Figure 4.20, as junction CPW width increases, the return loss of the SP4T switch in the ON state smoothens out and improves at lower frequencies, but suffers at higher frequencies, and shifts slightly left on the plot. However, the range of acceptable performance matches very well, with the measured return loss is better than 20 dB from DC to 15 GHz, whereas the EM simulation shows the expected return loss to be below 20 dB up to 16 GHz.

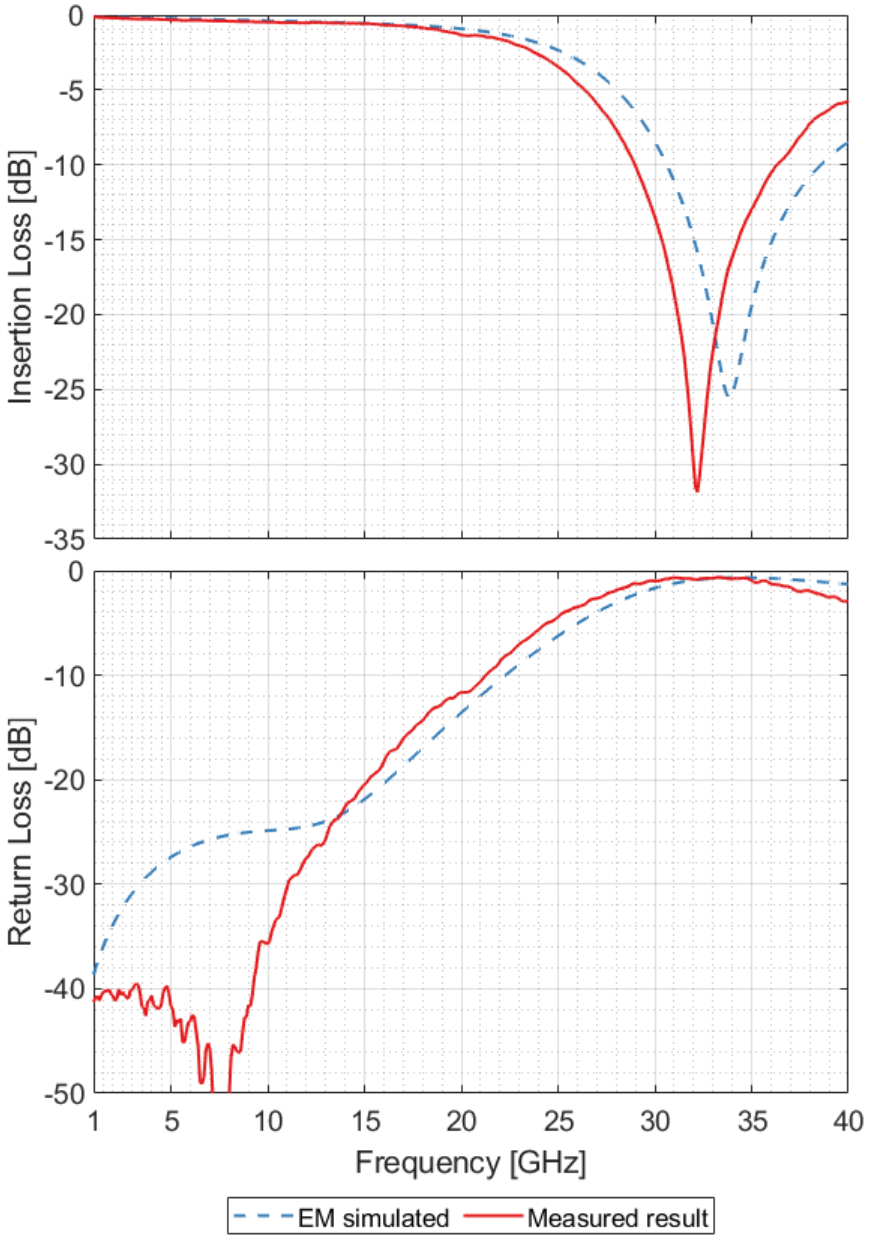

Figure 4.20: Measured and simulated RF performance of the released RF-MEMS SP4T switch in the ON state.

The SPST switches in this SP4T design must be actuated using a voltage applied from their corresponding ports. This is because the MEMS cantilevers are anchored to the CPW signal lines coming from the output ports (ports 2 to 5). However, the operation of some RF devices that use SP4T devices as components required the SPST switches to be actuated using a voltage applied through the signal line coming from port 1. An example of this would be capacitor banks, devices that are loaded with components in ports 2 to 5. In this case, the SPST switches in this design would be floating switches. As a result of this problem, a reversed orientation SP4T switch must be built, with SPST component switches facing the opposite direction from the original design. Figure 4.21 shows the EM model of the reversed orientation SP4T design, where all the SPST switches are oriented to anchor at the common junction CPW signal line, coming from the port 1 signal line.

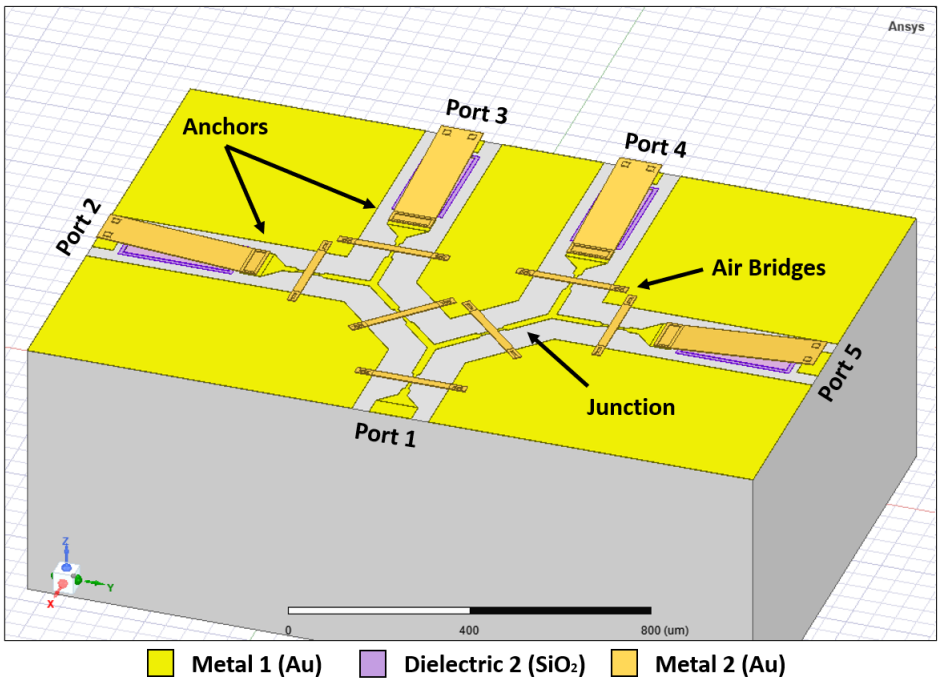

Figure 4.21: EM SP4T reverse orientation model.

The reverse oriented SP4T design was expected to have weaker performance because the SPST switches in the OFF state would load the junction and act as an open circuit CPW stub capacitor connected at the SP4T junction at the anchors. To find the ideal design dimensions, the CPW junction for the SP4T in the reverse orientation was parametrically swept from 20 to 60 μm in an EM simulation. Figure 4.23 presents the EM simulated RF performance of the SP4T reversed switch in the OFF state. The simulated isolation of the switch showed great performance, expected to be better than 20 dB from DC to 40 GHz. The return loss was predicted to be no worse than 0.5 dB from DC to 40 GHz for all variations. Much like the original SP4T design, the simulated RF performance in the OFF state improved as junction CPW signal line width increased.

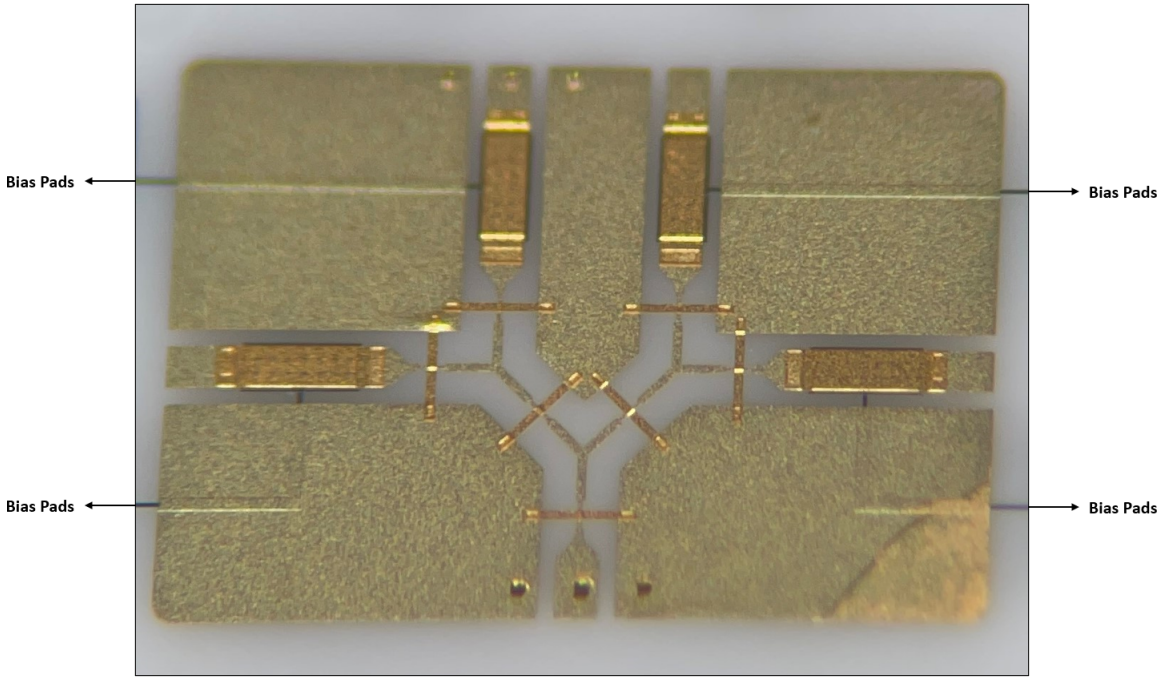

Figure 4.22: Microfabricated modified SP4T RF-MEMS switch.

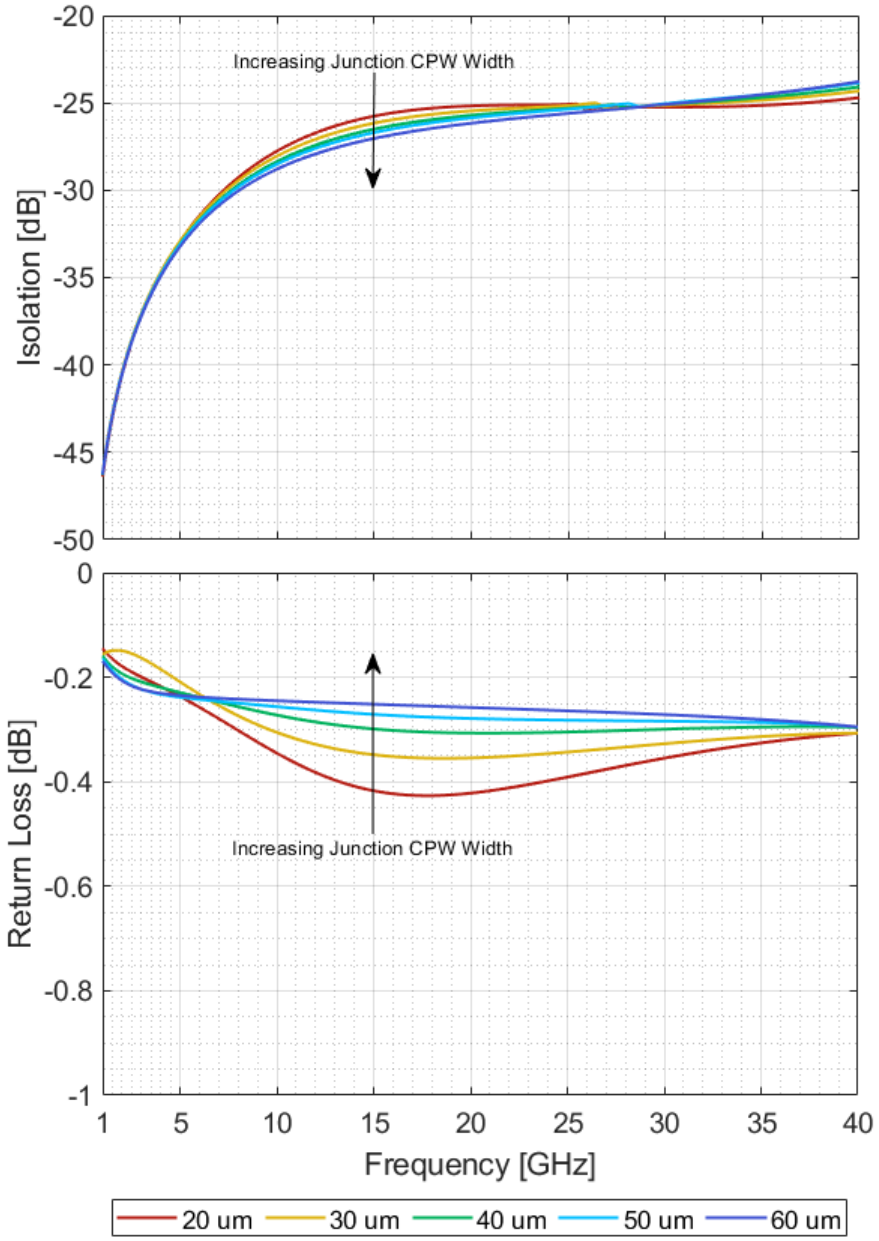

Figure 4.23: EM simulated RF performance of the SP4T reversed switch in the OFF state, with junction CPW width swept from 20 to 60 μm.

The EM simulated RF performance of the SP4T reversed switch in the ON state is presented in Figure 4.24, with the junction CPW width swept from 20 to 60 μm. The simulated insertion loss remained very low for all variations, with a value no worse than 2 dB from DC to 16 GHz. However, similar to the original SP4T design, the return loss in the ON state for the reversed orientation design seems to be the bottleneck performance metric. As expected, the up state cantilevers anchored on the CPW junction loaded the signal line. The frequency range where the simulated return loss performed better than 20 dB is much smaller than the original orientation SP4T for all variations. This range decreases quickly with increasing junction CPW width, with the best performing variation occuring at a junction CPW width of 20 μm. At this junction CPW width value variation, the simulated performance at low frequencies was good. The return loss was better than 20 dB from DC to 9 GHz.

The reversed orientation SP4T switch was fabricated, released, and the RF performance was tested. Figure 4.25 displays the measured RF performance of the reverse orientation Sp4T switch in the OFF state, with a junction CPW width of 20 μm, compared to its expected performance from the EM simulation. The return loss suffered greatly at higher frequencies due to the extention of the cantilevers from the SPST switches. However, at low frequencies, the performance was still acceptable. While the measured performance of the isolation followed the same profile as the EM simulated isolation curve, the actual measured values were worse than expected. Isolation remained better than 20 dB from DC to 8 GHz, and better than 15 dB from DC to 40 GHz. The simulation on the other hand, expected the isolation to remain better than 20 dB for DC to 40 GHz. This amount of extra loss when going from the simulation to the measurement results is well within expectations from microfabrication tolerances.

Figure 4.26 presents the plot for the measured and simulated RF performance of the

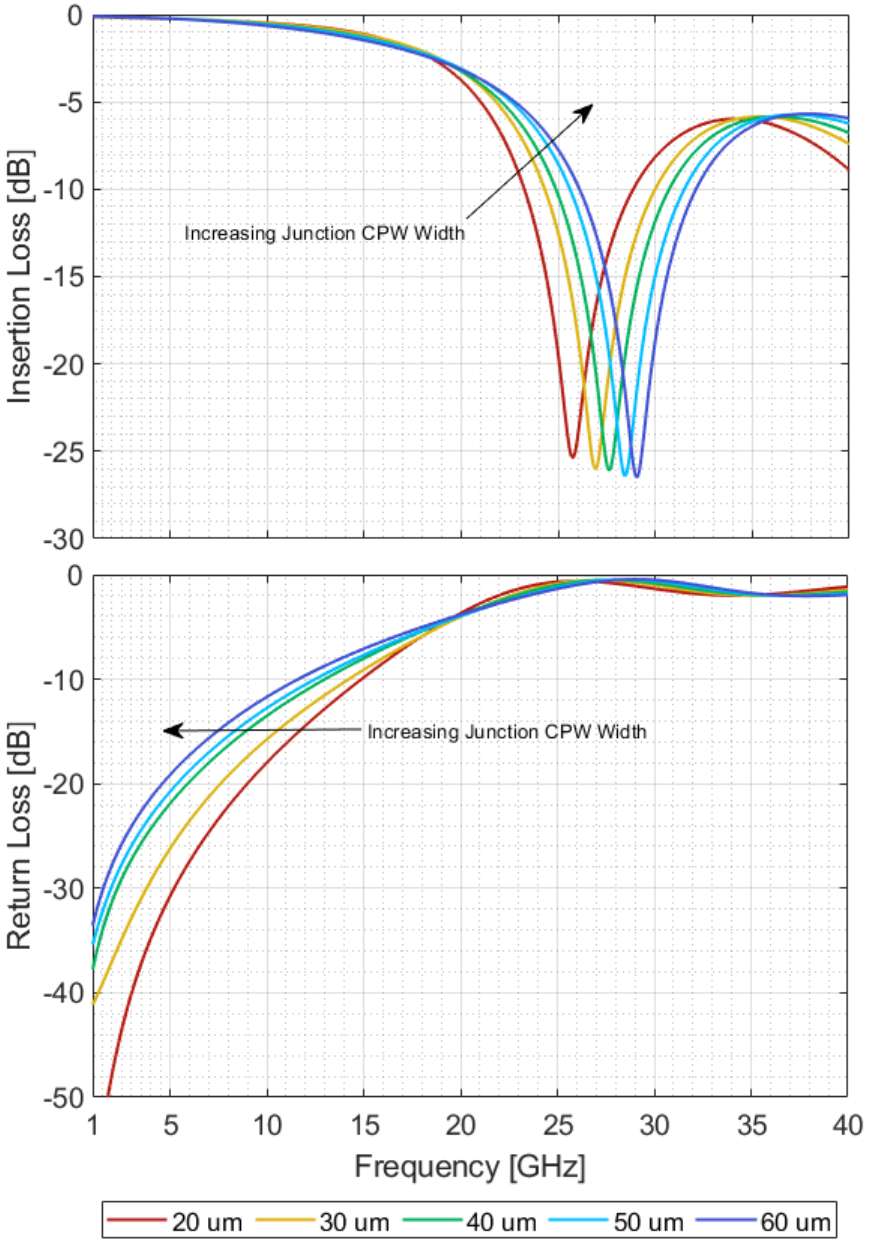

Figure 4.24: EM simulated RF performance of the SP4T reversed switch in the ON state, with junction CPW width swept from 20 to 60 μm.

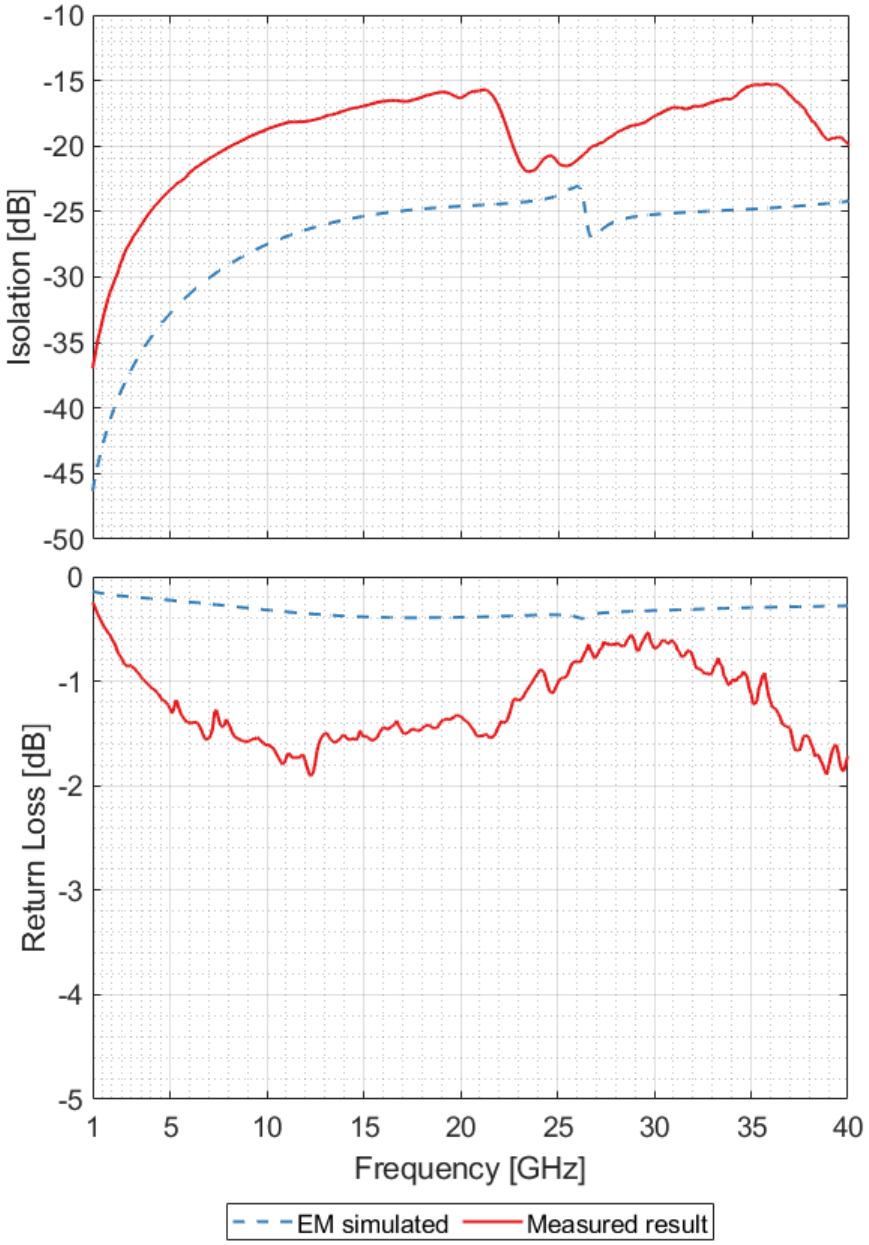

Figure 4.25: Measured and simulated RF performance of the reverse orientation SP4T switch in the OFF state.

reverse SP4T switch in the ON state, where the SPST switch for port 3 was actuated, while the rest remained in the OFF state (port 3 ON, ports 2, 4, 5 OFF). The measured results matched the simulation results very well. The insertion loss was measured to be slightly worse, but the plot of the measurement results matched nearly identically with the EM simulation insertion loss. The measured insertion loss remained below 1 dB from DC to 10 GHz.

The measured return loss suffered at lower frequencies, showing a slightly higher loss when compared to the EM simulation. This can be attributed to microfabrication tolerances changing the matching of the CPW junction, as well as the real reachable range of real world RF measurement capability of the RF probes used. The return loss was measured to be better than 20 dB from a range of DC to 7 GHz. The low frequency (DC to 5 GHz) performance in both the OFF and ON state was measured to be more than sufficient for use as components in designing more complex RF devices at said frequencies.

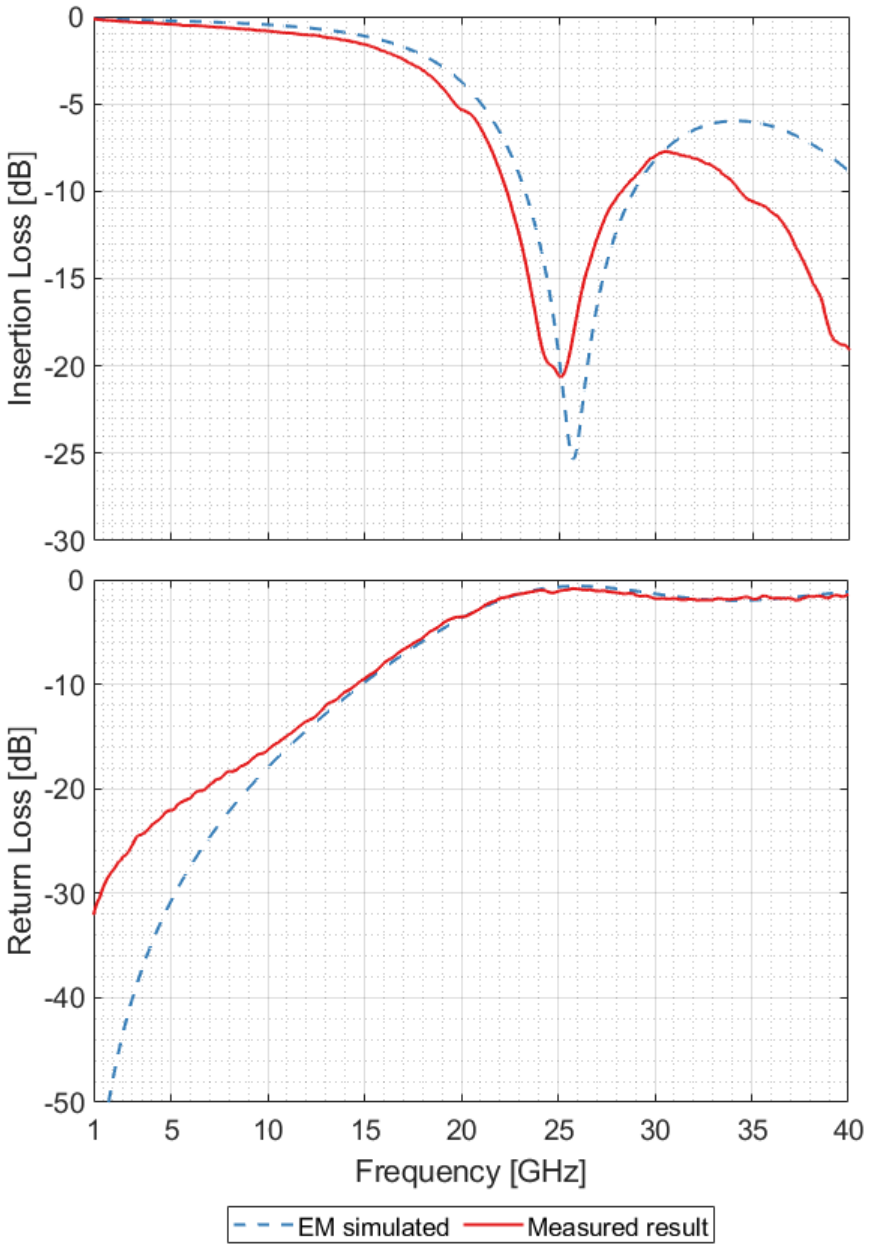

Figure 4.26: Measured and simulated RF performance of the reverse orientation SP4T switch in the ON state.

4.4 Single Port Triple Throw (SP3T) Switches

A single throw triple port (SP3T) switch was also designed using the RF-MEMS SPST switch, similar to the SP4T switch design. Figure 4.27 presents the EM model of the design, where one input port paths into three exit ports, determined by the actuation of the corresponding SPST switches.

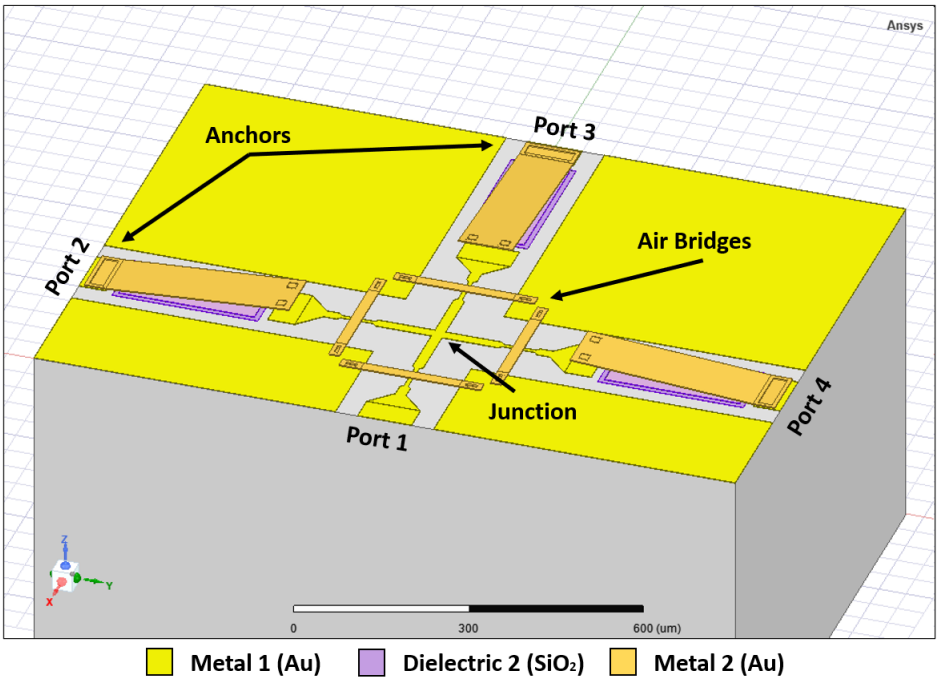

Figure 4.27: EM SP3T model.

Unlike the SP4T switch, the three exit ports do not have the same output due to symmetry. Ports 2 and 4 experience the same RF behaviour as they are symmetrical, but port 3 experiences a different response because it is not. The RF signal follows a different path when port 3 is on, as opposed to when ports 2 or 4 are on. In this design, the SPST switches are anchored on the signal line coming from the exit ports, like in the initial

SP4T design. A reverse orientation SP3T was also designed and presented later, with the schematic of both variations of the SP3T RF-MEMS switch shown in Figure 4.28.

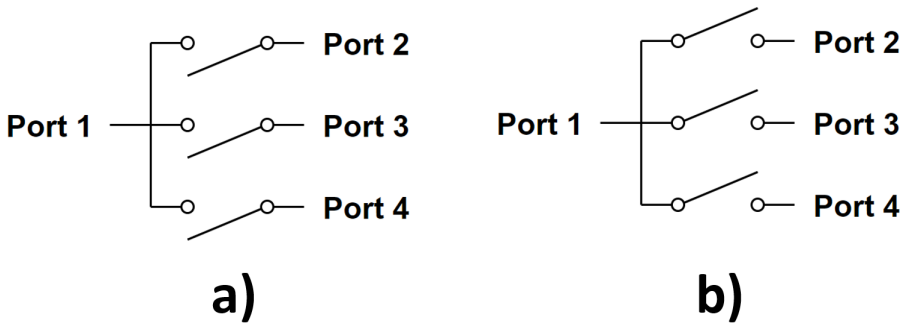

Figure 4.28: SP3T circuit schematic for variations where switches are anchored at the a) output ports, b) input port.

Much like the SP4T design, the CPW junction of the SP3T design was tuned in an EM simulation to find the width that returned the best RF performance. A parametric sweep was performed in HFSS, adjusting the width of the CPW junction to find the ideal design for OFF and ON states for both port 2 and port 3. Air bridges were used in the junction to connect the ground planes as well as suppress parasitic couple slot line modes. Figure 4.29 presents the results of the simulation with the SP3T switch in the OFF state, with the value for width swept from 20 to 60 μm. All three exit ports demonstrate a great simulated isolation in the OFF state, remaining better than 20 dB isolation from DC to 23 GHz for all parametric values. The return loss for all sweep values was also good, with return loss better than 0.6 dB from DC to 40 GHz for all variations.

The simulated RF performance when port 2 of the SP3T was actuated is shown in Figure 4.30. With port 2 in the ON state and ports 3 and 4 in the OFF state, the return loss improved with decreasing CPW junction width. A width of 20 μm showed a return

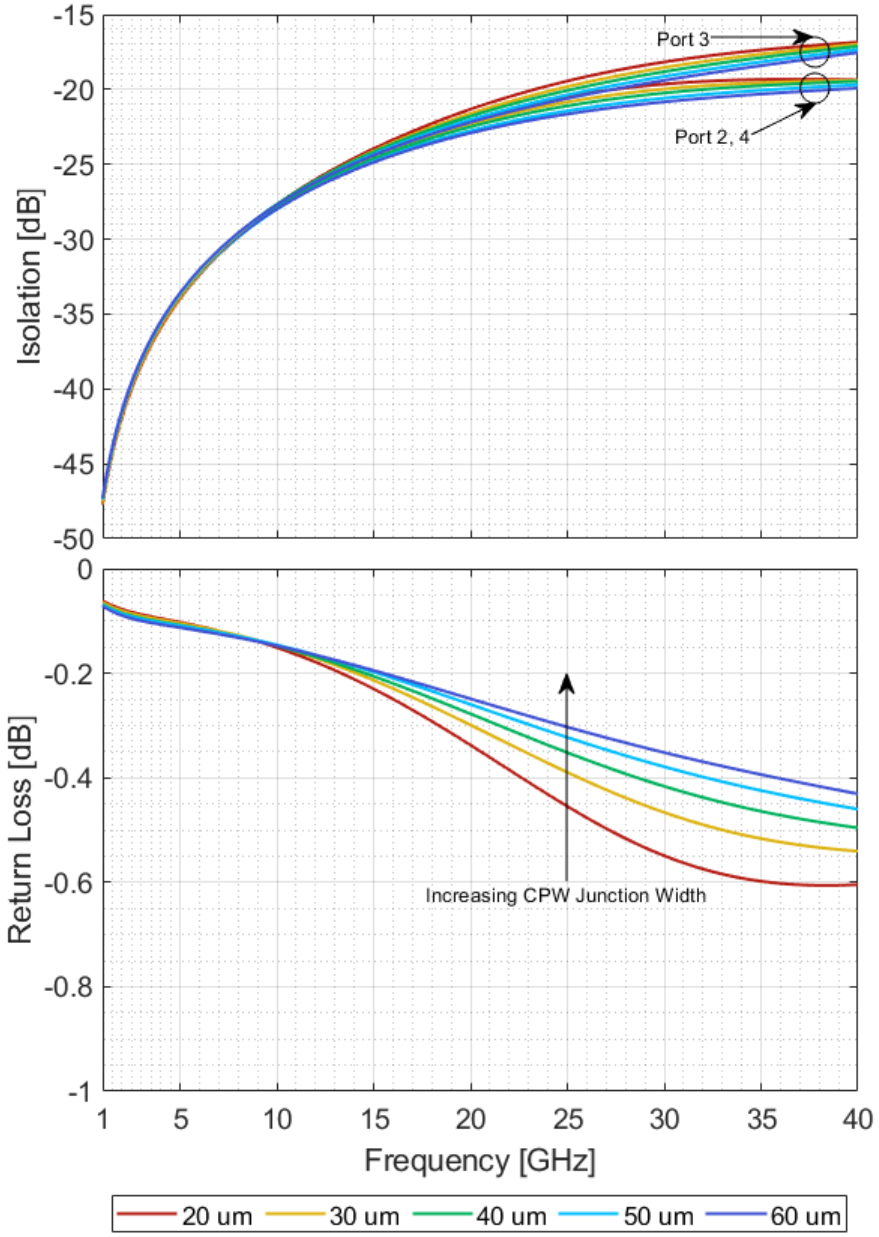

Figure 4.29: EM simulated RF performance of the SP3T switch in the OFF state, with junction CPW width swept from 20 to 60 μm.

loss better than 20 dB from DC to 27 GHz, whereas a width of 60 μm only performs better than 20 dB from DC to 13 GHz. Figure 4.30 also shows that port 3 isolation is simulated to perform better than the return loss of port 2 for all variations, with simulated isolation better than 20 dB from DC to 32 GHz. Due to symmetry, all simulated results for port 2 were used to infer the performance when only port 4 was actuated in the SP3T.

Unlike the SP4T switch designs, the SP3T switch output ports are not identical due to symmetry. An RF signal from port 1 to port 2 will experience the same pathing as port 1 to 4. However, a signal going from port 1 to port 3 will not experience the same, as the RF signal paths straight as opposed to being adjacent to the input port. The scenario when port 3 is turned on was studied separately due to this asymmetry. Figure 4.31 shows the EM simulated RF performance of the SP3T switch when port 3 is in the ON state, and ports 2 and 4 in the OFF state. A parametric sweep was conducted, sweeping the SP3T junction CPW width from 20 to 60 μm. The simulated RF performance displays an insertion loss up to 1.2 dB from DC to 40 GHz for the weakest performing parametric variation. The return loss shows improved performance with decreasing junction CPW width. At a width value of 20 μm, the simulated return loss performs better than 20 dB from DC to 35 GHz. The simulated RF isolation for ports 2 and 4 also perform better than 20 dB up to 35 GHz.

The SP3T switch was designed using a junction CPW width of 20 μm, fabricated, released, and tested. Figure 4.34 plots the measured and simulated RF performance of the SP3T switch with port 2 in the ON state, and ports 3 and 4 in the OFF state. The measured results matched closely with the EM simulation results, with the curve for the measurement results following the simulation plot closely, and magnitudes for both insertion loss and return loss following along closely. The measured return loss performed better than 20 dB for the range of DC to 23 GHz, while the insertion loss stayed better

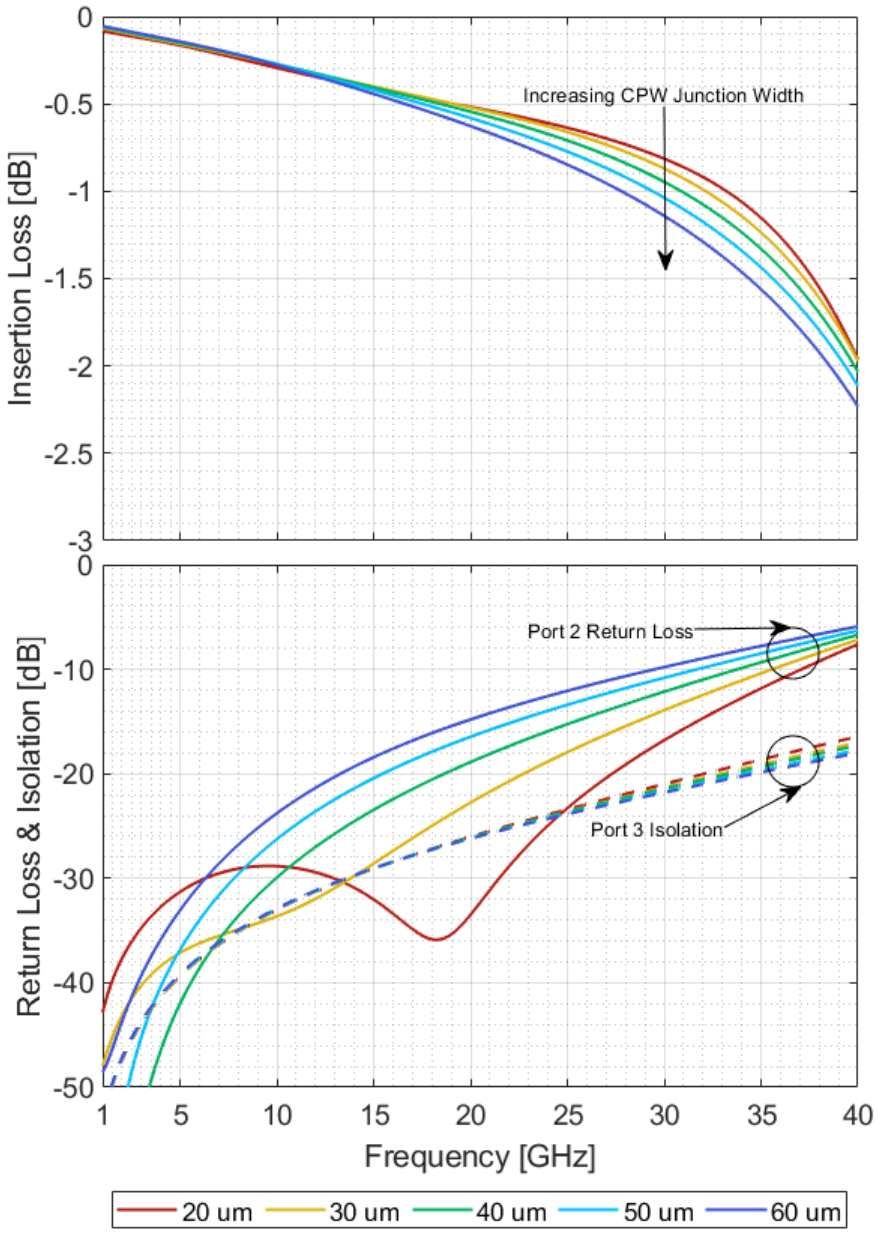

Figure 4.30: EM simulated RF performance of the SP3T switch with Port 2 ON, with junction CPW width swept from 20 to 60 μm.

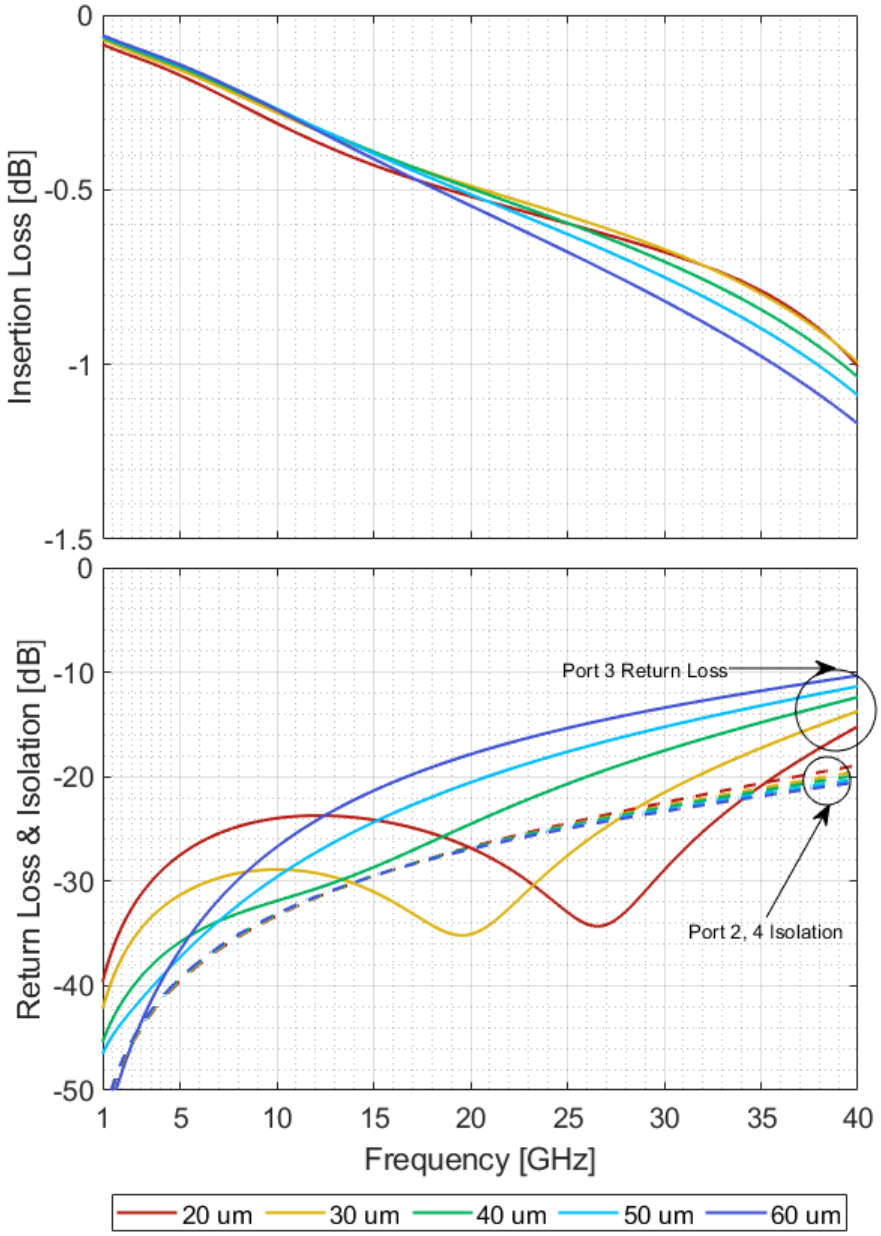

Figure 4.31: EM simulated RF performance of the SP3T switch with Port 3 ON, with junction CPW width swept from 20 to 60 μm.

than 0.5 dB for the same range. It should be noted that the performance after 25 GHz was only plotted to view the behaviour at higher frequencies, and is beyond the range of the recommended frequency of the RF probes used to test the devices.

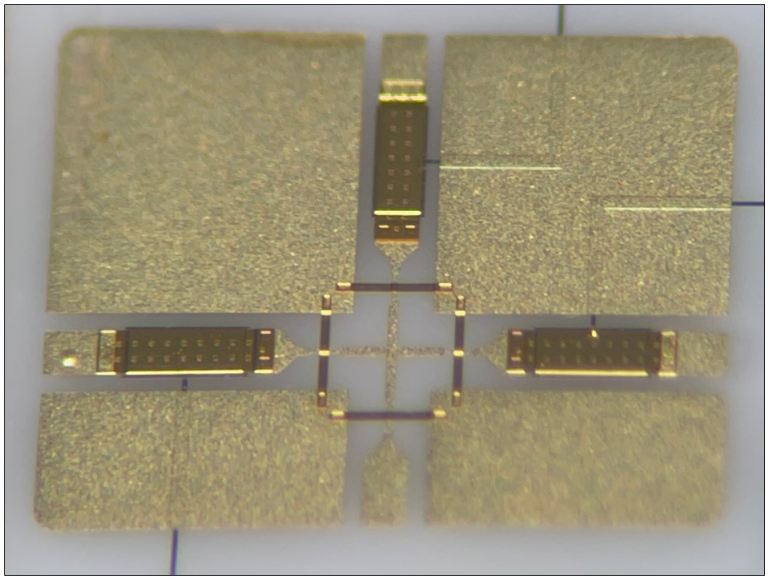

Figure 4.32: Microfabricated SP3T RF-MEMS switch.

Likewise, the measured RF performance of the SP3T switch with port 3 in the ON state is compared with its EM simulation counterpart in Figure 4.35. The measured return loss shows a trend that loosely follows the EM simulated return loss for the same state. With port 3 on, and ports 2 and 4 off, the measured return loss is better than 20 dB from DC to 25 GHz, with insertion loss for the same range better than 1 dB.

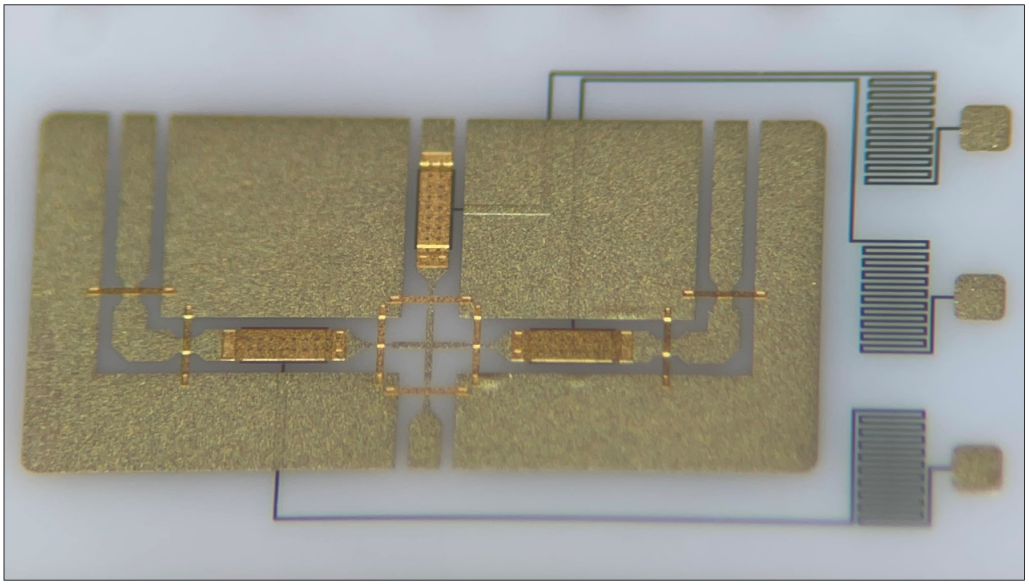

Figure 4.33: Microfabricated SP3T RF-MEMS switch with extended ports.

For the same reasons as the SP4T switch, another design for the SP3T switch was created, where the switches face the opposite direction from the original design. Figure 4.36 shows the EM model of the reverse orientation SP3T design. This is for the case where SPST components are actuated with a bias from the signal line coming from the input port CPW, and not from the ports where the switches lead to (ports 2 to 4). With bias applied from the port 1 signal line, the original SP3T configuration would have floating switches that could not be actuated, since the bias would not extend out to the upper electrode of the RF SPST switches through their anchors. This necessitated a design where all switches were anchored to the CPW junction connected to the input signal CPW line.

This reverse oriented SP3T switch design was expected to have weaker performance because the SPST switches in the OFF state would act as open circuit stubs and load the junction. An EM simulation was performed while sweeping the junction CPW width to

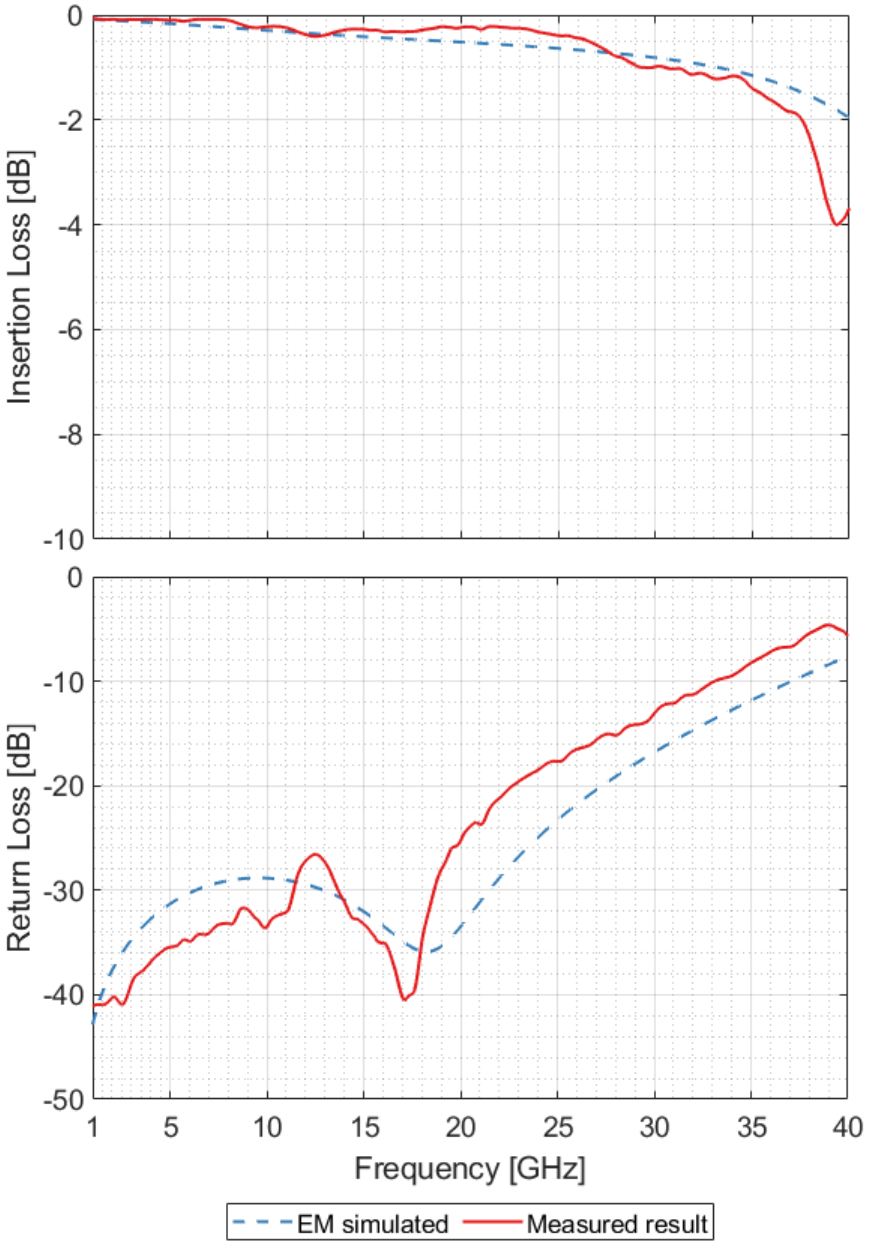

Figure 4.34: Measured and simulated RF performance of the SP3T switch with Port 2 in the ON state.

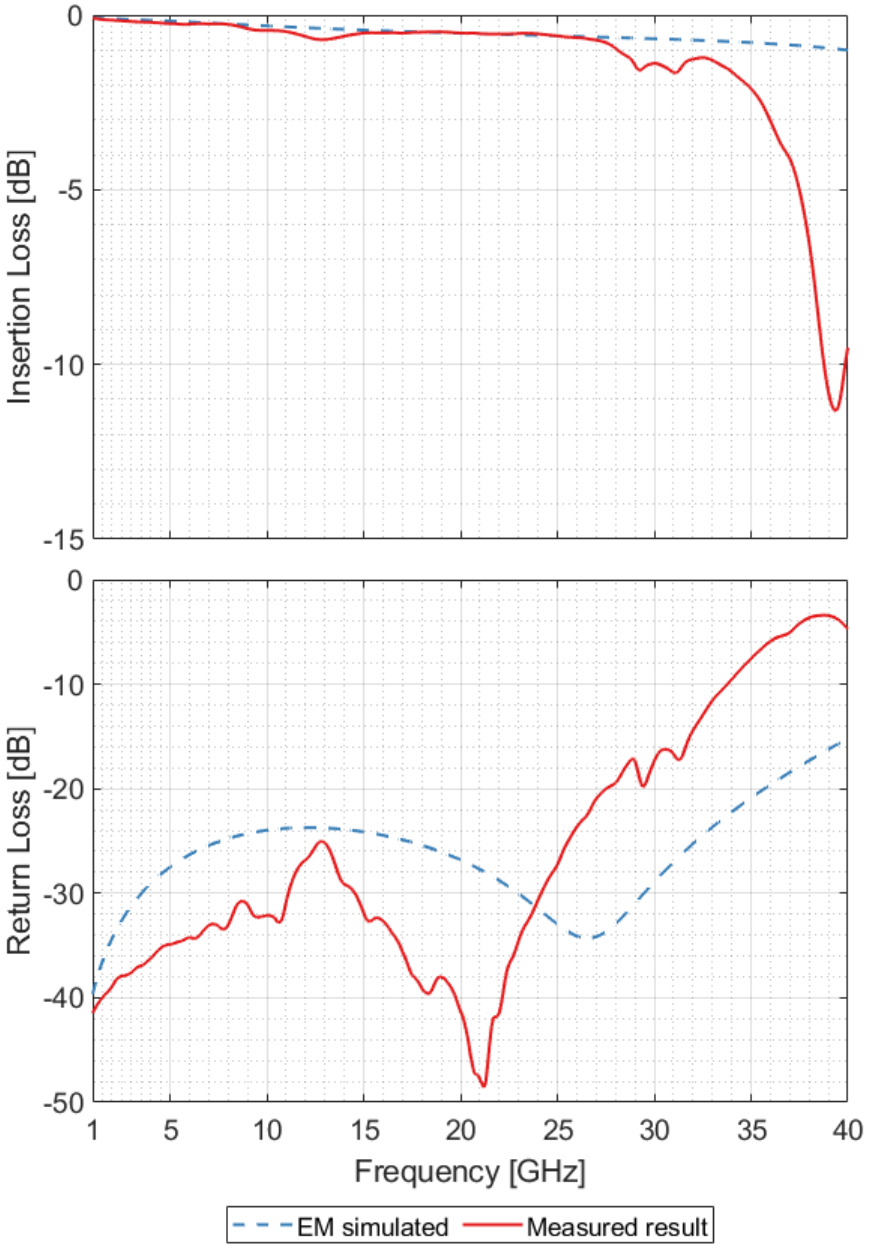

Figure 4.35: Measured and simulated RF performance of the SP3T switch with Port 3 in the ON state.

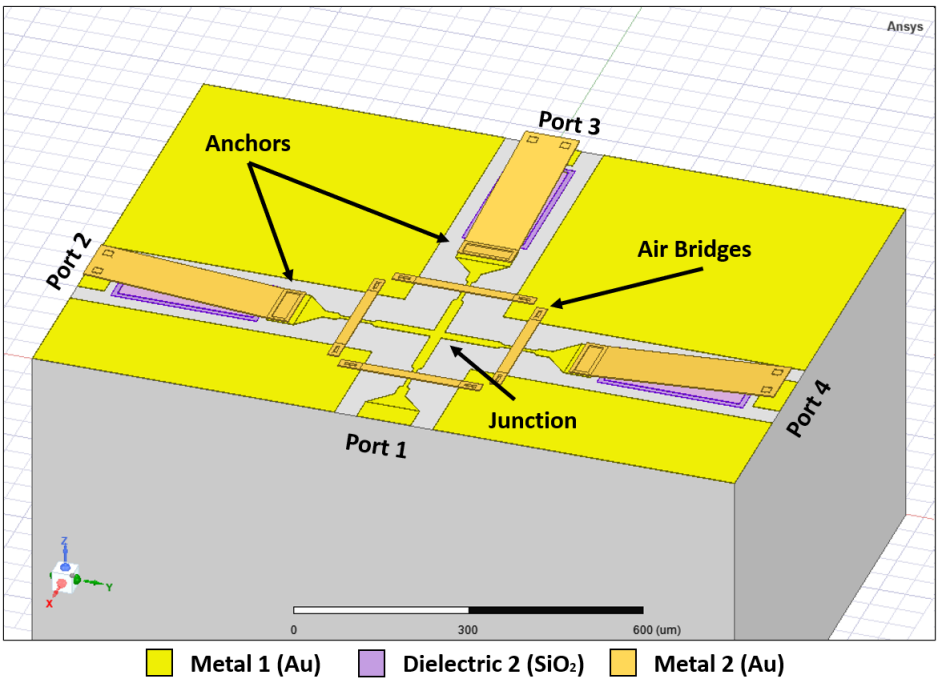

Figure 4.36: EM SP3T reverse orientation model.

find the best performing variation for this design.

Figure 4.37 shows the EM simulated RF performance of the SP3T reverse oriented switch design in the OFF state, with a parametric sweep for the junction CPW width from 20 to 60 μm. All variations of the reversed SP3T in the OFF state show a great simulated RF performance. The isolation in the OFF state for all ports remained better than 20 dB from DC to 25 GHz for all parametric variations. The return loss for the switch stayed below 0.5 dB for all width values, with the worst performing variation being 20 μm, dipping to 0.45 dB return loss at its lowest point.

The EM simulated RF performance of the SP3T reverse oriented switch variation, with port 2 in the ON state and ports 3 and 4 in the OFF state, is shown in Figure 4.38. It is shown that return loss for the switch in the ON state is significantly worse than the original variation of the design for the SP3T. The best performing variation with a width of 20 μm, has a simulated return loss better than 20 dB from DC up to 13 GHz, whereas the initial SP3T design showed the same return loss but up to 27 GHz. However, the performance at lower frequencies remains good, with return loss dipping to 40 dB below 5 GHz for a junction CPW width of 20 μm. EM simulated insertion loss remains better than 1 dB up to 18 GHz for all junction width variations. Isolation of ports 2 and 4 when port 3 is on is simulated to be much better than the return loss of all possible variations, being better than 20 dB from DC to 25 GHz for all junction CPW width values.

The simulated performance of the reverse orientation SP3T switch with port 3 in the ON state and ports 2 and 4 in the OFF state can be seen in Figure 4.39, with the junction line width parametrically swept for. The simulated RF performance in this state is slightly better than the last, with a return loss better than 20 dB from DC up to 16 GHz for the best performing variation (20 μm). As before, the isolation for ports in the OFF state (ports 2 and 4 in this case) remain better than 20 dB for a much wider range of frequency

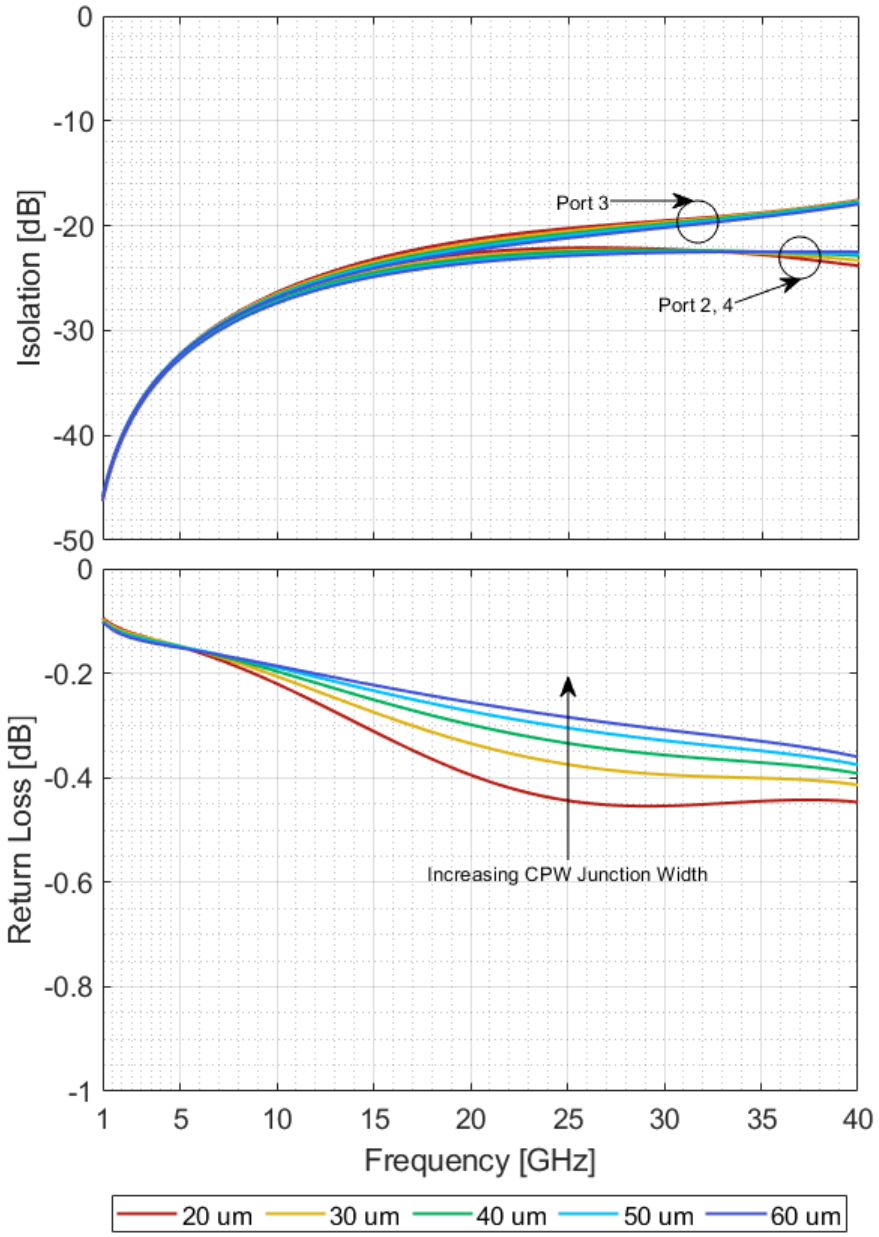

Figure 4.37: EM simulated RF performance of the SP3T reverse orientation switch in the OFF state, with junction CPW width swept from 20 to 60 μm.

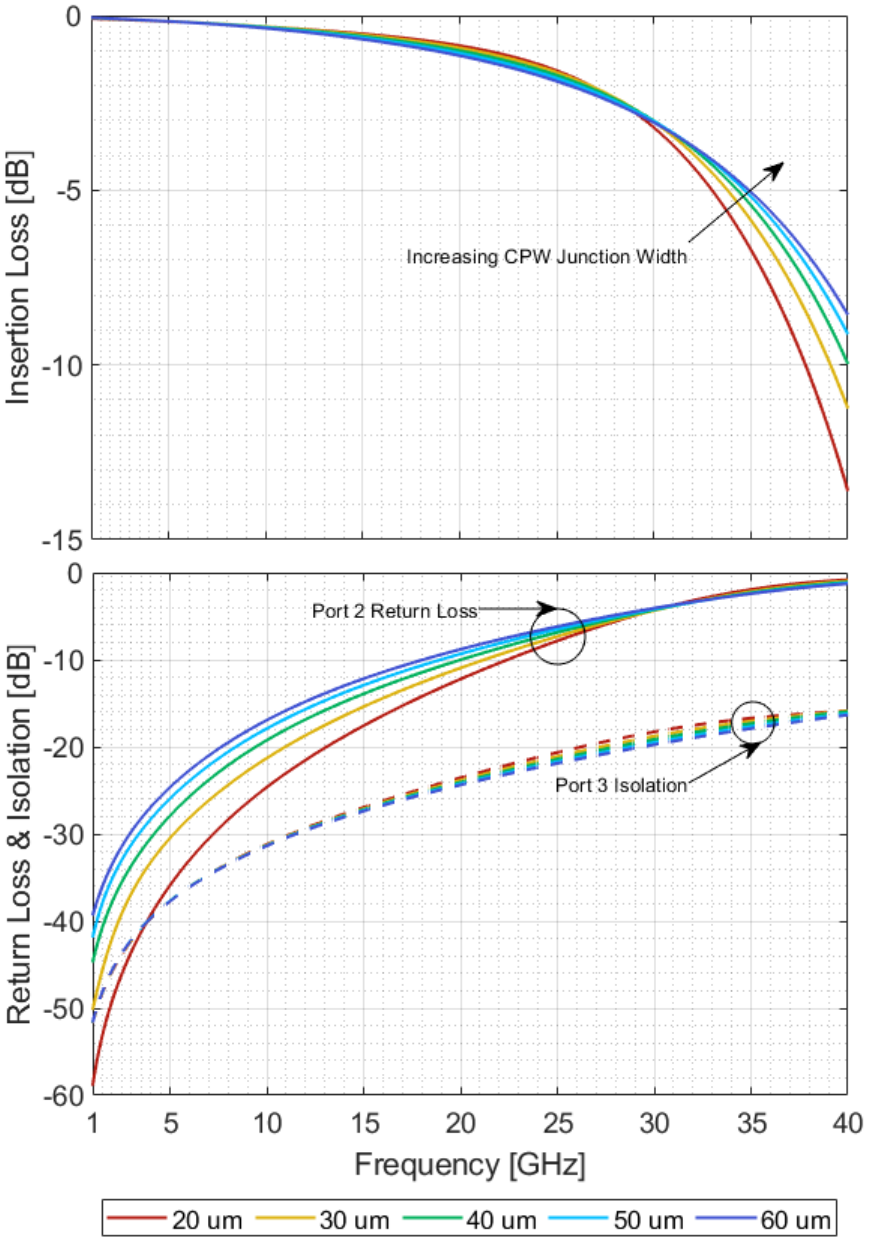

Figure 4.38: EM simulated RF performance of the SP3T reverse orientation switch with Port 2 ON, with junction CPW width swept from 20 to 60 μm.

than the return loss for the port in the ON state (port 3).

The final design for all devices was chosen for the RF performance in both of the ON states, looking primarily at the variations with the simulated return loss being better than 20 dB for the longest frequency ranges. In all cases, a junction CPW width of 20 μm was used for the best performance, while making sure the line didn't get too thin for microfabrication practicality.

The reverse orientation SP3T switches were fabricated, released, and tested. The measured and corresponding simulated RF performance of the SP3T reversed switches with port 2 in the ON state is shown in Figure 4.43. The measured insertion loss followed the curve of the EM simulation closely from DC to around 25 GHz, where it then deviated. The insertion loss stayed better than 1 dB from DC up to 20 GHz. At lower frequencies, the measured return loss was worse than the EM simulation, with a measured return loss better than 20 dB from DC to 8 GHz, whereas the simulation maintained a return loss better than 20 dB up to 13 GHz. This mismatch in performance is likely due to the microfabrication tolerances throwing off the dimensions of the CPW line and especially the junction widths.

Figure 4.44 shows the measured and simulated RF performance of the SP3T reverse orientation switch with port 3 in the ON state, and ports 2 and 4 in the OFF state. The measured and simulated insertion loss curves matched almost perfectly up to around 25 GHz, staying better than 1 dB before deviating after 25 GHz. For the return loss, much like the previous state (port 2 ON, ports 3 & 4 OFF), the measured performance was weaker than the EM simulation. Measured return loss was better than 20 dB from DC to 10 GHz, while the simulation crossed 20 dB at 16 GHz. Like before, this is likely due to the microfabrication tolerances.

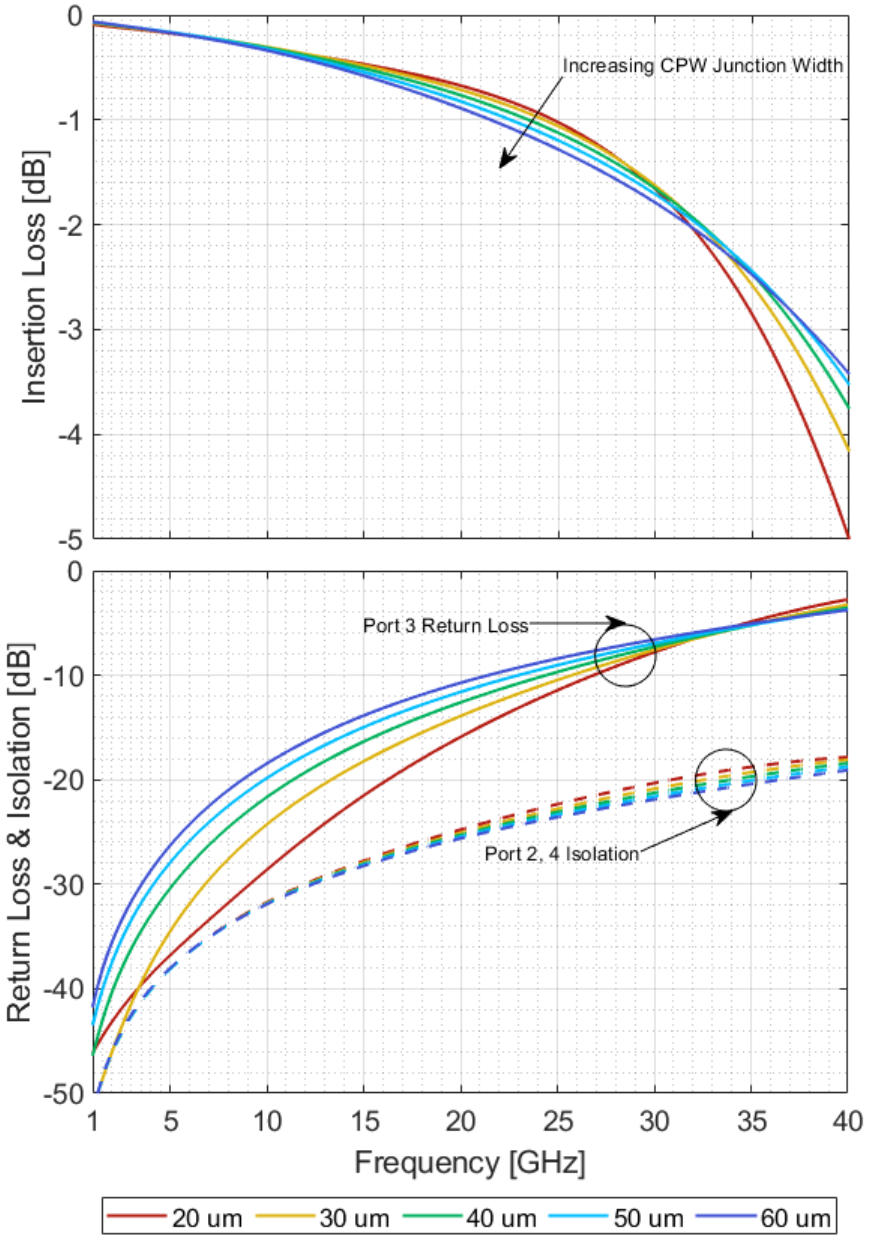

Figure 4.39: EM simulated RF performance of the SP3T reverse orientation switch with Port 3 ON, with junction CPW width swept from 20 to 60 μm.

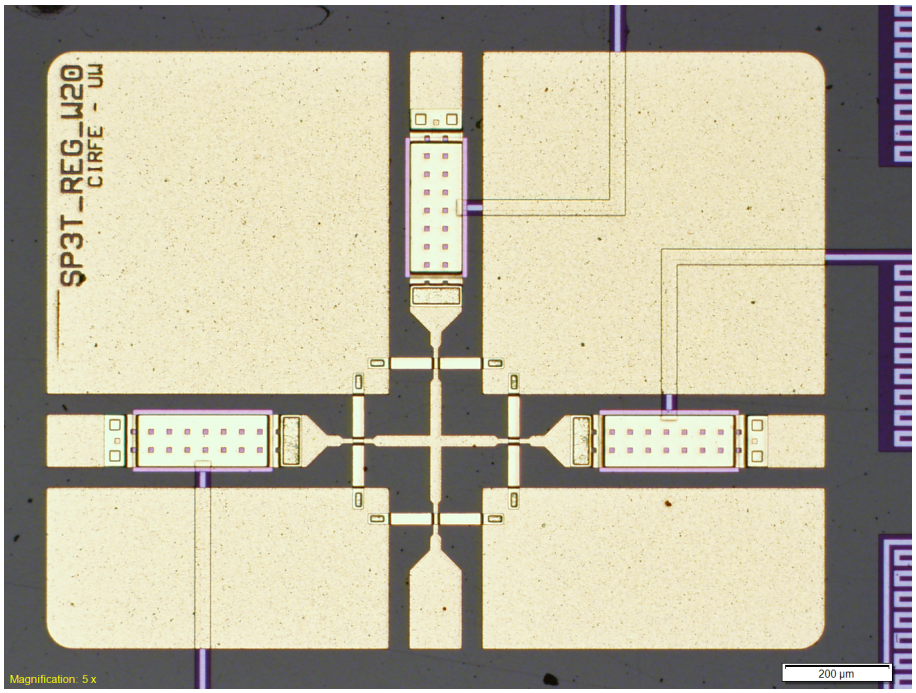

Figure 4.40: Optical micrograph of released modified SP3T RF-MEMS switch.

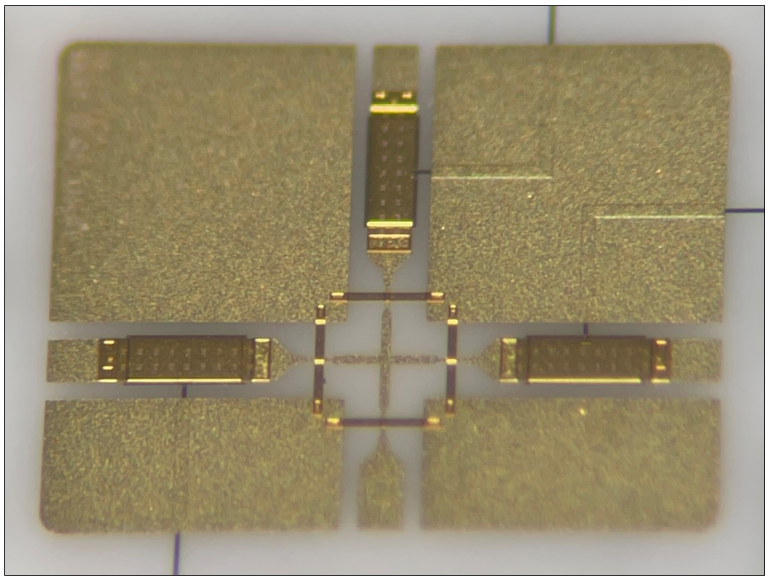

Figure 4.41: Microfabricated modified SP3T RF-MEMS switch.

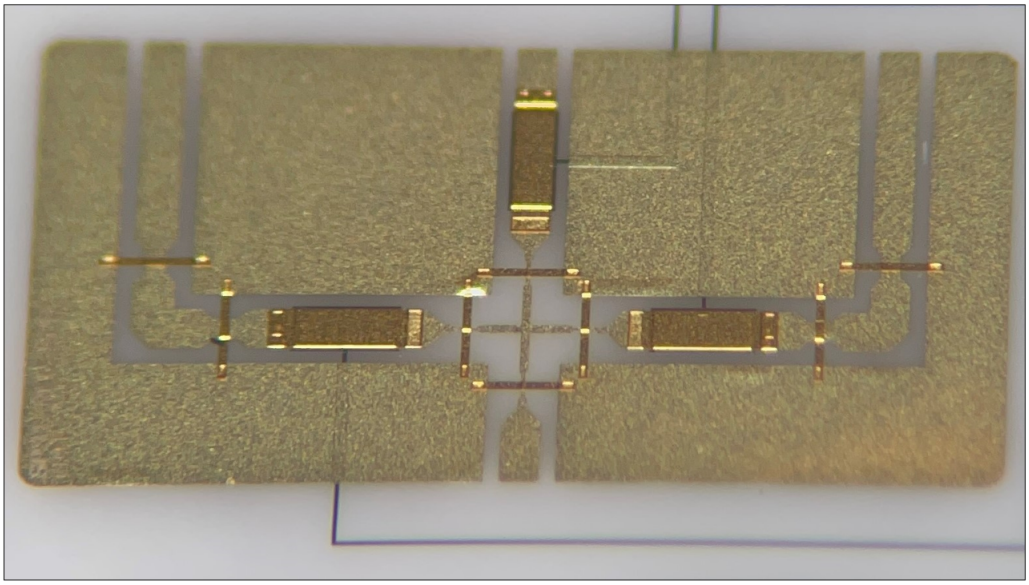

Figure 4.42: Microfabricated modified SP3T RF-MEMS switch with extended ports.

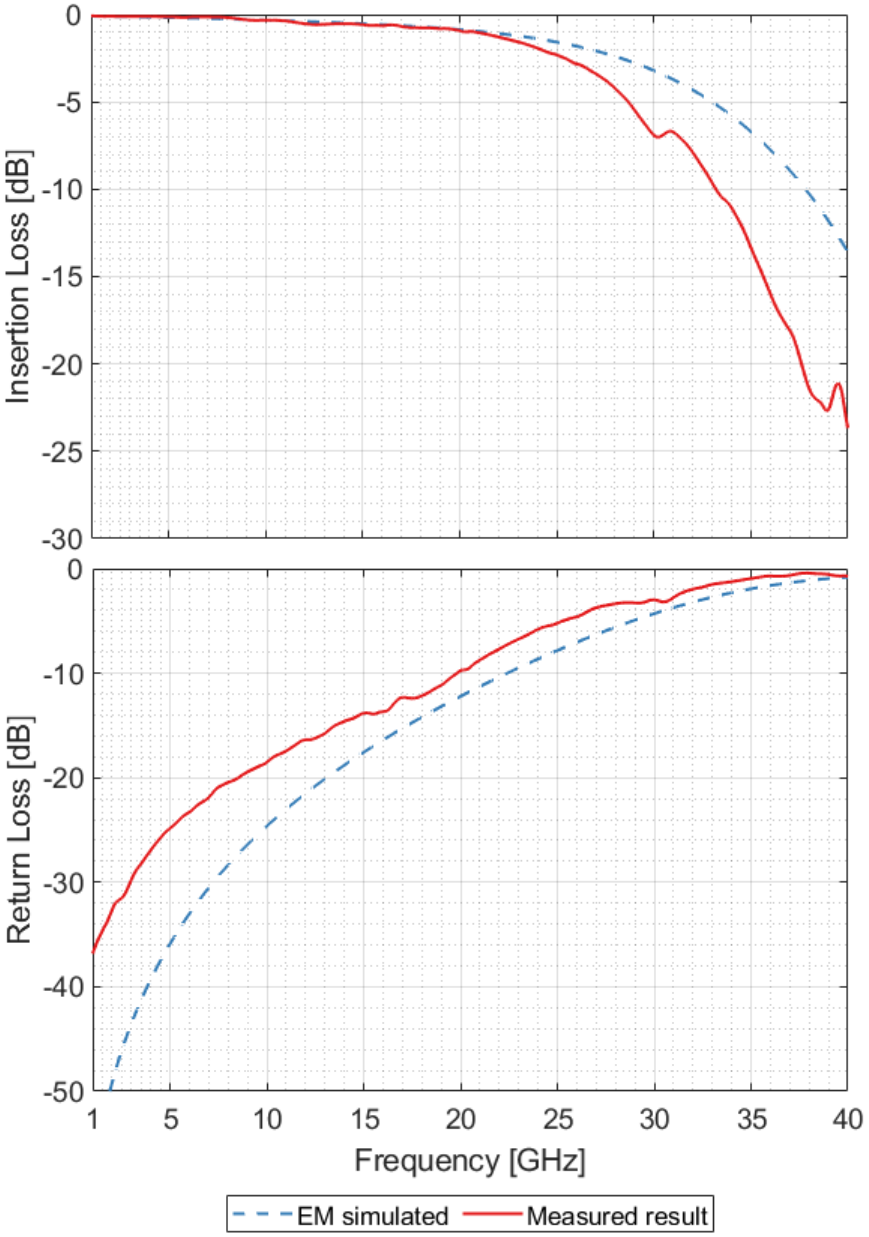

Figure 4.43: Measured and simulated RF performance of the SP3T reverse orientation switch with Port 2 in the ON state.

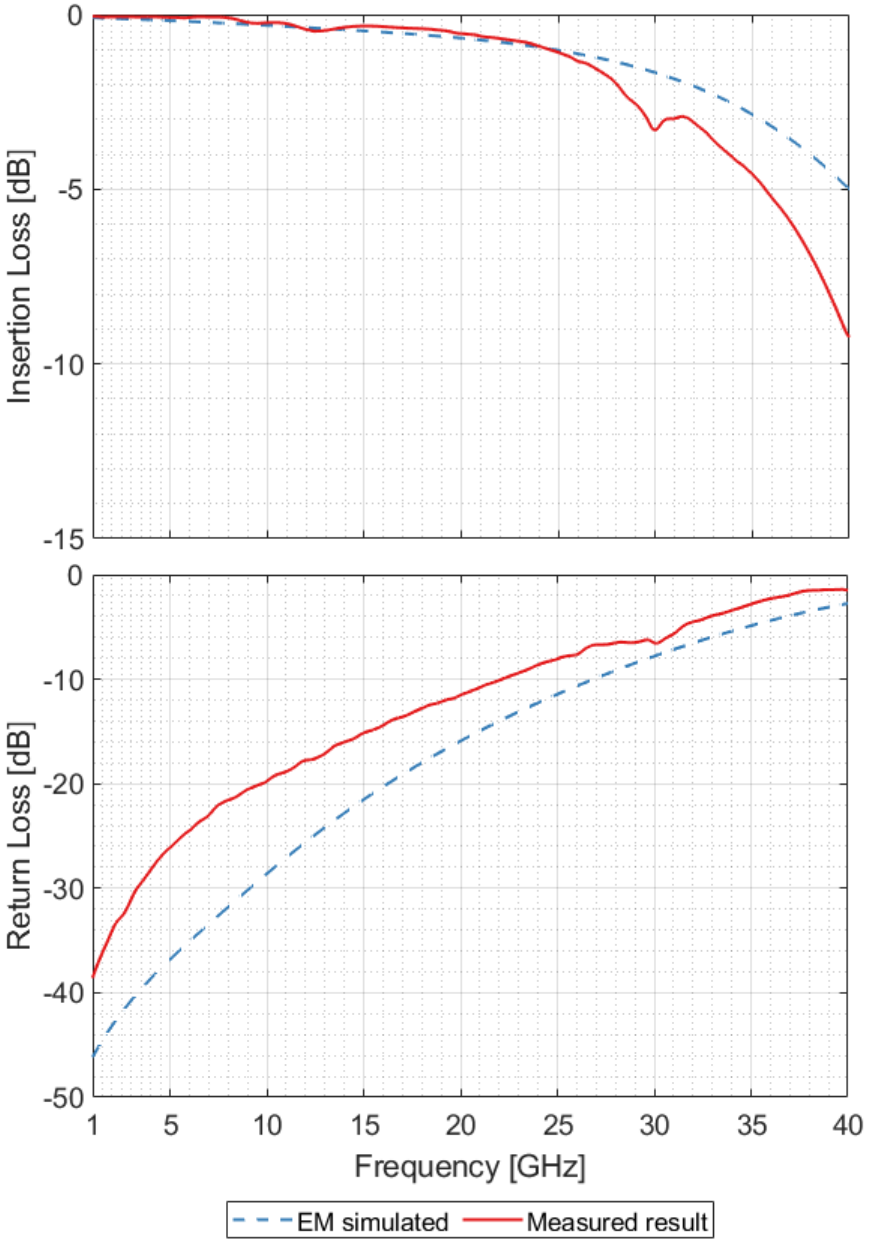

Figure 4.44: Measured and simulated RF performance of the SP3T reverse orientation switch with Port 3 in the ON state.

4.5 Capacitor Banks

Switched RF-MEMS capacitor banks are critical components for the realization of reconfigurable RF devices [1] [29]. The previously discussed SP4T RF-MEMS switch was used to design a switchable capacitor bank. Ports 2 to 5 of the switch were loaded with capacitors. As such, the capacitor bank had to be biased with a voltage applied on the input port signal line. Because of this, the reverse orientation design for the SP4T was used. The schematic of the capacitor bank is shown in Figure 4.45.

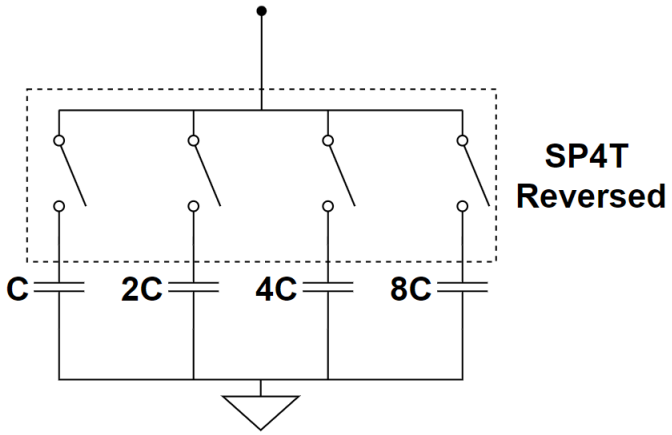

Figure 4.45: Capacitor bank schematic.

The capacitor bank was designed to use capacitor components valued at a unit capacitance C, 2C, 4C, and 8C. With this configuration, the switches could be actuated in combinations such that 16 states were achievable, starting from C_o (OFF-state capacitance, when all SPST switches were not actuated), increasing in increments of C up to 15C. Similar MEMS based capacitor banks were previously report in literature, using commercial SPDT RF-MEMS switches with SMD capacitors [30] and interdigital capacitors [17], and

CMOS MEMS based switched capacitors [16].

The parameter of interest when designing the capacitor bank variations was the capacitance value seen at the input port, with the individual capacitors connected to the SP4T as parameters. The target frequency range was 3 to 4 GHz. Two variations of the capacitor bank were designed, with a unit capacitance C value of 70 fF and 100 fF. The capacitance values for all capacitors used in both variations can be seen in Table 4.3. The self resonance frequency was considered during the initial design, and confirmed to be above the intended operation frequency. When operated at states that feature higher capacitance, the capacitor banks were expected to slope up as the frequency approached the self-resonance frequency.

Table 4.3: Capacitance values for capacitor bank.

Parameter	**Capacitance (fF)**	
	Variation 1	**Variation 2**
C1	C = 70	C = 100
C2	2C	2C
C3	4C	4C
C4	8C	8C

The capacitor bank devices were achieved using either open circuit (OC) co-planar waveguide (CPW) stub capacitors, or metal-insulator-metal (MIM) capacitors. The capacitors used in the capacitor bank variations listed below were designed for use at the target frequency of 3.6 GHz.

The MIM capacitors have the advantage of having a higher quality factor and a smaller footprint, with the downside of being more complicated to implement in terms of micro-

fabrication. OC CPW stub capacitors have the benefit of being simpler to implement, but with a much larger footprint on the substrate.

CPW Capacitor Banks

Co-planar waveguide (CPW) stubs were used to achieve on-chip capacitors by terminating one end with an open circuit, and adjusting the length to increase the capacitance. To match the desired values from Table 4.3, a circuit model was used to adjust the line lengths for the necessary capacitance values at a target frequency of 3.6 GHz. The final lengths of the OC CPW stub capacitors is displayed in Table 4.4. The EM simulation results of the capacitors were imported into the circuit simulation as sNp files to improve the accuracy of the circuit simulation.

Table 4.4: OC CPW stub lengths for CPW capacitor banks..

Parameter	**OC CPW Length (um)**	
	Variation 1	**Variation 2**
C1	500	750
C2	1000	1500
C3	1950	2800
C4	3500	4600

EM simulations of the CPW stub capacitor components for both variations of the CPW capacitor bank were conducted to verify the capacitance values of the stubs, and verify the lengths to be used. Figure 4.46 shows the capacitance values of the stubs used for variation 1, and Figure 4.47 shows the capacitance values of the stubs used in variation 2 of the CPW capacitor bank. Both figures show that for a frequency of 3.6 GHz, the

capacitance values from the EM simulations match the capacitance values listed in Table 4.3.

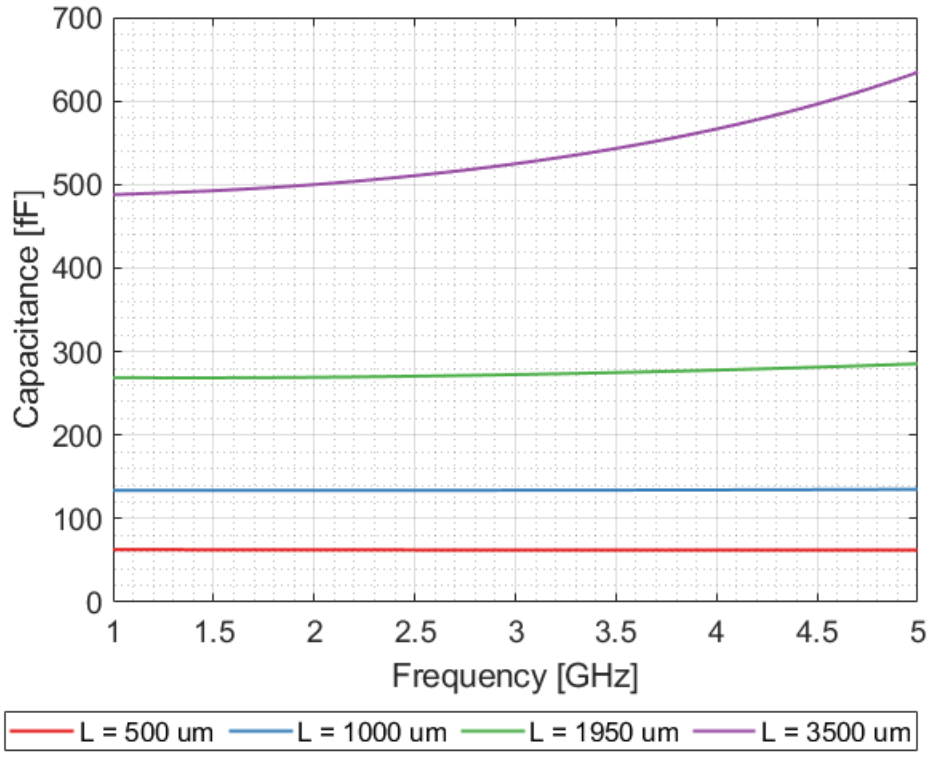

Figure 4.46: EM simulated OC CPW stub capacitors for variation 1

The final model of the CPW capacitor bank includes attaching the OC stubs to the four ports of the reverse orientation SP4T. The model of the CPW capacitor bank is shown in Figure 4.48. The layout for the two variations of CPW capacitance banks is shown in Figure 4.49.

The circuit simulation results for the CPW capacitor bank variation with lower ca-

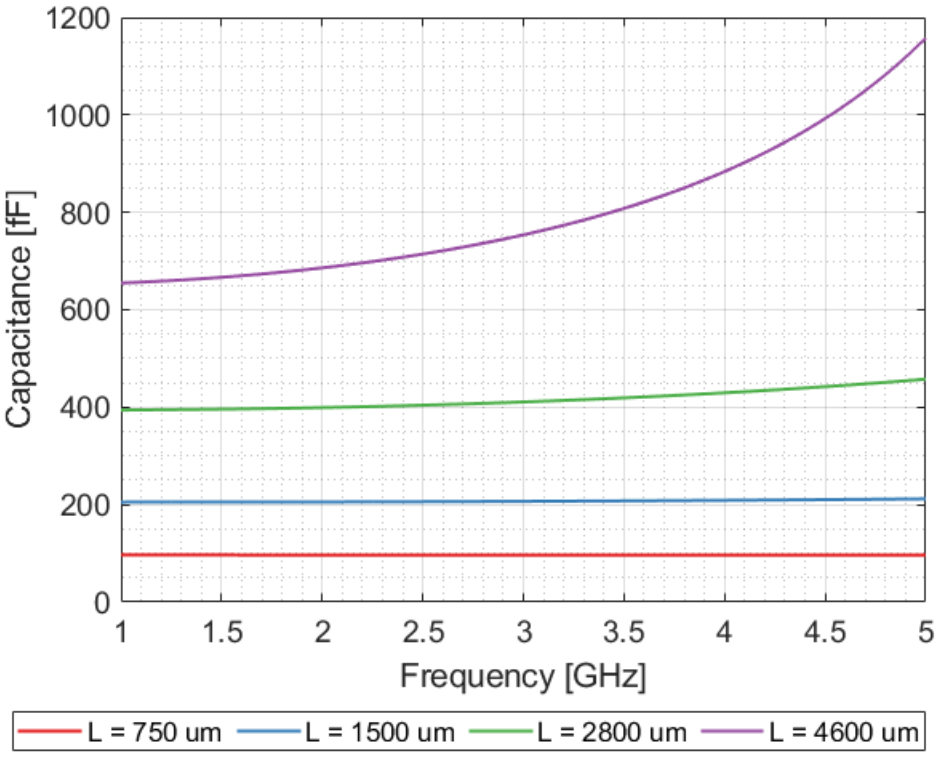

Figure 4.47: EM simulated OC CPW stub capacitors for variation 2

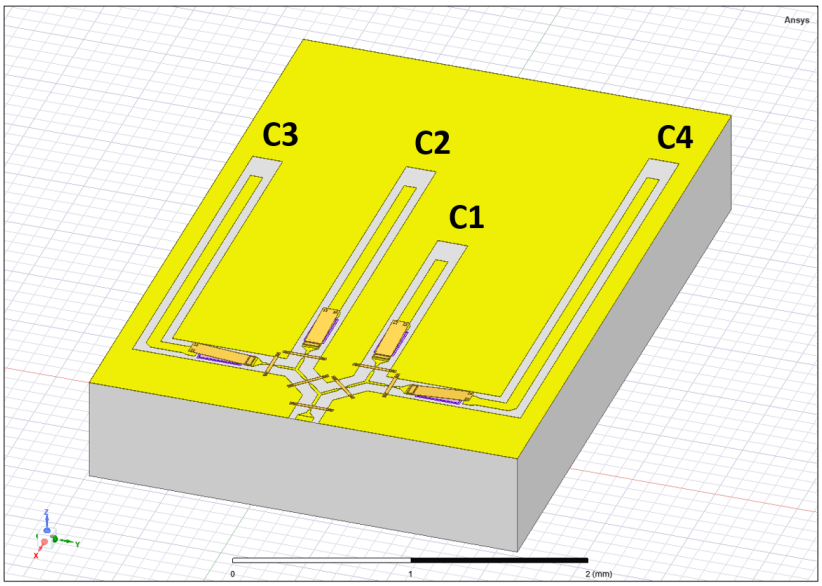

Figure 4.48: EM CPW capacitor bank model.

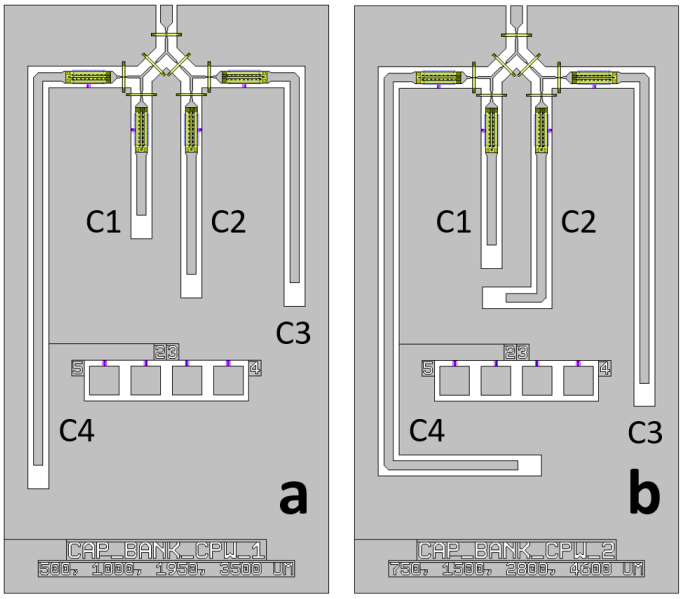

Figure 4.49: CPW capacitor bank layout.

pacitance values is shown in Figure 4.50. At lower states, the capacitance remains nearly constant with increasing frequency. But at higher capacitance value states, the capacitance slopes up with frequency as it approaches the self resonance frequency of the capacitor. At 3.6 GHz, the expected capacitance range is from 320 fF to 2.05 pF, with a consistent spacing between the individual states. The minimum capacitance is around 330 fF from 2 to 4 GHz. The maximum capacitance at state 16 goes from 1500 fF at 2 GHz, to 2340 fF at 4 GHz.

The circuit simulation results for the second variation of CPW capacitor bank is shown in Figure 4.51. At lower capacitance states, the capacitance remains relatively constant with increasing frequency. However, at higher capacitance value states, it can be seen that the capacitance increases when approaching the self resonance frequency. With the higher capacitance values, it can be seen that the self resonance frequency is much lower, and the slope of capacitance vs frequency is steeper at higher states than the first variation. At 3.6 GHz, the simulated capacitance range is from 330 fF to 3.4 pF. The spacing between the states is also not as consistent, as some states (where more switches are actuated or more capacitor components are used) have higher trend upwards faster with frequency. The minimum capacitance remains the same as the previous variation, with a value of 330 fF from 2 to 4 GHz, with all switches in the OFF state. The maximum capacitance at state 16 goes from 2 pF at 2 GHz to 4.5 pF at 4 GHz for the range of 2 to 4 GHz. The self resonance frequency of the first variation is further away from that of the second variation, due to being designed with lower capacitance values.

The CPW capacitor bank devices were fabricated using the microfabrication process reported above, released, and tested. Unfortunately, the RF-MEMS SPST switches had a poor yield that stemmed from the fabrication and reliability issues discussed in Chapter 3. Because of this, ball bonding was used to actuate the SPST switches to acquire mea-

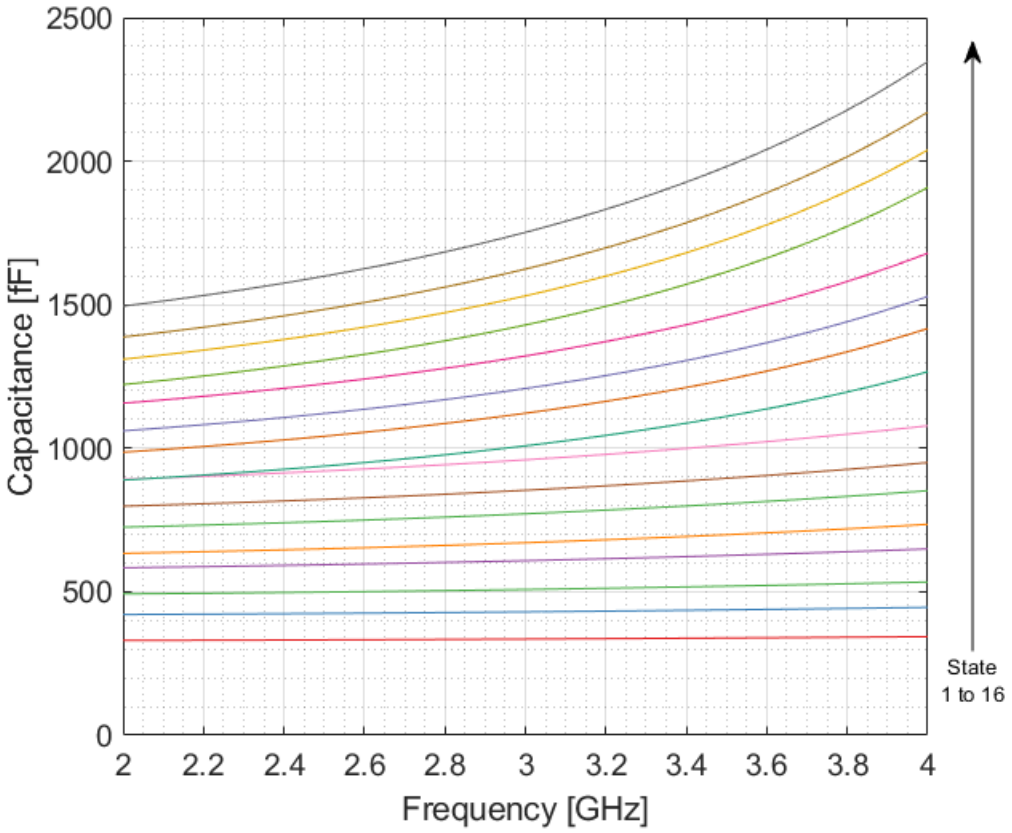

Figure 4.50: Circuit simulation capacitance values of the 16 states for the CPW capacitor bank, variation 1.

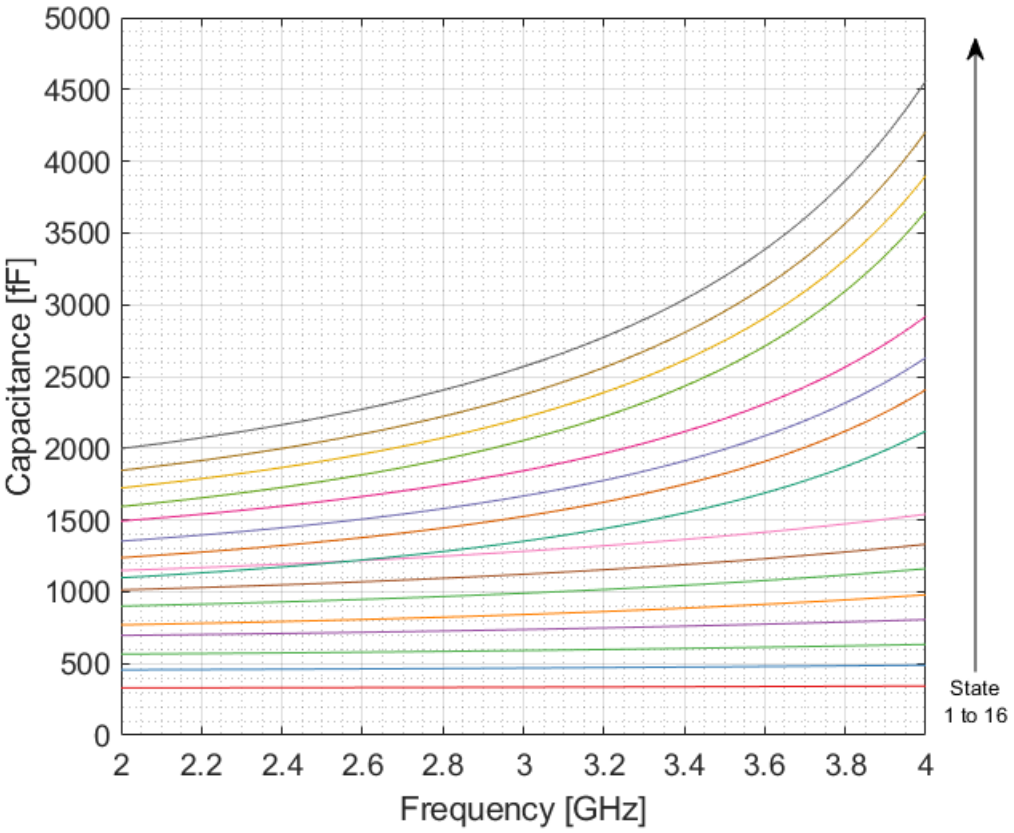

Figure 4.51: Circuit simulation capacitance values of the 16 states for the CPW capacitor bank, variation 2.

surement results for all states of the switched-capacitor banks and evaluate the fabricated performance of the switched-capacitor bank designs irrespective of the SPST, and compare them to the simulated performance.

Figure 4.53 shows the measured capacitance values of the 16 possible states for the first variation of the device, while Figure 4.54 shows the test results for the second variation. The measured results match up very well with the values from the circuit simulations. The OFF state capacitance is measured to be 400 fF rather than 330 fF, and the capacitance spacing between states is less consistent at higher capacitance values.

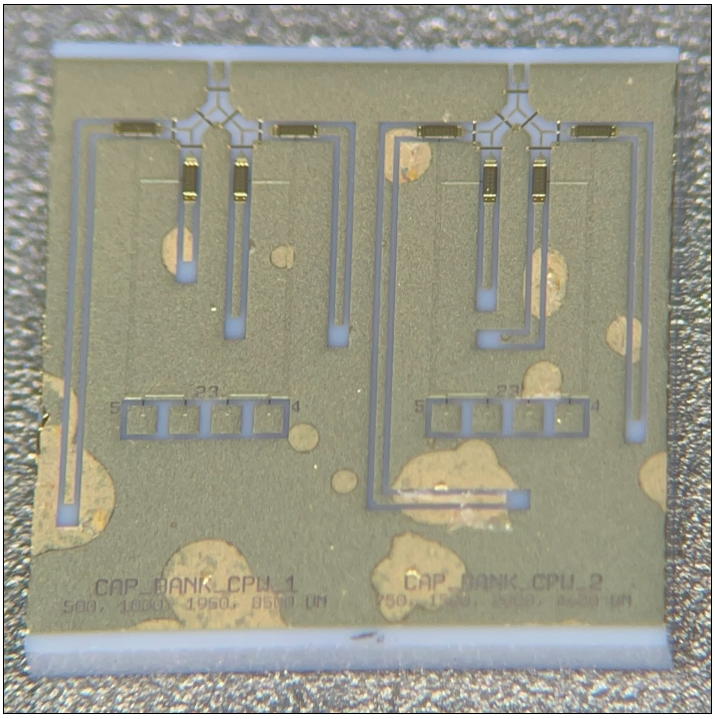

Figure 4.52: Microfabricated CPW loaded RF-MEMS capacitor bank.

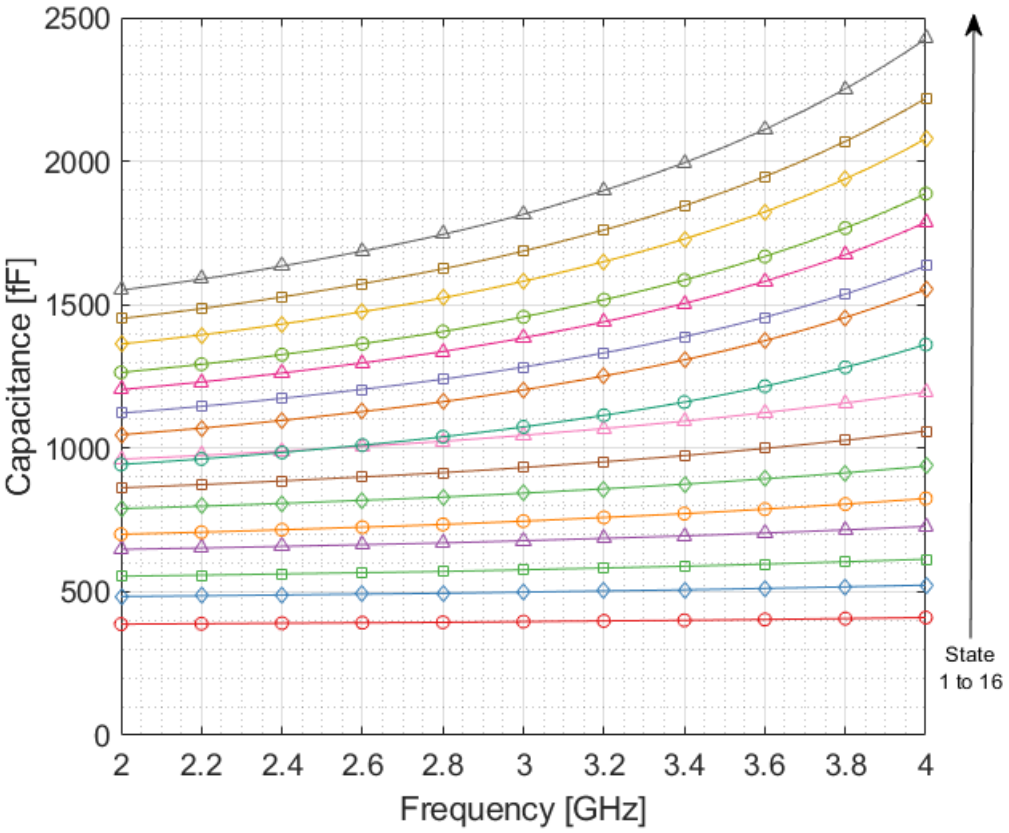

Figure 4.53: Measured capacitance values of the 16 states for the CPW capacitor bank, variation 1 (ball bonded).

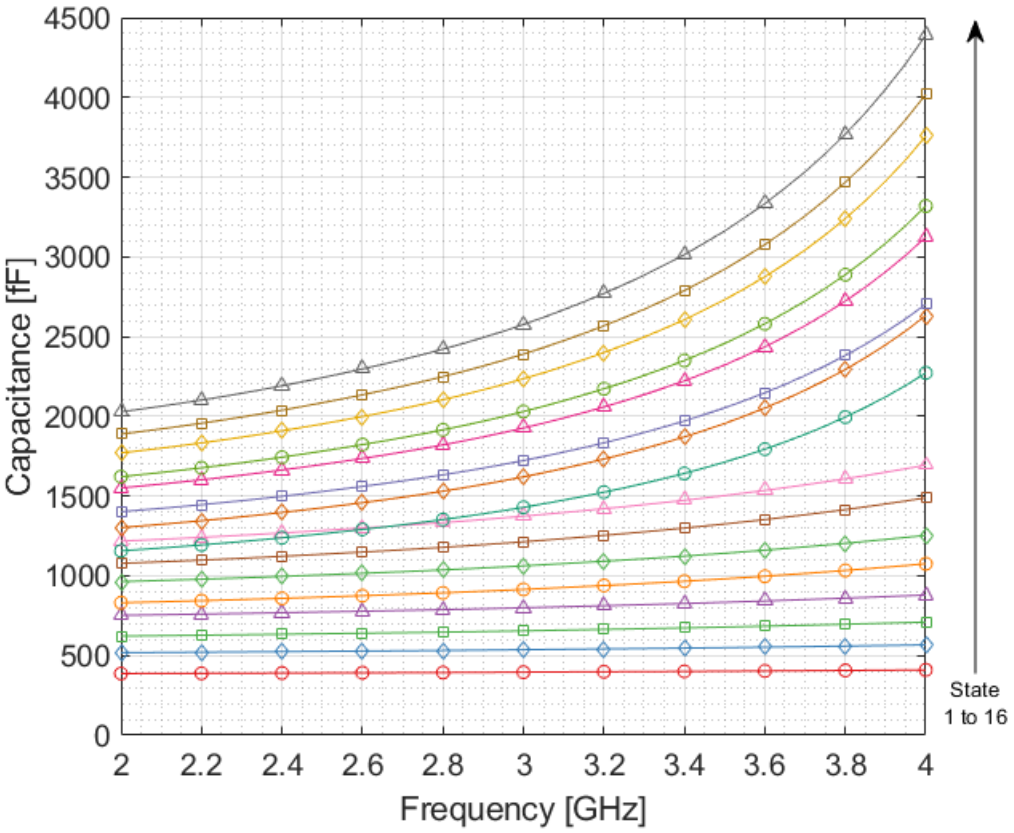

Figure 4.54: Measured capacitance values of the 16 states for the CPW capacitor bank, variation 2 (ball bonded).

MIM Capacitor Banks

A capacitor bank at was designed and fabricated using metal-insulator-metal (MIM) capacitors instead of OC CPW stub capacitors. With monolithic integrated circuits, space is often limited, and MIM capacitors have the benefit of realizing comparable high capacitance values while taking up significantly less space than OC CPW stubs. MIM capacitors also offer the advantage of a higher Q-factor than OC CPW stub capacitors.

However, since the capacitance values rely on the thicknesses of the process layers and overlapping area of the conductors, the microfabrication process must be finely tuned. Any microfabrication tolerance issue like thickness variations in the dielectric layer or distortions in feature dimensions from microfabrication can affect the capacitance.

Table 4.5: Overlapping area values for MIM capacitor banks.

Parameter	**Overlapping Area (um^2)**	
	Variation 1	**Variation 2**
C1	1089	1351
C2	2604	3916
C3	6156	9342
C4	13504	19352

Like the CPW capacitor bank device, the MIM capacitor bank is designed by incorporating four MIM capacitors of different values matching Table 4.3 into the previously designed SP4T reversed RF-MEMS switch. An EM model of the MIM capacitor bank can be seen in Figure 4.55. The layout of the two device variations can be observed in Figure 4.56 and the overlapping area values for the component MIM capacitors can be seen in Table 4.5.

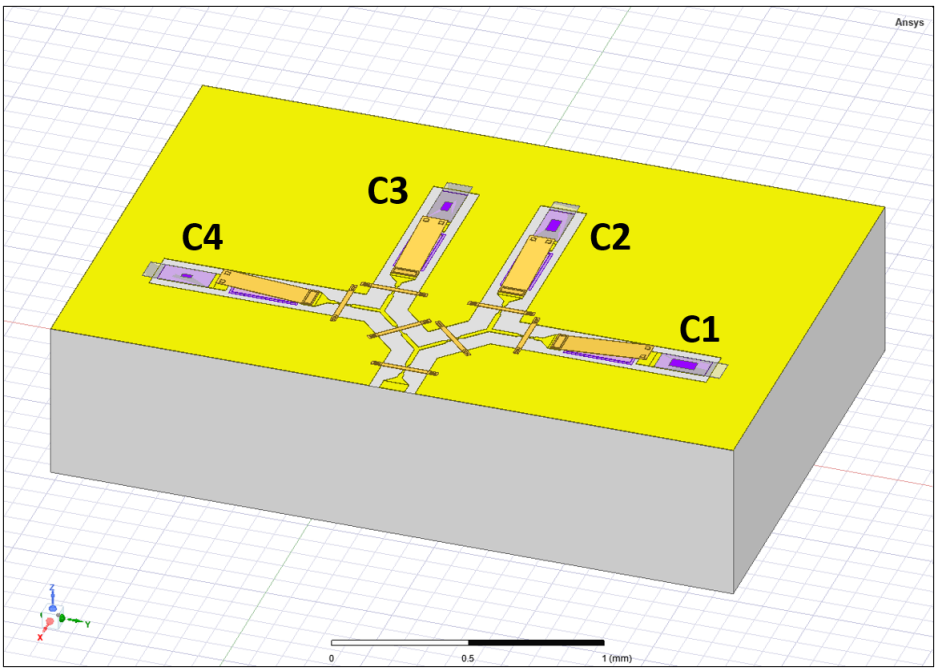

Figure 4.55: EM MIM capacitor bank model.

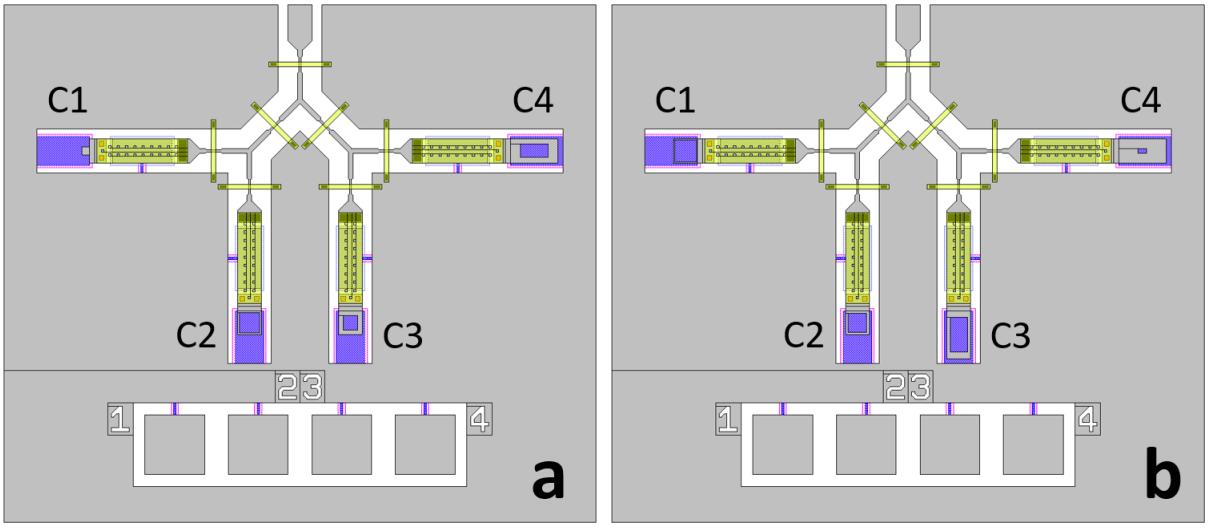

Figure 4.56: MIM capacitor bank layout.

For MIM capacitors, the dielectric constant varies with frequency. To find the dielectric constant of the SiO_2, test capacitors were fabricated using the same microfabrication process and tested using RF proves and a vector network analyzer. Using the S-parameters extracted from testing, the capacitance at 3.6 GHz was used to find the dielectric constant at the target frequency.

This extracted dielectric constant value was used to design the MIM capacitors, and was imported into an EM simulation to verify the capacitor designs at the target frequency. To further improve the reliability of the capacitors, the thickness of the dielectric was measured prior to patterning of the upper metal layer before patterning. This was to find the necessary overlapping area with the measured SiO_2 dielectric constant and thickness to realize the desired capacitance values.

A circuit simulation of the two MIM capacitor bank variations was conducted using lumped capacitors in a schematic simulator. Figure 4.57 shows the variation with smaller capacitance values, while Figure 4.58 reports the simulated capacitance values of the capacitor bank variation designed with larger values in mind. Like the CPW based capacitor banks, variation 1 has a self resonance frequency further away from the operation frequency, and has less capacitance variation versus frequency for higher states in the range of 2 to 4 GHz. The OFF state capacitance for the circuit simulation is seen to be 310 fF for both variations. Variation 1 has a maximum capacitance range of 1.5 pF at 2 GHz to 2.34 pF at 4 GHz, and has less variation in capacitance in incremental capacitor bank states when compared to variation 2.

With the second variation of the MIM based capacitor banks, the simulated maximum capacitance range at state 16 goes from 2 pF at 2 GHz, to 4.5 pF at 4 GHz, due to the self resonance frequency being much closer to the operational frequency. The increments in capacitance vs operational states is less consistent, especially state 8 to 9, and 12 to 13.

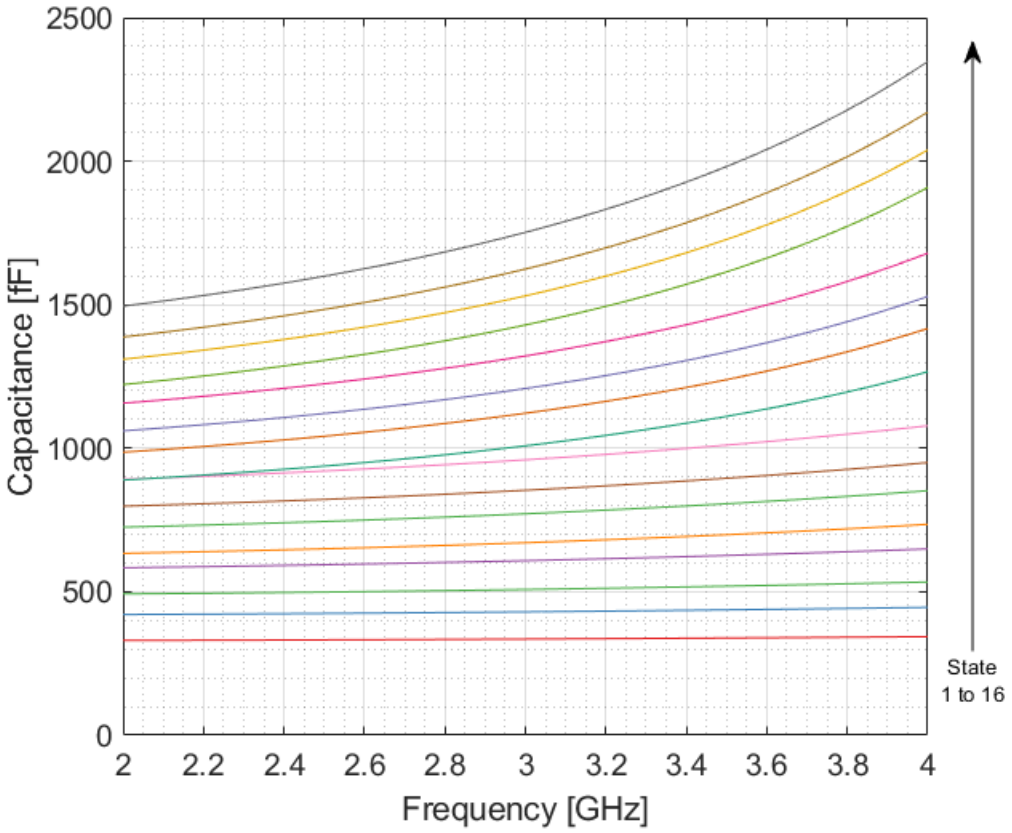

Figure 4.57: Circuit simulation capacitance values of the 16 states for the capacitor bank, variation 1.

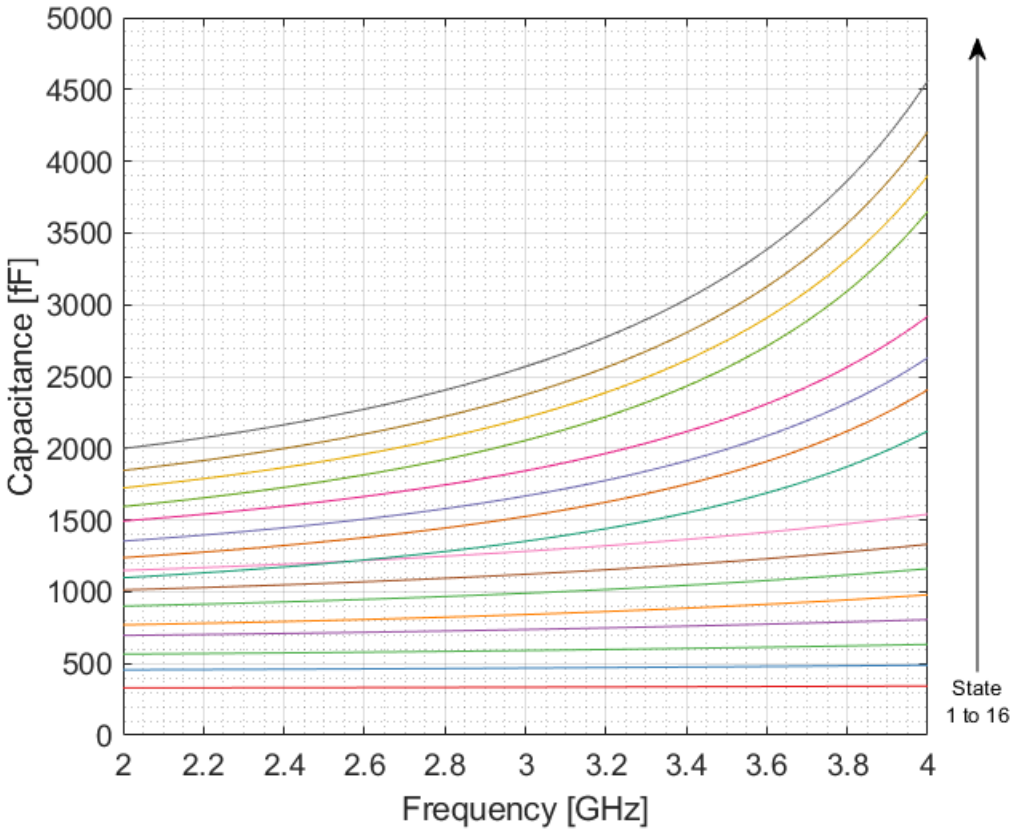

Figure 4.58: Circuit simulation capacitance values of the 16 states for the capacitor bank, variation 2.

The released MIM based capacitor banks can be seen in Figure 4.59 and Figure 4.60. Unfortunately, the MIM based capacitor banks did not survive the microfabrication process and due to the issue with oxygen plasma etching of the Cr layer mentioned in the previous section. Because the Cr layer acted as the bottom electrode of the devices, damage to this layer affected the capacitance values and ruined the devices. As discussed before, alternative fabrication steps will be taken to avoid this issue for future devices.

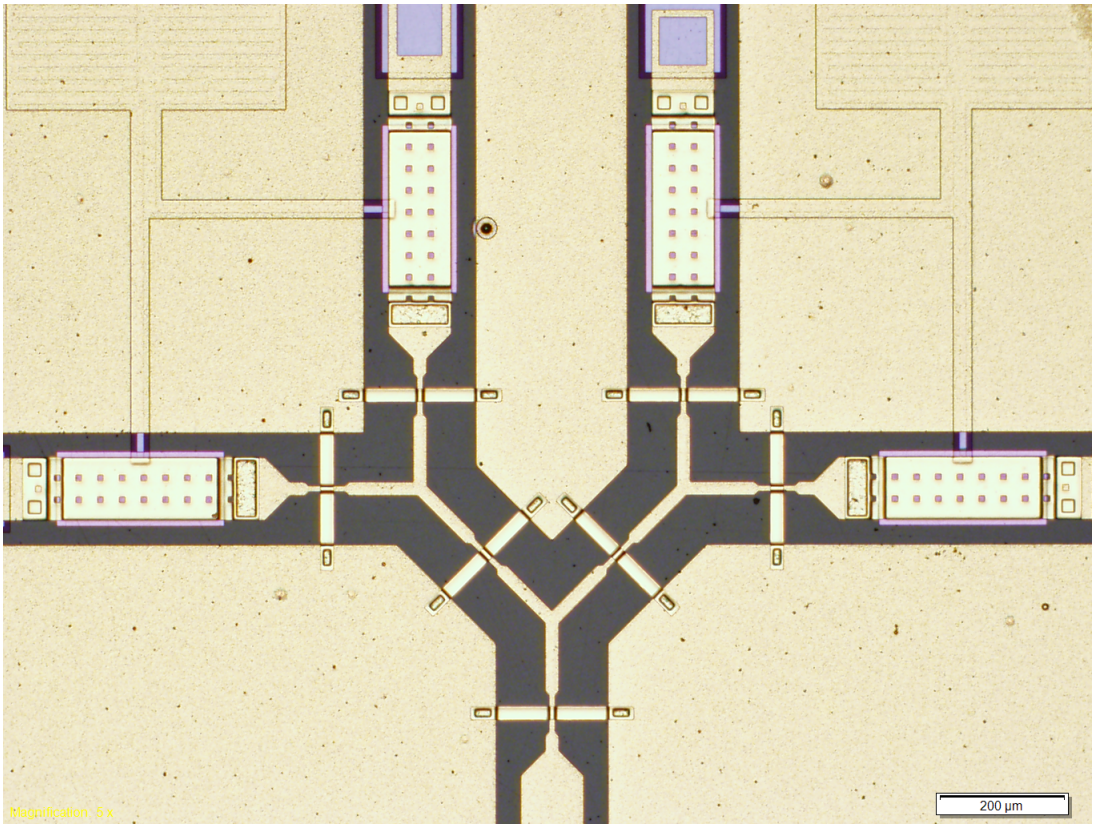

Figure 4.59: Optical micrograph of released MIM loaded RF-MEMS capacitor bank.

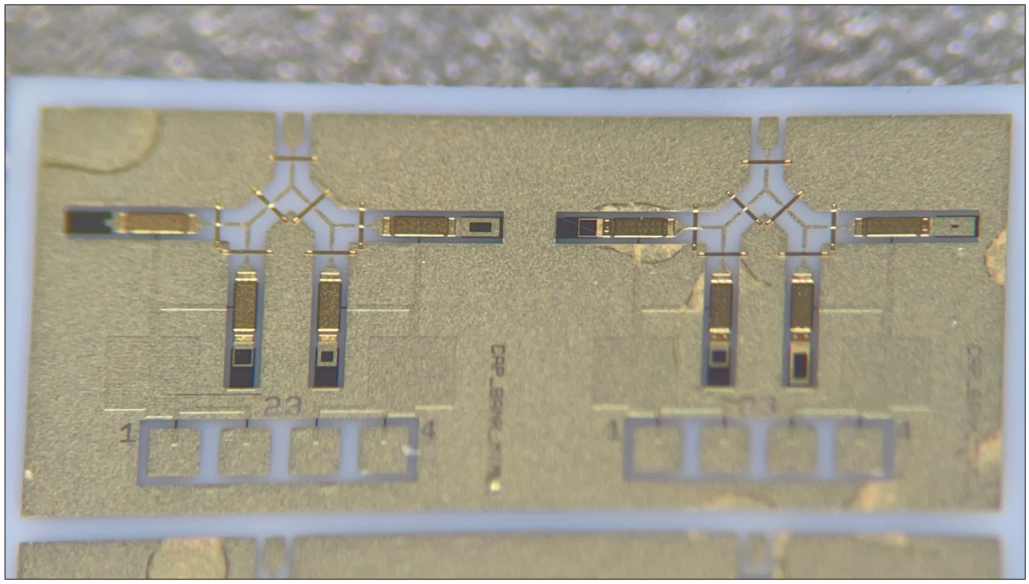

Figure 4.60: Microfabricated MIM loaded RF-MEMS capacitor bank.

Chapter 5

Design and Testing of Reconfigurable RF Phase Shifters

This chapter reviews the design of a reconfigurable 360° RF-MEMS phase shifter at a center frequency of 3.6 GHz, with a bandwidth of 400 MHz. To accomplish this, a distributed MEMS transmission line (DMTL) is periodically loaded using the previously designed RF-MEMS switched-capacitor banks to achieve a 40° reconfigurable phase shifter at a frequency and bandwidth of 3.6 GHz and 400 MHz respectively. This design is then integrated with switched-line phase shifters to extend the total phase shift range to 360°.

A distributed MEMS transmission line was demonstrated using the concept of synthetic transmission lines, and achieved a phase shift by loading the line with MEMS bridge capacitors [15]. When actuated, the bridge would pull-in, and load the line. However, this results in a digital phase shifter, limited by the number of bits, and the number of switch states per bit, and leaving large discrete gaps in phase between different states. Analog phase shifters have also been demonstrated to be realizable by loading transmission lines

with varactor diodes, avoiding this issue [14].

5.1 Distributed MEMS Transmission Line (DMTL) Phase Shifters

The propagation constant of a transmission line is given by Eqn. 5.1,

$$\gamma = \alpha + j\beta \tag{5.1}$$

where γ is the propagation constant, α is the attentuation constant, and *beta* is the phase constant of a transmission line. The propagation constant for a lossless line can also be expressed and simplified to Eqn. 5.2

$$\gamma = \sqrt{Z'Y'} = \sqrt{(R' + j\omega L')(G' + j\omega C')} \approx j\omega\sqrt{L'C'} \tag{5.2}$$

where ω is the angular frequency, and Z' is the series impedance, Y' is the shunt admittance, R' is the resistance, L' is the inductance, G' is the conductance, and C' is the capacitance of the transmission line per unit length.

The phase constant of the transmission line can be expressed as

$$\beta = Im(\gamma) = \omega\sqrt{L'C'} \tag{5.3}$$

From this, the equation for the phase velocity of the transmission line as

$$V_p = \frac{\omega}{\beta} = \frac{1}{\sqrt{L'C'}} \tag{5.4}$$

The phase shift per unit length of the transmission line is given by Eqn. 5.5 [1],

$$\Delta\phi = \beta_1 - \beta_2 = \omega\left(\frac{1}{V_{p1}} - \frac{1}{V_{p2}}\right) \tag{5.5}$$

where V_{p1} is the initial phase velocity of the transmission line per unit length and V_{p2} is the phase velocity of the transmission line per unit length after being loaded. Combining Eqn. 5.4 and 5.5, the phase shift per unit length reduces to

$$\Delta\phi = \omega\left(\frac{1}{\sqrt{L_1'C_1'}} - \frac{1}{\sqrt{L_2'C_2'}}\right) \tag{5.6}$$

Therefore, increasing the load capacitance decreases the phase velocity of the transmission line, creating a phase delay along the line and achieving a relative phase shift from the original state. A DMTL phase shifter can be designed with multiple bits to increase the maximum possible amount of phase shift, and increase the number of possible states/configurations. Typical MEMS phase shifters use MEMS bridge switch capacitors which are only capable of 2 states, and thus use a lot of bits to achieve more states and a smaller step size [15]. Analog performance can be achieved using analog variable capacitor components like varactors [14].

5.2 3-Bit Reconfigurable 40° DMTL Phase Shifter Design

A distributed MEMS transmission line (DMTL) RF phase shifter was designed by loading a CPW transmission line with the MEMS switched-capacitor banks presented in Chapter 4. The design specifications of the RF phase shifter was to achieve a 40° relative phase delay at 3.6 GHz, with a bandwidth of 400 MHz. Additional variations at 3.75 GHz and 3.9 GHz were also designed, with the same amount of phase shift and bandwidth. A 3-bit design was used for the 40° phase shifters. The circuit schematic can be seen in Figure 5.1.

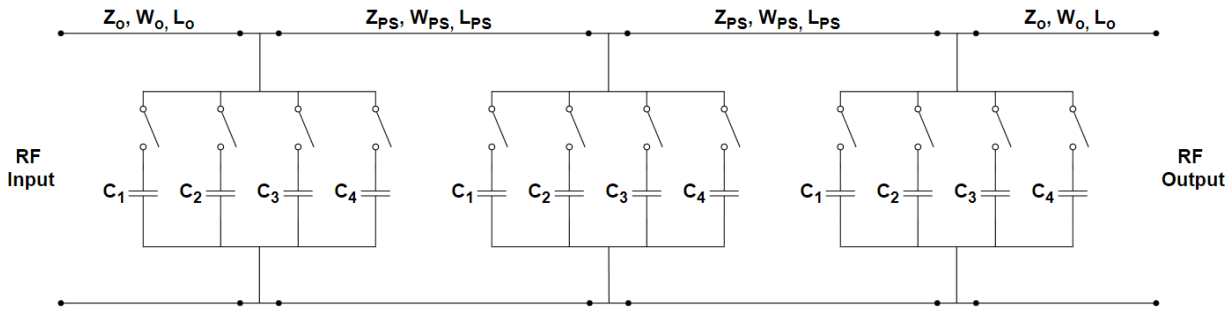

Figure 5.1: Circuit schematic for the 40 degree RF phase shifter design.

An ideal lumped model circuit simulation was used to find the required capacitance values for the corresponding design specifications of the phase shifter. The EM results of the SP4T switches from Chapter 4 were imported into the circuit model to improve the reliability of the model, and the values were tuned again to meet the required phase shift. Two variations of the RF phase shifter were designed for each desired frequency, one using the MIM capacitors and the other using the open circuit CPW stubs as capacitors to load the capacitor banks. For the capacitance values, C1 to C4 were designed to be the values

at which when all 3 bits were actuated to C1, C2, C3, or C4, the corresponding phase shift would be 10°, 20°, 30°, and 40°. C4 would be the capacitor with the highest capacitance out of the four, and its maximum capacitance was limited to the highest achievable capacitance from the previous capacitor bank designs.

The capacitor values were designed this way to make simulating and testing of the phase shifter simpler, actuating only one SPST per bit at a time. The final design would readjust the capacitance values, and use the C4 capacitance as the largest possible capacitance from the switched-capacitor bank, when all 4 switches would be actuated.

The characteristic impedance of the transmission line, Z_{PS}, was also increased to offset the effect of loading the line with capacitance and make the effective line impedance closer to 50Ω when loaded with the capacitors.

An EM simulation was run for each variation at each frequency to have a more reliable prediction of the phase shifter performance, and then compared to the circuit simulation. The EM simulation model for the OC CPW stub loaded 40° RF phase shifter is shown in Figure 5.2.

The final dimensions of the OC stub CPW loaded 40° RF phase shifters can be seen in Table 5.1. The OC stub width (W_C) and OC stub line impedance (Z_C) were kept constant at 75μm and 58Ω respectively. The OC stub length (L_C), bit transmission line length (L_{PS}), width (W_{PS}), and impedance (Z_{PS}) were tuned for each frequency to achieve a total phase shift from 0° to 40° in 10° increments, at target frequency.

The EM and circuit simulated RF performance of the OC stub CPW loaded 40° RF phase shifter, centered at 3.6 GHz, can be seen in Figure 5.3. The simulations present the RF performance of the phase shifter when the switched-capacitor banks for all 3 bits are off (C0), and switched from C1 to C4. The insertion loss is very low for both the EM and

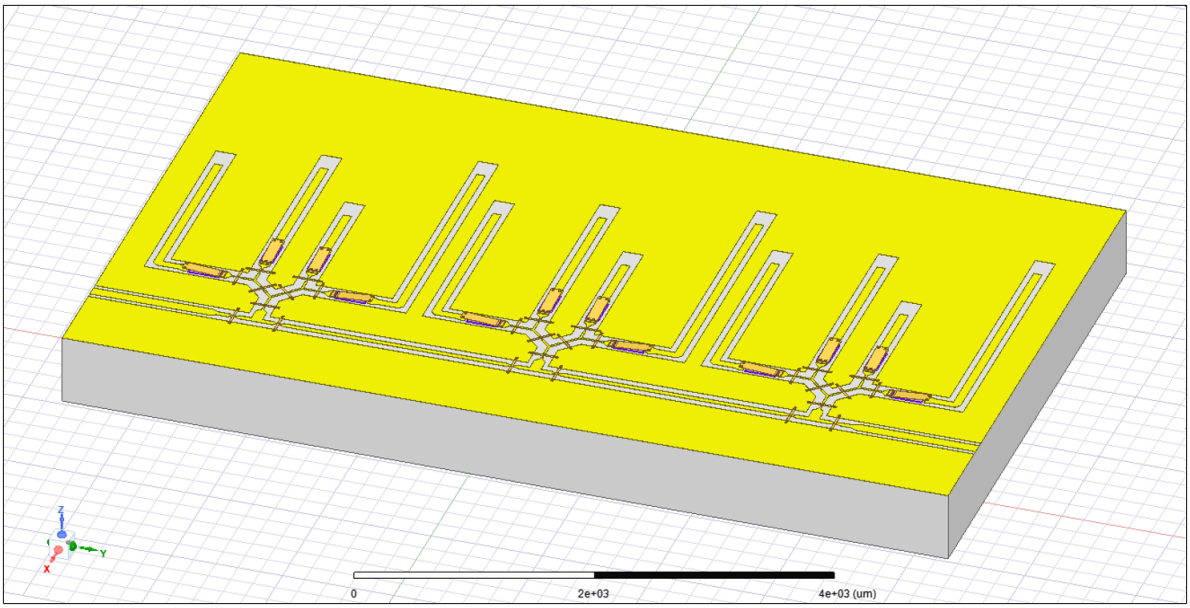

Figure 5.2: EM CPW based 40° phase shifter model.

Table 5.1: CPW based 40° phase shifter parameters.

Target Frequency (GHz)	**3.6**				**3.75**				**3.9**			
CPW Capacitor #	**C1**	**C2**	**C3**	**C4**	**C1**	**C2**	**C3**	**C4**	**C1**	**C2**	**C3**	**C4**
OC Stub Length, L_C (μm)	600	1400	2100	2800	550	1300	1950	2600	500	1200	1750	2400
OC Stub Width, W_C (μm)	75											
OC Stub Line Impedance, Z_C (Ω)	58											
Line Length, L_{PS} (μm)	2925				2700				2500			
Line Width, W_{PS} (μm)	60				55				50			
Line Impedance, Z_{PS} (Ω)	64				66.5				69			

circuit simulations, staying better than -2dB for all states. When looking at the return loss, though the values themselves aren't identical, the profiles of the EM simulation match well with that of the circuit simulation. All states gave a return loss better than -15dB.

Figure 5.4 shows the phase and relative phase shift of the OC stub CPW loaded 40° RF phase shifter, centered at 3.6 GHz. Though there are differences in the phase between simulation techniques, looking at the relative phase shift shows a very good match between the EM and circuit simulations. Each state shows a phase delay of roughly 10° increments, sloping down with increasing frequency.

Figures 5.5 and 5.6 show the EM and circuit simulated RF performance and phase for the OC CPW stub loaded 40° RF phase shifter centered at 3.9 GHz. The results show comparable behaviour and performance as the phase shifter at 3.6 GHz.

Figure 5.7 shows the microfabricated and released OC CPW stub loaded 40° RF-MEMS phase shifter centered at a frequency of 3.6 GHz. The yield was very low due to the microfabrication issues discussed in Chapter 3. Because of this, ball bonding was used to actuate the SPST switches to acquire measurement results for the simulated states of the 40° RF-MEMS phase shifters, evaluate the fabricated performance of the design irrespective of the SPST reliability, and compare them to the simulated RF performance.

The measured RF performance of the released OC stub loaded 40° RF phase shifters at 3.6 GHz can be seen in Figure 5.8 and the phase in Figure 5.9. Comparing the measured insertion loss and return loss to the EM simulation results from Figure 5.3, it can be observed that the two match very well. The measured insertion loss stays better than 1.6dB even when the actuated to a phase shift of 40° (C4). This is expected since C4 loads the phase shifter with the most capacitance. When not operating, the insertion loss stays steady near 0.54dB. In all states from C0 to C4, the return loss remains lower than 17dB.

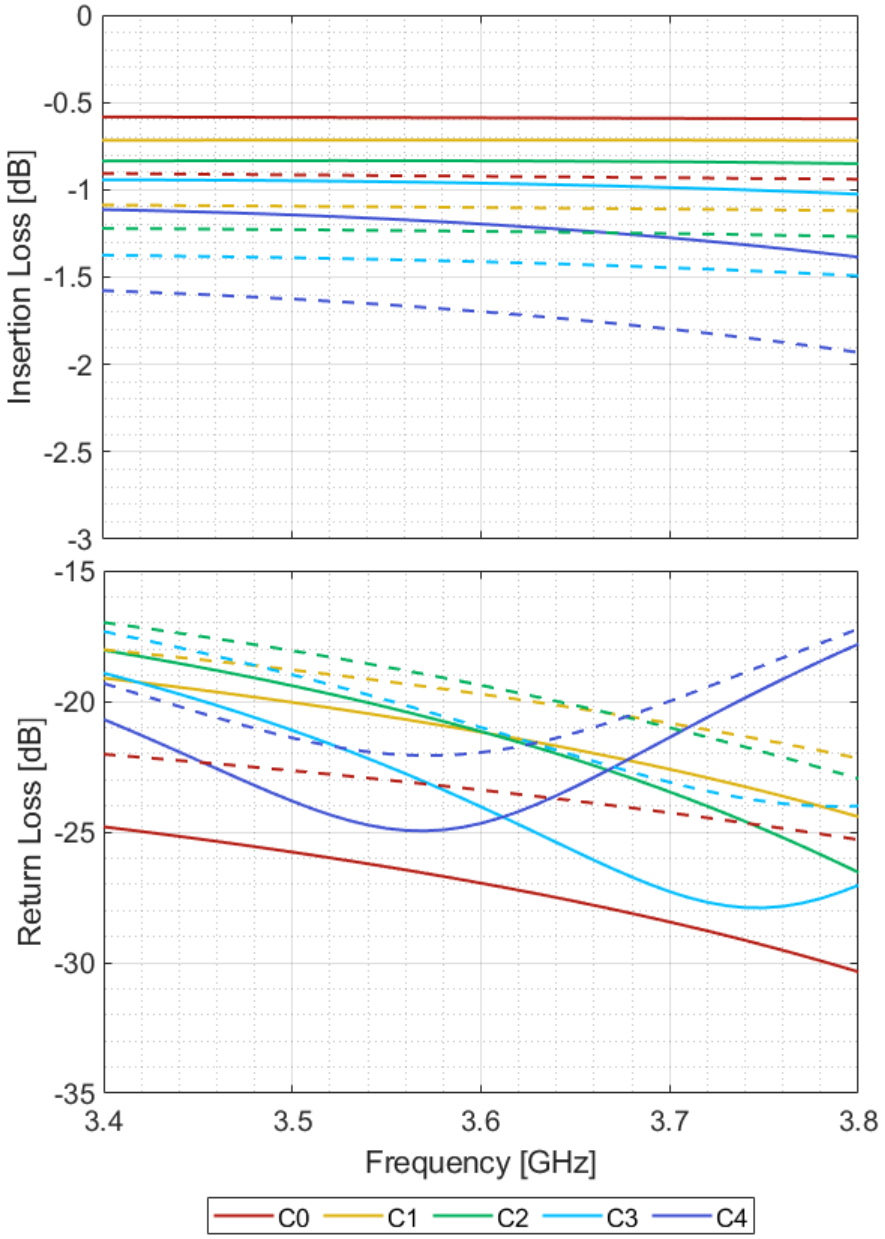

Figure 5.3: Simulated EM (line) and circuit (dash) RF performance of the OC stub CPW loaded 40° RF phase shifter at 3.6 GHz

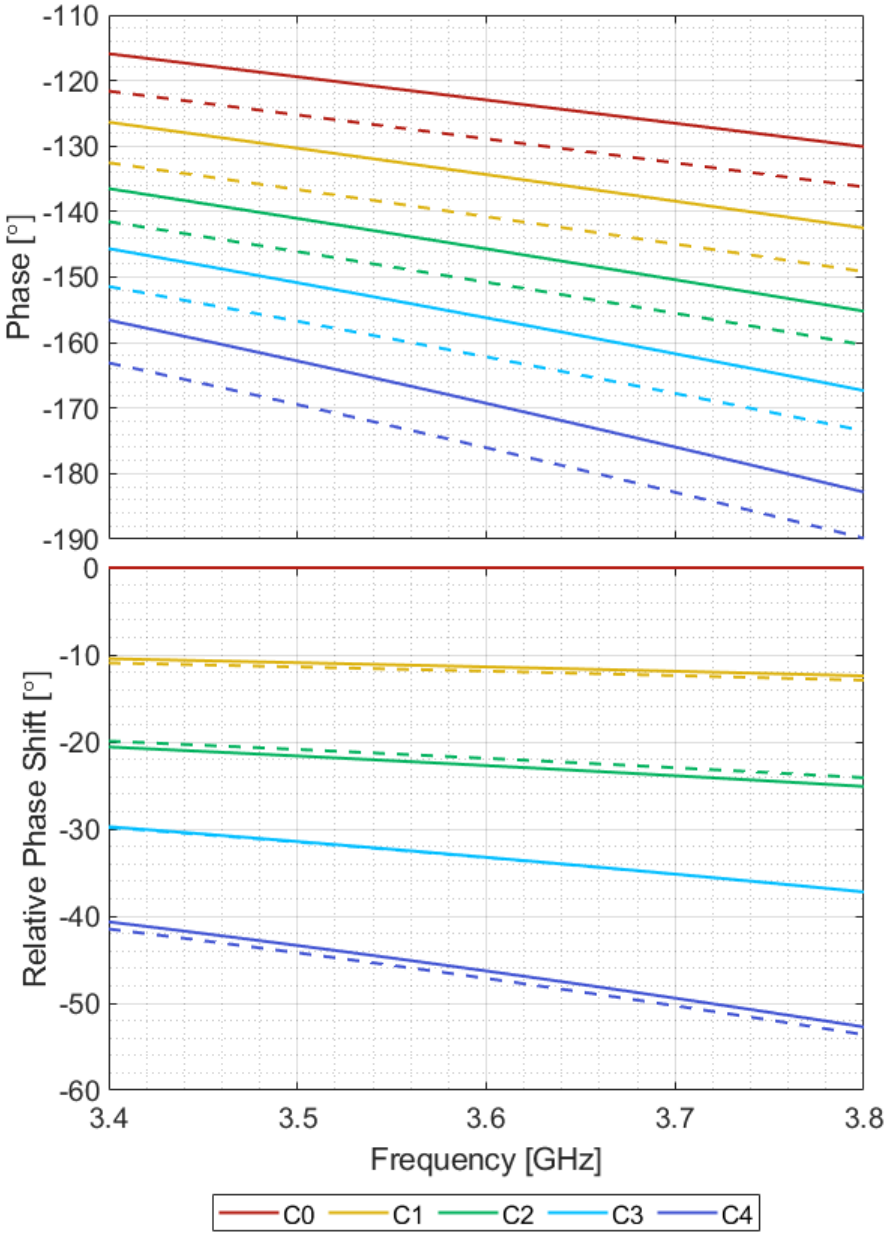

Figure 5.4: Simulated EM (line) and circuit (dash) phase of the OC stub CPW loaded 40° RF phase shifter at 3.6 GHz

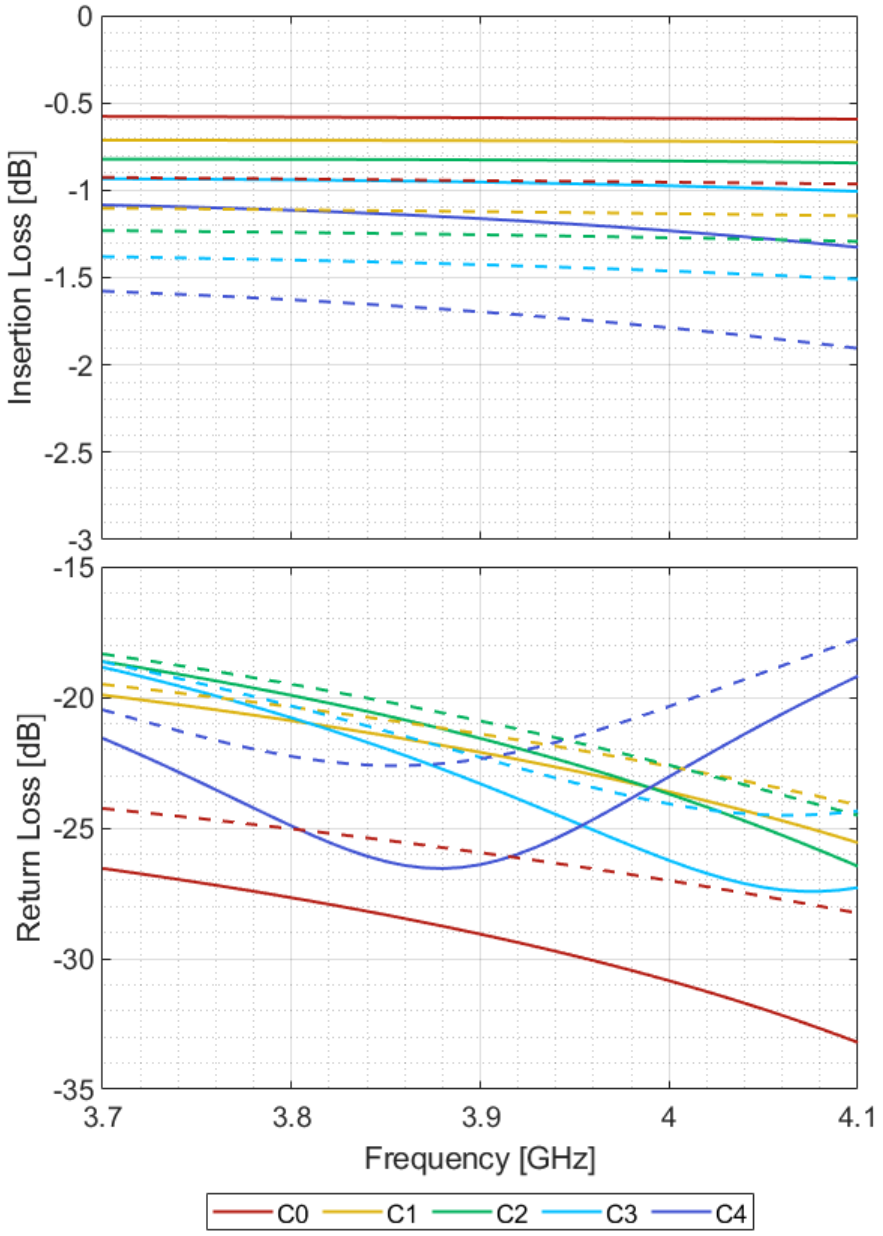

Figure 5.5: Simulated EM (line) and circuit (dash) RF performance of the 40° CPW based phase shifter at 3.9 GHz

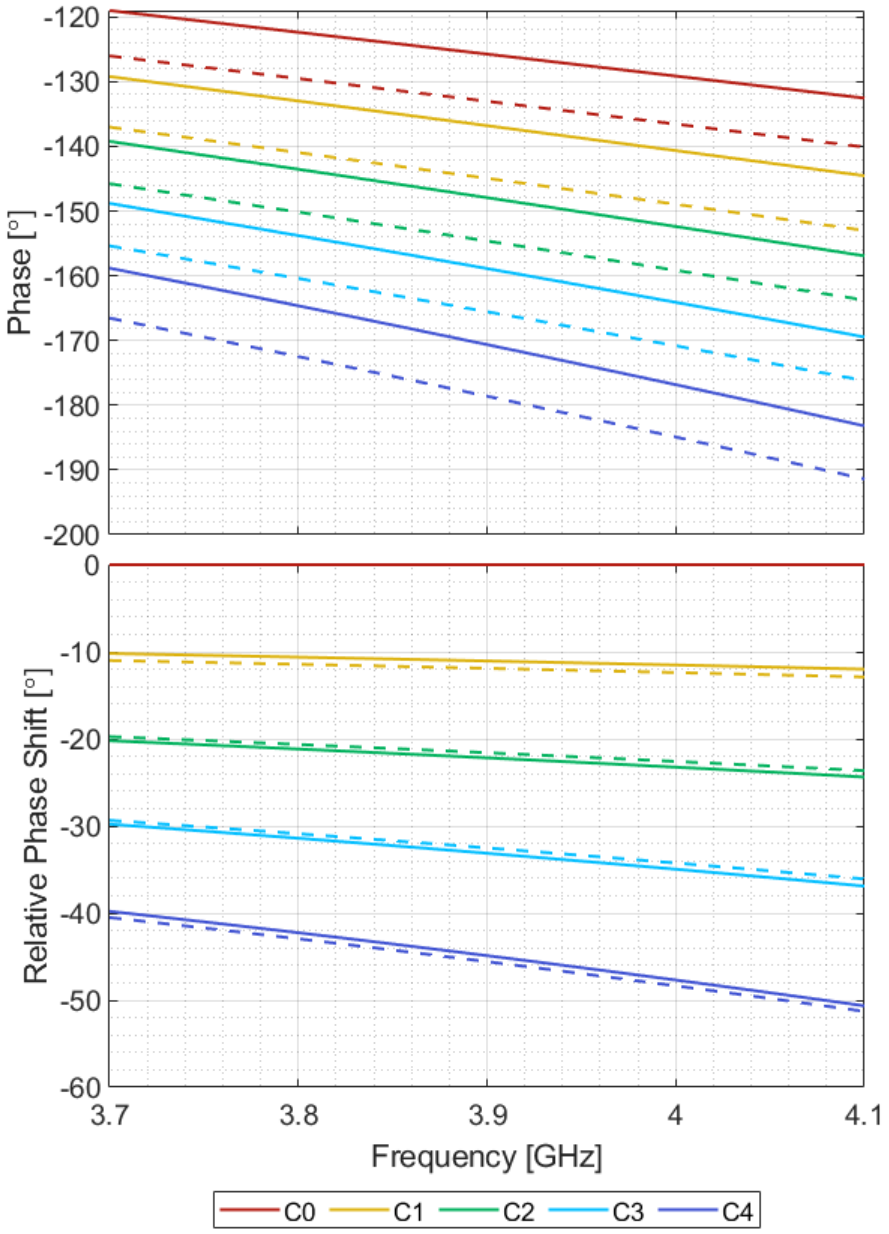

Figure 5.6: Simulated EM (line) and circuit (dash) phase of the 40° CPW based phase shifter at 3.9 GHz

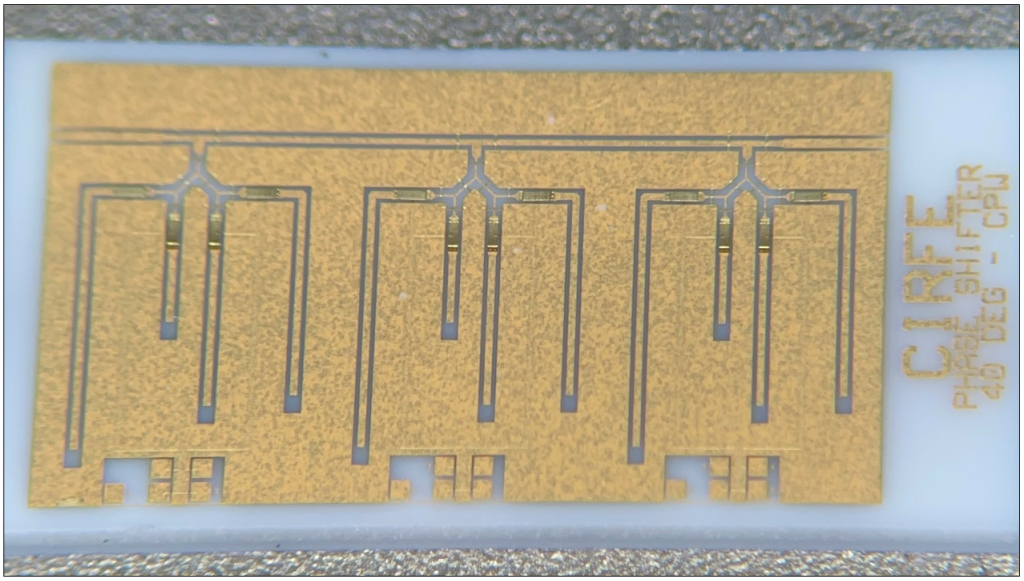

Figure 5.7: Microfabricated OC CPW stub loaded 40° RF-MEMS phase shifter centered at 3.6 GHz.

Looking at the circuit simulated relative phase shift and comparing it to the EM simulation from Figure 5.4, the measured performance matches greatly with the EM simulation results. From 3.4 GHz to 3.8 GHz, a relative phase shift of 10° intervals can be observed as the phase shifter actuates the capacitor bank from C0 to C4. The phase shift also increases with higher frequency.

The measured RF performance and phase of the OC stub loaded 40° RF phase shifter designed at 3.9 GHz can be seen in Figures 5.10 and 5.11. Much like the phase shifter at 3.6 GHz, the results match very closely to the EM simulation results in Figures 5.5 and 5.6. The only exception is the relative phase shift at C4, where the measured phase shift is less than expected; the phase delay is at -36° at 3.7 GHz, rather than the simulated -40°.

Because the measured results match well with the simulation models, a circuit simulation is used to find the performance of the 40° phase shifter in all possible combinations of the switched-capacitor bank bits. Each bit has 16 combinations, from C = 0 (OFF) to C = $15C_O$ where C_O is the unit capacitance of the capacitor bank. The capacitor values for the switched-capacitor banks for each bit is changed to use C4 as the maximum capacitance C=$15C_O$ (when all 4 switches are actuated to all 4 capacitors). Each bit has 16 combinations, from C = 0 (OFF) to C = $15C_O$ where C_O is the unit capacitance of the capacitor bank.

With 3 bits/switched-capacitor banks, the total number of configurations possible is 4096. The circuit simulated RF performance and phase of the 40° RF-MEMS phase shifters at 3.6 GHz, with all possible configurations, is shown in Figures 5.12 and 5.13. The insertion loss does not get worse than 2dB for all configurations. The worst return loss possible out of all the combinations is at 10dB. If the design specifications call for a better return loss, then the phase shifter can be operated at only the states that have a return loss below that requirement.

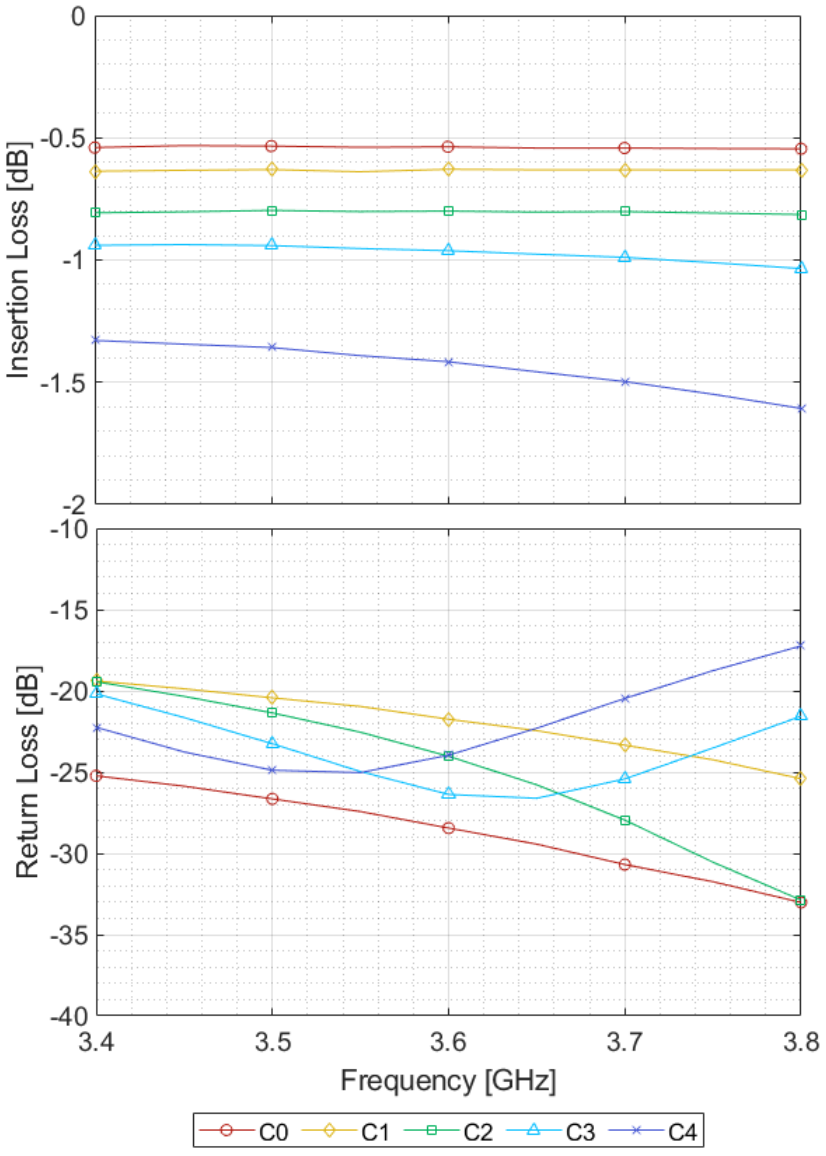

Figure 5.8: Measured RF performance of the OC stub loaded 40° RF phase shifter at 3.6 GHz (ball bonded).

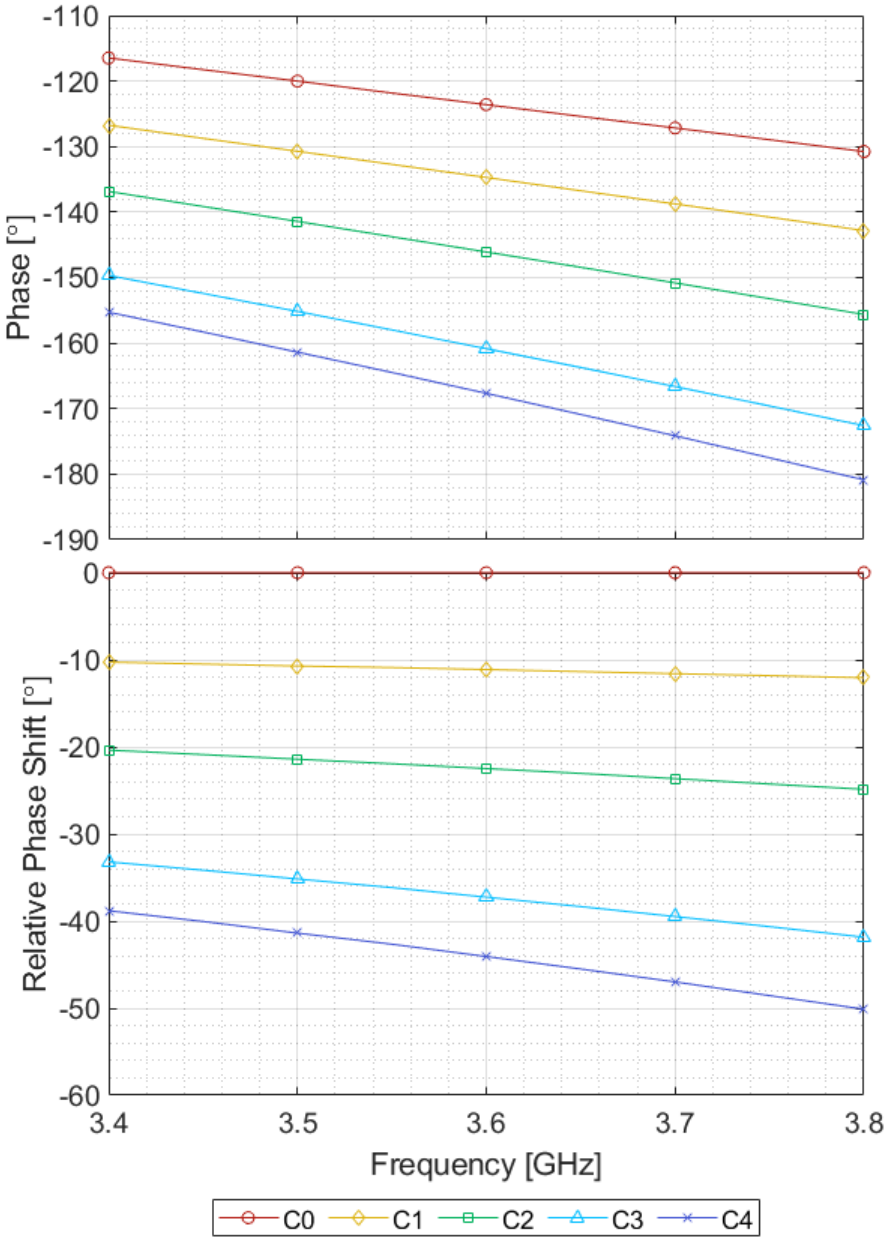

Figure 5.9: Measured phase of the OC stub loaded 40° RF phase shifter at 3.6 GHz (ball bonded).

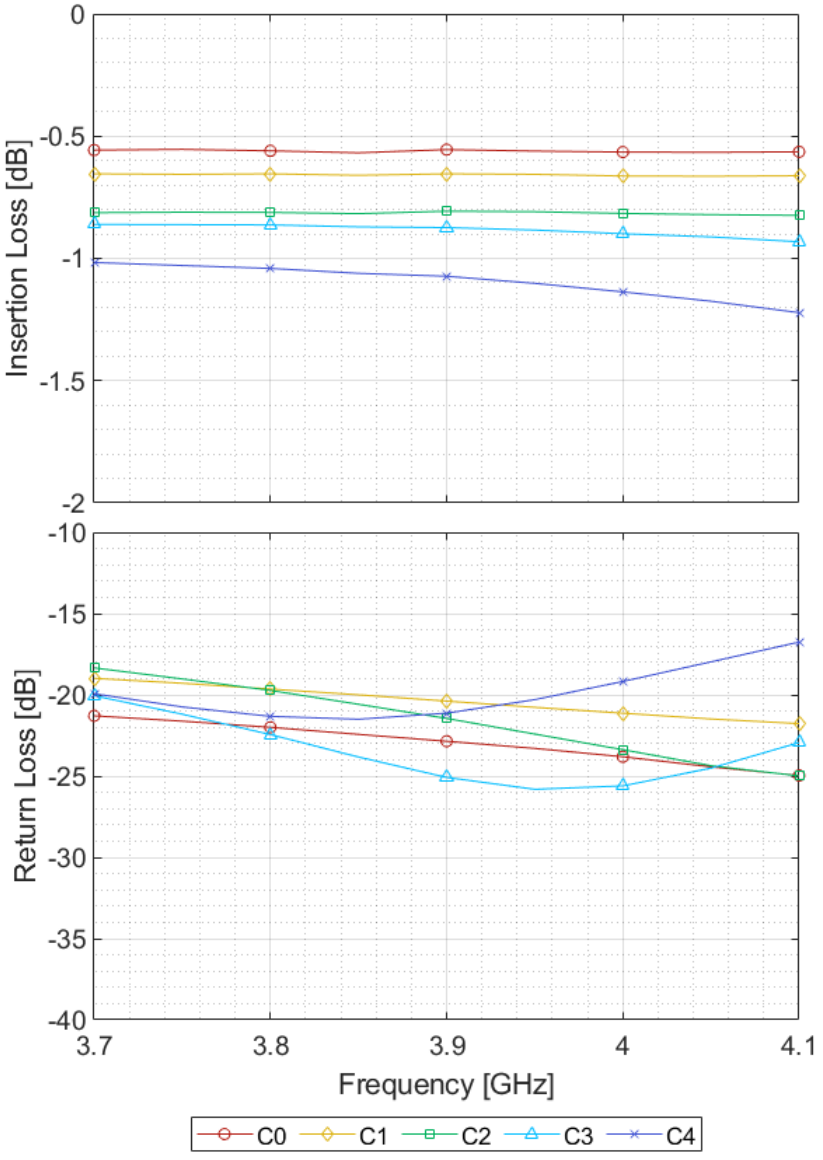

Figure 5.10: Measured RF performance of the OC stub loaded 40° RF phase shifter at 3.9 GHz (ball bonded).

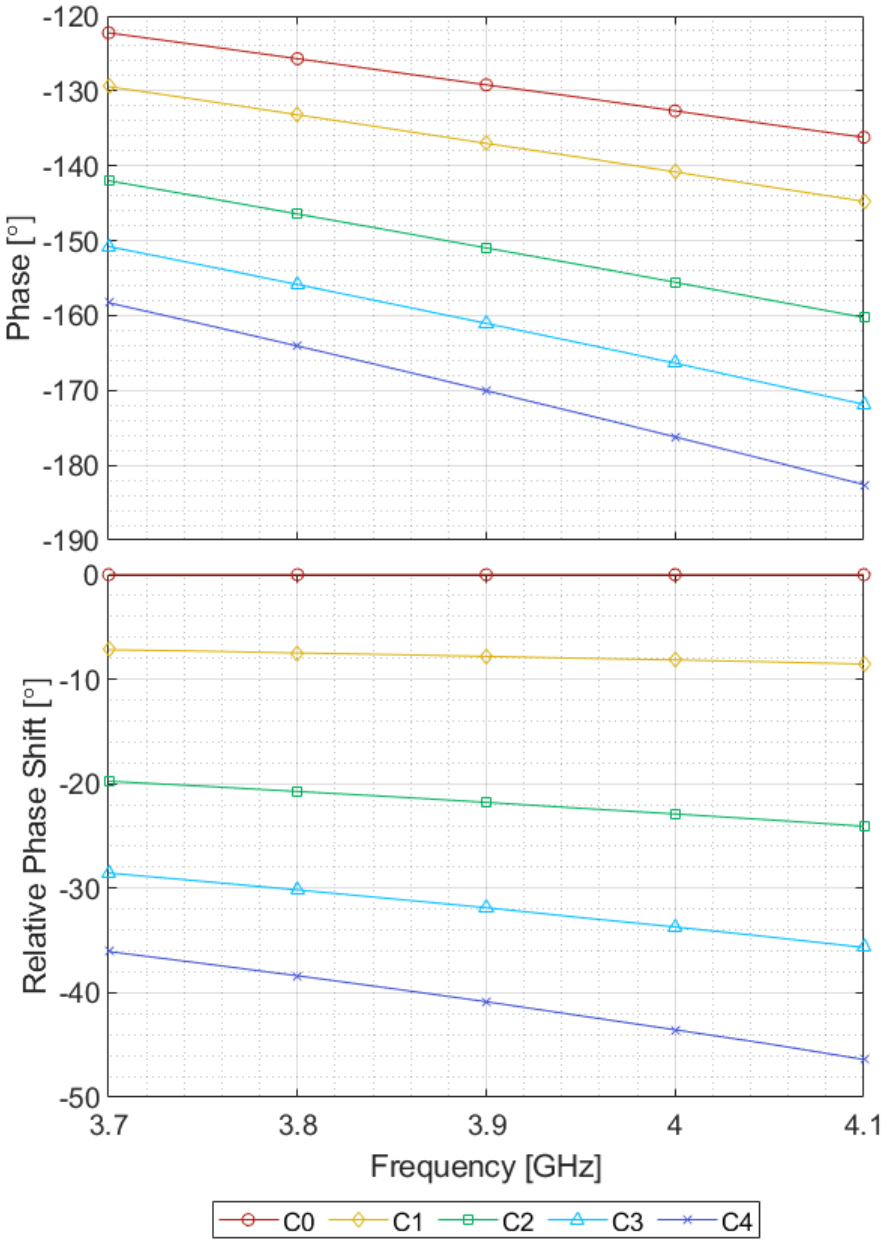

Figure 5.11: Measured phase of the OC stub loaded 40° RF phase shifter at 3.9 GHz (ball bonded).

From looking at the simulated relative phase shift, it is clear that the high number of possible configurations allow for reconfigurability with very small step sizes. This allows the digital phase shifter to operate much like an analog phase shifter.

The same plots for the 40° reconfigurable phase shifter centered at 3.9 GHz can be seen in Figures 5.14 and 5.15. The figures show very similar results to that of the phase shifter centered at 3.6 GHz. With so many possible combinations, the step size of the phase shift from 0° to 40° is so small that it can operate like a pseudo-analog phase shifter. For better return loss performance, the configurations that have a return loss worse than 15dB can be filtered out. This will likely result in a slightly larger step size for phase shift, but still have more than enough possible configurations for a reliable phase shifter.

The EM simulation model for the MIM capacitor loaded reconfigurable 40° RF phase shifter can be seen in Figure 5.16. Much like the OC CPW stub loaded version, this design consists of a 3 bit DMTL design using the previously designed switched-capacitor bank designs from Chapter 4 to load the transmission line. The design parameters for the MIM capacitor loaded phase shifter centered at 3.6 GHz, 3.75 GHz, and 3.9 GHz can be seen in Table 5.2.

Table 5.2: MIM based 40° phase shifter parameters.

Target Frequency (GHz)	**3.6**				**3.75**				**3.9**			
MIM Capacitor #	**C1**	**C2**	**C3**	**C4**	**C1**	**C2**	**C3**	**C4**	**C1**	**C2**	**C3**	**C4**
Capacitor Cutout Width (W_C) (μm)	600	1400	2100	2800	550	1300	1950	2600	500	1200	1750	2400
Capacitor Overlapping Area (A_C) (μm^2)	975	2944	4959	6864	784	2775	4524	6400	784	2431	4224	5775
Line Length, L_{PS} (μm)	2925				2700				2500			
Line Width, W_{PS} (μm)	60				55				50			
Line Impedance, Z_{PS} (Ω)	64				66.5				69			

Figure 5.17 and 5.18 show the Rf performance and phase of the 40° MIM loaded phase

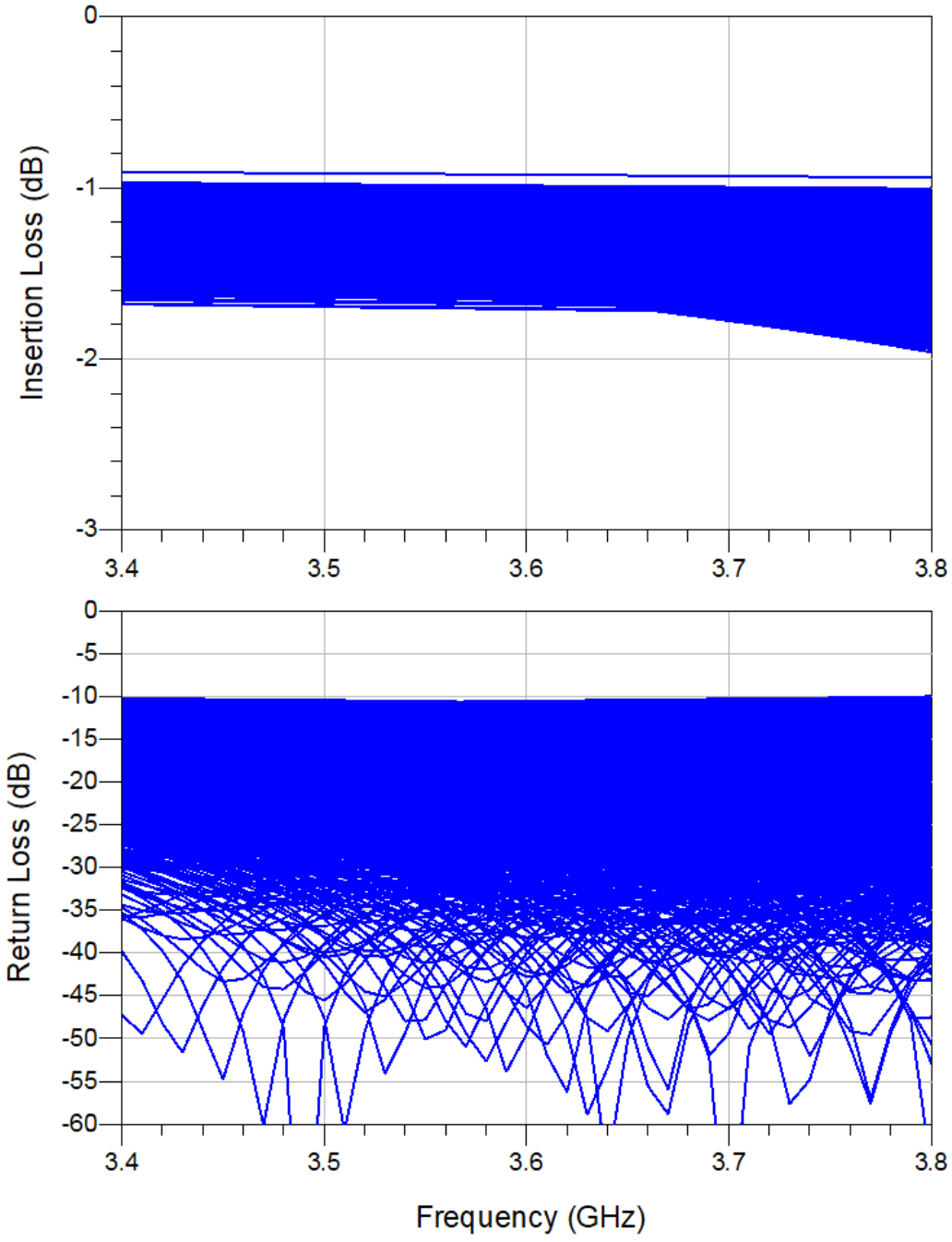

Figure 5.12: Circuit simulated RF performance of the 40° RF-MEMS phase shifter at 3.6 GHz, showing all possible configurations.

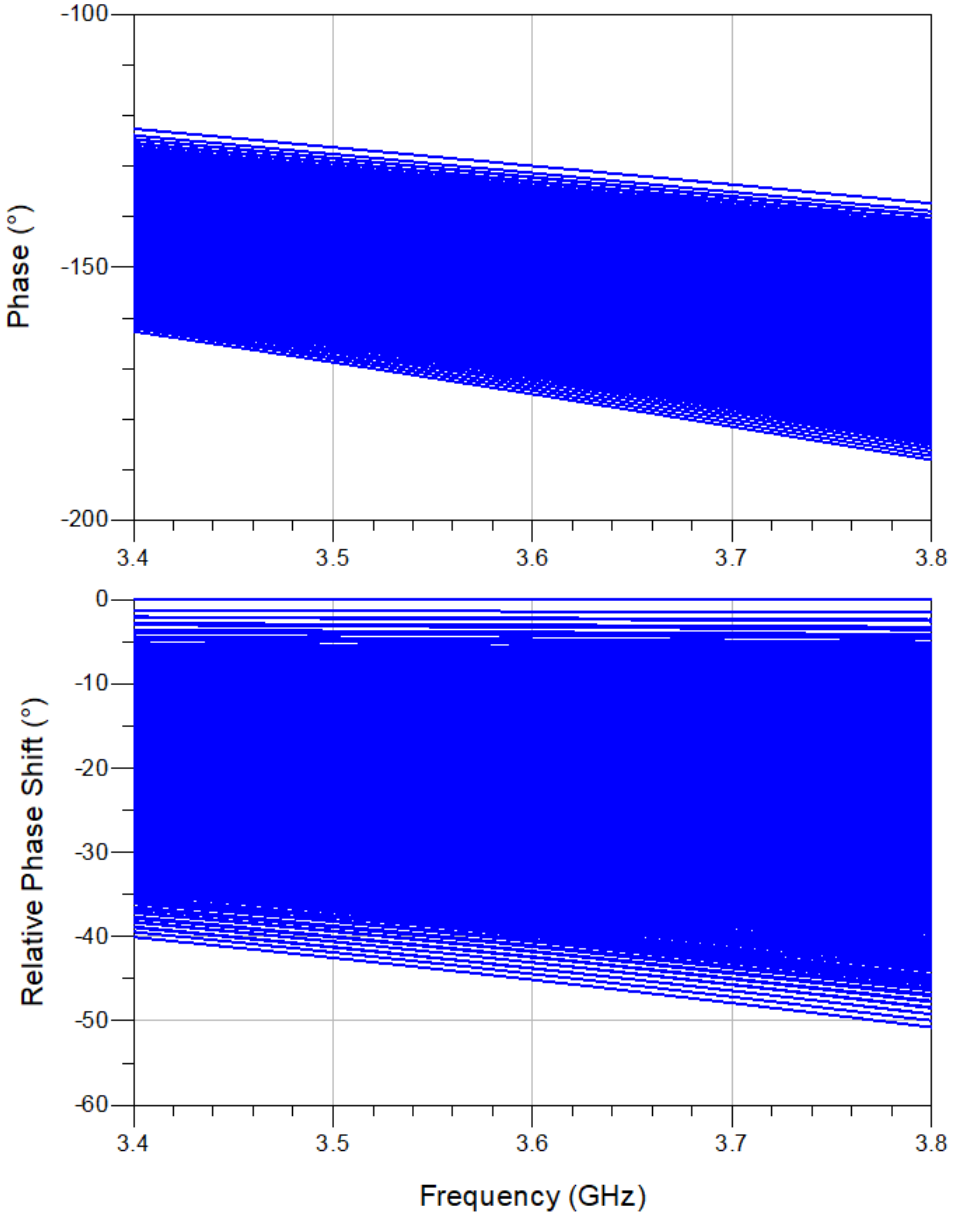

Figure 5.13: Circuit simulated RF phase of the 40° RF-MEMS phase shifter at 3.6 GHz, showing all possible configurations.

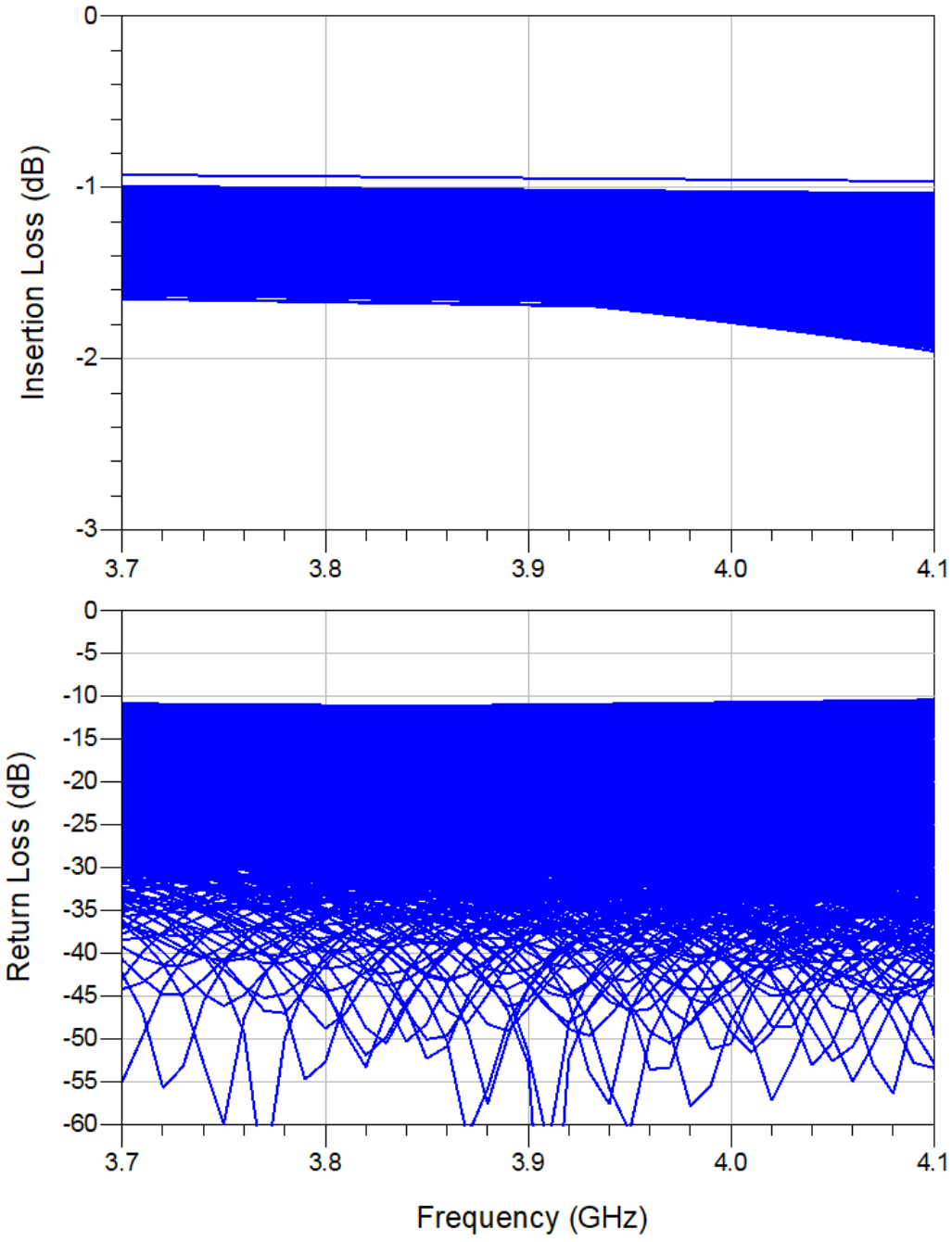

Figure 5.14: Circuit simulated RF performance of the 40° RF-MEMS phase shifter at 3.9 GHz, showing all possible configurations.

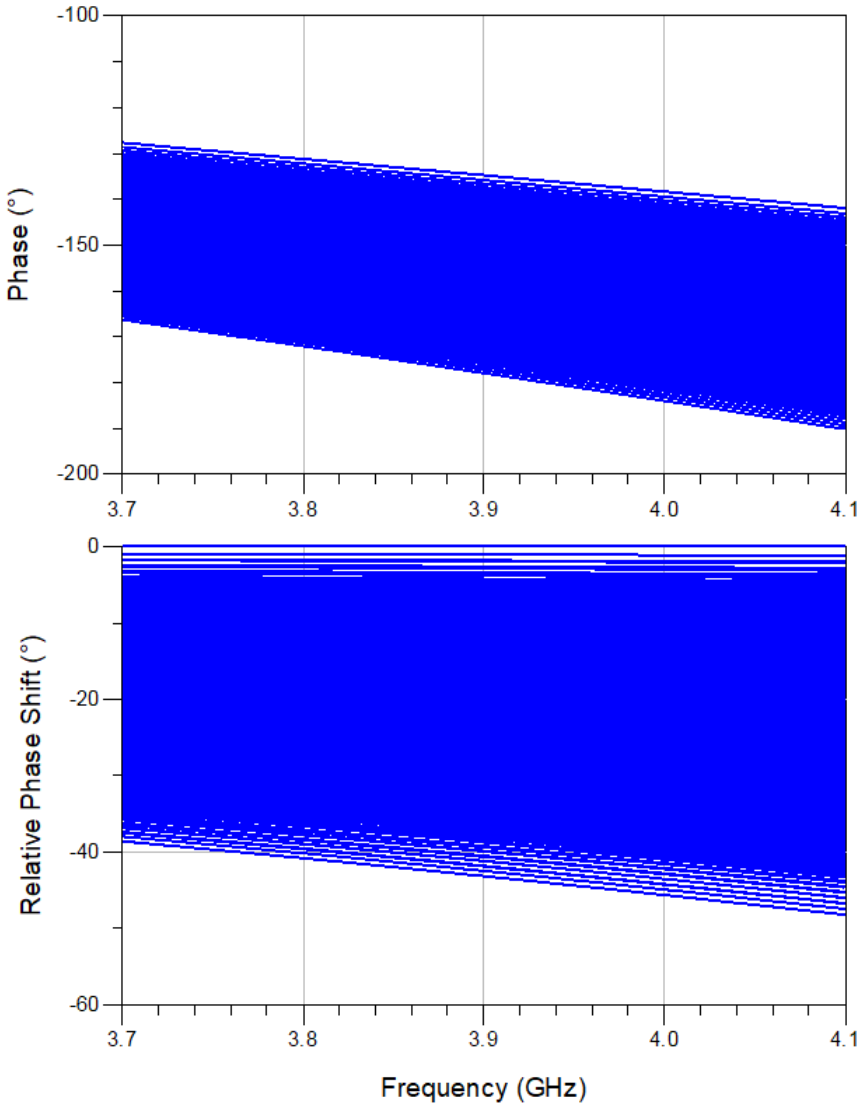

Figure 5.15: Circuit simulated RF phase of the 40° RF-MEMS phase shifter at 3.9 GHz, showing all possible configurations.

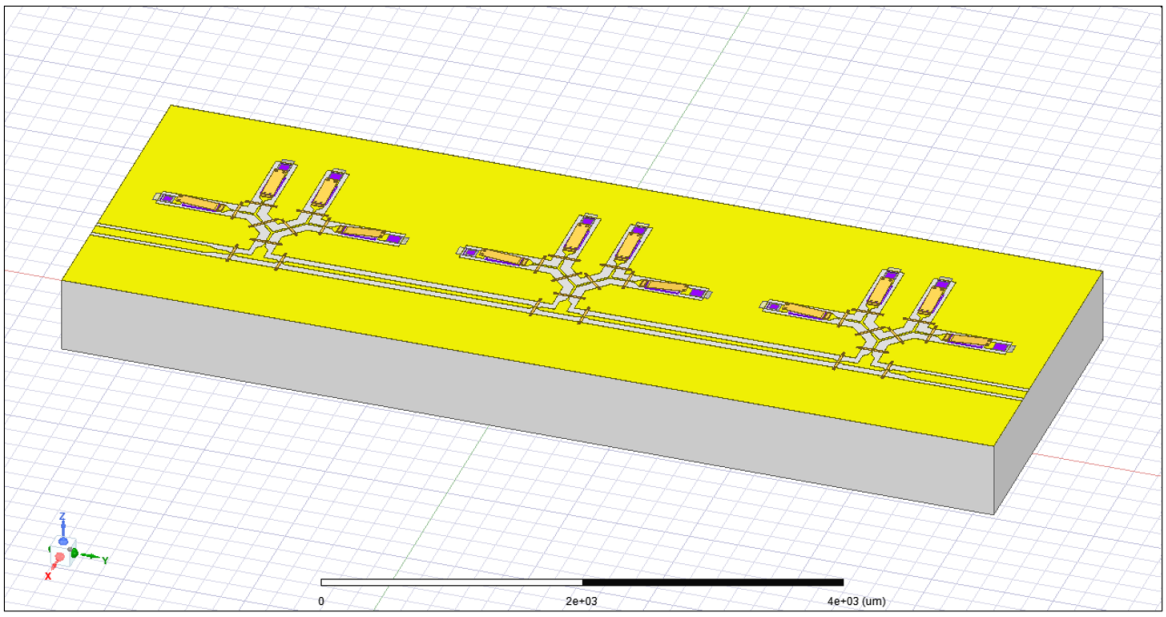

Figure 5.16: EM MIM based 40° phase shifter model.

shifter at 3.6 GHz. The simulation is run at different configurations, with all 3 bits switched to the same capacitor, from C0 to C4, changing the phase in increments of 10°Ṫhe performance and relative phase shift is nearly identical to that of the OC CPW stub loaded design. This is to be expected, as the only difference is the capacitor technology used to load the switched-capacitor banks. Therefore, Figures 5.12 and 5.13 can be used to show the circuit simulated RF performance and phase for all configurations of the MIM loaded 40° phase shifter at 3.6 GHz.

The MIM capacitor loaded 40° RF phase shifter devices centered at 3.6 GHz, 3.75 GHz, and 3.9 GHz were fabricated, released, and tested. The fabricated and released MIM capacitor loaded 40° phase shifter design can be seen in Figure 5.19. Unfortunately, due to the fabrication issues discussed in Chapter 3, the MIM capacitors (and by extension the MIM loaded phase shifters) did not operate as intended, and the yield of the devices was low.

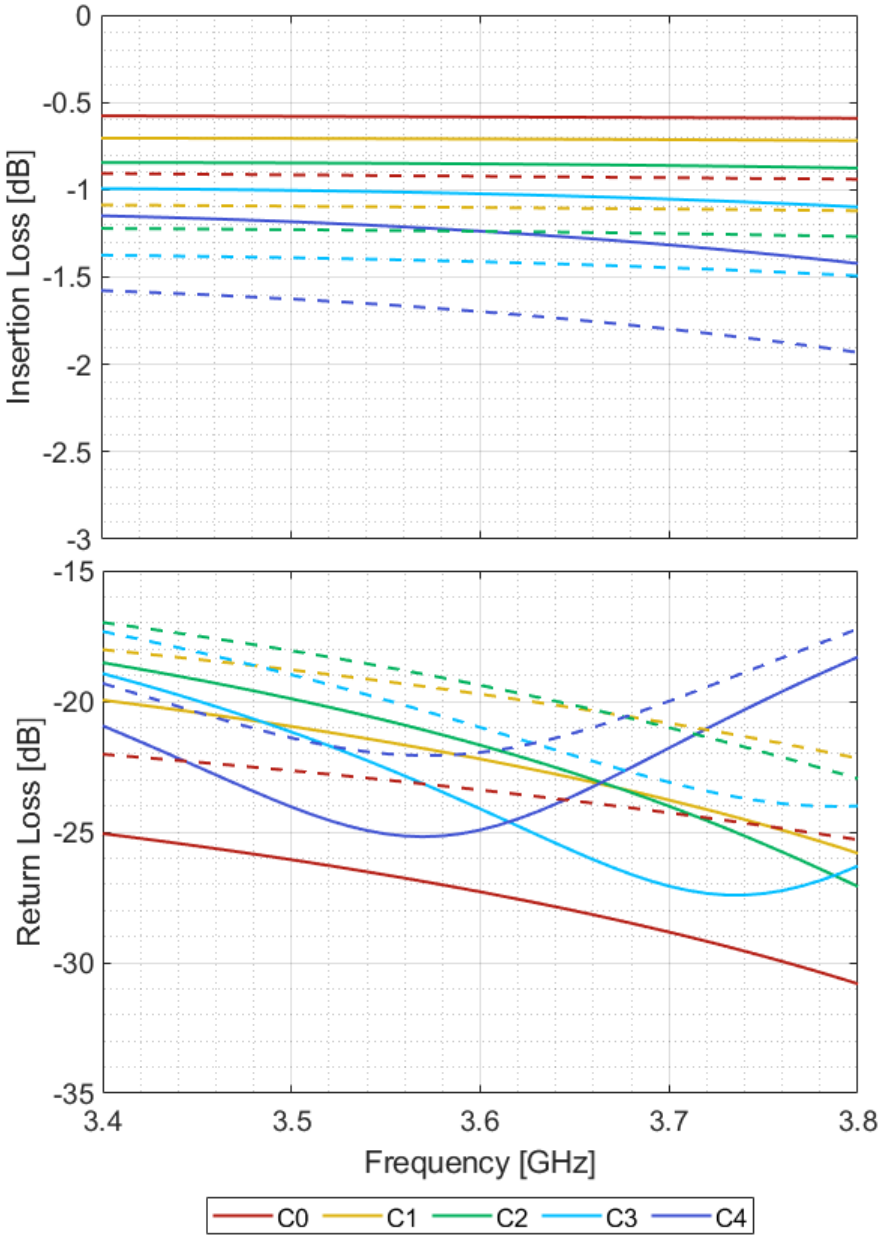

Figure 5.17: Simulated EM (line) and circuit (dash) RF performance of the 40° MIM loaded phase shifter at 3.6 GHz

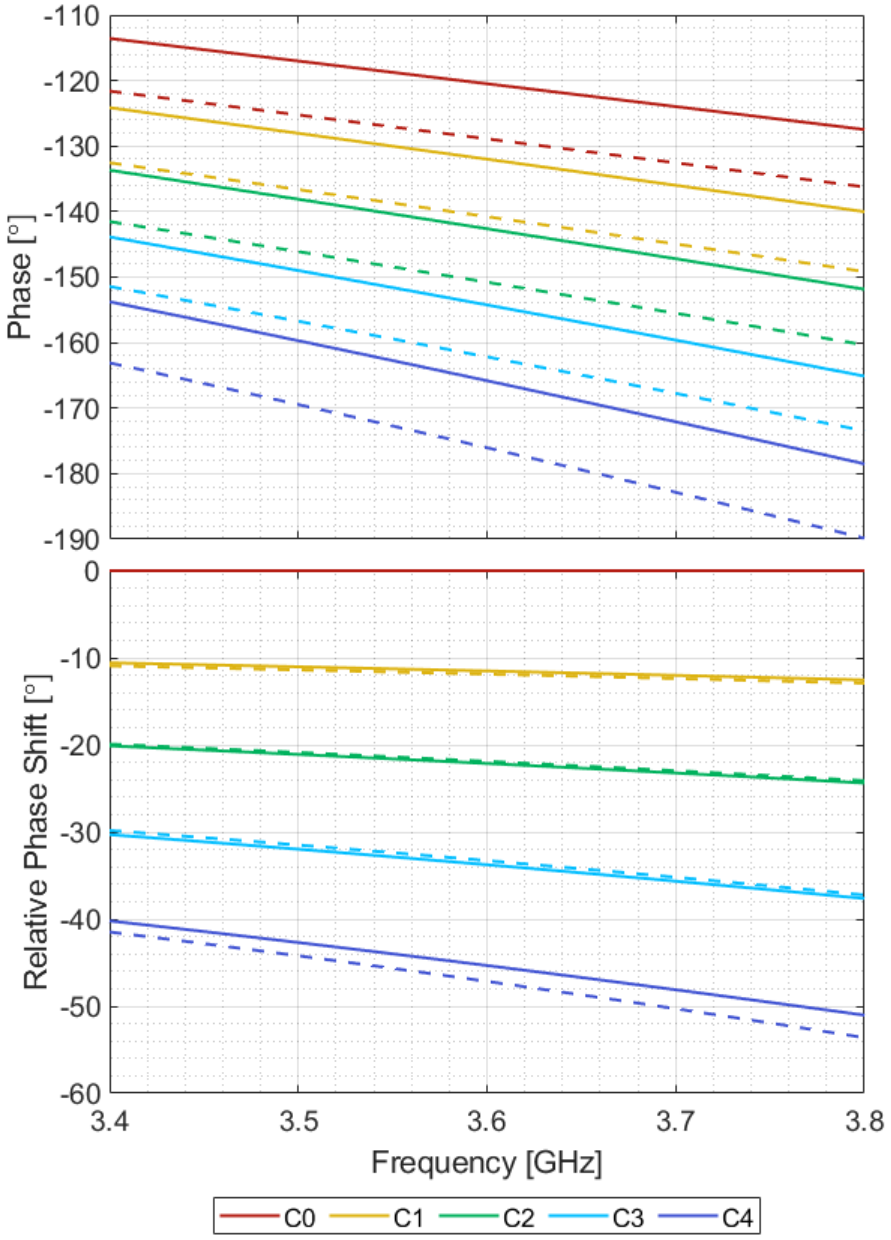

Figure 5.18: Simulated EM (line) and circuit (dash) phase of the 40° MIM loaded phase shifter at 3.6 GHz

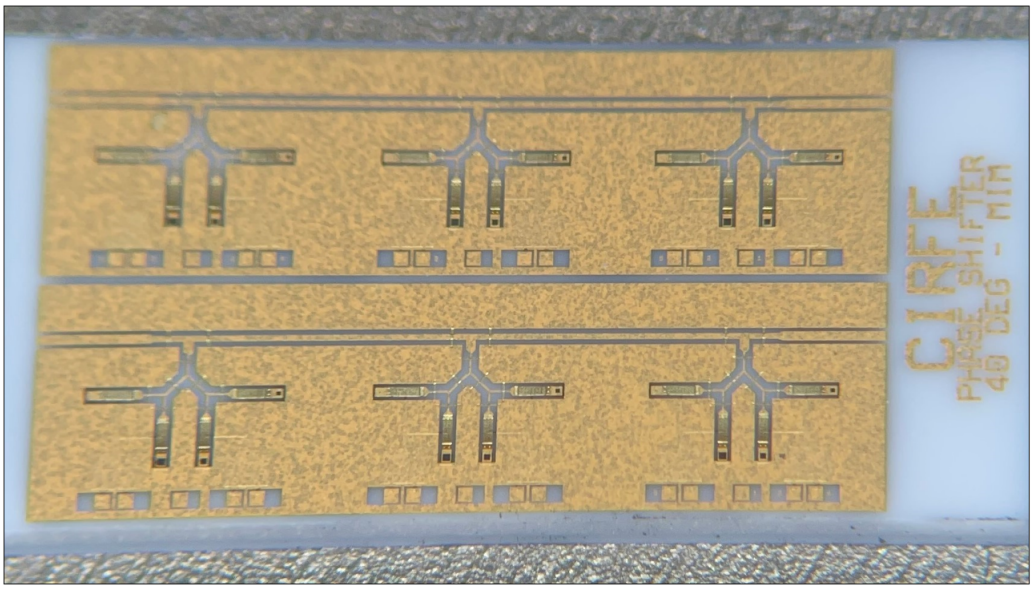

Figure 5.19: Microfabricated MIM capacitor loaded 40 degree RF-MEMS phase shifter.

5.3 Reconfigurable 360° RF-MEMS Phase Shifter Design

The previously presented reconfigurable 40° phase shifter designs were incorporated with two circuits making up a switched-line phase shifter, serving as a phase extension to increase the range to 360° of phase shift. The switched-line phase shifters consist of two digital phase shifters, one with a relative phase shift of 0° (reference), 40°, and 80°, and the other 0° (reference), 120°, 240°. Combining these options results in a switched-line phase shifter capable of phase shifts of 40° increments, from 0° to 320°. Combined with the reconfigurable 40° phase shifter, a range of 0° to 360° is achieved.

The schematic of the 360° RF-MEMS phase shifter can be seen in Figure 5.20. The switch uses both versions of the RF-MEMS SP3T switches designed in Chapter 4 to actuate

which path the RF signal travels down. An example of this can be seen in Figure 5.21, showing the different RF paths for the 360° phase shifter at 0° to 40° and at a relative phase shift of 320° to 360°.

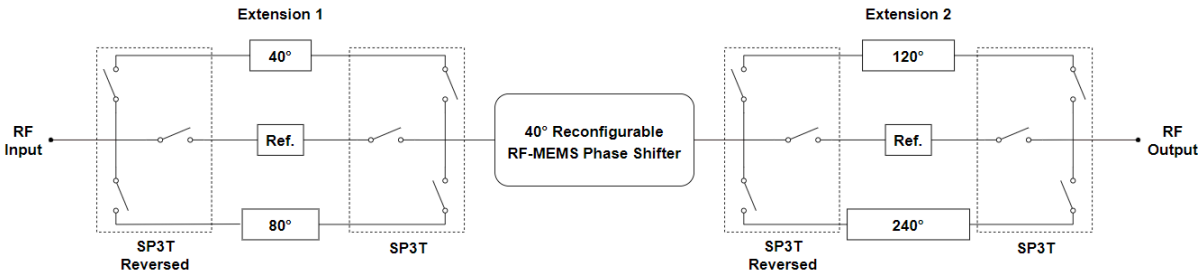

Figure 5.20: Circuit schematic for reconfigurable 360° RF-MEMS phase shifter.

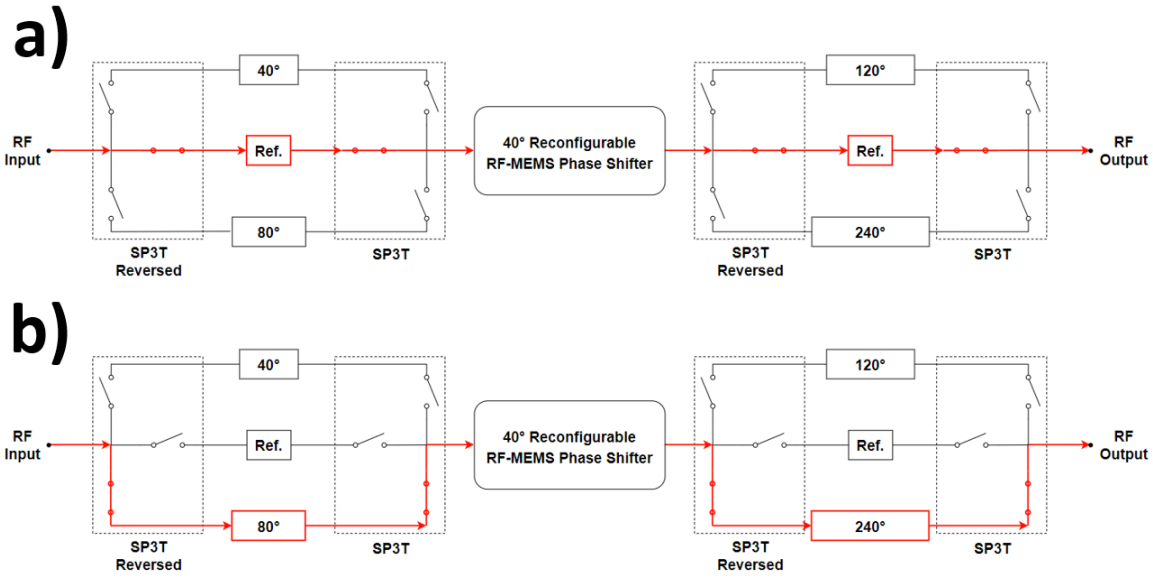

Figure 5.21: RF path for the reconfigurable 360° RF-MEMS phase shifter at a) 0-40°, b) 320-360°.

Switched Line RF-MEMS Phase Shifter

The switched-line RF-MEMS phase shifter circuits were designed at specific electrical lengths at a frequency of 3.6 GHz, so that the phase difference from the reference line would be 0°, 40°, or 80° for the first circuit, and 0°, 120°, or 240° for the second circuit. The two circuits are placed on both sides of the reconfigurable 40° RF-MEMS phase shifter. The design specifications for the switched-line phase shifter circuits can be seen in Table 5.3, including actual physicial length, and reference length and phase at 3.6 GHz.

Table 5.3: Switched-line phase shifter parameters at 3.6 GHz.

	CPW Path #	**CPW Length** (μm)	**Reference Length** (μm)	**Reference Phase** (°)
Circuit #1	**L1**	120	0	0
	L2	4120	4000	40
	L3	8120	8000	80
Circuit #2	**L1**	470	0	0
	L2	12470	12000	120
	L3	24470	24000	240

These circuits were then fabricated, released, and the RF performance and phase was measured. The microfabricated switched-line RF phase shifter circuits can be seen in Figure 5.22. Looking at the measured phase of the two switched-line RF-MEMS phase shifters centered at 3.6 GHz (Figure 5.23), the relative phase shift in comparison to the reference phase matches well with the desired phase shift. The amount of phase shift from the measured results is slightly larger than designed for, but this is likely due to the larger number of discontinuities (bends) in the CPW circuit for higher degree phase shift paths. This can be adjusted for in future designs.

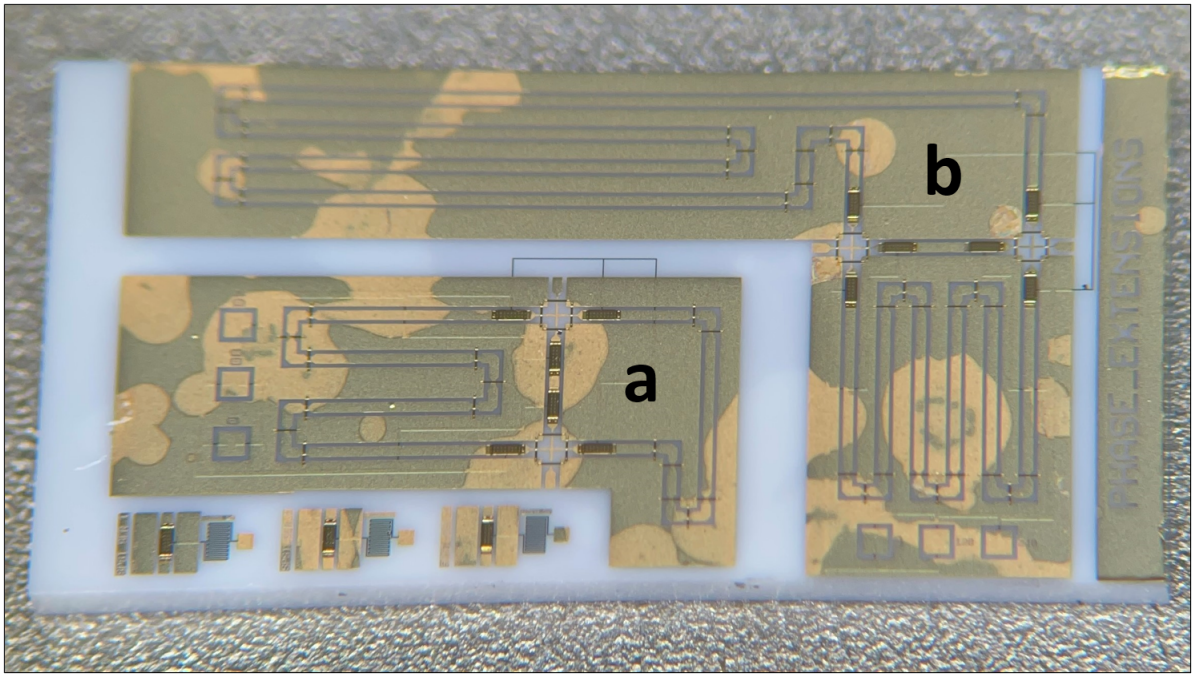

Figure 5.22: Microfabricated switched line phase shifters for (a) 0°, 40°, 80° and (b) 0°, 120°, 240° at 3.6 GHz.

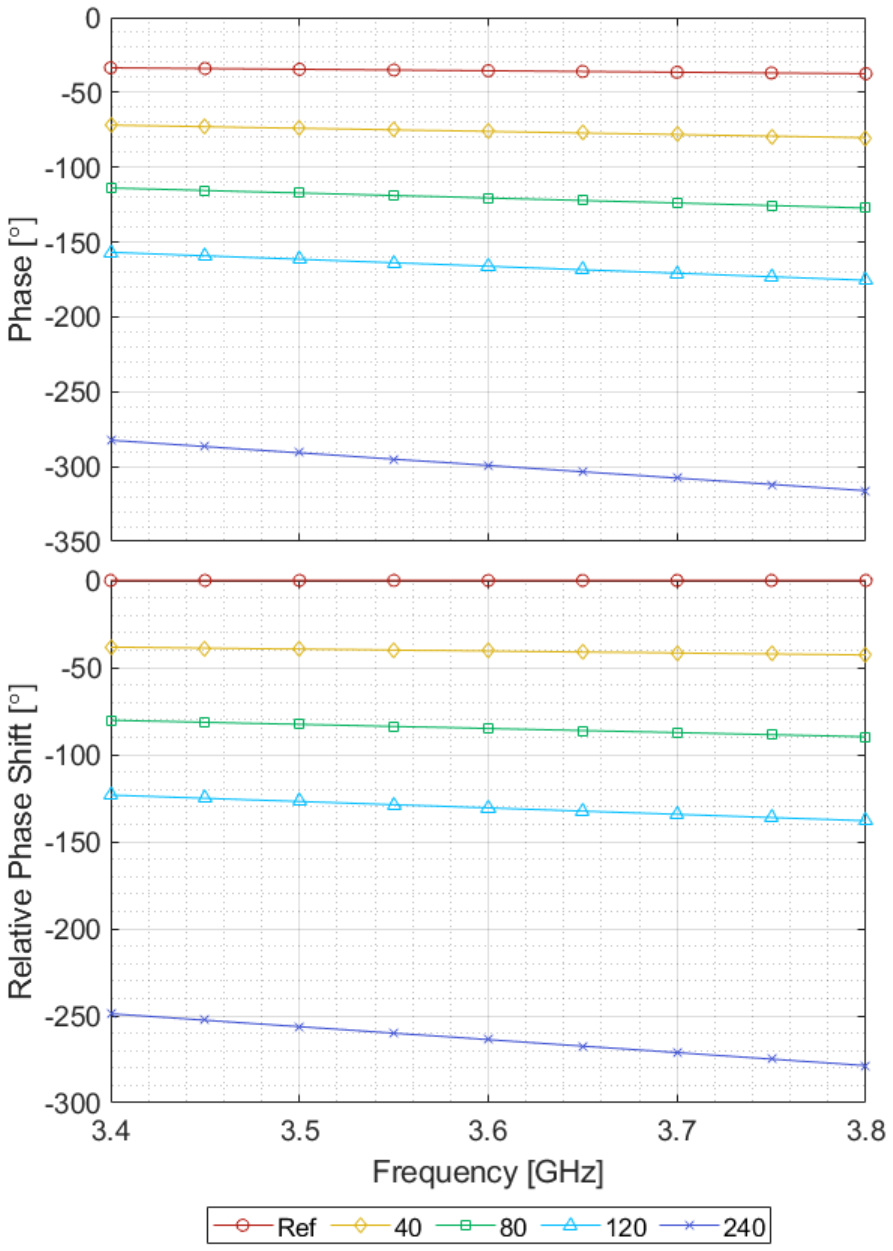

Figure 5.23: Measured phase of the two switched-line RF-MEMS phase shifters at 3.6 GHz.

Reconfigurable 360° RF-MEMS Phase Shifter

Combining the 3 bit reconfigurable 40° phase shifter with the 2 bit switched-line phase shifter results in a possible full range reconfigurability for phase shift. The total number of configurations possible with this design is 36864. Because of the small phase shift step size of the tunable 40° phase shifter used, and the large number of combinations, the step size of the reconfigurable 360° phase shifter is expected to also be very small.

Figure 5.24 presents the EM simulation models for the tunable 360° RF phase shifter, loaded using a) OC CPW stub capacitors and b) MIM capacitors. The lumped circuit simulation for these designs was run in a few states, and compared to the corresponding EM simulation results for the same states to verify the reliability of the circuit simulation results. A circuit simulation was then conducted for the 360° RF phase shifter at 3.6 GHz, with a phase shift step size of 10° for the phase shift, to limit the number of configurations and simulation load. The simulation results can be seen in Figure 5.25 and 5.26, plotting the simulated RF performance and phase respectively.

The simulated performance shows a reconfigurability range for the relative phase shift from 0° to 360° at 3.6 GHz. For the states simulated, the worst insertion loss did not exceed 3.5dB, and all the return loss was better than 16dB for all simulated configurations. It is likely that simulating all 36864 states will result in a number of states with much worse return loss performance. However, those states can be filtered out to fit the design requirements of the phase shifter.

The reconfigurable 360° RF phase shifters for 3.6 GHz, 3.75 GHz, and 3.9 GHz were fabricated and released. Figure 5.27 shows the released design loaded using OC CPW stubs, and Figure 5.28 shows the device loaded using MIM capacitors. Unfortunately, due to the large number of SPST RF-MEMS switches and the reliability issues with the

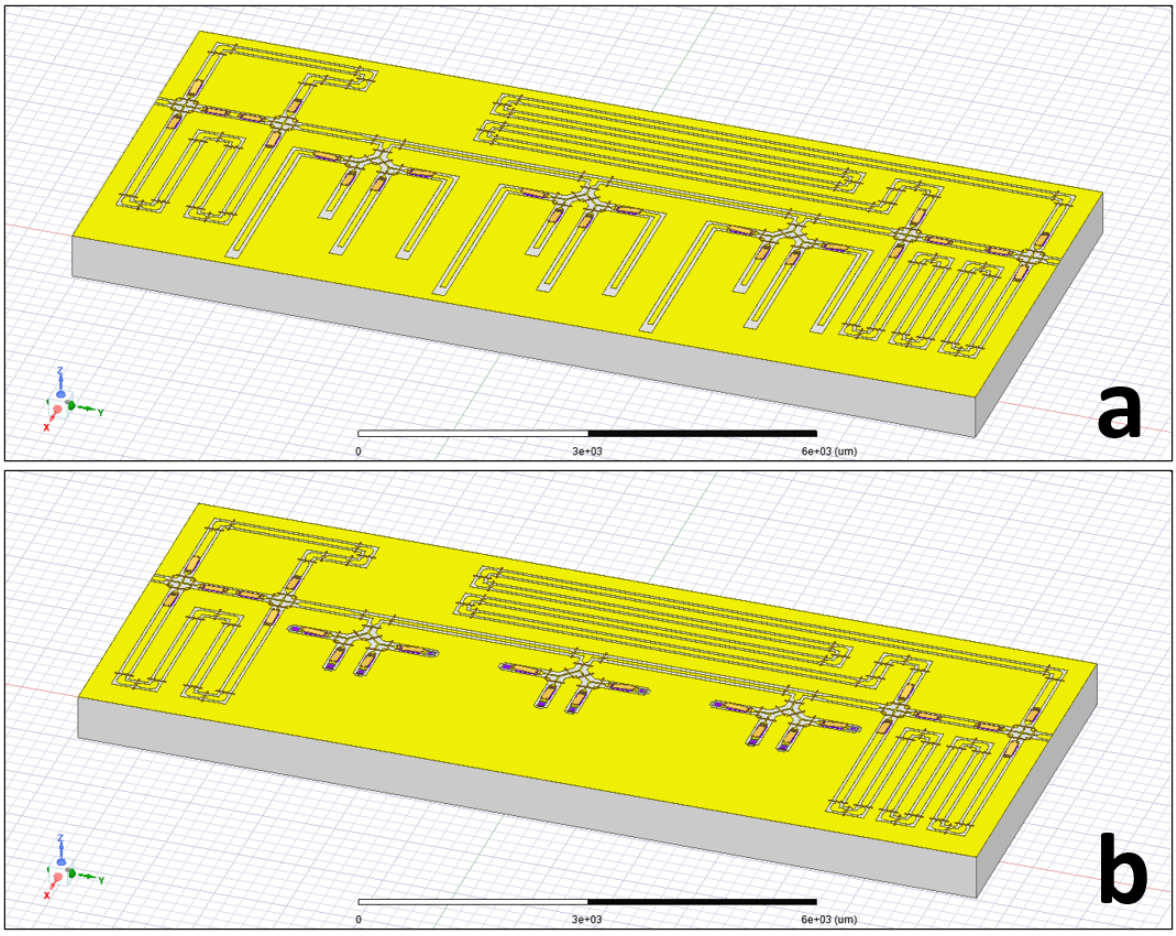

Figure 5.24: 360° Tunable RF phase shifter EM models, using a) OC CPW stub capacitors, and b) MIM capacitors.

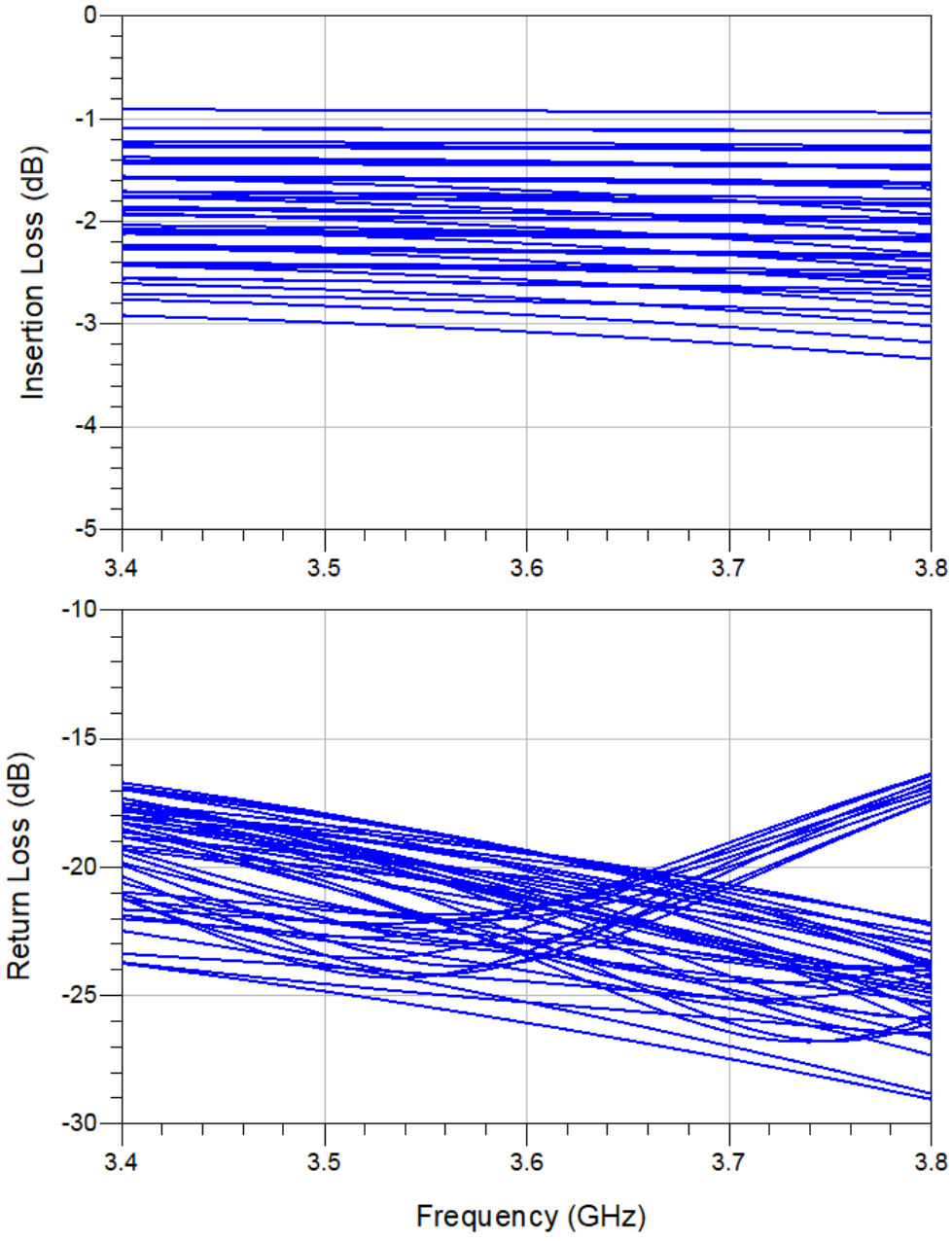

Figure 5.25: Circuit simulated RF performance of the 360° RF phase shifter at 3.6 GHz.

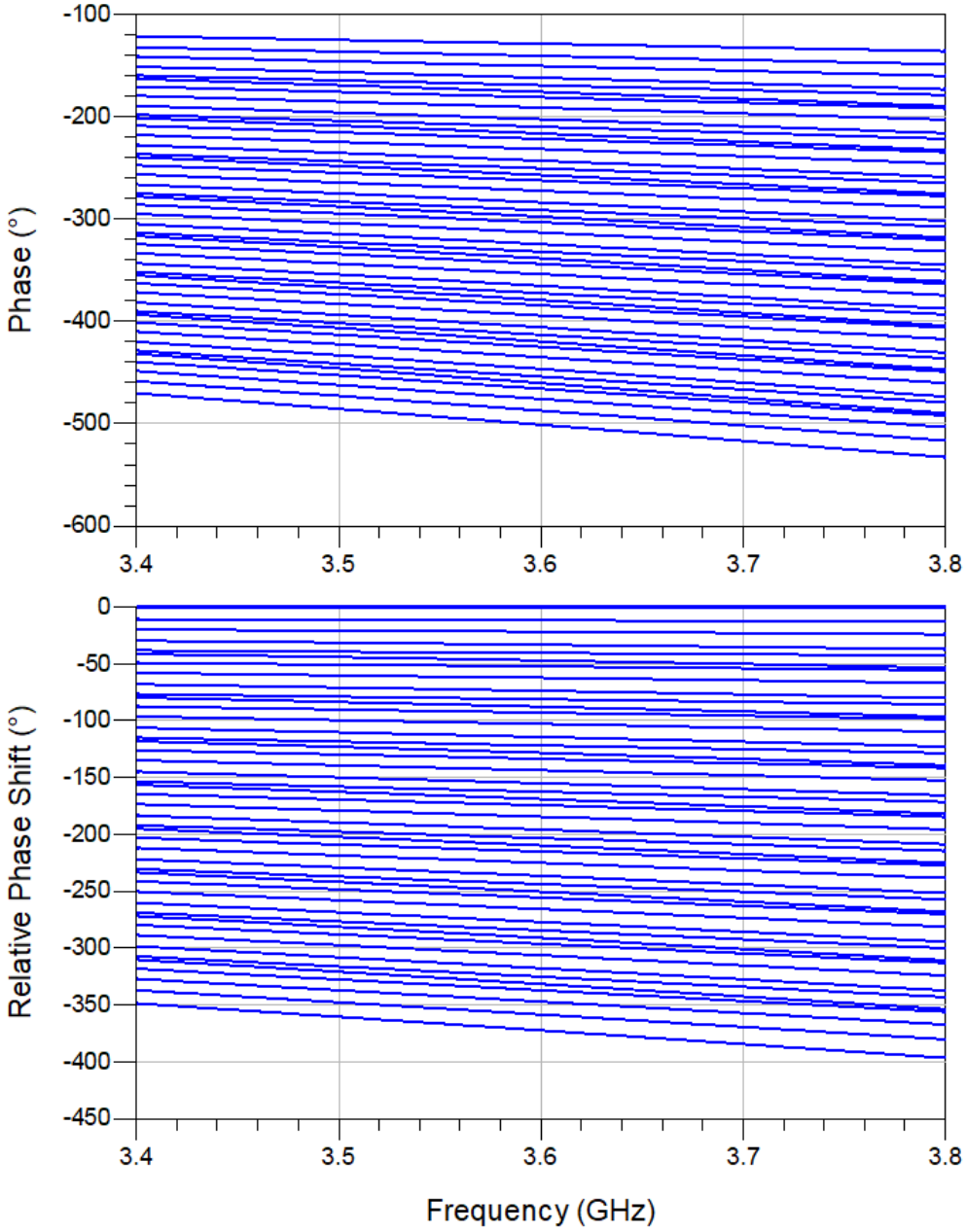

Figure 5.26: Circuit simulated RF phase of the 360° RF phase shifter at 3.6 GHz, at 10° intervals.

microfabrication process discussed in Chapter 3, some of the switches did not survive. Thus, the microfabrication process issues discussed in that chapter must be addressed and a new batch of phase shifters must be fabricated.

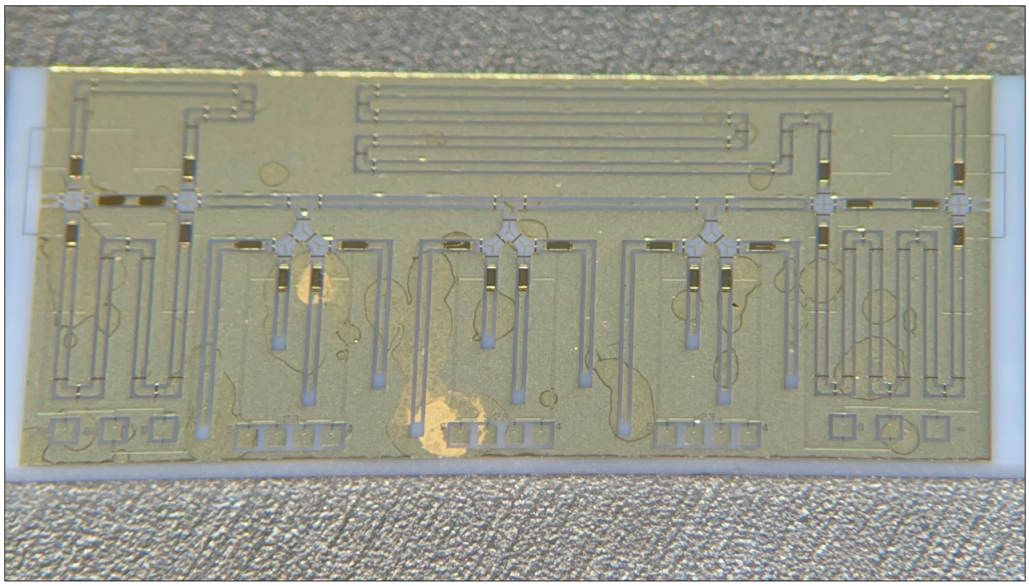

Figure 5.27: Microfabricated CPW capacitor loaded 360° RF-MEMS phase shifter.

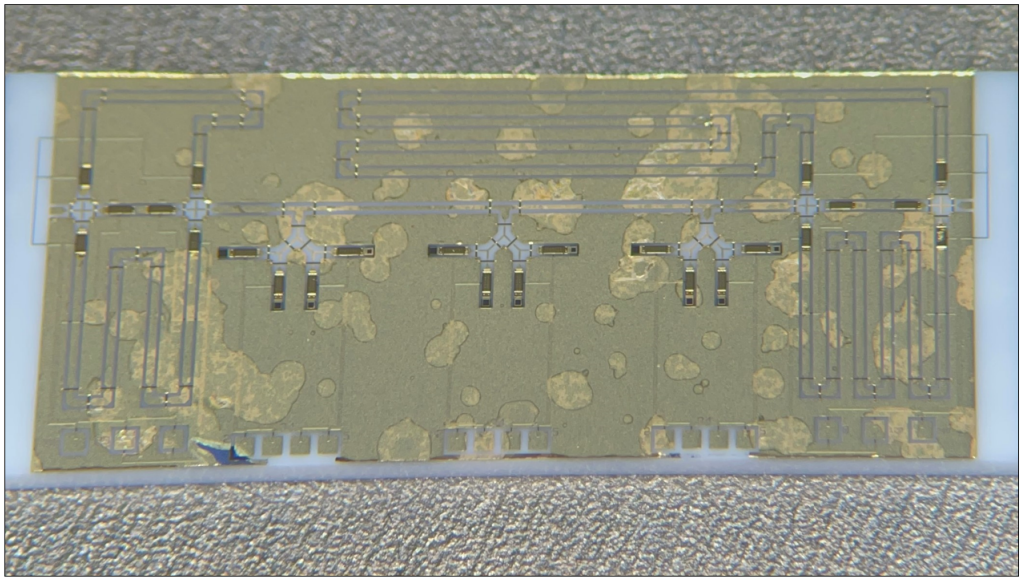

Figure 5.28: Microfabricated MIM capacitor loaded 360° RF-MEMS phase shifter.

Chapter 6

Conclusion

This thesis deals with the process of using RF-MEMS switches to develop a design for a monolithicly integrated 360° reconfigurable phase shifter at 3.6 GHz. The first part of this thesis goes over the microfabrication processes and testing methods of RF-MEMS devices. Chapter 4 focuses on the development of RF-MEMS components to be used as the foundation for the overall phase shifter design. Finally, chapter 5 presents the design of a 40° reconfigurable phase shifter, followed by a switched-line phase shifter spanning 0° to 320° to use as a phase extension to achieve a full range reconfigurable phase shifter at 3.6 GHz.

At each step, the thesis presents the initial design, EM simulation model, and compares the simulated performance to the working RF-MEMS devices to achieve an accurate model for the next step of the design. In this way, it ensures that the overall simulated model for more complex devices is reliable. Chapter 4 reports the design of an SPST switch that can operate up to 20 GHz demonstrating a good insertion and return loss performance, as well as two SP4T and two SP3T multiport RF switches that incorporate the SPST

in their design. Using the SP4T design, two variations of two switched-capacitor banks are developed, using MIM or CPW open stubs, both offering their own advantages and disadvantages. Chapter 5 makes use of the previous RF-MEMS devices presented in chapter 4 and employs them to design a reconfigurable phase shifter. The switched-capacitor banks were incorporated as the tunable element in a distributed MEMS transmission line design to achieve a phase shift up to 40° at 3.6 GHz. The SP3T switches were used to create switched line phase shifters in increments of 40° , from 0 to 320° . These two complex RF phase shifters were then integrated together into a reconfigurable 360° RF-MEMS phase shifter design, simulated, and fabricated. Due to the issues mentioned in chapter 3, the yield of the fabricated devices was poor, and the 360° phase shifter devices did not work. For future work, the fabrication process can be repeated with this in mind to have a better yield and test the fully fabricated devices.

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APPENDICES

Appendix A: Microfabrication Device Wafer Figures

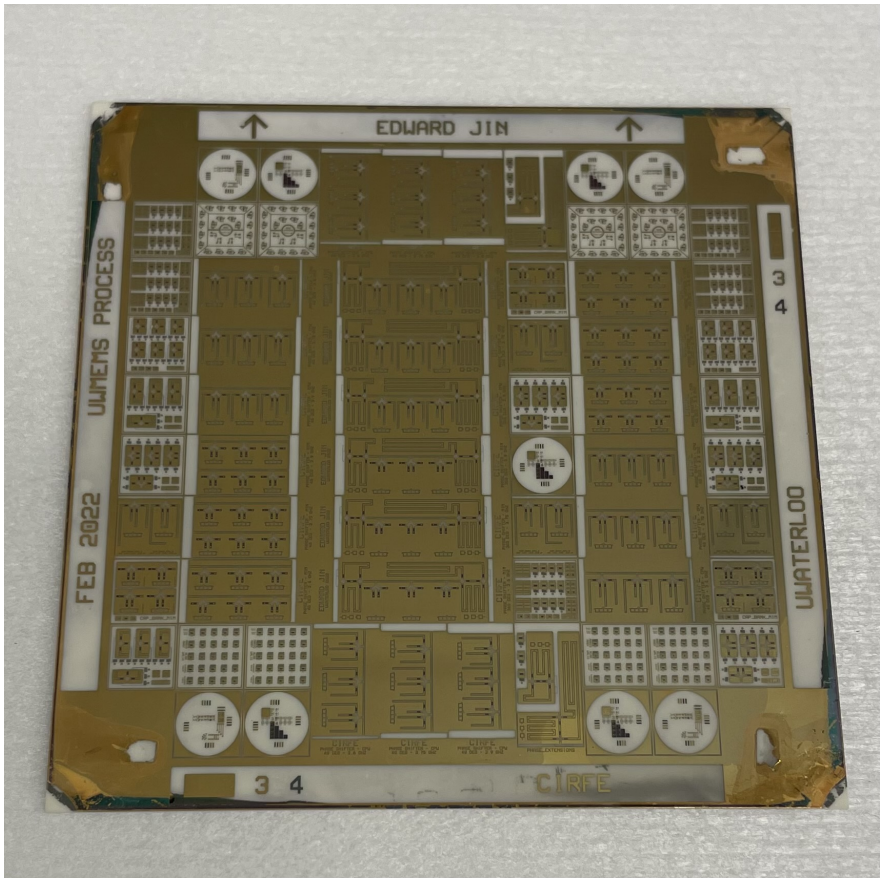

Figure A1: Device wafer after layer 3 Au and layer 4 SiO_2 patterning, before polyimide sacrificial layer deposition.

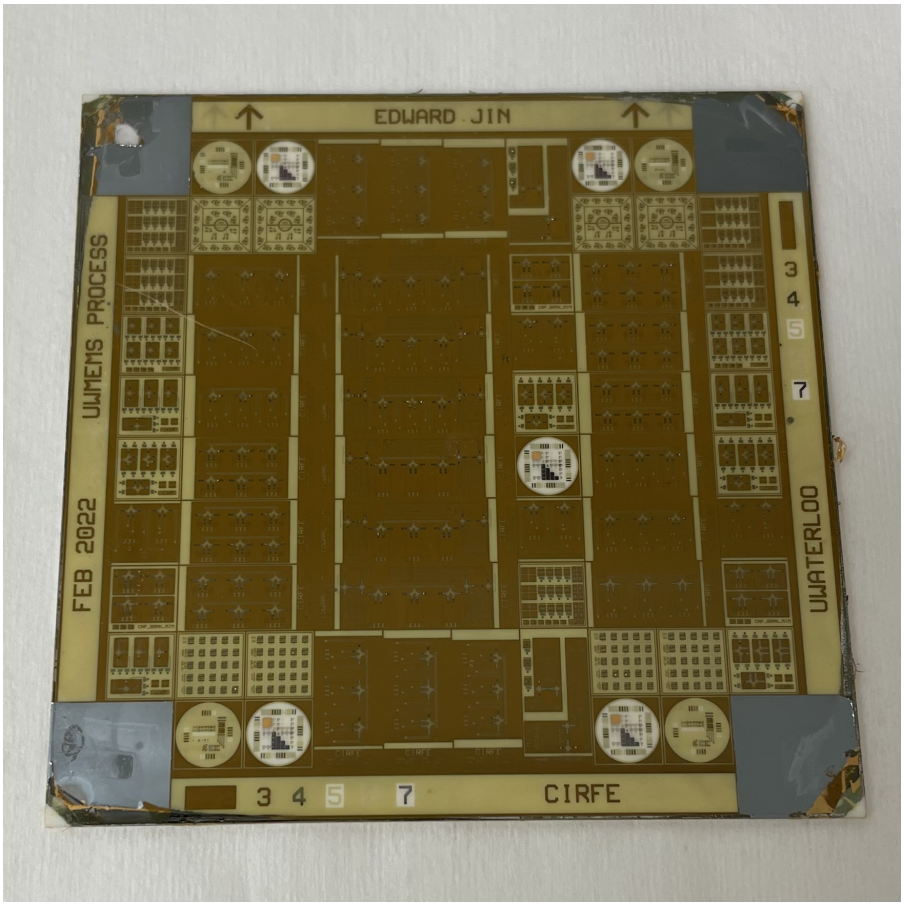

Figure A2: Device wafer right before release of sacrificial layer.

Appendix B: Microfabrication Test Structures

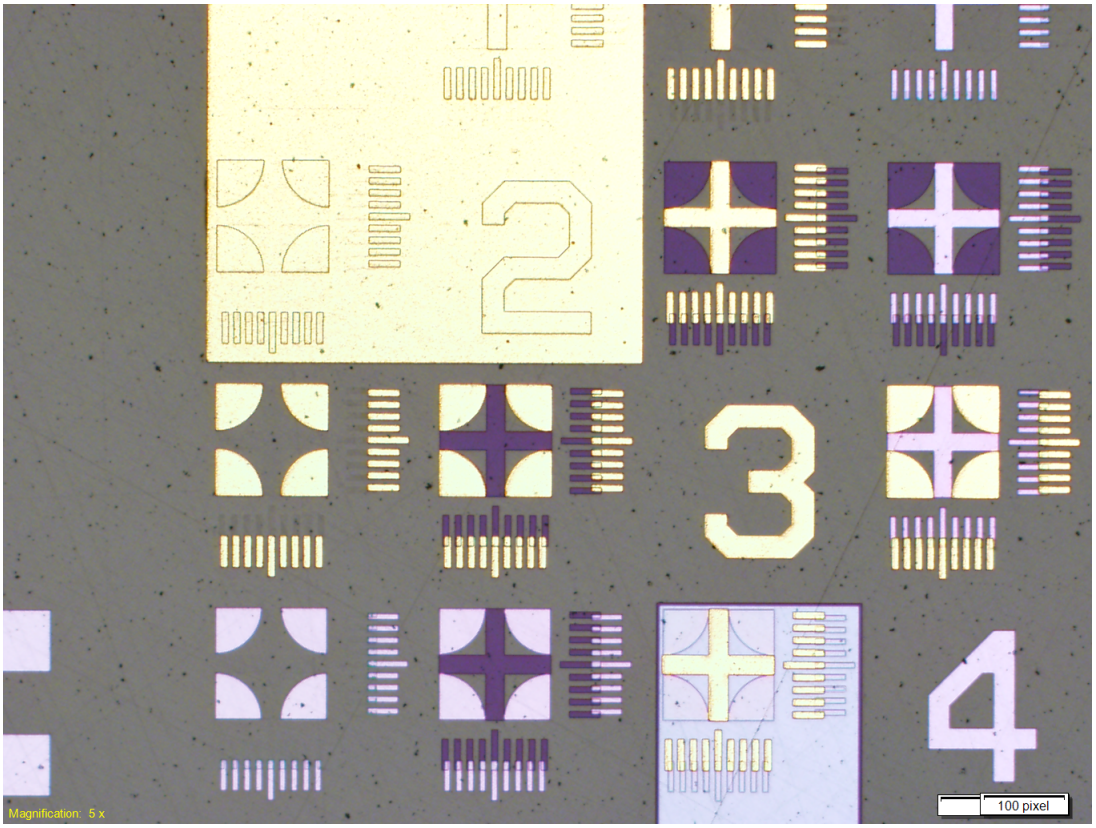

Figure B1: Test structures for alignment of layers 1 to 4.

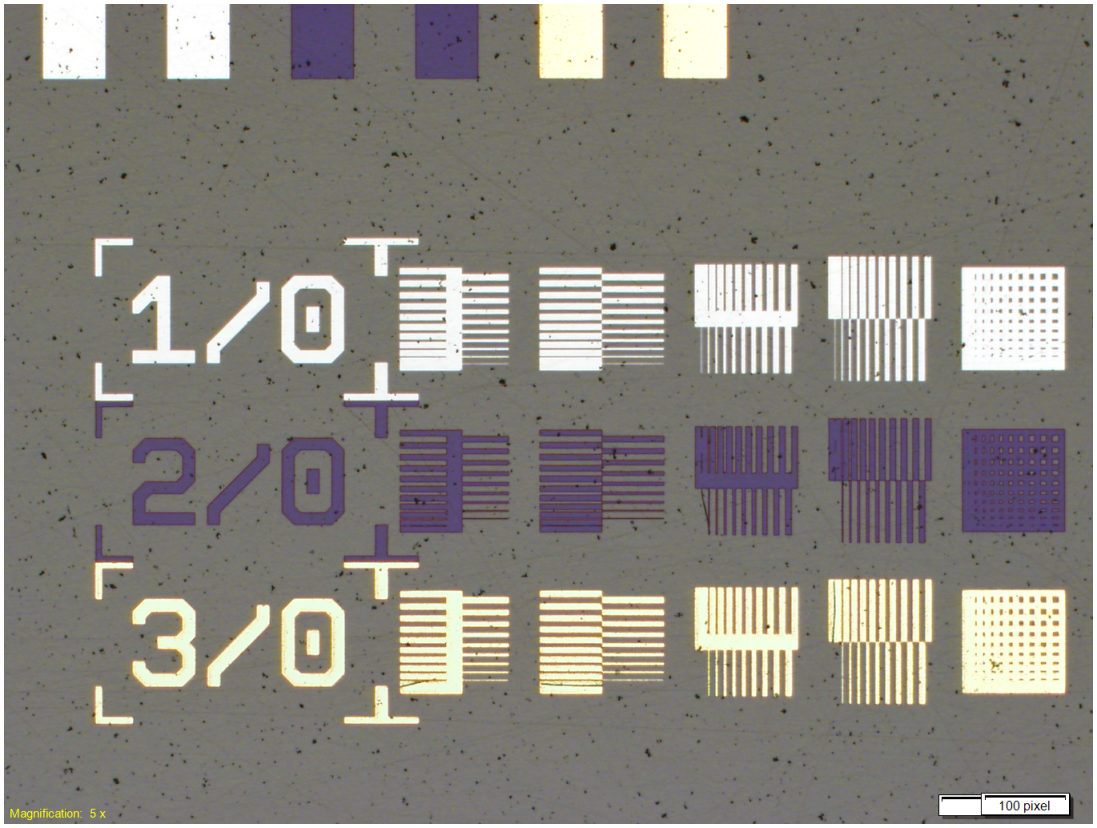

Figure B2: Test structures for feature size of layers 1 to 3 (1 to 10 μm).