Effect of Layer Transfer and Plasma Etching on The Behavior of Transition-Metal Dichalcogenide Field-Effect Transistor Arrays

by

Mohammad Nouri

A thesis

presented to the University of Waterloo

in fulfillment of the

thesis requirement for the degree of

Doctor of Philosophy

in

Electrical and Computer Engineering (Nanotechnology)

Waterloo, Ontario, Canada, 2023

© Mohammad Nouri 2023

Examining Committee Membership

The following served on the Examining Committee for this thesis. The decision of the Examining Committee is by majority vote.

External Examiner	Michael Adachi School of Engineering Science, Simon Fraser University
Supervisor	William S. Wong Dept. of Electrical & Computer Engineering
Internal Member	Chris Backhouse Dept. of Electrical & Computer Engineering
Internal Member	Youngki Yoon Dept. of Electrical & Computer Engineering
Internal-external Member	Yuning Li Dept. of Chemical Engineering

Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

The application of two-dimensional (2D) layered transition metal dichalcogenide (TMDC) for high-performance large-area memory applications requires establishing long-term electrical stability through an understanding of the carrier transport and the effect of the materials processing on the device behavior. In this Ph.D. dissertation, a novel two-step approach for creating arrays of thin-film and few-layer molybdenum disulfide (MoS_2)-based field-effect transistors is developed through mechanical exfoliation and a dry etching process. Few-layer structures (~ 3 monolayers) were fabricated using a dry etching process to thin multilayer (~ 60-90 nm thick) TMDC structures. Then, the effect of plasma etching of the TFT backchannel surface and bulk defects in the layers on the electrical performance and stability of the n-channel depletion-mode TFTs were investigated. The etching improved the threshold voltage of the TFTs, resulting in a positive threshold voltage shift of +40 Volts after etching the back channel, correlating to a bulk trap density of approximately 1×10^{16} $cm^{-3}eV^{-1}$ per monolayer. Etching the MoS_2 surface resulted in a threshold voltage shift of 0.2 V per nanometer of MoS_2 removed (for MoS_2 thicknesses >15nm). For etched MoS_2 layers reduced to < 15 nm, a threshold voltage change of ~1.8 V per nanometer was measured. The backchannel surface was also found to be doped and roughen due to the dry etching process but did not significantly affect the device performance until the MoS_2 thickness was below 15 nm. An observed degradation of the carrier transport and electrical stability of these samples were found to be due to the proximity of the etched surface approaching the active channel region of the device. The results reveal the performance tradeoffs of fabricating large-area arrays of few-layer TMDC TFTs using a mechanical exfoliation and dry etching approach.

Hydrogen-contained passivation layers were then used to mitigate the impact of the surface defects on the TFT's electrical performance. It is discovered that the diffusion of the hydrogen into the active region of the TMDC devices after the passivation process causes n-type doping, leading to a degradation in the electrical performance and stability of the devices and a negative threshold voltage shift. Furthermore, it is shown that hydrogen diffusion has a higher impact on the electrical performance of TMDC devices with thicknesses less than 15 nm due to the hydrogen diffusion length. Therefore, a hydrogen barrier layer was used to reduce the adverse effect of hydrogen-containing backchannel passivation layers and processes. This approach might be used to make hydrogen-contained passivation layers more compatible with the TMDC semiconductors for developing the next generation of TMDC-based memory devices.

Finally, dual-gate TMDC-based TFT arrays were fabricated using a bilayer dielectric on pristine and backchannel etched TMDC films. The electrical characterization shows that the dual-gate TFTs suffered due to trap states on the backchannel surface of the etched TMDC-based TFTs. The research also revealed that the effectiveness of the top-gate electric field in regulating the electrical performance and stability of dual-gate TFTs is affected by both the presence of backchannel surface traps and the distance between the top gate and the active channel region. The findings of this study demonstrate that using a dual-gate structure is a feasible method for managing and adjusting the electrical performance and stability of TMDC-based TFTs affected by backchannel surface states.

Acknowledgments

I am deeply grateful to everyone who has contributed to my journey throughout my Ph.D. dissertation. This accomplishment would not have been possible without their support, encouragement, and guidance.

First and foremost, I extend my heartfelt thanks to my supervisor, Professor William Wong, for his invaluable advice, mentorship, and unwavering support throughout my research. His knowledge, expertise, and dedication have been a constant source of inspiration and motivation.

I would like to express my sincere gratitude to my advisory committee, Professor Christopher James Backhouse, Professor Youngki Yoon, and Professor Yuning Li, for their insightful feedback, constructive criticism, and guidance throughout my research. Their expertise and encouragement helped me navigate through the challenges I encountered. I would also like to thank Professor Michael Adachi for accepting the role of my external Ph.D. examiner.

I also extend my gratitude to the lab managers, Richard Barber and Dr. Czang-Ho Lee, for their technical support and expertise that made my experiments possible.

I am grateful to my colleagues: Dr. Mozhgan Sadeghianlemraski. Dr. Celal Con, Dr. Mohsen Asad, Dr. Won-tae Park, Dr. Ali Tari, Hyunwoo Choi, and Pranav Gavirneni for their support, stimulating discussions, and collaboration. Their encouragement and insights have been a significant source of motivation for me.

I would like to thank my parents for their unwavering support and encouragement throughout my academic journey. Their love and support have been a constant source of strength for me.

Last but not least, I would like to express my deepest appreciation to my wife, Mozhgan. Her unwavering love, emotional, and financial support throughout my academic journey have been immeasurable. Her encouragement, sacrifices, and belief in me have been my constant source of strength, especially during challenging times.

I am deeply thankful to everyone who has played a part in my academic journey, and I am honored to have had their support and guidance along the way.

This work was performed at the Giga-to-Nanoelectronics (G2N) Centre at the University of Waterloo. The author acknowledges support from the Natural Sciences and Engineering Research Council Strategic Partnership Grant.

Dedication

I dedicated this thesis to my love Mozhgan.

Table of Contents

Examining Committee Membership ii

Author's Declaration iii

Abstract iv

Acknowledgments vi

Dedication viii

List of Figures xiii

List of Tables xvi

List of Abbreviations xvii

Chapter 1 Introduction 1

1.1 Introduction 1

1.2 Two-dimensional materials 2

1.3 Transition metal dichalcogenides 3

1.4 MoS_2 properties 5

1.5 Thin-film transistors 7

1.5.1 Materials for thin-film transistors 9

1.5.2 Trap states in 2D semiconductors 9

1.5.3 The electronic properties of TMDC-based thin film transistors 12

1.5.4 Current-Voltage Relations of a TFT 13

1.5.5 Threshold voltage 15

1.5.6 Subthreshold swing 17

1.5.7 Field effect Mobility 18

1.5.8 State-of-art TMDC Field effect transistors 19

Chapter 2 Challenges of developing TMDC-based devices 22

2.1 Introduction 22
2.2 TMDC synthesis 22
2.2.1 Bottom-up method 22
2.2.2 Top-down method 24
2.3 TMDC thinning process 25
2.4 TMDC/dielectric interface traps 26
2.5 TMDC bulk traps 27
2.6 Backchannel surface traps 28
2.6.1 Backchannel surface passivation 29
2.6.2 Dual gate structure 31
2.7 Organization of dissertation 31
Chapter 3 The fabrication process of TMDC-based TFT arrays using the dissolving tape method and dry etching process 33
3.1 Introduction 33
3.2 Large–area TMDC exfoliation 33
3.3 MoS_2 device array fabrication 37
3.4 Dry etching process 38
3.5 Conclusion 41
Chapter 4 Effect of large-area exfoliation and etching on the electrical behavior of transition-metal dichalcogenide field-effect transistor arrays 42
4.1 Introduction 42
4.2 Experimental 42
4.3 Results and Discussion 43
4.3.1 TFT configurations 43

4.3.2 MoS_2 bulk thickness effect 44

4.4 Conclusion 54

Chapter 5 Effect of hydrogen-containing passivation layers on the electrical performance of transition-metal dichalcogenide field-effect transistors 55

5.1 Introduction 55

5.2 Experimental 56

5.2.1 Backchannel passivation process 56

5.2.2 Chemical Analysis and Electrical Characterization 57

5.3 Results and Discussion 57

5.4 Conclusion 65

Chapter 6 Effect of backchannel surface traps on dual gating of dry-etched multilayer transition metal dichalcogenides TFTs 66

6.1 Introduction 66

6.2 Experimental 66

6.2.1 The top-gate TFT fabrication process 66

6.2.2 Electrical characterization 67

6.3 Results and Discussion 68

6.4 Conclusion 77

Chapter 7 78

7.1 Conclusions 78

7.2 Suggestions for Future Work: 79

7.3 Publications and conferences 80

References 82

Appendix A Supplementary Information for Chapter 4 90

Appendix B Supplementary Information for Chapter 5 94

Appendix C Supplementary Information for Chapter 6 98

List of Figures

Figure 1.2-1: contemporary 2D monolayers' physical structures. Reproduced with permission from [11]. Copyright © 2014, Nature Publishing Group. 3

Figure 1.4-1: Schematics of structural polytypes of MoS_2. Reproduced with permission from [17]. Copyright © 2012, Nature Publishing Group. 6

Figure 1.4-2: (a) Vibration Modes and (b) Raman Spectra of 2H-MoS_2 with a different number of layers. Reproduced with permission from [17]. Copyright © 2012, Nature Publishing Group. 7

Figure 1.5-1: (a) Schematic of a MoS_2 TFT, (b) TFT in OFF state, (c) TFT in ON state. 8

Figure 1.5-2: Band diagram of an n-type TFT under different conditions of gate voltage (a) No gate bias, (b) Negative gate bias, (c) Positive gate bias. 13

Figure 1.5-3: (a) Carrier concentration profile of TFT in the linear regime. (b) Pinch-off (c) saturation regime. 14

Figure 2.2-1: (a) Optical micrograph of CVD growth MoS_2 on SiO_2 substrate and (b) single layer MoS_2 triangle with a 123 μm grain size. Reproduced with permission from [57]. Copyright © 2013, Nature Publishing Group. 23

Figure 2.2-2: (a) parent MoS_2 bulk material. (b) transferred MoS_2 films on SiO_2 substrate using mechanical exfoliation. 24

Figure 3.2-1. Modified mechanical exfoliation procedure. 34

Figure 3.2-2: Optical micrograph of exfoliated MoS_2 flakes on a SiO_2 substrate, transferred by the modified method using a dissolvable adhesive. The inset shows the transferred MoS_2 flakes by the conventional method. 35

Figure 3.2-3: The AFM images of transferred MoS_2 flakes on a SiO_2 substrate using (a) conventional exfoliation and (b) modified exfoliation method. 36

Figure 3.2-4: Raman spectroscopy of MoS_2 films with different thicknesses. 37

Figure 3.3-1: Optical micrograph of the MoS_2 TFT array with a resulting channel width of 40 μm and a channel length of 20 μm for each TFT. (b) Schematic of bottom-gate MoS_2 TFTs. 38

Figure 3.4-1: Atomic force microscopy images of (a) As-transferred MoS_2 film. (b) to (g) are AFM images after dry etching for 8 s, 16 s, 24 s, 26s, 28s, and 32 s, respectively. The thickness and root mean square (rms) of the MoS_2 film at each step are added under each image. 40

Figure 3.4-2: Thickness variations of multiple MoS_2 at different plasma exposure duration. 40

Figure 4.3-1: Cross-sectional schematic of MoS_2 TFT with deposited drain and source (a) after and (b) before the plasma etching process. (c) Drain current vs. gate voltage characteristics for the TFTs. 44
Figure 4.3-2: Drain current vs. gate voltage characteristics for a typical transferred and as-fabricated TFT with a MoS_2 bulk thickness = 90 nm. The inset shows the output characteristics of the MoS_2 TFT. 45
Figure 4.3-3: The electrical characteristics of MoS_2 TFTs are plotted for different t_s. (a) the threshold voltage of MoS_2 TFTs as a function of semiconductor thickness, (b) TFT ON and OFF current variations vs. t_s, the blue square symbols show the ON/OFF-current ratio variations, (c) the subthreshold swing vs. t_s, and (d) the field-effect mobility vs. t_s. 47
Figure 4.3-4: (a) XPS surface analysis of a dry etched MoS_2 film. The inset shows the XPS results of the layer of the unexposed surface. (b) and (c) show the energy band diagram and cross-section schematics of dry-etched MoS_2 TFT with thicknesses above and below 15 nm, respectively. 51
Figure 5.2-1: Schematic of bottom-gate MoS_2 TFTs with a passivation layer. 56
Figure 5.3-1: The electrical characteristics of MoS_2 TFTs in bare condition (black curve), after passivation with 100 nm SiN_x (red curve), after exposure to H_2 plasma (green curve), and after passivation with SiN_x/SiO_x bilayer dielectric (blue curve) are plotted for different t_s. (a) the threshold voltage of MoS_2 TFTs as a function of semiconductor thickness, (b) TFT ON/OFF-current ratio variations vs. t_s, (c) the subthreshold swing vs. t_s, and (d) the field-effect mobility vs. t_s. 59
Figure 5.3-2: Secondary ion mass spectroscopy results of a MoS_2 film, (normalized to the hydrogen signal intensity), after exposing to H_2 plasma (olive curve), after passivating with 100 nm SiN_x (red curve), after passivating with bilayer $SiNx/SiO_x$ (blue curve), and at bare condition (black curve). TOF-SIMS data are normalized to the total ion counts. 63
Figure 6.2-1: (a) cross-sectional schematic and (b) optical micrograph of dual-gate MoS_2 TFTs. 67
Figure 6.3-1: The electrical characteristics of the bottom gate (blue curves), top gate (red curves), and top gate pristine (green stars) MoS_2 TFTs are plotted for different t_s. (a) the threshold voltage of MoS_2 TFTs as a function of semiconductor thickness, (b) TFT ON/OFF-current ratio variations vs. t_s, (c) the subthreshold swing vs. t_s, and (d) the field-effect mobility vs. t_s. 70
Figure 6.3-2: The electrical characteristics of the bottom gate backchannel etched (lines) and pristine (stars) MoS_2 TFTs with different top gate biases are plotted for different t_s. (a) the threshold voltage

of MoS_2 TFTs as a function of semiconductor thickness, (b) TFT ON/OFF-current ratio variations vs. t_s, (c) the subthreshold swing vs. t_s, and (d) the field-effect mobility vs. t_s. 74
Figure 6.3-3: Energy band diagram of dual gate TFTs with (a) pristine, (b) etched, and (c) thick MoS_2 channels. 76

Figure S 1: Absolute parameter values of MoS_2 TFTs at different MoS_2 bulk thicknesses. The threshold voltage, the I_{on}/I_{off} ratio, the field-effect mobility, and the subthreshold swing as a function of the MoS_2 bulk thickness are plotted in (a) – (d), respectively. Each symbol represented an individual TFT, and dashed lines connect their parameter variations with the MoS_2 bulk thickness. . 91
Figure S 2: Electrical stability measurement of a TFT with different MoS_2 bulk thicknesses............ 91
Figure S 3: Off-current variations of MoS_2 TFTs after passivation at different t_s. 94
Figure S 4:The electrical characteristics of bare MoS_2 TFT (black curve), after passivation with 50 nm PECVD SiO_x (green curve), and after passivation with 50 nm E-beam SiO_x (blue curve) are plotted for different t_s. (a) the threshold voltage of MoS_2 TFTs as a function of semiconductor thickness, (b) TFT ON/OFF-current ratio variations vs. t_s, (c) the subthreshold swing vs. t_s, and (d) the field-effect mobility vs. t_s. 95
Figure S 5: Electrical stability measurement of TFTs with 10 nm MoS_2 bulk thicknesses in different backchannel conditions. 96
Figure S 6: OFF current of the bottom gate, top gate, and top gate pristine MoS_2 TFT as a function of MoS_2 bulk thickness. 98
Figure S 7: Electrical stability measurement of (A) etched dual-gate MoS_2 TFT with t_s = 5 nm, (B) etched dual-gate MoS_2 TFT with t_s = 25 nm, (C) pristine dual-gate MoS_2 TFT with t_s = 25 nm, and (D) pristine dual-gate MoS_2 TFT with t_s = 40 nm at different top gate voltages. 99

List of Tables

Table 1: Typical features of various multilayer MoS_2 TFTs. ... 21
Table 2: Bias-stress measurement parameters at different t_s. ... 93
Table 3: Bias-stress measurement parameters for t_s = 10 nm at different backchannel conditions ... 97
Table 4: Bias-stress measurement parameters ... 102

List of Abbreviations

TMDC	Transition Metal Dichalcogenide
2-D	Two-Dimensional
D_A	Acceptor channel doping,
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
k_B	Boltzmann constant
L	Channel Length
W	Channel Width
CVD	Chemical Vapor Deposition
I-V	Current-Voltage
N_t	Density of bulk traps
D_t	Density of interface traps
Cs	Depletion region capacitance
D_D	Donor channel doping,
V_d	Drain Voltage
Q_f	Effective charge in the depletion region
μ_e	Effective mobility
FETs	Field-Effect Transistors
MOSFET	Metal-Oxide-Semiconductor Field Effect
Φ_{ms}	Metal-semiconductor work function difference
ts	MoS_2 bulk thickness
PECVD	Plasma-Enhanced Chemical Vapor Deposition
S	Subthreshold swing
V_{th}	Threshold Voltage
E_a	Trap activation energy
XPS	X-ray Photoelectron Spectroscopy

Chapter 1
Introduction

1.1 Introduction

CMOS technology has become well established in the semiconductor industry over the past 40 years. The industry has used Moore's Law as a reference for technological progress. According to this law, the number of transistors in a dense integrated circuit is doubled almost every two years [1]. The International Technology Roadmap for Semiconductors (ITRS) was developed to outline the next steps to reach this aggressive projection. Until today, the miniaturization of the transistor's physical dimensions to about 5 nm makes Moore's Law projection valid [2]. However, further decreasing the physical dimensions leads to so-called short-channel effects, which lower the electrical performance.

Furthermore, the devices suffer from variations in the device parameters and low reliability over time [3]. Unfortunately, Moore's Law can not be further valid with only the current established technology, design, and materials. Thus, new technologies, such as spintronics [4], single electron devices [5], and molecular computing [6], are being evaluated as solutions for the described problem. However, despite the exciting and promising applications based on these technologies, they are unlikely to provide a platform to replace the CMOS technology in the near future.

Metal-oxide-semiconductor field effect (MOSFET) technology with two-dimensional (2D) channel materials is a promising solution for sustaining the Moore's Law projection. As such, the discovery of the field effect in graphene by Novoselov et al. in 2004 triggered extensive

research in this field [7]. Gradually, different 2D materials, such as transition metal dichalcogenides (TMDCs), are introduced as potential semiconductors for realizing the next generation of field-effect transistors (FETs) [8-10]. This chapter briefly reviews transition metal dichalcogenides' structural and electrical properties. Then the device physics of TMDC-based thin film transistors is reviewed.

1.2 Two-dimensional materials

2D layered materials are a group of materials having an atomically thin, layered crystalline phase. The intralayer bonding in these materials is covalent, and the layers are held together with weak van der Waals bonding. Figure 1.2-1 shows different physical structures of 2D layered materials, including archetypical 2D crystalline graphene, transition metal dichalcogenides (TMDs), diatomic hexagonal boron nitride, and monoatomic buckled crystals known as Xenes (e.g., germanene and phosphorene). These materials are considered 2D since the crystalline solid is the thinnest form that can be created. Moreover, they have a fully terminated surface with no dangling bond and more superior intralayer charge transport than interlayer [11].

Research in the field of 2D materials grew significantly after the first demonstration of a field-effect graphene transistor by Andre Geim and Konstantin Novoselov in 2004 [7]. Although their pioneering mechanical exfoliation fabrication method was the first approach for processing graphene and other 2D materials, other approaches, such as chemical vapor deposition [12] and epitaxial growth [13], are also used to obtain 2D materials.

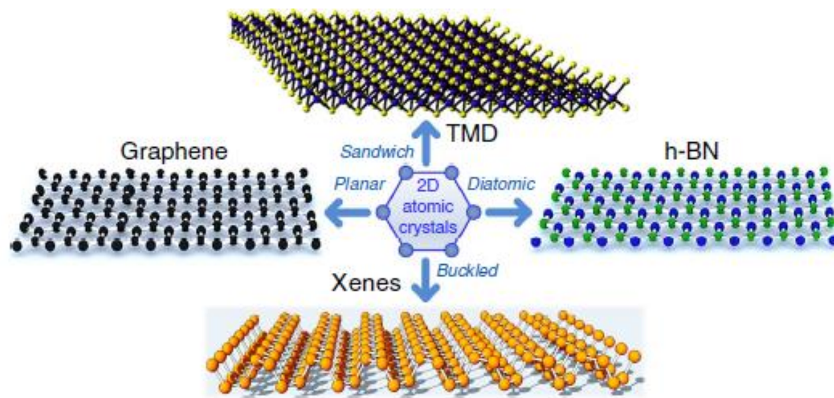

Figure 1.2-1: contemporary 2D monolayers' physical structures. Reproduced with permission from [11]. Copyright © 2014, Nature Publishing Group.

Graphene was the first 2D material obtained by mechanical exfoliation. The lack of a band gap makes it unappealing for switching applications. Therefore, transition metal dichalcogenides attract attention due to having a tunable bandgap.

1.3 Transition metal dichalcogenides

Transition metal dichalcogenides (TMDCs) are another group of 2D materials that can be thinned to a monolayer. The general formula of this group is MX_2, where M is a transition metal from groups IV, V, or VI, and X is a chalcogen (S, Se, or Te). In a monolayer of TMDC, a metal layer (M) is sandwiched by two chalcogen layers (X), and these sublayers are covalently bonded together. Single layers are bonded with weak Van der Waals forces, enabling bulk exfoliation to a monolayer. Bandgaps around 1-2 eV for several members of the TMDCs group make them suitable for FET switching devices [14].

Furthermore, carrier transport in these materials relies on the number of layers. For instance, while the bandgap of bulk MoS_2 is 1.3 eV and indirect, monolayer MoS_2 is 1.8 eV and direct, making a monolayer MoS_2 appealing for optoelectronic applications [14]. TMDCs can be utilized as electrodes such as tungsten ditelluride (WTe_2), insulators such as hafnium disulfide (HfS_2), and semiconductors such as molybdenum disulfide (MoS_2), tungsten disulfide (WS_2) and tungsten diselenide (WSe_2).

The advantages offered by 2D TMDCs over conventional 3D semiconductors like Si, Ge, and III-Vs include their ultra-thin bodies that enable superior electrostatic gate control and carrier confinement compared to bulk 3D semiconductors. This feature can be beneficial in reducing short-channel effects in ultra-scaled FETs based on 2D TMDCs, as the ultra-thin bodies of these materials can lead to a significant reduction in the characteristic channel length scaling (L_{CH}) factor "λ" given by:

$$\boldsymbol{\lambda = \sqrt{\frac{t_{ox} t_{body} \varepsilon_{body}}{\varepsilon_{ox}}}} \qquad \textbf{(Equation 1-1)}$$

, where t_{ox} and t_{body} are oxide and semiconductor thickness, respectively, and ε_{ox} and ε_{body} are their correspondence dielectric constants [15]. As channel length decreases, the gate can control a lower fraction of charge in the channel region due to the extended drain space charge region into the channel. This issue leads to short-channel effects. A straightforward formula to determine the scaling limit of FETs, which is the minimum length required to avoid short-channel effects, is that L_{CH} must be greater than three times the characteristic "channel length (L_{CH}) scaling" factor " λ." Low L_{CH} can be achieved in the 2D TMDCs due to their ultra-thin body thickness.

Additionally, 2D TMDCs have the advantage of having a broad range of sizable band gaps and various band alignments. They also lack surface "dangling bonds," a feature not found in conventional 3D semiconductors. This characteristic enables the formation of pure, defect-free interfaces compared to conventional Si-based devices. This property though also makes the TMDC materials sensitive to surface contamination and microfabrication processes that may modify the surface properties of the layers and affect the overall device performance

Among the TMDCs, MoS_2 has been one of the most studied TMDCs due the natural availability as molybdenite. It possesses promising semiconducting characteristics and can enable potential applications in nanoelectronics [16]. While these properties provide a strong motivation for selecting MoS_2 as the target semiconductor for this research, there are still many unknowns to how the processing of the materials affect the resulting fabricated device and its performance. In this thesis, the effect of processing of few-layer and multi-layer MoS_2 structures was investigated. The thesis investigates the effect of conventional microfabrication techniques to develop a fundamental understanding of these processes on the device characteristics of TMDC-based field-effect transistors.

1.4 MoS_2 properties

MoS_2 consists of a stack of planes where the hexagonal structure of closely packed molybdenum and sulfur atoms connected by covalent bonds. The MoS_2 planes are stacked with weak Van der Waals interactions in the range of 200 meV per unit cell [14]. Each monolayer thickness is approximately 0.65 nm. MoS_2 has three well-known structural polytypes: 2H

(hexagonal symmetry), 1T (tetragonal symmetry), and 3R (rhombohedral symmetry). Among them, 2H-MoS_2 has semiconducting properties (Figure 1.4-1).

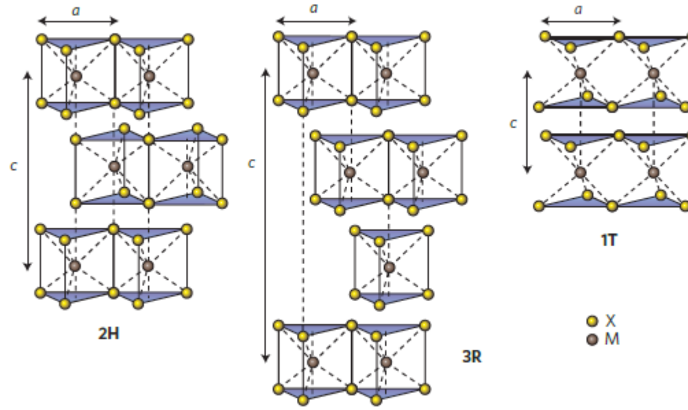

Figure 1.4-1: Schematics of structural polytypes of MoS_2. Reproduced with permission from [17]. Copyright © 2012, Nature Publishing Group.

MoS_2 has a tunable bandgap depending on the number of layers. While a MoS_2 monolayer has a direct bandgap of 1.8 eV, the bulk has an indirect bandgap of 1.3 eV [9]. Thus, the number of layers determines the electrical properties of the MoS_2 film. In order to define the number of layers of MoS_2 flakes, Raman spectroscopy is used [17]. The number of layers changes the phonon vibration properties of MoS_2. In the Raman spectroscopy of MoS_2, out-of-plane A_{1g}, and in-plane E_{2g}^1 and E_{1u} modes are the key active phonon modes near the 406cm^{-1} and 382cm^{-1} wave numbers (Figure 1.4-2 (a)). By increasing the number of layers from mono to bulk, A_{1g} and E_{2g}^1 have upshift and downshift, respectively (Figure 1.4-2 (b)). The upshift of the A_{1g} with increasing the number of layers is due to the increased effective restoring force acting on the atoms because of higher interlayer interactions. At the same time, the downshift of the E_{2g}^1

is due to long-range Columbic interlayer interactions, which decreases the restoring forces on the atoms [18, 19].

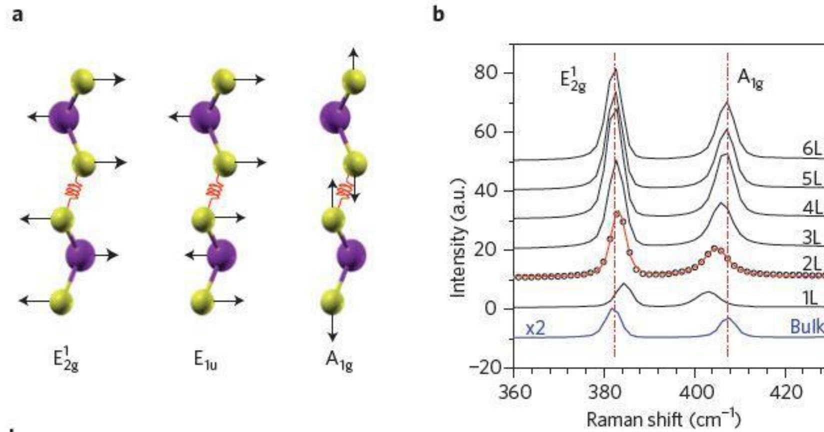

Figure 1.4-2: (a) Vibration Modes and (b) Raman Spectra of 2H-MoS_2 with a different number of layers. Reproduced with permission from [17]. Copyright © 2012, Nature Publishing Group.

The monolayer has attracted attention for optoelectronics applications. At the same time, multilayer TFTs show a higher drive current originating from the multiple conduction channels and less stringent device fabrication processes, making multilayer MoS_2 suitable for fabricating thin-film transistors [9]. Thus, multilayer MoS_2 will be used in this research to fabricate thin film transistors (TFTs).

1.5 Thin-film transistors

TFTs are field-effect transistors (FETs) comprising three electrodes: a drain (d), source (s), and gate (g) contact. The working principle of TFTs is similar to the MOSFET. In a TFT illustrated in Figure 1.5-1 (a), the gate electrode controls the carrier flow from the source to

the drain. The gate voltage creates a transverse electric field that has either of these effects: 1) depleting the semiconducting channel of carriers that block the current flow from source to drain (off-state), 2) or increasing the channel carrier concentration in the semiconductor to enable the flow of current (on-state) happening at gate voltages higher than the threshold voltage (Figure 1.5-1 (b), (c)). In an ideal transistor, the off-current is very small ($I_D<10^{-12} A/cm^2$), and the ratio between the on and off current is > 10^4 [20].

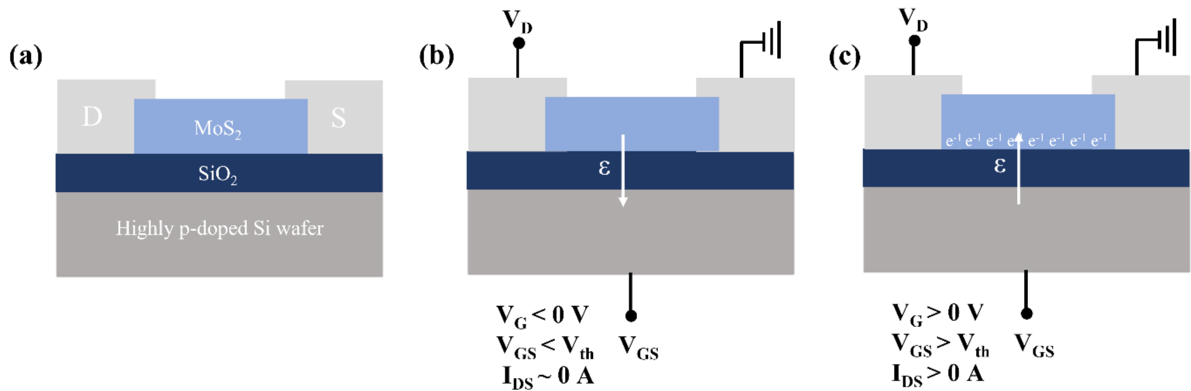

Figure 1.5-1: (a) Schematic of a MoS_2 TFT, (b) TFT in OFF state, (c) TFT in ON state.

Different materials are used as a semiconductor for fabricating thin film transistors. The following section discusses the two most prominent material systems for TFT fabrication.

1.5.1 Materials for thin-film transistors

Disordered and 2D materials are two categories of materials investigated for thin-film transistor applications [17, 21]. Although both material systems have distinctive features that make them suitable for electronic applications, they differ in various ways.

Disordered materials lack long-range order in their atomic structure, such as amorphous silicon, organic semiconductors, and some metal oxides [20]. In addition, they often have high defect densities, which can lead to poor charge carrier mobility and electrical stability. In TFT applications, disordered materials are frequently used for the semiconductor because they can be deposited at low temperatures over large area, making them compatible with glass and flexible substrates. However, their low mobility and stability can constrain their performance [21].

On the other hand, 2D materials refer to single-crystal materials that comprise single or multi-layers of atoms [17]. The lower defect density in the bulk of the 2D materials than in disorder materials results in a higher field effect mobility and stability. However, other trap sites, backchannel surfaces and semiconductor/dielectric interfaces, can significantly affect their electrical properties. The challenges with 2D materials are their synthesis, processing, and lack of understanding of the processing effect on the electrical properties of the TFTs. These challenges are discussed in detail in Chapter 2.

1.5.2 Trap states in 2D semiconductors

Trap states in 2D semiconductors are present in various locations, including the TMDC bulk, TMDC/dielectric interface, and TMDC backchannel surface [22].

Defects, such as vacancies, dislocations, and grain boundaries, have been detected in TMDCs, regardless of the synthetic approach. The sample preparation approach defines the dominant type of defects, with sulfur vacancies being the primary type of trap in CVD-deposited and mechanically exfoliated samples [23, 24].

Bulk traps in multi-layer TMDC-based TFTs can have multiple negative effects on the electrical performance of the device. Firstly, they can make the threshold voltage (V_{th}) a negative value, causing the TFT to operate as a depletion mode device. The threshold voltage is the gate voltage, at which the gate begins to control current flow by effectively modulating the conductivity of the semiconductor. Since bulk traps can capture and hold some charge carriers, they can change the threshold voltage [25] due to the electrostatic shielding from the occupied trap states.

Secondly, bulk trap states have the capability to seize and immobilize charge carriers present in the semiconductor substance. This entrapment diminishes the pool of available carriers for conducting, leading to a decline in the flow of current in the transistor. As time elapses, the captured carriers can be liberated, giving rise to a delayed reaction or hysteresis in the behavior of the transistor [26]. Furthermore, bulk traps can decrease the field-effect mobility (μ_e) of the TFT. Field-effect mobility measures the transport of charge carriers through a solid under the influence of an electric field and scattering mechanisms. When charge carriers come across trap states, they have the potential to deflect from their intended trajectory due to the presence of localized energy levels [26]. This deflection, known as scattering, hampers the mobility of the carriers, degrading the charge transport within the semiconductor. Consequently, charge

transport efficiency is reduced, resulting in a decline in carrier mobility. These scattering events have a negative impact on the overall conductivity of the transistor [26]. The effect of bulk trap states on the electrical transport of TMDC-based TFTs is investigated in Chapter 4.

Therefore, in TMDC-based TFTs having multiple layers, the bulk material plays an important role in the device behavior. It is important to understand how defects in the bulk affect the TFT performance and how these defect states may be minimized in multi-layer TMDC-based TFTs to enhance their electrical performance. In this research, the bulk traps are minimized by etching the TMDC bulk thickness using a dry plasma etch. This approach may lead to an improvement in the electrical performance and stability of multi-layer TMDC-based TFTs. The approach is systematically discussed in Chapter 4, showing the role of the TMDC bulk in affecting the electrical behavior of the TFT.

Traps at the semiconductor/dielectric interface capture electrons under a large positive gate bias and release them at a large negative gate bias. This trapping behavior changes the threshold voltage [25]. The cause of this effect is due to unscreened Coulomb scattering by the trapped charges at the interface [27]. On the other hand, microfabrication processes on the backchannel surface, such as dry etching, can induce traps on the surface by increasing surface roughness [28], sulfur vacancies [29], or oxidizing the surface [30]. Additionally, oxygen and water molecule adsorbates on the backchannel surface are another source of surface traps that capture electrons from the channel, resulting in an increase in the threshold voltage due to electron depletion under a large positive gate bias [25]. This issue causes a degradation in the electrical

properties of TMDC-based TFTs. The following sections will explain the basics of the electronic properties of TMDC-based TFTs.

1.5.3 The electronic properties of TMDC-based thin film transistors

The band diagram of an n-type MoS_2 TFT under different applied gate voltages is depicted in Figure 1.5-2. Ideally, the band diagram is flat when the gate voltage is zero (Figure 1.5-2 (a)). A region depleted of free carriers forms by applying a negative gate bias for an n-type semiconductor. A positively charged region forms when the mobile charges are depleted, causing the conduction and valence bands to bend upward (Figure 1.5-2 (b)). During the accumulation of electrons at the gate dielectric/channel layer interface by an applied (in this case, $V_G > 0$ V) gate bias, a downward (positively sloped) bending of the bands occurs (Figure 1.5-2 (c)). For the investigated MoS_2 TFTs, there can be two classifications for operation based on the gate voltage: a) accumulation mode and b) depletion mode devices. In the depletion mode, the devices are turned off by depleting the channel layer under negative bias. In contrast, the former devices require positive voltage to be turned on [20].

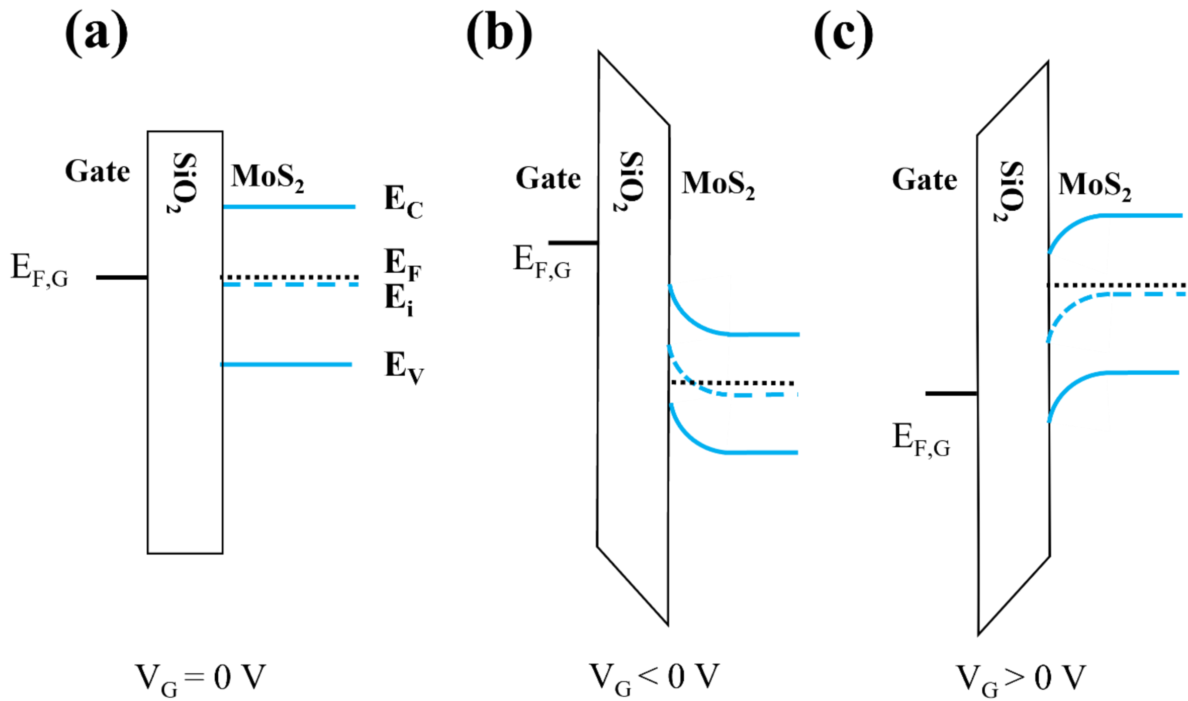

Figure 1.5-2: Band diagram of an n-type TFT under different conditions of gate voltage (a) No gate bias, (b) Negative gate bias, (c) Positive gate bias.

1.5.4 Current-Voltage Relations of a TFT

In the TFTs, parameters such as the threshold voltage (V_{th}), field-effect mobility μ_e, ratio between ON and OFF currents, and subthreshold swing (S) are often extracted with equations governing the relationships between current and voltage characteristics in MOSFETs.

When $V_d < V_g\text{-}V_{th}$, the TFT works in linear mode, and when $V_d > V_g\text{-}V_{th}$, the device works in saturation mode, where V_d is the drain voltage, and V_g is the gate voltage. The gradual-channel approximation can be used to determine the linear and saturation current of TFTs:

$$I_d = \frac{W\mu_n C_g}{2L}\left[2\left(V_g - V_{th}\right)V_d - V_d^2\right] \qquad for\ 0 \le V_d \le V_d(sat) \qquad \textbf{(Equation 1-2)}$$

$$I_d(sat) = \frac{W\mu_n C_g}{2L}\left(V_g - V_{th}\right)^2 \qquad for\ V_d > V_d(sat) \qquad \textbf{(Equation 1-3)}$$

Where C_g is the specific capacitance of the gate dielectric, W and L are the TFT channel width and length, respectively.

In the first equation, the squared term is negligible when V_d is low, and the device behaves like a variable resistor with the I_d proportional to the V_d (Figure 1.5-3 (a)). At higher V_d values, the surrounding region of the drain becomes depleted of electrons, making a pinch-off point, and the I_d does not change by increasing the V_d (Figure 1.5-3 (b)). When V_G-V_{th} < V_d, the device is in saturation mode (Figure 1.5-3 (c)). In this mode, the device is like a constant current source where the gate voltage varies with the drive current [31].

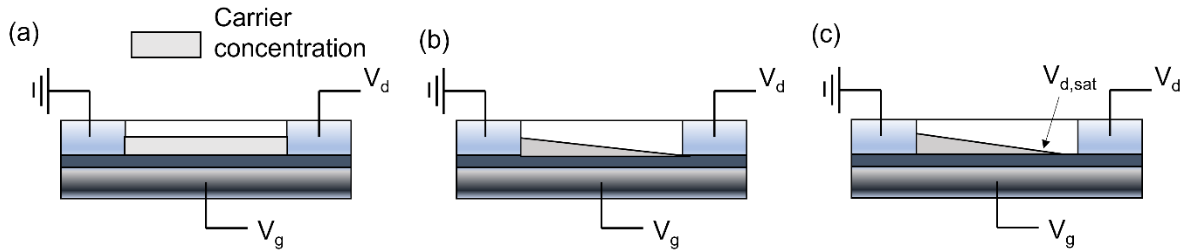

Figure 1.5-3: (a) Carrier concentration profile of TFT in the linear regime. (b) Pinch-off (c) saturation regime.

The existence of short-range order in the disorder materials enables us to use the relationships governing the I-V characteristics for single crystal materials [20]. Furthermore, it is possible to use these relationships for 2D materials due to their single crystalline properties.

1.5.5 Threshold voltage

Ideally, the threshold voltage is positive for an n-channel MoS_2 TFT, and the device works in enhancement mode. However, the threshold voltage can be negative, and the TFT operates in the depletion mode. In this research, it is observed that the MoS_2 TFTs on SiO_2 dielectric operate in depletion mode, and the threshold voltage is a high negative value, which is not ideal for low-power applications. The negative threshold voltage might be due to the trapped charges (Q_T) given by: $Q_T \approx -qN_T t_s(E_F - E_i)$, where N_t is the bulk trap density, t_s is the MoS_2 thickness, q is the electron charge, and E_F and E_i are the Fermi and the midgap energy levels, respectively. Thus, the threshold voltage can be written as:

$$V_{th} \approx \frac{qN_t t_s(E_F - E_i)_{threshold}}{C_g} \qquad \textbf{(Equation 1-4)}$$

In practice, the semiconductor/dielectric interface is not ideal due to the MoS_2 transferring process, which is done in the air. Thereby the threshold voltage equation can be related to the bulk and interface trap densities for thin film transistors [26]:

$$V_{th} \approx \frac{qN_t t_s(E_F - E_i)_{threshold}}{C_g} - \frac{Q_f}{C_g} + \frac{qD_t(E_F - E_i)_{threshold}}{C_g} - \frac{q(D_D - D_A)}{C_g} + \Phi_{ms} \qquad \textbf{(Equation 1-5)}$$

, where Q_f is the effective charge in the depletion region, D_D and D_A are the donor and acceptor channel doping, respectively, and Φ_{ms} is the metal-semiconductor work function difference [26]. As a result, traps inside the semiconductor bulk, interfaces, and/or doping concentration variation may lead to a negative threshold voltage, resulting in the TFT operating as a depletion mode device.

In the case of multi-layer TMDC TFTs, when the TMDC thickness is higher than the maximum gate electric field screening length (ℓ), the gate cannot control the trapped charges in bulk. The maximum gate electric field screening length, ℓ, is given by:

$$\boldsymbol{\ell = (\varepsilon_s / q^2 N_t)^{1/2}} \quad \textbf{(Equation 1-6)}$$

, where ε_s is the MoS_2 dielectric constant [26]. Thus, the TFT structures in this thesis is expected to have a screening length of ~ 15 nm. This issue may lead to a high negative threshold voltage. Etching processes may be used to remove these bulk defects and improve the gate control over the trap states by thinning the film. As a result, removing these defects and TMDC bulk thinning can change the threshold voltage of the transistor. This hypothesis is investigated in Chapter 4.

Furthermore, the nature of the metal-semiconductor interface (the work function of the metal electrodes), can also affect the threshold voltage of the TFT. The work function differences between the metal and the semiconductor can induce a Schottky barrier at the interface, shifting the threshold voltage. To achieve high performance in TMDC TFTs, it is necessary to form a metal-TMDC junction with low contact resistance. Titanium is commonly used as a drain and source contact for mechanically exfoliated MoS_2 flakes due to the small Schottky barrier between MoS_2 and Ti (~60 meV) [32]. Thus, the research presented uses Titanium as the drain-source contact.

1.5.6 Subthreshold swing

In equations 1.5-1 and 1.5-2, it is assumed that the transistor does not have a flow of charges at gate voltages lower than V_{th}. In reality, the channel may not be completely depleted. The drain current near threshold is characterized by an exponential behavior and is characterized by plotting the I_d-V_g curve in a semi-log form. Extracting the inverse slope of the linear part of the semi-log curve provides the subthreshold swing (*S*). For switching applications of the TFT, having small values of *S* is preferable, meaning that the transistor can rapidly change from an Off- to an On-state by small gate voltage variations. In the case of the Si-MOSFET with an inversion layer, the theoretical subthreshold swing is given by:

$$\boldsymbol{S \equiv \frac{dV_g}{dlogI_d} \approx \frac{k_BT}{q}\left(1+\frac{C_S}{C_g}\right)ln10}$$ **(Equation 1-7)**

, where C_S is the depletion region capacitance and k_B is Boltzmann constant.

In the case of disordered materials, the interface and semiconductor bulk states also have an impact on the sub-threshold swing. Within the sub-threshold regime for a given variation in V_G, the interface and bulk trap states will capture a portion of the induced surface charge leading to the more trapped charge and reducing the concentration of free charge that results in less band bending under applied gate bias [26]. This effect changes the threshold voltage of the transistor in order to maintain the same drive current resulting in a larger *S* for the device.

Accounting for the trap states, the subthreshold current [26] is given by:

$$\boldsymbol{I_D \propto \frac{k_BT}{q}\mu_e.\, e^{\frac{C_gV_G}{qN_Tt_sk_BT}}/L}$$ **(Equation 1-8)**

For the inverse subthreshold slope, we find:

$$^{1}/_{S} = \left(\frac{dlog_{10}I_D}{dV_G}\right) = \left(\frac{C_g}{q^2\left(\frac{k_BT}{q}\right)(N_t t_s)}\right) \times log_{10}e \qquad \textbf{(Equation 1-9)}$$

Considering the effect of interface traps, the inverse subthreshold slope can be written as:

$$^{1}/_{S} = \left(\frac{C_g}{q^2\left(\frac{k_BT}{q}\right)(N_t t_s + D_t)}\right) \times log_{10}e \qquad \textbf{(Equation 1-10)}$$

The MoS_2 TFT subthreshold swing value has a theoretical limit of 60 mV/dec [33], but the typical value for our devices on SiO_2 dielectric is around 2 V/dec. This value can vary with changing trap density in the MoS_2 TFT structure.

1.5.7 Field effect Mobility

Field-effect mobility measures the transport of charge carriers through a solid under the influence of an electric field and scattering mechanisms. In monolayer 2D materials, charge carriers move primarily in a 2D plane, leading to unique electronic and optical properties compared to 3D materials [17]. The field-effect mobility of TFTs can be significantly affected by the number of layers in 2D materials.

The impact of the multilayer 2D structure on field-effect mobility depends on several factors, including the number of layers, stacking order, and properties of individual layers [34]. Generally, multilayer 2D materials exhibit higher field-effect mobility than their single-layer counterparts due to increased carrier density and reduced Coulomb scattering in the multilayer structure [34]. In multilayer MoS_2, varying the number of layers can tune the bandgap, interlayer interactions, and Coulomb scattering [17].

However, the impact of the multilayer structure on field-effect mobility can also depend on interface quality between layers. Defects or impurities at interfaces can act as scattering centers for charge carriers and reduce mobility [17]. Backchannel surface and semiconductor/dielectric interface traps can also significantly impact field-effect mobility. Investigating the thickness-dependent behavior of each trap site can help reveal their effects on the electrical performance. Further research is needed to fully understand these factors.

The linear or saturation regimes are used to extract the field-effect mobility μ_e. I_d can be fitted to a straight line with respect to V_G in the linear regime (when $V_d << V_d$ (sat)), and mobility is derived in the linear region from the slope of the line as follows:

$$\boldsymbol{\mu_e = \left[\frac{\partial I_{ds}}{\partial V_{gs}}\right] \times \left[\frac{L}{C_g V_{ds} W}\right],} \qquad \textbf{(Equation 1-11)}$$

The typical field effect mobility value for non-passivated multilayer MoS_2 TFT on SiO_2 is reported as 22 $cm^2/V.s$ [35-37].

1.5.8 State-of-art TMDC Field effect transistors

In 2004, the first TMDC transistor was reported, which utilized WSe_2 as the transistor channel material [38]. This transistor displayed a mobility of up to 500 $cm^2/V.s$, ambipolar behavior, and an on/off current ratio of 10^4 at a low temperature of 60 K. The first n-type MoS_2 transistor was introduced by Kis, *et al.* in a top-gated structure with a single layer of MoS_2 [8]. This transistor exhibited a significant on/off current ratio of approximately 10^8, a large room-temperature mobility of 200 $cm^2/V.s$, and a subthreshold swing of 74 mV/decade. In another study, a p-type FET with WSe_2 was created using a top-gate geometry with high-k dielectric

and chemically doped source/drain contacts [39]. This monolayer transistor had a hole mobility of 250 cm^2/V.s, an on/off current ratio of 10^6, and a subthreshold swing of 60 mV/decade.

Recently, many advanced devices using MoS_2 have been explored. One of these devices used atomic-layer-deposited (ALD) high-k dielectric integration on MoS_2 crystals and dual-gate n-channel with ALD Al_2O_3 as the gate dielectric [40]. This device showed high field-effect mobility of electrons. However, the commercial fabrication processes of single-layer MoS_2 with high-k dielectric layers are limited by their compatibility with the large-area fabrication methods. As a result, multilayer MoS_2 FETs have been thoroughly investigated. Table 1 shows the reported features of multilayer MoS_2 TFTs with SiO_2 dielectric. These FETs display electrical parameter dependence on the thickness of the MoS_2 bulk, for few layer and monolayer structures. The MoS_2 bulk plays an essential role in the behavior of multilayer TFTs. This topic is further investigated in Chapter 4. Studying the TFTs with different thicknesses fabricated in this thesis, with the state-of-art, shows the value of the typical features are close to the state-of-art (Chapter 4).

Table 1: Typical features of various multilayer MoS_2 TFTs.

Thickness (nm)	Electrodes	Effective mobility ($cm^2/V.s$)	Subthreshold swing (V/dec)	Threshold voltage (V)	Reference
2.8	Cr/Au	20	1.6	-30	[37]
5	Ti/Au	13	1	-10	[41]
10	Au	24	0.24	-1.3	[36]
15	Cr/Au	20	2	-25	[42]
20	Ti/Au	20-30	-	-	[34]
32	Ti/Ni	37	3-4	-30	[43]
39	Ti/Ni	32	3-4	-35	[43]
50	Au	23	4	-40	[35]

Chapter 2

Challenges of developing TMDC-based devices

2.1 Introduction

High mobility, a low surface dangling bond, and a tunable bandgap make TMDCs interesting materials for TFT operation [8, 44]. However, the advance of the TMDC-based TFTs for different applications, such as memory devices, needs a reliable method for depositing high-quality TMDC layers and controlling their thicknesses. Furthermore, long-term stability is required for developing TMDC-based devices. This requirement is impeded by the existence of traps in the TMDC bulk, the semiconductor/dielectric interfaces, and/or the backchannel surface. A more precise understanding of the factors involved in the bias instability helps improve the two-dimensional semiconductor performance for the next generation of memory devices. This chapter will discuss common TMDC deposition methods, the TMDC thinning process, and prior investigations of the trap sources' impact on TMDC devices.

2.2 TMDC synthesis

Various methods have been successfully used to synthesize TMDC, which are classified into two groups. Bottom-up methods (e.g., chemical vapor deposition (CVD)) and top-down methods (e.g., mechanical exfoliation).

2.2.1 Bottom-up method

For many years, the chemical vapor deposition technique has been utilized for growing TMDC films [45-48]. Various approaches are used to deposit TMDCs from the vapor phase.

These approaches include MoO_3 or Mo metal sulfurization or selenization using sulfur/ selenium vapor phase [49, 50], MoS_2 powder direct evaporation [51], single precursor thermolysis [52], and utilizing multiple precursors e.g., H_2S, MCl_5, or $M(CO)_6$ [53-55]. CVD technique leads to synthesizing large-area TMDC films; however, the deposited film is polycrystalline with a smaller grain size than those made by mechanical exfoliation [56, 57] (Figure 2.2-1). Furthermore, the technique requires high temperatures (700-1000 ˚C) that prevent using large-area substrates such as glass [55]. In addition, this method introduces impurities, causing structural defects, wrinkles, and contaminations in the deposited films. This issue can lead to changes in the electrical properties of the TMDC film [58, 59].

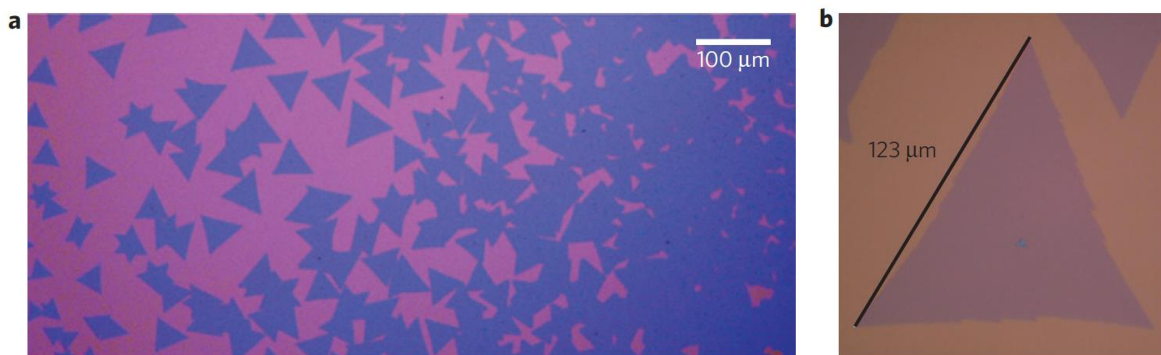

Figure 2.2-1: (a) Optical micrograph of CVD growth MoS_2 on SiO_2 substrate and (b) single layer MoS_2 triangle with a 123 μm grain size. Reproduced with permission from [57]. Copyright © 2013, Nature Publishing Group.

2.2.2 Top-down method

The crystal quality, purity, and grain size of TMDC films are essential for high-performance applications. Mechanical exfoliation using the scotch-tape method is the easiest and the most popular method for obtaining high-quality, thin, microscale sheets on arbitrary substrates, and it is still the best approach for studying the fundamental properties and prototyping of TMDC-based devices [60-62]. This method uses an adhesive tape to liberate a thin layer of TMDC from the parent bulk material (Figure 2.2-2 (a)). The thickness of the thin layer is further reduced by repeating the exfoliation process. Eventually, the tape with the exfoliated materials is placed on the desired substrate and subsequently peeled away (Figure 2.2-2 (b)). TMDC flakes on the target substrate can be detected using optical contrast induced by the thickness/substrate interface effects [63]. Furthermore, atomic force microscopy and Raman spectroscopy are used to characterize the transferred TMDC flakes further.

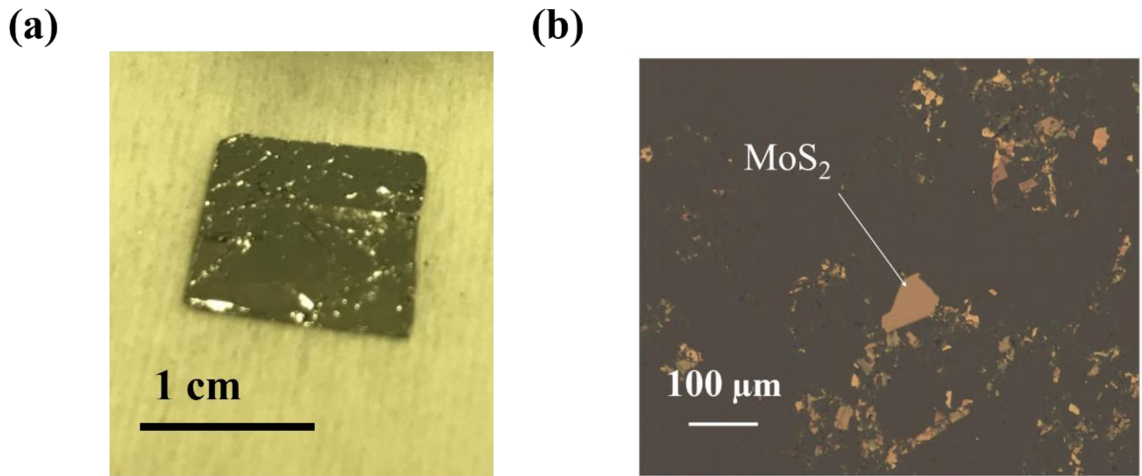

Figure 2.2-2: (a) parent MoS_2 bulk material. (b) transferred MoS_2 films on SiO_2 substrate using mechanical exfoliation.

Unfortunately, the mechanical exfoliation method causes defects in the TMDC semiconductor [42, 64] at the interface states between the semiconductor and gate dielectric structure [27, 65] and the backchannel surface [66-69]. Furthermore, processing the transferred TMDC flakes with this approach is difficult due to the small and discontinuous shapes, leading to different fabrication yields and unpredictable device characteristics [9, 70, 71]. Recently, some attempts have been made to increase the lateral dimensions of the transferred flakes up to 500×500 μm^2 using additional annealing steps and intermediate materials in the exfoliation process (e.g., Au) [68, 72]; however, the TMDC flakes transferring yield in these approaches are low. In this thesis, mechanical exfoliation using a soluble tape is developed to address the problems of the conventional mechanical exfoliation method, which will be explained in Chapter 3.

2.3 TMDC thinning process

In the mechanical exfoliation technique, the thickness of the flakes is not well controlled. Moreover, there is a tradeoff between the area and thickness of flakes, where thinner ones result in smaller areas. Therefore, an etching technique that reduces the thickness of the flakes without reducing their area is needed. The dry etching technique provides the ability to etch the TMDC flakes uniformly. Moreover, the etch rate is independent of the initial thickness of the flake [73-76]. Different precursor gases were reported in the literature, such as Ar, SF_6/N_2, Cf_4, etc. [73-76]. This project used an SF_6/O_2 dry etching process to thin the TMDC layers to achieve few-layer (3 – 4 layers) structures (Chapter 3). Exposure to the plasma may change the physical and electrical properties of the TMDC film. Huang et al. [28] show the surface

morphology of TMDC film significantly varies after the dry etching process. This variation might be due to a nonuniform reaction on the surface because of adsorbates on the surface. Furthermore, different etch rates of Mo and S in the sandwich structure of S-Mo-S might be another root cause of the nonuniform etching process on the TMDC surface [28].

Moreover, plasma exposure may lead to the incorporation of impurities in the TMDC film. Neal et al. [77] studied the effect of oxygen plasma exposure on the electrical properties of MoS_2 TFTs. They show after the plasma exposure, the MoS_2 film is doped with oxygen molecules, which leads to p-type doping and conductivity variations. Furthermore, the oxygen incorporation can create new energy states within the bandgap of MoS_2 and cause significant lattice distortions [78]. These new states can act as trap sites for charge carriers and reduce their mobility, which can be undesirable for some electronic applications.

The TMDC synthesis process may create trap states at the semiconductor/dielectric interface, semiconductor bulk, or at the backchannel surface. Thus, it is necessary to understand the role of each trap location in determining the electrical properties of the TFT. The following sections will review prior investigations on each trap site.

2.4 TMDC/dielectric interface traps

Traps at the semiconductor/dielectric interface capture electrons under large positive gate bias and release them at large negative gate bias, causing a change in the threshold voltage [25], suggesting an unscreened Coulomb scattering by the trapped charges at the interface [27].

Illarionov et al. show the role of dielectric material on the density of TMDC/dielectric interface traps by fabricating TMDC TFTs on SiO_2 and hBN dielectrics. They illustrate a better electrical performance for the TFTs on hBN rises from the lower TMDC/dielectric interface trap density [65]. Furthermore, the dielectric cleaning procedure plays an important role in the TMDC/dielectric interface trap density. Shen et al. use an oxygen plasma cleaning procedure to control the density of the TMDC/dielectric interface trap [79]. The effect of TMDC/dielectric interface traps on the electrical performance is observed in TFTs with small [27, 65, 69] and large [80, 81] TMDC bulk thicknesses. These studies suggest that the TMDC bulk thickness might significantly impact electrical performance. This topic is discussed in the next section.

2.5 TMDC bulk traps

Regardless of the synthesis approaches, bulk defects have been detected in TMDCs. These defects include vacancies, dislocations, and grain boundaries [22]. The sample preparation approach defines the dominant type of defects [23]; for instance, sulfur vacancy is the primary type of trap in the CVD-deposited and mechanically exfoliated samples [23, 24]. Shu et al. have investigated the effect of TMDC bulk traps on the electrical performance of multilayer TMDC-based devices. They have studied the electrical stability of dielectric supported and suspended multilayer MoS_2 TFTs, showing both structures have bias instability, rising from the MoS_2 bulk traps besides some minor impact from the backchannel surface traps [42]. It is shown that the TMDC bulk traps are filled with free carriers at a positive gate bias, causing a

decrease in conduction and a positive threshold voltage shift [25]. In another study, a multilayer MoS_2 TFT was passivated with cyclized transparent optical polymer (CYTOP) to decouple the effect of backchannel surface traps [64]. The authors have shown the MoS_2 bulk traps have a more dominant impact on the bias stability of the devices than the semiconductor/dielectric interface traps.

In these studies, the role of TMDC bulk traps is detected in multilayer TMDC TFTs, suggesting the TMDC thickness may play a role in bulk trap impact on the electrical performance. Kim et al. [82] have studied the effect of TMDC bulk thickness on pristine and backchannel passivated TFTs. They show that the electrical instability decreases by reducing the semiconductor thickness due to reducing the TMDC bulk trap density. In this study, the backchannel trap density was low due to utilizing thin TMDC flakes transferred with an intact and passivated backchannel surface. Therefore, the effect of backchannel surface traps was insignificant. However, different processes on the TMDC films, such as TMDC bulk thickness thinning [28, 29, 74], may introduce traps on the backchannel surface, affecting the electrical performance. The following section reviews the previous investigation on the backchannel surface traps.

2.6 Backchannel surface traps

Microfabrication processes on the backchannel surface, such as dry etching, can induce traps on the backchannel surface by increasing the surface roughness [28], increasing the sulfur vacancies [29], or oxidizing the surface [30]. Furthermore, the oxygen and water molecule adsorbates on the backchannel surface are another source of the surface traps. These traps

capture electrons from the channel, causing an increase in the threshold voltage due to electron depletion under a large positive gate bias. This issue causes electrical instability in the current–voltage characteristics [25]. Doherty et al. [83] have studied the electrical stability of uncapped MoS_2 TFTs with thicknesses ranging between 4 nm to 8 nm. After an electrical stress test, they show that the uncapped TFTs in ambient air have a substantial threshold voltage shift, significantly reduced by measuring in a vacuum chamber. These effects correlated to the backchannel surface traps due to the adsorption of oxygen and water molecules on the surface.

The review of the prior investigations shows that the effect of TMDC bulk traps is mainly observed for the TMDC devices with large thicknesses. In contrast, most studies on the backchannel surface are done on mono and few-layer TMDCs. This observation suggests that TMDC bulk thickness may define the primary trapping mechanism in the device; however, this topic has not been thoroughly studied yet. Therefore, in this thesis, the effect of TMDC bulk thickness on the electrical performance of TMDC TFTs is investigated, and the dominant trap source as a function of TMDC bulk thickness is revealed (Chapter 4). Furthermore, backchannel surface passivation can be used to reduce the effect of backchannel surface traps. This topic will be explained in the following section.

2.6.1 Backchannel surface passivation

Different backchannel encapsulation layers, including poly methyl methacrylate (PMMA) [83], SU-8 photo resist [83], hexagonal boron nitride (h-BN) [65], and plasma-enhanced chemical vapor deposition (PECVD) silicon nitride (SiN_x) [83], are used to mitigate the impact

of the backchannel surface traps on the TFT's electrical performance. SiN_x is a standard passivation material for electronic devices due to its large band gap and high thermal stability [84, 85]. However, it is shown that the SiN_x passivation leads to change and degradation of the electrical performance of the TMDC-based TFTs [83, 86]. A recent study ascribed the electrical performance variation to the TMDC crystal damage during the SiN_x deposition [83]. At the same time, another report suggests the role of trapped charges inside the MoS_2 film in changing the electrical performance of TMDC-based devices [86]. Furthermore, introducing hydrogen contamination into the active region during the passivation process is another possibility reported for PECVD SiN_x coated onto the backchannel surface of TFTs with various semiconductors [87, 88]. It was shown that hydrogen atoms could physically or chemically adsorb and replace sulfur vacancy defects [89, 90] in a TMDC film. Koh et al. [91] studied the effect of hydrogen adsorption and diffusion into the TMDC layer using density functional theory. They reported that conductivity enhancement of the TMDC film through forming S-H bonding. In addition, it is shown that hydrogen plasma exposure to a monolayer TMDC film leads to the creation of trap states [89, 92], causing degradation of the electrical performance of TMDC-based devices [93]. A more precise understanding of the root cause of the electrical performance variations of TMDC TFTs after SiN_x passivation will lead to overcoming the impediments of using this dielectric. Previous investigations are mainly done on mono to few-layer TMDCs [37, 65, 83, 86, 94-96]. Furthermore, none of these studies have systematically examined more than one TMDC bulk thickness for the comparative effect of passivation on electrical performance. Thereby, the impact of the SiN_x passivation process on the electrical performance of TMDC TFTs with various thicknesses is investigated in Chapter 5.

2.6.2 Dual gate structure

The effect of backchannel surface traps can be minimized by proper passivation using dielectric material [36, 83, 97, 98], which can be used as a top gate dielectric for fabricating a dual-gate device. A dual gate above and below the TMDC is used to perform electrostatic modulation of contact resistance, threshold voltage, and the TMDC channel [99-102]. This device architecture has applications in logic operations [101], optoelectronic response control [103], and memory devices [101, 104]. However, the investigation of dual gate TMDC TFTs is usually done on pristine backchannel surface semiconductors; thus, the effect of backchannel surface traps on the electrical performance of dual gate TFTs is ambiguous. Furthermore, the previous reports studied the dual gate effect on few-layer TMDCs films (TMDC thickness < 10 nm) [8, 99-106]; nevertheless, the impact of TMDC thickness on dual gating of dry-etched TMDC TFTs is unclear. This topic will be studied in Chapter 6.

2.7 Organization of dissertation

This Ph.D. dissertation studies the effect of the microfabrication process on the electrical performance of TMDC-based TFTs, covering the influence of large-area exfoliation of TMDC flakes, dry etching process impact on the backchannel surface, and the impact of PECVD passivation process. Finally, it describes the effect of the microfabrication process on the electrical performance of a dual gate structure electrical.

To address the introduced problems of the TMDC deposition method, a two-step mechanical exfoliation and etching approach for transferring and controlling the thickness of TMDC will be presented in Chapter 3.

In Chapter 4, the effect of the two-step mechanical exfoliation and etching approach on the electrical performance and stability of multi- and few-layer TMDC-based transistors was investigated. In this chapter, device parameters were extracted using current-voltage (I-V) and gate-bias-stress measurements to determine the effect of the process on the interface, bulk defects, and backchannel surface states on the performance of the device. PECVD SiN_x was used to passivate the TMDC devices to control the impact of backchannel surface traps. In Chapter 5, the effect of PECVD SiN_x passivation on TMDC TFTs with varying TMDC thicknesses was studied. This chapter explored the effect of SiN_x thicknesses, hydrogen plasma exposure, dielectric deposition with an electron beam and PECVD, and incorporation of hydrogen diffusion barriers on TMDC-based transistors. Chapter 6 explores the effect of backchannel surface traps on the electrical performance of dual-gate TMDC-based TFTs using dry-etched and pristine TMDC. Bilayer SiO_x/SiN_x dielectric is used to fabricate the dual gate structure. Finally, Chapter 7 summarizes the contribution of this Ph.D. thesis to the 2D semiconductor field and points out suggestions for future work.

Chapter 3

The fabrication process of TMDC-based TFT arrays using the dissolving tape method and dry etching process

3.1 Introduction

This chapter presents a two-step mechanical exfoliation and etching approach for transferring and controlling the thickness of molybdenum disulfide (MoS_2) as the active semiconductor. Atomic force microscopy (AFM) was used to characterize the thickness and surface morphology of transferred MoS_2 flakes and extract the etch rate of the dry etching process. Raman spectroscopy was used to verify the thicknesses and quality of processed MoS_2 flakes by referencing the frequency difference between the $E^1{}_{2g}$ and A_{1g} peaks to the number of MoS_2 layers.

3.2 Large–area TMDC exfoliation

The fabrication of TDMC TFTs was performed on a highly doped p^+-Si wafer with 100 nm of thermally grown SiO_2. The TMDC layer was transferred onto the Si wafer using adhesive tape attached to bulk MoS_2 (Figure 3.2-1 (a)). The tape peels off several layers of MoS_2 that are then mounted onto the final process wafer (Figure 3.2-1 (b) and 1(c)). In a conventional exfoliation process where the carrier tape is peeled away, leaving the transferred MoS_2 on the process wafer, inducing a mechanical strain on the MoS_2 that leads to structural failure of the TMDC layers. While the adhesive tape separates a large area from the bulk, subsequent tape removal may cause micro-cracking of the TDMC layers after the transfer, reducing the useful area available for device fabrication. To alleviate these challenges, an approach using a water-

soluble carrier tape (3M™ Water-Soluble Wave Solder Tape) was used, allowing the MoS_2 to be gently and reliably released without mechanical degradation. Water-soluble tape is previously used as a transfer method for 2D materials [107, 108]. The tape can be used as a temporary support layer to hold the material in place before transferring it to another substrate. This process is often called "dry transfer" or "tape transfer" and is a common method for transferring 2D materials [108]. The work presented in this thesis has scaled this approach to larger areas and demonstrates the feasibility of extending this technique towards large-scale manufacturing.

In this process, the carrier tape/MoS_2 was placed onto a process wafer followed by a 5-minute thermal anneal at 110 ˚C under ambient conditions to remove water and enhance the adhesion between MoS_2 and the SiO_2 surface (Figure 3.2-1 (d)). The tape was then dissolved by submerging the sample in water (Figure 3.2-1 (e)), leaving the transferred TDMC layer intact (Figure 3.2-1(f)).

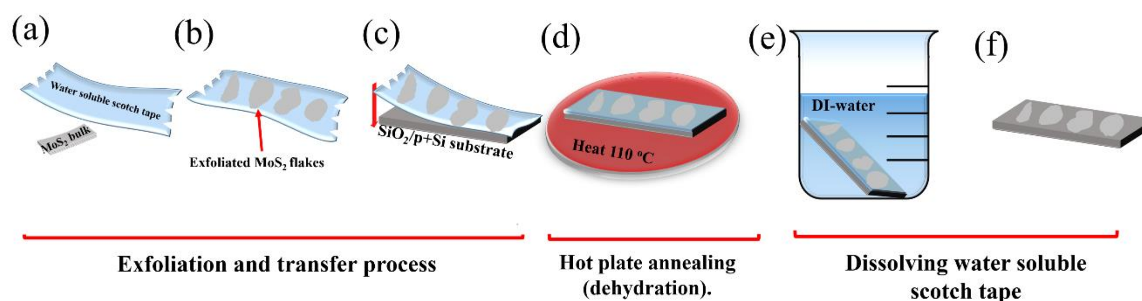

Figure 3.2-1. Modified mechanical exfoliation procedure.

MoS_2 flakes up to a few square millimeters were transferred (Figure 3.2-2) using the dissolving tape method, which is significantly larger (> 40×) in the area compared to transferred layers using the conventional exfoliation approach (inset of Figure 3.2-2). AFM is used to characterize the quality of the transferred MoS_2 films with both methods. The results reveal microcracks and large thickness variations on the surface of MoS_2 transferred by the conventional exfoliation method (Figure 3.2-3 (a)). In contrast, the transferred MoS_2 films with the modified dissolving tape have a relatively smooth uniform surface with rms = 0.5 nm (Figure 3.2-3 (b)).

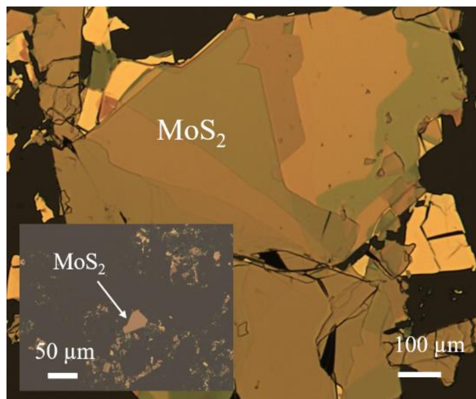

Figure 3.2-2: Optical micrograph of exfoliated MoS_2 flakes on a SiO_2 substrate, transferred by the modified method using a dissolvable adhesive. The inset shows the transferred MoS_2 flakes by the conventional method.

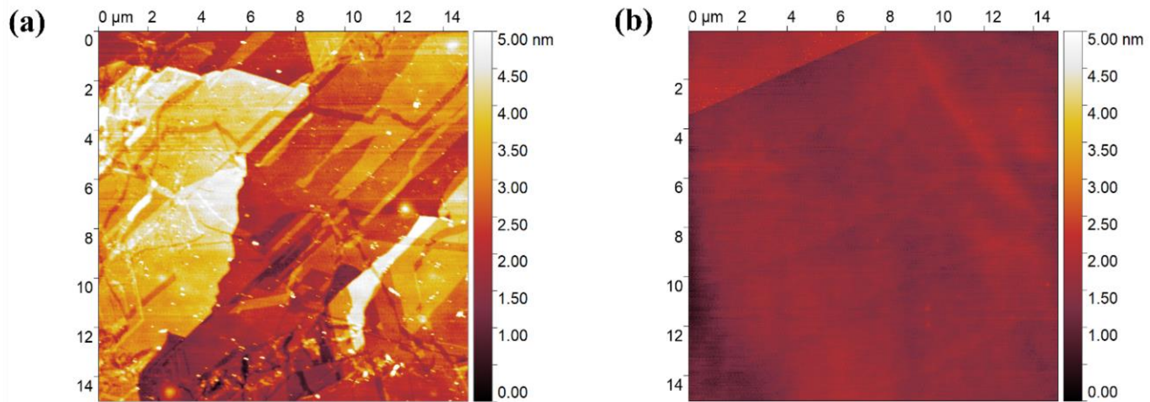

Figure 3.2-3: The AFM images of transferred MoS_2 flakes on a SiO_2 substrate using (a) conventional exfoliation and (b) modified exfoliation method.

The modified dissolving tape transfer process is further studied by investigating the effect of DI water rinse on the MoS_2 film. Raman spectroscopy was used to check for potential oxidation of the semiconductor, a possible degradation mechanism during DI water rinse reported by other groups [30, 109]. Oxidation of the MoS_2 flakes creates a lattice distortion, which can be detected by a shift and the intensity reduction of the E^1_{2g} and A_{1g} peaks. These Raman results showed no measurable variation to indicate oxidation of the MoS_2 film after the dissolving tape transfer process (Figure 3.2-4).

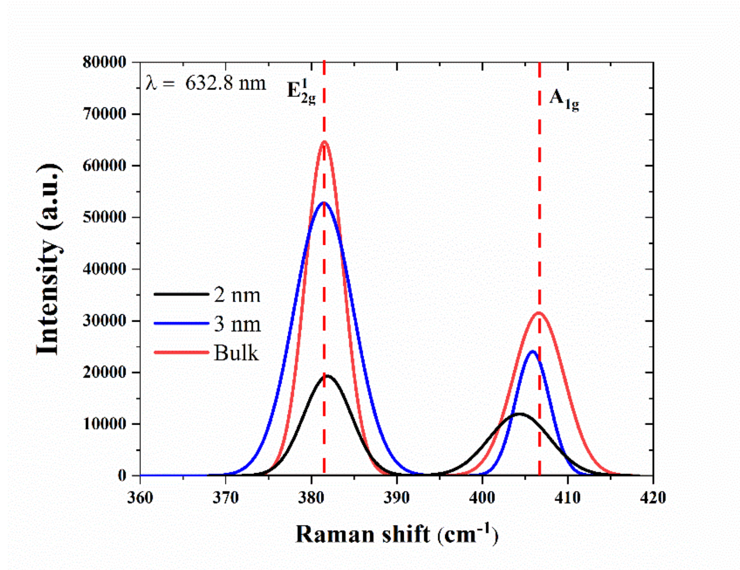

Figure 3.2-4: Raman spectroscopy of MoS_2 films with different thicknesses.

3.3 MoS_2 device array fabrication

After transferring the MoS_2 layer onto the substrate, an array of individual square islands, 40 µm × 40 µm, was patterned by conventional photolithography and dry etched in an SF_6/O_2 plasma to define the active regions of an array of devices. The Phantom II Reactive-ion Etching system was used for the dry etching process. The plasma is typically applied for 60 sec for the patterning process.

Subsequently, top electrode contacts were patterned on the islands to complete the bottom-gate transistor devices. For this, the Intelvac E-beam evaporator was utilized. Previous work has shown that low work-function metals such as Ti and Sc lead to a higher current than high work-function metals (e.g., Au) [71] due to a lower Schottky barrier (The effective Schottky barrier for Ti is around ~ 0.05 eV.). The thickness of Ti is set to 50 nm, then 100 nm Al is deposited

over the Ti layer. The lift-off of the photo-resist forms the final top electrodes by placing the sample in Remover PG at 80 °C for 1 hour. The optical micrograph and schematic of the TFT array are depicted in Figure 3.3-1. Finally, the samples are annealed in a vacuum oven at a pressure = 1×10^{-5} Torr at 120 °C for 1 hour to remove the water molecule adsorbates on the TFT backchannel surface.

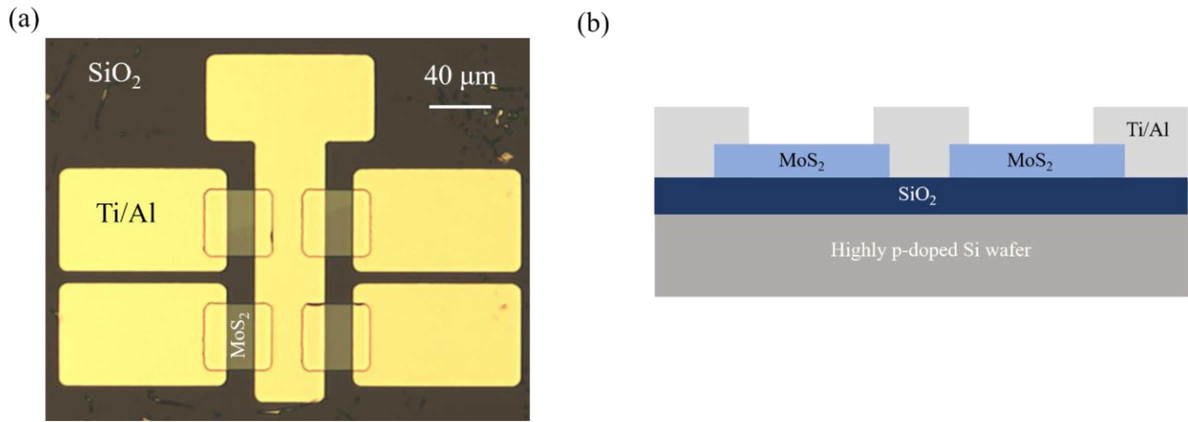

Figure 3.3-1: Optical micrograph of the MoS_2 TFT array with a resulting channel width of 40 µm and a channel length of 20 µm for each TFT. (b) Schematic of bottom-gate MoS_2 TFTs.

3.4 Dry etching process

In this project, an SF_6/O_2 dry etching process was used to thin the TMDC layers to achieve few-layer (3 – 4 layers) structures. During this process, the following chemical reactions occur:

$SF_6 + e \rightarrow SF_5 + F + e$ (1)

$O_2 + e \rightarrow 2O + e$ (2)

$SF_5 + O \rightarrow SOF_4 + F$ (3)

$MoS_2 + 6F \rightarrow MoF_4 + 2SF$ (4)

In chemical reactions of (1) and (2), the plasma will form. Then, the SF_5 and O reactions will lead to the formation of F radicals (3). Finally, F reacts with MoS_2, leading to the formation of MoF_4 and SF (4). These products are highly volatile (a boiling point of −49.0 °C) and are pumped out of the chamber without further reaction [110].

In this process, the SF_6 and O_2 gases flow rates were 10 sccm and 20 sccm, respectively, with a plasma power of 75 W and a chamber pressure of 150 mTorr. To define the MoS_2 film thickness and the etch rate of the process, AFM measurements were done before and after the dry etching process for plasma exposure durations of 8 s to 32 s (Figure 3.4-1). The thickness variation as a function of etching duration is plotted in Figure 3.4-2, indicating that the etch rate is ~2.6 nm/s (~4 layers/s). Raman spectroscopy was used to verify the layer thicknesses by referencing the frequency difference between the E^1_{2g} and A_{1g} peaks to the number of MoS_2 layers. The reference bulk MoS_2 (thickness = 90 nm) shows a frequency difference of about 26 cm^{-1}, which is in agreement with a previous report [19] (Figure 3.2-4). The frequency differences for the 3 nm and 2 nm are 24.4 cm^{-1} and 22.5 $cm^{-1,}$ respectively, which agree with previously reported layers with similar MoS_2 thicknesses [19, 111].

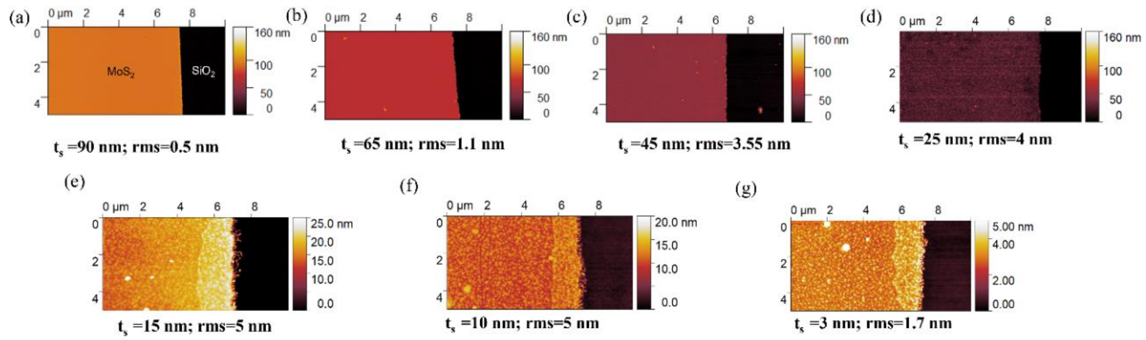

Figure 3.4-1: Atomic force microscopy images of (a) As-transferred MoS_2 film. (b) to (g) are AFM images after dry etching for 8 s, 16 s, 24 s, 26s, 28s, and 32 s, respectively. The thickness and root mean square (rms) of the MoS_2 film at each step are added under each image.

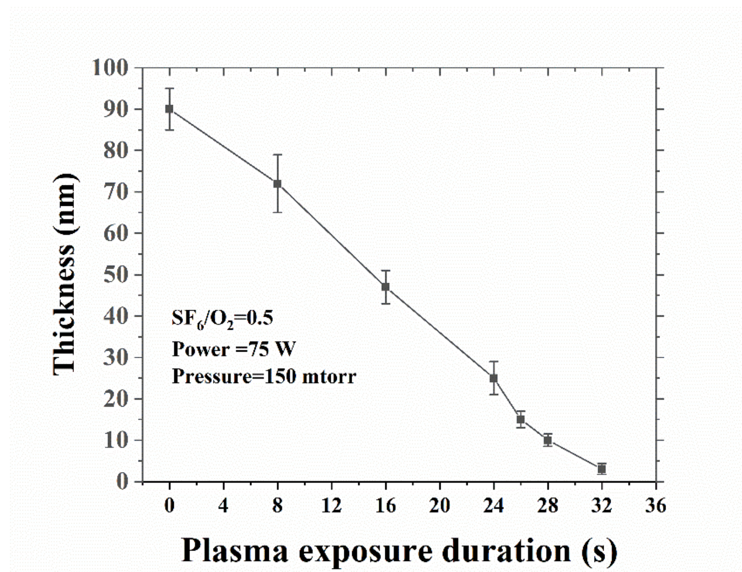

Figure 3.4-2: Thickness variations of multiple MoS_2 at different plasma exposure duration.

3.5 Conclusion

In summary, a novel two-step mechanical exfoliation and dry-etching process were used to transfer multilayer and control the thickness of MoS_2 films. The technique allows nearly all transferred material to be utilized in fabricating multiple electronic devices over a large area. Furthermore, this approach alleviates the problems associated with conventional exfoliation methods by eliminating the introduction of mechanical micro-cracking of the MoS_2 during the transfer process and increasing the transferred area by about 40×. However, the major limitation of this process is the size of the exfoliated source material used in the transfer. An SF_6/O_2 dry etching process with etch rate of ~2.6 nm/s (~4 layers/s) is used to reduce the thickness of transferred TMDC films to a few-layer structure (3-4 layers), which is confirmed by the Raman spectroscopy. As a result, a process for fabricating multilayer and few-layer MoS_2 TFT arrays is developed.

Chapter 4
Effect of large-area exfoliation and etching on the electrical behavior of transition-metal dichalcogenide field-effect transistor arrays

4.1 Introduction

In this chapter, the effect of the device processing on the electrical performance and stability of multi- and few-layer TMDC-based transistors was investigated using a two-step mechanical exfoliation and etching approach of molybdenum disulfide (MoS_2) as the active semiconductor. In Chapter 3, it is shown that this methodology enables large-area transfer and thinning for the fabrication of few-layer TFT arrays from a single large-area MoS_2 flake. In this chapter, device parameters were extracted using current-voltage and gate-bias-stress measurements to determine the effect of the process on the interface, bulk defects, and backchannel surface states on the performance of the device. The resulting analysis provides an additional understanding of the effects of device processing on the operation and performance parameters of TDMC field-effect transistors for next-generation electronic memory devices.

4.2 Experimental

Bottom-gate, top-contact MoS_2 TFT arrays were fabricated using the soluble tape method and the dry etching process, as discussed in Chapter 3. The electrical performance of the MoS_2 TFTs was measured before and after the dry etching process. Device parameters were extracted

from current-voltage (I-V) characteristics performed in a vacuum of 1×10^{-5} Torr, under dc- and pulsed-gate (30 ms pulses) voltage operation using a pair of Keithley 2400 source meters.

The chemical composition of MoS_2 thin film, from surface to bulk, was characterized using X-ray photoelectron spectroscopy (XPS) by Thermo-VG Scientific ESCALab 250 Microprobe equipped with a monochromatic Al Kalpha X-ray source (1486.6 eV).

4.3 Results and Discussion

4.3.1 TFT configurations

For this investigation, two configurations are studied: (a) the plasma etching process is done before the drain and source deposition, and (b) the plasma etching process is done after the drain and source deposition (Figure 4.3-1 (a) and (b)). Figure 4.3-1 (c) illustrates the I-V characteristics of these configurations. It is observed configuration (a) is almost shorted, while configuration (b) shows a field effect behavior. The reason might be the effect of the plasma etching process, roughening, and oxidizing the backchannel surface of the MoS_2 film (This issue will further elaborate). This issue may cause a short between the drain and source, while in configuration (b) drain and source are not in direct contact with the plasma exposed surface. Hence, configuration (b) is used for investigating the effect of TMDC bulk thickness on the electrical performance of TFTs.

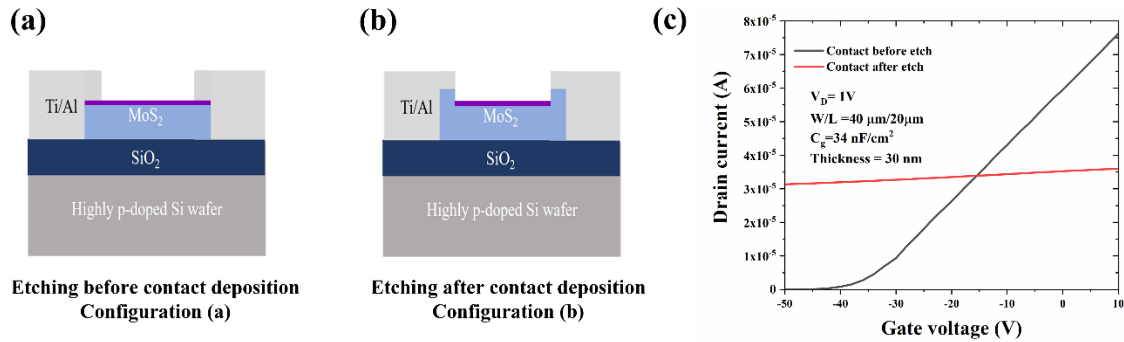

Figure 4.3-1: Cross-sectional schematic of MoS_2 TFT with deposited drain and source (a) after and (b) before the plasma etching process. (c) Drain current vs. gate voltage characteristics for the TFTs.

4.3.2 MoS_2 bulk thickness effect

The I-V transfer characteristic of an as-fabricated MoS_2 (thickness of 90 nm) is shown in Figure 4.3-2, showing n-channel depletion-mode operation [9, 112] with a large threshold voltage (V_{th}) of -52 V. The high threshold may originate from trapped charges: (i) within the MoS_2 layers, which are due to intrinsic defects; (ii) at the MoS_2 backchannel surface, which can be caused by surface defects or environmental contaminants; or (iii) at the semiconductor-dielectric interface due to the exfoliation process.

To resolve the origin of this large V_{th}, the device I-V characteristics were measured as a function of MoS_2 bulk thickness (t_s) after each etching step.

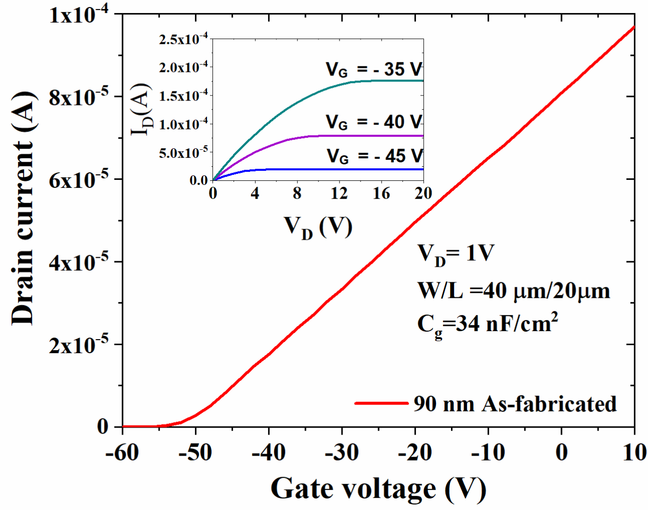

Figure 4.3-2: Drain current vs. gate voltage characteristics for a typical transferred and as-fabricated TFT with a MoS_2 bulk thickness = 90 nm. The inset shows the output characteristics of the MoS_2 TFT.

The V_{th} evolution versus thickness, t_s, is shown in Figure 4.3-3. V_{th} improved by +17 V when the semiconductor thickness was etched from 90 nm to 15 nm. As t_s decreased from 15 nm to 3 nm, the V_{th} improved further, shifting an additional +22 V to -11 V. The reduction of t_s below 15 nm caused an abrupt increase in the rate of the V_{th} shift from ~ 0.2 V/nm (for t_s>15nm) to ~1.8 V/nm (for t_s<15 nm). To investigate the effect of the MoS_2 bulk thickness on the electrical performance, the threshold voltage equation can be related to the bulk and interface trap densities for thin film transistors [26]:

$$\mathbf{V_{th}} \approx \frac{qN_t t_s (E_F - E_i)_{threshold}}{C_g} - \frac{Q_f}{C_g} + \frac{qD_t (E_F - E_i)_{threshold}}{C_g} - \frac{q(D_D - D_A)}{C_g} + \Phi_{ms}, \quad \text{(Equation 4-1)}$$

where N_t is the bulk trap density, q is the electron charge, $(E_F - E_i)_{threshold}$ is the energy difference between the Fermi and the midgap energy level at the threshold, assumed to be equal to half of bandgap energy. Q_f is the effective charge in the depletion region, C_g is the gate capacitance, D_t is the MoS_2/SiO_2 interface trap density, D_D and D_A are the donor and acceptor channel doping, respectively, and Φ_{ms} is the metal-semiconductor work function difference [26].

To further understand the source of the V_{th} variation, multiple identical devices were measured, and the absolute parameter values for threshold voltage, ON/OFF current ratio, field-effect mobility, and subthreshold swing as a function of MoS_2 bulk thickness were extracted. The results are plotted in Appendix A, Figure S 1.

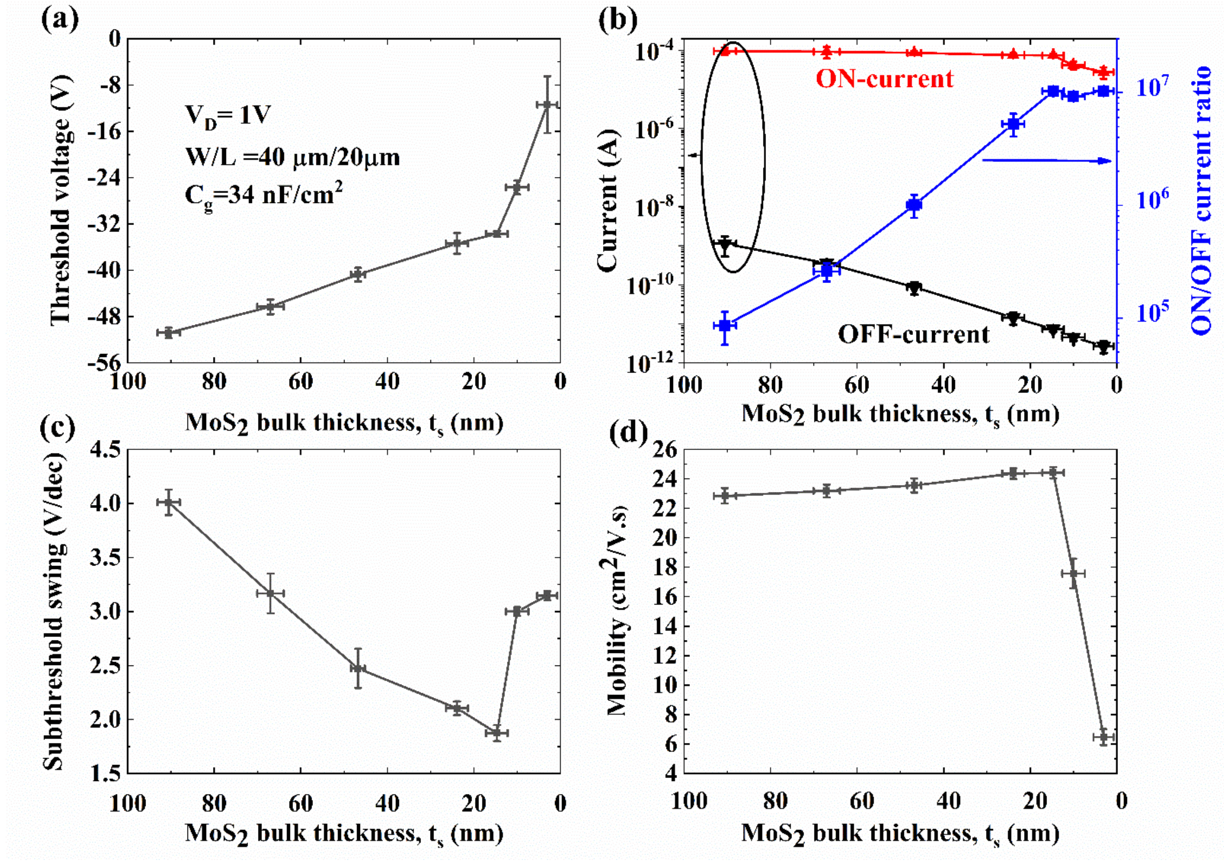

Figure 4.3-3: The electrical characteristics of MoS_2 TFTs are plotted for different t_s. (a) the threshold voltage of MoS_2 TFTs as a function of semiconductor thickness, (b) TFT ON and OFF current variations vs. t_s, the blue square symbols show the ON/OFF-current ratio variations, (c) the subthreshold swing vs. t_s, and (d) the field-effect mobility vs. t_s.

Figure 4.3-3 shows the average value of several device parameters with their standard deviations and their dependence on the TMDC thickness. The standard deviation of these

parameters are less than 10%, indicating the reproducibility of the process. This reproducibility demonstrates the robustness of the fabrication process for single MoS_2 flake. As the MoS_2 layer thickness decreased from 90 nm to 15 nm, the TFT ON/OFF current ratio increased nearly three orders of magnitude due to a decrease in the leakage current with relatively small changes to the ON-current (Figure 4.3-3 (b)). Further reducing t_s (from 15 nm to 3 nm) decreases the ON-current by 60 %, correlated to a decrease in the field-effect mobility.

The origin of the reduced leakage current may be due to the reduction of bulk trap states in the MoS_2. Therefore, the trap state density was further investigated through the extraction of the subthreshold swing (*S*) (Figure 4.3-3 (c)). In this case, the trap density can be extracted using the following:

$$1/S = \log_{10} e \times \left(\frac{C_g}{q^2\left(\frac{k_B T}{q}\right)(N_t t_s + D_t)}\right), \qquad \textbf{(Equation 4-2)}$$

where k_B is Boltzmann's constant, and T is the absolute temperature [26, 113]. The bulk trap density for each thickness can be extracted from this equation. XPS measurements did not show compositional variation at the MoS_2/SiO_2 interface (the result will be explained later); therefore, D_t is considered constant at about $\sim 6\times10^{12}$ $cm^{-2}eV^{-1}$, according to the previously reported values [112]. The results show that when t_s is reduced from 90 nm to 15 nm, *S* decreases by ~ 2.1 V/dec, and N_t reduces from $\sim 9.11\times10^{17}$ $cm^{-3}eV^{-1}$ to $\sim 4.76\times10^{17}$ $cm^{-3}eV^{-1}$, which is correlated to ΔV_{th} ~ 21 V (extracted from Equation 1.5-4), in agreement with Figure 4.3-3. Furthermore, the result suggests the concentration of bulk trap states in the TMDC layers may be responsible for the leakage current, and this concentration decreased as a function of

the MoS_2 thicknesses. This observation agrees with a previous report [92], which investigated the effect of inducing traps in the semiconductor bulk of TMDC-based TFTs.

As the MoS_2 thickness is reduced during etching, the $N_t t_s$ product in Equation 2 becomes small compared to D_t. As t_s decreases from 15 nm to 3 nm, D_t may be extracted from Equation 2 by measuring the subthreshold swing of the device. Using this approach, D_t was found to increase from 6×10^{12} $cm^{-2}eV^{-1}$ to ~1.2×10^{13} $cm^{-2}eV^{-1}$. The change in D_t is expected as the MoS_2 layer is reduced due to the increasing surface-to-volume ratio of the structure. The increase in D_t suggests the etching process is introducing backchannel surface states due to the etching process. The initial removal of the MoS_2 diminishes the number of bulk defects within the MoS_2 layer until the structure becomes a few layers thick. At $t_s < 15$ nm, the backchannel surface states dominate the device behavior, and the removal of bulk defects may be offset by surface states introduced by the etching due to the proximity of the backchannel surface defects to the active TFT channel region.

Exploring this hypothesis further, the impact of the TMDC thickness on the carrier field-effect mobility (μ_e) of the TFT operating in the linear regime was analyzed using the relationship:

$$\boldsymbol{\mu_e} = \left[\frac{\partial I_{ds}}{\partial V_{gs}}\right] \times \left[\frac{L}{C_g V_{ds} W}\right], \quad \textbf{(Equation 4-3)}$$

at V_{ds}=1 V. As can be seen in Figure 4.3-3 (d), reducing t_s from 90 nm to 15 nm leaves μ_e nearly constant. The contact resistance, R_s, was also extracted using the Y function method to determine the effect R_s has on the parameter extraction. These calculations show that the effect on the extracted carrier mobility due to the contact resistance was less than 15% for the measured TFTs. A similar conclusion may be made from the output characteristic of the TFT,

showing the ohmic behavior of the I-V characteristics at low drain voltages (inset of Figure 4.3-2).

An interesting outcome from the I-V measurements was the positive V_{th} shift as the MoS_2 thickness was reduced due to the removal of bulk defects in the TMDC for multilayer MoS_2 structures. However, when t_s is reduced to less than 15 nm, the threshold voltage continues to improve, but a significant drop in the field effect mobility was observed.

The positive shift in the V_{th} for t_s< 15 nm shows a variation in the field effect due to a negatively charged layer on the backchannel surface. To investigate this possibility, surface analysis on the dry-etched samples was performed using XPS, revealing a 5 nm thick layer having oxygen incorporation in the MoS_2 film (Figure 4.3-4). The fluorine peak was not observed in the measurement. This finding suggests that the MoS_2/SiO_2 interface is not affected during the dry etching process. Moreover, the oxygen incorporation by forming the MoO_3 on the backchannel surface is responsible for the negative charge, consistent with previous reports on the p-type doping in exfoliated or CVD MoS_2 with oxygen [77, 78]. By reducing t_s to less than 15 nm, the oxygen-doped layer and the accumulation region become closer, leading to a positive shift in the threshold voltage (Figure 4.3-4 a,b). The oxygen doping concentration in the channel layer is estimated to be $\sim 1\times 10^{19}$ cm $^{-3}$, extracted from the V_{th} variation for t_s <15 nm (Equation 1.5-4), in agreement with the doping concentration value reported in [114]

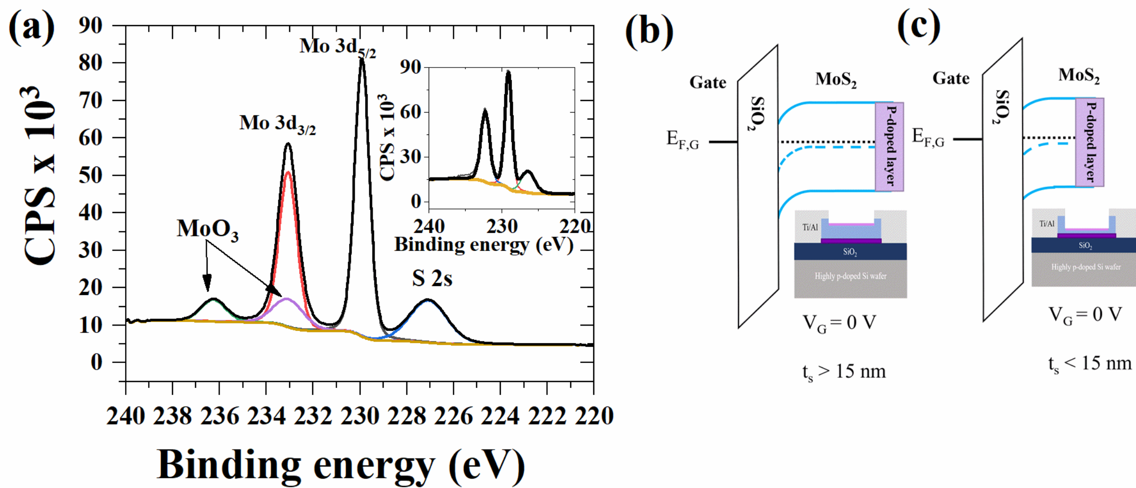

Figure 4.3-4: (a) XPS surface analysis of a dry etched MoS_2 film. The inset shows the XPS results of the layer of the unexposed surface. (b) and (c) show the energy band diagram and cross-section schematics of dry-etched MoS_2 TFT with thicknesses above and below 15 nm, respectively.

The change in the carrier transport was likely due to carrier scattering when the dry-etched layer moved closer to the accumulation layer of the active channel region as the MoS_2 layer was thinned. This tradeoff in the electrical behavior and carrier transport characteristics may be specific to thinner TMDC structures since the proximity of the backchannel will begin to encroach into the accumulation layer of the TFT channel region. Past reports [34, 115] have shown the transport and electrical characteristics degradation for few- and monolayer devices where the backchannel surface defects dominate the device operation. The correlation between the semiconductor thickness and the field-effect mobility provides additional insight into the

TMDC materials transport mechanism, where the backchannel surface quality can play a significant role in the transistor operation.

To quantify this surface effect on the carrier transport, the backchannel surface morphology was measured. The root mean square (rms) surface roughness of the as-transferred MoS_2 film was 0.5 nm, while this roughness increased to 5 nm after etching 75 nm of the MoS_2. Further etching resulted in a slight smoothening of the surface with an rms roughness of ~1.7 nm. This roughness variation has been shown to be due to the redeposition of the sputtered MoS_2 on the surface, creating a non-uniform distribution of peaks and valleys on the surface for multilayer structures [28]. Once the peaks and valleys form, the peaks are removed more quickly compared to the valleys of the MoS_2 surface that has been observed in the previous report creating a smoother surface [116]. Nevertheless, the final roughness of 1.7 nm is 3× greater than the original as-transferred surface roughness and is nearly equal in magnitude to the overall thickness of the TMDC layer. Given the proximity of this surface to the accumulation layer and the thickness of the overall channel layer, the observed field-effect mobility degradation may be due to carrier scattering from the backchannel surface.

Electrical stability measurements of the TFT structures correlate with the measured device characteristics. It was found that reducing the MoS_2 bulk thickness from 65 nm to 15 nm improved the electrical stability of the TFTs operating under constant dc bias (Figure S 2). In agreement with the extracted parameters from the I-V characteristics, the electrical stability begins to degrade as the MoS_2 thickness is brought below 15 nm. The improvement in the electrical stability with decreasing t_s from 65 nm to 15 nm supports the hypothesis that the electrical characteristics are dominated by bulk defects that affect the leakage current and

carrier transport. As the bulk defect density is reduced, the effect of surface states becomes dominant as the TFT backchannel moves closer to the active region of the device. The degradation in the electrical stability with decreasing t_s from 15 nm to 2 nm suggests the observed increase in trap states within the MoS_2 is due to surface states that dominate the device's active region. This conclusion is further supported by the change in V_{th} and the reduced field effect mobility shown in Figure 4.3-3 c and d. Extracting the trap activation energy (E_a) from the electrical stability measurements also shows that E_a remains almost constant at 0.33 eV down to t_s = 15 nm. This extracted E_a value can be attributed to the donor-like sulfur vacancy traps in MoS_2 bulk, reported in computational investigations by Li *et al.*[117]. On the other hand, at t_s = 2 nm, E_a increases to $\sim$ 0.45 eV, representing a transition in the dominant defect mechanism for the thinner layers, which is in agreement with the effect of the backchannel surface states discussed in the previous sections.

This effect may be used to tune the threshold voltage for TMDC-based memory devices (along with backchannel passivation with dielectric materials such as PMMA and SiN_x) to create memory arrays having unique electrical characteristics for memory encryption.

4.4 Conclusion

In summary, the electrical characteristics of the fabricated devices showed the existence of trap states within the MoS_2 bulk and backchannel surface traps. It was observed that the impact of MoS_2 bulk traps is more dominant for multilayer TMDC devices having thicknesses greater than 15 nm. The MoS_2 bulk trap density can be reduced using a dry etching process, improving the electrical performance and stability of the transistors.

On the other hand, the etching process produced surface states on the TFT backchannel that altered the electrical stability and the carrier transport for MoS_2 thicknesses less than 15 nm. This degradation resulted from the proximity of the defects on the etched backchannel surface to the active device region. In addition, the presented transfer-and-thinning process was found to provide a means to control the electrical performance and stability of the TDMC-based transistors that may be a useful approach for further developing nonvolatile memories based on multi- and few-layer TDMC materials.

Chapter 5

Effect of hydrogen-containing passivation layers on the electrical performance of transition-metal dichalcogenide field-effect transistors

5.1 Introduction

In the last chapter, it is shown that bulk trap states for multilayer TMDC devices dominate the electrical behavior of the TFTs. At the same time, few-layer structures are affected mainly by the backchannel surface states. Therefore, backchannel encapsulation layers can be utilized to mitigate the impact of surface defects on the TFT's electrical performance.

This chapter examined the impact of hydrogen-contained passivation layers and the effect of hydrogen exposure on TMDC TFTs with devices with varying TMDC thicknesses. A SiO_x thin film H-diffusion barrier was also used to determine the efficacy of bilayer dielectric layers on molybdenum disulfide (MoS_2)-based transistors. Device parameters were extracted using current-voltage and dc gate-bias measurements as a function of time to determine the effect of passivation and plasma exposure on the electrical stability of the device. In addition, Time-of-flight secondary ion mass spectroscopy was used to determine the hydrogen depth profile in the MoS_2 layer. The resulting analysis provides a better understanding of how the passivation process on 2D electronic materials affects the electrical performance of TMDC field-effect transistors for next-generation nonvolatile memory devices.

5.2 Experimental

5.2.1 Backchannel passivation process

MoS_2 TFTs were passivated using SiN_x (100 nm thickness) and SiO_x (50 nm thickness), and bilayers of SiO_x/SiN_x (50 nm/100 nm thicknesses). PECVD is used to deposit the SiN_x (with SiH_4 (5 sccm flow rate), and NH_3 (100 sccm flow rate)) and SiO_x (with SiH_4 flow of 5 sccm and NO_2 flow of 100 sccm) layers deposited at a plasma power = 25 W, chamber pressure = 1000 mTorr, and a temperature = 300 ºC. Finally, the passivation layers were patterned using a dry etching process with CF_4 and O_2 precursor gases. The bilayer passivation layers were used to investigate the effect of SiO_x as a hydrogen diffusion barrier, in which an electron beam is used to deposit the SiO_x layer. The schematic of the TFT is depicted in Figure 5.2-1.

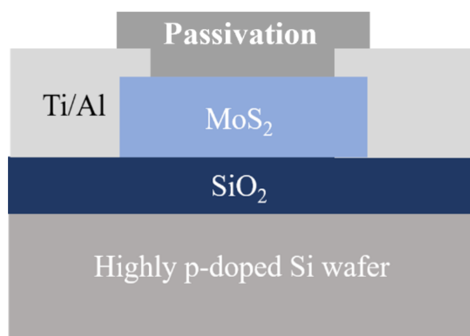

Figure 5.2-1: Schematic of bottom-gate MoS_2 TFTs with a passivation layer

5.2.2 Chemical Analysis and Electrical Characterization

Time-of-flight secondary ion mass spectroscopy (TOF-SIMS) was used to confirm the incorporation of hydrogen atoms in the MoS_2 for structures that were pristine and exposed to H_2 during the deposition of the SiN_x. In addition, the effects of the SiO_x passivation using PECVD and electron-beam deposition were used to determine the extent of hydrogen incorporation due to the precursor gas during the PECVD process. TOF-SIMS was also used to characterize the effectiveness of SiO_x as a hydrogen diffusion barrier using various SiN_x/SiO_x bilayer passivation structures. The data is acquired using Bi^+ (30 kV) as the analysis ion source and Cs (1 kV) as the sputtering ion source.

The electrical characteristics were determined using I-V characterization of TFT structures with different backchannel conditions, including bare, hydrogen exposed, PECVD SiN_x passivated, PECVD SiO_x passivated, electron beam SiO_x passivated, and bilayer passivated with H-diffusion barriers. The I-V measurements were performed under pulsed (duty cycle = 4%) under dark conditions within an evacuated chamber at a pressure of 1×10^{-5} Torr.

5.3 Results and Discussion

The effect of the deposition of hydrogen-containing SiN_x passivation layers on the electrical parameters of the transistors of different TMDC layer thicknesses (t_s) is shown in Figure 5.3-1. The electrical performance parameters for multiple bare MoS_2 TFTs with different MoS_2 thicknesses are shown, comparing reference devices (black curves) with 100 nm SiN_x-passivated devices (red curves). In Figure 5.3-1 (a), the threshold voltage (V_{th}) does

not change for MoS_2 thicknesses between 25 nm to 15 nm. Unexpectedly, thinner MoS_2 layers (t_s < 15 nm) were found to exhibit a negative V_{th} shift compared to the reference TFTs; an increase from 26 V to 43 V was measured for t_s decreasing from 10 nm to 3 nm. The V_{th} shift sources from a change in the trap density, possibly due to the formation of states in the MoS_2 layer during the SiN_x deposition process. The ON/Off current ratio, subthreshold swing, and field effect mobility variations of SiNx passivated TFTs with different ts were measured to explore this possibility.

Figure 5.3-1 (b) shows that the ON/Off current ratio does not change notably after the SiN_x passivation for t_s > 15 nm. However, the ON/OFF current ratio for t_s < 15 nm degrades from 10^7 (bare TFT - reference) to 10^2 after the SiN_x passivation. This degradation is mainly due to the off-current increase from 10^{-12} A to about 10^{-7} A (see Appendix B, Figure S 3) because of a rise in the off-state leakage current, pointing to a trap density variation.

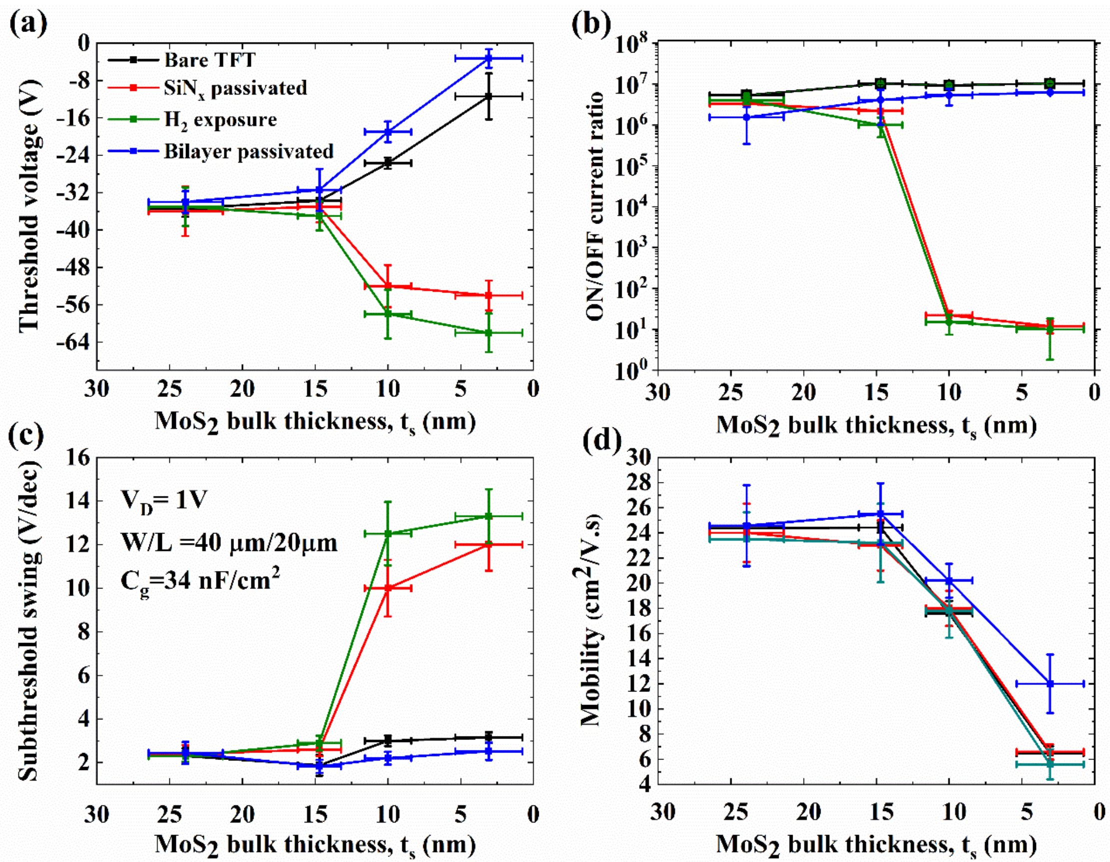

Figure 5.3-1*:* The electrical characteristics of MoS_2 TFTs in bare condition (black curve), after passivation with 100 nm SiN_x (red curve), after exposure to H_2 plasma (green curve), and after passivation with SiN_x/SiO_x bilayer dielectric (blue curve) are plotted for different t_s. (a) the threshold voltage of MoS_2 TFTs as a function of semiconductor thickness, (b) TFT ON/OFF-current ratio variations vs. t_s, (c) the subthreshold swing vs. t_s, and (d) the field-effect mobility vs. t_s.

Therefore, the trap density variation is further investigated through the extraction of the subthreshold swing (S) (Figure 5.3-1 (c)). For $t_s > 15$ nm, S remains constant at around 2.2 V/dec after the SiN_x passivation. For thinner TMDC layers, S is found to increase for devices having $t_s < 15$ nm after the SiN_x passivation. The increase might be due to the bulk density variation. This variation can be extracted using:

$$1/S = log_{10}^{e} \times \left(\frac{C_g}{q^2\left(\frac{K_B T}{q}\right)(N_t t_s + D_t)}\right) \quad \textbf{(Equation 5-1)}$$

After the passivation process, the total trap density ($N_t t_s + D_t$) for $t_s < 15$ nm increases by about ~4×; however, the trap density is constant for $t_s > 15$ nm. This increase may be due to the passivation layer moving closer to the active accumulation layer of the TFT for the thinner samples.

The impact of SiN_x passivation on the carrier field-effect mobility of the TFT operating in the linear regime was determined using:

$$\mu_e = \left[\frac{\partial I_{ds}}{\partial V_{gs}}\right] \times \left[\frac{L}{C_g V_{ds} W}\right] \quad \textbf{(Equation 5-2)}$$

As can be seen in Figure 5.3-1 (d), the passivation of TFTs for all thicknesses leaves μ_e nearly constant, indicating the carrier transport was not measurably affected by the passivation process.

The impact of bulk defects in the SiN_x is investigated using different thicknesses of the SiN_X passivation layer and the effect of an annealing process at 300 ºC in a vacuum. The results indicate SiN_x bulk traps and the annealing process do not impact the electrical performance of the TFTs. The possibility of MoS_2 layer degradation due to contamination by the hydrogen

plasma during the SiN_x deposition was also considered. Figure 5.3-1 shows the changes in the device parameters for bare MoS_2 TFTs exposed to hydrogen plasma using the conditions for the SiN_x deposition (green curve). The electrical performance variations after H_2 exposure are similar to the SiN_x passivated TFTs, suggesting hydrogen incorporation into the MoS_2 channel might cause the device performance variations after the SiN_x passivation. The SIMS measurement confirms the existence of hydrogen in the MoS_2 layer (this measurement will be discussed later).

The incorporation of the hydrogen in the MoS_2 layers can be investigated by extracting the channel doping concentration (D_D) using:

$$\mathbf{V_{th}} \approx \frac{\mathbf{qN_t t_s (E_F - E_i)_{threshold}}}{\mathbf{C_g}} - \frac{\mathbf{Q_f}}{\mathbf{C_g}} + \frac{\mathbf{qD_t (E_F - E_i)_{threshold}}}{\mathbf{C_g}} - \frac{\mathbf{q(D_D - D_A)}}{\mathbf{C_g}} + \mathbf{\Phi_{ms}} \qquad \textbf{(Equation 5-3)}$$

The threshold voltage and total trap density variations ($N_t t_s + D_t$) for $t_s < 15$ nm are used to extract the n-type channel doping enhancement after the SiN_x passivation. The doping concentration increases from ~2×10^{12} cm^{-2} to ~1.3×10^{13} cm^{-2}, which is close to the degenerate limit in MoS_2, reported by Fang et al. [118]. In addition, the channel doping enhancement is in accord with the previous computational study, showing the n-type doping after the hydrogen incorporation in the MoS_2 layer [91]. However, TFTs with $t_s > 15$ nm do not show doping variation due to the limited diffusion length of hydrogen into the MoS_2 layer. SIMS measurements show hydrogen atoms diffuse about ~10 nm into the MoS_2 layer.

To further investigate the effect of hydrogen incorporation into the TMDC layers, SiO_x passivation layers were incorporated using PECVD with hydrogen-containing precursors. A similar trend to H_2 exposed and SiN_x passivated TFTs were observed. At the same time, the

electron beam deposited SiO_x did not cause electrical performance degradation due to the reduction of H incorporation and plasma damage in the deposition process (see Appendix B, Figure S 4). Thus, the electron beam deposited SiO_x layer can be used as a hydrogen diffusion barrier [87].

The electron beam deposited SiO_x was used to mitigate the hydrogen diffusion problem during the SiN_x deposition. The effectiveness was tested using a bilayer consisting of a 50 nm SiO_x layer deposited directly on the MoS_2 surface, followed by a 100 nm thick SiN_x film. The bilayer passivation had a minor impact on the V_{th} of TFTs with t_s >15; however, for t_s < 15 nm, the V_{th} shows a positive shift of ~6 V after the bilayer passivation (Figure 5.3-1 (a)). Furthermore, the TFTs show a high ON/OFF current ratio, about 10^7, close to the values found for the bare TFTs ((b)). For t_s < 15 nm, *S* decreases from 3.2 V/dec to about 2.2 V/dec (Figure 5.3-1 (c)), attributed to the reduction of the trap density from 1.1×10^{13} $cm^{-2}eV^{-1}$ to 0.78×10^{13} $cm^{-2}eV^{-1}$ (t_s = 3 nm), equivalent to a ΔV_{th} = 8 V (calculated from Equation 1.5-4), which is in agreement by the electrical measurements. After the bilayer passivation, the field-effect mobility was also improved for t_s < 15 nm. Previous studies have suggested the plasma etching of TMDC layers adversely affected the carrier transport in the TFTs due to backchannel surface defects, creating a higher probability for carrier scattering [29, 30]. However, the passivated thinner TFTs reduce this scattering effect only if hydrogen contamination is minimized during the passivation process. Thus the bilayer passivated TFTs show higher effective mobility. Furthermore, the electrical performance improvement by the trap density reduction indicates

the effectiveness of the bilayer dielectric for passivating the backchannel surface and blocking hydrogen diffusion during the passivation layer deposition.

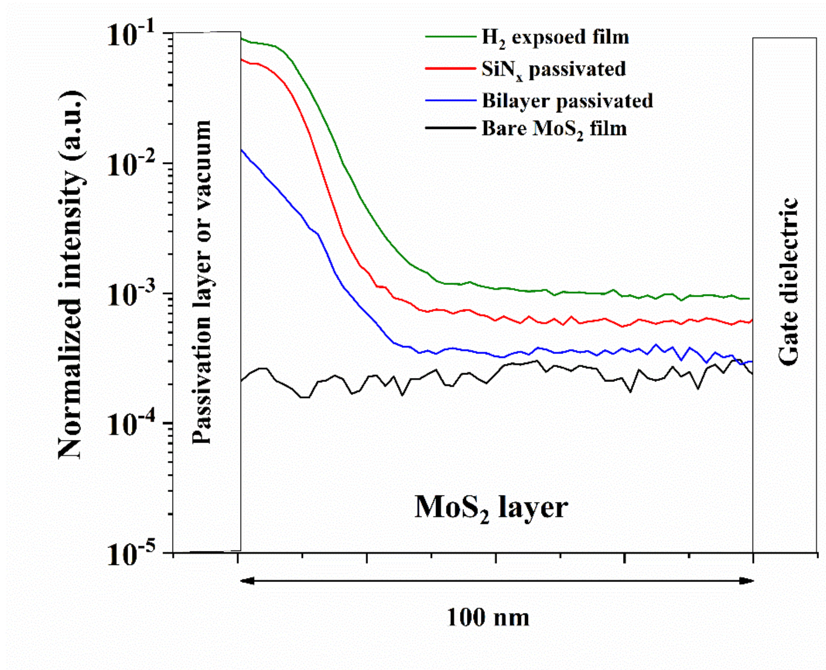

Figure 5.3-2: Secondary ion mass spectroscopy results of a MoS_2 film, (normalized to the hydrogen signal intensity), after exposing to H_2 plasma (olive curve), after passivating with 100 nm SiN_x (red curve), after passivating with bilayer SiNx/SiO_x (blue curve), and at bare condition (black curve). TOF-SIMS data are normalized to the total ion counts.

Exploring this hypothesis further, the impact of the passivation layer and its effect on the hydrogen concentration in the MoS_2 semiconductor was analyzed using TOF-SIMS characterization to determine the hydrogen depth profile in the TMDC layer for different passivation layers (Figure 5.3-2). The electron-beam deposited SiO_x layer in the bilayer

passivation was an effective H diffusion barrier due to its small hydrogen diffusion coefficient [119]. The result shows a ~ 6× reduction in the H signal intensity at the surface compared to the SiN_x passivated sample. This finding agrees with ~ 5× decrease in the H-doping concentration, extracted using Equation 1.5-4. The TOF-SIMS measurements also verified H incorporation in the PECVD SiO_x deposited film, while the H content in the electron beam deposited film is negligible.

These results show the H content in the SiH_4 precursor gas for depositing SiO_x and SiH_4 and NH_3 for depositing SiN_x provides the highest concentration of H within the MoS_2 layers. With an increasing H concentration, the n-type doping concentration increases, and the quality of the MoS_2 layers degrades, leading to a negative V_{th} shift and higher S, which agrees with previous computational investigations [91, 92]. However, due to the small size of the hydrogen atoms, the scattering process and the effective mobility are not affected. In addition, the existence of this doped MoS_2 layer decreases the ability of the gate electric field to deplete the channel and increase the OFF current.

Electrical stability measurements are used further to support the effect of hydrogen on the MoS_2 TFTs. The electrical stability of few-layer MoS_2 TFTs was also observed to degrade after passivating the TFT with 100 nm thick SiN_x. This degradation in the electrical stability gives more evidence of the effect of hydrogen-containing passivation layers on the degradation of the device parameters V_{th} and *S,* shown in Figure 5.3-1. In contrast, the TFTs with the bilayer dielectric showed better electrical stability (see Appendix B). These results show the efficacy of using a bilayer SiN_x/SiO_x passivation layer to stop hydrogen diffusion from SiN_x into the

MoS_2 TFTs, creating a unique approach to enhancing the electrical performance and stability of multi- and few-layer TMDC electronic devices.

5.4 Conclusion

This study explored the SiN_x passivation effect on TMDC TFTs with varying TMDC thicknesses. Hydrogen incorporation into the active region of the TMDC devices after SiN_x passivation was found to increase the trap density and change the doping, which leads to the degradation of the electrical performance and stability of TMDC devices. The impact of hydrogen contamination on the electrical performance depends on the TMDC bulk thickness due to the limited diffusion length of the hydrogen atoms. Thus, TMDC TFTs with thicknesses < 15 nm showed higher degradation in this research. This finding points to the higher sensitivity of the thin TMDC devices to the fabrication process, especially hydrogen-containing films and processes. The diffusion concentration of hydrogen atoms into the active region of the TMDC devices can be reduced by 6× times using a SiO_x barrier layer. The barrier layer, combined with SiN_x passivation, forms a bilayer coating to passivate the TFT backchannel surface and improve the electrical performance and stability of the thin TMDC devices. Utilizing a barrier layer effectively diminishes the adverse impact of hydrogen-containing backchannel passivation layers and processes. This approach may be used to develop the next generation of TMDC-based memory devices with high electrical performance and stability.

Chapter 6

Effect of backchannel surface traps on dual gating of dry-etched multilayer transition metal dichalcogenides TFTs

6.1 Introduction

The last chapter demonstrates that a proper dielectric layer can passivate the TFTs' backchannel surface and improve the electrical performance of the TMDC-based TFTs. Furthermore, this dielectric can be used as a top gate dielectric layer and form a dual gate structure. In this chapter, we investigate the effect of backchannel surface traps and TMDC bulk thickness on the electrical performance of dual-gate TMDC-based TFTs using dry-etched and pristine MoS_2 as the active semiconductor. Device parameters are extracted using current-voltage and gate-bias-stress measurements in a vacuum to determine the effect of electrostatic control of the backchannel surface traps on the performance of the device. The resulting analysis further elaborates on the role of the TMDC bulk thickness on the top gate electric field of the dual-gate field-effect transistors for next-generation electronic memory devices.

6.2 Experimental

6.2.1 The top-gate TFT fabrication process

After fabricating MoS_2 TFTs with various thicknesses using the soluble tape method and the dry etching process (Chapter 3), bilayer SiO_x (50 nm)/ SiN_x (100 nm) is used as the dielectric for fabricating the top gate configuration. Then, 100 nm Al is deposited and patterned on the

dielectrics as the top gate metal. Finally, the dielectric layer is patterned using conventional lithography and a dry etching process with CF_4 and O_2 precursor gases. The schematic and optical micrograph of the TFTs are depicted in Figure 6.2-1.

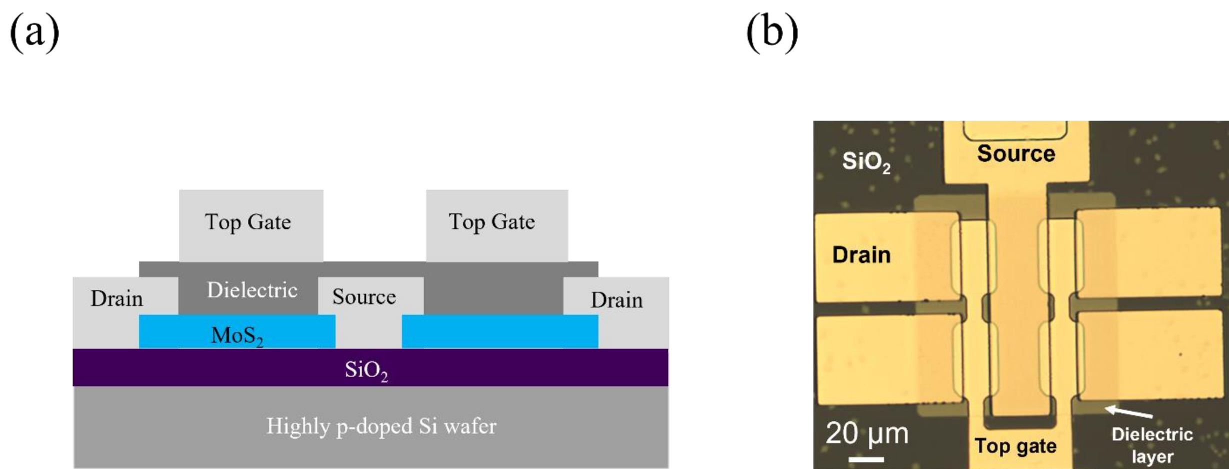

Figure 6.2-1: (a) cross-sectional schematic and (b) optical micrograph of dual-gate MoS_2 TFTs.

6.2.2 Electrical characterization

A pair of Keithley 2400 source meters is used to extract the electrical performance of the MoS_2 TFTs at different backchannel conditions from the drain current-gate voltage characteristics. The TFTs were measured in three modes: (1) top gate, (2) bottom gate, and (3) dual gate, which sweeps the bottom gate and applies constant DC bias on the top gate. The drain current was

measured under pulsed (duty cycle = 4%) in a dark evacuated chamber at a pressure of 1×10^{-5} Torr.

6.3 Results and Discussion

The electrical performance of pristine and backchannel etched MoS_2 TFTs in top-gate, and bottom-gate modes are measured (Figure 6.3-1). For the top gate (bottom gate) measurement, the bottom gate (top gate) is grounded to prevent spurious dual-gate coupling [100]. The threshold voltage (V_{th}) variations as a function of t_s are shown in Figure 6.3-1 (a). Previously we found that the root cause of the trap density variation with t_s of the bottom gate TFT is the MoS_2 bulk trap density reduction (Chapter 4); thus, a similar variation trend of the top-gate TFTs with t_s points to a similar root cause. Nevertheless, the top-gate TFTs have about 8V higher V_{th}, indicating a higher trap density top-gate TFTs relative to the bottom-gate one. Top-gate TFTs with pristine backchannel surface ($t_s \approx 25$ nm and 40 nm) are measured to understand further the source of the top gate negative V_{th} shift. The results show that the V_{th} of the pristine top-gate TFTs (green stars) and the bottom-gate TFTs with the same t_s are close. This result indicates the MoS_2/ bilayer dielectric interface traps might be the root cause of the low electrical performance of the etched top-gate TFTs. Previously, we showed that the dry etching process leads to the degradation of the MoS_2 backchannel surface (Chapter 5). To investigate the impact of the MoS_2/bilayer dielectric interface traps on the top gate TFTs, the ON/OFF current ratio, subthreshold swing, and the field effect mobility as a function of MoS_2 bulk thickness are analyzed.

Figure 6.3-1 (b) shows the ON/Off current ratio of the bottom and top-gate TFTs with various t_s. Reducing t_s from 40 nm to 3 nm increases the ON/OFF current ratio of TFTs about seven times due to the OFF current reduction by decreasing t_s; however, the top-gate TFTs have about four orders of magnitudes lower ON/OFF current ratio due to the higher OFF current leakage (Figure S 6). This increase might be due to the higher trap density of the top gate than the bottom gate structure. This effect reduces the ability of the gate electric field to deplete the channel region.

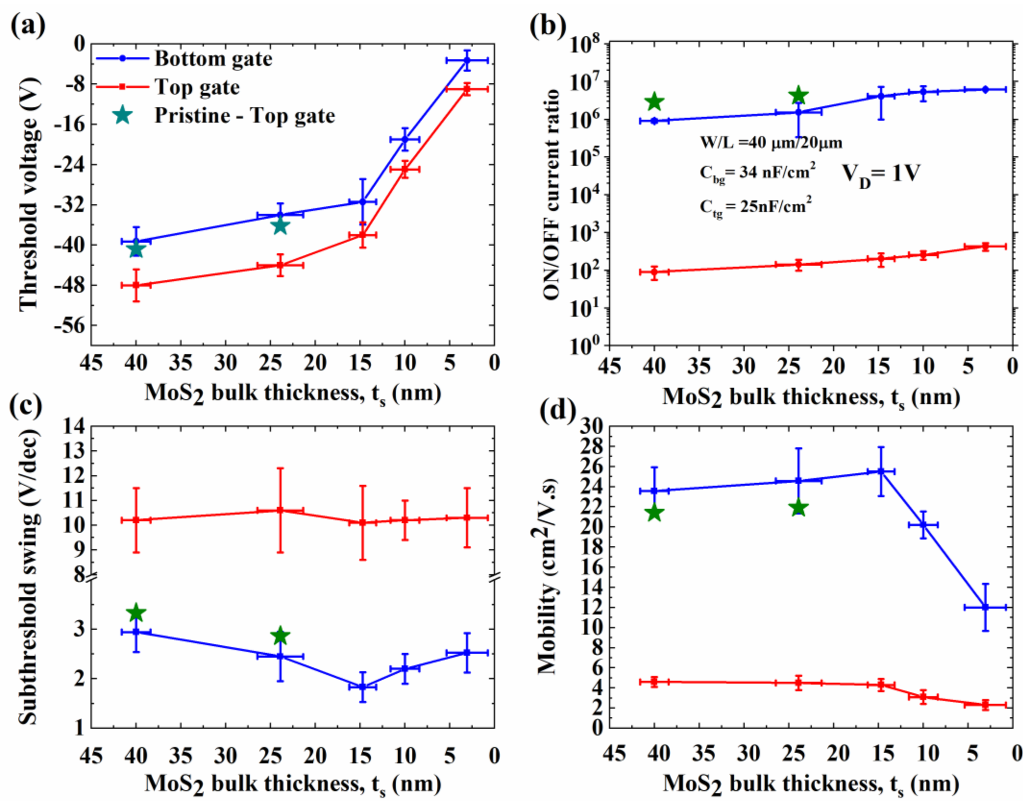

Figure 6.3-1: The electrical characteristics of the bottom gate (blue curves), top gate (red curves), and top gate pristine (green stars) MoS_2 TFTs are plotted for different t_s. (a) the threshold voltage of MoS_2 TFTs as a function of semiconductor thickness, (b) TFT ON/OFF-current ratio variations vs. t_s, (c) the subthreshold swing vs. t_s, and (d) the field-effect mobility vs. t_s.

This effect is further studied through the extraction of the subthreshold swing (*S*) (Figure 6.3-1 (c)). The result shows that the etched top-gate TFTs have about ~5 times higher S than the

bottom and pristine top-gate TFTs. These observations might be expressed as the trap density distribution (D_t) variations, given by:

$$S = 2.3\left(\frac{k_BT}{q}\right)\left[1 + \frac{qD_t}{C_g}\right] \quad \textbf{(Equation 6-1)}$$

,where k_B is Boltzmann's constant, and T is the absolute temperature [113]. Results show that the D_t for the etched top-gate TFTs is about 3×10^{13} $cm^{-2}eV^{-1}$ for different t_s, while the D_t for the pristine top-gate TFTs is two times lower and decreases with reducing t_s. This observation indicates the MoS_2 bulk trap density variation has a minor impact on the electrical performance of the etched top-gate TFTs, and the backchannel surface might have a dominant effect on the electrical performance.

The impact of backchannel surface traps on the carrier field-effect mobility (μ_e) of the top-gate TFTs operating in the linear regime was analyzed using:

$$\mu_e = \left[\frac{\partial I_{ds}}{\partial V_{gs}}\right] \times \left[\frac{L}{C_g V_{ds} W}\right] \quad \textbf{(Equation 6-2)}$$

As shown in Figure 6.3-1 (d), μ_e of the top-gate TFTs are about ~6 times lower than the bottom-gate and pristine top-gate TFTs and have a minor variation with t_s. This observation suggests that the backchannel surface traps have a more dominant impact than the MoS_2 bulk traps on the electrical transport of the backchannel etched top-gate TFTs. In contrast, the effect of MoS_2 bulk traps on the electrical transport of the pristine top-gate TFTs is more significant. Next, the impact of backchannel surface traps on the electrical performance of a dual-gate configuration is investigated.

Figure 6.3-2 (a) shows the V_{th} variation of the dual-gate TFTs (bottom-gate sweep with a constant top gate bias (V_{TG})) from V_{TG} = -40 V to V_{TG} = 10 V as a t_s function. The results show the V_{th} of the etched dual-gate TFTs (solid lines) with t_s > 15 nm does not change after applying V_{TG}. However, for t_s < 15 nm using a negative (positive) V_{TG} leads to a positive (negative) V_{th} shift due to the depletion (accumulation) of the carriers in the channel. On the other hand, pristine dual-gate TFTs (stars) with t_s > 15 nm show V_{th} variation with V_{TG}. These results suggest the backchannel surface traps in the etched dual-gate TFTs may attenuate the top-gate field effect and decrease the V_{th} modulation ability by the top gate. Figure 6.3-3 (a) and (b) show the energy band diagram of pristine and backchannel etched TFTs. The top gate electric field effect leads to forming of a second channel close to the MoS_2/dual dielectric interface. The existence of the interface traps at the dual dielectric/MoS_2 causes weaker depletion of the second channel due to the top gate electric field attenuation. Furthermore, Figure 6.3-3 (a) and (c) depict the thin and thick MoS_2 TFT energy band diagram differences, in which the proximity of the top-gate active region to the bottom-gate one leads to a more significant performance modulation.

The expected ΔV_{th} for the pristine dual-gate TFTs is given by: $\Delta V_{th} = -\frac{C_{TG}}{C_g}\Delta V_{TG}$, where C_{TG} is the top-gate dielectric capacitance [120]. Thus the expected ΔV_{th} for the pristine dual-gate TFTs with V_{TG} = 40 V is about 30 V; however, the measured ΔV_{th} for t_s = 40 nm and t_s = 25 nm are about 10 V and 15 V, respectively. It is shown that the impact of the backchannel surface trap on the electric field of the pristine top-gate backchannel TFTs is low (Figure 6.3-2). Therefore, the increase of ΔV_{th} by reducing the thickness points to the impact of

distance between the top gate and the active region (a similar effect can be seen for the backchannel etched TFTs). Thus, the smaller measured ΔV_{th} is due to the back gate proximity to the channel area effect arising from the MoS_2 bulk traps. This finding is in agreement with the effect of MoS_2 bulk thickness on the electrical performance of top-gate TFTs (Figure 6.3-2). Considering the impact of top-gate proximity to the channel, we expect to have a ΔV_{th} of about 20 V and 17 V for the backchannel etched TFT with t_s = 10 nm and 15 nm, respectively; however, the measured values are 10 V and 2 V, which may arise from the backchannel surface traps. To further investigate, the ON/OFF current ratio, subthreshold swing, and effective mobility are analyzed.

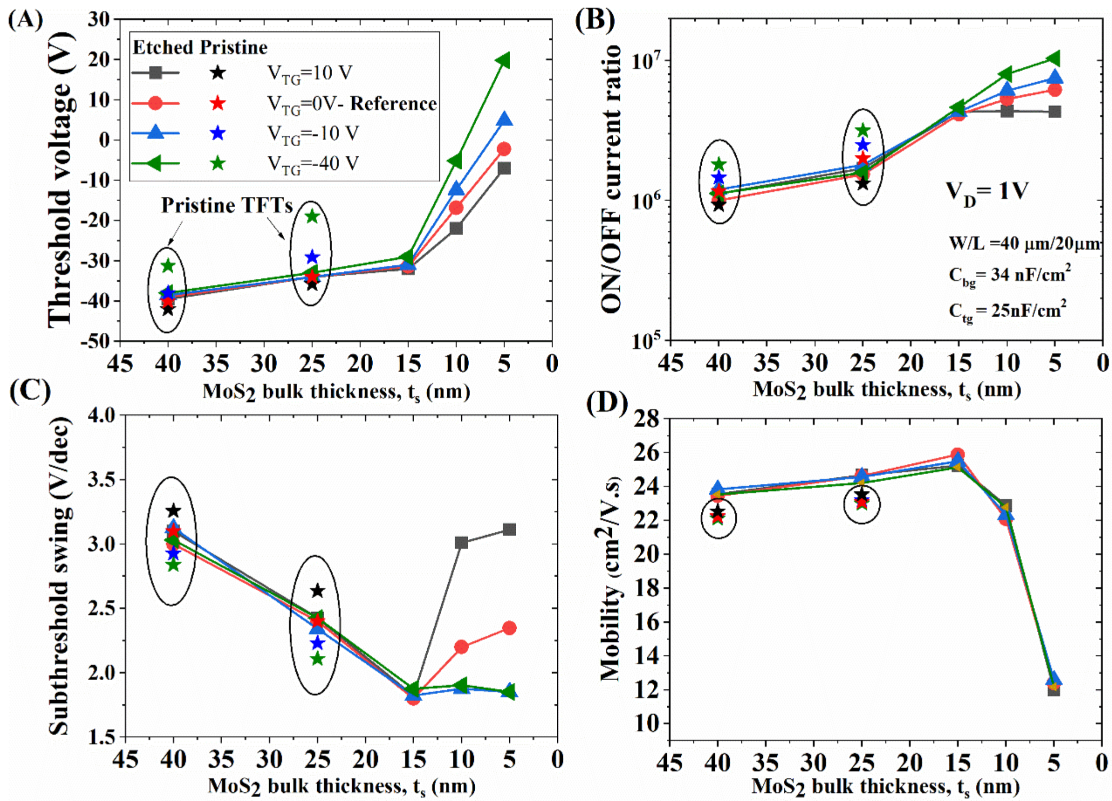

Figure 6.3-2: The electrical characteristics of the bottom gate backchannel etched (lines) and pristine (stars) MoS_2 TFTs with different top gate biases are plotted for different t_s. (a) the threshold voltage of MoS_2 TFTs as a function of semiconductor thickness, (b) TFT ON/OFF-current ratio variations vs. t_s, (c) the subthreshold swing vs. t_s, and (d) the field-effect mobility vs. t_s.

The ON/OFF current ratio variation with t_s is depicted in Figure 6.3-2 (b), indicating no change for the etched dual-gate TFTs with t_s > 15 nm after applying V_{TG}; however, the ON/OFF current ratio varies with V_{TG} for t_s < 15 nm. Applying a negative (positive) V_{TG} causes an increase (decrease) in the ON/OFF current ratio due to the off-current leakage decrease

(increase). Furthermore, the pristine dual-gate TFTs with $t_s > 15$ nm results show that applying V_{TG} leads to ON/OFF current ratio variations, indicating the role of the backchannel surface traps in reducing the top-gate field effect. Moreover, the ON/OFF current ratio variations with positive V_{TG} increase with reducing t_s for etched (when $t_s < 15$ nm) and pristine dual-gate TFTs, showing the top-gate proximity effect.

Similarly, applying V_{TG} causes a change in the *S* of the etched dual-gate TFTs with $t_s < 15$ nm (Figure 6.3-2 (c)) and no *S* variation of the TFTs with $t_s > 15$ nm. Nevertheless, the pristine dual-gate TFTs with $t_s > 15$ nm have *S* variation, indicating the role of the backchannel surface traps in reducing the top-gate field effect, in agreement with the V_{th} and ON/OFF current ratio variations. Furthermore, the pristine dual-gate TFTs have *S* modulation with $V_{TG} < -10$ V for $t_s = 25$ nm and 40 nm, equivalent to a D_{it} decrease of about ~ 2×10^{12} $cm^{-2}eV^{-1}$ and ~ 1×10^{12} $cm^{-2}eV^{-1}$, indicating the effect of the top-gate proximity to the active region.

Interestingly, effective mobility does not change by applying V_{TG}, meaning that electrical transport is unaffected. This effect shows other trap sites (MoS_2/SiO_2 interface and MoS_2 bulk traps) and contact resistance have a higher impact on the effective mobility than the backchannel surface traps in the dual gate configuration. Therefore, the effective mobility can be improved by lowering the trap density at the MoS_2/SiO_2 interface (e.g., using an atomic layer deposited dielectric), higher quality MoS_2 bulk, and low work function drain/source metals such as Scandium.

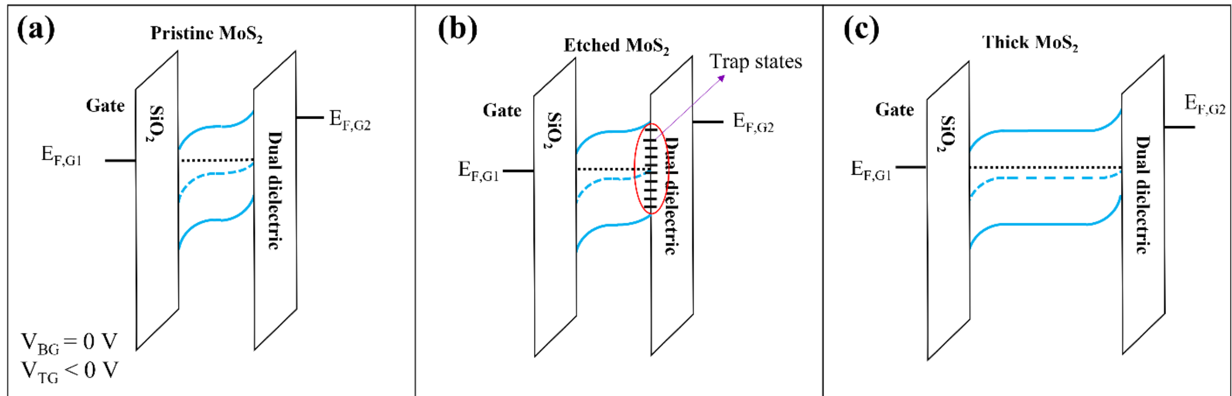

Figure 6.3-3: Energy band diagram of dual gate TFTs with (a) pristine, (b) etched, and (c) thick MoS_2 channels.

In addition, the current stability of an etched dual-gate TFT with t_s = 5 nm is observed to improve after applying V_{TG} = -40V. However, applying V_{TG} = -40V to the etched dual-gate TFT with t_s = 25 nm does not notably change the current stability (see Appendix C, Figure S 7). This difference in the electrical stability of the etched dual-gate TFTs with t_s = 5 nm and 25 nm implies a reduction in the top-gate bias impact on the TFT's active region. To elaborate on this effect, the electrical stability of a pristine dual-gate TFT with t_s =25 nm is measured (Appendix C, Figure S 7). The result shows a bias stability improvement after applying V_{TG} = -40V, indicating the backchannel surface is the root cause of this effect, which agrees with the conclusion from the variations of the electrical parameters in Figure 6.3-2.

Furthermore, the current stability improvement of thinner TFTs is higher than thicker ones after applying a negative top gate voltage, pointing to the impact of the top-gate proximity to the active region, which agrees with the conclusion from Figure 6.3-2. The electrical stability

measurements of etched and pristine dual-gate MoS_2 TFTs are further discussed in the supplementary. These results suggest that the backchannel surface traps and the distance between the top gate to the active region affect the ability of the top gate to modulate the electrical performance and stability of MoS_2 TFTs with various thicknesses. In addition, the adverse impact of the backchannel surface traps, created during the fabrication process, can be controlled using a dual gate configuration.

6.4 Conclusion

In summary, dual-gate MoS_2 TFT arrays were fabricated using a bilayer SiO_x/SiN_x dielectric on pristine and backchannel etched MoS_2 films. The existence of trap states on the backchannel surface of the etched MoS_2 TFTs leads to the degradation of the electrical performance of the top-gate MoS_2 TFTs. Furthermore, it has been discovered that the ability of the top-gate electric field to modulate the electrical performance and stability of dual-gate MoS_2 TFTs is affected by the existence of the backchannel surface traps and the distance between the top gate to the active channel region. This study provides significant insights into the influence of the backchannel surface traps and the impact of TMDC bulk thickness on the device performance. In addition, the dual-gate structure is a practical approach to controlling and modulating the electrical performance and stability of the MoS_2 TFTs with backchannel surface states for realizing the next generation of memory devices.

Chapter 7

7.1 Conclusions

The thesis describes a novel two-step mechanical exfoliation and etching method used to fabricate single-crystal multilayer MoS_2 transistor arrays, which allows for utilizing large areas of transferred material to create electronic device arrays. However, the size of the exfoliated source material used in the transfer is a major limitation of this process. In addition, the electrical characteristics of the devices showed that the MoS_2 bulk and backchannel surface traps exist as trap states, which can impact the performance and stability of multilayer TMDC devices with thicknesses greater than 15 nm. A dry etching process can be used to reduce the MoS_2 bulk trap density and improve electrical performance and stability. Conversely, the etching process can create surface states on the TFT backchannel, which alters electrical stability and carrier transport for TMDC thicknesses less than 15 nm.

Hydrogen-containing passivation layers were used to mitigate the impact of the surface defects on the TFT's electrical performance. The study found that hydrogen incorporation into the active region of TMDC devices after the passivation layer leads to increased trap density and changes in doping, resulting in the degradation of electrical performance and stability. In addition, thin TMDC devices with a thickness of less than 15 nm were found to be more sensitive to the fabrication process, especially hydrogen-containing films and processes. To reduce the adverse impact of hydrogen-containing backchannel passivation layers and processes, a SiO_x barrier layer combined with SiN_x passivation forms a bilayer coating to improve the electrical performance and stability of thin TMDC devices.

Finally, the thesis discusses the fabrication of dual-gate MoS_2 TFT arrays using a bilayer SiO_x/SiN_x dielectric on pristine and backchannel etched MoS_2 films. The existence of trap states on the backchannel surface of the etched MoS_2 TFTs can lead to the degradation of the electrical performance of the top-gate MoS_2 TFTs. The study shows that the top-gate electric field's ability to modulate the electrical performance and stability of dual-gate MoS_2 TFTs is affected by the existence of backchannel surface traps and the distance between the top gate to the active channel region. The dual-gate structure is a practical approach to controlling and modulating the electrical performance and stability of MoS_2 TFTs with backchannel surface states, which may be used to develop the next generation of memory devices.

7.2 Suggestions for Future Work:

According to the results and analysis obtained in this dissertation, some suggestions for future studies are briefly addressed below:

1. To decrease the thickness of the MoS_2 flakes to monolayer and improve the electrical performance of the TFTs, it is essential to address the backchannel surface defects formed during the plasma etching process. Thereby, it is recommended to do more studies on optimizing the plasma etching process. This study can be done by replacing oxygen with inert gases and controlling the machine parameters. The successful outcome of this project may lead to the fabrication of high-performance monolayer MoS_2 TFT arrays.

2. MoS_2 bulk thickness is an essential parameter in defining the electrical performance of the device. Therefore, the effect of this parameter on the performance of the MoS_2-based gas sensors is suggested to be investigated.

3. It is shown that electron beam-deposited silicon oxide is an effective H-barrier; however, this method is not compatible with large-area electronics. Therefore, it is suggested to develop a low-hydrogen content PECVD SiO_x, which can be compatible with the large-area fabrication process.

4. The atomic layer deposited Al_2O_3 is shown to degrade the electrical performance of the MoS_2 TFTs [96]. Thus, using SiO_x as a barrier layer is recommended to reduce the adverse impact of the Al_2O_3 deposition.

5. Measuring the resistivity variation of MoS_2 film after dry etching process using transition line method can be used to further investigate the effect of oxygen doping on the electrical performance of the TFTs.

7.3 Publications and conferences

1. **M. Nouri**, W.T Park, & W.S. Wong, "Effect of large-area exfoliation and etching on the electrical behavior of transition-metal dichalcogenide field-effect transistor arrays," Submitted to ACS Applied Electronic Materials (25/05/2023 - Accepted)
2. **M. Nouri** & W.S. Wong, "Effect of hydrogen-containing passivation layers on the electrical performance of transition-metal dichalcogenide field-effect transistors" (in preparation 2023)
3. **M. Nouri** & W.S. Wong, "Effect of backchannel surface traps on dual gating of dry-etched multilayer transition metal dichalcogenides TFTs" (in preparation 2023)

4. Sadeghianlemraski, M., **Nouri, M.**, Wong, W.S. and Aziz, H., 2022. The Use of Green-Solvent Processable Molecules with Large Dipole Moments in the Electron Extraction Layer of Inverted Organic Solar Cells as a Universal Route for Enhancing Stability. Advanced Sustainable Systems, 6(2), p.2100078
5. **M.Nouri**, M.Asad, W.S.Wong, Fabrication of Thin-Film Transistors Using Large-Area Exfoliation of Single-Crystal MoS2 Layers and Inkjet-Printing, IEEE International Flexible Electronics Technology Conference (IFETC)- 2019
6. **M. Nouri** & W.S. Wong "Fabrication of multilayer MoS2 field-effect transistor arrays using a modified exfoliation method" 62nd Electronic Materials Conference (EMC)- 2020
7. **M. Nouri** & W.S. Wong "Effect of plasma etching on the transport properties and electrical stability in transition-metal dichalcogenide field-effect transistors" Materials Research Society (MRS)- 2022

References

[1] G. E. Moore, "Cramming more components onto integrated circuits," *Proceedings of the IEEE,* vol. 86, pp. 82-85, 1998.

[2] https://www.hpcwire.com/off-the-wire/marvell-and-tsmc-collaborate-to-deliver-data-infrastructure-portfolio-on-5nm-technology/.

[3] S. E. Thompson and S. Parthasarathy, "Moore's law: the future of Si microelectronics," *Materials today,* vol. 9, pp. 20-25, 2006.

[4] D. D. Awschalom and M. E. Flatté, "Challenges for semiconductor spintronics," *Nature physics,* vol. 3, pp. 153-159, 2007.

[5] R. McNeil, M. Kataoka, C. Ford, C. Barnes, D. Anderson, G. Jones*, et al.*, "On-demand single-electron transfer between distant quantum dots," *Nature,* vol. 477, pp. 439-442, 2011.

[6] Y. Benenson, T. Paz-Elizur, R. Adar, E. Keinan, Z. Livneh, and E. Shapiro, "Programmable and autonomous computing machine made of biomolecules," *Nature,* vol. 414, pp. 430-434, 2001.

[7] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos*, et al.*, "Electric field effect in atomically thin carbon films," *science,* vol. 306, pp. 666-669, 2004.

[8] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS2 transistors," *Nat Nanotechnol,* vol. 6, pp. 147-50, Mar 2011.

[9] S. Kim, A. Konar, W. S. Hwang, J. H. Lee, J. Lee, J. Yang*, et al.*, "High-mobility and low-power thin-film transistors based on multilayer MoS2 crystals," *Nat Commun,* vol. 3, p. 1011, 2012.

[10] G. W. Shim, W. Hong, J. H. Cha, J. H. Park, K. J. Lee, and S. Y. Choi, "TFT Channel Materials for Display Applications: From Amorphous Silicon to Transition Metal Dichalcogenides," *Adv Mater,* p. e1907166, Mar 16 2020.

[11] D. Akinwande, N. Petrone, and J. Hone, "Two-dimensional flexible nanoelectronics," *Nat Commun,* vol. 5, p. 5678, Dec 17 2014.

[12] Y. Zhan, Z. Liu, S. Najmaei, P. M. Ajayan, and J. Lou, "Large-area vapor-phase growth and characterization of MoS2 atomic layers on a SiO2 substrate," *Small,* vol. 8, pp. 966-971, 2012.

[13] J. Kedzierski, P.-L. Hsu, P. Healey, P. W. Wyatt, C. L. Keast, M. Sprinkle*, et al.*, "Epitaxial graphene transistors on SiC substrates," *IEEE Transactions on Electron Devices,* vol. 55, pp. 2078-2085, 2008.

[14] Z. M. Wang, *MoS2: materials, physics, and devices* vol. 21: Springer Science & Business Media, 2013.

[15] S. Das, J. A. Robinson, M. Dubey, H. Terrones, and M. Terrones, "Beyond graphene: progress in novel two-dimensional materials and van der Waals solids," *Annual Review of Materials Research,* vol. 45, pp. 1-27, 2015.

[16] R. Ganatra and Q. Zhang, "Few-layer MoS2: a promising layered semiconductor," *ACS nano,* vol. 8, pp. 4074-4099, 2014.

[17] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, "Electronics and optoelectronics of two-dimensional transition metal dichalcogenides," *Nat Nanotechnol,* vol. 7, pp. 699-712, Nov 2012.

[18] L. Liang and V. Meunier, "First-principles Raman spectra of MoS 2, WS 2 and their heterostructures," *Nanoscale,* vol. 6, pp. 5394-5401, 2014.

[19] C. Lee, H. Yan, L. E. Brus, T. F. Heinz, J. Hone, and S. Ryu, "Anomalous lattice vibrations of single-and few-layer MoS2," *ACS nano,* vol. 4, pp. 2695-2700, 2010.

[20] S. D. Brotherton, *Introduction to thin film transistors: physics and technology of TFTs*: Springer Science & Business Media, 2013.

[21] R. A. Street, "Thin-film transistors," *Advanced Materials,* vol. 21, pp. 2007-2022, 2009.

[22] Z. Yu, Z.-Y. Ong, S. Li, J.-B. Xu, G. Zhang, Y.-W. Zhang*, et al.*, "Analyzing the Carrier Mobility in Transition-Metal Dichalcogenide MoS2Field-Effect Transistors," *Advanced Functional Materials,* vol. 27, p. 1604093, 2017.

[23] J. Hong, Z. Hu, M. Probert, K. Li, D. Lv, X. Yang*, et al.*, "Exploring atomic defects in molybdenum disulphide monolayers," *Nature communications,* vol. 6, pp. 1-8, 2015.

[24] H. Qiu, T. Xu, Z. Wang, W. Ren, H. Nan, Z. Ni*, et al.*, "Hopping transport through defect-induced localized states in molybdenum disulphide," *Nature communications,* vol. 4, pp. 1-6, 2013.

[25] N. Kaushik, D. M. A. Mackenzie, K. Thakar, N. Goyal, B. Mukherjee, P. Boggild*, et al.*, "Reversible hysteresis inversion in MoS2 field effect transistors," *npj 2D Materials and Applications,* vol. 1, 2017.

[26] D. W. Greve, "Field effect devices and applications: devices for portable, low-power, and imaging systems," 1998.

[27] Y. Guo, X. Wei, J. Shu, B. Liu, J. Yin, C. Guan*, et al.*, "Charge trapping at the MoS2-SiO2 interface and its effects on the characteristics of MoS2 metal-oxide-semiconductor field effect transistors," *Applied Physics Letters,* vol. 106, p. 103109, 2015.

[28] Y. Huang, J. Wu, X. Xu, Y. Ho, G. Ni, Q. Zou*, et al.*, "An innovative way of etching MoS2: Characterization and mechanistic investigation," *Nano Research,* vol. 6, pp. 200-207, 2013.

[29] S. Kim, M. S. Choi, D. Qu, C. H. Ra, X. Liu, M. Kim*, et al.*, "Effects of plasma treatment on surface properties of ultrathin layered MoS

2," *2D Materials,* vol. 3, p. 035002, 2016.

[30] J. Jadwiszczak, C. O'Callaghan, Y. Zhou, D. S. Fox, E. Weitz, D. Keane*, et al.*, "Oxide-mediated recovery of field-effect mobility in plasma-treated MoS2," *Science advances,* vol. 4, p. eaao5031, 2018.

[31] C. R. Newman, C. D. Frisbie, D. A. da Silva Filho, J.-L. Brédas, P. C. Ewbank, and K. R. Mann, "Introduction to organic thin film transistors and design of n-channel organic semiconductors," *Chemistry of materials,* vol. 16, pp. 4436-4451, 2004.

[32] W. Choi, D. Yin, S. Choo, S.-H. Jeong, H.-J. Kwon, Y. Yoon*, et al.*, "Low-temperature behaviors of multilayer MoS2 transistors with ohmic and Schottky contacts," *Applied Physics Letters,* vol. 115, p. 033501, 2019.

[33] Y. Yoon, K. Ganapathi, and S. Salahuddin, "How good can monolayer MoS2 transistors be?," *Nano letters,* vol. 11, pp. 3768-3773, 2011.

[34] S. L. Li, K. Wakabayashi, Y. Xu, S. Nakaharai, K. Komatsu, W. W. Li*, et al.*, "Thickness-dependent interfacial Coulomb scattering in atomically thin field-effect transistors," *Nano Lett,* vol. 13, pp. 3546-52, Aug 14 2013.

[35] N. Liu, J. Baek, S. M. Kim, S. Hong, Y. K. Hong, Y. S. Kim*, et al.*, "Improving the Stability of High-Performance Multilayer MoS2 Field-Effect Transistors," *ACS Appl Mater Interfaces,* vol. 9, pp. 42943-42950, Dec 13 2017.

[36] J. Roh, J. H. Ryu, G. W. Baek, H. Jung, S. G. Seo, K. An*, et al.*, "Threshold Voltage Control of Multilayered MoS2 Field-Effect Transistors via Octadecyltrichlorosilane and their

Applications to Active Matrixed Quantum Dot Displays Driven by Enhancement-Mode Logic Gates," *Small,* vol. 15, p. 1803852, 2019.

[37] M. J. Kim, Y. Choi, J. Seok, S. Lee, Y. J. Kim, J. Y. Lee*, et al.*, "Defect-free copolymer gate dielectrics for gating MoS2 transistors," *The Journal of Physical Chemistry C,* vol. 122, pp. 12193-12199, 2018.

[38] V. Podzorov, M. Gershenson, C. Kloc, R. Zeis, and E. Bucher, "High-mobility field-effect transistors based on transition metal dichalcogenides," *Applied Physics Letters,* vol. 84, pp. 3301-3303, 2004.

[39] H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, "High-performance single layered WSe2 p-FETs with chemically doped contacts," *Nano letters,* vol. 12, pp. 3788-3792, 2012.

[40] H. Liu, A. T. Neal, and P. D. Ye, "Channel length scaling of MoS2 MOSFETs," *ACS nano,* vol. 6, pp. 8563-8569, 2012.

[41] T. Li, G. Du, B. Zhang, and Z. Zeng, "Scaling behavior of hysteresis in multilayer MoS2 field effect transistors," *Applied Physics Letters,* vol. 105, p. 093107, 2014.

[42] J. Shu, G. Wu, Y. Guo, B. Liu, X. Wei, and Q. Chen, "The intrinsic origin of hysteresis in MoS2 field effect transistors," *Nanoscale,* vol. 8, pp. 3049-56, Feb 7 2016.

[43] R. Yang, Z. Wang, and P. X.-L. Feng, "Electrical breakdown of multilayer MoS 2 field-effect transistors with thickness-dependent mobility," *Nanoscale,* vol. 6, pp. 12383-12390, 2014.

[44] H. Wang, L. Yu, Y. H. Lee, Y. Shi, A. Hsu, M. L. Chin*, et al.*, "Integrated circuits based on bilayer MoS(2) transistors," *Nano Lett,* vol. 12, pp. 4674-80, Sep 12 2012.

[45] K. Kam and B. Parkinson, "Detailed photocurrent spectroscopy of the semiconducting group VIB transition metal dichalcogenides," *The Journal of Physical Chemistry,* vol. 86, pp. 463-467, 1982.

[46] R. Späh, M. Lux-Steiner, M. Obergfell, E. Bucher, and S. Wagner, "n-MoSe2/p-WSe2 heterojunctions," *Applied physics letters,* vol. 47, pp. 871-873, 1985.

[47] W. Jaegermann and D. Schmeisser, "Reactivity of layer type transition metal chalcogenides towards oxidation," *Surface science,* vol. 165, pp. 143-160, 1986.

[48] C.-H. Lee, E. C. Silva, L. Calderin, M. A. T. Nguyen, M. J. Hollander, B. Bersch*, et al.*, "Tungsten ditelluride: a layered semimetal," *Scientific reports,* vol. 5, pp. 1-8, 2015.

[49] Y. H. Lee, X. Q. Zhang, W. Zhang, M. T. Chang, C. T. Lin, K. D. Chang*, et al.*, "Synthesis of large-area MoS2 atomic layers with chemical vapor deposition," *Advanced materials,* vol. 24, pp. 2320-2325, 2012.

[50] Y.-C. Lin, W. Zhang, J.-K. Huang, K.-K. Liu, Y.-H. Lee, C.-T. Liang*, et al.*, "Wafer-scale MoS 2 thin layers prepared by MoO 3 sulfurization," *Nanoscale,* vol. 4, pp. 6637-6641, 2012.

[51] S. Wu, C. Huang, G. Aivazian, J. S. Ross, D. H. Cobden, and X. Xu, "Vapor–solid growth of high optical quality MoS2 monolayers with near-unity valley polarization," *ACS nano,* vol. 7, pp. 2768-2772, 2013.

[52] J. Pütz and M. A. Aegerter, "MoS x thin films by thermolysis of a single-source precursor," *Journal of Sol-Gel Science and Technology,* vol. 19, pp. 821-824, 2000.

[53] J.-W. Chung, Z. Dai, and F. Ohuchi, "WS2 thin films by metal organic chemical vapor deposition," *Journal of crystal growth,* vol. 186, pp. 137-150, 1998.

[54] X. Ling, Y.-H. Lee, Y. Lin, W. Fang, L. Yu, M. S. Dresselhaus*, et al.*, "Role of the seeding promoter in MoS2 growth by chemical vapor deposition," *Nano letters,* vol. 14, pp. 464-472, 2014.

[55] S. J. McDonnell and R. M. Wallace, "Atomically-thin layered films for device applications based upon 2D TMDC materials," *Thin Solid Films,* vol. 616, pp. 482-501, 2016.

[56] M. E. McConney, N. R. Glavin, A. T. Juhl, M. H. Check, M. F. Durstock, A. A. Voevodin*, et al.*, "Direct synthesis of ultra-thin large area transition metal dichalcogenides and their heterostructures on stretchable polymer surfaces," *Journal of Materials Research,* vol. 31, pp. 967-974, 2016.

[57] A. M. Van Der Zande, P. Y. Huang, D. A. Chenet, T. C. Berkelbach, Y. You, G.-H. Lee*, et al.*, "Grains and grain boundaries in highly crystalline monolayer molybdenum disulphide," *Nature materials,* vol. 12, pp. 554-561, 2013.

[58] R. Addou, S. McDonnell, D. Barrera, Z. Guo, A. Azcatl, J. Wang*, et al.*, "Impurities and electronic property variations of natural MoS2 crystal surfaces," *ACS nano,* vol. 9, pp. 9124-9133, 2015.

[59] A. Pisoni, J. Jacimovic, O. S. Barišić, A. Walter, B. l. Náfrádi, P. Bugnon*, et al.*, "The role of transport agents in MoS2 single crystals," *The Journal of Physical Chemistry C,* vol. 119, pp. 3918-3922, 2015.

[60] C. Liu, H. Chen, X. Hou, H. Zhang, J. Han, Y.-G. Jiang*, et al.*, "Small footprint transistor architecture for photoswitching logic and in situ memory," *Nature nanotechnology,* vol. 14, pp. 662-667, 2019.

[61] X. Qian, J. Liu, L. Fu, and J. Li, "Quantum spin Hall effect in two-dimensional transition metal dichalcogenides," *Science,* vol. 346, pp. 1344-1347, 2014.

[62] D. Li, M. Chen, Z. Sun, P. Yu, Z. Liu, P. M. Ajayan*, et al.*, "Two-dimensional non-volatile programmable p–n junctions," *Nature nanotechnology,* vol. 12, pp. 901-906, 2017.

[63] N. Vardy, "MoS2 Thin Film Transistors using PECVD Dielectrics and Optical Contrast Modeling for Thickness Measurement," University of Waterloo, 2015.

[64] S. G. Seo, J. Joeng, K. Kim, K. Kim, and S. H. Jin, "Bias Stress Instability in Multilayered MoS 2 Field-Effect Transistors Under Pulse-Mode Operation," *IEEE Transactions on Electron Devices,* vol. 67, pp. 1864-1872, 2020.

[65] Y. Y. Illarionov, G. Rzepa, M. Waltl, T. Knobloch, A. Grill, M. M. Furchi*, et al.*, "The role of charge trapping in MoS2/SiO2 and MoS2/hBN field-effect transistors," *2D Materials,* vol. 3, p. 035004, 2016.

[66] G. Z. Magda, J. Pető, G. Dobrik, C. Hwang, L. P. Biró, and L. Tapasztó, "Exfoliation of large-area transition metal chalcogenide single layers," *Scientific reports,* vol. 5, p. 14714, 2015.

[67] M. j. Velický, G. E. Donnelly, W. R. Hendren, S. McFarland, D. Scullion, W. J. DeBenedetti*, et al.*, "Mechanism of gold-assisted exfoliation of centimeter-sized transition-metal dichalcogenide monolayers," *ACS nano,* vol. 12, pp. 10463-10472, 2018.

[68] S. B. Desai, S. R. Madhvapathy, M. Amani, D. Kiriya, M. Hettick, M. Tosun*, et al.*, "Gold-Mediated Exfoliation of Ultralarge Optoelectronically-Perfect Monolayers," *Adv Mater,* vol. 28, pp. 4053-8, Jun 2016.

[69] A. Di Bartolomeo, L. Genovese, F. Giubileo, L. Iemmo, G. Luongo, T. Foller*, et al.*, "Hysteresis in the transfer characteristics of MoS2 transistors," *2D Materials,* vol. 5, p. 015014, 2017.

[70] Y. Zhang, H. Li, H. Wang, H. Xie, R. Liu, S. L. Zhang*, et al.*, "Thickness Considerations of Two-Dimensional Layered Semiconductors for Transistor Applications," *Sci Rep,* vol. 6, p. 29615, Jul 12 2016.

[71] S. Das, H. Y. Chen, A. V. Penumatcha, and J. Appenzeller, "High performance multilayer MoS2 transistors with scandium contacts," *Nano Lett,* vol. 13, pp. 100-5, Jan 9 2013.

[72] Y. Huang, E. Sutter, N. N. Shi, J. Zheng, T. Yang, D. Englund*, et al.*, "Reliable exfoliation of large-area high-quality flakes of graphene and other two-dimensional materials," *ACS nano,* vol. 9, pp. 10612-10620, 2015.
[73] M. H. Jeon, C. Ahn, H. Kim, K. N. Kim, N. T. Li, H. Qin*, et al.*, "Controlled MoS(2) layer etching using CF(4) plasma," *Nanotechnology,* vol. 26, p. 355706, Sep 4 2015.
[74] S. Xiao, P. Xiao, X. Zhang, D. Yan, X. Gu, F. Qin*, et al.*, "Atomic-layer soft plasma etching of MoS2," *Sci Rep,* vol. 6, p. 19945, Jan 27 2016.
[75] S. Kim, M. S. Choi, D. Qu, C. H. Ra, X. Liu, M. Kim*, et al.*, "Effects of plasma treatment on surface properties of ultrathin layered MoS2," *2D Materials,* vol. 3, p. 035002, 2016.
[76] Y. Liu, H. Nan, X. Wu, W. Pan, W. Wang, J. Bai*, et al.*, "Layer-by-layer thinning of MoS2 by plasma," *ACS nano,* vol. 7, pp. 4202-4209, 2013.
[77] A. T. Neal, R. Pachter, and S. Mou, "P-type conduction in two-dimensional MoS2 via oxygen incorporation," *Applied Physics Letters,* vol. 110, p. 193103, 2017.
[78] M. R. Islam, N. Kang, U. Bhanu, H. P. Paudel, M. Erementchouk, L. Tetard*, et al.*, "Tuning the electrical property via defect engineering of single layer MoS 2 by oxygen plasma," *Nanoscale,* vol. 6, pp. 10033-10039, 2014.
[79] H. Shen, J. Ren, J. Li, Y. Chen, S. Lan, J. Wang*, et al.*, "Multistate memory enabled by interface engineering based on multilayer tungsten diselenide," *ACS Applied Materials & Interfaces,* vol. 12, pp. 58428-58434, 2020.
[80] Y. Park, H. W. Baac, J. Heo, and G. Yoo, "Thermally activated trap charges responsible for hysteresis in multilayer MoS2 field-effect transistors," *Applied Physics Letters,* vol. 108, p. 083102, 2016.
[81] A.-J. Cho, S. Yang, K. Park, S. D. Namgung, H. Kim, and J.-Y. Kwon, "Multi-layer MoS2 FET with small hysteresis by using atomic layer deposition Al2O3 as gate insulator," *ECS Solid State Letters,* vol. 3, p. Q67, 2014.
[82] C.-K. Kim, C. H. Yu, J. Hur, H. Bae, S.-B. Jeon, H. Park*, et al.*, "Abnormal electrical characteristics of multi-layered MoS

2

FETs attributed to bulk traps," *2D Materials,* vol. 3, p. 015007, 2016.
[83] J. L. Doherty, S. G. Noyce, Z. Cheng, H. Abuzaid, and A. D. Franklin, "Capping Layers to Improve the Electrical Stress Stability of MoS2 Transistors," *ACS Applied Materials & Interfaces,* vol. 12, pp. 35698-35706, 2020.
[84] X.-s. Wang, G. Zhai, J. Yang, and N. Cue, "Crystalline Si 3 N 4 thin films on Si (111) and the 4× 4 reconstruction on Si 3 N 4 (0001)," *Physical Review B,* vol. 60, p. R2146, 1999.
[85] T. Ma, "Making silicon nitride film a viable gate dielectric," *IEEE transactions on electron devices,* vol. 45, pp. 680-690, 1998.
[86] K. Chen, D. Kiriya, M. Hettick, M. Tosun, T.-J. Ha, S. R. Madhvapathy*, et al.*, "Air stable n-doping of WSe2 by silicon nitride thin films with tunable fixed charge density," *Apl Materials,* vol. 2, p. 092504, 2014.
[87] A. Tari and W. S. Wong, "Effect of dual-dielectric hydrogen-diffusion barrier layers on the performance of low-temperature processed transparent InGaZnO thin-film transistors," *Applied Physics Letters,* vol. 112, p. 073506, 2018.
[88] J. Park, S. Kim, C. Kim, S. Kim, I. Song, H. Yin*, et al.*, "High-performance amorphous gallium indium zinc oxide thin-film transistors through N 2 O plasma passivation," *Applied Physics Letters,* vol. 93, p. 053505, 2008.

[89] S. W. Han, G.-B. Cha, Y. Park, and S. Hong, "Hydrogen physisorption based on the dissociative hydrogen chemisorption at the sulphur vacancy of MoS2 surface," *Scientific reports,* vol. 7, pp. 1-7, 2017.

[90] H. Li, M. Huang, and G. Cao, "Markedly different adsorption behaviors of gas molecules on defective monolayer MoS 2: a first-principles study," *Physical Chemistry Chemical Physics,* vol. 18, pp. 15110-15117, 2016.

[91] E. W. K. Koh, C. H. Chiu, Y. K. Lim, Y.-W. Zhang, and H. Pan, "Hydrogen adsorption on and diffusion through MoS2 monolayer: First-principles study," *International journal of hydrogen energy,* vol. 37, pp. 14323-14328, 2012.

[92] A. Soman, R. A. Burke, Q. Li, M. D. Valentin, T. Li, D. Mao*, et al.*, "Hydrogen Plasma Exposure of Monolayer MoS2 Field-Effect Transistors and Prevention of Desulfurization by Monolayer Graphene," *ACS applied materials & interfaces,* vol. 12, pp. 37305-37312, 2020.

[93] S. W. Han, G.-B. Cha, K. Kim, and S. C. Hong, "Hydrogen interaction with a sulfur-vacancy-induced occupied defect state in the electronic band structure of MoS 2," *Physical Chemistry Chemical Physics,* vol. 21, pp. 15302-15309, 2019.

[94] Y. Y. Illarionov, K. K. Smithe, M. Waltl, T. Knobloch, E. Pop, and T. Grasser, "Improved hysteresis and reliability of MoS 2 transistors with high-quality CVD growth and Al 2 O 3 encapsulation," *IEEE Electron Device Letters,* vol. 38, pp. 1763-1766, 2017.

[95] W. J. Woo, I.-K. Oh, B.-E. Park, Y. Kim, J. Park, S. Seo*, et al.*, "Bi-layer high-k dielectrics of Al2O3/ZrO2 to reduce damage to MoS2 channel layers during atomic layer deposition," *2D Materials,* vol. 6, p. 015019, 2018.

[96] J.-G. Song, S. J. Kim, W. J. Woo, Y. Kim, I.-K. Oh, G. H. Ryu*, et al.*, "Effect of Al2O3 deposition on performance of top-gated monolayer MoS2-based field effect transistor," *ACS applied materials & interfaces,* vol. 8, pp. 28130-28135, 2016.

[97] W. Park, J. Park, J. Jang, H. Lee, H. Jeong, K. Cho*, et al.*, "Oxygen environmental and passivation effects on molybdenum disulfide field effect transistors," *Nanotechnology,* vol. 24, p. 095202, 2013.

[98] J. Roh, I.-T. Cho, H. Shin, G. W. Baek, B. H. Hong, J.-H. Lee*, et al.*, "Fluorinated CYTOP passivation effects on the electrical reliability of multilayer MoS2 field-effect transistors," *Nanotechnology,* vol. 26, p. 455201, 2015.

[99] P. Bolshakov, A. Khosravi, P. Zhao, P. K. Hurley, C. L. Hinkle, R. M. Wallace*, et al.*, "Dual-gate MoS2 transistors with sub-10 nm top-gate high-k dielectrics," *Applied Physics Letters,* vol. 112, p. 253502, 2018.

[100] M. S. Fuhrer and J. Hone, "Measurement of mobility in dual-gated MoS2 transistors," *Nature nanotechnology,* vol. 8, pp. 146-147, 2013.

[101] F. Liao, Z. Guo, Y. Wang, Y. Xie, S. Zhang, Y. Sheng*, et al.*, "High-performance logic and memory devices based on a dual-gated MoS2 architecture," *ACS Applied Electronic Materials,* vol. 2, pp. 111-119, 2019.

[102] G.-H. Lee, X. Cui, Y. D. Kim, G. Arefe, X. Zhang, C.-H. Lee*, et al.*, "Highly stable, dual-gated MoS2 transistors encapsulated by hexagonal boron nitride with gate-controllable contact, resistance, and threshold voltage," *ACS nano,* vol. 9, pp. 7019-7026, 2015.

[103] D. J. Groenendijk, M. Buscema, G. A. Steele, S. Michaelis de Vasconcellos, R. Bratschitsch, H. S. van der Zant*, et al.*, "Photovoltaic and photothermoelectric effect in a double-gated WSe2 device," *Nano letters,* vol. 14, pp. 5846-5852, 2014.

[104] S. Bertolazzi, D. Krasnozhon, and A. Kis, "Nonvolatile memory cells based on MoS2/graphene heterostructures," *ACS nano,* vol. 7, pp. 3246-3252, 2013.

[105] X. Zou, J. Xu, H. Huang, Z. Zhu, H. Wang, B. Li*, et al.*, "A comparative study on top-gated and bottom-gated multilayer MoS2 transistors with gate stacked dielectric of Al2O3/HfO2," *Nanotechnology,* vol. 29, p. 245201, 2018.

[106] X. Li, T. Li, Z. Zhang, X. Xiong, S. Li, and Y. Wu, "Tunable low-frequency noise in dual-gate MoS 2 transistors," *IEEE Electron Device Letters,* vol. 39, pp. 131-134, 2017.

[107] M. Sharma, A. Singh, P. Aggarwal, and R. Singh, "Large-Area Transfer of 2D TMDCs Assisted by a Water-Soluble Layer for Potential Device Applications," *ACS omega,* vol. 7, pp. 11731-11741, 2022.

[108] A. Castellanos-Gomez, M. Buscema, R. Molenaar, V. Singh, L. Janssen, H. S. Van Der Zant*, et al.*, "Deterministic transfer of two-dimensional materials by all-dry viscoelastic stamping," *2D Materials,* vol. 1, p. 011002, 2014.

[109] G. Ye, Y. Gong, J. Lin, B. Li, Y. He, S. T. Pantelides*, et al.*, "Defects engineered monolayer MoS2 for improved hydrogen evolution reaction," *Nano letters,* vol. 16, pp. 1097-1103, 2016.

[110] F. Ghasemi, A. Abdollahi, and S. Mohajerzadeh, "Controlled Plasma Thinning of Bulk MoS2 Flakes for Photodetector Fabrication," *ACS Omega,* vol. 4, pp. 19693-19704, Nov 26 2019.

[111] K. Gołasa, M. Grzeszczyk, R. Bożek, P. Leszczyński, A. Wysmołek, M. Potemski*, et al.*, "Resonant Raman scattering in MoS2—From bulk to monolayer," *Solid state communications,* vol. 197, pp. 53-56, 2014.

[112] C.-H. Lee, N. Vardy, and W. Wong, "Multilayer MoS2 Thin-film Transistors Employing Silicon Nitride and Silicon Oxide Dielectric Layers," *IEEE Electron Device Letters,* pp. 1-1, 2016.

[113] B. G. Streetman and S. Banerjee, *Solid state electronic devices* vol. 4: Prentice hall Englewood Cliffs, NJ, 1995.

[114] S. Wang, X. Zeng, Y. Zhou, J. Lu, Y. Hu, W. Wang*, et al.*, "High-Performance MoS2 Complementary Inverter Prepared by Oxygen Plasma Doping," *ACS Applied Electronic Materials,* vol. 4, pp. 955-963, 2022.

[115] M. W. Lin, Kravchenko, II, J. Fowlkes, X. Li, A. A. Puretzky, C. M. Rouleau*, et al.*, "Thickness-dependent charge transport in few-layer MoS(2) field-effect transistors," *Nanotechnology,* vol. 27, p. 165203, Apr 22 2016.

[116] J. T. Drotar, Y.-P. Zhao, T.-M. Lu, and G.-C. Wang, "Mechanisms for plasma and reactive ion etch-front roughening," *Physical Review B,* vol. 61, p. 3012, 2000.

[117] L. Li, R. Long, T. Bertolini, and O. V. Prezhdo, "Sulfur adatom and vacancy accelerate charge recombination in MoS2 but by different mechanisms: time-domain ab initio analysis," *Nano letters,* vol. 17, pp. 7962-7967, 2017.

[118] H. Fang, M. Tosun, G. Seol, T. C. Chang, K. Takei, J. Guo*, et al.*, "Degenerate n-doping of few-layer transition metal dichalcogenides by potassium," *Nano letters,* vol. 13, pp. 1991-1995, 2013.

[119] N. Nickel, "Hydrogen diffusion through silicon/silicon dioxide interfaces," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena,* vol. 18, pp. 1770-1772, 2000.

[120] M. J. Spijkman, K. Myny, E. C. Smits, P. Heremans, P. W. Blom, and D. M. De Leeuw, "Dual-gate thin-film transistors, integrated circuits and sensors," *Advanced Materials,* vol. 23, pp. 3231-3242, 2011.

[121] F. Libsch and J. Kanicki, "Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors," *Applied Physics Letters,* vol. 62, pp. 1286-1288, 1993.

[122] J.-M. Lee, I.-T. Cho, J.-H. Lee, and H.-I. Kwon, "Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in InGaZnO thin film transistors," *Applied Physics Letters,* vol. 93, p. 093504, 2008.
[123] M. J. Chow, A. A. Fomani, M. Moradi, G. Chaji, R. A. Lujan, and W. S. Wong, "Effects of mechanical strain on amorphous silicon thin-film transistor electrical stability," *Applied Physics Letters,* vol. 102, p. 233509, 2013.

Appendix A

Supplementary Information for Chapter 4

In this chapter, several identical devices were tested to gain a deeper understanding of the origin of the high V_{th} observed in Figure 4.3-2. The absolute values of key parameters such as threshold voltage, ON/OFF current ratio, field-effect mobility, and subthreshold swing were determined as a function of the thickness of the MoS_2 bulk. Then, the electrical stability of MoS_2 TFTs with various bulk thicknesses is explored to reveal the characteristic of trap states.

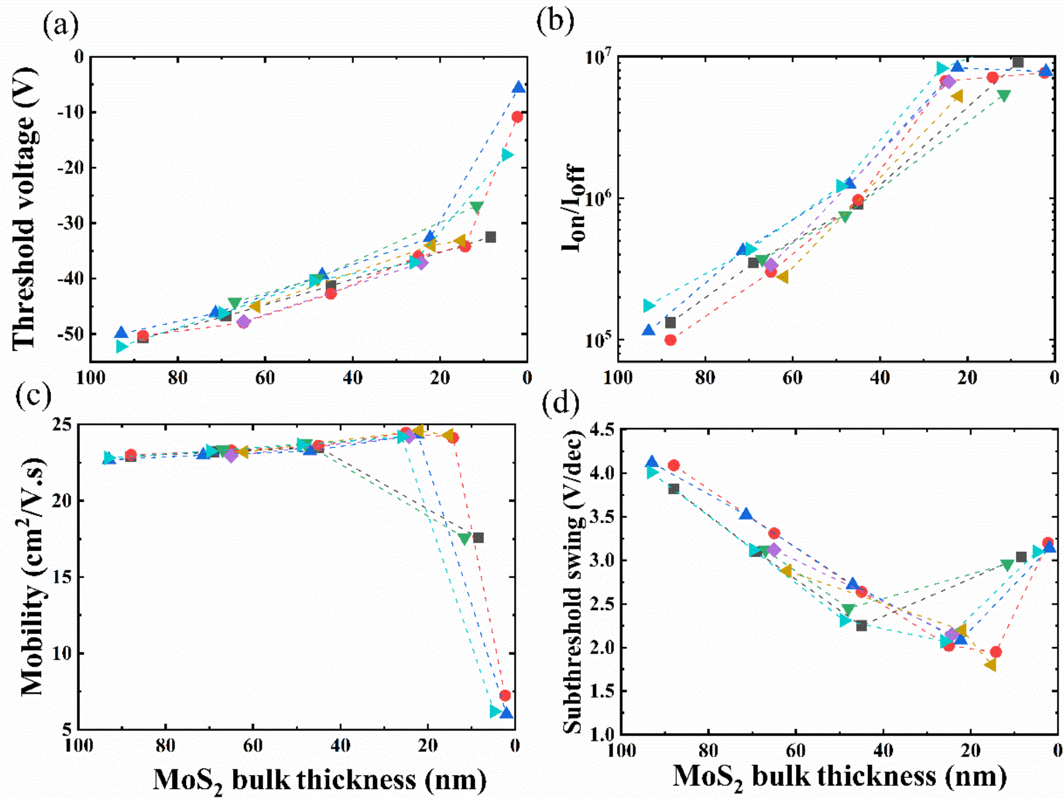

Figure S 1: Absolute parameter values of MoS_2 TFTs at different MoS_2 bulk thicknesses. The threshold voltage, the I_{on}/I_{off} ratio, the field-effect mobility, and the subthreshold swing as a function of the MoS_2 bulk thickness are plotted in (a) – (d), respectively. Each symbol represented an individual TFT, and dashed lines connect their parameter variations with the MoS_2 bulk thickness.

Electrical stability measurement

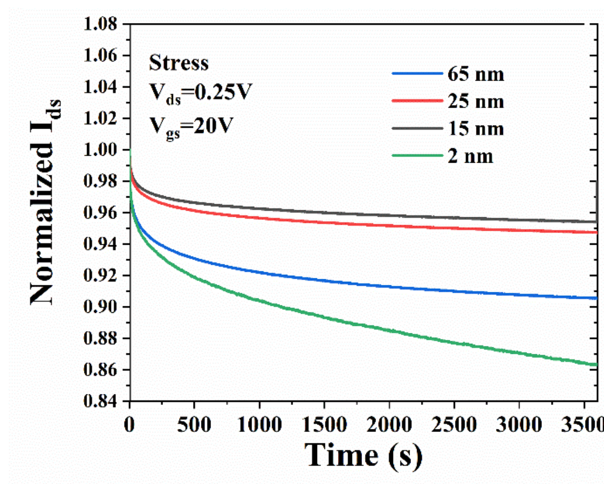

Figure S 2: Electrical stability measurement of a TFT with different MoS_2 bulk thicknesses.

To further investigate the effect of the defect states and process parameters on the TFT performance, the device current-voltage (I-V) characteristics were measured over time. For these time-dependent measurements, MoS_2 TFTs were measured having: 1) as-transferred

devices with an initial MoS_2 bulk thickness of 65 nm and 2) processed devices with thicknesses of 25 nm, 15 nm, and 2 nm. The drain current was measured in dark conditions under pulsed (duty cycle = 3%) and dc gate biases with V_{gs}=20 V and V_{ds} = 0.25 V in an evacuated chamber at a pressure of 1×10^{-5} Torr.

Figure S 2 compares the normalized I_{ds} $\left(Norm.I_{ds} = \frac{I_{ds}(t)}{I_{ds}(t=0)}\right)$ response over time for four MoS_2 bulk thicknesses. The as-transferred TFT (t_s = 65 nm), I_{ds} decreased by 9% after applying 3600 s of dc gate bias. The current stability was observed to improve after etching 40 nm of MoS_2. In this case, I_{ds} decreased by 4 % from its initial value after 3600 s of dc bias. After removing an additional 10 nm of MoS_2, the I_{ds} degradation dropped to 3% of its initial value. This improvement in the electrical stability with decreasing t_s (from 65 nm to 15 nm) implies a reduction in the density of trapped charges. In contrast, at a lower thickness (t_s = 2 nm), the I_{ds} degradation increased to 14 % after 3600 s.

The change in the electrical stability is related to the density of defect states in the semiconductor, where the current vs. time dependence is expected to follow a stretched-exponential behavior, typically observed in disordered semiconductor thin-film devices [121, 122]. This behavior is modeled by:

$$\frac{I_{ds}(t)}{I_{ds}(t = 0\ s)} = exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]$$

, where τ is the carrier relaxation time, and β is the dispersion parameter [123]. The carrier relaxation time and the dispersion parameter may be used to extract the thermal activation

energy (E_a) of the trap states in the bulk semiconductor, with $\tau = \upsilon^{-1}exp(E_a/\beta kT)$ where υ is an empirical frequency [123].

Table 1 provides β, τ, and E_a parameters, extracted from the fitting of I_{ds} vs. time curves for TFTs under different processing conditions. The carrier relaxation times were found to increase by approximately two orders of magnitudes as the MoS_2 is etched from a thickness of 65 nm to 15 nm. Interestingly, β remains nearly constant for t_s >15 nm, suggesting that the dispersion of energy barrier height for charge trapping is not affected by the etching process. Furthermore, E_a remains almost constant at 0.33 eV down to t_s = 15 nm. On the other hand, at t_s = 2 nm, τ decreases about five orders of magnitude, β increases to 0.27, and E_a increases to ~ 0.45 eV.

Table 2: Bias-stress measurement parameters at different t_s.

t_s (nm)	β	τ(s)	E_a(eV)
65	0.17	1×10^9	0.32
25	0.17	5×10^{10}	0.33
15	0.17	1×10^{11}	0.33
2	0.27	4×10^6	0.45

Appendix B

Supplementary Information for Chapter 5

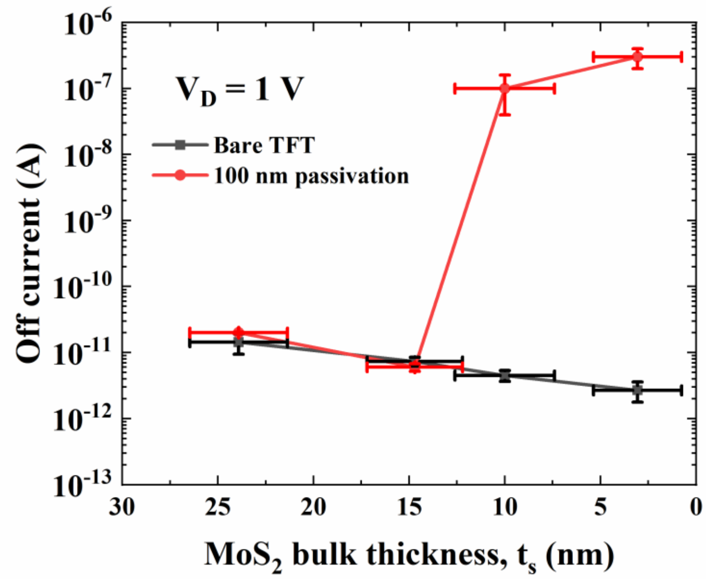

Figure S 3: Off-current variations of MoS_2 TFTs after passivation at different t_s.

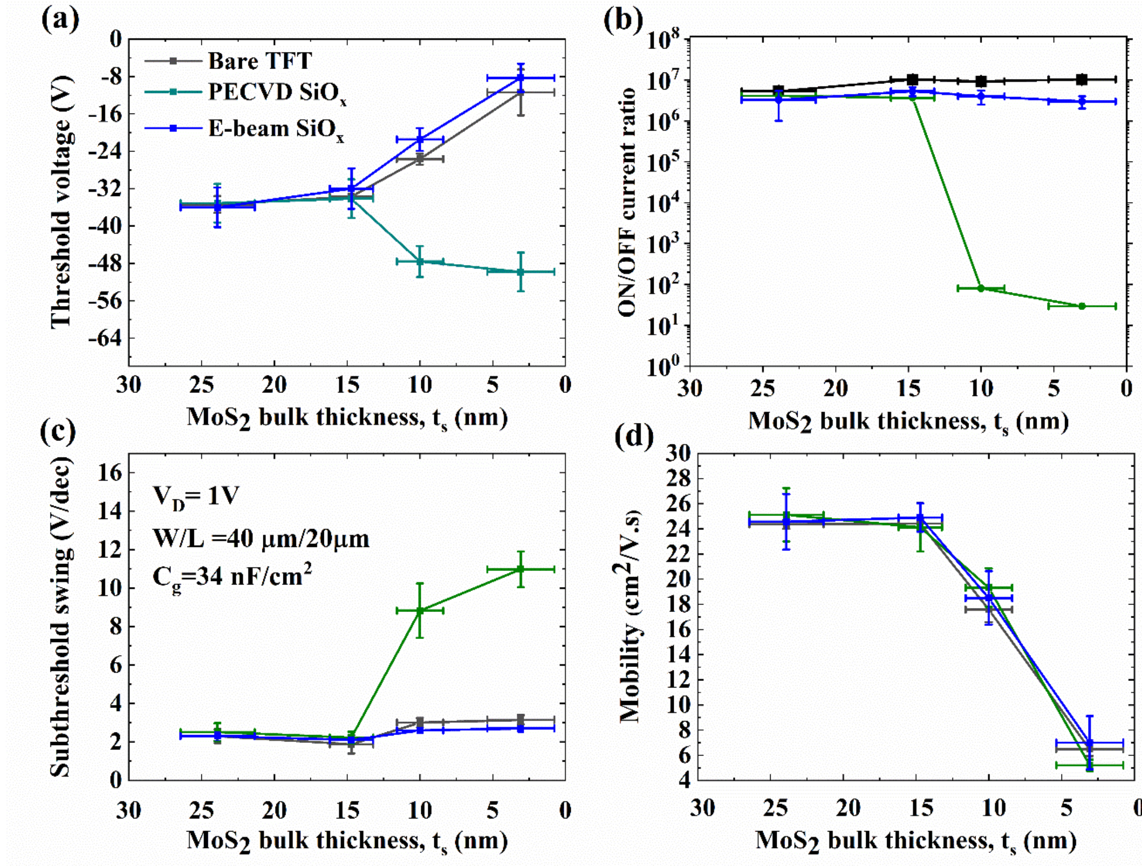

Figure S 4:The electrical characteristics of bare MoS_2 TFT (black curve), after passivation with 50 nm PECVD SiO_x (green curve), and after passivation with 50 nm E-beam SiO_x (blue curve) are plotted for different t_s. (a) the threshold voltage of MoS_2 TFTs as a function of semiconductor thickness, (b) TFT ON/OFF-current ratio variations vs. t_s, (c) the subthreshold swing vs. t_s, and (d) the field-effect mobility vs. t_s.

Electrical stability measurement

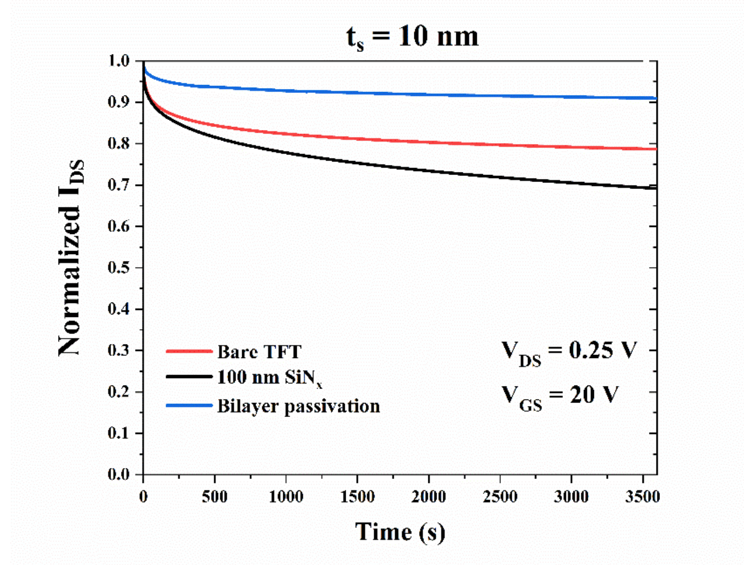

Figure S 5: Electrical stability measurement of TFTs with 10 nm MoS_2 bulk thicknesses in different backchannel conditions.

The carrier relaxation time is found to decrease about one order of magnitude after 100 nm SiN_x passivation. Moreover, β increases from 0.2 to 0.3, suggesting that the dispersion of energy barrier height for charge trapping is increased by hydrogen contamination. Furthermore, E_a increases from 0.3 eV in the bare condition to 0.4 eV for the SiN_x passivation condition. This extracted E_a value can be attributed to the traps due to the hydrogen adsorption in MoS_2 bulk, reported in computational investigations by Han et al. [89]. On the other hand, for the bilayer passivated TFT, τ increases about three orders of magnitude, and β and E_a remain unchanged. This improvement shows the bilayer dielectric is an effective passivation

layer for the MoS_2 backchannel surface, which agrees with the earlier observation of S and V_{th} variations (Figure 5.3-1).

Table 3: Bias-stress measurement parameters for t_s = 10 nm at different backchannel conditions

t_s = 10 nm	**β**	**τ(s)**	**E_a(eV)**
Bare TFT	0.2	5×10^6	0.3
100 nm SiN_x	0.3	1×10^5	0.4
Bilayer	0.2	2×10^9	0.3

Appendix C

Supplementary Information for Chapter 6

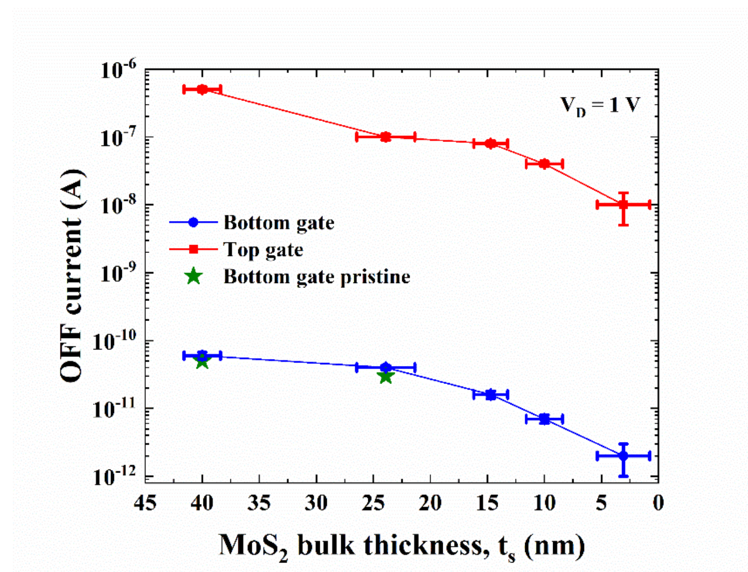

Figure S 6: OFF current of the bottom gate, top gate, and top gate pristine MoS_2 TFT as a function of MoS_2 bulk thickness.

Electrical stability measurement

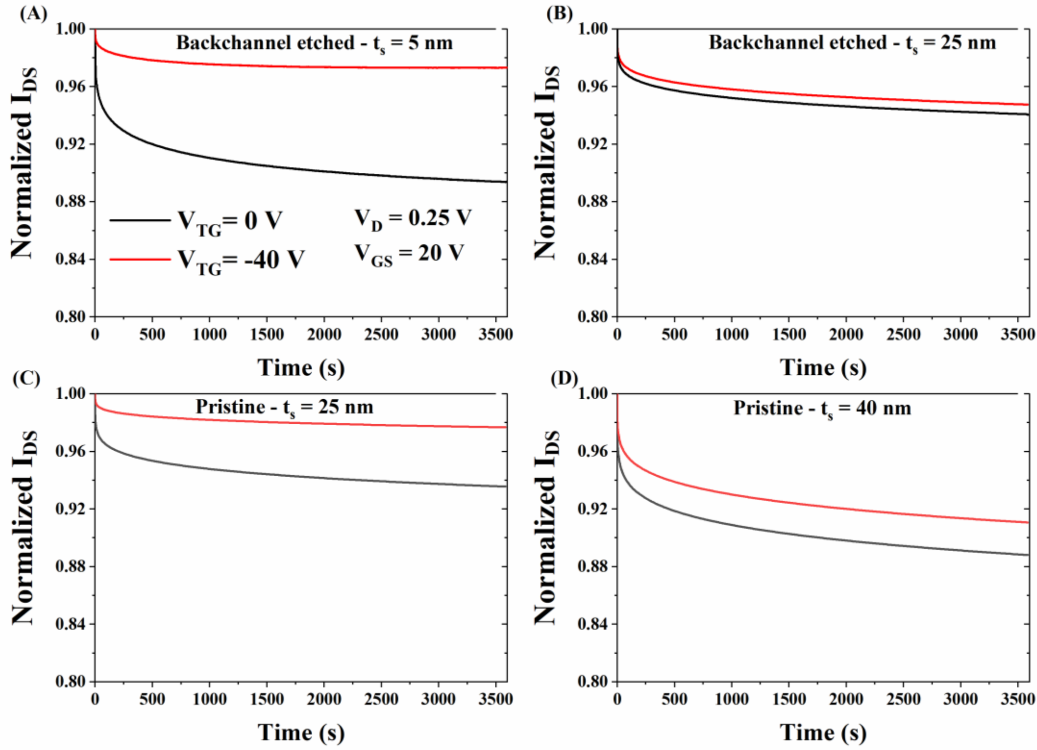

Figure S 7: Electrical stability measurement of (A) etched dual-gate MoS_2 TFT with t_s = 5 nm, (B) etched dual-gate MoS_2 TFT with t_s = 25 nm, (C) pristine dual-gate MoS_2 TFT with t_s = 25 nm, and (D) pristine dual-gate MoS_2 TFT with t_s = 40 nm at different top gate voltages.

Figure S 7 compares the normalized I_{ds} $\left(Norm.I_{ds} = \frac{I_{ds}(t)}{I_{ds}(t=0)}\right)$ responses over time for etched and pristine dual-gate TFTs with different t_s. The etched dual-gate TFT (t_s = 5 nm) I_{ds} decreased by 7% after applying 3600 s of dc gate bias with V_{TG} = 0V (Figure S 7 (a)). The current stability

was observed to improve after applying V_{TG} = -40V. In this case, I_{ds} decreased by 3 % from its initial value after 3600 s of dc bias. However, applying V_{TG} = -40V to the etched dual-gate TFT with t_s = 25 nm does not notably change the current stability (Figure S 7 (b)). This difference in the electrical stability of the etched dual-gate TFTs with t_s = 5 nm and 25 nm implies a reduction in the top gate electric field impact on the TFT's active region. To elaborate on this effect, the electrical stability of a pristine dual-gate TFT with t_s =25 nm is measured (Figure S 7 (c)). The result shows a bias stability improvement by ~5 % after applying V_{TG} = -40V, indicating the backchannel surface is the root cause of this effect, which agrees with the conclusion from the variations of the electrical parameters in Figure 6.3-1. Figure S 7 (d) illustrates applying V_{TG} = -40V to the pristine backchannel TFT with t_s = 40 nm leads to an improvement in the bias stability of ~ 2%. In contrast, the improvement of the pristine dual-gate TFT with ts = 25 nm is about 5 % (Figure S 7 (c)), pointing to the impact of the top gate proximity to the active region, which agrees with the conclusion from Figure 6.3-2.

The change in the electrical stability is related to the density of defect states in the semiconductor, where the current vs. time dependence is expected to follow a stretched-exponential behavior.

Table 4 provides β, τ, and E_a parameters extracted from the fitting of I_{ds} vs. time curves for TFTs under different processing and bias conditions. The results show β remains nearly constant after apply V_{TG} for all TFTs, suggesting that the dispersion of energy barrier height for charge trapping is not affected by the top gate field effect. Furthermore, E_a remains almost constant at 0.3 eV, showing the trap's activation energy is independent of the top gate electric

field. The carrier relaxation time is found to increase by approximately three orders of magnitudes after applying V_{TG} = -40 V to the etched dual-gate TFT with t_s = 5 nm, while the 25 nm TFT does not show any change in the carrier relaxation time. Furthermore, τ of the dual-gate TFT with t_s =25 nm has about 20 times increase. In contrast, the pristine dual-gate 40 nm TFT shows a six times increase, indicating the effect of backchannel proximity. This result suggests the backchannel surface traps and the distance between the top gate to the active region affect the ability of the top gate to modulate the electrical performance and stability of MoS_2 TFTs with various thicknesses. In addition, the dual gate structure is a practical approach to controlling and modulating the electrical performance and stability of the MoS_2 TFTs with backchannel surface states for realizing the next generation of memory devices.

Table 4: Bias-stress measurement parameters

	β		τ (s)		E_a (eV)	
	V_{TG}=0V	V_{TG}=-40 V	V_{TG}=0V	V_{TG}=-40 V	V_{TG}=0V	V_{TG}=-40 V
Etched - 5 nm	0.17	0.17	1×10^{9}	1×10^{13}	0.29	0.31
Etched - 25 nm	0.17	0.17	4×10^{10}	4×10^{10}	0.33	0.33
Pristine - 25 nm	0.17	0.17	2×10^{10}	4×10^{11}	0.28	0.29
Pristine – 40 nm	0.17	0.17	8×10^{8}	5×10^{9}	0.27	0.28