Low-Power and High-Performance Drivers for OLEDoS Microdisplays

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

The rapid growth of the microdisplay market, driven by the demand for smartwatches, head-mounted displays in Virtual Reality (VR) and Augmented Reality (AR), and other portable devices, has presented a need to enhance their energy efficiency. This thesis focuses on reducing the power and energy consumption of microdisplays while maintaining display luminance, and image quality; and enhancing key features such as resolution, refresh rate, and color depth.

First, a novel driving method and pixel circuit are proposed that reduces the number of subframes in a digitally-driven display. The dual-driver method offers flexibility in different design modes, allowing for the enhancement of various display characteristics. In the low-power mode, the operating frequency is reduced, resulting in decreased dynamic power consumption by the drivers. Experimental results on a proof-of-concept array fabricated using TSMC 65 nm technology demonstrate a significant 39% reduction in power consumption compared to a conventional array. Furthermore, designing the display in other modes yields remarkable improvements, with up to 8.5 times enhancement in refresh rate or resolution. In addition, the high color depth mode presents an opportunity to increase color depth from 8 bits to 14 bits, enhancing the visual experience.

Additionally, this thesis investigates power reduction techniques specific to row drivers in microdisplays. Circuit techniques are proposed to recycle energy in the row driver, thereby reducing dynamic power consumption. Measurement results on proof-of-concept arrays implemented in TSMC 65 nm technology reveal substantial reductions of up to 30% in the power consumption of the row driver using different energy recycling techniques. Applying these techniques led to a significant reduction in the dynamic power consumption of the row driver. For instance, employing the direct energy restoration technique resulted in a remarkable decrease of over 45% in the dynamic power consumption of the row driver.

Finally, a digital data driver with a data energy recycling feature is presented to further reduce the dynamic power consumption of microdisplays. Measurement results obtained from a proof-of-concept array fabricated using TSMC 65 nm technology demonstrate an average power consumption reduction of 16% in the display's data driver when subjected to randomly generated test images.

This thesis addresses the pressing need for energy-efficient microdisplays, offering innovative driving methods, pixel circuit design, and dynamic power reduction techniques. The proposed solutions provide significant power savings while preserving display quality and enabling enhancements in resolution, refresh rate, and color depth, contributing to extended battery life and improved user experience in portable electronic systems.

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Dedication

To the courageous women of Iran

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List of Abbreviations

AMOLED Active-Matrix OLED 2, 4, 12, 13, 18, 22, 23, 28, 43, 54, 55

AR Augmented Reality iv, 3–5, 7, 18, 87

CAGR Compound Annual Growth Rate 1, 3

CMOS Complementary Metal–Oxide–Semiconductor 5, 13, 22, 49

CRT Cathode Ray Tube 3

DAC Digital-to-Analog Converter 5, 13, 18–22, 89

DRAM Dynamic Random Access Memory 13

DUT Device Under Test 45

GUI Graphical User Interface 14

HMD Head-Mounted Devices 2, 3

IGZO Indium Gallium Zinc Oxide 11

LCD Liquid Crystal Display 2, 3, 14

LCoS Liquid Crystal on Silicon 3–5

LED Light-Emitting Diode 10, 23, 26, 30

LSB Least Significant Bit 24

MIM Metal-Insulator-Metal 48, 79, 82

MOS Metal Oxide Semiconductor 43, 48

MOSCAP Metal Oxide Semiconductor Capacitor 77, 79, 82

MSB Most Significant Bit 24, 27

NMOSCAP N-channel Metal Oxide Semiconductor Capacitor 47

NTE Near To Eye 3

OLED Organic Light-Emitting Diode x, xi, 3, 5, 6, 10, 11, 14–17, 20, 27, 29, 30, 32, 43, 44, 47–49, 54

OLEDoS OLED on Silicon 3–6, 43, 86

PPI Pixels Per Inch 5, 16, 54, 82, 85

PVT Process, Voltage, and Temperature 45

PWM Pulse Width Modulation x, xi, 13, 24–29, 33, 34, 42, 49, 50, 55

RGB Red, Green, and Blue x, 12, 18

SRAM Static Random Access Memory 13

SVGA Super Video Graphics Array 42

TADF Thermally Activated Delayed Fluorescence 10, 11

TFT Thin-Film Transistor 12

TFT-LCD Thin-Film Transistor LCD 2, 54

UHD Ultra-High-Definition 18

UI User Interface 16

UXGA Ultra Extended Graphics Array x, 3

VGA Video Graphics Array xi–xiii, 26, 27, 33, 37, 42, 45, 46, 51, 52, 76, 77, 80

VR Virtual Reality iv, 3–5, 7, 9, 18, 87

XGA Extended Graphics Array 16, 18

Chapter 1

Introduction

In recent years, the market for portable displays, particularly microdisplays, has witnessed substantial growth due to the escalating need for compact and portable devices. These displays have become an essential component in various applications, including but not limited to, virtual and augmented reality headsets, smartphones, and wearable gadgets. Nonetheless, the design challenges associated with microdisplays are quite significant, encompassing concerns related to power consumption, resolution, refresh rate, and display uniformity, among others. To sustain the growth momentum of the microdisplay market, it is vital to address these challenges effectively.

1.1 Portable Displays Technology and Market

Portable display technology has become an essential part of most portable electronic devices such as laptops, smartphones, watches, and smart wearable displays. The market for these devices is substantial and has been growing rapidly in recent years. A prime example of the portable display market is the global smartwatch market, which was valued at USD 30.4 billion in 2021 and is expected to grow at a Compound Annual Growth Rate (CAGR) of 20.1% from 2022 to 2030 [8].

The rise in demand for smartwatches across the world is due to the increasing inclination of consumers toward smart technologies and growing health awareness among consumers. With the increasing demand for smartwatches, the demand for smartwatch display panels is expected to surge in the market. The graph depicted in Fig. 1.1 illustrates the projected growth of the smartwatch display panel market until 2027, highlighting the growth for flexible and rigid panel types [1]. In addition, the rising advancements in smartwatch technologies and the integration of various latest technologies in smartwatches

Figure 1.1: Forecast of the smartwatch display panel market growth [1].

are estimated to fuel the growth of the smartwatch display panel market over the forecast period. The advent of flexible displays has enabled the development of rollable displays that can be used in smartwatches or fitness bands [9, 10]. Most smartwatches are powered by rechargeable lithium-ion batteries, making them convenient for on-the-go use. Battery life and display resolution are the two primary features that customers consider before purchasing smartwatches.

Active-Matrix OLED (AMOLED), Liquid Crystal Display (LCD), and Thin-Film Transistor LCD (TFT-LCD) are the most common display technologies used in modern smartwatches. Among these, AMOLED stands out for its many advantages. AMOLED displays are flexible and thin, making them an ideal choice for small wearable devices like smartwatches. The color reproduction of AMOLED displays is also superior to other technologies, with more saturated and vibrant colors. Additionally, AMOLED displays offer a faster touch response and are more battery-efficient, thanks to the technology's ability to only activate individual pixels. Another feature that sets AMOLED displays apart is the always-on display, which allows users to see important information at a glance without having to wake up the watch. However, one downside of AMOLED displays is that they can be more expensive than other technologies.

1.1.1 Microdisplay

Microdisplays are small displays usually less than two inches diagonal. The small size of these displays enables them to be used in cameras, projectors, and Head-Mounted De-

Figure 1.2: Photograph of the output image by 0.5-inch UXGA OLED microdisplay [2].

vices (HMD). Microdisplays are intended to be viewed indirectly using an optical system in projectors or they are intended to be viewed directly in HMDs for VR or AR applications. The earliest microdisplays have been used in Cathode Ray Tube (CRT) HMDs for military purposes in the late 1990s [11]. However, these days the popular technologies for microdisplay fabrication are LCD, Liquid Crystal on Silicon (LCoS), and OLED on Silicon (OLEDoS).

Microdisplays are playing a crucial role in Near To Eye (NTE) display market and they have been used in newly designed AR/VR HMDs for medical and gaming purposes. The market for AR and VR displays is expected to witness a substantial growth from USD 1.8 billion in 2023 to USD 8.2 billion by 2028, with a CAGR of 35.6% from 2023 to 2028, as reported in [12]. This market is being driven by a variety of factors including the increasing use of AR and VR HMDs across various industries, the rising popularity of Metaverse, and the adoption of these devices in the gaming industry. These factors are expected to have a significant impact on the market's growth in the coming years. Companies like Sony, eMagin, and Kopin are currently leading in the production of microdisplays. Sony's OLED microdisplay is widely used in high-end camera viewfinders and AR/VR devices. Fig. 1.2 shows a 0.5-inch UXGA OLED microdisplay of Sony corporation. On the other hand, eMagin is known for its OLED microdisplays, which are used in military and medical devices. In addition, Kopin is known for its LCoS microdisplay technology used in AR/VR devices. With the increasing demand for AR/VR devices and portable displays,

companies are focusing on developing high-resolution and low-power microdisplays to cater to the needs of the market.

Among different technologies, OLEDoS microdisplay is more suitable for AR and VR applications compared to LCoS, because of its desirable properties - no backlight requirement, its higher contrast ratio, and faster response time [13, 14, 15]. Employing silicon as the substrate in OLEDoS microdisplays makes it possible to have a high resolution, low power, and low cost[16, 17]. OLEDoS displays have the superiority in implementing the peripheral circuitry of the panel over displays implemented on amorphous silicon or polycrystalline silicon. In OLEDoS displays data and row driver, signal generator block, and DC-DC converters could be implemented along with the display panel on a single chip.

1.2 Portable Displays Design Challenges

Displays serve as a crucial component in the human-machine interface of nearly all portable electronic devices. Like other types of displays, designing a portable display requires careful consideration of factors such as resolution, cost, refresh rate, viewing angle, and fast response. Additionally, lightweight construction, low energy consumption, and flexibility are particularly essential features for portable device applications.

Designing portable displays that meet the strict requirements for size, weight, and power consumption can be challenging. These constraints impose a strict limit on battery size, making it crucial to design energy-efficient displays that can provide reasonable operating times for portable devices. This is especially crucial for healthcare devices, where battery life can be a critical factor in life-or-death situations. In terms of balancing power consumption with performance, AMOLED displays are among the most promising technologies. However, to further reduce power consumption, power-saving techniques such as reduced functionality mode and sleep state should be implemented when the hardware is not in use. Additionally, effective software management should be employed to maximize battery life while maintaining system performance. Typically, a significant portion of the energy budget in smart glasses is consumed by displaying video content on the microdisplay, which can quickly deplete the battery. To create energy-efficient displays, various techniques have been explored. These techniques have been found to be particularly effective for images with predominantly dark backgrounds or videos with a low data rate. By reducing the refresh rate or power supply of specific areas of the display, power consumption can be minimized without compromising the overall display quality [18, 6, 19]. However, designing displays with low power consumption becomes more challenging when the application requires bright images with a high data refresh rate. It is important to

note that many microdisplay applications, such as those for AR and VR, require high-speed video data rates.

To mitigate the challenge of small size requirements in portable displays, one possible solution is to leverage the standard Complementary Metal–Oxide–Semiconductor (CMOS) process. This approach is particularly useful for two widely-used technologies, OLEDoS and LCoS, as they can benefit from integrating peripheral circuitry with the pixel array [20]. This integration enables the consolidation of a complete display system, which includes a data driver, row driver, signal generator, and DC-DC converter, into a single chip, thereby improving the overall efficiency and functionality of the system. In order to achieve a high-resolution OLEDoS microdisplay, the pixel circuit should be simple enough to be integrated into a unit subpixel area of tens of μm^2. The luminance of the pixel circuit is proportional to the current density, and given the pixel area mentioned above, the OLED emission current should range from tens of pico-amperes (pA) to a few nano-amperes (nA) for a reasonable display luminance [21, 14, 13].On the other hand, using standard CMOS transistors as the driving transistors of the pixel circuit leads to currents in the range of hundreds of nano-amperes when a supply voltage is applied to the transistor gate. To reduce the current, the transistor should operate in the subthreshold region with a narrow gate voltage range. For OLEDoS displays that use analog data driving methods, designing a Digital-to-Analog Converter (DAC) for the data drivers is challenging when the data range is narrow. This requires a high-resolution DAC, or if increasing the resolution of the DAC is not feasible, it may cause a reduction in the number of display bits. Therefore, research has focused on increasing the driver's data voltage range in such microdisplays [22, 14, 23]. Note that using the digital driving method, the problem could be solved by reducing the highest voltage value that represents a value of '1'.

Portable displays are often required to have high resolutions and refresh rates to meet the demands of applications such as AR and VR or video gaming. Higher resolutions, measured in Pixels Per Inch (PPI), require more capacitance per data or row line, leading to an increase in dynamic power consumption for the data and row line buffers. Similarly, a higher refresh rate also increases the dynamic power consumption of the drivers. Thus, there exists a trade-off between reducing dynamic power consumption and meeting the higher resolution and refresh rate requirements of these displays.

Ensuring luminance uniformity has always been a challenging requirement for all displays. The main sources of non-uniformity are the threshold voltage variation of the driving transistor and the electrical characteristic variation of OLEDs. To overcome the V_{th} variation, most proposed methods divide the programming time into several phases [22, 13]. These methods store the threshold voltage value in one phase and then apply the data value in another phase in a way that eliminates the threshold voltage value from

the current equation. This makes the emission current independent of the variation in the threshold voltage of the driving transistor. However, using the digital data driving method reduces the effect of the V_{th} variation of driving transistors because the driving transistor operates in the linear region. Additionally, several internal and external compensation methods have been developed to solve the OLED characteristic variation over time.

1.3 Thesis Organization

The increasing demand for portable electronic devices has highlighted the need for low-power displays. This thesis introduces two novel methods that effectively reduce the dynamic power consumption of display drivers. Furthermore, one of these methods can also be utilized to enhance other features of the display, such as resolution, refresh rate, and color depth, depending on the requirements of the microdisplay application. The proposed methods can be employed to design low-power microdisplays suitable for use in portable devices. Ultimately, products equipped with these low-power displays will benefit from a longer battery life.

This thesis is organized as follows — In Chapter 2, an overview of existing low-power display designs is provided, along with the latest ideas to increase resolution, refresh rate, and color depth in such displays. Chapter 3 presents an introduction to the two most widely used data-driving methods for microdisplays and provides a comprehensive discussion of the digital data-driving methods. Chapter 4 of this thesis introduces a novel dual-driver pixel circuit and its peripheral row and data drivers that result in a significant reduction in the number of subframes and consequently, a substantial decrease in the power consumption of the drivers. The proposed dual-driver method can be utilized in different modes to enhance various display characteristics, and the highest enhancement achievable in each mode is thoroughly investigated. Additionally, since the maximum current for OLEDoS is in the nano-ampere range, a new signal processing technique is proposed in this chapter to modify the high level of the binary data voltage. Lastly, the results of the measurements using the dual-driver technique on a proof-of-concept array fabricated using TSMC 65 nm technology are compared with the conventional counterpart. Energy recycling techniques aimed at achieving low-power row and data drivers in OLEDoS microdisplays are presented in Chapter 5. Specifically, three new energy recycling techniques for the row driver are introduced, and a novel approach is proposed to reduce the dynamic power consumption of the data driver. To demonstrate the effectiveness of these techniques, three proof-of-concept arrays are implemented using TSMC 65 nm technology, and the power consumption of drivers utilizing our techniques is compared to that of conventional microdisplay drivers.

In Chapter 6, the contributions of this thesis are summarized, and potential directions for future research are discussed.

1.4 Summary

Nowadays, portable electronic devices are highly sought-after due to their diverse applications in healthcare, the military, and gaming. The display interface serves as the crucial point of interaction between humans and machines for these devices, including portable devices like VR and AR glasses that integrate microdisplays into their architecture. However, in displays, there is a trade-off between power consumption and higher resolution or refresh rate, and microdisplays are no exception. Therefore, it is crucial to explore energy-efficient microdisplay designs that do not compromise other essential features like brightness, resolution, and refresh rate.

Chapter 2

Low-Power and High-Performance Display Design Overview

The display industry is currently focused on improving various aspects of display technology, such as increasing resolution, refresh rate, pixel density, and color depth. While these advancements pose inherent challenges, they also give rise to additional concerns, notably higher power consumption. This becomes particularly problematic for portable devices that operate on battery power. In this chapter, we provide an overview of the state-of-the-art methods aimed at enhancing power consumption and other important features of displays.

2.1 Energy Consumption in Portable Devices

In today's world, portable devices have become an essential part of our daily lives. Most individuals possess a smartphone and laptop, and many also use tablets, smartwatches, fitness bands, and head-mounted displays, among others. As these devices operate on battery power, energy consumption is a crucial factor that requires attention and is often a significant selling point. For instance, the limited battery life of smartwatches that necessitates daily charging is a significant drawback. No smartwatch can operate for weeks while using all of its features.

To increase the battery life of a portable device, it is crucial to identify the contribution of each block to power consumption and determine the most power-hungry blocks. Authors in [3] and [24], have conducted research to analyze the average power consumption of each

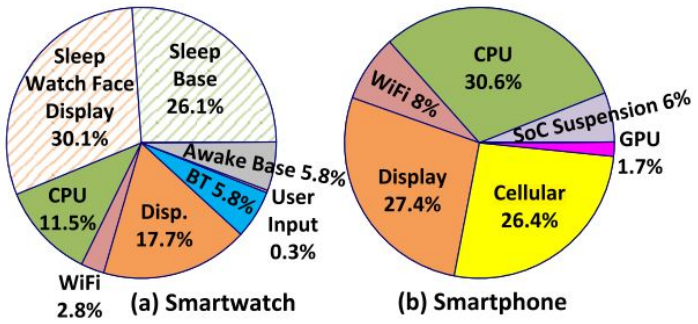


Figure 2.1: Component-level energy percentage breakdown averaged over all users for (a) smartwatches, and (b) smartphones[3].

primary block in smartwatches and smartphones. Fig. 2.1 shows the energy percentage breakdown of components in smartphones and smartwatches that averaged over users who participated in the research. The study revealed that the display of a smartwatch consumes 17.7% of the overall energy in active mode and 30.1% in sleep mode, while the display of a smartphone on average drains 27.4% of the overall energy. Hence, our research aims to propose low-power displays to reduce energy consumption from a significant energy-hungry block in portable devices.

2.2 Microdisplay Energy Consumption

As previously discussed, microdisplays find extensive applications in portable devices, particularly head-mounted devices, for exhibiting moving video images. In such devices, the system electronics and microdisplay transfer, process, and display large volumes of data, which can result in rapid battery depletion. To identify the primary sources of energy consumption in these devices, it is necessary to investigate the average power consumption of each key component. In a study conducted by Yan et al. [25], the power consumption of the microdisplay was measured in smartphone-based virtual reality applications. The results showed that the microdisplay consumed 47% and 51% of the system power in VR video and VR gaming, respectively, indicating that it is the primary power-consuming block in head-mounted devices. Therefore, reducing the energy consumption of the microdisplay is crucial for extending the battery life of these devices.

2.3 Low-Power Display Design

The study of low-power displays can be classified into three main categories: device, pixel circuit, and driving method. At the device level, researchers have focused on enhancing the power and energy efficiency of Light-Emitting Diode (LED)s for a given luminescence. This has resulted in the development of advanced technologies such as OLEDs and micro-LEDs, which continue to be the subject of intense research [26, 27, 28]. At the pixel circuit level, research has been focused on utilizing circuit techniques to improve dynamic power efficiency and reduce the leakage current of driving transistors [29, 30]. At the driving method level, the research focus is to reduce dynamic power consumption by proposing new data and row driver architectures along with its pixel circuit design. Some of these methods include reducing the supply voltage based on image content or employing adaptive refresh rate [18, 31]. In the following sections, we will provide a brief review of these techniques.

2.3.1 Device

Energy-efficient OLED technology has emerged as a promising solution to the power consumption challenges faced by electronic devices [32]. OLEDs consume less power than traditional LED displays as they do not require a backlight. Moreover, OLEDs have the potential to achieve high levels of luminance efficiency, which refers to the amount of light produced per unit of power consumed [33, 34]. Several research efforts have been devoted to enhancing OLED technology's power efficiency by improving materials and designing efficient structures [35].

Conducting research at the device level to identify the most suitable material for low-power OLED displays necessitates the exploration of novel materials with desirable characteristics such as charge transport properties, enhanced luminescence efficiency, and extended operational lifetimes [36, 37]. In pursuit of this objective, researchers have undertaken the synthesis and characterization of a diverse range of compounds encompassing fluorescent, phosphorescent, and Thermally Activated Delayed Fluorescence (TADF) properties, with the aim of achieving high-efficiency OLEDs [38, 39, 40].

One of the strategies for enhancing OLED material technology's energy efficiency is to improve the materials' charge transport properties, which can increase the efficiency of the device [41, 42, 43]. In general, the efficiency of the blue emitter is less than green and red emitters. So, there have been efforts to introduce highly efficient blue emitters that can be used in OLED displays [44, 45]. To enhance the blue emitter in OLEDs, research endeavours encompass several avenues. These include the utilization of TADF emitters,

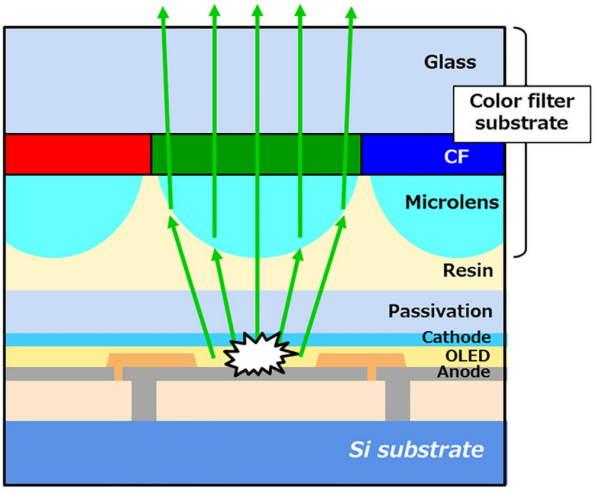


Figure 2.2: High-efficiency OLED device structure with microlens [4].

the development of exciton harvesting materials, the optimization of host materials, the introduction of specific dopant molecules, and the exploration of novel organic materials [46, 4]. TADF is a mechanism employed to enhance the efficiency and lifetime of OLEDs by capturing triplet excitons [47, 48]. In recent years, there has been significant research focused on enhancing the efficiency of TADF and reducing the driving voltage of OLEDs utilizing these compounds [49, 50]. These efforts aim to improve the performance and energy efficiency of OLED technology.

In [4], the authors proposed a high-efficiency OLED microdisplay utilizing a novel technology that incorporates a microlens array as shown in Fig. 2.2. The microlens structure facilitates the refraction of light emitted from the OLED at the interface between the microlens and the resin material, resulting in the accumulation and efficient extraction of light in the forward direction. As a result, the proposed OLED achieved three times higher efficiency compared to conventional OLEDs.

An additional area of research in device-level studies involves the development of a low leakage transistor characterized by a small I_{off} [51, 52, 53]. This research area holds significant importance, especially in the design of access transistors for pixel circuits [54]. By minimizing the leakage current, the pixel circuit can maintain its value for extended durations, resulting in a potential reduction in the refresh rate and dynamic power consumption. Authors in [30] used an Indium Gallium Zinc Oxide (IGZO) thin-film transistor with extremely low I_{off} in their pixel circuit design. They demonstrated that their proposed display can retain the state after switching off the power supply of the drivers for several

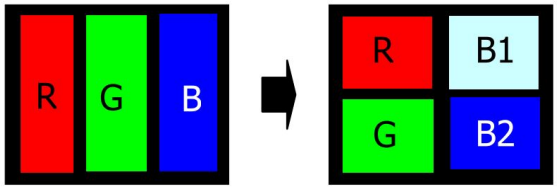


Figure 2.3: (a) RGB is replaced with (b) RGB1B2 for longer lifetime and lower power consumption [5].

hundred seconds. While this technique could be beneficial in reducing power consumption when the content needs a low refresh rate, it does not reduce the power significantly in other applications.

2.3.2 Pixel Circuit

Besides device-level approaches to save power in the display's panel, power saving could be considered while designing the pixel circuit. Here we will discuss some of the pixel circuit-level methods that are useful for power saving in displays.

As previously discussed, reducing the leakage current in the pixel circuit can lead to a decrease in the refresh rate and subsequently reduce dynamic power consumption. While efforts at the device level focus on proposing transistors with lower leakage, at the pixel circuit design level, novel pixel circuitry has been introduced to minimize the leakage current [55, 56]. Authors in [57] presented a novel pixel circuit design for low frame rate AMOLED smartwatch displays. The proposed circuit incorporates a leakage-prevention mechanism that aims to balance the leakage currents at the gate nodes of the driving Thin-Film Transistor (TFT)s.

As previously stated, due to the relatively lower efficiency of the blue emitter, the researchers in [5] proposed an innovative pixel architecture for a four sub-pixel AMOLED panel. Unlike conventional RGB display panels where the blue sub-pixel is fluorescent (Fig. 2.3a), all sub-pixels in their proposed architecture are phosphorescent, which results in better light efficiency (Fig. 2.3b). The new architecture includes two blue sub-pixels: a light blue sub-pixel (B1) that can effectively render most images, and a dark blue sub-pixel (B2) that is used only for high-saturation blue. Additionally, the proposed architecture eliminates the issue of the blue sub-pixel limiting the display lifetime, thus increasing

the panel's operational lifetime and reducing power consumption by 20%. Another low-power pixel architecture approach has been introduced in reference [58]. In this work, the authors proposed an alternative to the pentile-type architecture for AMOLED displays. The key innovation lies in separating the blue and red data lines, which were shared in the conventional pentile architecture. As a result of this separation, power consumption is notably reduced, especially for images with dominant red or blue colors.

The idea of using a standard CMOS Static Random Access Memory (SRAM) cell to design a low-power AMOLED display has been studied for several years [59, 60, 61]. Replacing the conventional 2T1C pixel circuit which is equivalent to a Dynamic Random Access Memory (DRAM) cell, with an SRAM cell enables the display to only refresh the image content when it is necessary. Hence, in low data rate applications, the dynamic power consumption will reduce significantly [29]. However, this method is limited to special applications and displays that use a digital driving method. Moreover, While it reduces dynamic power consumption, it also increases static power and as a result, the benefit is not that impressive.

Usually, the dynamic power consumption of the data driver is substantial. Thus, reducing this dynamic power could be favourable for low-power display design. In [19], the data signal is provided at the half range of 0 to $V_{DD}/2$ to achieve a considerable power saving. Moreover, a new pixel circuit has been proposed that exploits two different supply voltages of V_{DD} and $V_{DD}/2$, and the data will be converted to the full range inside the pixel circuit. While this method is promising to decrease the dynamic power consumption of data drivers and data lines, it increases the pixel area and uses two different supply voltages and extra control signals in the panel.

In displays that use the analog driving method, the power consumption of DACs and data line buffers are significant. Authors in [62] proposed a new pixel circuit with in-pixel digital-to-analog conversion and PWM technique to realize different grey levels inside the pixel circuit. Incorporating the function of DAC in pixel and using a digital data driver with low voltage swing instead of an analog data driver with DACs and buffers led to a low-power driver.

2.3.3 Driving Method

The next phase of enhancing power efficiency lies within the driving method and the architecture of the display driver. The driving method category encompasses advanced approaches aimed at reducing power consumption and energy usage in displays [63]. Typically, these state-of-the-art techniques incorporate advanced algorithms that utilize image

Table 2.1: Classification of display power saving techniques.

Techniques	**Features**	**Applications**	**Displays**
Idling	Not functional during low-power mode	Interactive applications	LCD and OLED
Partial idling or dimming	Disabling objects not of interest	Mixed active/idle objects	LCD and OLED
Color remapping	Altered look and feel	GUI	LCD and OLED
Backlight scaling	Minor color distortion	All	LCD
Supply voltage scaling	Requires pre-processing	All	OLED
Adaptive refresh rate	May cause image deterioration	Low data rate applications	LCD and OLED

content and employ pre-processing methods to effectively reduce power consumption.

Table 2.1 presents a classification of the prevalent power-saving techniques across various display technologies. The first category entails the implementation of display idling techniques when the user is not actively engaged with the device. This can be achieved by employing methods such as utilizing a camera to detect the user's eye gaze [64, 65] or automatically initiating display shutdown after a predetermined period of user inactivity. These techniques have universal applicability across all display technologies and effectively contribute to power consumption reduction.

Partial idling or diming offers advantages when specific parts of the display are relevant to the user, and there exists both foreground and background content [66]. These techniques conserve power by modifying the background objects' color to darker shades, reducing the luminance of the background content, or completely turning it off [67, 68]. Implementing such methods in LCD displays necessitates zoned backlighting, while OLED displays offer greater flexibility, allowing the dimming of specific sections of the display.

Color mapping technique involves reducing the power consumption of the display by altering the color of the image [69, 70, 71, 31]. Given the varying efficiency of OLED emitters, modifying the image's color can lead to significant reductions in power consumption. While this method proves advantageous for Graphical User Interface (GUI) applications, it is clearly unsuitable for natural images, photographs, or videos, where preserving color accuracy is crucial.

Another commonly employed technique to conserve power is by reducing the backlight intensity in LCD displays and compensating for the potential loss in image quality by enhancing the color and/or adjusting the contrast of the displayed image [72, 73, 74]. This

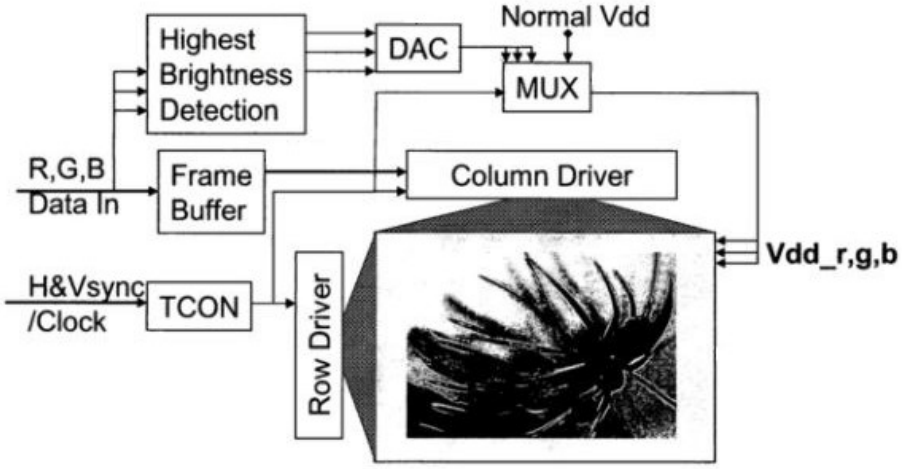


Figure 2.4: Low-power OLED display system with variable supply voltage based on the image content [6].

approach effectively achieves power savings while maintaining an acceptable level of visual quality [75, 76, 77].

In the analog driving method, driving transistors operate in the saturation region. For each gate-source voltage (each grey level), there is a freedom to reduce the drain-source voltage (V_{ds}) of the driving transistor while the transistor is still in the saturation region with almost the same current intensity [78, 6]. Exploiting this feature, authors in [6] proposed a method to reduce the power consumption based on the image contents. For example, when the current required for the highest brightness in a specific image is less than the maximum brightness that is achievable with the available supply voltage (V_{DD}), the supply voltage could be reduced while ensuring that the driving transistor is in the saturation region for all required grey levels. Fig. 2.4 illustrates one of the possible embodiments of their proposed method. Unlike a typical display system that has a global supply voltage, in this system, a specific V_{DD} connection is used for each color. The mentioned method is explicitly for the displays that use the analog driving method. Similarly, in [18] a system is provided that monitors the content of a selected segment of the display and adjusts the supply voltage of the driving transistors in that segment according to the required data values of that segment. Implementing supply voltage scaling in digitally driven displays poses greater challenges. Directly scaling the supply voltage has a significant impact on the current flowing through the OLED and the resulting brightness

of the pixel circuit. Consequently, algorithms must be employed to compensate for image degradation and restore luminance. However, the extent of restoration achievable through this method is limited, and in cases where the original OLED current is excessively high, the image compensation may not fully restore the original luminance [78].

Another widely used low-power technique is the adaptive refresh rate method [79, 31]. This approach enables dynamic changes to the frame rate of the display based on the content of the image to be displayed [80, 81]. In instances that require precise video quality, the display is typically operated at higher refresh rates (above 60 Hz). However, in other video modes such as mobile video capture and streaming, lower refresh rates (25-30 fps) are commonly used. For low data rate modes such as User Interface (UI), static images, and text, the refresh rate can be reduced (1-15 fps) to achieve substantial power savings. This approach may potentially lead to image deterioration or introduce noticeable flicker artifacts. In [82] an ultra-low-power backplane and system are proposed that utilizes static memory in each pixel circuit in order to eliminate the unnecessary data transfer and reduce the needless refresh cycles. Therefore, only the changing part of the display will be refreshed and if the content of the image or video is not changing the data transfer circuits can go idle to even use less power.

2.4 High-Performance Display Design

In addition to power consumption, factors such as cost, uniformity, resolution, refresh rate, color depth, and response time hold significant importance for display design, depending on the specific application and available resources. This section will explore various novel approaches and concepts aimed at enhancing resolution, color depth, and refresh rate.

2.4.1 Resolution

Display resolution is the number of distinct pixels in each dimension. It is commonly referred to as $width \times height$ with the units in pixels. For example, an Extended Graphics Array (XGA) display resolution is 1024×768. This means that the width and height of an XGA display consist of 1024 and 768 pixels, respectively. On the contrary, the term display resolution sometimes describes the pixel density which is the number of pixels per unit distance or area. Pixel density is usually reported by PPI. For example, an XGA display whose dimensions are 12 inches by 9 inches, has a resolution of approximately 85 PPI. In this thesis document, we use the former definition of resolution.

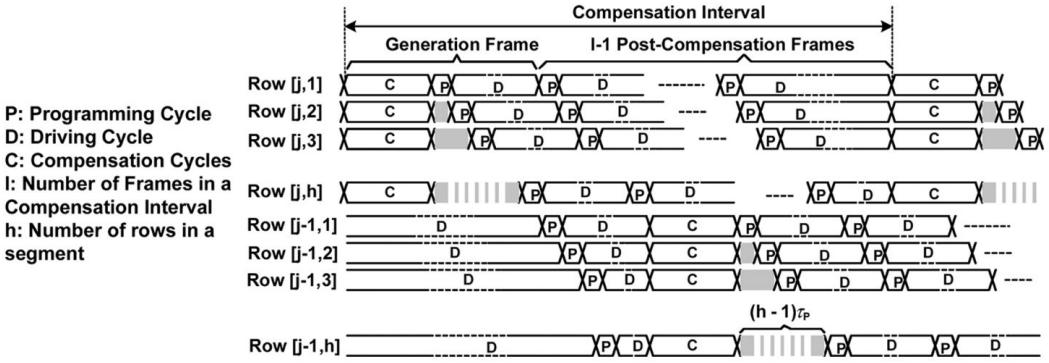


Figure 2.5: Interleaving addressing scheme for high-resolution and low-power displays [7].

Generally, increasing the resolution will inversely affect the available programming time of each row since the row driver should scan the whole rows in the same timing budget of a frame. Hence, the gate voltage may not reach the desired value in the available short programming time.

To develop a high-resolution display, high-speed operation of pixel circuits is required. Moreover, most displays utilize a technique to compensate for the OLED luminance degradation over time. Authors in [7] provided a new high-resolution parallel addressing scheme. This scheme increases the speed of the display panel without limiting the programming time. It separates the compensation operation from the input data operation. In this method, a rather wider compensation time is specified to generate the threshold voltage (V_{th}) for several rows and frames simultaneously. Fig. 2.5 shows the proposed interleaving addressing scheme. In this figure, I is the number of frames in a compensation interval and h is the number of rows in a segment of the display that their compensation operation is in parallel. Since the compensation operations for several rows occurs concurrently and only the data input operations are one at a time, a considerable time slot of the frame will be saved that could be used to increase the resolution of the display panel. However, This method needs complicated circuit operations and complex control signals especially in the V_{ss} line which may cause circuit instability.

In a high-resolution display design, it is a challenge to provide an adequate compensation time for each row to capture the correct value of the threshold voltage and this limits the highest resolution achievable for the display panel. Therefore, authors in [83] proposed

a new compensation and driving scheme in which the compensation time is independent of the display resolution. This empowers the designers to achieve Ultra-High-Definition (UHD) resolution for AMOLEDs. The proposed method specifically works for analog driving methods and it needs extra control signal lines and a relatively complex row driver.

Another limitation of a high-resolution display with the analog driving method is the slower charge time for lower data levels. Authors in [84] provide a high-speed analog driving architecture that could be used in high-resolution display panels. Using the controlled amplitude precharge technique, their proposed method reduces the convergence time and enables high-speed operation.

The previous methods provide a higher display resolution by introducing high-speed driving methods. However, reducing the pixel pitch to increase the resolution for a display with a fixed size is also popular, especially in VR and AR applications [85]. This latter solution is practical when the programming time is not the limiting factor to increase the resolution. Instead, the major limitations are the pixel circuit area and the constraints for the whole display size. For this purpose, pixel circuits that employ simple structure have been proposed that while they do compensate for the threshold voltage variation, they also have a small area [86, 87]. One commonly employed technique to decrease the pixel pitch involves reducing the number of data lines, row lines, or both within a display [88, 89]. This reduction effectively reduces the pixel area, resulting in a higher-resolution display. However, miniaturizing the pixel circuit leads to an increase in luminance variation, and as a result, the luminance uniformity of the display decreases.

2.4.2 Refresh Rate and Color Depth

A high refresh rate is key to a great user experience, especially in AR and VR applications which results in a fast user interface response. High-end displays today run at 144Hz, while 60Hz, 90Hz, and 120Hz displays constitute the majority of displays in the market. Assuming an XGA display that runs at 90Hz, the available programming time for each pixel is 14.4us in the analog driving method. Increasing the refresh rate leads to lower programming time for each row, as a result, the available time may not be sufficient for the storage capacitor to reach the final value of data or execute a proper threshold voltage compensation. Thus, new driving methods are desired to obtain higher refresh rates.

Color depth is the number of bits used to indicate the color of a sub-pixel. A color depth of 8 for each RGB sub-pixel is equal to 16777216 color variations for the display (i.e. $2^8 \times 2^8 \times 2^8 = 16777216$). For displays with the analog driving method, the color depth is determined by the precision of the DAC. Therefore, there have been a lot of attempts to

increase the number of bits (i.e. precision) of DACs in recent years [90, 91, 92]. On the other hand, in displays with the digital driving method, the color depth is proportional to the programming time budget. In this method, a color depth of 8 is equal to at least 8 subframes (i.e. set of programming and emitting time slots) in each frame. Therefore, the color depth is in a trade-off with the display's resolution and refresh rate. For example, increasing the resolution leads to less programming time available for scanning the display, thus it is necessary to reduce the number of subframes for proper operation. As a result of the reduction in the number of subframes the color depth of the display decreases.

All driving schemes that offer a high-speed programming time could be exploited to increase the refresh rate and color depth instead of increasing the resolution [7, 83, 93]. Moreover, one can use the techniques to increase all of these factors to some extent based on the application requirement.

2.5 Summary

The primary energy resource of portable devices is rechargeable batteries with a limited lifetime, so exploiting power-efficient blocks is necessary for such devices. Usually, the display panel is the most power-hungry module in a portable device and it is essential to improve the energy consumption of that. Similarly in portable devices that exploit microdisplays, this module is the most power-hungry block. Hence, utilizing a power-efficient microdisplay reduces the overall power consumption of the device significantly. On the other hand, resolution and power are the most demanding factors in portable displays. We have mentioned some of the existing ideas to improve these features in both displays and microdisplays. The focus of almost all existing methods is to just improve one factor. Moreover, previous ideas are applicable to a specific driving method. Thus, a general method to improve these factors on every display regardless of the driving method is desirable.

Chapter 3

Data Driving Methods and Conventional Display Architecture

Microdisplays can be driven using either analog or digital data-driving methods. In general, digital driving methods offer advantages such as higher tolerance to pixel luminance variation, simpler driver circuitry, and lower energy consumption. This can be attributed to the elimination of the power-hungry DAC and the operation of the driving transistor within the pixels in the linear region, the two primary factors responsible for the decreased power and energy consumption in digital displays when compared to their analog counterparts.

This chapter explores the two widely used methods for data driving in displays: analog and digital. For each method, the conventional display architecture is illustrated. Subsequently, our attention shifts towards discussing the popular digital data-driving methods, accompanied by a comprehensive analysis of their inherent merits and limitations.

3.1 Analog Driving Method

Although analog driving methods for high-resolution OLED microdisplays are known to exhibit high power and energy consumption, as well as a more complex driver, they continue to be widely used and have been the subject of research in recent years [2, 87, 21]. The uniformity of luminance is a crucial criterion for microdisplays, and various techniques have been suggested to address luminance-related issues in microdisplays that utilize analog driving methods [22].

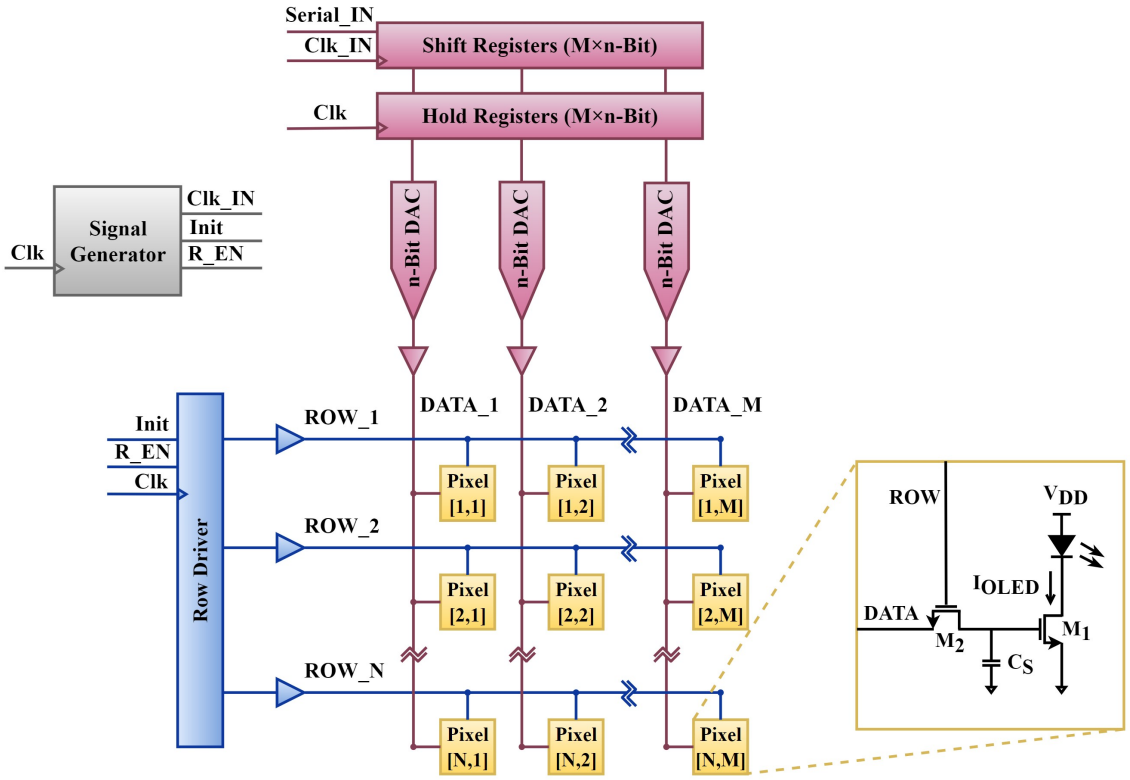


Figure 3.1: The conventional $N \times M$ active matrix display with the analog data driving method and its pixel circuit.

Fig. 3.1 illustrates a conventional analog-driven display and its pixel architecture. Considering an n-bit color depth, the analog driving method necessitates an n-bit DAC for each data line to convert digital data from the hold register into an analog voltage. To accommodate this conversion, both shift and hold registers have a size equivalent to $M \times n$, where M corresponds to the number of columns in the display. This sizing is imperative to ensure that all data bits are simultaneously available for the analog voltage conversion. The signal generator generates the necessary control signals for both the row and data driver. The Init signal is utilized to initiate the scanning process of the row driver, while the R_EN signal ensures that the row signal is enabled during a specific portion of the programming time. This ensures that the data value is stable before enabling the row.

Fig. 3.2 shows the timing diagram for a frame using the analog data driving method. An 8-bit DAC is utilized to provide the analog grey level of data for the data line when the color depth is 8 bits. As demonstrated, the activation of the access transistors (i.e., M_2

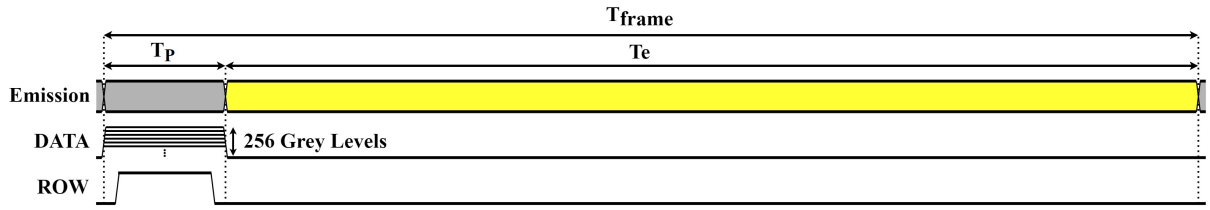


Figure 3.2: The timing diagram of a frame with the analog data driving method.

transistors) of pixels in a particular row is achieved by the ROW signal. Following this, the storage capacitor (C_S) of each corresponding pixel is charged by its respective analog data line. Subsequently, during the emission period of this particular row, the row driver scans the remaining rows in the display and sets the storage capacitors to their intended analog grey levels.

The analog approach for compact microdisplay applications has a significant disadvantage wherein the size of the DAC and buffer amplifier is considerably larger than that of a data line. In order to address this issue, Kimura *et al.* [86] proposed the use of selective analog switches to share a single DAC among multiple data lines. Although this approach helps reduce the area, the programming time available for each row decreases as the number of data lines sharing a single DAC increases.

3.2 Digital Driving Method

In contrast to the analog data driving technique where the driving transistors operate in the saturation region, the digital driving approach merely involves switching the pixel on or off, with the driving transistor operating in the linear region. As previously mentioned, digital displays consume less energy and are easier to integrate into fully digital systems. The digital method divides each frame into several smaller subframes to achieve this. The level of perceived luminance is modulated by the overall duration for which pixels remain turned on within a given frame. Displays utilizing digital driving, unlike their analog counterparts, do not require a DAC or an analog buffer array, resulting in a simplified circuit architecture and design flow. Mizukami *et al.*[94] constructed the first prototype of a digitally-driven AMOLED display that exhibited enhanced resolution and superior image uniformity when compared to its analog equivalents. An additional benefit of the digital driving method is that, due to the lack of a DAC, the potential for attaining higher resolution microdisplays increases as the size of CMOS technology shrinks.

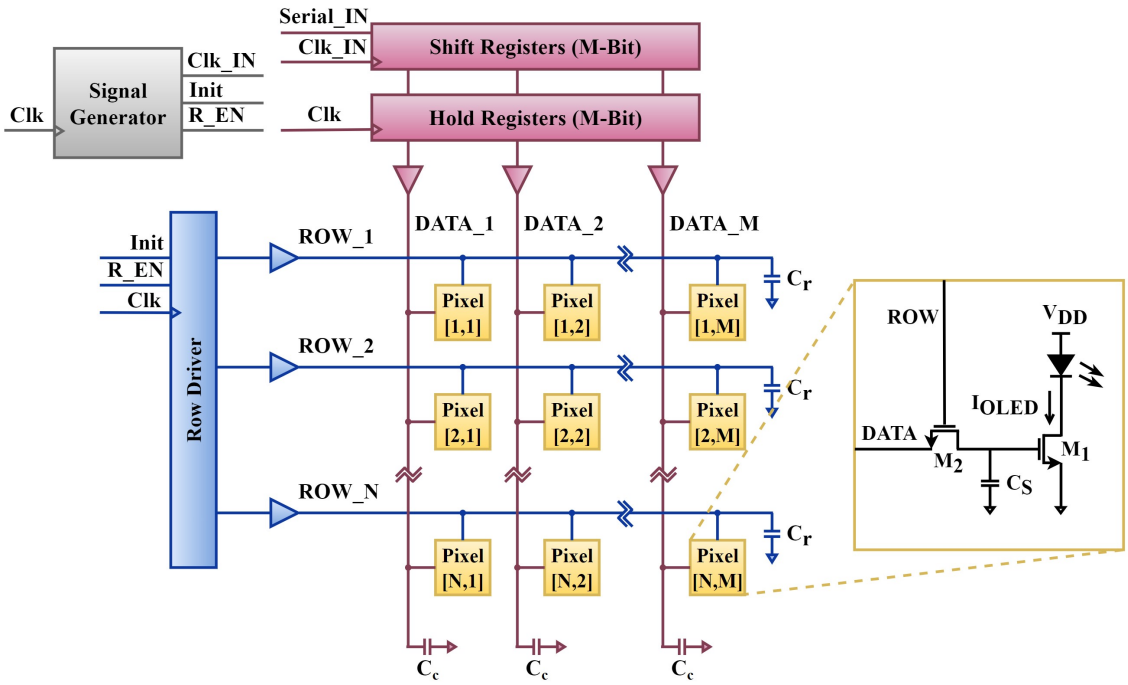


Figure 3.3: The conventional $N \times M$ active matrix display with the digital data driving method and its pixel circuit.

Fig. 3.3 illustrates the peripheral circuitry (i.e., data and row driver and the signal generator) and the pixel array of an $N \times M$ AMOLED display using the digital data driving method. The data driver consists of a shift and a hold register of size M and data line buffers are responsible for charging and discharging the data lines with proper data values. The size of the shift and hold registers is equivalent to the number of data lines since, during each programming cycle, each pixel in a row is programmed by a single bit/slice of data. The row driver also consists of a shift register that enables one row at a time using row buffers. The pixel circuit adopts the widely used 2T1C architecture. For simplicity, we assume that the driving transistor is an NMOS and the LED is connected between V_{DD} and the drain of the driving transistor. The signal generator block generates all control signals required for the operation of the data and row driver. It produces the fast clock signal (Clk_IN) for the data driver's shift register, the Init signal to initialize the scanning process, and the R_EN signal to enable the row line for a specific subset of the programming time when the data value is in a stable state.

Here we show the overall capacitance of a row line with a capacitor named C_r at

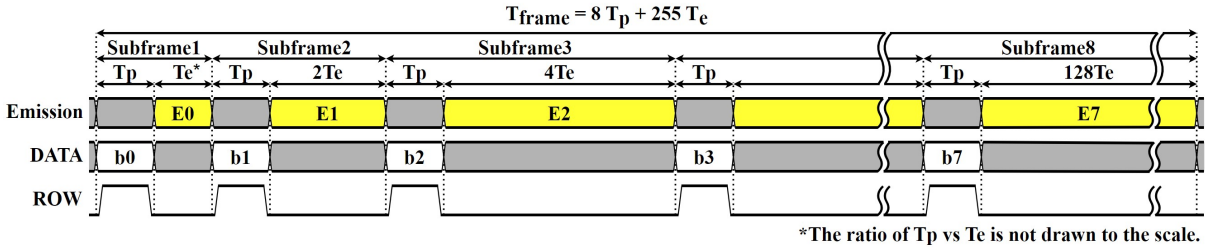


Figure 3.4: The timing diagram of a pixel in a frame with the weighted PWM method.

the end of each row. This is not an actual capacitor, and it only represents the total parasitic capacitance of the interconnects and the gate capacitance of pixel circuits in a row. The latter is a nonlinear capacitor that changes with the voltages applied to the access transistor's terminals. Similarly, C_c represents the total capacitance of each data line. This capacitor is used to represent the total parasitic capacitance of the interconnects, as well as the source/drain capacitance of access transistors on a data line.

Two commonly used digital driving methods are weighted PWM and unweighted PWM. In this section, we will explore and compare these methods.

3.2.1 Weighted PWM Method

The weighted PWM method for data driving involves subframes with emission times that vary based on the weight of the bit in the binary representation of the data [95]. The timing diagram depicted in Fig. 3.4 illustrates the waveforms of a weighted PWM data driving method for a display with an 8-bit color depth. Assuming b0 represents the Least Significant Bit (LSB), its emission time is equivalent to $2^0.T_e = T_e$, while the emission time for b1 is twice as long, and so on. Consequently, for the Most Significant Bit (MSB), the emission time is $2^7.T_e = 128T_e$. A frame time of the weighted pulse-width modulation method is

$$T_{f\_W} = n\,T_{p\_W} + (2^n - 1)\,T_{e\_W}. \tag{3.1}$$

Here, n is the color depth or the number of bits used to represent each color in the display. Additionally, the programming time and emission time for a single row in the weighted PWM method are denoted by T_{p_W} and T_{e_W}, respectively. In general, to ensure that all rows in the display are programmed with the appropriate data, the row driver must scan through the remaining rows of the display during the shortest emission time of

a specific row. As a result, the emission time for each row must exceed the time required to program the rest of the display. We can express this requirement mathematically as:

$$T_e \geq (N-1)T_p \tag{3.2}$$

where N is the number of rows in the display. Considering the minimum feasible emission time from Eq. 3.2, Eq. 3.1 is rephrased as follow:

$$T_{f\_W} = [n + (2^n - 1)(N-1)]\, T_{p\_W}. \tag{3.3}$$

Once the refresh rate (RR) of a display is known, the frame time (T_f) can be calculated as $T_f = 1/RR$. With this information, it is possible to determine the available programming time for each row with this method. It is important to note that a longer programming time allows for lower frequency and power consumption in the drivers, or higher resolution and color depth in the display. Therefore, the amount of time available for programming each row (T_p) plays a crucial role in determining the data and row drivers' frequency. Since T_p and the drivers' frequency are proportional to each other, T_p can serve as an indicator of the display's frequency and overall performance.

One of the limitations of the unweighted PWM method is that the data transfer rate to the display is not constant during a frame, resulting in a potential bottleneck when increasing the resolution and color depth of the design. To address this, Ji et al. proposed a modified weighted PWM method in [96], which reduces the data transfer bandwidth by tactfully adjusting the bit scan sequence.

3.2.2 Unweighted PWM Method

The unweighted PWM digital data driving method with a color depth of 8 bits, has 255 subframes (i.e. programming and emission time slots) during each frame time (Fig. 3.5). For example, if the grey level for a pixel is 50 in a frame, during 50 out of 255 programming times, logical '1' will be stored in the storage capacitor of the pixel circuit while for the rest of them (205) logical '0' will be stored. As shown in Fig. 3.5, D1 to D255 represent the DATA value for each subframe that could be logical '1' or '0', based on the total grey level. The access transistor of each pixel is turned on and off 255 times during a frame and the emission time is equal after all programming times. A frame time for the unweighted PWM data driving method is

$$T_{f\_UW} = (2^n - 1)\,(T_{p\_UW} + T_{e\_UW}). \tag{3.4}$$

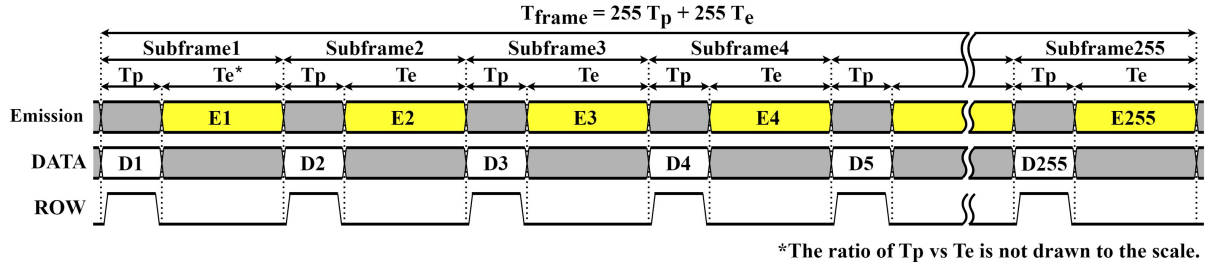


Figure 3.5: The timing diagram of a pixel in a frame with the unweighted PWM method.

Based on the minimum feasible emission time for each subframe in Eq. 3.2, the previous equation has been rephrased as:

$$T_{f\_UW} = N\,(2^n - 1)\,T_{p\_UW}. \tag{3.5}$$

If the refresh rate of the display is known, the frame time can be calculated. Eq. 3.5 can then be used to determine the maximum programming time available for the unweighted PWM data driving method, based on the color depth and number of rows in the display.

3.2.3 Comparison of Unweighted and Weighted PWM Methods

Generally, during the programming times, the LEDs are not emitting light or the emitted light is not in accordance with the desired grey level. Therefore, to have better image quality, it is preferred to use a method that requires fewer programming times per frame. Eq. 3.6 and Eq. 3.7 calculate the percentage of overall programming time per frame for the weighted and unweighted methods, respectively.

$$\frac{Total\ T_{p\_W}}{T_{f\_W}} = \frac{n\,T_{p\_W}}{[n + (2^n - 1)(N - 1)]\,T_{p\_W}} = \frac{n}{n + (2^n - 1)(N - 1)} \tag{3.6}$$

$$\frac{Total\ T_{p\_UW}}{T_{f\_UW}} = \frac{(2^n - 1)\,T_{p\_UW}}{N\,(2^n - 1)\,T_{p\_UW}} = \frac{1}{N} \tag{3.7}$$

Based on the equations mentioned above, the percentage of programming time to the whole frame time in the weighted and unweighted scheme for a color depth of 8 bits and a full VGA (480×640) size display is 0.006% and 0.2%, respectively. As the weighted PWM method needs less programming time in a frame, the image quality is better in this method.

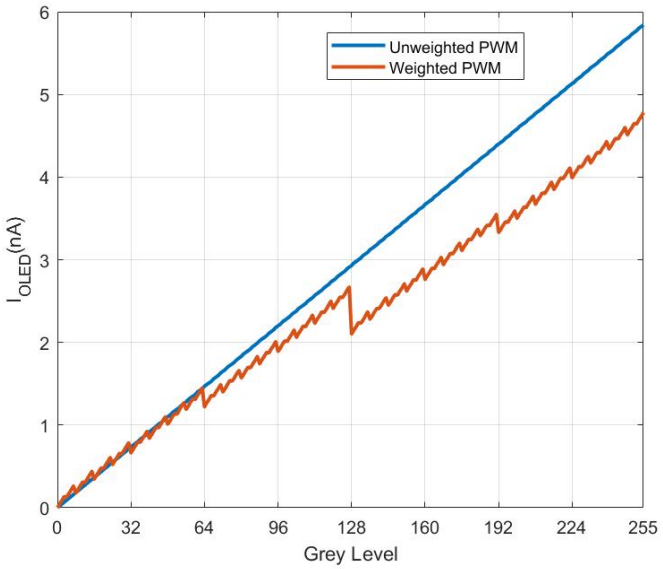


Figure 3.6: The grey level linearity for unweighted and weighted PWM methods.

Although the weighted method is superior to the unweighted method in image quality, the situation is reversed when the grey level linearity is desirable. Fig. 3.6 illustrates the simulation results for the grey-level linearity of these methods. In this simulation, we used the conventional 2T1C pixel circuit depicted in Fig. 3.3 and a VGA-sized display. The C_S value is 20fF, and the W/L size of M_1 and M_2 transistors are chosen as $1.7um/0.5um$ and $0.4um/0.5um$, respectively, in TSMC 65 nm Technology. Moreover, the high voltage to represent logical '1' data is 0.4V.

As shown in Fig. 3.6, the weighted method exhibits several fractions in its grey-level linearity. This is due to the voltage drop that occurs across the storage capacitor and the non-uniform emission times in this driving method. During the programming of the (MSB), the voltage across the storage capacitor should be maintained for approximately half of the frame time (i.e., E7 in Fig. 3.4). As a result, the voltage drop across the storage capacitor (C_S) will affect the desired current flowing through the OLED. As an example, the largest non-linearity occurs during the transition from a grey level of 127 to 128. In this case, the binary representation of 128 is "10000000". As a result, logical '1' is stored during the last programming time (i.e., b7), and the capacitor must maintain the voltage for the long emission time of E7. On the other hand, the situation is different for the grey level of 127. The binary representation of this grey level is "01111111", indicating that during the

first seven programming times (i.e. b0-b6), the logical '1' value is stored on the capacitor, and the emission times are shorter. Consequently, the voltage drop in grey level 127 is lower than in grey level 128. To improve the linearity of the weighted method, additional programming times can be added to restore the data values during the long emission times of the more significant bits. In [97], the authors suggested a driving technique for flexible AMOLED displays that divide the emission time of the more significant bits and place these segments between the subframes of lower significant bits. This method enhances the linearity of the grey level and increases the color depth of the display. Reducing the leakage current of the access and driving transistors is another solution to minimize the voltage drop. Alternatively, a larger storage capacitor could be used. However, this would increase the pixel circuit area and decrease the display resolution, which is not ideal. Therefore, there is a design trade-off between the resolution and the grey-level linearity of the display.

3.3 Summary

The digital data driving method is preferable for power-efficient microdisplay designs due to its simpler peripheral circuitry and greater area efficiency. Among the two commonly used digital driving methods, the unweighted PWM method offers improved linearity at the cost of requiring a higher number of subframes, which in turn leads to increased dynamic power consumption. As digital methods typically involve a higher number of subframes compared to analog counterparts, it is crucial to develop techniques that effectively reduce the dynamic power consumption of these subframes. Implementing such methods would greatly contribute to additional power savings in microdisplays, further enhancing their overall energy efficiency.

Chapter 4

Proposed Dual-Driver Pixel Circuit and Associated Drivers

The digital data driving methods necessitate multiple subframes within a frame to represent a particular shade of grey. As the color depth of a display increases, so does the required number of subframes, resulting in higher dynamic power consumption of the drivers. This chapter introduces a novel driving method and its corresponding pixel circuit designed to reduce the number of subframes needed while maintaining the same color depth and image quality. This is achieved by simultaneously programming two sets of data information during each programming cycle. We selected the weighted PWM data driving method as the reference method for this chapter due to its lower number of subframes per frame.

4.1 Dual-Driver Pixel Circuit

The proposed idea divides the data bits into two smaller segments and each sub-data has a lower number of bits, however, all segments put together, provide the same dynamic range of data. By means of multiple drivers in each pixel, each sub-data participates in the light intensity separately and the summation of currents from those drivers produces the same amount of current that a conventional pixel circuit will produce for that data. Assume a display with n-bit color depth, by dividing data into two (n/2)-bit segments, the OLED is driven separately for each part of data by means of two drivers. As shown in Fig. 4.1, the data is divided into two segments and each segment has its own driver to control the desired current for that segment. We refer to the piece of data and the data line which

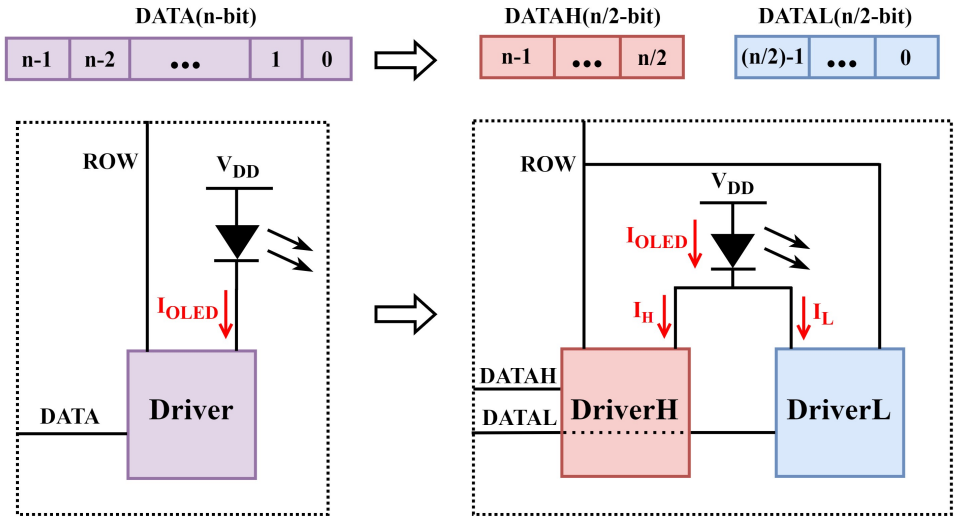


Figure 4.1: Splitting data into two segments and driving each one separately.

corresponds to more significant bits as DATAH and the one with less significant bits as DATAL. Assuming both drivers are in the on state, hence,

$$I_H = 2^{\frac{n}{2}} \times I_L \tag{4.1}$$

where I_H and I_L are the currents associated with DriverH and DriverL, respectively. At each programming time, a pair of data bits will be programmed, and the weight of the bit associated with DriverH is $2^{(n/2)}$ times more than the bit associated with DriverL (DriverL drives less significant bits of the DATA). To guarantee the same brightness of OLEDs for each data value, the drivers are designed so that for each grey level, the OLED average current during a frame of a dual-driver pixel circuit is equal to the OLED average current during a frame of the conventional pixel circuit. So, it can be expressed as:

$$\overline{I_{OLED\,conv}} = \overline{I_{OLED\,prop}} = \overline{I_H} + \overline{I_L}. \tag{4.2}$$

Without loss of generality the conventional 2T1C pixel circuit shown on the left of Fig. 4.2, has been chosen as the baseline pixel circuit that has NMOS driving (M_1) and access (M_2) transistors, and the LED is connected between V_{DD} and the drain of M_1. The right-hand image of Fig. 4.2 shows the dual-driver pixel circuit. There are two sets of drivers in this pixel. DriverH consists of transistors M_3 and M_5, and capacitor C_{S1}. DriverL consists

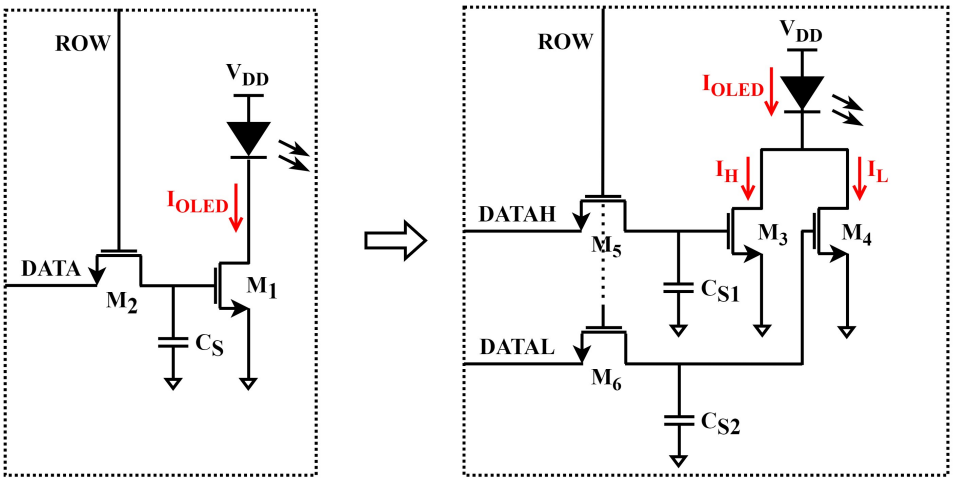


Figure 4.2: The conventional 2T1C pixel circuit and the dual-driver counterpart.

of transistors M_4 and M_6, and capacitor C_{S2}. For 8-bit color depth, the M_4 current (I_L) should be 16 times smaller that the M_3 current (I_H) based on Eq. 4.1. We will discuss the implementation details of the dual-driver pixel circuit design later in Section 4.5.

The dynamic power consumption of a circuit can be determined using the widely recognized equation provided below:

$$P_{dyn} = \alpha C_L V_{DD}^2 f \tag{4.3}$$

where C_L represents the capacitive load, f corresponds to the operational frequency, and α denotes the switching activity. With this equation in mind, driving two sets of data in parallel with the dual driver method reduces the number of required subframes. Therefore, the frequency of drivers and associated dynamic power consumption is reduced, as described by 4.3. Reducing the number of subframes by half can also improve other important features of a display such as color depth, refresh rate, and/or resolution. In this thesis, we restrict to a dual-driver pixel circuit. However, as it may be apparent to the reader, the concept of two drivers can be extended to three or more drivers with a further reduction in the number of subframes. Thereby, the associated benefits are more, yet they come at the cost of increasing pixel complexity.

Expanding the dual-driver concept to accommodate a greater number of drivers presents the potential to further reduce the number of subframes. Theoretically, increasing the driver count results in a reduced number of subframes, with the anticipated benefit of

lowering power consumption or enhancing other display features. However, the practical implications of increasing the number of drivers are noteworthy. This approach would enlarge the pixel circuit area and necessitate additional data lines, making it challenging to implement in high-resolution displays requiring a dense pixel configuration. Moreover, increasing the number of drivers also amplifies the intrinsic capacitance of a row line and increases the load on data line buffers, as more data lines must be charged or discharged. When dealing with a higher number of drivers, these added capacitances contribute to an increase in dynamic power consumption, which could potentially negate the expected power reduction benefits.

The 2T1C pixel circuit used as the baseline here requires a compensation technique to enhance its luminance uniformity, Extensive research has been conducted to address this issue [95, 98]. To maintain uniformity of display and mitigate the adverse effects of OLED degradation and aging in the proposed dual-driver pixel circuit, one potential method is to fine-tune the highest voltage stored in the storage capacitor as a logical 1 to adjust the current flowing through each driving transistor. It is important to note that the main objective of this research is to propose a new driving method that is low-power and/or high-performance. The designer is free to choose a compensation method that suits their needs to ensure a uniform display in the dual-driver pixel circuit.

4.2 Dual-Driver Display Architecture

Fig. 4.3 shows the proposed $N \times M$ dual-driver display architecture and its pixel circuit. Each column consists of two data lines to provide DATAH and DATAL to each pixel in a given row. In this architecture, at first, the shift register stores the data associated with the less significant part of the data (DATAL). When DATAL for a row is ready, data in the shift register will be stored in the hold register. Next, by disabling the SET signal (SET='0') the intrinsic capacitors of the DATAL lines are charged or discharged, according to the stored values in the hold register. Afterward, in the next cycle, the values in the hold register will be updated with the data associated with the more significant part of the data. The select line of the demultiplexer changes to SET = '1', and the values in the hold register may charge or discharge the DATAH lines' intrinsic capacitor. At this time, the DATAL lines are in the tristate mode, and later the data values will be transferred to C_{S2} capacitors by charge sharing. Note that the driving transistor (M_4) is designed based on the maximum voltage that will be delivered to C_{S2} after the charge sharing. When both data line values are stable, the row signal is enabled. Consequently, DATAH and DATAL are stored on two storage capacitors (i.e., C_{S1} and C_{S2}) in a pixel circuit at the same time

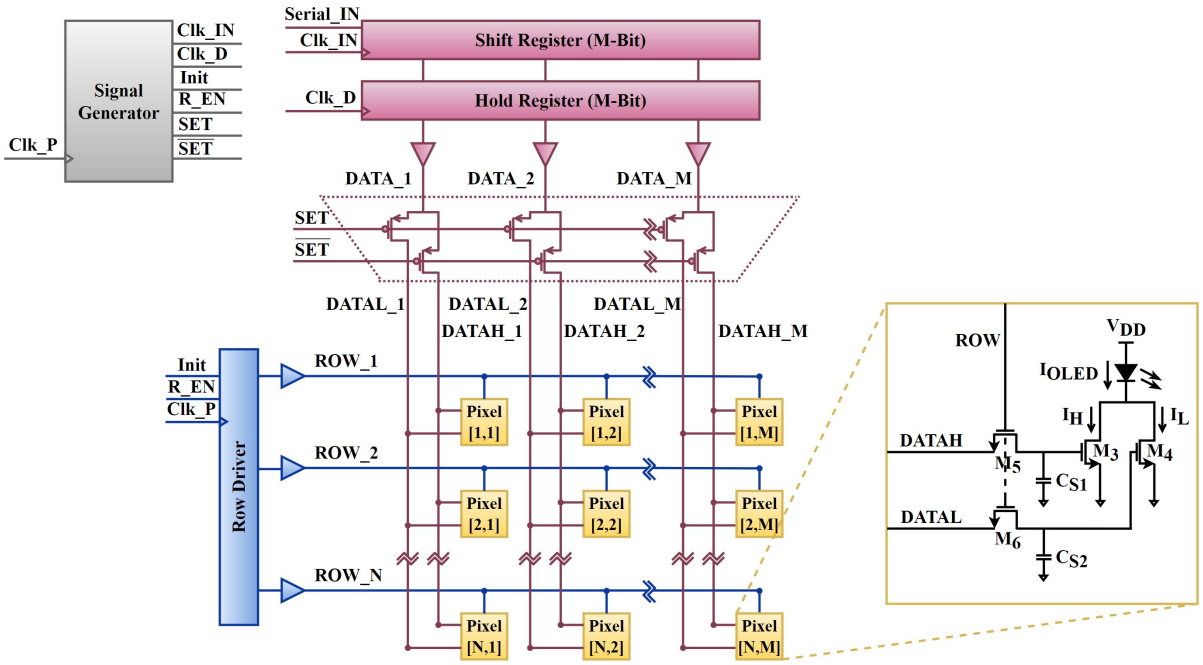


Figure 4.3: The dual-driver architecture for an $N \times M$ active matrix display and its pixel circuit.

and each contributes to the light intensity depending on the data value.

As mentioned earlier, the baseline driving method chosen here is the weighted PWM driving method. We can rewrite the frame time equation from Eq. 3.3 as follows for a conventional display using the weighted PWM data driving method:

$$T_{f_{conv}} = [n_{conv} + (2^{n_{conv}} - 1)(N_{conv} - 1)]\, T_{p_{conv}} \tag{4.4}$$

where $T_{p_{conv}}$ is the programming time, n_{conv} is the color depth or the number of bits, and N_{conv} is the number of rows in the conventional display. Using Eq. 4.4, the programming time of a VGA display with a refresh rate of 60 Hz and an 8-bit color depth is approximately 136.4 ns. So, the operating frequency of the driver is 7.33 MHz. We will consider this display as our baseline to clarify the benefits of the dual-driver method in different design modes.

Fig. 4.4 illustrates the timing diagram of a frame using the dual-driver method. Here, there are 4 subframes in each frame and two sets of data will be programmed in each

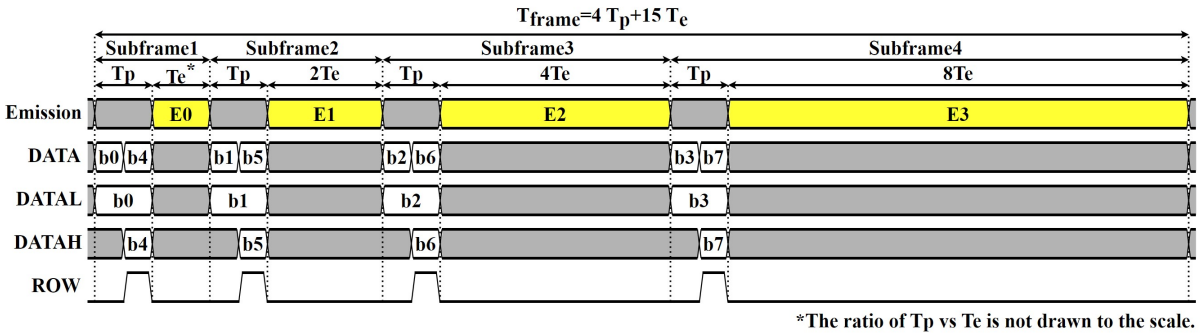


Figure 4.4: The timing diagram of a dual-driver pixel in a frame with the weighted PWM method.

programming time. As we discussed earlier, first the DATAL lines receive their data values and later in the second half of the programming time, the DATAH lines will be updated with new data values to be stored in the pixel circuits. Using the same approach as before, a frame time in dual-driver architecture is

$$T_{f_{prop}} = [\frac{n_{prop}}{2} + (2^{\frac{n_{prop}}{2}} - 1)(N_{prop} - 1)]\, T_{p\,prop} \tag{4.5}$$

where $T_{f_{prop}}$ and $T_{p\,prop}$ are the frame time and the programming time, n_{prop} is the color depth, and N_{prop} is the number of rows in the dual-driver display.

4.3 Dual-Driver Design Modes

A dual-driver display can be designed in several different modes optimizing various display features. The following list outlines these modes:

1. *Low-power mode*
2. *High-resolution mode*
3. *High refresh rate mode*
4. *High color depth mode*
5. *Mixed mode*

Each mode will be discussed in detail in the following subsections:

4.3.1 Low-Power Mode

Using the same refresh rate (or same frame times), resolution, and color depth for the conventional and dual-driver displays, we have:

$$\begin{cases} T_{f_{conv}} = T_{f_{prop}} \\ N_{conv} = N_{prop} = N \\ n_{conv} = n_{prop} = n \end{cases} \tag{4.6}$$

then, applying these conditions to Eq. 4.4 and Eq. 4.5, the ratio of programming time available in the dual-driver display to the conventional counterpart is given by

$$\frac{T_{p\,prop}}{T_{p\,conv}} = \frac{n + (2^n - 1)(N - 1)}{\frac{n}{2} + (2^{\frac{n}{2}} - 1)(N - 1)}. \tag{4.7}$$

For a fair comparison, one should consider the fact that two bits of data will be programmed in each dual-driver display's programming time, therefore,

$$\frac{T_{pb\,prop}}{T_{pb\,conv}} = \frac{T_{p\,prop}/2}{T_{p\,conv}} = \frac{n + (2^n - 1)(N - 1)}{n + 2\,(2^{\frac{n}{2}} - 1)(N - 1)} \tag{4.8}$$

where, $T_{pb\,prop}$, and $T_{pb\,conv}$ are the programming time for 1 bit of data in the dual-driver and conventional displays, respectively. In the above equation, the first term n in the numerator and denominator is much smaller and can be ignored. Therefore, the ratio can be approximated as

$$\frac{T_{pb\,prop}}{T_{pb\,conv}} \cong \frac{2^n - 1}{2\,(2^{\frac{n}{2}} - 1)} = k_m \tag{4.9}$$

where k_m is the dual-driver coefficient, representing the enhancement rate achieved by the dual-driver method in various modes. In the low-power mode, k_m is the ratio of the programming time for 1 bit in the dual-driver display to the programming time for 1 bit of a conventional display. Fig. 4.5 shows a frame of the conventional display and the dual-driver display in the low-power mode. These figures also illustrate the enlarged timing diagram of their first subframe. Based on Eq. 4.9 for an 8-bit color depth, $k_m = 8.5$. This means that the maximum programming time available for each row in the dual-driver display is 17 times larger than the conventional counterpart and the timing available to program each bit is 8.5 times more.

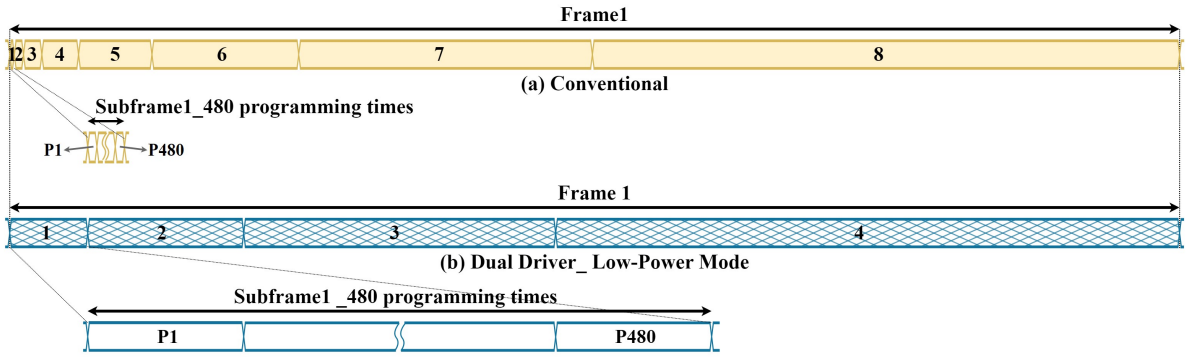


Figure 4.5: (a) The timing diagram of the conventional and (b) the dual-driver display in low-power mode.

Let us explore the origins of power reduction in this mode. Having fewer subframes means fewer row signal toggling which leads to the less dynamic power consumption of the row driver. On the other hand, the extension of the programming time per bit (i.e., 8.5 times) in the proposed method results in the row buffers' relaxed timing design. The operating frequency ratio is given by

$$\frac{f_{conv}}{f_{prop}} = \frac{T_{pb\,prop}}{T_{pb\,conv}} = k_m \tag{4.10}$$

here, f_{conv} and f_{prop} are the operating frequencies of the display drivers in the conventional and dual-driver architectures, respectively. Using Eq. 4.10, the operating frequency of the dual-driver display is approximately 0.86 MHz, which is 8.5 times smaller than the baseline display (7.33 MHz). The substantial decrease (i.e., 1/8.5) in the operating frequency and complexity of the signal generator module results in a considerable reduction in the power consumption of this module. Finally, for the data driver, while the programming time is extended, the data line buffer's timing constraint is relaxed and as a result, the power consumption is reduced.

In a display, key display parameters such as refresh rate, operating frequency, color depth, and the maximum number of rows are interdependent. For example, a high refresh rate leads to a higher operating frequency, etc. Therefore, for a given architecture, it is a good idea to explore this interdependence and the design space. Fig. 4.6 explores the design space in these four dimensions for the conventional and dual-driver pixel architecture in the low-power mode. While lowering the operating frequency of the drivers is desirable, for other characteristics (refresh rate, color depth, and resolution) a higher value is demanding.

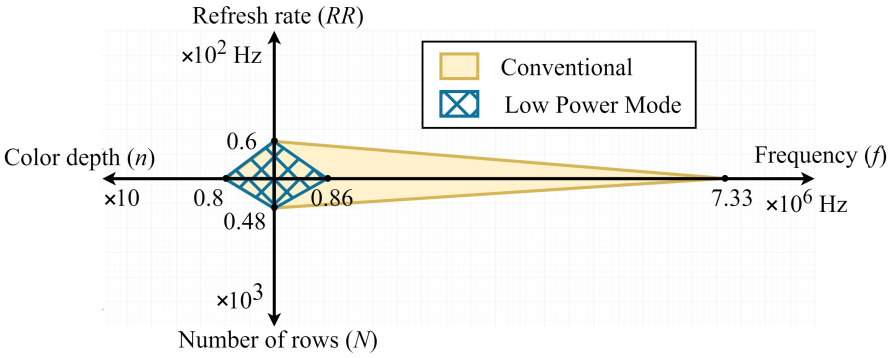


Figure 4.6: The conventional, and the dual-driver display characteristics in low-power mode.

The design space shown in the figure illustrates a dramatic decrease (8.5 times) in the operating frequency of the display in this mode.

4.3.2 High-Resolution Mode

Instead of extending the programming time in the proposed method, the extra time could be exploited to enhance other features of the display. In this mode, the refresh rate, frequency of operation (or programming time of 1 bit), and color depth are the same. Therefore,

$$\begin{cases} T_{f_{conv}} = T_{f_{prop}} \\ 2\,T_{p\,conv} = T_{p\,prop} = 2\,T_p \\ n_{conv} = n_{prop} = n \end{cases} \tag{4.11}$$

using Eq. 4.4, Eq. 4.5, and considering that N_{conv}, and N_{prop} are much larger than 1 in practice (it can be dismissed in the equations), then,

$$\frac{N_{prop}}{N_{conv}} \cong \frac{2^n - 1}{2\,(2^{\frac{n}{2}} - 1)} = k_m. \tag{4.12}$$

Like the low-power mode, for an 8-bit color depth $k_m = 8.5$, so based on Eq. 4.12, if the conventional display has 480 rows (VGA), the dual-driver display could program 4080 rows (8.5 times more) with the same programming time per bit. Fig. 4.7 illustrates the

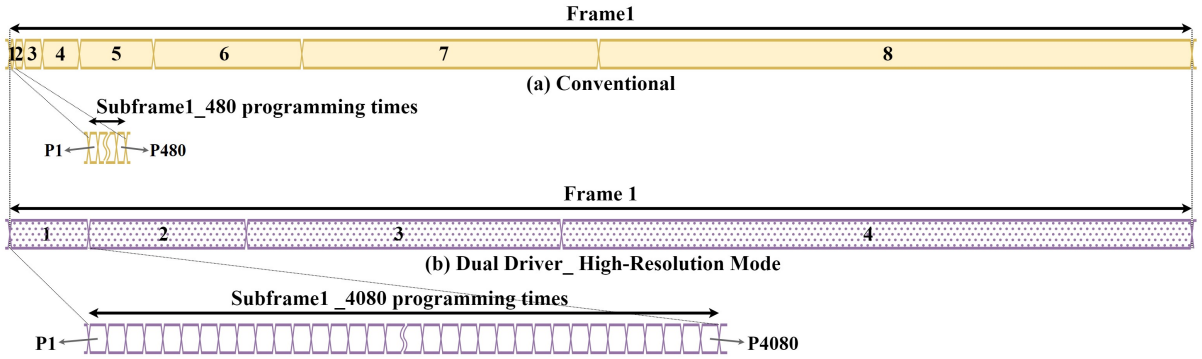


Figure 4.7: (a) The timing diagram of the conventional and (b) the dual-driver display in high-resolution mode.

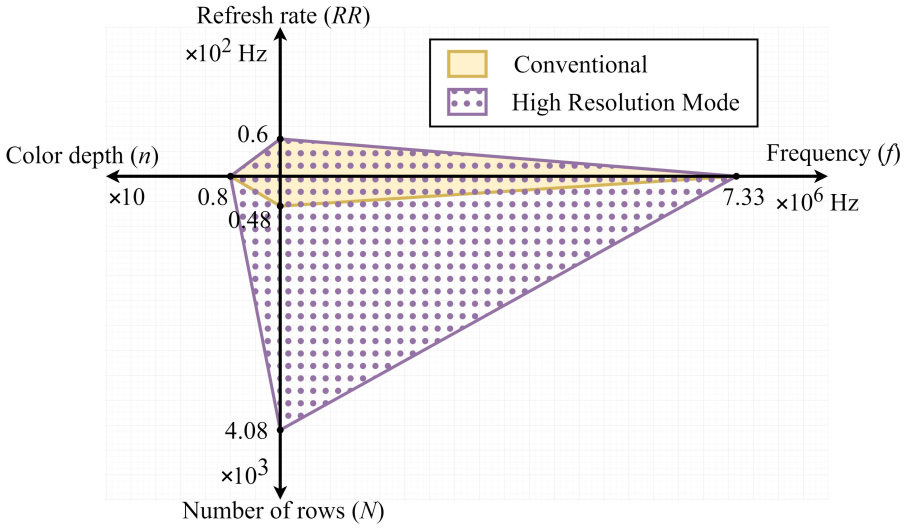


Figure 4.8: The conventional, and the dual-driver display characteristics in high-resolution mode.

frame timing diagram for the dual-driver display in the high-resolution mode in comparison with the conventional display. Here, the quantity and length of the subframes are equal to the previous mode, however, the difference is the utilization of the longer subframe time in the two modes. While in the low-power mode, the programming time was extended to reduce the operating frequency, in the high-resolution mode the available extra time will be utilized to program a higher number of rows (Look at the enlarged waveform of the

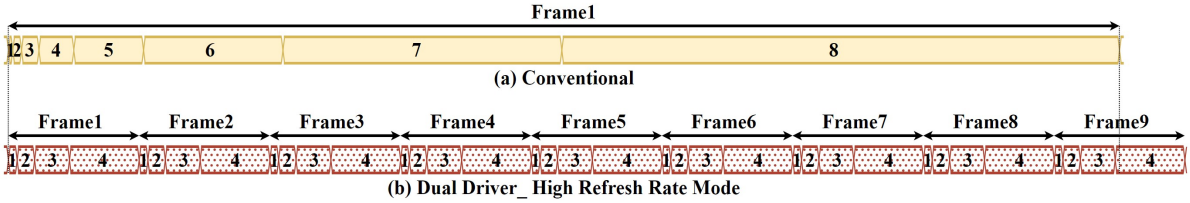


Figure 4.9: (a) The timing diagram of the conventional and (b) the dual-driver display in high refresh rate mode.

first subframe in Fig. 4.7b). Also, the purple tetrahedron with a dot filling in Fig. 4.8, shows the dual-driver display's characteristics in this mode. Compared to the baseline the number of rows that represent the maximum feasible resolution is increased from 480 to 4080 rows.

4.3.3 High Refresh Rate Mode

Similar to the approach in previous modes, here the assumptions are equal resolution, operating frequency, and color depth for the displays,

$$\begin{cases} N_{conv} = N_{prop} = N \\ 2\,T_{p\,conv} = T_{p\,prop} = 2\,T_p \\ n_{conv} = n_{prop} = n \end{cases} \tag{4.13}$$

applying the above assumptions to Eq. 4.4 and Eq. 4.5, the frame time ratio can be expressed as

$$\frac{T_{f_{conv}}}{T_{f_{prop}}} = \frac{n + (2^n - 1)(N-1)}{n + 2\,(2^{\frac{n}{2}} - 1)(N-1)} \cong \frac{2^n - 1}{2\,(2^{\frac{n}{2}} - 1)} = k_m. \tag{4.14}$$

The above equation is approximated because the term n in the numerator and denominator is much smaller and can be ignored. Thus, the refresh rate ratio is given by

$$\frac{RR_{\,prop}}{RR_{\,conv}} = \frac{T_{f_{conv}}}{T_{f_{prop}}} = k_m \tag{4.15}$$

where $RR_{\,conv}$ and $RR_{\,prop}$ are the refresh rates of the conventional and proposed displays. Fig. 4.9 compares the timing diagram of the conventional display and the dual-driver

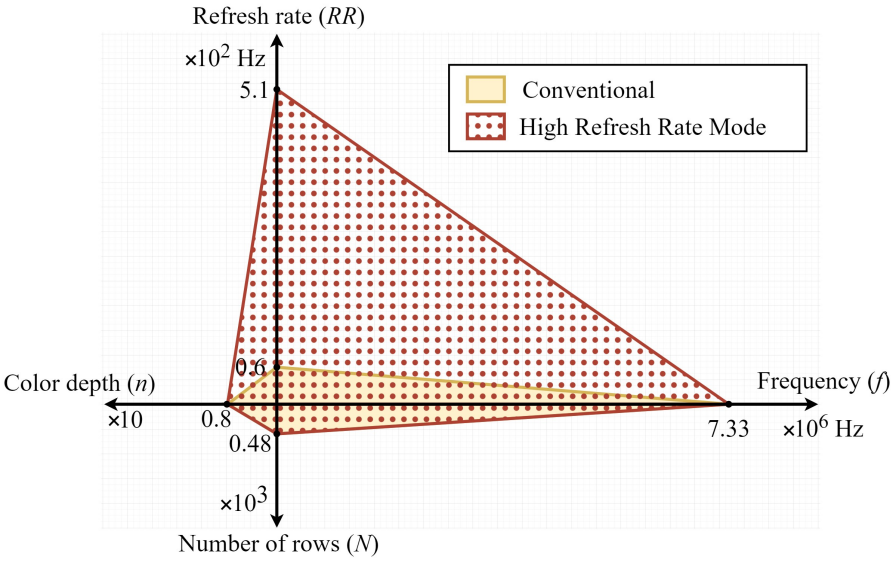


Figure 4.10: The conventional, and the dual-driver display characteristics in high refresh rate mode.

display in the high refresh rate mode. Since the ratio of the refresh rates is equal to the dual-driver coefficient (k_m), it is expected that using the proposed method in this mode results in an increase of the refresh rate by 8.5 times. Therefore, if the baseline has a refresh rate of 60 Hz, the dual-driver display's refresh rate is 510 Hz. This increase in the refresh rate can be seen in the design space by a red tetrahedron filled with dots in Fig. 4.10 which shows the benefit of the dual-driver method in a high refresh rate mode compared to the baseline.

4.3.4 High Color Depth Mode

To operate the dual-driver display in the high color depth mode, the resolution, operating frequency, and refresh rate should be the same,

$$\begin{cases} N_{conv} = N_{prop} = N \\ 2\,T_{p\,conv} = T_{p\,prop} = 2\,T_p \\ T_{f_{conv}} = T_{f_{prop}} \end{cases} \tag{4.16}$$

from Eq. 4.4, Eq. 4.5, and considering the above assumptions we have,

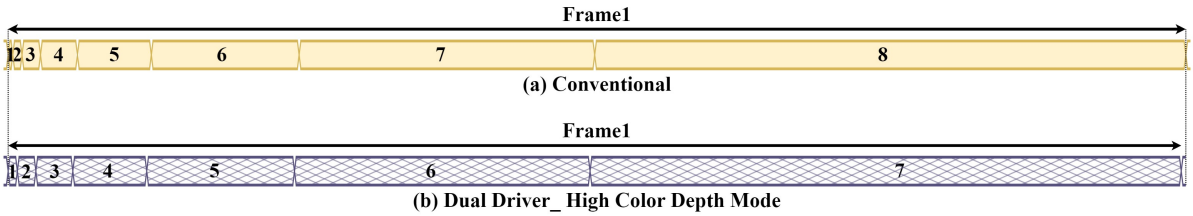


Figure 4.11: (a) The timing diagram of the conventional and (b) the dual-driver display in high color depth mode.

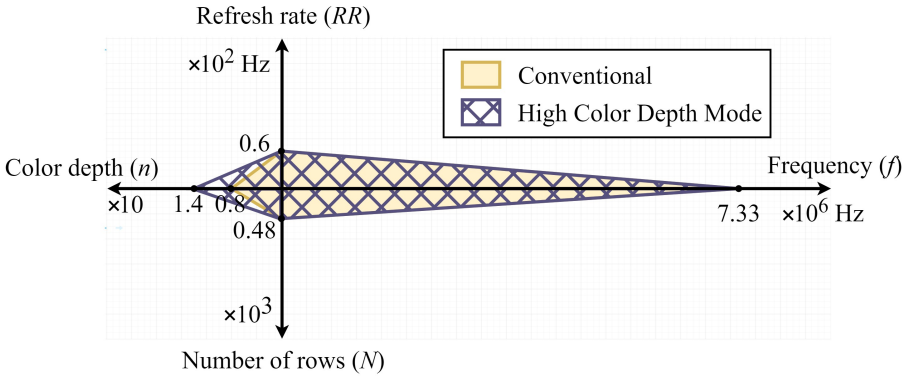


Figure 4.12: The conventional, and the dual-driver display characteristics in high color depth mode.

$$n_{conv} + (2^{n_{conv}} - 1)(N-1) = n_{prop} + 2\,(2^{\frac{n_{prop}}{2}} - 1)(N-1) \tag{4.17}$$

since n_{conv} and n_{prop} are much smaller than the second terms, the above expression can be approximated as

$$2^{n_{conv}} - 1 = 2\,(2^{\frac{n_{prop}}{2}} - 1). \tag{4.18}$$

Considering a color depth of 8 bits for the conventional display, from Eq. 4.18, the color depth of the dual-driver display is 14 bits. Fig. 4.11 illustrates the timing diagram for the dual-driver display operating in high color depth mode compared to the conventional display's timing diagram. As shown in the figure, for a color depth of 14 in the proposed display, 7 subframes are required to program the data. Fig. 4.12 depicts the design space in the high color depth mode. As illustrated, there is a significant increase in color depth from 8 bits in the baseline to 14 bits in the dual-driver method.

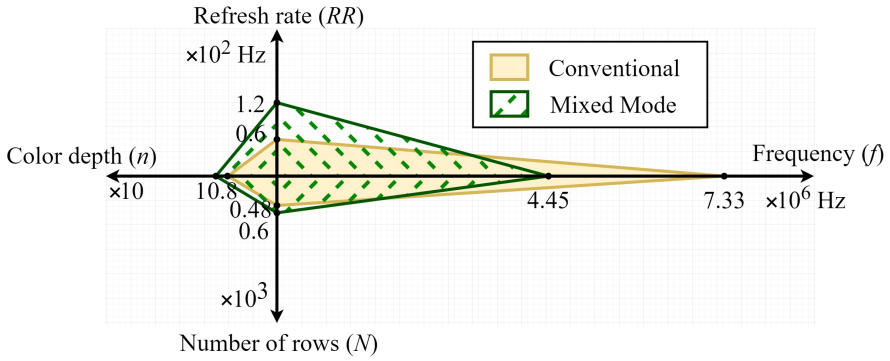


Figure 4.13: The conventional, and the dual-driver display characteristics in mixed mode.

4.3.5 Mixed Mode

Previous modes focus on enhancing one specification or feature at a time to the maximum capacity. Usually, the improvement of several features at the same time is more desirable. Therefore, the designer can choose to improve more than one characteristic simultaneously. For example, from Eq. 4.4, and Eq. 4.5, it is possible to increase the refresh rate from 60 Hz to 120 Hz, color depth from 8 bits to 10 bits, the display size from VGA to Super Video Graphics Array (SVGA) (800×600) and decrease the operational frequency from 7.33 MHz to 4.45 MHz, all at the same time. The dashed-filled green tetrahedron of Fig. 4.13 shows the display's features for the above example of the mixed mode. Note that this is one example of the mixed mode, there are lots of other feasible solutions to Eq. 4.5 that the designer may choose based on the design constraints. All these benefits come at the expense of extra pixel circuit area and extra data lines. The derived equations for the first 3 modes show that the dual-driver method enhances the features with a factor of k_m which is proportional to the color depth (n). Therefore, if the baseline display has a higher color depth, the dual-driver coefficient (k_m) would be higher whereby the dual-driver enhancement in those modes increases.

In this chapter, the baseline approach selected to demonstrate the advantages of the proposed method is the weighted PWM data driving method. However, employing the dual driver method to displays utilizing alternative data driving methods, such as the unweighted PWM driving method or analog driving method, also presents comparable opportunities for enhancing the design.

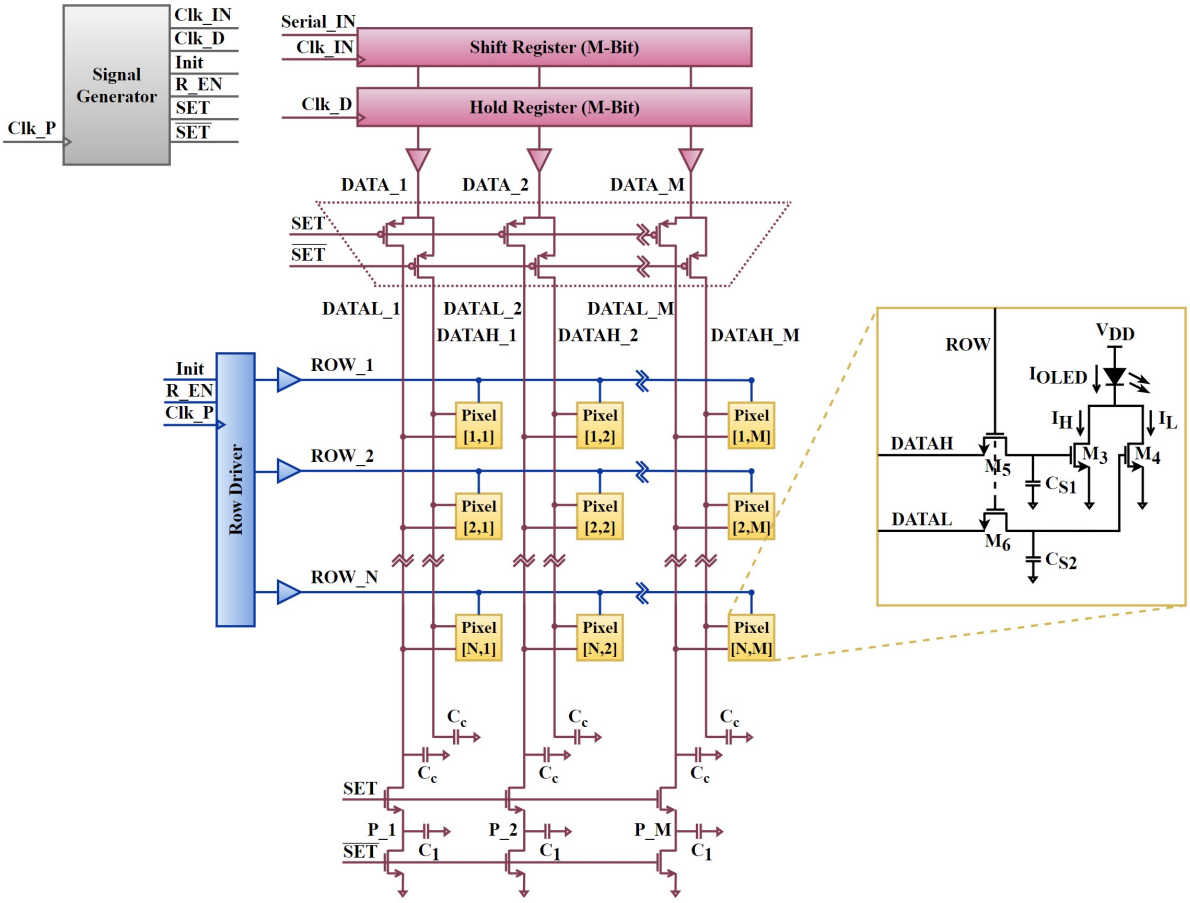


Figure 4.14: The dual-driver display architecture with signal processing.

4.4 Dual-Driver Architecture with Signal Processing Technique for Low Current Pixel Circuit

In general, the proposed dual-driver method is independent of the display media, however, in this thesis, we propose an OLEDoS dual-driver microdisplay. As media like OLED become more energy-efficient, they consume less current for the same light intensity. Consequently, the driver's current needs to be matched and reduced with an appropriate gate voltage. Based on the I-V curve of a top-emitting OLED designed for an AMOLED microdisplay in [99] to achieve a maximum luminance of 1200 cd/m2, the maximum emission current is approximately 3 nA. Even a minimum-sized Metal Oxide Semiconductor (MOS)

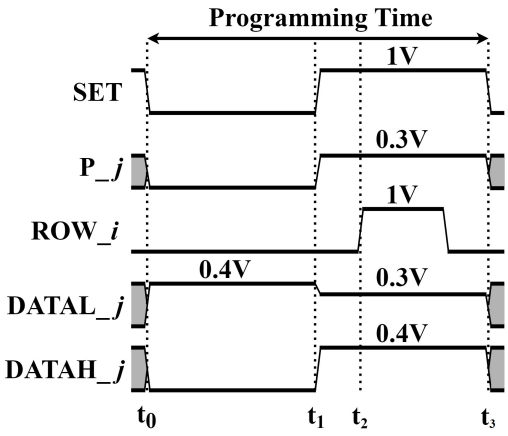


Figure 4.15: The waveform of signals for the programming time of row i and column j.

transistor can produce a much larger on-current required by the OLED. To produce such a small driving current either it is required to reduce the maximum voltage stored on the gate of the driving transistor or to increase its length. While the second option reduces the threshold voltage variation and thus results in a uniform display, it requires a larger pixel circuit area. We chose to reduce the maximum voltage stored on the pixel circuit's storage capacitor because it results in a power-efficient design. Therefore, the supply voltage (V_{DD}) of the data line buffers in Fig. 3.3 and Fig. 4.3 are 0.4V. Considering the relation between drivers' current in Eq. 4.1, for an 8-bit color depth I_L is 16 times smaller than I_H. To achieve this, we need even a smaller voltage (approximately 0.3V) to store on C_{S2}.

Fig. 4.14 illustrates the dual-driver display architecture with the signal processing technique. The C_c is the intrinsic capacitor of each data line that consists of the parasitic capacitance of the data line interconnects and the capacitance of the drain/source of the access transistors. A capacitor, C_1, and two switches (implemented with NMOS transistors) are added at the end of each DATAL line.

Fig. 4.15 shows the programming time of row i and column j, using the signal processing method. Assuming that both data bits needed to be stored are '1'. At t_0, DATAL values are already in the hold register and SET='0'. The DATAL_j line charges to 0.4V (equal to the buffer's V_{DD}), and node P_j discharges to the ground via the bottom switch while it is isolated from the rest of the data line. Meanwhile, the hold register receives the value associated with DATAH. Next, at t_1 the SET signal enables, and the data line buffer disconnects from DATAL_j and connects to DATAH_j to charge the capacitor of that line to 0.4V. Meantime, the switch between C_c and C_1 connects, and since $C_1 = C_c/3$, the final

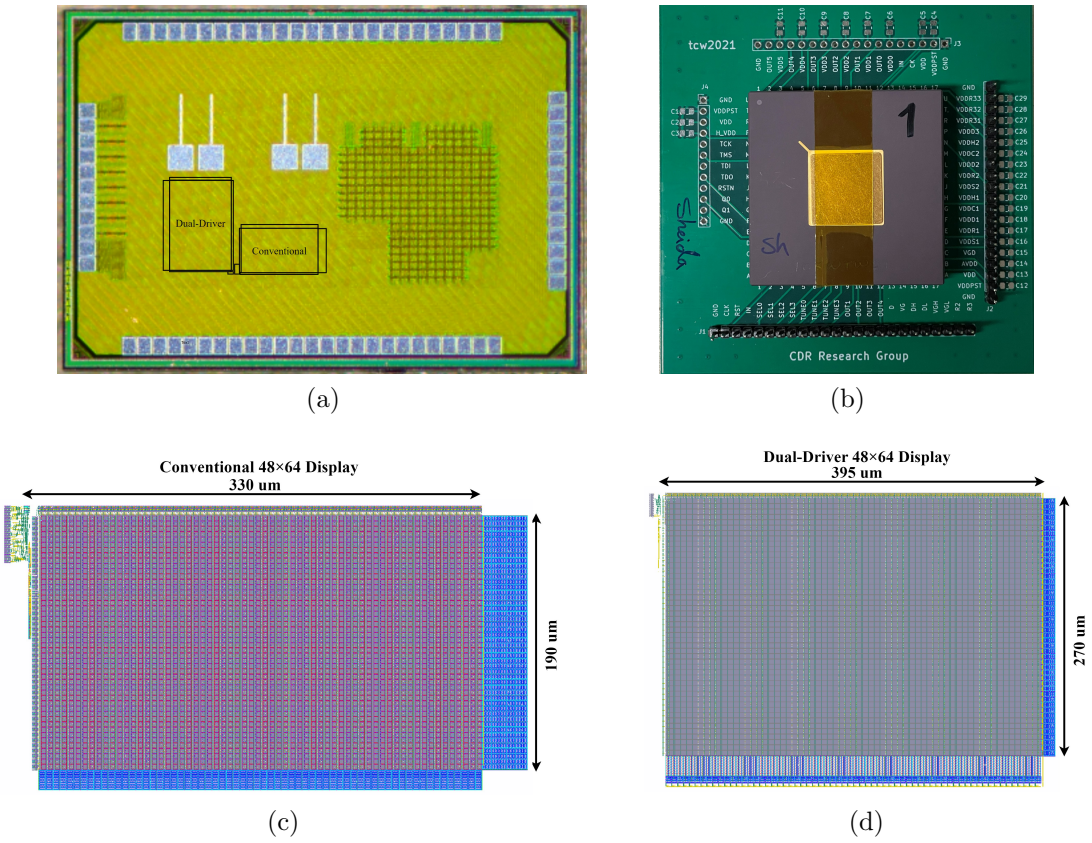
voltage after charge sharing is 0.3V. Thus, at time t_2 when the row signal is enabled the maximum voltage of 0.4V and 0.3V would be stored in the C_{S1} and C_{S2} capacitors of the dual-driver pixel circuit. This signal processing method empowers the designer to design the dual-driver pixel circuit with a smaller driving transistor for a media that requires a small current.

As previously stated, maintaining a precise current relationship is critical in the dual-driver pixel circuit to ensure the uniformity of the display. To achieve this uniformity, adjusting the supply voltages of the data lines buffer and employing a tunable C_1 to provide specific highest voltage values for each storage capacitor are effective solutions that ensure the required current flow. Furthermore, utilizing a tunable C_1 enables compensation for variations in Process, Voltage, and Temperature (PVT) and facilitates the adjustment of the C_1 to C_c relationship after the display has been manufactured.

4.5 Dual-Driver Display's Experimental Results

To verify the effectiveness of the proposed dual-driver method, two experimental proofs-of-concept 48×64 pixel arrays (i.e., the conventional and dual-driver architectures shown in Fig. 3.3 and Fig. 4.14) with their signal generator, row driver, and data driver are designed and implemented using TSMC 65 nm technology. The signal generator module generates the signals for a VGA (i.e., 480×640) display with a refresh rate of 60 Hz. The row and column capacitor per pixel has been extracted from the layout and extra capacitors have been added at the end of each row and column to mimic the capacitance load of a VGA-sized array. Fig. 4.16a and Fig. 4.16b display the micrograph image of the test chip with the location of each array and the packaged test chip mounted on PCB for measurement purposes, respectively. Additionally, Fig. 4.16c and Fig. 4.16d present the implementation layout and size of the arrays and the extra capacitors that have been integrated into the design.

The measurement setup of our implemented test chip is illustrated in Fig. 4.17. The packaged test chip depicted in Fig. 4.16b serves as the Device Under Test (DUT) in this setup. The FPGA board is programmed with a Verilog code, which generates various test images transmitted as a Serial_IN signal to the DUT. Additionally, the code allows us to select different internal signals to be displayed on the oscilloscope for verification purposes. Within the setup, the data driver, signal generator, row driver, pixel array, and IO pads are separate voltage islands. Each of these voltage islands is supplied with the corresponding voltages by dedicated power supplies, except for the one whose power consumption we intend to measure. To measure the power consumption of a specific module, we connect



(a) (b)

(c) (d)

Figure 4.16: (a) The micrograph of the test chip, and (b) the packaged test chip. (c) The conventional, and (d) the dual-driver 48×64 sized array with extra capacitors to mimic VGA sized array.

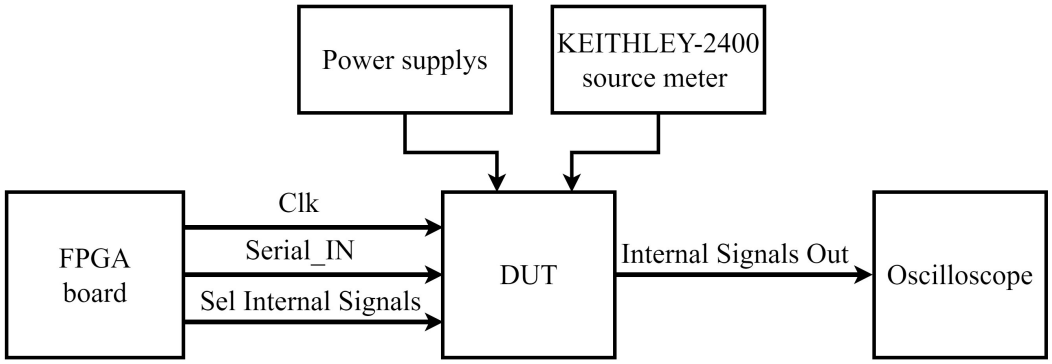


Figure 4.17: The measurement setup for the test chip.

its power supply to a KEITHLEY-2400 source meter. This instrument not only provides the supply voltage but also precisely measures the current drawn from that supply voltage. In this thesis, power consumption is calculated by measuring the energy drawn from the supply voltage over a fixed frame duration. Given that the chosen refresh rate for the display in this document is 60 Hz, the frame time is set at 16.6 ms. The power consumption of a module within a frame is determined by multiplying the average current during that frame by the supply voltage. Since the frame time remains constant, it simplifies the calculation of energy consumption. Consequently, in this document, the absolute values of power and energy exhibit a linear correlation.

We mimicked the implementation of OLED using a diode-connected transistor shown in Fig. 4.18a and Fig. 4.18b while ensuring that the V_{DS} of the driving transistor is the same as when it drives an OLED with a maximum current of 3 nA. The V_1 is 0.4V so the driving transistors operate in the linear region (V_{DS}=50mV).

Fig. 4.18c and Fig. 4.18d illustrate the layout implementation of the pixel circuits. All storage capacitors are implemented using N-channel Metal Oxide Semiconductor Capacitor (NMOSCAP) with a capacity of 12 fF. Table 4.1 shows the design parameters of the implemented dual-driver and conventional pixel circuits. The maximum current of the conventional and dual-driver pixel circuit is 3 nA and the maximum currents for two drivers in the proposed method are calculated using Eq. 4.1 for a display with 8-bit color depth. The OLED media necessitates a 6V supply voltage for the pixel circuit. Consequently, in our pixel circuit designs, we opted for the high-voltage transistors available in the TSMC 65 nm technology library instead of the standard transistors designed for a 1V supply voltage. The minimum dimensions of these high-voltage transistors are 0.4um in width and 0.5um in length, with a threshold voltage of approximately 0.54V. As the stored voltage for a

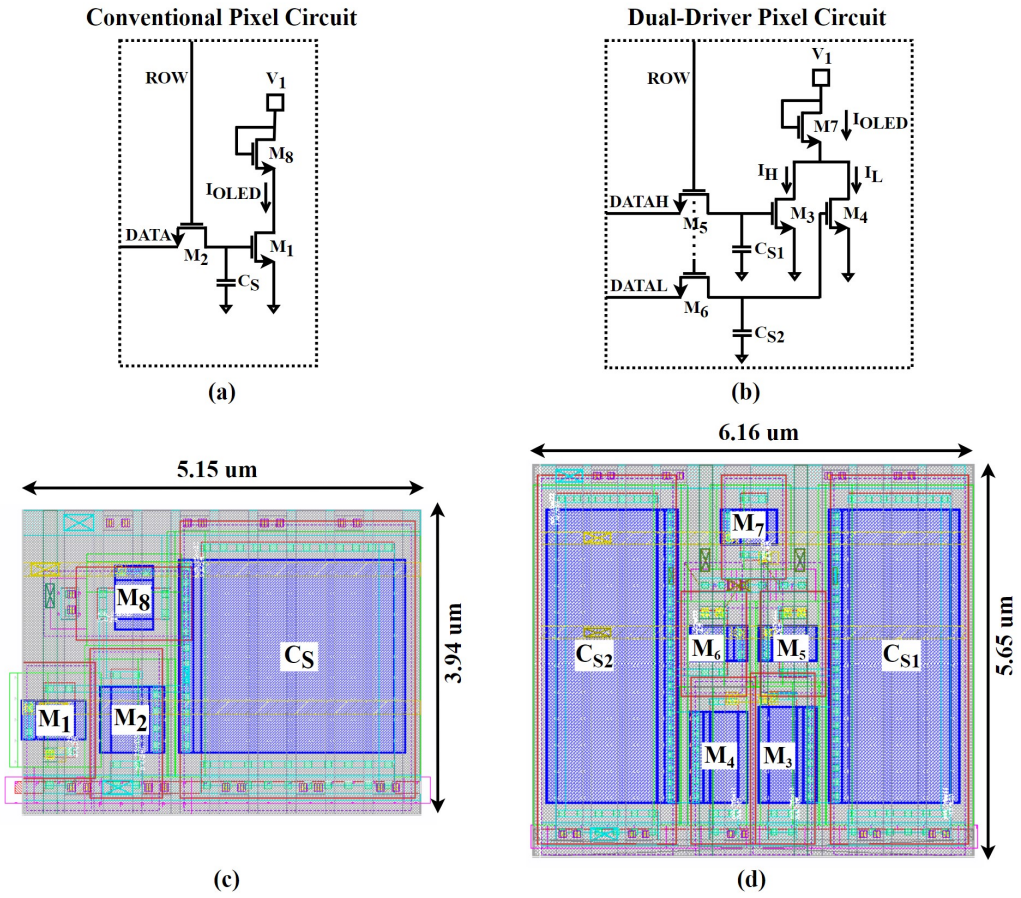


Figure 4.18: Mimicking the OLED with a diode-connected transistor for (a) the conventional, and (b) the proposed pixel circuit. The implemented layout of (c) the conventional, and (d) the proposed pixel circuit.

logical '1' is 0.4V and 0.3V for DriverH and DriverL, respectively, both of these transistors are operating in the subthreshold region to generate the required small currents needed for the design. Using the dual-driver method the pixel circuit area is increased by 71% compared to the baseline, primarily because in-pixel capacitors C_{S1} and C_{S2} are realized with MOS transistors. Alternatively, one can use Metal-Insulator-Metal (MIM) capacitors which may reduce the area of the proposed design. The C_c capacitor value per data line is estimated to be approximately 550 pF based on the post-simulation results, while the C_1 capacitor was designed to be tunable with a central value of 183 pF.

The initial step in verifying the proposed method is to demonstrate that the luminance

Table 4.1: Design parameters of pixel circuits.

Design Parameter	Value
Process	65 nm standard CMOS process
Color depth (bit)	8
(W/L) ratio of M_1 $(\mu m/\mu m)$	0.4/0.85
(W/L) ratio of M_2, M_5, and M_6 $(\mu m/\mu m)$	0.4/0.5
(W/L) ratio of M_3 $(\mu m/\mu m)$	0.4/1.4
(W/L) ratio of M_4 $(\mu m/\mu m)$	0.4/1.3
(W/L) ratio of diode-connected transistors $(\mu m/\mu m)$	0.4/0.5
C_S, C_{S1}, C_{S2} (fF)	12
Conventional pixel area $(\mu m/\mu m)$	3.94×5.15
Proposed pixel area $(\mu m/\mu m)$	5.65×6.16
Maximum emission current- I_{OLED} (nA)	3
I_H (nA)	2.82
I_L (pA)	176
Maximum voltage on C_S and C_{S1} capacitors (V)	0.4
Maximum voltage on C_{S2} capacitor (V)	0.3
Row and data drivers power supply except for the data lines' buffer (V)	1
Data lines' buffer power supply (V)	0.4

of the dual-driver pixel circuit is equivalent to that of the conventional counterpart. Fig. 4.19 illustrates the simulation results of the OLED currents versus different grey levels for designed pixel circuits. The blue dashed graph is the conventional pixel circuit's current. The red graph of Fig. 4.19 shows the OLED current produced by the proposed method and it is the summation of the DriverH and DriverL currents (see Eq. 4.2). DriverL produces a current (green graph with cross markers) based on the 4 least significant bits of the data and DriverH produces a current (orange graph with dot markers) based on the 4 most significant bits of the data. As illustrated, the dual-driver pixel circuit produces almost the same OLED current as the conventional one for different grey levels.

Fig. 4.20 illustrates the current measured from the implemented displays. Since one pixel current is too small to be measured with our equipment, the whole display is programmed with the same grey level and the overall current has been measured and then divided by the number of pixels in the display. The measured current proves that the dual-driver pixel creates almost the same current as the conventional pixel circuit.

As previously stated, the weighted PWM method exhibits steps at intervals of powers

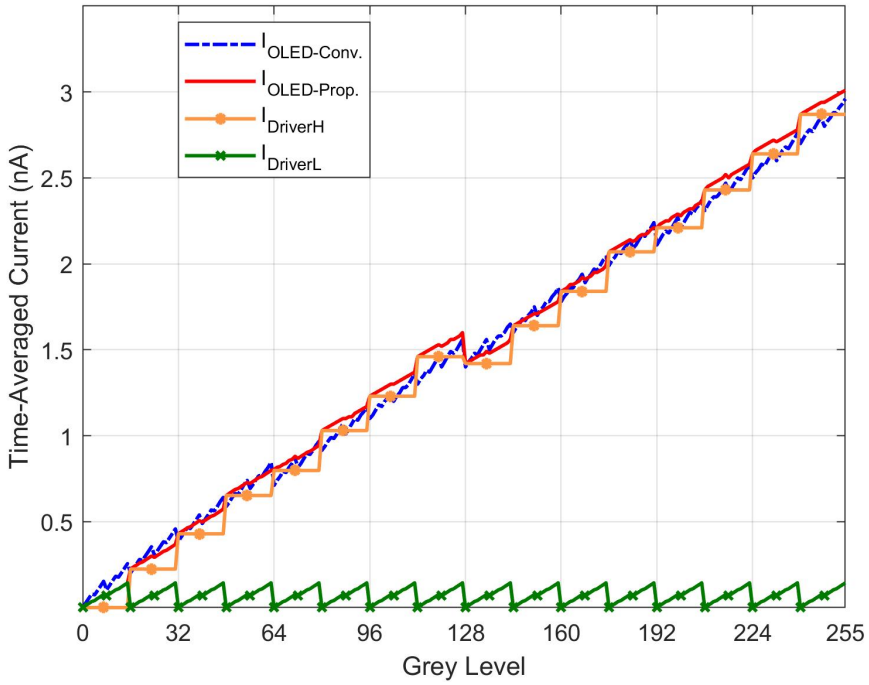


Figure 4.19: The simulated time-averaged current of the conventional and proposed pixel circuits.

of 2 grey levels due to the influence of access transistor leakage and varying emission time durations. The most significant step occurs between grey levels 127 and 128, where one scenario involves 7 subframes receiving a value of '1', while in the other scenario, only one subframe with a longer emission time is assigned a '1'. The impact of access transistor leakage is more pronounced in the latter scenario (grey level 128). It is worth noting that utilizing an unweighted PWM technique would result in a linear grey level for both the conventional and dual-driver approaches. Moreover, it is important to highlight that the advantages of the proposed method are not reliant on the baseline driving technique, and comparable benefits can be attained using an unweighted PWM driving technique.

As we mentioned before, the dual-driver architecture may operate in different modes. While the maximum benefit of each mode has been discussed before, it is required to study the low-power mode in detail to measure the extent of the power reduction that comes as the benefit of this proposed method. Fig. 4.21 shows the measured power consumption of the signal generator, the data driver, and row driver modules using 4 different test

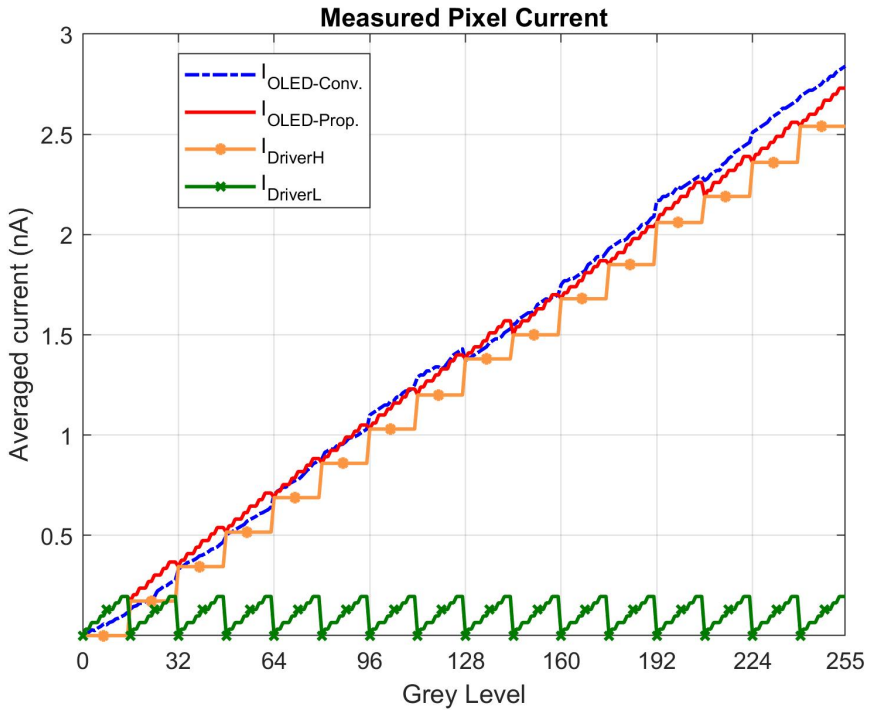


Figure 4.20: The measured averaged current for the conventional and proposed pixel circuits.

images in VGA displays employing the conventional and proposed methods. The average bar illustrates the average power consumption of the 4 test images. Note that while the power consumption of the data driver changes based on the image content, the power consumption of the row driver and signal generator are independent of it.

Based on the measurement results, the first source of power reduction is from row drivers. The proposed technique reduces the row signal activity by half within a frame, and a smaller row buffer is achieved by extending the programming time, which allows for a longer rise time. This, in turn, results in a notable decrease in the power consumption of the row driver, despite an increase in the row line capacitor due to having two access switches per pixel. Notably, this increase in the row line capacitor is limited to approximately 1.5 times, considering the intrinsic capacitor of the interconnects. The second origin of power saving is the data driver. Again, having 8.5 times longer programming time, makes it possible to design smaller data line buffers and reduces the power consumption of the data driver. Lastly, the signal generator is extremely simple in the proposed method. This is

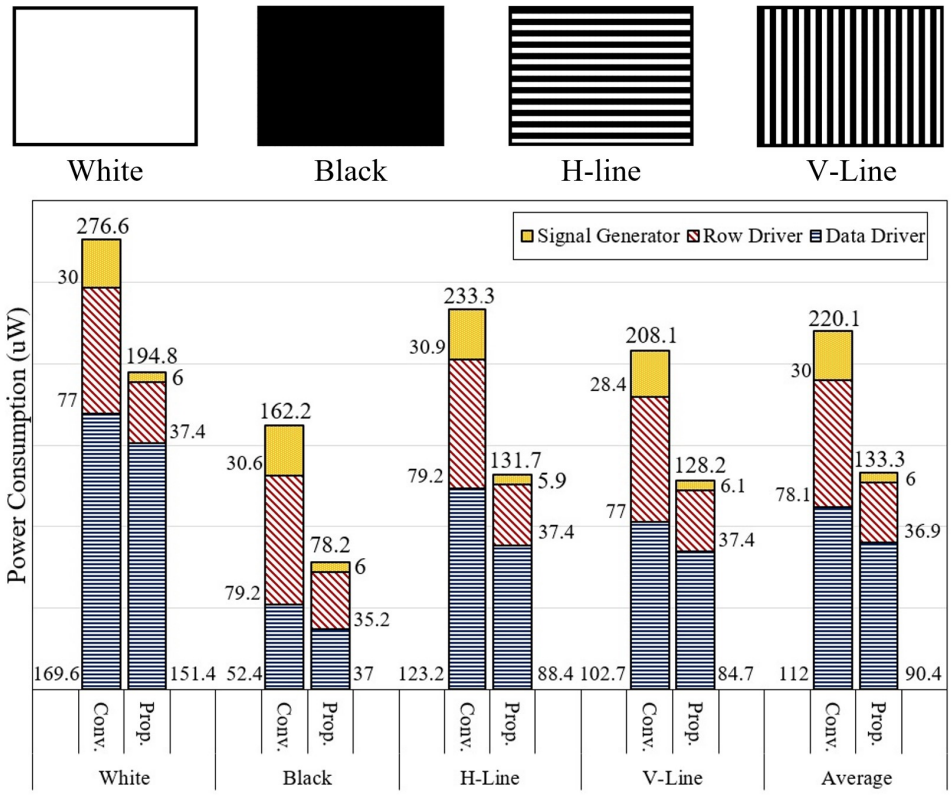


Figure 4.21: Measured power consumption of different blocks for the conventional and proposed VGA displays using 4 different test images shown above the graph.

mainly because of having a smaller number of subframes during a frame and therefore a smaller counter in that block.

As expected, the power consumption of the white image is the highest and it is the lowest for the black image. The power consumption saving ranges from 51.8% for a black image to 29.5% for a white image. Taking a simple average of these four images results in a power saving of 39.4%.

Additionally, the proposed method provides an opportunity to increase the resolution, color depth, and refresh rate of microdisplays. It is noteworthy that the power consumption of the pixel array remains the same since it is related to the image content and the maximum luminance of the pixel is the same for both methods. This significant reduction of power consumption is obtained at the expense of more area and a doubling of data lines.

4.6 Summary

This chapter proposed a new driving method that reduces the number of subframes in a digitally driven display. Designing the dual-driver method in different modes may result in enhancement of the power consumption, resolution, refresh rate, and/or color depth of the display. A new pixel circuit with two drivers and its associate data and row drivers is proposed. The measurement results using the dual-driver method on a proof-of-concept array implemented in TSMC 65 nm technology show a 39.4% reduction in the power consumption of the drivers compared to a conventional array for the same pixel brightness. It is shown that the proposed dual-driver display may enhance the resolution or refresh rate by 8.5 times. In another design mode, using this method increases the color depth of the display from 8 bits to 14 bits. It is also possible to enhance all mentioned features at the same time, but the improvement of each feature will be less. The benefit of the dual-driver display comes at the cost of a larger pixel circuit and doubling the data lines.

Chapter 5

Proposed Low-Power Drivers with Energy Restoration Techniques

There is a growing demand in the market for displays that offer higher resolutions, pixel densities (PPI), and refresh rates. Display technology is advancing rapidly, with designers striving to enhance these display characteristics. Increasing the resolution and pixel densities (PPI) of a display necessitates larger capacitors per row or data lines, leading to increased dynamic power consumption for the display drivers. Additionally, a higher refresh rate is directly proportional to the driver's dynamic power consumption. Therefore, it is crucial to employ methods that can effectively lower the dynamic power consumption given the ongoing focus on enhancing display features.

The objective of the energy restoration or energy recycling method is to reduce power consumption by reusing energy that would otherwise be wasted in the circuit. Previous studies have focused on implementing energy recycling approaches to reduce power consumption in TFT-LCD displays that utilize the dot inversion driving method [100, 101]. This method involves the neighbour data lines operating at reverse voltages and toggling during each programming cycle. Researchers have leveraged the predictable nature of dot inversion to recycle energy and decrease dynamic power consumption [102, 103]. However, AMOLED display driving methods differ significantly. The behaviour of the data driver in AMOLED displays is dependent on the image content, and the charging or discharging process cannot be predicted in advance. On the other hand, with the improvement in OLED efficiency, the power consumption of the drivers has emerged as the primary power component in the display module. Consequently, in scenarios characterized by low data activity, such as a smartwatch in clock display mode, the power consumption of the row driver becomes equally critical. Hence, it is advantageous to introduce novel techniques

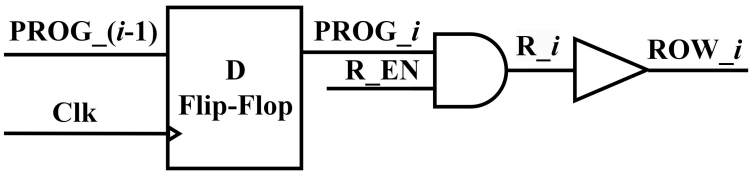


Figure 5.1: The row driver circuitry of ROW_i.

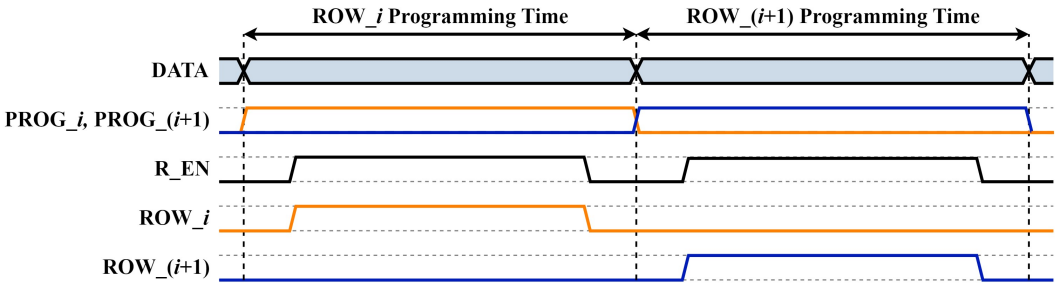


Figure 5.2: The programming time of two consecutive rows with digital data driving method.

aimed at reducing the dynamic power consumption of both the row and data drivers in an AMOLED display. This chapter proposes four energy recycling techniques to tackle this challenge. The first three techniques focus on reducing dynamic power consumption in the row driver, while the fourth technique is designed to address dynamic power consumption in the data driver.

The baseline display for this chapter is the $N \times M$ display architecture depicted in Fig. 3.3, along with the unweighted PWM data driving method illustrated in Fig. 3.5. The row driver circuitry for the mentioned baseline architecture is depicted in Fig. 5.1. It consists of a flip-flop module employed for shifting the PROG_i signals. Furthermore, an AND gate enables the row line exclusively when the R_EN signal is active. This design ensures the row line is activated only when the associated data value is stable. Fig. 5.2 demonstrates the timing diagram of two successive programming times using the unweighted PWM driving scheme. During each programming time when the data values are stabled on data lines, the row enable will be enabled.

The flowchart of Fig. 5.3 depicts the scanning process of a single data line for a subframe in the conventional display. Once the new data value stabilizes on the data line, the row signal becomes active, allowing the pixel circuit to receive and store the new data value on its storage capacitor. Subsequently, the row line is deactivated. This procedure will

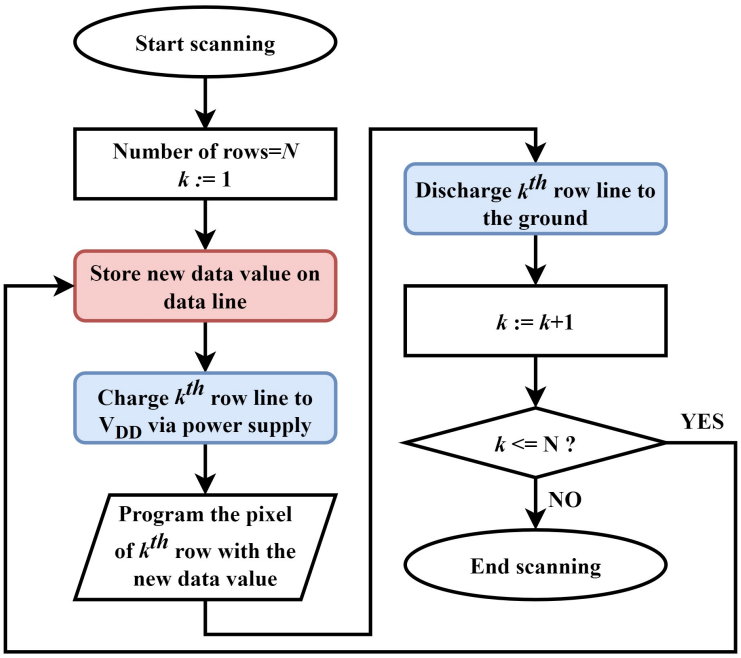


Figure 5.3: The process of scanning a data line in a conventional display.

be repeated for every row line of the display during a subframe time. In this chapter, the flowcharts use a color scheme to differentiate actions concerning the row driver, which is denoted by the blue color, from actions related to the data driver, which is represented by the red color.

5.1 Energy Restoration Techniques for Row Driver

In general, row drivers sequentially scan all rows in the display one at a time and repeat the same operation. This sequential row driving method is universal, regardless of the data driving method used (digital or analog). The proposed charge recycling technique involves transferring a portion of the energy stored in the row capacitor to the next row, thereby reducing the amount of energy required to fully charge that row. Hence, the power consumed from the supply voltage is reduced substantially.

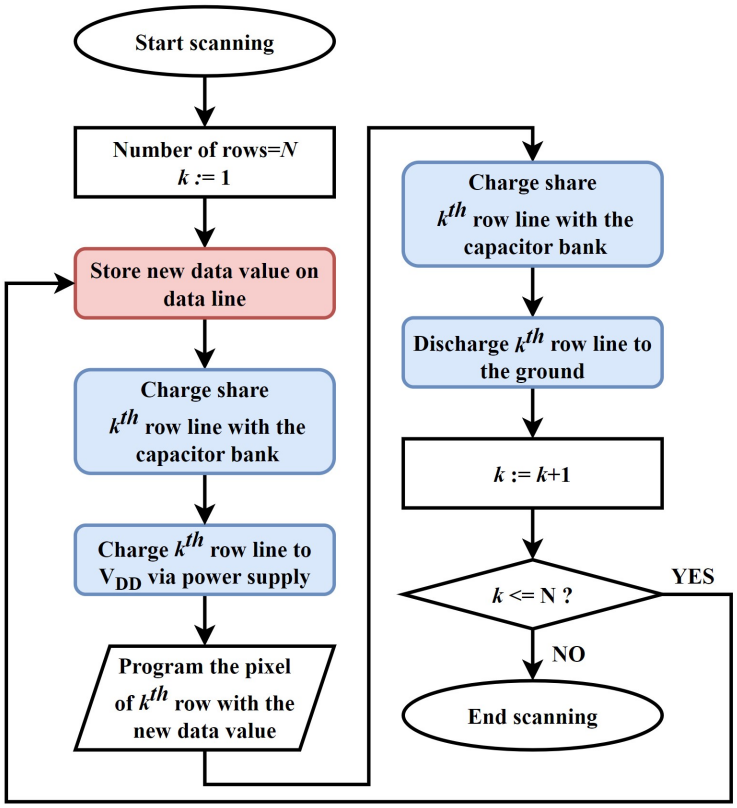


Figure 5.4: The process of scanning a data line in a display with one-capacitor bank energy restoration technique.

5.1.1 One-Capacitor Bank Energy Restoration

Once a row line has been programmed with new data values, it is necessary to deactivate the signal associated with that particular row. Consequently, the energy stored on the row line is discharged to the ground. To harness this energy, a portion of it is stored in a capacitor bank, serving as an energy reservoir for future utilization. Fig. 5.4 provides a flowchart of the scanning process of a data line employing the one-capacitor bank energy restoration technique. As depicted, when the data line value stabilizes, the row line capacitor receives energy from the capacitor bank and subsequently becomes fully charged to the V_{DD} via the row line buffer. Additionally, after programming the pixel circuit with the new data value, the row line transfers energy back to the reservoir and eventually discharges entirely to the ground. This iterative process is repeated for all row lines in the display.

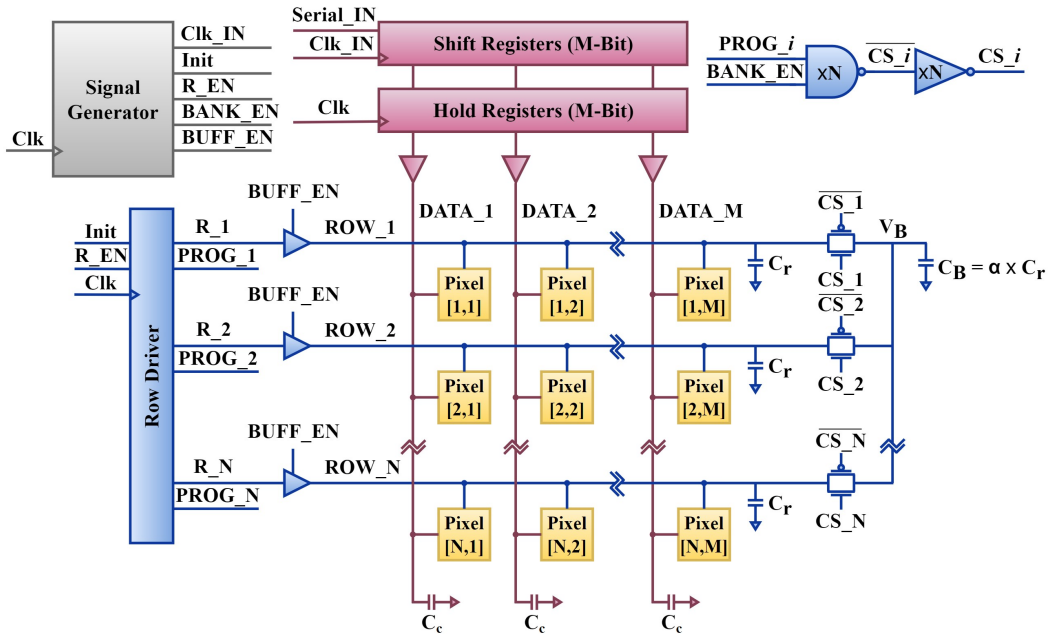


Figure 5.5: The $N \times M$ active-matrix display with one-capacitor bank energy recycling technique.

Fig. 5.5 illustrates the $N \times M$ active-matrix display employing the row driver energy recycling technique with a single capacitor bank. Here the signal generator block has two extra output signals named BANK_EN, and BUFF_EN compared to the conventional architecture of Fig. 3.3. To implement the energy recycling technique a set of NAND and NOT gates, and a switch (transmission gate (CS_i)) are added per row. The intrinsic capacitor for one row is denoted as C_r, while an additional capacitor added for energy recycling purposes is represented as C_B. The row driver is similar to the configuration shown in Fig. 5.1, however, it incorporates a row buffer with an enable signal (BUFF_EN) to facilitate tristate mode operation. The PROG_i signal is an additional output from the row driver for each row that is enabled exclusively during the programming time of that row.

Before delving into the energy restoration operation, it is important to note two significant points. Firstly, it is observed that the voltage (V_B) of the capacitor bank toggles between two values - the stored voltage (V_S) and the recycled voltage (V_R) - after several rounds of energy recycling. To clarify, V_S refers to the voltage of the capacitor bank after it has received energy and is storing it, while V_R refers to the voltage of the capacitor bank after it has delivered energy to a row and is in the process of restoring/recycling energy.

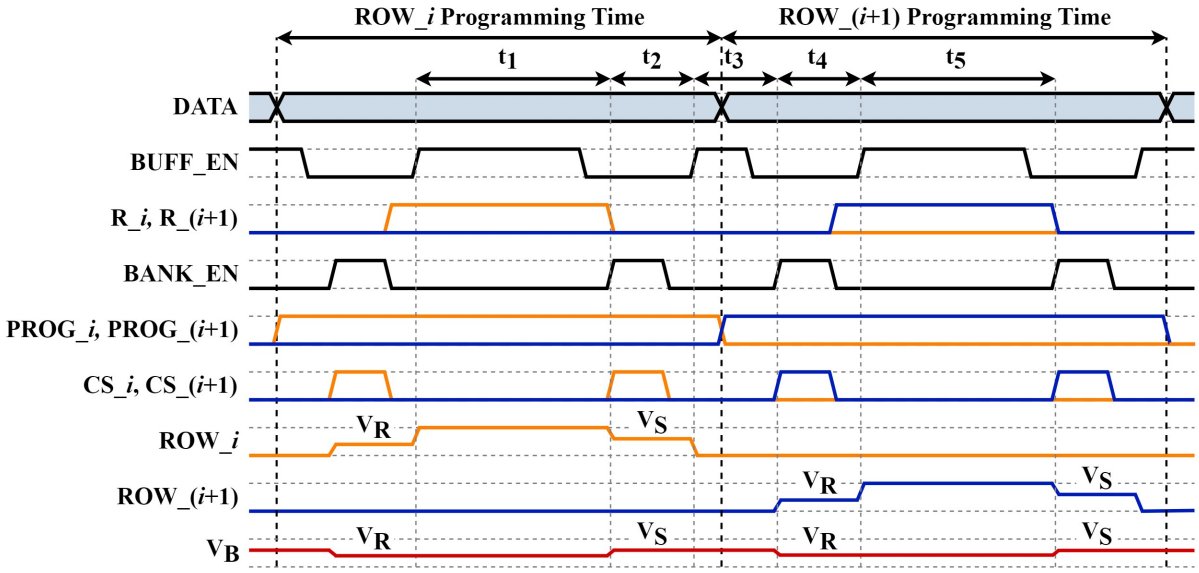


Figure 5.6: The timing diagram of the control and row signals of two consecutive rows using one-capacitor bank energy recycling technique.

Secondly, The maximum energy to be restored is proportional to α (where $\alpha = C_B/C_r$) and it is desirable to study the impact of α on the level of energy restoration.

Having established these notes, let us now discuss the specifics of the energy restoration process, as illustrated by the waveforms in Fig. 5.6. The figure illustrates the control and row signals of two consecutive rows using this technique. The orange and blue colors represent the signals of i and i+1 rows, respectively. At the time t_1 the intrinsic capacitor of i^{th} row (C_r) is fully charged, and all pixels in the row get the new data value. However, before discharging the energy stored in the intrinsic capacitor of the i^{th} row, it is essential to transfer a certain proportion of that energy to the capacitor bank (C_B). Looking at the BUFF_EN signal, it is already disabled before t_2. So, while $i^{th}C_r$ is disconnected from supply voltages, at time t_2 the BANK_EN is activated and since the PROG_i signal is also active, the CS_i switch will be connected for charge sharing between $i^{th}C_r$ and C_B. To calculate the final voltage after charge sharing the capacitor charge sharing equation is used as follows:

$$Q_t = Q_{t+1} \tag{5.1}$$

in this equation, Q_t and Q_{t+1} are the overall capacitors' charge before and after charge sharing. So, the charge of $i^{th}C_r$ and C_B are

$$C_r \times V_{ROW\_i}(t_1) + C_B \times V_B(t_1) = C_r \times V_{ROW\_i}(t_2) + C_B \times V_B(t_2). \tag{5.2}$$

In our theoretical calculations, we make the assumption that multiple rounds of charge recycling have been completed, and the stored/restored voltages of the bank have reached a steady state. Thus, at time t_1, the bank voltage is equal to the recycled voltage (V_R) from the previous round, and the final voltage after the charge sharing is the stored voltage (V_S), therefore,

$$C_r \times V_{DD} + \alpha C_r \times V_R = C_r \times V_S + \alpha C_r \times V_S \tag{5.3}$$

rewriting the above equation, V_S is

$$V_S = \frac{V_{DD} + \alpha V_R}{1 + \alpha}. \tag{5.4}$$

After storing a part of the energy in the bank, the CS_i switch turns off and at the end of t_2 the BUFF_EN is activated and R_i is equal to '1'. This means that the rest of the energy on the $i^{th}C_r$ discharges to the ground via the NMOS transistors in the row line buffer. In the next programming time, at time t_4 the $(i+1)^{th}$ row line is already disconnected from the row buffer, by activating the BANK_EN signal since PROG_(i+1) is on, the CS_(i+1) turns on to enable receiving charge from the bank. The capacitors' charge before and after the charge sharing is

$$C_r \times V_{ROW\_(i+1)}(t_3) + C_B \times V_B(t_3) = C_r \times V_{ROW\_(i+1)}(t_4) + C_B \times V_B(t_4). \tag{5.5}$$

Considering that the before and after charge sharing voltages of the bank are V_S and V_R, respectively, then

$$C_r \times 0 + \alpha C_r \times V_S = C_r \times V_R + \alpha C_r \times V_R \tag{5.6}$$

replacing V_S from Eq. 5.4 and rewriting the equation, V_R is

$$V_R = \frac{\alpha V_{DD}}{1 + 2\alpha}. \tag{5.7}$$

V_R represents the restored/recycled voltage using the energy recycling technique with one capacitor bank. After energy restoration, CS_(i+1) turns off. At the end of t_4, since

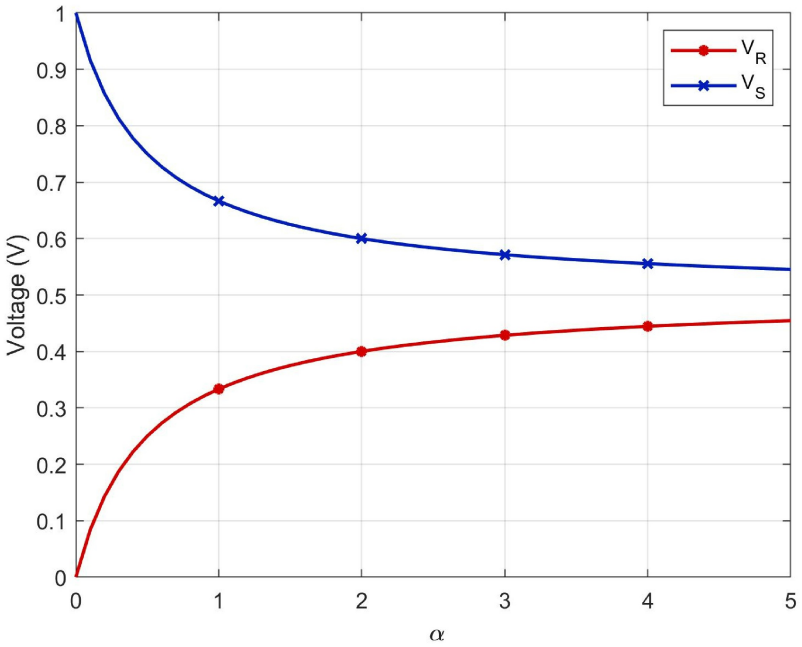


Figure 5.7: The stored (V_S) and recycled (V_R) voltages versus α, using the energy recycling technique with one capacitor bank.

R_$(i+1)$=0, by activating BUFF_EN, the $(i+1)^{th}C_r$ will be fully charged to V_{DD} via the PMOS transistors in the row line buffer. This procedure repeats again for the rest of the rows in the display. Each time that a row is charged to V_{DD} a portion of energy stores on the C_B capacitor for future reuse and the rest discharges to the ground; and each time that a C_r needed to charge, it first receives energy from C_B and then it charges to V_{DD} via the PMOS transistor of that row.

Fig. 5.7 shows the stored and recycled voltages for various sizes of the capacitor bank (α) based on Eq. 5.4 and Eq. 5.7 considering V_{DD}=1. The figure clearly indicates that the recycled voltage increases with an increase in the size of the capacitor bank and the maximum voltage that can be recycled is less than $V_{DD}/2$=0.5V. The amount of recycled charge obtained at each cycle is equal to the product of C_r and V_R. It is crucial to mention that choosing a larger α does not necessarily lead to more energy savings. This is because a larger capacitor bank necessitates a larger switch and more power consumption of the controlling signals, which can offset any potential energy savings. Moreover, as shown in the figure the recycled voltage reaches a saturation point for values of α greater than 2. When α=2, 40% of the dynamic power consumption of the row buffers will be saved using

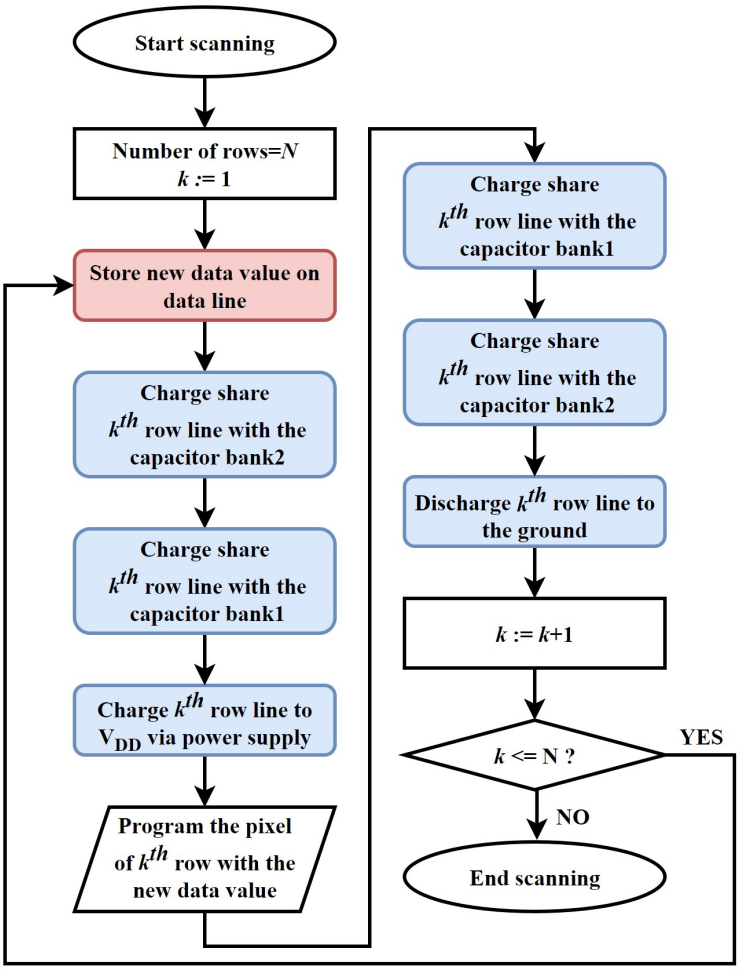


Figure 5.8: The process of scanning a data line in a display with the two-capacitor bank energy restoration technique.

this technique ignoring the power overhead of the additional circuit.

5.1.2 Two-Capacitor Bank Energy Restoration

As previously mentioned, it has been determined that a single capacitor bank can restore a maximum voltage that is lower than $V_{DD}/2$. To maximize energy recycling between row lines, a two-step recycling technique is also explored. The scanning process of this

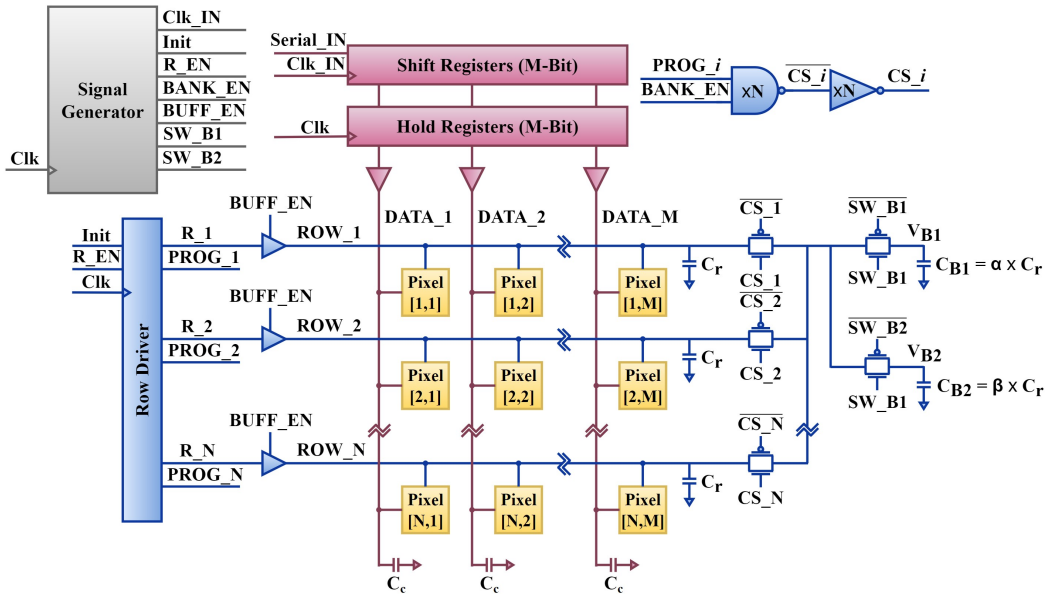


Figure 5.9: The $N \times M$ active-matrix display with two-capacitor bank energy recycling technique.

technique closely resembles the previous one, but with the distinction of a two-step charge-sharing mechanism, as depicted in Fig. 5.8. Once the new data value stabilizes, the row line initially receives energy from a lower energy capacitor bank (C_{B2}) and subsequently engages in charge sharing with the other capacitor bank (C_{B1}). Similarly, prior to fully discharging the energy of the row line to the ground, it first transfers energy to the C_{B1} capacitor bank and then to the C_{B2} capacitor bank.

The display architecture utilizing the two-capacitor bank energy recycling technique is depicted in Fig. 5.9. Compared with the one-capacitor bank architecture of Fig. 5.5, two switches (i.e., SW_B1 and SW_B2) along with their controlling signals and an extra capacitor (C_{B2}) are added here. In this technique, after programming data in a row, first, the intrinsic capacitor of that row (C_r) charge shares with C_{B1}. Subsequently, C_{B1} is disconnected from the row, and C_{B2} is connected to the row to store even more energy from the row line. During the programming of the subsequent row, the capacitor of that row line acquires energy initially from C_{B2}, followed by C_{B1}. This order of energy restoration is crucial to attain maximum energy restoration. Note that the row driver circuitry is similar to the conventional row driver circuit (shown in Fig. 5.1), with the exception being the inclusion of the BUFF_EN signal in the row buffer to facilitate tri-state mode operation.

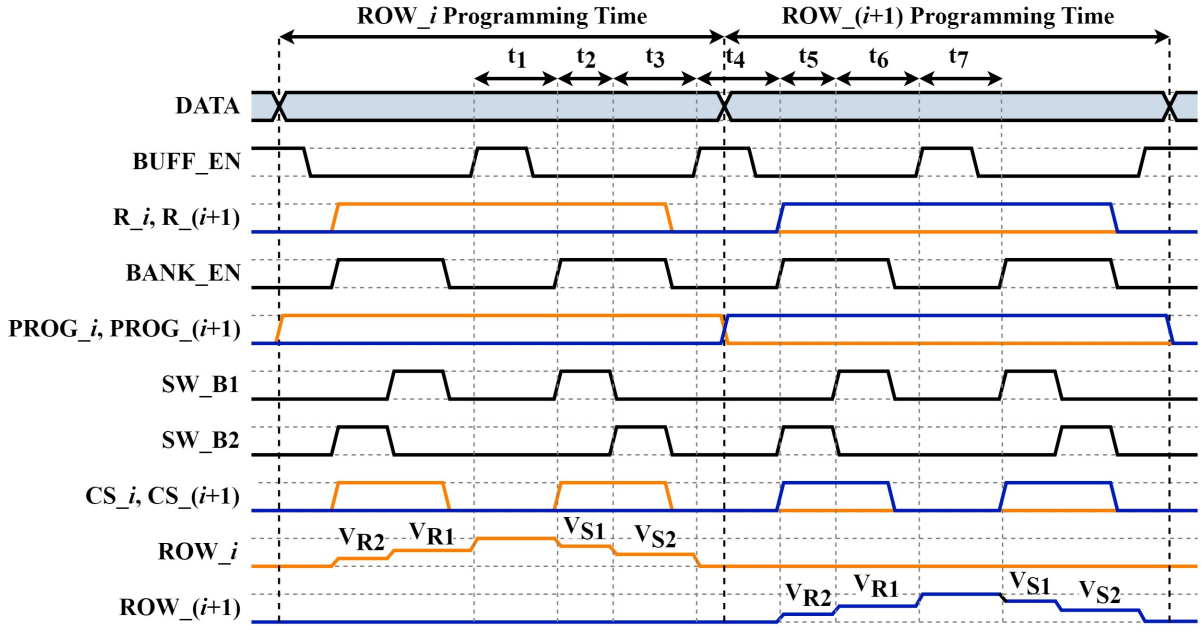


Figure 5.10: The timing diagram of the control and row signals of two consecutive rows using the two-capacitor bank energy recycling technique.

As depicted in Fig. 5.10, the waveforms of two successive programming times are illustrated with this technique to demonstrate this approach. The adoption of the two-capacitor bank technique involves two stages of energy storage and recycling for every row signal. Similar to the previous section, following several cycles of charge sharing between the row lines and the capacitor banks, the voltage of each bank oscillates between two distinct values (i.e., the stored value and the recycled value). V_{S1} and V_{S2} refer to the C_{B1} and C_{B2} voltages after receiving energy from a row line (i.e., stored value) and V_{R1} and V_{R2} refer to their voltages after transferring energy (i.e., restored/ recycled value) to a row line, respectively.

Let us study the effect of α and β coefficients on the maximum voltage that can be recycled with this technique. Similar to what we had in the previous section at time t_1 the i^{th} row is fully charged, and the pixels are programmed with new data values. At the beginning of t_2, the row line is in tristate mode (look at BUFF_EN signal) and since both PROG_i and BANK_EN are active the CS_i switch is turned on. Additionally, SW_B1 is activated, causing C_r to undergo charge sharing with C_{B1} and store a portion of its energy therein. From Eq. 5.4 the stored voltage value is

$$V_{S1} = \frac{V_{DD} + \alpha V_{R1}}{1 + \alpha}. \tag{5.8}$$

At the time t_3, SW_B1 is deactivated, while SW_B2 is activated. Hence, the $i^{th}C_r$ disconnects from C_{B1} and engages in charge sharing with the second bank (C_{B2}) with the rest of the energy left on it. So,

$$C_r \times V_{ROW\_i}(t_2) + C_{B2} \times V_{B2}(t_2) = C_r \times V_{ROW\_i}(t_3) + C_{B2} \times V_{B2}(t_3) \tag{5.9}$$

considering that the $i^{th}C_r$ and C_{B2} voltages before charge sharing are V_{S1} and V_{R2}, respectively, the above equation could be rewritten as follows:

$$C_r \times V_{S1} + \beta C_r \times V_{R2} = C_r \times V_{S2} + \beta C_r \times V_{S2} \tag{5.10}$$

replacing V_{S1} from Eq. 5.8 and rewriting the equation, V_{S2} is

$$V_{S2} = \frac{V_{DD} + \alpha V_{R1} + (1 + \alpha)\beta V_{R2}}{(1 + \alpha)(1 + \beta)}. \tag{5.11}$$

At the start of t_4, when BUFF_EN is activated and R_i is set to '1', the remaining energy stored in the $i^{th}C_r$ discharges to the ground through NMOS transistors in the row line buffer. During the subsequent programming cycle, the $(i+1)^{th}C_r$ receives energy from C_{B2}, which has a lower energy state. The capacitors' charge levels before and after sharing are

$$C_r \times V_{ROW\_(i+1)}(t_4) + C_{B2} \times V_{B2}(t_4) = C_r \times V_{ROW\_(i+1)}(t_5) + C_{B2} \times V_{B2}(t_5) \tag{5.12}$$

since the $((i+1)^{th}C_r$ and C_{B2} voltages are '0' and V_{S2} (From the last charge sharing at time t_3), respectively, the above equation can be expressed in the following form:

$$C_r \times 0 + \beta C_r \times V_{S2} = C_r \times V_{R2} + \beta C_r \times V_{R2} \tag{5.13}$$

replacing V_{S2} from Eq. 5.11 and rewriting the equation, V_{R2} is

$$V_{R2} = \frac{\beta V_{DD} + \alpha\beta V_{R1}}{(1 + \alpha)(1 + 2\beta)}. \tag{5.14}$$

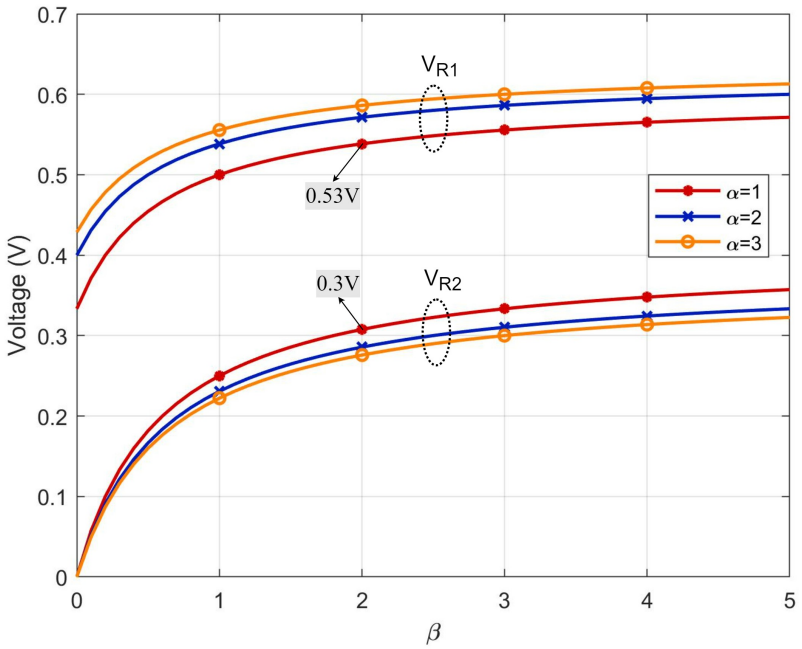


Figure 5.11: The recycled voltage from C_{B2} (V_{R2}) and C_{B1} (V_{R1}) versus β for different α, using the energy recycling technique with two capacitor banks.

The value of V_{R2} represents the amount of energy that can be recycled during the first step of energy restoration. Next, at the beginning of t_6, SW_B2 is turned off and SW_B1 is turned on. As a result, the $(i+1)^{th}C_r$ disconnects from C_{B2} and connects to C_{B1}. So,

$$C_r \times V_{ROW\_(i+1)}(t_5) + C_{B1} \times V_{B1}(t_5) = C_r \times V_{ROW\_(i+1)}(t_6) + C_{B1} \times V_{B1}(t_6) \tag{5.15}$$

at the time t_5 the $(i+1)^{th}C_r$ charge is V_{R2} which was obtained from the previous charge sharing with C_{B2}, and the charge of C_{B1} is V_{S1}, which was obtained from the charge sharing that occurred at time t_2.Therefore,

$$C_r \times V_{R2} + \alpha C_r \times V_{S1} = C_r \times V_{R1} + \alpha C_r \times V_{R1} \tag{5.16}$$

replacing V_{S1} and V_{R2} from Eq. 5.8 and Eq. 5.14 and rearranging the above equation, V_{R1} is

$$V_{R1} = \frac{(\alpha + \beta + 2\alpha\beta)V_{DD}}{(1+2\alpha)(1+2\beta) - \alpha\beta}. \tag{5.17}$$

V_{R1} is the total voltage that can be recycled using two capacitor banks for a given V_{DD} and capacitor ratios. Assuming V_{DD}=1, Fig. 5.11 illustrates the recycled voltages versus the ratio of the second capacitor bank to C_r (i.e., β) for various values of α. By comparing Fig. 5.11 and Fig. 5.7, it becomes evident that using two capacitor banks provides benefits. For instance, when α =2, the maximum recycled voltage increases from 0.4V to 0.57V by using two capacitor banks with β=2. The benefit of extra energy recycling comes at the expense of two extra switches and their control signals and an additional capacitor. Similar to what we mentioned for choosing the proper size for α, according to Fig. 5.11 the recycled voltage value saturates for larger β values. Hence, it is necessary to carefully consider the overhead of control signal power consumption during the design process.

The concept of energy recycling can be extended to a greater number of capacitor banks. Assuming all banks start with no charge and have the same size (C_r), during the initial round of charge sharing, 50%, 25%, 12.5%, 6.25%, and so forth, of the energy on C_r would be distributed to the respective banks. Subsequently, for the next row's capacitor, the recycled energy would be 25%, 12.5%, 6.25%, 3.125%, and so on. By calculating this series, it becomes evident that the maximum energy transfer achievable is limited to 50% of the initial energy on C_r. Consequently, for a higher number of capacitor banks, the recyclable energy reaches a saturation point.

Taking into account the additional area required for more capacitor banks and the increased power consumption associated with generating specific enable signals for switches to implement this technique for a greater number of banks, it becomes apparent that increasing the number of banks beyond 2 may not yield significant benefits. Also, each additional bank necessitates two extra time slots for charge sharing. This time-related overhead serves as a critical factor that enforces a limitation on the number of banks employed.

5.1.3 Direct Energy Restoration

Previous energy recycling techniques used capacitor banks to transfer the energy from one row to another. However, the energy can be transferred between rows directly avoiding the area required for the capacitor banks. Fig. 5.12 illustrates the scanning procedure of the direct energy restoration technique. This technique employs a single charge-sharing time slot within each programming cycle. At the beginning of each row's programming time, the row line has already received some energy directly from the preceding row and requires complete charging to V_{DD}. Subsequently, towards the end of the programming time for that row line, it will directly transfer a portion of its energy to the next row line and then fully discharge.

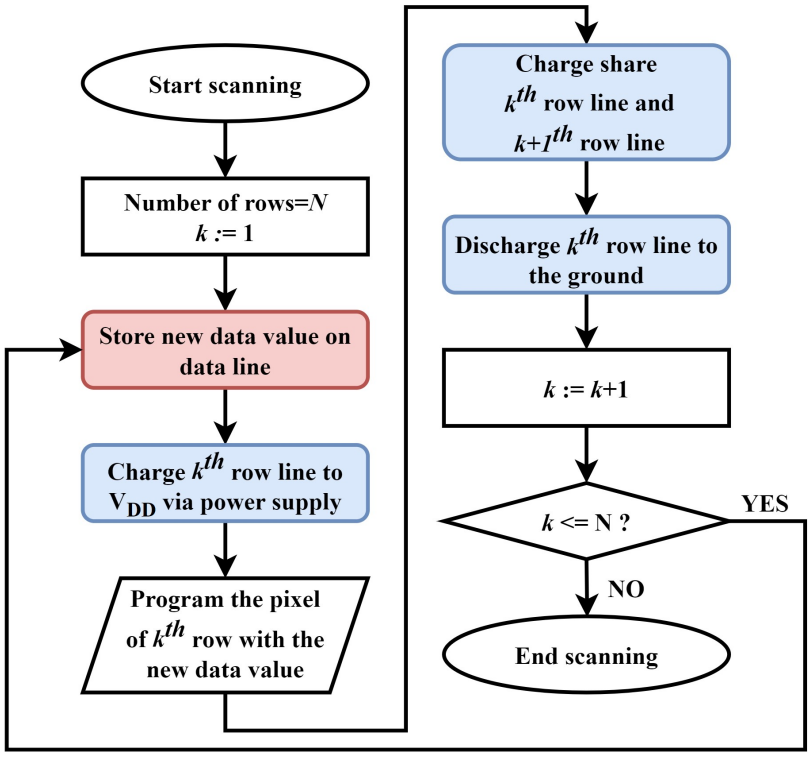


Figure 5.12: The process of scanning a data line in a display with the direct energy restoration technique.

Fig. 5.13 illustrates the $N \times M$ display utilizing the direct energy restoration technique. Compared to the energy restoration architecture with one capacitor bank (depicted in Fig. 5.5)), in this technique, there are two buffer enable signals generated by the signal generator, and the row driver generates a distinct BUFF_EN_i signal for each row buffer. Employing this enable signal, the row line is isolated from the supply voltage and ground during specific time intervals. This allows for the transmission gate to create a connection between two consecutive rows. To generate the enable signals for these switches, a pair of NAND and NOT gates are used for each row.

During each charge-sharing event between two adjacent rows, it is essential for both rows to be in the tri-state mode to ensure efficient energy transfer without any energy loss. In other words, each row line must enter the tri-state mode twice: once when receiving energy from the preceding row and once when transmitting energy to the subsequent row. To achieve this, the row driver circuit depicted in Fig. 5.14 utilizes two BUFF_EN signals

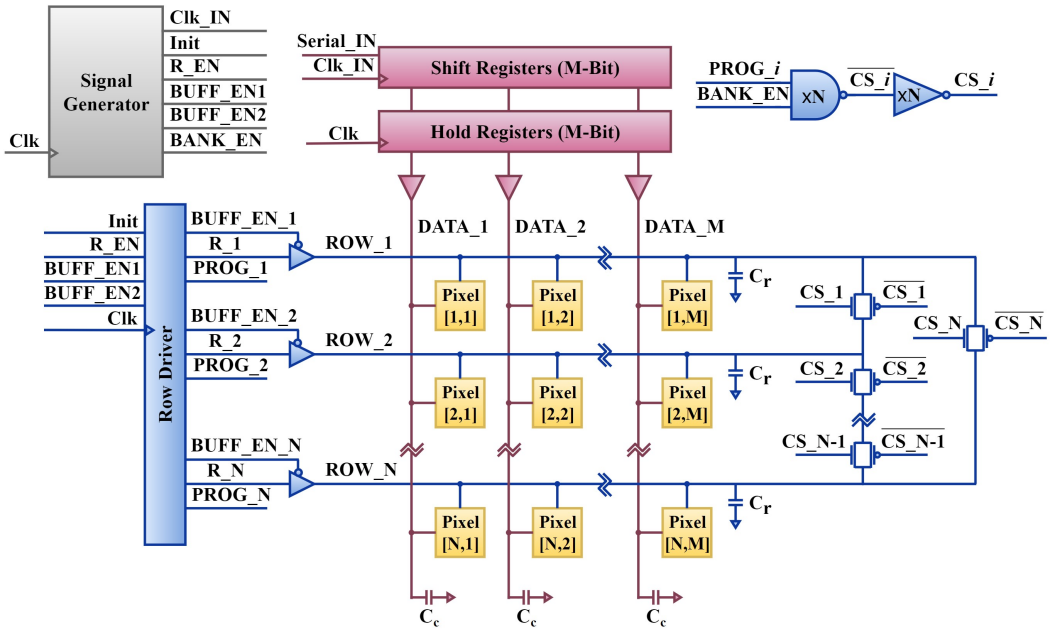


Figure 5.13: The $N \times M$ active-matrix display with direct energy recycling technique.

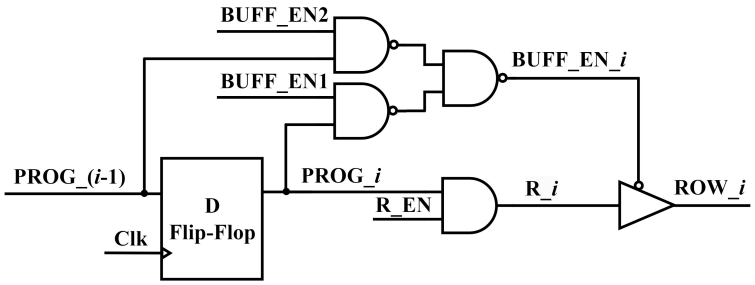


Figure 5.14: The ROW_i driver in a display that employs the direct energy recycling technique.

to generate the BUFF_EN_i signal unique to each row.

Fig. 5.15 shows the timing diagram of signals when employing the direct energy restoration technique. At the time t_1 the pixels of the i^{th} row have already been programmed with proper data values and the row enable signal (ROW_i) can be disabled. However, a portion of energy must be recycled prior to discharging it to the ground. Therefore, at time t_2 the buffers of both lines (i.e., i^{th} and $(i+1)^{th}$ row lines) are isolated from the supply voltage and ground. Subsequently, at time t_3, the CS_i signal becomes '1' and the switch between

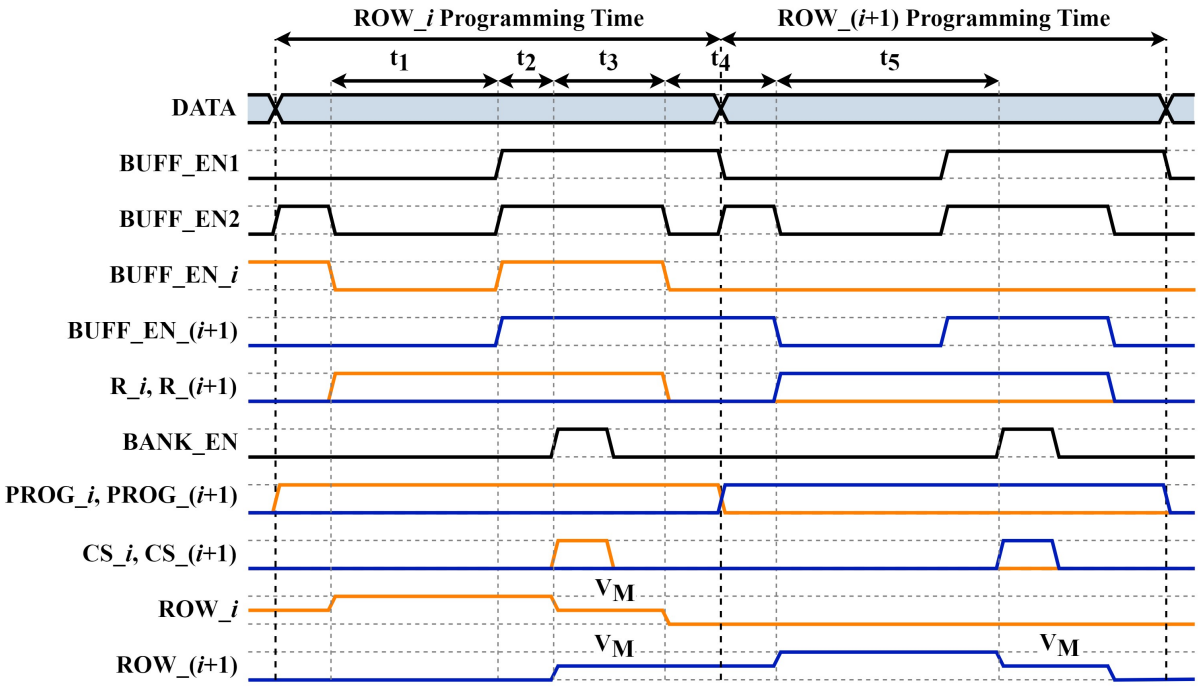


Figure 5.15: The timing diagram of the control and row signals of two consecutive rows using direct energy recycling technique.

the i^{th} row (i.e., the energy donor row) and the $(i+1)^{th}$ row (i.e., the energy acceptor row) is activated. This allows the charge sharing between the fully charged capacitor of the i^{th} row and the capacitor of the $(i+1)^{th}$ row, which is at voltage zero. As a result of this charge-sharing process, both capacitors reach the final voltage of V_M.

As we mentioned before, the C_r capacitor consists of two components, one being a non-linear capacitor of the access transistors' gate, and the second being the liner interconnect wiring capacitance. The former is at its maximum value if the gate voltage is at V_{DD}, and the source and drain terminals are at 0V. It is at its minimum value if all terminals are at 0V. This is attributed to the change in the transistor's channel capacitance. This results in the energy donor row exhibiting a higher average capacitance than the energy acceptor row during the charge-sharing time slot, ultimately leading to a final voltage that exceeds half of the V_{DD} voltage.

Later, at time t_4, the buffer for the energy donor row is enabled, causing the remaining energy stored in the capacitor of the i^{th} row to discharge to the ground. Note that at this point, the buffer for the energy acceptor row remains deactivated. At the time t_5, the

buffer of the $(i+1)^{th}$ row is enabled and the capacitor is fully charged to V_{DD} via the PMOS transistors in the buffer. This process is then repeated for subsequent rows in the display. By implementing this technique in the row driver, the dynamic power consumption of the row buffers is reduced by over 50%. Moreover, this technique necessitates less area and timing overhead since it eliminates the need for a capacitor bank and reduces the number of charge-sharing time slots associated with each programming time to only one.

It is important to note that the threshold voltage of the pixel access transistor must be high to prevent the access transistor of the energy acceptor row from turning on after the charge-sharing process. In our specific design, we have implemented high threshold voltage access transistors to ensure the proper functionality of the circuit.

5.2 Energy Restoration Technique for Data Driver

The data driver is the most power-intensive component in the display's peripheral circuitry. Our simulation results demonstrate that the power consumption of the data driver can be up to 1.7-9.8 times higher than that of the row driver, depending on the image content. Considering this and the increase in dynamic power consumption resulting from advancements in display characteristics, it is critical to reduce the dynamic power consumption of the data driver to enhance overall energy efficiency. The flowchart depicted in Fig. 5.16 illustrates the scanning process of a data line in a display utilizing the energy recycling technique on the data driver. At the beginning of each programming time, a comparison takes place between the new data value and the previous data value associated with the data line. If there is a disparity between these values, the data line can assume one of two roles: an energy donor, signifying a change in data value from '1' to '0', or an energy acceptor, signifying a change in data value from '0' to '1'. Consequently, as long as a discrepancy exists between the previous and new data values, the data line will be connected to the capacitor bank as well as other donor/acceptor data lines. Following the charge-sharing process, the data line will either discharge or fully charge depending on its new data value. The rest of the scanning process follows a conventional approach.

Fig. 5.17 shows the energy recycling technique on the data driver. To implement the energy recycling feature, the following circuit components have been added to each data line:

1. A data storage unit (i.e., storage capacitor) to store the previous value of the data.
2. A transmission gate to be utilized as a switch to connect the capacitor of the data line (C_c) to the capacitor bank (C_B).

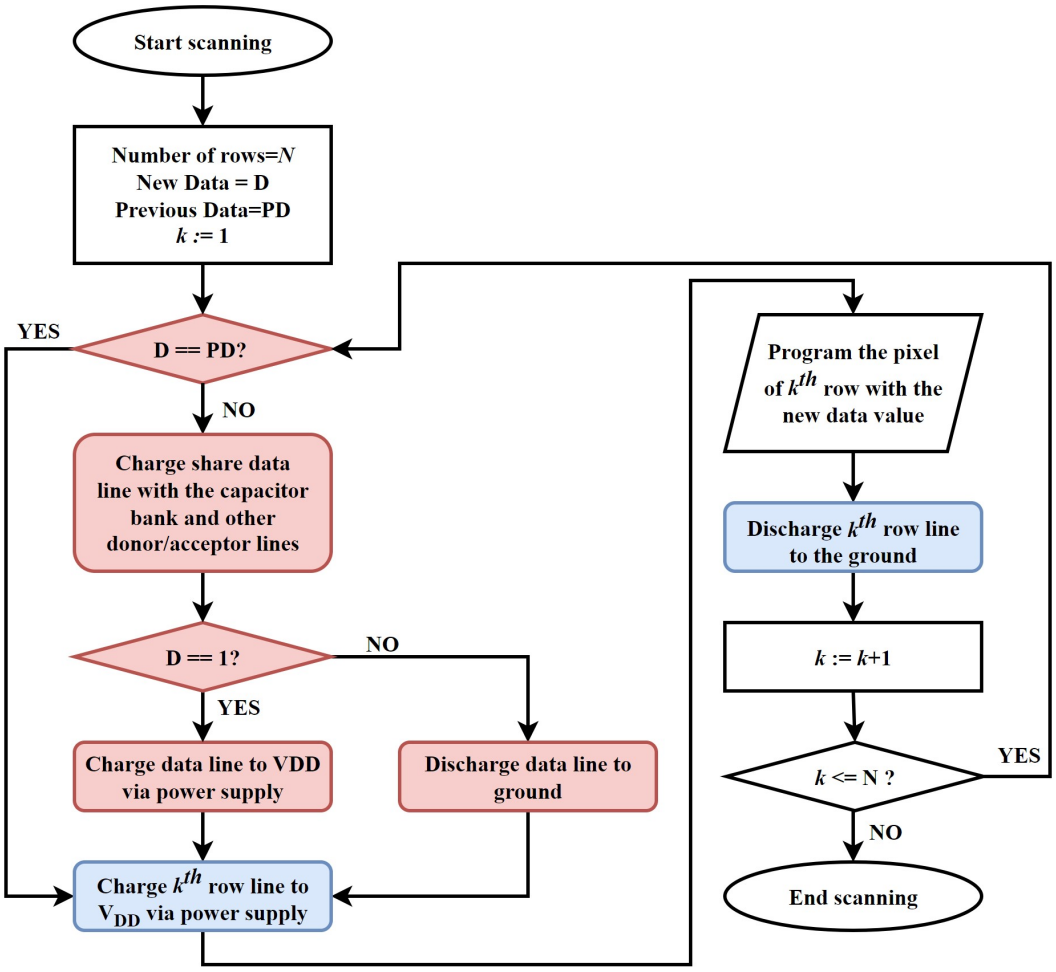


Figure 5.16: The process of scanning a data line in a display with the energy restoration technique for data driver.

3. A circuit to generate the charge recycling signal (i.e., CS_j) for enabling and disabling the transmission gates.

In addition, a shared capacitor bank (C_B) and control signals generated in the signal generator block are also required.

At each charge recycling interval, a data line will be connected to the bank in two scenarios:

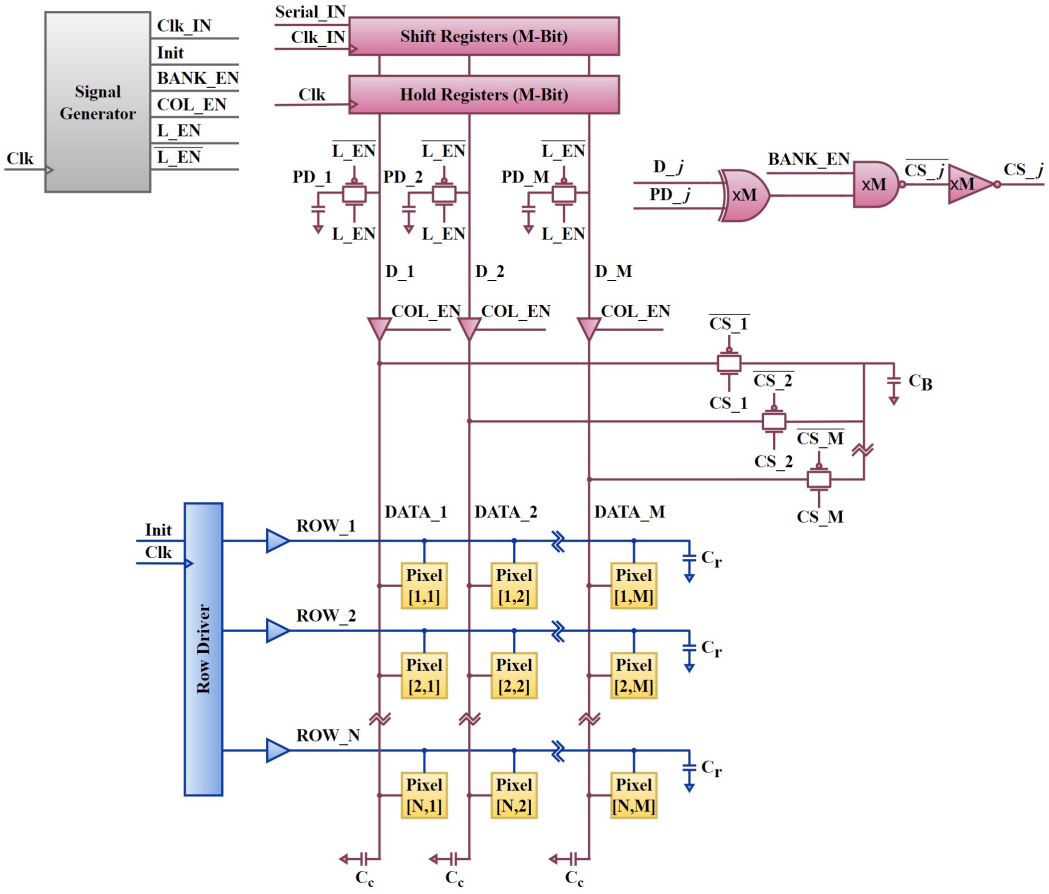


Figure 5.17: The $N \times M$ active-matrix display architecture using the energy recycling technique in the data driver.

- If the current data on the data line is '1' and the next data is '0'. This means that the energy on the C_c capacitor of the line is going to be discharged to the ground. Therefore, first, a portion of energy will be stored in the capacitor bank (C_B) and later the remaining energy will be discharged to the ground. These data lines are referred to as donor data lines during this specific recycling interval.

- If the current data on the data line is '0' and the next data is '1', the data line is referred to as an acceptor data line, as it receives some energy from the capacitor bank and is then fully charged to V_{DD} using the supply voltage.

In cases where the data value remains unchanged between two consecutive programming

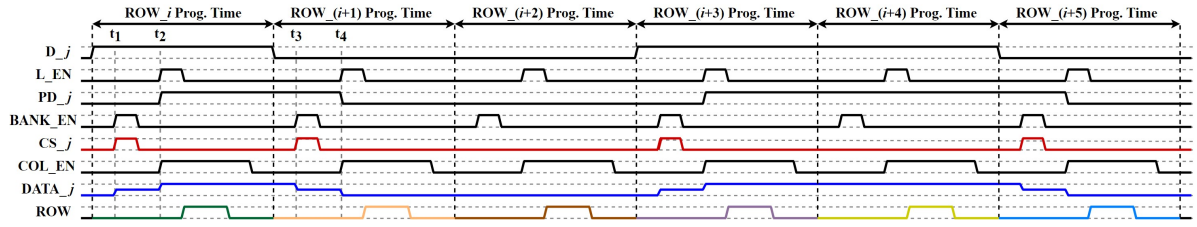


Figure 5.18: The waveforms of six consecutive programming times using the energy recycling technique in the data driver.

cycles, the data line is not connected to the capacitor bank and retains its value.

As previously stated, each data line incorporates a circuit that generates its corresponding charge recycling signal (CS_j), which is responsible for enabling or disabling the connection to the capacitor bank. This circuit utilizes an XOR gate to identify any variation between the previous data (PD_j) and current data (D_j) values. During the recycling interval (activated by the BANK_EN signal), if a discrepancy exists between the current and previous data values, the NAND and inverter gates produce an output that links the data line to the capacitor bank via the data line transmission gate for the duration of the recycling interval.

Fig. 5.18 illustrates the timing diagram of the control, row, and data signals for 6 consecutive programming times of the j^{th} data line, assuming a data sequence of "0100110". The signal L_EN is enabled in each programming time and stores the data on a small capacitor that later in the next programming time is used as the previous data (PD_j).

At the beginning of the first programming time, the data line's buffer is disconnected from the supply voltages (COL_EN=0). At the time t_1, the current data value (D_j) is '1' and the previous data value (PD_j) is '0', therefore the data line's XOR gate output is '1'. Since the bank enable signal (BANK_EN) is enabled at time t_1 and the output of the XOR is '1', at that time the data line's charge recycling signal (CS_j) will be enabled. So, the transmission switch of this data line turns on to connect it to the capacitor bank to receive energy from the bank.

Note that during this charge recycling interval, all data lines whose previous and current data values are different will be connected to the capacitor bank at the same time. Those data lines that currently have a value of '1' will be the donor of the energy and those that currently have a value of '0' will be the acceptor of the energy from the bank and other data lines. At the time t_2, this new data value will be stored in the storage unit's capacitor for comparison in the next programming cycle. Also, since the COL_EN is enabled, the

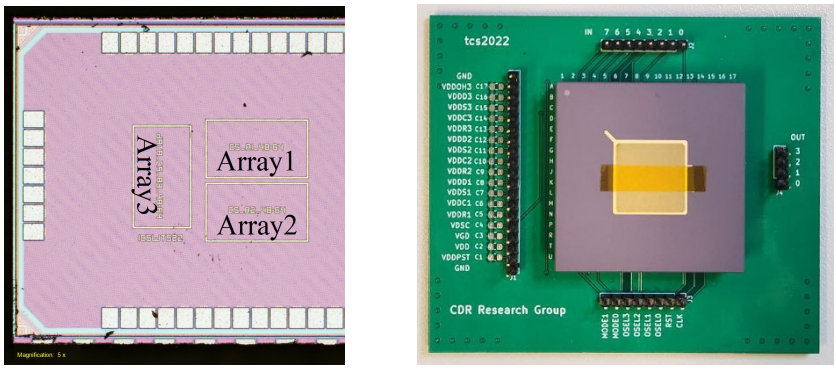
capacitor of the data line will be fully charged to V_{DD} via the PMOS transistors in the data line's buffer. At time t_3, the previous data value is '1' and the next data is '0', so the data line will be connected to the bank to donate a portion of its energy. It will be fully discharged at time t_4 when the data line's buffer is enabled. At the charge recycling interval of the 3^{rd} row's programming time, the previous and next data values are both '0', and the data line is not connected to the bank. Later, for programming the 4^{th} row the data line is getting some energy from the bank. It will hold the value of '1' at the charge recycling interval of the 5^{th} row because the previous data value and the next one, are both '1'. Finally, at the charge recycling interval of the 6^{th} row because the next value is '0' the data line donates a part of the energy to the bank and then fully discharges.

It should be noted that the proposed method can also be implemented without the capacitor bank, which can help save on area. In such a scenario, there is no energy reservoir to transfer energy between programming cycles. Instead, during each programming cycle, the available donor data lines will transfer some of their energy to the existing acceptor data lines. The capacitor bank plays a crucial role in transferring energy between programming cycles and serves as an energy reservoir. It is especially beneficial in cases where there are insufficient donor data lines during a specific programming cycle. For instance, in the case of an image with horizontal black and white strips, all data lines act as donors during the programming time of a black line and as acceptors during the programming time of a white line. Without the capacitor bank, there would be no energy available to provide to the data lines when required. This is typically not the case for most real-life images, as there are usually both donor and acceptor data lines in each programming cycle. Therefore, the required size of the capacitor bank can be determined based on the characteristics of the images for the intended application of the display.

5.3 Measurement Results

To verify the effectiveness of the proposed techniques we have designed and implemented three experimental proof-of-concept 48×64 pixel arrays, including their signal generator module, row driver, and data driver, using TSMC 65 nm technology. The implementation of each module (i.e., data driver, row driver, and signal generator) allows for the separate measurement of their power consumption. Each implemented array has the following modes:

- *Array 1*: This array has three modes, the conventional mode, the one capacitor bank, and the two capacitor bank energy restoration modes for the row driver.



(a) (b)

Figure 5.19: (a) The micrograph of the implemented arrays on the test chip, and (b) the packaged test chip on the PCB board for the measurement.

- *Array 2*: This array has two modes, the conventional mode and the direct energy restoration mode for the row driver.
- *Array 3*: This array has two modes, the conventional mode, and the data driver energy restoration mode.

In all arrays, the signal generator module is responsible for generating signals to drive a VGA display with a resolution of 480×640, a color depth of 8 bits, and a refresh rate of 60 Hz. Fig. 5.19 displays the micrograph of the test chip, as well as the packaged test chip. The measurement configuration employed for these arrays follows a similar arrangement as illustrated in Fig. 4.17. In the case of these displays, distinct voltage islands are allocated to the row driver, data driver, signal generator, IO pads, and overhead circuitry, ensuring separate power supply management for each component. The appropriate voltages corresponding to each supply voltage island are connected accordingly, with the KEITHLEY-2400 source meter employed to measure the current drawn from the specific supply voltage island under examination. This methodology ensures accurate current measurement for the targeted supply voltage.

The average extracted capacitors from the pixel circuit layout are 1.65 fF for the row line and 1.05 fF for the data line. Consequently, when considering all 640 pixels in a row, the total row line capacitance amounted to approximately 1.05 pF. However, since there were only 64 pixels in a row, additional capacitors were needed to compensate for the remaining data lines (i.e., 640-64), resulting in an approximate value of 950 fF. Similarly, the total capacitance of a data line, taking into account all 480 pixels on the line, is approximately

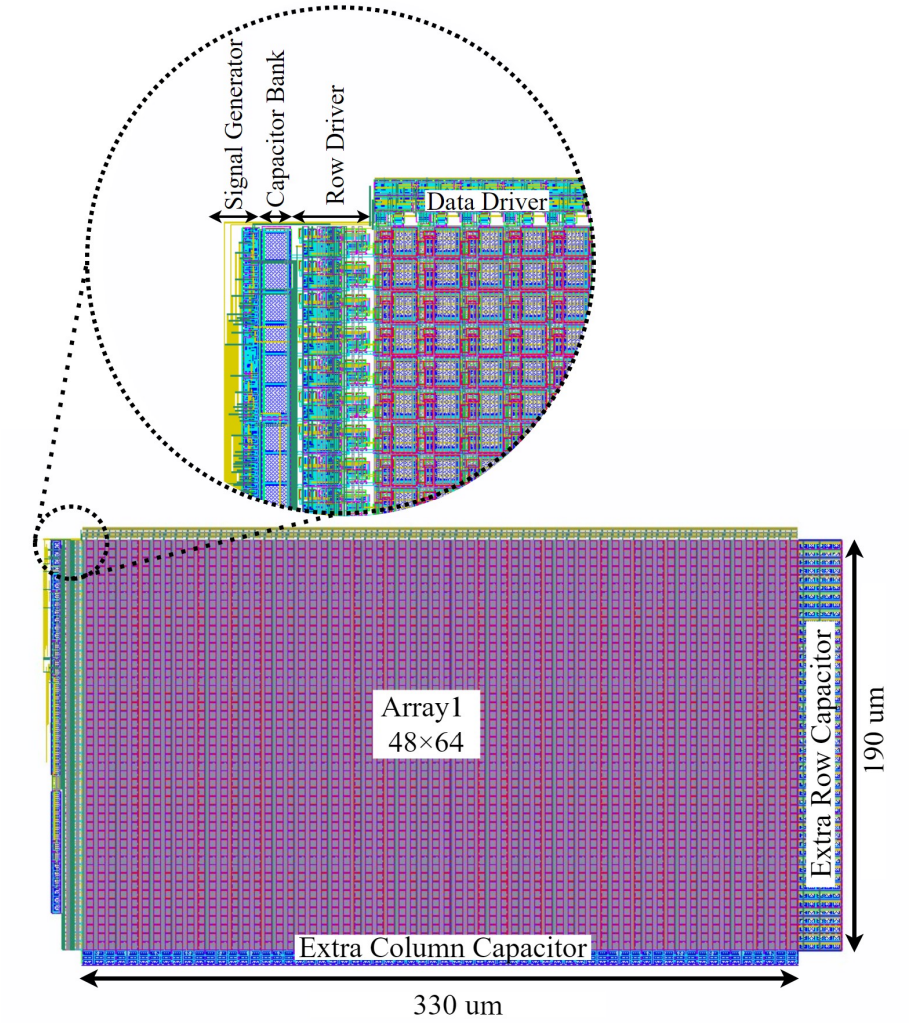


Figure 5.20: The layout of *Array 1* and the enlarged version that shows different blocks.

504 fF. However, with only 48 pixels on a data line, additional capacitors were required to compensate for the remaining rows (i.e., 480-48), amounting to an approximate value of 453 fF. Therefore extra Metal Oxide Semiconductor Capacitor (MOSCAP) capacitors have been added at the end of the row and data lines to replicate the capacitance load of a VGA-sized array.

To begin with, let's analyze the results of *Array 1* and *Array 2*, as both of them employ techniques aimed at reducing the dynamic power consumption of the row driver.

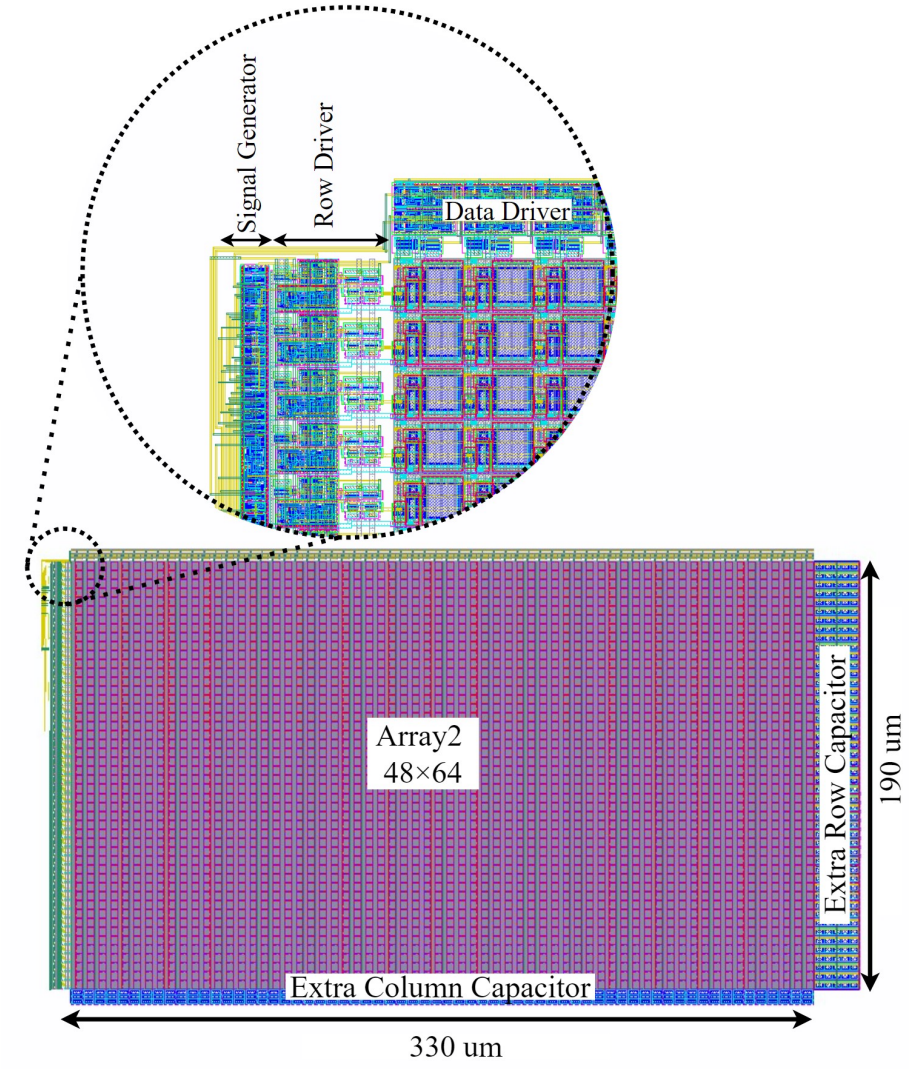


Figure 5.21: The layout of *Array 2* and the enlarged version that shows different blocks.

Fig. 5.20 shows the layout implementation and size of *Array 1*. The enlarged section of the layout demonstrates the incorporation of the capacitor bank in our design. Given that this particular test chip supports multiple modes, we have included two capacitor banks in order to disable one of them for conducting measurements of the one-capacitor bank technique. Furthermore, the sizes of the capacitor banks can be adjusted to facilitate the examination of the impact of varying sizes on power consumption reduction. The figure

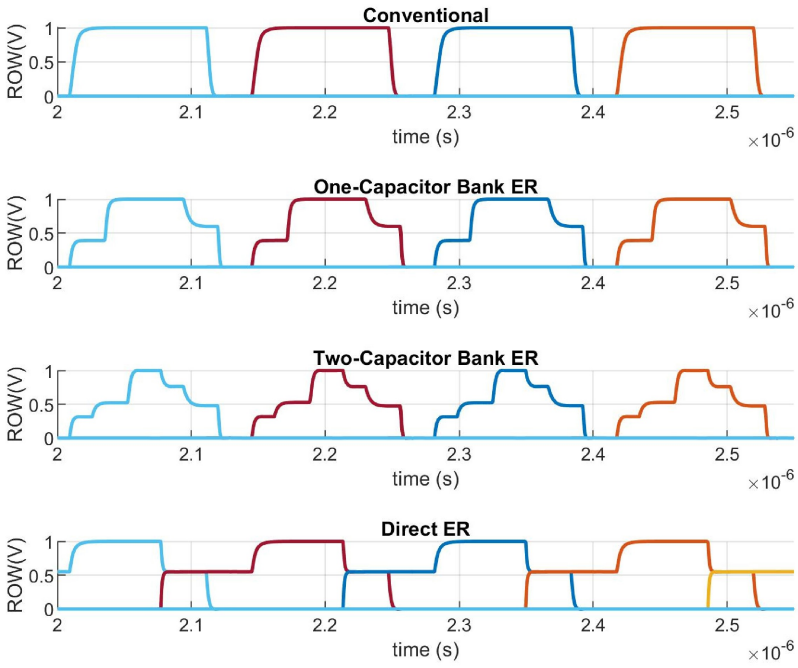


Figure 5.22: Four consecutive row signals using the conventional display and displays with the one-capacitor bank, two-capacitor bank, and direct energy restoration techniques.

depicts the capacitor banks implemented using MOSCAPs. To reduce the area overhead, an alternative approach could have been used by implementing MIM caps on top of the row driver layout.

Fig. 5.21 demonstrates the layout of *Array 2*. This layout closely resembles that of *Array 1*, except for the absence of the capacitor bank due to the implementation of the direct energy restoration technique, which eliminates the need for a bank.

Fig. 5.22 depicts the simulation results of four consecutive row signals in the conventional display mode, as well as the displays using the three proposed energy recycling techniques for the row driver. The results obtained from the simulation support the theoretical formula that was previously derived. The formula predicted that setting α to 2 in the one capacitor bank energy restoration mode would yield a stored voltage of 0.6V, with 0.4V restored on the next row capacitor, consistent with the findings depicted in Fig. 5.7. In the investigation of the two-capacitor bank energy restoration mode, α was set to 1, and β was set to 2. The results of the simulation show that the restored voltage for V_{R1} is 0.53V and for V_{R2} is 0.3V, which agrees with the results presented in Fig. 5.11. Hence,

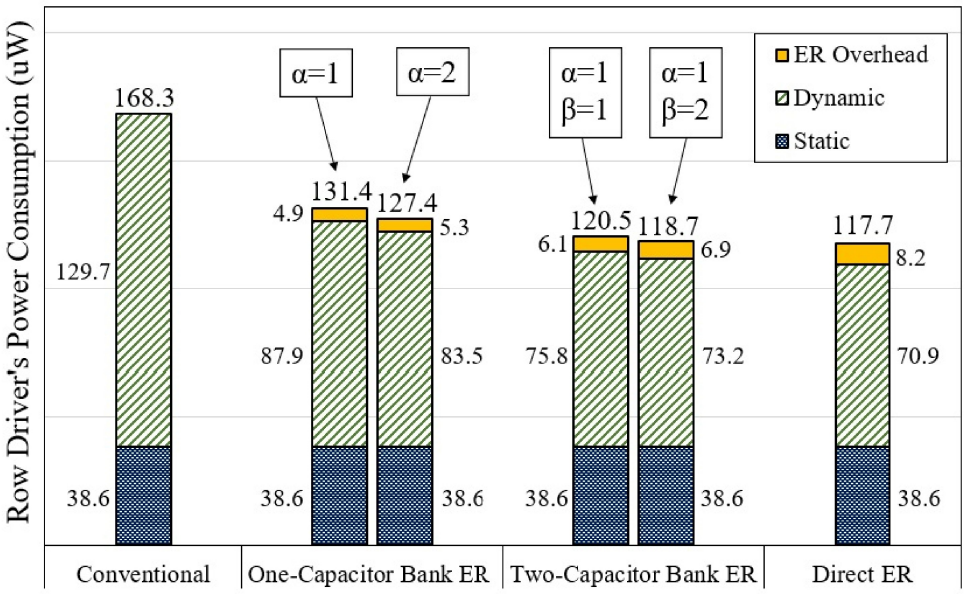


Figure 5.23: The measurement results of the row driver's power consumption for different power-saving techniques and different capacitor bank sizes in a VGA display.

the simulation findings validate that the restored voltages of V_{R1} and V_{R2} conform to both the theoretical equations of Eq. 5.14 and Eq. 5.17 and the values illustrated in Fig. 5.11. Finally, the simulation waveforms for the direct energy restoration mode are presented. In contrast to the first two methods, there is an overlap between consecutive row signals in this mode, necessitating the use of high threshold voltage access transistors to prevent the programming of data that belongs to the previous row.

Fig. 5.23 illustrates the measurement results for the power consumption of the row driver in the VGA-sized arrays. The power consumption of each row line in the proof-of-concept arrays was measured and then scaled by a factor of 10 to find the power consumption of the row driver in a VGA display. In both *Array 1* and *Array 2*, the power consumption of the row driver is the same in the conventional mode, with dynamic power consumption accounting for nearly 77% of the total power. The dynamic power consumption is reduced by the suggested energy recycling techniques, but the static power consumption remains constant in all scenarios. The measurement of a single capacitor bank demonstrates a power reduction of 22% and 24% for two cases with α =1 and α =2, respectively. These reductions were determined after taking into account the power consumption overhead associated with the signals and components necessary for the energy

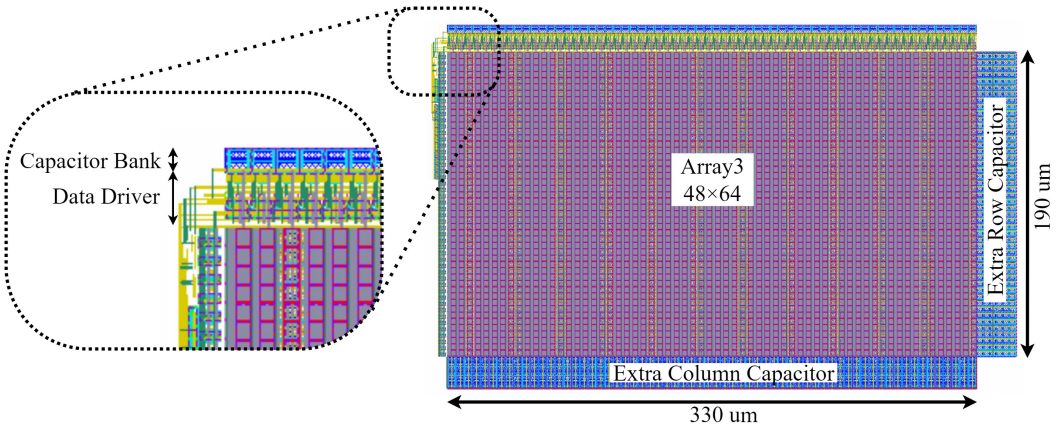


Figure 5.24: The layout of *Array 3*.

recycling technique. Theoretical calculations suggest that a larger capacitor bank yields greater energy savings. However, several factors, such as saturation of stored voltage, an increase in the area of the capacitor bank, and higher power consumption of control signals, offset this advantage as α exceeds 2. The energy restoration technique using two capacitor banks was evaluated through measurements for two cases with values of $\alpha = \beta = 1$ and $2\alpha = \beta = 2$, on silicon. The results indicate a power reduction of 28% and 29% for the respective cases. The obtained results confirm that the use of two capacitor banks effectively reduces the dynamic power consumption of the row driver, in comparison to the one-capacitor bank mode. The measurements also reveal that there is a saturation of restored voltage when doubling the size of the second capacitor bank. The measurement results for the direct energy restoration technique indicate a power reduction of 30% in the row driver. This method saves slightly more dynamic power consumption compared to the two-capacitor bank method. However, it has a higher overhead in terms of signal generation. Our measurements indicate that the power consumption of the row driver remains consistent across various test images, confirming its image independence.

Besides the power consumption overhead associated with the circuit used to enact the energy recycling technique, another significant consideration is the timing overhead linked to these techniques. Each of these techniques necessitates the allocation of time-sharing slots within the programming time for energy transfer. As previously mentioned, direct, one-capacitor bank and two-capacitor bank energy recycling techniques require 1, 2, and 4 charge-sharing time slots, respectively. In our implementation, we have set each charge-sharing time slot to 1/8 of the programming time. However, reducing this time slot to 1/16 of the programming time is possible while obtaining equivalent results. For displays

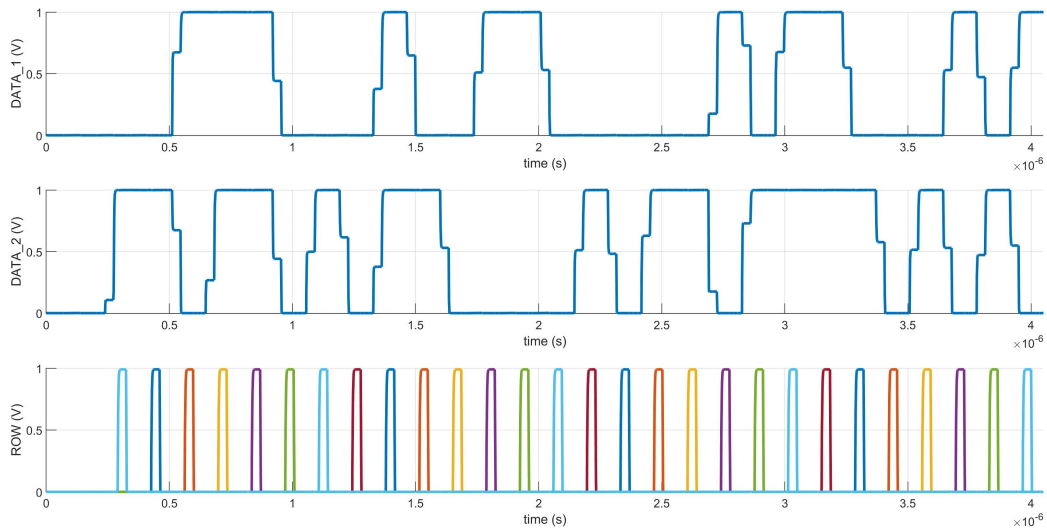


Figure 5.25: The data driver energy recycling technique waveforms for the first two data lines, along with the row enable waveforms.

with strict programming time limitations like high resolution and refresh rate displays, techniques like direct or one-capacitor bank energy restoration can be chosen to minimize timing overhead.

It is important to note that implementing these techniques on displays with higher resolution, pixels per inch (PPI), and refresh rates can result in a higher percentage reduction in overall power consumption. This is because displays with higher resolution have a higher ratio of dynamic power consumption to static power consumption. Thus, reducing the dynamic power consumption by half has a greater impact on the overall power consumption.

Next, let's delve into the results obtained from the latest implemented array, *Array 3*, which incorporates the data driver energy recycling technique. Fig. 5.24 illustrates the layout of the array employing the data driver energy recycling technique. As shown in the enlarged section of the figure, the capacitor bank is a narrow blue rectangular shape positioned at the top of the array's layout with a size of approximately $0.2C_c$ or 100 fF per data line. This capacitor bank is used as the energy reservoir in our implementation. The capacitor bank's area overhead accounts for 2.5% of the display's total area and could have been avoided by using MIM capacitors on the data driver's circuit instead of the MOSCAP employed.

Figure 5.26: Random test images with different black-to-white pixel ratios.

Table 5.1: Comparing Power Consumption of conventional and low-power data driver arrays with random test images.

Test Image	*0% (Black)**	*10%*	*20%*	*30%*	*40%*	*50%*	*60%*	*70%*	*80%*	*90%*	*100%(White)**	*Average*
Conventional Array Power Consumption (uW)												
Row Driver	168.3	168.3	168.3	168.3	168.3	168.3	168.3	168.3	168.3	168.3	168.3	168.3
Signal Generator	18.3	18.3	18.3	18.3	18.3	18.3	18.3	18.3	18.3	18.3	18.3	18.3
Data Driver	**297.9**	**753**	**1130**	**1418**	**1560**	**1653**	**1527**	**1306**	**1047**	**702**	**299.3**	**1063.0**
Total Driver	484.5	939.6	1316.6	1604.6	1746.6	1839.6	1713.6	1492.6	1233.6	888.6	485.9	1249.6
Low-Power Data Driver (uW)												
Row Driver	169	169	169	169	169	169	169	169	169	169	169	169.0
Signal Generator	18.5	18.5	18.5	18.5	18.5	18.5	18.5	18.5	18.5	18.5	18.5	18.5
Data Driver	**300.9**	**596**	**849**	**1030**	**1132**	**1155**	**1080**	**946**	**779**	**566**	**312**	**795.1**
Energy Recycling Overhead	**37.1**	**69**	**100**	**129**	**147.8**	**159**	**147**	**117**	**89**	**57**	**28**	**98.2**
Total Driver	525.5	852.5	1136.5	1346.5	1467.3	1501.5	1414.5	1250.5	1055.5	810.5	527.5	1080.8
Power Consumption Reduction %												
Data Driver (Including the ER Circuit)	-13.5	11.7	16.0	18.3	18.0	20.5	19.6	18.6	17.1	11.3	-13.6	16.0
Total Driver (Signal Generator, Row and Data Drivers)	-8.5	9.3	13.7	16.1	16.0	18.4	17.5	16.2	14.4	8.8	-8.6	13.5

*** No Energy Recycling**

Fig. 5.25 presents the data value waveforms of the first two data lines, depicting the programming of distinct pixel circuits on these lines. These waveforms correspond to a randomly generated test image in which 50% of the pixels are black. It is evident from the figure that the level of restored voltage varies based on the number of available donor and acceptor data lines at each programming cycle as well as the amount of the capacitor bank energy.

Fig. 5.26 depicts a set of 10 randomly generated test images, each characterized by varying black-to-white pixel ratios. These images were employed to evaluate the power consumption of the array. Table 5.1 provides a comparative analysis of the measured power consumption of the array in both conventional and data driver energy recycling modes. The design of the array allows for individual measurement of the power consumption of each primary block of the display driver. According to the measurement results, it was observed that the power consumption of the row driver and signal generator blocks remains unaffected by the image displayed, also consistent between both conventional and low-power data driver modes. The energy recycling overhead entry in the table includes the power consumption of the signal generator block, necessary for generating the required signals in the proposed method as well as the extra circuitry needed for each data line energy restoration. The power consumption of the data driver is notably influenced by

the test image, as observed in the conventional array. Specifically, the highest power consumption of the data driver occurs during the 50% random test image, which aligns with the expectation that the dynamic power consumption of the data driver is directly proportional to the level of data activity.

The data driver low-power technique demonstrates the highest energy recycling when the number of donor and acceptor data lines is closely matched (e.g., 50% test image). The extent of energy recycling is directly proportional to the balance between the donor and acceptor data lines, and this effectiveness decreases as the balance between these lines becomes less optimal. In situations where there is an uneven number of donor and acceptor data lines between programming cycles, the presence of a capacitor bank generally aids in enhancing the overall power recycling capacity. The results obtained from measuring *Array 3* in the low-power mode demonstrate that, after accounting for the additional power consumption associated with the energy recycling circuitry, the data driver power is reduced up to 20%. Furthermore, the overall power consumption of the driver, which includes the row driver, data driver, and signal generator, is reduced up to 18% with the utilization of the proposed technique. This power reduction is achieved specifically during the peak power consumption of the display. This finding highlights the potential benefits of the proposed data driver energy recycling technique, especially in scenarios where there is a high data toggle rate and power consumption is a significant concern. It should be noted that in the cases of white or black images, no energy recycling occurs due to the absence of donor and acceptor data lines. In fact, the overhead of the extra energy recycling circuitry in these extreme cases can result in a deterioration of the driver's power consumption. The measurement results indicate that the overall driver power consumption may degrade by 8.5% in such scenarios. However, it is important to highlight that these cases are infrequent, and a power gating mechanism could be implemented to disable the extra circuitry for such rare occurrences. Furthermore, the measurement results reveal that even with a low data activity (e.g., 10% or 90% test images), the proposed low-power technique still yields benefits.

The previous tests focused on measuring the power consumption of the drivers for a subframe with a black-and-white image. However, to evaluate grey levels, it is necessary to run the display for a full frame and measure the power consumption accordingly. For this purpose, real-life test images from Fig. 5.27 were selected to examine the power consumption in a broader context. Table 5.2 presents the power consumption of each test image for a full frame duration. Among the four real-life images used, the power consumption reduction of the drivers ranged from 7.5% for the Lenna image to 14.1% for the Houses image. As discussed previously, the effectiveness of this technique is more prominent when the data activity rate is higher in an image. Therefore, the Houses image,

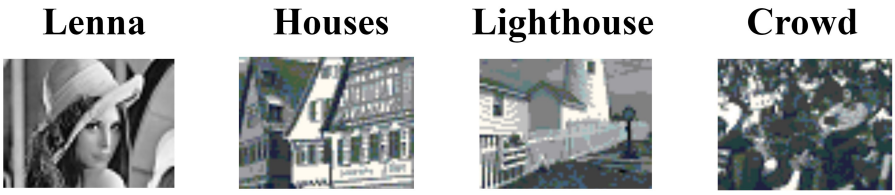


Figure 5.27: Four real-life test images.

Table 5.2: Comparing Power Consumption of conventional and low-power data driver arrays with real-life test images.

Test Image	***Lenna***	***Houses***	***Lighthouse***	***Crowd***	***Average***
Conventional Array Power Consumption (uW)					
Row Driver	168	168	168	168	168
Signal Generator	18	18	18	18	18
Data Driver	**672**	**875**	**802**	**786**	**783.8**
Total Driver	858	1061	988	972	969.8
Low-Power Data Driver (uW)					
Row Driver	169	169	169	169	169
Signal Generator	18	18	18	18	18
Data Driver	**549**	**637**	**603**	**594**	**595.8**
Energy Recycling Overhead	**58**	**87**	**75**	**71**	**72.8**
Total Driver	794	911	865	852	855.5
Power Consumption Reduction %					
Data Driver (Including the ER Circuit)	9.7	17.3	15.5	15.4	14.4
Total Driver (Signal Generator, Row and Data Drivers)	7.5	14.1	12.4	12.3	11.6

which exhibits a higher data activity compared to the Lenna image, achieves a greater amount of power saving. Based on the findings presented it can be inferred that the proposed method offers distinct advantages, particularly in high data rate applications. Applying the proposed technique to high-specification displays can significantly reduce the overall power consumption even more, as dynamic power consumption has a more impactful role in displays with higher resolution, PPI, and refresh rate.

In our literature review, we extensively examined a range of low-power driving techniques that have been assessed across diverse technologies and display dimensions. Given the wide spectrum of state-of-the-art low-power driver designs applied to various array sizes, backplane technologies, and media technologies, it proves challenging to provide a comprehensive and meaningful comparison in a table format. Furthermore, some patented concepts lack detailed information pertaining to the power consumption of displays utilizing these techniques. In consideration of these complexities and limitations, it was not feasible to include a comparative table in this research.

5.4 Summary

This chapter presented four low-power techniques aimed at reducing the dynamic power consumption of the drivers in OLEDoS microdisplays. First, three energy recycling techniques have been proposed to mitigate the dynamic power consumption of the row driver. Theoretical formulas have been formulated to assess the impact of capacitor bank sizing on techniques that make use of a capacitor bank. Additionally, a fourth technique is introduced to address the dynamic power consumption of the data driver. To validate the effectiveness of these techniques, three proof-of-concept arrays were implemented using TSMC 65 nm technology. Measurement results from *Array 1* demonstrate that the utilization of low-power techniques incorporating capacitor banks can result in a power consumption reduction of up to 29% in the row driver. In contrast, the third technique, which involves direct energy transfer between two consecutive rows, was evaluated using measurements obtained from *Array 2*, revealing a 30% decrease in the row driver's power consumption. Lastly, the findings from *Array 3* indicate that the data driver's energy recycling technique can reduce the power consumption of the data driver by up to 20% after considering the power consumption of the additional circuitry.

Chapter 6

Conclusion

6.1 Thesis Contribution

The demand for portable display technology is experiencing significant growth, and devices such as cell phones, smartwatches, and laptops have become indispensable in people's lives. Additionally, there is a considerable demand for VR and AR applications that incorporate microdisplays. As all these devices operate on battery power, achieving a longer battery life has become a crucial distinguishing feature in the market. It is widely recognized that the display component is one of the major power consumers, and reducing its power consumption would have substantial benefits. In this thesis, we have focused on exploring new low-power drivers for microdisplays, with the primary objective of significantly decreasing the power consumption of this energy-intensive component.

We initially investigated the dual-driving method for digitally driven microdisplays, introducing a novel dual-driver pixel circuit. This method effectively reduces the number of subframes within a frame. Different design modes were examined, with a specific focus on the low-power mode, where the significant reduction in subframes resulted in a lowered operating frequency of the drivers. Consequently, this led to reduced power consumption in all peripheral circuitry of the display. Experimental results obtained from a proof-of-concept array, implemented in TSMC 65 nm technology, revealed a notable 39.4% decrease in driver power consumption compared to a conventional array while maintaining the same pixel brightness. Furthermore, we explored how the dual-driver method can be applied to improve other essential display features. Firstly, due to the fewer subframes, extended programming times are possible. This extra time can be utilized to program up to 8.5 times more rows, effectively increasing the display resolution by this factor. Secondly,

the refresh rate of the display can be enhanced, as each frame time job is completed sooner with the dual-driver method. Lastly, the surplus time resulting from the reduced number of subframes can be harnessed to increase the color depth of the design. Our research demonstrates the versatile advantages of the proposed dual-driving method. It significantly reduces power consumption in low-power mode, enhances display resolution, improves refresh rate, and enables increased color depth.

The second major contribution of this thesis involves the proposal of new low-power row drivers utilizing energy recycling techniques. The central idea is to harness and reuse the energy that would otherwise be wasted in the row driver. Three distinct energy recycling techniques have been developed, effectively reducing the dynamic power consumption of the row driver. The first two techniques employ capacitor banks as energy reservoirs to facilitate energy transfer between row lines. These methods ensure the independent operation of row lines while achieving an impressive power saving of up to 29% in a proof-of-concept display implemented using TSMC 65 nm technology. The third method introduces a direct energy transfer between two adjacent row lines, simplifying the process and eliminating the need for a separate capacitor bank. This approach enables the recycling of over half of the voltage, resulting in an overall 30% reduction in the row driver's power consumption.

Another significant contribution of this thesis is the proposal of a low-power data driver using the energy recycling concept. The data driver, being the most power-hungry block in the peripheral circuitry of the display, poses challenges in recycling energy due to its dependency on the image content. However, in this study, we have explored a low-power data driver with an energy recycling technique that effectively reduces the dynamic power consumption in a microdisplay, utilizing simple circuits for implementation. To validate the effectiveness of the proposed low-power data driver, we implemented it in a proof-of-concept display using TSMC 65 nm technology. Remarkably, employing this technique led to a reduction of up to 18.4% in the total power consumption of all peripheral circuitry. It is worth noting that the power consumption of the display increases with higher data activity in the image. Consequently, the proposed technique exhibits greater efficacy when power consumption is at its peak, addressing the critical need for power-saving measures in such scenarios.

6.2 Future Research Direction

To further expand the scope of research conducted in this thesis, there are several areas that can be explored in all three aspects discussed.

Building upon the proposed dual-driver method, its potential applications for other display enhancements can be investigated. An essential avenue to explore is compensation methods for dual-driver displays, leveraging the advantages offered by this technique.

While the dual-driver concept was studied here in the context of digitally driven displays, extending this concept to analog-driven displays holds promising potential. Implementing the dual-driver approach in analog-driven displays could lead to a significant reduction in the size of the DAC module by half, resulting in substantial benefits in terms of area reduction and power savings. Hence, a thorough investigation into this area is well-warranted.

Combining the energy recycling techniques in a single display can lead to further dynamic power savings. By integrating energy restoration in the data driver with the direct energy restoration technique for the row driver, higher power efficiency can be achieved while using only two charge-sharing times.

As previously mentioned, the data driver's energy restoration potential is more pronounced in high-data activity scenarios. To further enhance the technique, a pre-processing algorithm can be implemented to assess the data activity in the subsequent frame. By employing power gating, the energy restoration circuitry can be disabled when the data activity falls below a certain threshold. Similarly, the capacitor bank's effectiveness in transferring energy between programming times can be optimized using a pre-processing algorithm. This algorithm can assess the necessity of the capacitor bank from one programming cycle to another and disable it if it is not required for specific image contents. By leveraging these pre-processing algorithms and integrating multiple energy recycling techniques, the display can achieve even greater power savings, offering an efficient and adaptable solution for varying image contents and scenarios.

An additional aspect worth investigating is the combination of the dual-driver method with either energy restoration on the row driver, data driver, or both. Implementing these methods in a display can further reduce the dynamic power consumption of the display drivers. While these combined approaches offer potential benefits, it is essential to strike a balance between power savings and the associated circuit complexities. Thorough analysis and optimization are required to identify the most efficient combination of methods that maximizes energy recycling while minimizing any potential drawbacks, such as increased timing complexity or additional power consumption from the extra circuitry.

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