Design, Optimization and Fabrication of Amorphous Silicon Tunable RF MEMS Inductors and Transformers

by

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Abstract

High performance inductors are playing an increasing role in modern communication systems. Despite the superior performance offered by discrete components, parasitic capacitances from bond pads, board traces and packaging leads reduce the high frequency performance and contribute to the urgency of an integrated solution. Embedded inductors have the potential for significant increase in reliability and performance of the IC. Due to the driving force of CMOS integration and low costs of silicon-based IC fabrication, these inductors lie on a low resistivity silicon substrate, which is a major source of energy loss and limits the frequency response. Therefore, the quality factor of inductors fabricated on silicon continues to be low. The research presented in this thesis investigates amorphous Si and porous Si to improve the resistivity of Si substrates and explores amorphous Si as a structural material for low temperature MEMS fabrication.

The process development for depositing thick amorphous Si films at low temperature with good uniformity and surface roughness is presented. The film is optimized for our proposed application with acceptable optoelectronic properties and mechanical stress. Porous Si is also studied as another candidate to improve the resistivity of Si substrates. A Teflon etch cell was machined to electrochemically form porous Si at room temperature and the process conditions are optimized to achieve thick films with suitable porosity for multi-layer applications.

Planar inductors are built-on undoped amorphous Si in a novel attempt to improve the isolation of RF passive devices from the low resistivity Si substrate. A 56% increase in Q was measured by incorporating a thick amorphous Si film before depositing the underpass of the inductor. Planar inductors are also built-on a porous Si and amorphous Si bilayer and showed 47% improvement in Q compared to the same structure without a porous Si layer.

Amorphous Si is proposed as a low temperature alternative to polysilicon for MEMS devices. Tunable RF MEMS inductors and transformers are fabricated on low resistivity Si in a six mask process. The design concept is based on an amorphous Si and Al bimorph coil that is suspended and warps in a controllable manner that is accurately predicted by thermomechanical simulations. The tuning of the devices is achieved by applying a DC voltage and due to joule heating the air gap can be adjusted. A tunable inductor with a

32% tuning range from 5.6 to 8.2 nH and a peak Q of 15 was measured. A transformer with a suspended coil demonstrated a 24% tuning range of the mutual coupling between two stacked windings.

The main limitation posed by post-CMOS integration is a strict thermal budget which cannot exceed a critical temperature where impurities can diffuse and materials properties can change. The research carried out in this work accommodates this temperature restriction by limiting the RF fabrication processes to 150℃ to facilitate system integration on silicon.

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Contents

1 Introduction **1**
1.1 Research Motivation 1
1.1.1 Inductors and Transformers on Silicon 2
1.1.2 Low Temperature and Low Loss Films 3
1.1.3 Low Temperature MEMS Fabrication 3
1.1.4 Tunable RF MEMS Devices 4
1.2 Research Objectives 6
1.3 Structure of Thesis 7

2 Background **8**
2.1 Brief History 8
2.1.1 Amorphous Silicon 8
2.1.2 Porous Silicon 11
2.2 Mechanical Properties of Silicon 13
2.2.1 Structural Materials for MEMS Integration 14
2.2.2 Amorphous Silicon as a Structural Material 15
2.3 Integrated Inductors on Silicon 16
2.3.1 Modeling Parameters 17
2.3.2 Inductor Performance Metrics 24
2.3.3 Previous Work 26
2.4 Integrated Transformers on Silicon 31
2.4.1 Modeling Parameters 32
2.4.2 Transformer Performance Metrics 33

2.4.3 Previous Work 36
2.5 Summary 38

3 Development of Low Temperature Formation of Low Loss Films on Si 40
3.1 Development of Undoped Amorphous Silicon Thick Films 41
3.1.1 Film Formation 41
3.1.2 Film Characterization and Results 46
3.1.3 Summary 58
3.2 Formation of Porous Silicon Thick Films 59
3.2.1 Film Formation 59
3.2.2 Film Characterization and Results 64
3.2.3 Summary 70

4 Planar Inductors built on Low Temperature and Low Loss Films on Si 71
4.1 Design of Planar Inductors on Silicon 72
4.1.1 Basic Structure 72
4.1.2 Design Parameters 73
4.1.3 Film Thicknesses 75
4.1.4 Design Rules 79
4.2 Planar Inductors on Amorphous Silicon 79
4.2.1 Device Fabrication 79
4.2.2 Results and Discussion 81
4.3 Planar Inductors on Porous Silicon 85
4.3.1 Device Fabrication 86
4.3.2 Results and Discussion 89
4.4 Summary 92

5 Amorphous Si Thick Films for sub 150℃ MEMS Fabrication 94
5.1 Lowering a-Si:H Thick Film Deposition to 150℃ 95
5.2 Film Stress Issues of a-Si:H Thick Films as a Mechanical Material 97
5.3 Integration Issues of a-Si:H Thick Films as a Mechanical Material 100
5.3.1 Critical Role of Step Coverage of an Anchor 101

5.3.2 Optimizing the Step Coverage of a-Si:H Thick Films 102
5.4 Fabrication and Testing of a Simple MEMS Device with a-Si:H Thick Film 104
5.4.1 Simple Vertical Bimorph Thermal Actuator 104
5.5 Summary 109

6 Tunable RF MEMS Inductors and Transformers using Amorphous Si Thick Films as a Mechanical Material 111
6.1 Tunable RF MEMS Inductors 111
6.1.1 Device Design 112
6.1.2 Device Fabrication 112
6.1.3 Results and Discussion 117
6.2 Tunable RF MEMS Transformers 119
6.2.1 Device Design 120
6.2.2 Device Fabrication 121
6.2.3 Results and Discussion 121
6.3 Simulations Involving Traditional RF Materials 134
6.4 Future Outlook of post-CMOS and MEMS 136
6.5 Summary 137

7 Conclusions 138
7.1 Contributions 138
7.2 Future Work 140

Appendix A Recipes Developed in this research for MEMS Processing 142

Appendix B Calculating the Hydrogen Content in a-Si:H 147

Appendix C Extracting the Optical Bandgap of a-Si:H 149

List of Thesis Publications 151

List of Acronyms 153

References 155

List of Figures

1.1 Integrated transformer-based front-end wireless transceiver on CMOS. . . . 3
1.2 MEMS dual-band filter with contact switched inductors. 5
1.3 Integrated VCO with on-chip MEMS inductors. 5

2.1 Density of states distribution in a-Si:H. 11
2.2 Cross-section of MEMSCAP's PolyMUMPs commercial MEMS process. . . 15
2.3 Conventional compact model of a planar inductor on Si. 17
2.4 Schematic of self and mutual inductances in a coil. 18
2.5 Planar inductor layouts. 20
2.6 Effect of ground shield on Q. 27
2.7 Cross-section of a multi-metal layer inductor. 27
2.8 Effect of layout optimization on Q. 28
2.9 Bulk micromachined inductor. 29
2.10 Surface micromachined inductor. 30
2.11 Self-assembling tunable inductor. 31
2.12 3-D Inductors by plastic deformation magnetic assembly. 31
2.13 Conventional compact model of a transformer on Si. 32
2.14 Schematic symbol of a monolithic transformer. 33
2.15 Planar transformer layouts. 36
2.16 Magnetic transformers fabricated in a flip-chip process. 37
2.17 Transformers fabricated with a permalloy magnetic core. 37
2.18 Millimeter-wave inductors and transformers operating in the 30-100 GHz. . 38

3.1 Trion PECVD System in the CIRFE Lab. 42

3.2 Variation in deposition thickness with time of PECVD a-Si:H thick films. . 44
3.3 Trion RIE System in the CIRFE Lab. 45
3.4 Variation in etched thickness with time of RIE a-Si:H thick films. 46
3.5 Film uniformity of PECVD a-Si:H thick film. 47
3.6 Surface roughness of PECVD a-Si:H thick films. 48
3.7 Capacitance-voltage measurements of a-Si:H thick film. 50
3.8 CPW transmission line used to extract loss tangent of a-Si:H thick films. . 52
3.9 Insertion loss of CPW line on a-Si:H thick films with different thicknesses. 53
3.10 Structure used to measure conductivity of a dielectric film. 54
3.11 Measured dark and photoconductivity of a-Si:H thick film. 55
3.12 Infrared transmission spectrum of a-Si:H thick film. 56
3.13 UV spectrum and Tauc plot of a-Si:H thick film. 58
3.14 Porous Si formation steps. 61
3.15 Schematic of a single wafer etch cell. 65
3.16 Photograph of Teflon etch cell machined for this study. 65
3.17 SEM of PS formed with 25% HF concentration and 1 mA/cm^2 current density for 45 min. 66
3.18 PS formed with 12.5% HF concentration and 20 mA/cm^2 currenty density. 67
3.19 Border between PS formation and c-Si substrate. 67
3.20 PS formed with 12.5% HF concentration and 40 mA/cm^2 current density. . 68
3.21 PS formed from with 5 mA/cm^2 current density and varying HF concentration. 69
3.22 Photograph of electrochemical etching of c-Si with a particle defect. 70

4.1 Schematic of a planar inductor. 72
4.2 Q versus metal layer thickness. 76
4.3 Q versus dielectric layer thickness. 77
4.4 Q versus conductivity of DIEL_1 and DIEL_2 layers. 78
4.5 Process flow of planar inductors. 80
4.6 Fabricated planar inductors incorporating a-Si:H on c-Si. 82
4.7 Influence of thickness of a-Si:H layer on performance of fabricated planar inductor. 83

4.8 Influence of light-induced conductivity of a-Si:H on performance of fabricated planar inductor. 84
4.9 Comparison between modeled, simulated and measured results of a fabricated planar inductor. 85
4.10 Schematic cross-section of planar inductor incorporating PS. 86
4.11 SEM of PS pore size formed with 25% HF concentration and 1 mA/cm^2 current density for 45 min. 87
4.12 SEM of PS thickness formed with 25% HF concentration and 1 mA/cm^2 current density for 45 min. 88
4.13 Micrograph of fabricated inductor on PS and a-Si:H. 88
4.14 Measured RF performance of a fabricated inductor with PS and a-Si:H. . . 90
4.15 Measured RF performance of a fabricated inductor on PS showing the influence of applied current density. 91
4.16 Effective substrate resistivity of Si incorporating PS and a-Si:H. 91

5.1 PECVD surface deposition kinetics in a trench. 95
5.2 Schematic of an optical stress gauge. 98
5.3 Measured stress of PECVD a-Si:H thick films with varying thicknesses. . . 100
5.4 Simulated stress distribution in the anchor. 101
5.5 Simulated displacement and stress in a bimorph cantilever beam. 102
5.6 SEM cross-section of a-Si:H thick film coverage over a step of resist. 103
5.7 SEM cross-section of a-Si:H thick film coverage over extreme sidewall. . . . 104
5.8 Fabrication steps of simple bimorph cantilever beams. 107
5.9 SEM of fabricated bimorph thermal actuators incorporating a-Si:H. 108
5.10 Overlay of microscope images showing the actuated tip of a fabricated bimorph thermal actuator. 108
5.11 Measured and simulated tip deflection of a fabricated bimorph thermal actuator incorporating a-Si:H as a mechanical material. 109

6.1 Schematic indicating the direction of current flow for a single metal layer MEMS inductor. 113
6.2 Fabrication process of a RF MEMS inductor. 114

6.3 Cross-sectional schematic of tunable RF MEMS inductor. 115
6.4 Micrograph image of a fabricated RF MEMS tunable inductor. 115
6.5 SEM of a fabricated tunable RF MEMS inductor. 116
6.6 Thermomechanical simulation of a tunable RF MEMS inductor. 116
6.7 Measured inductance of a fabricated RF MEMS tunable inductor. 118
6.8 Measured Q of a fabricated RF MEMS tunable inductor. 119
6.9 Fabrication process of a tunable RF MEMS transformer. 121
6.10 Cross-section schematic of a tunable RF MEMS transformer. 122
6.11 Micrograph of a fabricated tunable RF MEMS transformer. 123
6.12 SEM of a fabricated tunable RF MEMS transformer. 123
6.13 Thermomechanical simulation of a tunable RF MEMS transformer. 124
6.14 Measured magnetic coupling of a fabricated tunable RF MEMS transformer. 125
6.15 Measured mutual inductance of a fabricated tunable RF MEMS transformer. 126
6.16 Measured and simulated S-parameters of a fabricated tunable RF MEMS transformer. 127
6.17 Comparison of measured and simulated results of a resistively heated plate transformer. 128
6.18 Schematic of resistively heated plate transformer design. 129
6.19 Fabricated resistively heated plate transformer design. 130
6.20 Comparison of measured and simulated results of a thermally actuated plate transformer. 131
6.21 Schematic of thermally actuated plate transformer design. 132
6.22 Fabricated thermally actuated plate transformer design. 133
6.23 Comparison of simulations using alumina and gold of a fabricated RF MEMS inductor. 135
6.24 Comparison of simulations using alumina for a fabricated RF MEMS transformer. 135
6.25 MEMS-based IC product market. 136

C.1 Absorbed, transmitted and reflected light in a thin film. 149

List of Tables

2.1 Comparison of mechanical properties of common materials compared to Si. 14
2.2 High temperature steps in MEMSCAP's PolyMUMPs process. 15
2.3 Comparison of thermomechanical properties of poly-Si and a-Si:H. 16
2.4 Fitting parameters for modified Wheeler formula. 20
2.5 Conductivity and skin depth of metal layers commonly used in IC processes. 21
2.6 Summary of equations and description of parameters in the compact model of a planar inductor. 24

3.1 PECVD process conditions for deposition of a-Si:H thick films at 250℃. . . 43
3.2 RIE process conditions for etching a-Si:H thick films. 46
3.3 Experimental results of stain etching of c-Si. 64
3.4 Experimental results of electrochemical etching of c-Si. 66

4.1 General trends of inductor design parameters. 74
4.2 Design rules for the fabrication of planar inductors. 79
4.3 Dimensions and measured performance of fabricated planar inductors. . . . 81
4.4 Experimental parameters for forming PS for 45 min. 87
4.5 Comparison of some planar inductors reported in literature compared to this work. 92
4.6 Comparison of some planar inductors on PS reported in literature compared to this work. 92

5.1 Variation in deposition rates for PECVD a-Si:H films. 96
5.2 PECVD process conditions for depositing a-Si:H thick films 97

6.1 Inductor compact model parameters fitted to measured results for different applied voltages of a fabricated tunable RF MEMS inductor in this work. . 118
6.2 Design rules for the fabrication of MEMS inductors and transformers in this work. 120
6.3 Transformer compact model parameters fitted to measured results for different applied voltages. 126

A.1 Amorphous Si PECVD recipe. 143
A.2 Amorphous Si RIE recipe. 143
A.3 Photolithography steps. 144
A.4 Spin-on sacrificial layer recipe. 145
A.5 Sacrificial layer RIE recipe. 146
A.6 Release process. 146

Chapter 1

Introduction

1.1 Research Motivation

A wireless radio frequency (RF) receiver must select the desired signal out of many unwanted and potentially interfering signals and then amplify it with near perfect quality. In addition to these challenges of modern day engineering, the consumer market places strict constraints on low cost, low power, and high volume production. In order to meet these requirements, an integrated system is the most promising solution.

Many technology tradeoffs exist in RF integrated circuits (ICs) for wireless communication systems. The optimum technology for RFICs may follow the same path as digital ICs - toward complementary metal-oxide-semiconductor (CMOS) integration where cost decreases as the level of integration increases [1]. However, the technical requirements for an RF transceiver are far more complex than digital ICs where, in the later case, parameters such as power dissipation, operating speed, and manufacturing yield are the main performance concerns. In the case of RFICs, in conjunction with the requirements of digital ICs, issues such as noise, linearity, gain, and efficiency must also be addressed.

Today, commercial implementations of high performance wireless transceivers use a mixture of processing technologies to implement an integrated solution. These on- and off-chip components are often mixed together to reach design specifications which can complicate packaging, increase costs, and decrease performance reliability. Due to recent research efforts, high frequency performance of devices on silicon (Si) are approaching those

achieved on gallium arsenide (GaAs), but at higher power dissipation [1]. Nonetheless, higher integration with Si technology will reduce the need for routing high frequency signals which can potentially reduce the overall power dissipation of the system as a whole.

1.1.1 Inductors and Transformers on Silicon

An inductor is a device capable of producing a voltage in response to a changing current. The changing current produces a time-varying magnetic field which induces an electromotive force (emf). A low loss inductor is the last passive element to be successfully integrated onto Si ICs. High performance on-chip inductors are in increasing demand in today's communication systems with an emphasis on RF and mixed-signal ICs, and system on chip (SoC) applications. Inductors are widely used in RF circuits, such as filters, voltage controlled-oscillators (VCO), low-noise amplifiers (LNA), and impedance matching circuitry. The key parameters used to characterize the performance of inductors are the inductance (L), the quality factor (Q) and the self-resonance frequency (f_{res}). A constant L over a broad frequency range is necessary for a reliable circuit design. A high Q improves the insertion loss of a filter and enhances the phase noise performance of a VCO, for instance. An increase in f_{res} allows the device to be operated at higher frequency. In general, the trace capacitance to ground lowers f_{res}, and the substrate conductivity lowers the Q at RF frequencies.

The conventional monolithic inductor is implemented as a metal trace on oxide over a conductive Si substrate. The Q is limited by the series resistance of the thin film metalization at low frequency and the low substrate resistivity at high frequency. Due to the driving force of CMOS integration and low costs of Si-based ICs, these inductors must lie on a conductive Si substrate which is a major source of energy loss and limits the RF performance. As a result, the Q factor of inductors fabricated on low resistivity Si is low ($Q < 10$). In matching circuits for example, the Q of the inductor is much lower than that of the capacitor and hence, dominates the overall Q of the circuit. The wide range of applications of inductors emphasizes this need for improving the performance of an inductor fabricated on low resistivity Si.

A transformer is simply two inductive coils coupled together and are also integrated into RF systems. Figure 1.1 is a wireless transceiver with an on-chip transformer integrated

on CMOS to perform matching and single-ended to differential conversion (one set of ports on the primary side and two sets on the secondary side). This front-end architecture has been used in Bluetooth products [2].

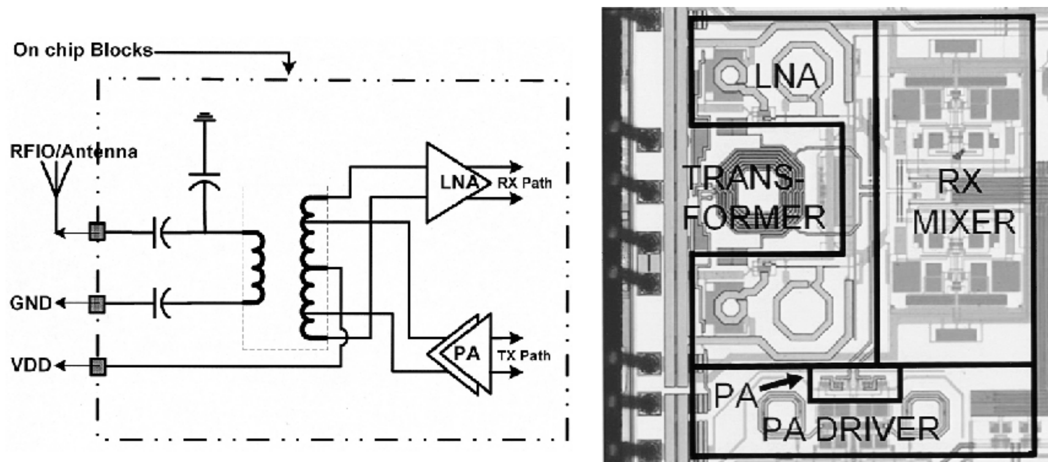


Fig. 1.1: Integrated transformer-based front-end wireless transceiver on CMOS, from [2].

1.1.2 Low Temperature and Low Loss Films

To improve the performance of inductors on Si, thick low loss films on Si with minimum stress are required. In addition, with the continued search for low-k dielectrics and metal alloys, a low thermal budget is always preferred. Plasma enhanced chemical vapor deposition (PECVD) of hydrogenated amorphous Si (a-Si:H) is an attractive choice because the substrate can remain at a low temperature. Porous Si (PS) is another low temperature material that is formed by electrochemically etching pores in the Si substrate improving the resistivity. It is a wet etching process that can take place at room temperature.

1.1.3 Low Temperature MEMS Fabrication

In the last few decades, CMOS technology has dominated microelectronics fabrication for ICs. The minimum feature size has continued to decrease with increasing integration density as predicted by semiconductor roadmaps. Microsensors and microactuators are

being integrated with on-chip CMOS circuitry exploring the opportunities of CMOS-based microelectromechanical systems (MEMS).

In pre-CMOS MEMS integration, the MEMS structures are first micromachined and must meet strict criteria in terms of issues such as contamination and planarization before being able to continue with commercially available CMOS microelectronics processing. In intermediate-CMOS MEMS integration, the CMOS process is interrupted for additional micromachining steps. This approach requires custom fabrication facilities. In post-CMOS MEMS integration, the MEMS devices are built on top of a CMOS substrate. This approach is advantageous because the CMOS wafers are fabricated at any industrial CMOS foundry where advanced technologies can be exploited for MEMS. The main limitation of post-CMOS is the stringent thermal budget for the additional micromachining steps, limiting process temperatures to 400℃ [3]. Amorphous Si is a promising candidate as a structural material for MEMS because it has similar mechanical properties similar to polysilicon but offers much lower temperature deposition suitable for post-CMOS integration.

1.1.4 Tunable RF MEMS Devices

Micromachining techniques have been applied to RF transceivers in order to overcome some limitations of traditional IC processing. For example, MEMS switches have the potential for improved isolation, insertion loss, and linearity compared to solid-state devices [1]. There has been a lot of interest in the tunablility of RF MEMS devices such as tunable filters and tunable capacitors for reconfigurable RF systems for a miniaturized on-chip solution. Tunable filters have a huge range of applications from fine tuning the center frequency of narrowband filters, or selecting a different frequency band in a broadband implementation. Examples of the integration of reconfigurable RF MEMS on-chip can be found in literature. Figure 1.2 shows a tunable filter tuned with a MEMS contact switch to select one of two inductors to change the center frequency of a dual-band filter. Figure 1.3 presents a fully integrated VCO with MEMS inductors. The MEMS inductors are made of thick electroplated metal for improved high performance and are built on top of CMOS active circuits for an integrated solution.

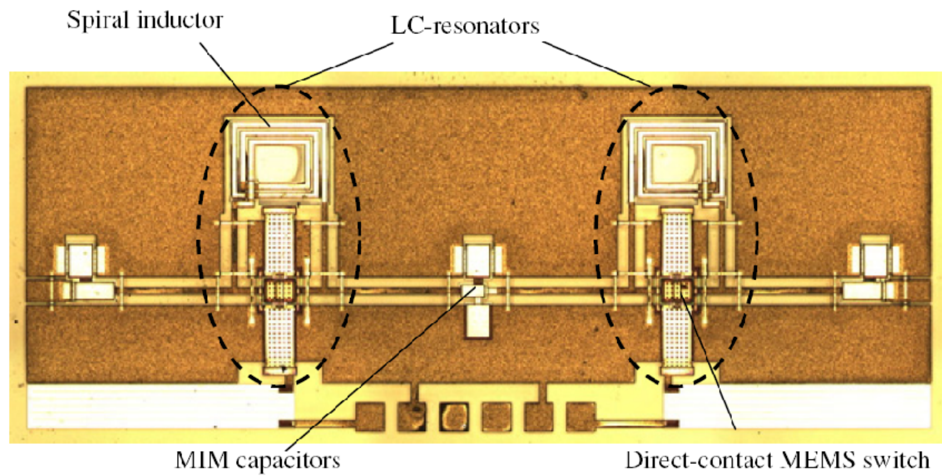


Fig. 1.2: Micrograph of a MEMS dual-band filter with contact switched inductors, from [4].

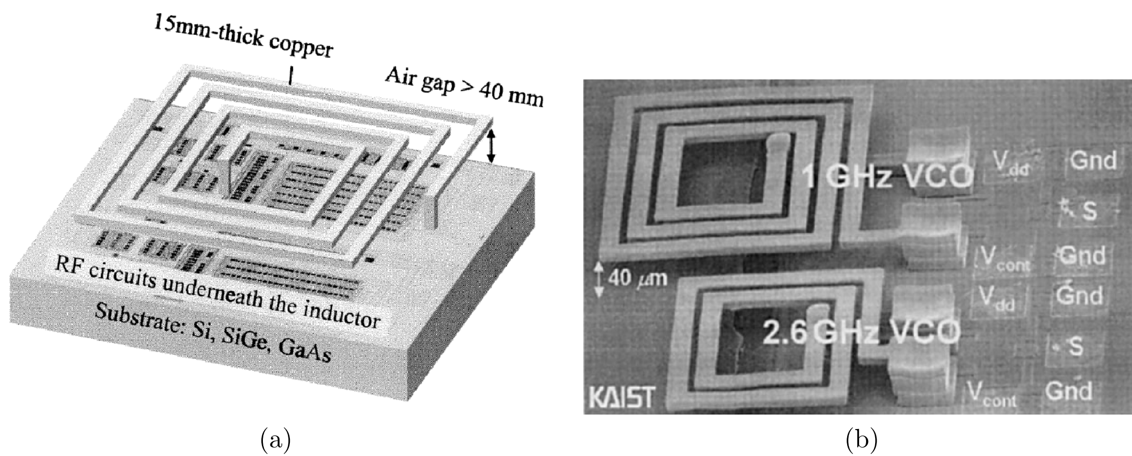


Fig. 1.3: (a) Schematic and (b) SEM image of an integrated VCO with MEMS inductors, from [5].

Tunable inductors also show great promise - these devices can be implemented in filters, matching networks of LNAs and tank circuits of VCOs. Tunable inductors could also improve the reliability of a system by overcoming the tolerances introduced by manufacturing limitations. Furthermore, tunable transformers can improve the performance of an RF system by improving the Q of an inductor topology by increasing the coupling, for instance.

1.2 Research Objectives

The purpose of this thesis is to explore new materials for the fabrication of low temperature RF MEMS devices. These materials are applied to the design and fabrication of planar inductors and RF MEMS tunable inductors and transformers. This research topic is divided into four main steps:

(i) **Process development and characterization of low temperature and low loss materials:** Undoped amorphous Si and porous silicon are investigated as candidate thin films for improving the effective silicon substrate resistivity. Amorphous silicon films can be deposited by plasma enhanced chemical vapor deposition allowing the substrate to remain at a low temperature and porous Si can be electrochemically formed at room temperature.

(ii) **Planar inductors built on Si incorporating novel films:** Two processes are explored for the fabrication of planar inductors on Si in a two metal sub 250℃ layer process. The first device incorporates thick undoped amorphous Si films in a novel application functioning as an isolation layer for building planar inductors. The second device has an additional porous Si layer with amorphous Si serving as an encapsulating material and then planar inductors are fabricated. The RF performance of the two devices are compared for the same device layout.

(iii) **Application of amorphous Si as a structural material for low temperature MEMS fabrication:** Amorphous Si is deposited at 150℃ and critical reliability issues in MEMS are examined. The mechanical stress is measured and the sidewall coverage of 3-D structures are discussed.

(iv) **Design and fabrication of tunable RF MEMS inductors and transformers:** Low temperature amorphous Si is applied to RF MEMS devices. A bimorph structural layer incorporating amorphous Si and aluminum is formed to create 3-D coils achieving several hundred microns of vertical displacement due to the developed stress in the two materials. These devices can be tuned by applying a voltage across the terminals. Fabricated devices are compared to thermomechanical simulations.

1.3 Structure of Thesis

Background information of the research carried out in this thesis is addressed in Chapter 2. This includes a brief history of two low temperature candidate films investigated in this work, amorphous Si and porous Si, and the compact model of an inductor and a transformer is presented. Previous work in these areas is also summarized. In Chapter 3, the characterization of PECVD amorphous Si and electrochemically etched porous Si prepared in our lab is presented. Planar inductors are fabricated on both these films and the results and discussion are included in Chapter 4. In Chapter 5, amorphous Si is studied for its potential as a structural material for low temperature MEMS fabrication. Chapter 6 applies the amorphous Si films to RF MEMS devices. Tunable RF MEMS inductors and transformers incorporating amorphous Si in a bimorph structure are designed, fabricated, and tested. The measured results are compared with thermomechanical simulations. Chapter 7 summarizes the research contributions of this thesis and future work related to this topic is proposed.

Chapter 2

Background

This chapter provides a background overview of the topics covered in this thesis. An introduction to amorphous silicon and porous silicon films is given and some applications are introduced. The physical model of a planar inductor which forms the basis of the devices presented in this research is explained. This model is also used to understand the losses in transformers which are simply two inductor coils coupled together. The figures of merit for both inductors and transformers are provided and are used to evaluate the performance of the devices fabricated in this research. In addition, a survey of inductors and transformers fabricated on Si by conventional IC processing and MEMS micromachining techniques is summarized.

2.1 Brief History

2.1.1 Amorphous Silicon

Non-crystalline semiconductors are classified as materials with no long-range order. Long-range order only exists in crystalline silicon (c-Si) where a crystal of any size can be represented by repeatable unit cells. Non-crystalline silicon materials are categorized as polysilicon (poly-Si), nanocrystalline silicon (nc-Si), microcrystalline silicon (μc-Si), and hydrogenated amorphous silicon (a-Si:H). Polysilicon is composed of randomly oriented crystals separated by grain boundaries with long-range order only limited within the crystal

grains. Nanocrystalline Si and microcrystalline Si materials contain randomly oriented crystals embedded in an amorphous network. The crystallinity of nc-Si and μc-Si is defined as the ratio of the crystal phase to the crystal and amorphous phases. In a-Si:H films, only short-range order exists meaning that the neighboring atoms have essentially the same bond length and bond angle as c-Si, however approximately three atomic distances from a given atom, the lengths and angles deviate by $\pm 10\%$.

The electronic properties of c-Si are superior to those of non-crystalline counterparts which have high defect density resulting in low carrier mobility. However, there are other advantages of non-crystalline technology which are attractive:

(i) **Large-area deposition:** The maximum area of c-Si is limited by the diameter of the ingot, but a-Si:H has been explored for roll-to-roll technology (similar to newspaper printing). This can result in lower manufacturing costs for industry-scale processing.

(ii) **Low temperature deposition:** In c-Si technology, the processing temperature is limited by the melting point of Si (1413℃), but non-crystalline materials can be deposited by physical and chemical vapor deposition techniques which offer much lower deposition temperatures. Temperatures are being reduced to below 100℃ to expand substrate possibilities.

(iii) **Good optoelectronic properties:** In the visible range, the absorption length of a-Si:H thin films is much shorter than c-Si which creates many opportunities in the area of optical sensors and solar cells.

Amorphous Si was first deposited by sputtering and thermal evaporation in the 1950s when it was found to have a high defect density which prevented it from being a useful semiconductor. In 1969, Chitick deposited hydrogenated amorphous silicon by glow discharge of silane (SiH_4) where properties such as lower defect density, increased conduction, and metastability were observed, but the significance of the research was overlooked. In 1975, Spear and LeComber successfully carried out substitutional doping by adding phosphine or diborane to the deposition gas and reported an improvement in conductivity by a factor of 10^8 [6]. In 1977, Fritzche discovered the crucial role hydrogen plays in achieving low defect density of a-Si:H and that hydrogen is present in the glow discharge of SiH_4. Following these discoveries, the interest in a-Si:H material took off.

The material properties of a-Si:H are strongly dependent on deposition conditions. Amorphous Si can be deposited by chemical vapor deposition (CVD) or sputtering. Thermal CVD requires high substrate temperature, so this method has limited applications. Hot-wire CVD (HWCVD) is a technique where the decomposition of the gas molecules occur at a metal wire heated to $\sim$2000℃. This allows the substrate (located a certain distance from the hot-wire) to remain at room temperature; however, film uniformity is often an issue. In a PECVD process, the energy for the dissociation of the gases is provided by the RF plasma generated between an electrode and the substrate. This deposition method allows the substrate to remain at low temperature (100-350℃). PECVD is the preferred method for large area electronics due to low substrate temperature, film uniformity, and good adhesion to the substrate [6]. Growth of a-Si by sputtering is due to the ion bombardment of a solid Si target. However, sputtered a-Si with argon is unhydrogenated, so the material will typically have poor electronic transport properties. Sputtering can take place in the presence of hydrogen, however sputtered films may suffer from severe ion bombardment damage due to the high energy of ions reaching the surface of the film.

The bandgap of a semiconductor strongly influences the electrical and optical properties of the material. However, there has been much debate over whether a bandgap exists in a-Si:H. It has been accepted that the bandgap of a material is influenced by the short range order, which is comparable for amorphous and crystalline material. So the abrupt band edges of the extended states typical of crystalline material are replaced with broadened tail states or localized states [6]. These band tail states are due to the variation in bond lengths and bond angles in the amorphous network. The band tails play a crucial role in electronic transport which occurs near the edges of the bandgap. In addition, deep states in the midgap exist due to broken bonds. These defect states serve as trapping centers which influence many material properties such as metastability in a-Si:H. Figure 2.1 is the Mott-Davis-Street model of the density of states in amorphous semiconductors and has been well accepted as it serves to explain many material properties.

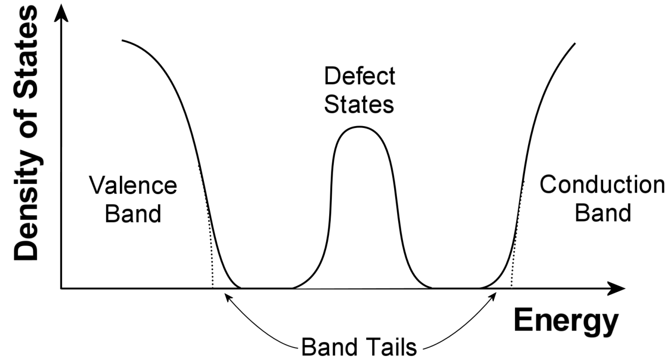


Fig. 2.1: Mott-Davis-Street density of states distribution model of a-Si:H.

2.1.1.1 Applications of Amorphous Silicon Thin Films

Amorphous Si can be deposited over large area with good uniformity and caters to the needs of large area electronics. It is also compatible with Si-based fabrication processes and can be easily integrated with low capital costs. Due to the low temperature deposition it is being explored for organic light emitting diode (OLED) displays [7, 8] and it is a promising material for low cost solar cells [9,10]. Amorphous Si has also received attention in biomedical applications such as X-ray imaging [11,12], detectors for genetic analysis [13], and electronic portal imaging devices (EPIDs) for portal dosimetry [14].

2.1.2 Porous Silicon

Porous Si is another semiconductor that can display high resistivity and is defined as a material with a large surface to volume ratio. The electrochemistry of silicon exhibits unusual behavior, many of which are still not well understood today. In the early days of Si manufacturing, the need for a surface with low defect density led to developing chemical polishing solutions. Porous Si was accidentally discovered by Uhlir in the mid 1950s when performing electropolishing experiments on Si wafers in a hydrofluoric (HF) electrolyte [15]. Uhlir discovered that under certain conditions of applied current density and electrolyte composition, the Si did not dissolve uniformly, but instead holes were formed which propagated primarily in the <100> direction of the bulk Si wafer. The

results were curious, but the layer was non-uniform and the material was ignored. In the late 1980s, Canham's experiments revealed that electrochemically etched Si produces a strong orange-red photoluminescence when subjected to ultraviolet (UV) light [16]. With the discovery of light emission of PS, applications in the area of optoelectronic switches, displays, and lasers were explored. However, issues with the material's chemical and mechanical instability and low electroluminescence efficiency led to fading interest. Though the unique features of PS, the formation of large thicknesses, variable pore sizes, and compatibility with conventional Si-based technologies; inspired research into applications outside the area of optoelectronics, such as biomedical and sensor applications. There is a growing interest in PS as new applications are being discovered and more research effort is being invested into modeling electrochemical pore formation.

Porous Si pore dimensions can range from 1 nm to 10 μm and morphologies can range from sponge-like to perfect cylindrical pores. The key variables that can be controlled during the formation of PS include: electrolyte type, HF concentration, applied current density, doping type and level of the c-Si, and front/back-side illumination. There are three main types of electrolytes: aqueous, organic, and oxidizing electrolytes. The different composition of these electrolytes result in different dissolution peaks observed in the current-voltage characteristics of the applied current density [17]. Porous Si can also be formed by pure chemical etching in a hydrofluoric and nitric acid solution, but may result in inhomogeneous porosity and thickness [18].

The exact dissolution of Si is unclear and different mechanisms have been proposed. The variation in the proposed models is the mechanism behind the difference in dissolution rate between the pore tips and the pore walls which form the pores. It is agreed that holes are required for pore formation, therefore, n- and p-type Si pore formation mechanisms are different. Illumination of n-type substrates is required to generate enough minority carriers for the dissolution of Si and back- and front-side illumination to produce different surface morphologies.

Other porous materials can also be formed. Silicon carbide [19] and silicon germanium [20] behave similarly to Si when electrochemically etched. These materials are also being studied for Si-based optoelectronics.

2.1.2.1 Applications of Porous Silicon

Advantages of PS layers include large aspect ratios, uniformly defined arrays, and compatibility with Si-based technology. Macropore arrays are applied to bio-chips where a matrix of tiny test tubes is coated with a biochemical substance that reacts only with specific molecules or DNA sequences [17]. Another area of interest is that highly porous Si can biodegrade in the human body and is non-toxic opening up many opportunities for implantable medical devices [21]. Microporous Si has been used for "artificial nose" or gas sensor applications based on the change in resistivity of PS as different molecules are absorbed [22]. Another type of sensor is a chemical sensor as a safety tool for HF detection in an unknown liquid. The current-voltage curve of a Si electrode in HF can be sensed which is useful as HF is a major health hazard in semiconductor manufacturing [23]. The first application of exploiting the visible photoluminescence (PL) from PS was for the fabrication of electroluminescent (EL) solid-state devices. The quantum efficiency of of the EL from PS is about 1% which is still one order of magnitude smaller than that of state-of-the-art light-emitting diodes based on III-IV semiconductors [24] and the long-term stability of devices based on PS films is generally poor. However, considerable advances have been made in the last decade, but more are still needed to meet specifications. In the area of MEMS, PS has been used as a sacrificial layer where good formation selectivity can be formed in differently doped areas or a masking layer can be used [25]. Porous Si can also be used as a layer or trench for isolating the low resistivity Si substrate and/or neighboring devices for system integration. Interest in this material as a low cost Si substrate for microwave circuits stems from its properties such as high resistivity in the MΩ cm regime and lower dielectric constant than Si [26].

2.2 Mechanical Properties of Silicon

Silicon displays some amazing mechanical properties as listed in Table 2.1. The Young's modulus of Si approaches that of steel, the Knoop hardness is close to quartz, and the yield strength is three times higher than steel [27]. Despite this quantitative evidence, Si wafers tend to break and chip with excessive handling which contribute to the common misconception that Si is a mechanically fragile material. But Si wafers are large and

relatively thin, and even stainless steel at wafer dimensions could deform [27]. In addition, due to the crystallographic network of Si, it has a tendency to break along crystal planes.

Table 2.1: Comparison of mechanical properties found in literature of common materials compared to Si [27].

Material	Yield Strength (GPa)	Knoop Hardness (kg/mm^2)	Young's Modulus (GPa)	Density (g/cm^3)	Thermal conductivity (W/cm ℃)	Thermal expansion coefficient (10^{-6}/℃)
Si_3N_4	140	3490	385	3.1	0.19	0.8
SiO_2	84	820	73	2.5	0.0014	0.55
Al	1.7	130	70	2.7	2.36	25
Steel	21	660	200	7.9	0.329	17.3
Si	**70**	**850**	**190**	**2.3**	**1.57**	**2.33**

2.2.1 Structural Materials for MEMS Integration

Polysilicon deposited by low pressure chemical vapor deposition (LPCVD) is one of the most widely used structural materials in MEMS [28]. However, LPCVD films deposited below a critical temperature of 550℃ require high temperature annealing (∼1000℃) to form poly-Si [28]. In addition, poly-Si films are known to exhibit high compressive stress which may require further annealing [29].

PolyMUMPs (multi-user MEMS process) is the industry's longest-running MEMS foundry [30]. It is a three-layer poly-Si surface and bulk micromachining process with two sacrificial layers and one metal layer in an eight mask process (Fig. 2.2). There are several high temperature thermal treatments required in this process as listed in Table 2.2. The polysilicon layers are deposited by LPCVD at 580℃ and require high temperature annealing at 1050℃ for one hour in order to achieve low stress films.

Poly-Ge and poly-SiGe are other promising low temperature structural materials that have been investigated. For example, films deposited by PECVD at 520℃ with high deposition rates and low stress have been reported [31]. On the other hand, LPCVD films deposited at 450℃ resulted in low stress, but had a low deposition rate [32]. These processing temperatures are on the borderline of post-CMOS integration.

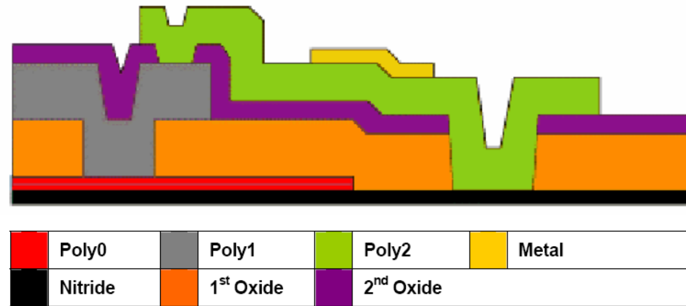


Fig. 2.2: Cross-section of MEMSCAP's PolyMUMPs commercial MEMS process, from [30].

Table 2.2: High temperature steps in MEMSCAP's PolyMUMPs process [30].

Step	Temperature	Description
1st Oxide and 2nd Oxide anneal	1050℃	1 hr thermal treatment
Poly0, Poly1 and Poly2 deposition	580℃	LPCVD deposition
Poly1 and Poly2 anneal	1050℃	1 hr thermal treatment

2.2.2 Amorphous Silicon as a Structural Material

Based on the mechanical properties of Si listed in Table 2.1 and since poly-Si is deposited at temperatures above 550℃, there is an interest in employing a-Si:H as a low temperature material for MEMS fabrication. However, only a limited amount of literature has been published on the mechanical properties of a-Si:H [33–35]. Within the last few years, an interest in a-Si:H for MEMS and RF applications has surfaced. Smooth a-Si:H films were used as the sacrificial layer in a surface micromachining process to fabricate MEMS switches and tunable capacitors [36]. Amorphous Si deposited by hot-wire CVD was studied for electrostatic microresonators and demonstrated performance comparable to poly-Si resonators [37]. Ion implantation and deposition of thin film a-Si:H on high-resistivity Si substrates to reduce charge trapping at the SiO_2/Si interface improved the RF performance of transmission lines [38]. In the area of microelectronics, stress and strain of a-Si:H thin films has been studied for the application of thin film transistors (TFTs) on flexible substrates to determine the change in electronic properties with mechanical bending of the substrate [39].

Table 2.3 summarizes the mechanical properties of a-Si:H that have been reported in literature in comparison to poly-Si. The density, Young's modulus, and Poisson's ratio of a-Si:H are close to reported values of poly-Si. The thermal conductivity of a-Si:H is smaller than that of poly-Si due to hydrogen incorporated in the network [34], but these properties are strongly dependent on deposition conditions. For simple MEMS devices like cantilever beams, the difference in Young's modulus can be easily compensated for by changing the physical dimensions of the structure [35]. Most importantly, the deposition temperature of a-Si:H is significantly lower than that of as-deposited poly-Si or the recrystallization temperature of a-Si:H. As mentioned, the commercially available PolyMUMPs process deposits poly-Si at 580℃ by LPCVD and then the films are annealed at 1050℃ for an hour to lower the stress (Table 2.2).

Table 2.3: Comparison of thermomechanical properties found in literature of poly-Si and a-Si:H thin films [33, 40, 41].

Material	**Density** (g/cm^3)	**Young's modulus (GPa)**	**Poisson's ratio**	**Thermal expansion coefficient** ($10^{-6}/K$)	**Thermal conductivity (W/m K)**	**Processing temperature** (℃)
poly-Si	2.33	151±6	0.25	2.3	15	550-650
a-Si:H	2.30	124±5	0.22	4.4	5	200-300

2.3 Integrated Inductors on Silicon

Figure 2.3 is the standard lumped model of a planar inductor on a Si substrate. This model is only useful over a limited frequency range; however, it is a good starting point for understanding the losses associated with inductors on Si.

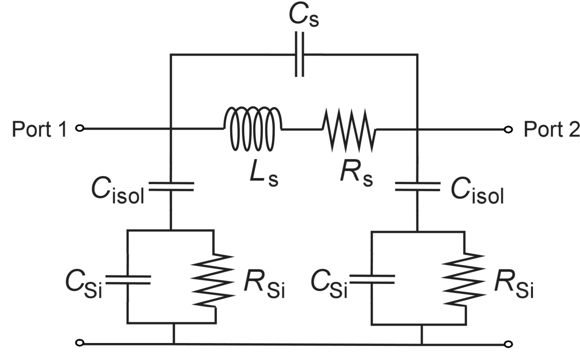


Fig. 2.3: Conventional compact model of a planar inductor taking into account the parasitic losses in the metal, isolation layer, and Si substrate.

2.3.1 Modeling Parameters

Since the purpose of an inductor is to store magnetic energy, the resistance and capacitance in a non-ideal inductor are counter-productive, and thus are considered parasitics. The parasitic resistance dissipates energy through ohmic losses, and the parasitic capacitances stores electric energy. In this section, the physical origin of all the parameters identified in the compact model will be explained and equations will be provided.

2.3.1.1 Series Inductance

The simplest equation relating inductance to device dimensions is expressed as:

$$L_s = n^2 \mu \frac{wt}{\ell} \tag{2.1}$$

where n is the number of turns, w, t, and ℓ are the width, thickness, and length of the conductor, and μ is the permeability of the metal. This equation is limited because the overall inductance is composed of the self inductance and the mutual inductance of pairs of wires. A comprehensive collection of equations and tables for inductance calculations was summarized by Grover [42].

Greenhouse developed an algorithm for calculating the inductance of a planar rectangular spiral inductor that expanded from Grover's method [43]. The Greenhouse method

states that the general equation for the inductance of a coil of any shape is the sum of [43]:

$$L_T = L_0 + M_+ - M_- \tag{2.2}$$

where L_T is the total inductance, L_0 is the sum of self inductances of all straight segments, M_+ and M_- are the sum of positive and negative mutual inductances between all segments. Mutual inductance is positive when the direction of current in two parallel wires is in the same direction and negative when the current is in the opposite direction. Two wires which are orthogonal to each other have no mutual coupling since their magnetic fluxes are not linked. For modeling purposes, rectangular coils are divided into linear segments, and the self inductance of the individual segments and the mutual inductance of pairs of segments are calculated. A schematic explanation of the self and mutual inductances is shown in Fig. 2.4 where the arrows correspond to the direction of current flow.

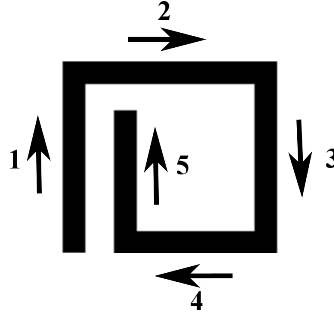


Fig. 2.4: Schematic of current flow in a coil to illustrate self and mutual inductances.

The total inductance can be calculated by:

$$L_T = L_1 + L_2 + L_3 + L_4 + L_5 + 2M_{1,5} - 2\left(M_{1,3} + M_{2,4} + M_{3,5}\right) \tag{2.3}$$

where L_i is the self inductance of segment i and $M_{i,j}$ is the mutual inductance between segments i and j. The DC self inductance of a wire with a rectangular cross-section is given by [44]:

$$L_{self} = 2\ell\left[ln\left(\frac{2\ell}{w+t}\right) + \frac{1}{2} + \frac{w+t}{3\ell}\right] \tag{2.4}$$

In general, wires with a smaller cross-section have a slightly larger inductance due to the increased magnetic flux generated external to the wire [44].

The mutual inductance between two parallel conductors is a function of the length of the conductors and the geometric mean distance (GMD) between them [43]:

$$M = 2\ell D \tag{2.5}$$

where M is the mutual inductance and D is the mutual inductance parameter calculated from [43]:

$$D = ln\left(\frac{\ell}{GMD} + \sqrt{1 + \frac{\ell^2}{GMD^2}} - \sqrt{1 - \frac{GMD^2}{\ell^2}} + \frac{GMD}{\ell}\right) \tag{2.6}$$

where GMD is approximately equal to the distance, d, between the centers of the conductors. The exact value of GMD is calculated as the distance between two infinitely thin imaginary filaments whose mutual inductance is equal to the mutual inductance between the two original conductors [43]:

$$ln\left(GMD\right) = ln\left(d\right) - \left[\frac{1}{12\left(d/w\right)^2} + \frac{1}{60\left(d/w\right)^4} + \frac{1}{168\left(d/w\right)^6} + \ldots\right] \tag{2.7}$$

Inductors can be designed in various layouts as shown in Fig. 2.5. Based on the inductor shape, another popular expression for the low frequency inductance of planar spiral inductors is the modified Wheeler formula [45]:

$$L_{MW} = \frac{K_1 \mu_0 n^2 d_{avg}}{1 + K_2 \rho} \tag{2.8}$$

where $d_{avg} = \frac{1}{2}\left(d_{out} + d_{in}\right)$ as labeled in Fig. 2.5, $\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}}$ which is defined as the fill ratio, and K_1 and K_2 are fitting parameters found in Table 2.4.

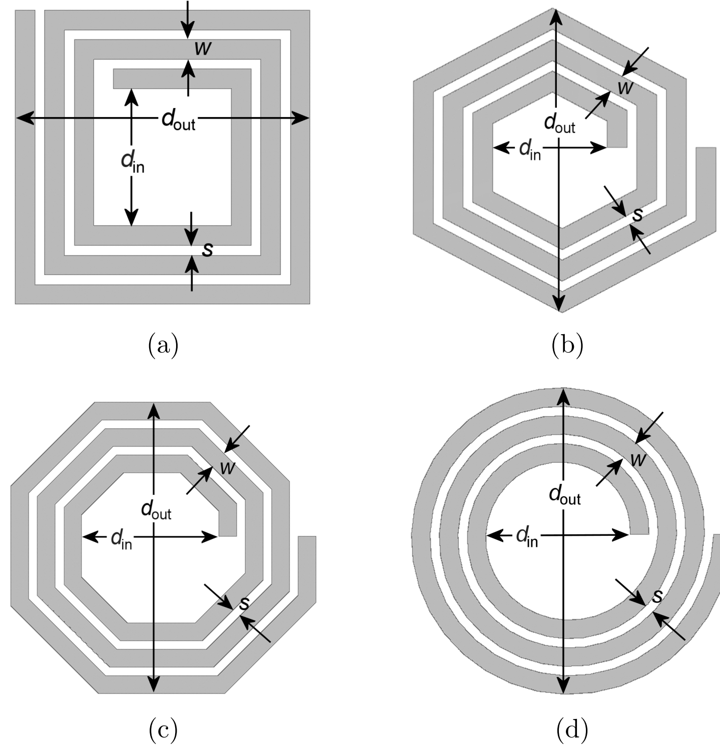


Fig. 2.5: Planar inductor layouts (a) square, (b) hexagonal, (c) octagonal, and (d) circular.

Table 2.4: Fitting parameters for modified Wheeler formula [45].

Layout	K_1	K_2
square	2.34	2.75
hexagonal	2.33	3.82
octagonal	2.25	3.55

2.3.1.2 Series Resistance

The most important parameter for improving the low frequency performance of an inductor is the series resistance (R_s). This parameter models the losses due to the finite conductivity of thin film metalization which gives rise to energy losses through heat. Alternating magnetic fields penetrate the conductor and create opposing electric fields and hence, increase the resistivity of the conductors in the inner cross-sectional area. Therefore,

current tends to travel in the outer layer of the conductors and the current distribution becomes non-uniform as frequency is increased. The adverse effects of the induced eddy currents are categorized as skin and proximity effects. In the skin effect, the time-varying magnetic field induces eddy currents in the conductor itself. In the proximity effect, the time-varying fields produced by neighboring conductors influence the main conductor. Regardless of the induced mechanism or combination of mechanisms, eddy currents increase the AC resistance and therefore, reduce the net current flow in the conductor.

The distribution of eddy currents depends on the geometry and orientation of the conductor with respect to the impinging time-varying magnetic field. The critical parameter that influences eddy currents is the skin depth:

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{2.9}$$

where ρ is the resistivity of the conductor, μ is the permeability, and f is the operating frequency. The skin depth is also known as the depth of penetration since it describes the distance incident electric current and magnetic flux penetrate the surface of the conductor. The severity of the eddy current effect is determined by the ratio of the skin depth to the conductor thickness. Eddy currents are negligible only if the skin depth is much greater than the conductor thickness such that negligible energy escapes. Table 2.5 lists the conductivity and skin depth at 2 and 10 GHz of metals commonly used in IC processes.

Table 2.5: Conductivity and skin depth of metal layers commonly used in IC processes [46].

Metal	**Conductivity (S/m)**	**Skin Depth at 2 GHz (μm)**	**Skin Depth at 10 GHz (μm)**
Al	3.72×10^7	1.84	0.824
Au	4.55×10^7	1.51	0.675
Cu	5.80×10^7	1.48	0.660
Ag	6.30×10^7	1.42	0.634

The linear segments of an inductor can be treated as microstrip transmission lines. In this case, the high frequency current moves toward the bottom surface of the wire. Therefore the current density, J, is attenuated away from the bottom surface as a function of distance, x, and is represented by [44]:

$$J(x) = J_0 \exp(-x/\delta) \tag{2.10}$$

The current is calculated by integrating the current density of the cross-sectional area of the wire, A [44]:

$$I = \int J \; dA = \int_0^t J_0 \exp(-x/\delta) w \; dx = J_0 w \delta \left[1 - \exp(-t/\delta)\right] \tag{2.11}$$

The series resistance of an inductor is calculated by [44]:

$$R_s = \frac{\rho \ell}{w\delta \left[1 - \exp(-t/\delta)\right]} = \frac{\rho \ell}{w t_{eff}} \tag{2.12}$$

where ρ is the resistivity of the wire, ℓ is the total length of all segments, and t_{eff} is the effective thickness due to the skin effect. At low frequency, R_s is approximated as the DC resistance of the inductor.

2.3.1.3 Series Capacitance

The series capacitance (C_s) models the parasitic coupling between the input and output ports which create paths for current to flow without passing through the spiral inductor. This capacitance is attributed to the crosstalk between adjacent turns, and the overlap between the coil and the underpass. However, since the adjacent turns are almost at the same potential, the effect of crosstalk capacitance is often neglected [44]. The capacitance between the spiral and the underpass is more significant due to the potential drop between the ports. Therefore, it is sufficient to model the series capacitance as the sum of all overlap capacitances [44]:

$$C_s = \frac{n w^2 \epsilon_{ox}}{t_{oxM_1-M_2}} \tag{2.13}$$

where n is the number of overlaps, w is the width of the spiral line, and $t_{ox_{M1-M2}}$ is the thickness of the dielectric between the spiral and the underpass.

2.3.1.4 Substrate Parasitics

The conductive nature of Si produces losses and limits the operating frequency of inductors. The Si substrate resistivity can vary from 10 KΩ cm (lightly doped) to 0.001 Ω cm (heavily doped) [44]. There are two main sources of losses that occur in the substrate:

(i) current caused by coupling of the electric energy to the substrate; and

(ii) currents due to time-varying magnetic fields that penetrate the substrate which produce electric fields.

In general, a metal-oxide-semiconductor (MOS) device can be modeled by a three-element network: the oxide capacitance between the spiral and the substrate (C_{ox}), the resistance of the Si substrate (R_{Si}), and the capacitance of the substrate (C_{Si}) [44]. The electric energy capacitance effect is represented by C_{Si}. The majority carrier concentration of Si determines the conductivity which is modeled by R_{Si}. Since the lateral dimensions of spiral inductors are comparable to the thickness of the Si substrate (and much larger than the thickness of the oxide), C_{Si} and R_{Si} are proportional to the area occupied by the inductor and the parameters are given by [44]:

$$C_{ox} = \frac{\ell w \epsilon_{ox}}{2t_{ox}} \tag{2.14}$$

$$C_{Si} = \frac{\ell w C_{sub}}{2} \tag{2.15}$$

$$R_{Si} = \frac{2}{\ell w G_{sub}} \tag{2.16}$$

where C_{sub} and G_{sub} are the capacitance and conductance per unit area of the Si substrate, ϵ_{ox} is the dielectric constant, and t_{ox} is the thickness of the oxide. Note, the area of the inductor is approximated by $\ell \times w$. The factor of two in the above equations is due to the assumed even distribution of losses at the input and output ports (Fig. 2.3). C_{sub} and G_{sub} are constants that depend on the substrate doping and are usually used as fitting parameters.

Table 2.6 summarizes the equations for the various parameters in the lumped physical model of a spiral inductor on silicon.

Table 2.6: Summary of equations and description of parameters in the compact model of a planar inductor on Si.

Equation	Effect
L_s	Mutual inductive coupling
$C_s = \frac{nw^2\epsilon_{ox}}{t_{oxM_1-M_2}}$	Feed through capacitance between spiral and underpass
$R_s = \frac{\rho\ell}{w\delta[1-\exp(-t/\delta)]}$	Skin effect of metal
$C_{ox} = \frac{\ell w\epsilon_{ox}}{2t_{ox}}$	Oxide capacitance between spiral and silicon substrate
$C_{Si} = \frac{\ell w C_{sub}}{2}$	Silicon substrate capacitance
$R_{Si} = \frac{2}{\ell w G_{sub}}$	Silicon substrate ohmic losses by capacitive coupling

2.3.2 Inductor Performance Metrics

The principal figure of merit of an inductor is the quality factor. The Q of a passive device is defined as:

$$Q = 2\pi \frac{\text{energy stored}}{\text{energy loss in one oscillation cycle}} \tag{2.17}$$

The self-resonance frequency, f_{res}, is a measure of the operating range of the device and occurs at the frequency the inductance is in resonance with its parasitic capacitances. Above f_{res}, the parasitic capacitances dominate, so the inductor must be operated below f_{res}.

Calculating the values of L, Q, and f_{res} are critical to a good design. Unfortunately, there are no straight-forward and accurate equations that can be used to calculate these parameters so often simulation software is used. Electromagnetic (EM) simulations are time consuming; however, lumped element approaches use first order approximations and lack accuracy. Nonetheless, the compact model introduced in this section is a good starting point for the design of planar inductors on Si.

In microwave circuits, inductors are commonly used well below f_{res}. In this case, the Q factor is defined as Q_{eff}, which is the ratio of the imaginary part to the real part of the one-port input impedance with the other port grounded [47]:

$$\begin{aligned} Q &= \frac{\omega L_s}{R_s} \frac{R_p}{R_p + \left[\left(\frac{\omega L_s}{R_s} \right)^2 + 1 \right]} \left[1 - \frac{R_s^2 \left(C_s + C_p \right)}{L_s} - \omega^2 L_s \left(C_s + C_p \right) \right] \\ &= \frac{\omega L_s}{R_s} \times \text{substrate losses} \times \text{self-resonance losses} \end{aligned} \tag{2.18}$$

where R_p and C_p are the combined parallel impedance of C_{ox}, C_{Si} and R_{Si} and are derived as:

$$R_p = \frac{1}{\omega^2 C_{ox}^2 R_{Si}} + \frac{R_{Si} \left(C_{ox} + C_{Si} \right)^2}{C_{ox}^2} \tag{2.19}$$

$$C_p = C_{ox} \frac{1 + \omega^2 \left(C_{ox} + C_{Si} \right) C_{Si} R_{Si}^2}{1 + \omega^2 \left(C_{ox} + C_{Si} \right)^2 R_{Si}^2} \tag{2.20}$$

The first factor in Eqn. (2.18) is the intrinsic Q of the inductor, the substrate loss factor models the semiconducting Si substrate, and the self-resonance factor accounts for the losses due to the parasitic capacitances. The substrate loss factor approaches 1 as R_p approaches infinity, which occurs when R_{Si} approaches 0 or infinity (Si substrate is a short or open). A patterned ground shield, which is discussed in the next section, can act as a short.

The L and Q are defined by the inductor's input impedance and can be extracted from measured S-parameter by converting to equivalent Z-parameters:

$$L = \frac{Im \left(Z_{11} \right)}{2\pi f} \tag{2.21}$$

$$Q = \frac{Im \left(Z_{11} \right)}{Re \left(Z_{11} \right)} \tag{2.22}$$

2.3.3 Previous Work

Although Si substrates are lossy, they facilitate integration with CMOS processes and are ideal for SoC applications. The issue with building inductors on Si is the significant amount of induced magnetic fields that can penetrate and generate eddy currents in the substrate that opposes the useful magnetic field generated by the inductor itself. Inductors on high resistivity Si [48], quartz [49], and sapphire [50] substrates have been explored and demonstrated high Q, but these materials are expensive or not common in CMOS processes. The literature search presented in this section is restricted to inductors fabricated on low resistivity Si substrates. MEMS Inductors fabricated by employing micromachining techniques are also summarized.

2.3.3.1 Conventional RFIC Inductors

Typically, planar inductors consist of two metal layers: the first metal is the underpass to access the inner turn, and the top metal is the inductor coil. Various techniques to improve the Q of planar inductors using standard processes are discussed in this section.

Patterned Ground Plane

To reduce substrate losses, a conductive shield was introduced between the inductor and the substrate to achieve a shielding effect. Yue patterned a metal ground shield with slots oriented perpendicular to the direction of current in the spiral which act as open circuits to impede the path of the induced eddy currents [51]. This scheme demonstrated an improvement in Q from 5.1 to 6.8 at 2 GHz compared to an inductor with a non-patterned ground shield (Fig. 2.6). However, this technique increases the parasitic capacitance to the substrate which reduces f_{res}.

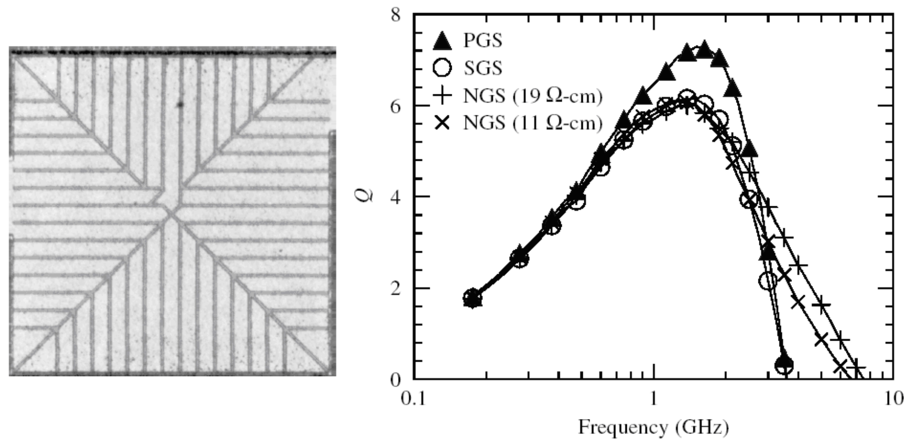


Fig. 2.6: Effect of ground shields on Q (PGS = patterned ground shield, SGS = standard ground shield, NGS = unshielded ground shield), from [51].

Multi-Metal Layers

It can be seen from the equations provided that reducing R_s increases Q. However, due to area constraints, wider tracks are not always feasible and limit miniaturization. In addition, parasitic capacitance is increased, which limits the frequency response. Therefore, the conductance of traces was increased by joining adjacent metal layers using multiple vias to create thicker metal lines. Soyuer showed that by using the metalization scheme outlined in Fig. 2.7, the Q factor was improved from 7.2 to 9.3 at 2.4 GHz for a 2 nH inductor [52].

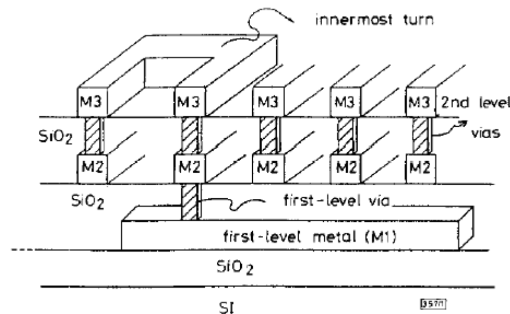


Fig. 2.7: Cross-section of a multi-metal layer inductor, from [52].

Layout Optimization

Another approach is to fabricate an inductor with a varied width in order to minimize the series resistance of the inductor coil. By studying the field distributions in the coil, it was found that ohmic losses dominate in the outer turns, and magnetic losses dominate in the inner turns. An algorithm to vary the trace width resulted in a layout optimized structure (Fig. 2.8). Lopez-Villegas fabricated a 35 nH inductor with a Q of 17 and values greater than 40 predicted for a 20 nH inductor at 3.5 GHz [53].

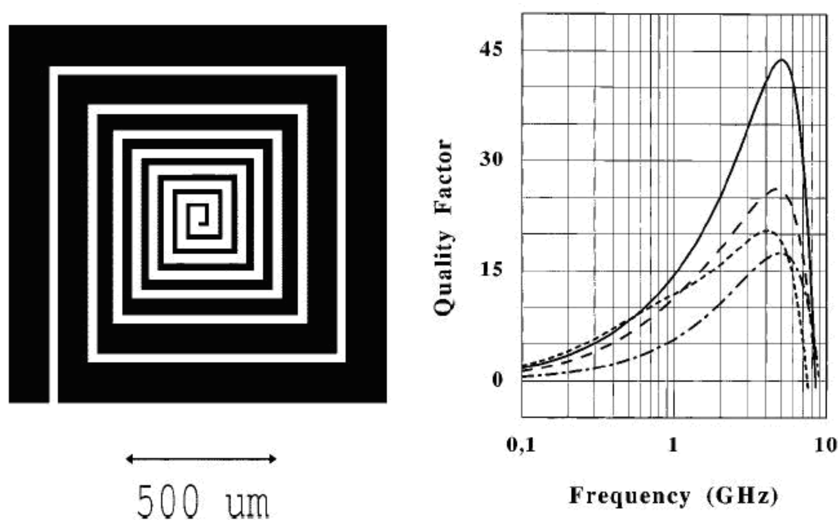


Fig. 2.8: Improvement in Q with layout optimization (—) compared to various single-width: 40 (— —), 25 (- -) and 10 (— ·) μm inductors, from [53].

2.3.3.2 RF MEMS Inductors

In MEMS technology, surface and bulk micromachining techniques have evolved to reduce sources of performance degradation in the low-resistivity Si by increasing the distance between the coil and the substrate.

Suspended Inductor using Bulk Micromachining

Bulk micromachined inductors are fabricated by removing the substrate under the inductor by front-side etching (Fig. 2.9). The planar inductor is suspended on a thin SiO_2 membrane by using an anisotropic etch (e.g. KOH) that naturally stops at the <111> crystal planes resulting in a precise trench beneath the structure. This device displayed an improved Q of 22, and f_{res} from 800 MHz to 3 GHz after the substrate was removed [46]. However, these structures may have limitations in respect to batch processing and increased packaging complexity. Bulk micromachining opened the MEMS processing era, but restricted designs in terms of industrial compatibility and structural issues associated with etching of the substrate. This is why surface micromachined inductors dominate the literature survey.

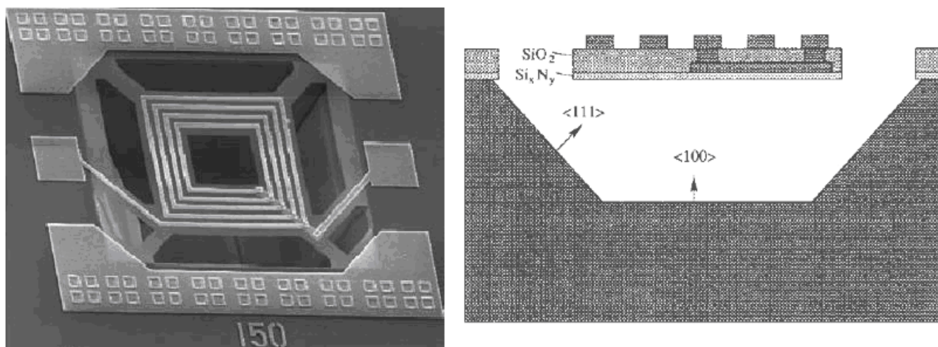


Fig. 2.9: Bulk micromachined inductor, from [46].

Elevated Inductor using Surface Micromachining

Yoon fabricated CMOS-compatible elevated spiral inductors by incorporating a 3-D photoresist mold to suspend the structures (fig 2.10). Similar to LIGA (X-ray lithography, electroplating, and molding), this process consists of fabricating mold inserts followed by electroplating. A high Q of 70 at 6 GHz was achieved with an inductance of 1.38 nH and f_{res} over 20 GHz [54].

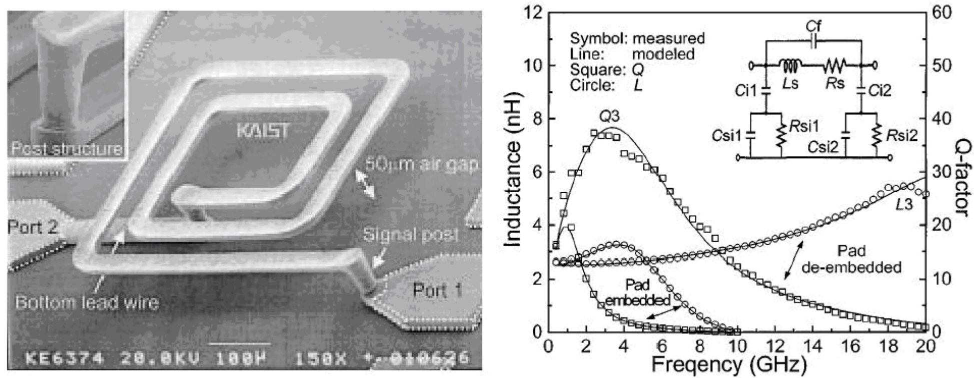


Fig. 2.10: Surface micromachined inductor, from [54].

Self-Assembly Inductor

Another method to achieve improved performance is to reduce the parasitics by physically lifting the inductor above the plane of fabrication using self-assembly techniques. Lubecke used the PolyMUMPs process to fabricate inductors with a 0.5 μm chromium-gold layer over a 1.5 μm layer of poly-Si [55]. Due to the difference in the residual stress of the two layers, the inductor bends away from the substrate. However, the anchor introduces an added resistance which limits the performance, so hinges were investigated. A 1.2 nH inductor was fabricated with a measured Q of 13 at 9 GHz (Fig. 2.11).

Plastic Deformation Magnetic Assembly Inductor

Plastic deformation magnetic assembly (PDMA) allows surface micromachined structures to be permanently bent without external energy. The structural layer is composed of a ductile metal such as gold, aluminum, or copper, and a magnetic material is adhered such as electroplated ferromagnetic permalloy ($Ni_{80}Fe_{20}$). After the structure is released, by applying an external magnetic field underneath the substrate, the structure bends away from the substrate. When the bending angle reaches a certain threshold, irreversible plastic deformation is reached and the structures retain their shape. Vertical spiral inductors and solenoid inductors were fabricated using this process (Fig. 2.12). The vertical spiral inductor displayed an improved Q from 8 to 24 and f_{res} from 1.1 GHz to 5.5 GHz [56].

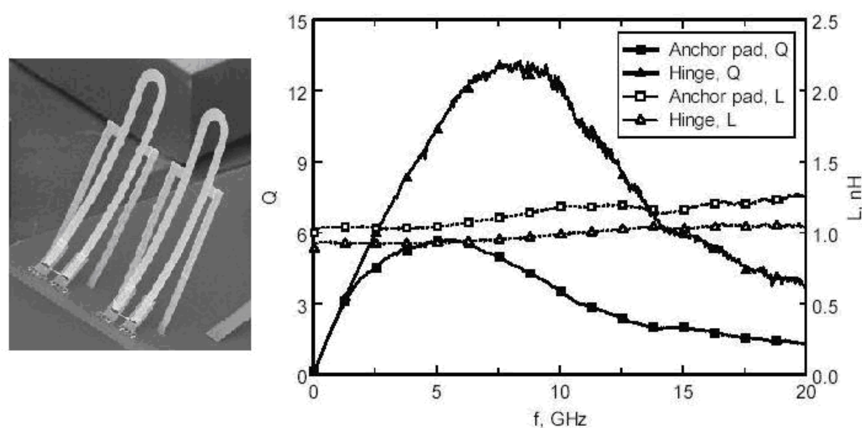


Fig. 2.11: Self-assembling tunable inductor, from [55].

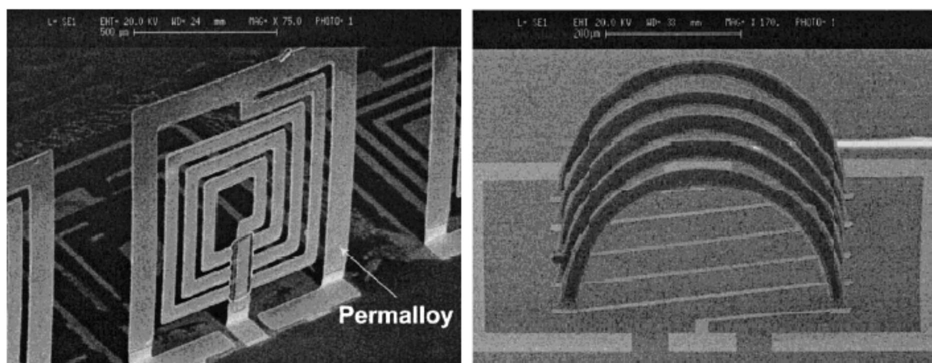


Fig. 2.12: 3-D Inductors by plastic deformation magnetic assembly, from [56].

2.4 Integrated Transformers on Silicon

Transformers are simply two inductor coils coupled together. Therefore, much of the background and modeling of inductors can also be applied to transformers with additional coupling components. In literature, many examples of monolithic transformers in RF circuits can be found. Transformers are used in filters to tune the center frequency [57], increase the Q of inductors [58], and to cancel out the parasitic capacitances to improve the high-frequency performance [59]. Transformers have also been implemented in VCOs [60]

and power oscillators [61], mixers [62], and LNAs [63].

The operation of a transformer is based on the mutual coupling between two conductors. The design is based on the coupling of alternating current from one winding to a second winding without significant loss of power. Research demonstrated that the Q of a two-port transformer can be higher than the Q of the inductor itself by as much as $(1 + k_m)$ factor [64]. Compared with spiral inductors, less research has been done on modeling and design of integrated transformers [65]. This could be due to transformer performance being more sensitive to the physical dimensions, and since various layouts exist making it difficult to obtain a generic model [65].

2.4.1 Modeling Parameters

Figure 2.13 is a compact model of a transformer based on Long's model [66] simplified by grounding two ports. This model is simply two inductor models as presented in Fig.2.3 with an added coupling coefficient. The transformer coupling is modeled by L_m, the magnetic coupling, L_p and L_s account for the leakage of the magnetic flux between the windings, and R_p and R_s represent the ohmic losses of the conductor windings. The other terms are as defined for the compact model of a planar inductor.

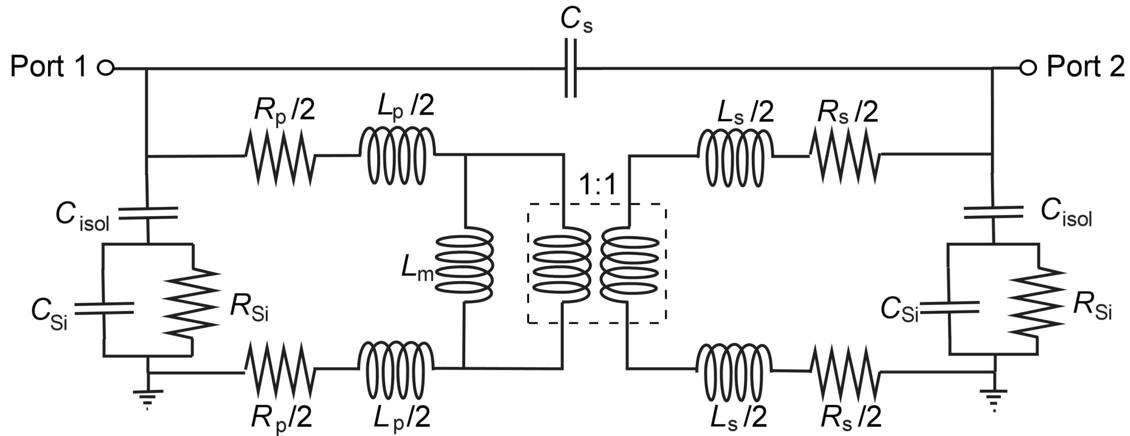


Fig. 2.13: Conventional compact model of a transformer on Si with 1:n turns ratio. It is based on the compact model of an inductor in Fig. 2.3.

2.4.2 Transformer Performance Metrics

Figure 2.14 is the schematic symbol of a planar monolithic transformer which can be realized from two inductor coils. Magnetic flux produced by the current i_p in the primary winding at P induces a current in the secondary winding that flows out of terminal S. This produces a potential across a load connected between S and $\overline{S}$. The phase of the voltage induced at the secondary winding depends on the connection scheme of the load. The AC signal is applied between terminals P and $\overline{P}$. In the non-inverting connection, the load is connected to S with $\overline{S}$ grounded which, results in a minimal phase shift at the secondary terminal. In the inverting connection, S is grounded, and the load is connected at $\overline{S}$ so the output is out of phase with the applied AC signal.

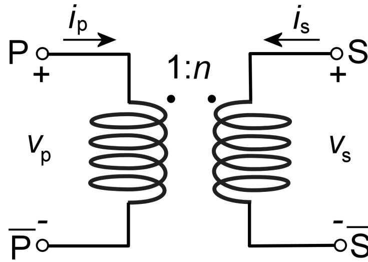


Fig. 2.14: Schematic symbol of a monolithic transformer. The primary (P) and secondary (S) coils are coupled by the turns ratio (n)

The parameters of interest are the turns ratio, n, and the magnetic coupling coefficient, k_m. The transformation between the primary and secondary windings are related to the turns ratio by:

$$n = \frac{v_s}{v_p} = \frac{i_p}{i_s} = \sqrt{\frac{L_s}{L_p}} \tag{2.23}$$

where L_p and L_s are the self inductances of the primary and secondary windings. The magnetic coupling coefficient is related to the self and mutual inductances by:

$$k_m = \frac{M}{\sqrt{L_p L_s}} \tag{2.24}$$

where M is the mutual inductance between the primary and secondary windings. The ideal

value for coupling is $k_m = 1$, where there is no leakage of the magnetic flux between the two coils, while uncoupled coils have a $k_m = 0$. Physically, leakage inductance is due to magnetic flux that links only one winding (not both). Methods of increasing k_m include: increasing the number of windings in order to increase M, reducing the spacing between windings to reduce the leakage inductance, or introducing magnetic material between the two windings to confine the magnetic field. In an IC process, the materials used have magnetic properties similar to air which prevent good confinement of the magnetic flux, therefore the coupling is considerably less than one [66].

For an inductor, the performance is well evaluated by Q. However, for transformers, a conventional figure of merit does not exist. The power transfer efficiency, G_{max}, is often used to describe the performance of the transformer [65]:

$$G_{\max} = \left|\frac{S_{21}}{S_{12}}\right| \left(n - \sqrt{n^2 - 1}\right) \tag{2.25}$$

where $n = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|}$ and $\Delta = S_{11}S_{22} - S_{12}S_{21}$. S_{11} is the return loss at port 1 and S_{21} is the insertion loss from port 1 to port 2.

In planar circuits, monolithic transformers are constructed using coils in the same plane, or in a stacked configuration. The mutual inductance and the parasitic coupling capacitance depend on the length of each winding. Overlaying or interleaving the coils maximizes the periphery between windings and increases the mutual inductance, however, the interwinding capacitance is also increased. Obviously, there are tradeoffs with the various designs (Fig. 2.15).

The parallel conductor winding (Shibata coupler) promotes edge coupling of the magnetic field between the windings (Fig. 2.15(a)). One disadvantage of this design is the asymmetry between the two windings because the lengths are not equal and therefore, the self inductances are not equal. In order to maximize the mutual inductance, the separation between the windings must be minimized.

To overcome the asymmetry in Shibata's design, Frlan came up with a symmetric design where the two windings have the same length (Fig. 2.15(b)). This ensures that the electrical characteristics of the primary and secondary windings are identical. Another advantage of this design is that the terminals are on opposite sides of the device for easy connection

to other circuitry. The interleaving of the mutual inductance achieves moderate coupling ($k_m \approx 0.7$). [45]. The coupling can be improved by reducing the width and spacing of the conductors, but this increases the series resistance.

Stacked metal layers for inductors were first designed by Finlay (Fig. 2.15(c)). The overlay structure makes use of both lateral and vertical magnetic coupling for a high coupling coefficient ($k_m \approx 0.9$) and an overall reduction in area [45]. However, this is classified as an asymmetrical design because the windings are implemented on different levels of metal and differences in metal thickness, sheet resistance, distance from substrate (upper winding is shielded from the substrate), etc. cannot be avoided. The main drawback is the large port-to-port capacitance between the windings which limits the operating frequency. In some cases, this capacitance can be incorporated in resonator applications [45]. Or this capacitance can be reduced by introducing a slight offset between the two windings or by increasing the vertical separation which will result in minimized reduction in k_m [45].

The coupling coefficient can be approximately calculated as [45]:

$$k_m \approx 0.9 - \frac{d_s}{d_{avg}} \; for \; d_s < 0.7\, d_{avg} \tag{2.26}$$

where d_s is the distance between the centre of the two spirals, and d_{avg} is the average diameter of the spirals. As $d_s < 0.7\ d_{avg}$, the coupling is more difficult to model [45].

Mohan implemented concentrically wound (or tapped) planar spirals (Fig. 2.15(d)). The common periphery between the primary and secondary winding is limited to one turn which leads to low mutual coupling (k_m = 0.3-0.5) [45]. The mutual coupling between adjacent turns contribute to the self inductance of each individual winding and as a result, the transformer has less mutual inductance, and more self inductance compared to the Frlan and Finlay configurations. There is no symmetry between the windings and applications of this implementation are limited, but may be applied to three-port broadband applications [45].

As discussed, each transformer configuration has its advantages and disadvantages in terms of symmetry, self-resonance frequency, self and mutual coupling, and real estate. IC designers must choose which layout will best suit the application at hand.

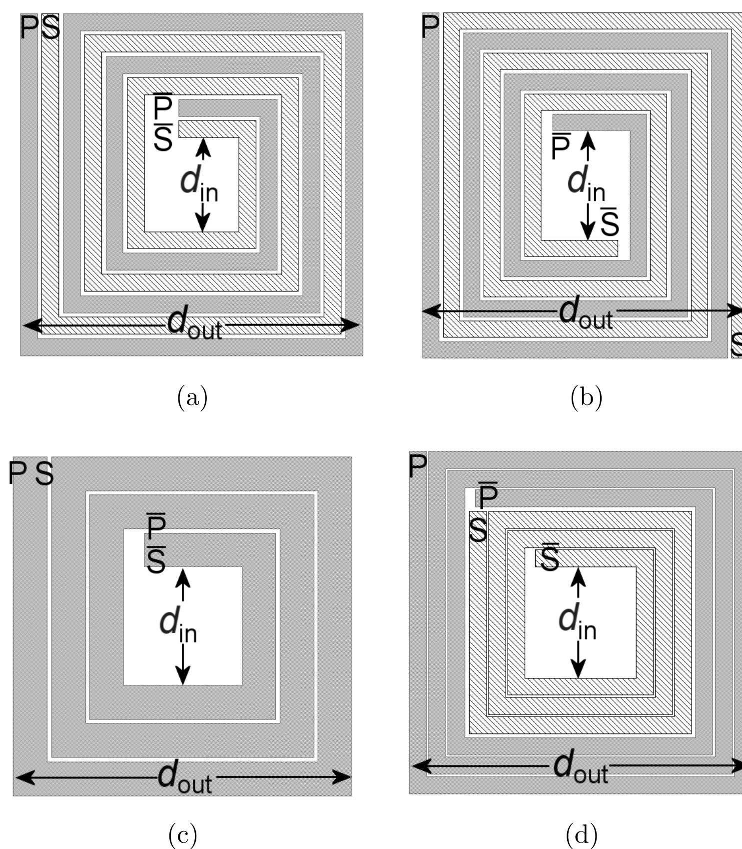


Fig. 2.15: Various planar transformer layouts, (a) interleaved, (b) symmetric, (c) stacked, and (d) concentric.

2.4.3 Previous Work

Some of the techniques reported in literature for the integration of transformers are briefly summarized in this section.

Transformers Fabricated with a Flip-Chip Process

Magnetic materials confine inductive coupling in transformers and to simplify the fabrication steps, the primary and secondary coils are manufactured separately and

assembled by flip-chip technology (Fig. 2.16). However, this design was only tested up to 10 MHz.

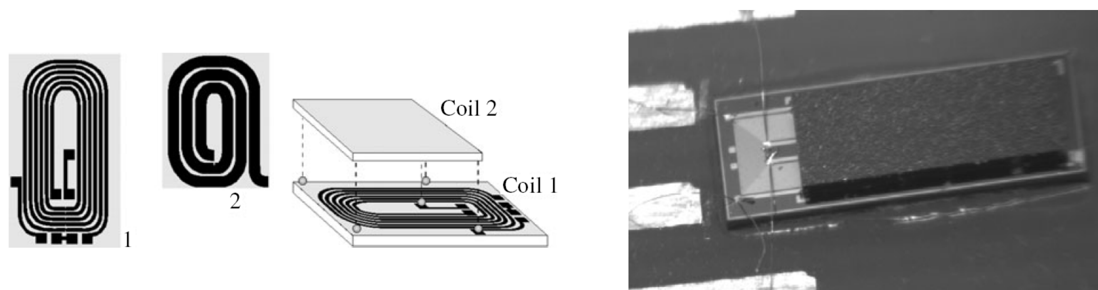


Fig. 2.16: Magnetic transformers fabricated in a flip-chip process measured up to 10 MHz, from [67]

MEMS Transformers with Magnetic Cores

Transformers were fabricated with electroplated permalloy magnetic cores in a surface micromachining process (Fig. 2.17). The fabrication process is complex due to the integration of magnetic materials, but this device has a high coupling coefficient of 0.85. This design was only tested up to 10 MHz.

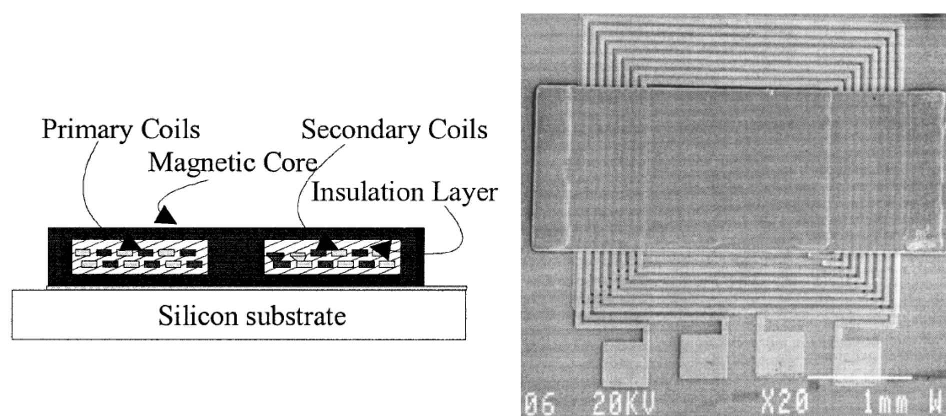


Fig. 2.17: Transformers fabricated with an electroplated permalloy magnetic core measured up to 10 MHz, from [68]

Spiral Transformers operating from 30-100 GHz

Transformers with f_{res} beyond 100 GHz were fabricated and a stacked transformer with reported S_{21} of -2.5 dB at 50 GHz occupying an area of only 30 $\times$ 30 μm^2 (Fig. 2.18). This work shows that spiral structures can be integrated for millimeter-wave applications. However, only inductances in the hundreds of picohenries can be realized for these dimensions.

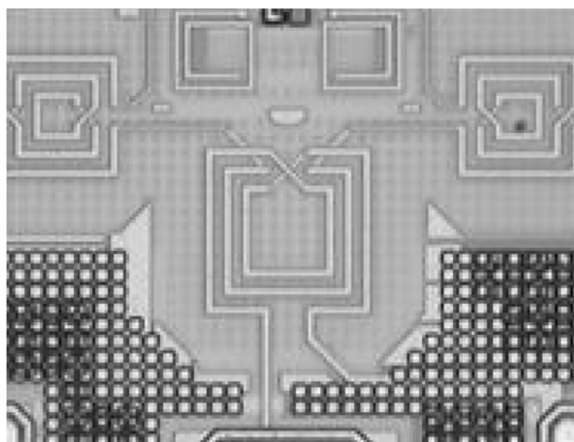


Fig. 2.18: Millimeter-wave inductors and transformers operating in the 30-100 GHz regime, from [69]

2.5 Summary

In this chapter, the applications of a-Si:H thin films in the microelectronics industry are summarized. Amorphous Si can be deposited at low temperature by PECVD which is attractive for many applications. Porous Si is also presented and the vast range of applications from optoelectronics to bio-chips is introduced. Both of these materials are low loss films that can be grown and formed at low temperature which is ideal for post-CMOS integration on Si.

In the area of integrating RFICs, it was shown that there is a lot of room for improving the quality factor of inductor on Si by studying the physical parasitics. Previous work

was summarized where joining metal layers, patterning ground planes, and optimizing layout were explored using traditional IC processes. Moreover, huge improvements in Q are achieved by bulk and surface micromachining techniques where the distance between the inductive coil and the lossy Si substrate is increased, reducing the parasitic losses. The modeling and and various layouts of transformers are also presented because these devices suffer from similar losses as inductors. The extensive scope of both inductors and transformers applied in RF circuits is emphasized and new approaches are needed in order to reach an integrated system on-chip solution.

Chapter 3

Development of Low Temperature Formation of Low Loss Films on Si

The main property that attracts researchers to study amorphous Si films is the low temperature deposition. This unleashes opportunities in many areas in terms of substrate and material selection and post-processing system integration. Amorphous Si has been thoroughly researched in the area of TFTs and solar cells where low defect density and high mobility are required. This is achieved by introducing dopant gases which significantly increase the conductivity of the semiconductor. However, undoped a-Si:H displays low conductivity, and this is the feature that will be explored in this thesis for improving the isolation of RF devices on Si. One obvious drawback of using a-Si:H as a dielectric is a high dielectric constant of 11.9. Porous silicon is another film that is studied in this work because by etching pores into the c-Si substrate, the effective dielectric constant is lowered. Porous Si is also a low temperature process as it can be formed at room temperature. The formation and properties of these low temperature and low loss films are studied in this chapter. In this context, these films are referred to as *thick* films because we are dealing with thicknesses greater than 1 μm. This also emphasizes the distinction from traditional thicknesses of hundreds of nanometers employed in traditional *thin* film microelectronics.

3.1 Development of Undoped Amorphous Silicon Thick Films

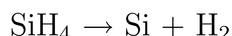
Dopant gases are introduced during the deposition of a-Si:H to achieve highly conductive electronic-grade films. However, in this work, undoped a-Si:H is applied in a novel application as a dielectric film deposited on Si to increase the effective resistivity of the substrate.

3.1.1 Film Formation

This process development in this work is focused on plasma enhanced CVD of a-Si:H films since our goal is to explore integration opportunities of a low thermal budget. The direct cause of the deposition of a-Si:H by PECVD is the dissociation of silane as neutral radicals or ions. Some gas dissociation reactions which require low activation energies include [6]:

$$SiH_4 \rightarrow SiH_2 + H_2$$

$$SiH_4 \rightarrow SiH_3 + H$$

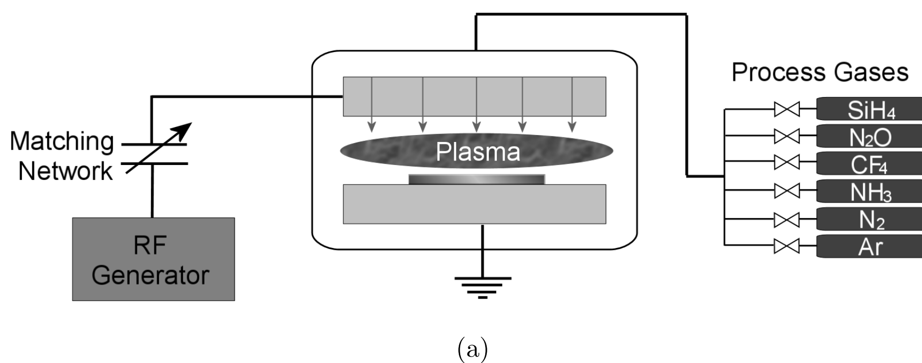


$$SiH_4 \rightarrow Si + H_2$$

There are other reactions which occur, but these require higher energies. SiH_3 accounts for 80% of the molecules present in a silane plasma [6].

Atomic hydrogen (H) plays a crucial role in the properties of a-Si:H. Since hydrogen is a light atom with only one bond, it can penetrate into the bulk material where it attaches to Si dangling bonds and strengthens weak Si-Si bonds. Thus, it traverses the Si network and passivates defects reducing the defect density which is important for device quality films. The stable bonding configurations in an a-Si:H network are Si-H bonds and unstrained Si-Si bonds [6] and it is believed that hydrogen is related to the mechanical film stress which is discussed in Chapter 5. The incorporation of hydrogen in the film depends on the deposition conditions in order for significant diffusion to occur. In PECVD a-Si:H films, if the substrate temperature is too high, the film does not retain hydrogen due to thermal excitation, and hence the hydrogen content decreases as substrate temperature increases. If the substrate temperature is too low, the diffusion coefficient is low and structural equilibrium cannot be achieved. Therefore, these hydrogen interactions determine the optimum growth temperature of 200-300℃ for PECVD a-Si:H [6].

In the PECVD chamber, reactive gases are separated by electrodes with a small gap and thus form a parallel-plate capacitor as shown in Fig. 3.1(a). The electrode the substrate sits on is grounded, and the other electrode is driven by an RF voltage. The electrons in the gas follow the electric field and decompose the gas molecules producing radicals and ions in a plasma. Therefore, the deposition species are decomposed in the plasma, rather than decompose by thermal means, allowing the substrate to remain at low temperature. A photograph of the Trion PECVD system in the Centre for Integrated RF Engineering (CIRFE) lab is shown in Fig. 3.1(b).



(a)

(b)

Fig. 3.1: (a) Schematic and (b) photograph of Trion PECVD load-lock system in the CIRFE lab.

In general, the PECVD process conditions which affect the film properties are [6]:

- **Pressure:** Determines the mean free path of the molecules which influences where reactions take place - at the growing surface or in the plasma. The chamber pressure of the Trion system can be set to a maximum of 1 T.
- **Flow rate:** Determines the residence time of the gas species in the reactor. For the deposition of undoped a-Si:H in our system, SiH_4 is the only gas used. If the flow rate is increased, the deposition rate will increase until there is sufficient reactant species in the plasma being consumed in the growing film.
- **Power:** Controls the rate molecules dissociate which influences the deposition rate; the higher the RF power, the higher the deposition rate. The Trion system has a 300 W, 100 kHz RF generator. For the a-Si:H thick films in our work, a reasonably fast deposition rate is required.
- **Temperature:** Controls the chemical reactions that take place at the growing surface and the hydrogen content of the film. The Trion system can be controlled from 50 to 400℃ by a resistive heater. In our work, a substrate temperature of 250℃ is used for the fabrication of planar devices, and 150℃ for the fabrication of MEMS devices.

Amorphous Si was deposited at a substrate temperature of 250℃ with the process conditions listed in Table 3.1. For the material characterization of a-Si:H, this recipe served as a starting point. Different film thicknesses were deposited and the deposition rate can be extracted from Fig. 3.2.

Table 3.1: PECVD process conditions for deposition of a-Si:H thick films at 250℃ giving a deposition rate of 3.3 Å/s (100 kHz parallel plate system with 8” electrode).

Parameter	**Setting**
Pressure	600 mT
RF Power	114 mW/cm^2
SiH_4 Gas Flow	10 sccm
Substrate Temperature	250 ℃
Deposition Rate	**3.3 Å/s**

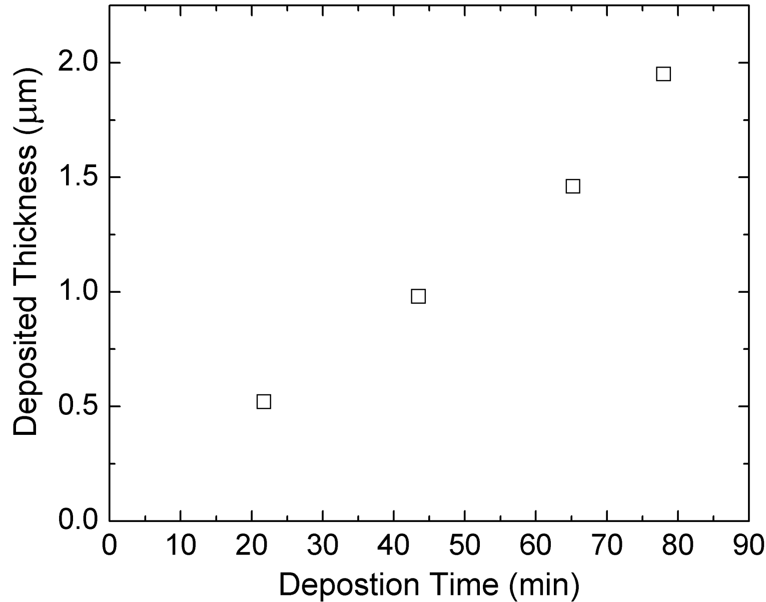
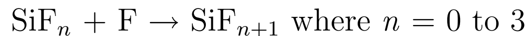


Fig. 3.2: Variation in deposition thickness with time of our PECVD a-Si:H thick films.

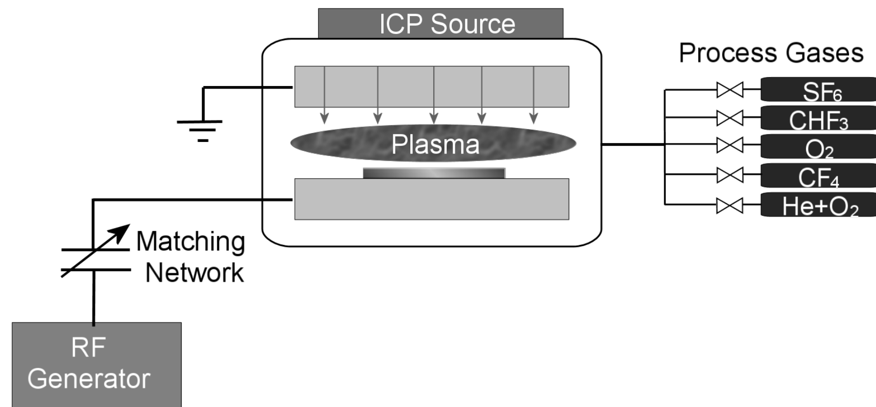
In order to measure the deposition rate, the a-Si:H films need to be patterned and etched. Silicon can be wet etched in a KOH solution, but for the application as a dielectric layer, the side wall angle of etched vias are of great importance and dry etching by reactive ion etching (RIE) in an SF_6 plasma allows more control. In the plasma, the SF_6 molecules will dissociate and produce F molecules which take part in the etching of Si:



$$SiF_n + F \rightarrow SiF_{n+1} \text{ where } n = 0 \text{ to } 3$$

When $n = 4$, SiF_4 leaves the substrate in a gaseous form. The chamber pressure needs to provide sufficient energy to ionize the available gas molecules. Increasing the pressure will result in an increase in the etch rate provided that each ion produced actually interacts with the layer being etched before being neutralized. In addition, if the pressure is increased, the mean free path of the ions decreases giving a more isotropic etch. Our a-Si:H films were etched by RIE with the Trion system in the CIRFE lab (Fig. 3.3). Process conditions were optimized to give a stable etch rate that can be accurately timed as to not over etch into the underlying Si substrate and to allow thick films to be etched in a reasonable amount of

time. The dry etch process conditions are listed in Table 3.2. The variation in the etched thickness and time is plotted in Fig. 3.4 to extract the etch rate.



(a)

(b)

Fig. 3.3: (a) Schematic and (b) photograph of Trion RIE system in CIRFE lab.

Table 3.2: RIE process conditions for etching a-Si:H thick films with an etch rate of 67 Å/s (parallel plate system with 8" electrode).

Parameter	**Setting**
Pressure	50 mT
RF Power	155 mW/cm^2
SF_6 Gas Flow	30 sccm
Etch Rate	**67 Å/s**

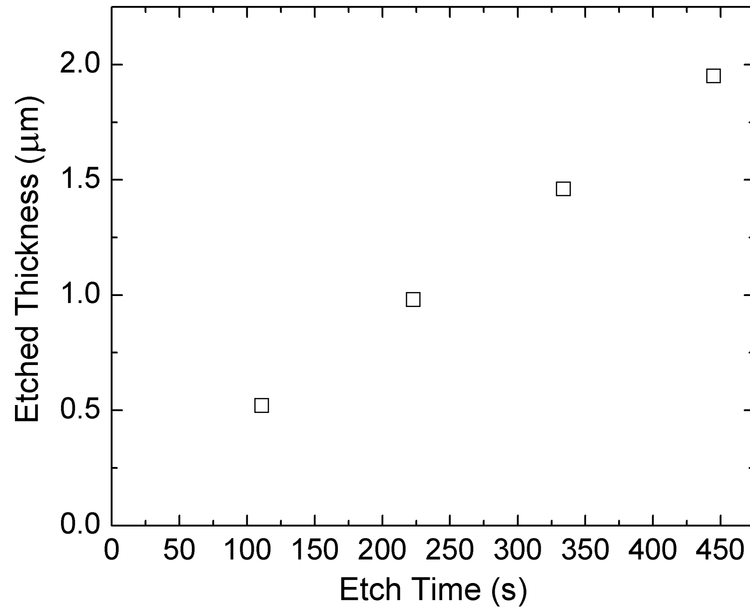


Fig. 3.4: Variation in etched thickness with time of our RIE a-Si:H thick films.

3.1.2 Film Characterization and Results

After developing a process to grow and etch undoped a-Si:H in the lab, material characterization is carried out to verify the film properties. The surface roughness and film uniformity of thick a-Si:H films is important for the development of multi-layer processes in the subsequent chapters. Verifying the dielectric losses and conductivity is crucial for

the application of undoped a-Si:H as an isolation layer. Finally, the hydrogen content and optical bandgap is extracted from IR and UV spectroscopy.

3.1.2.1 Film Uniformity of a-Si:H Thick Films

The film uniformity of 1 μm PECVD a-Si:H thick film deposited on a glass wafer was determined by etching a pattern and measuring the step height with a surface profiler as shown in Fig. 3.5. The variation in film thickness varies by less than ± 5% which is acceptable for our deposition system which can accomodate upto 8" substrates.

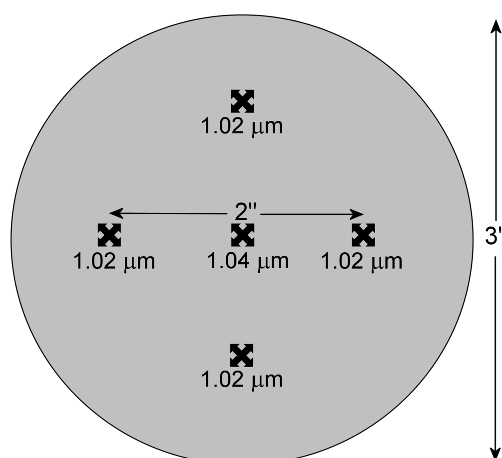


Fig. 3.5: Film uniformity of 1 μm a-Si:H thick film deposited on glass for this study. The step height was measured with a surface profiler to determine the variation in film thickness across the wafer.

3.1.2.2 Surface Roughness of a-Si:H Thick Films

The surface roughness of PECVD a-Si:H 1 to 4 μm thick films was measured with a Veeco optical profiler. The average roughness is calculated over the entire measured area. The surface roughness of a 4 μm thick film over a 121×92 μm^2 area was measured to be 1.04 nm as shown in Fig. 3.6(d). The increase in surface roughness for increasing film thicknesses is minimal and this magnitude of nanometer roughness (less than 0.1%) will not pose any problems for stacking films in multi-layer processes developed for device applications.

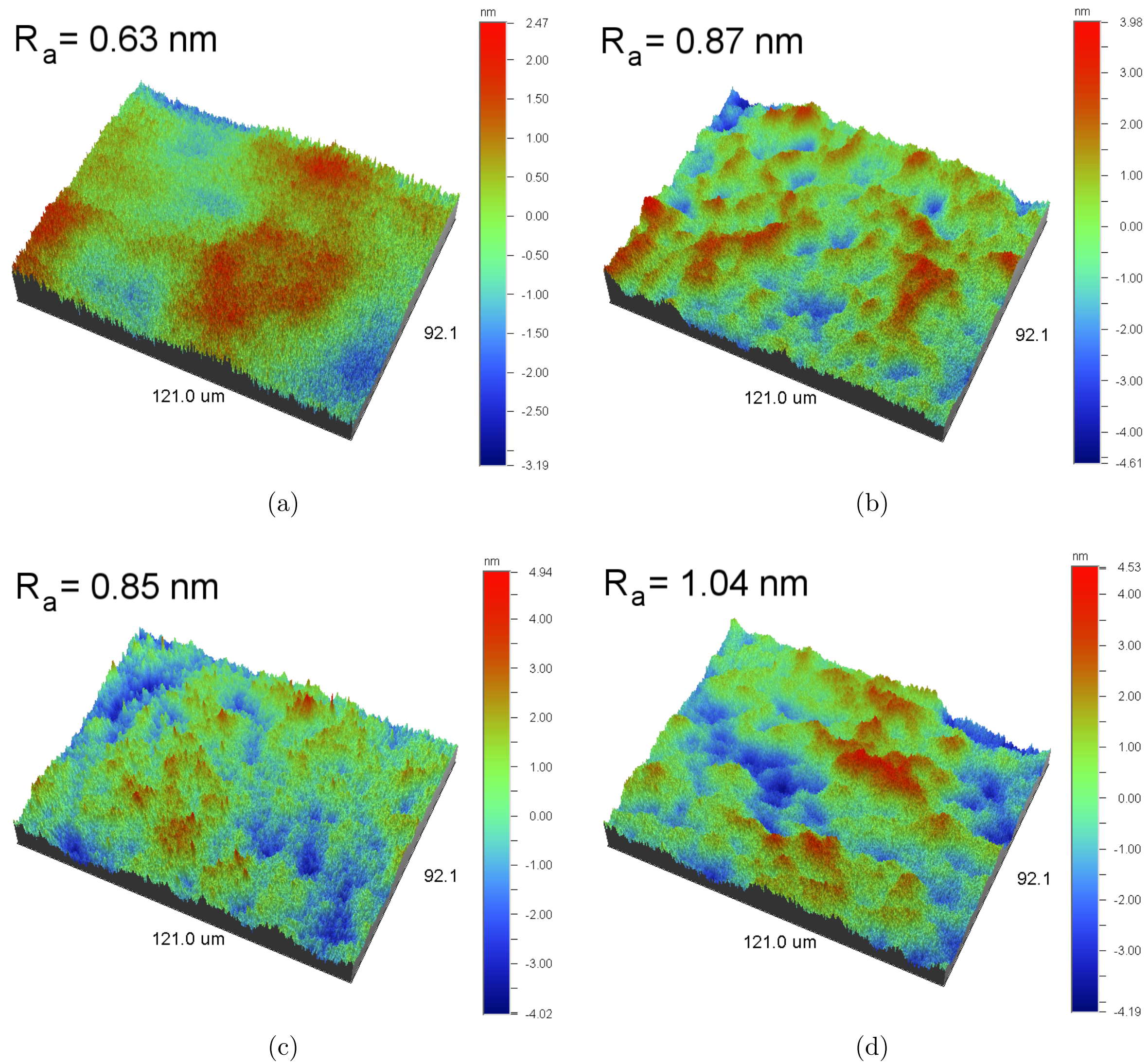


Fig. 3.6: Surface roughness of our PECVD a-Si:H thick films (a) 1 μm, (b) 2 μm, (c) 3 μm, and (d) 4 μm. The average surface roughness calculated over an area of 21×92 μm^2 is less than 0.1%.

3.1.2.3 Dielectric Constant of a-Si:H Thick Films

The dielectric constant of a material is a physical measure of the electrical polarizability. Electrical polarizability is the tendency of a material to allow an externally applied electric

field to induce electric dipoles in the material. The polarization, P, is related to the electric field, E, and displacement, D [70]:

$$D = \epsilon_0 E + P \tag{3.1}$$

where $\epsilon_0 = 8.8542\times10^{-14}$ F/cm. The polarization is related to the electric field by the electrical susceptibility, χ_e:

$$P = \epsilon_0 \chi_e E \tag{3.2}$$

$$D = \epsilon_0 \left(1 + \chi_e\right) E = \epsilon_0 \epsilon_r E \Rightarrow \epsilon = \frac{D}{E} \tag{3.3}$$

When an electric field is applied to a perfect insulator, a displacement current will be generated. Permittivity, ϵ, is defined as the ratio of the displacement current to the electric field. The dielectric constant is crucial in determining the coupling capacitance between conductors in the same plane, or in different metal layers. In a perfect vacuum, there are no atoms to polarize, so $\chi_e = 0$ and $\epsilon_r = 1$. When an electric field is generated in a vacuum, the permittivity is defined as the permittivity of free space, ϵ_0. The relative dielectric constant is defined as:

$$\epsilon_r = \frac{\epsilon}{\epsilon_0} \tag{3.4}$$

The dielectric constant is extracted from the measuring the capacitance of a parallel plate capacitor:

$$\epsilon_r = \frac{C\,t}{\epsilon_0\,A} \tag{3.5}$$

where C is the capacitance, A is the area of the deposited metal, and t is the thickness of the dielectric.

Capacitors were fabricated to measure the dielectric constant of a-Si:H. First, 1 μm of Al was sputtered on a Corning glass substrate, followed by 0.5 μm of a-Si:H deposited by PECVD with the conditions given in Table 3.1. Then a portion of the a-Si:H was dry etched in order to make contact with the bottom metal layer. Another 1 μm of Al was sputtered through a shadow mask with 600 μm diameter dots in order to form parallel-

plate capacitors. The capacitance-voltage (CV) measurements taken with a Keithley semiconductor characterization system are shown in Fig. 3.7. A dielectric constant of 11.66 was measured at 1 MHz which corresponds to values found in literature [6].

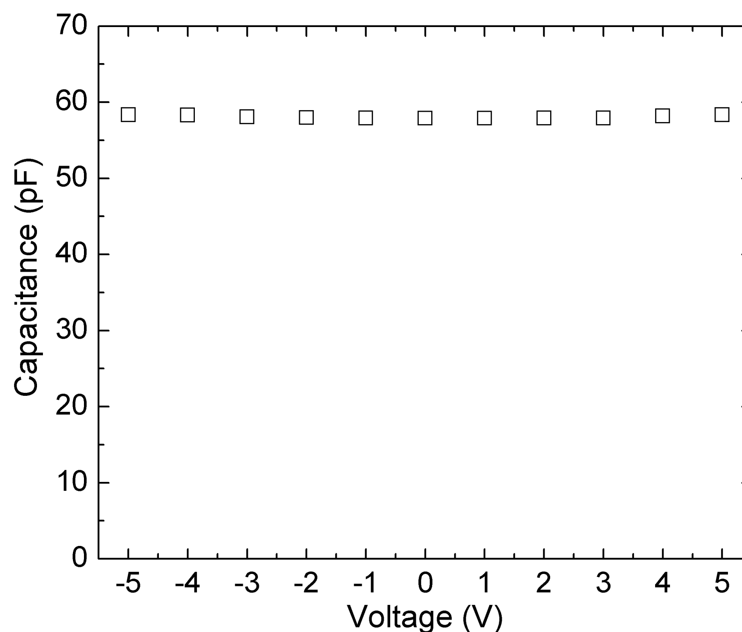


Fig. 3.7: Capacitance-voltage measurements of 0.5 μm of a-Si:H with 6 mm diameter capacitor. A dielectric constant of 11.66 is extracted for our a-Si:H films

3.1.2.4 Loss Tangent of a-Si:H Thick Films

In a solid, three polarization mechanisms dominate: electronic, atomic, and dipolar polarization. Each polarization mechanism has an associated response time and therefore, contributes to the dielectric constant in different frequency ranges. When an AC field is applied, dielectric losses due to molecular motion and relaxation are activated. The molecules align with the electric field, and as the polarity changes, so does the alignment. Therefore, the permittivity is defined as a complex number to incorporate the dielectric losses due to polarization:

$$\epsilon = \epsilon' - j\epsilon'' \tag{3.6}$$

A common quantity associated with dielectrics is the loss tangent (also known as loss angle or dissipation factor):

$$tan\delta = \frac{\epsilon''}{\epsilon'} \tag{3.7}$$

To extract the loss tangent of a-Si:H films, the loss of transmission lines are measured. The propagation factor of a wave propagating through a material is given by:

$$T = exp\left(-\gamma\ell\right) = exp\left[-\left(\alpha + j\beta\right)\ell\right] \tag{3.8}$$

where γ is the propagation constant, α is the attenuation constant, and β is the phase constant defined as:

$$\beta = \frac{2\pi}{\lambda_g} \tag{3.9}$$

where λ_g is the guided wavelength of the transmission line:

$$\lambda_g = \frac{2\pi}{\omega\sqrt{\epsilon\mu}} = \frac{\lambda_0}{\sqrt{\epsilon_r\mu_r}} \tag{3.10}$$

The reflection coefficient, Γ, is given as [71]:

$$\Gamma = K \pm \sqrt{K^2 - 1}\; such\, that\, |\Gamma| \leq 1 \tag{3.11}$$

where $K = \frac{S_{11}^2 - S_{11}^2 + 1}{2S_{11}^2}$. The transmission coefficient can be simplified by approximating $\alpha = 0$:

$$T = exp\left(-j\omega\sqrt{\epsilon\mu}\,\ell\right) \tag{3.12}$$

and is also defined in terms of the reflection coefficient as:

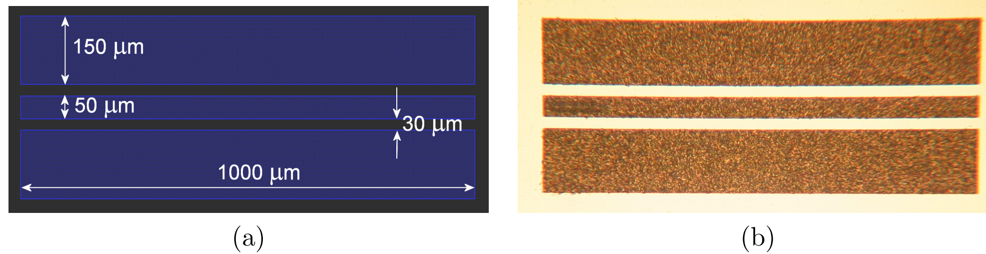
$$T = \frac{S_{11} + S_{21} - \Gamma}{1 - \left(S_{11} + S_{21}\right)\Gamma} \tag{3.13}$$

The complex dielectric constant as a function of frequency is extracted from:

$$\epsilon_r = \frac{\frac{1}{\Lambda^2}\lambda_0^2}{\mu_r} \tag{3.14}$$

where $\frac{1}{\Lambda^2} = -\left[\frac{1}{2\pi\ell} ln\left(\frac{1}{T}\right)\right]^2 \Rightarrow Re\left\{\frac{1}{\Lambda}\right\} = \frac{1}{\lambda_g}$.

Accurately measuring the loss tangent of thin films is challenging and often electromagnetic (EM) simulators are used in conjunction with curve fitting of measured results. The S-parameters of fabricated coplanar waveguide (CPW) lines was measured and the losses in the metal were de-embedded with EM simulations. Using Eqn. (3.14), the loss tangent of a-Si:H was calculated to be 0.005 at 4 GHz. This value is similar to the loss tangent of c-Si [70]. This method of extracting the loss tangent of a film is not accurate enough to distinguish the difference between the losses in the substrate and the film. Either much thicker a-Si:H films are required, or the spacing of the CPW transmission line has to be greatly reduced by an improved photolithography process. The insertion loss of CPW transmission lines on a-Si:H with different film thicknesses is shown in Fig. 3.9. The dimensions and micrograph of the CPW line are shown in Fig. 3.8 and the metal film thickness is 2 μm of Al. When 1 μm of a-Si:H is deposited on p-type <100> 8-12 Ω cm c-Si, the insertion loss is -1.7 dB at 1.5 GHz. By doubling the a-Si:H thickness to 2 μm, the insertion loss improves by 0.4 dB, for 3 μm thick film the loss improves by another 0.35 dB, and for 4 μm the loss improves by 0.2 dB. For an a-Si:H film thickness less than 3 μm, the insertion loss can be approximated to have a linear dependence on the film thickness. These results can be accurately predicted with simulations.



(a) (b)

Fig. 3.8: (a) Layout and (b) micrograph of a CPW transmission line used to extract the loss tangent of our a-Si:H thick films.

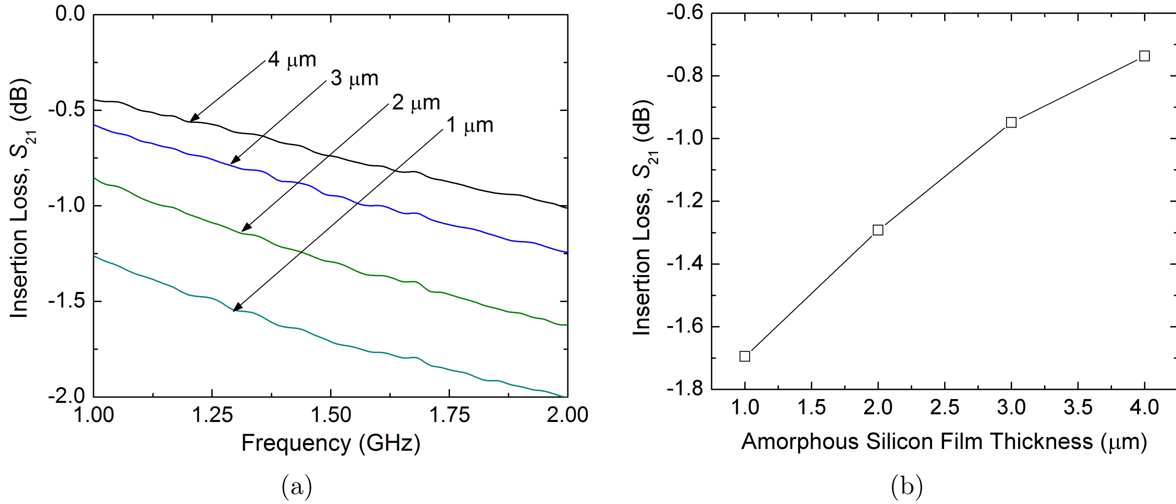


Fig. 3.9: The measured insertion loss of CPW transmission lines on 1, 2, 3, and 4 μm PECVD a-Si:H. (a) A 4 μm a-Si:H film results in an S_{21} of -0.45 dB at 1 GHz. (b) The S_{21} at 1.5 GHz is plotted for each film thickness where a linear dependence exists for films less than 2 μm.

3.1.2.5 Conductivity of Undoped a-Si:H Thick Films

When an electrical potential is applied across a material, free charges flow and an electric current can be measured. Electrical conductivity, σ, is a measure of how well a material accommodates the transport of electrons. It is defined as the ratio of current density, J, to the electric field, E:

$$\sigma = \frac{J}{E} \tag{3.15}$$

In order to measure the conductivity of a-Si:H, 1 μm was deposited by PECVD on a glass substrate, and Al was sputtered using a shadow mask to form two contacts with a GMD separation of 1.3 mm over a length of 10 mm. The conductivity of the material was measured from current-voltage (IV) measurements. A linear fit is used to calculate the conductivity:

$$\sigma = \frac{d}{A}\frac{dI}{dV} \tag{3.16}$$

where d is the thickness of the film, and A ($D \times L$) is the area between the two metal contacts (Fig. 3.10).

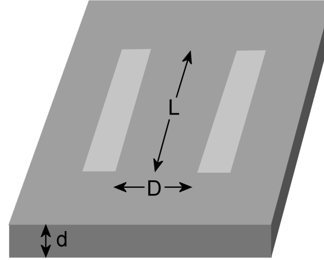


Fig. 3.10: Structure used to measure conductivity of a dielectric film in this work.

The conductivity of a-Si:H was measured in the dark and the IV characteristics are shown in Fig. 3.11(a). Then the sample was illuminated by a halogen tungsten lamp with an intensity of 4 mW/cm^2 and the photoconductivity was extracted from the IV characteristics in Fig. 3.11(b). A dark conductivity of $1{\times}10^{-10}$ S/cm and a light-induced conductivity, photoconductivity, in a-Si:H of $1{\times}10^{-6}$ S/cm was calculated. This decrease in conductivity is due to the creation of defects in localized gap states in the a-Si:H material [72]. This is one of the most widely studied metastablility effects in a-Si:H and was discovered due to the degradation of solar cells exposed to sunlight. It was observed that there's an initial decrease in the photoconductivity during illumination and then a decrease in dark conductivity after illumination [6]. However in our work, ideally, the devices would be packaged so undoped a-Si:H is treated as a dielectric material.

3.1.2.6 Hydrogen Content of a-Si:H Thick Films

Atomic hydrogen plays a crucial role in the material properties of a-Si:H. Since hydrogen is a light atom with only one bond, it can penetrate into the bulk of the material and passivate defects. The origin of stress in a-Si:H films is not well understood [73], but is generally accepted that hydrogen incorporation and bonding configurations with Si is related to stress since hydrogen relieves strained bonds. A non-destructive technique to measure the hydrogen content is Fourier Transform infrared (FTIR) spectroscopy. In the infrared spectrum of a-Si:H, three absorption regions exist [74]:

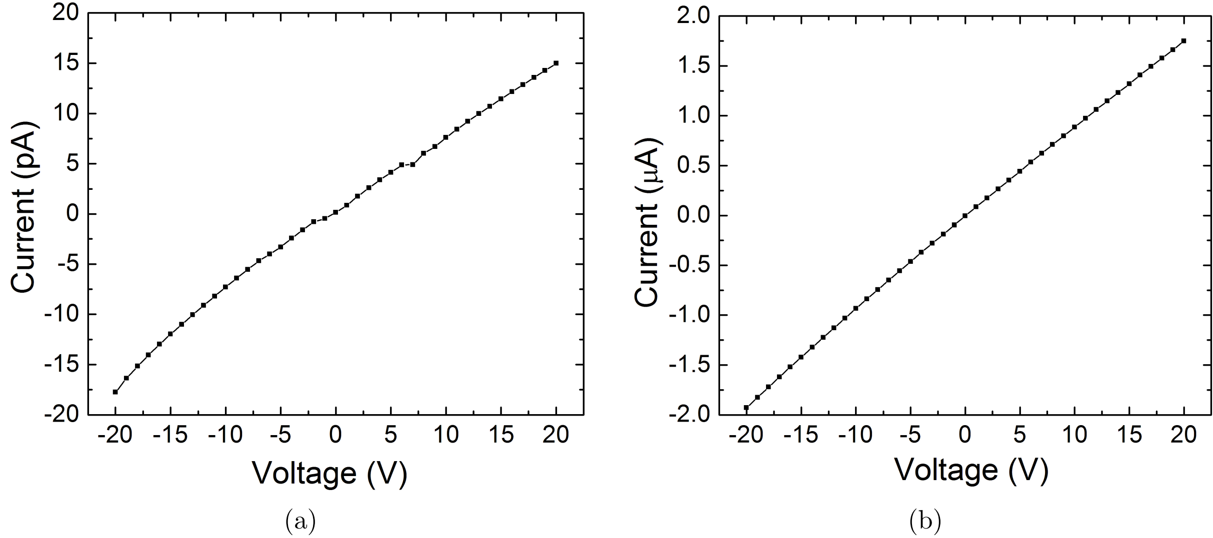


Fig. 3.11: Conductivity of 1 μm a-Si:H thick film measured in this research, (a) dark conductivity of 1×10^{-10} S/cm and (b) photoconductivity of 1×10^{-6} S/cm is calculated.

- wagging mode at 640 cm^{-1}
- dihydride bending or scissor modes at 840-890 cm^{-1}
- stretching modes at 2000 and 2100 cm^{-1}

FTIR analysis was carried out on 1 μm of a-Si:H deposited by PECVD on a c-Si substrate and the hydrogen content was calculated as described in Appendix B. Figure 3.12(a) is the measured transmitted light in the infrared regime. All transmission measurements are made relative to an uncoated reference c-Si substrate. The normalized transmission spectrum is shown in Fig. 3.12(b). The hydrogen content (C_H) was calculated from the absorption of the wagging mode at 640 cm^{-1} with proportionality coefficient, $A_{640} = 2.1\times10^{19}$ cm^{-2} [74], and found to be 20 at.%. Device quality a-Si:H films typically have C_H of 10 at.% [75]. The stretching mode at 2000 cm^{-1} is commonly associated with isolated monohydride (SiH) absorption, and at 2100 cm^{-1} with clustered monohydrides and polyhydrides (SiH_2, SiH_3). The concentration of these bonds can be calculated from the Gaussian deconvolution of the peaks at 2000 and 2100 cm^{-1} as shown in Fig. 3.12(c). These hydrogen bonding configurations can provide some information about the microstructure of the network. In our films, there was no measurable variation in the absorption of

the deconvoluted peaks with change in thickness. This means that during film growth, there is no obvious change or redistribution of the hydrogen bonding configurations [76]. The incorporation of hydrogen in the amorphous network is discussed in relation to the mechanical film stress in Chapter 5.

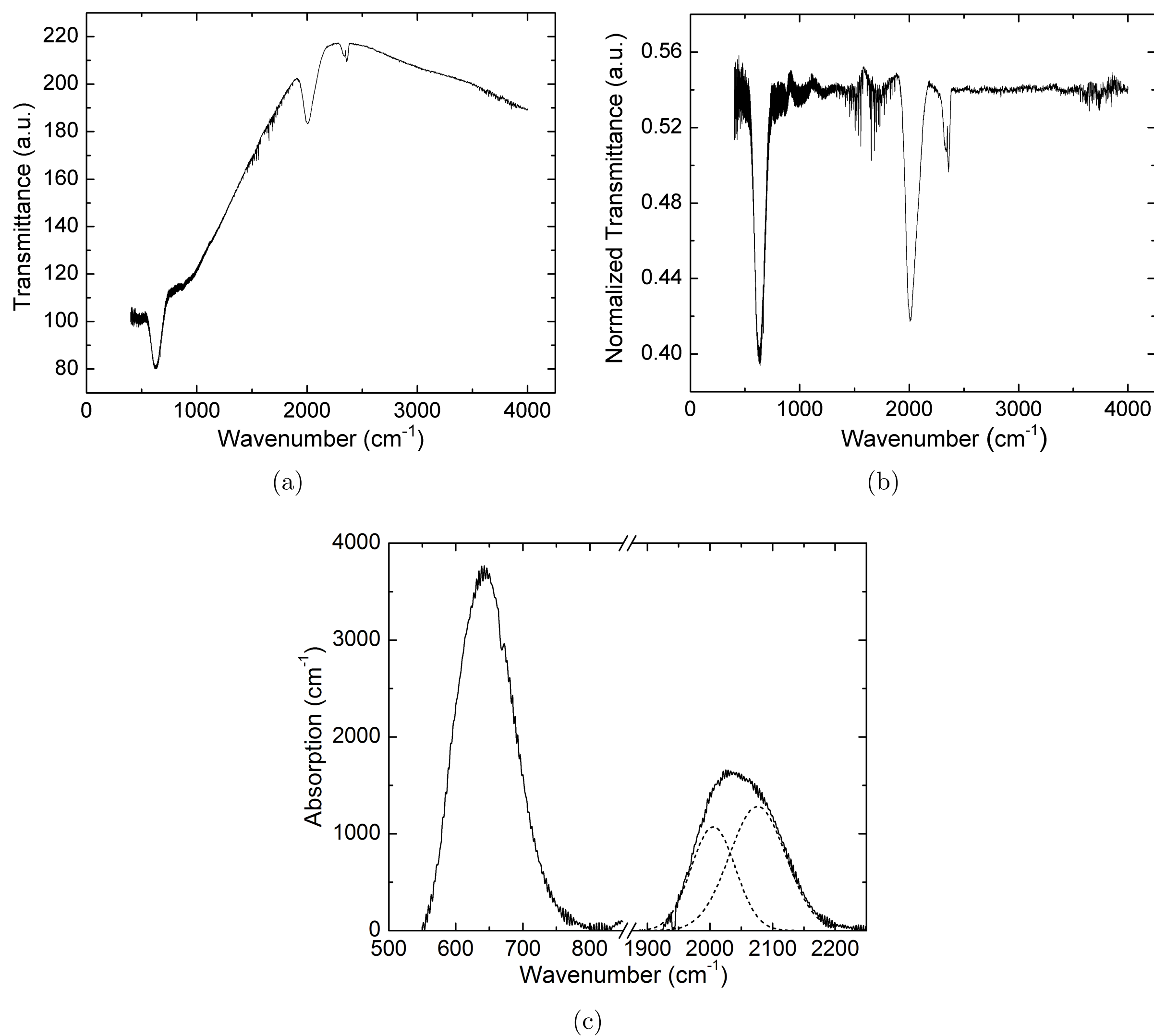


Fig. 3.12: (a) Infrared transmission spectrum of our PECVD a-Si:H thick films, (b) normalized infrared transmission spectrum with c-Si substrate absorption removed, and(c) Gaussian deconvolution of the peaks at 2000 and 2100 cm^{-1}.

3.1.2.7 Optical Bandgap of a-Si:H Thick Films

The optical bandgap is calculated with the following equations:

$$\alpha = -\frac{1}{d}\left[ln\left(\frac{T}{0.59359217}\right)\right] \tag{3.17}$$

$$\sqrt{\alpha h\upsilon} = A\left(h\upsilon - E_{opt}\right) \tag{3.18}$$

where α is the absorption coefficient and E_{opt} is the optical bandgap. The derivation of these equations is described in Appendix C.

UV measurements of a glass substrate with 1 μm a-Si:H film deposited by PECVD are shown in Fig. 3.13(a). The Tauc plot was extracted and is shown in Fig. 3.13(b). By extrapolation, an optical bandgap of 1.72 eV was verified which is in good agreement with values reported in literature [6]. Note that since this definition of the gap is based on extrapolation of the density of states, this value is more useful for comparing a-Si:H films prepared by different methods. In our work, we calculate the bandgap to ensure that the material we are depositing is indeed amorphous silicon. Since we are interested in using undoped a-Si:H as an insulating material, determining the defects in the bandgap are not a priority.

Light reflected from the front and back surfaces of the sample will interfere which introduces an oscillating behavior in the transmission versus wavelength graph. Thin film interference can be used to determine the thickness when the index of refraction is known. Interference arises from the refractive index discontinuity between the film and the substrate. Maximum reflectance occurs at wavelengths for which the optical thickness satisfies:

$$t = \frac{m\lambda_0}{2n_1} = \frac{(m+1)\,\lambda_1}{2n_1} = \frac{(m+2)\,\lambda_2}{2n_1} = \frac{(m+i)\,\lambda_i}{2n_1}\ or\ m = \frac{\lambda_1}{\lambda_0 - \lambda_1} \tag{3.19}$$

Given two maximums the thickness can be found as:

$$t = \frac{\lambda_0\lambda_1}{2n_1\left(\lambda_1 - \lambda_0\right)} \tag{3.20}$$

From Fig. 3.13(a) and $n_{a-Si:H} = 3.9$ at 800 nm [77], a film thickness of 1.2 μm is extracted (actual thickness measured by a surface profiler was found to be 1.0 μm). This is a simple, non-destructive method to estimate the film thickness.

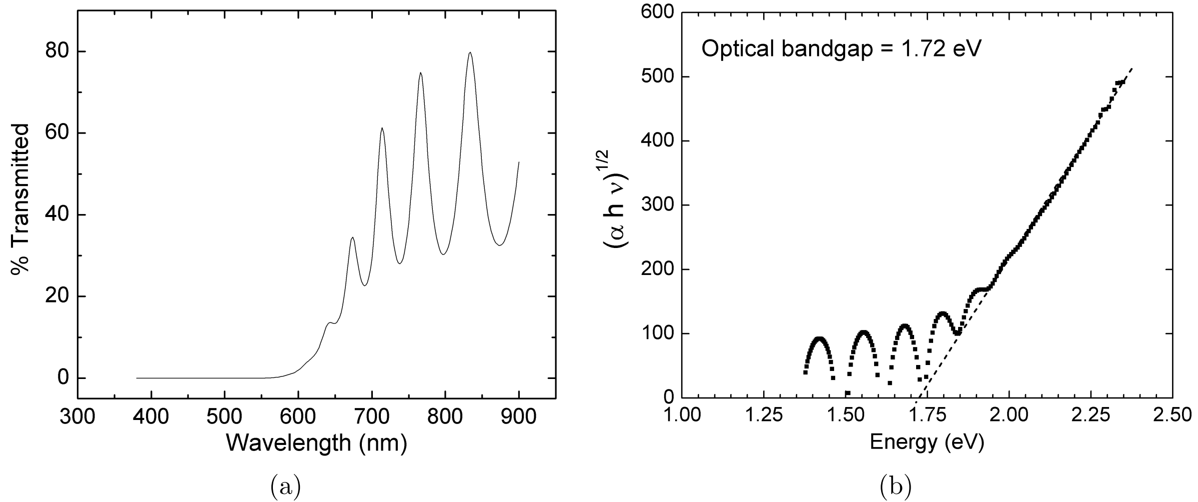


Fig. 3.13: (a) UV spectrum and (b) Tauc plot of 1 μm PECVD a-Si:H thick film deposited on a glass substrate for this study. An optical bandgap of 1.72 eV is extracted.

3.1.3 Summary

Process development of the deposition and etching of a-Si:H has been presented in this section. The film uniformity and surface roughness is good for continuing with the fabrication of a multi-layer process. The growth rate and etch rate are controlled and repeatable and can be adopted in industry-scale processing. The basic optoelectronic properties of our a-Si:H films have been verified and are in agreement with values reported in literature. In the following chapters, a-Si:H is used for the fabrication of planar inductors, and is also proposed as a structural material for the fabrication of MEMS inductors and transformers. It is also explored as the encapsulating layer for the formation or porous Si films.

3.2 Formation of Porous Silicon Thick Films

Porous Si is another low temperature candidate film explored to improve the isolation of RF devices on low resistivity Si.

3.2.1 Film Formation

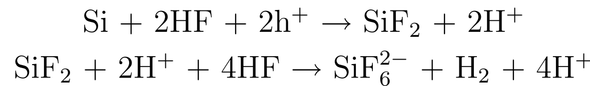
Porous Si can be formed by electrochemical or chemical etching. The discussion in this report will be focused on the pore formation of p-type Si substrates and HF-ethanol electrolytes due to the relative ease of forming PS layers without the requirement of illumination.

3.2.1.1 Electrochemical Etching

Porous Si can be formed by electrochemical etching of a Si substrate in an HF-based solution. When a positive voltage is applied to the Si substrate with respect to an electrode placed in the electrolyte, a current flows through the system. If purely HF is used to form PS, hydrogen bubbles stick to the surface of the substrate and lateral and in-depth inhomogeneity is observed. For efficient bubble elimination, ethanol is used to improve the electrolyte penetration in the pores [15]. Platinum (Pt) or any order HF-resistant conducting material is used as the electrode.

The simplicity of forming pores in Si contrasts to the complexity of physical and chemical mechanisms involved in the process. Si is known to be virtually inert against attack of HF acid, but when a current flows through the interface, electrochemical etching occurs [78]. This dissolution of Si only occurs when holes are available at the interface, meaning the Si electrode is positively biased - such that electrochemically etching of Si is also called anodization. Lehmann and Gosele proposed the theory illustrated in Fig. 3.14. When a hole from the bulk arrives at the electrolyte interface, the Si-H bond is attacked by F^- ion and is replaced with Si-F bond (Fig. 3.14(a)). This is the rate-limiting step for pore formation. Due to the polarization of the bonded fluoride molecule, another F^- ion attack occurs releasing an H_2 molecule and as a result, injection of one electron into the Si network (Fig. 3.14(b) and (c)). These two Si-F bonds polarize the remaining two Si backbonds which weaken the bond strength and can be attacked by HF or H_2O (Fig. 3.14(d)). The surface

atoms of the Si remain bonded to H (Fig. 3.14(e)). The reaction product SiF_4 would be gaseous, but it reacts with HF and stays in the solution and gives rise to hydrogen bubbles. This results in pit formation, changing the surface geometry and hence, the electric field distribution. As long as the walls of the pores are depleted of holes, they will be protected against further dissolution. This mechanisms can be described in two-steps as [26]:



$$Si + 2HF + 2h^+ \rightarrow SiF_2 + 2H^+$$
$$SiF_2 + 2H^+ + 4HF \rightarrow SiF_6^{2-} + H_2 + 4H^+$$

If a high current density is applied, many holes are available at the surface and the Si dissolution is limited by the diffusion of F^- ions which results in electropolishing. In the case of a low current density, the etching is limited by the hole diffusion in the pits and pores are formed [79]. Pores grow preferentially along <100> directions toward the source of holes [80] because Si atoms in the <111> surface have three bonds connected to the substrate lattice, while those in the <100> surface have only two, thus weaker attachment to the surface [79]. It should be noted that PS quickly oxidizes in ambient so an encapsulating layer is required. Amorphous Si is explored for this application in the next chapter for the fabrication of planar inductors.

3.2.1.2 Stain Etching

Porous Si can also be produced by pure chemical etching, known as stain etching, in an HF:HNO_3 solution. The pore structure of both methods is similar, however stain etching may result in inhomogeneous porosity and thicknesses [79]. The oxidation-reduction chemistry is essentially the same as that of anodization where points on the Si surface are random localized anodes and cathodes [81]. In this case, the oxidizing agent is HNO_3 which injects holes and oxidizes the Si which is removed by reacting with HF. Similar to electrochemical Si dissolution, chemical etching can result in polishing or pore formation depending on the concentration of HF:HNO_3. Many holes are injected in the case of HNO_3-rich solutions, and the Si dissolution is limited by the presence of fluoride ions which results in polishing of the surface. An HF-rich solution results in a process limited by the available holes and can lead to stain etching.

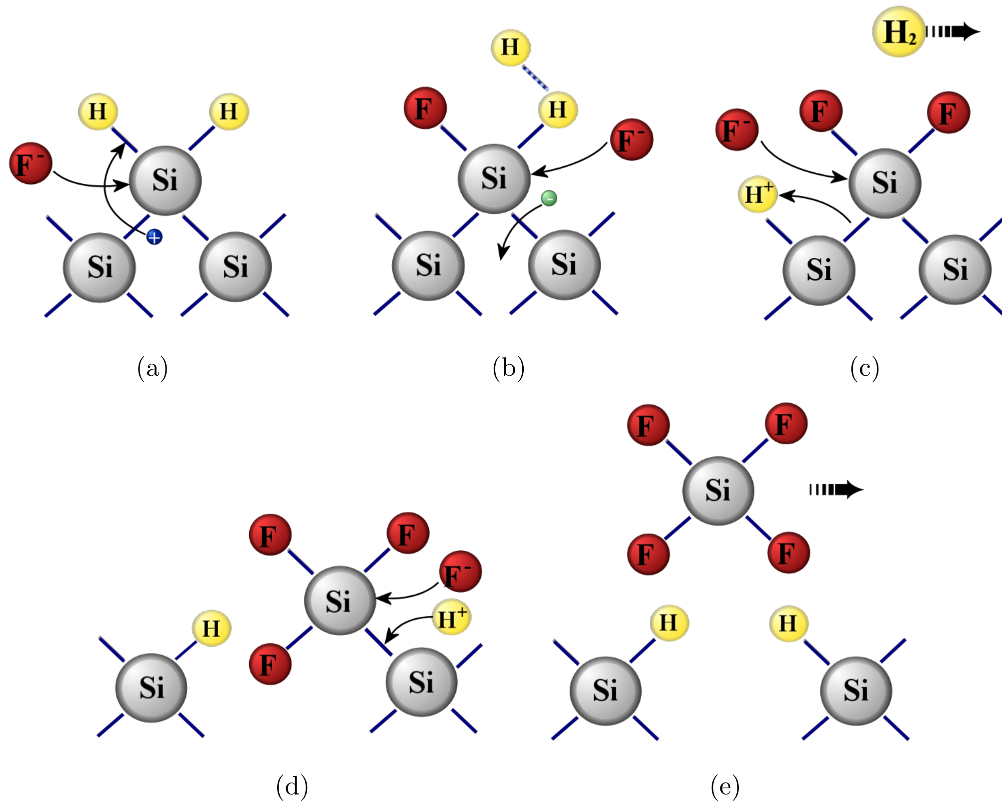


Fig. 3.14: Porous Si formation steps. (a) hole from bulk travels to electrolyte interface, Si-H bond is attacked by F^- ion (b) Si-H bond replaced with Si-F bond due to polarization of Si-F bond, another F^- ion attack occurs and electron is injected (c) releases H_2 and two Si-F bonds polarize Si back-bonds weakening bond strength (d) allows attack of HF or H_2O (e) product is SiF_4 which reacts with HF and produces bubbles, results in pit formation changing surface geometry and electric field distribution.

There have been limited attempts to form PS by stain etching [15]. The main advantage of electrochemical etching versus pure chemical etching is the increased control over the pore morphology due to more externally controllable parameters. However, stain etching of PS has also displayed electroluminescent properties and benefits from process simplicity.

3.2.1.3 Modeling Parameters

Besides the chemical reactions discussed, other factors affect the formation of PS. Many models have been developed to help understand the limiting reactions that can exist in order to gain more insight into pore formation. Parameters such as the width of the space charge region, the pore tip radius, the diffusion lengths of carriers, etc. influence the geometry and morphology of pores [17]. However, it is not clear which effects dominate, and these mechanisms are also related which emphasizes the complexity for modeling the formation of PS. No single theory is close to a global description of the complex reactions and resulting morphologies of the Si surface in the formation of PS [80]. The theories that have been developed tend to have a limited scope of validity due to the numerous controllable parameters (current density, electrolyte composition, substrate type and doping, and illumination source).

Porosity

Porosity is defined as the fraction of voids within the PS layer and is destructively determined by weighing the sample before (m_1) and after (m_2) anodization, and after removal of the PS layer (m_3) [15]:

$$Porosity = \frac{m_1 - m_2}{m_1 - m_3} \tag{3.21}$$

Typically a weak KOH solution ($< 5\%$) is used to etch away the PS. Generally, 90% is the highest porosity that can be achieved before cracking due to large capillary stress associated with the evaporation of the solvent from the pores [15].

Layer Thickness

The PS film thickness is given by [15]:

$$d = \frac{m_1 - m_3}{\rho\, A} \tag{3.22}$$

where A is the area of the etched surface, and $\rho = 2.33$ g/cm^3, the density of Si. The

thickness can also be measured by measuring the step height with a profiler after the film is etched, but both methods are destructive.

Pore Morphology

Porous Si pore morphology can be classified in terms of pore orientation, fill of pores, branching, and depth variation. Pore size is the most commonly used parameter for characterizing morphology [80]. The average pore sizes are classified as: micropores (< 10 nm), mesopores (10-50 nm), or macropores (> 50 nm). Reported dimensions can range from 1 nm to 10 μm, and the structure can vary from sponge-like to perfect cylindrical-shaped pores [17].

Electrical Properties

The effective resistivity of PS can be approximated by a volumetric expression [82]:

$$\rho_{eff} = \frac{\rho}{(1-P)\ g_0} \tag{3.23}$$

where P is the porosity, ρ is the resistivity of the Si substrate, and g_0 is the percolation strength of the Si network [83]:

$$g_0 = (1-P)^2 \tag{3.24}$$

The effective dielectric constant of PS is approximated by [84]:

$$\epsilon_{r,PS} = \epsilon_{r,Si}\ (1-P) + \epsilon_{r,air}\ P \tag{3.25}$$

Another method for estimating the dielectric constant of PS based on Bruggeman's equation [84]:

$$(1-P)\ \frac{\epsilon_{r,Si} - \epsilon_{r,PS}}{\epsilon_{r,Si} - 2\epsilon_{r,PS}} + P\frac{\epsilon_{r,air} - \epsilon_{r,PS}}{\epsilon_{r,air} - 2\epsilon_{r,PS}} = 0 \tag{3.26}$$

3.2.2 Film Characterization and Results

3.2.2.1 Stain Etching

Experimental work was carried out to form PS by stain etching of p-type <100> 8-12 Ω cm c-Si wafers. The c-Si substrates were etched in $HF:HNO_3:H_2O$ = 1:5:10 solution, but after 15 min nothing was observed. So a solution of $HF:HNO_3$ = 19:1 was used and the c-Si substrate was immersed for 60 s and vigorous etching occurred. From scanning electron microscope (SEM) analysis, the pore sizes could not be resolved as they are in the range of 1 nm and the thickness of the PS layer determined by Eqn. (3.22) is less than 100 nm (Table 3.3). As warned by researchers, stain etching is a difficult process for forming thick and uniform PS films.

Table 3.3: Experimental results of stain etching c-Si. The trial runs were unsuccessful for our application which requires thick porous Si layers.

$HF:HNO_3$	Time (s)	Pore size (nm)	Avg. Thickness (nm)	Observations
1:5	900	–	–	No visible etching
19:1	60	< 1	< 100	Vigorous etching and bubbling

3.2.2.2 Electrochemical Etching

Based on the schematic in Fig. 3.15, a single wafer Teflon etch cell was machined for the electrochemical etching of porous Si and photographs are shown in Fig. 3.16. P-type <100> 8-12 Ω cm c-Si wafers were used for electrochemical etching. Prior to processing, samples were weighed on a Mettler microgram balance. The electrolyte for the anodization of Si is composed of $HF:C_2H_5OH$ (ethanol) mixture and a power supply provides the constant current source between the Pt and Si electrodes. The exposed area of the Si to the electrolyte is 12.6 cm^2. After etching, the samples were weighed and then the PS was etched in 1% KOH and weighed again to determine the porosity and thickness of the film.

The experimental results of electrochemically etching of p-type c-Si are displayed in Table 3.4. The samples were anodized for 20 min and the porosity and thickness were determined gravimetrically. The effective dielectric constant and substrate resistivity were

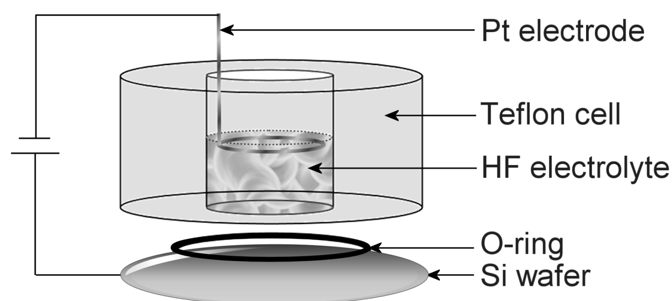
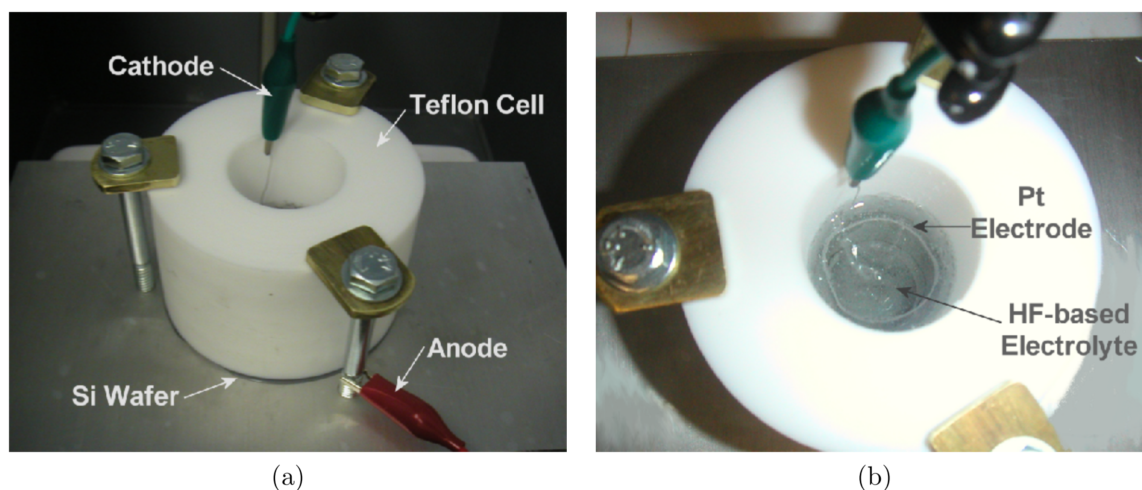


Fig. 3.15: Schematic of a single wafer etch cell.



(a) (b)

Fig. 3.16: (a) Photograph of Teflon etch cell machined in this study for the formation of PS and (b) showing the Pt electrode and HF electrolyte.

estimated based on Eqn. (3.25) and (3.23). For increasing current density and constant HF concentration, the porosity increases; and for increasing HF concentration and constant current density, the porosity also increases. These experimental values are reported in detail elsewhere [15].

The thickness of a PS layer etched with 12.5% HF and 1 mA/cm^2 for 45 min is shown in Fig. 3.17 (these parameters are adpoted for the fabrication of planar inductors in the next chapter). The transition between the bulk c-Si and PS is clearly visible from this cross-section. The branching of the pores is dense with short, random branches.

Table 3.4: Experimental results of electrochemical etching of c-Si for 20 min carried out in this research.

HF concentration	**Current density (mA/cm^2)**	**Porosity**	**Avg. Thickness (μm)**	**Effective dielectric constant**	**Effective resistivity (Ω cm)**
10%	10	66%	11.3	4.7	3.8×10^2
10%	20	90%	14.3	2.1	1.5×10^4
20%	10	85%	9.73	2.6	4.4×10^3

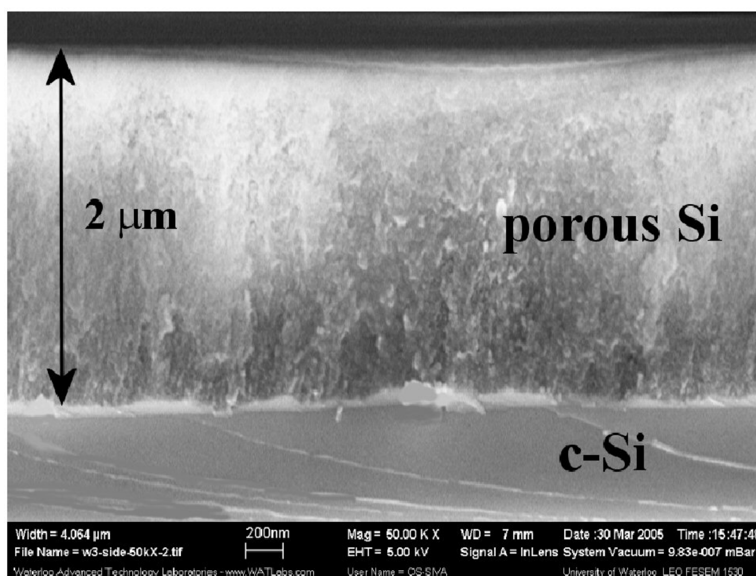
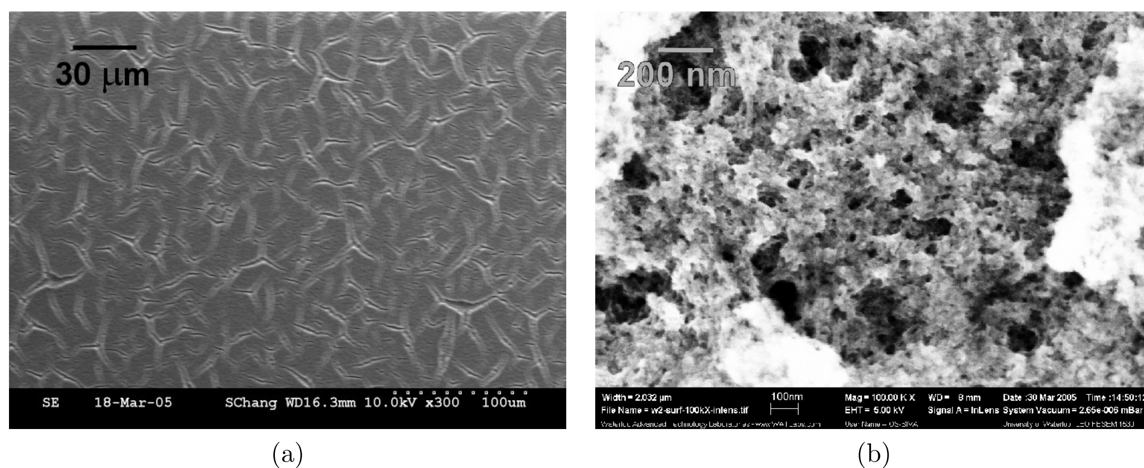


Fig. 3.17: SEM of PS formed from p-type <100> 8-12 Ω cm c-Si with 25% HF concentration and 1 mA/cm^2 current density for 45 min. The transition between PS and c-Si is obvious with an average PS thickness of 2 μm, viewed at 50k×.

SEM analysis was carried out to study the different surface morphologies and to estimate the average pore size of the PS layers. Porous Si was formed by etching p-type <100> 8-12 Ω cm c-Si with 12.5% HF concentration and 20 mA/cm^2 currenty density. From Fig. 3.18(a), the PS film is cracked, but with higher magnification, the pore sizes are estimated to be between 10-50 nm as shown in Fig. 3.18(b). The surface morphology is sponge-like and from may not withstand further processing. After taking SEM images, the PS layer was removed in 1% KOH for 60 s and the cross-section of the interface between

the PS and the c-Si is shown in Fig. 3.19. The edge is rough which can be expected for a process with a fast removal rate, however removing the PS layer is only required to determine the porosity and thickness.



(a) (b)

Fig. 3.18: PS formed from p-type <100> 8-12 Ω cm c-Si with 12.5% HF concentration and 20 mA/cm^2 currenty density, viewed at (a) 300× and (b) 100k×.

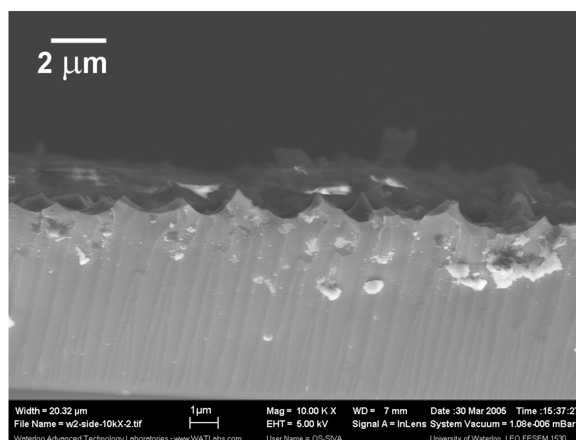
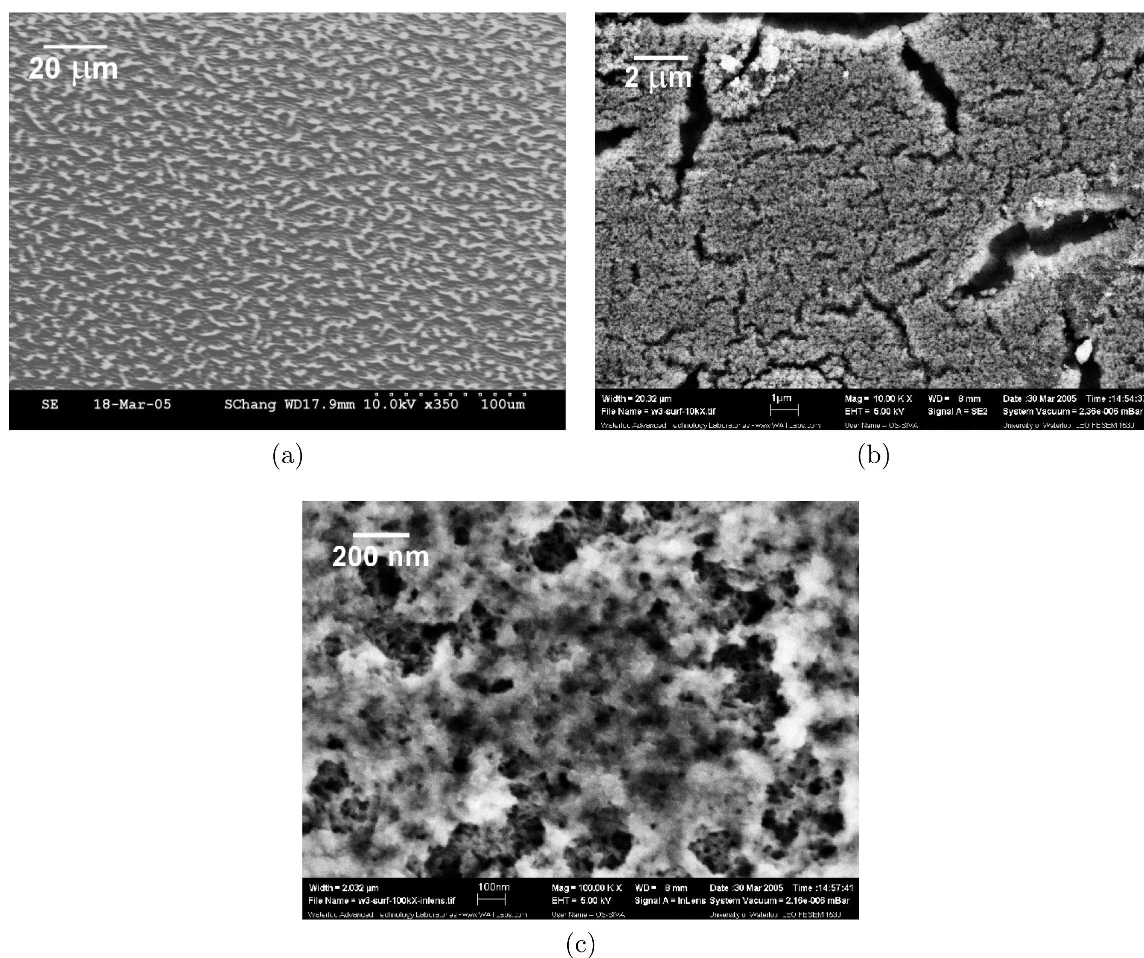


Fig. 3.19: Border between PS and c-Si after etching the layer, viewed at 10k×.

A different surface morphology is observed when the current density is increased from 20 to 40 mA/cm^2 as shown in Fig. 3.20(a). However, with an increased magnification,

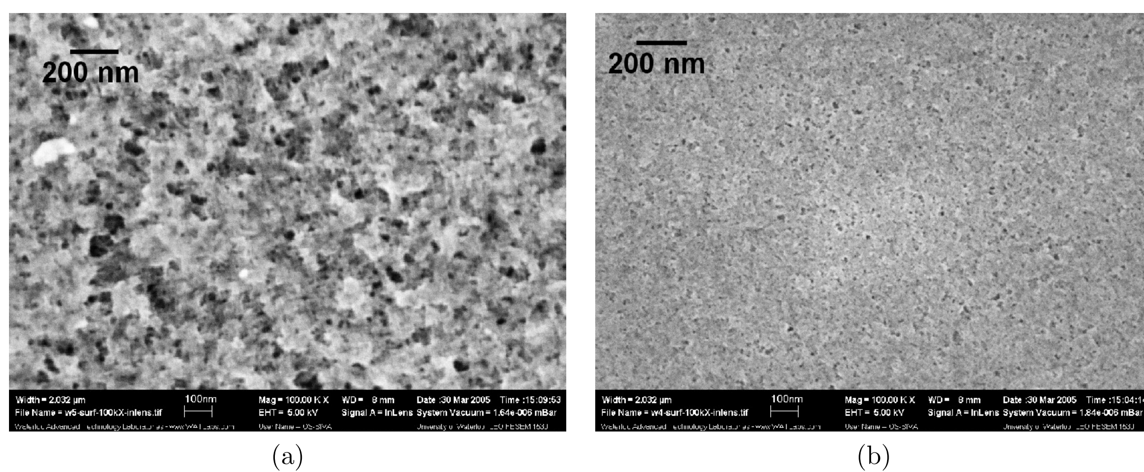
there are some cracks in the PS film with 1 μm gaps shown in Fig. 3.20(b). The pore size can be determined with 100k× magnification and are estimated to range from 50-100 nm (Fig. 3.20(c)). By comparing Fig. 3.18(b) and Fig. 3.20(c), when the PS layer is analyzed under the highest magnification, the pore morphology is similar. However, longer cracks are observed in the PS layer etched with a lower current density of 20 mA/cm^2. Nonetheless, from these SEM images, depositing films over the cracked PS layer would result in a low yield for multi-layer devices.



(a) (b) (c)

Fig. 3.20: PS formed from p-type <100> 8-12 Ω cm c-Si with 12.5% HF concentration and 40 mA/cm^2 current density, viewed at (a) 350×, (b) 10k× and (c) 100k×.

It was observed that electrochemical etching with 12.5% HF resulted in cracks throughout the PS layer. Figure 3.21 shows the surface morphology of two different HF concentrations with constant current density. With 12.5% HF and 5 mA/cm^2, the pore sizes are less than 10 nm as shown in Fig. 3.21(a). When the HF concentration is cut in half to 6.25%, the pore sizes increase and range from to 10 to 50 nm as shown in Fig. 3.21(b).



(a) (b)

Fig. 3.21: PS formed from p-type <100> 8-12 Ω cm c-Si with 5 mA/cm^2 current density and HF concentration of (a) 12.5% and (b) 6.25%, viewed at 100k×.

From the SEM images presented, it can be seen that it is difficult to control the porosity and pore sizes of PS layers. High aspect ratio, cylindrical pores are reported in literature, but in our experimental work, both the HF concentration and applied current density were varied, and resulted in randomly oriented pores. The formation of PS is known to suffer from repeatability issues being a wet etching process.

Electrochemical etching can also be used to identify defects at the surface. In a trial run, there was a particle on the surface of the Si wafer that initiated vigorous etching with hydrogen bubble formation (Fig. 3.22). This is another application of electrochemical etching of PS for defect mapping. In an electrolyte, the chemical reaction caused by the current through the defect can be sensed and initiates etching [23].

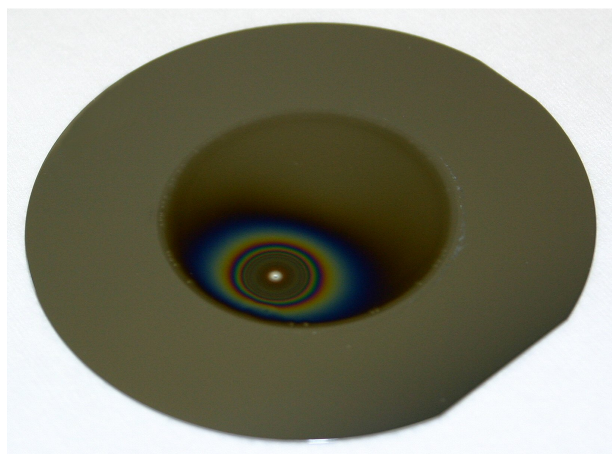


Fig. 3.22: Photograph of electrochemical etching of c-Si with a particle defect on the wafer surface.

3.2.3 Summary

In this chapter, the development of the deposition and dry etching of a-Si:H films processed in the CIRFE lab are reported. The dielectric constant is calculated from CV measurements and found to be 11.7. The loss tangent was extracted from CPW lines on different thicknesses of a-Si:H films and is estimated to be close to that of c-Si, 0.05 at 4 GHz. The dark and photoconductivity of our undoped films was determined by IV measurements and were calculated to be 1×10^{-10} S/cm and 1×10^{-6} S/cm respectively. The optical bandgap has also been verified to be 1.72 eV. The chemical reactions for forming porous Si were summarized and both stain etching and electrochemical etching for forming PS were explored. It was found that the electrochemically formed films with our machined etch cell produced thicker PS material ideal for the application of the isolation of RF devices from the c-Si substrate. SEM images are shown to distinguish the variation in HF concentration of the electrolyte and the applied current density. In the next chapter, planar inductors are built on these amorphous Si and porous Si films.

Chapter 4

Planar Inductors built on Low Temperature and Low Loss Films on Si

A low resistivity Si substrate is a cost-effective solution for RFICs, but it is a major source of energy loss and limits the performance of integrated passive devices. In order to improve the high frequency performance of an inductor on Si, the isolation layer the inductor lies on can be improved. Conventionally, oxide is the dielectric used to separate the metal coil and the lossy Si substrate in commercial processes. However, stoichiometric SiO_2 requires high processing temperatures which place limits on integration. Oxides can be deposited at lower temperature, however these films suffer from porosity issues and are of low quality. In addition, if the thickness of the isolation layer is increased to improve the performance of an inductor, the resulting Q would increase, but this introduces film stress as a crucial factor. One of the main components which contribute to the overall stress is the large difference in the thermal expansion coefficients of conventional dielectrics such as SiO_2 and Si_3N_4 with Si [85]. In this chapter, planar inductors fabricated on low loss and low temperature films are presented.

4.1 Design of Planar Inductors on Silicon

The formation and material characterization of low temperature and low loss materials presented in the previous chapter are applied to the fabrication of planar inductors on low resistivity Si. The compact model of a planar inductor on Si was introduced in Chapter 2. The device layout parameters optimized in the design stage and the tradeoffs with performance are addressed in this section.

4.1.1 Basic Structure

The basic structure of a planar inductor is composed of a metal coil and a metal underpass or overpass to access the inner turn. Figure 4.1(a) is a cross-section and Fig. 4.1(b) is a top view schematic of a planar inductor with an underpass designed in this section. The substrate (SUB) in our study is low-resistivity p-type <100> 8-12 Ω cm c-Si and both amorphous Si and porous Si are explored as the DIEL_1 layer to improve the isolation of the inductor from the Si substrate. For the fabricated devices, sputtered Al is used as the metal layers (MET_1 and MET_2).

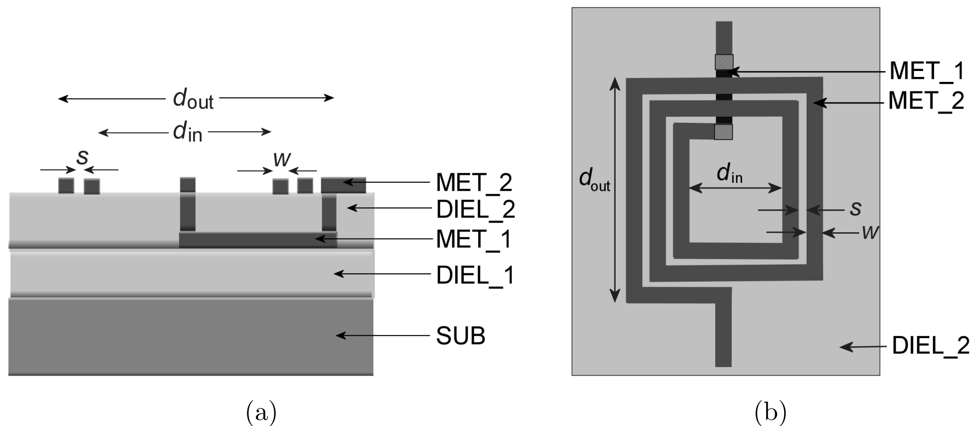


Fig. 4.1: Schematic (a) cross-section and (b) top view of a planar inductor. The substrate (SUB) in our study is p-type <100> 8-12 Ω cm c-Si and both amorphous Si and porous Si (DIEL_1) are explored to improve the isolation of the inductor from the Si substrate.

4.1.2 Design Parameters

The tradeoffs of the design parameters of an inductor namely, the number of turns, n, the separation distance between windings, s, the width of the metalization, w, the thickness of the metalization, t, and the thickness of the isolation layer underneath the spiral, h, are summarized based on the results of Sonnet simulations [86] that were performed. These guidelines are taken into account during design and layout stages. The equations presented in Chapter 2 to estimate the compact model parameters are also useful for improving the performance of planar inductors. ASITIC [87] is another tool that can be used during the early design stages of planar inductors.

Number of Turns

The inductance value increases when the number of turns increases. However, this increase is not linear, as the area of the inner windings is much smaller compared to the outer windings when the outer size of the spiral is kept constant. The f_{res} decreases with each added winding because the capacitive coupling between the metal winding and the substrate increases. The peak Q also decreases as the number of windings increases because of the increased metal losses compared to the increase in inductance. Therefore, designing the number of turns of an inductor depends on whether the application calls for a high inductance value or a high Q.

Separation between Windings

As the separation between windings increases, the inductance decreases as the diameter of the inner spiral decreases when the overall size of the inductor is kept constant. The capacitive coupling between adjacent windings decreases and therefore, increases the f_{res}. The peak Q increases slightly as the separation between windings increases, but is not as sensitive as the decrease in inductance.

Width of Windings

As the width of the metal windings increases, the inductance decreases due to the smaller diameter of the inner loop when the overall size of the inductor is kept constant. The

f_{res} also decreases because of the increased capacitive coupling between the spiral and the substrate as the overlapping area has increased. However, the series resistance decreases as the width increases which improves the Q.

Thickness of Metal

As a rule of thumb, the thickness of the metal should be at least two times greater than the skin depth at the desired operating frequency in order to minimize the series resistance as shown in Eqn. (2.9). Increasing the thickness of the metal increases the Q and f_{res} is independent.

Thickness of Isolation Layer

At low frequency, a change in the thickness of the isolation layer underneath the inductor does not vary the inductance since the performance is not limited by the losses in the substrate. However, due to the capacitive coupling effects and the increased losses in the Si substrate, Q and f_{res} decrease as the dielectric thickness decreases. This is why there is a desire to fabricate the inductor as far away as possible from the conductive substrate; however, this increases the fabrication complexity and can introduce other factors such as stress. This concept is used in Chapter 6 where air is introduced in between the inductor and the substrate by surface micromachining techniques.

The general trends of the design parameters observed from the simulations carried out in Sonnet are summarized in Table 4.1. These observations are useful for the initial design of planar inductors and also shows the performance tradeoffs.

Table 4.1: General trends of inductor design parameters.

Design Parameter	**Change**	L	Q	f_{res}
number of turns, n	↑	↑	↓	↓
separation between windings, s	↑	↓	↑	↑
width of metal, w	↑	↓	↑	↓
thickness of metal, t	↑	unchanged	↑	unchanged
thickness of isolation layer, h	↑	unchanged	↑	↑

4.1.3 Film Thicknesses

The film thicknesses of the dielectric and metal layers were determined by simulations and by taking into account the fabrication yield of the planar inductors.

Metal Thicknesses

Due to the skin effect, the thicker the metalization, the better the RF performance of the inductor. Referring to Fig. 4.1(a), the thickness of MET_1 and MET_2 were varied in Sonnet simulations. The simulated numerical values are not of great importance, as the inductor dimensions are arbitrary, instead the relative trends are addressed. According to Fig. 4.2, it was found that increasing MET_1 from 0.1 to 0.5 μm did not bring any improvement in Q. Also the curves showing an increase in MET_1 from 0.1 to 1 μm only showed moderate improvement in performance. This shows that the thickness of the MET_1 layer which forms the underpass does not need to be maximized which is ideal for planarization issues of subsequent layers. When MET_2 is increased from 1 to 2.5 μm, the Q showed a large increase from 5.9 to 13.7. The thickness of this layer can be restricted by the chosen deposition method and a reasonable deposition time. So for the inductors fabricated in this chapter, the metal layers are chosen to be sputtered Al and MET_1 = 0.5 μm and MET_2 = 2 μm.

Dielectric Thickness

It is known that the thicker the dielectric layers, the better the RF performance of an inductor. However, with thin dielectric films, mechanical film stress is often an issue for thick films. The stress in a-Si:H is measured in Chapter 5 to explore the opportunities of using a-Si:H in the area of MEMS. As shown in Fig. 4.3(a) and (b) the Q increases as the a-Si:H film increases. However, by observing the curves labeled DIEL_1, 2 = 1, 3 μm in Fig. 4.3(a) and DIEL_1, 2 = 3, 1 μm in Fig. 4.1(b), the coil is the same distance from the Si substrate, however, a higher Q is given when DIEL_1 is the thicker film. However, the decrease in thickness of the DIEL_1 layer gives an increase in parasitic capacitance between the coil and the underpass which will decrease f_{res}. Moreover in terms of fabrication yield, the thinner DIEL_1 is, the better the sidewall coverage of the

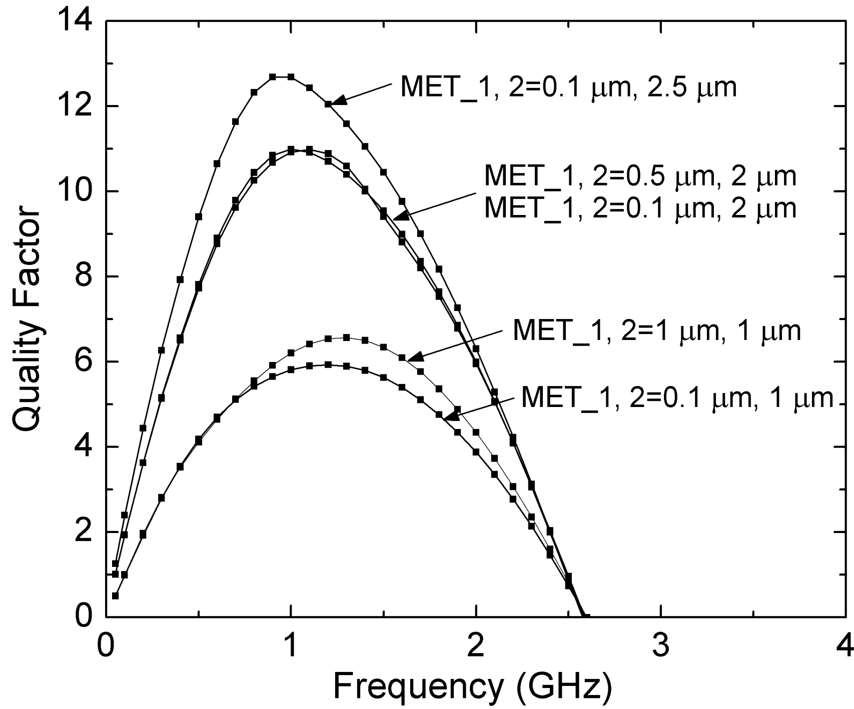
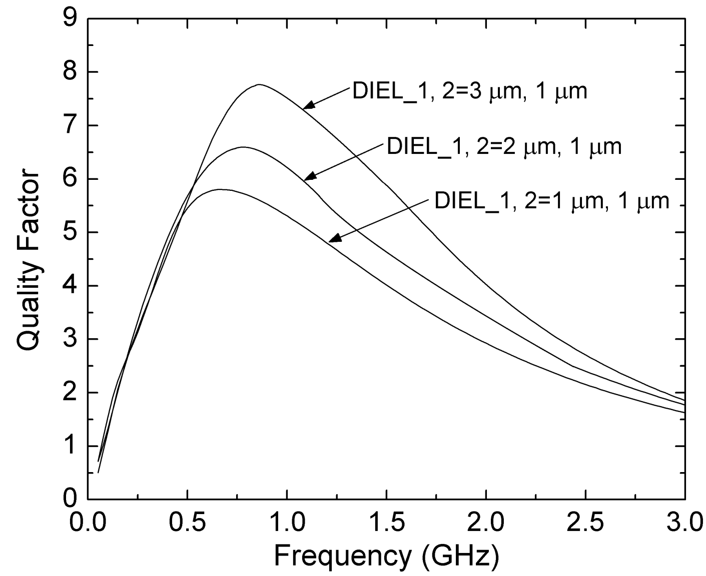
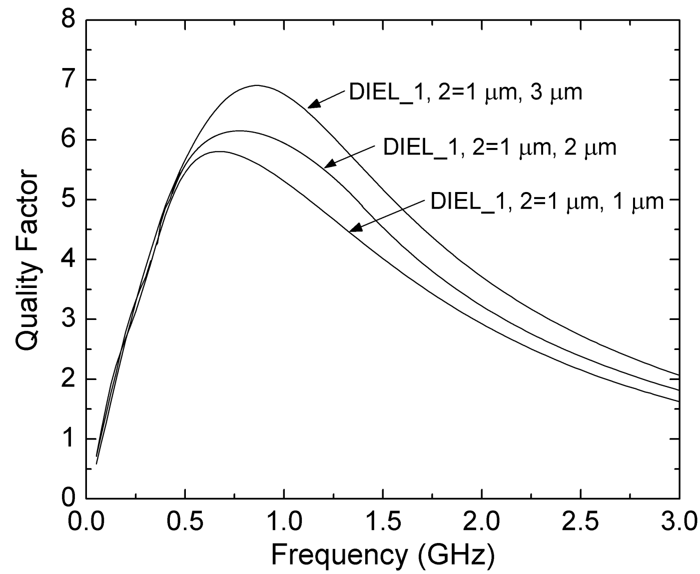


Fig. 4.2: Quality factor versus thickness of MET_1 and MET_2 layers. Simulations were carried out on c-Si substrate with 10 Ω cm resistivity, with DIEL_1 and DIEL_2 set to 1 μm a-Si:H and inductor dimensions of $n = 2$, $w = 50$ μm, $s = 20$ μm, and $d_{out} = 80$ μm.

vias would be. Having addressed these general tradeoffs, the DIEL_1 and DIEL_2 layers are maximized for RF performance without introducing stress as an issue. Intrinsic a-Si:H is deposited by PECVD for the dielectric layers with DIEL_1 = 1.5 μm and DIEL_2 = 1.5 μm. For these simulations, MET_1 = 1 μm and MET_1 = 2 μm were kept constant, which can be seen by the same slope of the traces at low frequency.



(a)



(b)

Fig. 4.3: Quality factor versus conductivity of (a) different DIEL_1 thicknesses and (b) different DIEL_2 thicknesses. Simulations were carried out on c-Si substrate with 10 Ω cm resistivity, with MET_1 and MET_2 set to 1 μm Al and inductor dimensions of $n = 2$, $w = 50$ μm, $s = 20$ μm, and $d_{out} = 80$ μm.

Amorphous Silicon Conductivity

The initial characterization of our a-Si:H films is described in the previous chapter. However, for the application of planar inductors, simulations were carried out to determine if further film optimization was required. Recall the light-induced properties of a-Si, our films have a measured photoconductivity of 1×10^{-6} S/cm and a dark conductivity of 1×10^{-10} S/cm. Planar inductors on Si were simulated in Sonnet with 1 μm a-Si:H as DIEL_1 and DIEL_2 layers, and 1 μm Al as MET_1 and MET_2 layers in Fig. 4.1. Even though these devices would ultimately be packaged, the influence of the conductivity on the peak Q is displayed in Fig. 4.4. It was found that as long as the conductivity of the dielectric layers is less than 10^{-4} S/cm, the peak Q is near its maximum for the given dimensions. Therefore, further optimization of the dark conductivity ($\sigma_{dark} = 1\times10^{-10}$ S/cm) is not a priority.

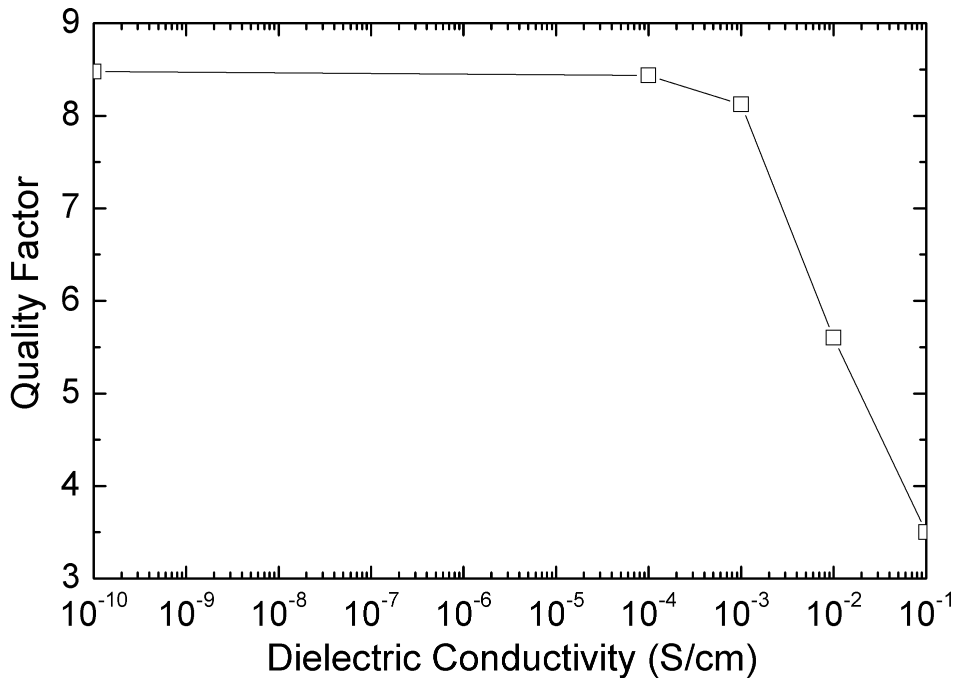


Fig. 4.4: Quality factor versus varying conductivities of 1 μm DIEL_1 and DIEL_2 and 1 μm Al as MET_1 and MET_2. Simulations were carried out on c-Si substrate with 10 Ω cm resistivity and inductor dimensions of $n = 2$, $w = 50$ μm, $s = 20$ μm, and $d_{out} = 80$ μm.

4.1.4 Design Rules

Various inductors were designed with different layouts and dimensions based on the design rules established in Table 4.2. The DIEL_1 and DIEL_2 film thickness were set to 1.5 μm because stress issues were not observed and the films are obtained in a reasonable deposition time. In the last section of this chapter, porous Si is also explored as the DIEL_1 layer in addition to the 1.5 μm of a-Si:H. The metal layers should be maximized in order to reduce losses due to the skin effect (Section 2.3.1.2). The MET_1 layer was set to 0.5 μm to avoid planarization issues in the subsequent layers. The MET_2 layer was set to 2 μm to reduce the series resistance in the metal.

Table 4.2: Design rules for the fabrication of planar inductors in this work.

Mask #	**Mask layer**	**Min. width (μm)**	**Min. spacing (μm)**	**Min. Enclosure (μm)**
	DIEL_1			
1	MET_1	20	10	20
2	DIEL_2	20	20	
3	MET_2	20	10	20

4.2 Planar Inductors on Amorphous Silicon

After designing planar inductors in a two mask process, emulsion masks were fabricated in-house [88]. The first fabrication run of planar inductors was built on a-Si:H thick films.

4.2.1 Device Fabrication

Figure 4.5 shows the step-by-step process flow of a planar inductor. In Fig. 4.5(a), the devices in this section are fabricated on low resistivity p-type <100> 8-12 Ω cm c-Si. The wafers are cleaned in a standard RCA 1 solution and then dipped in 1% HF prior to processing (Fig. 4.5(a)). In Fig. 4.5(b), a blanket a-Si:H film is deposited by PECVD with the process conditions listed in Table 3.1 for a thickness of 1.5 μm. Then 0.5 μm of Al is sputtered and patterned with the first mask. The MET_1 layer is wet etched

in PAN solution and serves as the underpass of the inductor as shown in Fig. 4.5(c). In Fig. 4.5(d), another 1.5 μm thick a-Si:H film is deposited and patterned to form vias to access MET_1 and dry etched with the process conditions listed in Table 3.2 (Fig. 4.5(e)). Then in Fig. 4.5(f) the MET_2 layer is composed of 2 μm of sputtered Al and in the final step, Fig. 4.5(g), it is patterned and wet etched to form the inductor coil and contact pads.

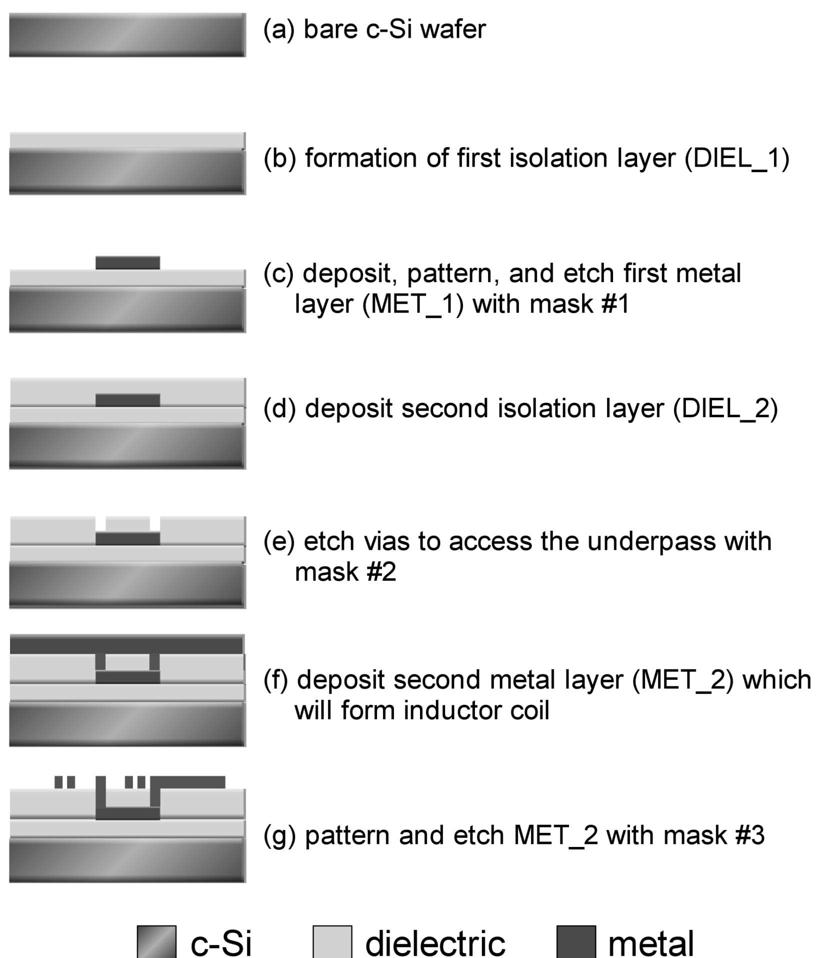


Fig. 4.5: Process flow of planar inductors fabricated in this research (3 mask process). In this section, a-Si:H thick films are used as DIEL_1 and DIEL_2, and sputtered Al serves as MET_1 and MET_2.

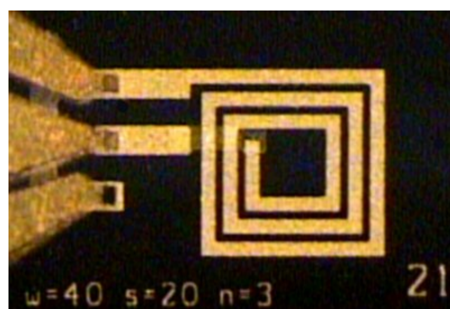
4.2.2 Results and Discussion

Planar spiral inductors with various dimensions and layouts were fabricated with a-Si. Figure 4.6 are micrograph images of a square and helix inductor fabricated in the CIRFE lab. The 1-port S-parameters were measured from 0.5 MHz to 20 GHz with an Agilent 8510 network analyzer and Cascade Microtech coplanar GSG probes. The parasitic effects of the probe pads were de-embedded with an open test structure and the inductance (Eqn. (2.21)) and quality factor (Eqn. (2.22)) are extracted from the input impedance.

Various inductor layouts were designed and fabricated and the measured performance is listed in Table 4.3. Some general trends in the design of planar inductors can be observed. As the number of turns is increased, L increases, but Q suffers due to the added series resistance, and f_{res} decreases due to the added coupling capacitance. When the width of the metal is increased and the outer diameter is kept constant, L decreases due to negative mutual coupling as the inner diameter shrinks. However, the series resistance decreases with increasing width, so Q increases. As the spacing between windings is increased and the other dimensions are kept constant, the capacitive coupling between windings decreases and therefore, increases f_{res}. These conclusions drawn from the experimental results are consistent with the simulation results discussed in Section4.1.2.

Table 4.3: Dimensions and measured performance of planar inductors on c-Si with a-Si:H as the dielectric layer fabricated in this work.

#	**layout**	$\boldsymbol{n}$	$\boldsymbol{w}$ **(μm)**	$\boldsymbol{s}$ **(μm)**	$\boldsymbol{d_{out}}$ **(μm)**	$\boldsymbol{d_{in}}$ **(μm)**	$\boldsymbol{Q_{max}}$	$\boldsymbol{L}$ **(nH)**	$\boldsymbol{f_{res}}$ **(GHz)**
1	square	2	30	10	300	160	8.2 at 3.7 GHz	1.6	20
2	square	2	50	10	500	280	7.1 at 1.6 GHz	2.7	10.2
3	square	2	60	10	500	240	7.3 at 1.5 GHz	2.3	10.6
4	square	4	30	20	500	140	5.9 at 1.1 GHz	6.2	6.8
5	circular	4	50	20	640	120	5.1 at 1.0 GHz	5.3	6.1



(a)

(b)

Fig. 4.6: Planar inductors fabricated in this work incorporating a-Si:H on c-Si (a) square ($n = 3$, $w = 40$ μm, $s = 20$ μm) and (b) helix ($n = 3$, $w = 40$ μm, $s = 20$ μm).

4.2.2.1 Influence of Thickness of Amorphous Silicon Layer

The positive influence of a-Si:H as the isolation material for an inductor on Si is verified by a controlled run with the DIEL_1 layer omitted. As shown in Fig. 4.7, the peak Q was measured to be 4.3 at 4.6 GHz for a 1.6 nH. By adding a 1.5 μm layer of a-Si:H prior to depositing the first metal layer, the Q improved by 56% at the same frequency. This increase in Q is observed for all of the devices listed in Table 4.3 regardless of device dimensions. Despite the high dielectric constant of a-Si, by increasing the distance between the inductor and the substrate, the losses coupled with the Si substrate is reduced. However, increasing the DIEL_1 film thickness introduces other concerns such as mechanical film stress in multi-layer processes. The stress in thick a-Si:H films is discussed in Chapter 5.

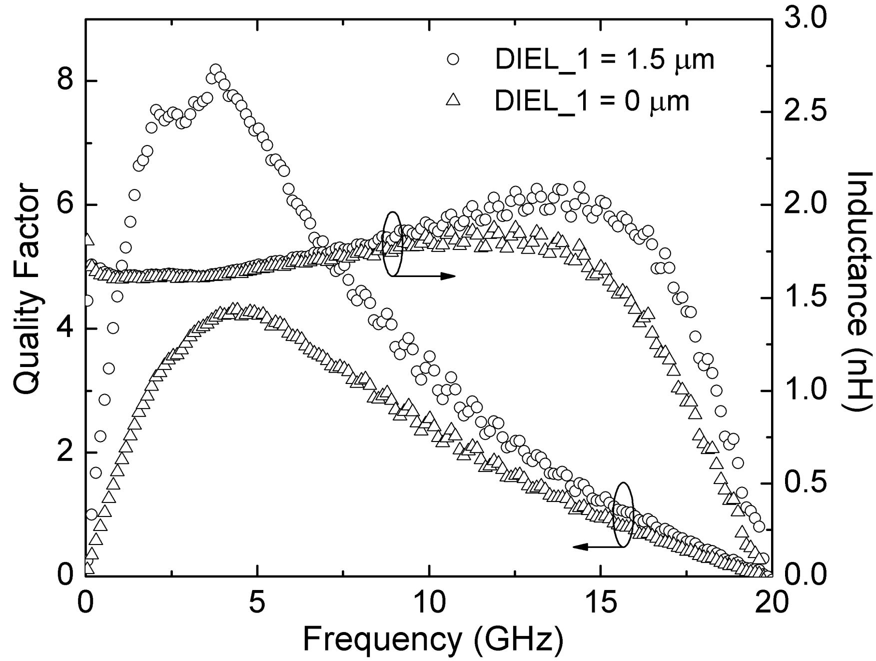


Fig. 4.7: Influence of thickness of a-Si:H layer (DIEL_1) on performance of a fabricated 1.6 nH inductor. By introducing 1.5 μm of thick a-Si:H film, the Q increased by 56%.

4.2.2.2 Influence of Conductivity of Amorphous Silicon Layer

It is well known that light incident on a-Si:H increases the conductivity. This photoconductivity is attributed to the optically excited carriers which contribute to the overall conduction in the bulk of the material. In the application of planar inductors, the photoconductivity leads to increased eddy current effects in the a-Si:H layer. In order to demonstrate the role of the conductivity in the PECVD a-Si:H films, devices were measured under illumination. There is a 16% decrease in Q when the S-parameters are extracted with illumination compare to in the dark (Fig. 4.8). Nonetheless, ultimately these devices would be packaged so the photoconductivity effect of a-Si:H can be neglected.

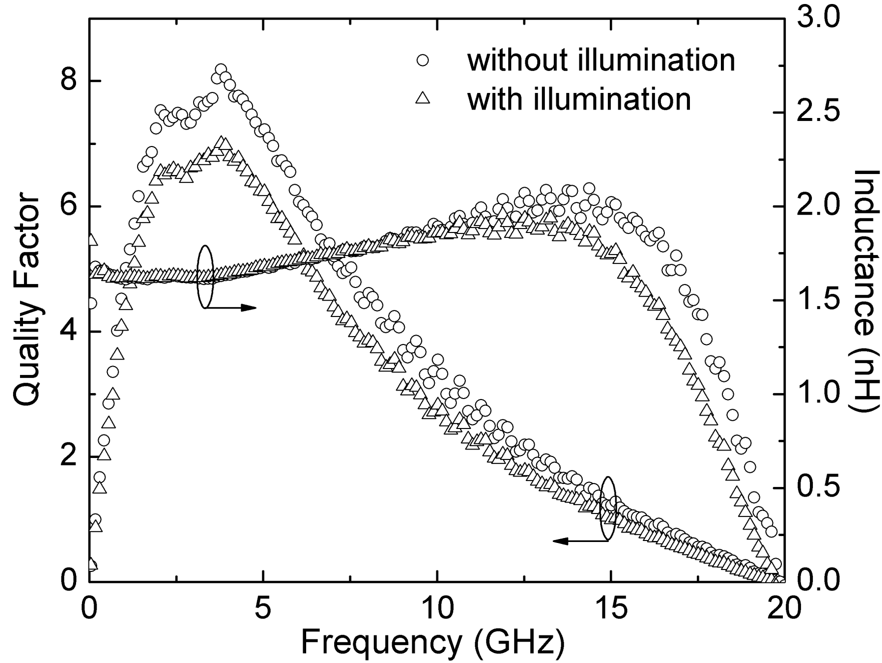


Fig. 4.8: Influence of light-induced conductivity of a-Si:H on performance of a fabricated 1.6 nH inductor. When the inductor is measured with illumination, there is a 16% decrease in Q.

4.2.2.3 Comparison of Compact Model, Simulation and Measurement Results

The parameters in the equivalent circuit model (Fig. 2.3) were extracted using the method described in [89]. The parameters Q and L calculated from this model are only valid at low frequency due to omitted effects such as eddy currents in the substrate. In addition, simulations were carried out in Sonnet taking into account the losses in the Al in addition to the losses in the a-Si:H and Si substrate. The measured results are in close agreement with the simulation results (Fig. 4.9).

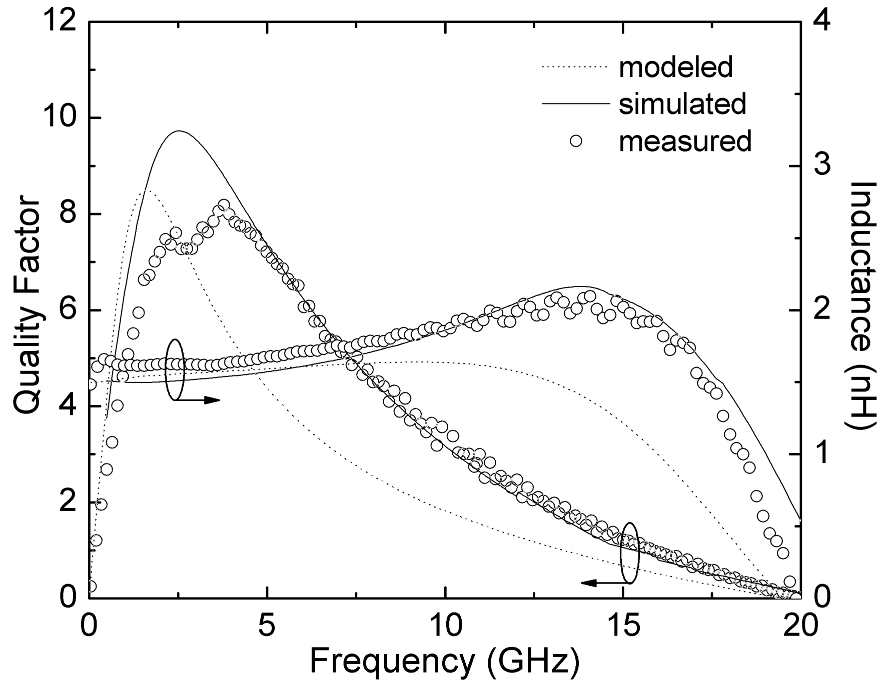


Fig. 4.9: Comparison between modeled, simulated and measured results of a fabricated 1.6 nH planar inductor. The simulation results accurately predict the performance, and the modeled results show the same trend at low frequency.

4.3 Planar Inductors on Porous Silicon

In order to further improve the performance of planar inductors on Si, porous Si is investigated to improve the substrate resistivity. However, as mentioned in the previous chapter, PS requires a capping layer to prevent further oxidation. Therefore, typically after forming PS an oxidation step is carried out at ∼1100℃ [90] which poses limitations and is outside the scope of our goal of integrating low temperature films. Another approach for fabricating inductors with PS is etching away the Si substrate and pasting the structure on a glass wafer [91]. This technique has limited applications, but gives some insight on the losses in the substrate. Table 4.6 summarizes some of these approaches. In this section, a-Si:H deposited by PECVD is used as a low temperature and high resistivity encapsulating

layer for PS to build planar inductors on top.

4.3.1 Device Fabrication

Planar inductors were fabricated on PS and a-Si:H films based on the structure depicted in Fig. 4.10. The fabrication process is similar to the steps outlined in Fig. 4.5 with an added step at the beginning of the process. The porous Si layer was electrochemically formed in 25% HF solution with two different applied current densities of 1 and 5 mA/cm^2 for 45 min. The electrolyte is composed of a 1:1 rartio of 49% HF and ethanol which improves the wettability of Si and allows the solution to penetrate the pores.

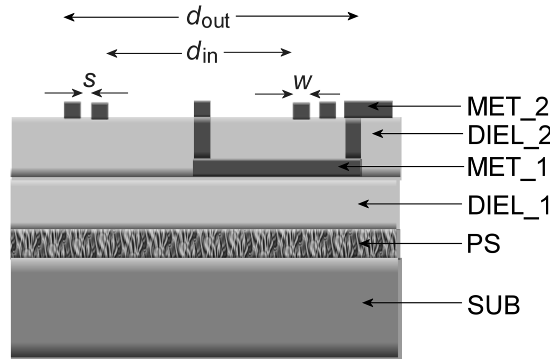


Fig. 4.10: Schematic cross-section of planar inductor incorporating PS in a two metal layer fabrication process. Amorphous Si is used as DIEL_1 layer to encapsulate the PS layer.

The porosity and thickness of the layers are determined gravimetrically by Eqn. (3.21) and Eqn. (3.22) and are listed in Table 4.4. As expected, the porosity increases as the current density increases with constant HF concentration. For the same anodization time, the higher current density results in a thicker PS layer. From SEM analysis, it was found that the size of the pores for both samples ranged from 10-20 nm as shown in Fig. 4.11. The transition from c-Si to PS is clearly visible in Fig. 4.12 where the branching of the pores is dense with short and random branches.

Table 4.4: Experimental parameters for forming PS by electrochemical etching of p-type <100> 8-12 Ω cm c-Si for 45 min and corresponding values of porosity and thickness determined gravimetrically.

Sample	HF concentration	Current density	Porosity	Thickness
1	25%	1 mA/cm^2	68%	2.2 μm
2	25%	5 mA/cm^2	77%	3.6 μm

To reduce oxidization, immediately following the formation of PS, 1.5 μm of PECVD a-Si:H is deposited. The fabrication process continues with step (b) in Fig. 4.5. The same film thicknesses are adopted from the inductors fabricated without a PS layer (DIEL_1 = 1.5 μm a-Si, MET_1 = 0.5 μm Al, DIEL_2 = 1.5 μm a-Si, MET_2 = 2 μm Al). A micrograph image of a fabricated inductor on PS is shown in Fig. 4.13.

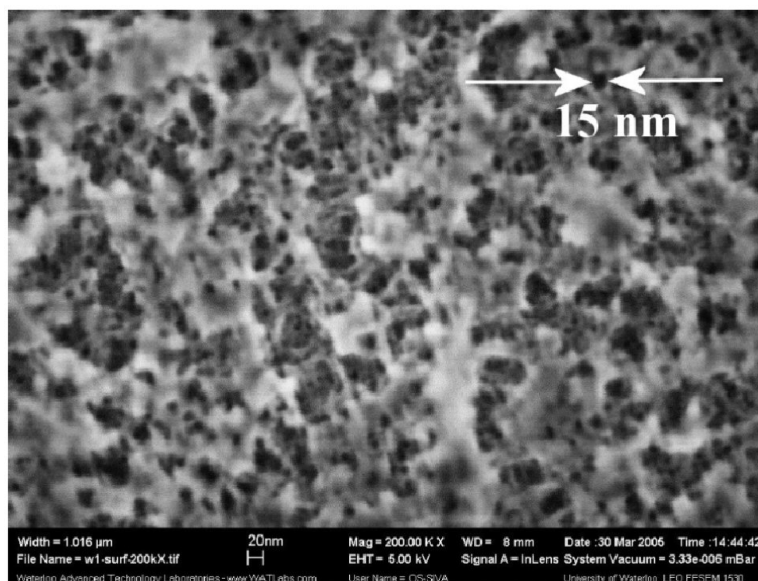


Fig. 4.11: SEM of PS formed from p-type <100> 8-12 Ω cm c-Si with 25% HF concentration and 1 mA/cm^2 current density for 45 min, pore sizes range from 10-20 nm, viewed at 200k×.

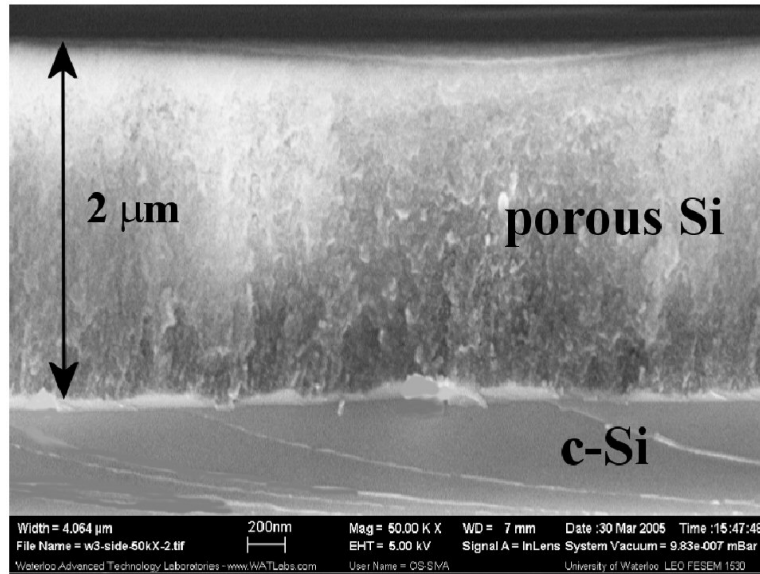


Fig. 4.12: SEM of PS formed from p-type <100> 8-12 Ω cm c-Si with 25% HF concentration and 1 mA/cm^2 current density for 45 min. The transition between PS and c-Si is clearly seen with an average PS thickness of 2 μm, viewed at 50k×.

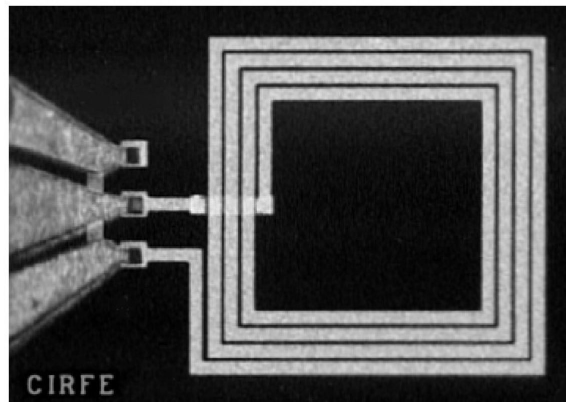


Fig. 4.13: Micrograph of an inductor on PS and a-Si:H thick film fabricated in this work ($n = 4$, $w = 40$ μm, $s = 10$ μm, $d_{in} = 600$ μm, $d_{out} = 1000$ μm).

4.3.2 Results and Discussion

The S-parameters of the inductors were measured from 0.5 MHz to 20 GHz with an Agilent 8510 network analyzer and Cascade Microtech coplanar GSG probes. The parasitic effects of the probe pads were de-embedded with an open test structure. The inductance and quality factor were extracted from the Z-parameters in Eqn. (2.21) and (2.22).

The fabricated inductors incorporating PS and a-Si:H were compared to the previously fabricated devices with the same dimensions, film thicknesses and process parameters but with the PS layer omitted. The influence of the PS layer on the RF performance of an inductor is shown in Fig. 4.14. The Q of a 1.6 nH inductor improved by 46.7% when 3.6 μm of PS (current density of 5 mA/cm^2) was incorporated beneath the first a-Si:H film (DIEL_1). At low frequency, the PS layer has little impact on Q because the energy dissipation of the inductor is dominated by the series resistance of the metal. The frequency at which the peak Q occurs increases, indicating that the PS layer improved the resistivity of the Si substrate by suppressing the substrate losses until a higher frequency of 6.4 GHz. As the frequency is further increased, the capacitance of the a-Si:H layer is effectively short-circuited and the substrate effects dominate and Q rolls-off at a lower frequency when PS = 0 μm. The inductance value with and without a PS layer is the same and constant in the useful operating range since the same device dimensions were used. The inductor with PS = 0 μm has a f_{res} of 20 GHz, while the inductor with PS = 3.6 μm has $f_{res} > 20\ GHz$ as seen from the Q and L traces in Fig. 4.14. The improvement in f_{res} is due to the increased effective capacitance of the Si substrate with the incorporation of a PS layer.

As shown in Table 4.4, the porosity and thickness of the PS layer can be adjusted by varying the applied current density. In Fig. 4.15, the thicker PS layer of 3.6 μm with 77% porosity (5 mA/cm^2) has 37.5% improvement in Q for a 1.6 nH inductor compared to 2.2 μm with 68% porosity (1 mA/cm^2) PS layer and $f_{res}$of both inductors is greater than 20 GHz. Similar to Fig. 4.14, the thicker PS layer with higher porosity suppresses the substrate effects as the frequency increases. If the thickness of the a-Si:H film (DIEL_1) is increased, the same improved trend in the roll-off of Q would be observed.

Electromagnetic simulations were carried out in Sonnet to approximate the effective substrate resistivity of the Si substrate incorporating the PS film. The 1.6 nH inductor

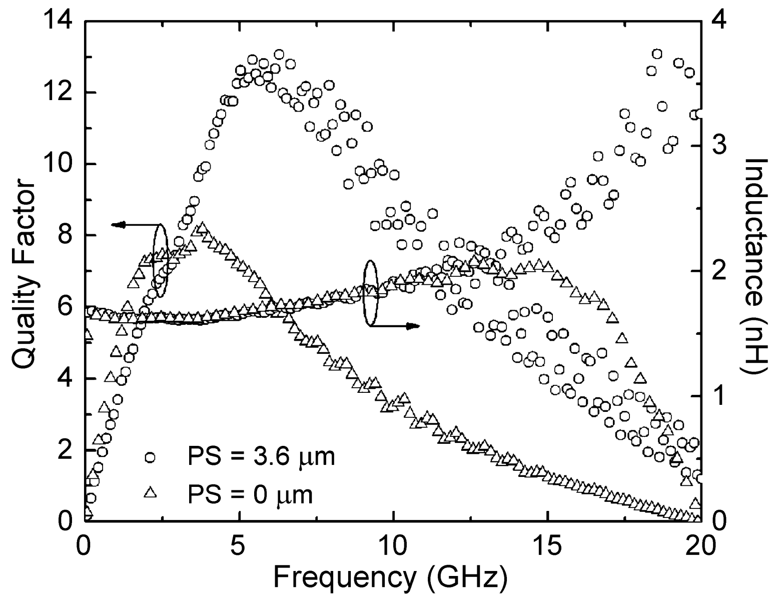


Fig. 4.14: Measured RF performance of a fabricated 1.6 nH inductor. A 46.7% improvement in Q is measured by incorporating a 3.6 μm with 77% porosity PS layer.

without a PS layer was simulated with the measured dimensions, film thicknesses and material properties and simulation results were in close agreement with experimental results. The Si substrate resistivity was varied and the peak Q was extracted and plotted in Fig. 4.16. As the substrate resistivity increases, the performance of the inductor improves. Based on the measured Q of the inductors incorporating PS with current densities of 1 and 5 mA/cm^2, the effective substrate resistivity is estimated to be 15 and 57 Ω cm, respectively, compared with the original Si resistivity of 8-12 Ω cm. These results indicate that PS increases the effective substrate resistivity and in turn, improves the Q of inductors on Si. In order to further increase the effective substrate resistivity, the thickness of the PS layer can be increased by prolonging the etch time. However, the porosity should be less than 90% because the film will be mechanically unstable and too fragile for device fabrication.

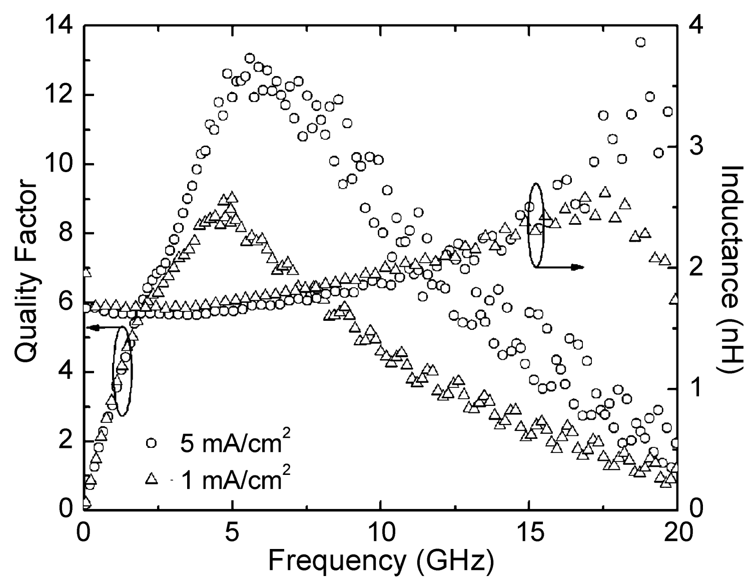


Fig. 4.15: RF performance of a fabricated 1.6 nH inductor showing the influence of applied current density for the formation of PS on the Q of the inductor.

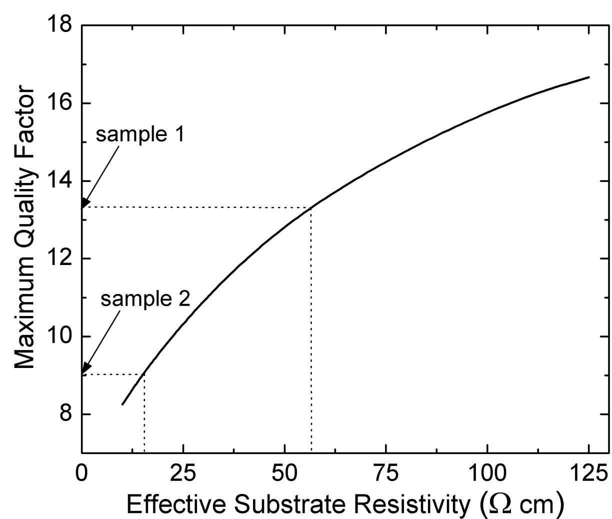


Fig. 4.16: Sample 1 (1 mA/cm^2) has an effective substrate resistivity of 15 Ω cm and sample 2 (5 mA/cm^2) is 57 Ω cm. The original c-Si substrate resistivity is 10 Ω cm.

4.4 Summary

In this portion of the research, a-Si:H and PS are investigated in a novel attempt to improve the isolation of planar inductors on Si. Two runs of planar inductors were fabricated on p-type <100> 8-12 Ω cm c-Si . The first run had 1.5 μm PECVD a-Si:H as the isolation layer separating the inductor and the Si and the Q improved by 56% compared to when the a-Si:H layer was omittted. The measured results are compared to other approaches for designing planar inductors and are listed in Table 4.5. Our results are comparable to inductors fabricated in commercial processes, moreover, these devices are fabricated in a sub 250℃ process. The second fabrication run presented in this chapter incorporated a 3.6 μm PS layer encapsulated by 1.5 μm a-Si:H. By adding the PS layer, the isolation of useful energy from the substrate increases and the Q improved by 47%. These results are listed in Table 4.6 in comparison with other approaches reported in literature. Again, the planar inductors presented in this work have the added advantage of being fabricated in a low temperature process while showing comparable performance to other designs reported in literature.

Table 4.5: Comparison of some planar inductors reported in literature compared to this work.

Inductor Type	Q_{max} **at freq.**	L	f_{res}	**Dimensions**	**Reference**
Multi-metal layers	9.3 at 2.4 GHz	2.1 nH	15 GHz	230 μm^2	Soyuer [52]
Patterned ground shield	6.8 at 2.0 GHz	7.4 nH	3.6 GHz	—	Yue [51]
Polygon spiral	6.7 at 4.9 GHz	3.0 nH	—	200 μm^2	Niknejad [92]
a-Si:H as isolation	8.2 at 3.7 GHz	1.6 nH	20 GHz	200 μm^2	This work

Table 4.6: Comparison of some planar inductors on PS reported in literature compared to this work.

Inductor Type	Q_{max} **at freq.**	L	f_{res}	**Temperature**	**Reference**
PS on glass	45 at 1.5 GHz	11.4 nH	1.6 GHz	—	Royet [91]
Oxidized PS	13 at 4.6 GHz	6.3 nH	13.8 GHz	1120℃	Nam [90]
PECVD oxide as cap	11 at 4.8 GHz	4.6 nH	13.4 GHz	—	Chong [93]
PECVD a-Si:H as cap	13 at 6.3 GHz	1.6 nH	$>$ 20 GHz	250℃	This work

In the next chapter, a-Si:H will be explored as a structural layer for MEMS applications. Even though PS showed improved RF performance, the films prove to be too fragile for building MEMS devices which require stacking thick films. The followings chapters will present MEMS devices incorporating low temperature a-Si:H films and the research on porous Si films will be exclusively applied to the planar devices presented in this chapter.

Chapter 5

Amorphous Si Thick Films for sub 150℃ MEMS Fabrication

Microelectromechanical systems is an enabling technology having a major impact on many industries. The electronics are fabricated using traditional IC processes, while the sensors and actuators are realized by micromachining techniques. Low temperature MEMS fabrication offers the added flexibility of system integration with CMOS technology making a-Si:H an interesting candidate because it can be deposited at low temperature and is easily integrated with low-cost Si-based IC fabrication processes.

Another rising concern in the reliability of MEMS is continuous sidewall coverage especially when large steps and complex 3-D structures are being introduced and integrated with thin film processes. Typical metal structural layers used in MEMS are deposited by physical vapor deposition (PVD) which is a relatively directional process compared to chemical vapor deposition (CVD). In this chapter, we have deposited a-Si:H at low temperature (150℃) and studied the film properties for feasibility for MEMS applications. We report on the design, fabrication and performance of the first thermal actuator incorporating a-Si:H as a structural layer.

5.1 Lowering a-Si:H Thick Film Deposition to 150℃

The favored method for depositing a-Si:H is by the plasma decomposition of silane (SiH_4). The energy from the plasma dissociates SiH_4 molecules and allows the substrate to remain at low temperature [94]. As shown in Fig. 5.1, three mechanisms are responsible for precursor transport to sidewall structures: direct transport, re-emission, and surface diffusion. Direct transport occurs when the flux arrives from the gas phase without colliding with other surfaces. Indirect methods include re-emission and surface diffusion due to a low sticking coefficient allowing precursors to reach areas less accessible to the direct flux.

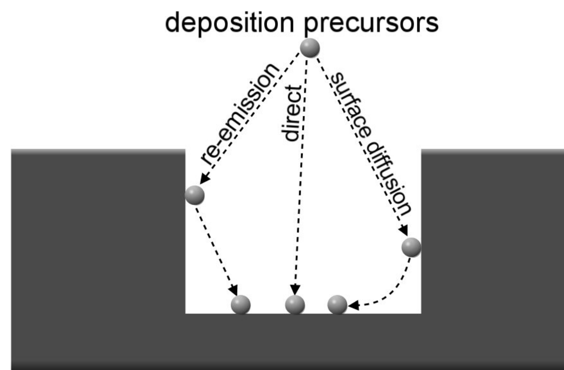


Fig. 5.1: PECVD surface deposition kinetics in a trench.

In order to develop a process for depositing PECVD a-Si:H that is compatible for MEMS applications, different issues are a priority compared to electronic-grade a-Si:H films. Low defect density a-Si:H is grown between 200 and 300℃ and at low RF power resulting in a low deposition rate [6]. For MEMS applications, high deposition rates, low film stress, and good substrate adhesion are the main concerns. Only reasonably high deposition rates are practical for films in the micron range and with these thick films, mechanical stress can cause films to flake off or bubble from the substrate. These requirements are highly dependent on the PECVD deposition parameters: chamber pressure determines the mean free path of molecules; RF power establishes the dissociation rate; gas flow determines the residence time in the chamber; and substrate temperature influences the reactions that take place at the growing surface. In the following sections we describe our process development and material characterization of a-Si:H films for MEMS.

The substrate temperature for the films deposited by PECVD for MEMS is kept at 150℃ in order to ensure the applicability of this process to a wide range of MEMS and post-processing of devices. This also provides more flexibility for choosing sacrificial layer materials and allows certain photoresists to be used. In our PECVD system, silane is diluted with argon (Ar) because it can increase the deposition rate [95] and lead to an enhanced SiH_4 dissociation rate [96]. It was observed that if the SiH_4 pressure was further increased, the deposition rate would increase, but unreacted species were left on the chamber walls due to the low temperature of the substrate chuck and required a long chamber clean. Therefore, the SiH_4/Ar gas flow was kept constant. In order to achieve a practical deposition rate, the chamber pressure and the RF power were varied while maintaining stable plasma. The measured deposition rates are listed in Table 5.1. The a-Si:H films reported in this section and the fabricated cantilever beams in the next section were deposited with the process conditions that resulted in the highest deposition rate of 5.1 Å/s for our system (Table 5.2). The same dry etch process developed in the initial material characterization stage is used for etching the a-Si:H films deposited at 150℃ and give the same etch rate (Table 3.2). This is a rough indication that the density of the films deposited between 150-250℃ do not differ by a significant amount.

Table 5.1: Variation in deposition rates for our PECVD a-Si:H thick films (SiH_4 gas flow = 10 sccm, Ar gas flow = 7 sccm, substrate temperature = 150℃). The 5.1 Å/s deposition rate was the maximum rate obtained with our system (100 kHz parallel plate system with 8” electrode).

Pressure (mT)	**RF Power (mW/cm^2)**	**Deposition Rate (Å/s)**
500	77	3.8
500	93	4.1
750	93	4.6
750	114	5.1

Table 5.2: PECVD process conditions developed for depositing a-Si:H thick films with a deposition rate of 5.1 Å/s (100 kHz parallel plate system with 8" electrode).

Parameter	**Setting**
Pressure	750 mT
RF Power	114 mW/cm^2
SiH_4 Gas Flow	10 sccm
Ar Gas Flow	7 sccm
Substrate Temperature	150°C
Deposition Rate	**5.1 Å/s**

5.2 Film Stress Issues of a-Si:H Thick Films as a Mechanical Material

In our application of a-Si:H as a structural material, thick films in the micron range are required. This requires an understanding of the mechanical film stress of our films.

For the application of inductors on low resistivity Si, if the thickness of the isolating layer is increased, the Q will improve. However, thick films tend to lead to an increase in stress. Mechanical film stress can lead to damage of the entire structure when thin films are stacked. Whether or not film stress causes a problem depends on the deposition conditions and mismatch with the substrate. A small level of stress can sometimes strengthen structures, but high levels of stress usually lead to problems. Tensile stress failure causes cracks and the film may peel off of the substrate. Compressive stress failure is characterized by buckling which can appear as bubbles. Accurate assessment of the deformation caused by film stress is critical for developing controllable processes and producing high quality devices.

In general, the stress measured in films deposited on a substrate depends on [34]:

- thermal expansion coefficient between the substrate and film;
- microstructure of the bulk of the film; and
- mismatch in strain at the interface.

The contribution from the strain at the interface should only be noticeable a few nanometers from the interface and is often neglected [97]. Therefore the measured stress is

attributed to a thermal and intrinsic component. The thermal stress is calculated by [34]:

$$\sigma_{th} = \frac{(\alpha_{sub} - \alpha_{film})\ (T_{dep} - T_{meas})\ E_{film}}{1 - \upsilon_{film}} \tag{5.1}$$

where α_{sub} and α_{film} are the thermal expansion coefficients of the substrate and film, T_{dep} and T_{meas} are the deposition and measurement temperatures, and E_{film} and υ_{film} are the Young's modulus and Poisson's ratio of the film.

An optical stress gauge measures wafer deflection by means of reflected light as shown in Fig. 5.2. A fiber-optic bundle contains both transmitters and receivers of light and the intensity of the returning light defines the distance from the end of the bundle to the back of the wafer. Deflection is measured before and after film deposition and the difference in the readings is the total deflection due to the film deposition. The extreme sensitivity of the instrument (0.03 μm) can measure tensile and compressive stresses ranging from 1 to 10^7 MPa. If the wafer has bowed away from the light sensor after coating (increased meter reading) then it is under compressive stress. A wafer that bows toward the light sensor (decreased meter reading) is under tensile stress.

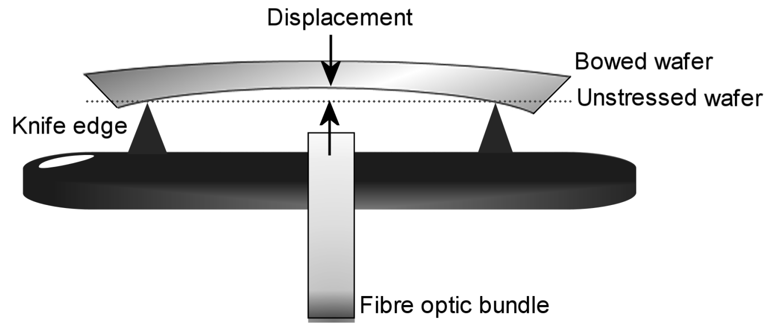


Fig. 5.2: Schematic of an optical stress gauge test setup for film stress measurements by measuring wafer curvature.

The total stress is calculated from Stoney's equation [98]:

$$\sigma = \frac{d}{R^2}\ \frac{E_{sub}}{(1 - \upsilon_{sub})}\ \frac{t_{sub}^2}{t_{film}} \tag{5.2}$$

where d is the deflection, R is the knife edge radius of the instrument ($R = 7.1$ cm), E_{sub} and υ_{sub} are the Young's Modulus and Poisson's ratio of the substrate, t_{sub} and t_{film} are the substrate and film thicknesses. This equation can be applied given that the following are satisfied: substrate thickness is much thicker than the film thickness, the thickness of the wafer is uniform, and the deflection is small compared to wafer thickness. For the double-sided polished c-Si wafers used in this study, $E_{sub} = 130$ GPa and $\upsilon_{sub} = 0.28$ were adopted [99].

Thick films in the micron range exhibited compressive stress ranging from 130-370 MPa as shown in Fig. 5.3. The observed decrease in stress with increasing film thickness is not what was expected. However, our films are uniquely deposited at low temperature (150℃) and could be a result of improved ordering of the amorphous network for prolonged deposition times [76]. The hydrogen content of the a-Si:H thick films was measured to be 20 at.% and was presented in Chapter 3. This explains the low stress measured in our films (it is difficult to obtain films with low stress and low C_H [97]). There was no change in the FTIR spectrum for different film thicknesses. Our PECVD system does not accommodate hydrogen dilution and the substrate temperature of our films is kept constant at 150℃, so the hydrogen content in our a-Si:H films cannot be adjusted by a signficant amount.

Some researchers conclude that the stress in a-Si:H films is correlated to the hydrogen incorporation in the network [73]. It is generally agreed that hydrogen incorporation in the silicon matrix is related to stress because hydrogen tends to relieve strained bonds. It is unclear if the bulk hydrogen concentration is directly related to stress, but silicon-hydrogen bonding configurations do play a role. The network of a-Si:H is composed of clusters of Si atoms surrounded by H atoms at the boundaries forming microvoids [97]. A film with a large SiH_2/SiH ratio (> 1), physically corresponds to small Si clusters and large microvoids. A large number of microvoids corresponds to more positions available for atoms to move to which provides more flexibility in the film when experiencing stress, leading to tensile stress. On the other hand, a film with small SiH_2/SiH ratio (< 1), corresponds to large Si clusters and compressively stressed film.

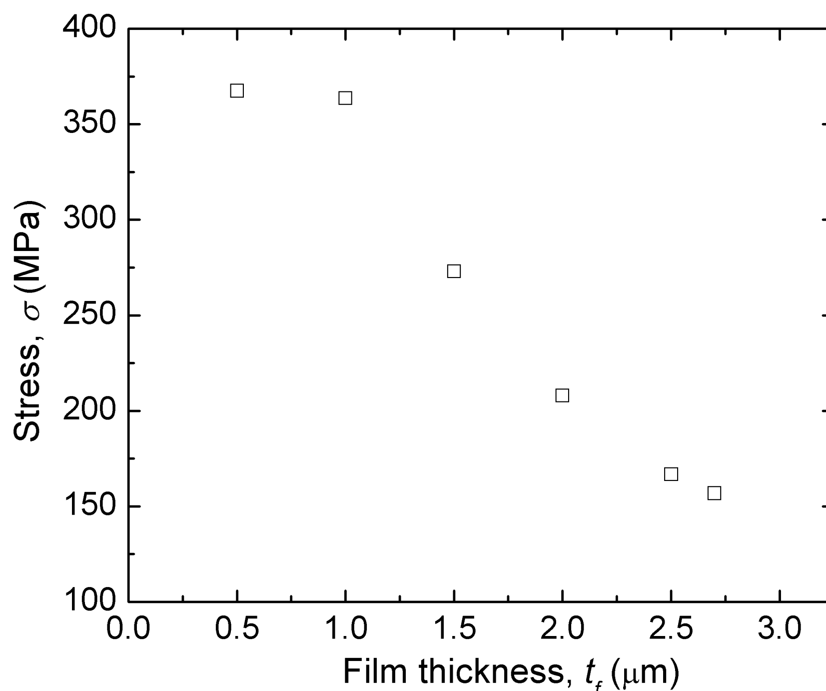


Fig. 5.3: Measured stress in our PECVD a-Si:H thick films with varying thicknesses deposited on a double-sided polished c-Si substrate. The measured compressive stress decreased as film thickness increased.

5.3 Integration Issues of a-Si:H Thick Films as a Mechanical Material

For the incorporation of our a-Si:H films as a structural layer for low temperature MEMS fabrication, sidewall coverage is an anticipated issue. PECVD a-Si:H was deposited over various test structures and the sidewall coverage was studied by SEM. Based on the degree of film coverage, the stress and deflection of a simple cantilever beam were simulated to determine the relationship with the sidewall angle formed with the substrate. Bimorph thermal actuators were designed, fabricated and tested to determine the feasibility of a-Si:H as a structural layer in a low temperature MEMS process.

5.3.1 Critical Role of Step Coverage of an Anchor

A simple bimorph cantilever beam was simulated in Coventor [100] to determine the role the sidewall angle of the a-Si:H film and conformal Al film plays on the tip deflection and the stress. Figure 5.4(a) is a cross-sectional schematic of the anchor of the simulated structure with a 60° sidewall angle and 1 μm a-Si:H and 1 μm Al with an air gap of 2 μm. The thinnest section of the sidewall coverage was kept constant at 0.5 μm. For simulation purposes, a sacrificial layer with a 90° sidewall angle was assumed. Figure 5.4(b) shows the distribution of the von Mises stress, a scalar average of the 3-D principal stresses, in the supported anchor of the bimorph structure. For a sidewall angle of 60°, the beam experiences a maximum stress of 260 MPa at the base of the anchored structure and inner edge of the a-Si:H layer.

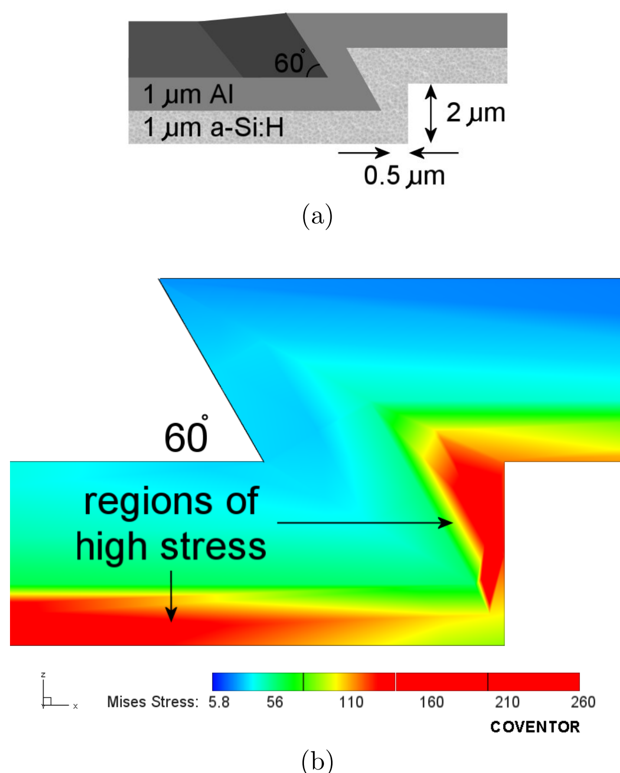


Fig. 5.4: (a) Cross-section schematic of a bimorph anchor with 60° sidewall angle. (b) Simulated stress distribution in the anchor.

Figure 5.5 shows that as the sidewall angle between the deposited a-Si:H film and the substrate is varied, the maximum displacement of the tip of the bimorph cantilever beam reaches a maximum at a sidewall angle of 100°. The related stress at the anchored support is minimized at a sidewall angle of 75°. These results indicate an optimal sidewall angle range of 75-100°. Comparing this to the SEM image of our experimental structure (Fig. 5.6), an average sidewall angle of 80° is indeed within the range of maximum displacement and minimum stress for a simple cantilever beam.

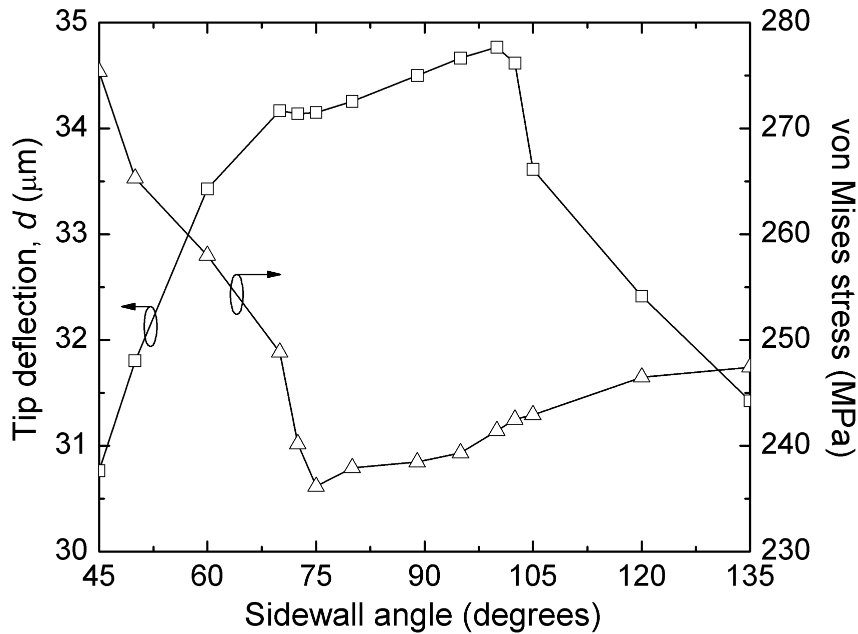


Fig. 5.5: Simulated displacement and von Mises stress of a bimorph cantilever beam with varying sidewall angles. An optimal sidewall angle in the range of 75-100° results in minimum stress and maximum deflection.

5.3.2 Optimizing the Step Coverage of a-Si:H Thick Films

To study the sidewall coverage of PECVD a-Si:H films, test structures were prepared with photoresist. Figure 5.6 is a SEM cross-section of 1.5 μm a-Si:H film deposited over a 2.7 μm step height of resist. A cusp at the edge of the step is observed due to the high

arrival angle at the edges and low surface mobility of adsorbed atoms at low substrate temperature. This is also expected from Ar diluted SiH_4 [101] and high pressure and RF power settings required for our thick films. This film morphology results in a section of the sidewall coverage having a thickness of only 1 μm (67% of the deposited film). This non-uniform film thickness may not be an issue for the actuation of beams and bridges because the cusp formation can provide extra support at the anchor which experiences the most stress during large deflections.

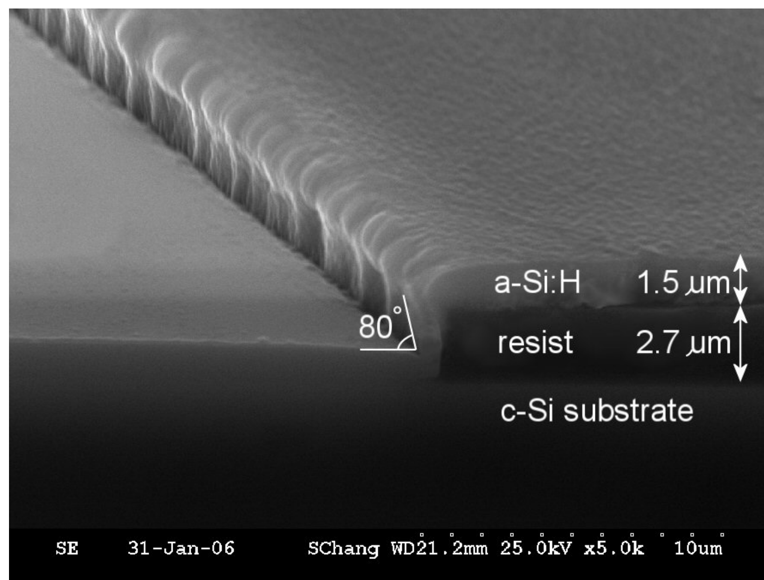


Fig. 5.6: SEM cross-section of 1.5 μm a-Si:H thick film deposited over 2.7 μm step of resist on a c-Si substrate in this work. An 80° sidewall angle is estimated, viewed at 75° tilt. (Cusp formation is seen at the edge of the step.)

Unique sacrificial layer structures were created to investigate the sidewall coverage in extreme cases. As seen in Fig. 5.7, precursors passed through a 1 μm vertical gap to deposit by re-emission and surface diffusion covering a 2 μm deep concave enclosure. The thickness of the film in the shadowed zone is only on the order of hundreds of nanometers and if the deposition time was extended, the opening would eventually be sealed and a huge void would remain. If desired, the PECVD process conditions could be optimized to improve the coverage in the enclosure, an option unavailable to most PVD processes.

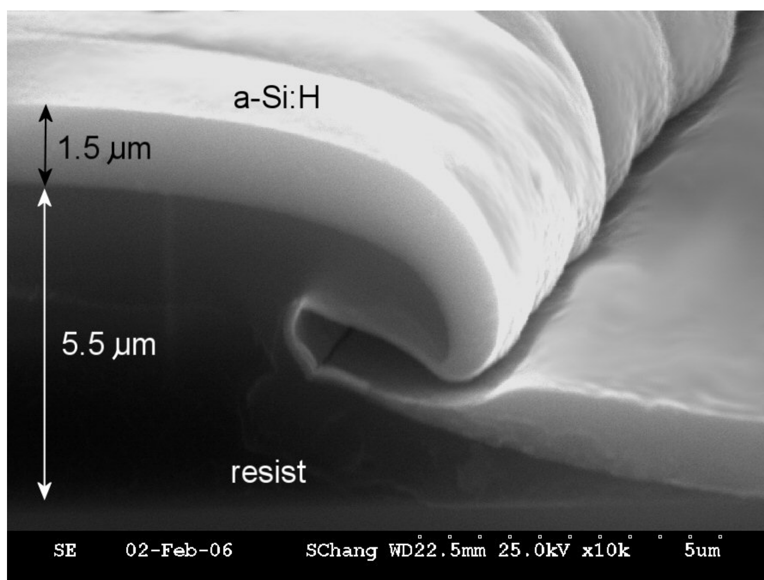


Fig. 5.7: SEM cross-section of resist with an extreme sidewall profile and 1.5 μm a-Si:H thick film coverage, viewed at 75° tilt. A few hundreds of nanometers of a-Si:H covers the concave enclosure

5.4 Fabrication and Testing of a Simple MEMS Device with a-Si:H Thick Film

In order to evaluate the potential applications of incorporating a-Si:H in a low temperature MEMS process, bimorph thermal actuators were designed, fabricated, and tested.

5.4.1 Simple Vertical Bimorph Thermal Actuator

Bimorph thermal actuators are widely used in MEMS due to large displacement, low actuation voltage and relative ease in fabrication [35]. Applying a voltage causes a temperature change and due to the difference in the coefficient of thermal expansion (CTE) of the two layers the beam deflects. The final position of the beam is a balance between the shear force imposed by the difference in CTE and the spring constant of the beam itself.

5.4.1.1 Design and Fabrication

The radius of curvature in a bimorph beam can be calculated by [102]:

$$\frac{1}{r} = \frac{6b_1b_2E_1E_2t_1t_2(t_1_t_2)(\alpha_1 - \alpha_2)\Delta T}{(b_1E_1t_1^2)^2 + (b_2E_2t_2^2)^2 + 2b_1b_2E_1E_2t_1t_2(2t_1^2 + 3t_1t_2 + 2t_2^2)} \tag{5.3}$$

where $b_{1,2}$ is the width, $t_{1,2}$ is the thickness, $\alpha_{1,2}$ is the TEC, $E_{1,2}$ is the Young's modulus, ΔT is the temperature change and the subscripts 1 and 2 indicate the bottom and top layer, respectively. The minimum radius of curvature is given by equating the thickness and width of the two layers. Approximating the Young's moduli of both layers as having the same order of magnitude introduces only a small percentage of error. This gives the following simplified equation for estimating the radius of curvature:

$$\frac{1}{r} = \frac{3\Delta\alpha\Delta T}{8t} \tag{5.4}$$

where $\Delta\alpha$ is the difference in CTE of the two layers and t is the total thickness of the beam. The vertical tip deflection of the beam can be evaluated from the radius of curvature by:

$$d = \frac{\ell^2}{2r} \tag{5.5}$$

where ℓ is the free deflection length of the structure and $\ell < r$. This gives the following relationship for the deflection of a bimorph cantilever beam:

$$d = \frac{3\ell^2\Delta\alpha\Delta T}{16t} \tag{5.6}$$

In order to maximize deflection, $\Delta\alpha$ and ℓ should be large, and t should be as small as possible. Variation in the Young's modulus from poly-Si to a-Si:H for example, only has a small effect on the transducer characteristics and is easily compensated for by changing the physical dimensions of the structure [35]. The thermal energy required to raise the temperature of the beam is dependent on the heat capacity of the layers. Energy loss is mostly due to the heat transfer to the substrate and the surrounding atmosphere. To minimize the input power for a given deflection, the surface area of the device needs to be minimized. We have designed and simulated bimorph thermal actuators with various

widths and lengths were designed and simulated. Practical film thicknesses were selected based on the tolerable stress in the overall structure.

Bimorph thermal actuators were fabricated in the process illustrated in Fig. 5.8. After wafer preparation of low resistivity p-type <100> 8-12 Ω cm c-Si substrates, a non-photosensitive resist was spin coated and baked. This sacrificial layer was patterned with another resist and removed in developer, then etched back by RIE to give a thickness of 2 μm. The process conditions in Table 5.2 was used to deposit 1 μm of a-Si:H by PECVD and then 1 μm of Al was sputtered, giving a total beam thickness of 2 μm. The Al was patterned and wet etched and then served as a mask for etching the a-Si:H layer by RIE (process conditions listed in Table 3.2). As a final step, the sacrificial layer was wet etched releasing the bimorph structure. Due to residual stress in the layers, the beams bent away from the substrate upon release.

5.4.1.2 Results and Discussion

Figure 5.9 shows an SEM image of one of our fabricated bimorph thermal actuators incorporating a-Si:H. After the sacrificial layer was removed, a device with a beam length of 500 μm resulted in a tip deflection of hundreds of microns. This thermal actuator was tested by applying a voltage across the terminals and deflection was monitored. Figure 5.10 is an overlay of images of the tip deflection at different voltages which was measured with an angled mirror (test setup described elsewhere [103]). An applied voltage of 1.2 V straightens the beam to a flat position. Figure 5.11 shows the measured tip deflection obtained for various applied voltages. The mechanical performance was verified by repeating the measurements after several days. We also performed a finite element analysis in Coventor using the a-Si mechanical properties listed in Table 2.3 and modeling the residual stress in the layers. The simulated results are also shown in Fig. 5.11.

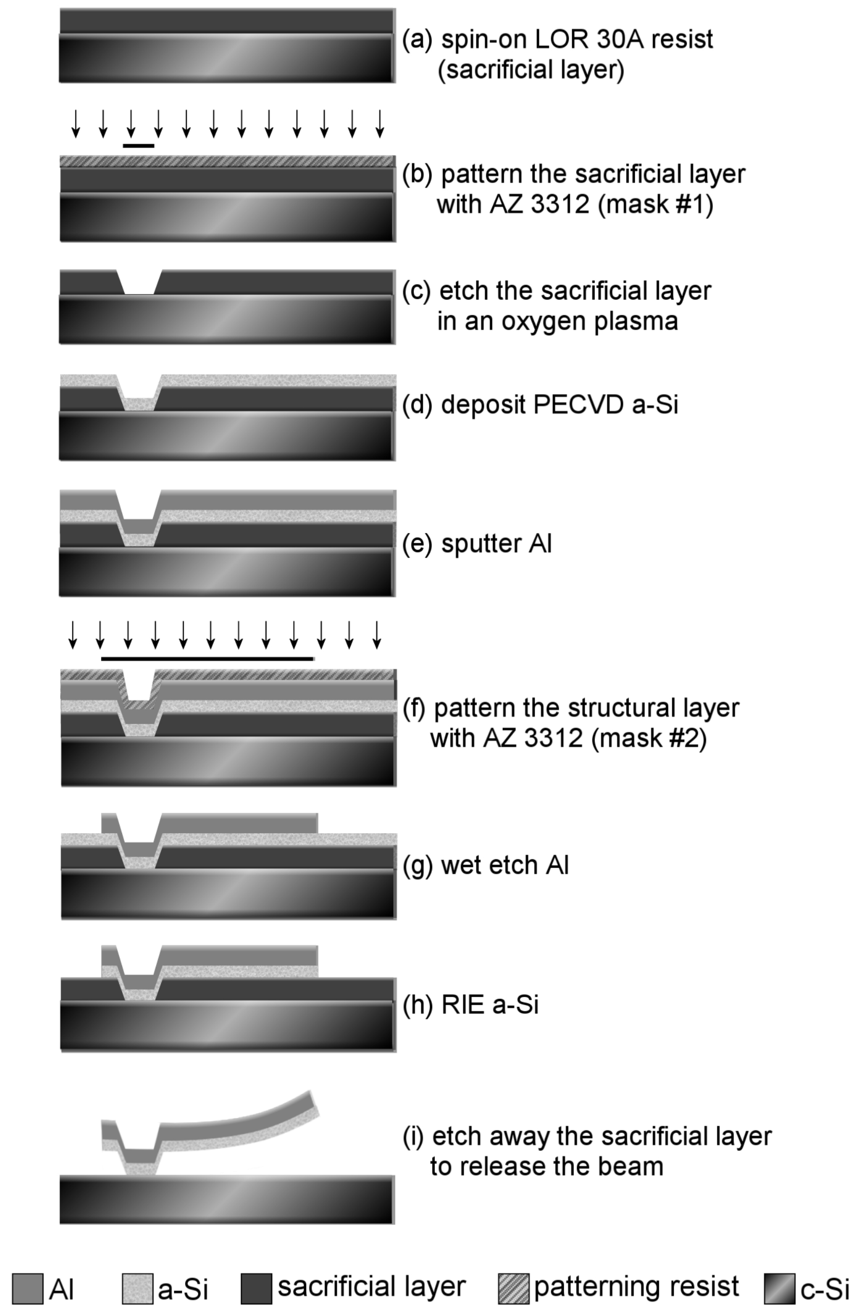


Fig. 5.8: Process steps for fabricating simple bimorph cantilever beams in this work (2 mask process).

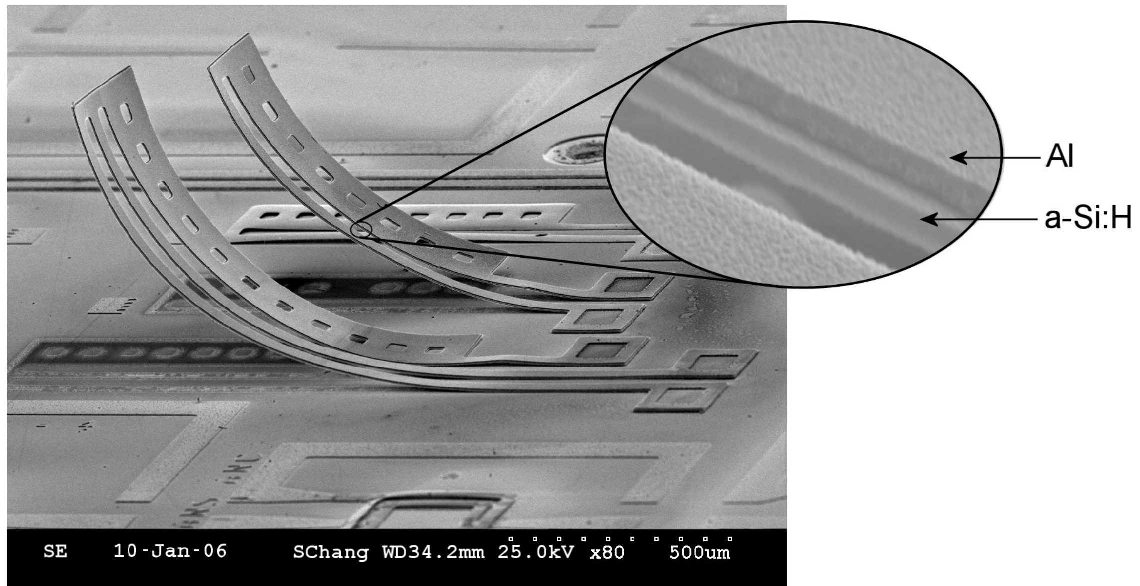


Fig. 5.9: SEM of bimorph thermal actuators incorporating a-Si:H fabricated in this research, viewed at 75° tilt. The tip of the beam reaches hundreds of microns of vertical displacement.

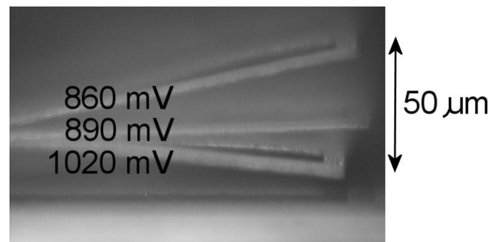


Fig. 5.10: Overlay of microscope images showing the actuated tip with various applied voltages of a fabricated bimorph thermal actuator, viewed through an angled mirror.

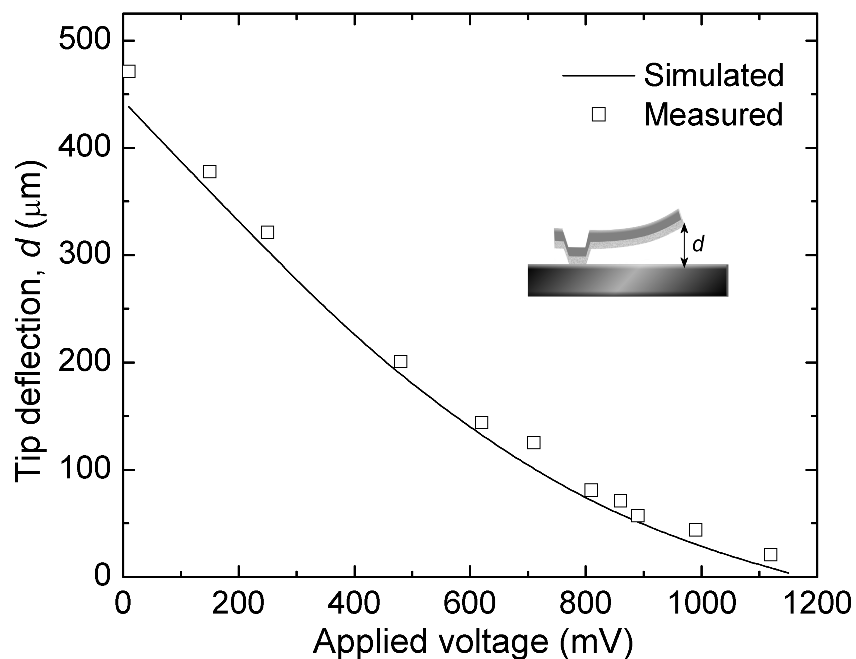


Fig. 5.11: Measured and simulated tip deflection of a fabricated bimorph thermal actuator incorporating a-Si:H as a mechanical material.

5.5 Summary

In this chapter, a-Si:H deposited by PECVD at 150℃ is proposed as a structural layer for low temperature MEMS fabrication. The deposition of thick a-Si:H films and the characterization of the mechanical stress and hydrogen incorporation in the film is presented. The sidewall coverage of various test structures was investigated and resulted in a sidewall angle of about 80° with the substrate. Simulation results show that this angle is within the region of maximum deflection and minimum stress in the anchor of a simple cantilever beam. Bimorph thermal actuators incorporating PECVD a-Si:H deposited at 150℃ were designed and fabricated. The measured deflection is on the order of hundreds of microns and is in close agreement with thermomechanical simulations. From the experimental results of the fabricated bimorph thermal actuators, a-Si:H is justified as

a promising candidate for the structural layer in low temperature MEMS fabrication. In the next chapter, tunable inductors and transformers are fabricated with an a-Si:H and Al bimorph in order to explore the feasibility of an RF MEMS application.

Chapter 6

Tunable RF MEMS Inductors and Transformers using Amorphous Si Thick Films as a Mechanical Material

In this chapter, amorphous silicon deposited by PECVD at 150℃ is applied to RF MEMS devices. The design, fabrication, and testing of novel tunable RF MEMS inductors and transformers based on the bimorph effect of an a-Si:H and Al structural layer is presented. The fact that these devices are fabricated on Si in a low temperature process enhances the possibility of system integration of MEMS devices with other commercially available CMOS processes.

6.1 Tunable RF MEMS Inductors

Microelectromechanical inductors have been fabricated using surface [54,104,105] and bulk [106, 107] micromachining to elevate and suspend the coil from the substrate. Surface tension self-assembly [108], stress-engineered metal [109], and plastic deformation magnetic assembly [56] are other methods that have been developed to bend the inductor away from the lossy Si substrate. Tunable inductors would further benefit wireless communication circuitry where accurate impedance matching and frequency tuning would increase the flexibility and reliability of the system. Tunable inductors have been explored by adjusting

the distance between coupled coils where a large tuning range and acceptable Q is attained; however, the inductance is small, in the range of 1 nH [55, 110]. An electrostatic inductor fabricated at low temperature displays a large tuning range, but only operates up to 1 MHz [111]. Another approach that has been employed is introducing microrelays for achieving discrete inductance values [112]. A large tuning range was measured, but the reported Q is low. In this section, a novel tunable inductor based on the thermal actuation of an a-Si:H/Al bimorph structural layer fabricated on Si at low temperature is presented. The fabrication process developed in this work is carried out below 150℃, rendering this process highly integrable.

6.1.1 Device Design

The tunability of the inductor is based on the bimorph effect: when a voltage is applied, due to the difference in CTE of two materials, the structure deforms in a controllable manner. In the first stage of designing and fabricating tunable RF MEMS inductors, the coil is designed in a simplified manner as a single metal layer. This results in significant negative mutual coupling of adjacent lines and decreases the overall inductance of the device (Fig. 6.1). Our goal was to achieve a high inductance with a large tuning range, so multi-turn inductors were designed. Various inductor layouts were explored, including circular, rectangular, and helical shapes. Depending on the application, an inductor in the 1 nH range would have a much smaller footprint and less vertical displacement and consequently a smaller tuning range would be observed.

6.1.2 Device Fabrication

The surface micromachined tunable inductor is composed of an a-Si:H/Al structural layer. In the as-fabricated device, the inductor coil warps due to the interlayer stress of the two films. The a-Si:H has 300 MPa of compressive stress and the Al layer has 10 MPa of tensile stress. The larger the mismatch in stress of the two films, the larger the vertical deflection. The stress in the a-Si:H layer can be controlled, for example, by film thickness and hydrogen content, and thermal annealing.

Fig. 6.1: Schematic indicating the direction of current flow for a single metal layer MEMS inductor.

The process steps are outlined in Fig. 6.2. The substrate used is p-type <100> 8-12 Ω cm c-Si. The Si substrate is cleaned in a standard RCA 1 solution for 15 min at 70℃ prior to processing. The DIEL_1 and DIEL_2 layers are a-Si:H thick films and are deposited by PECVD at 150℃ using the recipe in Table 5.2 and etched by RIE using the recipe in Table 3.2. The MET_1 and MET_2 layers are Al and are deposited by DC sputtering. Photoresist is used as a sacrificial layer and is etched away in the final step to release the device. Due to the built-in stress of the thin films, the inductor coil warps in a controllable manner. A schematic cross-section of the inductor showing the film thicknesses is illustrated in Fig. 6.3.

When a DC voltage is applied across the inductor, the 3-D structure flattens as shown in Fig. 6.4. An SEM image of a fabricated 6-turn inductor with 50 μm metal width and 15 μm spacing is shown in Fig. 6.5. The layout was simulated in Coventor and the vertical displacement of the released structure is shown in Fig. 6.6 displaying good agreement of the 3-D displacement. It should be restated that the underlying layer of the bimorph structure is undoped a-Si:H ($\sigma_{a-Si} = 1{\times}10^{-6}$ S/cm) effectively functioning as an isolation layer.

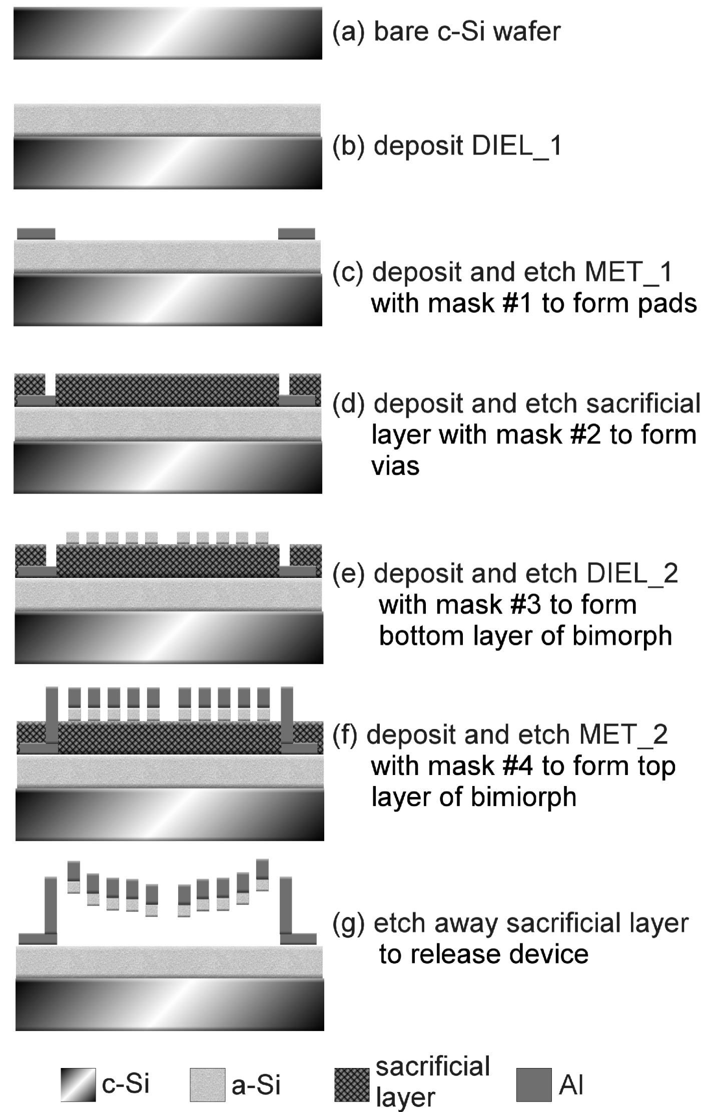


Fig. 6.2: Process steps for fabricating a tunable RF MEMS inductor in this work (4 mask process).

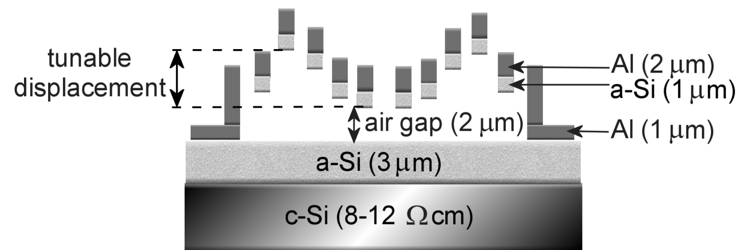
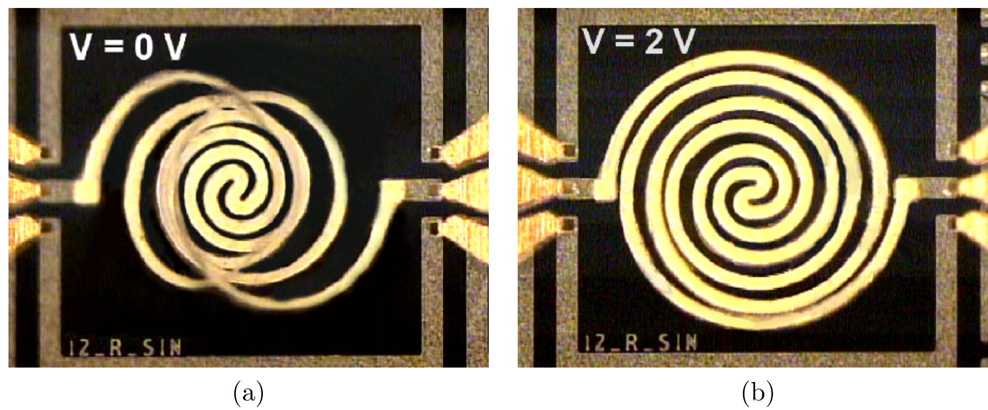


Fig. 6.3: Cross-sectional schematic of a tunable RF MEMS inductor for this study.



(a) (b)

Fig. 6.4: Micrograph image of the top view of an RF MEMS tunable inductor fabricated in this work with (a) no actuation and (b) 2 V applied across the coil.

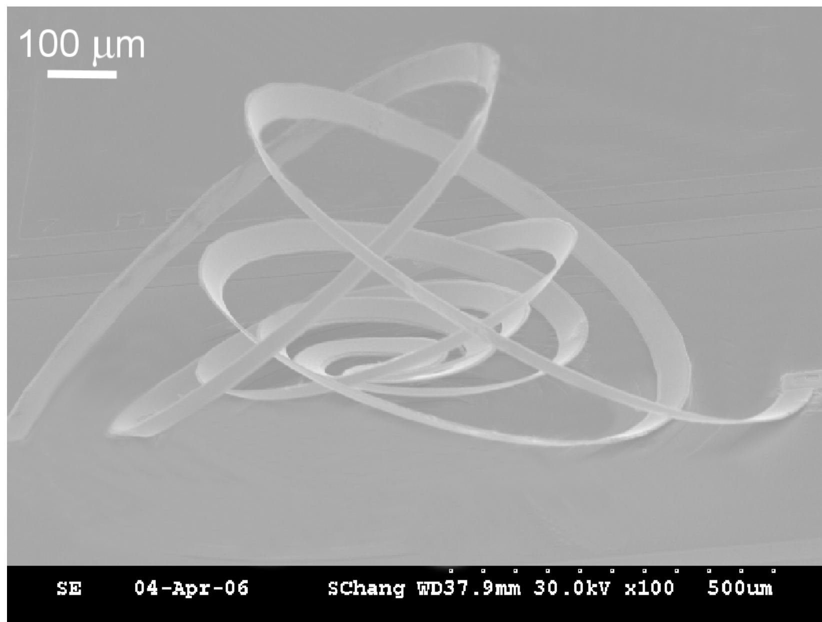


Fig. 6.5: SEM of a tunable RF MEMS inductor fabricated in this research. The outer turns reach hundreds of microns of vertical displacement.

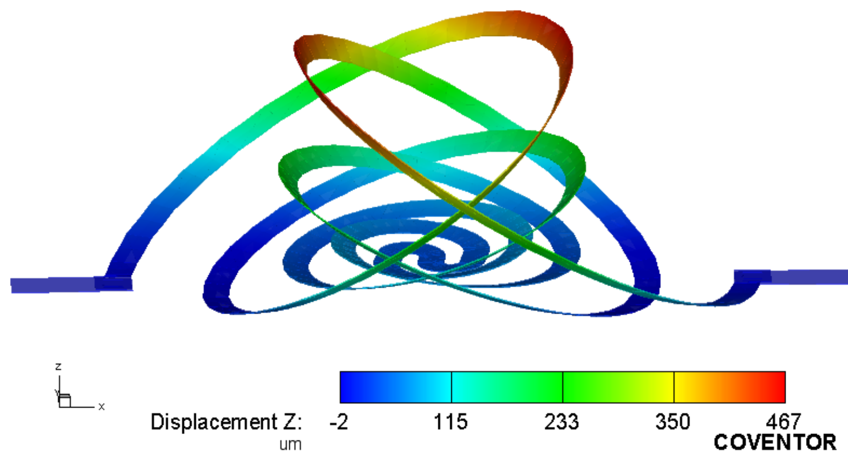


Fig. 6.6: Thermomechanical simulation performed in Coventor of a fabricated tunable RF MEMS inductor. This simulated structure corresponds well to the fabricated devices in this work.

6.1.3 Results and Discussion

The S-parameters of the fabricated inductors were measured from 50 MHz to 20 GHz with an Agilent 8510 network analyzer and Cascade Microtech GSG probes. The parasitic effects of the probe pads were de-embedded with an open test structure. The Q of the inductor is calculated from the ratio of the imaginary part to the real part of the one-port input impedance that is derived from the two-port measurement. As illustrated in Fig. 6.7, the measured inductance at low frequency can be tuned from 8.3 down to 5.6 nH by increasing the applied voltage to 2 V (drawing a current of 110 mA) and the corresponding Q is shown in Fig. 6.8. With no applied voltage, the inductor has a peak Q of 15 at 4 GHz. When voltage is applied, the Q rolls off at a lower frequency because the distance between the inductor and the substrate is reduced. The self-resonance frequency is 7 GHz and does not vary to a large extent with applied voltage. The repeatability of the thermal actuation and the corresponding measured RF response has been verified. In order to reduce the power consumption of the device presented, electrostatic actuation can be used the tune the RF MEMS inductor.

Based on the compact model in Fig. 2.3, the measured S-parameters are fitted to the compact model using a gradient search parameter optimization in Agilent ADS [113]. The fitted model parameters for varying applied voltages are listed in Table 6.1. The fitted L_s correspond to the measured results in Fig. 6.7. The R_s does fluctuate with applied voltage indicating that the proximity effect of neighboring conductors induces some losses. From thermomechanical simulations it can be seen that the distance between two conductors is at a minimum from 0.75 to 1.5 V. The C_s is very low since there is no coupling with an underlying metal layer and the crosstalk between adjacent turns is not significant. The C_{isol} increases as the coil is brought closer to the substrate with increased applied voltage which corresponds to a decrease in the input impedance of the two-port circuit. This causes the Q to roll off at a lower frequency due to increased losses in the Si substrate. The compact model of the inductor serves as a reasonable approximation for low frequency performance and gives some insight on the effects of the parasitics.

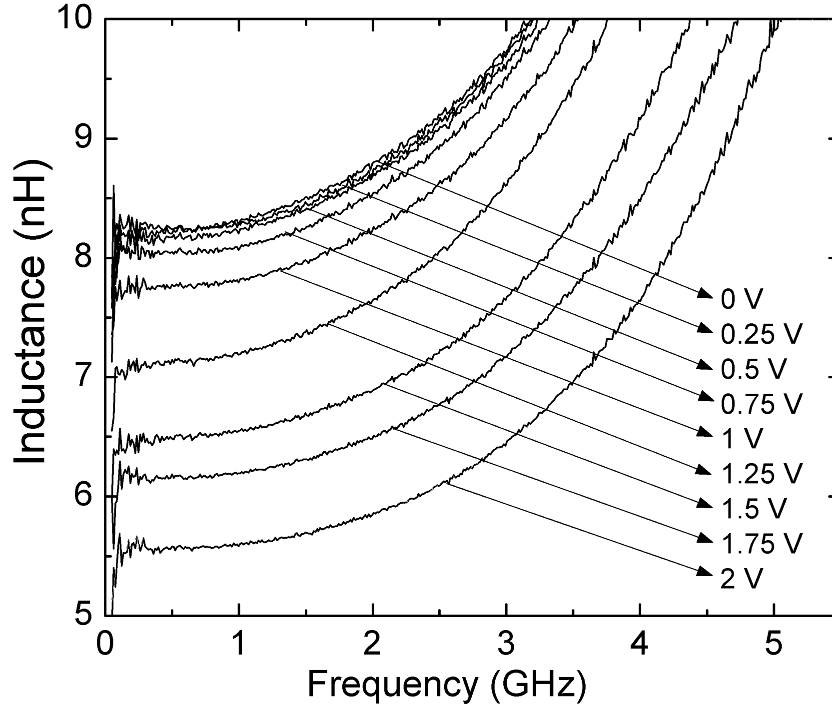


Fig. 6.7: Measured inductance of a fabricated RF MEMS tunable inductor with 0 to 2 V applied across the terminals. A 32% tuning range is achieved.

Table 6.1: Inductor compact model parameters fitted to measured results for different applied voltages of a fabricated tunable RF MEMS inductor in this work.

Voltage (V)	L_s **(nH)**	R_s **(Ω)**	C_s **(fF)**	C_{diel} **(fF)**	R_{Si} **(Ω)**	C_{Si} **(fF)**	Z_{in} **at 1 GHz (Ω)**
0	7.6	11	0.24	75	0.65	170	2.1
0.25	7.6	9.6	0.20	75	1.6	110	2.1
0.5	7.6	9.2	0.11	76	2.6	240	2.1
0.75	7.2	7.7	0.15	84	21	89	1.9
1	6.7	8.6	0.27	88	19	180	1.8
1.25	6.4	10	0.14	120	49	130	1.3
1.5	5.8	9.0	0.15	120	52	140	1.4
1.75	5.5	11	0.17	120	65	240	1.4
2	5.1	12	0.13	120	54	190	1.4

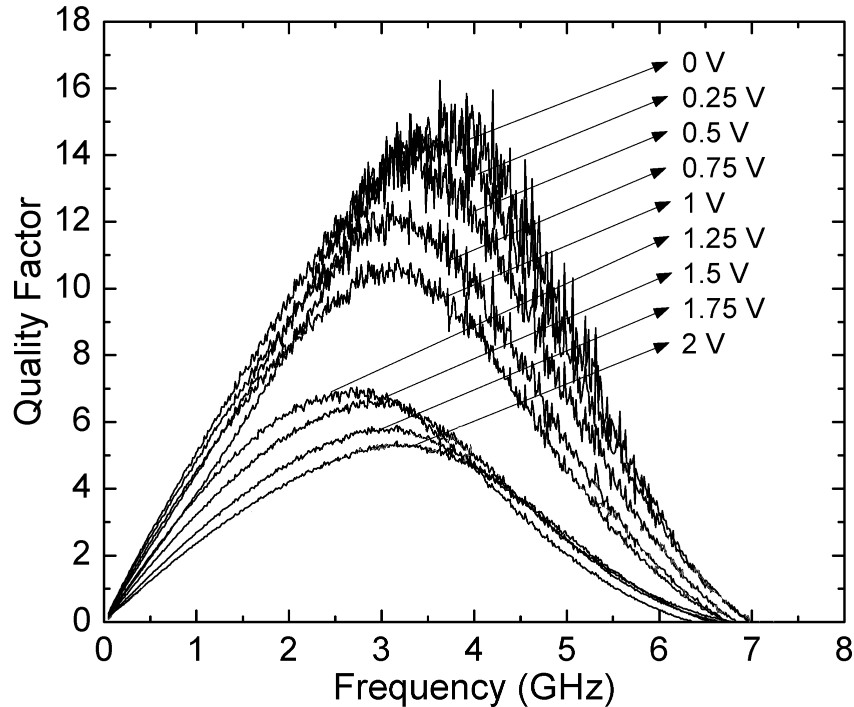


Fig. 6.8: Measured Q of a fabricated RF MEMS tunable inductor with 0 to 2 V applied across the terminals. The inductor has a peak Q of 15 with no applied voltage.

6.2 Tunable RF MEMS Transformers

After fabricating tunable RF MEMS inductors, transformers were explored in a six mask process. Transformers are key components in many RF circuits such as voltage-controlled oscillators, mixers, low-noise amplifiers, and power amplifiers. Transformers have also been used to tune the center frequency of filters [57], increase the Q of inductors [58], and tunable transformers could further increase the flexibility and reliability of wireless communication systems. One of the major challenges of successfully integrating RFICs on Si continues to be the poor performance of inductors. Although the low resistivity Si substrate is considered a cost-effective solution, it is a major source of energy loss and limits the Q of inductors at high frequency. Since transformers are simply two inductor coils coupled together they suffer from the same limitations. Therefore, a high degree

of transformer coupling tunability and an easily integrable process are important for RF integration.

6.2.1 Device Design

One major drawback of passive inductive elements is the occupation of large real-estate for on-chip designs. Furthermore, these large dimensions often require long interconnects for routing which introduce extra losses to the system. In integrated designs, area is expensive, and inductors and transformers often limit miniaturization goals. Therefore, stacked coils which offer reduced area and high mutual coupling with a tradeoff of low frequency response, are often used. In the stacked winding configuration, f_{res} is low due to the high capacitive coupling between the windings. However, if the air gap is adjusted, then the coupling coefficient of the stacked transformer can be tuned.

The design rules adopted for the fabrication of RF MEMS devices in a six mask process is listed in Table 6.2. The ETCH layer is used with the DIEL_3 layer as release holes to improve the fabrication yield. For this process, chrome masks were made by Advanced Reproductions Corp. [114].

Table 6.2: Design rules for the fabrication of MEMS inductors and transformers in this work.

Mask #	**Mask layer**	**Min. width (μm)**	**Min. spacing (μm)**	**Min. Enclosure (μm)**
	DIEL_1			
1	MET_1	20	10	15
2	DIEL_2	20	20	
3	MET_2	20	10	15
4	ANCHOR	20	20	
5	DIEL_3	20	10	15
6	MET_3	20	10	15
	ETCH	15	30	

6.2.2 Device Fabrication

Tunable transformers were fabricated with the process outlined in Fig. 6.9. This process requires three metal layers and six masks. Full fabrication details and recipes for this process are given in Appendix A.

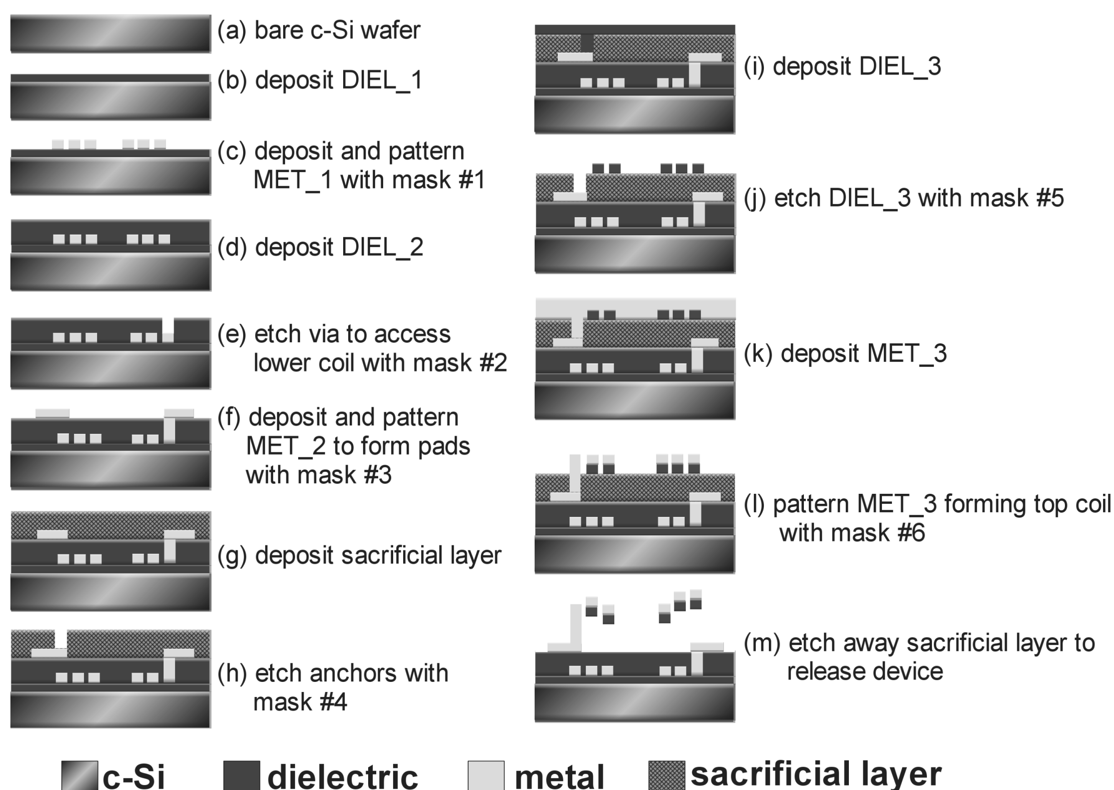


Fig. 6.9: Process steps for fabricating tunable RF MEMS transformers in this research (6 mask process). The dielectric layers are a-Si:H thick films and the metal layers are sputtered Al.

6.2.3 Results and Discussion

In this section, various transformer designs are reported. The first design is similar to the tunable inductor presented in the previous section, but a planar coil is designed in the first metal layer and the coupling with the stacked coil is tunable. In addition, smaller tuning

ranges are explored with the top coil embedded on a plate anchored along one edge. These plates are actuated by two methods: a resistive heater, and by thermal actuators.

6.2.3.1 Bimorph Coil Design

A tunable RF MEMS transformer on Si based on the bimorph effect of an a-Si:H and Al structural layer fabricated in a sub 150℃ process. The cross-section of the device is illustrated in Fig. 6.10. The stress developed in the bilayer allows the suspended coil to achieve hundreds of microns of vertical displacement. An SEM image of one of the fabricated transformers is shown in Fig. 6.12. Thermomechanical simulations performed in Coventor provide an exact match of the vertical displacement to the experimental structure as shown in Fig. 6.13. The tunability of the mutual inductance of the transformer is achieved by exploiting the difference in thermal expansion coefficients of the a-Si:H and Al thin films. By applying a DC voltage across the suspended coil, the temperature of the bimorph is increased due to joule heating and hence the structure deforms in a controllable manner reducing the distance between the two coils. Figure 6.11 shows the two extreme cases of vertical displacement of the suspended coil. The fact that the underlying layer of the bimorph and the top layer of the substrate is undoped a-Si:H ensures electrical isolation between the primary and secondary coil.

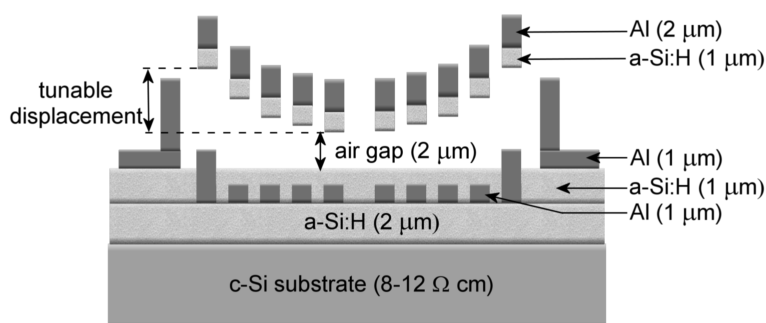
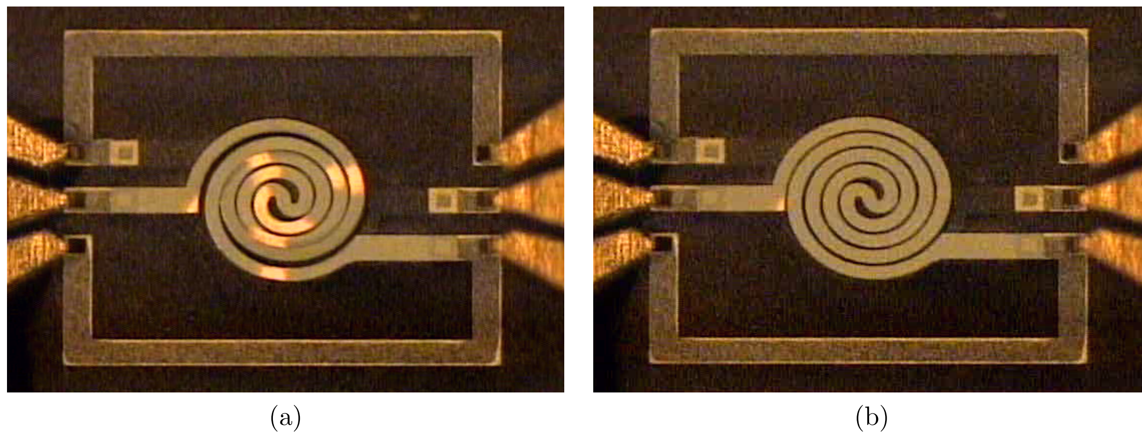


Fig. 6.10: Cross-section schematic of a tunable RF MEMS transformer on c-Si fabricated in a sub 150℃ process for this study.



(a) (b)

Fig. 6.11: Micrograph of a fabricated tunable RF MEMS transformer with (a) no applied voltage and (b) 1.25 V applied across the top coil. The light reflecting portions of the top coil indicate a deformed structure when no voltage is applied.

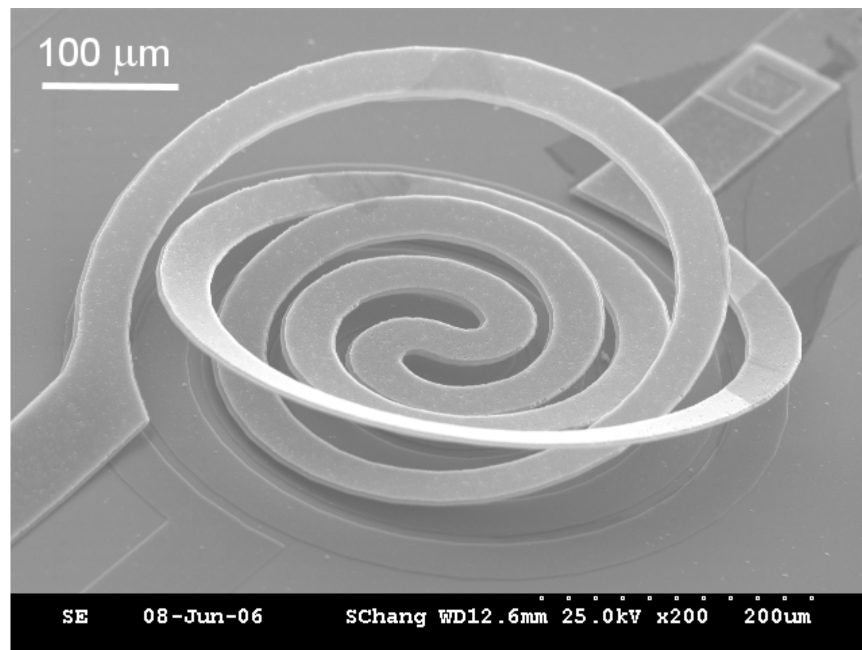


Fig. 6.12: SEM of a tunable RF MEMS transformer fabricated in this work, viewed at 60° tilt. The vertical height of the outer turns of the inductor reaches 170 μm.

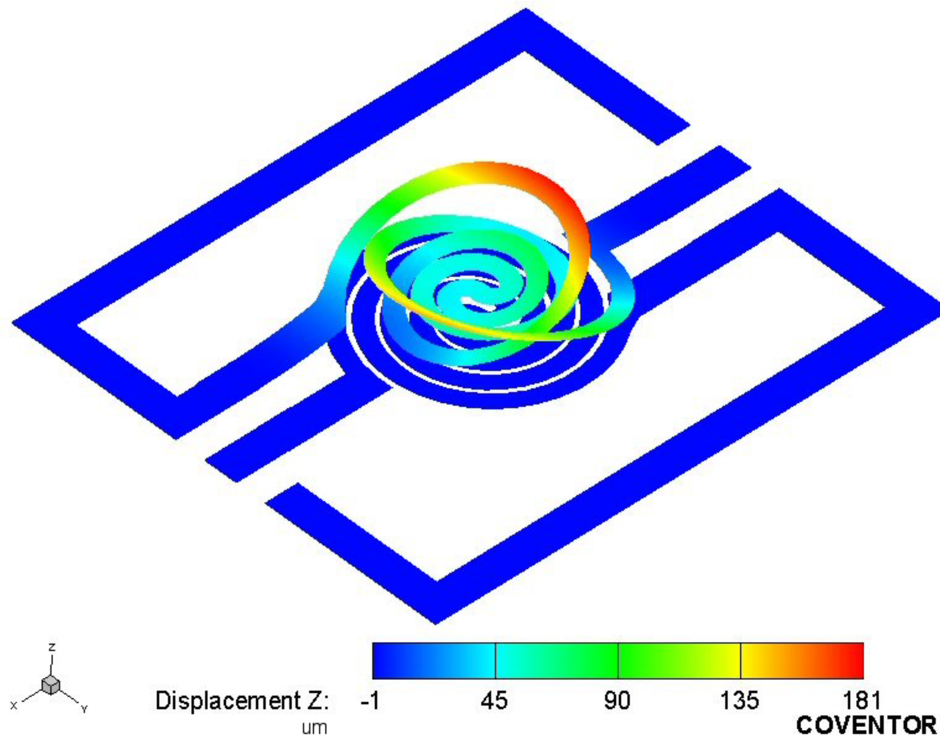


Fig. 6.13: Thermomechanical simulation performed in Coventor of the vertical displacement of a fabricated tunable RF MEMS transformer. The simulated results are consistent with the measured vertical displacement of our devices.

The performance of the transformer is extracted from the measured S-parameters from 50 MHz to 20 GHz. As the applied voltage is increased from 0 to 1.25 V the magnetic coupling coefficient (k) ranges from 0.44 to 0.58 as shown in Fig. 6.14 and the mutual inductance (L_m) increases from 0.94 to 1.2 nH as shown in Fig. 6.15. When the suspended coil is flat (applied voltage of 1.25 V), the transformer has an insertion loss of 4.2 dB at 9.0 GHz and 1 dB bandwidth from 4.9 to 13.4 GHz and return loss better than 8.5 dB over the 1 dB bandwidth as presented in Fig. 6.16. The device was simulated in Sonnet and the results are in good agreement with measured results.

The model presented in Fig. 2.13 was fitted to the measured S-parameters up to 6 GHz using a gradient search parameter optimization method in Agilent ADS. For each measured voltage, the model parameters were extracted and are listed in Table 6.3. The

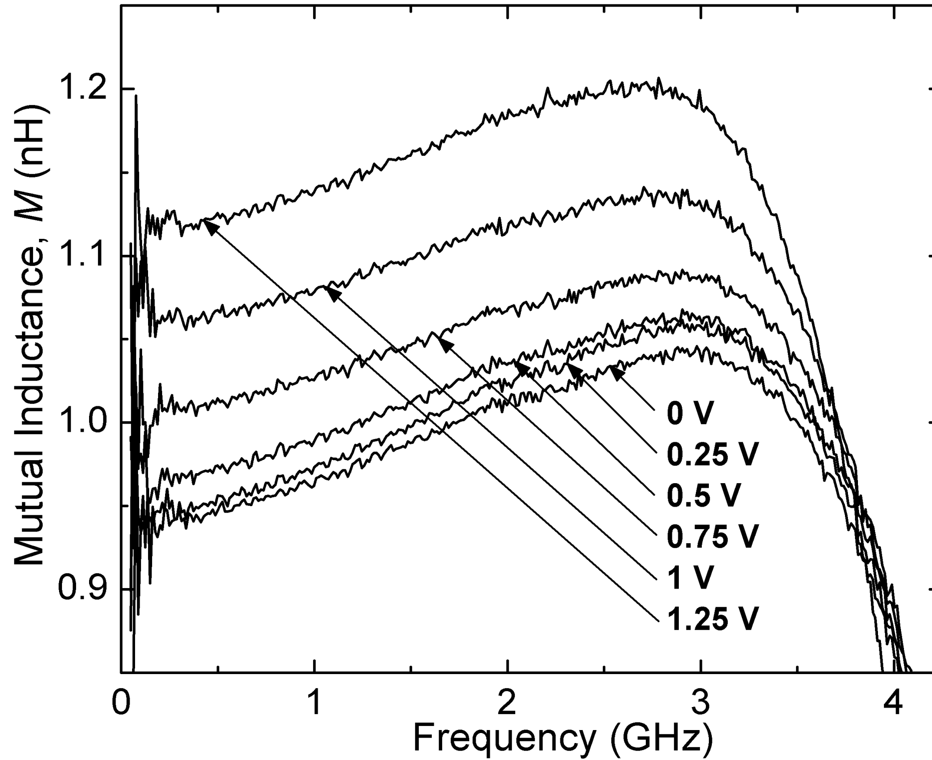


Fig. 6.14: Measured magnetic coupling of a tunable RF MEMS transformer fabricated in this work. When the applied voltage is varied from 0 to 1.25 V, the magnetic coupling ranges from 0.44 to 0.58 at low frequency.

inductance, L_p and L_s, are constant due to the same dimensions of the individual coils. L_m and k increase as the two coils are brought closer together agreeing well with measured values. The parasitic capacitance, C_{diel}, increases as the air gap between the suspended coil and the substrate which the planar coil lies on decreases as voltage is increased. The series resistance of the primary and secondary coils do not vary, but R_p is smaller than R_s due to a thicker metal layer and less losses from the skin effect. The parasitic coupling from the input and output is negligible as the extracted values of C_s remain low.

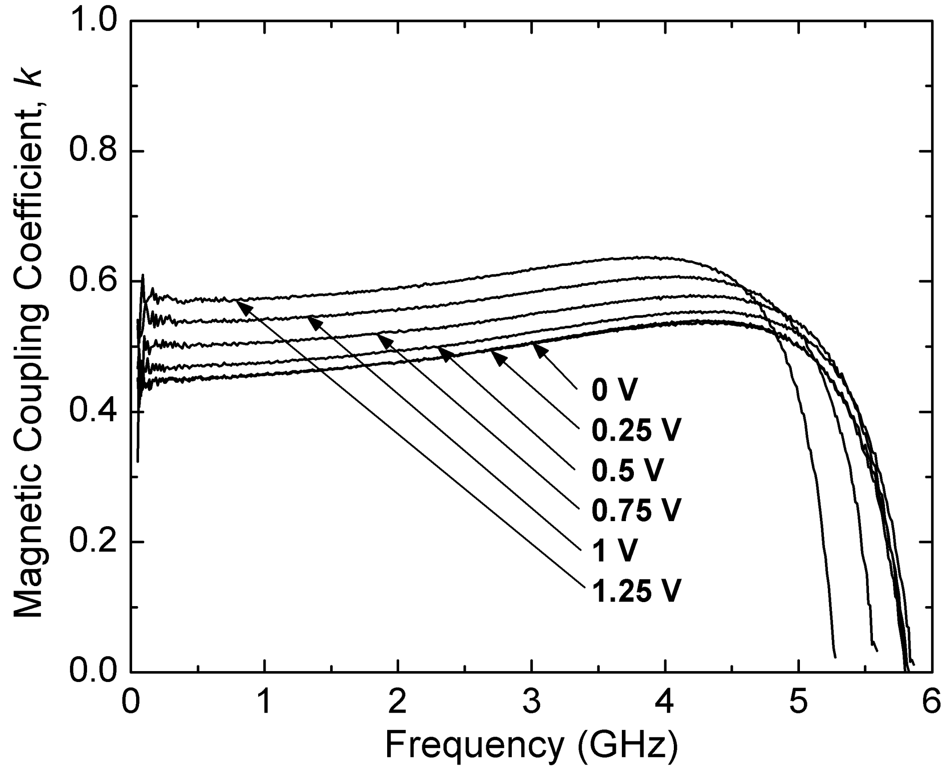


Fig. 6.15: Measured mutual inductance of a tunable RF MEMS transformer fabricated in this work. When the applied voltage is varied from 0 to 1.25 V, the mutual inductance ranges from 0.94 to 1.2 nH at low frequency.

Table 6.3: Transformer compact model parameters fitted to measured results for different applied voltages.

Voltage (V)	L_p (nH)	L_s (nH)	L_m (nH)	R_p (Ω)	R_s (Ω)	C_s (fF)	C_{diel} (fF)	R_{Si} (Ω)	C_{Si} (fF)	k
0	2.9	2.8	0.91	5.5	7.6	0.77	570	120	250	0.46
0.25	2.9	2.8	0.91	5.4	7.6	0.77	570	120	250	0.46
0.5	2.9	2.8	0.91	5.4	7.5	0.76	570	120	250	0.48
0.75	2.9	2.8	0.96	5.3	7.4	0.76	670	130	230	0.51
1	2.9	2.9	0.27	1.0	7.5	0.76	770	130	240	0.55
1.25	2.9	2.9	1.1	5.7	7.5	0.77	860	130	300	0.59

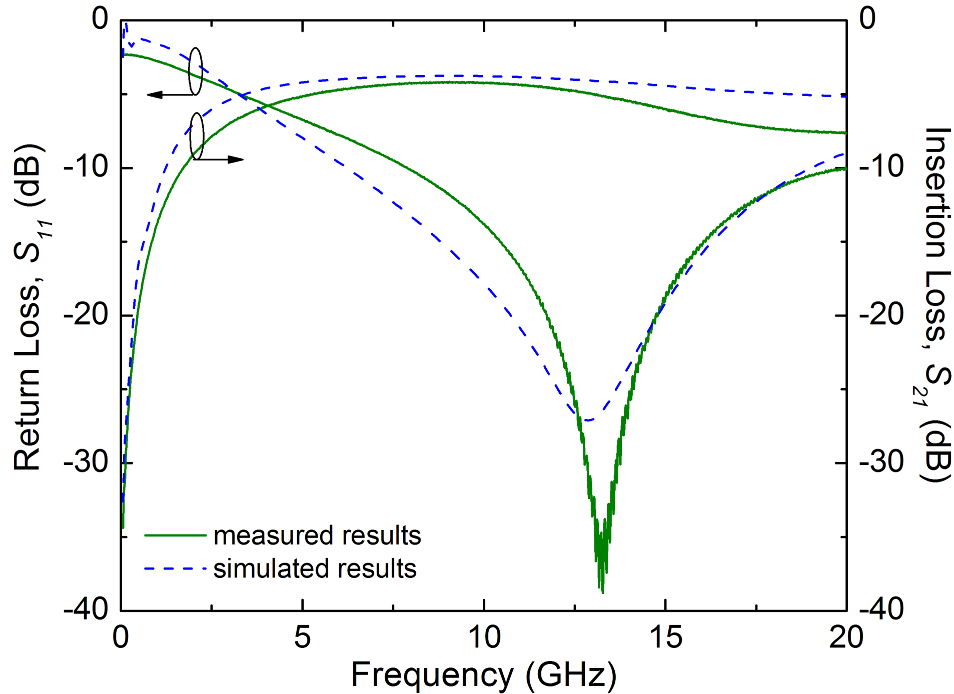


Fig. 6.16: Measured and simulated RF performance of a fabricated tunable RF MEMS transformer in this research. An insertion loss of 4.2 dB is measured at 9 GHz with 1.25 V applied (maximum coupling). This is in good agreement to the value determined by simulations.

6.2.3.2 Anchored Plate Design

Another approach taken in this research to change the distance between the two coils of a transformer is to fabricate the top coil on a plate anchored along one edge, and resistive heating or thermal actuators are used to move the plate. Since the plate is anchored along one edge, the maximum displacement is constricted, and the tunability of this design is limited but offers more precise inductance tuning. In this section, two designs are presented.

When the sacrificial layer is etched, the plate is released and bends based on the bimorph effect of the a-Si:H plate and the Al traces. When a DC voltage is applied across the resistive path, due to joule heating, the plate moves closer to the substrate. Figure 6.18(a) shows the design layout and Fig. 6.18(b) is the corresponding schematic shown in Coventor. An SEM image of a fabricated device is shown in Fig. 6.18(c). This transformer is laid out in

a non-inverting configuration of the primary and secondary coils and has the following coil dimensions: $n = 3\ \mu$m, $w = 50\ \mu$m, $s = 10\ \mu$m. When voltage is applied to flatten the plate, the maximum coupling is measured. These measured results are compared to simulations performed in Sonnet and the maximum coupling is in good agreement (Fig. 6.17). The 3-D deflection is predicted by thermomechanical simulations performed in Coventor (Fig. 6.19).

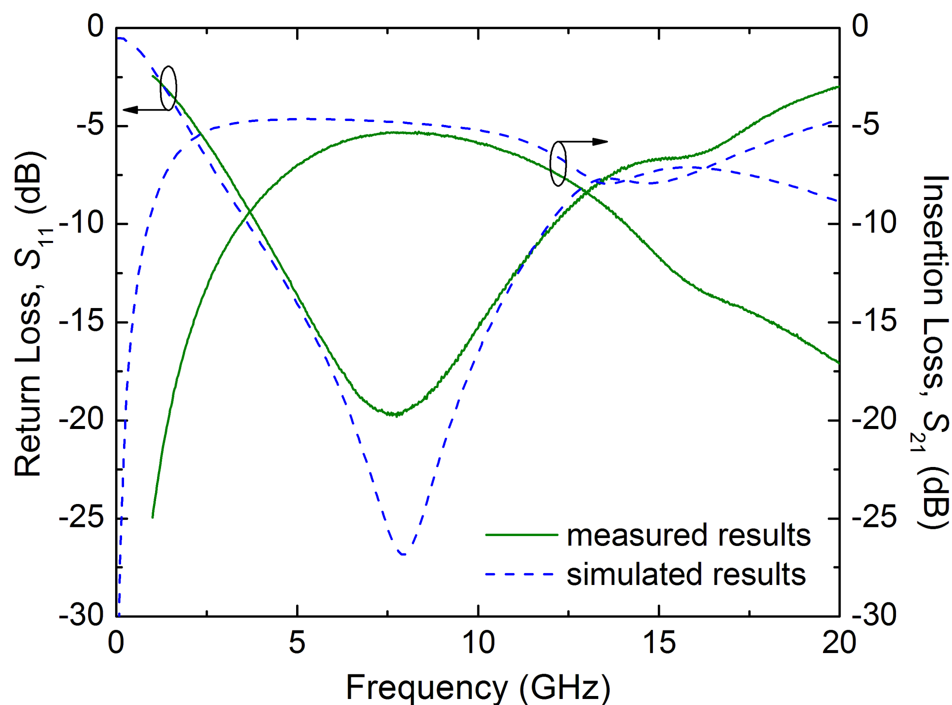


Fig. 6.17: Comparison of measured and simulated results of a resistively heated plate transformer.

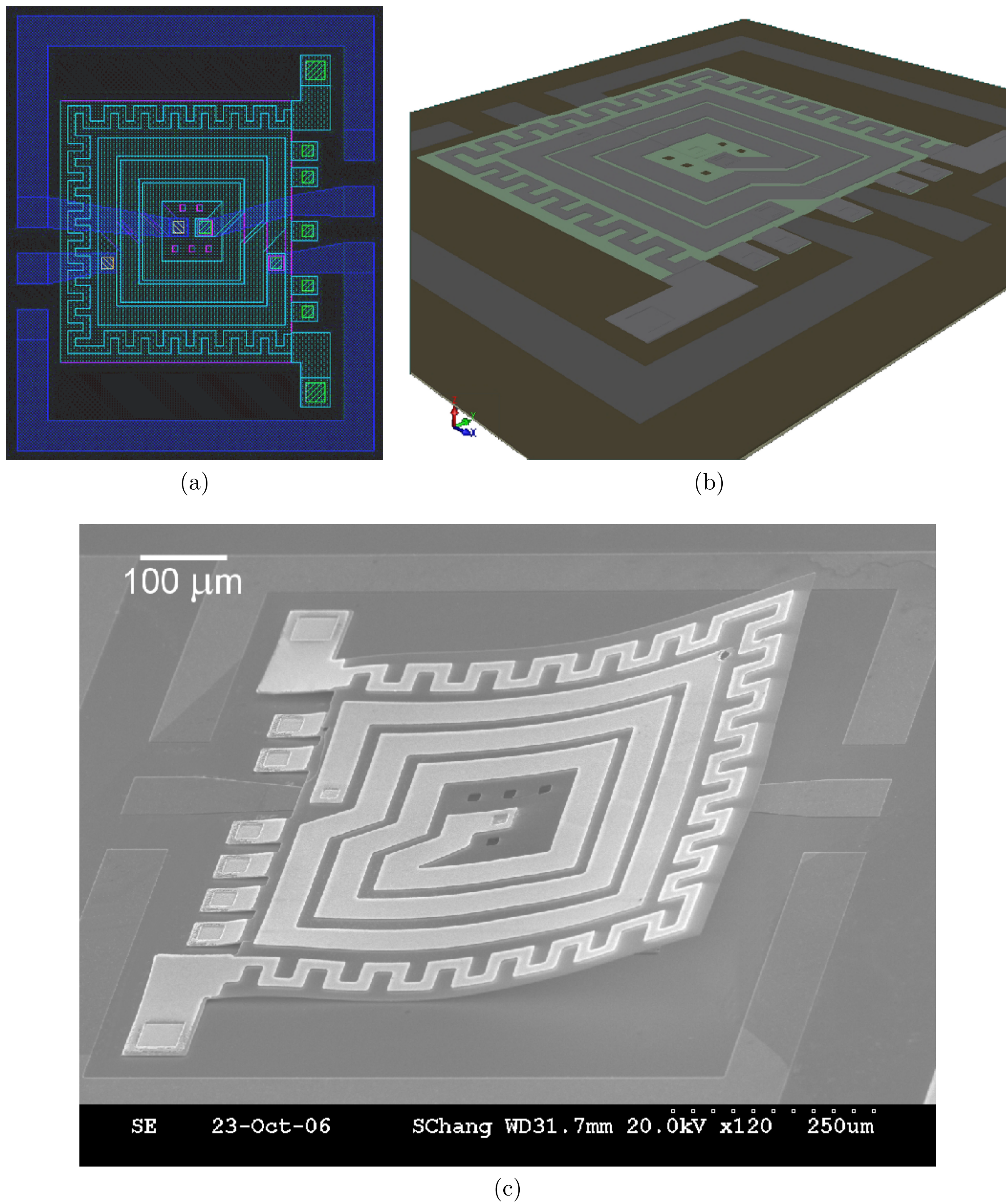


Fig. 6.18: (a) Layout, (b) Coventor schematic, and (c) SEM image of a resistively heated plate transformer design ($n = 3$ μm, $w = 50$ μm, $s = 10$ μm).

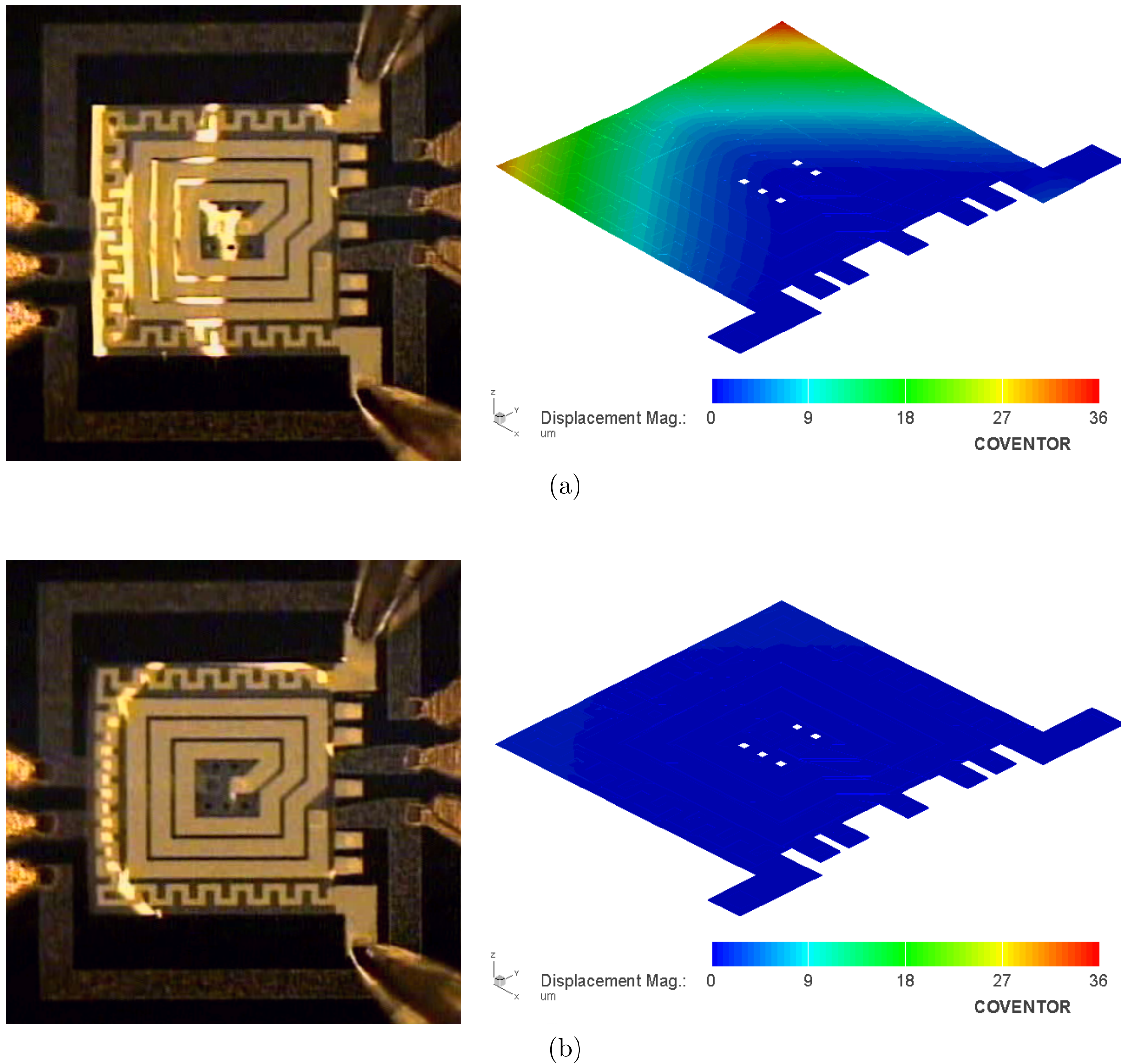


Fig. 6.19: (a) Microscope image Coventor simulation with no applied voltage and (b) microscope image and Coventor simulation with applied voltage of a fabricated resistively heated plate transformer design (n = 3 μm, w = 50 μm, s = 10 μm).

Another approach for moving the plate is using thermal actuators. Two thermal actuators are connected to opposite sides of the plate and anchored on the same edge as the plate. This design was implemented because it was shown in section 5.4.1 that bimorph thermal actuators are capable of hundreds of microns of vertical displacement. The layout is shown in Fig. 6.21(a) and the corresponding schematic in Coventor is shown in Fig. 6.21(b). An SEM image of a fabricated device is shown in Fig. 6.21(c). This transformer is laid out in a non-inverting configuration of the primary and secondary coils and has the following coil dimensions: $n = 2$ μm, $w = 50$ μm, $s = 10$ μm.

When the device is released, the plate curls upwards as shown in Fig. 6.22.

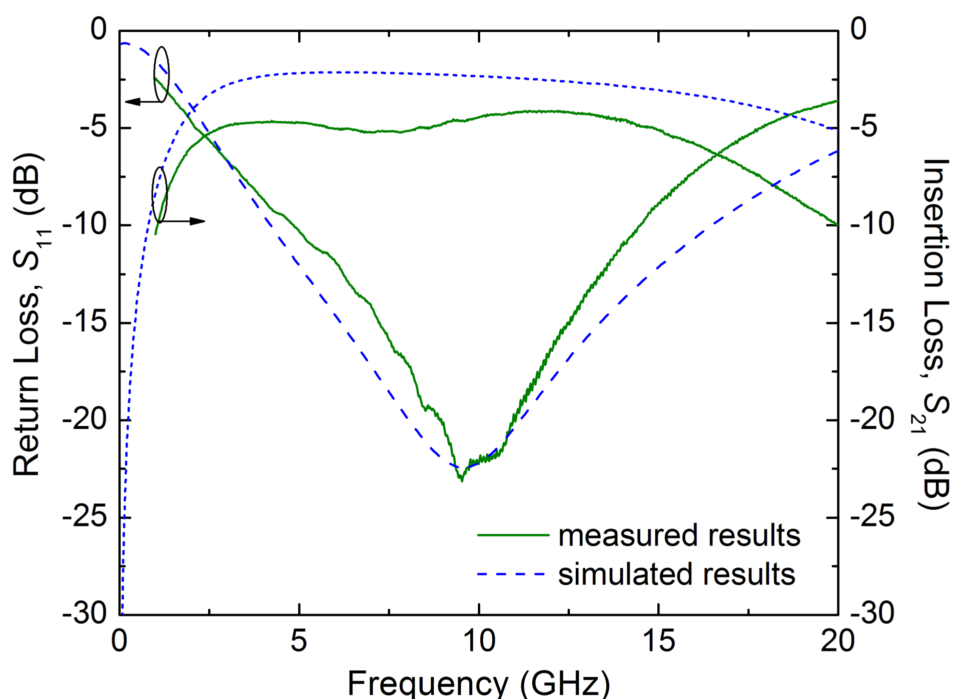
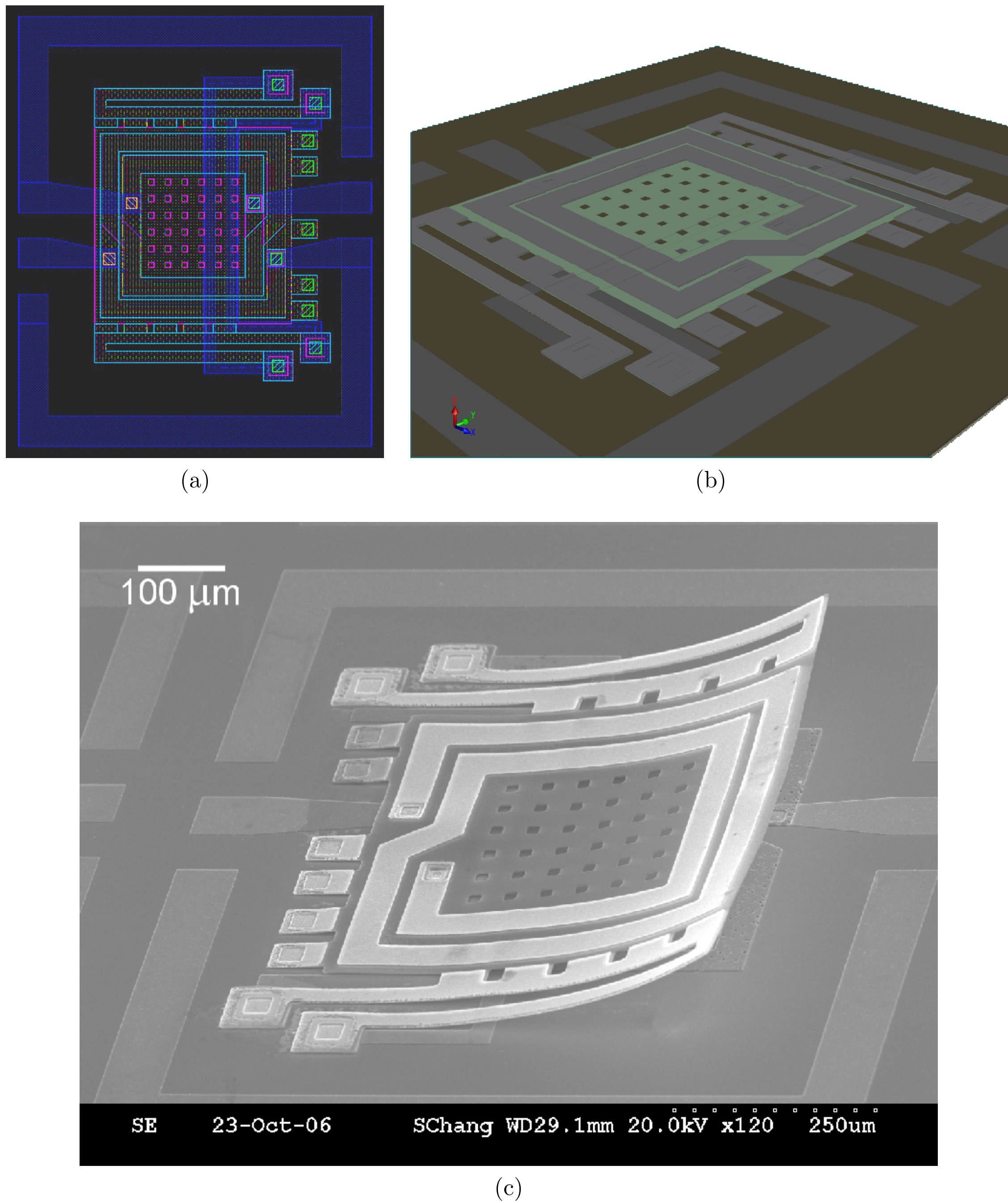


Fig. 6.20: Comparison of measured and simulated results of a thermally actuated plate transformer.



(a) (b)

(c)

Fig. 6.21: (a) Layout, (b) Coventor schematic, and (c) SEM image of a thermally actuated plate transformer design (n = 2 μm, w = 50 μm, s = 10 μm).

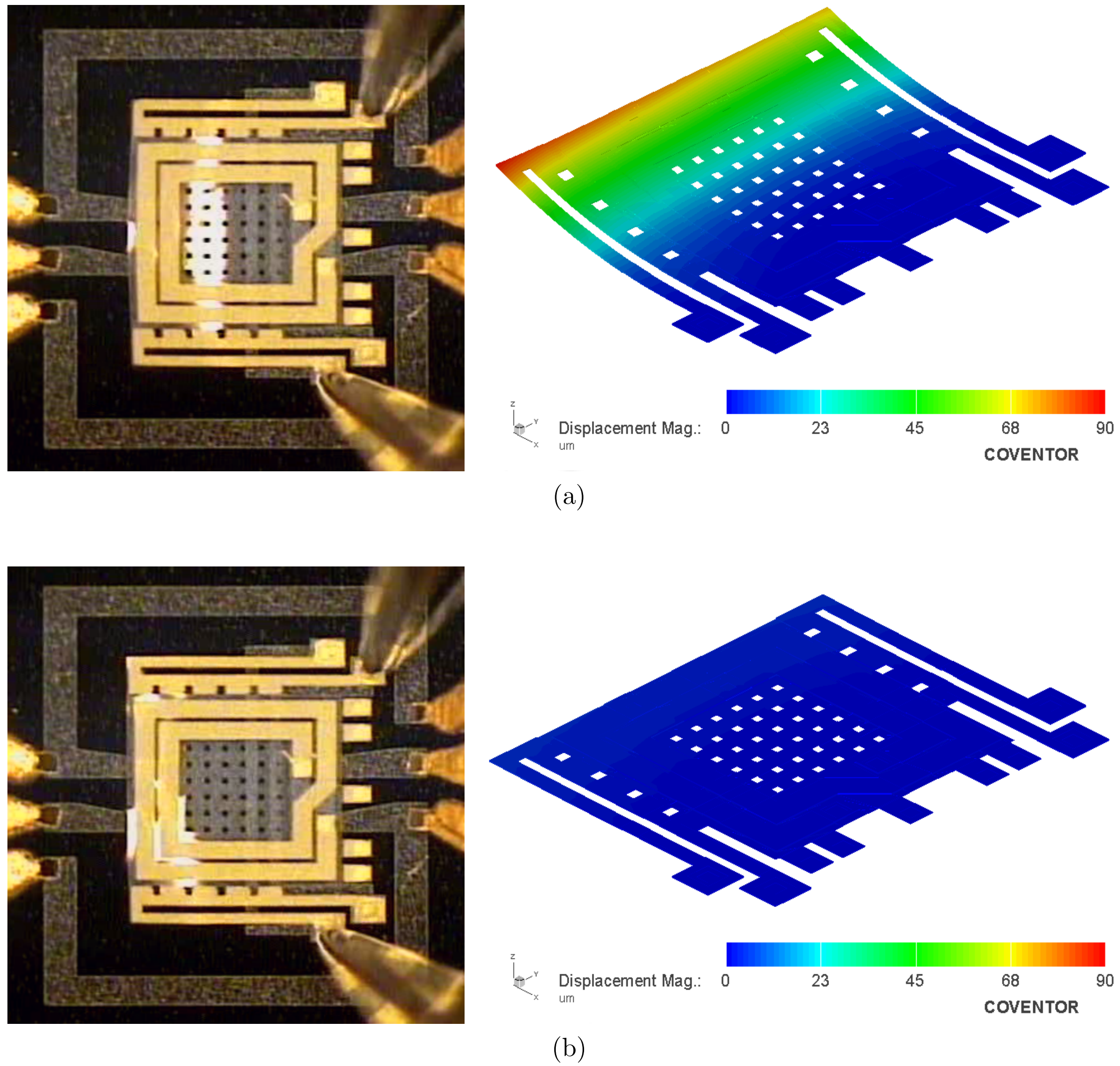


Fig. 6.22: (a) Microscope image and Coventor simulation with no applied voltage and (b) microscope image and Coventor simulation with applied voltage of a fabricated thermally actuated plate transformer design ($n = 3$ μm, $w = 50$ μm, $s = 10$ μm).

6.3 Simulations Involving Traditional RF Materials

In order to improve the RF performance of the devices fabricated in this work, high performance RF materials are required with the tradeoff of increased costs. The c-Si substrate can be replaced with alumina (Al_2O_3) which is a popular substrate for microwave circuits with a loss tangent of 0.0003 [70]. In addition, metals with higher conductivity can reduce the losses in the Al traces due to the skin effect ($\sigma_{Al} = 3.7\times10^7$ S/m). Gold (Au) has a higher conductivity ($\sigma_{Au} = 4.6\times10^7$ S/m) and is widely used for RF MEMS, but there are contamination issues so it will not be adopted in traditional CMOS processes. Copper (Cu) and silver (Ag) have even higher conductivities ($\sigma_{Cu} = 5.8\times10^7$ S/m, $\sigma_{Ag} = 6.3\times10^7$ S/m), but these materials oxidize rapidly so extra processing steps are required.

As a comparison to our measured results, the tunable inductor presented in Fig. 6.8 is analyzed. When voltage is applied to the 3-D coil, it is actuated and lies planar to the substrate. The Q is at a minimum due to the decrease in distance between the inductor and the substrate. This planar structure is simulated in Sonnet as shown in Fig. 6.23 with the trace labeled *Si+Al*. By changing the substrate from 10 Ω cm Si to alumina, the Q increases from 4.5 to 12.5 labeled as Al_2O_3+*Al*. Furthermore, if the metal is changed from Al to Au, a larger width of the peak Q is observed and is marked as Al_2O_3+*Au*. The improvement in Q is due to the decrease in losses of the current coupled to the substrate. The f_{res} is constant in all cases because the parasitic capacitance is dominated by the coupling between adjacent lines which does not change. These improvements are achieved by changing the material properties, and not the design of the inductor.

The RF MEMS transformer shown in Fig. 6.11(b) is simulated in the flat position. Since it was observed that changing the metal from Al to Au did not show much improvement in the performance at the frequency range we're analyzing, only the substrate was changed. Figure 6.24 shows the simulated S-parameters of the fabricated device dimensions on both silicon and alumina substrates. The power transferred from the primary to the secondary coil is improved by 3 dB on the alumina substrate. Depending on the application, this tradeoff between performance and cost needs to be evaluated.

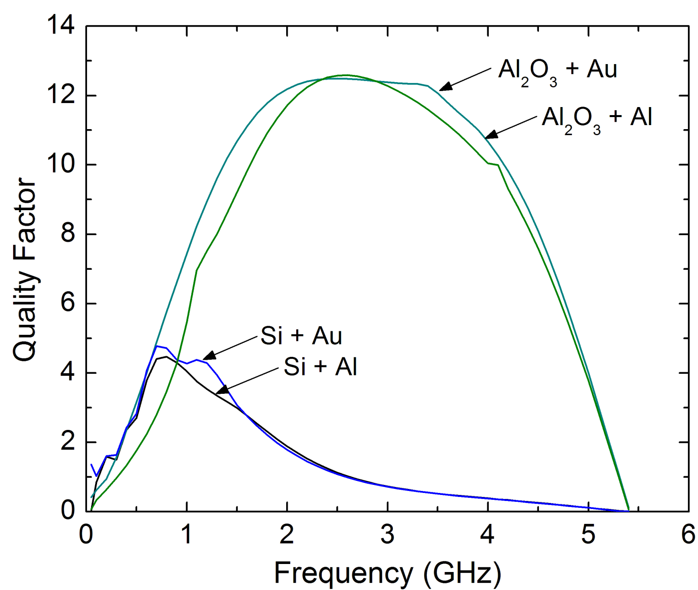


Fig. 6.23: Comparison of simulations using alumina and gold of a fabricated RF MEMS inductor. By changing the Si substrate to alumina, and the Al to Au, the Q improves from 4.5 to 12.5.

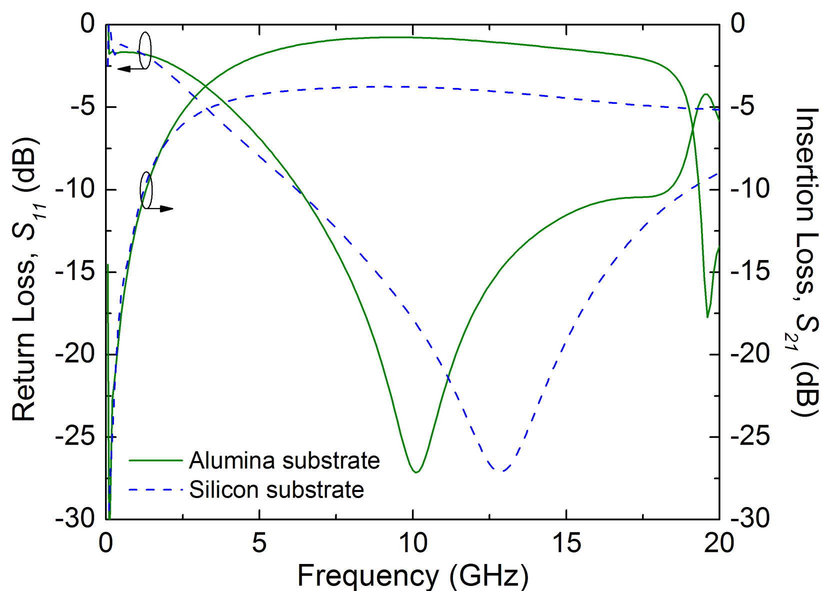


Fig. 6.24: Simulations indicate that by changing the Si substrate to alumina, the transmission loss from the coupling of the two coils improves by 3 dB.

6.4 Future Outlook of post-CMOS and MEMS

Commercial MEMS products include pressure sensors, accelerometers, position sensors in hard drives, and digital light processing (DLPs) in televisions to name a few. RF MEMS is one of the hottest development areas with the ultimate goal of developing a single-chip cell phone [115]. The MEMS-based IC products represented a US$8 billion market in 2005 and is estimated to grow exponentially in the next decades as shown in Fig. 6.25. There is a demand to integrate the electrical components using standard IC processes with the mechanical devices using micromachining techniques in order to realize a system on chip. Post-CMOS integration has received the most attention in CMOS-MEMS integration because industrial CMOS foundries can be exploited for MEMS. The main limitation posed by post-CMOS integration is a strict thermal budget that does not exceed a critical temperature where impurities can diffuse and materials properties can change. The research carried out in this work accommodates this temperature restriction by limiting the RF MEMS fabrication process to 150℃.

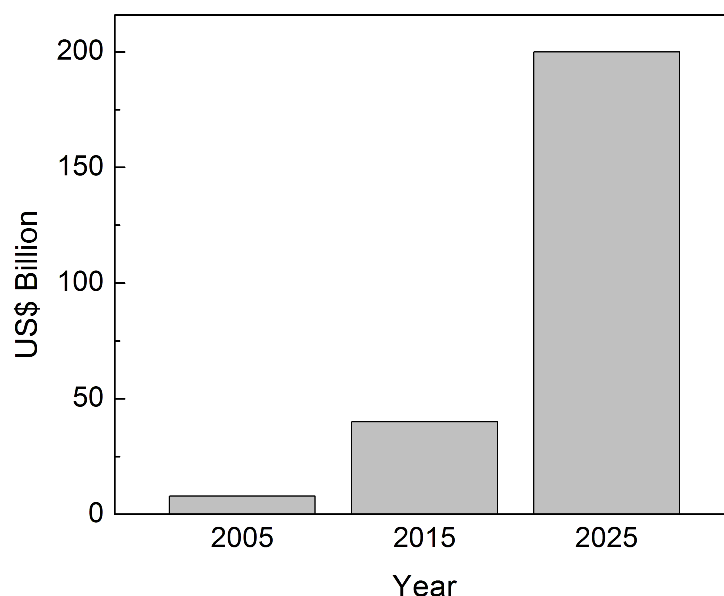


Fig. 6.25: In 2005, MEMS-based IC products created a US$8 billion market and is predicted to grow beyond US$40 billion in 2015 and US$200 billion in 2025 [115].

6.5 Summary

In this chapter, we have presented novel RF MEMS tunable inductors and transformers fabricated at a low temperature of 150℃. The top inductor coil is composed of an a-Si:H/Al bimorph and tunability is achieved by applying a low actuation voltage across the terminals. Due to the difference in CTE of the two layers, the inductor flattens as the applied voltage is increased. For the single tunable inductor design, a 32% tuning range from 5.6 to 8.2 nH is measured and with no applied voltage a peak Q of 15 is extracted. In addition, the mutual coupling of a transformer with the released top coil coupled with a planar coil could be tuned by 24%. Another transformer design with the top coil lying on a plate anchored at one edge is also presented, and this approach results in a narrow tuning range with higher precision. In conclusion, large displacement achievable by a-Si:H/Al bimorphs is explored to tune the magnetic coupling of a released coil. By applying a low DC voltage across the top coil, the mutual inductance or the coupling between two coils can be tuned. These devices are fabricated in a low temperature process that is ideal for RF MEMS integration where a low thermal budget is required.

Chapter 7

Conclusions

To conclude, the contributions of the research presented in this thesis is summarized. In addition, based on the results of our research, future work in various areas is proposed.

7.1 Contributions

The major contributions of this thesis can be summarized as follows:

- The process development for depositing low temperature PECVD undoped a-Si:H thick films with good uniformity and surface roughness is presented. The optoelectronic properties of our a-Si:H thick films are measured. The dielectric constant was determined by CV measurements and calculated to be 11.7, close to the value of c-Si. A dark conductivity of 1×10^{-10} S/cm and a photoconductivity of 1×10^{-6} S/cm was measured with an IV setup which correspond to values found in literature. The optical bandgap of a-Si:H was verified to be 1.72 eV from UV spectroscopy. The loss tangent of a-Si:H was estimated by measuring the loss of CPW lines fabricated on different a-Si:H film thicknesses and the results were fitted to EM simulations and a loss tangent of 0.005 at 4 GHz was extracted.

- A Teflon etch cell was machined to electrochemically etch pores in c-Si to form a porous Si layer. The applied current density and electrolyte composition were varied and the PS films were weighed before and after to determine the porosity and thickness, and pore sizes were determined by SEM analysis. The methodologies developed allowed effective dielectric constant and substrate resistivity to be estimated for improving the conductivity of c-Si substrates.

- Planar inductors were built-on undoped a-Si:H in a novel attempt to improve the isolation from the low resistivity Si substrate. A 56% increase in Q was measured by incorporating 1.5 μm of a-Si:H before depositing the underpass of the inductor. The fabrication process requires 3 masks.

- Planar inductors fabricated on porous Si have been investigated by other researchers. However, since PS quickly oxidizes in ambient, a high temperature oxidation step is carried out to protect the porous layer. The difference in our approach is we used PECVD a-Si:H as the encapsulating layer conforming to our goal of developing low temperature processes. Planar inductors were built on top of the porous Si and a-Si:H bilayer and showed 47% improvement in Q compared to the same device structure without a PS layer.

- Amorphous Si is proposed as a low temperature alternative to poly-Si for MEMS devices. The PECVD process conditions were optimized for a substrate temperature of 150℃ in order to achieve a reasonable deposition rate for thick films. The mechanical film stress of a-Si:H films with different thicknesses was measured and the compressive stress was found to decrease as film thickness increased. This result is attributed to the prolonged deposition time of thicker films resulting in an improved ordering of the amorphous network.

- Step coverage is crucial for the reliability of anchoring any MEMS device. The step coverage of PECVD a-Si:H was studied by SEM analysis and an aspect ratio of 0.8 was measured. PECVD a-Si:H presents this advantage as typical metal structural layers in MEMS are deposited by PVD processes which suffer from poor sidewall coverage and may require heating of the substrate or angling the substrate.

- The bimorph effect of a-Si:H and Al was explored and simple cantilever beams reaching 500 μm of vertical displacement were fabricated in a 2 mask process. This was useful for determining the thermomechanical simulation parameters required to design more complex structures and to predict the 3-D structure.

- Tunable RF MEMS inductors and transformers were fabricated on Si in a 6 mask process. The top coil is composed of an a-Si:H/Al bimorph and after etching away the sacrificial layer, the structure warps in a controllable manner. The tuning is achieved by applying a DC voltage and due to joule heating, the structure flattens to the original layout prior to release. A tunable inductor with a 32% tuning range from 5.6 to 8.2 nH and a peak Q of 15 on Si was measured. A transformer with a 3-D warped coil coupled with a planar coil demonstrated a 24% tuning range of mutual inductance. Since these devices are fabricated in a process with a maximum temperature of 150℃ , there is a lot of flexibility in terms of the sacrificial layer used and the wafer carrier. In addition, there is always the possibility of post-processing CMOS chips with the low temperature MEMS process presented.

7.2 Future Work

This work opens up many avenues of research that can be explored:

- Since the tunable inductors and transformers presented in this work reach hundreds of microns of vertical displacement, packaging is an immediate concern with obvious challenges. Nonetheless, various packaging techniques of MEMS devices are currently being developed [116]. Cavity clearance of hundreds of microns is not uncommon; wafer bonding is ultimately limited by the substrate thickness, and spin-on polymers can achieve up to 500 μm thick encapsulation layers [117]. In addition, more sophisticated commercial processes which offer a smaller minimum feature size will reduce the footprint and the maximum vertical displacement of the MEMS inductors and transformers can be optimized to ease packaging concerns. The RF performance of the MEMS devices should be compared before and after packaging.

- The inductors and transformers discussed in this research are only one of many MEMS devices that could be fabricated with this low temperature process presented. These fabricated prototype structures justify the possibility of substituting poly-Si with a-Si:H for low temperature processing. In addition, electrostatic actuation of MEMS devices incorporating an a-Si:H and metal bimorph could be designed to reduce power consumption.

- The focus of this research was to improve the performance of RF devices fabricated on low resistivity Si substrates to facilitate the possibility of post-CMOS integration and to address cost issues. The fabricated inductors demonstrated acceptable Q for a passive device integrated on Si. In order to improve the RF performance, the Si wafer can be substituted with alumina, quartz, or other high-performance RF substrates which will give higher Q and improved coupling as shown in the simulations. This tradeoff in performance comes with increased material costs.

Appendix A

Recipes Developed in this research for MEMS Processing

The following recipes were developed for the sub-150℃ RF MEMS fabrication process presented in this thesis. The recipes and process parameters provided in this appendix are specific to the equipment in the University of Waterloo's Centre for Integrated RF Engineering lab.

Amorphous Silicon PECVD Deposition

The recipe in Table A.1 was developed for the Trion PECVD load-lock system for depositing 1 μm of a-Si:H. In this system, the RF matching network cannot be tuned and in order achieve reasonable deposition rates for thick films, this recipe results in a high reflected power that can vary from 30 to 40 W. After deposition up to 2 μm thick films of a-Si:H, the chamber should be cleaned with the standard high and low pressure clean process for a total of 40 min. This system can accommodate up to 8" wafers with good film uniformity.

Table A.1: Amorphous Si PECVD recipe for depositing 1 μm at 150℃ (Trion load-lock 100 kHz parallel plate system with 8" electrode).

Step	**Description**	**Time (s)**	**Pressure (mT)**	**RF Power (W)**	**Ar (sccm)**	**SiH_4 (sccm)**
1	Purge	180	0	0	0	0
2	Ar Flush	180	250	0	30	0
3	Purge	180	0	0	0	0
4	Deposition	2000	750	37[a]	5	10
5	Purge	180	0	0	0	0
6	Ar Flush	180	250	0	30	0
7	Purge	180	0	0	0	0

[a]The RF power is the forward minus reverse power.

Amorphous Silicon RIE

The recipe in Table A.2 was developed for etching a-Si:H in the Trion RIE system. Two knobs on the back of the system offer coarse and fine manual tuning of the capacitors in the RF matching network. With this recipe, the reflected power can be tuned to less than 5%. The etch rate can be accurately timed and the etching of the film can be viewed through the peep hole on the front of the system (while wearing proper eye protection). This system can accommodate 8" wafers with good etching uniformity.

Table A.2: Amorphous Si RIE recipe for etching 1 μm (Trion parallel plate system with 8" electrode).

Step	**Description**	**Time (s)**	**Pressure (mT)**	**RF Power (W)**	**SF_6 (sccm)**
1	Purge	180	0	0	0
2	Etch	150	50	50	30
3	Purge	180	0	0	0

Aluminum DC Sputtering

Aluminum is sputtered in the Intlvac E-beam evaporator / DC magnetron sputtering system. This system can accommodate five 6" wafers in one deposition (holders are used

for smaller wafers). The recipe is automatically loaded from the computer which runs standard setup steps (warming the gun, sputtering with the shutter closed, etc.). The user adjustable parameters for the sputtering step are set as: Ar flow = 50 sccm, power = 500 W, time = 55 min giving a film thickness of 1 μm (deposition rate of 3 Å/s).

Aluminum Wet Etching

This recipe was developed for wet etching Al films. The etchant is called PAN (phosphoric-acetic-nitric) etch and is composed of H_3PO_4:H_2O:$C_2H_4O_2$:HNO_3 = 16:2:1:1. The PAN etch is heated in a beaker on the hot plate to 37℃ which etches 1 μm of sputtered Al in 4 min (etch rate of 4.2 nm/s). The etch rate is highly sensitive to the temperature, if the solution is heated a few degrees higher to 40℃, the Al film will etch much faster and the edges of the pattern may be rough.

Photolithography

The photolithography steps outlined in Table A.3 was developed to pattern the a-Si:H and Al layers with the Oriel mask aligner.

Table A.3: Photolithography steps for patterning with AZ 3312.

Step	Description	Process
1	Dispense photoresist	Use EFD fluid dispensing system with a syringe to cover the substrate with AZ 3312
2	Spin-on photoresist	Spin-on AZ 3312 at a speed of 3000 rpm for 30 s (this gives a thickness of 0.8 μm)
3	Soft-bake	Soft-bake the substrate on the vacuum hot plate at 90℃ for 60 s
4	Exposure	Expose the photoresist with the Oriel mask aligner for 12 s at 400 W/cm^2
5	Post-exposure bake	Bake the substrate after exposure on the vacuum hot plate at 110℃ for 60 s
6	Develop	Develop the substrate in AZ MIF 300 developer for 30 s at room temperature then rinse thoroughly with DI water

Spin-on Sacrificial Layer

For this low temperature process, Microchem's LOR 30A is used as the sacrificial layer. The steps for applying LOR 30A as a sacrificial layer are outlined in Table A.4. After the LOR is patterned, it is etched in the developer. Fresh developer ensures a consistent etch rate for a repeatable process.

Table A.4: Spin-on sacrificial layer recipe for Microchem's LOR 30A.

Step	**Description**	**Process**
1	Dehydration	Dehydrate the wafer on the vacuum hot plate at 150℃ for 120 s
2	Dispense	Use EFD fluid dispensing system with a syringe to cover the substrate with LOR 30A
3	Spin-on	Spin-on LOR 30A at a speed of 3000 rpm for 45 s (this gives a thickness of 3 μm)
4	Prebake	Prebake the substrate on the vacuum hot plate at 150℃ for 120 s
5	Full-bake	Bake the substrate in the vacuum oven from 150-190℃ (depending on the desired undercut) for 30 min
6	Imaging resist	Follow the steps outlined in Table A.3 to pattern the LOR 30A, use fresh developer and develop for an additional 90 s (total developing time of 120 s)
7	Etch	Fully etch the LOR 30A with the RIE recipe in Table A.5.

Patterning the Sacrificial Layer

After patterning the sacrificial layer, the LOR and AZ 3312 layers are etched with the recipe listed in Table A.5. LOR is etched by acetone, so an oxygen plasma is required to remove the AZ 3312 resist. The recipe is accurately timed to give 1.5 μm thick sacrificial layer. It's suggested that the LOR be etched in smaller timed intervals and measure the step height to achieve the desired thickness.

Table A.5: Sacrificial layer RIE recipe (Trion parallel plate system with 8” electrode).

Step	**Description**	**Time (s)**	**Pressure (mT)**	**RF Power (W)**	**CF_4 (sccm)**	**O_2 (sccm)**
1	Purge	180	0	0	0	0
2	Etch	45	50	50	2	48
3	Purge	180	0	0	0	0

Releasing Devices

In the final processing step, the devices are released by wet etching. Care must be taken to ensure that the MEMS devices do not stick to the substrate or become dislodged due to abrasive handling. In order to prevent stiction, when the substrate is moved from bath to bath, the substrate should be kept flat so that the devices remain covered in liquid. The devices should never be blown dry with a nitrogen gun because the anchored structures cannot withstand such high pressure. The process steps are outlined in Table A.6. If the Toussimis CO_2 dryer is used for drying the substrate, it must be clean and free of any acids before entering the chamber. If the sacrificial layer is not completely removed before using the CO_2 dryer, the results will not be good, and the substrate should be kept in the PG remover for a longer period of time in step 1.

Table A.6: Release process for removing LOR 30A.

Step	**Description**	**Process**
1	Remove LOR 30A	Heat 3 petri dishes of PG remover to 50℃, place the device in each dish for 120 s, and gently remove and place into the next clean solution
2	Clean with IPA	Prepare 3 petri dishes of pure isopropyl alcohol (IPA), place the device in each dish for 120 s, and gently remove and place into the next clean solution
3	Drying process	The substrate can be dried in the convection oven at 120℃ for 30 min or in the CO_2 dryer

Appendix B

Calculating the Hydrogen Content in a-Si:H

One non-destructive technique to calculate the hydrogen content of a-Si:H is through Fourier Transform infrared spectroscopy where a thin film is deposited on a c-Si substrate. In the infrared spectrum of a-Si:H, three main absorption regions exist: wagging mode at 640 cm^{-1}; doublet dihydride bending or scissor modes at 840-890 cm^{-1}; and two stretching modes at 2000 and 2100 cm^{-1}. The absorption at these modes is related to the hydrogen content in the bulk of the material through the strengths of oscillation and can be calculated from:

$$N_H = AI = A \int \frac{\alpha}{\omega} d\omega \tag{B.1}$$

where A is a proportionality constant (related to the inverse of the oscillator strength and determined empirically), I is the integrated absorbance, α is the absorption coefficient, ω is the wavenumber in cm^{-1}, and the integral is over the absorption band of interest. The wagging mode absorption is related to the total hydrogen content independent of the bonding configurations[1]:

$$N_{630} = A_{630} \int \frac{\alpha_{630}(\omega)}{\omega} d\omega \tag{B.2}$$

[1]A.A. Langford, M.L. Fleet, B.P. Nelson, "Infrared absorption strength and hydrogen content of hydrogenated amorphous silicon," *Phys. Rev. B*, vol. 25, pp. 13367-13377, 1992

where $A_{630} = 2.1 \times 10^{19}$ cm^{-2}.

The hydrogen content in at.% is calculated by:

$$C_H = \frac{N_H}{N_H + N_{Si}} \tag{B.3}$$

where $N_{Si} = 5 \times 10^{22}$ cm^{-2}.

The transmission is related to the absorption coefficient by:

$$T = \frac{4T_0 e^{-\alpha d}}{\left(1 + T_0\right)^2 - \left(1 - T_0\right)^2 e^{-\alpha d}} \tag{B.4}$$

There is a mismatch in the refractive index in the infrared regime between a-Si:H and c-Si which gives rise to interference fringes in the transmission spectrum. Therefore, substrate absorption needs to be removed by dividing the transmission of the sample by that of the bare c-Si substrate and multiplying by 0.54, which is the transmission of c-Si in the non-absorbing regions.

Appendix C

Extracting the Optical Bandgap of a-Si:H

When light is incident on a sample, some light is transmitted, absorbed, and reflected as shown in Fig. C.1.

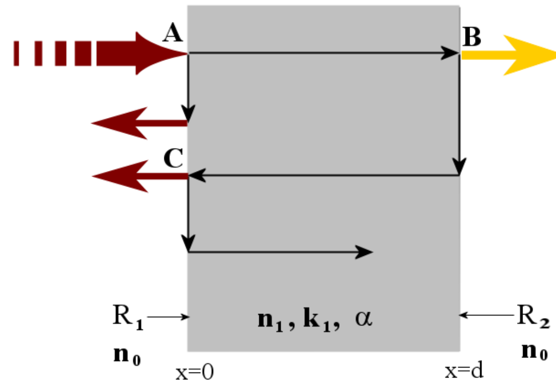


Fig. C.1: Schematic representation of absorbed, transmitted and reflected light in a thin film.

When I_i is incident on a material, some light is reflected at A, $I_{r1} = R_1 I_i$, and $(1 - R_1)\, I_i$ travels through the sample and is attenuated. The intensity of the light at B is $(1 - R_1)\, I_i e^{-\alpha d}$ and some light is transmitted where $I_{t1} = (1 - R_2)\,(1 - R_1)\, I_i e^{-\alpha d}$. At C, some of the light reflected at B is back-reflected, etc. When all of the components

are summed, the transmittance is approximated as:

$$T = \frac{I_t}{I_i} = \frac{(1 - R_1)(1 - R_2)^2 e^{-\alpha d}}{1 + R_1 R_2^2 e^{-\alpha d} - 2\sqrt{R_1 R_2} e^{-\alpha d} cos\phi} \tag{C.1}$$

and when the reflectivity of both sides of the material are equal, $R_1 = R_2 = R$, the transmittance is calculated by:

$$T = \frac{(1 - R)^2 e^{-\alpha d}}{1 + R^2 e^{-2\alpha d} - 2R\, e^{-2\alpha d} cos\phi} \tag{C.2}$$

where $\phi = \frac{4\pi n_1 d}{\lambda}$, α is the absorption coefficient, and R is the reflection coefficient:

$$R = \frac{(n_0 - n_1)^2 + k_1^2}{(n_0 + n_1)^2 + k_1^2} \tag{C.3}$$

where k is the extinction coefficient related to the absorption coefficient by $\alpha = \frac{4\pi k_1}{\lambda}$.

The reflection coefficient for air/dielectric boundary is:

$$R = \left(\frac{1 - n}{1 + n}\right)^2 \tag{C.4}$$

The absorption coefficient can be used to calculate the optical bandgap of a semiconductor. Light with energy higher than the bandgap is absorbed. For indirect semiconductors like Si, $\alpha^{1/2}$ is plotted versus hv and the extrapolated intercept on the hv axis yields the optical bandgap. This is referred to as a Tauc plot:

$$\sqrt{\alpha hv} = A\,(hv - E_{opt}) \tag{C.5}$$

$$\alpha = -\frac{1}{d}\left[ln\left(\frac{\sqrt{(1 - R)^4 + 4T^2R^2} - (1 - R)^2}{2TR^2}\right)\right] \; or \; \alpha = -\frac{1}{d}\left[ln\left(\frac{T}{0.59359217}\right)\right] \tag{C.6}$$

List of Thesis Publications

Journal Papers:

[J1] S. Chang, S. Sivoththaman, "A novel RF MEMS inductor incorporating an amorphous silicon bimorph," *IEEE Electron Device Lett.*, vol. 27, pp. 905-907, 2006.

[J2] S. Chang, S. Sivoththaman, "Development of low temperature MEMS process with PECVD amorphous silicon," *J. Micromech. Microeng.*, vol. 16, pp. 1307-1313, 2006.

[J3] S. Chang, S. Sivoththaman, "On-chip inductors incorporating porous silicon and amorphous silicon for RF integrated circuits," *J. Vac. Sci. Tech. A*, vol. 24, pp. 841-845, 2006.

[J4] S. Chang, S. Sivoththaman, "Low loss inductors built-on PECVD intrinsic amorphous silicon for RF integrated circuits," *Can. J. Electr. Comput. Eng.*, vol. 30, pp. 69-72, 2005.

Oral Conference Presentations:

[C1] S. Chang, S. Sivoththaman, "A tunable RF MEMS transformer on silicon," *7th IEEE Topical Meeting Si Monolithic ICs.*, Long Beach, USA, Jan. 10-12, 2007 (**Student paper award, 2nd place**).

[C2] S. Chang, S. Sivoththaman, "Fabrication of a tunable RF MEMS inductor on silicon in a sub-150°C process," *32nd Int. Conf. Micro- and Nano-Eng.*, Barcelona, Spain, Sept. 17-20, 2006.

[C3] S. Chang, S. Sivoththaman, "On-chip inductors incorporating porous silicon and amorphous silicon for RFICs," *14th Can. Semi. Tech. Conf.*, Ottawa, Canada, Aug. 16-19, 2005.

[C4] S. Chang, S. Sivoththaman, "Low loss inductors fabricated on PECVD intrinsic amorphous silicon for RFICs," *18th IEEE CCECE Conf.*, pp. 329-333, Saskatoon, Canada, May 1-4, 2005 (**Student paper award**).

List of Acronyms

a-Si:H	hydrogenated amorphous silicon
AC	alternating current
c-Si	crystalline silicon
CMOS	complementary metal-oxide-semiconductor
CPW	coplanar waveguide
CTE	coefficient of thermal expansion
CV	capacitance-voltage measurement
CVD	chemical vapor deposition
DC	direct current
DLP	digital light processing
EL	electroluminescence
EM	electromagnetic
emf	electromotive force
EPID	electronic portal imaging device
f_{res}	self-resonance frequency
FTIR	Fourier transformer infrared
GSG	ground-signal-ground
HWCVD	hot-wire chemical vapor deposition
IC	integrated circuit
IV	current-voltage measurement
L	inductance
LIGA	X-ray lithography, electroplating, and molding
LNA	low noise amplifier

LPCVD low pressure chemical vapor deposition
μc-Si microcrystalline silicon
MEMS microelectromechanical systems
MIM metal-insulator-metal
MOS metal-oxide-semiconductor
nc-Si nanocrystalline silicon
OLED organic light emitting diode
PAN phosphoric-acetic-nitric acid
PDMA plastic deformation magnetic assembly
PECVD plasma enhanced chemical vapor deposition
PL photoluminescence
poly-Si polysilicon
PolyMUMPs polysilicon multi-user MEMS process
PS porous silicon
PVD physical vapor deposition
Q quality factor
RCA Radio Corporation of America
RF radio frequency
RFICs radio frequency integrated circuits
RIE reactive ion etching
S_{11} return loss
S_{21} insertion loss
S-parameters scattering parameters
SEM scanning electron microscope
SoC system on chip
TFT thin film transistor
UV ultraviolet
VCO voltage-controlled oscillator
Z-parameters impedance parameters

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