Design of CMOS Distributed Amplifiers

for Broadband Wireline and Wireless Communication Applications

by

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Abstract

While the RF building blocks of narrowband system-on-chip designs have increasingly been created in CMOS during the past decade, researchers have started to look at the possibility of implementation of broadband transceivers in CMOS technology. High speed optical links with operating frequencies of up to 40 GHz and ultra wideband (UWB) wireless systems operating in 3 to 10 GHz frequency band are examples of these broadband applications. CMOS offers a low fabrication cost, and a higher level of integration compared with compound semiconductor technologies that currently claim broadband RFIC applications.

In this work, we focus on the design of broadband low-noise amplifiers: the fundamental building blocks of high data rate wireline and wireless telecommunication systems. A well established microwave engineering technique -distributed amplification- with a potential bandwidth up to the cut-off frequency of transistors is employed. However, the implementation of distributed amplifiers in CMOS imposes new challenges, such as gain attenuation because of substrate loss of on-chip inductors, a typical large die area, and a large noise-figure. These problems have been addressed in this dissertation as described below.

On-chip inductors, the essential components of the distributed amplifiers' gate and drain transmission lines, dissipate more and more power in silicon substrates as well as in metal lines as frequency increases, which in turn reduces the gain and deteriorates the input/output matching. Using active negative resistors implemented by a capacitively source degenerated configuration, we have fully compensated the loss of the transmission

lines in order to achieve a flat gain of 10 dB over the entire DC-to-44 GHz bandwidth.

We have addressed another drawback of distributed amplifiers, large die area, by utilizing closely-placed RF transmission lines instead of spiral inductors. Because of a more compact implementation of transmission lines, the area of the distributed amplifiers is considerably reduced at the expense of extra design steps required for the modeling of the closely-placed RF transmission lines. A post-layout simulation method is developed to take into account the effect of inductive and capacitive coupling by incorporating a 3D EM simulator into the design process. A 9-dB 27-GHz distributed amplifier has been fabricated in an area as small as 0.17 mm^2 using 180nm TSMC's CMOS process.

For wireless applications (UWB), a very low-noise figure is required for the broadband preamplifier. Conventional distributed amplifiers fail to provide a low noise figure mainly because of the noise injected by the terminating resistor of the gate transmission lines. We have replaced the terminating resistor with a frequency-dependent resistor which trades off the low frequency input matching of the distributed amplifier (not required for UWB) with a better noise performance. Our proposed design provides a gain of 12 dB with an average noise figure of 3.4 dB over the entire 3-10 GHz band, advancing the state-of-the-art implementation of broadband LNAs.

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Contents

1 Introduction **1**

1.1 Motivation 1

1.2 Broadband Communication Applications 4

1.2.1 Optical Communication Systems Overview 4

1.2.2 Ultra Wideband Technology Overview 13

1.3 Semiconductor Technologies for RF ICs 16

1.4 Thesis Outline 20

2 Broadband Amplification Techniques **22**

2.1 Inductive Peaking 22

2.2 Capacitive Peaking 25

2.3 Negative Feedback 29

2.4 Distributed Amplification 32

2.4.1 Distributed Amplifier Analysis 32

2.4.2 Distributed Amplifier Design Guideline 39

2.4.3 Previous Research on CMOS DAs 40

3 Broadband RF CMOS Modeling 48

3.1 Radio Frequency MOSFET Modeling 48

3.2 On-Chip Spiral Inductor Modeling 53

3.2.1 Loss Mechanisms in On-Chip Inductors 54

3.2.2 EM-Based On-chip Inductor Modeling 56

3.2.3 Physical-Based On-chip Inductors Model 57

3.2.4 Broadband On-Chip Inductor Modeling 61

4 Area-Efficient DA Design 64

4.1 Co-simulation Methodology 65

4.1.1 Final S-parameters Calculation 67

4.1.2 Case Study 68

4.2 Area-Efficient CMOS DA 73

4.3 Measurement Results 77

5 Loss-Compensated DA Design 82

5.1 Lossy On-Chip Inductor 83

5.2 Analysis of Lossless/Lossy/Loss-Compensated Transmission lines 84

5.3 Negative Resistor Implementation 88

5.4 40 GHz CMOS DA Design 90

5.5 Implementation and Measurement Results 91

6 Low-Noise Broadband Amplifier Design 98

6.1 Low-Noise DA Design 98

6.1.1 Noise Sources in CMOS DAs 99
6.1.2 Proposed Low-Noise DA Technique 100
6.1.3 Implementation and Measurement Results 103
6.2 Non-Distributed Wideband LNA Design 108
6.2.1 Ultra-Wideband LNA Design 110
6.2.2 Effect of Gate-Drain Capacitance 110
6.2.3 Proposed Input Matching Technique 112
6.2.4 Flat Gain 117

7 Conclusions 121

7.1 Publications 124

A Lumped-Element Modeling of CMOS DAs 128

A.1 Why Lumped-Element Modeling? 128
A.2 Lumped-Element DA Analysis 131
A.2.1 ABCD Transmission Matrix and Properties 131
A.2.2 Final Two-Port Network 133
A.3 Image Impedance Termination 137
A.3.1 Definition and Calculation of Image Impedance Matrix 137
A.3.2 Realization of Image Impedance Matrix 140
A.4 Simulation Results and Comparison 144
A.5 Summary 144

B Glossary of Mathematical Symbols 147

List of Tables

1.1 SONET/SDH Standards 5

2.1 Summary of Reported Performance of CMOS Distributed Amplifiers. . . . 41

4.1 Area Efficiency of Reported Performance of CMOS Distributed Amplifiers. 81

6.1 Optimized values of the proposed low-noise amplifier circuit components. . 118

7.1 Comparison of this work with previous CMOS Distributed amplifiers . . . 123

List of Figures

1.1 All-broadband wireline and wireless communication access networks. 2

1.2 Block diagram of optical communication system. 7

1.3 Structure of single-mode optical fiber. 8

1.4 RZ and NRZ binary data streams. 9

1.5 Frequency spectrum of random binary data. 11

1.6 Time and frequency representation of narrowband and wideband signals. . 13

1.7 UWB Spectrum 14

1.8 Narrowband and Ultra Wideband transceiver architecture. 15

1.9 Application spectrum of semiconductor technologies 17

1.10 Cross-section of a typical CMOS process. 19

2.1 Inductive and capacitive peaking techniques. 23

2.2 Inductively peaked amplifier's frequency response. 24

2.3 Capacitively peaked amplifier's frequency response. 27

2.4 Block diagram of amplifier with negative feedback. 29

2.5 Feedback amplifier frequency response for several values of feedback (β). . 31

2.6 Schematic diagram of distributed amplifier. 33
2.7 Transmission line circuit for gate line of distributed amplifier 34
2.8 Transmission line circuit for drain line of distributed amplifier 35
2.9 Differential DA. 43
2.10 Distributed amplifier Darlington cell 44
2.11 Coplanar stripline structure in CMOS technology. 45
2.12 Coplanar waveguide structure in CMOS technology. 46

3.1 Radio frequency MOSFET model. 49
3.2 Distributed radio frequency MOSFET model. 50
3.3 Small signal model of RF MOS transistors including gate resistor. 51
3.4 Multi-Finger MOSFET Layout. 52
3.5 Layout of square and octagonal spiral inductors. 53
3.6 Cross-section of typical CMOS substrate layers. 56
3.7 π circuit model of on-chip inductor. 58
3.8 Modeling frequency-depends series inductor and resistor. 63

4.1 Modeling of passive part of RF ICs. 66
4.2 Adjacent square spiral inductors layout. 69
4.3 Results Comparison 70
4.4 Post and pre-layout simulation results 72
4.5 Interconnects mutual inductors 75
4.6 EM simulation results for unloaded closely-placed transmission lines. . . . 76

4.7 Die microphotograph and measurement results 78

4.8 Measured noise figure of proposed twenty-stage CMOS DA. 79

5.1 Schematic diagram and power gain of transmission line 85

5.2 Negative Resistance Implementations 88

5.3 S-parameters simulation results for (un)compensated CMOS DAs. 92

5.4 Schematic diagram of loss-compensated DA gain cell. 93

5.5 Chip layout of loss-compensated CMOS DA. 94

5.6 Die microphotograph of loss-compensated CMOS DA. 94

5.7 Measured S-parameters 95

5.8 Measured noise figure of loss-compensated CMOS DA. 96

5.9 Stability K factor of loss-compensated CMOS DA. 97

6.1 Low-noise DA. 102

6.2 Noise figure versus input matching. 103

6.3 Schematic diagram and layout of Proposed Low-noise DA. 104

6.4 Die microphotograph of low-noise CMOS DA. 105

6.5 Measured and simulated S-parameters of low-noise CMOS DA. 106

6.6 Measured noise figure of low-noise CMOS DA. 107

6.7 Measured 1-dB compression points of low-noise CMOS DA. 107

6.8 Schematic diagram of inductively source degenerated amplifier 109

6.9 Effect of C_{gd} on input impedance. 111

6.10 Input impedance of LNA as a function of LS. 113

6.11 Input impedance of LNA as a function of CP. 114
6.12 Input impedance of LNA as a function of M1 width (WNFET1). 115
6.13 Input impedance of LNA as a function of M2 width (WNFET2). 116
6.14 Complete schematic diagram of LNA excluding biasing circuitry. 117
6.15 Wideband LNA. 118
6.16 Proposed UWB LNA S-Parameters. 120
6.17 Proposed LNA noise figure. 120

A.1 Stage k of a uniform N-stage CMOS DA. 132
A.2 Final two-port network. 134
A.3 Definition of scalar and matrix image impedances. 136
A.4 Simulated amplifier voltage gain 141
A.5 Magnitude of Z_{11} (logarithmic scale) as a function of frequency. 143
A.6 Simulated amplifier voltage gain 145

Chapter 1

Introduction

1.1 Motivation

Ever increasing demand for ultra high speed connections drives the telecommunication industry toward the deployment of broadband wireline and wireless networks. An ultimate broadband communication network is the one that distributes the broadband signal to each one of the customers' devices at their premises. As depicted in Figure 1.1, the proposed all-broadband communication network consists of two sub-networks:

- a broadband wireline network that delivers the signal to the premises, and
- a broadband wireless network that distributes the signal within the premises.

The second network needs to be implemented over a wireless connection as many of today's electronic devices are portable.

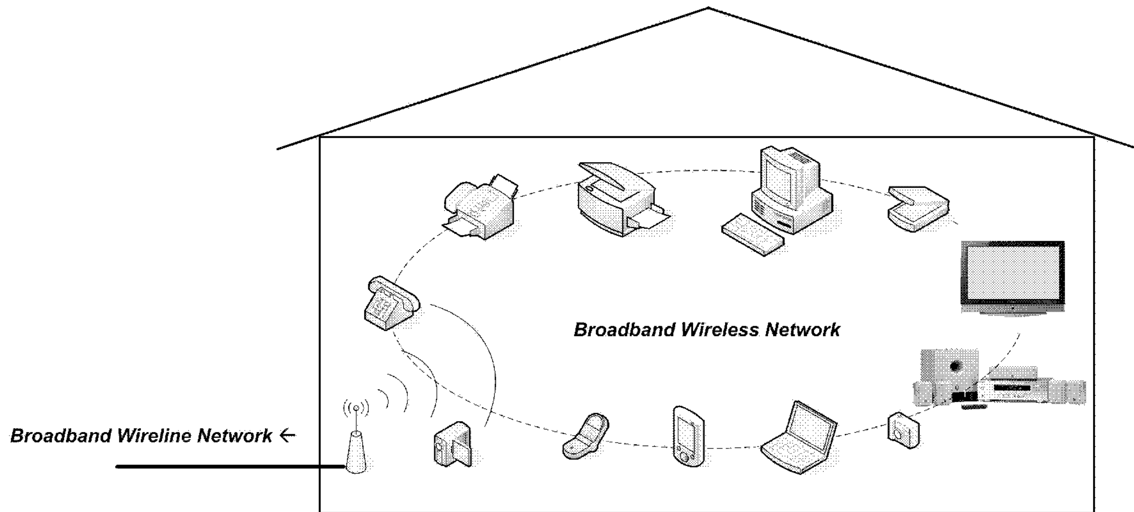


Figure 1.1: All-broadband wireline and wireless communication access networks.

The wireline broadband networks are locally delivered through cable (cable modem) and telephone (DSL) networks in many areas, while optical networks are responsible for providing the broadband data for these local networks. In the remote areas that are out of reach of the optical networks, Satellite Internet is considered as the only available choice for broadband networking. Cable and DSL connections generally deliver a minimum of around 150 Kbps and an average max of around 1 Mbps for cable and 2 Mbps for DSL. Cable and DSL broadband connections will reach their limits for future communication services, especially those that transfer videos in real time. As the demand for internet connections with higher speed increases, the only solution is to extend the optical network closer to customers' homes and businesses. Ultimately in the future, broadband fiber optics networks will reach the customers' premises, eliminating the need for Cable and

DSL networks. Because of the extremely large bandwidth of an optical fiber, all-optical access networks that reach customers' homes and offices will provide ultra high-speed data over a highly reliable and secure communication channel to every customer. In *Fiber-to-the-Home (FTTH)* technology, a single optical fiber delivers all communications needs to the customer's home or office as a bundled service such as in the so-called Triple Play service which delivers high-speed Internet, television, and telephone service over a single broadband connection.

For the second part of the broadband network, which distributes the broadband signal within the premises wirelessly, the current market solution is WiFi or Bluetooth technologies. WiFi is a technology for wireless local area networks (WLAN) based on the IEEE 802.11 specifications. The maximum achievable speed is 54 Mbps. Bluetooth is an industrial specification for wireless personal area networks (PANs), also known as IEEE 802.15.1 with a maximum achievable speed of 2.1 Mbps. Newly declassified Ultra Wideband technology seems to be the most promising technology with the capability of transferring data at very high data rates. UWB transmitters do not modulate the signal with a carrier frequency like traditional narrowband technologies (WiFi, WiMAx, CDMA, ..) but transmit very-short-duration pulses, often of durations of less than one nanosecond, that represent the stream of binary data. A UWB signal is compressed in time, and spread over a very wide bandwidth (3GHz to 10 GHz). UWB can transmit and receive wireless signals at rates in excess of several hundred Mbits per second, while consuming a small amount of power and without interfering with existing communications signals.

To decrease the deployment cost of optical networks, the introduction of inexpensive and mass-produced optical/electrical components to send, transfer, receive, and convert the optical signal is essential. The same argument is valid for the wireless sub-network. The lower the cost of the UWB transceivers, the more wide spread use of UWB-enabled devices will become. Therefore, researchers are concentrating on the full integration of broadband transceivers in a low-cost high-yield semiconductor technology. This dissertation is devoted to the design of broadband amplifiers, the fundamental building blocks of high data-rate wireline and wireline communication systems, in a standard CMOS process.

1.2 Broadband Communication Applications

Concerning the major application of broadband amplifiers, this section reviews the broadband optical and UWB communication systems. The two basic differences between wireless and optical communication systems are the transmission medium and the carrier frequency. In wireless communication, the transmission medium is air and the carrier frequency is in the range of a few GHz , whereas in optical communication optical fiber and the optical carrier frequency is 200 THz. The goal is to arrive at the specifications of the broadband amplifiers needed for the proper operation of these broadband communication systems.

1.2.1 Optical Communication Systems Overview

In today's telecommunication networks, optical fibers are mostly used for transferring high volumes of digital data among the bases, with each base distributing data among its users

Bit Rate (Mbps)	SONET	SDH
51.84	OC-1	-
155.52	OC-3	STM-1
622.08	OC-12	STM-4
1244.16	OC-24	
2488.32	OC-48	STM-16
9953.28	OC-192	STM-64
39813.12	OC-768	STM-256

Table 1.1: SONET/SDH Standards .

through a local area network (Cable and DSL LAN). Although optical communication systems are in service for base-to-base communication, soon every internet user will need a communication link with the capacity of a few Gbps, thereby increasing the demand for technologies such as FTTH and FTTB. Table 1.1 summarizes the evolution of fiber optics systems through SONET/SDH standards [1]; the speed of optical fiber communication has increased from a few Mbps to tens of Gbps of data in recent years [1]. As the electronic systems that can process the data at such a high bit rate are essential for the construction of these optical standards, bit rates over 40 Gbps are difficult to achieve using current semiconductor technologies.

An optical communications system is composed of three components: an optical trans-

[1]Synchronous Digital Hierarchy (SDH) and Synchronous Optical Network (SONET) refers to a group of fiber-optic transmission rates that can transport digital signals with different capacities.

mitter, a communication channel, and an optical receiver [2] which will be discussed in detail in the following sections.

Optical System

Figure 1.2 is the block diagram of a complete optical system, including its optical and electrical building blocks. An optical transmitter converts an electrical signal into an optical form and feeds the resulting signal to an optical fiber. In the transmitter part, the data , received in the form of parallel low-speed channels, is converted to serial data by a multiplexer (MUX). The serial data streams are then retimed by the clock signal that is generated by a frequency synthesizer. A laser diode converts the electrical data to optical form. The optical signal (light) is then transferred by an optical fiber.

The role of the optical communication channel is to transfer the optical signal from the transmitter to the receiver without distortion. Optical fibers are ideal candidates for transferring light because their attenuation rates are as small as $0.2dB/km$ for the optical signal. Typically, an optical fiber is a cylindrical dielectric waveguide that is most commonly fabricated by using high-purity, low-loss materials such as silica glass [4]. Fiber optics offers a wide variety of core sizes to match the diverse requirements of fiber systems. The structure of a fiber consists of an inner core, the cladding, and a protective buffer coating, illustrated in Figure 1.3. The core is the area through which light travels, carrying data. Surrounding the core is the cladding, also made of glass but with a lower refractive index than the core. The lower refractive index causes the light in the core to reflect off the cladding and remain in the core. To protect the fiber core and the cladding, several layers

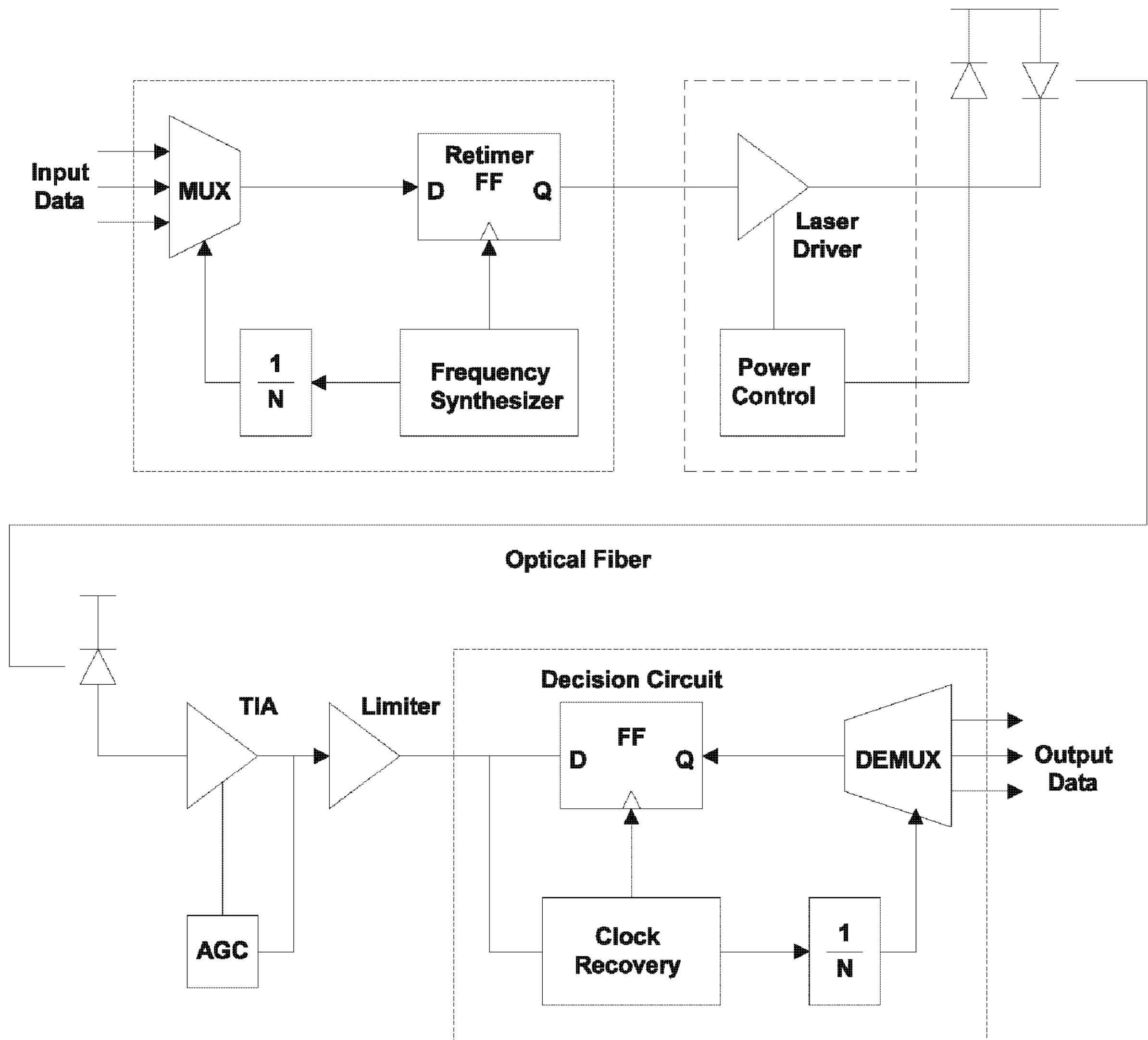


Figure 1.2: Block diagram of optical communication system [3].

of plastic coatings are applied to preserve the strength. Buffer coatings are available in two sizes: 250 microns and 900 microns. Fibers show the lowest attenuation in the vicinity of wavelengths of 1300 nm and 1550 nm. The fibers are modified in such a way that their

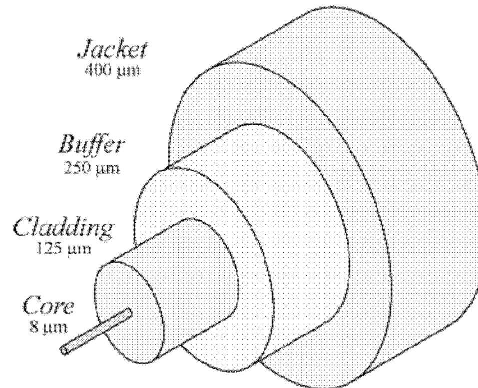


Figure 1.3: Structure of single-mode optical fiber.

minimum dispersion occurs at the wavelengthes where they exhibit the lowest attenuation.

An optical receiver converts the optical signal that is received at the output end of the optical fiber into an electrical signal. At the receiver end, the light signal is converted back to a current by a photodetector. After the current signal is amplified by a broadband transimpedance amplifier to a voltage signal, it is limited to form a digital signal. Since there is no clock that is accompanied by a data signal, the clock is extracted by a clock recovery circuit. Then, the final digital signal is produced by a decision circuit using the clock signal. The receiver must incorporate a demultiplexer (DEMUX) to reproduce the original parallel channels.

Digital Data Formats

It is important to know in which format the data is transferred in a communication system in order to be able to process the data in an efficient way. The binary data in optical

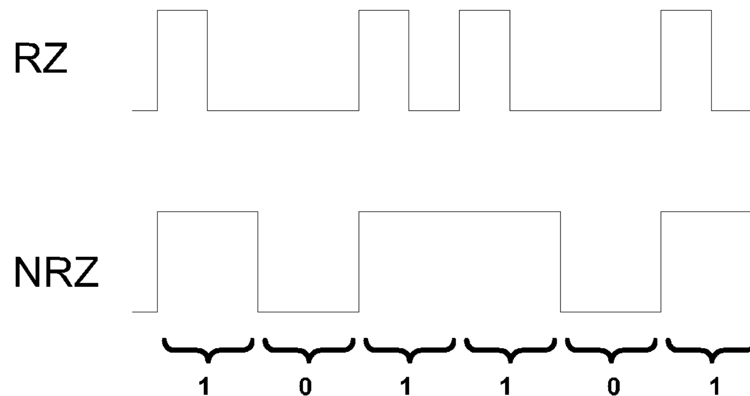


Figure 1.4: RZ and NRZ binary data streams.

communications systems is conveyed in two different formats:

RZ Format In the “return to zero” (RZ) format, each bit consists of two sections: the bit value followed by a ’0’ logic value.

NRZ Format In “non return to zero” (NRZ) format, each bit consists only of one part which corresponds to the bit value.

Figure 1.4 exemplifies a stream of binary bits ”101101” in both formats. It is clear that the bandwidth required for transferring data in the NRZ format is half of that in the RZ transmission systems. This comes at the price of missing data transitions in the case of having consecutive ONEs or ZEROs.

A long run of consecutive ONEs or ZEROs in the random data causes two main problems in the design of clock recovery circuits [3]:

- Oscillator is vulnerable to more jitter as the recovered clock drifts due to the lack of

data transitions for a long period of time.

- A long run of ONEs or ZEROs looks like a DC signal that can not be passed through the high-pass AC coupling circuits, and therefore, the data can not be transferred from one stage to the next one in the system.

As a solution, random NRZ data may be encoded so as to limit the maximum run length [2]. For instance, the 8-bit/10-bit (8B/10B) coding method converts a sequence of 8 bits to 10 bits while guaranteeing a maximum run length of 5 bits [5]. The 8B/10B coding decomposes each byte into two blocks of 5 bits and 3 bits, converting them to two blocks of 6-bits and 4-bits respectively. Thus, the data rate increases by 25% but many aspects of the circuit design are relaxed.

Assume that the stream of the random binary can be mathematically modeled by

$$x(t) = \sum_{k} b_k p(t - kT_b), \tag{1.1}$$

where b_k is ± 1, and T_b is the period of each transmitted bit. It can be easily shown that the frequency spectrum of the data is give by:

$$S_x(f) = T_b[\frac{sin(\pi f T_b)}{\pi f T_b}]^2, \tag{1.2}$$

Figure 1.5 plots the normalized frequency response of a random binary stream. The frequency is normalized by $1/T_b$; therefore, as seen the majority of the signal power is bound in between $-1/T_b$ and $1/T_b$.

[2]The run length is a period that there no transition in random data, or in other words, is a period of having consecutive ONEs or ZEROs in a random data.

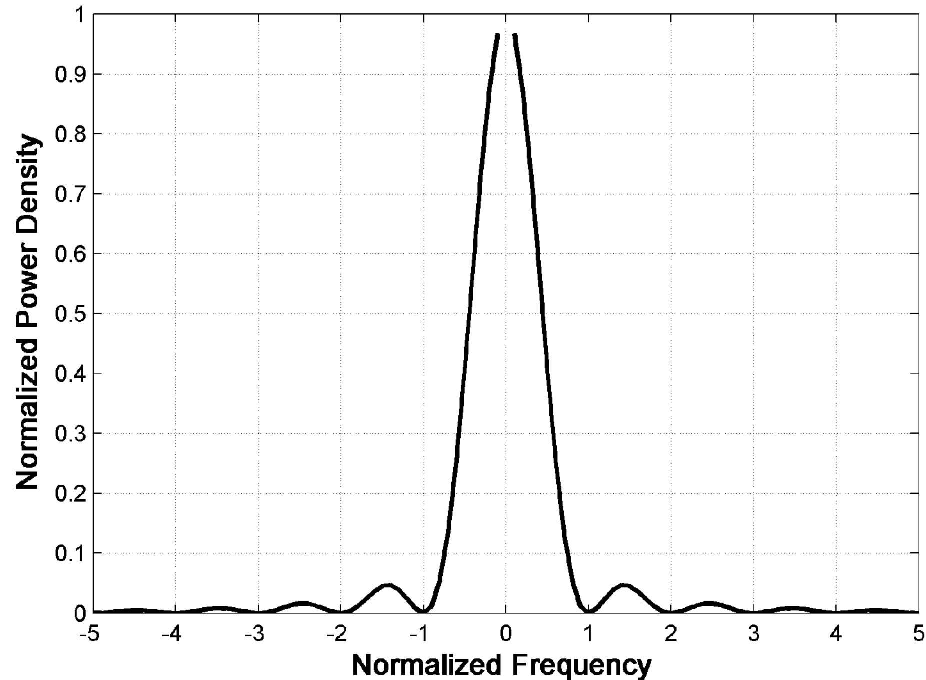


Figure 1.5: Frequency spectrum of random binary data.

Our concern is to obtain the specifications of the broadband amplifier based on the system performance requirement. Bandwidth is one of the most important characteristics of the amplifier to be used as a transimpedance amplifier (TIA) or a limiting amplifier in an optical fiber receiver. There is a design tradeoff in the selection of the appropriate bandwidth for the amplifier:

- Increasing the bandwidth of the amplifier increases the total noise of the integrated circuits, and leads to a higher noise figure.

- Limiting the bandwidth of the amplifier introduces intersymbol interference (ISI) in

the random data.

The ISI-noise trade-off is quantified for a single pole system in [3], and concluded that a bandwidth of $0.5R_b$ to $0.7R_b$ is the optimal solution for the preamplifier, where R_b is the optical system's bit rate. However, since most of the amplifiers have multiple zeroes and poles, a $0.7R_b$ is the usual choice. For example, for OC-768 40 Gbps optical communication systems, an amplifier bandwidth of 28 GHz is required. For the limiting amplifier, as its noise performance only has a minimal effect on system performance, a larger bandwidth equal to data rate is required (40 GHz for a 40 Gbps optical channel).

The gain of the amplifier must be large enough to overcome the noise of the subsequent stages. Since, in most cases, the gain is in tradeoff with bandwidth and supply voltage, at high speeds and low voltage the limited gain of the amplifier makes the design of the following stage very difficult.

The noise figure of the preamplifier must be minimized. Since the amplifiers are the first stage of the overall system, their noise performance directly affects the noise performance of the system, and consequently the sensitivity of the receiver. The problem of noise becomes more severe when supply voltage is scaled down.

The dynamic response of the amplifier is also important. Since a TIA may receive large input currents, the amplifier may distort the signal with the introduction of non-linearity. However, the binary nature of the data implies that a high nonlinearity can be tolerated. The automatic gain controlled amplifiers are used to monitor the signal amplitude and continuously adjust the gain so that the output relatively remains constant.

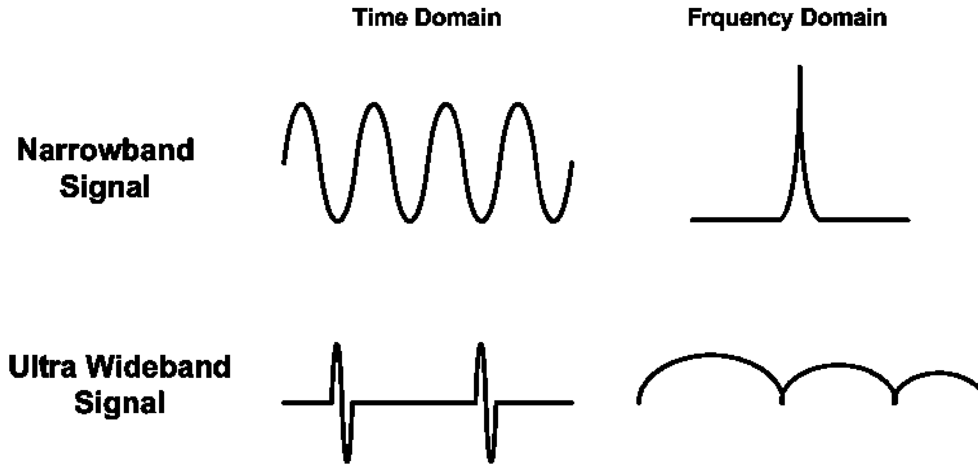


Figure 1.6: Time and frequency representation of narrowband and wideband signals.

The design of broadband amplifiers for optical communication applications will be discussed in Chapters 4 and 5.

1.2.2 Ultra Wideband Technology Overview

Ultra-Wideband (UWB) is a short-range wireless technology capable of transferring wireless data at data rates in excess of 100 Mbps. Unlike other narrowband wireless technologies, UWB does not modulate the signal with a carrier frequency; instead, it transmits impulses with durations of less than one nanosecond. The UWB signal is dense in time domain and largely spread in frequency domain. Figure 1.6 illustrates the conventional narrowband signal and UWB signal both in time and frequency domains.

In February 2002, the Federal Communications Commission (FCC) authorized the unlicensed use of UWB in 3.1-to-10.6 GHz with a power cap of -41 dBm [6]. The UWB signal

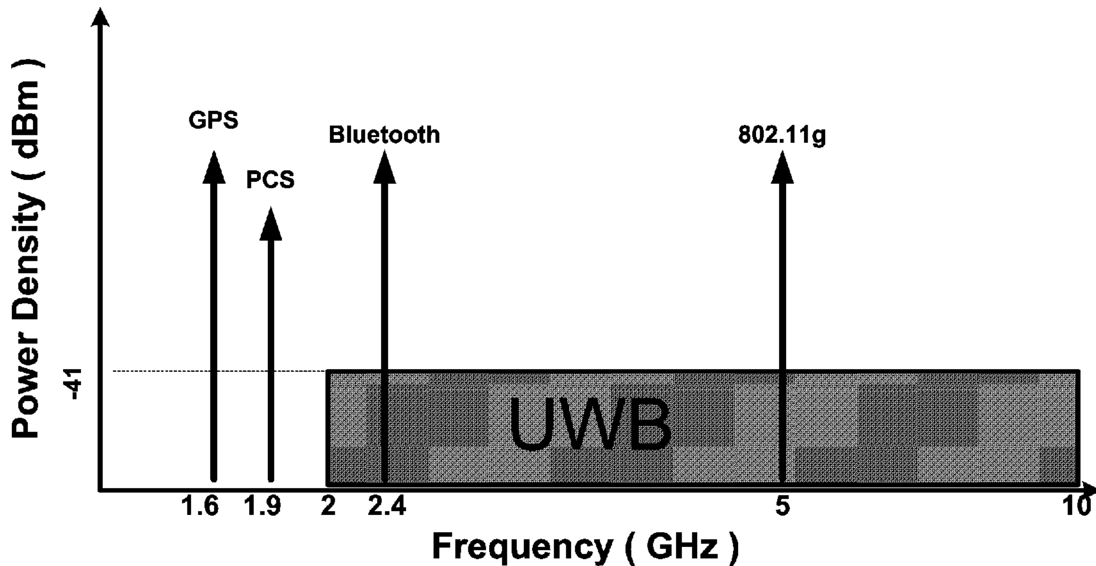


Figure 1.7: UWB Spectrum

should not interfere with other wireless standards as the signal power is spread over a large bandwidth (see Figure 1.7). The main application of UWB technology is in short-range wireless networking. UWB can replace the data cables in the home or business that are used for transferring digital data at high data rates. The low power operation of the UWB transceivers promises a dominant position for UWB systems in home networking. Intel has already started an intensive research program to develop UWB transceivers to be supplied with Intel's next generation chipsets [7].

In addition to its high-speed and low-power operation, UWB offers a simpler transceiver architecture than narrowband wireless systems as displayed in Figure 1.8. Single channel UWB transceivers do not incorporate any mixer and oscillator as no frequency down conversion is required. The simplicity of the UWB architecture results in a very low cost for

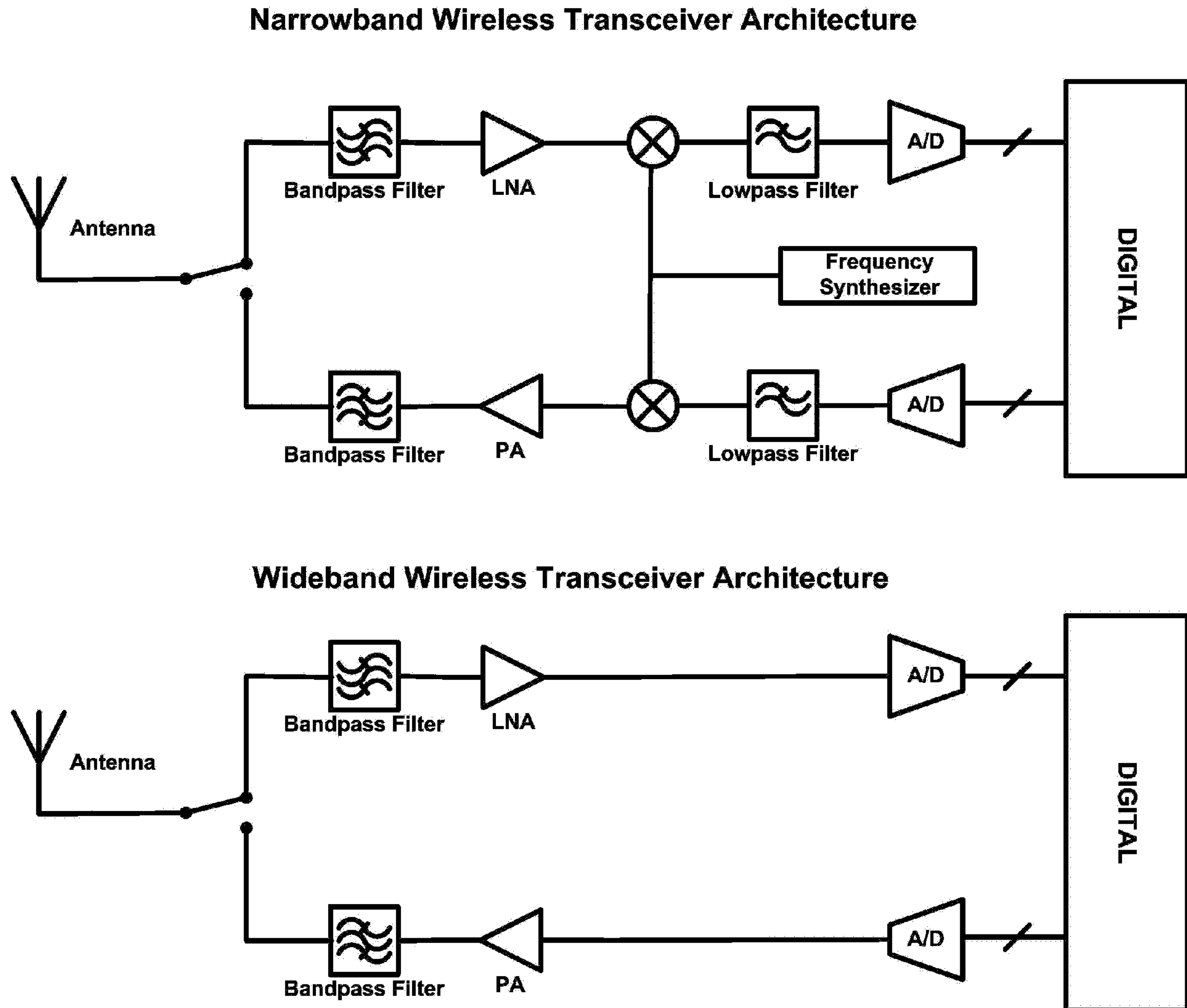


Figure 1.8: Narrowband and Ultra Wideband transceiver architecture.

design and fabrication of UWB prototypes. However, the proposed orthogonal frequency-division multiplexing (OFDM) requires a more sophisticated transceiver architecture [8].

The specification of required broadband amplifier can be extracted from the UWB tech-

nology characteristics. The bandwidth of the amplifier needs to be 3-10 GHz to completely recover the UWB signal. Typically a power gain larger than 10 dB is necessary as a very weak UWB signal received by antenna. As the amplifier is the first stage of the system, the broadband amplifier should not add significantly to the signal's noise. The design of broadband amplifiers for UWB applications will be discussed in Chapter 6.

1.3 Semiconductor Technologies for RF ICs

There is a vast array of semiconductor materials and device structures that can deliver the performance needed for design of broadband RF circuits and systems. These semiconductor materials are Silicon (Si), Silicon Carbide (SiC), Silicon Germanium (SiGe), Gallium Arsenide (GaAs), Gallium nitride (GaN) , and Indium Phosphide (InP). The device structures are categorized into Metal-Semiconductor Field Effect Transistors (MESFETs), Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), Bipolar Junction Transistors (BJTs), Heterojunction Bipolar Transistors (HBTs), and High Electron Mobility Transistors (HEMTs). Figure 1.9 shows the application spectrum of the semiconductor technologies.

A semiconductor technology is qualified for the implementation of broadband RF ICs if it meets the following conditions [10]:

- Active Devices: the transistor speed must satisfy $f_T > 4 \times bit\,rate$ and $f_{MAX} > 5 \times bit\,rate$. For instance, 40/50 GHz for 10 Gbps OC-192 and 160/200 GHz for 40 Gbps OC-768.

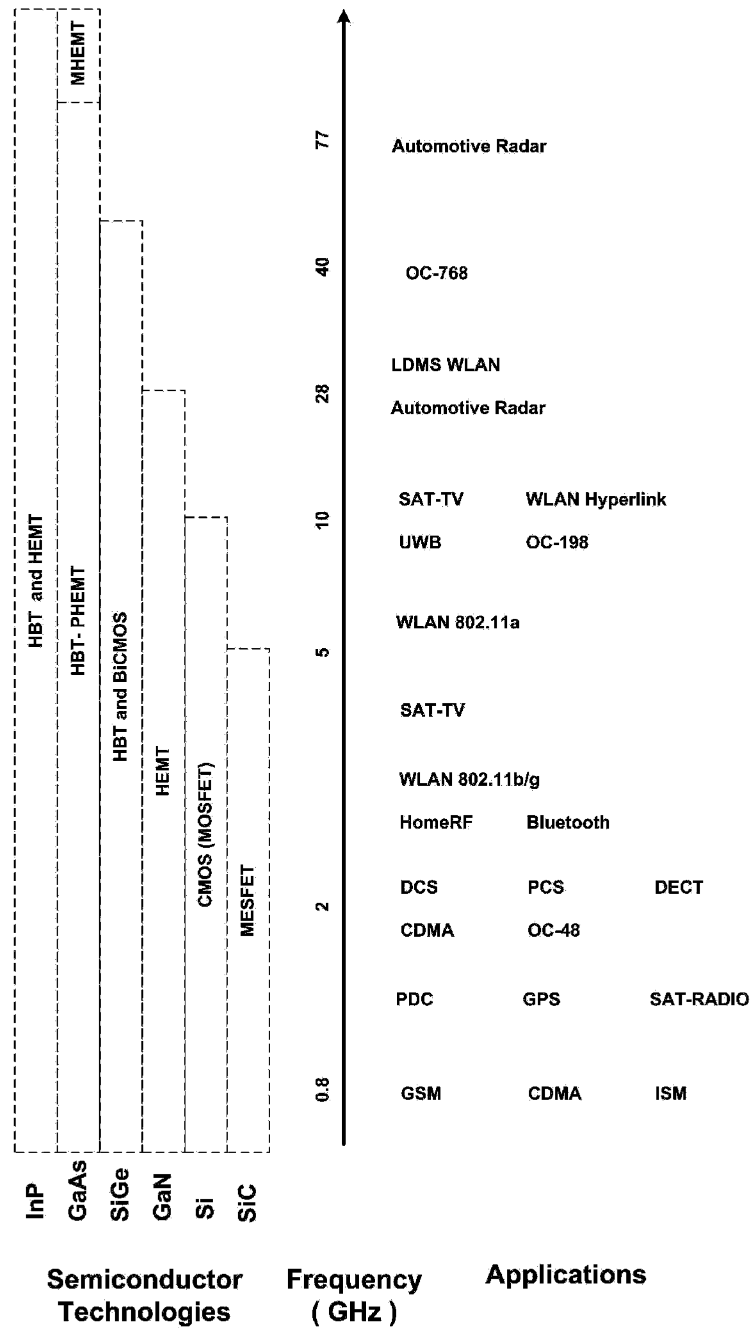


Figure 1.9: Application spectrum of semiconductor technologies based on ITRS 2005 [9].

- Passive Devices: high quality inductors with a resonance frequency well above the frequency of operation, and high quality capacitors and varactors.

- Interconnects: a large number of metal layers to increase the level of integration.

GaAs (Gallium Arsenide) has been the dominant technology for implementing OC-192 10 Gb/s and OC-768 40 Gb/s optical communication circuits. In the last three decades, the aggressive scaling of CMOS technology, driven by the digital market, has improved the intrinsic speed of MOSFETs by three orders of magnitude. While current CMOS processes offer an f_T over 100 GHz, an f_T of around 250 GHz is expected for 37 nm CMOS technology, the next generation of CMOS. Despite fast scaling, the current CMOS technology performance seems to be inadequate for systems operating at 40 Gb/s but is suitable for implementation of optical system's building blocks such as amplifiers, oscillators, multiplexers and demultiplexers for research purposes. For UWB applications, CMOS can be used for implementation of the complete transceiver as reported in [11, 12].

A cross section of a typical CMOS process is illustrated in Figure 1.10. The features of CMOS technology for broadband communication circuits can be listed as follows[13]:

- A high level of integration, possible system-on-a-chip solution of broadband optical and wireless transceivers.

- Lower costs compared to those of their contenders (SiGe or GaAs).

- Fast scaling and high yield technology.

- The availability of several metal layers in CMOS process.

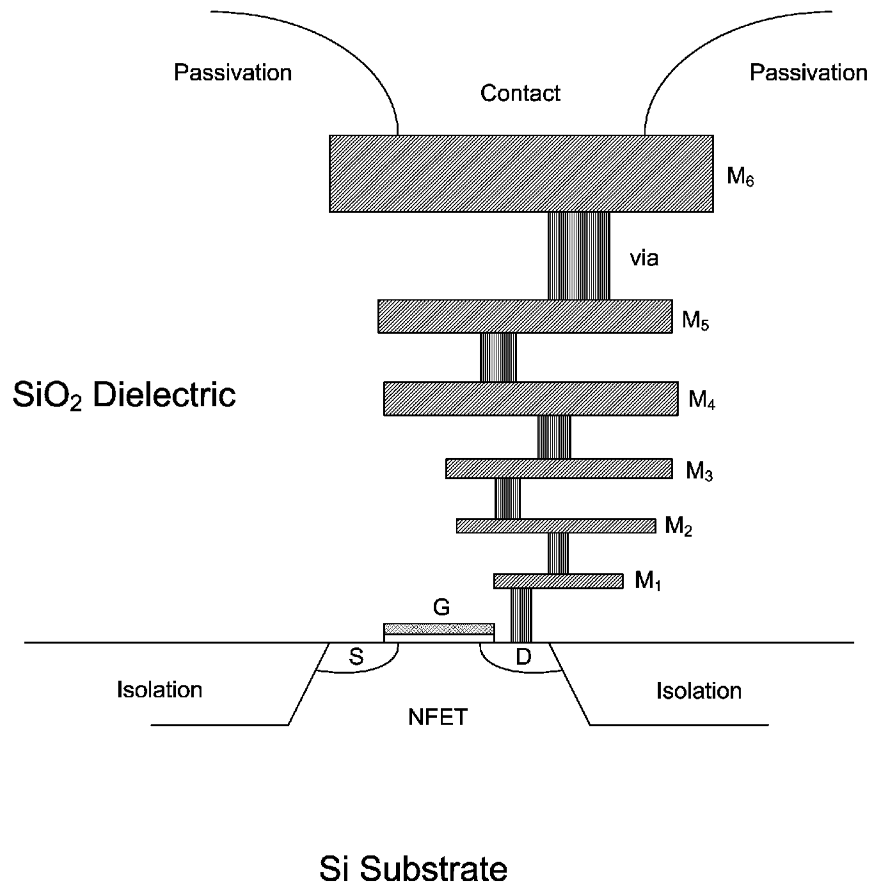


Figure 1.10: Cross-section of a typical CMOS process.

- The availability of relatively high quality passive devices: inductors [3] , transmission lines, MOS varactor, and linear capacitors.

Consequently, CMOS technology is potentially a great candidate for fully-integrated broadband communication circuits. As in recent years, the share of CMOS in semicon-

[3] Inductors can usually be fabricated in deep submicron CMOS processes offering a thick top metal layer with a quality factor in the range of 5 to 15 depending on the size of the inductor.

ductors grows dramatically, eventually claiming all the areas previously claimed by other technologies, including high speed analog and digital circuits, imaging and display technologies, and instrumentation. Following this trend, it is expected that the next generation of broadband communications systems will be fully implemented in CMOS technology.

1.4 Thesis Outline

Chapter 2 focuses on the design techniques for broadband amplification including inductive peaking, capacitive peaking, negative feedback, and distributed amplification. Justifying the choice of distributed amplification as the circuit technique for broadband circuit technique, this chapter discusses the analysis and design of DAs. This chapter concludes with a review of previously published CMOS DAs. As the CMOS interconnects are not considered distributed elements, a lumped-element analysis is developed in Appendix A.

The broadband modeling of CMOS circuit components is essential for the design of CMOS DAs. Chapter 3 describes the available narrowband models of RF MOSFETs and on-chip spiral inductors, the main circuit components of CMOS DAs, and extends those for broadband applications.

In the following two chapters, we addressed two problems associated with CMOS DAs: the large die area and gain attenuation because of the frequency-increasing loss of on-chip inductors. Chapter 4 presents a highly compact design of CMOS DAs accompanied with introduction of a new modeling process. In Chapter 5, a loss competition technique is proposed that improves the gain flatness and bandwidth of CMOS DAs.

In Chapter 6, the CMOS DA design for broadband wireless applications is studied.

As the UWB application requires a very good noise performance, we need to study the noise by identifying the noise sources in CMOS DAs. As a major noise contributor, the terminator resistor of the CMOS DAs is replaced by a frequency-dependent resistor that improves the noise figure of the amplifier significantly. The chapter ends with a design of non-distributed low-noise amplifiers based on convectional inductively source degenerated MOSFETs.

Finally, this dissertation is summarized and concluded in Chapter 7.

Chapter 2

Broadband Amplification Techniques

Broadband amplification is essential for the operation of high data-rate wireline and wireless communication. Several circuit design techniques for broadband amplification are suggested for the bandwidth extension of the CMOS amplifiers. These circuit techniques, including inductive peaking, capacitive peaking, negative feedback and distributed amplification are studied in this chapter.

2.1 Inductive Peaking

Inductive Peaking (or Shunt Peaking) is widely used as an effective technique to enhance the bandwidth of amplifiers [14] [15]. The inherent parasitic capacitors of transistors are the major cause of bandwidth limitations in the amplifiers. In the inductive peaking method, an inductor is used in series with the output load to compensate for the gain degradation. The schematic diagram of an inductively peaked common-source amplifier is illustrated in

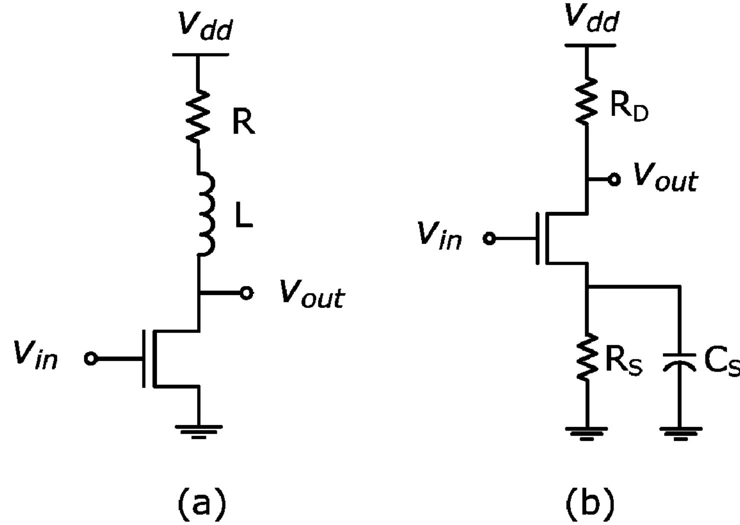


Figure 2.1: Inductive and capacitive peaking techniques.

Figure 2.1(a).

The insertion of an inductance L, in series with the load resistance increases the gain of the amplifier as frequency increases, compensating for the high-frequency gain degradation because of the parasitic capacitors of the transistors. In other words, this technique enhances the bandwidth of the amplifier by transforming the frequency response from that of a single pole to the one with two poles and a zero as follows:

$$\frac{v_{out}}{v_{in}} = \frac{g_m R_D}{1 + j\omega R_D C_D} \Longrightarrow \frac{v_{out}}{v_{in}} = \frac{g_m(R_D + j\omega L_D)}{1 + j\omega R_D C_D - w^2 L_D C_D} \tag{2.1}$$

The frequency response of a shunt peaked amplifier is characterized by the ratio of the R_D/L_D and $R_D C_D$ time constants. This ratio is denoted by m ($L = mR_D^2 C_D$) in [14]. To demonstrate the bandwidth improvement concept in the simplest form, all circuits

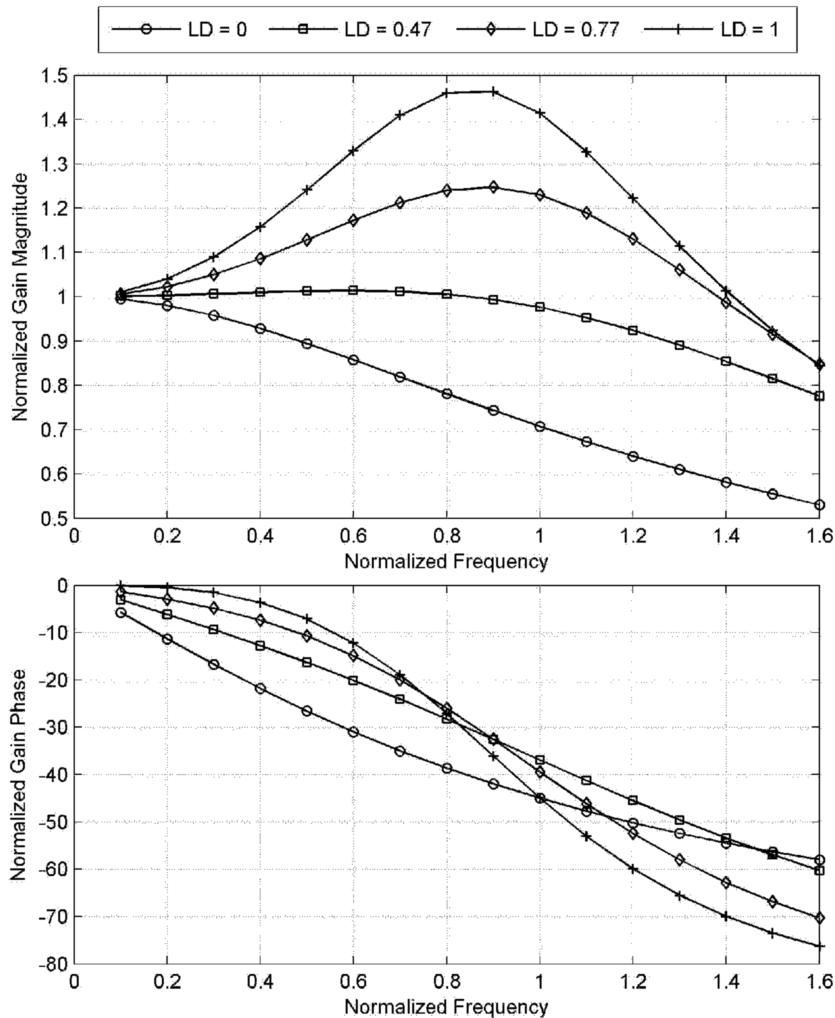


Figure 2.2: Inductively peaked amplifier's frequency response.

parameters are normalized. Therefore, the 3-dB bandwidth of the unpeaked amplifier is 1 (normalized bandwidth). The frequency response, magnitude and phase, of a shunt peaked amplifier is plotted in Figure 2.2 for different $L_D(L)$ values of 0, 0.47, 0.77, and 1. The L value of 0 features no shunt peaking, while the others provides more gain compensation

or overcompensation as L increases. The main drawback of this method is the bandwidth limitation introduced by the resonance of the series load inductor and parasitic capacitor seen at the drain of the transistor. To achieve a large gain, a large series inductor is required. This large inductor reduces the resonance frequency, and thus limits the amplifier bandwidth.

2.2 Capacitive Peaking

A capacitively peaked amplifier is a common source amplifier with a parallel RC network at its source as depicted in Figure 2.2(b). In the capacitive peaking technique, a capacitor is placed at the transistor source to compensate for the high-frequency response of MOS transistors [16]. The advantage of this method over the inductive peaking is that the implementation of high quality capacitors seems to be more practical than inductors which need sophisticated modeling and process customization.

To understand this circuit technique, we start with a simplified analysis of a common source amplifier with no degeneration ($R_S = 0$ and $C_S = 0$), assuming the frequency response of the amplifier is determined by a single dominant pole at $R_D C_D$ as

$$A_v(w) = g_m Z_D = \frac{g_m R_D}{1 + j\omega R_D C_D} \tag{2.2}$$

where C_D and Z_D are the total capacitance and impedance seen from the drain of the transistor. As 2.2 indicates, the gain of the amplifier decreases as frequency increases. To compensate for this frequency response, a parallel RC circuit is placed in the source of the transistor. As frequency increases, the impedance of this circuit tends toward zero,

approaching a simple common-source circuit. This frequency-decreasing source impedance offsets the effect of the amplifier's original pole on the frequency response. This can be justified mathematically assuming that the original voltage gain of the amplifier is given by

$$A_v(w) = \frac{g_m Z_D}{1 + g_m Z_S} \tag{2.3}$$

By replacing Z_D and Z_S, the gain is calculated as

$$A_v(w) = \frac{g_m R_D}{1 + g_m R_S} \frac{1 + j\omega R_S C_S}{(1 + j\omega R_D C_D)(1 + \frac{j\omega R_S C_S}{1+g_m R_S})} \tag{2.4}$$

The first term in the above equation shows the gain of the amplifier at mid-band frequencies, which is determined by the value of R_S. As computed in 2.4, this circuit adds a pole and zero to the amplifier's transfer function. If the values of the source capacitor are chosen such that $R_S C_S = R_D C_D$, the pole at $1 + j\omega R_D C_D$ is canceled by the zero at $1 + j\omega R_S C_S$, leaving the transfer function only one pole at $(1 + g_m R_S)/R_D C_D$. Comparing the common-source amplifier frequency response with that of the new circuit, we discover a bandwidth extension by a factor of $1 + g_m R_S$. Note that this design needs additional circuits to satisfy input/output matching conditions. The simulation gain of the amplifier for different values of C_S is shown in Figure 2.3. Note the improvement in the gain flatness comes at the price of reduction in the overall gain as the capacitive peaking technique acts as a negative feedback. Although this circuit effectively enhances the bandwidth of the common source amplifier, it is susceptible to instability as it produces a negative input resistance. To investigate this problem, an introduction on the stability of RF circuits follows.

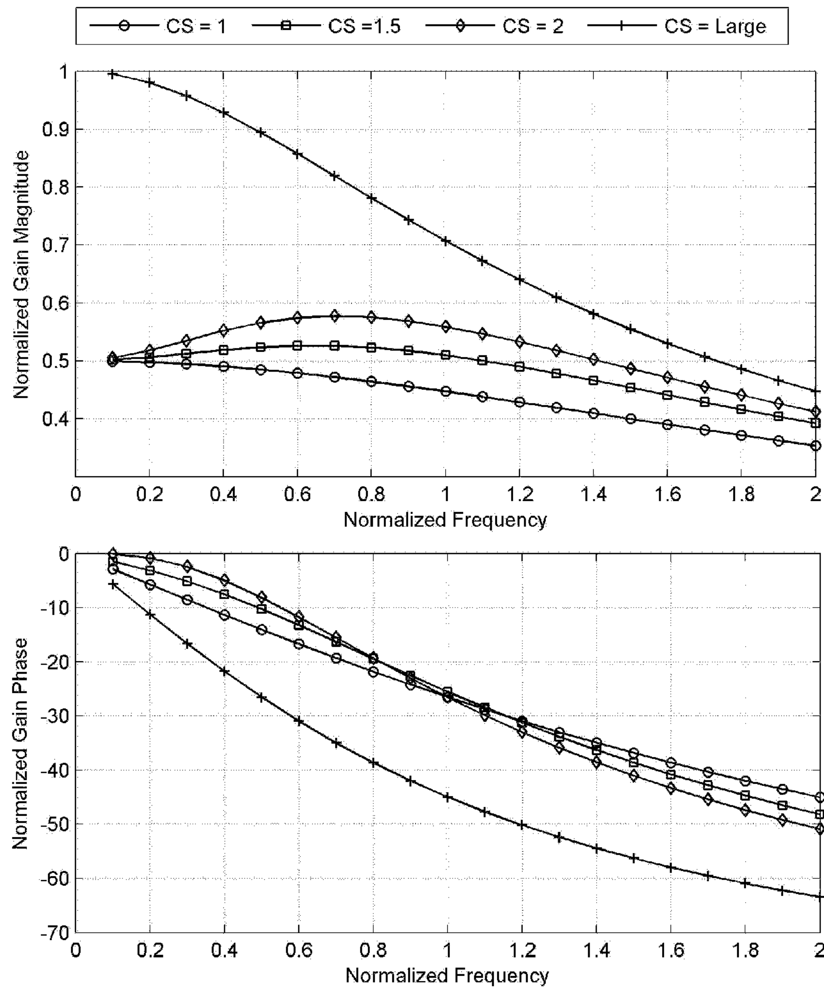


Figure 2.3: Capacitively peaked amplifier's frequency response.

Stability is the most important issue that should be considered in the design of any RF circuit, particularly for broadband amplifiers such that their stability condition must be

addressed over their large operating bandwidth. An amplifier is unconditionally stable if

$$|\Gamma_{in}| = |\frac{Z_{in} - Z_0}{Z_{in} + Z_0}| < 1$$
$$|\Gamma_{out}| = |\frac{Z_{out} - Z_0}{Z_{out} + Z_0}| < 1 \tag{2.5}$$

where Γ_{in} and Γ_{out} are the reflection coefficients of the amplifier at the input and output ports, respectively, and Z_0 is the characteristics impedance of the transmission lines connected to input and output ports. If any of the amplifier reflection coefficients is greater than one at operating frequencies of the amplifier, the amplifier is known to be conditionally stable (or potentially unstable) depending on the design of the matching networks. To evaluate the stability of the proposed amplifier, the first step is to calculate the input and output impedances of the amplifier. Ignoring the gate-drain capacitance of the transistor, the input impedance of the amplifier can be calculated as follows

$$Z_{in}(w) = \frac{1}{j\omega C_{gs}} + (1 + \frac{g_m}{j\omega C_{gs}})Z_S(w) \tag{2.6}$$

where Z_S is the total impedance placed at the source of the transistor:

$$Z_S(w) = R_S \| \frac{1}{j\omega C_S} = \frac{R_S}{1 + j\omega R_S C_S} \tag{2.7}$$

By simple algebraic manipulation, the real part of the Z_S is a negative input resistance that can be expressed as

$$\Re(Z_S(w)) = -\frac{g_m}{w^2 C_{gs} C_S} \tag{2.8}$$

for frequencies $w \gg 1/R_S C_S$.

Considering the values of R_S and C_S , the inequality condition in 5.6 is correct over the bandwidth of the proposed amplifier, suggesting some instability in the operation of the

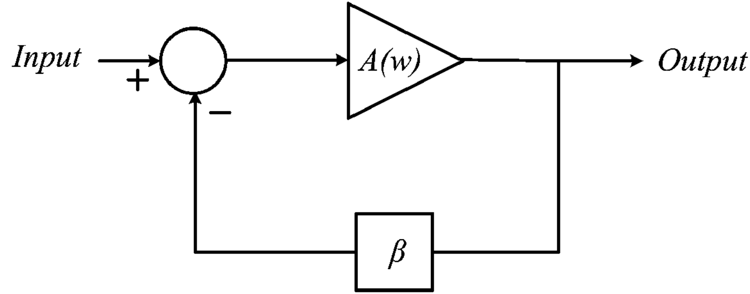


Figure 2.4: Block diagram of amplifier with negative feedback.

amplifier. Fortunately, this is not the case for the output port. A technique to stabilize the amplifier input network is to add a series resistance or a shunt conductance to the input port (gate of the transistor) [17]. The latter seems to be a more appropriate choice since it does not deteriorate the frequency response of the amplifier (S_{21}).

2.3 Negative Feedback

Negative feedbacks can be used for broadening the operation band of the amplifiers [18]. The block diagram of an amplifier with a negative feedback is displayed in Figure 2.4. Assuming the gain of the amplifier without feedback is given by $A(w)$, applying a constant feedback (β) to the amplifier circuit will change the transfer function to:

$$A_{feedback}(w) = \frac{A(w)}{1 + \beta A(w)}. \tag{2.9}$$

As in the previous section for simplicity of the analysis, we assume a single pole frequency response for the amplifier transfer function as

$$A(w) = \frac{A_0}{1 + \frac{j\omega}{w_C}}, \tag{2.10}$$

By replacing 2.10 into 2.9, the feedback transfer function can be calculated as:

$$A_{feedback}(w) = \frac{\frac{A_0}{1+\frac{j\omega}{w_C}}}{1 + \beta\frac{A_0}{1+\frac{j\omega}{w_C}}} \tag{2.11}$$

Further simplification of 2.11 results in the following transfer function for the feedback amplifier:

$$A_{feedback}(w) = \frac{\frac{A_0}{1+\beta A_0}}{1 + \frac{j\omega}{w_C(1+\beta A_0)}}. \tag{2.12}$$

Looking at the calculated feedback transfer function, we notice a bandwidth extension by a factor of $1 + \beta A_0$. This bandwidth extension comes at the cost of reducing the gain by the same factor, leaving the transfer function's gain-bandwidth product constant for any value of feedback. Figure 2.5 depicts the magnitude and phase of the feedback transfer with normalized gain and bandwidth. Note that $\beta = 0$ implies that no feedback is applied.

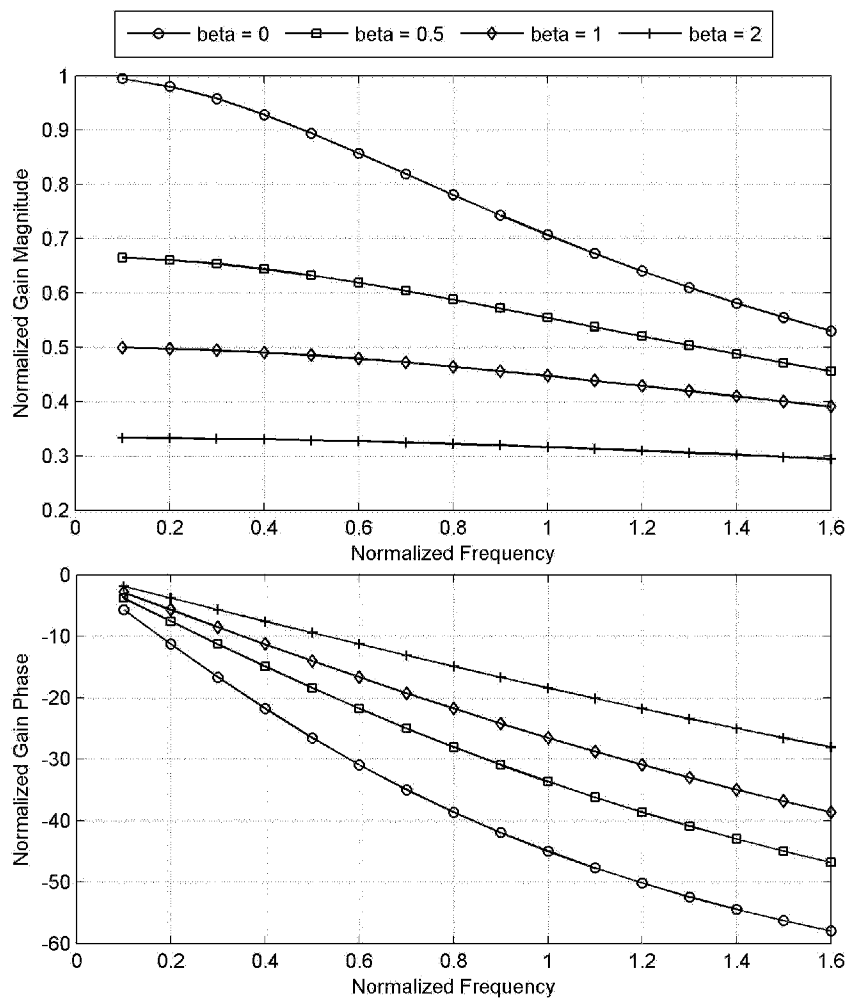


Figure 2.5: Feedback amplifier frequency response for several values of feedback (β).

2.4 Distributed Amplification

Distribution amplification has been around for more than 65 years dating back to the British Patent by Precival [19]. Later, Ginzton significantly developed the idea in 1948 [20]. Since then, distributed amplification has become a reliable technique for broadband amplifiers. Researchers have worked on the analysis, design (computer-aided), optimization, and implementation of DAs in different technologies. DAs overcome the traditional gain-bandwidth tradeoff of other amplifier configurations by accumulating the gains of the amplifier's stages in an additive pattern. Inherent transistor capacitors, the upper limit of the amplifier's bandwidth, are absorbed in the transmission lines that connect the gates and the drains of transistors. A schematic diagram of a DA is presented in Figure 2.6(a). In CMOS, the transmission lines are artificially created using lumped LC networks as depicted in Figure 2.6(b).

As discussed in the next section, the distributed amplification is an appropriate choice for broadband CMOS amplifiers since this topology relaxes the f_T requirement for a specific standard ($f_T > 4 \times Bitrate$). Relaxation of f_T requirement enables CMOS technology to compete with high-speed compound semiconductor technologies in the implementation of broadband communication circuits.

2.4.1 Distributed Amplifier Analysis

This section reviews the analysis of microwave DAs presented in [21, 22]. Figures 2.7 and 2.8 exhibit the equivalent circuits of the lossless gate and drain lines which can be isolated if the gate-drain capacitance of the transistor is neglected. The only dependency of gate

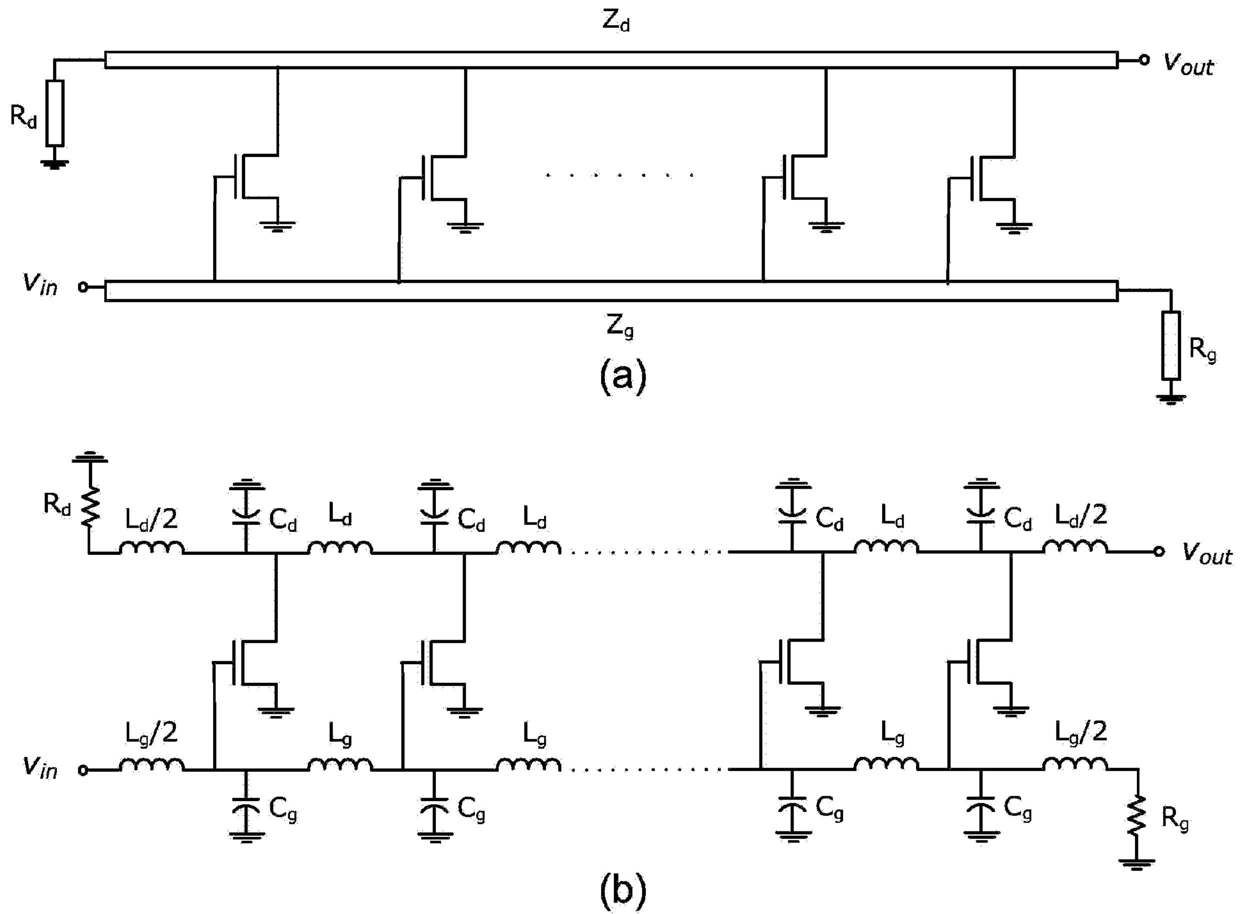


Figure 2.6: Schematic diagram of distributed amplifier.

and drain transmission lines is the coupling through the dependent current source, where $I_{dn} = g_m V_{cn}$. Now the basic transmission line theory can be used to calculate the gain of the amplifier. The loss of transmission lines is neglected in this analysis. For the gate

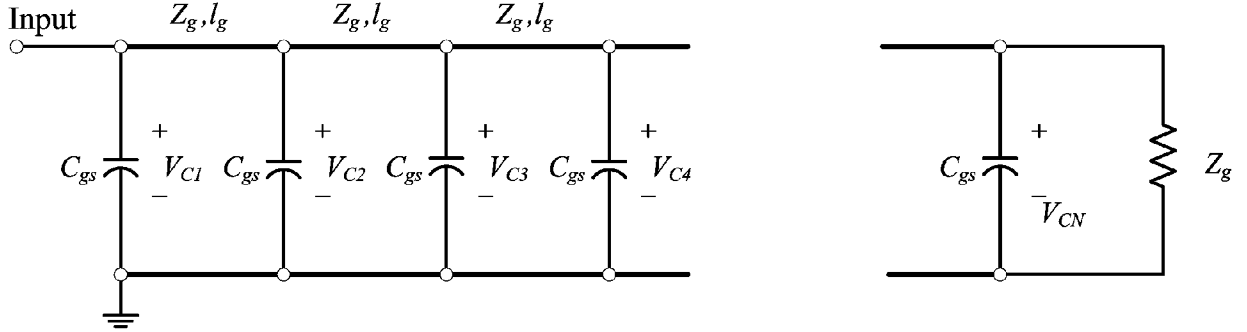


Figure 2.7: Transmission line circuit for the gate line of distributed amplifier [21].

lines, the series impedance and shunt resistance per unit length can be written as

$$Z = j\omega L_g, \tag{2.13}$$

$$Y = j\omega C_g + j\omega C_{gs}/l_g. \tag{2.14}$$

and the characteristic impedance is given by

$$Z_g = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_g}{C_g + C_{gs}/l_g}} \tag{2.15}$$

Now we can obtain the propagation constant of the gate transmission line as follows:

$$\gamma_g = \alpha_g + j\beta_g = \sqrt{ZY} = \sqrt{j\omega L_g[j\omega C_g + j\omega C_{gs}/l_g]}. \tag{2.16}$$

The propagation constant of a lossless transmission line can be simplified as follows:

$$\gamma_g = j\omega\sqrt{L_g(C_g + C_{gs}/l)} \tag{2.17}$$

For the drain lines, the series impedance and shunt reactance per unit length can be written

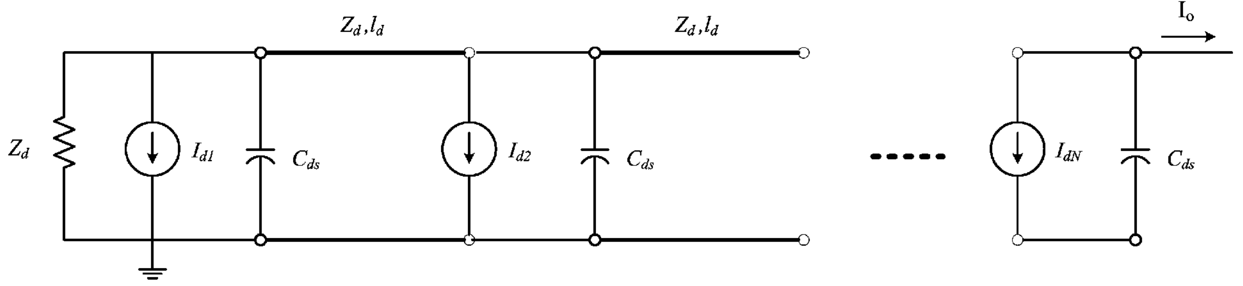


Figure 2.8: Transmission line circuit for the gate line of the distributed amplifier [21].

as

$$Z = j\omega L_d, \tag{2.18}$$

$$Y = j\omega(C_d + C_{ds}/l_d) \tag{2.19}$$

Similar to that of the gate lines, the characteristic impedances and the propagation constant of the drain lines can be written as

$$Z_d = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_d}{C_d + C_{ds}/l_d}}, \tag{2.20}$$

and

$$\gamma_d = \alpha_d + j\beta_d = \sqrt{ZY} = j\omega\sqrt{L_d C_d + C_{ds}/l_d)}. \tag{2.21}$$

For an incident input voltage V_i, the input voltage of each cell is expressed as

$$V_{cn} = V_i e^{-(n-1)\gamma_g l_g}, \tag{2.22}$$

for a phase reference at the first cell.

Each FET produces a current on the drain line of the form $-\frac{1}{2}I_{dn}e^{\pm\gamma_d z}$ in each direction. Since $I_{dn} = g_m V_{cn}$, the total output current at the Nth terminal of the drain line is

$$I_o = -\frac{1}{2}\sum_{n=1}^{N} I_{dn}e^{-(N-n)\gamma_d l_d} = \frac{g_m V_i}{2}e^{-N\gamma_d l_d}e^{\gamma_g l_g}\sum_{n=1}^{N} e^{-n(\gamma_g l_g - \gamma_d l_d)}. \tag{2.23}$$

Using $\sum_{n=1}^{N} x^n = (x^{N+1}-1)/(x-1)$, the previous equation can be simplified to

$$I_o = \frac{g_m V_i}{2}e^{-N\gamma_d l_d}e^{\gamma_g l_g}\times\frac{e^{-(N+1)(\gamma_g l_g-\gamma_d l_d)}-1}{e^{-(\gamma_g l_g-\gamma_d l_d)}-1} = \frac{g_m V_i}{2}e^{-N\gamma_d l_d}e^{\gamma_g l_g}\times\frac{e^{-(N+1)\gamma_g l_g}e^{(N+1)\gamma_d l_d}-1}{e^{-(\gamma_g l_g-\gamma_d l_d)}-1}. \tag{2.24}$$

The above expression can be further simplified to:

$$I_o = -\frac{g_m V_i}{2}\frac{e^{\gamma_d l_d}[e^{-N\gamma_g l_g}-e^{-N\gamma_d l_d}]}{e^{-(\gamma_g l_g-\gamma_d l_d)}-1}, \tag{2.25}$$

and by multiplying the nominator and denominator by $e^{-\gamma_d l_d}$, we obtain the following expression for the output current:

$$I_o = -\frac{g_m V_i}{2}\frac{e^{-N\gamma_g l_g}-e^{-N\gamma_d l_d}}{e^{-\gamma_g l_g}-e^{-\gamma_d l_d}}. \tag{2.26}$$

For a matched input and output, the amplifier power gain can be calculated as follows:

$$G = \frac{P_{out}}{P_{in}} = \frac{\frac{1}{2}\mid I_o\mid^2 Z_d}{\frac{1}{2}\mid V_i\mid^2/Z_g} = \frac{g_m^2 Z_d Z_g}{4}\mid\frac{e^{-N\gamma_g l_g}-e^{-N\gamma_d l_d}}{e^{-\gamma_g l_g}-e^{-\gamma_d l_d}}\mid^2. \tag{2.27}$$

By applying the synchronization condition $\beta_g l_g = \beta_d l_d$, the result can be further simplified such that

$$G = \frac{g_m^2 Z_d Z_g}{4}\frac{(e^{-N\alpha_g l_g}-e^{-N\alpha_d l_d})^2}{(e^{-\alpha_g l_g}-e^{-\alpha_d l_d})^2}. \tag{2.28}$$

For a lossless amplifier ($\alpha_g = 0$ and $\alpha_g = 0$), the gain is simplified as follows:

$$G = \frac{g_m^2 Z_d Z_g N^2}{4}, \tag{2.29}$$

showing the gain increases as N^2.

Further developing on the above analysis, Razavi calculates the voltage gain of the amplifier [3] as follows. If characteristics impedances of the gate and drain transmission lines are equal ($Z_{0G} = Z_{0G} = Z_{0L}$), the total voltage gain can be obtained by the following [3]

$$A_v = \frac{ng_m Z_{0L}}{2} = \frac{ng_m}{2}\sqrt{\frac{L_0}{C_0 + nC_{gs}/l}}. \tag{2.30}$$

For MOSFETs, the transit frequency is given as

$$f_T = \frac{gm}{2\pi C_{gs}} \tag{2.31}$$

By replacing g_m in Equation 2.30, the following gain expression can be obtained:

$$A_v = n\pi f_T C_{gs}\sqrt{\frac{L_0}{C_0 + nC_{gs}/l}}. \tag{2.32}$$

If $C_0 << nC_{gs}/l$, the gain can be simplified such that

$$A_v = \pi f_T \frac{l}{v}. \tag{2.33}$$

Equation 2.33 indicates that the voltage gain is proportional to the end-to-end delay of the transmission lines l/v, as well as the transit frequency of the transistors. If the amplifier is fed by a current source, the transimpedance gain is proportional to $A_v Z_{0L}$, and subsequently to $\pi f_T l L_0$. The product is independent of the gate-source capacitance of the transistors. This simple analysis gives some insight into the relationships among the gain, bandwidth, and delay of a DA.

Note that if the loss of transmission line is taken into account, this analysis cannot be considered accurate due to several nonidealities. In theory, a DA must provide an infinite

bandwidth and an unlimited gain, but in practice, this does not occur due to the following [3, 23]:

- Limited resistivity of the transmission lines causes the DC voltage to drop over the gate and drain transmission lines, limiting the number of stages, and thus, the achievable gain.
- The loss of the on-chip transmission lines attenuates the signal, leaving the far end stages without enough input signal amplitude. This become worse as the losses increase with frequency, and hence, the gain of the DA does not remain constant as frequency increases. This problem is tackled by introducing a loss compensation technique in Chapter 5.
- The output resistance of the transistors contribute to more loss in the drain transmission lines. However, this problem can be tackled using cascode gain cells.
- The gate-drain capacitance couples the drain and gate transmission lines which in turn reduce the gain amplifier and increase the reverse coupling. Again, these adverse effects can be controlled by employing a cascode configuration.
- Noise performance of the DAs is poor mainely because of the noise injected by the 50 Ω terminating resistor of the gate transmission line. Chapter 6. focuses on reducing the noise figure by replacing the terminating resistor with a low-noise network.

Moreover, the above analysis method based on transmission line theory cannot be accurately applied to CMOS DAs because CMOS interconnects of typical length are shorter

than one tenth of the wavelength, and cannot be considered as distributed elements. Therefore, a lumped-analysis is required for the accurate analysis of CMOS DAs. We present a matrix-based lumped-element analysis of CMOS DAs in Appendix A. However, for the design of the CMOS DAs in this dissertation we proceed with the gain, bandwidth, and matching expressions obtained based on the transmission line analysis because of their simplicity. Later we fine tune our design parameters using circuit simulation.

2.4.2 Distributed Amplifier Design Guideline

This section provides a brief strategy for the design of CMOS DAs based on bandwidth, characteristic impedance, and gain expressions. The first step in the design of a distributed amplifier is to find the values of the capacitors and inductors of the gate and drain transmission lines. The bandwidths of the gate and drain transmission lines are given by

$$BW_{gate} = \frac{1}{\sqrt{L_g C_g}} \text{ and } BW_{drain} = \frac{1}{\sqrt{L_d C_d}} \tag{2.34}$$

where L_g, L_d, C_g, and C_d are the inductor and capacitor of the gate and drain transmission lines. The characteristic impedance of the gate and drain transmission lines are obtained using

$$Z_{gate} = \sqrt{\frac{L_g}{C_g}} \text{ and } Z_{drain} = \sqrt{\frac{L_d}{C_d}} \tag{2.35}$$

To ensure proper matching at input/output ports, the characteristics impedance of the gate and drain transmission lines, Z_{gate} and Z_{drain}, must be chosen equal to or close to the terminating resistors of the lines, R_g and R_d, respectively. Since a proper DA design requires equal signal delays on the gate and drain transmission lines, the gate and drain

transmission lines' bandwidths are required to be equal. If the input and output ports are terminated with the same resistors, then this condition necessitates that the values of the inductors of capacitors of both lines be equal ($L_g = L_d$ and $C_g = C_d$). Note that C_g and C_d are the total capacitance seen from the corresponding nodes of the circuit, including the parasitic capacitors of the transistors and on-chip inductors. Therefore, these parasitic capacitors determine the minimum values of C_g and C_d and, consequently, the maximum achievable power gain of the distributed amplifier, which is given by

$$G = \frac{g_m R_d R_g N^2}{4}, \tag{2.36}$$

if the transmission lines are matched in their characteristics impedance.

2.4.3 Previous Research on CMOS DAs

Researchers around the world have extensively worked on the implementation of broadband amplifiers based on a distributed amplification technique. Several successful implementations of CMOS DAs are reported in the literature. These designs are distinguished from each other through the following traits:

- different implementation of on-chip inductors in CMOS technology, such as square spiral inductors, bond wire inductors, or coplanar waveguides, or
- different circuit topology for each gain cell, such as common-source, cascode, or differential amplifiers.

Table 2.1 summarizes the performance of CMOS DAs reported in the literature up to the date of this dissertation. The rest of this section highlights the contribution of each work.

Process / Ref.	BW (GHz)	G(dB)	A($mm \times mm$)	NF (dB)	S_{11} (dB)	S_{22} (dB)	$P_{DC}(mW)$
0.8 μm[24]	4.7	5	0.72×0.32	$5.1 - 7$	<-6	<-9	54
0.6 μm[25]	5.5	6.5	1.4×0.8	$5.3 - 8$	<-7	<-10	83.4
0.6 μm[26]	8.5	5.5	1.3×2.2	$8.7 - 13$	<-6	<-9.5	216
0.18 μm[27]	23	5	0.3×1.5	–	<-14	–	–
0.18 μm[28]	18	8	1.8×1.3	–	–	–	–
0.18 μm[29]	16	7.3	0.9×1.5	$4.3 - 6.1$	<-8	<-9	52
0.18 μm[30]	27	6	1.8×0.9	6	<-8	<-9	68
0.18 μm[31]	39	4	1.1×3.0	–	<-10	<-10	140
0.18 μm[32]	28	9	0.75×0.48	–	<-11	<-13	60
0.18 μm[33]	24	7.3	0.9×1.5	$4.3 - 6.1$	<-8	<-9	52
0.18 μm[34]	> 12.6	7.6	1.1×0.6	$5.5 - 9.0$	<-10	<-10	39.6
0.18 μm[35]	36	9.5	0.94×0.86	-	<-8	<-11	99
0.09 μm[36]	80	7	0.9×0.8	$6.0 - 6.9$	<-7	<-12	122
0.09 μm[37]	95	7.4	1.2×0.6	-	<-10	<-8	120

Table 2.1: Summary of Reported Performance of CMOS Distributed Amplifiers.

The first implementation of DA in a standard CMOS technology ($0.8\mu m$) is reported in [24]. The inductance that is required for the transmission lines is realized by the bond wire inductance of a plastic surface-mount package. The bond wire provides an inductance of 1 nH/mm with a good quality factor of around 25. This CMOS DA has a unity gain cutoff frequency of 4.7 GHz, and a gain of 5 dB with a gain flatness of ± 1.2 dB over the 300KHz to 3GHz band. The amplifier consumes 54 mW from a 3.0-V DC supply. The amplifier

exhibits a noise figure of 5.1 dB at 2 GHz. Because the proposed DA uses wire bonding for construction of the transmission lines which requires addition after-process manufacturing steps, it can not be considered as a fully integrated solution for CMOS DAs.

Two fully integrated CMOS DAs are presented by Allstot's group at the University of Washington [25, 26]. These amplifiers use on-chip spiral inductors. The difference between these two DAs lies in the cell configuration: the first one [25] employs a single-transistor common-source configuration, whereas the second one uses differential amplifiers for each stage. The amplifiers are four-stage designs, fabricated in a standard 0.6-μm three-layer metal digital-CMOS process. The first amplifier has a unity-gain cutoff frequency of 5.5 GHz, and a gain of 6.5 dB with a gain flatness of 1.2 dB over the 0.54 GHz band. The input and output are matched to 50Ω with maximum return input and output return losses of -7 and -10 dB, respectively. The amplifier dissipates 83.4 mW from a 3.0-V DC supply. The input-referred 1-dB compression point is better than +6 dBm over the amplifier's bandwidth. The second amplifier, a fully differential CMOS circuit topology, results in a wider bandwidth of 8.5 GHz compared to its single-ended DA. A schematic diagram of the differential DA is shown in Figure 2.9. However, the reported differential DA gain is 5.5 dB (lower than single-ended). As expected, both the power consumption and die area are significantly larger for the differential implementation. The next CMOS DA [27] was implemented using 0.18μm CMOS technology where coplanar striplines are used as the inductive elements as displayed in Figure 2.11. To achieve a final 50Ω characteristic impedance, the coplanar stripline characteristics impedance is designed to be 70Ω before loading the active devices. Several Substrate contacts are placed underneath the coplanar

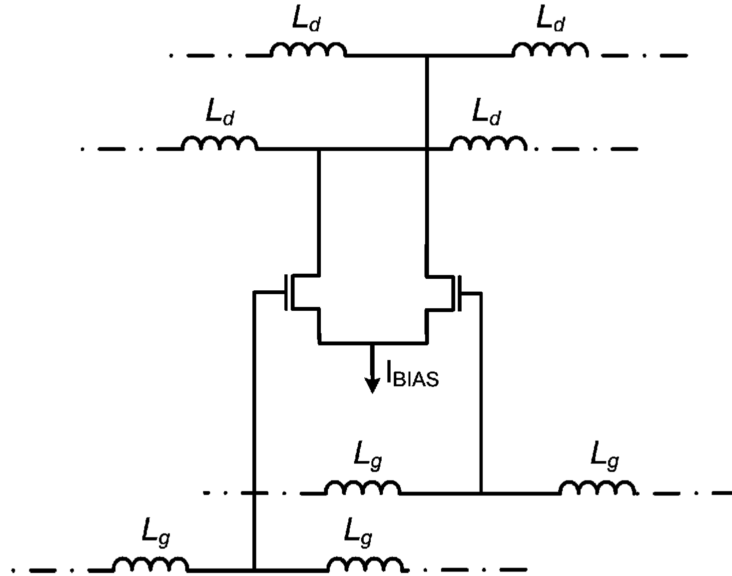


Figure 2.9: Differential DA.

striplines to prevent the formation of a continuous lossy low-inductance return pass. Advancing this work, a CMOS DA using coplanar waveguides was presented by Amaya et.al. [30]. The structure of a coplanar waveguide is shown in Figure 2.12. This DA achieves a gain of 6 dB over a 1-27 GHz frequency band. This amplifier dissipates 68 mW from a 1.8 V DC supply.

A group at Queen's University proposed a DA in $0.18\mu m$ CMOS technology [28] . The amplifier uses a Darlington cascode configuration for each gain cell, illustrated in Figure 2.10. This technique is used to enhance the g_m/C_{gs} ratio to achieve a larger gain for a specific bandwidth or a larger bandwidth for a specific gain compared with the simple common-source gain cells. Two amplifiers have been implemented, one with an on-chip power supply and the other one with an off-chip power supply, achieving gains of 5 and

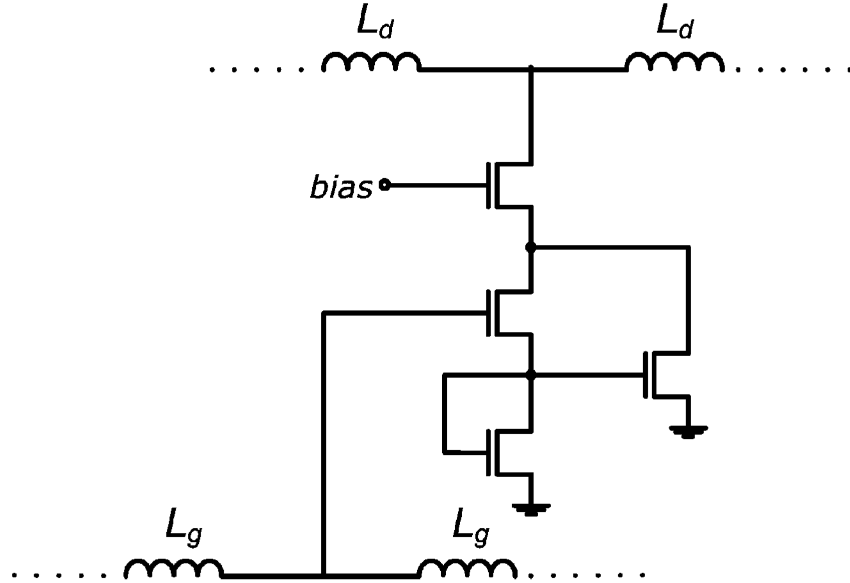


Figure 2.10: Distributed amplifier Darlington cell .

8 dB over a 1-10 G band, respectively. Liu et. al. at Nation Taiwan University designed three CMOS DAs during the past few years [29, 33, 37]. The first two DAs use a cascode configuration for the gain cells and m-derived transmission lines [29, 33]. The cascode configuration improves the reverse isolation of the amplifier as well as limits the output transmission loss by increasing the output resistance of the gain cells. These amplifiers, implemented in standard 0.18 μm CMOS technology employing on-chip spiral inductors, achieve a gain of 10.6 and 7.3 dB over the bandwidth of 14 and 22 GHz, respectively. The third work [37], which reported the largest DA bandwidth up to the writing of this dissertation, archives a gain of 7.4 dB with a unity-gain bandwidth of 80 GHz. The amplifier is devised based on a capacitive division technique that reduces the input gate capacitance of the transistors. Although this technique enhances the bandwidth of the

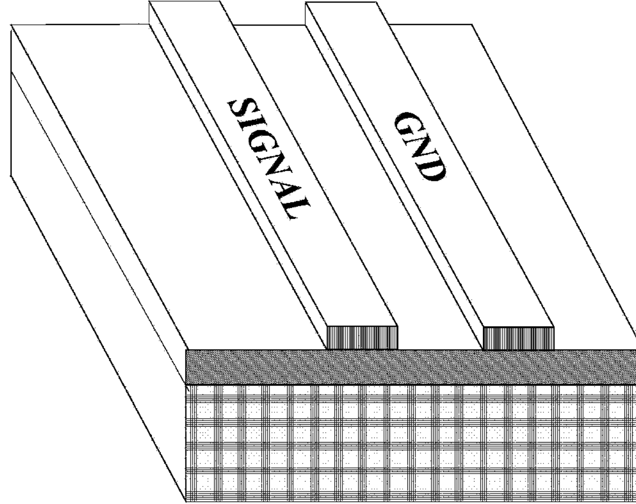


Figure 2.11: Coplanar stripline structure in CMOS technology.

amplifier, it conversely reduces the gain because of the voltage division at the gate of the transistors.

In many works on CMOS DA, a rolling-off gain versus frequency is reported. Shigematsu et. al. in [31] presented an RC degenerated common source gain cell to provide a flat gain within the amplifier's bandwidth. Although this method proves successful in flattening the gain, the proposed source degenerated transistor reduces the gain by a factor of $1 + g_m Z_{source}$. This technique has resulted in a small gain of 4 dB for the DA. To compensate for the loss of the transmission lines, we propose an alternative approach in Chapter 5 that is not in direct trade-off with the gain of the amplifier.

In another work, Lu et. al. [35] employed a non-uniform topology for gate and drain transmission lines to enhance the DA's gain and bandwidth performance. They have

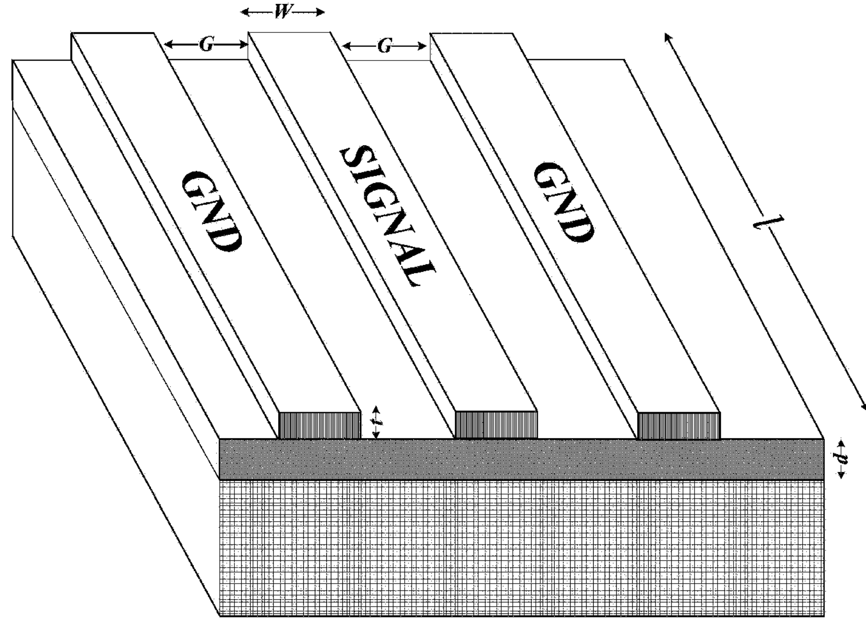


Figure 2.12: Coplanar waveguide structure in CMOS technology.

designed a DA with a 9.5 dB gain and 32 GHz bandwidth in a 0.18 μm CMOS process. The DA's power consumption is 99 mW provided by a 2.2 V DC supply.

A cascaded single-stage DA is reported in [32] that archives a gain of 9 dB with a unity gain bandwidth of 25 GHz. The cascaded topology connects the output of the first single-stage DA to the input of the second one. The purposed architecture multiplies the gains of two DAs rather than adding them if placed in a conventional format. Building on their work, they have proposed another CMOS DA with a larger bandwidth of 70 GHz [36]. In the second work, they cascaded two two-stage amplifiers to achieve a gain larger than 7 dB. The power consumptions of the first and second DA are 60 and 122 mW, respectively.

Finally, a macromachined CMOS DA is presented by Wang et.al. [34] with a bandwidth of 12.6-GHz. Deep trenches underneath the inductors of CMOS DA are created by dry etching to enhance their performance. As the quality of on-chip inductors improves, a 1-dB increase in amplifier gain and a 0.9-dB decrease in noise figure are achieved.

Chapter 3

Broadband RF CMOS Modeling

The first step in the design of RF CMOS circuits is to produce accurate models of the circuit components in their frequency band of the operation. These models are needed for the circuit design, simulation, and optimization. As CMOS DAs are constructed of the N-channel MOSFETs (NFETs) and on-chip inductors (or transmission lines), this section is devoted to the modeling of these RF devices.

3.1 Radio Frequency MOSFET Modeling

The radio frequency model of MOSFETs can be constructed upon its intrinsic low-frequency model (BSIM model [38]). As shown in Figure 3.1, several components must be added to the model usually neglected at low frequencies. The most important component, that will significantly affect the MOSFET performance at radio frequencies, is the gate polysilicon resistor.

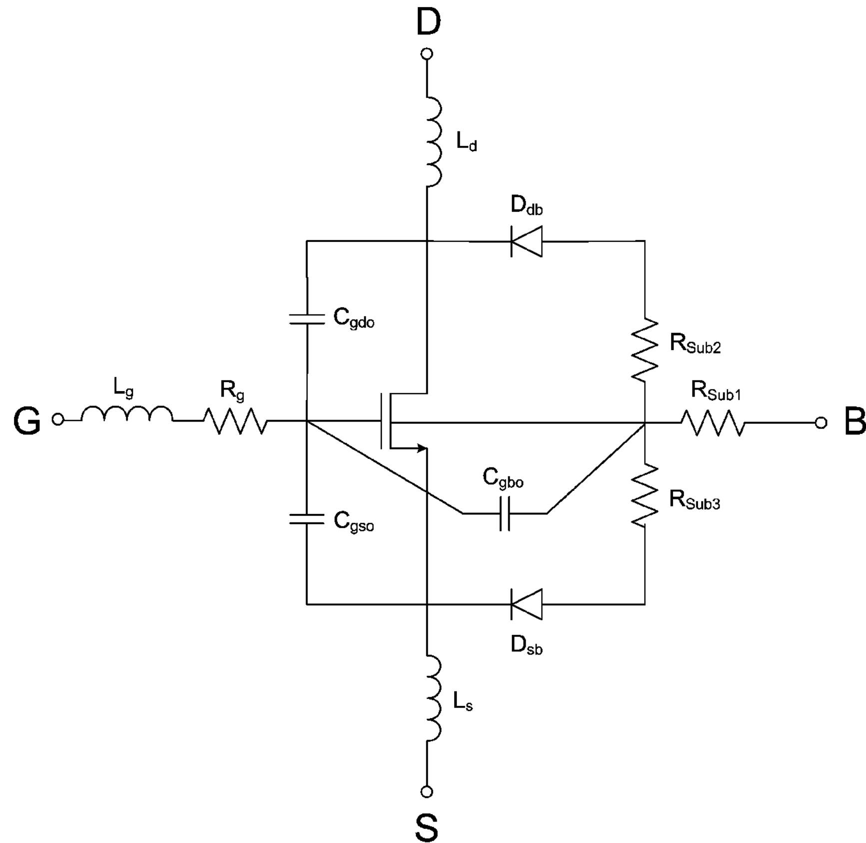


Figure 3.1: Radio frequency MOSFET model.

Gate Polysilicon Resistor

In RF/analog CMOS circuits, particulary amplifiers, MOSFET transistors usually require large W/L ratios to provide the transconductance (g_m) needed for the operation of the circuit. When large MOS transistors are used in analog/RF integrated circuits, the gate resistance becomes important. This resistance introduces thermal noise in the gate region, and causes a delay due to a distributed RC effect. In modern CMOS processes, the gate

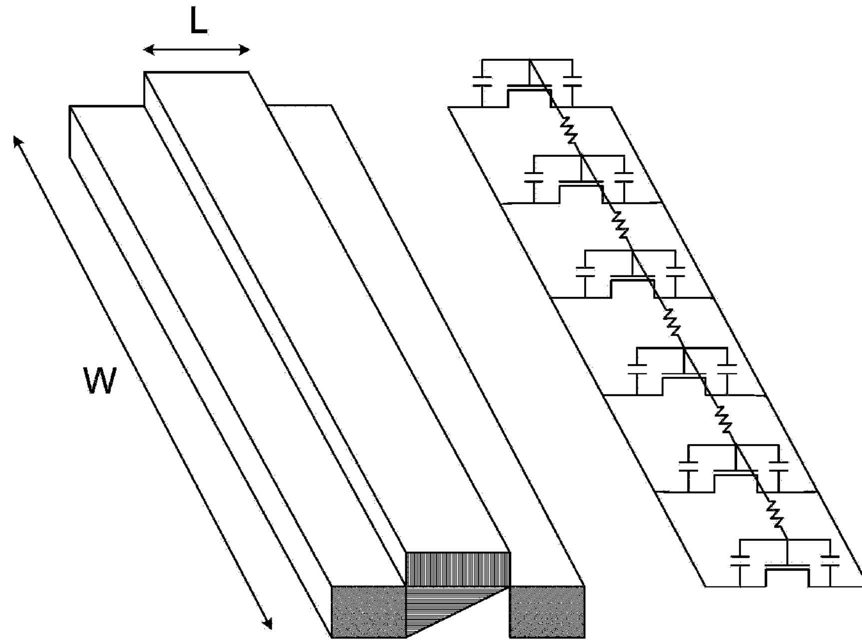


Figure 3.2: Distributed radio frequency MOSFET model.

is made of either a polysilicon layer or polysilicon/silicide layer.

To accurately model the gate resistor at very high frequencies, the MOSFET needs to be treated as a distributed device. As depicted in Figure 3.2, MOSFET parasitic elements, intrinsic and extrinsic capacitances, inductances, and resistances are distributed along the device. Although the figure shows a finite number of elements, the device can be divided into an infinite number of transistors and resistors.The typical resistance for a polysilicon gate ranges between 20-40 $\Omega/square$. Abou-Allam et al. in [39] present a complete small signal MOS model based on the distributed MOSFET. Consider a signal applied at the gate of the MOSFET at point x = 0. This signal produces voltages that are equal at any point on the gate, and therefore, the drain current is equal at any point along x if the

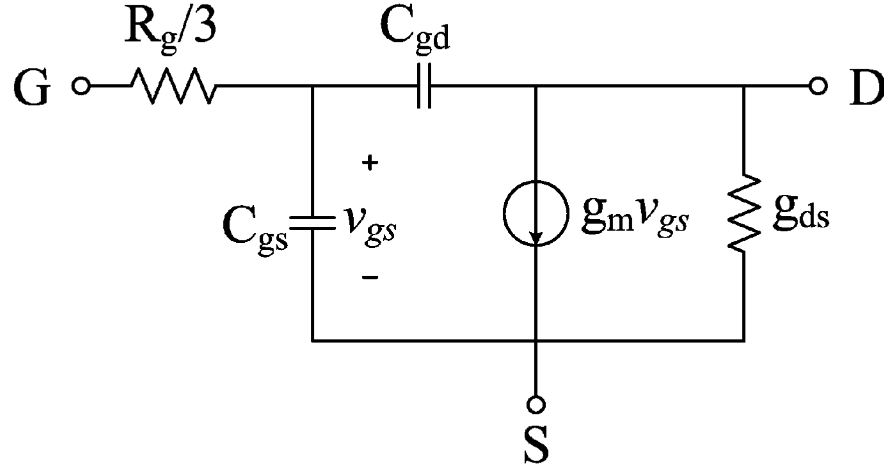


Figure 3.3: Small signal model of RF MOS transistors including gate resistor.

effect of gate resistance is not considered. While this may be true for small devices, it is not for large W devices. If the polysilicon gate resistance is not neglected, the voltage magnitude is different along the channel as the signal tries to charge the gate capacitance of each of the small transistors; this capacitance along with the distributed gate resistance will cause a delay in the charging mechanism. Therefore, the drain current is also different from one point to another. In this case, the gate functions like a transmission line, causing the applied signal to travel across it in the form of incident and reflected waves.

However, the distributed model is very accurate; it has been reported that lumped elements modeling of MOSFETs can predict its performance at high frequencies very accurately by adding a gate resistor with a value one third of the physical resistance of the polysilicon layer ($R_g/3$) [40]. This simple lumped-element circuit, shown in Fig 3.3, can accurately model the essential distributed gate resistance effect and is well suited for manual

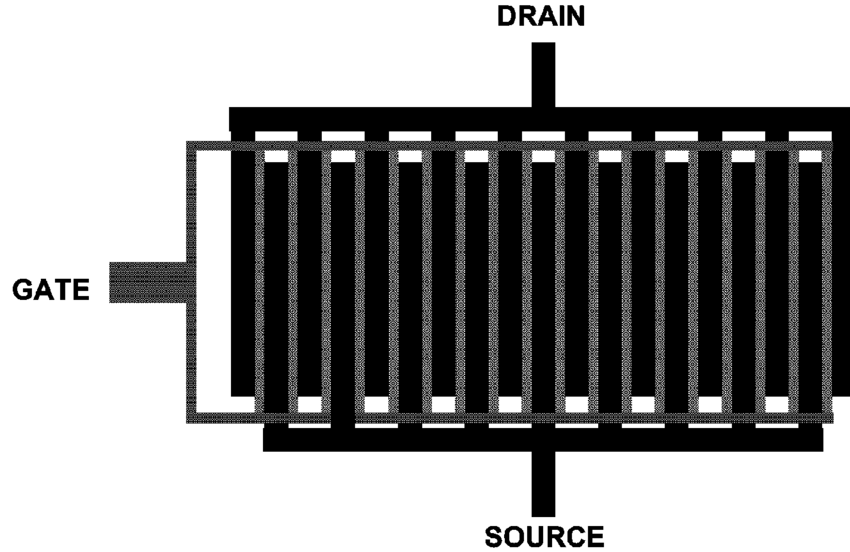


Figure 3.4: Multi-Finger MOSFET Layout.

analysis and design, and compact modeling.

To minimize the effect of the gate resistance on transistor performance, the MOS transistor is usually laied using multiple fingers, as depicted in Figure 3.4.As the total width of MOSFET is divided by the number of fingers (N_f), the gate resistance of the transistor is reduced by a factor of N_f as well. The equivalent resistance of the polysilicon gate from $R_g/3$ to $R_g/12$ can be further reduced if the gate lines are connected at both ends using metal interconnects.

Finally in addition to the polysilicon gate resistance, all the external capacitances and inductances of the MOSFET must be taken into account in high frequency modeling as shown in Figure 3.1. These capacitors and inductors are usually ignored for low-frequency modeling.

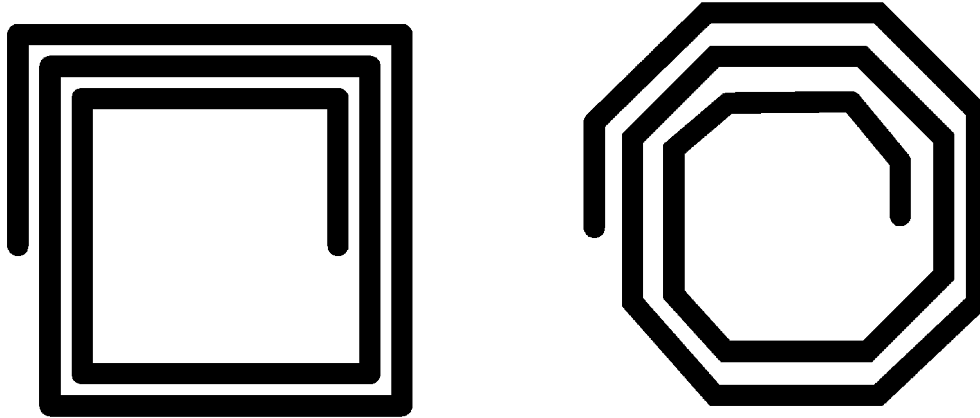


Figure 3.5: Layout of square and octagonal spiral inductors.

3.2 On-Chip Spiral Inductor Modeling

Typically, on-chip CMOS inductors are fabricated in the form of a spiral. A circular inductor offers the largest inductance per area as the circle has the largest ratio of perimeter to area amongst the two dimensional shapes. However, circular spiral inductors are practically impossible to lay out in current CMOS technologies as most CMOS processes limit all angles at 90 degrees. Therefore, a square version of the spiral is the most commonly used layout. As a compromise between a purely circular spiral and a square spiral, an octagonal spiral is an alternative for the technologies that allow the angle to be 45 degrees. The layouts of the different on-chip inductors are shown in Figure 3.5.

Because of the limited resistivity of the metal interconnects and semiconductive nature of the silicon substrates, the on-chip inductors dissipate a significant amount of power both in metal and substrate. The next section describes the loss mechanisms of on-chip inductors, and provides the expression for the quality factor of on-chip inductors.

3.2.1 Loss Mechanisms in On-Chip Inductors

The quality factor of an inductor is defined as

$$Q = \frac{E_{stored}}{E_{dissipated}} \tag{3.1}$$

Where E_{stored} and $E_{dissipated}$ are energy stored and dissipated per cycle, respectively. If one node of the inductor is connected to ground and the impedances seen from the other node is denoted by $Z_{equivalent}$, the qualify factor can be easily calculated by

$$Q = \frac{imag[Z_{equivalent}]}{real[Z_{equivalent}]} \tag{3.2}$$

Metal Loss

On-chip inductors are constructed from layers of metal, typically aluminum and/or copper. Metal conductors used in an inductor have a limited conductivity. Most of the reactive energy is stored in the magnetic field of the device, but energy is dissipated in the volume of the conductors in the form of heat. At increasingly higher frequencies, two phenomena known as the skin and proximity effects change the current distribution in the metal layers. This occurs because alternating magnetic fields of the device penetrate the conductors and create contrasting electric fields in the volume of the conductors.Therefore, they increase the resistivity of the conductors in the middle area forcing the currents to flow through the outer layer or skin of the conductors, decreasing the effective cross-section of the conductor, and thus increasing the resistance as frequency increases. This phenomenon becomes worse at higher frequencies. This increase in the AC resistance is known as the skin effect, and

typically has a $\sqrt{f}$ functional dependence. Moreover, if the nearby conductors enhance the magnetic field near a given conductor, the AC resistance will increase even further, which is the case for a spiral inductor.

Substrate Loss

On-chip inductors are placed on top of a conductive Si substrate with only a few micrometers of vertical distance. The Si substrate resistivity varies from 10 for a lightly doped Si substrate ($10^{13} atoms/cm^3$) to .001 $\Omega.cm$ for a heavily doped Si substrate ($10^{20} atoms/cm^3$). The conducting nature of the Si substrate leads to various forms of loss in the substrate. These losses are caused by the flow of three groups of currents in a conductive substrate which are explained as follows:

- Electric energy is coupled to the substrate through displacement current. This displacement current flows through the substrate to grounds in close proximity.
- On-chip inductors produce magnetic fields that penetrate the substrate because of the proximity of the inductor and substrate. The penetrated magnetic fields produce time-varying solenoidal electric fields across the substrate, which in turn induce substrate currents.
- Electromagnetic radiation occurs at much higher frequencies where the physical dimensions of the device approach the wavelength at the frequency of propagation. Even at 100 GHz, the wavelength is 3mm which is much larger than any on-chip device. Therefore, we can safely ignore the electromagnetic propagation loss.

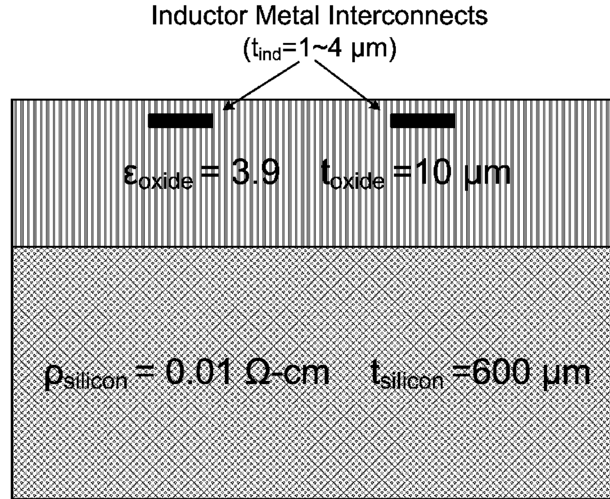


Figure 3.6: Cross-section of typical CMOS substrate layers.

3.2.2 EM-Based On-chip Inductor Modeling

3D Electromagnetic (EM) simulators model the on-chip CMOS spiral inductors by solving Maxwell's equations numerically, and satisfying the boundary conditions in the IC volume. A sample of the IC environment is shown in Figure 3.6. Maxwell [41], EM-Sonnet [42] and MagNet [43] are examples of such tools [44]. Faster quasi-3D simulators such as Momentum [45], which uses Green's functions approach to solve Maxwell's equations, are also available. EM simulators are accurate, but computationally intensive. Therefore, they are mostly used for accurately simulating simple structures, but not large three-dimensional structures. To simulate large systems, powerful processors and long simulation runs are necessary. This problem becomes worse in the case of an on-chip inductor, since the spacing between the conductors is usually small compared to their width. Simulators

such as ASITIC [46] [47] are customized for the simulation of on-chip spiral inductors and transformers. These tools use magnetostatic and electrostatic approximations to quickly solve the field matrices.

Where the passive components are placed close to each other, the individual modeling of each component fails to provide accurate results as the electromagnetic and electrostatic coupling among them is neglected. EM simulators are also ideal tools for the post-layout verification of passive structures including several passive components as will be discussed in Chapter 4. Although EM simulators provide the most accurate simulation results, they cannot easily be used for the design purposes. The main drawback of the EM simulation is that it does not provide a scalable model which is needed for high frequency circuit design. The next section discuses the compact modeling that can be used for the design of on-chip inductors.

3.2.3 Physical-Based On-chip Inductors Model

The disadvantage of 3D EM simulators indicates the need for a compact inductor model that can easily be incorporated into a circuit simulator. Figure 3.7 displays a typical integrated spiral inductor on silicon, where each part of the structure can be represented by a lumped element. Significant work has been done in the modeling of spiral inductors using several compact circuit models. In these models, an equivalent π circuit represents the spiral with the inductance and series resistance in the series branch. The spiral-to-substrate capacitances and the substrate parasitics and losses are presented in the shunt branches.

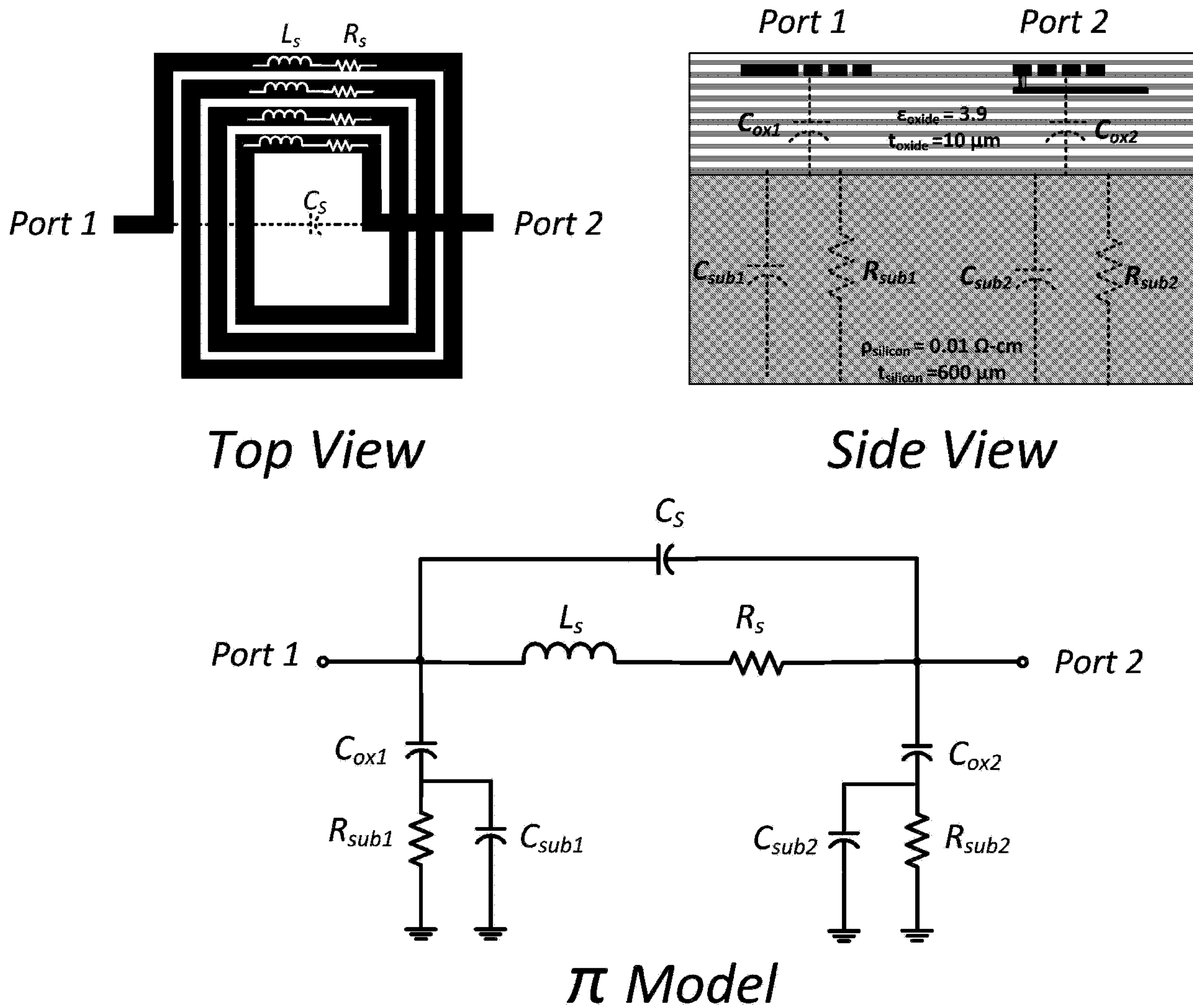


Figure 3.7: π circuit model of on-chip inductor.

The series resistance of the spiral inductor , R_S, is given by

$$R_S \approx \frac{l}{\sigma w \delta (1 - e^{-t/\delta})} \tag{3.3}$$

where l is the total length of the spiral, σ is the conductivity of the metal, t is the thickness of the metal, and w is the metal line width; δ is the skin length which models the increase in the resistance with the increase in the frequency due to the skin effect, and is given by

$$\delta = \sqrt{\frac{1}{\pi f \mu \delta}} \tag{3.4}$$

where f is the frequency, and μ is the magnetic permeability of the free space.

The spiral substrate oxide capacitance, C_{ox}, accounts for the inductor's parasitic capacitance between inductor and substrate. It is well approximated by the following equation:

$$C_{ox} \approx \frac{1}{2}\frac{\epsilon_{ox}}{t_{ox}} lw, \tag{3.5}$$

where ϵ_{ox} is the oxide permittivity, and t_{ox} is the oxide thickness between the spiral and the substrate.

The C_S capacitance models the so-called "underpass" interconnect. It is expressed as follows:

$$C_S \approx \frac{\epsilon_{ox}}{t_{ox,M1-M2}} nw^2, \tag{3.6}$$

where $t_{ox,M1-M2}$ is the oxide thickness between the spiral and the underpass.

The substrate capacitance, C_{Si} is given by the following expression:

$$C_{Si} = \frac{1}{2} C_{sub} lw \tag{3.7}$$

where C_{sub} is the substrate capacitance per unit area. The substrate resistance, R_{Si} can be expressed as

$$R_{Si} \approx \frac{2}{G_{sub}} lw \tag{3.8}$$

where G_{sub} is the substrate conductance per unit area. C_{sub} and G_{sub} are generally treated as fitting parameters as the substrate impedance is difficult to model.

Inductance Calculation

The L_S is defined as the series inductance of the on-chip inductor at low frequencies. Since spiral inductors are made of straight lines, the first step is to calculate the inductance of a straight line. If a conductor carries the currents with densities J_m of J_n over their cross sections A_m and A_n, its static self-inductance and mutual inductance can be generally expressed as [48]

$$L_{mn} = \frac{\mu}{4\pi I_m I_n} \int_{A_m} \int_{A_n} \oint_{C_m} \oint_{C_n} \frac{\overrightarrow{J_m}.\overrightarrow{J_n}}{r_{mn}} d_{J_n} d_{J_m} d_{A_n} d_{A_m}. \tag{3.9}$$

In case of a straight line with a width of w, a length of l, and a metal thickness of t, the integral in 3.9 can be simplified to

$$L = \frac{\mu_0 l}{2\pi}\{arsinh(\frac{l}{w+t}) + \frac{l}{w+t} arsinh(\frac{w+t}{l}) + \frac{w+t}{3l} - \frac{1}{3}(\frac{l}{w+t})^2[(1+\frac{(w+t)^2}{l^2})^{3/2} - 1]\}, \tag{3.10}$$

if w is much larger than t. If the w and t are in the same range, which is the case of a spiral inductor, a geometrical mean method is used for the calculation of the inductance as follows [49]:

$$L = \frac{\mu_0 l}{2\pi}[\ln(\frac{2l}{\rho}) - 1] \tag{3.11}$$

where

$$\ln(\frac{\rho}{c}) = \frac{25}{12} - \frac{1}{6}\{(\frac{w}{t})^2 \ln(\sqrt{1+(\frac{t}{w})^2}) + (\frac{t}{w})^2 \ln(\sqrt{1+(\frac{w}{t})^2})\} + \frac{2}{3}\{\frac{w}{t}\arctan(tw) + \frac{t}{w}\arctan(wt)\} \quad (3.12)$$

The expressions for self and mutual inductance (L and M) in nH can be significantly simplified to [50]

$$L = 2l(\ln\frac{2l}{w+t} + 0.5 + \frac{w+t}{3l}) \quad (3.13)$$

$$M = 2l(\ln[\frac{l}{GMD} + \sqrt{1+(\frac{l}{GMD})^2}] - \sqrt{1+(\frac{GMD}{l})^2} + \frac{GMD}{l}) \quad (3.14)$$

where GMD is the geomantic mean distance and given by

$$\ln(GMD) = \ln(d) - \frac{w^2}{12d^2} - \frac{w^4}{60d^4} - \frac{w^6}{168d^6} - \frac{w^8}{360d^8} - \cdots \quad (3.15)$$

Note that in the above equations all dimensions are in cm.

The total spiral inductor can now be calculated by breaking the spiral inductor into N straight line segments. The static self inductance L_i ($i = 1, 2, , N$) and mutual inductance between two different line segments M_{jk} ($k \neq j = 1, 2, , N$) can be computed using 3.14. Then, the total spiral inductance can be expressed as [51]

$$L = \sum_{i=1}^{N} L_i + \sum_{i=1}^{N}\sum_{j=1}^{N} M_{ij(i \neq j)} \quad (3.16)$$

3.2.4 Broadband On-Chip Inductor Modeling

As discussed earlier, the metal conductors of a spiral inductor experience two phenomena, the skin effect and magnetic field induced proximity effect, that increase loss of the on-chip

inductors as frequency increases.

The skin effect is attributed to the fact that alternating current in a metal conductor will flow increasingly on the surface as frequency increases. This will reduce the effective cross-section and causes the conductor resistance and inductance change with frequency. At high frequencies, the resistance of a conductor increases as a function of the square root of frequency and the inductance decreases slightly and then levels off.

The proximity effect is caused by an enhanced magnetic field in the central portions of the spiral tends to cause nonuniform current flow in the turns. Inner turns tend to have current flow only on the innermost edge of each turn, while outer turns tend to carry current on their outermost edges. This effect is frequency dependent as the magnetic field increases with increasing frequency. The non-uniform current flow tends to cause effective spiral resistance to rise faster than can be attributed to the skin effect. In addition, the net inductance will decrease due to an effective reduction in the radius of the spiral caused by the current crowding to the innermost edge of the inner turns.

One way of implementing these frequency dependent losses in the pi model is to use frequency dependent lumped elements. As general circuit simulators such as Spectre and Spice can only calculate the frequency-dependent elements values at one frequency point per simulation, this method is not appropriate for circuit simulation. If implemented this way, a frequency at which to calculate the element values is specified at simulation run-time and that value will be used for the entire simulation, even if a broadband circuit simulation is run. A revised method of implementing this frequency dependent behavior in an inductor model is to use an R-L ladder network, shown in Figure 3.8 to replace the

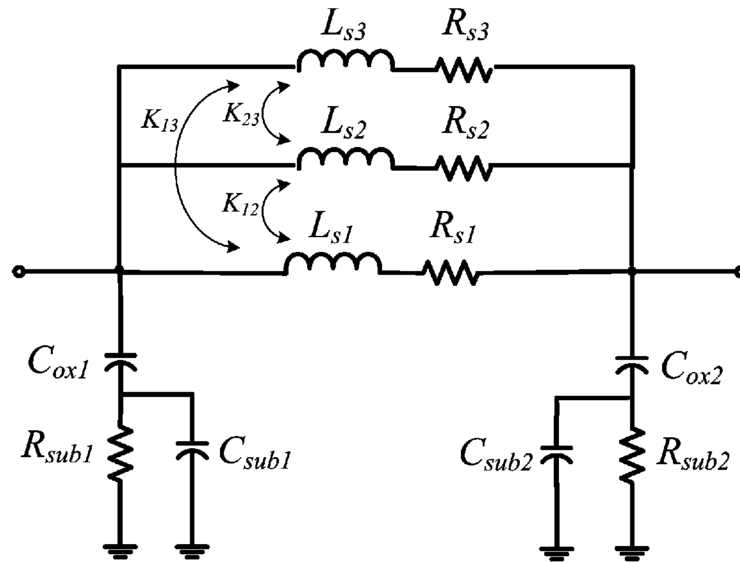


Figure 3.8: Modeling frequency-depends series inductor and resistor.

series loss elements in the model. The element values can be fitted such that the desired frequency dependent behavior is achieved while maintaining the ability to simulate all frequencies under all simulation conditions.

Chapter 4

Area-Efficient DA Design

A key drawback of a fully integrated DA is its large die area as it requires 2N+2 inductors for an N-stage implementation. If the on-chip spiral inductors are used, the area of these spiral inductors and their minimum separation from each other determines the total area of the chip. In the case of CMOS coplanar striplines and waveguides, they are usually placed distant from each other such that the capacitive and inductive coupling are minimized. Taking into consideration that the area of the on-chip spiral inductors and waveguides, and consequently the area of the CMOS DAs, does not scale with the technology's feature size, exploring alternative implementation of the inductors for cost-effective fully integrated CMOS chips is necessary. One possible solution of an area-efficient design is to place the passive components close to each other; a method which is usually avoided because of the lack of accurate models. To overcome this obstacle, we present an EM-based modeling methodology that can model the electromagnetic behavior of the passive component of an RF IC taking into account the effect of electromagnetic couplings.

4.1 Co-simulation Methodology

This section presents a general purpose modeling methodology for EM simulation of RF CMOS circuits and systems. Accurate design and modeling of active and passive components, particularly on-chip inductors and interconnects, is essential for a successful RF CMOS chip design. This method is developed for post layout simulation and verification of both closely placed on-chip inductors and interconnects.

In the conventional method, each passive CMOS component is modeled individually using EM simulators [52, 53]. This EM-simulation provides accurate results only if the simulated component is laid out in an area of the chip that is far enough from other circuit elements especially other passive components. Usually the EM-based simulation results are plugged into a circuit simulator along with other neighboring active and passive components. If the circuit components are placed close to each other in the final layout, their coupling may invalidate the accuracy of the final simulation of the circuits. In the proposed methodology, after the final layout, the circuit is partitioned in two parts: an active area (transistors) and a passive area (passive components such as inductors, capacitors, and resistors) as depicted in Figure 4.1. The passive area is simulated using a 3D EM simulator, and a corresponding N-port network model (based on S-parameter simulation) is obtained. This model along with the active device models (based on measurement) is used to obtain the electrical characteristics of the overall circuits as explained in Section 4.1.1. These post layout simulation results are more accurate because

- they take into account the effect of coupling, both inductive and capacitive, of the passive components, and

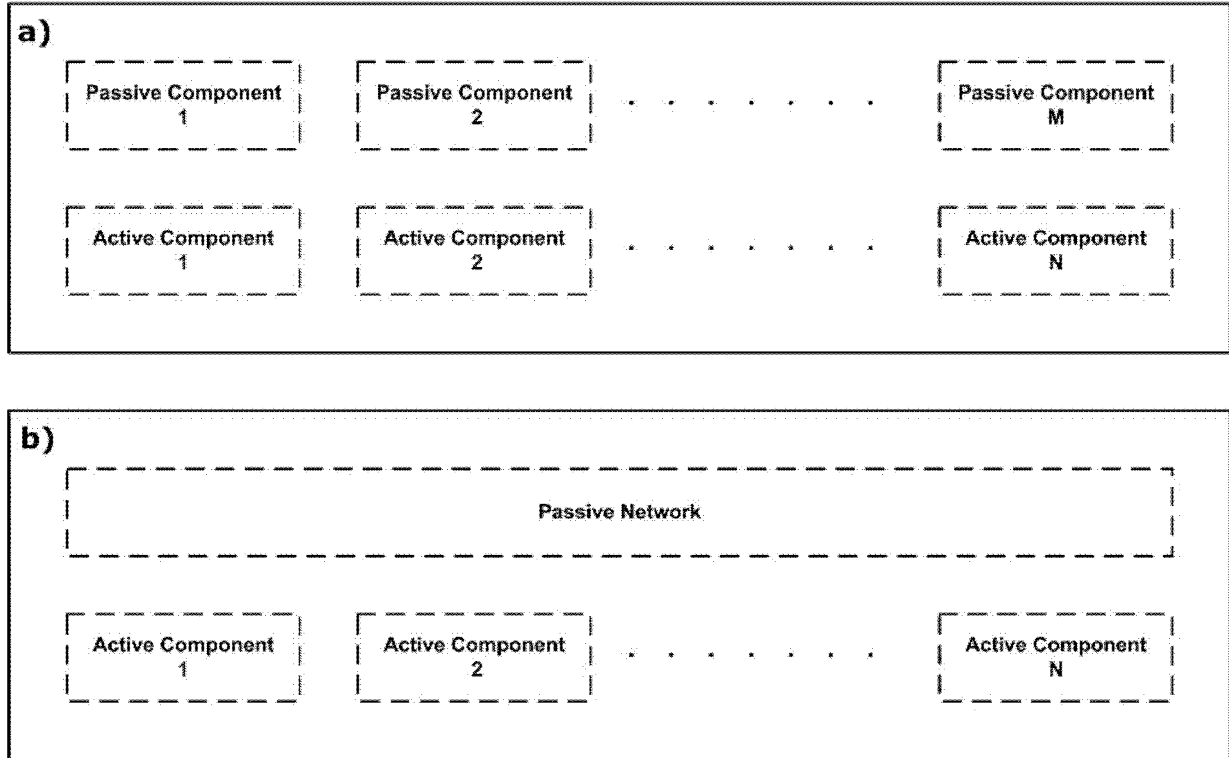


Figure 4.1: Representation of (a) individually modeled passive components, and (b) proposed passive and active partitioning.

- they take into account the parasitic effect of interconnects used to connect the passive components to each other or active components.

The next section explains how the results of the passive and active part of the RF circuit can be integrated to obtain the S-paymasters of the overall circuit.

4.1.1 Final S-parameters Calculation

Assume that we have a network with N passive sub-networks and M active sub-networks. Using a standard network analysis procedure [54], we can find the final S-parameters of the network as a function of its passive and active sub-networks' S-parameters:

First, we need to identify the internal and external ports of the network: internal ports are those ports that are terminated (load/ground) or connected to an adjacent sub-network. The rest of the ports, external ports, are those that act as ports of the main network. Assume that the network has K external ports and J internal ports. Next, record the information in the following (K+J) (K+J) matrix:

$$\begin{pmatrix} V_E^- \\ V_I^- \end{pmatrix} = \begin{pmatrix} S_{EE} & S_{EI} \\ S_{IE} & S_{II} \end{pmatrix} \begin{pmatrix} V_E^+ \\ V_I^+ \end{pmatrix} \tag{4.1}$$

where V_E^+,V_E^-,V_I^+, $V_I^-$and are the vectors of the incident and reflected voltages of external and internal ports, respectively. The elements of matrices S_{EE}, S_{EI}, S_{IE},and S_{II} are easily given by the equation

$$S_{ij} = \{ \begin{matrix} 0 & \text{if there is no direct connection between i and j through any of the subnetworks} \\ S_{ij_subnetwork} & \text{if there is a direct connection between i and j through one of the subnetworks} \end{matrix} \tag{4.2}$$

The next step is to find the connection matrix Γ for the internal ports: In this step, we enter the network connection configuration using connection matrix

$$V_E^- = \Gamma V_E^+. \tag{4.3}$$

The elements of Γ are given by the relation imposed on the internal ports by the interconnection among the sub-networks. For example, if port X of sub-network Y is directly

connected to port X' of sub-network Y', the following relations shall be plugged in the connection matrix as

$$\begin{aligned} V_{X'}^- &= V_X^+ \\ V_X^- &= V_{X'}^+. \end{aligned} \tag{4.4}$$

These relations set two elements, $S_{XX'}$ and $S_{X'X}$, of the Γ equal to 1. In another case, if port Z is terminated in a load with a reflection coefficient of Γ_L , the relationship

$$\frac{V_Z^+}{V_Z^-} = \Gamma_L \tag{4.5}$$

sets the value of S_{ZZ} in the connection matrix equal to $\frac{1}{\Gamma_L}$.

In the final expression of the equation, the final S-parameters of the external port of the network can be obtained using

$$S^R = \frac{V_E^-}{V_E^+} = S_{EE} + S_{EI}[\Gamma - S_{II}]^{-1} S_{IE} \tag{4.6}$$

4.1.2 Case Study

In this section, we propose two test structures to investigate the improvement in the accuracy of the simulation using the proposed post layout simulation method.

Adjacent spiral inductors

In the first case study, we compare the EM simulation results of two spiral inductors while they are simulated simultaneously on the same substrate with those that are simulated

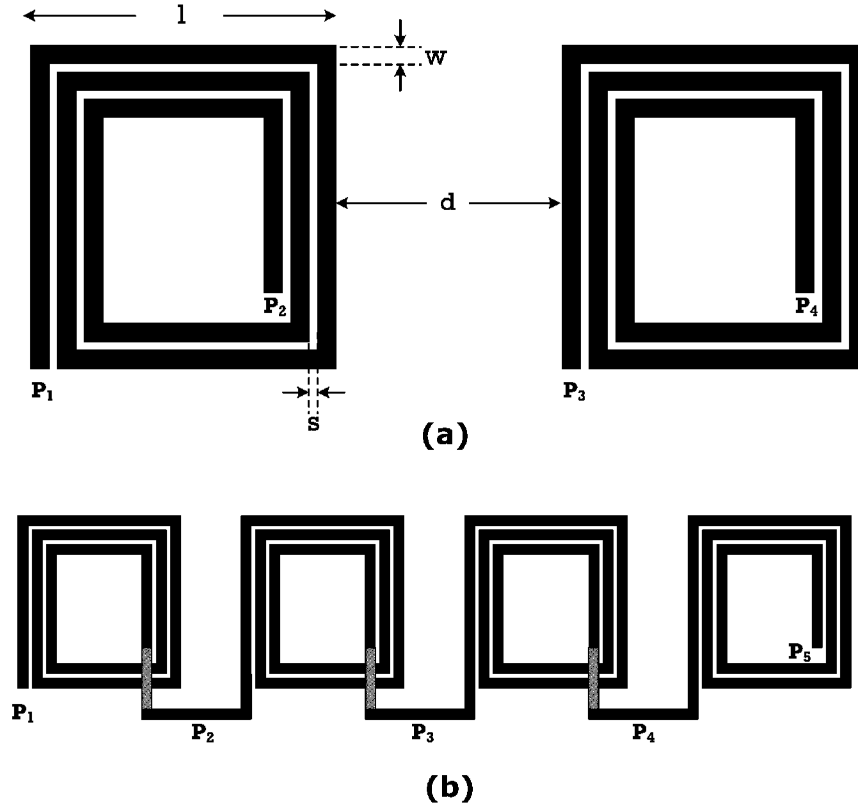


Figure 4.2: Layout of the simulated adjacent square spiral inductors, and b) layout of simulated artificial transmission line.

individually. Adjacent inductors can be found in many RF CMOS circuits such as differential LNAs and LC tank VCOs. The layout of the square spiral inductors is shown in Figure 4.2. A typical silicon substrate with a thickness of 600 μm and relative permittivity of 11.9 is chosen for EM simulation. Spiral inductors are implemented onto the top metal layer of technology with a thickness of 1 μm separated with 10 μm of silicon oxide dielectric from the silicon substrate. The network is simulated as a four-port network.

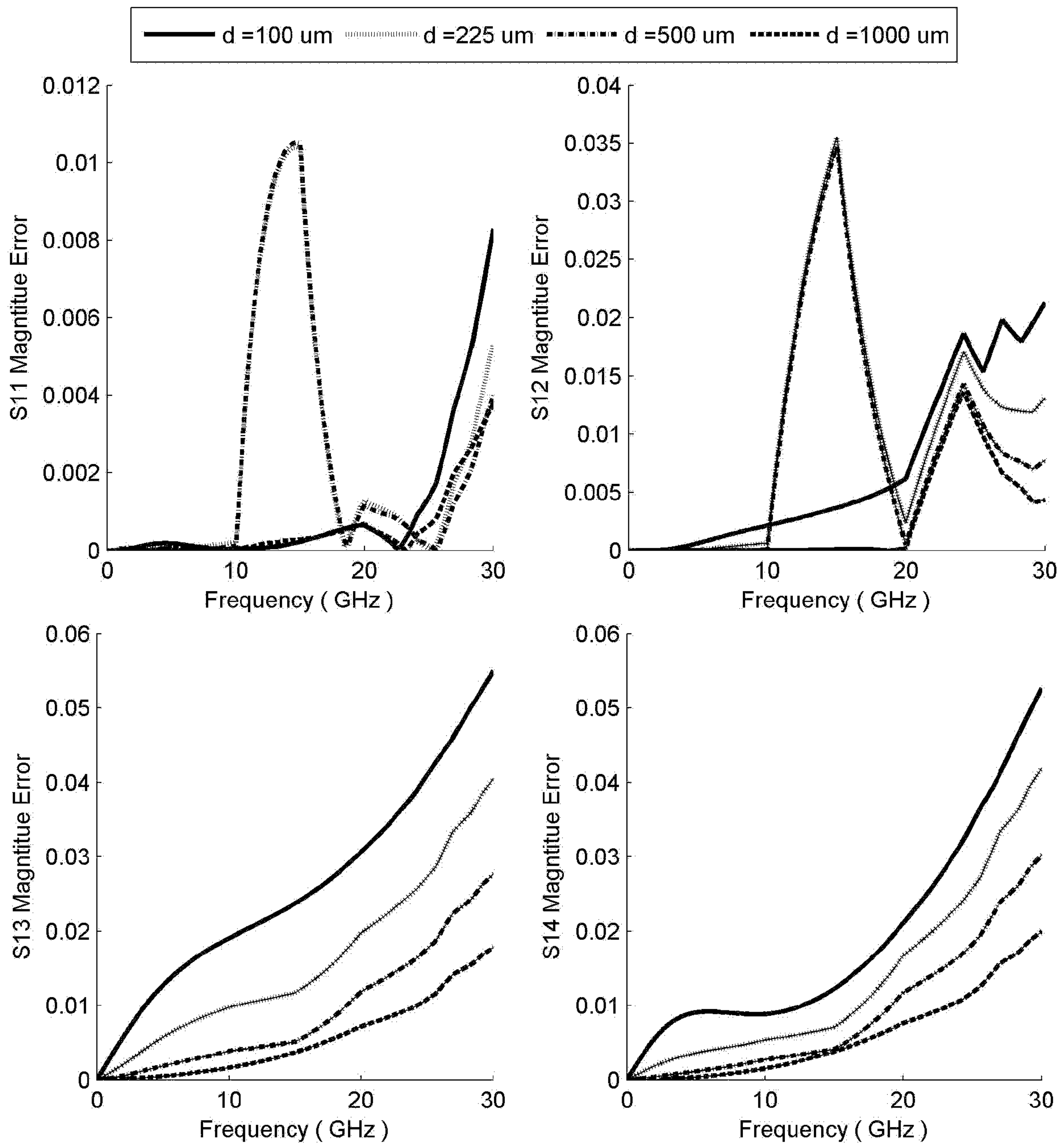


Figure 4.3: Difference between individually EM-modeled inductors S-parameters and post-layout EM modeled S-parameters of two adjacent inductors.

S_{11}, S_{12}, S_{21}, and S_{22} are regarded as the self coefficients, while S_{13}, S_{14}, S_{23}, and s_{24} are the ratio of the power transferred from one inductor to the adjacent inductor. The difference between S-parameters of the inductor in the combined network as a function of the inductors' distance (d) from each other with those of a single inductor is illustrated in Figure 4.3. If the inductors are modeled individually, clearly the effect of coupling between inductors is neglected ($S_{13} = 0$ and $S_{14} = 0$); however, when two spiral inductors are simulated simultaneously on the same substrate, the results indicate that a coupling as strong as a few percentages of power transfer exists among their ports. The coupling increases as the inductors proximate each other, and as frequency increases. Although the simulation results indicate that simulation errors remain below 10%, depending on the number of passive components and the circuit topology, these errors can be accumulated, degrading the circuit performance dramatically.

Artificial transmission lines of distributed amplifier

In the second case study, a more complicated structure is chosen. Since the interconnects with normal length are not considered as distributed elements, transmission lines in CMOS technology are artificially constructed from a ladder of inductors and capacitors. These transmission lines are used as matching networks to guarantee maximum power transfer from one stage to the next. Transmission lines are also used in distributed amplifiers to compensate for the frequency response of the MOSFETs, and to provide a flat gain over a large bandwidth. Transmission lines are among the best RF circuits for the purpose of comparing post and pre layout simulation results as they consist of several on chip

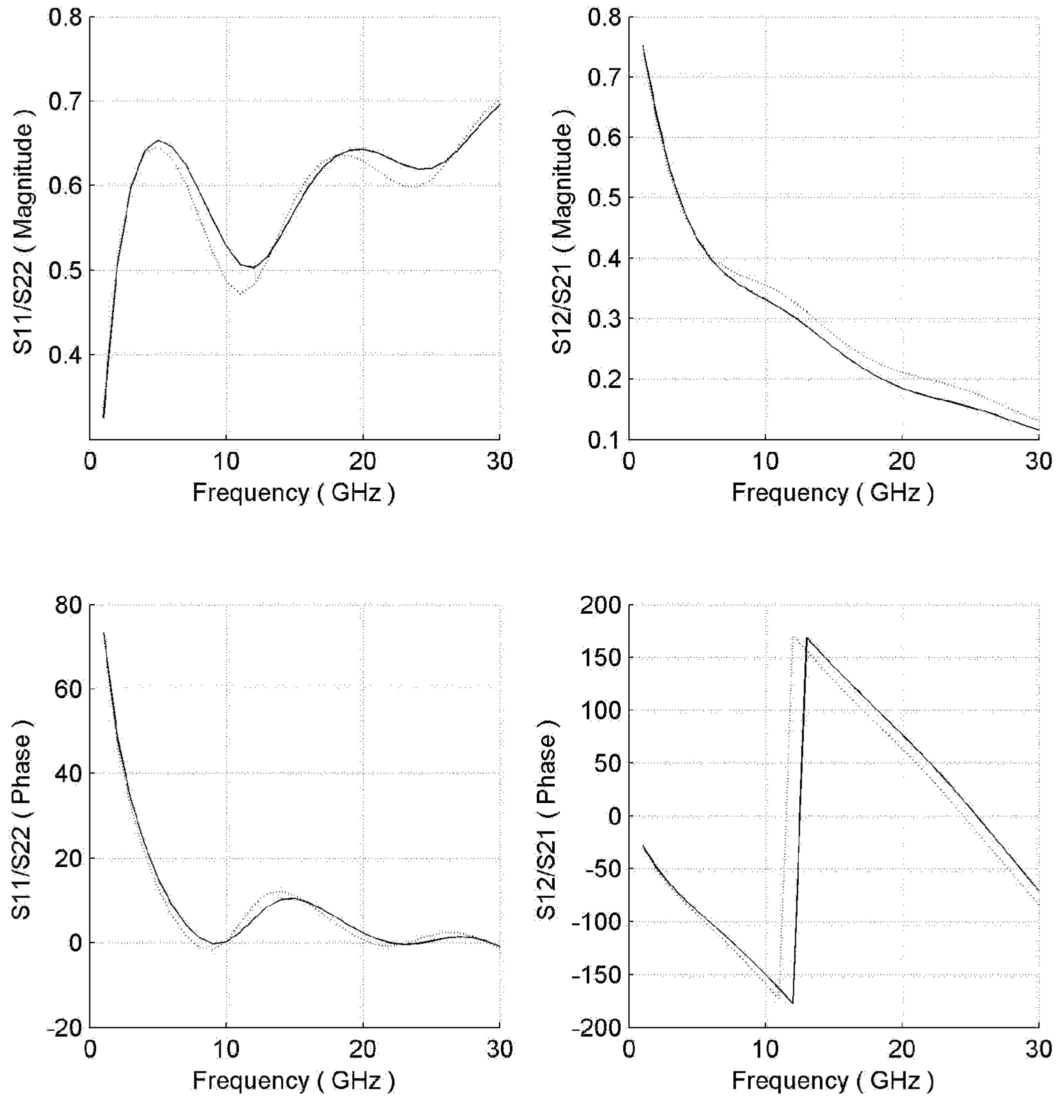


Figure 4.4: Post-layout (solid) versus pre-layout (dashed) EM simulation results of a four-stage artificial transmission line ($d = l/2$).

inductors, capacitors, and resistors, and operate over a wide frequency range. In this test structure, four identical spiral inductors are placed in a cascade topology as shown in Figure 4.2(b). Figure 4.4 shows S parameter simulation results when the inductors are modeled both separately (dashed lines) and simultaneously (solid lines). These results clearly indicate that a noticeable difference is seen between S-parameters of the same circuit based on two different methodologies. These results prove that the proposed post-layout simulation improves the accuracy of the simulation considerably, and must be used as the last step before final tape-out to ensure that the final layout meets the required performance of the RF CMOS circuit.

4.2 Area-Efficient CMOS DA

In this design, we use closely-placed single wire top-metal interconnects to provide the inductances needed for the gate and drain transmission lines. As the interconnects are placed close to each other, they cannot be individually modeled since inductive and capacitive coupling cannot be neglected. The self inductance of a straight interconnect line with a rectangular cross section and its mutual inductance with another interconnect can be approximated to

$$L_S = 2l \times ln(\frac{2\sqrt{e}l}{w+l}) \tag{4.7}$$

$$M = 2l \times ln(\frac{2l}{ed}) \tag{4.8}$$

assuming that the length of the interconnects (l) is several times larger than the widths (w), thickness (t), and the distance between two interconnects. One disadvantage of the compact layout is the decrease in inductance per unit length compared with the spiral inductors because of the negative mutual inductance of the adjacent interconnects ($-M_1$). Figure 4.5 shows the mutual inductance between interconnect segments, and the compact circuit model for the first segment of stage K. L_S is the self inductance of the interconnect segment, C_{ox} models the capacitive coupling between the interconnect and substrate, and R_{sub} represents the substrate loss. The mutual inductors between this segment and other interconnects are modeled using dependent current sources (up to 3rd order). To verify the accuracy of this lumped-element model, the overall structure of the interconnects is EM simulated in a three-dimensional environment using the methodology discussed in Section 4.1. Based on EM-simulated S-parameters, the equivalent circuits are correlated to be supplied to a Spectre circuit simulator.

The first step in the design of a distributed amplifier is to find the values of the capacitors and inductors of the gate and drain transmission lines such that they provide the required bandwidth of the DA. The resistive loss and substrate loss of the interconnects reduces the gain of the amplifier and degrades the input/output matching as frequency increases, preventing the DA from achieving its expected bandwidth. To overcome this performance degradation due to the limited quality factor of the interconnects, we devised the DA with a bandwidth several times larger than what we expected the presence of the resistive loss of the interconnects and substrate loss to be. This design technique results in smaller values for inductors requiring shorter transmission lines. As a proper DA design

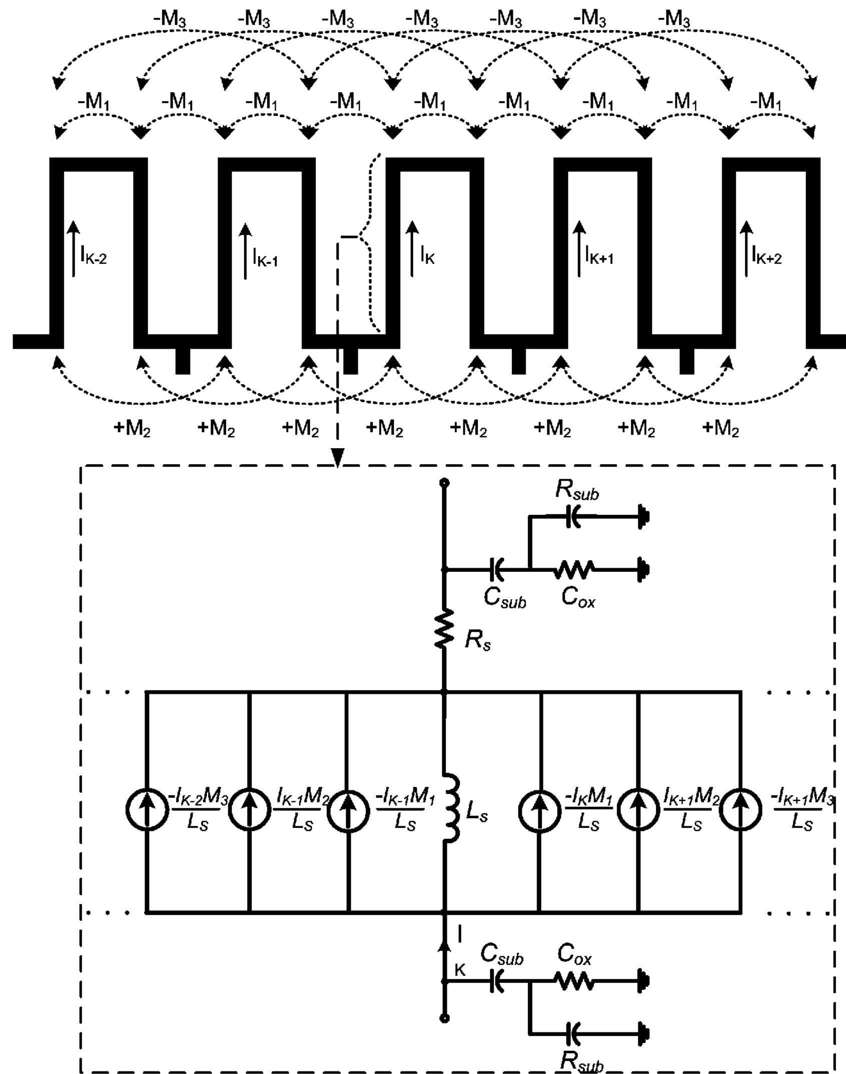


Figure 4.5: Mutual inductors between closely-placed interconnects, and equivalent circuit of segment K of CMOS interconnects.

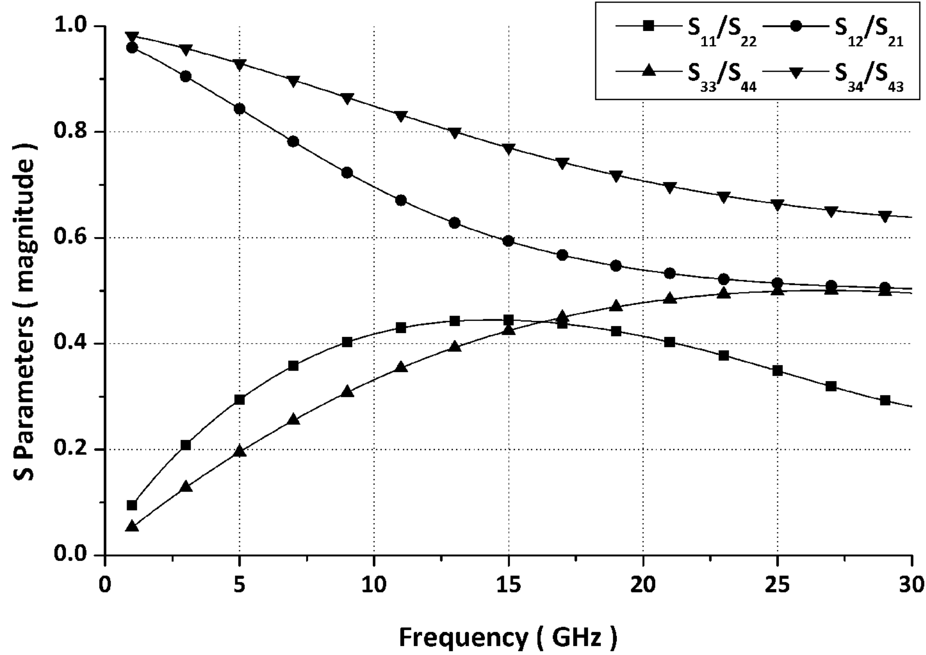


Figure 4.6: EM simulation results for unloaded closely-placed transmission lines.

requires equal signal delays on the gate and drain transmission lines, the gate and drain transmission lines' bandwidths, $1/\sqrt{L_gC_g}$ and $1/\sqrt{L_dC_d}$, are required to be equal.The EM simulation results for the proposed closely-placed transmission lines are shown in Figure 4.6.

To ensure proper matching at input/output ports, the characteristics impedance of the gate and drain transmission lines, $Z_{gate}(=\sqrt{L_g/C_g})$ and $Z_{drain}(=\sqrt{L_d/C_d})$, must be chosen equal to or close to the terminating resistors of the lines, R_g and R_d, respectively. If the DA is not connected to an off-chip load, it is not required to match the output line to

a 50 Ω load. Instead, we choose to terminate the output transmission lines with a 100 Ω to improve the gain of the amplifier. The 2 to 1 ratio of Z_{drain} to Z_{gate} is chosen because the total parasitic capacitance at the gate of the NMOS transistors is almost twice that of the parasitic capacitance at the drain terminal. Therefore, no additional capacitor is needed to equalize the bandwidths of the gate and drain transmission lines, as the inductors of the drain transmission line are two times larger than those of the gate transmission line ($L_d = 2L_g$ and $C_g = 2C_d$). This condition implies the drain interconnects' length is required to be two times the gate interconnects' length.

The proposed DA circuit is laid out in an area of 170 $\mu m \times 1000$ μm[1], and fabricated in a standard 0.18 μm TSMC CMOS technology with six metal layers. The transmission lines' interconnects are implemented onto the metal 6 layer with a thickness of 1 μm. The die microphotograph of the fabricated chip is shown in Figure 4.7.

4.3 Measurement Results

The S-parameters of the amplifier are measured on wafer using GSG RF probes according to the guidelines presented in [55]. A 40 GHz Agilent Vector Network Analyzer with a probe station is used in the measurements. The network analyzer is calibrated up to 35 GHz using the standard open/short/load/through method. The DC bias voltages (1-V DC, 1.8-V DC) are supplied through the RF input and output probes using bias-T connectors. The S-parameter measurement results are shown in Figure 4.7. The measured gain (S_{21}) of the

[1]As the proposed DA was implemented as part of a multi-project fabrication with preassigned bonding pads, the lateral dimension of the chip was increased from 170 μm to 400 μm

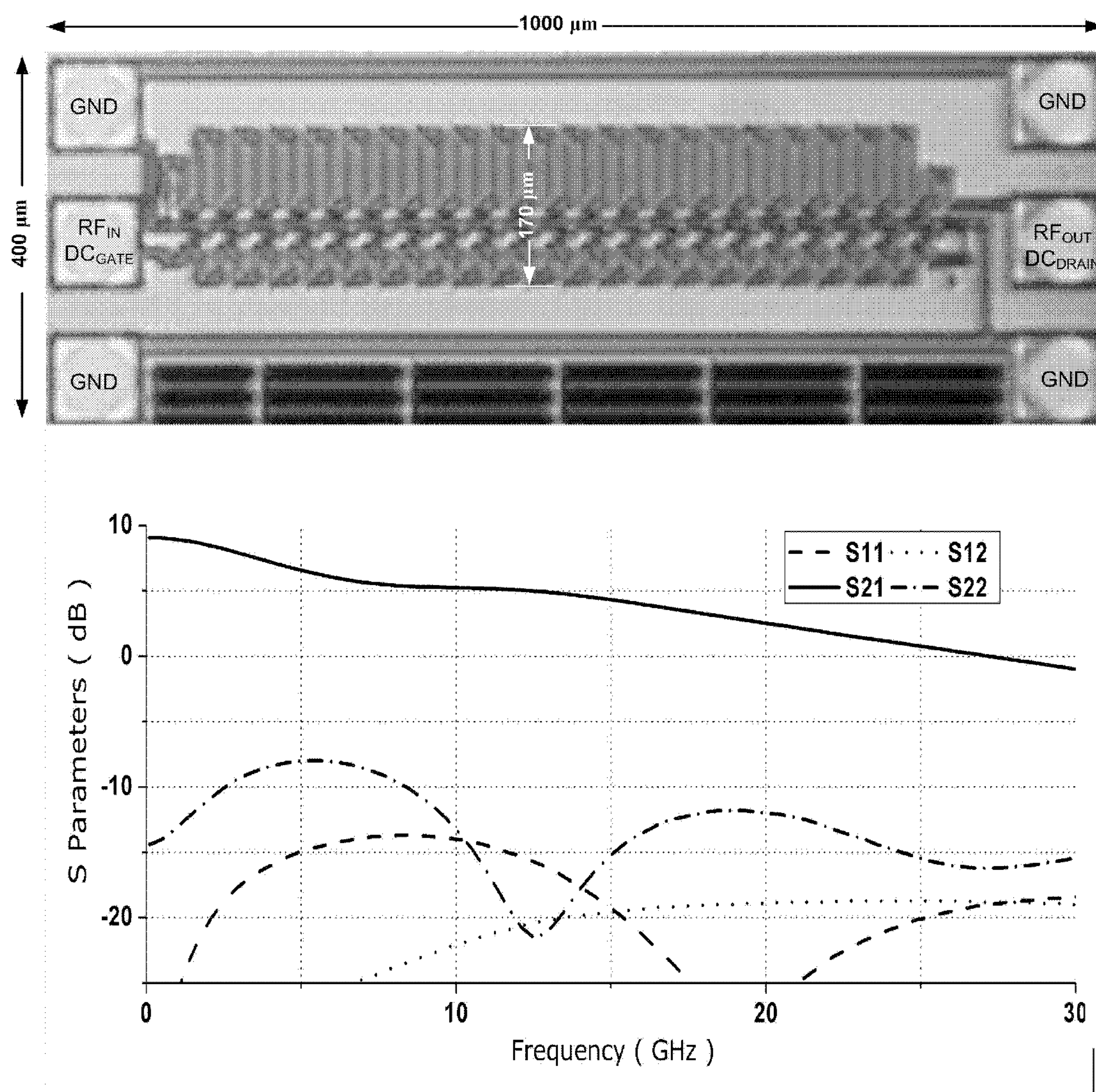


Figure 4.7: Die microphotograph of proposed twenty-stage CMOS DA, and S-parameters measurement results.

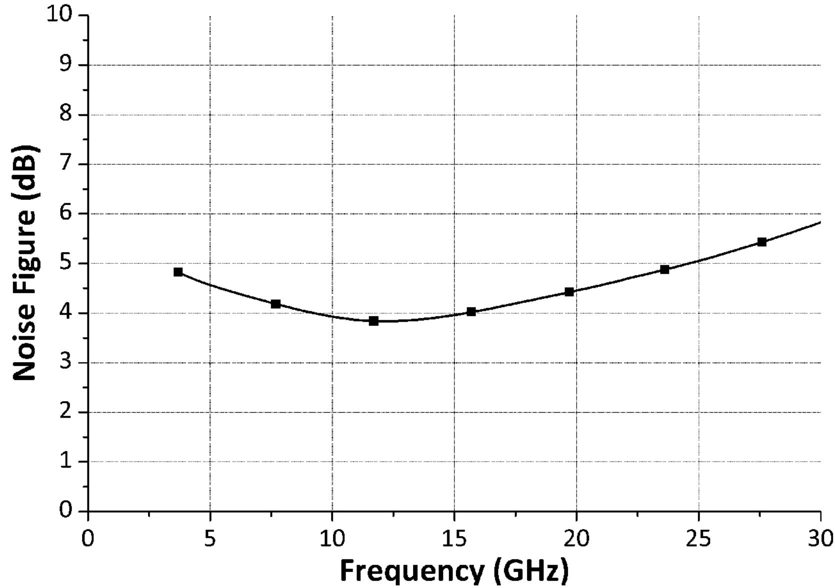


Figure 4.8: Measured noise figure of proposed twenty-stage CMOS DA.

amplifier is 9 dB, and the amplifier unity-gain bandwidth is 27 GHz. The measured values of S_{11}, S_{22} and S_{12} are limited to -12 dB, -8 dB and -18 dB within the DA's bandwidth, respectively.

We use a Noise Generator with a Noise Figure Meter for the measurement of the amplifier's noise figure. The NF Meter was calibrated with the noise source at the input of the cable connected to the output port probe. The NF Meter uses a Y-Factor method by having a pulsed power supply drive the noise source repeatedly as Hot/Cold, and then averages the results of 16 measurements. Figure 4.8 shows the measured noise figure of the DA averaging at 4.7 dB.

To evaluate the performance of the proposed DA, the bandwidth, gain, die area, and

calculated area efficiency of the previously published DAs and this work are summarized in Table 4.1 . The proposed DA has the smallest die area among the reported CMOS DAs. If we define the area of efficiency of a broadband amplifier as

$$\text{Area Efficiency} = \frac{\text{Gain} \times \text{Bandwidth}}{\text{Area}}, \tag{4.9}$$

the area efficiency of the proposed 0.18 mum CMOS DA is the best reported compared with the other area-efficient DAs even though they are implemented in 90 nm CMOS technology with significantly larger f_T than 0.18 mum CMOS technology. The DA consumes 20 mW and 65.8 mW from two 1-V and 1.4-V DC supplies.

Process / Ref.	BW (GHz)	G(dB)	A($mm \times mm$)	Area Efficiency ($GHz.dB/mm^2$)
0.8 μm[24]	4.7	5	0.32×0.72	102.0
0.6 μm[25]	5.5	6.5	0.8×1.4	31.9
0.6 μm[26]	8.5	5.5	1.3×2.2	16.3
0.18 μm[27]	23	5	0.3×1.5	255.5
0.18 μm[28]	18	8	1.3×1.8	61.5
0.18 μm[29]	16	7.3	0.9×1.5	86.5
0.18 μm[30]	27	6	0.9×1.8	100
0.18 μm[31]	39	4	1.1×3.0	47
0.18 μm[32]	28	9	0.48×0.75	700
0.18 μm[33]	24	7.3	0.9×1.5	129.8
0.18 μm[34]	> 12.6	7.6	0.6×1.1	>145.1
0.18 μm[35]	36	9.5	0.86×0.94	423.1
0.09 μm[36]	80	7	0.8×0.9	777.8
0.09 μm[37]	95	7.4	0.6×1.2	976.4
0.18 μm This Work	27	9	0.17×1.0	1429.4

Table 4.1: Area Efficiency of Reported Performance of CMOS Distributed Amplifiers.

Chapter 5

Loss-Compensated DA Design

Implementation of high-quality on-chip inductors still remains the greatest challenge of RF circuit design. As the on-chip transmission lines required for the operation of DAs reside above a silicon substrate with a relatively low resistivity, a significant amount of power is lost in the form of heat in the substrate. These losses degrade the DA's gain and input and output matching particularly as frequency increases beyond 10 GHz. In many recent works on CMOS DAs, a sloping gain versus frequency is reported. Shigematsu et. al. in [31] presents an RC degenerated common source gain cell to provide a flat gain within the amplifier's bandwidth. Although this method proves successful in flattening the gain, the proposed source degenerated transistor reduces the gain by a factor of $1 + g_m Z_{Source}$, resulting in a small gain of 4 dB for the DA. In this chapter, we investigate use of negative resistors to compensate for the loss of on-chip transmission lines. As the proposed loss compensation technique is not in direct trade-off with the amplifier's gain, it will result in a noticeable gain improvement compared with the work in [31].

5.1 Lossy On-Chip Inductor

Because of the low quality factor of the CMOS on-chip inductors, the DA's transmission lines attenuate the signal as it travels through from the input to the output. The loss of the on-chip inductor increases with frequency, reducing the gain of the amplifier as the frequency increases. Several works have been reported on the enhancement of the quality factor of the on-chip inductors. Yue et. al. suggests a patterned polysilicon ground shield underneath the spiral inductor [56] to decouple the inductor from the substrate. Others use a metal ground shield to prevent the elephantine waves from entering the substrate. Although using a ground shield can improve the quality factor, it can affect other on-chip inductors' characteristics significantly [57]. For example, a metal shield introduces a capacitive coupling between the spiral inductor and the metal shield which in turn lowers the resonance frequency of the inductor. In addition, the value of the inductor is also decreased because of the coupling of the inductors' segments through the metal shield. Another technique is to etch out the substrate underneath of the spiral by micromachining [58]. This technique does not affect other inductors' S-parameters adversely. Despite improving the quality factor of the on-chip inductors, these techniques can not fully eliminate their losses.

Besides the discussed manufacturing techniques, some researchers have used regenerative circuitry to compensate for the loss of on-chip inductors. Negative resistors are extensively used to improve the quality factor of inductors particulary in the design of voltage-controlled oscillators [59, 60]. The advantage of these circuit techniques is that they are capable of fully compensating for the on-chip losses. Of course, one of the draw-

backs is a higher power compensation for driving the loss compensation circuitry.

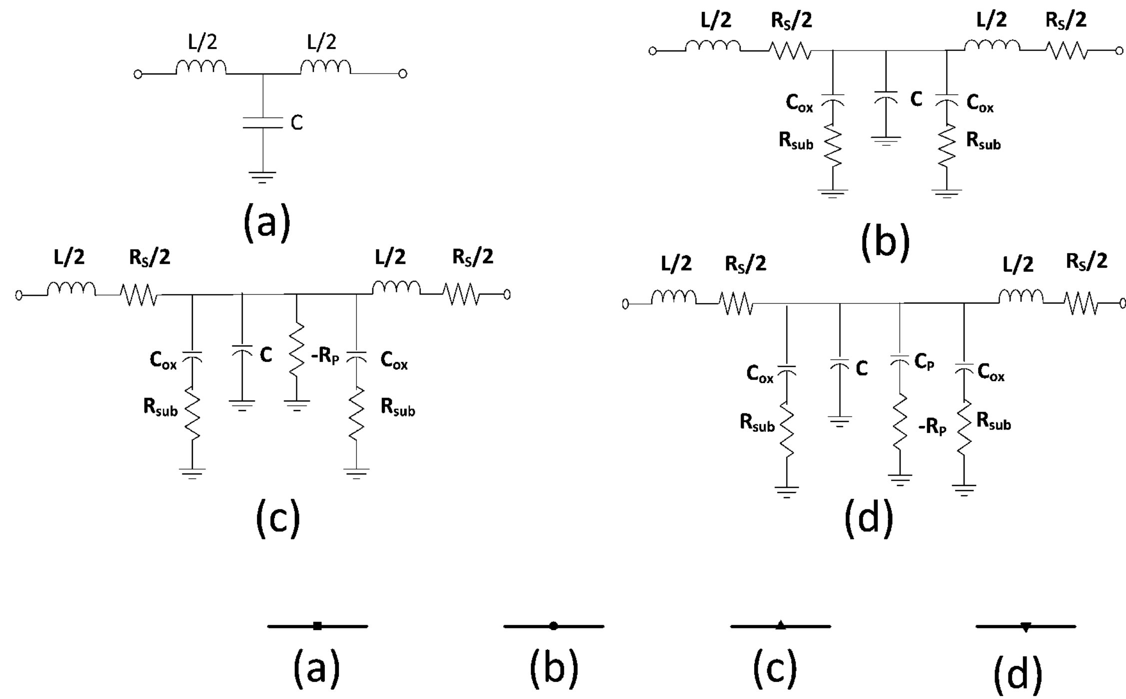
5.2 Analysis of Lossless/Lossy/Loss-Compensated Transmission lines

This section presents a step-by-step approach to arriving at the proposed loss compensation technique. Figure 5.1(a) shows an ideal LC transmission line terminated in its characteristic impedance. Bringing into the picture the loss of the on-chip inductors, the transmission line is redrawn in Figure 5.1(b). Shunt negative resistors are incorporated in the circuit to compensate for the transmission line's loss, as portrayed in Figure 5.1(c). Note that for a lossless transmission line, the propagation constant is purely imaginary :

$$\gamma = \alpha + j\beta = j\sqrt{LC}, \tag{5.1}$$

Therefore, the attenuation constant (α) is zero as expected. To find the value of the negative resistance required to fully compensate for the attenuation of the transmission lines, we use basic transmission line theory to calculate the propagation constant of lossy transmission lines with attenuation compensation networks (-G) as follows:

$$\begin{aligned} \gamma = \alpha + j\beta &= \sqrt{(R + j\omega L)(-G + j\omega C + \frac{1}{R_{sub}})} \\ &= \sqrt{-(R(G - \frac{1}{R_{sub}}) + w^2 LC) + j\omega(R(G - \frac{1}{R_{sub}}) - LC)}. \end{aligned} \tag{5.2}$$



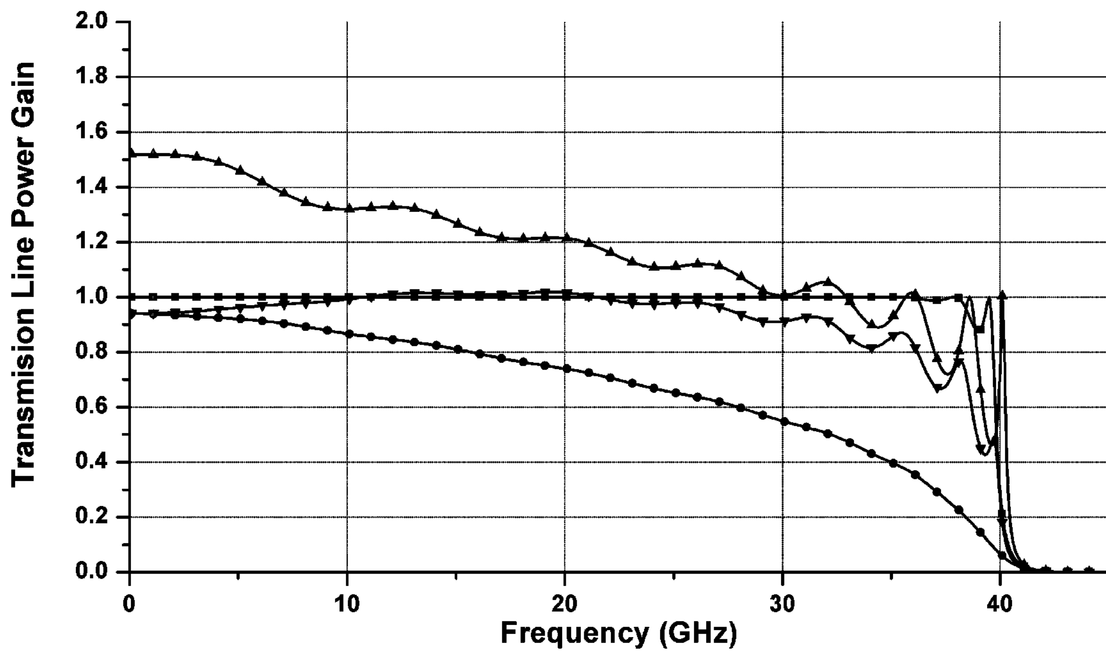


Figure 5.1: Schematic diagram and power gain of (a) lossless, (b) lossy, (c) loss-compensated, and (d) high-frequency loss-compensated transmission lines.

For simplicity, the coupling capacitor of the inductor and substrate is ignored in the negative resistor calculation. To make the attenuation constant of the compensated transmission line equal to zero, the propagation constant must be purely imaginary, requiring in turn that the imaginary term inside the square root in 5.2 be equal to zero. Therefore, the values of the negative shunt conductance can be obtained as

$$G = \frac{LC}{R} + \frac{1}{R_{sub}} \tag{5.3}$$

On the other hand, the characteristic impedance of the transmission line is also affected by the on-chip inductor losses and shunt negative conductance as follows:

$$Z = \sqrt{\frac{R + j\omega L}{-G + j\omega C + \frac{1}{R_{sub}}}} \tag{5.4}$$

For a fully compensated transmission line, the characteristic impedance can further be simplified to

$$Z = \sqrt{\frac{R + j\omega L}{-R + j\omega L}} \times \sqrt{\frac{L}{C}} \tag{5.5}$$

where $\sqrt{\frac{L}{C}}$ is the characteristic impedance of a lossless transmission line. At low frequencies, the characteristic impedance of the loss compensated transmission line is different from that of a lossless transmission line, leading to overshoot in the gain of the amplifier. Though at higher frequencies, the value of the characteristic impedances is approaching that of lossless line. In this study, we propose that the compensating negative resistor be isolated from the transmission line by a series capacitor as depicted in Figure 5.1(d).This configuration leads to the following improvements in the operation of the circuit:

- The negative resistance circuit does not affect the DC biasing of the circuit since it does not draw any DC current that passes through the transmission line components.

- The negative resistance circuit does not change the characteristic impedance of the transmission lines at lower frequencies, and, therefore, no gain variation at low frequencies will occur.

- The negative resistance is present only in the circuit at relatively higher frequencies when the effect of a series resistor on the gain of the DA is more evident and can be fully compensated.

All four circuits in Figure 5.1(a)-(d) are simulated. As plotted by a square-marked line in Figure 5.1, the power gain (S_{21}) of the lossless transmission line is flat (=1) over the entire bandwidth. As we incorporate the real on-chip inductor models, the gain of the transmission line decreases with frequency. As plotted in circular markers, the gain will reach to around zero at the vicinity of 40 GHz, implying that the total incident power is lost in the transmission line and is not reached to the output port. Adding a negative resistor with a value calculated in 5.3, the loss of the transmission line is fully compensated in the vicinity of 40 GHz. However as discussed before, the full compensation of loss around cutoff frequency results in over compensation in low frequency as shown by a up-triangle marked line. As suggested, a capacitor is placed in series with the negative resistor. The resultant gain, the down-triangle marked line, is relatively flat over the entire bandwidth, implying full loss compensation for the loss of the on-chip inductors over the transmission line's band.

After arriving at the proper circuit configuration for the transmission line's loss compensation, the next task is to implement the purposed negative circuit in CMOS technology. The next section discusses the possible implementation of negative resistors in

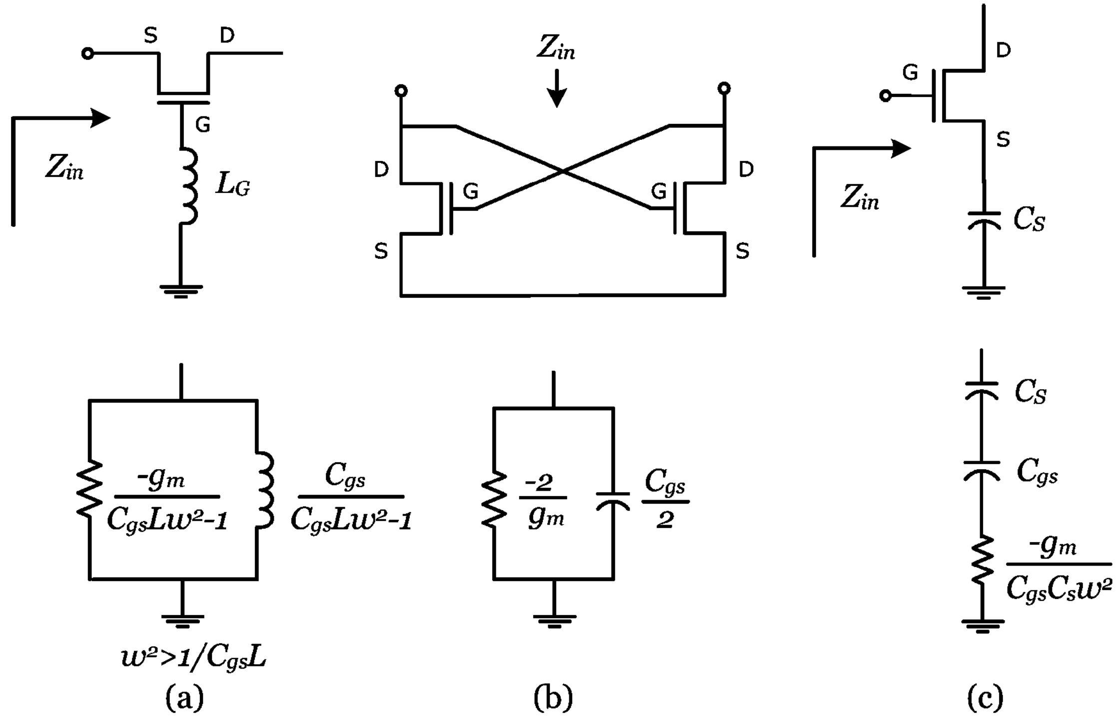


Figure 5.2: Negative Resistance Implementations

CMOS technology, and how to choose the most appropriate negative circuit topology for our application.

5.3 Negative Resistor Implementation

Negative resistors can be implemented using transistors and passive components in CMOS technology. Three negative resistor circuits and their equivalent small signal circuits are depicted in Figure 5.2. The negative resistance can be implemented using a capacitively source degenerated configuration, Figure 5.2(a). If the transistor model includes only

the transistor's transconductance (g_m) and the gate-source capacitor (C_{gs}), the equivalent circuit of a common gate transistor with an inductor in its gate is a frequency-dependent negative resistor in parallel to a frequency-dependent inductor, as shown in Figure 5.2(b). Although this circuit topology is employed for loss compensation of the transmission lines [61], it fails to provide isolation for the transmission line at lower frequencies. This circuit also occupies a larger die area than the two other negative resistor circuits because it incorporates an on-chip inductor. The second circuit, depicted in Figure 5.2(b), is a cross-coupled differential pair. The cross-coupled transistors produce a negative resistor of a value of -2/gm in parallel to a capacitor of $C_{gs}/2$. The cross-coupled negative resistor circuit is commonly used in circuits operating in differential mode. The cross-coupled differential pair is extensively used to improve the quality factor in differential LC-tank VCOs. The third negative resistor circuit is a capacitively source degenerated circuit. The input impedance seen from the gate of the transistor is equivalent to a negative resistor with a value of $g_m/(C_S C_{gs} \omega^2)$ in series with two series capacitors, C_{gs} and C_S [62]. The configuration is highly favorable to allow the shunt conductance of the negative resistor to increase with frequency because the resistor loss of on-chip inductors behaves similarly with respect to the frequency; therefore, the loss of on-chip inductors can be compensated for a wide frequency range. Among the three negative resistor circuits presented, the capacitively source degenerated amplifier provides the most favorable configuration needed for effective compensation of transmission line losses – this being a negative resistor in series with a capacitor. Since C_S blocks the DC current, it is necessary to parallel a resistor to this capacitor in order to provide the DC path required for biasing the common

source transistor. The value of the biasing resistor must be several times larger than the impedance of C_S, and small enough to provide the DC current needed for producing the required g_m for compensating the loss of transmission lines at those frequencies in which the negative circuits effectively compensate for the loss of on-chip inductors.

5.4 40 GHz CMOS DA Design

This section presents a summary of the design of a 40 GHz DA in 0.13 μm IBM's CMRF8SF CMOS process. CMRF8SF is a fully RF-characterized CMOS technology in which reliable RF models for active and passive components are provided, and accompanied by their equivalent chip layout. Therefore, the simulation results in this environment carry a significant accuracy in the GHz frequency range - unlike the simulation result in a digital CMOS process. To achieve a bandwidth of 40 GHz and a characteristic impedance of 50Ω simultaneously, the value of inductors and capacitors of the gate and drain transmission lines are computed as 398 pH and 159 fF, respectively. As discussed earlier, an m-derived network is required at both ends of the transmission lines to improve the matching at the vicinity of the cutoff-frequency. The sum of the parasitic capacitors of transistors and on-chip inductors and additional capacitors at each node of the transmission line should not exceed the calculated value of 159 fF. This condition limits the maximum achievable gain of the amplifier. In order to reduce the capacitive coupling, a cascode configuration is selected for the gain cells. Replacing the on-chip inductor models, the magnitude of the gain (S_{21}) of the DA is reduced as frequency increases, as shown in Figure 5.3 (dashed lines). To compensate for the reduction in the gain due to the loss of the on-chi inductors,

a capacitively source degenerated configuration is selected as explained in the previous section. The schematic diagram of the proposed DA's gain cells is drawn in Figure 5.4. An optimization process is employed to find the optimum value for achieving a maximally flat gain for the DA. The simulated loss-compensated S_{21} of the compensated DA is depicted in Figure 5.3 (solid lines). Both the gain flatness and phase linearity of the amplifier are significantly improved for the loss compensated network.

5.5 Implementation and Measurement Results

The proposed eight-stage CMOS DA chip is laid out in an area of 600 μm × 2500 μm as shown in Figure 5.5. For the models of the on-chip inductors to be valid, they are required to be placed at least 80 μm away from each other according to IBM's design manual [63][64]. To connect the inductors together, we need to use long interconnects. The parasitic inductance of these interconnects increase the series inductance of the transmission lines, alternating their characteristic impedance and bandwidth. To solve this problem, the outer diameter of the on-chip inductors is reduced from 100 μm to 90 μm to compensate for additional inductance produced by the interconnects.

There are four DC biases required for the operation of the DA, two provided through RF probes using T-bias connections, and two other DC biases using DC probes. The die microphotograph of the fabricated chip is shown in Figure 5.6.

The S-parameters of the amplifier are measured on wafer using GSG RF probes. A 110 GHz Anritsu Vector Network Analyzer with a Cascode probe station is used in the measurements. The network analyzer is calibrated up to 50 GHz using the standard

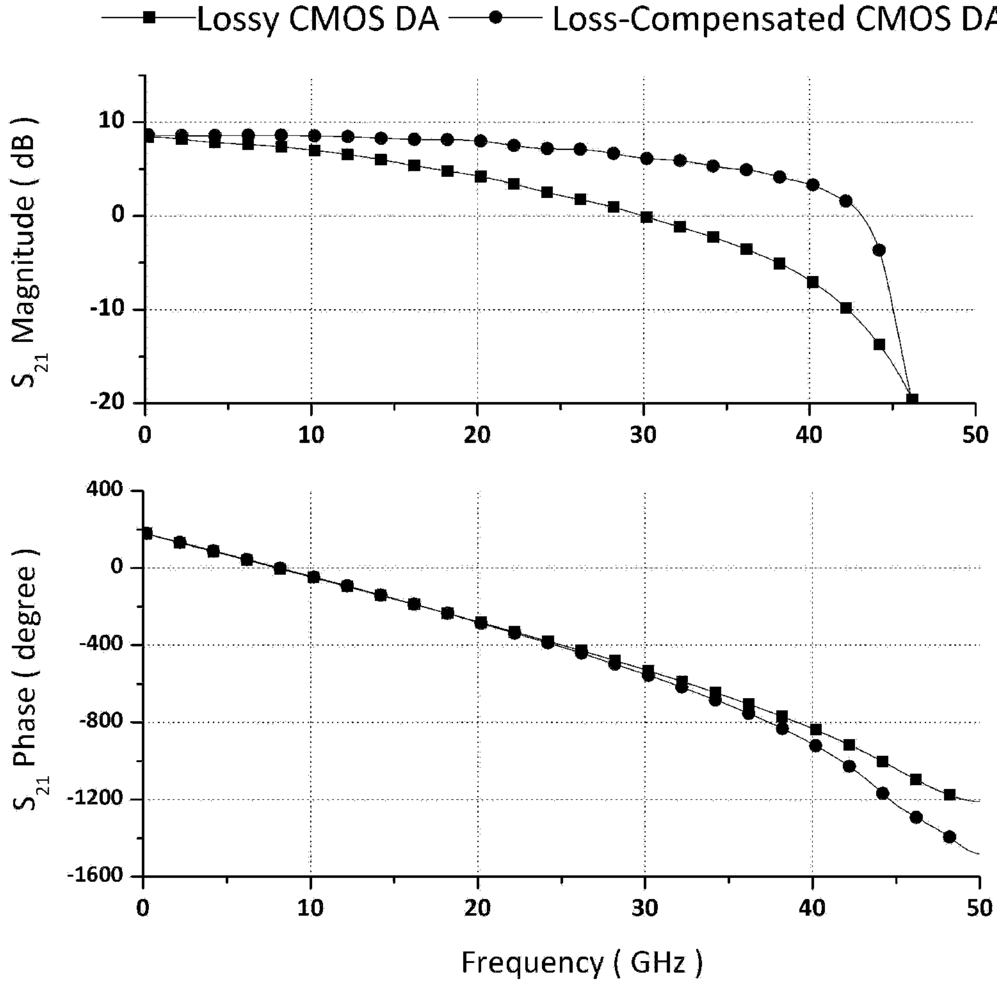


Figure 5.3: S-parameters simulation results for uncompensated and loss-compensated CMOS DAs.

open/short/load/through method. At full compensation, the power consumption is measured 44 mW and 59 mW for the DA and compensation circuitry, respectively. Figure 5.7 shows the DA's S-parameters measured using on-wafer probing. The DA exhibits an aver-

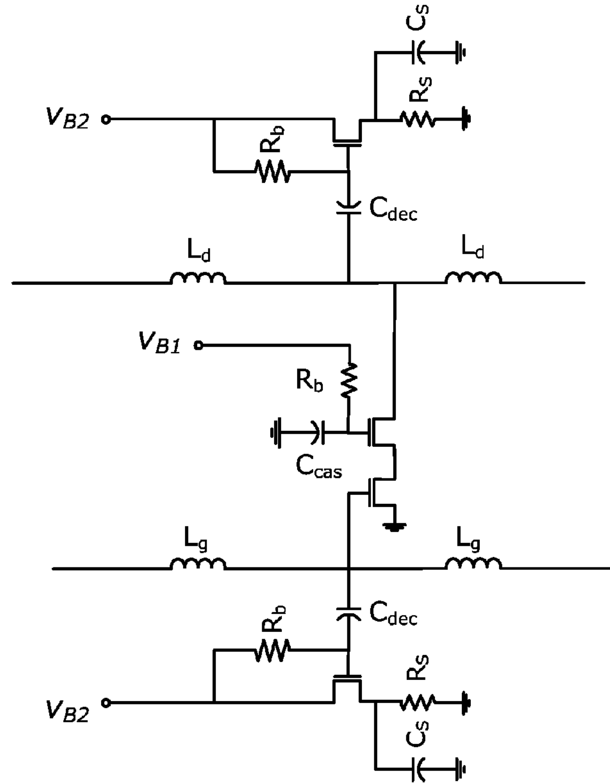


Figure 5.4: Schematic diagram of loss-compensated DA gain cell.

age gain of 9.8 dB with a gain variation from 8.6 dB to 10.6 dB. The 3-dB and unity-gain bandwidths of the DA are 43.9 GHz and 44.6 GHZ, respectively. The input and output return losses are better than -14 dB and -8 dB over the entire bandwidth, respectively. The reverse isolation is measured below -25 dB.

To measure the noise figure of the amplifier, a noise generator and noise meter are used as explained in Chapter 4. Figure 5.8 shows the measured noise figure of the DA averaging at 5 dB ranging from 2 dB to 7 dB. In addition to providing a large flat gain, the proposed amplifier exhibits a gain-bandwidth product comparable with those of the most recently

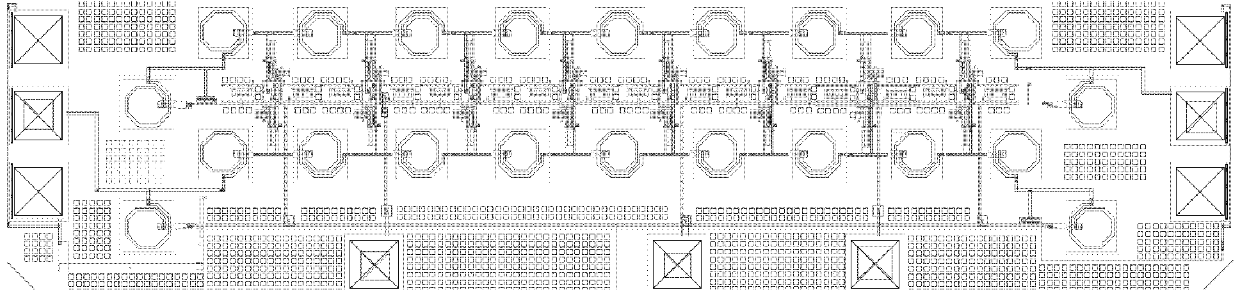


Figure 5.5: Chip layout of loss-compensated CMOS DA. .

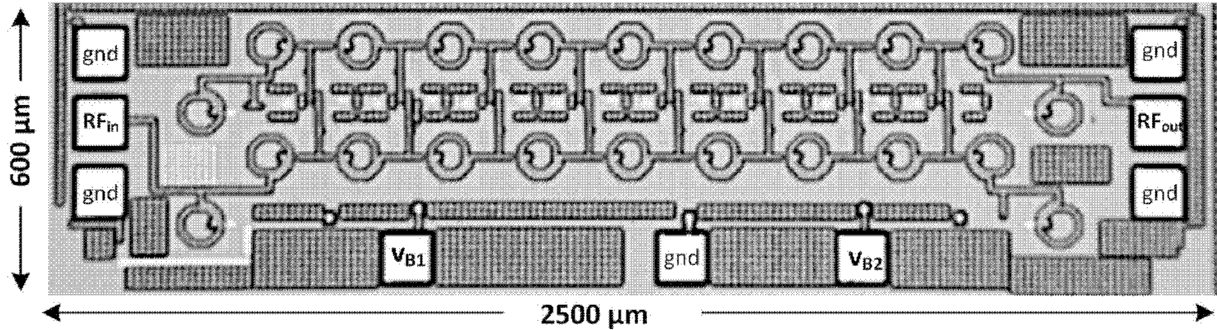


Figure 5.6: Die microphotograph of loss-compensated CMOS DA.

published CMOS DAs.

As the loss-compensated DA incorporate negative resistors, it is necessary to investigate the possibility of any instability in the operation of the circuit. As discussed earlier in Chapter 2, a circuit is unconditionally stable if

$$|\Gamma_{in}| = |\frac{Z_{in} - Z_0}{Z_{in} + Z_0}| < 1$$
$$|\Gamma_{out}| = |\frac{Z_{out} - Z_0}{Z_{out} + Z_0}| < 1 \tag{5.6}$$

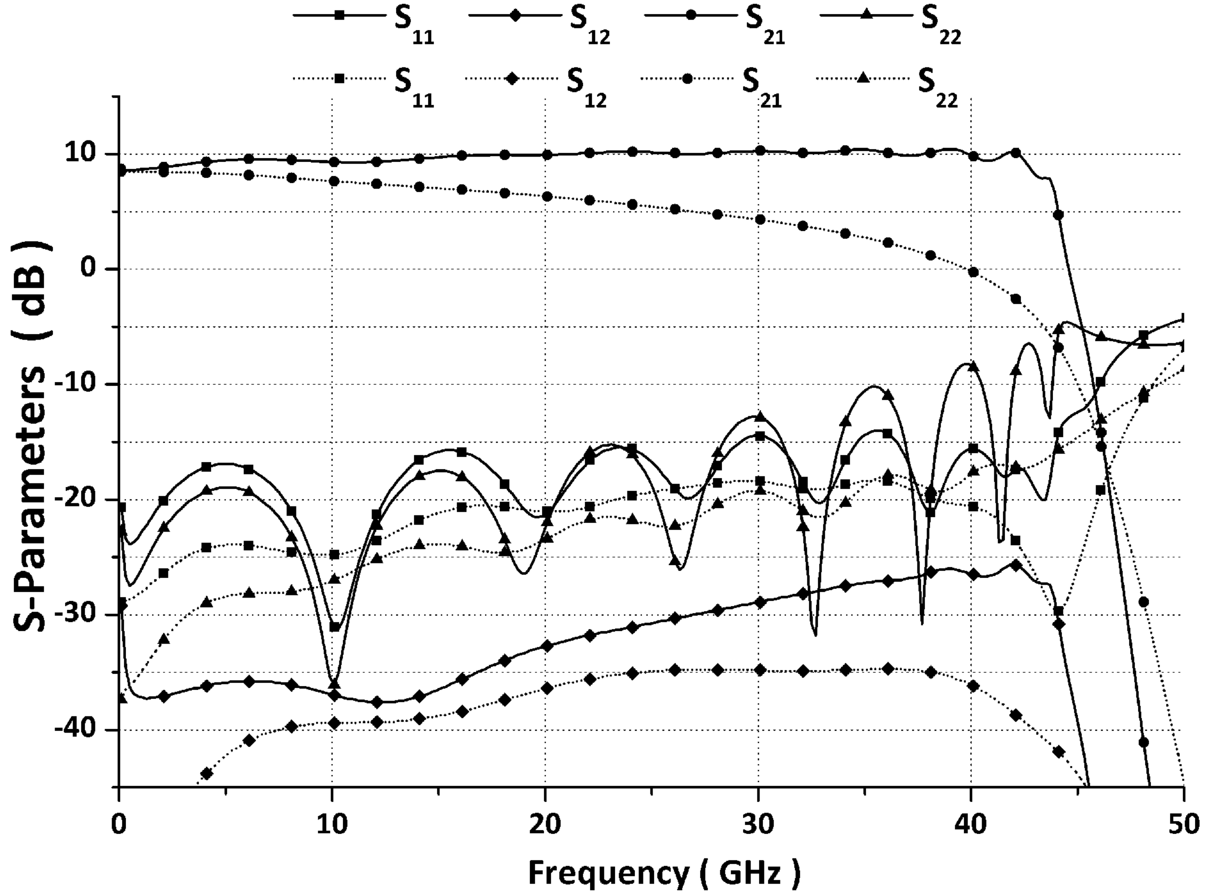


Figure 5.7: Measured S-parameters of lossy CMOS DA (dashed lines) and loss-compensated CMOS DA (solid lines).

where Γ_{in} and Γ_{out} are the reflection coefficients of the amplifier at the input and output ports, respectively, and Z_0 is the characteristics impedance of the transmission lines connected to input and output ports.

In 1962, John Rollett introduced a valuable measure of stability for an amplifier in [65],

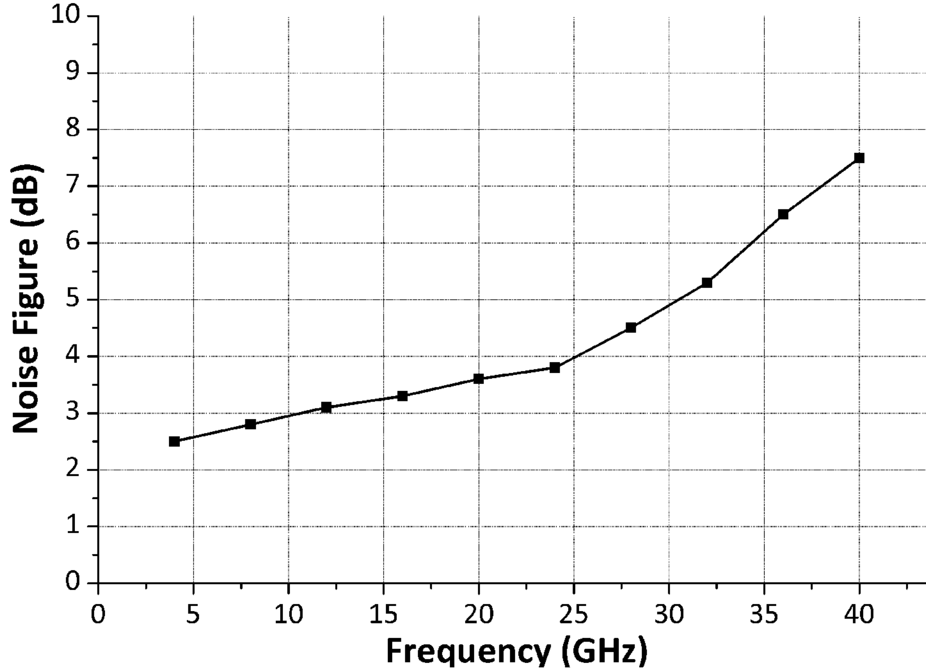


Figure 5.8: Measured noise figure of loss-compensated CMOS DA.

called K-factor, which can be easily computed from amplifier's S-parameters as follows:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{5.7}$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{5.8}$$

If K is less than 1, then the amplifier is potentially unstable. K-factor greater than one implies that the amplifier is unconditionally stable. Figure 5.9 depicts K-factor of the proposed amplifier computed based on S-parameter measurement results, proving that the

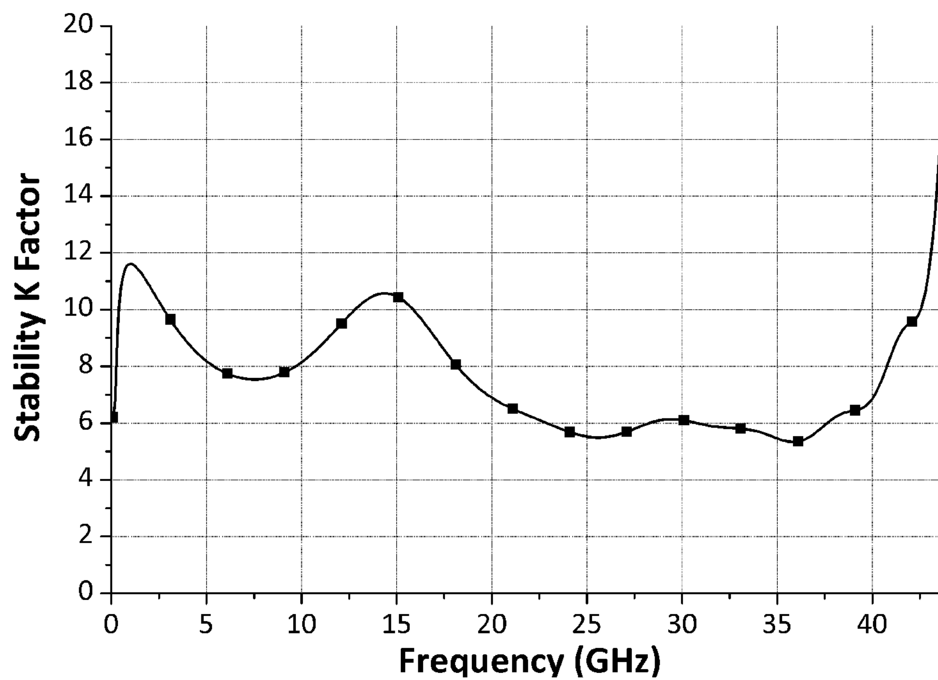


Figure 5.9: Stability K factor of loss-compensated CMOS DA.

amplifier is unconditionally stable over the entire frequency band and beyond.

Chapter 6

Low-Noise Broadband Amplifier Design

6.1 Low-Noise DA Design

This chapter focuses on implementation of the wideband LNAs in CMOS technology. Wideband LNA is the first front-end RF circuit after the antenna to increase the very limited power of the received UWB signal. A typical power gain larger than 10 dB and a very good noise performance is required, while the return loss of the amplifier must remain below -10 dB. In this work, two different circuit techniques are investigated for UWB applications: distributed amplifiers and inductively degenerated low-noise amplifiers (non-distributed).

One of the drawbacks of CMOS DAs is their relatively large noise figure because of thermal noise produced by resistive components of the gate transmission lines . To employ the distributed amplification technique for design of Ultra-Wideband broadband amplifiers,

the noise performance of distributed amplifiers needs to be improved. This chapter presents a novel low-noise technique that lowers the noise figure of the distributed amplifiers (DAs), making them suitable for UWB applications.

In the second part of the chapter, we try to extend the bandwidth of a narrowband inductively source-degenerated amplifier to make suitable for UWB application. The proposed circuit technique minimizes the circuit components at the gate of the amplifier, reducing the input-referred noise of the amplifier.

6.1.1 Noise Sources in CMOS DAs

There are three sources of noise in CMOS DAs:

Transistors

Transistors' noise sources, channel noise and gate induced noise, can be modeled as shunt current sources in the drain and gate of the transistor, respectively. The corresponding noise power densities are given by

$$\frac{\overline{i_d^2}}{\triangle f} = 4kT\gamma g_{d0} \tag{6.1}$$

$$\frac{\overline{i_g^2}}{\triangle f} = 4kT\sigma \frac{w^2 C_{gs}^2}{2g_{d0}} \tag{6.2}$$

where $\triangle f$ is the bandwidth in hertz, k is Boltzmann's constant in Joule/Kelvin, T is the temperature in Kelvin, γ is the bias dependent factor, g_{d0} is the zero-bias trains conductance of the transistor, and σ is the coefficient of the gate noise [52].

Terminating resistors

Both terminating resistors of the gate and drain transmission lines produce noise with power densities of $4KTR_d$ and $4KTR_g$, respectively. Although they produce the same noise powers assuming equal drain and gate characteristic impedances, the gate line terminating resistor contributes significantly more to the noise figure as amplifier gain increases because its noise is directly added to the input-referred noise.

On-Chip Transmission Lines (Inductors)

Because of limited quality of the on-chip transmission lines, the metal and substrate loss introduce additional noise in the circuit. Like the terminating resistors, the gate transmission line adds more to the amplifier's noise figure than the drain transmission line.

6.1.2 Proposed Low-Noise DA Technique

While the previous attempts for design of wideband LNAs [66, 67] were based on the bandwidth extension of the popular narrowband inductively source-degenerated amplifier [68], we propose an alternative design approach based on a modified distributed amplification method. Poor noise performance of the conventional DAs prevents the circuit topology to be used for UWB applications. There is no noise analysis for CMOS DAs in the literature. Because of analogy of noise expressions for MESFETs and MOSFETs, we can derive the noise figure expression of CMOS distributed amplifiers based on the expression derived for MESFET DAs in [69]. Assuming ideal transmission lines, the noise figure of an n-stage CMOS DA can be expressed as

$$F = \frac{S/N_{input}}{S/N_{output}} = 1 + (\frac{\sin n\beta}{n \sin \beta})^2 + \frac{4}{n^2 g_m^2 R_g R_d} + \frac{4\gamma g_{d0}}{n g_m^2 R_g} + \frac{R_g \omega^2 C_{gs}^2 \sigma g_{d0} \Sigma_{r=1}^{n} f(r,\beta)}{n^2 g_m^2}, \tag{6.3}$$

where $f(r, \beta)$ is the sum of vectors $(n - r + 1)e^{-j(n-r+1)\beta}$ and $\frac{\sin(r-1)\beta}{\sin\beta} e^{-j(n+1)\beta}$ and β is the phase constant of the transmission lines ($\beta_g = \beta_d = \beta$). The second, third, fourth, and fifth terms of the noise figure expression (6.3) represent the noise contribution of gate terminating resistor, drain termination resistor, transistors' channel noise, and transistor's gate induced noise, respectively . Large number of stages (n) will reduce the contribution of the gate resistor as $[(\sin n\beta)/(n \sin \beta)]^2$ can be neglected if β is not close to 0 or 180 degree. However, the area of the CMOS will increase proportionally with the number of stages. As in this work we choose the number of stage be 2 for the minimum die area, a significant contributor to the DA's noise figure is the terminating resistor of the gate transmission lines. Therefore, we focus on reducing the noise figure of the DA by minimizing the noise contribution of the gate transmission line terminating resistor. The available noise power from a terminating resistor is KTB when it is perfectly matched to the transmission line's characteristic impedance. As available noise power is independent of the resistor value, employing a non-uniform transmission line with a smaller terminating resistor will not result in an improved noise figure. In contrast, any mismatch between the real input impedance of the transmission line and the gate resistor simply reflects back some of the noise power to the resistor, improving the overall noise figure of the amplifier.

To improve the noise performance of the CMOS DAs, the terminating resistor of the

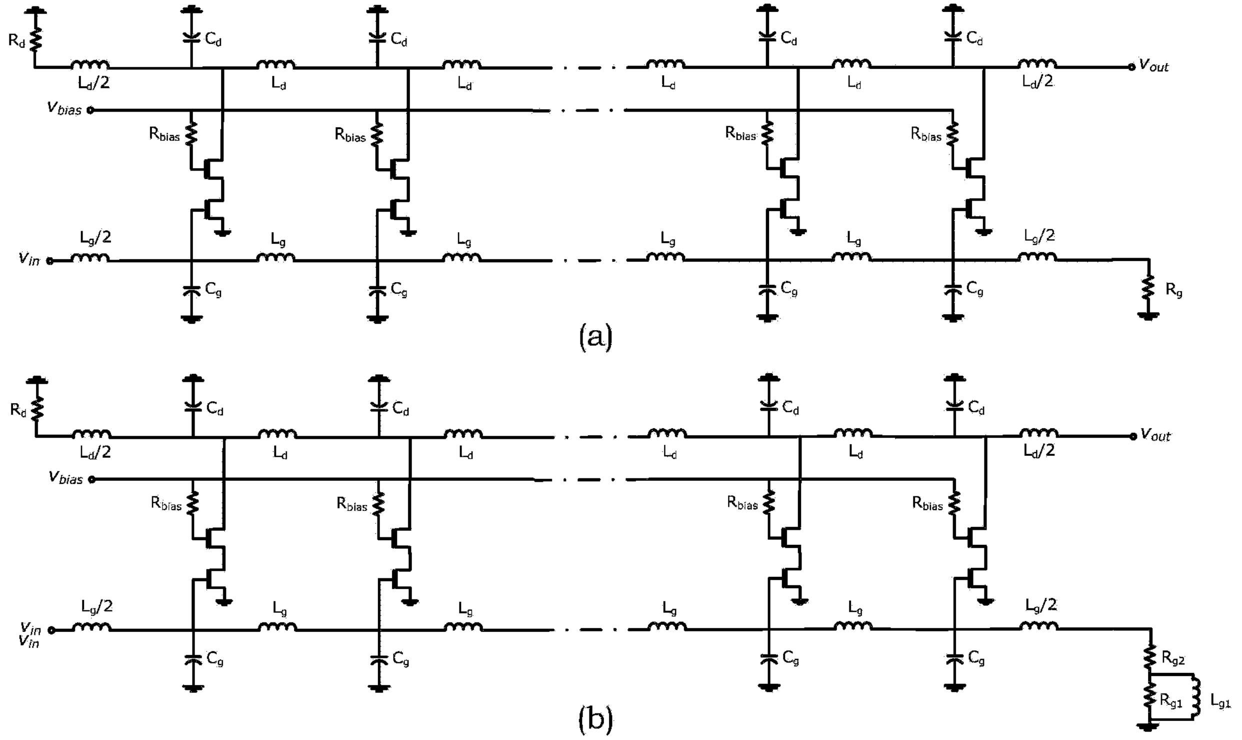


Figure 6.1: Low-noise DA.

gate lines is replaced by a frequency-dependent resistor, implemented by an RL ladder shown in Figure 6.1. The RL network is equivalent to a resistor less than 50 Ω (R_{g2}) at lower frequencies, and gradually reaches to 50 Ω in the vicinity of the upper cut-off frequency of the amplifier. The tradeoff between noise figure and input matching is illustrated in Figure 6.2. This terminating circuit produces less amounts of noise at low frequencies while adding an intentional mismatch, improving the average noise figure significantly. This improvement comes at the price of losing the perfect input matching at low frequencies, which can be tolerated as the UWB receiver does not operate at frequencies below 3 GHz.

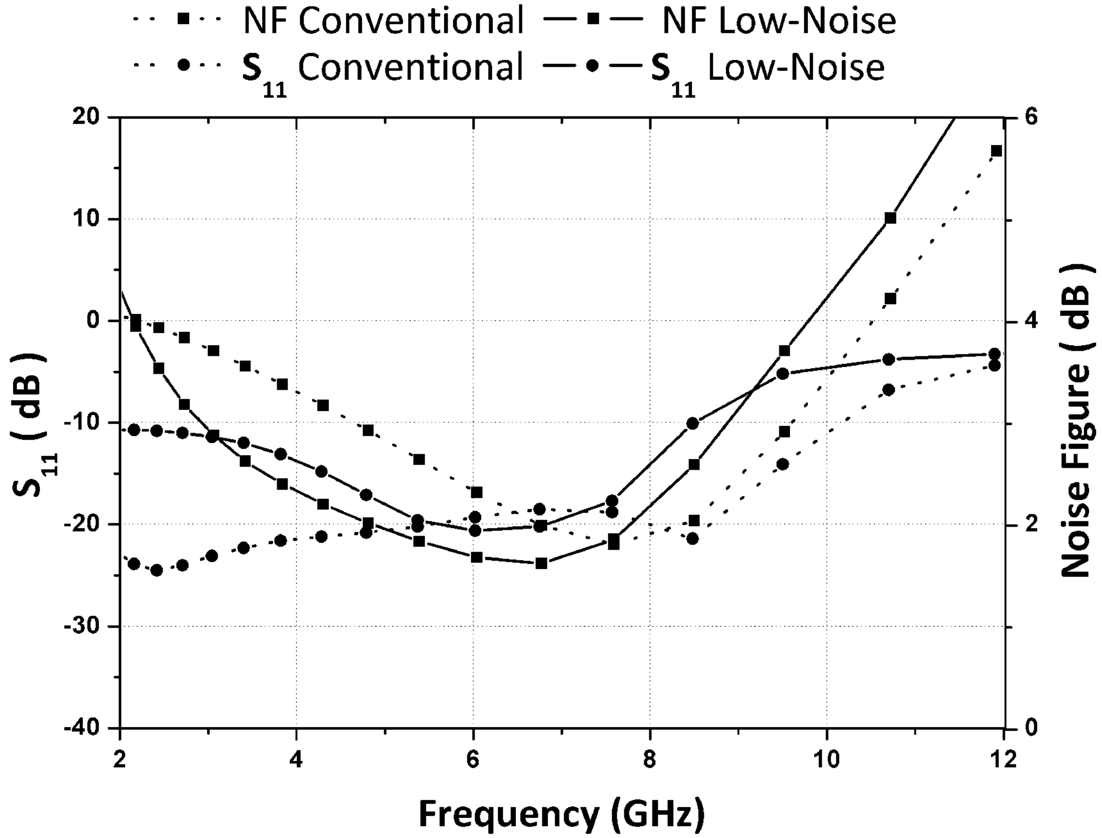


Figure 6.2: Noise figure versus input matching.

For frequencies above 3 GHz, we ensure that the input return loss remain below -10 dB.

6.1.3 Implementation and Measurement Results

The design of the proposed low-noise DA is carried out using a fully RF-characterized 0.13 μm CMOS kit. Spiral octagonal inductors are used for implementation of the gate and drain transmission lines. On-chip inductor models are closely correlated with their mea-

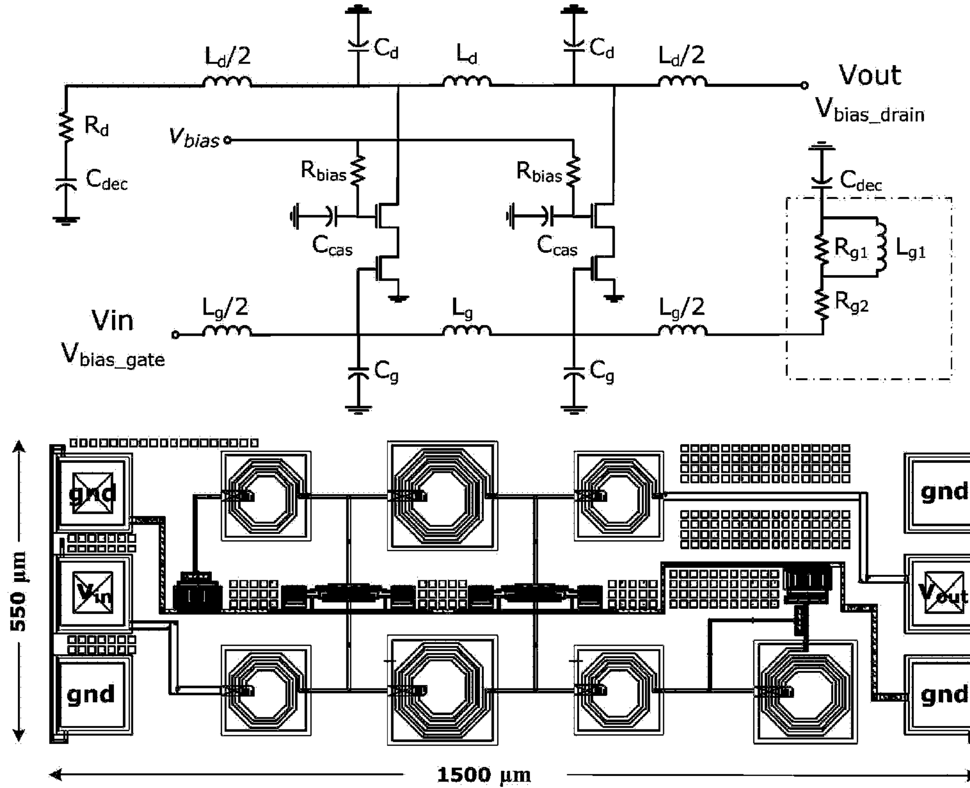


Figure 6.3: Schematic diagram and layout of Proposed Low-noise DA.

sured models to ensure enough accuracy in RF circuit simulation. We choose the number of stages to be minimum (N=2) in order to keep the chip area in a reasonable range, while still benefiting from the distributed amplification technique. A cascode configuration for the gain cells is selected to minimize the reverse coupling. Terminating resistors (networks) are placed in series with large decoupling capacitors to eliminate the unnecessary DC power dissipations in terminating networks. The size of the inductors is calculated to be 1.6 nH by satisfying bandwidth and characteristic impedance equations for a bandwidth of 10

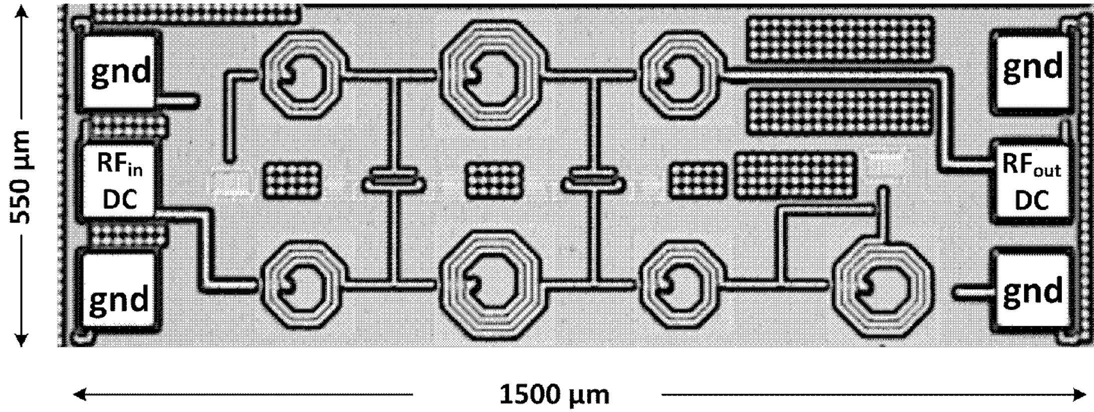


Figure 6.4: Die microphotograph of low-noise CMOS DA.

GHz, and input/output matching to a 50 Ω load. The maximum allowed transistor size is selected to achieve the maximum gain. Figure 6.3 shows the layout of the proposed low-noise CMOS DA and its simulated S-parameters.

Figure 6.4 shows the die microphotograph of the proposed low-noise DA. The total chip area is 0.55 mm by 1.5 mm. The amplifier performance is measured using on-wafer probing. A 110 GHz Anritsu Vector Network Analyzer (VNA) calibrated up to 13 GHz using the standard open/short/load/through method with a Cascode probe station is used in the measurements. Figure 6.5 shows the measured S-parameters of the CMOS DA. The devised amplifier exhibits a flat gain of 12 dB whereas the input and output return losses (S_{11} and S_{22}) remain below -10 dB over the UWB spectrum.

The linearity of the amplifier is measured using the embedded feature of the VNA. The power levels in VNA is calibrated with a power meter. Figure 6.7 depicts the measured 1-dB compression points are within the 3-10 GHz band.

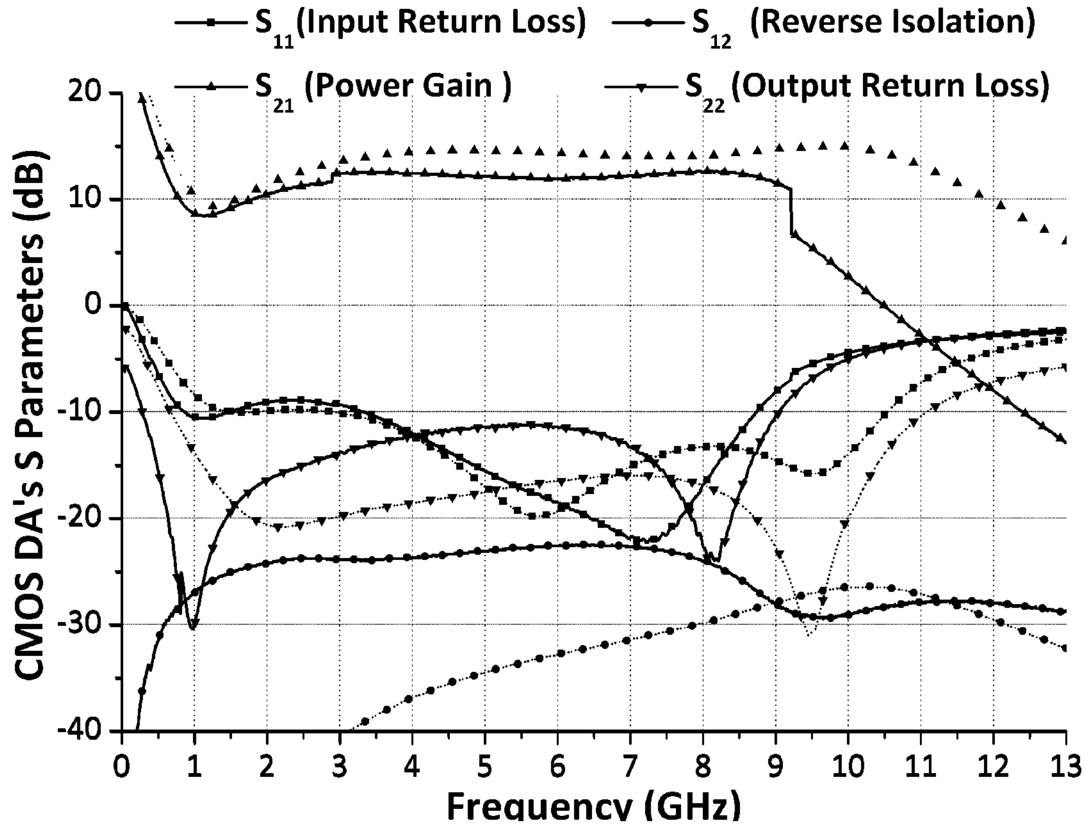


Figure 6.5: Measured (solid lines) and simulated (dotted lines) S-parameters of low-noise CMOS DA.

To measure the noise figure of the amplifier, a noise generator and noise meter are used as explained in Chapter 4.Figure 6.6 displays the measured noise figure of the DA as a function of frequency with an average of 3.4 dB over the 3-10 GHz band. The DA dissipates 30 mW from two DC power supplies of 0.6 and 1 V.

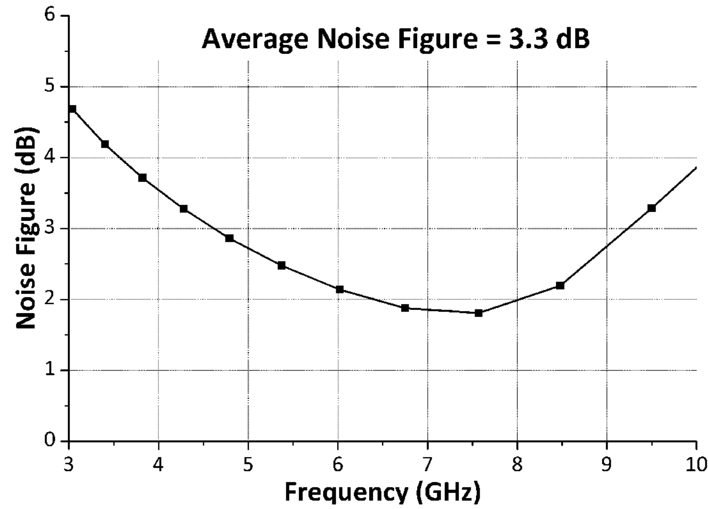


Figure 6.6: Measured noise figure of low-noise CMOS DA.

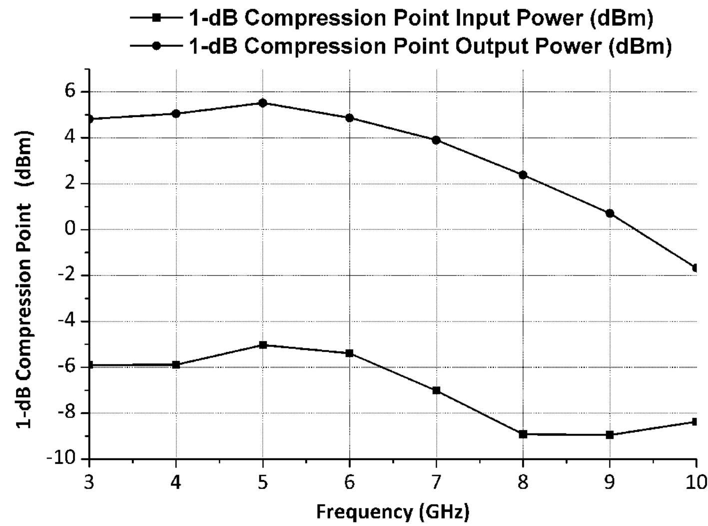


Figure 6.7: Measured 1-dB compression points of low-noise CMOS DA.

6.2 Non-Distributed Wideband LNA Design

Figure 6.8 shows the schematic diagram of a source degenerated LNA, and its equivalent input small-signal circuit. This circuit topology is primary invented for narrowband applications. The conventional LNAs employs an inductor (L_S) at the source of the NMOS transistor to achieve both low noise performance and pure resistive input matching at a single frequency [68]. Based on a simple transistor model (consisting of the transistor's transconductance g_m and gate-source capacitor C_{gs}), the input impedance of the LNA can be expressed as

$$Z_{in} = \frac{1}{j\omega C_{gs}} + j\omega L_s + g_m \frac{L_s}{C_{gs}} \tag{6.4}$$

When designing CMOS LNAs, the size of the transistor is usually optimized for the best noise performance, which subsequently determines the values of g_m and C_{gs} in 6.4. Choosing an appropriate value for L_S, the real part of the input impedance can be matched to the output impedance of the antenna, i.e. 50 Ω. The imaginary part of the input impedance is equal to zero at the resonance frequency of L_S and C_{gs}. Note that the input matching is significantly deteriorated as the frequency of the operation slides off the resonance frequency. Because the relatively small L_S ($< 1nH$ for deep submicron CMOS technology) resonates with C_{gs} at relatively high frequencies, another inductor (L_G) is usually connected to the gate to bring the resonance frequency down to the range where most narrowband wireless applications are positioned. To bring down the resonance frequency to less than 3 GHz, a relatively large gate inductor is needed (several nHs). Because of the low quality factor of the on-chip inductors, a large inductor is accompanied by a large series resistor that can significantly worsen the noise performance of the amplifier. Placing

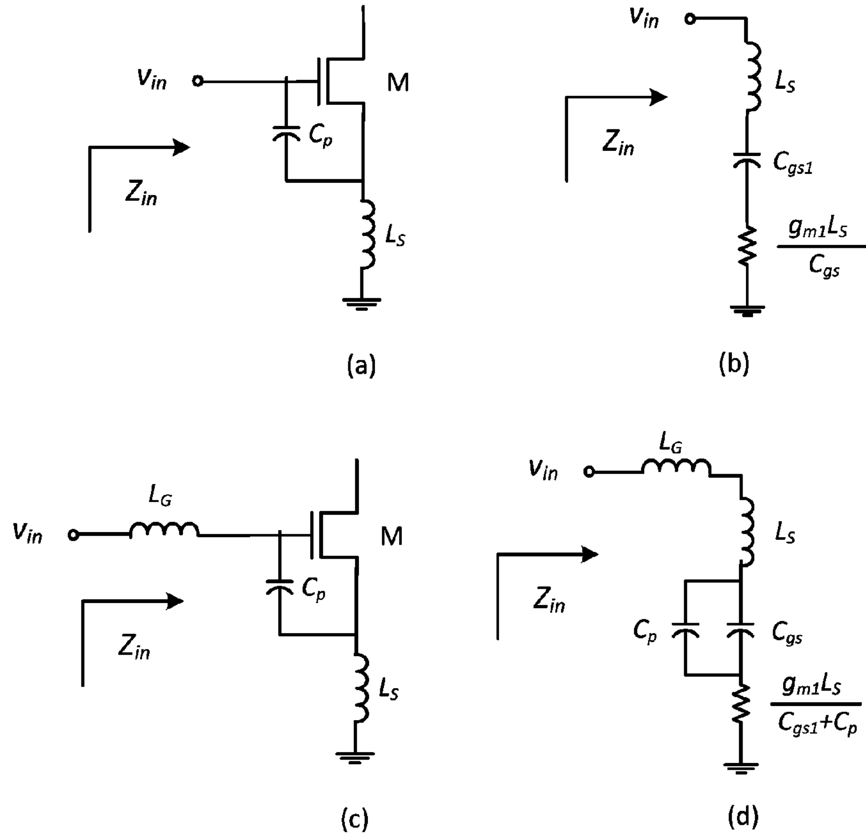


Figure 6.8: Schematic diagram of (a) inductively source degenerated amplifier,(b) its equivalent small-signal input circuit, (c) inductively source degenerated amplifier with additional circuit elements, and (d) its equivalent small-signal input circuit.

an additional capacitor C_P in parallel to transistor C_{gs} will decrease the gate inductance needed for the same resonance frequency. After the addition of these components, equation 6.4 can be rewritten as follows:

$$Z_{in} = \frac{1}{j\omega(C_{gs} + C_P)} + j\omega(L_s + L_G) + g_m \frac{L_s}{C_{gs} + C_p} \tag{6.5}$$

In the next section, we propose a modification to this circuit to broaden its operation band.

6.2.1 Ultra-Wideband LNA Design

A few new LNA designs are reported in the literature for Ultra Wideband applications [70, 67, 66]. The first work uses a resistive feedback to achieve a broadband input matching and a flat gain for the LNA. The second and third works use an LC ladder to broaden the performance of the source-generated LNA. Both of these methods comprise the noise performance of the LNA to achieve a broadband input matching. The first method uses a resistive feedback that introduces extra noise in the circuit, while the second method adds several low-quality factor on-chip inductors at the gate of the transistor. The input impedance calculation for a narrowband LNA in the previous section was based on a simple transistor (g_m and C_{gs}) model, which no longer holds accurate for the large transistors optimized for the minimum noise figure. Therefore, bringing into account the effect of gate-drain capacitance (C_{gd}) to calculate the input impedance of the amplifier is necessary.

6.2.2 Effect of Gate-Drain Capacitance

Considering the effect of C_{gd}, a parallel path is added to the input circuit as depicted in Figure 6.9. This path includes the C_{gd} in series with the impedance seen from the source terminal of the cascode transistor. If the gate-drain resistor of the cascode transistor is ignored, this impedance is equal to the parallel of C_{gs} and $1/g_m$. Since the symbolic analysis of the circuit results in a very complicated expression for the input impedance,

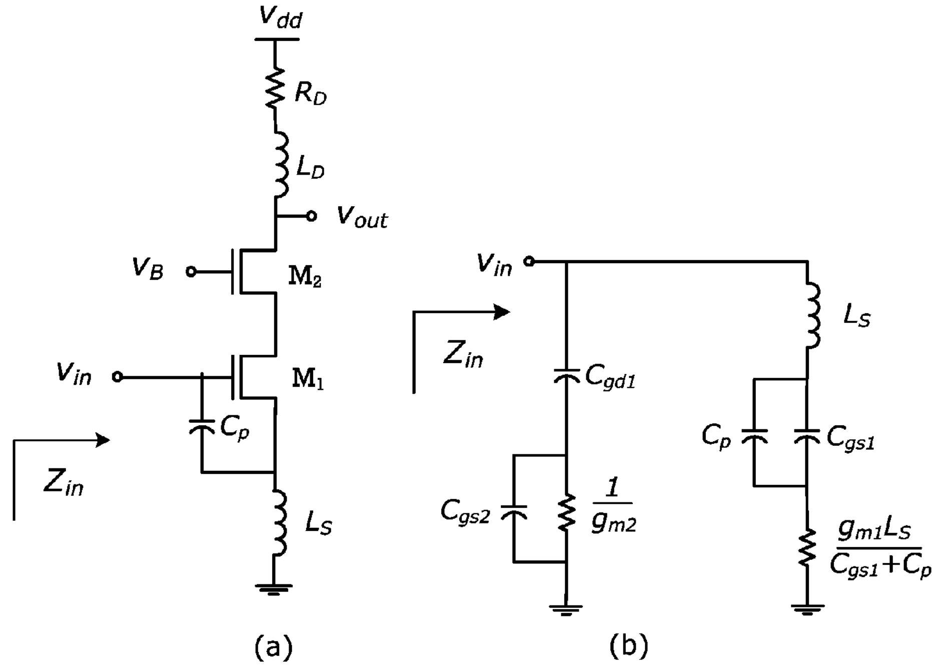


Figure 6.9: Effect of C_{gd} on input impedance.

the circuit is extensively simulated to evaluate the effect of each parameter on the input impedance. Figures 6.10, 6.11, 6.12, and 6.13 depict the real and imaginary part of the input impedances as functions of L_S, C_P, WM_1, and WM_2, respectively, while in each simulation other parameters shown in Table 6.1 are kept constant . In each simulation, one circuit parameter is swept in the desired range while all other parameters are kept constant. Simulation results in Figure 6.11 indicate that the real part of the input impedance does not stay constant with the frequency for small values of C_P. This implies that matching the real part of the input impedance to a 50 Ω resistor over a broad frequency range requires a large parallel capacitor (C_P). For large parallel capacitors, the imaginary part of the

input impedance follows a specific pattern with respect to frequency: in the first phase, the imaginary part decreases in absolute values in reverse with frequency, where the two capacitors $C_P + C_{gs}$ determine the behavior of the input network. The second phase starts with an increase in the absolute value of the imaginary part and ends with a decline in the absolute values. In this phase, the gate-drain capacitor (C_{gd}) of the transistor plays an important role. In the third phase, the imaginary part of the input starts to increase (sign value), and approaches the electrical behavior of the inductor L_S after changing the polarity. This three-phase behavior of the imaginary part is also evident in other parametric simulations (Figures 6.10 to 6.13). As demonstrated in Figure 6.11, for a particular value of C_P, there is a transistor size that provides the minimum variation of the real part of the input impedance with respect to frequency. The value of L_S determines the low-frequency response of the input impedance as shown in Figure 6.10. For a fully input matched design, the value of L_S is set such that a real impedance of 50 Ω is achieved. Figure 6.13 illustrates the variations in input impedance as a function of cascode transistor size. Obviously for larger cascode transistors, the effect of C_{gd} becomes more evident as the impedance seen at the source of the cascode transistor decreases.

6.2.3 Proposed Input Matching Technique

To exploit the three-phase behavior of the imaginary part of the input impedance, a fully matched LNA can be designed by adding a relatively small inductor to the transistor gate. As the gate inductor (L_G) is placed in series with the input impedance of the LNA, the imaginary part of the input impedance in the second phase is leveled at an absolute value

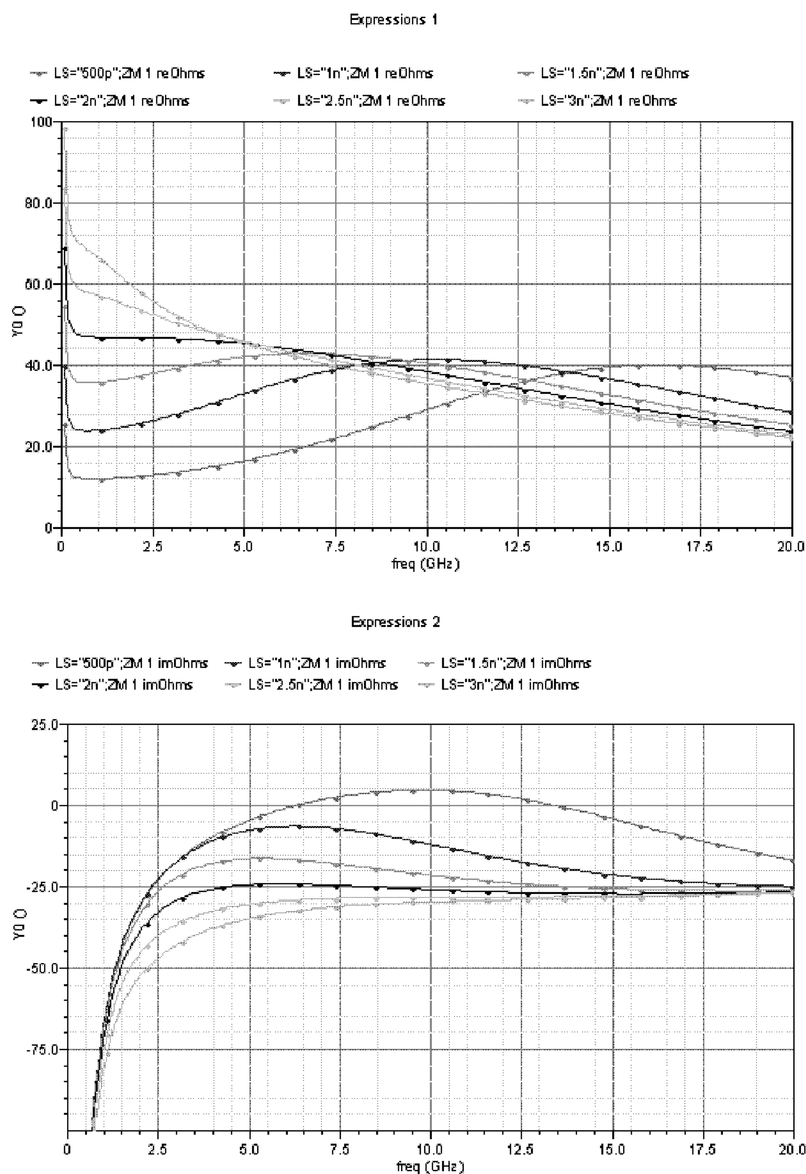


Figure 6.10: Input impedance of LNA as a function of LS.

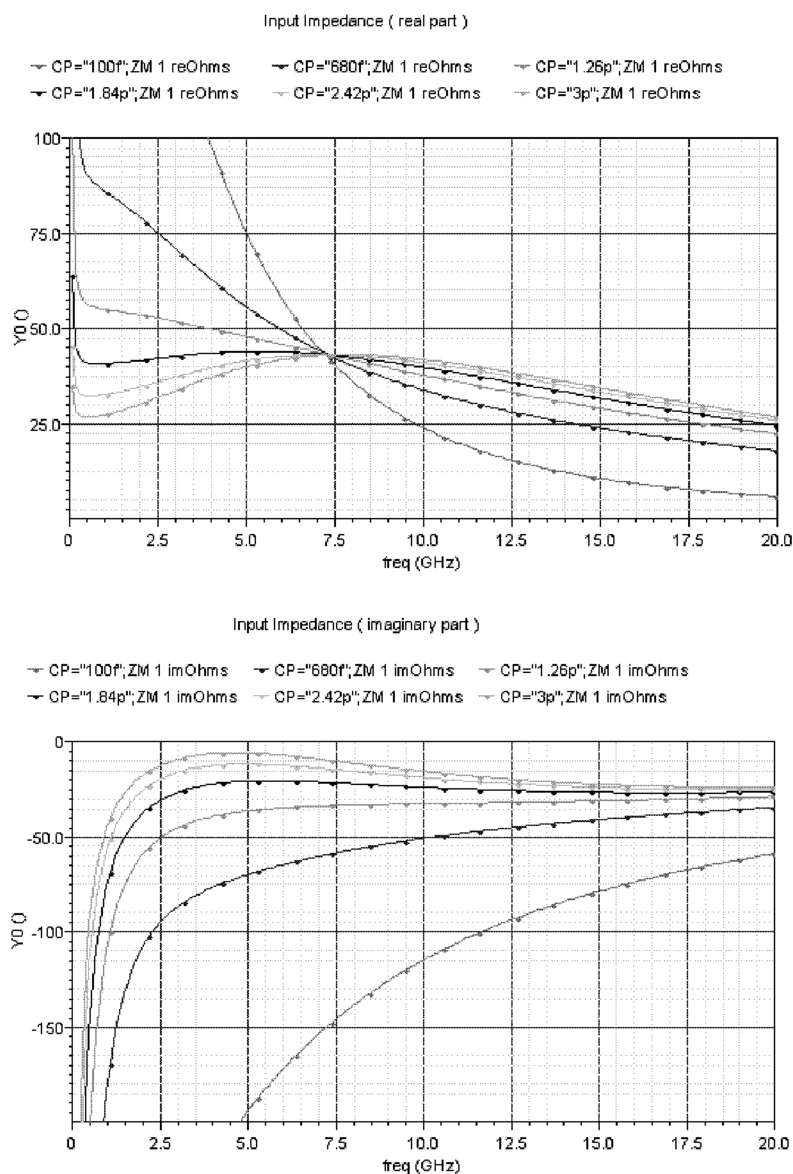


Figure 6.11: Input impedance of LNA as a function of CP.

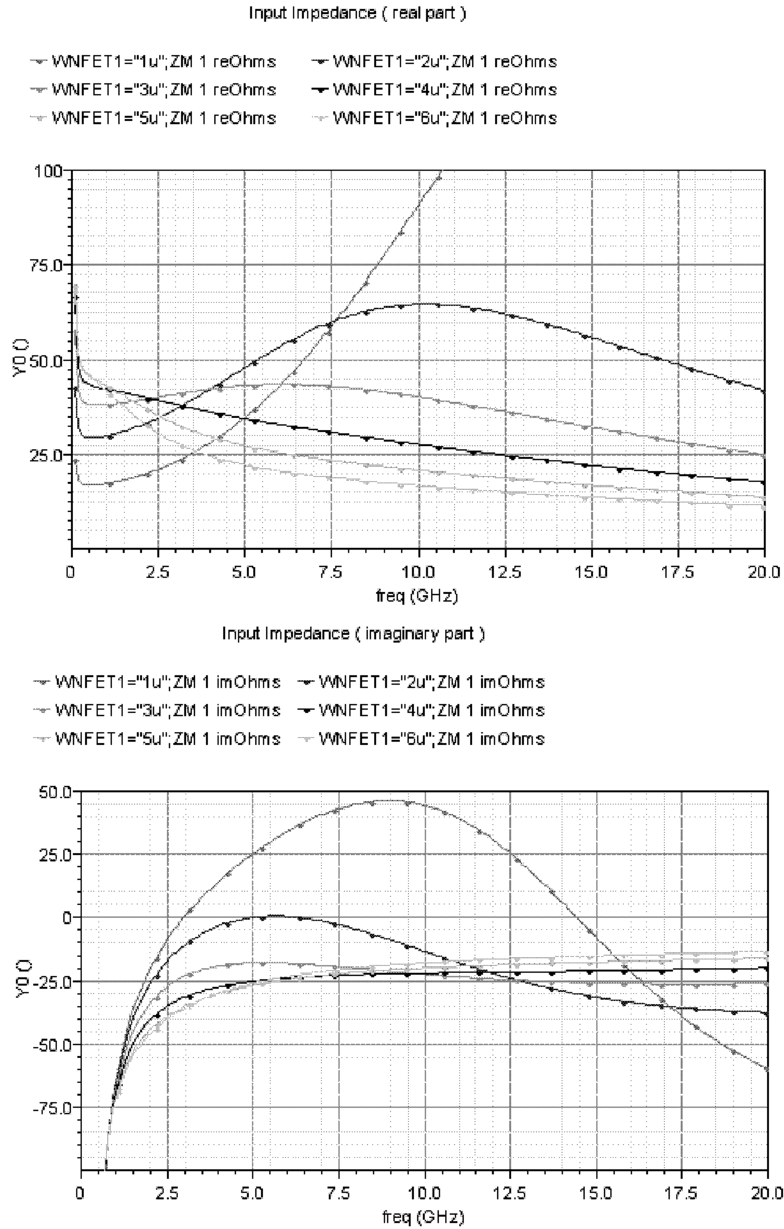


Figure 6.12: Input impedance of LNA as a function of M1 width (WNFET1).

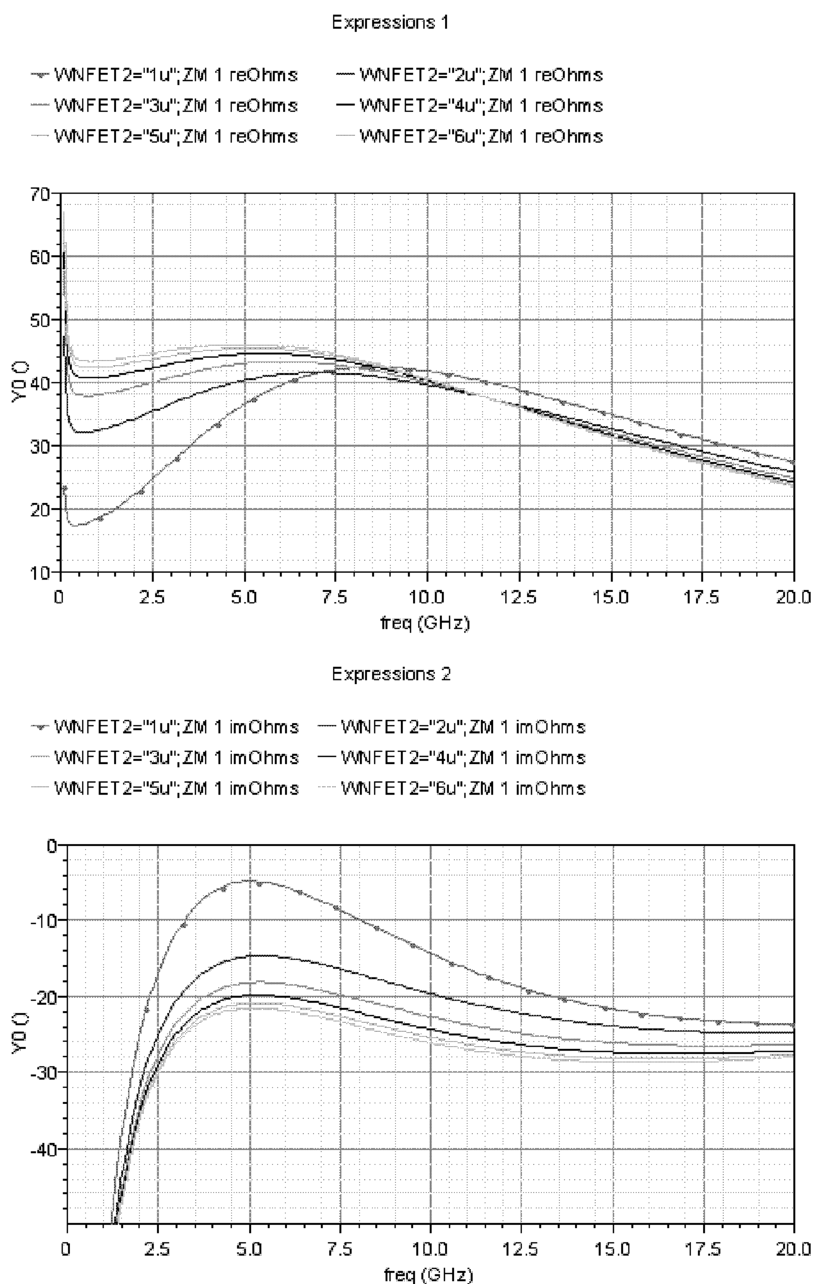


Figure 6.13: Input impedance of LNA as a function of M2 width (WNFET2).

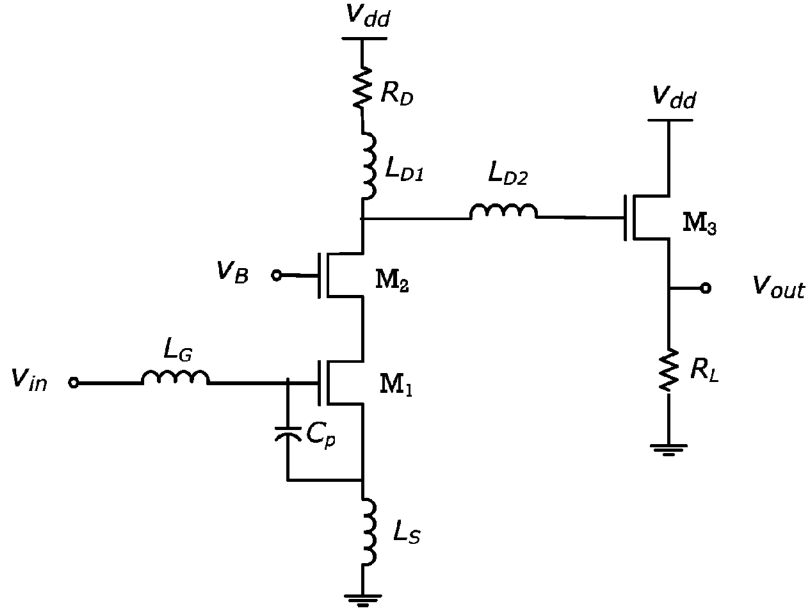


Figure 6.14: Complete schematic diagram of LNA excluding biasing circuitry.

close to zero. For a proper LNA design, an input impedance with a relatively constant real part and close-to-zero imaginary part over a broad frequency band is needed. This inductor is different from the gate inductor for narrowband design, which is devised to lower the resonance frequency. Because the proposed broadband matching can be achieved using a small size inductor (usually less than 500 pH), the noise performance of the LNA is not adversely affected.

6.2.4 Flat Gain

An inductive peaking technique [14] is usually employed in narrowband designs to compensate for LNA gain decline because of the source inductor. It is implemented by placing an

L_S	L_{D1}	L_{D2}	R_D	W_{M1}	W_{M2}	W_{M3}	C_P
1.6 nH	3 nH	3nH	100 Ω	150 μm	150 μm	50 μm	2 pF

Table 6.1: Optimized values of the proposed low-noise amplifier circuit components.

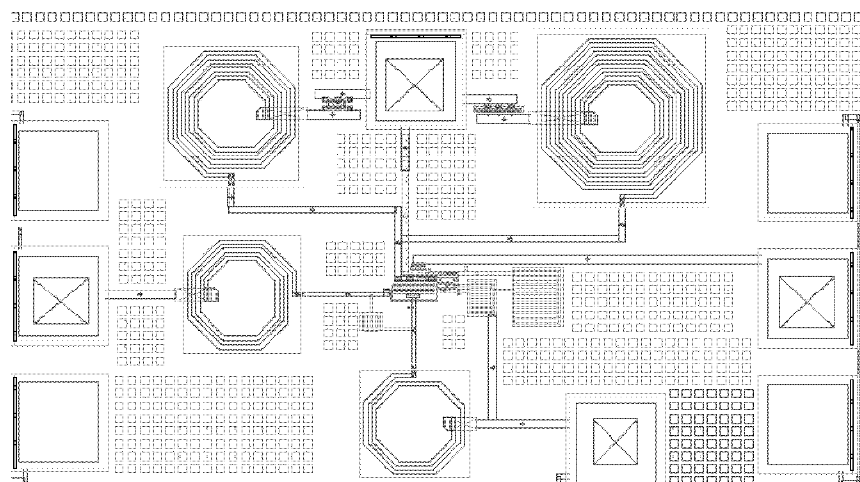


Figure 6.15: Wideband LNA.

inductor in series (L_D) with the drain resistor. This technique is not effective in this design, as a relatively large parallel capacitor ($C_P = 2pF$) is used. To achieve a flat gain over the 3-to-10 GHz band, a shunt inductance in addition to the series inductance is used [52]. A similar circuit based on a triple resonance technique also reported in [23] for broadband amplifiers in optical communications systems. The complete LNA circuit is illustrated in Figure 6.14. The LNA is simulated in a fully RF-characterized 0.13 μm CMOS technology. Optimized design parameters are listed in Table 6.1. S-parameter simulation results are demonstrated in Figure 6.16. The maximum input and output return loss is 14 dB and 10 dB within a 3-to-10 GHz band, respectively. The average power gain of the LNA is 8 dB, while the reverse coupling is less than -40 dB in the band. The minimum noise figure is 4 dB, yet averaged at 5 dB for the entire band as depicted in Fig 6.17. Figure 6.15 shows the layout of the proposed wideband LNA.

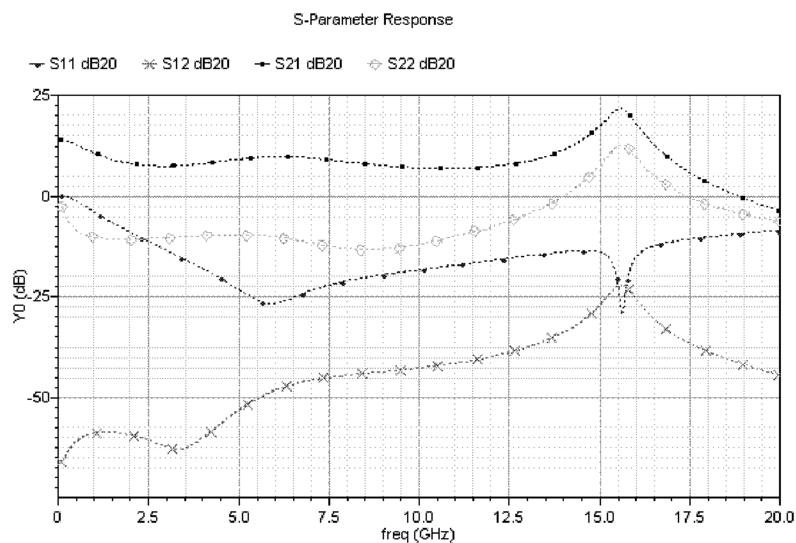


Figure 6.16: Proposed UWB LNA S-Parameters.

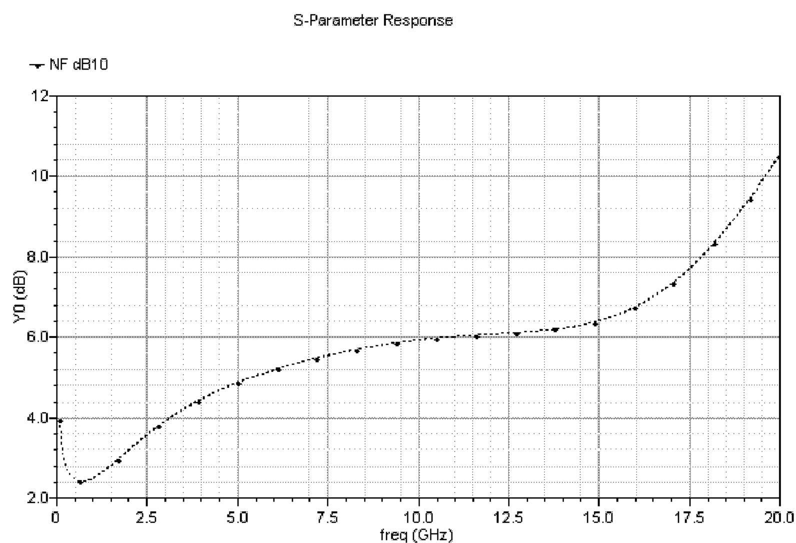


Figure 6.17: Proposed LNA noise figure.

Chapter 7

Conclusions

In this dissertation, the design of CMOS DAs for broadband wireline and wireless communication applications is studied.

Broadband preamplifiers/amplifiers are among the most important building blocks of broadband communications systems. Implementing these amplifiers in CMOS technology can be the first step toward a fully-integrated CMOS transceiver implementation. The circuit design is based on the distributed amplification technique. Since DAs do not suffer gain-bandwidth trade-off unlike other amplifier configurations, they can offer the gain/bandwidth performance required for the operation of broadband wireline and wireless transceivers. However, there are several issues that need to be resolved in order to make the distributed amplification a viable broadband amplification technique for RF CMOS IC designers.

In this dissertation, we addressed three major problems of CMOS DAs:

- large die area,

- performance degradation because of the transmission lines' losses in Si substrate, and
- large noise figure.

As summarized in Table 7.1, the proposed circuit techniques have improved the state-of-the-art performance of CMOS DAs in all of the above aspects.

An area-efficient CMOS DA has been proposed to address one of the main disadvantages of the DA compared with other broadband amplifiers. The proposed DA uses closely-placed interconnects instead of conventional spiral inductors or transmission lines. Implemented in an area of 0.17 mm by 1 mm in a 0.18 μm CMOS process, the CMOS DA exhibits the most compact implementation of a CMOS DA. Also the amplifier offers an area efficiency, defined as the ratio of gain-bandwidth product to area, significantly higher than those DAs implemented in CMOS technologies with the same feature size or smaller (90 nm CMOS).

Although distributed amplifiers can theoretically provide a bandwidth up to the cut-off frequency of transistors, this characteristic is dramatically affected by the loss of the transmission lines implemented on a semi-conductive substrate. In Chapter 5, we proposed a loss compensation technique that can fully compensate for the loss of the transmission lines (made of on-chip inductors) to achieve a flat gain over the entire bandwidth. The purposed DA achieves a gain of 10 dB over the entire 0-44 GHz bandwidth. The input and output return losses remain below -7 dB whereas amplifier consumes 44 mW from two 0.6-V and 1-V DC supplies.

Another drawback of a CMOS DA is its large noise figure which prevents it from being used as a preamplifier circuit topology in wireless transceivers. To solve this problem, we have replaced the terminating resistor of the gate transmission lines by a low-noise network.

Process / Ref.	BW (GHz)	G(dB)	A($mm \times mm$)	NF (dB)	S_{11} (dB)	S_{22} (dB)	$P_{DC}(mW)$
0.8 μm[24]	4.7	5	0.72×0.32	$5.1 - 7$	<-6	<-9	54
0.6 μm[25]	5.5	6.5	1.4×0.8	$5.3 - 8$	<-7	<-10	83.4
0.6 μm[26]	8.5	5.5	1.3×2.2	$8.7 - 13$	<-6	<-9.5	216
0.18 μm[27]	23	5	0.3×1.5	–	<-14	–	–
0.18 μm[28]	18	8	1.8×1.3	–	–	–	–
0.18 μm[29]	16	7.3	0.9×1.5	$4.3 - 6.1$	<-8	<-9	52
0.18 μm[30]	27	6	1.8×0.9	6	<-8	<-9	68
0.18 μm[31]	39	4	1.1×3.0	–	<-10	<-10	140
0.18 μm[32]	28	9	0.75×0.48	–	<-11	<-13	60
0.18 μm[33]	24	7.3	0.9×1.5	$4.3 - 6.1$	<-8	<-9	52
0.18 μm[34]	> 12.6	7.6	1.1×0.6	$5.5 - 9.0$	<-10	<-10	39.6
0.18 μm[35]	36	9.5	0.94×0.86	-	<-8	<-11	99
0.09 μm[36]	80	7	0.9×0.8	$6.0 - 6.9$	<-7	<-12	122
0.09 μm[37]	95	7.4	1.2×0.6	-	<-10	<-8	120
0.18 μm [AEDA]	27	9	0.17×1.0	3.8-5.5	<-12	<-8	85.8
0.13 μm [LCDA]	44	10	0.6×2.5	2.5-7.5	<-14	<-8	103
0.13 μm [LNDA]	$3 - 10$	12	0.55×1.5	2-4.5	<-9	<-11	30

Table 7.1: Comparison of reported performance of CMOS Distributed amplifiers with the works presented in this dissertation: Area Efficient DA (AEDA) , Loss-Compensated DA (LCDA), and Low-Noise DA (LNDA).

While the proposed network improves the noise of the CMOS DA, it degrades the input matching at low frequencies. This matching degradation can be tolerated for our intended UWB applications as the operation frequency band is 3 to 10 GHz. The devised CMOS

DA exhibits the lowest noise figure, 3.4 dB, reported for a CMOS DA in the literature.

In appendix A, a novel matrix-based lumped-element analysis of DAs is developed; the analysis is more suitable for the design in CMOS technology, and more flexible to optimize the amplifiers' figures of merit. An image impedance technique is employed for terminating the gate and drain lines of the amplifier. The simulation results indicate a higher gain and better gain uniformity over the bandwidth of the amplifier, compared to the transmission line matching technique. The image impedance matrix network is realized by using resistor, capacitor, and inductor components available in the technology.

In summary, we believe that distributed amplification will become a reliable circuit choice for the design of broadband amplifiers in CMOS technology. Offering a large bandwidth and a relatively flat gain accompanied with excellent input and output matchings are the unique characteristics of DAs that cannot be easily achieved by other broadband amplification techniques. With continuous scaling of CMOS technology, and the availability of thicker top metal layers, the loss of on-chip transmission lines will continue to decrease, leading to significant improvements in the performance of CMOS DAs.

7.1 Publications

Through the course of the Ph.D. program, the author have published the following journal and conference papers:

1. Kambiz K. Moez and Mohamed I. Elmasry,"A Lumped-Element Analysis of CMOS Distributed Amplifiers Based on Image Impedance Technique," *Microelectronics Jour-*

nal, vol. 37, no. 10 , pp 1136-1145, Oct. 2006.

2. Kambiz K. Moez and Mohamed I. Elmasry, "Area-Efficient CMOS Distributed Amplifier using Compact CMOS Interconnects," *IEE Electronics Letters*, , vol. 42, no. 17, pp 970-971, Aug. 2006.

3. Kambiz K. Moez and Mohamed I. Elmasry, "A 20-Stage CMOS Distributed Amplifiers using CMOS Interconnects for Artificial Transmission Lines," *IEEE Midwest Symposium on Circuit and Systems*, San Juan, Puerto Rico, USA.

4. Shahab Ardalan, Kambiz K. Moez, Manoj Sachdev, and Mohamed I. Elmasry, "Distributed Current Mode Logic," *IEEE Northeast Workshop on Circuits and Systems*, June 2006, Ottawa, Canada.

5. Kambiz K. Moez and Mohamed I. Elmasry, "A 3-10 GHz Low-Noise Amplifier for Ultra-Wideband Applications," *IEEE Northeast Workshop on Circuits and Systems*, June 2006 Ottawa, Canada.

6. Kambiz K. Moez and Mohamed I. Elmasry, "A Novel Loss Compensation Technique for Broadband CMOS Distributed Amplifiers," *IEEE International Symposium on Circuits and Systems*, May 21-24, 2006, Greece.

7. Kambiz K. Moez and Mohamed I. Elmasry, "A 10 GHz 15 dB CMOS Distributed Amplifier in 0.18um CMOS Process," *IEEE Design, Automation, and Test in Europe*, March 2006, Munich, Germany.

8. Kambiz K. Moez and Mohamed I. Elmasry, "Post Layout Simulation of RF CMOS Integrated Circuits with Passive Components," *2005 IEEE International Midwest Symposium on Circuits and Systems*, pp. 762-765, August 7-10, 2005, Cincinnati, Ohio, USA.

9. Kambiz K. Moez and Mohamed I. Elmasry, "Design of Broadband Bandpass CMOS Amplifiers Based on Modified Distributed Amplification Technique," *2005 IEEE International Midwest Symposium on Circuits and Systems*, pp. 794-797, August 7-10, 2005, Cincinnati, Ohio, USA.

10. Kambiz K. Moez and Mohamed I. Elmasry, "An Inductor-Free CMOS Broadband Amplifier," *IEEE Ph.D. Research in Microelectronics and Electronics Conference*, vol. 2, pp. 182-185, July 25-27, 2005, Lausanne, Switzerland.

11. Kambiz K. Moez and Mohamed I. Elmasry, "A Systematic Approach for Design of Broadband CMOS Amplifiers," *International IEEE Northeast Workshop on Circuits and Systems* , pp. 251-254, June 19-22, 2005, Quebec City, Canada.

12. Kambiz K. Moez and Mohamed I. Elmasry, "CMOS Distributed Amplifiers: An Integrated Solution for Broadband Optical and Wireless Communication Applications," *Second IFIP/IEEE International Conference on Wireless and Optical Communications Networks 2005*, March 6 - 8, 2005, Dubai, UAE.

13. Kambiz K. Moez and Mohamed I. Elmasry, "Design of CMOS Distributed Amplifiers for Maximum Bandwidth," *16th IEEE International Conference on Microelectronics*, pp. 317-319, December 6-8, 2004, Tunis, Tunisia.

14. Kambiz K. Moez and Mohamed I. Elmasry, "A Novel Lumped-Element Matrix-Based Analysis Method for CMOS Distributed Amplifiers," *IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 1048-51, May 23-26 2004, Vancouver, Canada.

Appendix A

Lumped-Element Modeling of CMOS DAs

A.1 Why Lumped-Element Modeling?

This appendix presents a systematic matrix-based lumped-element analysis of CMOS distributed amplifiers (DAs). Since transmission lines of the DAs are artificially constructed from a ladder of a finite number of inductors and capacitors, the conventional transmission-line-based analysis of microwave DAs cannot be accurately applied to CMOS DAs. The proposed lumped-analysis method in this appendix is also more intuitive for analog circuit designers than the transmission line analysis adapted from microwave amplifiers analysis because it provides the performance characteristics of the amplifiers as functions of circuit elements values, and not the transmission line characteristics. The image impedance technique is used for the design of input/output terminating networks. A new image impedance

matrix is defined to accommodate the extension of the theory from two-port to four-port networks, and a practical realization of the image impedance matrix is presented using the available circuit elements in CMOS technology. The simulation results clearly indicate an improved voltage gain and a better gain uniformity over the bandwidth of the proposed DA design terminated at its image impedance compared with the amplifier terminated at its nominal transmission line characteristics impedance.

As discussed in earlier chapters, the conventional microwave common-source FET DAs are constructed out of two transmission lines that connect drains and gates of field effect transistors (FETs). In this topology, the gate-source and drain-source capacitance of the transistors are absorbed into the transmission lines. Therefore, the parasitic capacitance of the transistor no longer limits the bandwidth, and instead introduces delay (latency) in the time domain response of the circuit. Bringing the distributed amplification technique to CMOS technology requires making essential changes in both analysis and design-changes which are justified below. The wavelength-frequency relation of electromagnetic waves traveling in the interconnects is given by

$$\lambda \times f = \frac{C}{\sqrt{\epsilon_{r,effective}}} \tag{A.1}$$

where λ is the wavelength, f is the frequency, C is the speed of light in free space (3108 m/s), and $\epsilon_{r,effective}$ is the effective relative permittivity of the silicon dioxide (3.9). Using the above relation, the wavelength is calculated to be 3.8 mm at 40 GHz. This implies that CMOS interconnects with lengths of up to 380 μm (one tenth of the wavelength) are not considered distributed elements at frequencies less than 40 GHz. This is the reason that transmission lines, which are essential to the operation of distributed amplifiers, are

realized by a ladder of inductors and capacitors in CMOS technology.

In this appendix, a new matrix-based lumped-element analysis for CMOS DAs is developed to provide the accuracy for the analysis of the DAs constructed of artificial transmission lines (LC ladders). Based on the new modeling of DAs, the amplifier's voltage and current gains, input and output impedance, and S-parameters can be obtained as functions of the circuit components' values. These functions are more intuitive for analog circuit designers than the transmission line analysis adapted from microwave amplifiers analysis since they provide a closed-form transfer function of the DA, where the system's zeros and poles can be easily located. Section A.2.1 of the appendix presents a definition of a four-port definition of ABCD matrices to facilitate the calculation of the overall ABCD matrix for a multi-stage CMOS DA. In Section A.2.2 , the final two-port ABCD matrix of the DA is calculated as a function of the elements of a four-port ABCD matrix. The application of the image impedance technique to the DAs is discussed in Section A.3 , and an image impedance matrix (IIM) is defined and then calculated to extend image impedance theory from the two-port networks to the four-port networks. A practical realization of IIM is presented in Section A.3.2 . Finally, to prove that the new approach is superior to the conventional design, both DA circuits terminated with image impedances and nominal transmission line characteristic impedances are simulated, with the results compared in Section A.4 .

A.2 Lumped-Element DA Analysis

A.2.1 ABCD Transmission Matrix and Properties

A schematic diagram of stage K of a uniform N-stage DA is depicted in A.1. An ABCD Transmission matrix is an effective representation for the analysis of cascaded networks since the overall ABCD matrix of the network can be readily computed by multiplying the ABCD matrices of the cascaded stages. An ABCD transmission matrix for the stage K of a DA is defined as follows:

$$\begin{bmatrix} V_{DK-1} \\ I_{DK-1} \\ V_{GK-1} \\ I_{GK-1} \end{bmatrix} = \begin{bmatrix} D_{11}^{(k)} & D_{12}^{(k)} & D_{13}^{(k)} & D_{14}^{(k)} \\ D_{21}^{(k)} & D_{22}^{(k)} & D_{23}^{(k)} & D_{24}^{(k)} \\ D_{31}^{(k)} & D_{32}^{(k)} & D_{33}^{(k)} & D_{34}^{(k)} \\ D_{41}^{(k)} & D_{42}^{(k)} & D_{43}^{(k)} & D_{44}^{(k)} \end{bmatrix} \begin{bmatrix} V_{DK} \\ I_{DK} \\ V_{GK} \\ I_{GK} \end{bmatrix}, \tag{A.2}$$

where the voltages and currents are denoted in Figure A.1. The DA ABCD matrix can be rewritten as a product of the following two ABCD transmission matrices as follows [71]:

$$D = A_1 \cdot A_2 \cdot A_1, \tag{A.3}$$

where

$$A_1 = \begin{bmatrix} 1 & \frac{1}{2YID_{12}} & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & \frac{1}{2YIG_{12}} \\ 0 & 0 & 0 & 1 \end{bmatrix}. \tag{A.4}$$

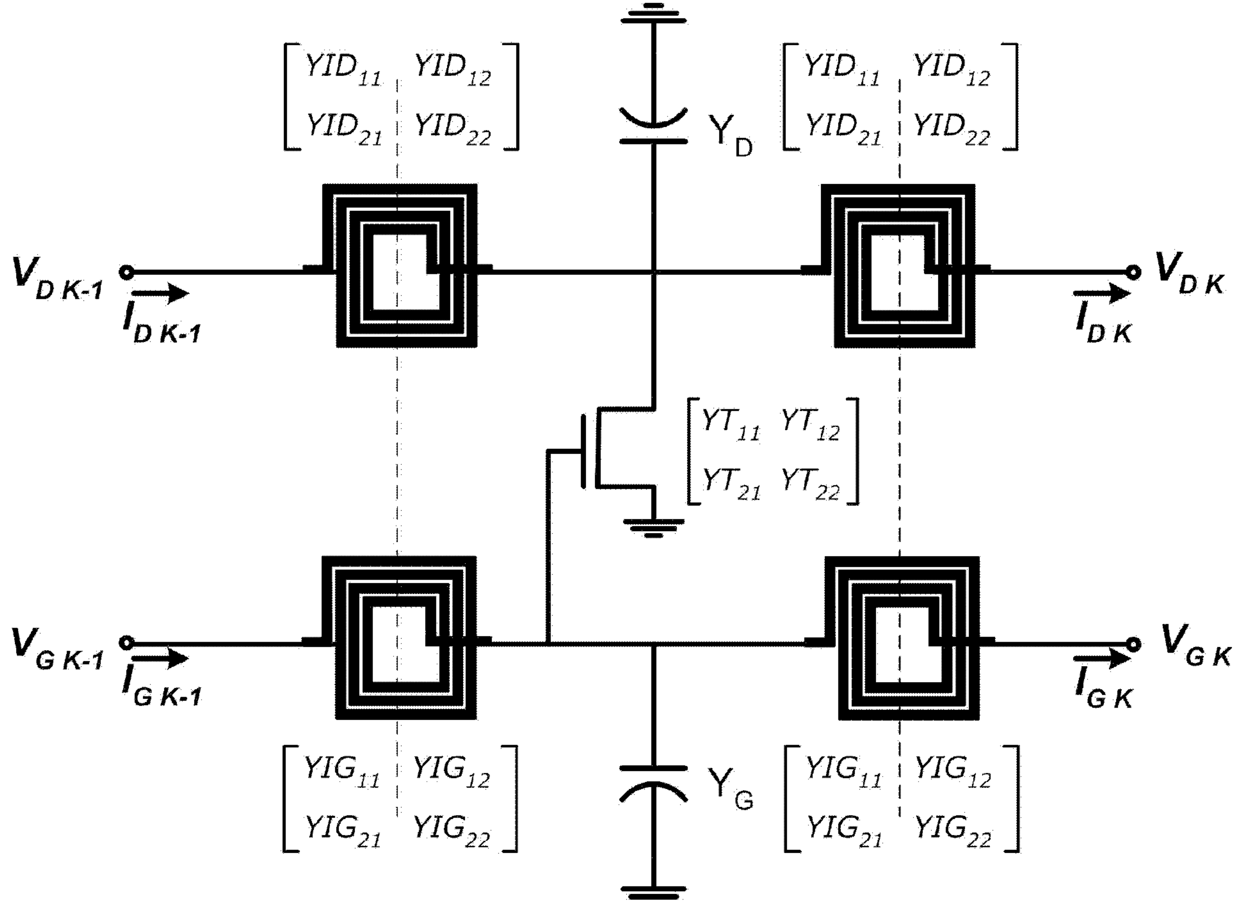


Figure A.1: Stage k of a uniform N-stage CMOS DA.

, and

$$A_2 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ YT_{22} + Y_D + YID_{11} + YID_{22} & 1 & YT_{21} & 0 \\ 0 & 0 & 1 & 0 \\ YT_{12} & 0 & YT_{11} + Y_G + YIG_{11} + YIG_{22} & 1 \end{bmatrix}, \quad \text{(A.5)}$$

where YID_{11}, YID_{12}, YID_{21}, and YID_{22} are the elements of the drain line's on-chip inductors admittance matrix, YIG_{11}, YIG_{12}, YIG_{21}, and YIG_{22} are the elements of gate line's on-chip inductors admittance matrix, and Y_{11}, Y_{12}, Y_{21}, and Y_{22} are the elements of the transistor's admittance matrix. The Y parameter of the on-chip inductors is assumed to be symmetrical in the above derivation,, where $YID_{12} = YID_{21}$ and $YIG_{12} = YIG_{21}$. The most important properties of the ABCD matrix stem from the fact that the amplifier network is reciprocal if regarded as a four-port network. If the directions of the currents in the ABCD matrix are modified toward the network, the inverse of the resulting ABCD matrix should be equal to itself, or, in other words, the inverse of the ABCD matrix is equal to

$$\begin{bmatrix} D_{11} & D_{12} & D_{13} & D_{14} \\ D_{21} & D_{22} & D_{23} & D_{24} \\ D_{31} & D_{32} & D_{33} & D_{34} \\ D_{41} & D_{42} & D_{43} & D_{44} \end{bmatrix}^{-1} = \begin{bmatrix} D_{11} & -D_{12} & D_{13} & -D_{14} \\ D_{21} & -D_{22} & D_{23} & -D_{24} \\ D_{31} & -D_{32} & D_{33} & -D_{34} \\ D_{41} & -D_{42} & D_{43} & -D_{44} \end{bmatrix}. \tag{A.6}$$

where D is the ABCD matrix of an N-stage DA and equal to $D^{(1)}D^{(2)}D^{(N)}$ in general, and where the DA, if uniform, is equal to $(D^{(k)})^N$ for any k =1..N. Furthermore, the reciprocity condition implies that the amplifier's impedance, admittance, and scattering matrices are symmetric ($Z = Z^t$, $Y = Y^t$, and $S = S^t$).

A.2.2 Final Two-Port Network

The next step is to calculate the 2×2 ABCD matrix of the amplifier from the G_0 port to the D_N port, whereas the other two ports, G_N and D_0, are terminated in the Y_{GT} and Y_{DT}

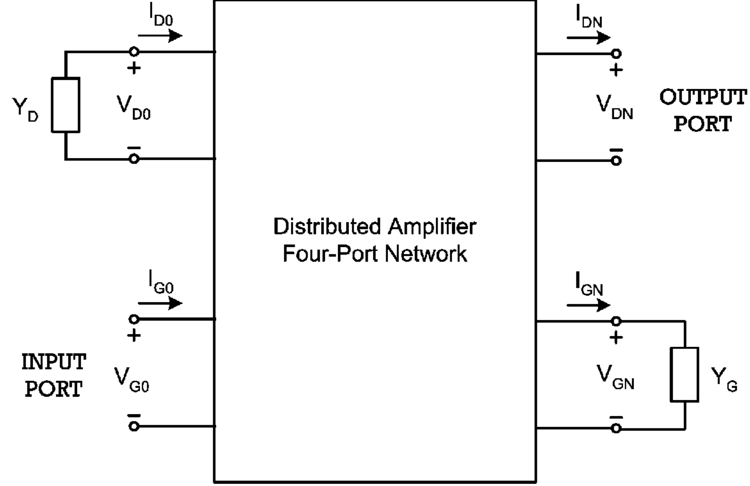


Figure A.2: Final two-port network.

admittances as shown in A.2. To obtain the ABCD matrix of the other two ports, I_{D0} and I_{GN} are replaced in the following matrix:

$$\begin{bmatrix} V_{D0} \\ -Y_{DT}\, V_{D0} \\ V_{G0} \\ I_{G0} \end{bmatrix} = \begin{bmatrix} D_{11} & D_{12} & D_{13} & D_{14} \\ D_{21} & D_{22} & D_{23} & D_{24} \\ D_{31} & D_{32} & D_{33} & D_{34} \\ D_{41} & D_{42} & D_{43} & D_{44} \end{bmatrix} \begin{bmatrix} V_{DN} \\ I_{DN} \\ V_{GN} \\ Y_{GT}\, V_{GN} \end{bmatrix}. \tag{A.7}$$

If the first line is multiplied Y_{DT}, and added to the second line, the dimension of the matrix is reduced to 3×4 as follows:

$$\begin{bmatrix} 0 \\ V_{G0} \\ I_{G0} \end{bmatrix} = \begin{bmatrix} D_{21} + D_{11}\, Y_{DT} & D_{22} + D_{12}\, Y_{DT} & D_{23} + D_{13}\, Y_{DT} & D_{24} + D_{14}\, Y_{DT} \\ D_{31} & D_{32} & D_{33} & D_{34} \\ D_{41} & D_{42} & D_{43} & D_{44} \end{bmatrix} \begin{bmatrix} V_{DN} \\ I_{DN} \\ V_{GN} \\ Y_{GT}\, V_{GN} \end{bmatrix}. \tag{A.8}$$

The dimension of the matrix can be further reduced to 3 3 by simple algebraic manipulations as follows:

$$\begin{bmatrix} 0 \\ V_{G0} \\ I_{G0} \end{bmatrix} = \begin{bmatrix} D_{21} + D_{11}\, Y_{DT} & D_{22} + D_{12}\, Y_{DT} & D_{23} + D_{13}\, Y_{DT} + D_{24}\, Y_{GT} + D_{14}\, Y_{DT}\, Y_{GT} \\ D_{31} & D_{32} & D_{33} + D_{34}\, Y_{GT} \\ D_{41} & D_{42} & D_{43} + D_{44}\, Y_{GT} \end{bmatrix} \begin{bmatrix} V_{DN} \\ I_{DN} \\ V_{GN} \end{bmatrix} \tag{A.9}$$

Then, from the first line of the above matrix, the V_{GN} can be obtained as a function of V_{DN} and I_{DN}. By replacing V_{GN} in the previous matrix, the final ABCD matrix of the DA two-port network can be simplified to the following equation:

$$\begin{bmatrix} V_{G0} \\ I_{G0} \end{bmatrix} = \begin{bmatrix} D_{31} - \frac{(D_{21}+D_{11}\, Y_{DT})(D_{33}+D_{34}\, Y_{GT})}{D_{23}+D_{13}\, Y_{DT}+(D_{24}+D_{14}\, Y_{DT})Y_{GT}} & D_{32} - \frac{(D_{22}+D_{12}\, Y_{DT})(D_{33}+D_{34}\, Y_{GT})}{D_{23}+D_{13}\, Y_{DT}+(D_{24}+D_{14}\, Y_{DT})Y_{GT}} \\ D_{41} - \frac{(D_{21}+D_{11}\, Y_{DT})(D_{43}+D_{44}\, Y_{GT})}{D_{23}+D_{13}\, Y_{DT}+(D_{24}+D_{14}\, Y_{DT})Y_{GT}} & D_{42} - \frac{(D_{22}+D_{12}\, Y_{DT})(D_{43}+D_{44}\, Y_{GT})}{D_{23}+D_{13}\, Y_{DT}+(D_{24}+D_{14}\, Y_{DT})Y_{GT}} \end{bmatrix} \begin{bmatrix} V_{DN} \\ I_{DN} \end{bmatrix} \tag{A.10}$$

Based on the above final two-port network ABCD matrix A.10, designers are able to calculate the closed form equations for the amplifier's parameters, such as voltage gain, current gain, and S-parameters, as functions of the circuit's elemental values. This enables a more intuitive circuit design by having a closed-form formula for amplifier transfer function by locating the zeros and poles of the system. From a microwave design perspective, the final S-parameters of the amplifier network can be obtained as a function of the S-parameters (or Y parameters) of the inductors and transistors. This will lead to a very

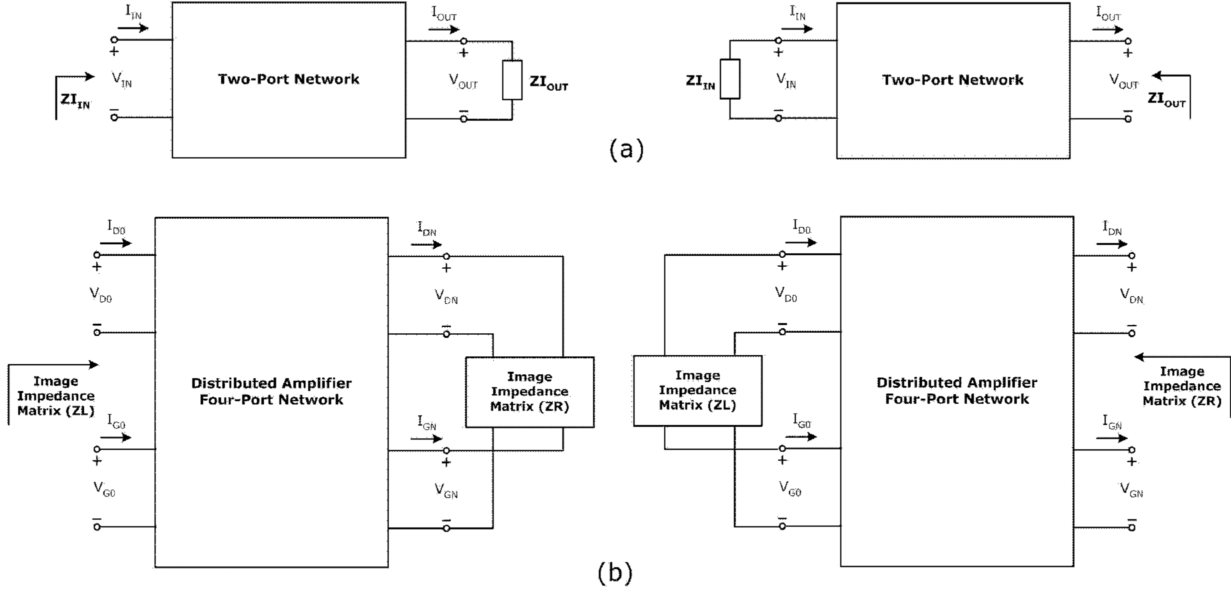


Figure A.3: Definition of (a) scalar image impedance, and (b) image impedance matrix (IIM).

highly accurate design of the DAs, since the EM-simulated/measured S-parameters of each individual component can directly be plugged in the DA model. Since there in no computationally extensive mathematical task involved in the calculation of the final two-port network characteristics, this modeling technique is extremely time efficient.

A.3 Image Impedance Termination

A.3.1 Definition and Calculation of Image Impedance Matrix

The image impedance method is used for the analysis and design of the periodical structure filters in [21]. This method can be applied to DAs because of their periodical structure. Based on the definition of image impedance for a two-port network, the image impedance at the input port, ZI_{IN}, is the input impedance at the input port when the output port is terminated in ZI_{OUT}, and the image impedance at the output port , ZI_{OUT}, is the input impedance at the output port when the input port is terminated with ZI_{IN} as illustrated in Figure A.3(a). In this case, both ports are matched when terminated in their image impedances. To extend the image impedance theory to four-port networks, an image impedance matrix (IIM) is defined instead of scalar image impedances. As shown in Figure A.3(b), the IIM ZL is the input impedance matrix of the left ports when the right ports are terminated in their IIM ZR, and vice versa. Because of the reciprocity of the network, the two image impedance matrices are equal (ZR = ZL = Z). Thus, it can be concluded from its definition that the IIM of the one-stage amplifier is equal to that of the N-stage amplifier. To calculate the IIM of a uniform DA with a given four-port ABCD matrix for

its stage k, these three sets of equations must be solved simultaneously:

$$\begin{bmatrix} V_{Dk} \\ V_{Gk} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_{Dk} \\ I_{Gk} \end{bmatrix}.$$

$$\begin{bmatrix} V_{DK-1} \\ I_{DK-1} \\ V_{GK-1} \\ I_{GK-1} \end{bmatrix} = \begin{bmatrix} D_{11}^{(k)} & D_{12}^{(k)} & D_{13}^{(k)} & D_{14}^{(k)} \\ D_{21}^{(k)} & D_{22}^{(k)} & D_{23}^{(k)} & D_{24}^{(k)} \\ D_{31}^{(k)} & D_{32}^{(k)} & D_{33}^{(k)} & D_{34}^{(k)} \\ D_{41}^{(k)} & D_{42}^{(k)} & D_{43}^{(k)} & D_{44}^{(k)} \end{bmatrix} \begin{bmatrix} V_{DK} \\ I_{DK} \\ V_{GK} \\ I_{GK} \end{bmatrix}.$$

$$\begin{bmatrix} V_{Dk-1} \\ V_{Gk-1} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_{Dk-1} \\ I_{Gk-1} \end{bmatrix}. \tag{A.11}$$

There are eight unknown voltages and currents and four unknown impedances in the above set of equations. Since there are eight equations in the set, all voltages and currents can be eliminated in order to end up with a relationship between the element of the image impedance matrix and the elements of the four-port ABCM of stage k of the DA.

If the transistor is assumed to be unilateral, that is, if $Y_{21} = 0$, then the following conditions must be met to render the above matrix equal to its reverse:

$$
\begin{aligned}
&D_{31} = D_{32} = D_{41} = D_{42} = 0 \\
&D_{11} = D_{22} \\
&D_{33} = D_{44} \\
&D_{21} = (D_{11}^2 - 1)/D_{12} \\
&D_{34} = (D_{33}^2 - 1)/D_{43} \\
&D_{13} = (-D_{11}D_{14} + D_{12}D_{24} + D_{14}D_{33})/D_{34} \\
&D_{23} = (D_{14} - D_{11}^2 D_{14} + D_{12}D_{24}D_{33} + D_{11}D_{12}D_{24})/D_{12}D_{34}
\end{aligned}
\tag{A.12}
$$

It is evident that the elements of the DA ABCD matrix are not independent. In the derivation of the previous conditions, D_{11}, D_{12}, D_{14}, D_{24}, D_{33}, and D_{34} are considered independent variables, and the other matrix elements are calculated as the functions of these independent variables.

The IIM of a simple DA network is calculated in this section. For the cell gain topology, a simple transconductance gain (g_m) is selected. The parasitic capacitance of transistors and inductors and the drain and gate line's capacitors are merged and denoted as Cd and C_g. The inductance of the drain and gate line's spiral inductors are denoted as L_d and L_g, whereas the parasitic series resistance of these inductors is ignored in this calculation. By solving the equation set in A.11, the elements of the IIM of a single-stage amplifier for the simple amplifier cell gain can be computed as follows:

$$
Z_{11} = \sqrt{\frac{2L_d - \omega^2 L_d^2 C_d}{C_d}}, \tag{A.13}
$$

$$Z_{22} = \sqrt{\frac{2L_g - \omega^2 L_g^2 C_g}{C_g}}, \tag{A.14}$$

$$Z_{21} = 0, \tag{A.15}$$

and Z_{12} can be calculated as function of Z_{11} and Z_{22} as follows:

$$Z_{21} = \frac{g_m(Z_{11}Z_{22} + j\omega L_d Z_{22} + j\omega L_g Z_{11}\omega^2 L_d L_g)}{w(wC_d C_g Z_{11} Z_{22} - jC_d Z_{11} - jC_g Z_{22} + j\omega^2 Z_{22} L_d C_d C_g + j\omega^2 Z_{11} L_g C_d C_g + wL_g C_g + wL_d C_d - \omega^3 L_d L_g C_d C_g)} \tag{A.16}$$

It is noteworthy to mention that the elements of a single-stage DA image matrix are equal to those of a uniform multi-stage DA. Simulation results for one-stage, three-stage, and five-stage DAs terminated in its image impedance matrix network are shown in Figure A.4(a). This amplifier network exhibits unstable behavior at DC and at its cutoff frequency. Except at these frequencies, the IIM-terminated DA provides a flat gain over the entire bandwidth.

A.3.2 Realization of Image Impedance Matrix

Since the analysis provided in previous sections is merely mathematical, exploring the possibility of a realization of the IIM network using available circuit components in CMOS technology is logical. In this section, we seek a practical realization of the IIM network while trying to eliminate the instability condition of the amplifier at DC and cutoff frequencies. Since the computed Z_{21} is 0 in the unilateral case, the IIM network appears to be a unilateral structure as well. Therefore, the solution appears to be the same circuit as that of one cell found in the amplifier, and terminated in the scalar impedances. Writing the equations to obtain the image impedance results in an unsolvable set of equations, and indicates that such a network is not feasible. Although the arrangement is not the

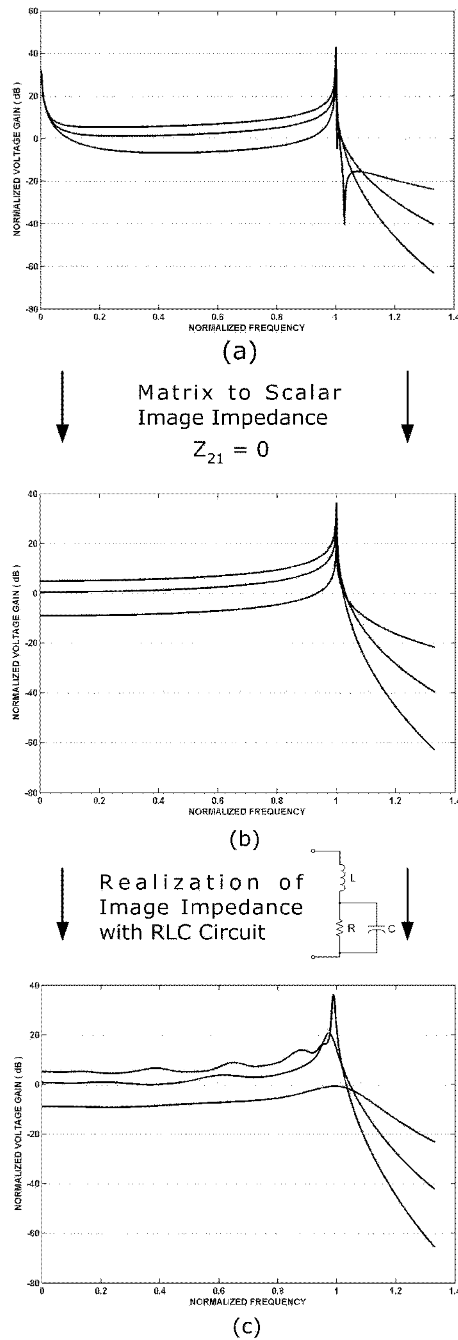


Figure A.4: Simulated amplifier voltage gains as functions of frequency for one-stage, three-stage and five-stage DAs terminated in (a) its IIM network, (b) scalar image impedance Z_{11} and Z_{22} (Z_{12} is ignored), and (c) fitted RLC image impedances.

only configuration that can be examined for realizing the IIM network, any answer to the question would result in a highly complicated network.

As the infinite magnitude of Z_{12} causes the instability of the amplifier at DC, one solution to this problem is to ignore the IMM matrix component Z_{12}. In this case, the realization of a unilateral two-port network is also simplified to the realization of scalar image impedances Z_{11} and Z_{22}. It is important to know how the voltage gain of the amplifier changes if Z_{12} is neglected; therefore, the distributed amplifier circuit is simulated using the model developed in Section A.2.2 . The simulation results, presented in Figure A.5(b), imply that there are no significant changes in the voltage gain of the DA over the entire bandwidth except at very low frequencies. At such frequencies, the gain overshoot is removed in the new amplifier configuration, resulting in a better gain-flatness and stability.

The task of realization of the IIM network is now simplified to the realization of Z_{11} and Z_{22} scalar impedances. As depicted in Figure A.5, Z_{11} is a pure ohmic impedance within the bandwidth of the amplifier and a pure imaginary impedance outside the bandwidth. Since Z_{11} is a mathematically computed impedance with no physical base for the realization, the solution is to fit a linear network of impedances to Z_{11}, which is a pure ohmic impedance at DC frequency, which scales down to zero at the cutoff frequency. The best circuit to model the behavior in this region is a resistor in parallel with a capacitor. To model the behavior of Z_{11} outside of the band, adding an inductor, in series, to the previous model is necessary. To find the values of R, L, and C in such a way as to obtain the circuit model closest to Z_{11}, a direct search method optimization algorithm [72, 73] is used to minimize the difference between the magnitudes of Z_{11} and the RLC model. The optimization algorithm converges

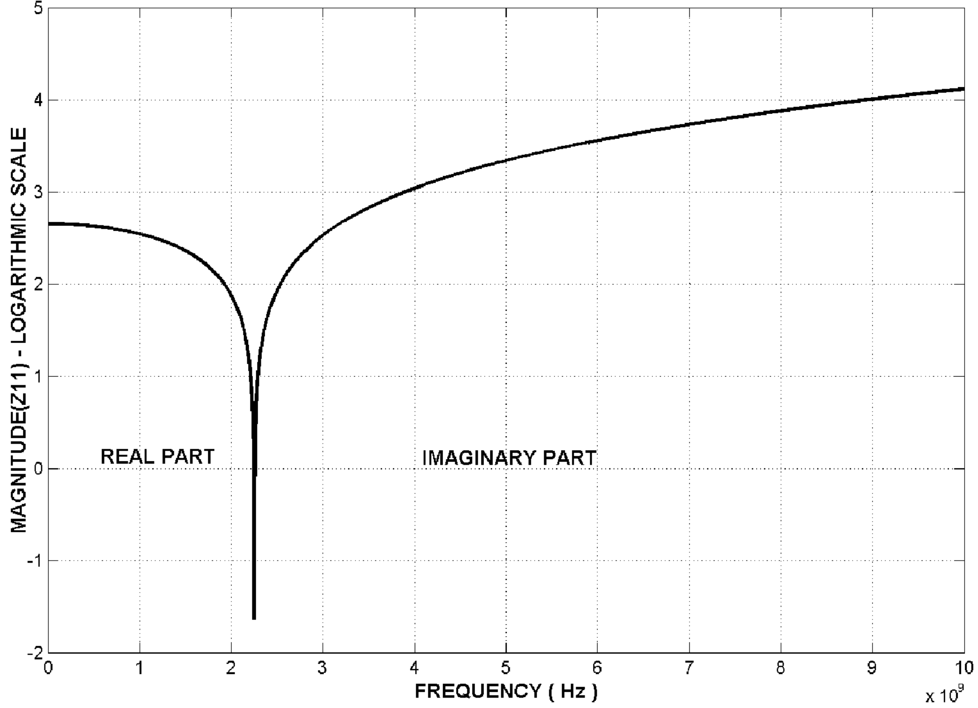


Figure A.5: Magnitude of Z_{11} (logarithmic scale) as a function of frequency.

to the following points:

$$L = .397L_d,\, C = .5118C_{ds},\, and\, R = 1.0232\sqrt{2L_d/C_{ds}}. \qquad \text{(A.17)}$$

The simulation results for the fitted RLC model are demonstrated in Figure A.4(c). Replacing Z_{11} with the linear RLC impedance, the other gain overshoots at the cutoff frequency are also omitted because the magnitude of the Z_{11} is not zero at this frequency anymore. This also improves the stability of the amplifier.

A.4 Simulation Results and Comparison

In this section, the voltage gain of a DA terminated at a fitted RLC circuit is compared with that of the conventional DA design terminated at nominal characteristic impedances of artificial transmission lines, which are $\sqrt{L_g/C_g}$ and $\sqrt{L_d/C_d}$, respectively. Based on the modeling methodology developed in this appendix, these two circuits with one, three, and five-stage gain cells are simulated, with the results shown in Figure A.6. These simulation results show the improvements in gain and gain uniformity achieved by the image impedance technique. The bandwidths of the gate and drain lines are given by and respectively. The upper limit of the amplifier bandwidth is determined by the minimum of the gate and drain line bandwidths which are equal if $L_dC_d = L_gC_g$. As a design guide, the product of L_d and C_d (and proportionally the product of L_d and C_d) must be minimized to achieve the largest possible bandwidth if the frequency response of the amplifier outside the bandwidth has no importance for the system specification. However, the minimum values of C_d and C_g are limited to the intrinsic capacitance of the transistors. The simulation results also indicate that the gain and the filtering behavior of the DA are improved by increasing the number of amplifier stages at the cost of using a greater die area.

A.5 Summary

In this appendix, a novel matrix-based lumped-element analysis method is developed for CMOS DAs. The lumped-element modeling of DAs provides the final two-port network

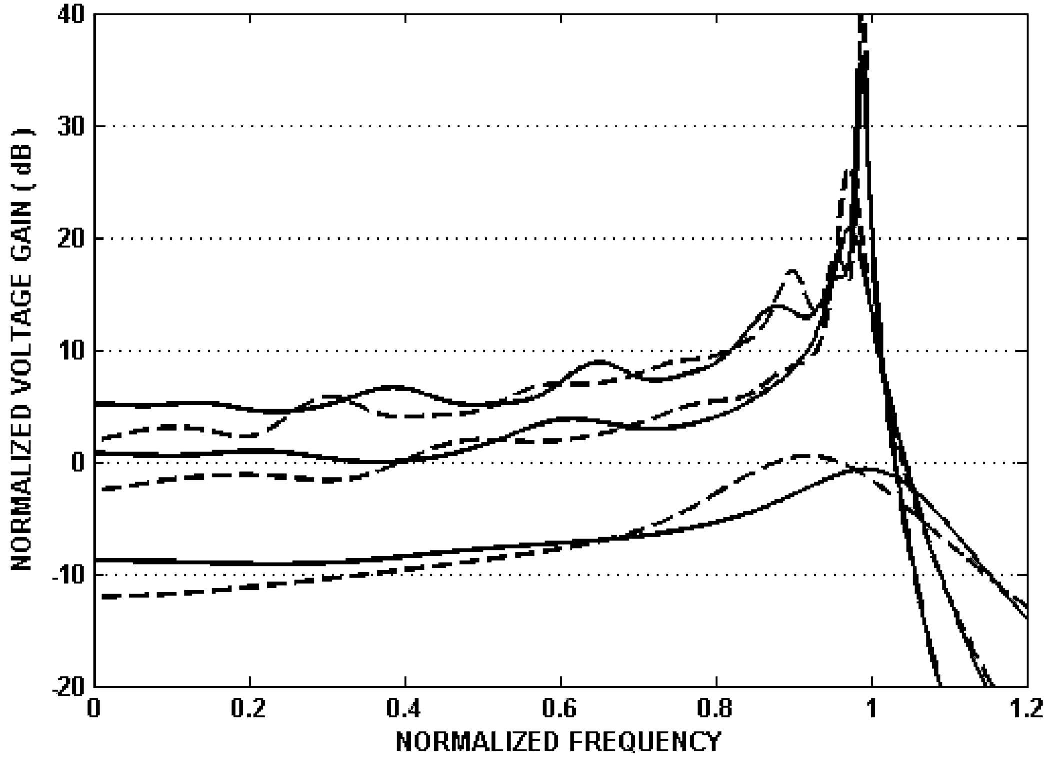


Figure A.6: Simulated amplifier voltage gains as functions of frequency for one-stage, three-stage and five-stage DAs terminated in fitted RLC image impedances (solid lines), and the nominal impedance characteristic impedance of gate and drain transmission lines (dotted lines).

characteristics as functions of the circuit elements which is more intuitive for analog circuit designers. S-parameters of the overall DA network can also been obtained if the S-parameters of each circuit component are provided by the means of the measurements or EM simulation. The image impedance technique is extended to accommodate the four-

port definition of a DA, and the defined IIM is computed for a DA with a simple gain cell element. The mathematically-computed IIM is realized using available circuit components (RLC circuit) which results in a higher voltage gain and a better gain uniformity than the conventional design using the transmission line matching.

Appendix B

Glossary of Mathematical Symbols

f frequency in Hertz

ω frequency in radians per second

λ wavelength

C speed of light

Z impedance or characteristic impedance

Y admittance

R resistance

C capacitance

L inductance or self inductance

M mutual inductance

g_m MOSFET's transconductance

C_{gs} gate-source capacitance

C_{gd} gate-drain capacitance

γ propagation constant

α attenuation constant

β phase constant

G power gain

A_v voltage gain

f_T cutoff frequency

BW bandwidth

w transistor channel width

l transistor channel length

σ metal conductivity

ϵ_{ox} oxide permittivity

J current density

μ permeability

F noise figure

NF noise figure in dB

w conductor width

t conductor thickness

GMD geometric mean distance

Z_{in} input impedance

Z_{out} output impedance

Γ_{in} input reflection coefficient

Γ_{out} output reflection coefficient

K stability factor

k Boltzmann's constant

T temperature in Kelvin

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