ADVANCEMENTS IN CURRENT-SOURCED INVERTER METHODOLOGIES FOR USE IN SMALL-SCALE POWER GENERATION

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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ABSTRACT

As the costs of large-scale power generation and transmission rise, distributed generation is becoming a prevalent alternative used by a growing number of both residences and businesses. Distributed generation systems typically consist of two main components: a small-scale, often high-efficiency or renewable power source, such as a fuel cell, solar panel, or wind turbine, and a power electronic converter to convert the raw power produced by the source to a usable form.

In North America, the majority of power used in residential and light commercial locations is provided in a form known as *single-phase three-wire*, or *split-phase*. This consists of two *half-phase* AC voltages, each of 110 to 120V rms, and one combined AC voltage of 220 to 240V rms. It is therefore necessary for distributed generation systems to supply power in this same form so that it can be used by standard loads such as lighting or appliances, and the excess power can be fed back into the distribution grid. The most common type of converter used to make this conversion is the voltage-sourced inverter (VSI). There are, however, some advantages to using a current-sourced inverter (CSI) instead. These include improved output voltage waveform quality, built-in voltage boost, and built-in overcurrent protection. However, there are also two obstacles that have prevented the adoption of current-sourced inverters to date.

The first obstacle to the use of current-sourced inverters is that they require a DC current input to operate. Therefore, a circuit and control algorithm must be developed to produce a DC current from a low DC voltage source. The first part of this thesis deals with the generation of a suitable DC current.

The second major obstacle to adopting current-sourced inverters is that no algorithm for producing single-phase three-wire outputs with a CSI presently exists in literature. The second part of this thesis develops such a switching algorithm, using a three-leg current-sourced inverter. The algorithm is demonstrated using simulation and experimental results, which show that the proposed system is able to successfully generate balanced output voltages under unbalanced loading conditions while equalizing switch utilization and minimizing output voltage ripple.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

DG ..... Distributed Generation (Generator)
DC ..... Direct Current
AC ..... Alternating Current
RPM ..... Revolutions Per Minute
VSI ..... Voltage-Sourced Inverter
CSI ..... Current-Sourced Inverter
PWM ..... Pulse Width Modulation
FACTS ..... Flexible AC Transmission Systems
IGBT ..... Isolated Gate Bipolar Transistor
GTO ..... Gate Turn-Off thyristor
RMS ..... Root-Mean-Square
RB-NPT (IGBT) ..... Reverse Blocking Non-Punch-Through
ODE ..... Ordinary Differential Equation
DSP ..... Digital Signal Processor
THD ..... Total Harmonic Distortion
PI ..... Proportional-Integral (controller)
MOV ..... Metal Oxide Varistor

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND AND LITERATURE REVIEW

1.1.1 DISTRIBUTED GENERATION

With energy costs rising worldwide and concerns being raised regarding the environmental impact and increasing scarcity of fossil fuels, *distributed generation*, or DG, is becoming viable and cost-effective as both a supplement and an alternative to large-scale power generation. Distributed generation refers to the generation of power on a small scale, at the distribution system level. It consists of low-power generators such as microturbines, solar cells, wind turbines and fuel cells, used to power houses or small businesses, and connected to the distribution grid. There are a number of advantages to distributed generation. Many distributed generators (DGs) make use of renewable energy sources that would not be viable on a larger scale. Combining a distributed generator with a grid connection provides a backup power source in case of an outage, as well as a potential source of income if the power generated by the DG exceeds the local requirements. In addition, many power utilities are adopting variable pricing schemes in an attempt to improve time distribution of loading throughout the day. This is known as *peak-shaving*, and is intended to reduce the peak requirements on the network, thereby delaying the need to add generation capacity. A distributed generator allows a customer to avoid paying for power during the expensive, peak periods of the day [1]. If the DG system has energy

storage capability, it is then possible to recharge the energy storage element during the less expensive periods.

Any distributed generation system requires two basic components. The first is a source of electrical power. Depending on the type of source, the raw power produced may be DC, constant frequency AC, or variable frequency AC. The voltage may be constant or variable. Therefore, the second basic component is a converter circuit to convert this raw power to the same standardized voltage and frequency as are supplied by the distribution grid. This allows it to either be used by local loads, such as lighting or appliances, or to be fed back into the grid. The most common types of power sources used in DG systems are the following:

- **Microturbine**
  Microturbines are small combustion turbines that operate with a turbine and compressor on the same shaft as the electrical generator. They can burn a number of fuels, such as natural gas, propane, and biofuel. Microturbines operate at speeds from 50,000 to 120,000 RPM, resulting in very high frequency AC power generation. The capacities of commercially-available microturbines range from tens to hundreds of kilowatts [2].
- **Wind Turbine**
  Wind turbines are not strictly distributed generators, as their most common implementation is in large numbers as part of a *wind farm*. These farms generally consist of up to a hundred wind turbines, each of which can produce as much as 6MW of power, with average units producing 1 to 1.5MW. Individual units are also common, particularly in the form of small, non-commercial turbines in remote areas. Individual units are found in a wide range of capacities, from the commercial units of over 1MW to residential units of as low as several hundred watts. Wind turbines generally produce AC power at variable frequency, depending on wind speed [3]. Since they rely on the presence of wind to provide power, they must be combined with energy storage or an alternate power source [4].
- **Solar Cells**
  A solar cell is another device for producing electrical power from a renewable

source, in this case, light from the sun. These cells are generally combined into solar panels, which can be placed on the roofs of buildings among other locations. A solar panel produces variable, low-voltage DC power. The level of the voltage, as well as the amount of power produced, depends on the intensity of the light shining on the panel [5][6]. Therefore, like wind turbines, solar cells must be paired with an alternative power source or an energy storage device to provide uninterrupted power.

- **Fuel Cell**

  Fuel cells produce electricity through a chemical reaction between hydrogen fuel and oxygen, usually derived from the atmosphere. Operating at steady-state, they produce a constant DC voltage; however, the voltage level does vary based on loading. A fuel cell behaves like a combination of a battery and a generator in that it produces a relatively constant DC voltage, but operates on external fuel, continuing to operate as long as that fuel is supplied.

- **Battery Pack**

  Technically, this is not a form of distributed generation because it does not actually produce electrical power. However, it does offer many of the same benefits, including providing backup power and redistributing load to less expensive, off-peak periods. Batteries produce a constant, low DC voltage through an internal chemical reaction. They must be recharged electrically, however, as they do not produce electricity from an external power source.

1.1.2 POWER ELECTRONICS CONVERTERS

The purpose of the converter in a distributed generation system is to convert the raw power generated into a form compatible with the local distribution grid, thereby allowing the power to be used by standard appliances or to be fed back into the grid. Residential and light-commercial power in North America is provided in *single-phase three-wire* form (also known as *split-phase*). Generally, this arrangement is implemented using a center-tap on the distribution transformer. It provides two outputs at 110 to 120V rms, referred to as *half-phases*. Together, these also form one high-voltage output at 220V to 240V rms. The type

of converter required to produce these outputs from a DG depends on the type of generator used.

A very common type of conversion is from low-voltage DC to split-phase, utility-voltage AC. Solar cells, fuel cells, and battery packs all require this type of conversion. It is generally done in two stages. First, the low, potentially variable, DC voltage is converted to a higher, constant DC voltage, using a boost DC/DC converter. Next, the higher DC voltage is inverted to produce the desired single-phase three-wire outputs, usually with a voltage-sourced inverter (VSI). This system is shown in Fig. 1-1. Conversions from AC sources such as wind turbines and microturbines are most often done by adding an AC/DC converter (rectifier) before the DC/DC boost stage in Fig. 1-1. The AC voltage is converted to DC by the rectifier, and from there the process remains the same.

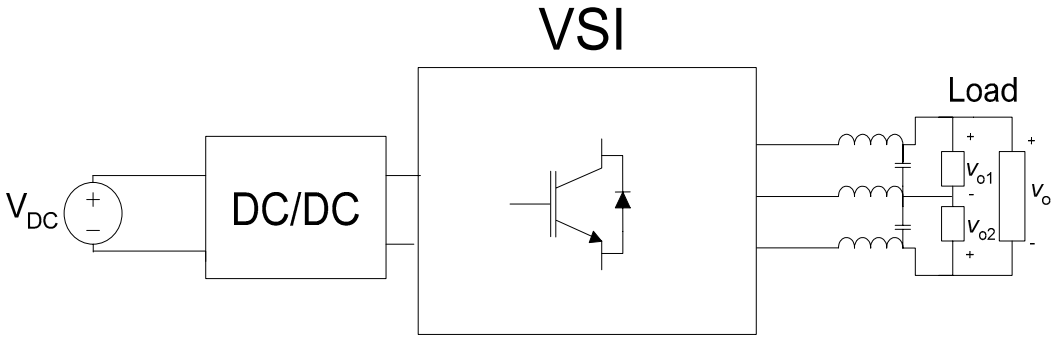

Fig. 1-1. Standard topology used to produce split-phase utility-voltage outputs from a low-voltage DC source

1.1.2.1 Voltage-Sourced Inverters

Existing voltage-sourced inverter topologies producing split-phase outputs are divided into two main categories: split DC capacitor or 'neutral point clamped' inverters, and three-leg inverters. An overview of some existing topologies is given in [7]. The split DC capacitor method establishes a loosely regulated balance of output voltages. An implementation of this scheme for photovoltaic systems is found in [8], and the basic topology is shown in Fig. 1-2. Two large DC capacitors hold the neutral point of the output approximately halfway between the positive and negative voltage rails. This approach successfully balances the output voltages when the difference between loads is not too large.

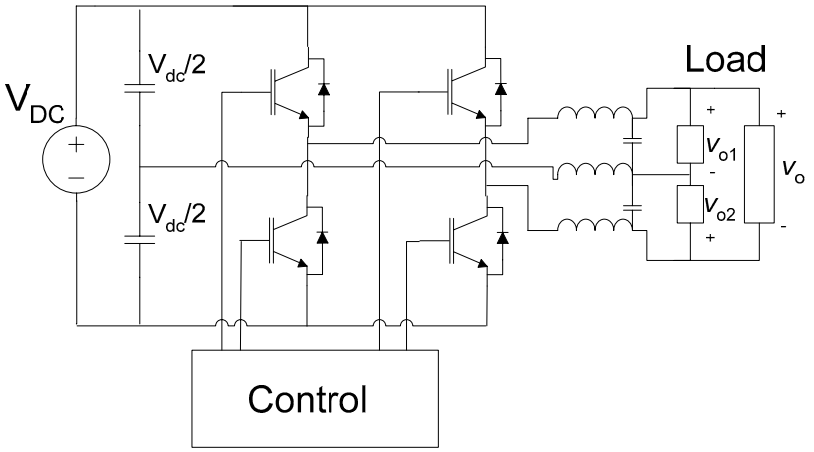

Fig. 1-2. Split DC capacitor method

The second category of VSI split-phase topologies relies on a third leg of switches to regulate the neutral point voltage (Fig. 1-3). Generally, the original four switches (numbered 1 to 4 in the figure) are used to control the total output voltage, V_o. The additional two switches (numbered 5 and 6) maintain the neutral point voltage at $V_{dc}/2$. This can be accomplished with very simple, decoupled control, where switches 1 to 4 work as in the single-phase case and switches 5 and 6 alternate with a 50% duty cycle to hold the average neutral point voltage halfway between the DC rails. While straightforward, this technique improves upon the results of the split capacitor method, at the cost of two additional switches.

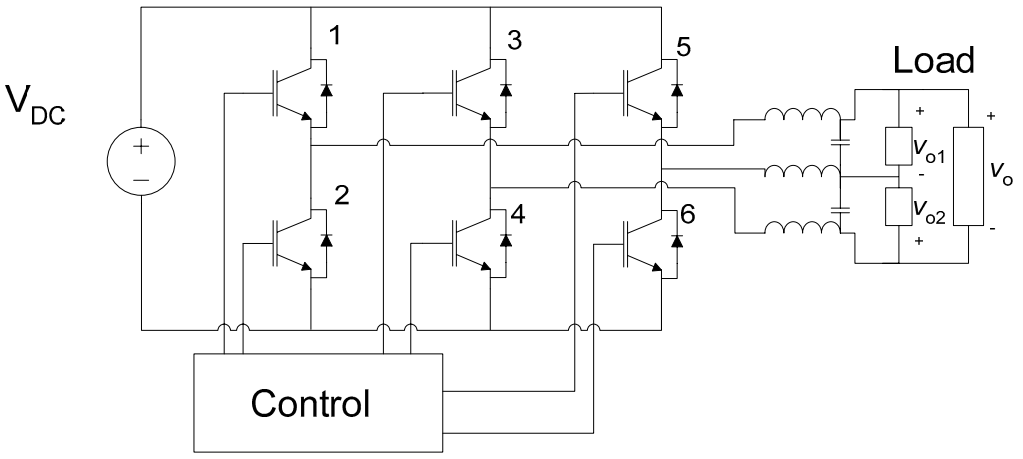

Fig. 1-3. Third-leg method

More complex switching schemes, such as state-feedback control, may also be implemented for this topology. These still tend to deal with switches 5 and 6 independently from switches 1 to 4 in terms of individual switching events. However, the modulation signals used to control the two groups of switches may be incorporated into a single control scheme in order to generate better regulated outputs [9][10]. These techniques provide better output voltage regulation, but are more complex and require measurement and feedback of output currents as well as voltages.

1.1.2.2 Current-Sourced Inverters

An alternative to the voltage-sourced inverter is the current-sourced inverter (CSI), shown in Fig. 1-4.

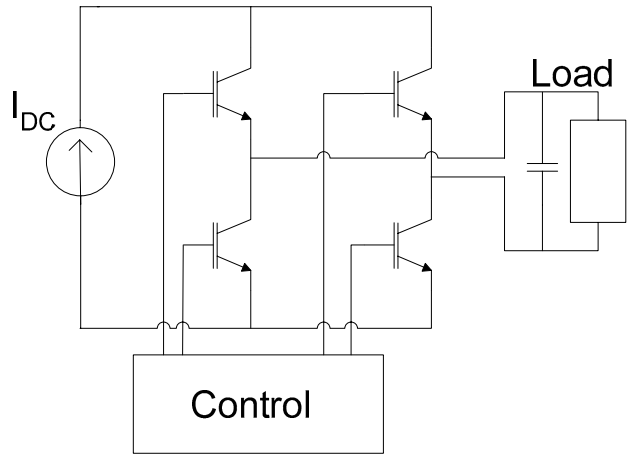

Fig. 1-4. Single-output current-sourced inverter topology

The CSI is the dual topology of the VSI. A VSI is supplied from a DC voltage, whereas a CSI is supplied from a DC current. The output of a VSI is a PWM-switched voltage, which must be low-pass filtered to achieve the desired output voltage waveform. The CSI's output is a PWM-switched current, which produces the desired voltage across an output filter capacitor. There are a number of advantages to using a CSI rather than a VSI. Several have previously been documented for FACTS converters [11][12][13] and medium- to high-voltage induction motor drives [14][15]. These benefits are also expected to be advantageous in split-phase generation:

- CSIs have built-in voltage boost capability, eliminating the need for a front-end DC/DC boost converter.
- Only a capacitor is required to filter the output, rather than an LC filter, because the output current is controlled directly. This reduces the filter components required and results in improved regulation of the output voltage.
- Since the DC current is regulated, usually using a large DC inductor, the CSI provides automatic short-circuit and over-current protection.
- The output capacitor limits the dv/dt values seen by the inverter's switches. This and the over-current protection both tend to improve inverter reliability.

- The CSI facilitates grid connection. Since the grid provides a strong voltage, the power transferred can be controlled directly by controlling the output current from the inverter. This is essentially equivalent to the operation of a CSI-based STATCOM [12][13]. Using a VSI, the power transferred to the grid must be controlled indirectly, by varying the voltages across the output filter inductors.

However, there are also a number of obstacles that have prevented the use of CSIs in distributed generation to date:

- The current-sourced inverter must be supplied with a DC current input. Therefore, while a DC/DC boost converter is not necessary, a front-end circuit is required to produce this DC current from a DC voltage source.

- Voltage-sourced inverters require switching elements that are unipolar in voltage and bidirectional in current. In other words, current must be able to flow in either direction, and only positive polarity voltage must be blocked. As the dual of the VSI, the CSI requires switching elements that are bipolar in voltage and unidirectional in current. They should be able to block voltage of either polarity, and current should flow in the forward direction only. This precludes the use of standard IGBTs, the most common type of switch used in medium-power voltage-sourced inverters, due to a lack of reverse voltage blocking capability. The alternatives to date have been less easily-controlled switches, such as GTOs, or the addition of series diodes to block reverse voltage, resulting in increased conduction losses. Recently, however, switches have been developed that combine the controllability of IGBTs with reverse voltage blocking capability, at the cost of a slight decrease in the switching speed. These are known as reverse-blocking non-punch-through, or RB-NPT, IGBTs [16].

- Existing current-sourced inverter topologies lack sufficient energy storage for use in distributed generation. During turn-on transients in the connected loads, the power requirements from the inverter may be several times those at steady-state. The energy storage device in a current-sourced inverter is a DC inductor, which cannot cost-effectively store energy on the same scale as a DC capacitor.

Therefore, without modification, this topology will be less able than a voltage-sourced inverter to withstand power transients at its outputs.

- There is no existing implementation of a current-sourced inverter producing split-phase outputs in literature. The third-leg approach for producing split-phase outputs from a voltage-sourced inverter could be adapted to suit current-sourced inverters. However, a new control technique will have to be developed, integrating all six switches into a single switching scheme in order to continuously provide a path for the DC current. Also, to maintain constant-RMS output voltages, the inverter control will have to vary based on the load impedances.

1.2 CONTRIBUTIONS

Through the completion of the research described in this thesis, the following contributions were made:

1. Development of a topology and control algorithm to create an artificial current source for use with current-sourced inverters. This includes an energy storage technique that allows the DC current to be held constant in the presence of large power transients at the inverter's output(s).

2. Modification of an existing control algorithm for three-phase current-sourced inverters, to allow its use with unbalanced or split-phase loads. This algorithm successfully balances the output voltages under severely unbalanced loading conditions, as well as with inductive and nonlinear loads.

3. Additions to the existing three-phase algorithm include calculation of control signals based on split-phase output voltage feedback, and management of shoot-through current to equalize conduction losses among the inverter switches under split-phase loading conditions.

4. Construction of a laboratory prototype current source preconditioning circuit and split-phase current-sourced inverter, based on existing current-sourced converter modules and measurement circuitry.

1.3 THESIS OUTLINE

The goals of this thesis are to overcome the main challenges in the adoption of CSIs listed above, and to design a viable split-phase distributed generation system based on a low-voltage DC source and a current-sourced inverter. The thesis is composed of the following five chapters:

Chapter 1 reviews the existing technologies and literature, and outlines the advantages and obstacles faced in designing a current-sourced inverter-based distributed generation system. It then provides an outline of the subsequent chapters and summarizes the contributions of the thesis.

Chapter 2 describes the method of generating a constant DC current from a DC input voltage. An analysis is given of how to calculate the DC current reference level to achieve the desired performance. In addition, a novel topology and control scheme is developed to enhance the energy storage capabilities of the current-sourced inverter, allowing the DC current to be held constant even in the presence of large power transients at the inverter's output(s).

Chapter 3 presents two switching algorithms to produce equal split-phase output voltages using a three-leg current-sourced inverter. The algorithms use different methods to successfully generate balanced, split-phase output voltages under highly unbalanced loading conditions, while minimizing switching losses and high-frequency voltage ripple at the outputs.

The designs in Chapters 2 and 3 are verified using simulation and experimental results.

Chapter 4 describes the hardware and software of the experimental setup in greater detail, outlining several challenges encountered and the steps taken to resolve them. It also lists some practical techniques used to improve the performance of the control hardware.

Finally, Chapter 5 summarizes the results and contributions, and outlines potential future research.

CHAPTER 2

VOLTAGE SOURCE-TO-CURRENT SOURCE TOPOLOGY

2.1 INTRODUCTION

In order to produce a constant-RMS AC voltage using a current-sourced inverter, a DC input current is required. To use a current-sourced inverter for distributed generation, it is therefore necessary to convert the available low DC voltage to a DC current. The desired value of that DC current must also be determined. Finally, the current must be held constant under a wide range of inverter loading conditions. The required block is labelled *V-to-I* in Fig. 2-1. The combination of this block and the supply voltage source must be made equivalent to a current source. It is assumed that the connected current-sourced inverter is using pulse-width modulation (PWM) [17] to produce a sinusoidal output voltage.

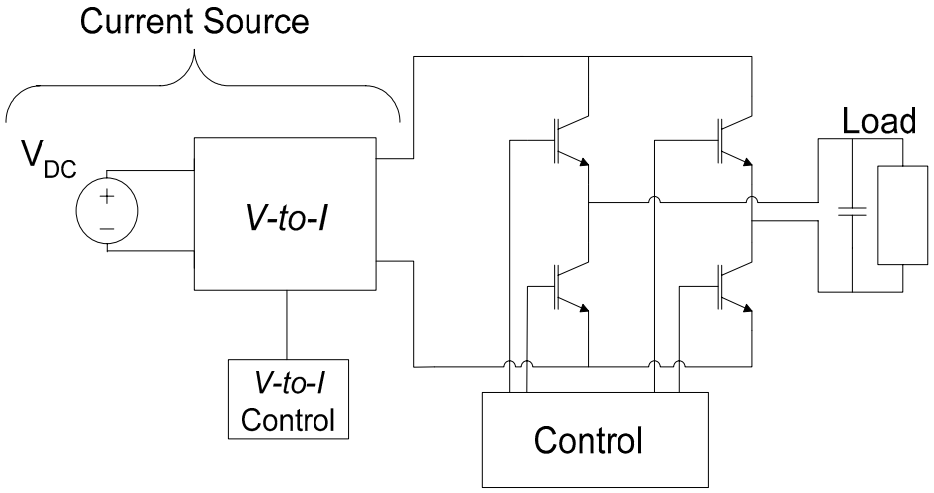

Fig. 2-1. Current-sourced inverter with voltage source-to-current source conversion block

2.2 OVERVIEW

This chapter begins with a brief review of current-sourced inverter technology, in section 2.3. Next, a basic circuit is presented in section 2.4 to produce a DC current from a DC voltage source, under relatively static loading conditions. Section 2.4 also covers the effects of ordering the DC current to various levels. Sections 2.5 and 2.6 build upon the earlier results, adding enhanced energy storage and a dynamic current reference level, to handle varying loads. Experimental results for this circuit are given in section 2.7. Finally, an optimized control algorithm is demonstrated in section 2.8.

2.3 REVIEW OF CURRENT-SOURCED INVERTER OPERATION

A current-sourced inverter controls its output voltage by alternately directing its DC input current into an output filter capacitor in the forward and reverse directions. The output capacitor is charged when current is injected into its positively-charged rail and discharged when current is injected into its negatively-charged rail. (Note that the positively-charged rail alternates, since the output is AC.) Periods when the capacitor is being actively charged or discharged will be referred to as *active states*. There is a third mode of operation, in which the DC current circulates through the two switches in a single leg of the inverter and does not enter the output capacitor in either direction. This is known as a *shoot-through*

state. When the inverter is in a shoot-through state, the output capacitor will slowly discharge through the connected load.

2.4 DC CURRENT CONTROL

It was realized in [18] that when the DC current for a closed-loop controlled CSI was supplied using only a DC voltage source and an inductor, the current in the inductor tended to rise uncontrollably. A circuit composed of a switch S and a diode D (marked *V-to-I* in Fig. 2-2) was therefore used to limit the DC current to a set value. The circuit is essentially a buck DC-DC converter. When the DC current is lower than the reference, the switch is turned on. This supplies energy to the DC inductor, causing the DC current to rise. When the DC current is higher than the reference, the switch is turned off, causing the inductor current to circulate through the freewheeling diode. This results in a loss of stored energy in the DC inductor and a drop in the DC current. The DC current can therefore be regulated by controlling the duty ratio of the switch in a closed loop.

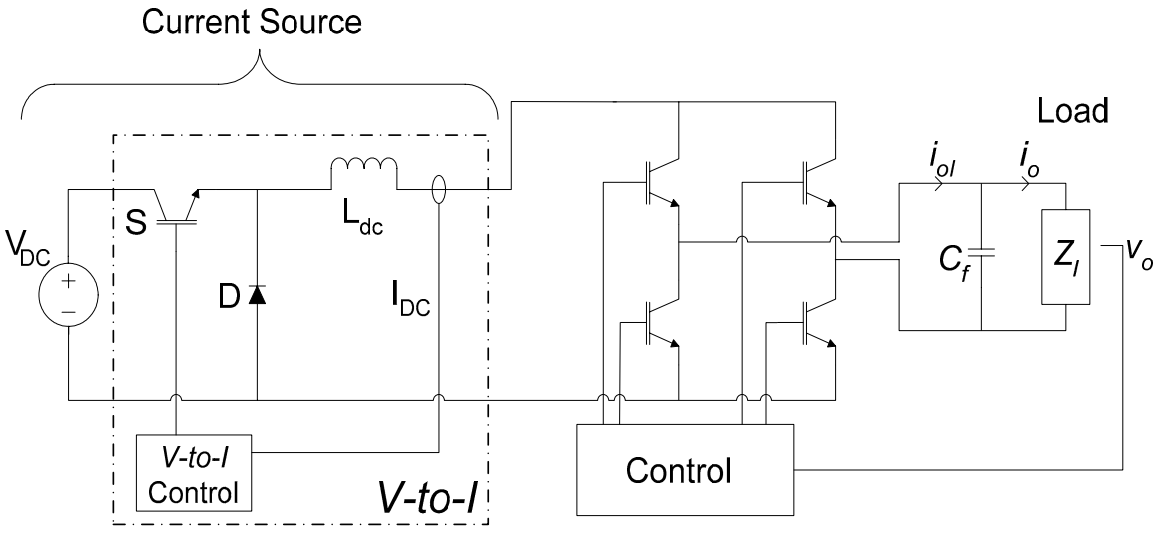

Fig. 2-2. Implementation of voltage source-to-current source conversion circuit

As implemented in [18], however, a large DC current ripple was experienced with this method. This can be understood by examining the effect of the reflected voltage at the input terminals of the current-sourced inverter (to the right of the inductor, L_{dc}). This switched voltage is dependent on the output voltage of the inverter and on its switching action. The DC plus low-frequency (120-Hz) component of the reflected voltage is equal to the output

voltage times the modulating signal of the inverter. (From this point forward, the 'reflected voltage' will refer to this DC plus low-frequency component only.) For a single-output inverter with an assumed constant DC current, the modulating signal is proportional to the output current. Therefore, the reflected voltage is proportional to output voltage times output current, i.e. instantaneous output power. Fig. 2-3 shows the resulting reflected voltage when the circuit in Fig. 2-2 is run under the following conditions (Case 1):

- DC Supply Voltage: 48V
- AC Voltage: 120V rms
- DC Inductor: 5mH
- AC Filter Capacitor: 15μF

These specifications will be used for all simulations in this chapter, unless otherwise noted. Case 1 also uses the following values for the DC current and load:

- DC Current: 18A
- Load: 400W (36-Ω resistor)

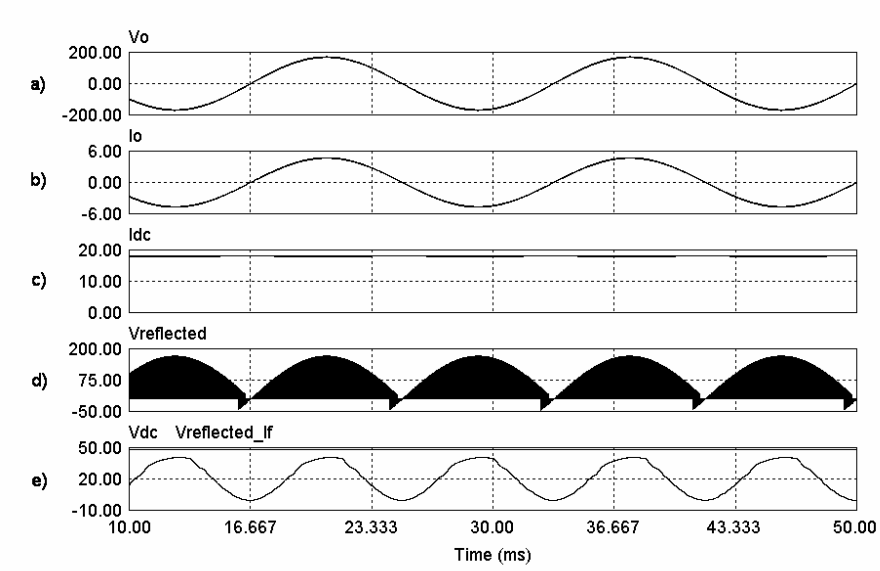

Fig. 2-3. Case 1: Reflected voltage under ideal operating conditions
a) Output voltage (V)
b) Output current (A)
c) DC Current (A)
d) Actual reflected voltage (switched) (V)
e) DC plus low-frequency components of reflected voltage compared to DC supply voltage (V)

Because the load is resistive, v_o and i_o are in phase. The impedance of C_f at the fundamental frequency should be much larger than that of Z_l; therefore, the fundamental component of i_{oI}, the switched current output from the inverter (Fig. 2-2), should also be nearly in phase with v_o. The resulting reflected voltage is a positively DC-shifted 120-Hz sine wave. If the peak of this voltage is higher than V_{DC}, the net voltage across the inductor at the peak will remain negative even with the switch on, and the DC current will fall below its reference. This is demonstrated in Case 2 (Fig. 2-4), where the DC current reference is 15A. This lower reference current results in a higher modulation index and a higher reflected voltage. As the low-frequency reflected voltage exceeds the supply voltage, the DC current dips lower. When the reflected voltage falls back below the supply voltage, the DC current is able to recover.

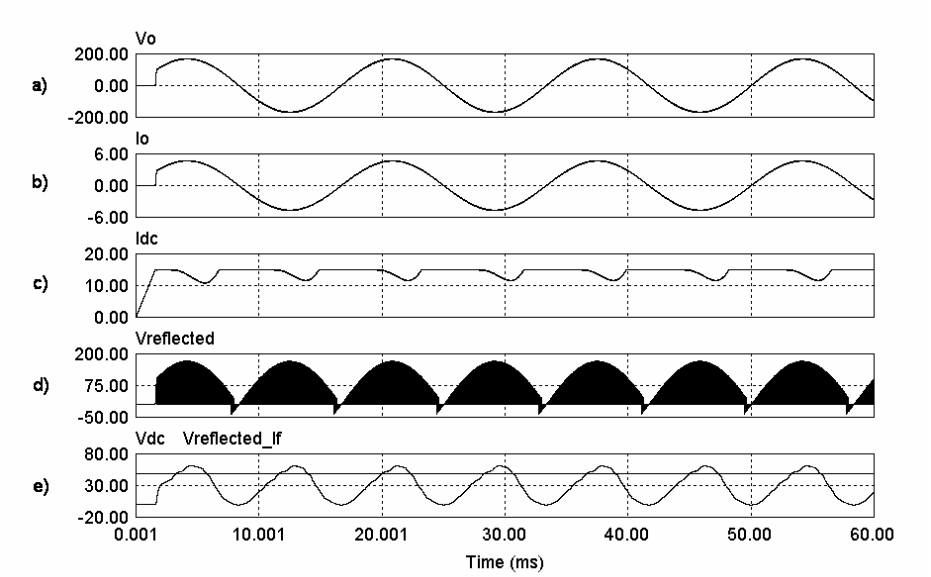

Fig. 2-4. Case 2: Effect of reflected voltage exceeding supply voltage
a) Output voltage (V)
b) Output current (A)
c) DC Current (A)
d) Actual reflected voltage (switched) (V)
e) DC plus low-frequency components of reflected voltage compared to DC supply voltage (V)

If the current falls too far, however, it may not be possible to recover. As the current falls, the modulation index rises to maintain the output voltage. This increases the reflected voltage, further decreasing the DC current. The result can be a complete loss of stored energy in the inductor and a failure in operation. This is seen in Case 3 (Fig. 2-5), where the current reference setting is 14A.

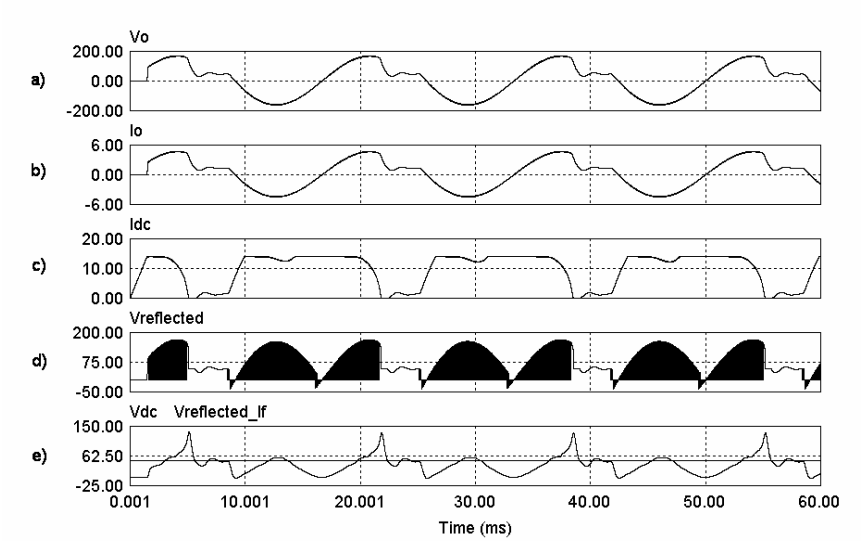

Fig. 2-5. Case 3: Insufficient DC current resulting in system failure
a) Output voltage (V)
b) Output current (A)
c) DC Current (A)
d) Actual reflected voltage (switched) (V)
e) DC plus low-frequency components of reflected voltage compared to DC supply voltage (V)

However, this failure can be prevented by maintaining a sufficiently high initial DC current. Just as a drop in the DC current causes the inverter's modulation index to increase, a higher DC current results in a lower modulation index and a reduction in the reflected voltage. Therefore, if the DC current is kept sufficiently high, the peak value of the 120-Hz reflected voltage will be lower than the supply voltage, and the current level will be sustainable. This circuit can then approximate an ideal current source, as was seen in Case 1.

2.4.1 IDEAL DC CURRENT

The exact DC current level required to maintain the peak reflected voltage below the supply voltage can be calculated. The goal is to maintain the supply voltage, V_{DC}, higher than the peak of the reflected voltage, $v_{reflected}$, i.e.,

$$V_{DC} > v_{reflected.} \tag{2-1}$$

Also, one can write

$$v_{reflected} = v_o * m, \tag{2-2}$$

where v_o is the AC output voltage, and m is the modulating signal of the PWM inverter. Assuming the effect of the filter capacitor is negligible,

$$m = \frac{i_o}{\mathrm{I_{DC}}}. \tag{2-3}$$

By substituting (2-2) and (2-3) into (2-1), the following relationship is derived:

$$\mathrm{V_{DC}} > \frac{v_o i_o}{\mathrm{I_{DC}}} \tag{2-4}$$

Note that this is equivalent to

$$\mathrm{V_{DC}I_{DC}} > v_o i_o . \tag{2-5}$$

It is in fact possible to restate this entire reflected voltage problem as one of power balance. If the *instantaneous* output power, $v_o i_o$, exceeds the available input power, $\mathrm{V_{DC}I_{DC}}$, energy will be removed from the system. (The *available* input power is the input power when the switch S is turned on. When the switch is off, the input power is zero.) The energy storage component in this system is the DC inductor. Therefore, as energy is removed, the DC current decreases, as was seen. The following analysis will continue in terms of reflected voltage; however, the same results can be achieved through power balance by simply moving $\mathrm{V_{DC}}$ and $\mathrm{I_{DC}}$ to the same side of the inequalities.

From (2-4), the supply voltage must be greater than the peak of the reflected voltage. Assuming the load is resistive, and so output voltage and current are in phase, this gives

$$\mathrm{V_{DC}} > \frac{\sqrt{2}\mathrm{V_{O,rms}}\sqrt{2}\mathrm{I_{O,rms}}}{\mathrm{I_{DC}}} = \frac{2\mathrm{P_O}}{\mathrm{I_{DC}}}. \tag{2-6}$$

The minimum current required to satisfy this inequality is defined as $\mathrm{I_{DC,ideal}}$, and is given by

$$\mathrm{I_{DC,ideal}} \cong \frac{2\mathrm{P_O}}{\mathrm{V_{DC}}}, \tag{2-7}$$

where the approximately equal to sign is used because the effect of the output capacitor is being neglected. For the test conditions used in Cases 1 to 3 above, this results in $I_{DC,ideal}$ = 16.67A, which is below the level used in Case 1 and above that used in Case 2, as expected.

The above analysis can be expanded to include inductive loads. Also, the effect of the output filter capacitor can be included in the calculations by considering it to be part of the load. To do so, i_o in (2-4) is replaced by the low-frequency component of the switched output current from the inverter, i_{oI} (shown in Fig. 2-2):

$$V_{DC} > \frac{v_o i_{oI,lf}}{I_{DC}}, \tag{2-8}$$

where *lf* denotes the low-frequency component. $i_{oI,lf}$ can be expressed in terms of v_o through the combined impedance of load and capacitor:

$$\vec{Z}_O = \left|\vec{Z}_O\right| \angle \vec{Z}_O = \vec{Z}_L \parallel \vec{X}_C \tag{2-9}$$

The instantaneous reflected voltage is then given by

$$v_{reflected} = \frac{v_o i_{oI,lf}}{I_{DC}} = \frac{\sqrt{2}V_{O,rms}\sin(\omega t)\left(\frac{\sqrt{2}V_{O,rms}}{\left|\vec{Z}_O\right|}\sin\left(\omega t - \angle \vec{Z}_O\right)\right)}{I_{DC}}, \tag{2-10}$$

which has a peak value of

$$V_{reflected,\,peak} = \frac{2V_{O,rms}^2 \cos^2\left(\frac{\angle \vec{Z}_O}{2}\right)}{\left|\vec{Z}_O\right| I_{DC}}. \tag{2-11}$$

Again, V_{DC} must be greater than $V_{reflected,peak}$. Therefore, substituting V_{DC} for $V_{reflected,peak}$ and solving for I_{DC} gives $I_{DC,ideal}$:

$$I_{DC} > \frac{2V_{O,rms}^2 \cos^2\left(\frac{\angle \vec{Z}_O}{2}\right)}{\left|\vec{Z}_O\right| V_{DC}} \equiv I_{DC,ideal} \tag{2-12}$$

As before, this is equivalent to maintaining the input power greater than the peak of the instantaneous output power.

Given a 15-μF filter capacitor, the result is $I_{DC,ideal}$ = 16.84A. Comparing this to the earlier result of 16.67A from equation (2-7), it is clear that neglecting the effect of the capacitor was reasonable.

2.4.2 REQUIRED AND MINIMUM DC CURRENT

There is another DC current threshold that is of interest: the lowest DC current reference level for which steady-state operation can be maintained. If the reference is set below this level, the current will fall below the reference and not recover, as in Case 3 above. This minimum reference level is the level at which the average real input power is equal to the real output power. Therefore, for steady state operation, the following inequality must be maintained:

$$V_{DC}\bar{I}_{DC} > \frac{V_{O,rms}^2}{\left|\vec{Z}_O\right|}\cos\left(\angle\vec{Z}_O\right) = P_O \tag{2-13}$$

This is equivalent to maintaining the supply voltage above the average reflected voltage:

$$V_{DC} > \frac{P_O}{\bar{I}_{DC}} = \bar{v}_{reflected} \tag{2-14}$$

The average DC current must be used here because once the reflected voltage exceeds the supply voltage, the DC current will not be constant. The threshold resulting from solving for $\bar{I}_{DC}$ is defined as $I_{DC,minimum}$, and is given by

$$\bar{I}_{DC} > \frac{V_{O,rms}^2}{V_{DC}\left|\vec{Z}_O\right|}\cos\left(\angle\vec{Z}_O\right) \equiv I_{DC,minimum}\,. \tag{2-15}$$

This is referred to as $I_{DC,minimum}$ because, given an infinite DC inductor, and therefore a constant DC current, this is the minimum current reference that would be required to maintain steady-state operation. Returning to the example above, $I_{DC,minimum}$ = 8.33A.

Clearly this reference level is insufficient in practical circumstances, as failure was seen in Case 3 (Fig. 2-5), with a reference current of 14A.

When the current is allowed to vary, there is no closed-form solution for the current reference that will result in an average DC current of $I_{DC,minimum}$, as required by (2-15). This threshold, denoted as $I_{DC,required}$, can be found through simulation, using a process of elimination. In the above example, $I_{DC,required}$ is already known to be between 12A and 14A from test cases 2 and 3. However, this method is slow and inefficient. The low-frequency variations in the current can instead be calculated using an ordinary differential equation.

$$\dot{I}_{DC} = \frac{\left(V_{DC} - v_{reflected}\right)}{L_{DC}} = \frac{\left(V_{DC} - \frac{2V_{O,rms}^2}{\left|\bar{Z}_O\right| I_{DC}} \sin(\omega t)\sin\left(\omega t - \angle\bar{Z}_O\right)\right)}{L_{DC}} \tag{2-16}$$

A Matlab script was written to test the sufficiency of a given DC current reference level, I_{REF}, using this formula. The formula is only valid when $I_{DC} < I_{REF}$ because when I_{DC} exceeds I_{REF}, the switch S is turned off to prevent it from rising further. Therefore, the first step is to find the angle ωt_0 at which $\dot{I}_{DC}$ becomes negative, for $I_{DC}=I_{REF}$. This is done through simple iteration, although a more advanced algorithm for finding zero-crossings could be used.

Once this starting angle is found, it is used as the initial point for Matlab's ODE solver, *ode45*. The solution of the differential equation given in (2-16) is followed until one of the following four exit conditions is reached.

1. Current reference is sufficient: I_{DC} returns to the reference level, I_{REF}.
2. Current reference is not sufficient: The DC current falls below the required output current:

$$I_{DC} < \frac{\sqrt{2}V_{O,rms}}{\left|\bar{Z}_O\right|} \sin\left(\omega t - \angle\bar{Z}_O\right) = i_{oI,lf} \tag{2-17}$$

At this level, the inverter's modulating signal will be at its maximum value. If the DC current falls further, the inverter will be unable to maintain the output voltage.

3. Current reference is not sufficient: After one complete period ($\omega t = \omega t_0 + \pi$), I_{DC} is still below the reference level, I_{REF}. If the current cannot recover within one complete period, it will continue to drop in subsequent cycles, until condition 2 is reached.

4. Current reference is not sufficient: I_{DC} reaches a local maximum below the reference level. If the current reaches a local maximum and begins dropping again, it is not necessary to continue solving to the end of the period because it is known that eventually condition 2 will be reached.

Exit conditions 1 and 2 are sufficient to achieve the desired results; however, 3 and 4 prevent unnecessary calculations, improving execution time.

Fig. 2-6 shows the results of this script for Case 2 and Case 3 above. These results are consistent with the simulation results in Fig. 2-4 and Fig. 2-5. Through further iterations of the script, the approximate required current is found:

$$I_{DC,required} \cong 14.6\text{A}, \tag{2-18}$$

which is between 14A and 15A, as expected.

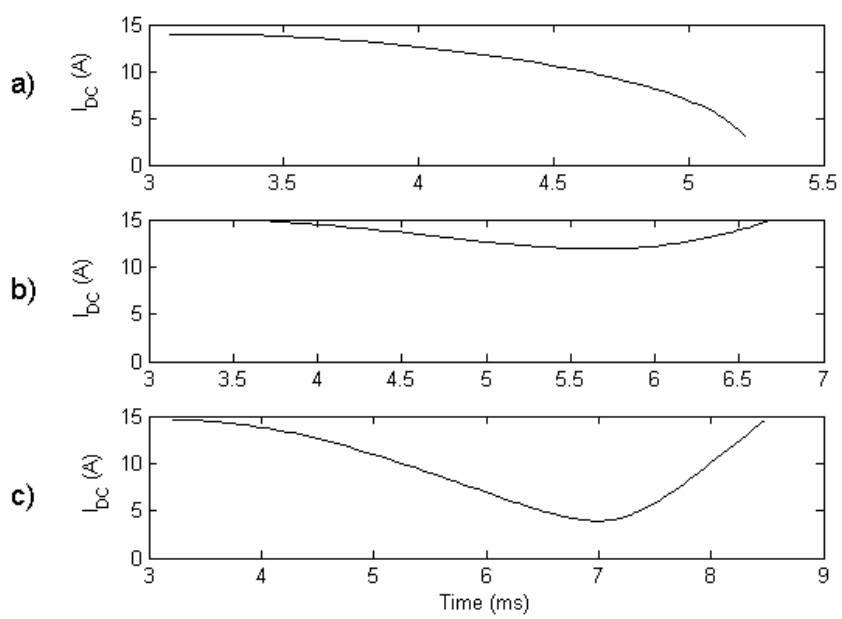

Fig. 2-6. Simulated variations in DC current using Matlab ODE-solver script
a) Current reference level of 14A: current cannot be maintained.
b) Current reference level of 15A: current can be maintained.
c) Current reference level of 14.6A = $I_{DC,required}$: minimum level at which current can be maintained.

A wrapper script was written to prepare a matrix of required current reference levels over the entire range of possible loads. This matrix can be calculated offline, and then used to dynamically set the DC current reference level during inverter operation, based on the measured load. If step changes in loading are possible, the current reference must be sufficient to maintain operation not only under current conditions, but also given the new load following a step change.

2.5 ADDITIONAL ENERGY STORAGE

The current source topology described in section 2.2 is capable of producing a constant current if the current reference is set greater than or equal to $I_{DC,ideal}$, or a sustainable current with DC and 120Hz components if the reference is set greater than or equal to $I_{DC,required}$. However, as well as the existent load, the current reference must be set to accommodate the worst-case step change in load, since it is no longer possible to increase the DC current level once the output power exceeds the available input power. Keeping a high DC current results

in larger losses and increased component stresses. Moreover, most loads do not exhibit step changes, but rather have a transient power spike during turn-on. These transients can be as high as ten times the steady-state power requirements for a period of several milliseconds (in the case of a light bulb), or two to three times the steady-state power for up to several seconds (in the case of an induction motor [19]). It is not feasible for the DC current reference to be set high enough to accommodate these transient loads. One alternative would be to store sufficient energy in the DC inductor to supply the power during these turn-on transients without the current dropping below the $I_{DC,required}$ threshold. However, this is not feasible either, given a practical inductor size. For example, a light bulb turn-on transient of 1000W for 10ms would require on the order of 10J of energy. To provide this energy from a DC inductor with a current of 20A, without the current falling below 15A, a 114mH inductor would be required. For a motor turn-on transient, the requirement would be much higher. If this current source topology is to function with transient power spikes, an additional energy storage technique is required.

2.5.1 SUPPLEMENTAL ENERGY-STORAGE CIRCUIT

Additional energy storage was introduced in the circuit of Fig. 2-2, as shown in Fig. 2-7. A high power draw at the output of the inverter, such as during a turn-on transient, results in a high reflected voltage at the inverter's input terminals, at the right side of the DC inductor. Therefore, in order to maintain the current in the DC inductor during these events, it is necessary to apply an equally high voltage to its left side. This is done by turning on the switch S_C. The capacitor is kept charged to a voltage above the peak of the output voltage. From (2-2), the maximum reflected voltage is equal to the output voltage, and occurs when the modulating signal, m, is equal to 1. Therefore, if the capacitor voltage, V_C, is kept higher than the peak of v_o, it will be possible to maintain the DC current under any loading condition.

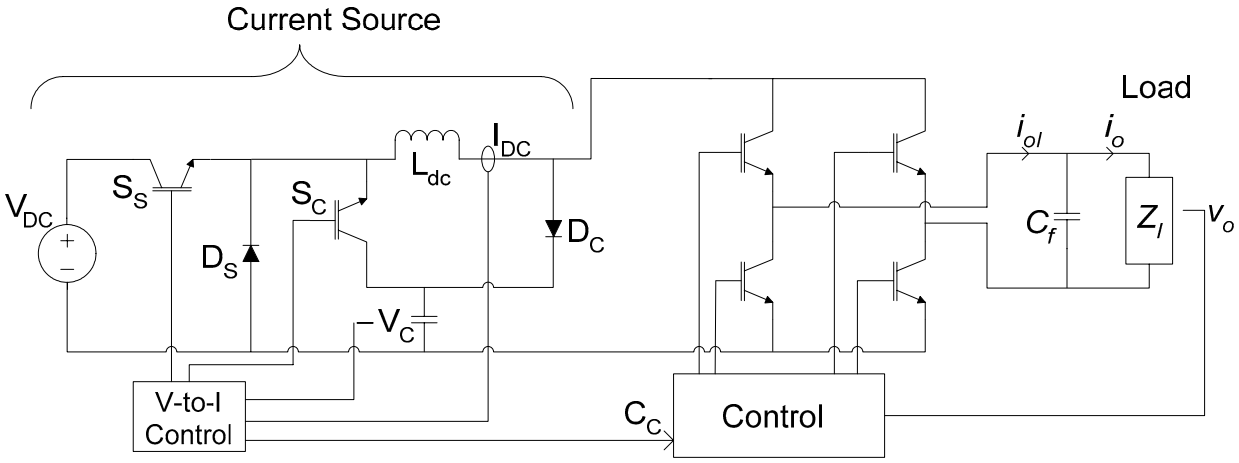

Fig. 2-7. Current-sourced inverter with voltage source-to-current source conversion circuit and supplemental energy storage

The energy-storage capacitor is charged through the diode D_C. Another reason for keeping $V_C > \max(v_o)$ is that a diode can be used in this position rather than a switch. During normal inverter operation, the diode will always be reverse biased, and will therefore not conduct. The capacitor can then be charged by opening the current path through the inverter, forcing the DC current into the diode path. Since the switch S_C is also off during charging, the DC current flows into the capacitor. This charging can only occur during shoot-through states, since interrupting the current through the inverter during an active state would affect the output current, and thereby the output voltage. During capacitor charging, the circuit behaves identically to a boost converter. A standard boost converter is shown in Fig. 2-8 for comparison. The entire inverter block in Fig. 2-7 corresponds to the switch S in Fig. 2-8. The diode D_C corresponds to the diode D. The capacitor voltage, V_C, corresponds to the output voltage of the boost converter, V_O. While the circuit is operating as a boost converter to charge the capacitor, the switch S_S remains closed and the switch S_C remains open. There is no theoretical limit to the capacitor voltage; although, to reduce switching losses, it is advantageous not to charge it higher than necessary.

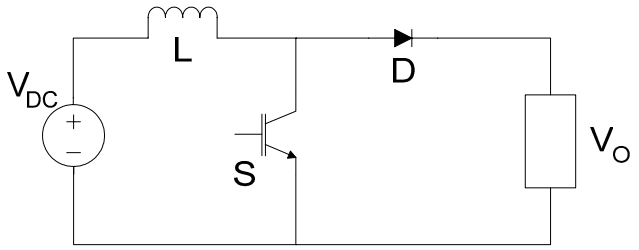

Fig. 2-8. Basic boost converter

The energy required to supply a transient power surge is equal to the power level of the surge times its length in time:

$$E_T = P_T * t_T \tag{2-19}$$

The available stored energy in the capacitor is

$$E_C = \frac{1}{2} C\left(V_C{}^2 - v_{o,peak}{}^2\right) \tag{2-20}$$

because the capacitor voltage cannot be allowed to fall below the peak output voltage. This supplemental energy-storage circuit can therefore supply the required power to any transient with energy $E_T<E_C$. Once the transient power spike has ended, the capacitor can be recharged during shoot-through states. The operation of this circuit is demonstrated through simulation in Fig. 2-9 and Fig. 2-10. The output power is 600W until time 0.06s, and then steps up to 1600W for approximately one cycle, before dropping back to 800W. This simulates the turn-on transient of a 200W incandescent light. For both tests, the DC current reference is 35A. Fig. 2-9 shows the results without the supplemental energy storage. When the spike in output power results in $I_{DC}<I_{DC,required}$, the DC current drops and is unable to recover. In Fig. 2-10, the effect of the additional energy-storage circuit is seen. Energy is taken from the capacitor to maintain the DC current level until the transient passes. The capacitor is then slowly recharged to its steady-state (constant) value. A 2.2-mF capacitor was used in this simulation. In order to supply larger transients, such as during turn-on of a motor, a larger capacitor or an ultracapacitor could be used.

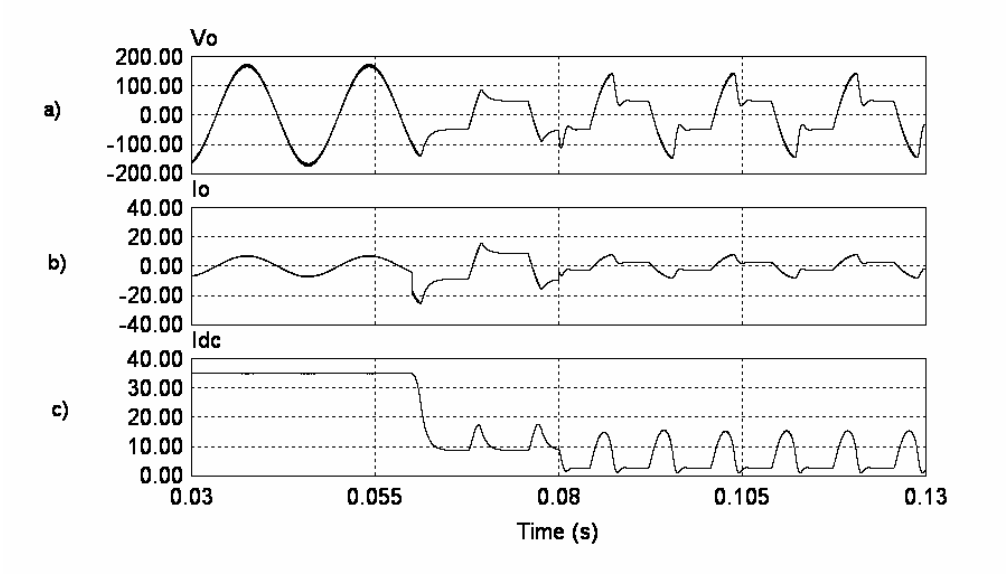

Fig. 2-9. Failure of Current-Sourced Inverter due to turn-on transient
a) Output (load) voltage (V) b) Output (load) current (A)
c) DC Current (A)

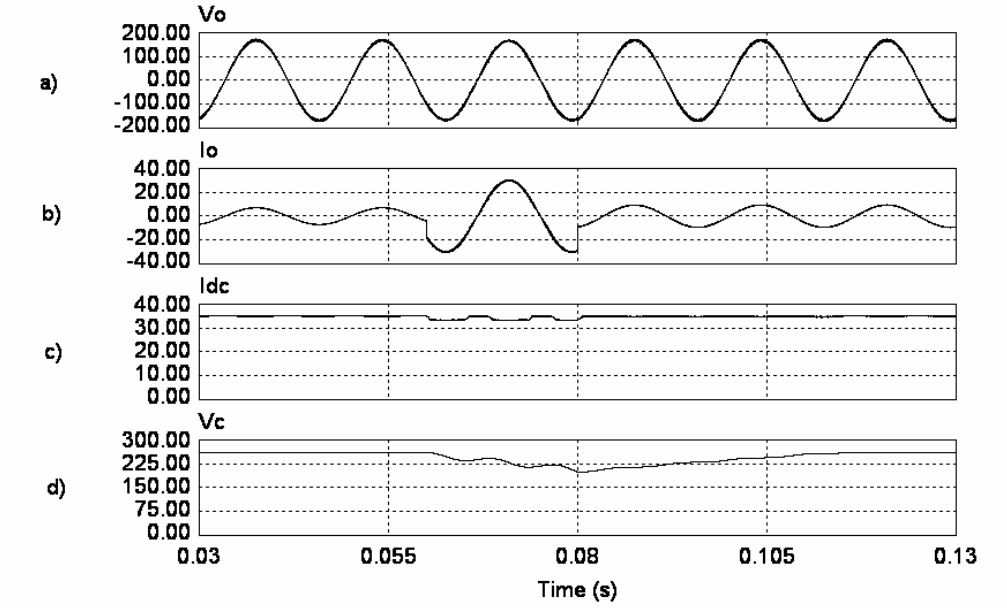

Fig. 2-10. Successful supply of 1800W turn-on transient, using supplemental energy-storage circuit
a) Output (load) voltage (V) b) Output (load) current (A)
c) DC Current (A) d) Capacitor Voltage (V)

2.5.2 STEADY-STATE OPERATION

As well as supplying transient power spikes, this supplemental energy-storage circuit can improve the steady-state operation of the inverter. In section 2.4, several thresholds for the DC current reference level were introduced. If the reference is set to at least $I_{DC,ideal}$, given in (2-12), the DC current can be held constant for a constant load. If the reference is set below $I_{DC,ideal}$, but above $I_{DC,required}$, steady-state operation can be maintained, but the DC current will exhibit cyclical 'dips' at 120Hz. Finally, $I_{DC,minimum}$ (2-15) is the theoretical minimum DC current for the input power to be at least equal to the output power. However, it is only valid if the DC current is held constant, which was not the case for the initial current source circuit described in section 2.4.

With the addition of the supplemental energy-storage circuit shown in Fig. 2-7, the DC current can in fact be held constant, regardless of its level, as long as the capacitor has sufficient stored energy. To maintain the energy in the capacitor at steady-state, it is simply necessary that the available input power to the circuit be at least equal to the output power:

$$V_{DC} I_{DC} \geq P_O , \tag{2-21}$$

or equivalently, $I_{DC} \geq I_{DC,minimum}$, as given by (2-15). The minimum DC current required for steady-state operation is reduced from $I_{DC,required}$ to $I_{DC,minimum}$. For the example given in section 2.4 above, this is a reduction from 14.6A to 8.33A, i.e., by 42.9%. The difference will be most pronounced when a small DC inductor is used.

In Fig. 2-11, a load power of 400W is drawn. While all other elements are unchanged from section 2.4, the additional energy storage allows this circuit to function with a DC current of only 10A. It failed with a current of 14A in Case 3 (Fig. 2-5) without the benefit of supplemental energy storage.

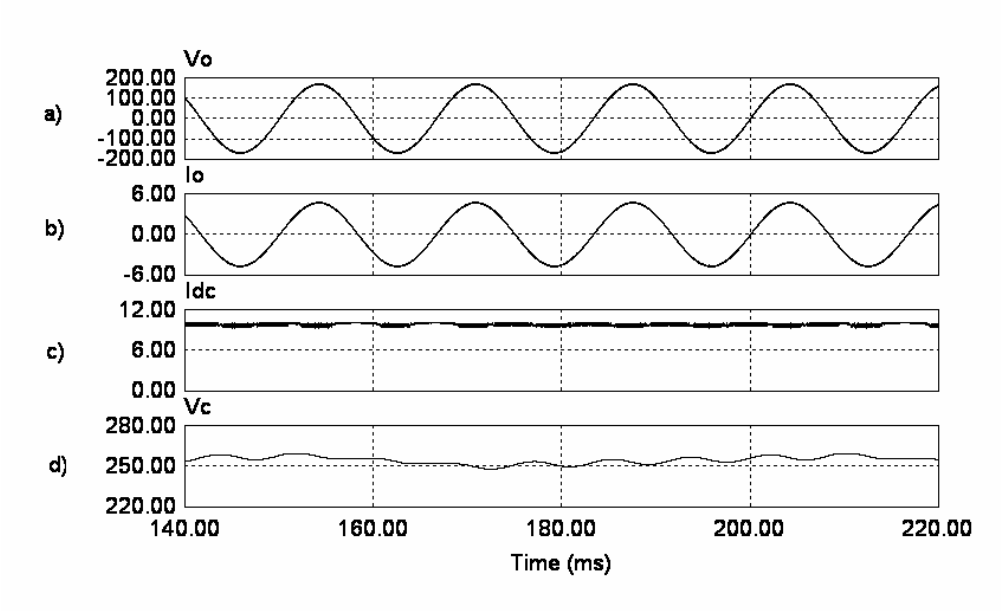

Fig. 2-11. Reduction of required DC current for steady-state operation due to addition of supplemental energy-storage circuit
a) Output (load) voltage (V) b) Output (load) current (A)
c) DC Current (A) d) Capacitor Voltage (V)

Reducing the operating DC current will result in lower conduction losses. Lower current and the elimination of 120Hz variations in the current result in lower stresses on the switching components. However, any switching (charging or discharging) of the energy-storage capacitor does increase switching losses, both in the six inverter switches and in the capacitor switch, S_C. Although the current being switched is lower, the voltage is higher. In addition, high-frequency variations in the DC current will be greater, as a large capacitor voltage, V_C, produces a large *di/dt* when applied across the DC inductor. (The precise switching action of the energy-storage circuit and its effect on the DC current at the switching frequency will be examined in section 2.5.3.) The benefit of lower DC current must be weighed against these drawbacks to determine whether operation of the capacitor energy-storage circuit at steady-state is desirable. Regardless of this choice, the circuit will allow recovery from turn-on transients or large step changes in loading, which otherwise would have resulted in failure. If it is only used during transients, no additional steady-state losses are incurred, since no components are added to the current path. The addition of this simple energy-storage circuit is therefore clearly beneficial.

2.5.3 METHOD OF CONTROL

The straight-forward control technique used for the tests presented thus far will be described in this section. Section 2.8 will present an alternative, optimized algorithm. Note that the results given in this chapter are intended to demonstrate the operation of the voltage source-to-current source preconditioning circuit, and do not cover the various possible inverter loading conditions. Chapter 3 investigates inverter control, and gives several test cases for various inverter loads.

The *V-to-I* control system controls the supply switch, the capacitor switch, and the charge-capacitor control signal, based on feedback of the DC current and the capacitor voltage, as was shown in Fig. 2-7. The primary goal of this system is to keep the DC current, I_{DC}, as close as possible to its reference level, I_{REF}. In the most basic implementation, the reference level is constant and pre-defined. The secondary goal is to hold the capacitor voltage near its reference level. As described in section 2.5.1, this level must be at least equal to the peak output voltage plus a sufficient amount to supply the necessary energy for the largest expected transient (2-20).

A digital control block is used both for the simulations throughout this chapter and for the experimental results of section 2.6. At each operation of the control block, the measured DC current and capacitor voltage are compared to a set of reference levels, as shown in Fig. 2-12. These levels are defined in Table 2-1 and Table 2-2.

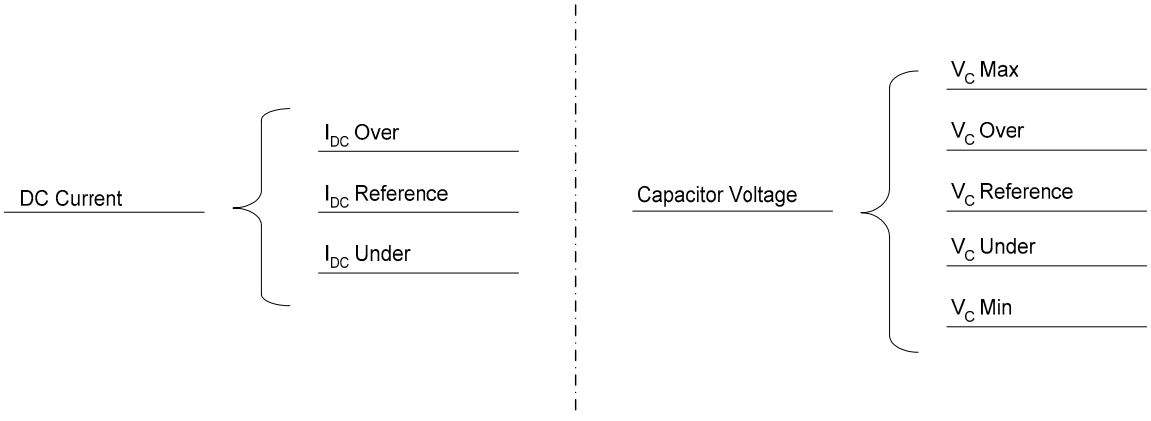

Fig. 2-12. Comparison of I_{DC} and V_C to reference levels

Table 2-1. DC Current Reference Levels

I_{DC} Over	Set slightly above I_{DC} Reference (1% to 4%). If I_{DC} rises above this level, it indicates that the reflected voltage is negative, and so the DC current is rising even with the supply switch, S_S, turned off.
I_{DC} Reference	The desired DC current level.
I_{DC} Under	Set 1% to 4% below I_{DC} Reference. If I_{DC} falls below this level, it indicates that the reflected voltage is greater than the supply voltage, and that the current is continuing to fall, even with the supply switch, S_S, turned on.

Table 2-2. Capacitor Voltage Reference Levels

V_C Max	The maximum safe capacitor voltage, based on component tolerances. The capacitor will never be charged beyond this level.
V_C Over	Set slightly above V_C Reference (4% to 5%). If V_C rises above this level, the controller will attempt to bring it back down to V_C Reference without disrupting the DC Current level.
V_C Reference	The desired capacitor voltage level.
V_C Under	Set slightly below V_C Reference (4% to 5%). If V_C falls below this level, the controller will attempt to bring it back up to V_C Reference without disrupting the DC Current level.
V_C Min	The minimum allowable capacitor voltage, equal to the peak output voltage plus a margin of error of several percent. The capacitor will never be discharged below this level, except at turn-on and shut-down.

As long as I_{DC} and V_C are between their respective 'Over' and 'Under' reference levels, the supplemental energy-storage circuit is not used. The supply switch, S_S, will simply be turned on if the DC current is below I_{DC} Reference, and turned off if it is above. Therefore, the maximum possible operating frequency of the switch is one half the frequency of the digital control block. However, the switch will only operate at this maximum frequency when the reflected voltage is equal to approximately half the supply voltage. When the reflected voltage is close to the supply voltage, the magnitude of the negative voltage across the DC inductor when the switch is off will exceed the magnitude of the positive voltage when the switch is on. I_{DC} will therefore fall faster than it rises, and so the switch will be left

on for several cycles for each cycle that it is turned off, as shown in Fig. 2-13. Likewise, when the reflected voltage is less than half the supply voltage, the supply switch must be off for several cycles for eachs one that it is on, as seen in Fig. 2-14. The circuit operation in these figures is as in Case I of section 2.4.

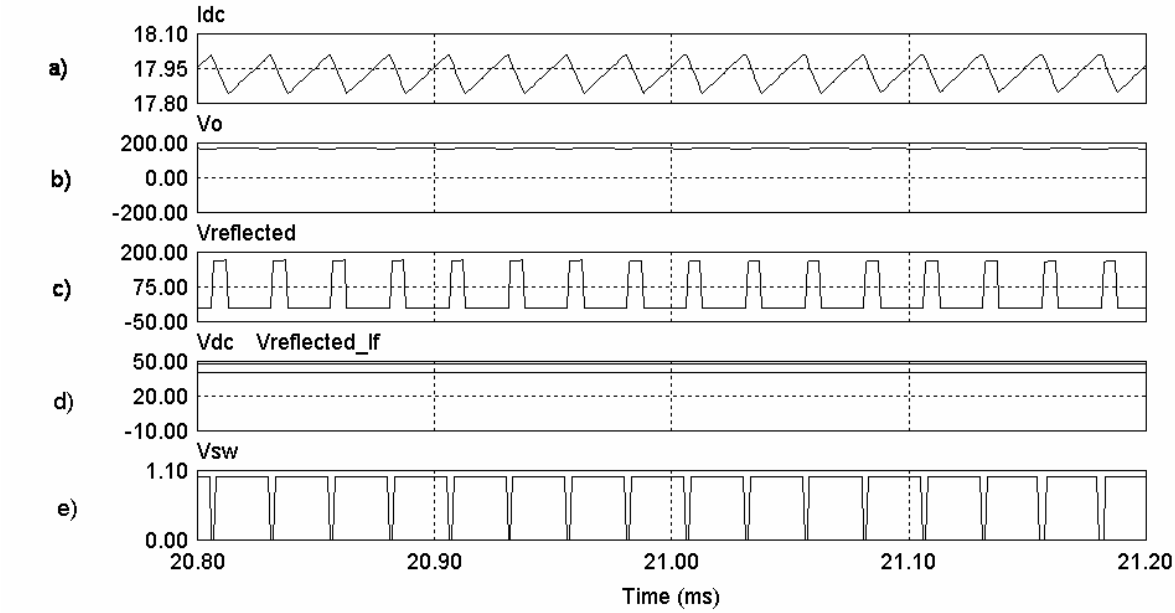

Fig. 2-13. Operation of supply switch when reflected voltage is nearly equal to supply voltage
a) DC Current (A)
b) Output voltage (V)
c) Reflected voltage (V)
d) Low frequency component of reflected voltage compared to supply voltage (V)
e) Gating signal to supply switch

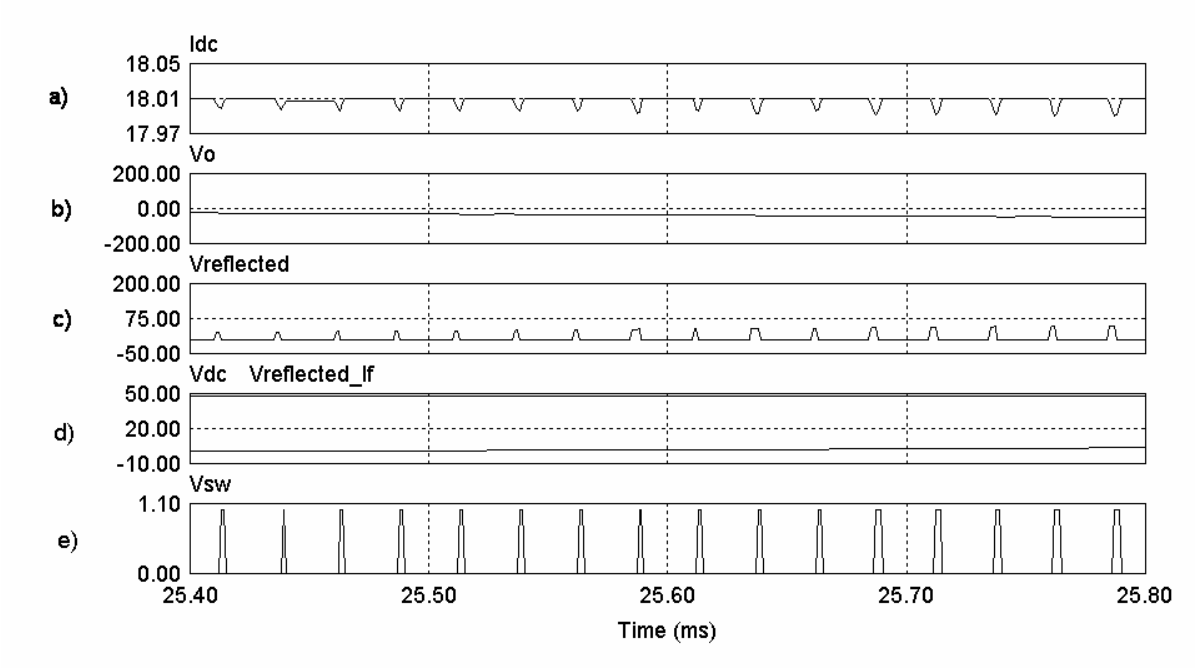

Fig. 2-14. Operation of supply switch when reflected voltage is approximately zero
a) DC Current (A)
b) Output voltage (V)
c) Reflected voltage (V)
d) Low frequency component of reflected voltage compared to supply voltage (V)
e) Gating signal to supply switch

If either I_{DC} or V_C moves outside of the range defined by its 'Over' and 'Under' reference values, they are controlled using either the capacitor switch, S_C, or the charge-capacitor control signal, C_C. When C_C is on during a shoot-through state of the current-sourced inverter, all inverter switches are turned off, forcing the DC current into the diode, D_C, path, and charging the energy-storage capacitor. This is the purpose of the control path shown between the *V-to-I* and inverter control blocks in Fig. 2-7.

Since it is not necessary to hold the capacitor voltage at a precise level, the signals specifying whether the capacitor voltage is under or over the reference range are latched. No attempt is made to correct the capacitor voltage until it reaches the V_C Over or V_C Under reference level. At that point, the respective V_C High or V_C Low signal is set to *true* until the voltage is returned to its ideal level. The control signals for the two switches and for charging of the capacitor are set as follows:

$$S_S = ((I_{DC}<I_{REF}) \text{ AND NOT}(V_C\_High)) \quad OR \quad ((I_{DC}<I_{DC}\_Over) \text{ AND } (V_C\_Low)) \qquad (2\text{-}22)$$

$$S_C = ((I_{DC}<I_{DC}\_Under) \text{ AND } (V_C > V_C\_Min)) \quad OR \quad ((I_{DC}<I_{REF}) \text{ AND } (V_C\_High)) \qquad (2\text{-}23)$$

$$C_C = ((I_{DC}>I_{DC}\_Over) \text{ AND } (V_C < V_C\_Max)) \quad OR \quad ((I_{DC}>I_{REF}) \text{ AND } (V_C\_Low)) \qquad (2\text{-}24)$$

The supply switch is turned on whenever energy needs to be added to the system. This is evidenced by one of I_{DC} and V_C being below its desired level while the other is not above its range. The capacitor switch is turned on when the DC current is too low or the capacitor voltage is too high. However, the current takes precedence, so the switch will never be turned on if the DC current is above its reference level. Likewise, the charge-capacitor control signal is set high when the DC current is too high or the capacitor voltage is too low, as long as the DC current is at least at its reference level. At steady-state, if the DC current reference level is set below $I_{DC,required}$, as described in section 2.4.2, these controls will result in periodic charging and discharging of the capacitor. When the reflected voltage rises above the supply voltage (the instantaneous power exceeds the input power), the capacitor switch is turned on when necessary to keep $I_{DC}>I_{DC}\_Under$. For each control cycle when the switch is on, the capacitor voltage is reduced slightly. Once the reflected voltage drops below the supply voltage, the DC current will return to its reference level. Each time the current exceeds its reference while the capacitor voltage is still low, the charge-capacitor signal will go high, and the capacitor will be charged during inverter shoot-through states. Assuming the DC current reference is greater than $I_{DC,minimum}$ (2-15), and so steady-state operation is sustainable, the capacitor voltage will return to its original level by the end of the 120-Hz cycle.

Fig. 2-15 shows control signals for the test given in Fig. 2-10. Because the DC current is very near to $I_{DC,minimum}$, the supply switch remains on a majority of the time. The capacitor switch is used periodically, as expected, whenever the instantaneous output power exceeds the supplied power, or equivalently, the 120Hz reflected voltage exceeds the supply voltage. At points in the cycle when the instantaneous power draw and reflected voltage are low, and the DC current is able to reach its reference level, the capacitor can be recharged. If the capacitor voltage is not low, the supply switch is turned off instead.

Fig. 2-16 shows a small time-slice of the previous figure, so that the switching action can be seen clearly. Small ripples are seen in the DC current due to switching of the inverter and of the supply switch. Larger ripples are seen due to charging and discharging of the capacitor. The higher the capacitor voltage, the larger these ripples will be, so it is desirable to keep the voltage as low as possible, while maintaining sufficient energy to supply any possible transients.

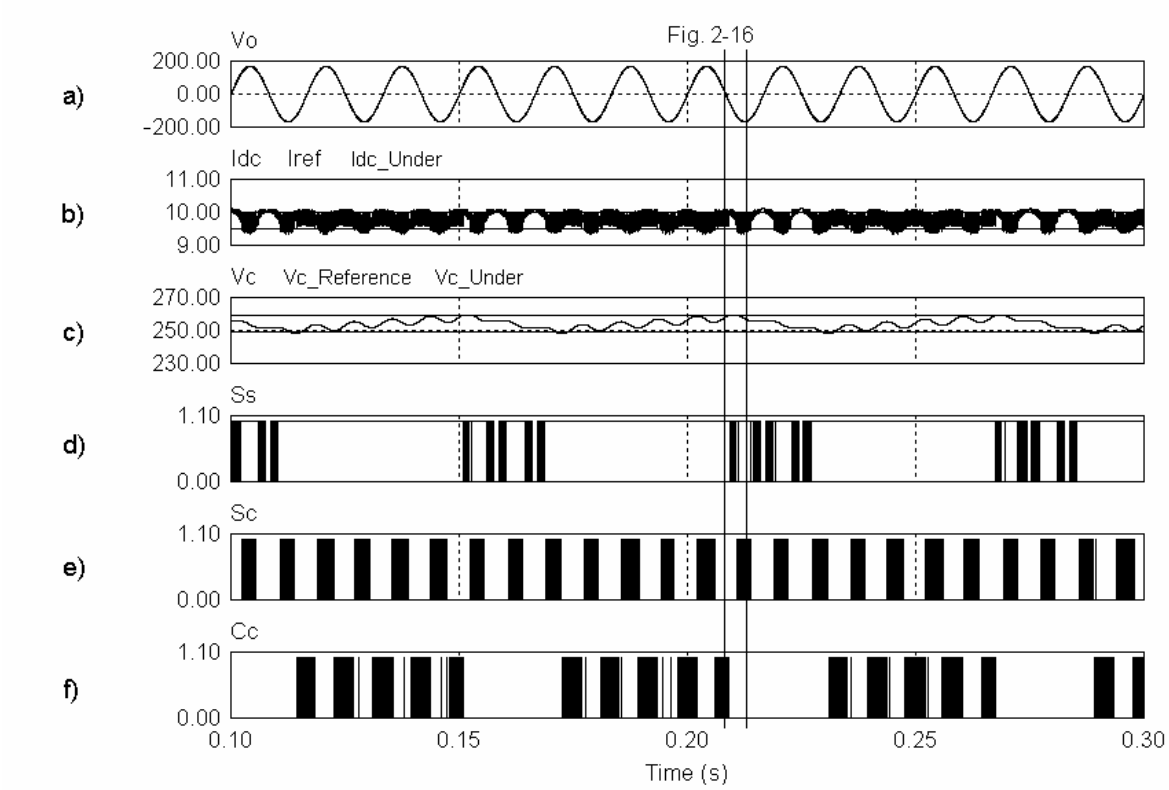

Fig. 2-15. Operation of *V-to-I* circuit controller
a) Output voltage (V)
b) Comparison of DC current to reference levels (A)
c) Comparison of capacitor voltage to reference levels (V)
d) Supply switch gating signal
e) Capacitor switch gating signal
f) Charge-capacitor control signal

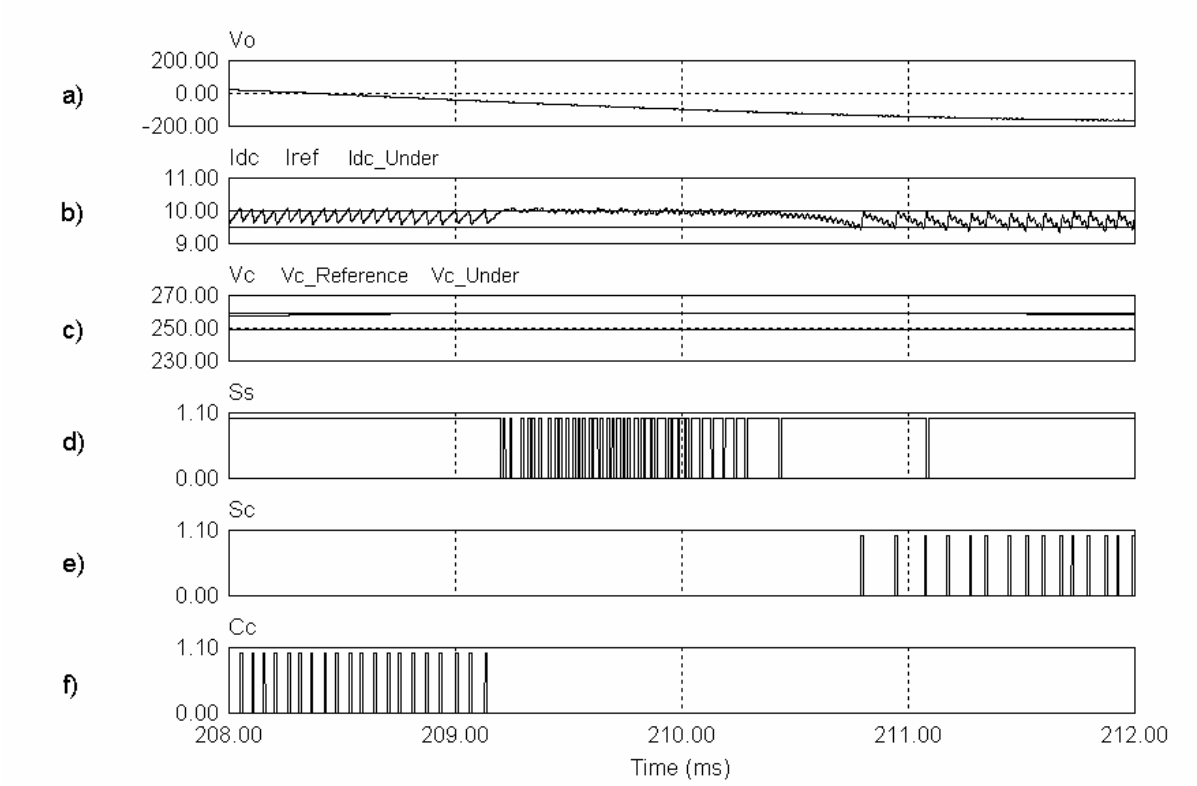

Fig. 2-16. Switching operation of *V-to-I* circuit controller over short time period
a) Output voltage (V)
b) Comparison of DC current to reference levels (A)
c) Comparison of capacitor voltage to reference levels (V)
d) Supply switch gating signal
e) Capacitor switch gating signal
f) Charge-capacitor control signal

2.6 DYNAMIC CURRENT REFERENCE SETTING

In order to keep losses minimal, it is desirable to modify the DC current reference level as the load changes, so that the current is never higher than necessary. Several schemes could be used to do this, depending on the objectives.

1. For constant DC current and minimal use of the energy-storage capacitor:

   As covered in section 2.4.1, to keep a constant DC current without using supplemental energy storage at steady-state, it is necessary to set the current reference level greater than or equal to $I_{DC,ideal}$ (2-12). $I_{DC,ideal}$ is equal to the peak

of the instantaneous output power divided by the DC source voltage, and therefore varies with changes in loading. The peak output power can be easily determined by tracking v_o and i_o over a single 120-Hz period and taking the maximum value. (v_o is measured directly, and i_o is known to be equal to $I_{DC}*m$.) The DC current reference can then be updated once each period. If a change in load causes $I_{DC,ideal}$ to rise above I_{DC}, the current can be maintained until the next reference update using the energy-storage capacitor.

2. For minimal DC current (allowing some 120-Hz ripple) and minimal use of the energy-storage capacitor:

   In this case, the current reference must be set greater than or equal to $I_{DC,required}$, which also varies with the loading level. There are two ways to determine $I_{DC,required}$ at run-time. The first is to produce a matrix of $I_{DC,required}$ values over the range of possible loading levels (resistive and inductive), using the scripts described in section 2.4.2. Then, at run-time, the real and reactive output powers can be calculated from the output voltage and current, measured as in case 1. The operating power is then compared to the matrix to find a value for $I_{DC,required}$. Also as in case 1, the DC current can be maintained by the energy-storage circuit if its required level changes between reference updates.

   The second method is to perform the analysis done by the script of section 2.4.2 in real-time, using the physical converter rather than a simulation. A series of potential current reference levels would be tested to determine whether they are sustainable without the use of the energy-storage circuit. If condition 2, 3, or 4 of section 2.4.2 is reached, the current reference is not sustainable. The energy-storage circuit would then be used to bring the DC current back up to the next potential level to be tested. Once a minimal sustainable level is found, the energy-storage circuit is not required again until a change in load is detected and the process is repeated. This method is preferable if nonlinear loads are expected, as their current requirements may be different from linear loads at the same power levels.

3. For minimal, constant DC current, using energy-storage capacitor at steady state:

   In this case, the DC current reference must be set greater than or equal to $I_{DC,minimum}$, as given by (2-15). $I_{DC,minimum}$ is equal to the RMS output power divided by the DC source voltage. The output power can be calculated using v_o and i_o, as in case 1.

2.7 EXPERIMENTAL RESULTS

Throughout this chapter, a single-phase current-sourced inverter was used to demonstrate the operation of the *V-to-I* circuit, for simplicity. Experiments were all done using a three-leg current-sourced inverter, however, as this inverter is required to produce split-phase output voltages. The three-leg inverter is shown in Fig. 2-17. Its operation is discussed in detail in Chapter 3. From the perspective of the *V-to-I* preconditioning circuit, however, it is identical to the single-phase case.

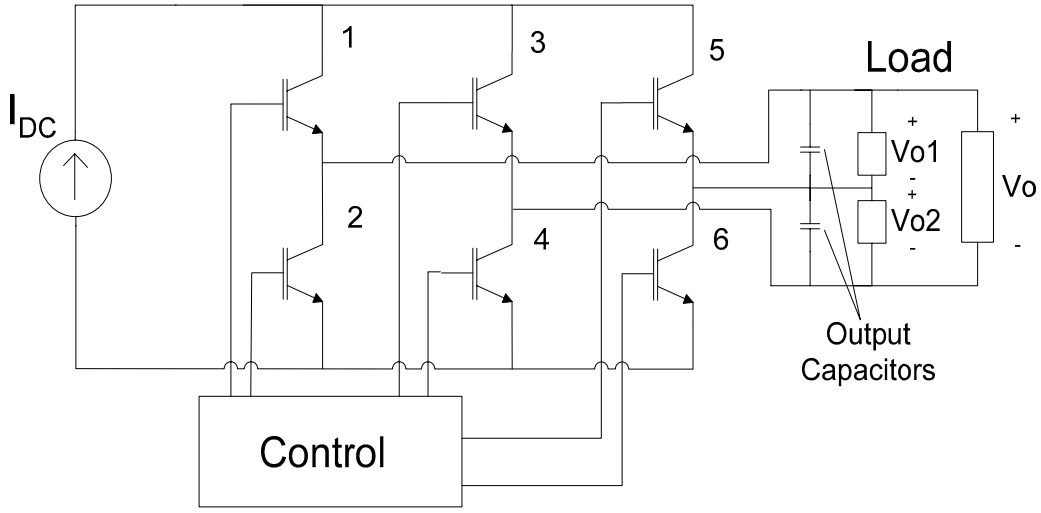

Fig. 2-17. Three-leg current-sourced inverter

Rather than directing the current in the forward or reverse direction through a single output capacitor, the three-leg inverter is able to direct the DC current in the forward or reverse direction through either or both output capacitors. In this way, it can independently control the two *half-phase* output voltages, as will be covered in Chapter 3. The reflected voltage from (2-2) then becomes

$$v_{reflected} = v_{o1}*m_1 + v_{o2}*m_2. \tag{2-25}$$

This is equal to

$$v_{reflected} \cong \frac{v_{o1}i_{o1} + v_{o2}i_{o2}}{\mathrm{I_{DC}}} = \frac{P_O}{\mathrm{I_{DC}}}, \tag{2-26}$$

which is identical to the single-phase case. Therefore, the operation of the voltage source-to-current source circuit is dependent only on the total output power, and remains unchanged regardless of whether a single-phase or split-phase inverter is used. In fact, this technique is equally appropriate for a three-phase inverter.

The specifications of the experimental prototype are the following. (Complete details are given in Chapter 4.) The inverter bridge was built with three Fuji Electric 2MBI50N-060 IGBT switch modules, in series with Fuji Electric 2FI50A-60 diode modules. These were used rather than reverse-blocking IGBTs due to availability. Two more 2MBI50N-060 switch modules and three more 2FI50A-60 diode modules were used for the front-end current source implementation, although only two reverse-blocking switches and two diodes were required. The inverter was controlled by an M67 DSP board by Innovative Integration, with a Texas Instruments TMS320C6701 processor. Measuring circuitry for the output voltages and DC current was also used, as well as driver circuits for the 8 switches.

A 50-mH DC inductor was used due to availability. However, in practice this circuit could be constructed with a much smaller inductor, such as the 5-mH inductor used in the simulations, or one even smaller. Choosing the inductor size is a trade-off between inductor cost and size, and switching frequency. A larger inductor allows the supply and capacitor switches to be operated at lower frequencies, reducing switching losses, but increases the capital cost and weight.

The energy-storage capacitor was 1mF, and the output filter capacitors were 15μF each.

Fig. 2-18 confirms that turn-on transients can result in large transient power draws, even in non-motorized loads. The figure shows the voltage across and current through a 150-W incandescent light bulb when it is initially switched on to a strong voltage source. It can be seen that the initial current draw is approximately ten times the steady-state value.

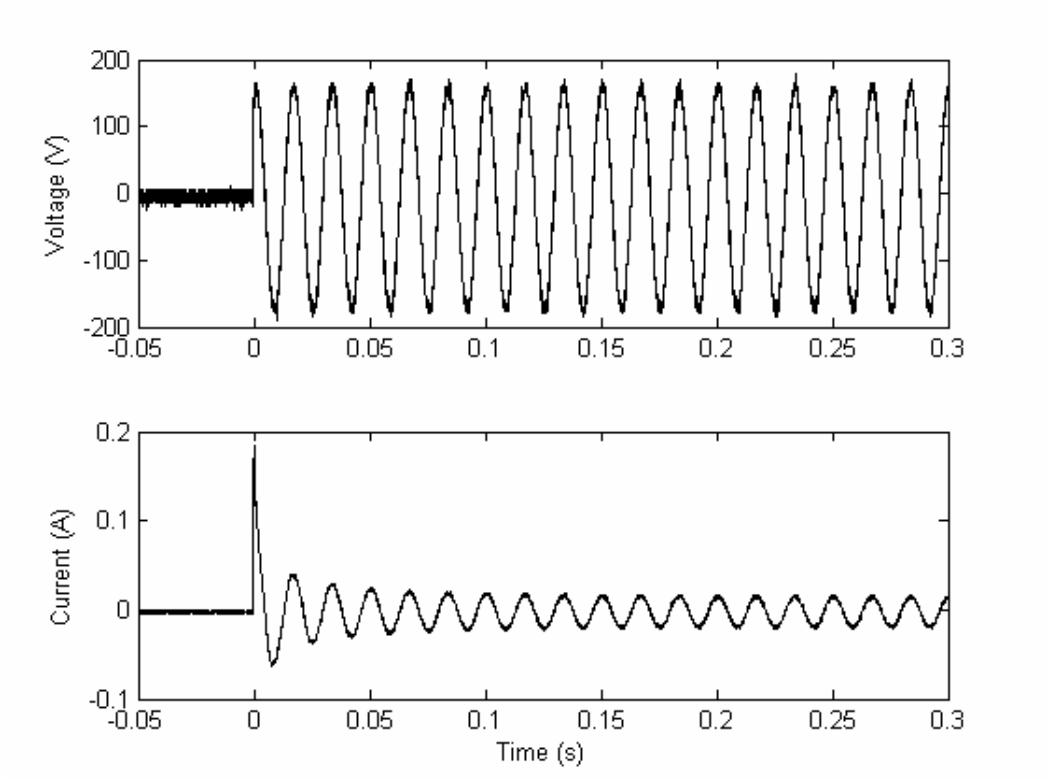

Fig. 2-18. Turn-on transient of 150-W incandescent light bulb

Fig. 2-19 and Fig. 2-20 show the operation of the circuit in the presence of a turn-on transient. The initial loads are

- Top 120-V output: 57.6W (250 Ω)
- Bottom 120-V output: 57.6W (250 Ω)
- Combined (240-V) output: 57.6W (1000 Ω)
- Total load: 172.8W

A 150-W light bulb is then switched on in parallel with the top 120-V load. Fig. 2-19 is the result without supplemental energy storage. The output power is temporarily greater than the available input power, resulting in a drop in DC current. Equivalently, the reflected voltage is temporarily increased above the supply voltage, resulting in the same drop. As the current drops, the input power decreases and the reflected voltage increases, preventing the current from recovering, even after the transient power spike has finished.

In Fig. 2-20, once an increase in load is detected, the capacitor switch turns on to bring the DC current back to an acceptable level for the new loading conditions. Unlike in the previous case, operation is maintained. The DC current is increased to a new reference level using energy from the capacitor, which is recharged once the transient period has ended. Within several cycles, the output voltages return to their balanced state. This transient time period could be reduced further by improving the output feedback controllers. Simple PI controllers were sufficient for this proof of concept; however, the results could be improved by optimizing the prototype's layout to reduce noise, allowing higher-gain controllers to be used, or by replacing the controllers with a more advanced type, such as state-feedback.

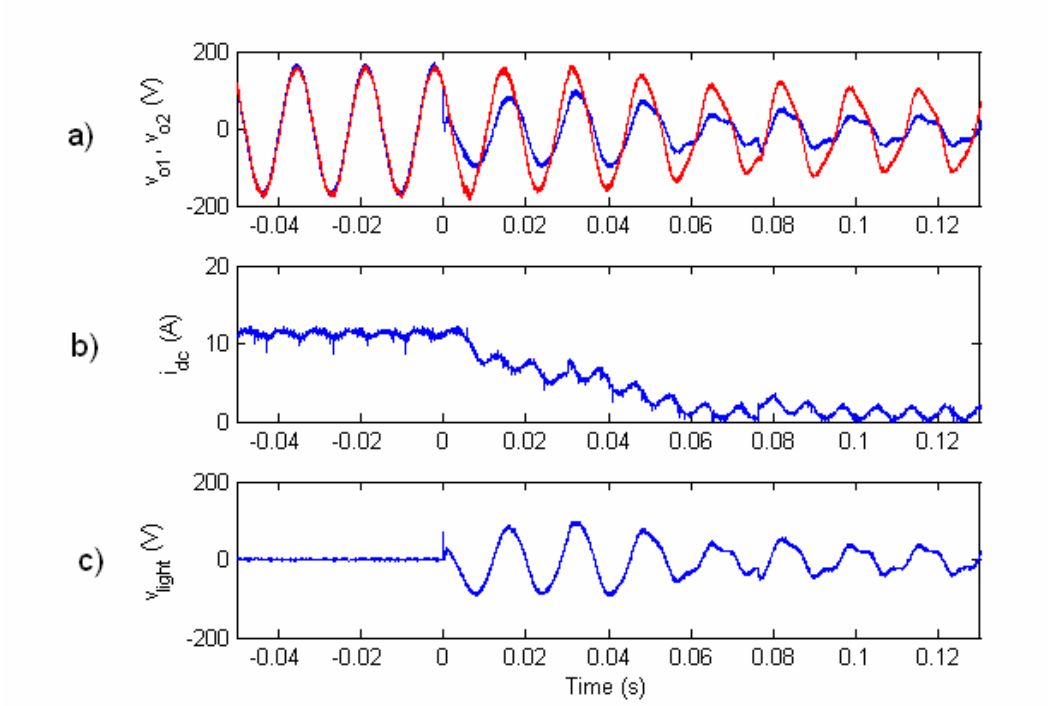

Fig. 2-19. Failure of experimental prototype Current-Sourced Inverter due to turn-on transient
a) Output (load) split-phase voltage (V)
b) DC Current (A)
c) Voltage across 150W lamp (equal to v_{o1} after turn-on) (V)

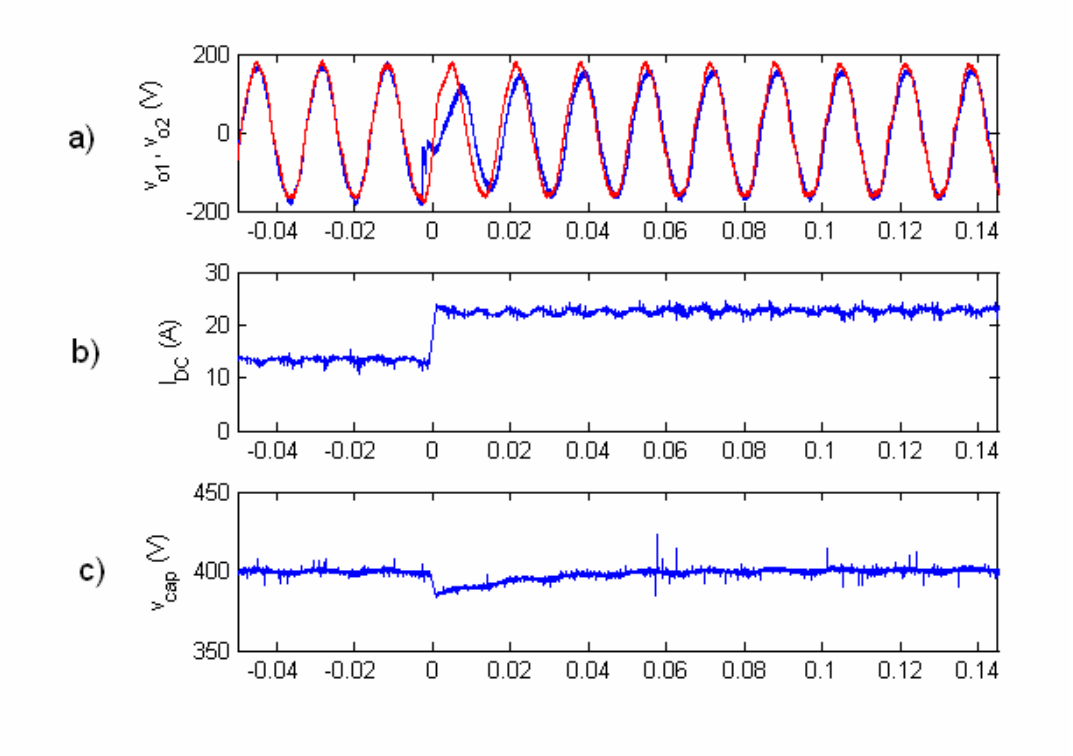

Fig. 2-20. Successful operation of experimental prototype current-sourced inverter during turn-on transient, with additional energy-storage circuit
a) Output (load) split-phase voltage
b) DC Current
c) Voltage across 150W lamp (equal to v_{o1} after turn-on)

It should be noted that although the current drops in Fig. 2-19, the change is not as fast as anticipated by simulations. This is also due to the gains of the closed-loop voltage controllers in the experimental prototype, set lower than in the simulations to account for noise in the feedback measurements. The output voltages are therefore no longer strong, as was assumed in the calculations of section 2.4.2. Therefore, when the output impedance drops rapidly, the voltage(s) also drop, reducing the effective power transient, which mitigates the effect on the DC current. This suggests that if only small transients such as those caused by light bulbs are expected, and if short-term deviations of the output voltages from their references are allowable, it may be possible to operate without supplemental energy storage. Instead, the output control would have to be altered to reduce the voltage temporarily when a sudden decrease in impedance is detected. The ITI Council, formerly the Computer Business manufacturers Association, provides guidelines on the acceptable

range for voltage fluctuations [20]. However, it will not be possible to accommodate for large turn-on transients, such as those caused by motors. Also, as described in section 2.4.2, the DC current will have to be set sufficiently high to accommodate any step change in load, resulting in increased conduction and switching losses and higher component stresses. Finally, the inclusion of the supplemental energy-storage circuit does not result in any additional losses when it is not in use, since no components are added to the current path. Therefore, the only reason not to include it would be if initial capital cost had to be minimized and no large transients were expected in the intended load.

2.8 ADVANCED ALGORITHM

It is possible to control the DC current and capacitor voltage more precisely than allowed by the basic algorithm described earlier in this chapter. By considering the output voltage and modulating signal of the current-sourced inverter, the effect of the reflected voltage on the DC current can be taken into account. Rather than simply comparing the DC current to a threshold, as was done in the previous sections, the *V-to-I* controller can then determine exactly how long the supply switch (S_S), capacitor switch (S_C), and/or charge-capacitor signal (C_C) need to be on to bring the DC current to its exact reference value.

2.8.1 OVERVIEW

This control algorithm is intended to operate at a discrete interval, T. It is designed such that at the end of each interval, 1) the DC current will be brought equal to its reference level, and 2) the energy-storage capacitor voltage will be brought as close to its reference level as possible, while achieving 1). The controller's inputs are the DC Current, I_{DC}, the energy-storage capacitor voltage, V_C, and the inverter output voltage and modulating signal, v_o and m, both of which are already used by the current-sourced inverter's controller. Using these inputs, it is possible to calculate the effect of the inverter's operation on the DC current. The controller can then determine how long the supply switch, S_S, should be turned on and how long the capacitor should be charged or discharged during the upcoming control period in order to achieve the stated goals. The controller's outputs are the lengths of time that the supply and capacitor switches should be turned on and the length of time that the charge-

capacitor signal should be high, during the period T. These are defined as $t_{on,S}$, $t_{on,C}$, and t_{charge}, respectively, and are each between 0 and T.

2.8.2 DESCRIPTION OF ALGORITHM

As with the original algorithm, the *V-to-I* controller will run at discrete intervals, with a constant period, T. T should be a multiple of the effective switching period, which, in the case of tri-level PWM inverters, is ½ the actual switching period [17]. Over a short time (several switching periods), the output voltage and modulating signal can be considered constant. Therefore, the change in DC current due to the reflected voltage over a single control period, T, can be easily calculated:

$$\Delta I_{DC,reflected} = -T\left(\frac{v_{reflected}}{L_{DC}}\right) = -T\left(\frac{v_o m}{L_{DC}}\right) \tag{2-27}$$

($\Delta I_{DC,reflected}$ refers the change in I_{DC} due to the reflected voltage.) Ignoring the supplemental energy-storage circuit to begin with, the desired time for the supply switch to be on during the switching period is then given by (2-28), where $\Delta I_{DC,source}$ refers the desired change in I_{DC} due to the source voltage:

$$t_{on,S,des} = \frac{L_{DC}\Delta I_{DC,source}}{V_{DC}} = \frac{L_{DC}\left(I_{REF} - I_{DC} + T\left(\frac{v_o m}{L_{DC}}\right)\right)}{V_{DC}} \tag{2-28}$$

If the calculated $t_{on,S,des}$ is longer than T, it shows that the DC supply cannot provide sufficient power to bring the DC current to its reference level (or to keep it there) within the period. In that case, the capacitor would have to be used as well. Assuming the capacitor is not overcharged (and therefore we do not want to lower its voltage more than necessary), the supply switch will then be left on for the entire period, and the capacitor switch, S_C, will be turned on for

$$t_{on,C} = \frac{V_{DC}}{V_C}\left(t_{on,S,des} - T + t_{on,C}\right) = \frac{\frac{V_{DC}}{V_C}\left(t_{on,S,des} - T\right)}{1 - \frac{V_{DC}}{V_C}}, \tag{2-29}$$

where $t_{on,S,des}$ is given by (2-28). This makes up for the difference between the desired energy to be supplied and that which can be supplied by the DC voltage source during the available period. The $t_{on,C}$ term on the right hand side of the first equation is present because the supply switch is reverse biased during $t_{on,C}$, when the capacitor switch is on. The capacitor must therefore make up this amount, as well as the shortfall between $t_{on,S,des}$ and T.

If the capacitor has been charged above its reference voltage, more of the inductor-charging could be shifted from the DC supply to the capacitor in order to reduce the capacitor voltage. In this case, the desired time for the capacitor switch to be on, in order to bring the capacitor voltage back to its reference level, is

$$t_{on,C,des} = \frac{C\left(\mathrm{V_C} - \mathrm{V_{C,REF}}\right)}{\mathrm{I_{DC}}}. \tag{2-30}$$

If this value is larger than $t_{on,C}$ from equation (2-29), it will be used instead. The remaining energy required to bring the DC current to its reference will then be provided by the DC supply. The actual on-time for S_S, $t_{on,S}$, is then calculated by adding the effect of $t_{on,C,des}$ to equation (2-28):

$$t_{on,S} = \frac{\mathrm{L_{DC}}\left(\mathrm{I_{REF}} - \mathrm{I_{DC}} + \mathrm{T}\left(\frac{v_o m}{\mathrm{L_{DC}}}\right)\right) - \mathrm{V_C}\left(t_{on,C,des}\right)}{\mathrm{V_{DC}}} \tag{2-31}$$

Again, the supply and capacitor switches cannot both be turned on at the same time. Therefore, this period cannot be concurrent with $t_{on,C}$. Also, control of the DC current takes precedence over the capacitor voltage. Therefore $t_{on,C}$ is capped at the point where $t_{on,S}$ from (2-31) would go negative, and the DC inductor would be overcharged.

$$t_{on,C,\max} = \min\left(\frac{\mathrm{L_{DC}}\left(\mathrm{I_{REF}} - \mathrm{I_{DC}} + \mathrm{T}\left(\frac{v_o m}{\mathrm{L_{DC}}}\right)\right)}{\mathrm{V_C}}, \mathrm{T}\right). \tag{2-32}$$

Thus far, cases have been covered where I_{DC} is below its reference and V_C is at or above its reference. It is also possible for I_{DC} to be above its reference (the DC inductor is overcharged) and/or for V_C to be below its reference. (All possible cases and the applicable controls given in this section are summarized in Fig. 2-21.)

I_{DC} can rise above its reference when the reflected voltage is negative. This will happen for part of the 60-Hz output cycle if the load is not entirely resistive. If the reflected voltage is negative, or I_{DC} is already above I_{REF}, $t_{on,S,des}$ (2-28) will be negative. It is impossible for the switch to be on for a negative time period, so some intervention is required. The current can be prevented from exceeding its reference by charging the capacitor. The required time to charge the capacitor is given by

$$t_{charge} = \frac{V_{DC}}{V_C}\left|t_{on,S,des}\right|, \tag{2-33}$$

where $t_{on,S,des}$ is negative and is given by (2-28).

The final case to consider is when the capacitor voltage is below its reference level. As long as $t_{on,S,des}$, as calculated by (2-28), is less than T, we can use the remaining available energy from the supply to charge the capacitor. The desired charging time is given by

$$t_{charge,des} = \frac{C\left(V_{C,REF} - V_C\right)}{I_{DC}} = -t_{on,C,des}. \tag{2-34}$$

Control of the DC current takes priority. Therefore, since t_{charge}, from (2-33), is the minimum time that the capacitor needs to be charged from the inductor in order to bring the DC current down to its reference level, if t_{charge} is greater than $t_{charge,des}$, t_{charge} will take precedence. In other words, the capacitor charging time will be the greater of the results of (2-33) and (2-34). If $t_{charge,des}$ is greater than t_{charge}, a new on time for the supply switch must be calculated, so that the DC current does not drop below its reference level through charging of the capacitor:

$$t_{on,S} = \frac{L_{DC}\left(I_{REF} - I_{DC} + T\left(\frac{v_o m}{L_{DC}}\right)\right) + V_C\left(t_{charge,des}\right)}{V_{DC}} \tag{2-35}$$

This equation is identical to (2-31), in terms of $t_{charge,des}$ rather than $t_{on,C,des}$. Again, as with (2-31), current control is the priority; therefore, t_{charge} cannot be set such that $t_{on,S}$ exceeds T because this would result in I_{DC} dropping below its reference. Therefore,

$$t_{charge,\max} = \min\left(\frac{V_{DC}T - L_{DC}\left(I_{REF} - I_{DC} + T\left(\frac{v_o m}{L_{DC}}\right)\right)}{V_C}, T\right). \tag{2-36}$$

The comprehensive voltage source-to-current source circuit control is summarized in Fig. 2-21.

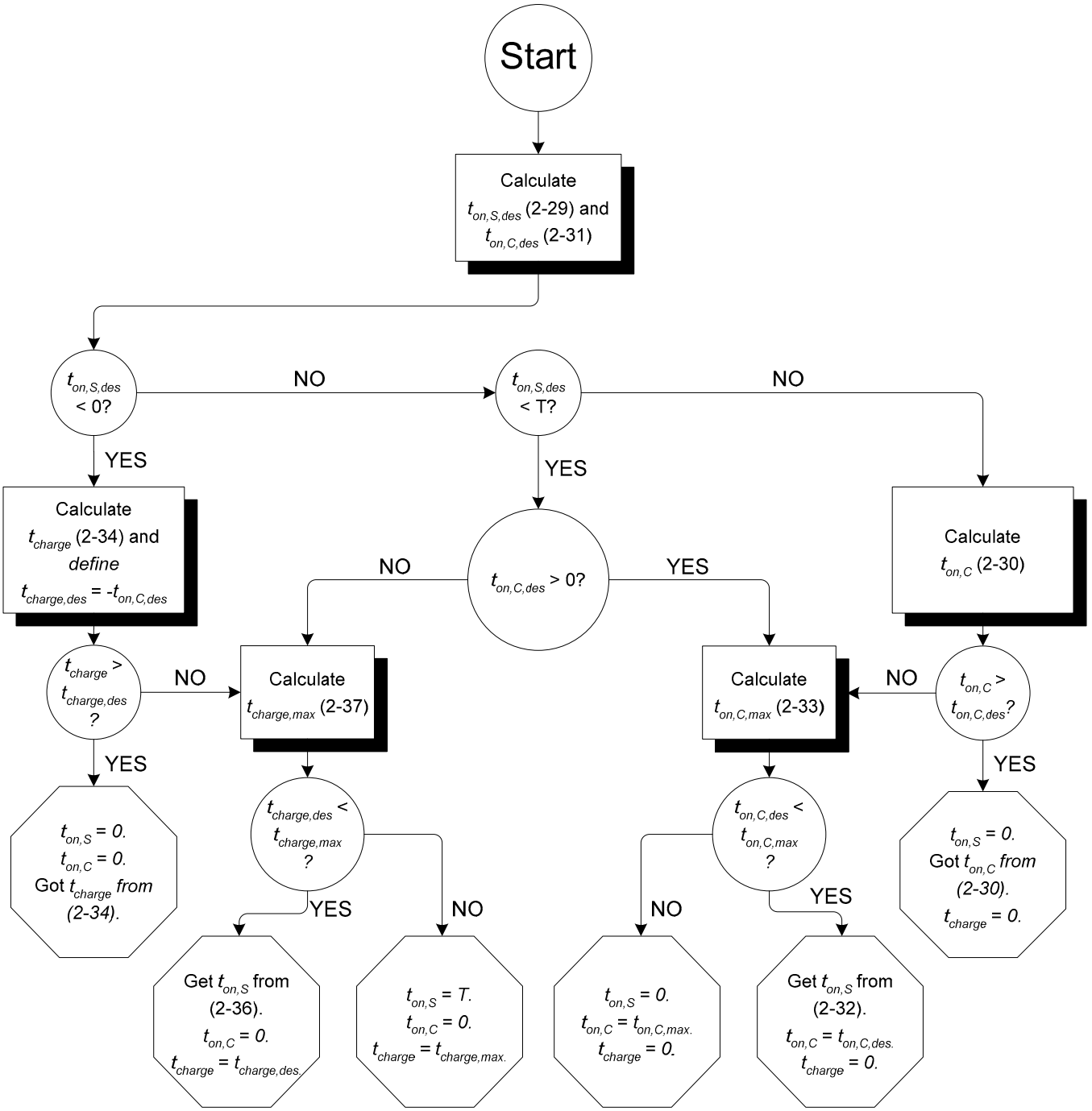

Fig. 2-21. Flowchart showing advanced control algorithm for *V-to-I* circuit

2.8.3 SUPPORTING RESULTS

The control board used to construct the experimental prototype of section 2.7 did not have the necessary speed or analog-to-digital conversion capabilities to implement this algorithm. Such an implementation was not necessary, however, since the feasibility of the experimental design was clearly shown using the basic algorithm. The advantages of this advanced control algorithm are demonstrated here using simulation results.

Comparing Fig. 2-22 to Fig. 2-15 in section 2.5.3, it is clear that the current regulation with this control technique is much more precise. The only difference between the two experiments is the *V-to-I* control method. In this case, the DC current is held to within 2% of the reference, rather than 10% in the earlier experiment. The frequencies of the supply and capacitor switches are now fixed at 20 kHz (when their duty ratios are not 0 or 100%). An alternate frequency could be chosen if desired. Under the previous method, these switching frequencies were variable and not directly controlled. The maximum frequency of the supply switch was approximately 50 kHz, and that of the capacitor switch was approximately 35 kHz.

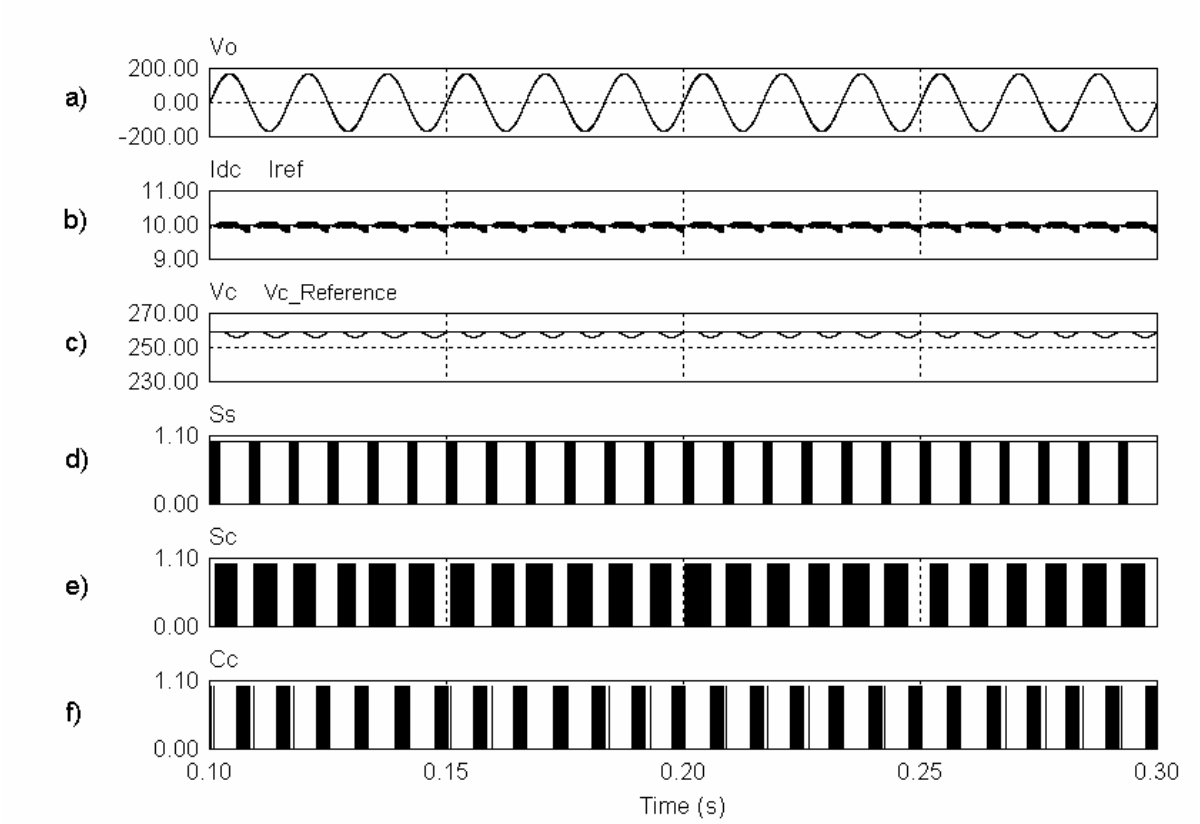

Fig. 2-22. *V-to-I* circuit controller operation with new control algorithm
a) Output voltage (V)
b) Comparison of DC current to reference levels (A)
c) Comparison of capacitor voltage to reference levels (V)
d) Supply switch gating signal
e) Capacitor switch gating signal
f) Charge-capacitor control signal

2.8.4 PRACTICAL MODIFICATIONS

Several slight modifications can be made to this theoretical algorithm to enhance its practicality. First, if any of the calculated *on* states, t_{on}, $t_{on,C}$, or t_{charge}, are very near to 0 or T (for example, less than t_{min}=1/100 T or greater than t_{max}=99/100 T), it can be rounded. This will prevent unnecessary switching and will only result in a very slight deviation of I_{DC} or V_C from its reference level, which can be corrected in the next cycle.

The inductor-charging periods, specifically the fast charging period using the capacitor, should coincide as much as possible with the periods of high instantaneous reflected voltage in order to balance the instantaneous voltage across the DC inductor, reducing the DC

current ripple. This can be accomplished in a straightforward manner if the control period is set equal to the effective switching period. The instantaneous reflected voltage is high when the inverter is in an active state, and is zero otherwise. Therefore, the $t_{on,C}$ period, if it is present, or otherwise the $t_{on,S}$ period, can be timed to coincide with the active state.

The capacitor-charging period, t_{charge}, can only occur during shoot-through states, as described in section 2.5.3. Charging of the capacitor causes added switching losses on the inverter switches. Therefore, the charging periods should be alternated between the two shoot-through states (the states when the DC current cycles in each of the two inverter legs) to spread these losses among the four inverter switches.

Finally, this algorithm brings the DC current and, if possible, the capacitor voltage to their reference values at the end of each control period: in this case 1/20 kHz. However, it is not necessary to control the capacitor voltage to a specific value. By eliminating this requirement and re-introducing a range of acceptable values for the capacitor voltage, unnecessary switching of the capacitor switch can be prevented. The range can be instituted by modifying the equations for $t_{on,C,des}$ and $t_{charge,des}$, (2-30) and (2-34) as follows:

$$t_{on,C,des} = \frac{C\left(\mathrm{V_C} - \mathrm{V_{C,Over}}\right)}{\mathrm{I_{DC}}} \tag{2-37}$$

$$t_{charge,des} = \frac{C\left(\mathrm{V_{C,Under}} - \mathrm{V_C}\right)}{\mathrm{I_{DC}}} \tag{2-38}$$

Rather than attempting to bring the capacitor voltage to a specific value, $\mathrm{V_{C,REF}}$, this control will simply attempt to keep it within the range ($\mathrm{V_{C,Over}}$, $\mathrm{V_{C,Under}}$). The current control still takes precedence, however, so the capacitor will be allowed to venture outside this range in order to maintain the DC current, as long as it does not go beyond its minimum or maximum allowable values.

Fig. 2-23 shows the results with these modifications. Note that the plot scales are different from Fig. 2-22, to clearly show the variations of the DC current and capacitor voltage. The capacitor voltage remains at the bottom of its range because the load is resistive. There are therefore no significant periods of negative reflected voltage, and so there is no reason to charge the capacitor once it has reached its desired range.

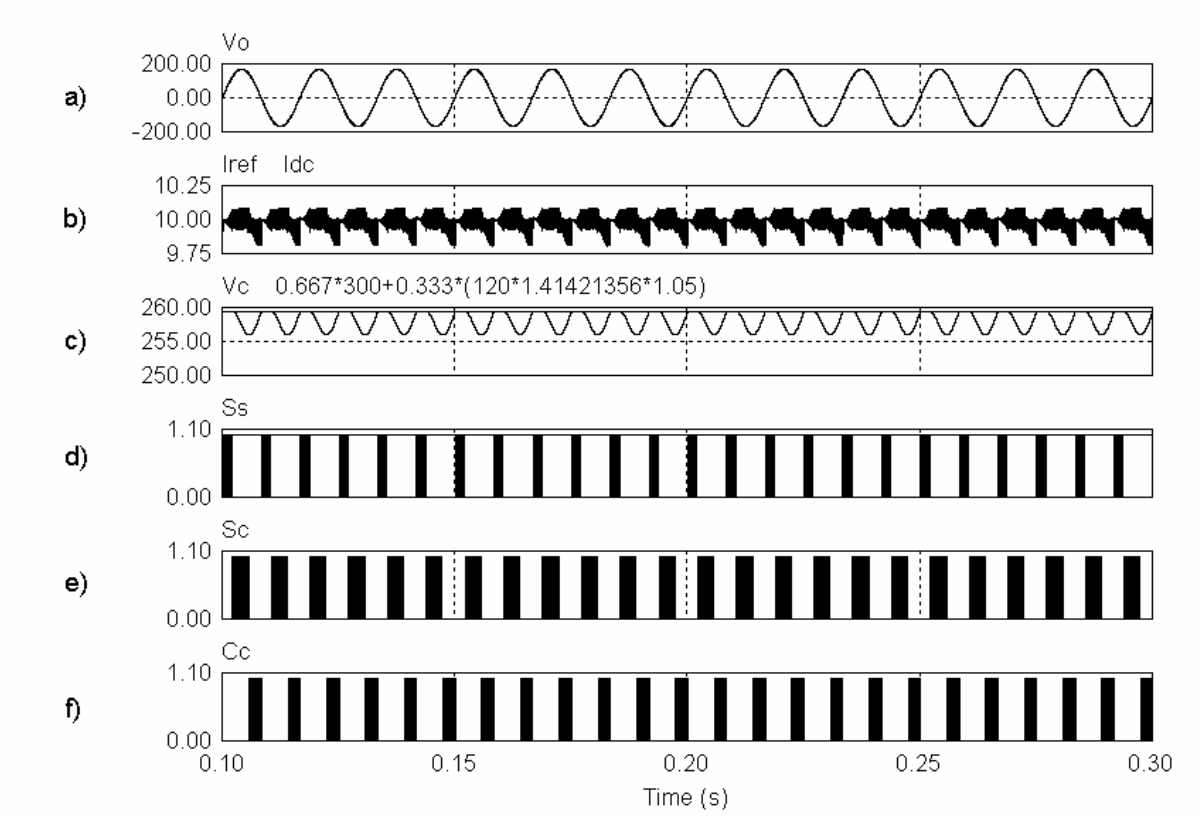

Fig. 2-23. Final *V-to-I* circuit controller operation including practical modifications
a) Output voltage (V)
b) Comparison of DC current to reference levels (A)
c) Comparison of capacitor voltage to reference levels (V)
d) Supply switch gating signal
e) Capacitor switch gating signal
f) Charge-capacitor control signal

Fig. 2-24 shows a period of the same test, when the capacitor is being used to maintain the DC current. As desired, charging of the inductor from the capacitor (with S_C) occurs during the active state (the period where v_o is increasing). Clearly, the DC current is controlled to its reference value within each control cycle. Fig. 2-25 shows the details of recharging the capacitor voltage to its reference range. While the voltage is below the desired range, all available energy beyond that required to maintain the DC current is used to recharge the capacitor. The supply switch is therefore left on 100% of the time. While the capacitor is being charged, the DC current drops, but the charging time is set such that the current can recover to its reference level by the end of each control cycle. Once the desired

capacitor voltage is reached, the supply switch is turned off when necessary to control the DC current. This will continue until the reflected voltage exceeds the supply voltage, and the capacitor must again be used to hold the DC current to its reference value, as in Fig. 2-24.

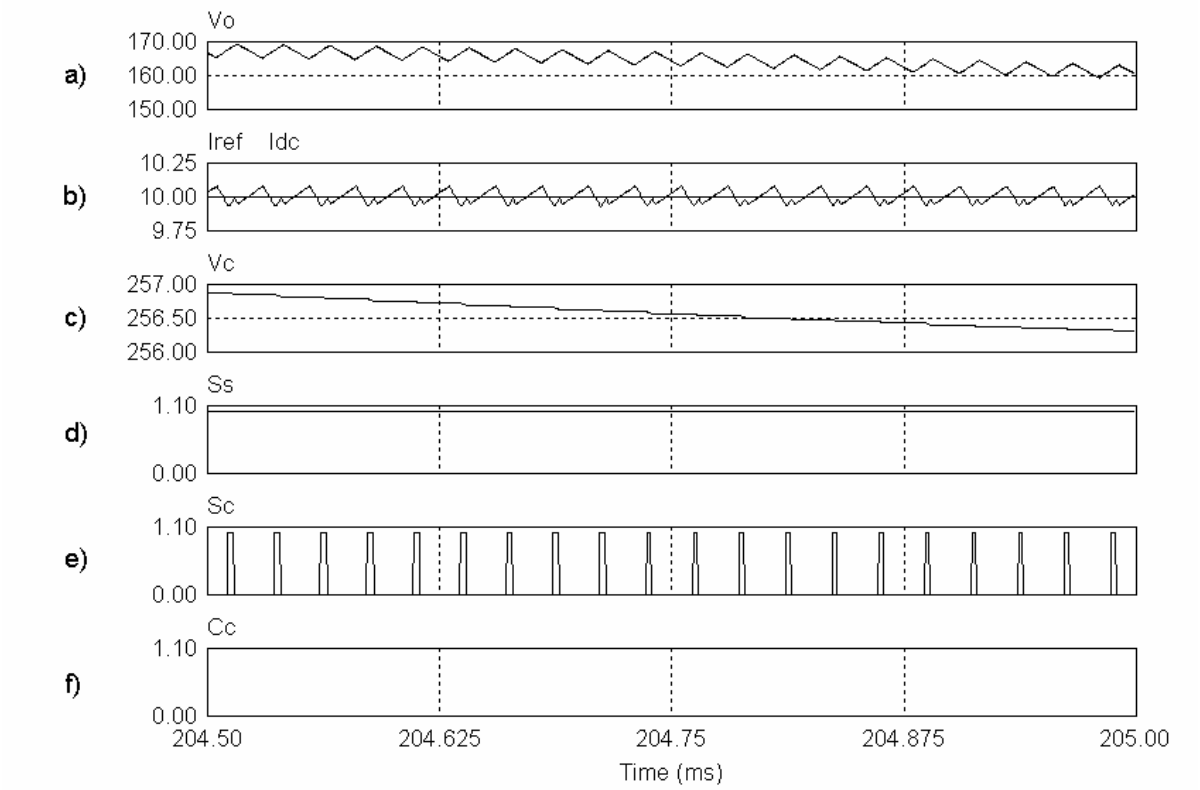

Fig. 2-24. Final *V-to-I* circuit controller operation: DC current being maintained through use of the energy-storage capacitor
a) Output voltage (V)
b) Comparison of DC current to reference level (A)
c) Energy-storage capacitor voltage (V)
d) Supply switch gating signal
e) Capacitor switch gating signal
f) Charge-capacitor control signal

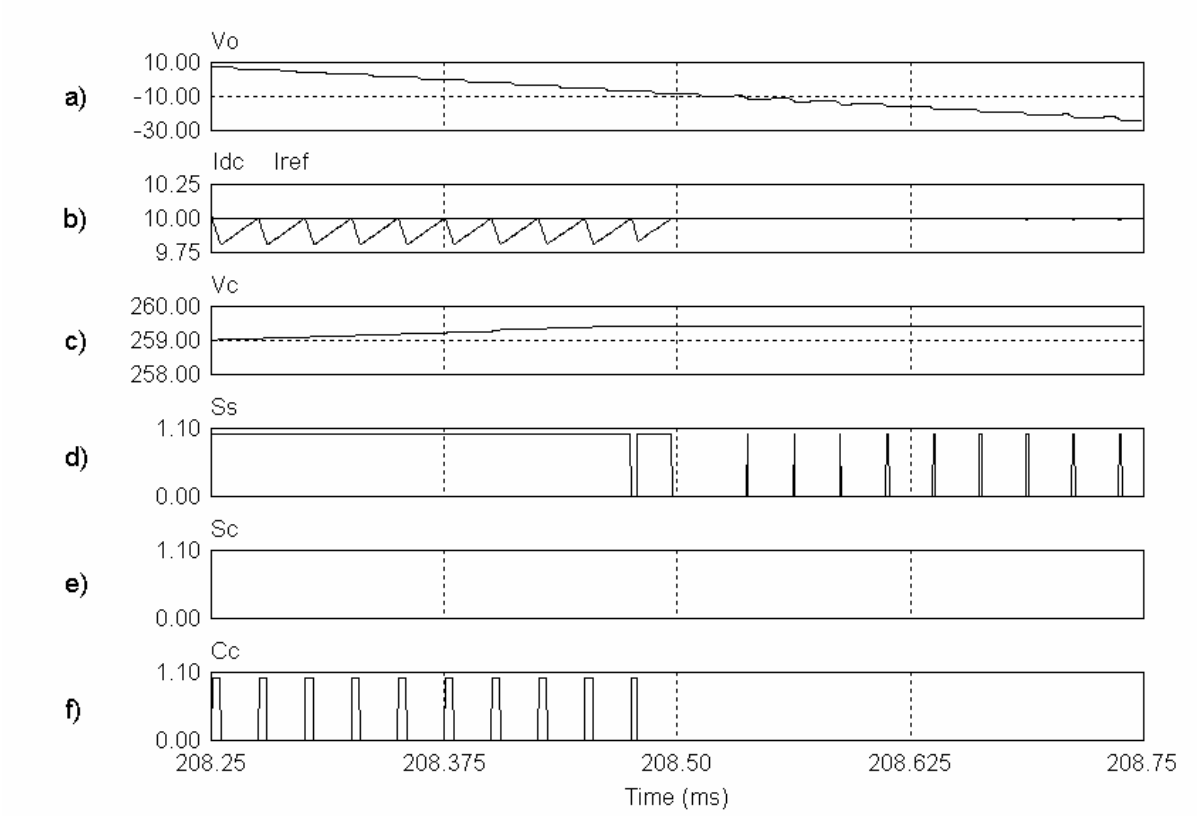

Fig. 2-25. Final *V-to-I* circuit controller operation: during and following charging of capacitor
a) Output voltage (V)
b) Comparison of DC current to reference level (A)
c) Energy-storage capacitor voltage (V)
d) Supply switch gating signal
e) Capacitor switch gating signal
f) Charge-capacitor control signal

2.8.5 ADVANTAGES

Some advantages to the control algorithm presented in this section over the basic control used in sections 2.5 and 2.6 are the following:

- Switching frequencies of supply switch and capacitor switch are known and controllable.
- Unnecessary switching is prevented, reducing switching losses.
- Ripple in DC current is reduced significantly by eliminating overshoot.

- DC current ripple is also reduced by synchronizing charging periods with discharge periods due to reflected voltage.
- Capacitor voltage can be kept within a narrower range.

2.9 SUMMARY

The objective of this chapter was to develop a topology and algorithm to produce a constant DC current, for use with a current-sourced inverter, from a low-voltage DC source. In section 2.2, the basic operation of current-sourced inverters was reviewed, and the terms *active state* and *shoot-through state* were introduced. In section 2.4, a simple circuit was developed to produce a constant DC current using a single switch and diode and a DC inductor. This circuit uses the same components as a boost converter, which would be required by a voltage-sourced inverter. Therefore, a CSI using this preconditioning circuit requires no additional components to a VSI, and possesses the advantages of CSIs listed in section 1.1.2.2. However, this circuit was unable to function during large step changes or transient spikes in inverter loading. Therefore, in section 2.5, a supplemental energy-storage sub-circuit was added, using an additional capacitor, switch, and diode, and in section 2.6 techniques were discussed for dynamically setting the DC current reference level while the system is in operation. The successful operation during steady-state and transient loads was demonstrated through simulations and experimental results in section 2.7. The additional energy storage circuit does add a small amount of complexity at the input versus a voltage-sourced inverter, but this is offset by a reduction in filtering requirements at the inverter's output(s) and by the other advantages of current-sourced inverters listed in section 1.1.2.2. Finally, a more advanced control algorithm was presented, which improved upon the earlier results by taking into account the effect of the current-sourced inverter's operation on the voltage source-to-current source circuit.

CHAPTER 3

GENERATION OF SPLIT-PHASE OUTPUTS

3.1 INTRODUCTION

Residential and light-commercial power in North America is supplied in *split-phase* form. When supplied from the distribution grid, split-phase voltages are produced using a centre-tap on the distribution transformer, as shown in Fig. 3-1. The two *half-phase* outputs, v_{o1} and v_{o2}, are each 110 to 120V rms, and are 180 degrees out of phase, as shown in Fig. 3-2. The overall output voltage, v_o, is therefore 220 to 240V rms, in phase with v_{o1}.

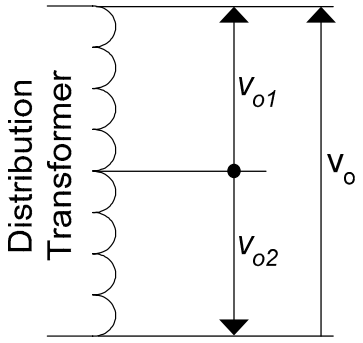

Fig. 3-1. Split-phase outputs from distribution transformer

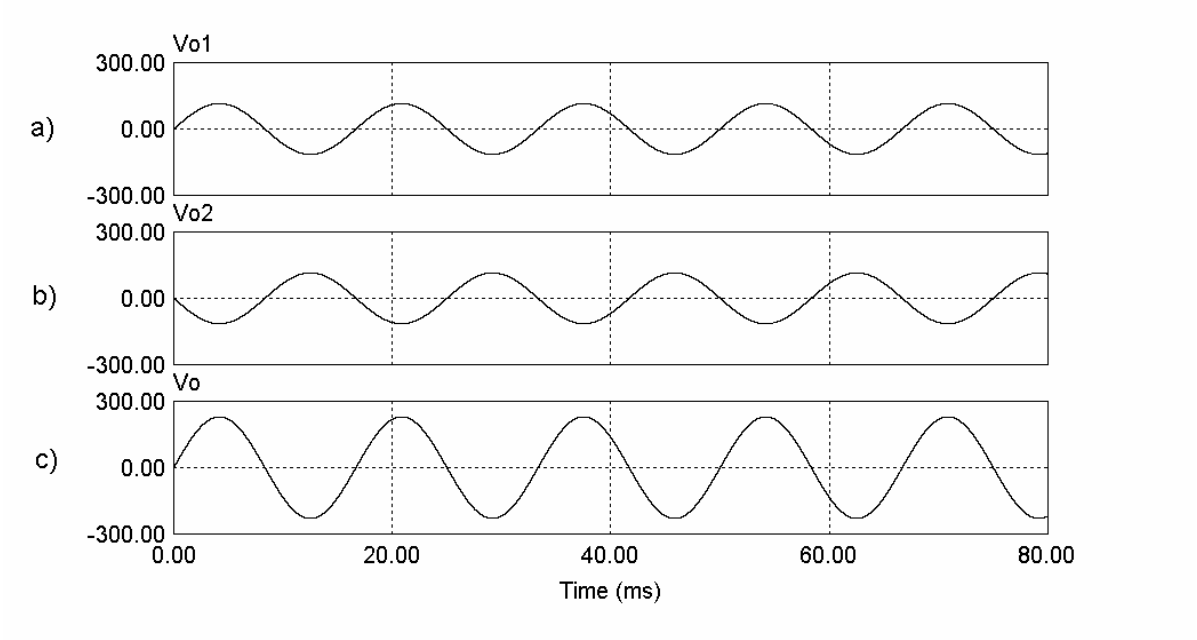

Fig. 3-2. Example of split-phase output voltages
a) Top *half-phase* output voltage (V)
b) Bottom *half-phase* output voltage (V)
c) Double output voltage (V)

The objective of this chapter is to produce split-phase output voltages like those shown in Fig. 3-2 using a three-leg current-sourced inverter, as shown in Fig. 3-3. Note that, in order to simplify voltage feedback control, the polarities of v_{o1} and v_{o2} are defined in the same direction, unlike in Fig. 3-1. The controller must then produce two identical output voltages, v_{o1} and v_{o2}, each 110 to 120V rms, and in phase. The current source, labelled I_{DC} in Fig. 3-3, is realized as described in Chapter 2. The basic control algorithm described in section 2.5.3 can be used without modification. Minor changes must be made to use the advanced algorithm of section 2.8 to work with a split-phase inverter; these will be described in the discussion section, 3.3.5.

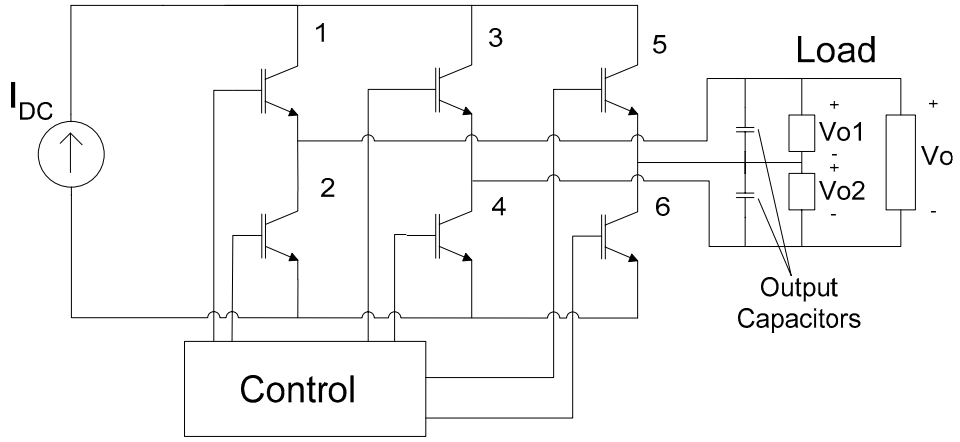

Fig. 3-3. Three-leg current-sourced inverter, designed to produce split-phase output voltages

3.2 REQUIREMENTS

3.2.1 REGULATION OF OUTPUT VOLTAGES

The operation of this three-leg inverter is the same as that of the two-leg inverter described in section 2.2, in that the output voltages are controlled by directing the DC current into each of the output filter capacitors in either the forward or reverse direction. However, in this case there are two output capacitors rather than one. The DC current can be directed into each capacitor separately or into both in series, again in either direction. As in the single-phase case, when an output capacitor is not being actively charged or discharged, it will slowly discharge through the connected load. When neither capacitor is being actively charged or discharged, the inverter is in a *shoot-through* state, with the DC current cycling through one of the three inverter legs. The result is that the output voltages *ripple* about their respective references as the capacitors are quickly charged beyond the desired levels and then more slowly discharge back below them. This is illustrated over several switching cycles in Fig. 3-4. Fig. 3-4(a) shows the voltage ripple at a single output, while Fig. 3-4(b) shows the current being injected from the inverter into the output capacitor. The *active states* in this case are states in which either or both output capacitors are being actively charged or discharged.

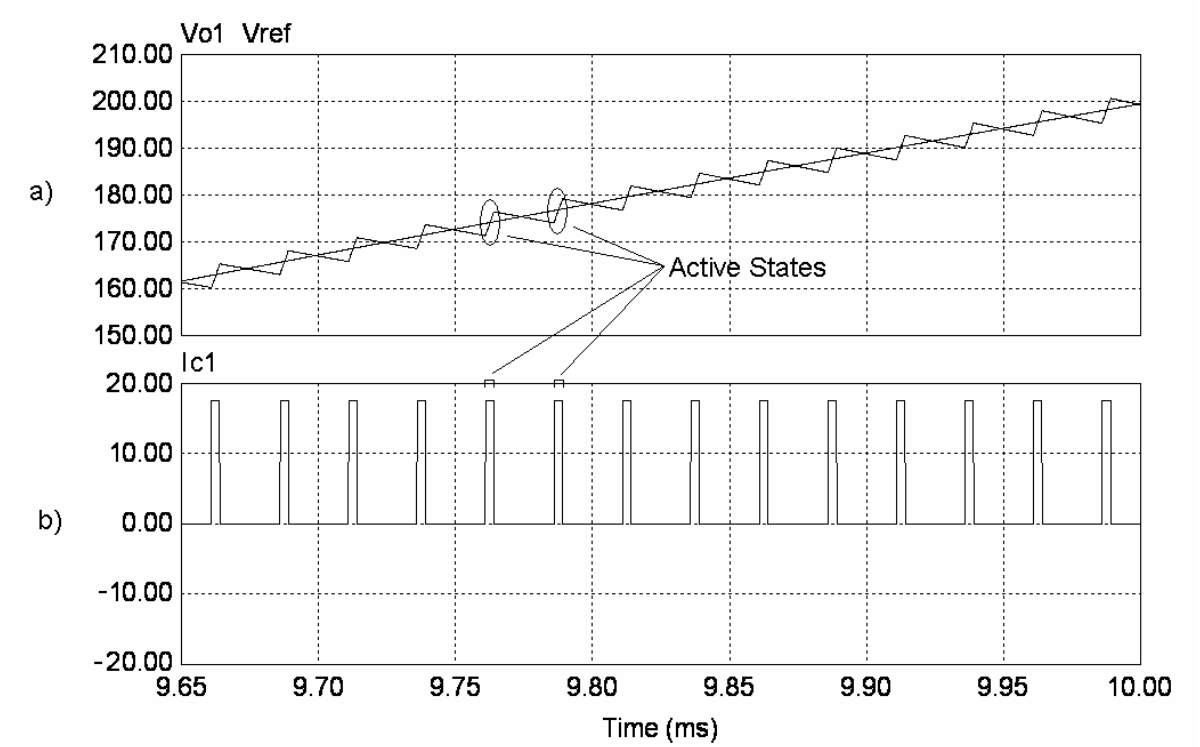

Fig. 3-4. Output voltage ripple due to inverter switching
a) Voltage ripple about reference (V)
b) Current into output capacitor (A)

There are two ways to evaluate the regulation of the output voltages: in the time domain and in the frequency domain. The time domain goal is to minimize the output voltage ripple. This is equivalent to minimizing the length (in time) of the active states, since the change in output voltage during an active state is proportional to the time spent charging the output capacitor. The lengths of the active states could be reduced by simply increasing the switching frequency of the inverter; however, this will also increase switching losses. Therefore, the specific goal of an algorithm attempting to improve regulation in the time domain is to minimize the lengths of the active states for a given switching frequency.

The goal of an algorithm being evaluated via the frequency domain is to reduce the harmonic components of the output voltages, particularly those closest to the fundamental frequency. In PWM-switched inverters, harmonics occur at multiples of the switching frequency. Single-phase, tri-level PWM inverters are able to completely eliminate the harmonic component at the switching frequency [17]. The new lowest-order component is

then at twice the switching frequency, and so the *effective* frequency is doubled. Ideally, this performance should be matched by the split-phase inverter. If the lowest order harmonic component cannot be eliminated completely, it should be minimized.

3.2.2 OPTIMIZING SWITCH USAGE

For ease of hardware design and manufacturing, all six switches used in the inverter should be the same. Therefore, current should be shared among the switches as evenly as possible to minimize the thermal ratings required. Specifically, the largest average current carried by any one switch should be minimized. One consequence of this requirement is that shoot-through current should be shared by all three legs of the inverter. In addition, to equalize the switching losses as much as possible, it is desirable that the switching frequencies of all six switches be the same.

3.3 FIRST PROPOSED ALGORITHM

3.3.1 OVERVIEW

This first algorithm attempts to optimize the output voltage regulations from a time domain perspective. Specifically, it is designed to minimize the largest component of ripple for either output voltage. In other words, the goal is to minimize the length, in time, of the longest active state, while successfully controlling the output voltages to their references, and meeting the switch equalization requirements of section 3.2.2. To achieve this goal, a multiple-reference PWM scheme is used, inspired by the three-phase PWM technique for CSIs suggested in [21]. In that case, switching patterns are generated to produce balanced, three-phase output voltages by comparing three modulating references to a triangular carrier signal. Each time the carrier crosses one of the references, one switch is turned on and one is turned off, so that in each complete switching cycle, six transitions are made and each switch turns on and off once. (There are six transitions because the carrier signal is triangular, so it crosses each reference signal twice per cycle.) In order to produce split-phase outputs, the algorithm presented here uses five modulating references instead of three, and a ‘sawtooth’ carrier signal rather than a triangular one, as shown in Fig. 3-5. This algorithm also has

exactly six changes of state per switching period, during which one switch is turned off and one turned on, so minimal switching is achieved.

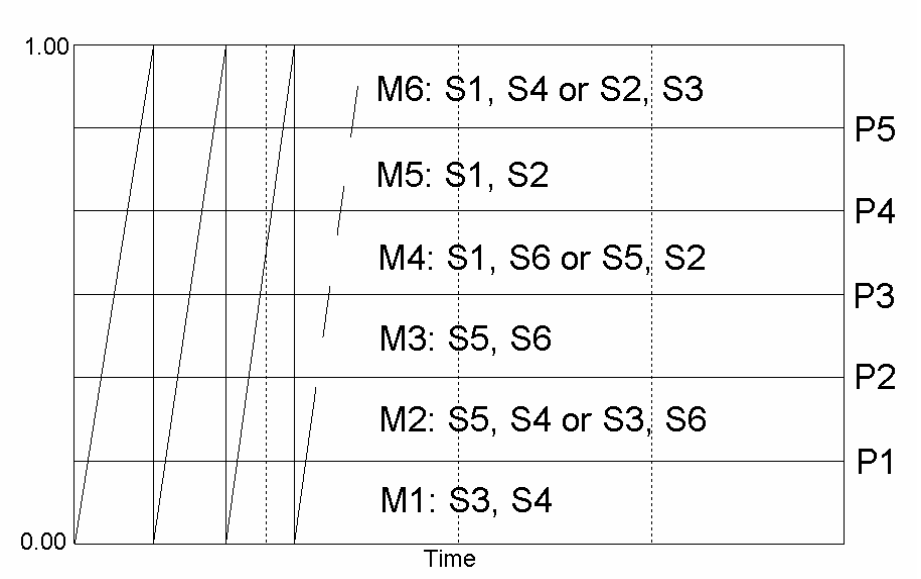

Fig. 3-5. Multiple-reference PWM implementation

3.3.2 DESCRIPTION OF ALGORITHM

Before the reference levels P1 to P5 in Fig. 3-5 can be set, the first step in controlling the split-phase output voltages is to produce two modulating signals, proportional to the desired current in each output. The inverter will then be switched such that the DC current is directed into the two outputs proportionally to these modulating signals. The two signals, *m1* and *m2*, are generated by inputting the errors between the two output voltages and their references to two PI controllers.

As described in section 3.2.1, in order to minimize output voltage ripple, it is desirable to minimize the lengths of the active states for the two outputs, given a constant switching frequency. To accomplish that goal, each of the two half-phases (v_{o1} and v_{o2} in Fig. 3-3) must have two active states in each switching cycle. All six states and the inverter switches that can be turned on during each state are shown in Fig. 3-5. (Switch numbering follows the convention used in Fig. 3-3.) The two active states for the top half-phase, v_{o1}, are M4 and M6. These are the states in which v_{o1} can be actively increased or decreased. The two active states for the bottom half-phase, v_{o2}, are M2 and M6. M6 is shared between the two

outputs and will affect both equally. (The remaining states, M1, M3, and M5, are shoot-through states.) By having two active states, rather than one, for each output, the required length of each individual active state is reduced.

The state transitions and conducting switches in each state can also be represented as a state diagram, as shown in Fig. 3-6. By viewing this diagram, it is clear that one of the two conducting switches remains on during each state transition; so, over a complete switching period, each switch is turned on and off only once. Therefore, all six switches will operate at the same frequency, and switching losses will be minimized.

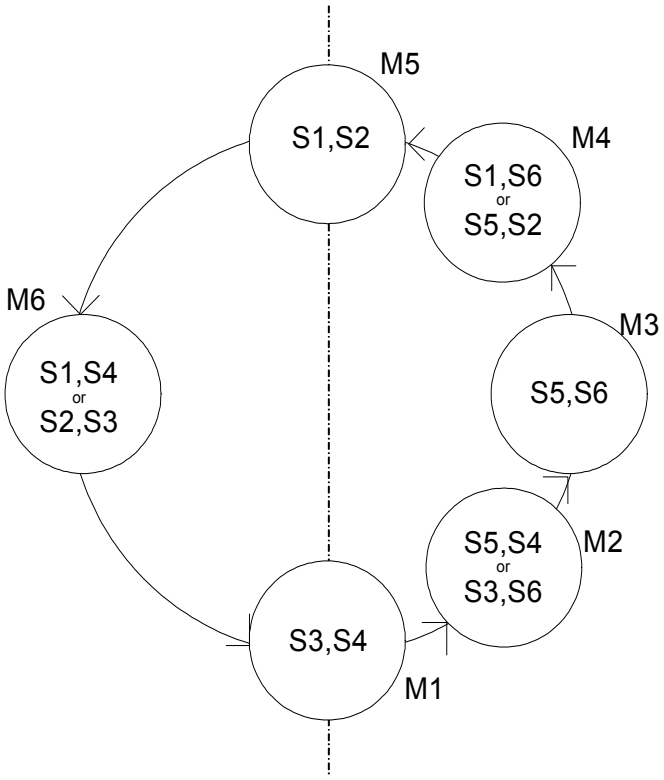

Fig. 3-6. Switching state diagram

As mentioned, the modulating signals *m1* and *m2* are used to control the length of time spent in each state by varying the levels P1 to P5 in Fig. 3-5. To do so, they must be split into a common component that will determine the time period of M6, and individual components that will determine the time periods of M2 and M4. The common component is designated v_{com}, and the two individual components v_{c1} and v_{c2}. The splitting should be done such that

$$v_{com} + v_{c1} = m1, \text{ and}$$
$$v_{com} + v_{c2} = m2. \tag{3-1}$$

This will ensure that the half-phase output currents track the modulating signals as desired.

While the magnitudes of the control signal components determine the time periods of the corresponding active states, their signs determine which of the two possible pairs of switches is turned on during those states. This, in turn, determines whether the affected output or outputs increase or decrease. The effects of the control signal components are summarized in Table 3-1, and Fig. 3-7 illustrates the entire control path as a block diagram.

Table 3-1. Relationship between control signals and outputs

Control Signal Component	Corres-ponding Active State	Affected Output(s)	Control Signal Sign	Conducting Switches	Effect on Output(s)
v_{com}	M6	v_{o1}, v_{o2}	+	S1, S4	Increase
			-	S2, S3	Decrease
v_{c1}	M4	v_{o1}	+	S1, S6	Increase
			-	S2, S5	Decrease
v_{c2}	M2	v_{o2}	+	S4, S5	Increase
			-	S3, S6	Decrease

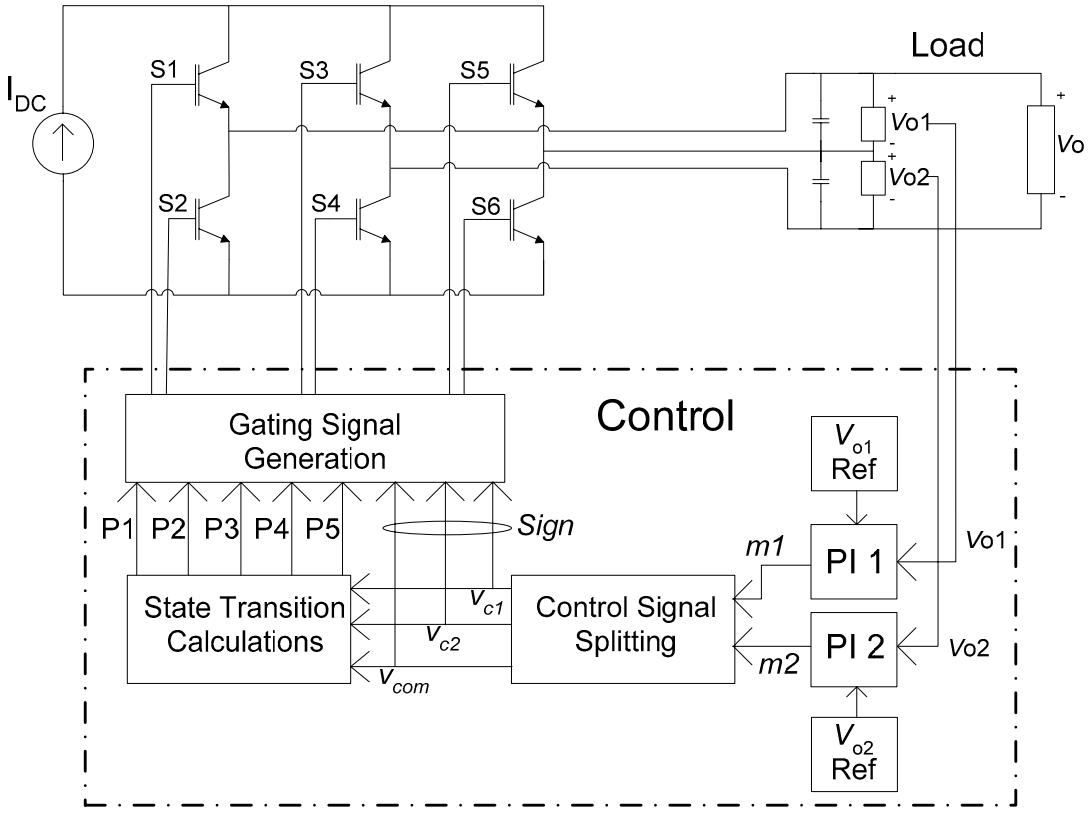

Fig. 3-7. Control path

Any set of control signal components that satisfies (3-1) will produce the desired output voltages. However, to minimize the largest component of output voltage ripple, the length of the longest active state (M2, M4 or M6) must be minimized. In terms of control signal components, this means that the largest of the magnitudes of v_{com}, v_{c1}, and v_{c2} should be minimized, constrained by (3-1). Due to (3-1), whenever one of these signals is reduced, another must increase. Therefore, the result of the minimization will be that two of the three signals will have the same magnitude, which will be greater than or equal to the magnitude of the third signal. As a result, the two longest active states will always have the same length. The control signals can be split into appropriate components using the pseudo-code in Table 3-2.

Table 3-2. Pseudo-code for v_{c1}, v_{c2}, and v_{com}

```
if (sign(m1) = sign(m2))

   if (|m1| > |m2|)
     vcom = m1/2
   else
     vcom = m2/2
   endif

else

   vcom = (m1+m2)/2

endif

vc1 = m1-vcom
vc2 = m2-vcom
```

To equalize conduction losses of the switches, shoot-through current can be split evenly among the three inverter legs. Once the lengths of the active states are set, the remaining time in the switching period is divided equally among the three shoot-through states, M1, M3 and M5. The resulting levels P1 to P5 in Fig. 3-5 will be

$$\begin{aligned} \mathrm{P1} &= \mathrm{S} = \frac{1-|v_{c1}|-|v_{c2}|-|v_{com}|}{3} \\ \mathrm{P2} &= \mathrm{S}+|v_{c2}| \\ \mathrm{P3} &= 2\mathrm{S}+|v_{c2}| \\ \mathrm{P4} &= 2\mathrm{S}+|v_{c1}|+|v_{c2}| = 1-\mathrm{S}-|v_{com}| \\ \mathrm{P5} &= 1-|v_{com}|, \end{aligned} \tag{3-2}$$

where S is the length of each shoot-through state.

3.3.3 SIMULATION RESULTS

3.3.3.1 Linear Loads

This simulation uses a DC current of 20A, 15-μF output capacitors at the top and bottom half-phases, and the following resistive loads:

120V (Top):	30W
120V (Bottom):	270W (2.25A)
240V:	150W (0.625A)
Total:	450W

This degree of load imbalance is not expected under average operating conditions, but is used as a worst-case test. The results are shown in Fig. 3-8. *m1* and *m2* are sinusoidal, demonstrating the linear relationship between them and the output currents. Since the two control signals affect the output currents linearly and do not interfere with each other, they can be generated with relatively low gain to minimize noise. They should also be robust when faced with noise, transients, or nonlinear loads. Note that v_{com}, v_{c1}, and v_{c2} are not expected to be sinusoidal, since it is their combined effect that generates the output currents.

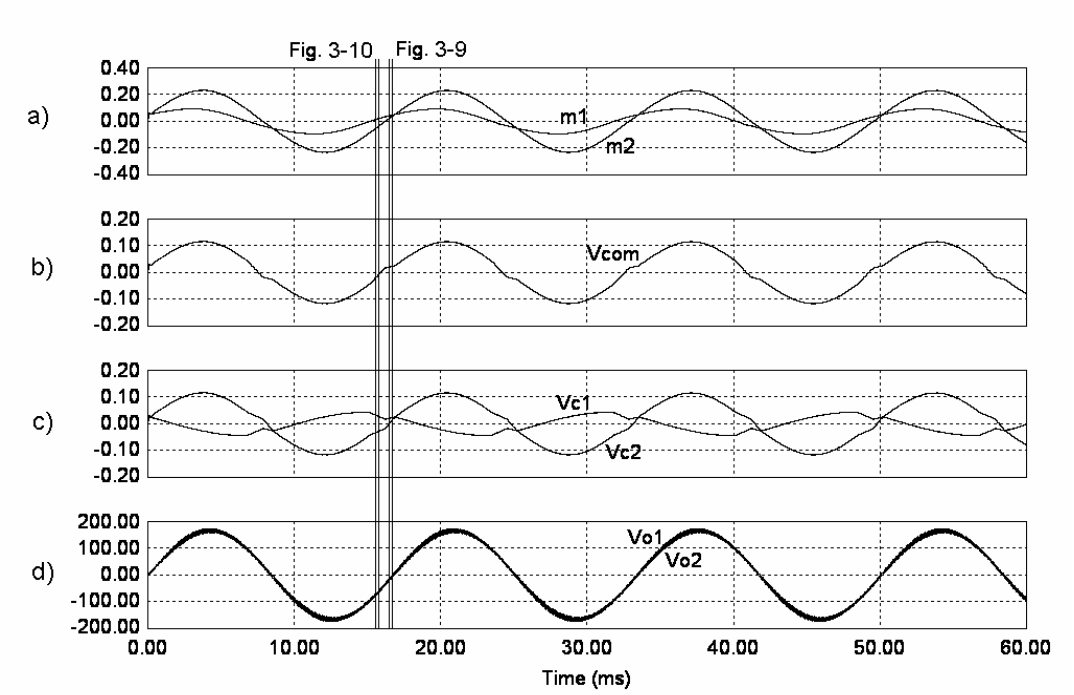

Fig. 3-8. Simulation results for unbalanced, resistive load
a) Modulating signals output from PI controllers
b) Common control signal, v_{com}
c) Individual control signals, v_{c1} and v_{c2}
d) Split-phase outputs, v_{o1} and v_{o2} (V)

Fig. 3-9 investigates the operation of the inverter over a small number of switching periods (marked on Fig. 3-8) at a point in the cycle when $m1 > m2 > 0$. The active states can be identified by sharp increases in one or both of the output voltages. The two longest active states are M6 (when S1 and S4 are conducting and both outputs are increasing) and M4 (when S1 and S6 are conducting and v_{o1} is increasing). As expected, they are of equal length. For comparison, this test was run again with the common active state, M6, manually set to zero. Therefore, there is only one active state for each output: M4 for v_{o1}, and M2 for v_{o2}. The output voltages are shown in Fig. 3-10. Comparing this to Fig. 3-9 e), it is clear that the voltage ripples are larger with only one active state per output, even though the operating frequencies of the switches remain unchanged.

Fig. 3-11 investigates the inverter operation during another period marked on Fig. 3-8, when $m1$ is greater than zero and $m2$ is less than zero. In this case, the longest two active states are M2 (when S3 and S6 are conducting and v_{o2} is decreasing) and M4 (when S1 and S6 are conducting and v_{o1} is increasing). Again, these two longest active states are minimized, so their lengths are equal. By examining the figure, it is clear that the ripple of v_{o1} is not optimal in this case; however, any improvement of v_{o1} would result in larger ripple of v_{o2}, so this is the optimal solution.

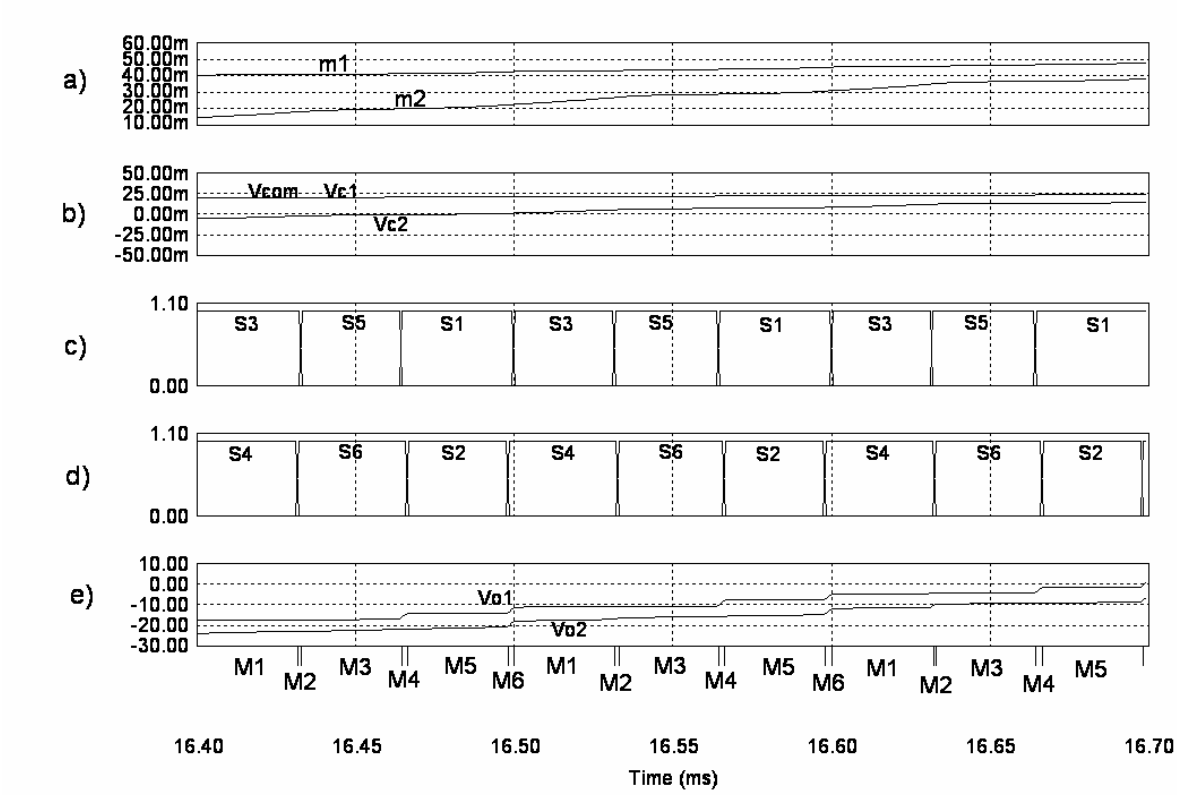

Fig. 3-9. Switching results for $m1 > m2 > 0$
a) Modulating signals
b) Control signal components
c) Gating signals for upper switches
d) Gating signals for lower switches
e) Output voltages (V)

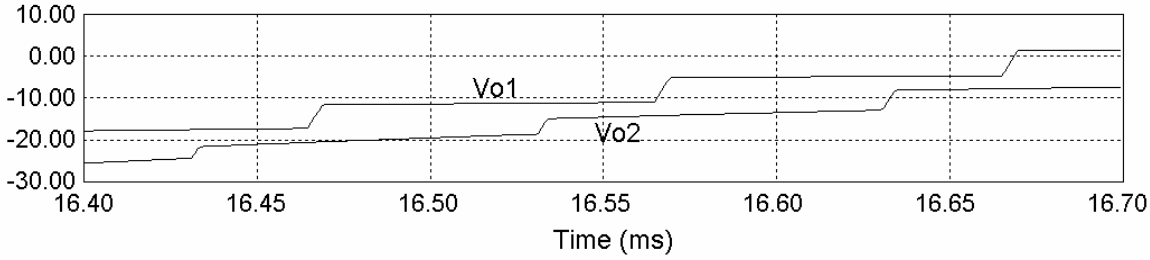

Fig. 3-10. Voltage ripple with only one active state for each output (V)

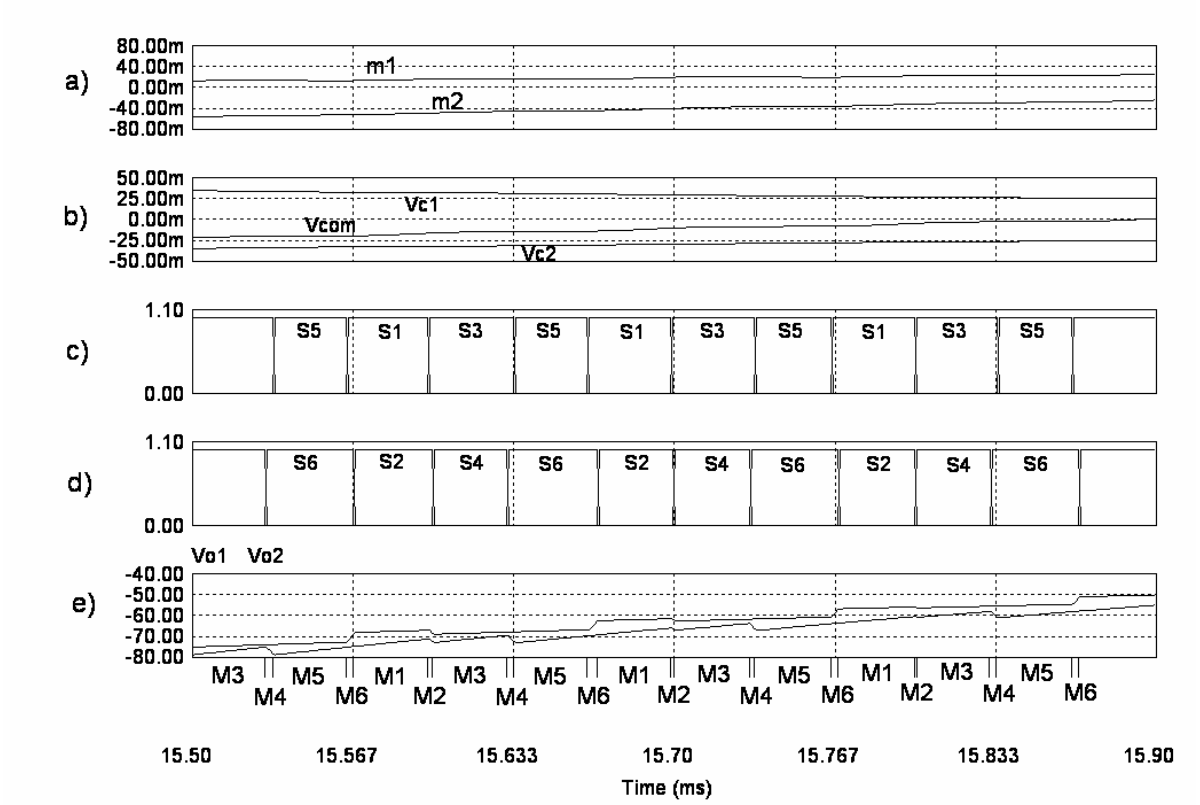

Fig. 3-11. Switching results for $m1>0$, $m2<0$
a) Modulating signals
b) Control signal components
c) Gating signals for upper switches
d) Gating signals for lower switches
e) Output voltages (V)

In Fig. 3-12, the Fourier transforms of the output voltages are investigated. Although the voltage ripple in the time domain has been mitigated, there still exists a significant harmonic component at the switching frequency of 10kHz. There are two causes for this harmonic component. Although there are two active states per switching cycle, the active states are not evenly spaced in time, as they are with single-phase, tri-level inverters. Also, only the largest ripple component is being minimized, so at least one of the two outputs will always have one active state longer than the other. The frequency domain results for this method are therefore not identical to those of single-phase, tri-level PWM inverters, with 'double effective switching frequency'. They do, however, show an improvement over a method using only one active state per output. Fig. 3-13 shows the frequency domain analysis of Fig. 3-10, where the M6 active state was eliminated. By comparing Fig. 3-12 to Fig. 3-13, it

is seen that the addition of the third, common active state significantly reduces the harmonic components of the noisier output, v_{o2}, at the expense of some increase in the harmonics of v_{o1}.

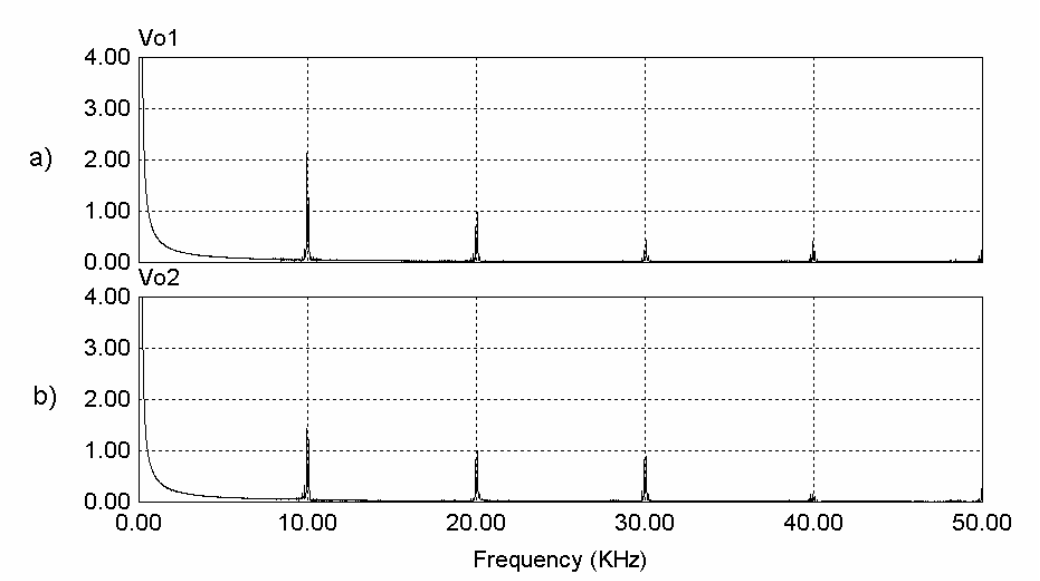

Fig. 3-12. Frequency domain results
a) Frequency response of top output, v_{o1} (V)
b) Frequency response of bottom output, v_{o2} (V)

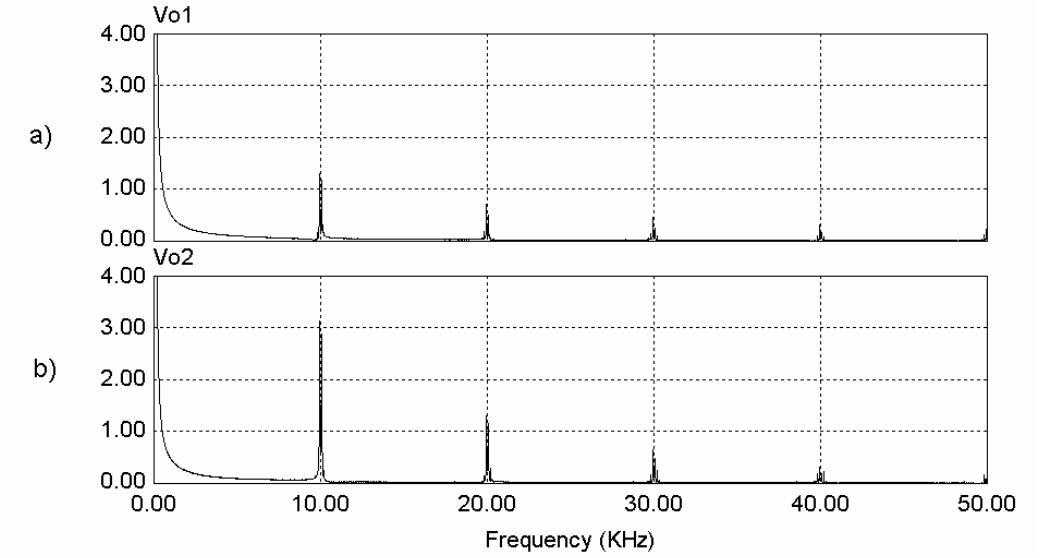

Fig. 3-13. Frequency domain results with M6 active state set to zero
a) Frequency response of top output, v_{o1} (V)
b) Frequency response of bottom output, v_{o2} (V)

3.3.3.2 Non-linear Load

In this simulation, the following arrangement is used to demonstrate the inverter's performance with a non-linear load:

120V (Top):	Diode Rectifier with
	200-μF filter capacitor and
	100-W resistive load
120V (Bottom):	200-W resistive load
240V:	150-W resistive load
Total:	450W

The results are given in Fig. 3-14. It is clear that the output voltages remain properly regulated and balanced in the presence of a significantly non-linear load at one output.

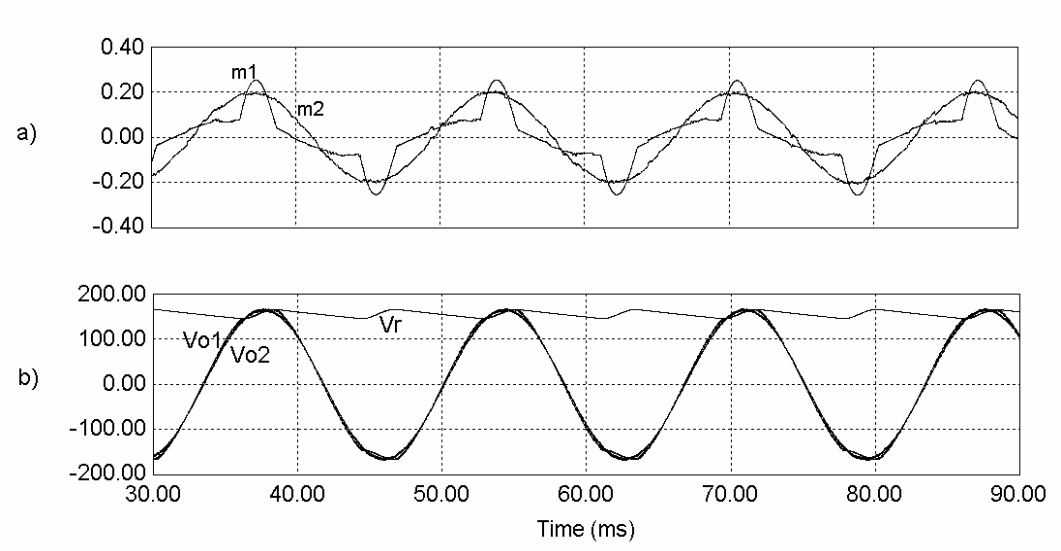

Fig. 3-14. Inverter operation with non-linear load
a) Modulating Signals *m1* and *m2*
b) Output voltages v_{o1} and v_{o2}, and rectifier output voltage, v_r (V)

3.3.4 EXPERIMENTAL RESULTS

The following experimental results were produced using the same experimental prototype as described in section 2.7. Further details on this experimental design, including specific design and control challenges overcome, are given in Chapter 4.

Two test cases are given. The first test, with results shown in Fig. 3-15, is identical to the first simulation of section 3.3.3. The two output voltages are sinusoidal, nearly in phase, and successfully balanced despite the severely unbalanced loading conditions. The RMS values of v_{o1} and v_{o2} are 120V and 117V, respectively. Note that the modulating signals are given for demonstration purposes only; the actual signals are digital and do not exhibit the noise seen here. In Fig. 3-16, a 31.5-mH inductor is added in series with the resistor of the bottom half-phase to show that the inverter functions equally well with inductive loads. This changes the load for the bottom output to 257.4W and 57.3Var. The top and 240-V loads remain at 30W and 150W, respectively. Again, the outputs voltages are seen to be well balanced, regardless of the significantly different current magnitude and phase at each output. In this case the RMS values are 120V and 115V. The same controller gains are used for both outputs, and they are left unchanged for both tests:

$$m_1 = 0.0035 v_{e1} + 2\frac{v_{e1}}{s} \quad \text{and}$$

$$m_2 = 0.0035 v_{e2} + 2\frac{v_{e2}}{s}, \tag{3-3}$$

where v_{eX} is the error of output voltage X (i.e. the difference between that voltage and its reference level).

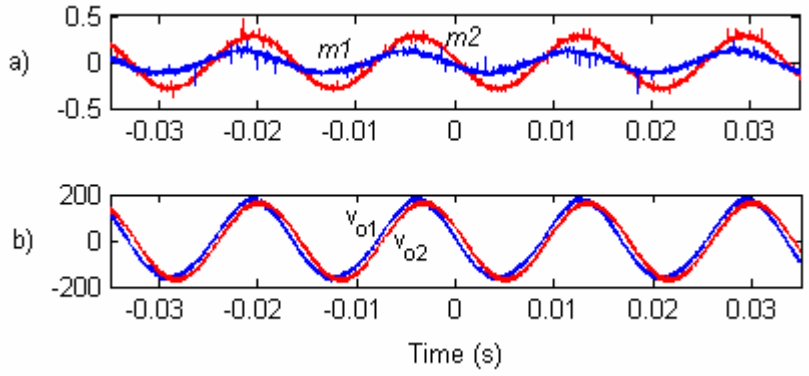

Fig. 3-15. Experimental results: resistive loads
a) Modulating signals *m1* and *m2*
b) Output voltages v_{o1} and v_{o2} (V)

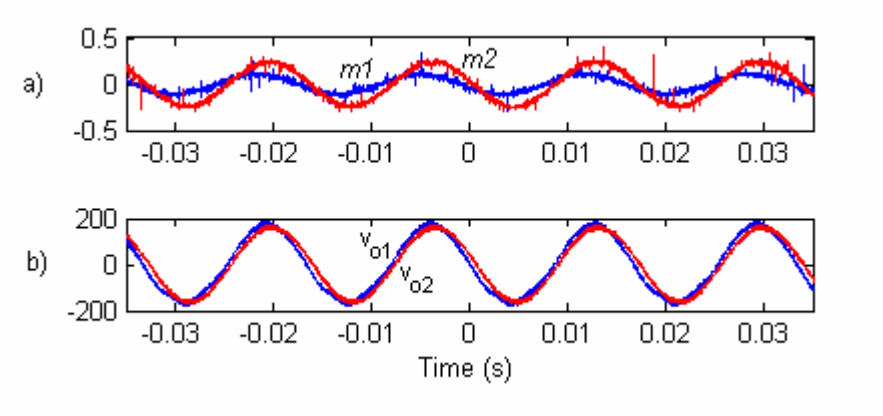

Fig. 3-16. Experimental results: Inductive and resistive loads
a) Modulating signals *m1* and *m2*
b) Output voltages v_{o1} and v_{o2} (V)

3.3.5 DISCUSSION

3.3.5.1 Optimal Limits for Control Signals

The lengths of the active states, M2, M4, and M6, are set according to the control signal components, v_{c1}, v_{c2}, and v_{com}, as described in section 3.3.2. The remainder of the switching period is divided evenly among the three shoot-through states, M1, M3, and M5. As can be seen in Figs. 3-9 and 3-11, the shoot-through states normally make up the majority of the period, so under normal conditions the control signals should not require limiting. However, during periods of very high current draw at the outputs, such as during a turn-on transient, it is possible that the sum of the control signal components will exceed 1. Without limits, this would result in the sum of the active states being longer than the switching period.

The simplest way to keep the control signals within acceptable limits is to limit the magnitudes of the two modulating signals generated by the PI controllers, *m1* and *m2*, to 0.5 each. Given the algorithm for separating these signals (Table 3-2), this will ensure that the sum of v_{c1}, v_{c2} and v_{com} is less than 1. However, these limits are not optimal because, generally, the modulating signal magnitudes could be higher than 0.5 without the sum of the control signal components being greater than one. For example, if *m1*=0.5, *m2* could be as high as 1 without the sum of the control signal components exceeding 1. (This can be verified using the pseudo-code in Table 3-2.)

A better approach would be to limit the modulating signal with the higher magnitude, based on the value of the smaller signal. If the signs of the two modulating signals are the same, the smaller signal's magnitude would be limited only to 1. The limit of the larger signal's magnitude would then be

$$\left|m_H\right|_{\max} = \frac{2}{3}\left(\left|m_L\right| + 1\right) \tag{3-4}$$

or 1, whichever is less. (m_H is the magnitude of the larger signal, and m_L is that of the smaller signal.) If the signs of the two modulating signals are different, the lower magnitude would be limited to 0.5 and the higher would be limited to

$$\left|m_H\right|_{\max} = \frac{2 - \left|m_L\right|}{3}. \tag{3-5}$$

These equations produce the maximum possible limits that will keep the sum of the control signal components, calculated as in Table 3-2, below one. However, the results could be improved still further by modifying the algorithm of Table 3-2. The original algorithm was designed to split the active states in such a way as to minimize the greatest component of output voltage ripple. However, if the control signals are being limited, the output voltages will be distorted, which is clearly a greater concern than high-frequency voltage ripple. Therefore, at times when the limits of equations (3-4) and (3-5) would be hit using the algorithm of Table 3-2, that algorithm can be modified to allow greater limits, at the cost of increased output voltage ripple. The modified algorithm is given in Table 3-3.

Table 3-3. Pseudo-code for v_{c1}, v_{c2}, and v_{com}, including optimal limits

```
/*
 * Absolute maximum limits
 */
if (|m1| > 1) |m1| = 1
if (|m2| > 1) |m2| = 1

/*
 * When signs of m1 and m2 are different,
 * the sum of their magnitudes must be < 1
 */
mH = max(|m1|,|m2|)
mL = min(|m1|,|m2|)

if (sign(m1) != sign(m2) && |m1|+|m2| > 1)
   if (mL > 0.5) mL = 0.5
   if (mH > 1-mL) mH = 1-mL
endif

/*
 * Calculate control signal components
 * vcom, vc1, vc2
 */
if (sign(m1) = sign(m2))
   if (|m1| > |m2|)
      vcom = m1/2
   else
      vcom = m2/2
   endif
else
   vcom = (m1+m2)/2
endif

vc1 = m1-vcom
vc2 = m2-vcom

/*
 * Redistribute signals, if necessary
 */
diff = |vcom| + |vc1| + |vc2| - 1

if(diff > 0)
   if (sign(m1) = sign(m2))
      if (|vcom| > mL) |vcom| = |vcom|-diff
      else |vcom| = |vcom|+diff
   else
      |vcom| = |vcom| - diff
   endif

   vc1 = m1-vcom
   vc2 = m2-vcom
endif
```

This algorithm functions in three steps. First, absolute limits are set. If *m1* and *m2* have the same sign, their magnitudes are each limited to 1. If they have different signs, the sum of their magnitudes is limited to 1. Once the limits have been set, the control signal components are calculated just as previously described in Table 3-2. Finally, if the sum of these components is greater than one, the balance between the common component (v_{com}) and individual components (v_{c1}, v_{c2}) is shifted in order to reduce their sum while maintaining the relationships of equations (3-1).

3.3.5.2 Improved Current Sharing

The goal of current sharing is to equalize the conduction losses in the six switches of the inverter as closely as possible. In the control scheme described above, the shoot-through current was divided evenly among the three legs of the inverter. Due to the low modulation indexes, shoot-through current represented the majority of the current conducted, resulting in similar total current in each switch. A better result would be obtained by minimizing the largest average current carried by any of the six switches. Optimal current sharing would be achieved in the following manner:

- Using the values calculated for v_{c1}, v_{c2} and v_{com}, determine the on-period of each switch during the active (non-shoot-through) states, M2, M4, and M6.
- Determine which of the two switches in each leg – S1-S2, S3-S4, and S5-S6 is on for a longer total time in each switching period.
- Instead of sharing the remaining time equally among the shoot-through states, M1, M3 and M5, share it in such a way that these three more heavily-loaded switches carry equal current.

3.3.5.3 Adaptation of Advanced *V-to-I* Algorithm for Split-Phase CSI

In order to use the advanced algorithm presented in 2.8 with this inverter, two small changes should be made. The first is that the instantaneous reflected voltage in this case is

$v_{o1}m1 + v_{o2}m2$, rather than $v_o m$ as in the single phase case. Everywhere that $v_o m$ appears in equations (2-28) to (2-36), it should be replaced with $v_{o1}m1 + v_{o2}m2$.

The second change involves synchronizing the inductor-charging states, particularly charging from the capacitor, with periods of high reflected voltage in order to reduce current ripple. The single-phase inverter had only one active state, so this was straightforward. The split-phase inverter has three active states, M2, M4 and M6. The highest instantaneous reflected voltage occurs during the active state M6, when both output capacitors are being charged or discharged (section 3.3). Therefore, the $t_{on,C}$ period, if it is present, or otherwise the $t_{on,S}$ period, should coincide with M6. This can be accomplished in a straightforward manner if the period of the *V-to-I* circuit, T, is set equal to the switching period of the inverter. If the beginning of the inverter switching cycle is shifted to M6, and the *V-to-I* control cycle is set to always begin with $t_{on,C}$ followed by $t_{on,S}$, they will coincide as desired. Of course, charging time of the capacitor (t_{charge}) must still coincide with shoot-through states, and, over several periods, capacitor-charging should be done in all three shoot-through states equally to equalize switching losses.

3.3.5.4 Adaptation to Voltage-Sourced Inverters

The methodology introduced here could be adapted to voltage-sourced inverters, such as that shown in Fig. 1-3. (In the VSI case, there would be two active states and two off-states in each switching cycle, rather than three active and three shoot-through states.) It has been tested by simulation and produces well-regulated outputs. Benefits would include compensation for unequal line losses at each output and, if desired, the capability of generating two AC voltage outputs of different magnitudes and/or phases from a single DC voltage supply. However, the primary benefit of this method for current-sourced inverters is that it can generate balanced (equal) output voltages given unbalanced loading conditions. In the VSI case, this is not required since the output voltages are not significantly affected by the load impedances. Therefore, this method's usefulness for voltage-sourced inverters is confined to special cases.

3.4 SECOND PROPOSED ALGORITHM

After work on the algorithm described in section 3.3 was completed, it was realized that the multiple-reference PWM method for three-phase current-sourced inverters in [21] could be applied more directly to the split-phase case. Initially, a direct implementation was not considered because of the different output requirements for three-phase and split-phase inverters. However, it will be shown in this section that the method can be applied directly, with one significant modification, and that it may be preferable to the algorithm described in section 3.3.

3.4.1 REVIEW OF ALGORITHM FOR THREE-PHASE INVERTERS

The control algorithm for three-phase current-sourced inverters described in [21] uses a three-leg inverter identical to that used to produce split-phase outputs throughout this chapter. The circuit diagram for such an inverter is shown again in Fig. 3-17, with the legs and switches labeled in a conventional manner for three-phase inverters. (Note that the positions of legs B and C have been swapped from section 3.3.)

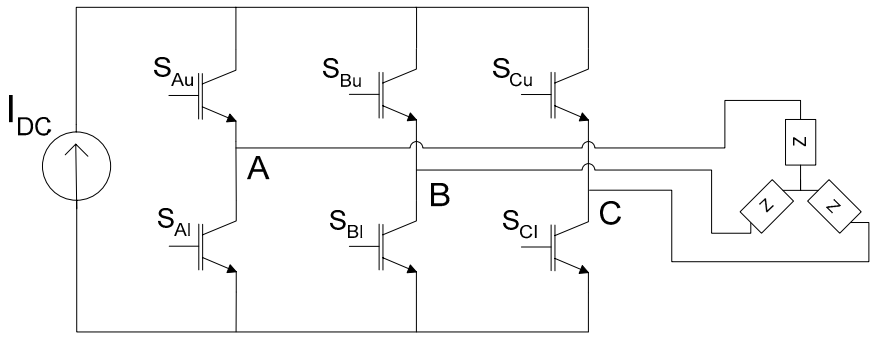

Fig. 3-17. Standard three-leg, three-phase CSI

The algorithm is designed to generate 3-phase current waveforms that are balanced and sinusoidal. To do this, the output line currents are modulated using the line-to-line voltages between three control signals, as shown in Fig. 3-18. The three control signals v_a, v_b, and v_c are compared to a high frequency triangular carrier wave, v_t (not shown). Discounting shoot-through, there are 6 possible regions of operation, corresponding to the 6 possible current paths from one phase of the inverter to another phase. For example, as seen in Fig.

3-18, when $v_a > v_t > v_b$, current flows out of phase A (and into either phase B or C). When $v_c > v_t > v_b$, current flows into phase B (and out of either phase A or C). In the diagram, the region described by the intersection of these two inequalities is labeled **A-B**. Whenever the triangular carrier wave is in this region, current will flow from phase A to phase B (i.e. switches S_{Au} and S_{Bl} will be on). It can be seen that the current in each phase will be proportional to the line-to-line voltage between two of the control signals.

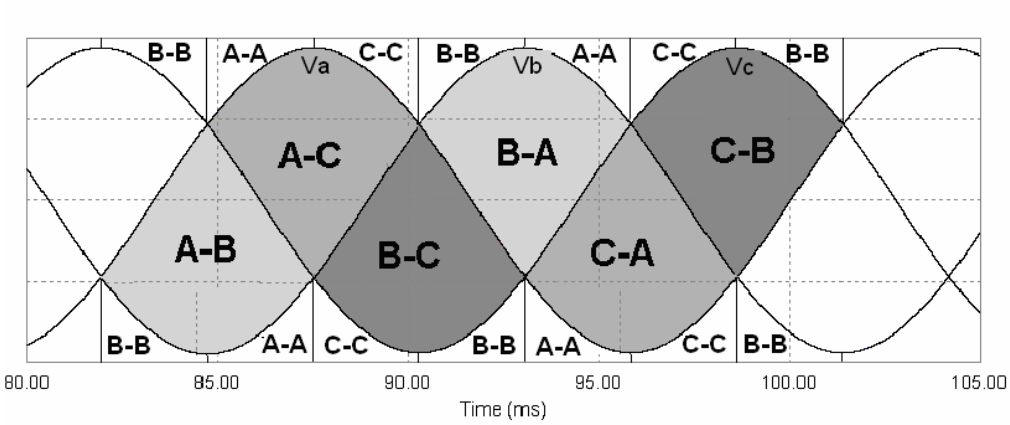

Fig. 3-18. Three-reference PWM for three-phase current-sourced inverters

When the carrier signal is outside of the regions bounded by the control signals, the DC current requires an alternate, shoot-through path. The shoot-through leg is chosen based on the current position in the 120-Hz cycle. For example, whenever the v_a control signal is between v_b and v_c, which occurs for one third of the cycle, shoot-through current will use leg B. This is denoted by **B-B** in Fig. 3-18. During this shoot-through state, switches S_{Bu} and S_{Bl} will be on.

The preceding rules result in the following logic functions for the 6 switches:

$$\begin{aligned} S_{Au,1} &= v_a > v_t > v_b \\ S_{Al,1} &= v_b > v_t > v_a \\ S_{Bu,1} &= v_b > v_t > v_c \\ S_{Bl,1} &= v_c > v_t > v_b \\ S_{Cu,1} &= v_c > v_t > v_a \\ S_{Cl,1} &= v_a > v_t > v_c \end{aligned} \tag{3-6}$$

$$
\begin{aligned}
S_{Au} &= S_{Au,1} + \{O \cdot [(v_a > v_c > v_b) + (v_b > v_c > v_a)]\} \\
S_{Al} &= S_{Al,1} + \{O \cdot [(v_a > v_c > v_b) + (v_b > v_c > v_a)]\} \\
S_{Bu} &= S_{Bu,1} + \{O \cdot [(v_a > v_b > v_c) + (v_c > v_b > v_a)]\} \\
S_{Bl} &= S_{Bl,1} + \{O \cdot [(v_a > v_b > v_c) + (v_c > v_b > v_a)]\} \\
S_{Cu} &= S_{Cu,1} + \{O \cdot [(v_b > v_a > v_c) + (v_c > v_a > v_b)]\} \\
S_{Cl} &= S_{Cl,1} + \{O \cdot [(v_b > v_a > v_c) + (v_c > v_a > v_b)]\}
\end{aligned}
\tag{3-7}
$$

$$
O = \overline{S_{Au,1} + S_{Al,1} + S_{Bu,1} + S_{Bl,1} + S_{Cu,1} + S_{Cl,1}} \tag{3-8}
$$

$S_{Au,1}$ to $S_{Cl,1}$ are the preliminary functions not taking into account shoot-through conditions. S_{Au} to S_{Cl} are the final gating signals applied to the IGBTs' gates.

This algorithm accomplishes many of the same goals laid out for split-phase inverters in section 3.2. At each switching point, when the triangular carrier crosses one of the control signals, only one switching transition occurs; one of the two conducting switches remains on at each transition, resulting in minimal switching. Shoot-through current is shared evenly among the three legs of the inverter, on average over each 120-Hz cycle, equalizing conduction losses. While the switches do not all operate at the same frequency over each switching period, the averages of their switching frequencies over a 120-Hz cycle are the same, and so their switching losses will be comparable. Finally, because a triangular carrier signal is used, the carrier passes between the control signals twice per switching period, resulting in two active states per output in each switching period, thereby doubling the effective switching frequency.

3.4.2 APPLICATION OF THREE-PHASE METHOD TO SPLIT-PHASE INVERTER

In order to apply the above technique to a split-phase inverter, it is necessary to generate the control signals v_a, v_b, and v_c. As in section 3.3, the first step is to generate two modulating signals, *m1* and *m2*, using PI controllers. (More advanced feedback control methods could be used instead, if desired.) The inputs to the PI controllers are the differences between the output voltages and their respective references. As with the method

in section 3.3, these modulating signals are proportional to the required currents in the two outputs.

As can be seen in Fig. 3-19, the current *into* the v_{o1} output capacitor is equivalent to the phase A current. Likewise, the current *out* of the v_{o2} output capacitor is equivalent to the phase C current. Therefore, the top output current is equal to the phase A current, i_A, and the bottom output current is equal to the opposite of the phase C current, or $-i_C$.

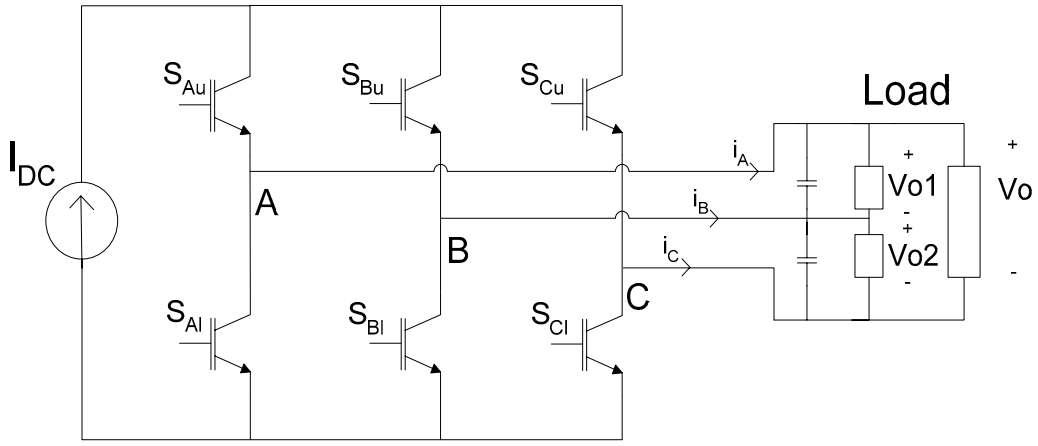

Fig. 3-19. Split-phase CSI with switches and legs labelled in the three-phase format

Using the three-phase switching algorithm from [21], illustrated in Fig. 3-18, the phase A current will be proportional to the difference between the v_a and v_b control signals. The phase C current will be proportional to the difference between the v_c and v_a control signals. Therefore, the following equations can be written:

$$\begin{aligned} v_a - v_b &= m1 \\ v_c - v_a &= -m2 \end{aligned} \tag{3-9}$$

In addition, it is desirable that

$$v_a + v_b + v_c = 0 \tag{3-10}$$

so that the two shoot-through states will be of approximately equal length. Solving for the three control signals results in

$$v_a = \frac{m1 + m2}{3}$$
$$v_b = \frac{m2 - 2m1}{3} \qquad (3\text{-}11)$$
$$v_c = \frac{m1 - 2m2}{3}.$$

Fig. 3-20 shows the results when the method from [21] is applied directly, using these control signals. The output loads are as in section 3.3.3.1:

120V (Top):	30W
120V (Bottom):	270W
240V:	150W
Total:	450W

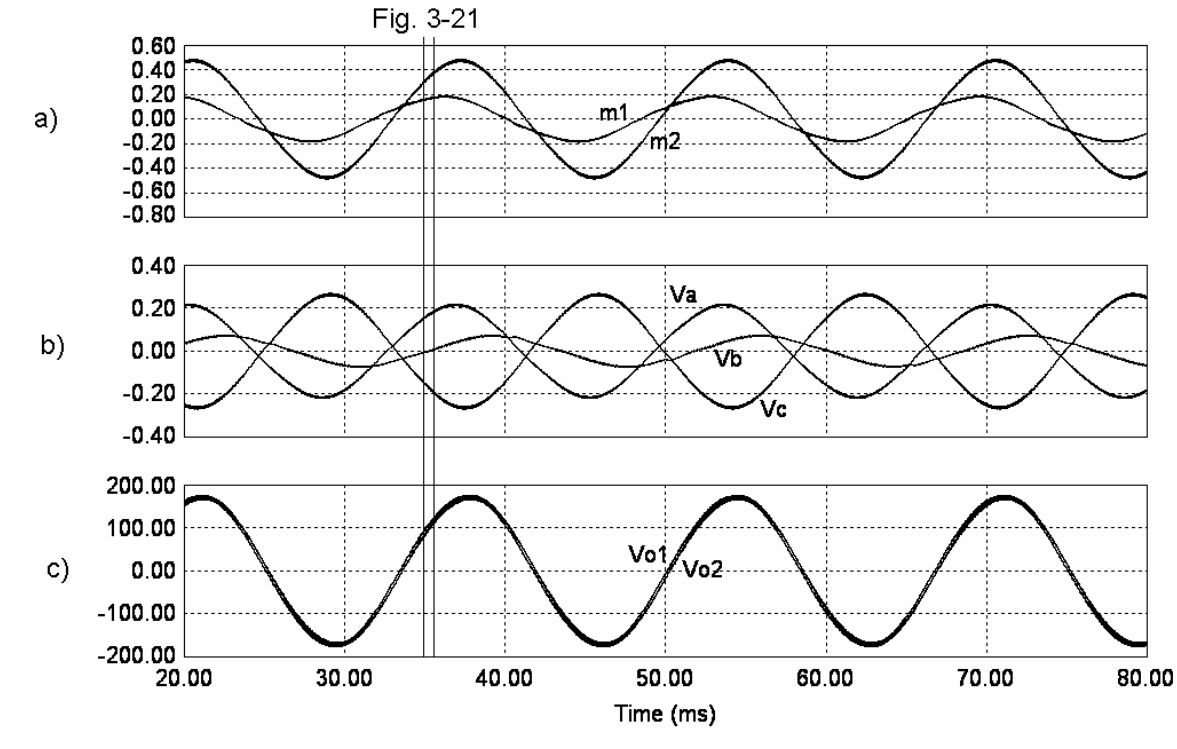

Fig. 3-20. Simulation results using three-phase algorithm to produce split-phase outputs
a) Modulating signals
b) Derived control signals
c) Output voltages (V)

Clearly, the output voltages are successfully regulated. Fig. 3-21 zooms in on a small section of these results, marked in Fig. 3-20, to show the switching action.

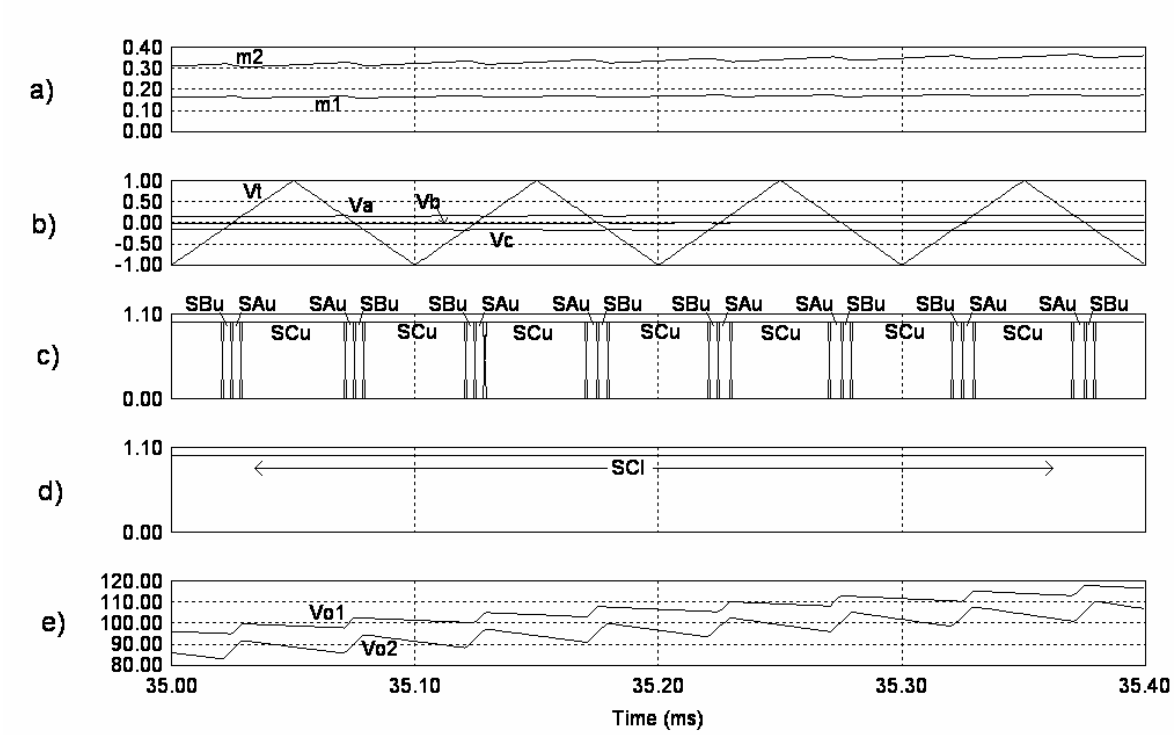

Fig. 3-21. Individual switching events from previous figure
a) Modulating signals
b) Derived control signals
c) Gating signals for upper switches
d) Gating signals for lower switches
e) Output voltages (V)

Fig. 3-21 illustrates why a modification must be made to this method to make it suitable for split-phase generation. The inverter leg used for shoot-through current is determined based on which of the three control signals, v_a, v_b, and v_c, is between the other two during the shoot-through period. In the three-phase case, the outputs and, therefore, the control signals are balanced. As a result, each of the three control signals spends approximately the same amount of time as the other two in the middle position, and so each shoot-through state is used equally, as seen in Fig. 3-18. In the split-phase case, however, to produce the desired outputs, the control signals must be nearly in phase. Therefore, one of the three signals

remains in the middle position for the majority of the period: in this case, v_b. The result is that the C leg carries the majority of the shoot-through current. During the time period examined by Fig. 3-21, in fact, all shoot-through current is carried by leg C. Consequently, switches S_{Cu} and S_{Cl} will have much higher conduction losses than the other switches.

3.4.3 APPLICATION OF THREE-PHASE ALGORITHM WITH EQUAL CURRENT SHARING

In order for this algorithm to be applied to unbalanced three-phase circuits, of which split-phase is an extreme example, a different method must be developed for sharing the shoot-through current. Such a method must satisfy two requirements. First, the three inverter legs must, on average, carry equal shoot-through current. Second, minimal switching must be maintained, i.e., only one switch can turn off and one can turn on at each switching transition, keeping one of the two conducting switches on.

To meet the minimal switching requirement, one of only two legs can be used for any given shoot-through state because one of the switches in the leg must already be on during the preceding active state. For example, consider the case shown in Fig. 3-21. The 'top' shoot-through state (when the triangular carrier is greater than all three control signals) transitions to and from the top active state, where switches S_{Au} and S_{Cl} are turned on. Therefore, only leg A or leg C can be used for this shoot-through state. (In Fig. 3-21, only leg C is used, satisfying the minimum switching requirement, but not the current-sharing requirement.) Likewise, in the bottom active state, switches S_{Bu} and S_{Cl} are turned on, so only leg B or leg C can be used for the bottom shoot-through state.

Shoot-through current can be equalized by alternating between the allowable legs for shoot-through states. First, it is necessary to determine the allowable legs for the top and bottom shoot-through states for all configurations of the control signals. The allowable legs for the top shoot-through state depend on which of the three control signals is the highest. For example, whenever v_a is greater than both v_b and v_c, the top active state will be in the region marked **A-C** in Fig. 3-18. During this top active state, current will travel from phase A to phase C, and so switches S_{Au} and S_{Cl} will be on. Therefore, whenever v_a is higher than the other two control signals, legs A and C are the allowable legs for the top shoot-through

state. Similarly, the allowable legs for the bottom shoot-through state depend on which of the three control signals is the lowest (the most negative). The allowable legs to carry shoot-through current for all configurations of the control signals can be determined by examining Fig. 3-18, and are given in Table 3-4.

Table 3-4. Allowable inverter legs to be used for each shoot-through state, to maintain minimal switching

Highest Control Signal	Allowable Legs for Top Shoot-Through State
v_a	A, C
v_b	A, B
v_c	B, C

Lowest Control Signal	Allowable Legs for Bottom Shoot-Through State
v_a	A, C
v_b	A, B
v_c	B, C

Note that the legs that can be used in the top shoot-through state when a given control signal is the highest are the same as those that can be used in the bottom shoot-through state when the same control signal is the lowest; i.e., when v_a is greater than the other two control signals, legs A or C can be used for the top shoot-through state, and when v_a is less than the other two control signals, legs A or C can be used for the bottom shoot-through state.

The next step is to determine a method for alternating the shoot-through states between these allowable legs. This can be done as follows. A continuous record is kept of the legs used in the previous two shoot-through states. At each new shoot-through state, one of the two allowable legs from Table 3-4 is chosen based on which one had been used least recently. For example, at the beginning of the top shoot-through state, if v_b is greater than v_a and v_c, the two allowable legs are A and B, from Table 3-4. If leg B was used for the preceding shoot-through state, then A would be used this time. If neither leg was used for the preceding shoot-through state (because leg C was used), then the state prior to that would be checked. Again, if leg B was used that time, then leg A would be used now.

Figs. 3-22 through 3-24 show the results of this new method. Fig. 3-22 is identical to Fig. 3-20, as expected, since only shoot-through current has been altered. Fig. 3-23 covers the

same time period as Fig. 3-21. Clearly the shoot-through current is now divided evenly among the three legs. It can also be seen that only one transition between switches is made at each crossing of a control signal by the triangular carrier; therefore, minimal switching is maintained. It should be noted that during this time period, switches S_{Au}, S_{Bu}, and S_{Cl} operate at twice the frequency of the other switches. However, this is not a concern because during the opposite half-cycle the opposite is true, as seen in Fig. 3-24. On average, the operating frequencies of all six switches are the same, as desired.

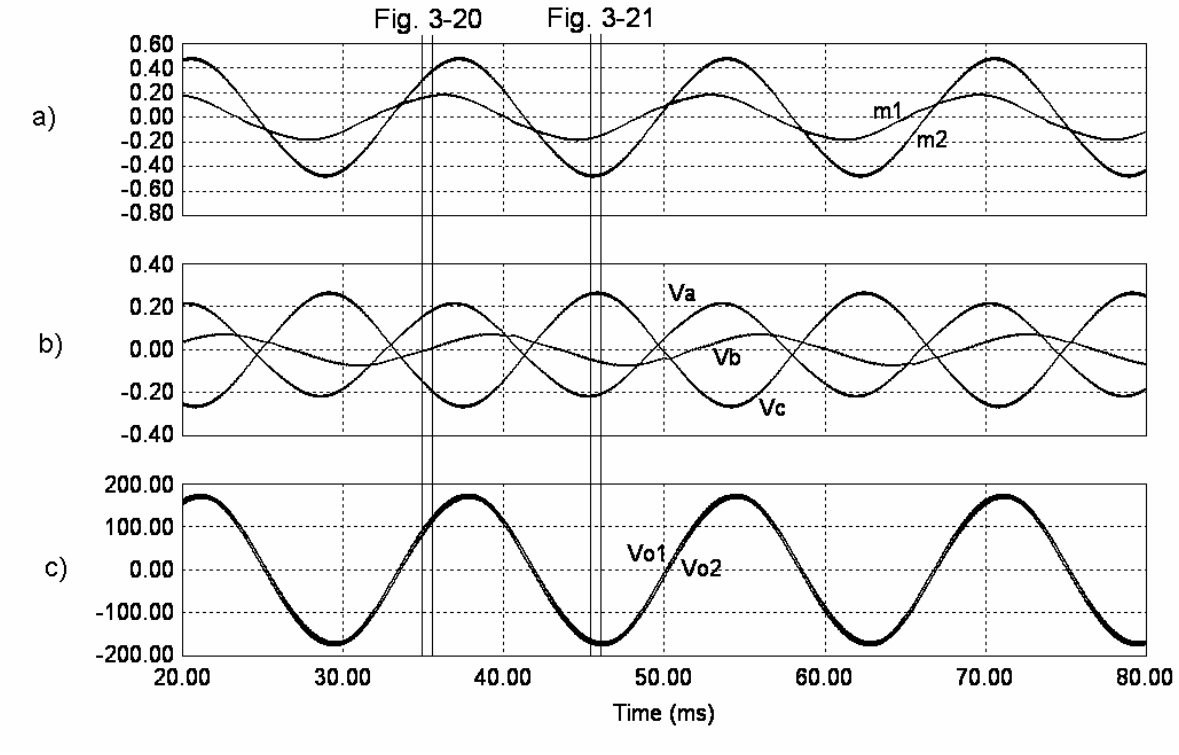

Fig. 3-22. Simulation results with modification of shoot-through states
a) Modulating signals
b) Derived control signals
c) Output voltages (V)

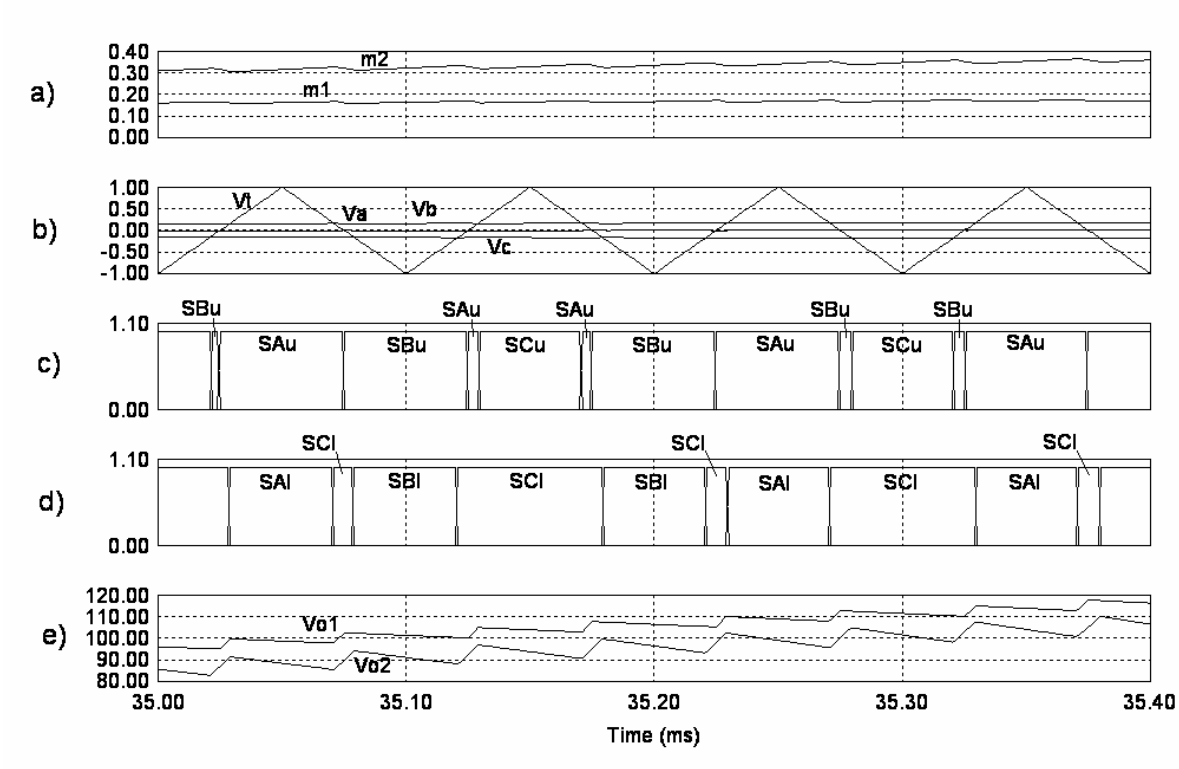

Fig. 3-23. Individual switching events showing modified shoot-through states, positive half-cycle
a) Modulating signals
b) Derived control signals
c) Gating signals for upper switches
d) Gating signals for lower switches
e) Output voltages (V)

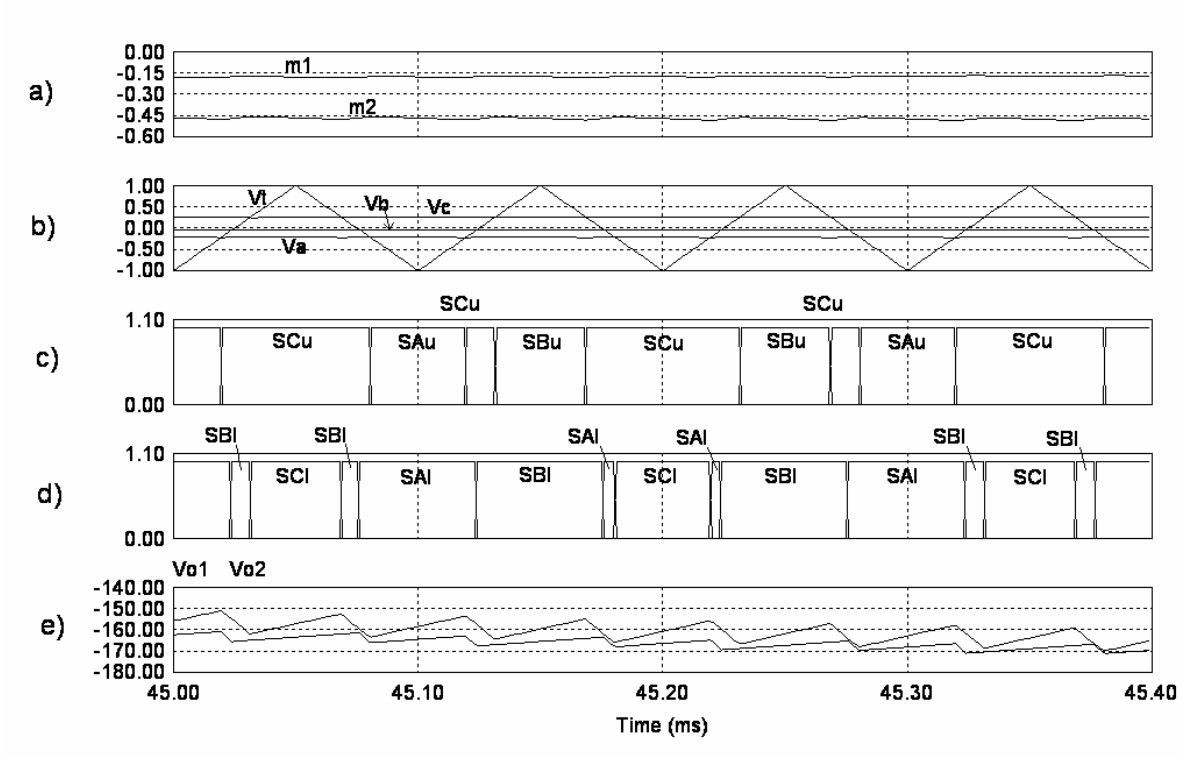

Fig. 3-24. Individual switching events showing modified shoot-through states, negative half-cycle
a) Modulating signals
b) Derived control signals
c) Gating signals for upper switches
d) Gating signals for lower switches
e) Output voltages (V)

The frequency domain results of this simulation are given in Fig. 3-25. Unlike with the method presented in section 3.3, the harmonic component at the switching frequency of 10kHz has essentially been eliminated. The lowest frequency switching harmonic is now at 20kHz.

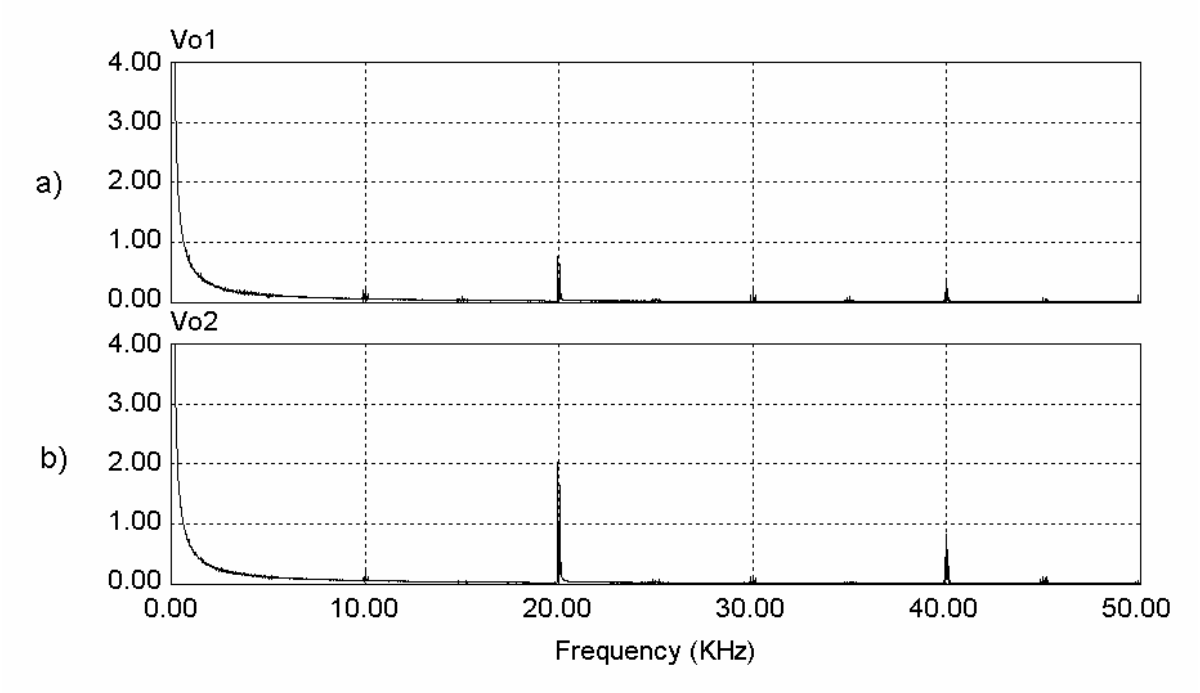

Fig. 3-25. Frequency domain results for the second method
a) Frequency response of top output, v_{o1} (V)
b) Frequency response of bottom output, v_{o2} (V)

3.4.4 ADDITIONAL SIMULATION RESULTS

This section shows the simulation results with inductive and nonlinear loads. In Fig. 3-26, a 31.5-mH inductor was connected in series with the bottom resistive load, resulting in the following loads:

120V (Top):	30W
120V (Bottom):	257.4W + 57.3Var
240V:	150W
Total:	437.4W + 57.3Var

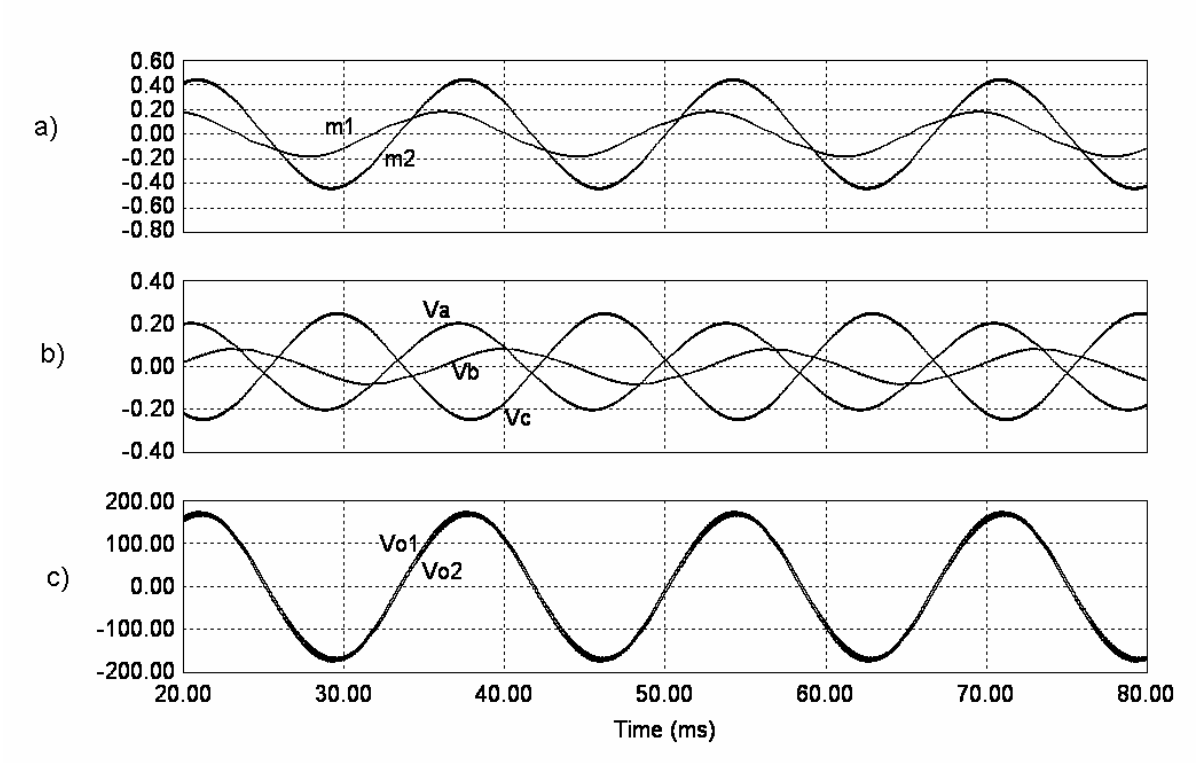

Fig. 3-26. Simulation results of modified three-phase method with inductive load
a) Modulating signals
b) Derived control signals
c) Output voltages (V)

In Fig. 3-27, the top inverter output was connected to a nonlinear load, as in section 3.3.3.2:

120V (Top):	Diode Rectifier with
	200-μF filter capacitor and
	100-W resistive load
120V (Bottom):	200-W resistive load
240V:	150-W resistive load
Total:	450W

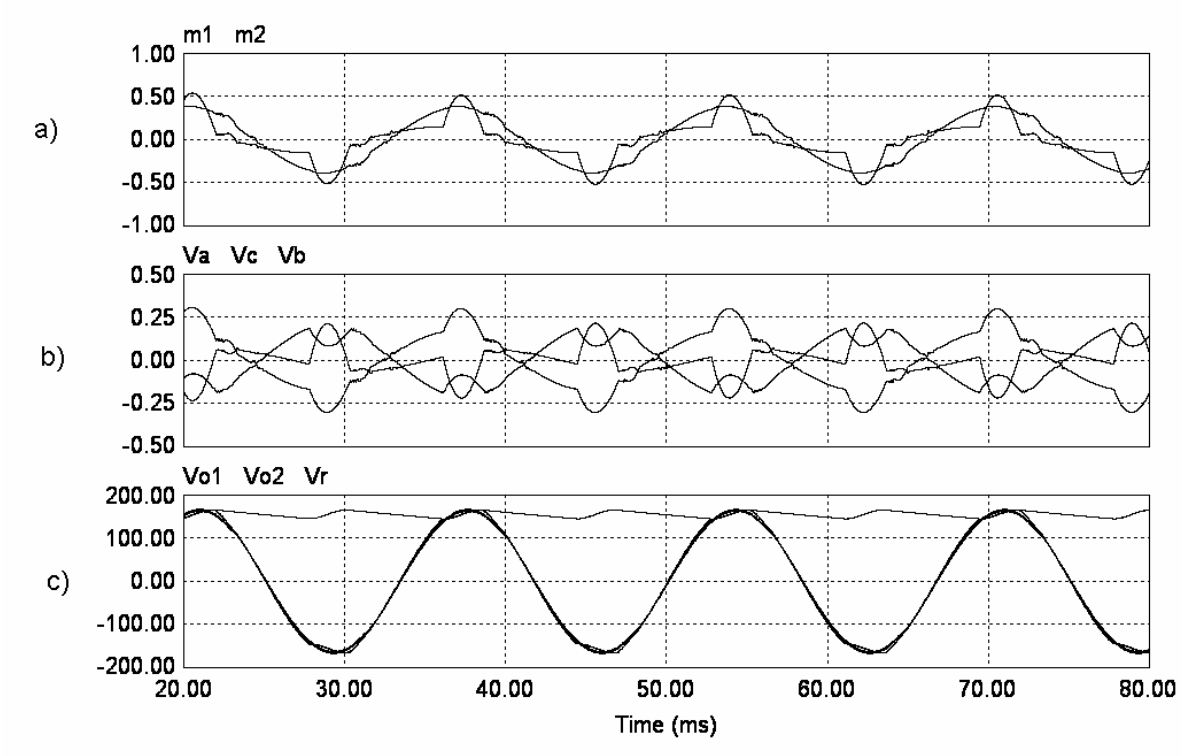

Fig. 3-27. Simulation results of modified three-phase method with nonlinear load
a) Modulating signals
b) Derived control signals
c) Output voltages, and rectifier voltage, v_r (V)

In both cases, the system performs as desired, producing balanced split-phase output voltages.

3.4.5 EXPERIMENTAL RESULTS

The test cases given here use the same experimental prototype as in section 3.3.4. The first test, with results shown in Fig. 3-28, uses the following loads:

120V (Top):	100-W resistive load
120V (Bottom):	200-W plus 33.9-Var inductive load
240V:	115-W resistive load
Total:	415W

The two output voltages are successfully balanced despite the significantly unbalanced loads. The voltages v_{o1} and v_{o2} are 115 V rms and 112 V rms, respectively. Both are

primarily sinusoidal, as desired, although some small variations from the reference are seen in the v_{o1} voltage. These are not present in simulations and are due to noise produced by the non-optimized experimental prototype, combined with the simple PI feedback controllers used. They could be eliminated by optimizing the converter layout to reduce noise generation and its effect on voltage feedback measurements, and by replacing the PI controllers with a more advanced method, such as state feedback.

The second test case was intended to show that the inverter and this control algorithm are able to operate with nonlinear loads such as diode rectifiers. The following test loads were used:

120V (Top):	Diode Rectifier with 430-μF filter capacitor and 80-W resistive load
120V (Bottom):	200-W plus 33.9-Var inductive load
240V:	115-W resistive load
Total:	395W

The results are given in Fig. 3-29. The bottom output voltage, v_{o2}, is 110 V rms, clearly sinusoidal, and well regulated. The diode rectifier does cause some distortion of the top half-phase voltage; however, a small amount of distortion is expected with an entirely non-linear load. The RMS value of this voltage is still within the desirable range, at 115 V rms, and it is still in phase with the bottom output voltage. Again, this result could be improved by using a more advanced controller than a basic proportional-integral to produce the modulating signals; however, this thesis is intended to demonstrate the effectiveness of the topology and PWM algorithm, and does not cover advanced feedback control techniques.

The PI controllers used throughout these tests were as follows:

$$m_1 = 0.0035 v_{e1} + 2\frac{v_{e1}}{s} \quad \text{and}$$

$$m_2 = 0.0035 v_{e2} + 2\frac{v_{e2}}{s}, \tag{3-12}$$

where v_{eX} is the error of output voltage X (i.e. the difference between that voltage and its reference level).

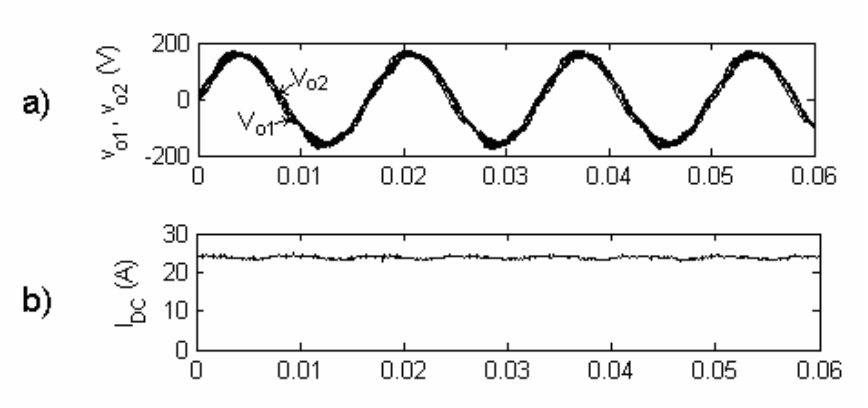

Fig. 3-28. Experimental results for Method 2: resistive and inductive loads
a) Output voltages v_{o1} and v_{o2} (V)
b) DC Current (A)

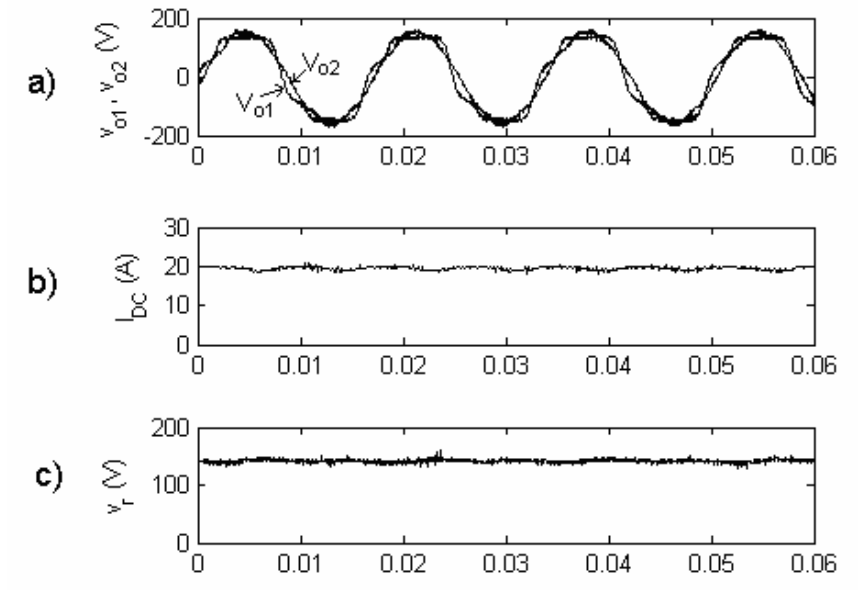

Fig. 3-29. Experimental results for Method 2: resistive, inductive, and nonlinear loads
a) Output voltages v_{o1} and v_{o2} (V)
b) DC Current (A)
c) Rectifier output voltage (V)

3.5 SUMMARY

In this chapter, two techniques were developed to produce single-phase three-wire, utility-voltage outputs using a current-sourced inverter. The required DC current was generated from a low DC voltage as described in Chapter 2. The techniques, described in sections 3.3 and 3.4, each successfully generated balanced, split-phase outputs, even under highly unbalanced loading conditions. They were equally effective with resistive, inductive, and non-linear loads. These results were achieved while closely matching the switching and conduction losses among the six inverter switches, and were demonstrated through simulation and experimental results. The first algorithm focused on minimizing the maximum ripple component of the two output voltages in the time domain, as described in section 3.2. The second algorithm was based on a technique for three-phase current-sourced inverters presented in [21], and has the advantage of doubling the effective switching frequency.

CHAPTER 4

EXPERIMENTAL PROTOTYPE DESIGN

4.1 INTRODUCTION

This chapter focuses on the hardware and software design of the experimental prototype used in Chapters 2 and 3. The hardware design section will discuss the components used in the power circuit, as well as the purpose and design of measurement and filtering circuitry. The software design section will then describe how the control algorithms presented in Chapters 2 and 3 were implemented in an Innovative Integration M67 DSP board.

4.2 HARDWARE DESIGN

4.2.1 POWER CIRCUIT

As mentioned in section 2.6, the power circuit consisted of the following components:

- 5 Fuji Electric 2MBI50N-060 IGBT switch modules (each containing two switches in series)
- 7 Fuji Electric 2FI50A-60 diode modules (each containing two diodes in parallel)
- 50mH DC inductor
- 1mF energy-storage capacitor
- 2 15μF output filter capacitors

- 2 fast-acting 25-A fuses, at the outputs of the DC source and the energy-storage capacitor

Two three-leg current-sourced converter modules had previously been constructed using these components, as shown in Fig. 4-1, and described in [22]. One of these modules was used as the inverter bridge. The other was re-wired to create the voltage source-to-current source circuit described in section 2.5.1, as shown in Fig. 4-2. The Metal Oxide Varistors (MOVs) used to protect the switches in both modules were replaced. Panasonic's ERZV20D391 model was used because the minimum of its operating range, i.e. 351V, is above the peak of the overall output voltage, which is the maximum voltage expected to be applied across the switches. Its maximum clamping voltage of 650V is slightly above the rated voltage of the switches, 600V. However, MOVs generally clamp at some point in their operating range, below the maximum rated level. Also, it is likely that the IGBTs can handle an 8% overvoltage without failing. No MOVs could be found with a lower clamping level, while still having an operating range above the peak output voltage; therefore, this was the best option. When the energy-storage capacitor was being tested, no MOV was connected across the capacitor switch, S_C, because an MOV with a sufficiently high DC operating voltage would not have a sufficiently low clamping voltage to provide any protection to the switch. Therefore, the circuit was first tested at low voltage to ensure proper operation, then tested at full voltage without an MOV.

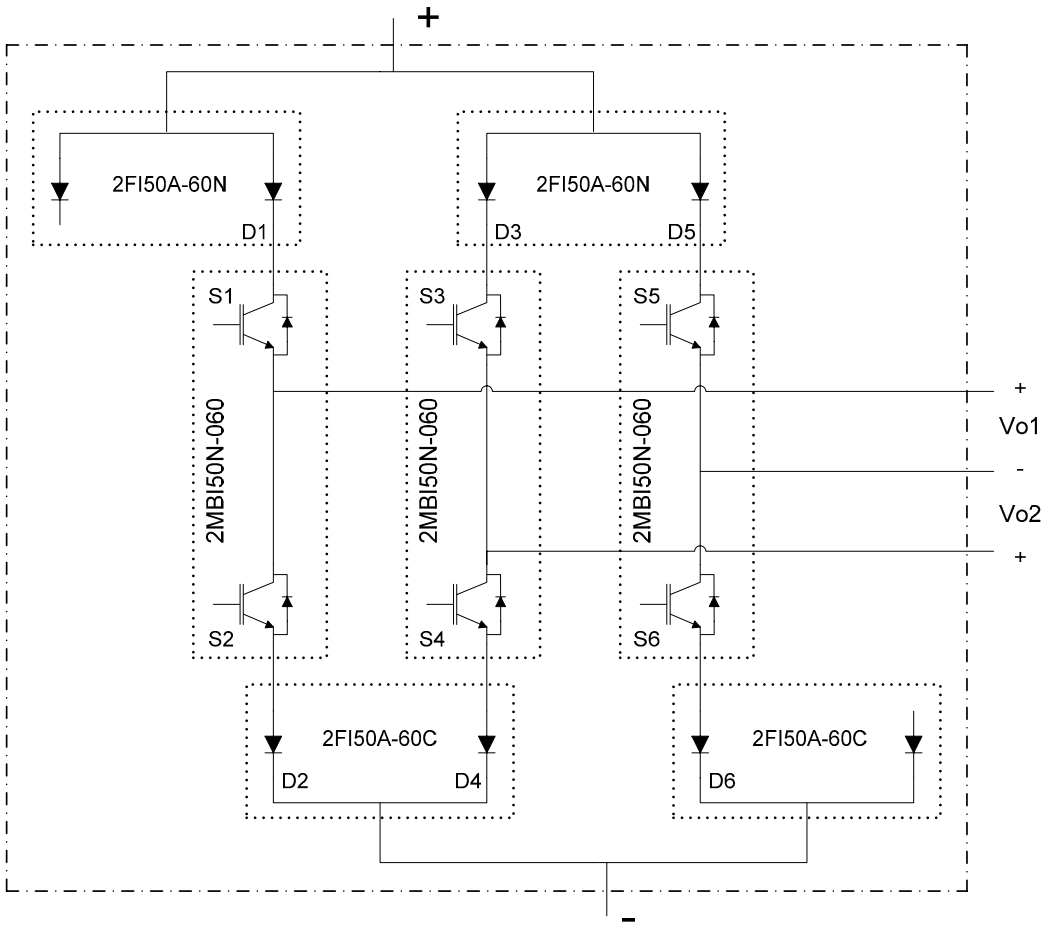

Fig. 4-1. Existing current-sourced converter module from [22]

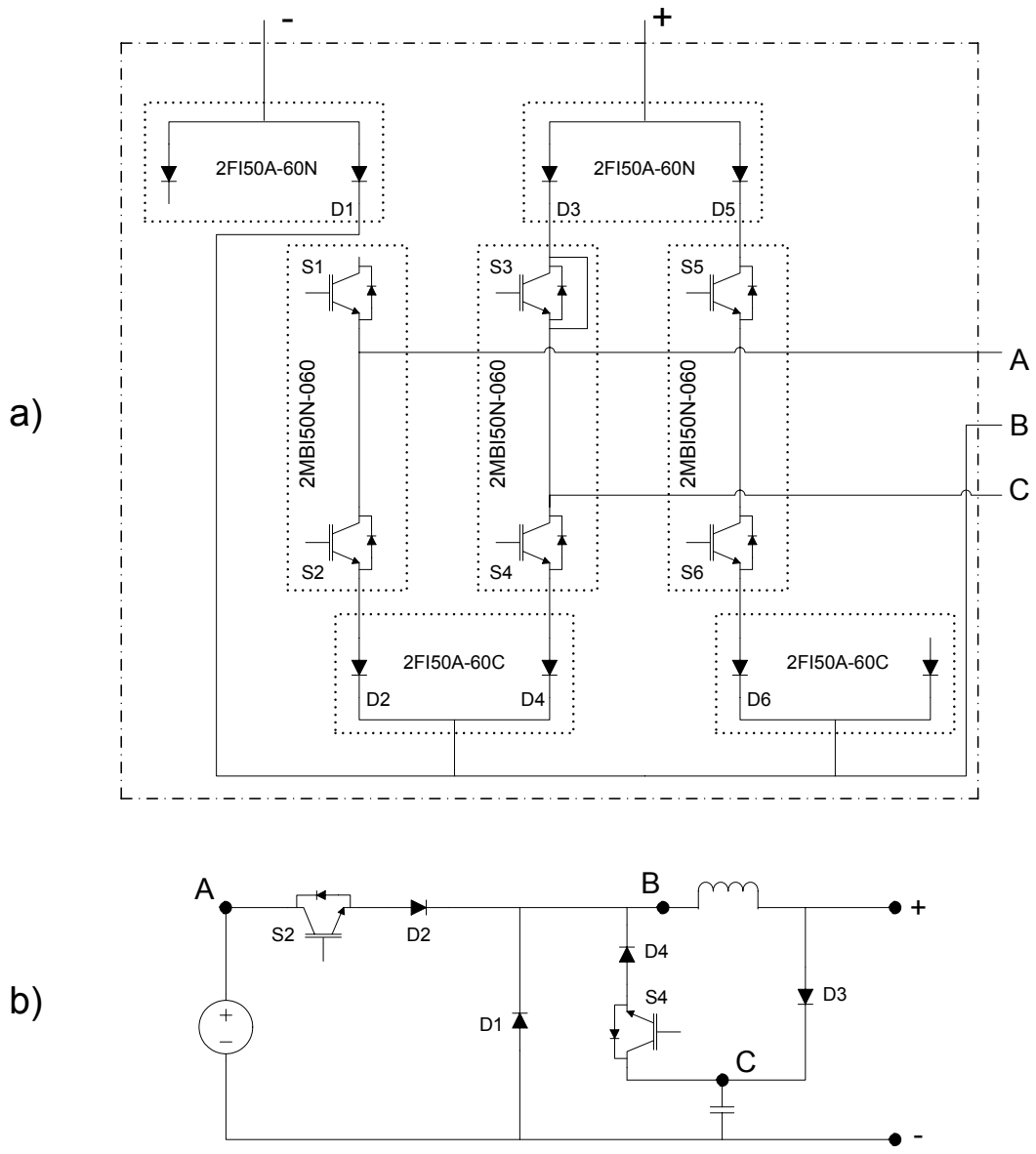

Fig. 4-2. CSI module modified to act as *V-to-I* circuit
a) Physical connections within CSI module
b) Resulting voltage source-to-current source circuit, equivalent to Fig. 2-7

4.2.2 MEASUREMENT AND FILTERING CIRCUITRY

Measurement of output voltages, DC current, and energy-storage capacitor current were also done using pre-constructed modules, which are described in [23]. The voltage measurement signals were then low-pass filtered to attenuate high-frequency noise. Identical second-order, Butterworth low-pass filters were designed for each of the two output

voltages, as shown in Fig. 4-3. The corner frequencies of these filters are 994.7 Hz, or approximately 1 kHz. The outputs of the filters were read by the control board using an A/D module.

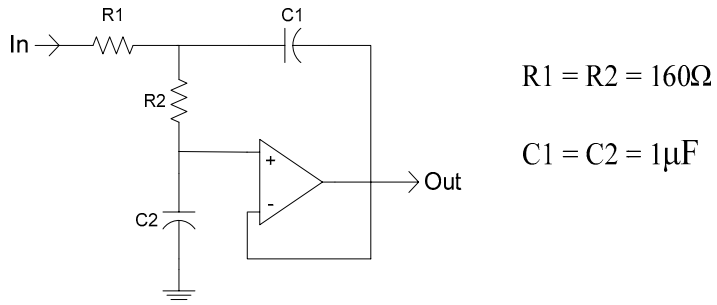

Fig. 4-3. Output voltage measurement low-pass filter

Due to the slow speed of the A/D module, it was not used for the DC current or capacitor voltage. Instead, the level comparisons shown in Fig. 2-12 of section 2.5.3 were performed using analog comparators, and a set of digital signals were sent to the control board, indicating whether the measured signals were above or below each reference level. It should be noted that this technique would not be appropriate for the more advanced control technique of section 2.8. Also, it would not be able to dynamically update the current reference as described in section 2.6. In those cases, a faster A/D circuit would be required.

The analog voltage and current reference levels were generated using simple voltage dividers, as shown in Fig. 4-4. These levels were compared to the outputs of the I_{DC} and V_C measurements using LM339 analog comparators.

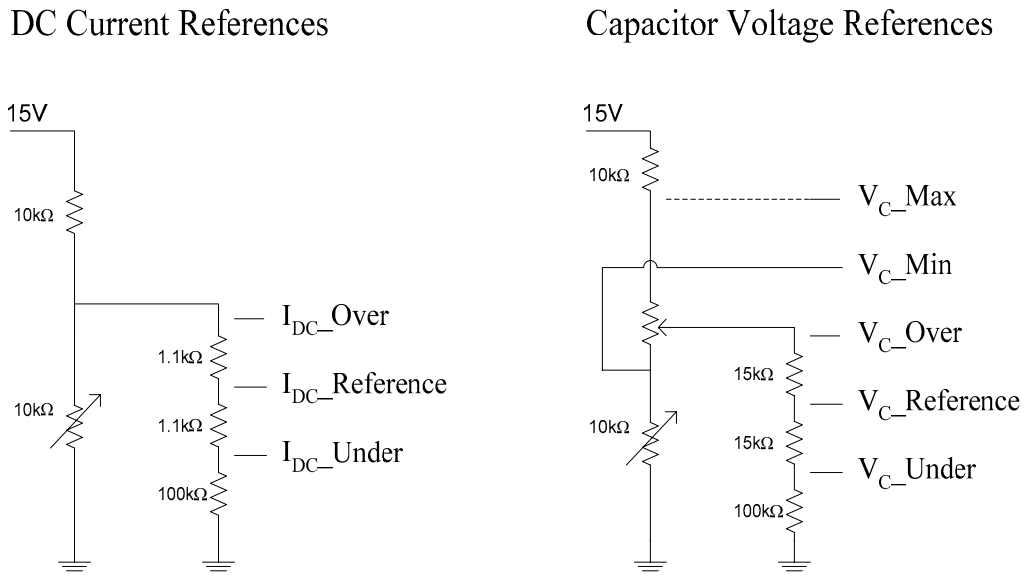

Fig. 4-4. Circuits to generate reference thresholds for DC current and energy-storage capacitor voltage

The DC current measurement circuit produces a voltage signal at 3/10 the actual current level. By varying the I_{DC}_Reference voltage level between 0 and approximately 7.5V, using a potentiometer, the DC Current Reference circuit can order the DC current to any level between 0 and 25A. The I_{DC}_Over and I_{DC}_Under reference levels are held at approximately 1% above and below I_{DC}_Reference. These 1% bands can be increased or decreased by replacing the 1.1-kΩ resistors shown.

The capacitor voltage reference circuit operates in a similar manner, except that it also produces thresholds for the maximum and minimum allowable voltage. (The maximum allowable voltage is based on component tolerances, and the minimum allowable voltage is equal to the peak inverter output voltage plus a 5% margin.) The DC voltage measurement circuit scales the voltage down by 50 times, so this circuit allows the capacitor voltage reference to be set anywhere between the minimum and maximum allowable levels of 360V and 470V by varying the potentiometer. As with the current reference circuit, the over- and under-voltage margins can be changed by swapping out the 15-kΩ resistors.

4.3 SOFTWARE DESIGN

The inverter was controlled by an M67 DSP board by Innovative Integration, with a Texas Instruments TMS320C6701 processor. The board included an optional analog to digital input sub-circuit, which was used to read the measured inverter output voltages. The controller's inputs and outputs are shown in Fig. 4-5.

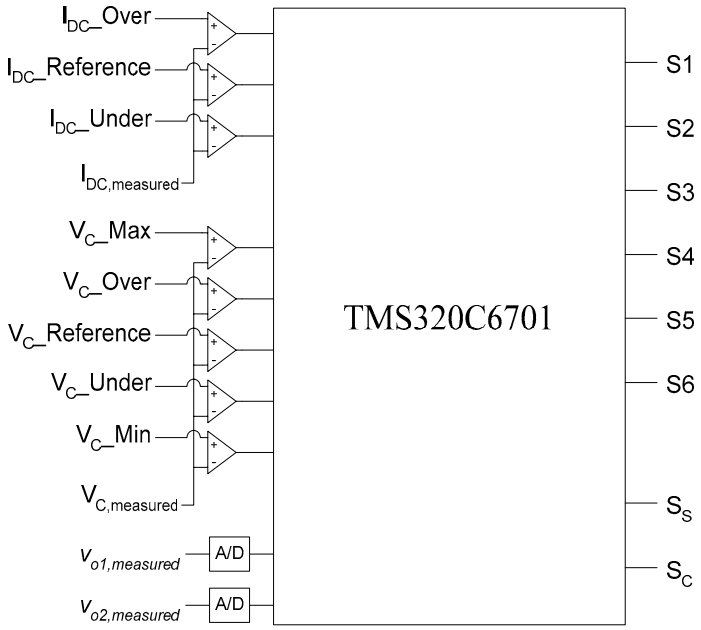

Fig. 4-5. Control Processor I/O

The code structure consisted of two primary components: the main loop, and a timer-based interrupt that performed the PWM and set the gate-driver outputs. The main loop performed the following tasks:

1. Read the latest values of the A/D inputs and the digital input pins.
2. Based on the DC current and capacitor voltage levels, determine the desired values of the voltage source-to-current source control signals, S_S, S_C, and C_C (Fig. 2-7).
3. Measure the differences between the two output voltages and their references, and calculate the modulating signals *m1* and *m2* (section 3.3) using digital PI controllers.

4. Separate the modulating signals into the control signal components v_{c1}, v_{c2}, and v_{com}, and then calculate the PWM threshold levels P1 to P5, as described in section 3.3.

The interrupt routine was responsible for performing the multiple-reference PWM, using the threshold levels calculated in the main loop. It generated the gating signals for the inverter bridge and sent them, along with those for the supply and capacitor switches (S_S and S_C), to the output pins.

The PWM switching frequency, as well as the control frequency for the *V-to-I* circuit, was set to 10kHz. In order to achieve this frequency, several challenges had to be overcome regarding the slow speed of the control hardware. The TMS320C6701 has a clock frequency of 20 MHz, or 2000 cycles per switching period. A/D conversions each took approximately 200 to 300 cycles, or 10% to 15% of a switching period, and were not interruptible.

4.3.1 MODIFIED DIGITAL PWM

The first modification to be made was in the method of generating the PWM gating signals. In the basic, analog form described in section 3.3, these signals are generated by comparing an analog triangular carrier signal with the reference levels P1 to P5. Switching events occur at every crossing of the carrier signal with a reference level.

Given the speed of the processor, it is not practical to simply recreate the triangular carrier signal and comparison in digital form. The resolution would be limited to the speed at which successive interrupts could be run, which is approximately every 30 cycles, even discounting the need to allow time between interrupt firings for the main loop to operate.

However, it is not necessary to perform these comparisons in real-time. The reference levels P1 to P5 vary with the output currents, at 60 Hz. Over a single switching period, they are essentially constant. Therefore, knowing the switching frequency, the crossing point of a theoretical triangular carrier signal with these references can be calculated in advance, at the beginning of each switching period. The interrupt routine then only needs to be run at these actual crossing times.

4.3.2 SYNCHRONIZATION OF A/D OPERATIONS

As mentioned in section 4.2.2, the comparisons of the DC current and energy-storage capacitor voltage with their respective references were done in analog circuitry due to the slow speed of the M67 board's A/D converter. The speed of A/D operations also posed problems for the PWM control. A single A/D operation required 10% to 15% of a switching period to complete, and did not allow the PWM interrupt to fire. Therefore, if an A/D conversion began near a PWM switching threshold, it would cause significant distortion. As mentioned above, the voltage signals being measured vary much more slowly than the switching speed; they can be considered constant over a single switching period. It is therefore not a problem that they cannot be measured quickly, only that the slow measurements interfere with PWM operation.

As a solution, the main loop was synchronized with the PWM switching. Before performing each A/D conversion, the main loop waited until the PWM interrupt set a flag indicating that a new shoot-through state was beginning. The A/D operation could then be performed, knowing that it had the full duration of a shoot-through state before the next threshold crossing (and consequential firing of the PWM interrupt routine). As seen in the simulation results of Chapter 3, the shoot-through states are generally much longer than the active states, so this synchronization will provide sufficient time for the A/D operations, without affecting PWM operation.

4.4 SUMMARY

This chapter discussed the physical prototype used to achieve the experimental results for Chapters 2 and 3. Section 4.2 covered the hardware design. It showed the layouts of the inverter bridge and voltage source-to-current source (*V-to-I*) circuits. The circuitry used to measure and filter signals for feedback control was also given. Section 4.3 focused on the digital controller software. It covered the general code layout, as well as challenges overcome to achieve the desired performance.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 CONCLUSIONS

This thesis is based on research into the use of a current-sourced inverter to generate utility-voltage split-phase AC power from a low-voltage DC source. As described in section 1.1.2.2 of the introduction, there are a number of advantages to using a current-sourced inverter, rather than the more common voltage-sourced inverter, for this task. However, a number of drawbacks also exist, which have prevented the widespread adoption of current-sourced inverters for distributed generation. This thesis focuses on resolving the two significant obstacles that remain at present:

1. While they eliminate the need for a boost converter input step required by voltage-sourced inverters, current-sourced inverters do require a method of generating a stable DC current from the available low-voltage source. Sufficient energy storage must be provided so that the DC current level is sustainable during large transient power draws.
2. To date, no method has been documented to produce split-phase outputs using a current-sourced inverter. Split-phase is the standard form of residential and light-commercial power delivery in North America, so such a method is required.

A simple circuit and a control algorithm have been developed to generate the required DC current from a low-voltage DC source under arbitrary loading conditions. Two control algorithms were developed to generate split-phase AC output voltages using a three-leg current-sourced inverter. The outputs generated were shown to be well balanced in the presence of highly unbalanced, as well as inductive or nonlinear, loads. In addition to theoretical and simulated analysis, laboratory prototypes were built of both the voltage source-to-current source circuit and the split-phase current-sourced inverter. Experimental results verified that the DC current level could be maintained, and that balanced split-phase output voltages could be produced, under a variety of loading conditions.

In Chapter 2, a circuit and control algorithm were developed to generate a constant DC current from a low-voltage DC source. The final design incorporated the following features:

1. Produced a constant current at a desired level, for use by a current-sourced inverter.

2. Included a simple energy-storage circuit which supplies the necessary power to handle turn-on transient events in the connected inverter's loads, without resulting in added losses when it is not in operation.

3. Identified the minimum current level at which the circuit could a) produce a constant current without the use of the supplemental energy-storage block, b) produce a sustainable, non-constant current without the use of the supplemental energy-storage block, and c) produce a constant current using the supplemental energy-storage block at steady-state.

This preconditioning circuit does require an additional switch and diode beyond those used by a boost converter, which is required by a voltage-sourced inverter. However, this is offset by the reduced complexity at the output filtering stage of the current-sourced inverter. The improved regulation and other advantages of current-sourced inverters may also be worth the incremental cost of a single switch, especially for specialized applications where excellent output wave-shaping is critical.

In Chapter 3, two methods were developed to generate split-phase output voltages using a three-leg current-sourced inverter. The first of these methods was designed to produce balanced, split-phase outputs under arbitrary loading conditions while achieving the following three goals:

1. Use a PWM switching scheme that operates all six inverter switches at the same frequency to equalize switching losses.
2. Share current, particularly shoot-through current, evenly among the inverter's three legs to equalize conduction losses.
3. Minimize the high-frequency ripple of the output voltages at a given switching frequency. (Ideally, generate half-phase output voltages comparable to the outputs of single-phase, tri-level PWM inverters, with double effective switching frequency.)

The first two goals were achieved. The method also reduced the output voltage ripple, so that the results were better than those of bi-level PWM inverters; however, the effective doubling of switching frequency seen in tri-level inverters was not achieved.

After completion of the first method, it was realized that these three goals could instead be achieved using a control technique for three-phase current-sourced inverters presented in [21]. The following contributions were added to make this technique suitable for split-phase AC voltage generation:

1. An algorithm was developed for calculating the control signals used by the three-phase PWM technique based on feedback of split-phase output voltages.
2. An improved method for sharing shoot-through current was designed, allowing shoot-through current to be shared equally among the three legs of the inverter under arbitrary loading conditions, rather than only for balanced, three-phase loads.

Once the above additions were made, the technique successfully produced balanced, split-phase output voltages even under highly unbalanced, inductive, or nonlinear loading

conditions, while equalizing switch usage. As in the three-phase case presented in [21], the method adopted was also able to completely eliminate the harmonic components of the output voltages at the switching frequency, achieving equal performance to that of tri-level PWM inverters.

In Chapter 4, the laboratory prototype used to produce supporting results for Chapters 2 and 3 was described in detail. The prototype consists of a three-leg current-sourced inverter, the voltage source-to-current source circuit designed in Chapter 2, resistive and inductive loads, and measurement and control circuitry. All components used in the power circuit are listed, and techniques used in the implementation of the control algorithm are described.

5.2 SUGGESTIONS FOR FUTURE WORK

One useful addition to this research would be to describe the combined current-sourced inverter and voltage source-to-current source circuit with a state space model. The fact that differential equations are used in the calculation of current reference levels in section 2.4.2 and in the development of the *V-to-I* control algorithm in section 2.8 suggests that a state space model could be used to optimize the system's control. State feedback control could also be used to improve output voltage regulation, particularly if its optimization takes into account the uncertainty due to noise in the feedback voltages experienced with the experimental prototype.

Another logical continuation of the research presented in this thesis would be to compare voltage-sourced inverter and current-sourced inverter topologies used in split-phase AC voltage generation from an efficiency perspective, using currently available switching elements.

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