Novel RF MEMS Varactors Realized in Standard MEMS and CMOS Processes

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Micro-Electro-Mechanical Systems (MEMS) varactors have the potential to replace conventional varactor diodes, due to their high loss and non-linearity, in many applications such as phase shifters, oscillators, and tunable filters.

The objective of this thesis is to develop novel MEMS varactors to improve the capacitance tuning ratio, linearity, and quality factor. Several novel varactor configurations are developed, analyzed, fabricated and tested. They are built by using standard MEMS fabrication processes, as well as monolithic integration techniques in CMOS technology.

The first capacitor consists of two movable plates, loaded with a nitride layer that exhibits an analog continuous capacitance tuning ratio. To decrease the the parasitic capacitance, a trench in the silicon substrate under the capacitor is adopted. The use of an insulation dielectric layer on the bottom plate of the MEMS capacitor increases the capacitors' tuning ratio. Experimental and theoretical results are presented for two versions of the proposed capacitor with different capacitance values. The measured capacitance tuning ratio is 280% at 1 GHz. The proposed MEMS vararctor is built using the MetalMUMPs process. The second, third, and fourth capacitors have additional beams that are called carrier beams. The use of the carrier beams makes it possible to obtain an equivalent nonlinear spring constant, which increases the capacitors' analog continuous tuning ratio. A lumped element model and a continuous model of the proposed variable capacitors are developed. The continuous model is simulated by commercial software. A detailed analysis for the steady state of the capacitors is presented. The measured capacitance tuning ratios of these three

capacitors are 410%, 400% and 470%, respectively at 1 GHz. Also, the self-resonance frequency is measured and found to exceed 11 GHz. The proposed MEMS variable capacitors are built by the PolyMUMPs process.

The fifth novel parallel-plate MEMS varactor has thin-film vertical comb actuators as its driver. Such an actuator can vertically displace both plates of the parallel-plate capacitor. By making use of the fringing field, this actuator exhibits linear displacement behavior, caused by the induced electrostatic force of the actuator's electrodes. The proposed capacitor has a low parasitic capacitance and linear deflection due to the mechanically connected and electrically isolated actuators to the capacitor's parallel-plates. The measured tuning capacitance ratio is 7:1 (600%) at 1 GHz. The fabricated MEMS varactor exhibits a self resonance frequency of 9 GHz and built by MetalMUMPs process.

The sixth parallel-plate MEMS varactor exhibits a linear response and high tuning capacitance ratio. The capacitor employs the residual stress of the chosen bi-layer, and the non-linear spring constants from the suspended cantilevers to obtain a non-linear restoring force that compensates for the non-linear electrostatic force induced between the top and bottom plates. Two existing techniques are used to widen the tuning range of the proposed capacitor. The first technique is to decrease the parasitic capacitance by etching the lossy substrate under the capacitor's plates. The second technique is employed to increase the capacitance density, where the areas between the top and bottom plates overlap, by applying a thin film of dielectric material, deposited by the atomic layer deposition (ALD) technique. The measured linear continuous tuning ratio for the proposed capacitor, built in the PolyMUMPs process, is 5:1 (400%).

The seventh and eighth MEMS variable capacitors have plates that curl up. These capacitors are built in 0.35 μm CMOS technology from the interconnect metallization layers. The plates of the presented capacitors are intentionally

curled upward to control the tuning performance.

A newly developed maskless post-processing technique that is appropriate for MEMS/CMOS circuits is proposed. it consists of dry and wet etching steps, developed to integrate the proposed MEMS varactors in CMOS technology. Mechanically, the capacitors are simulated by the finite element method in ANSYS, and the results are compared with the measured results. The seventh capacitor is a tri-state structure that exhibits a measured tuning range of 460% at 1 GHz with a flat capacitance response that is superior to that of conventional digital capacitors. The proposed capacitor is simulated in HFSS and the extracted capacitance is compared with the measured capacitance over a frequency range of 1 GHz to 5 GHz. The eighth capacitor is an analog continuous structure that demonstrates a measured continuous tuning range of 115% at 1 GHz with no pull-in. The measured quality factor for both CMOS-based capacitors is more than 300 at 1.5 GHz. The proposed curled-plate capacitors have a small area and can be realized to build a System-on-Chip (SoC). Finally, a tunable band pass filter that utilizes the MEMS variable capacitors in 0.18 μm CMOS technology from TSMC is designed, modeled and fabricated.

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Dedication

to my parents,

to my wife and my daughter,

to my sisters and my brothers in law,

to my friends,

without your love and support, it would have been very rough

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Chapter 1

Introduction

1.1 Motivation

Varactor tuning techniques are widely employed in phase shifters [12, 13], oscillators [14–16], and tunable filters [17–19]. The Micro-Electro-Mechanical Systems (MEMS) technology has the potential of realizing varactors with a performance that is superior to that of varactor diodes in areas such as non-linearity and losses. Conventional solid-state varactors are manufactured in silicon or gallium arsenide by using either p-n or Schottky-barrier junction structures. Several Figures of Merit (FoM), used for varactors, include capacitance tuning ratio, quality factor Q, and electrical self-resonance.

Recent efforts within the MEMS research have shown promising results in the realization of MEMS-based high performance tunable capacitors. These devices are composed of parallel metal plates, and the capacitance tuning functionality is achieved by adjusting the spacing between the parallel plates via electrostatic actuation. Some of the shortcomings of a solid-state varactor, including large resistive losses, have been solved by the parallel plate MEMS approach.

MEMS parallel plate varactors, with electrostatic actuators, are considered to be the most convenient configurations to build due to the simplicity of the fabrication [1]

and the lower power consumption compared with the thermal actuators. However, such types of MEMS capacitors have a maximum theoretical tuning capacitance ratio of 50% due to the collapse of the capacitor structure as the voltage is increased beyond the pull-in voltage [1].

1.2 Objectives

The purpose of this thesis is to propose a novel RF MEMS parallel-plate varactors with analog continuous, linear, and digital responses that have a high tuning capacitance ratio, high self-resonance frequency and high quality factor Q. Also, the thesis details the design, modeling and fabrication of such MEMS varactors. Theoretical and experimental results are introduced to verify the validity of the proposed MEMS varactors. The combination of the MEMS RF performance, along with other advantages such as, a small size, low weight, low manufacturing cost, and improved linearity, should make MEMS devices suitable and attractive replacement for the solid-state varactors in a wide range of RF applications.

A thin-film process and thick-film electroplated process from MEMSCAP are chosen to fabricate discrete MEMS varactors. 0.35 μm and 0.18 μm CMOS processes from Taiwan Semiconductor Manufacturing Company (TSMC) are used to implement varactors that can be integrated monolithically with active circuits to fabricate a SoC. The course of development efforts took the following three stages:

1. **Development of novel discrete MEMS variable capacitors with an analog continuous and high tuning capacitance ratio:** Four new versions of these varactors are introduced in Chapter 3. Such varactors represent the 1st stage of development in the proposed research in the thesis. The focus in that stage is on developing novel high tuning capacitance ratio as the tuning elements in RF and microwave applications. These variable capacitors are fabricated by PolyMUMPs and MetalMUMPs processes from MEMSCAP. The capacitors are

modeled, characterized, and the measured data are compared with simulated data.

2. **Fabrication of two novel structures of discrete MEMS variable capacitors with linear analog continuous and high tuning capacitance ratio utilizing wet etching of the silicon substrate and atomic layer deposition (ALD) post-processing for the first structure and a combination of parallel-plate with vertical thin film comb actuators for the second structure:** These MEMS varactors represent the 2nd stage of varactor development and exhibit a high tuning capacitance ratio with a linear response. By combining the parallel-plate topology with the vertical comb drive actuators for the first structure in Chapter 4 and employing the residual stress in bi-layer thin film to create curl up structure for the second varactor in the same chapter, linear capacitance responses in terms of applied *dc* bias voltages are obtained for both devices. The varactors are fabricated by the PolyMUMPs and MetalMUMPs processes, respectively, at the MEMSCAP's foundry. The varactors are characterized, simulated and measured.

3. **Design and fabrication of two newly developed structures of monolithically integrated MEMS variable capacitors by using the interconnect metallization in CMOS technology, with analog linear continuous and digital tri-state varactors:** The 3rd stage of MEMS varactor development focuses on integrating them monolithically in CMOS technology. These varactors exhibit a high tuning capacitance ratio, high quality factor for linear and digital capacitance responses. Both devices utilize a new post-processing technique to build high quality factor MEMS variable capacitors for the RF and microwave applications in RFIC and SoC. The residual stress in bi-layer thin films is employed to create novel structures that demonstrate a digital tri-state capacitance response for the first structure and an analog linear continuous response for the second structure. The variable capacitor is manufactured by the Taiwan Semi-

conductor Manufacturing Company (TSMC). After the capacitor is modeled, characterized, simulated and measured, the measurement results, are compared with the simulated results.

1.3 Structure of the Thesis

The motivation and research objectives are outlined in this chapter. A literature review of conventional and CMOS-based MEMS varactors, is provided in Chapter 2.

In Chapter 3, several proposed MEMS varactors are described. The high tuning range in the parallel-plate capacitors of analog continuous type is the major scope in this chapter. These capacitors represent the first stage of development of MEMS varactors. They exhibit high tuning capacitance ratio, however, not a perfect linear response. They are fabricated by standard MEMS processes such as PolyMUMPs and MetalMUMPs from MEMSCAP. In addition, the measured, modeled, and simulated data are introduced.

Novel MEMS variable capacitors that exhibit a linear and high tuning capacitance ratio are examined in Chapter 4. The simulated and measured results are given for the two unique structures.

Chapter 5 includes the development of novel MEMS variable capacitors that are fabricated monolithically in the interconnect metallization of the TSMC 0.35 μm and TSMC 0.18 μm CMOS technology. The capacitors have a high quality factor which is in excess of 300 at 1.5 GHz, and demonstrate a high tuning capacitance ratio for two novel structures: analog linear continuous and digital tri-state capacitors.

Chapter 6 summarizes the contributions of this thesis (also, see Appendix A) and points out problems that will be solved in future work.

Chapter 2

Literature Survey

2.1 Introduction

MEMS varactors can be easily built using surface micromachining in a parallel plate orientation by having two plates, separated by an air gap, facing each others. Applying a *dc* bias across these two plates induces an electrostatic force that causes the plate to deform toward the other plate. MEMS varactors can be classified into two categories depending on the actuation direction of the plates.

1. MEMS parallel-plate varactors with a vertical displacement

2. MEMS interdigitated varactors with a lateral displacement

In this chapter we provide a comprehensive review of the published work on MEMS varactors, as well as a discussion of their main design considerations such as capacitance tuning ratio, linearity, self resonance and quality factor.

2.2 Conventional MEMS Parallel-Plate Varactors

The schematic model of conventional MEMS parallel-plate varactors is shown in Fig. 2.1 The capacitor consists of two plates facing each other. The applied *dc* bias

voltage across the two plates induces on electrostatic force which deforms the top plate toward the bottom plate. When approaching one third of the total gap's distance, the top plate will not have an equilibrium position and the top plate will end up snapping on the bottom plate. The tuning of such a capacitor, which corresponds to the one

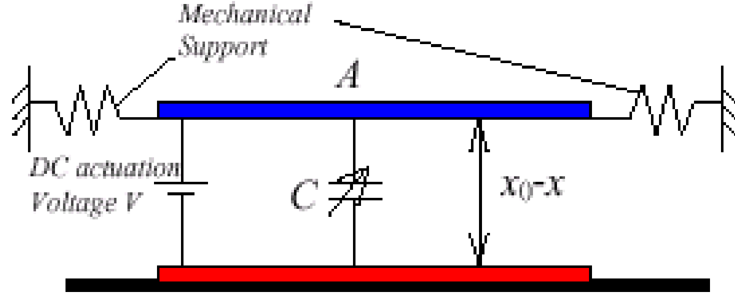


Figure 2.1 Conventional MEMS parallel-plate varactor [1].

third displacement will simply be 50% [1]. When V_{dc} is applied, an electrostatic force F_e is generated between the two plates given by:

$$F_e = \left[\frac{\epsilon_o \cdot A \cdot V_{in}^2}{2 \cdot d^2} \right], \tag{2.1}$$

At the equilibrium stage, the electrostatic force F_e induced by the applied dc voltage will equal the restoring force $F_m = K_m \cdot X$ generated by the spring constant K_m of the supporting beams shown in Fig. 2.1.

One of the conventional parallel-plate varactors built in PolyMUMPs process [20] was proposed by Dec et al [1]. This capacitor has a measured nominal capacitance of 2.05 pF. The theoretical capacitance though was 0.6 pF by using the following formula: $C = \epsilon A/d$ for an air gap of 0.75 μm which is the space of the second oxide layer. The measured capacitance of the experimental device is significantly larger than the designed values due to the warping caused by the residual stress. This residual stress in case of the poly2 that has compressive stress and the metal, which has a tensile stress, on top of it produces warping of the capacitor plates, which effectively

results in an equivalent smaller separation between the two plates and, thus, a higher parallel-plate capacitance [1]. The capacitor achieved a Q-factor of 20 at 1 GHz, and as expected a tuning range of only 50%.

PolyMUMP's process [20] has been used to fabricate the varactor [1], which uses three structural layers from Poly-silicon and two sacrificial layers from silicon oxide. The varactor was released later using HF sacrificial layer etch. The top plate, which is made of poly2 and gold on top of it, is suspended over the bottom plate poly1. The top plate is suspended by four beams which are anchored to the silicon nitride layer. The top plate is designed to deform down toward the bottom plate when a *dc* bias voltage is applied across the top plate and the bottom plate. The SEM photograph is shown in Fig. 2.2. The supporting beams were designed using the T-

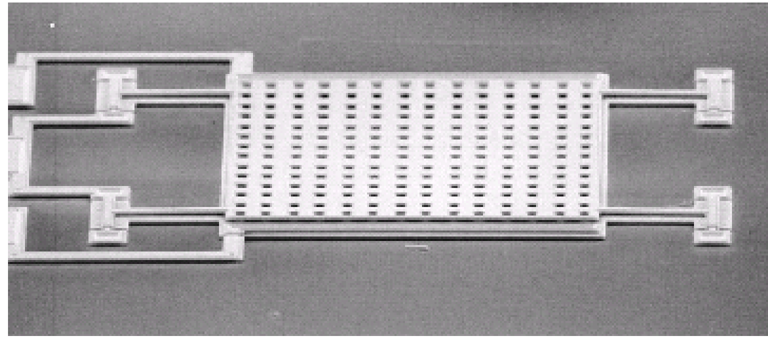


Figure 2.2 SEM photograph of the conventional two parallel-plate varactor [1].

type suspension as shown in Fig. 2.3. The standard pad in the PolyMUMP's process, which has a size of 118 μm x 118 μm, produces a parasitic capacitance of 1.5 pF. The higher the capacitance that the RF pads produces, the worse the tuning range will be. Therefore, a low parasitic pad, which has a parasitic capacitance of only 0.25 pF has been developed [1]. The new pads were made by replacing the conductive layers in the conventional pads by the two silicon oxide layers. This 2.75 μm oxide layers will be trapped underneath the poly2 layer as shown in Fig. 2.4.

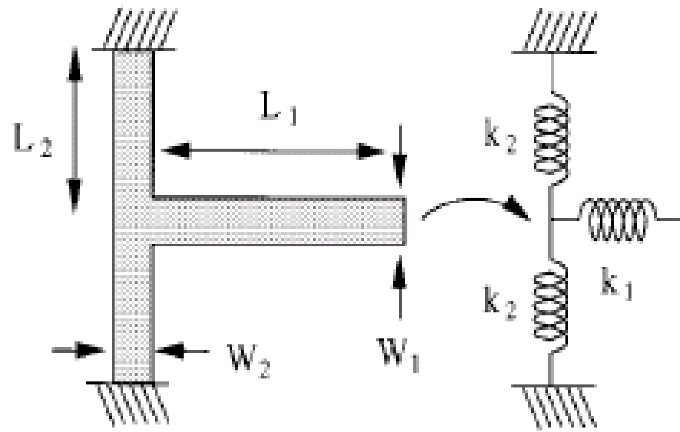


Figure 2.3 Simplified diagram and a spring model of the T-type suspension [1].

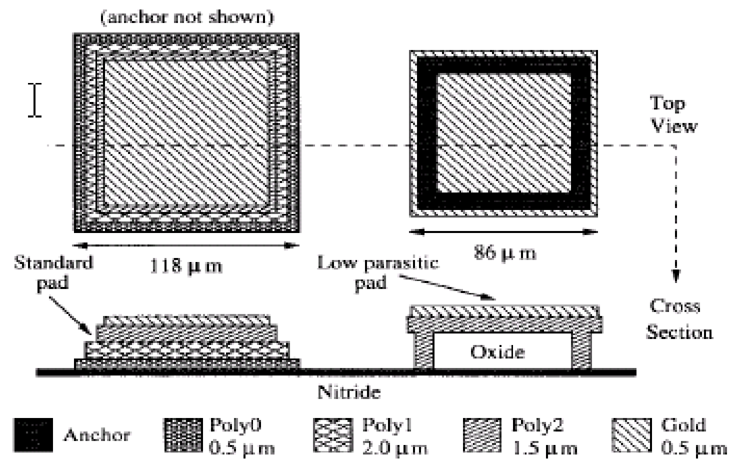


Figure 2.4 Simplified top and cross-section views of a conventional and the developed RF pad in PolyMUMP's process [1].

2.3 Three Parallel-Plate MEMS Varactor

The three parallel-plate varactor is an improved design reported by [1]. This capacitor is built on the same concept of the conventional parallel-plate varactor mentioned in the previous section, however, it has two fixed plates, the first is at the top and the second is at the bottom while the moving plate is in the middle as shown in Fig. 2.5. The moving plate will collapse on the top plate after moving one third of the distance between the middle plate and the top plate. Also, it can move one third of the distance downward. The swing from the maximum up point and the maximum down point represents the new tuning range. The maximum theoretical tuning range that

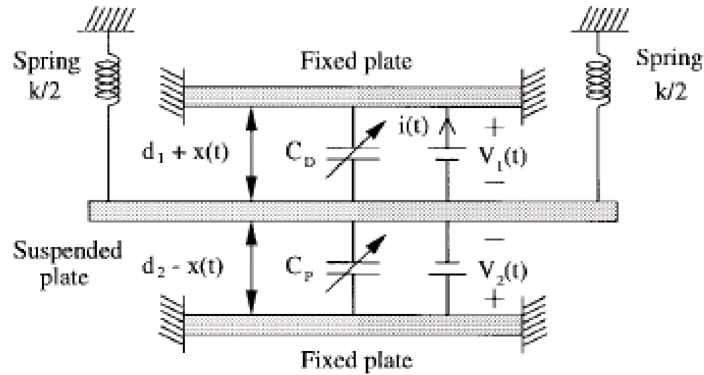


Figure 2.5 Three parallel-plate varactor [1]

can be obtained from this capacitor is 2:1 which is 100% when the distances d_1 and d_2 are equal.

The SEM photograph of the varactor with three parallel-plates (1.9 pF design value) is shown in Fig. 2.6. It is clear from the photograph that the top plate is warped upward. The warpage is believed to be caused by the residual stress. Furthermore, the difference in the residual stress types between the two layers, which the top layer consists of, enhances the warpage.

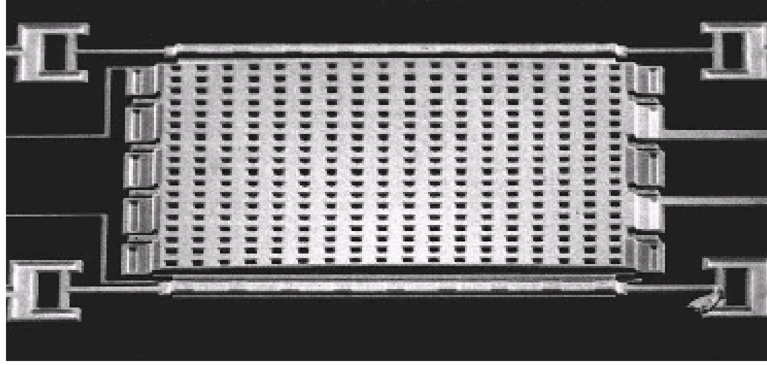


Figure 2.6 SEM photograph of the three-plate varactor [1]

2.4 Wide Tuning Range MEMS Varactor Using Different Gap Spacing

2.4.1 MEMS Varactor Using Different Gap Spacing (No. 1)

A MEMS parallel-plate varactor that has a wide tuning range was presented by [2]. It uses the same concept of the conventional parallel plate varactor but with new topology. The difference of the spacing between the electrostatic actuator's plates, which are E_3 and E_1, from the spacing between the actual capacitor's plates, which are E_2 and E_1, extended the tuning range further. The schematic model of the wide-tuning-range tunable capacitor is shown in Fig. 2.7.

For the fabricated prototype tunable capacitors, a maximum controllable tuning range of 69.8% has been achieved experimentally, exceeding the theoretical tuning range limit 50% of conventional two-parallel-plate tunable capacitors. The distances d_1 and d_2 can be chosen so that the maximum allowable displacement which is one third will be equal to the total distance between the two plates of the capacitor.

The values of d_1, d_2 are 2 μm and 3 μm, respectively. In this case, d_1 can be tuned to 1 μm before the pull-in effect occurs between E_1 and E_3, which corresponds to a

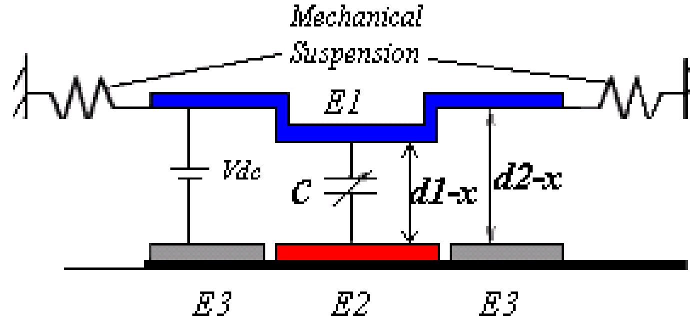


Figure 2.7 A schematic model of the wide tuning range two-plate MEMS varactor [2]

maximum theoretical tuning range (MTTR) of 100% as follow:

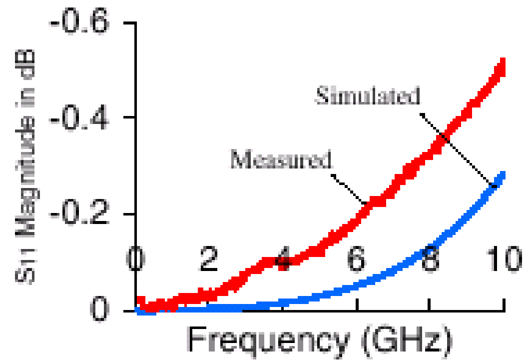
$$MTTR = \left[\frac{d_2}{3 \cdot d_1 - d_2}\right], \tag{2.2}$$

The simulated tuning range using CoventorWare is 90.8% with a pull-in voltage of 19 V. The maximum experimental tuning ranges of five fabricated devices are 50.9%, 44.7%, 55.6%, 59.2%, and 69.8% [2] with a pull-in voltage of approximately 17-20 V.

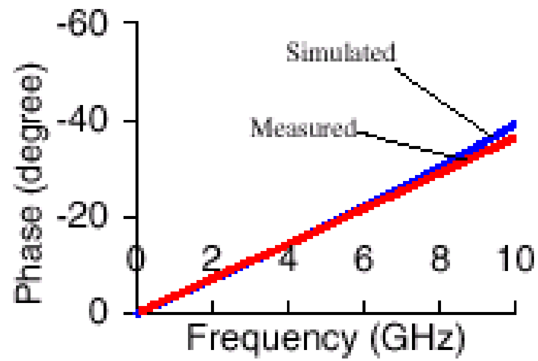
The S_{11} scattering parameter of the wide-tuning-range varactor at *dc* bias voltage equal to zero is measured using RF probe station up to 10 GHz [2]. The measurement results is plotted in Fig. 2.8, which shows a nearly ideal capacitive behavior in the tested frequency range with a return loss lower than 0.6 dB. The measurement data agrees with the simulation data that was obtained using Sonnet em Suite [21] software when $V_{dc} = 0$ V.

2.4.2 MEMS Varactor Using Different Gap Spacing (No. 2)

An enhanced version of the wide extended range varactor mentioned in section 2.4.1 with a tuning range of 300% is reported in [3]. The capacitor consists of two types of beams as illustrated in Fig. 2.9. The lower beam is 2 μm above the CPW while the upper beam that holds the top electrostatic actuator is 8 μm above the bottom electrostatic actuator. The upper beam (which is suspended $g_2 = 6$ μm above the



(a)



(b)

Figure 2.8 The simulated vs. measured S_{11} parameter of the wide-tuning-range varactor, (a) magnitude, and (b) phase [2]

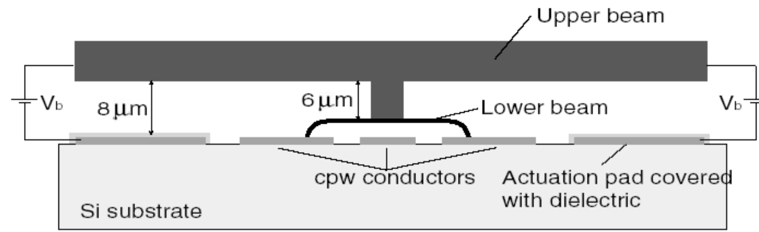
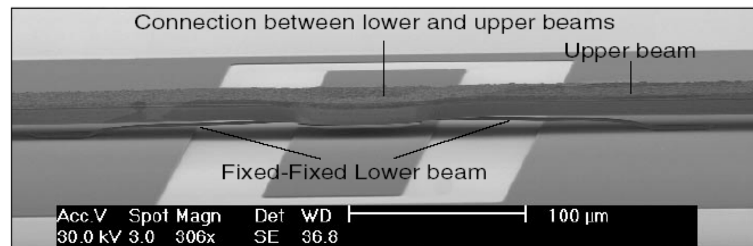
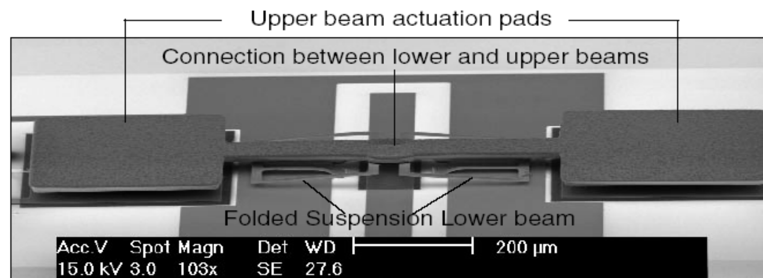


Figure 2.9 A schematic diagram of the fixed-fixed lower beam varactor [3]

lower beam) has no anchor points, but is connected to the middle of the lower beam. A SEM photo of the fabricated capacitor is shown in Fig. 2.10. Although the upper beam is almost 1 mm long, it is very stiff due to its construction of a 13 μm thickness of low-stress electroplated Au. The upper beam also forms two 360 x 300 μm^2 pads (upper pads) that are suspended a total distance of $g_{tot} = g_1 + g_2 = 8$ μm above the two bottom electrostatic actuation pads. When a *dc* bias voltage is applied between the upper beam and the two actuation pads, the lower beam deflects because its spring constant is three orders of magnitude lower than the upper beam's. Moreover, because of the height difference between the two beams, the collapse of the upper beam does not occur until it moves by approximately 2.5 μm downwards. This means that the upper beam does not snap before the lower beam touches the center conductor of the CPW line while the *dc* voltage keeps increasing. When this happens both beams have moved by about 2 μm, which is the maximum allowable distance the lower beam can travel. Fig. 2.11 illustrates the maximum tuning range obtained using this capacitor.



(a)



(b)

Figure 2.10 SEM pictures of the two capacitors, (a) folded-suspension lower beam and a dielectric layer underneath the lower beam, and (b) fixed-fixed lower beam with no dielectric layer between the lower beam and the center conductor of the cpw [3]

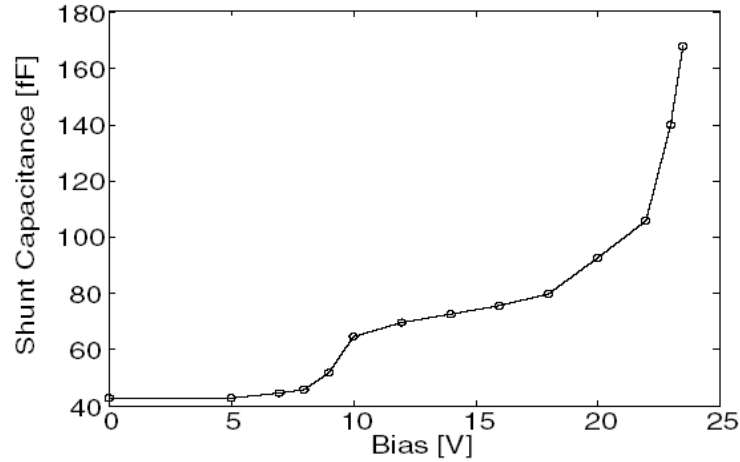


Figure 2.11 Extracted shunt capacitance of the MEMS varactor as a function of the applied bias voltage. The tuning range of this capacitor is nearly 300% [3]

2.5 Flip-Chip MEMS Varactor (1-D and 2-D array)

A MEMS varactor that has a quality factor of 80 at 40 GHz was reported in [4]. The high resistive silicon substrate and the high conductive materials, such as gold and chromium, used in fabricating the capacitor enhanced the obtained quality factor.

It is well known that low-resistivity silicon used in IC foundry processes is not a good substrate for RF applications due to its high losses at RF frequencies. Therefore, a flip-chip assembly process with silicon removal technology has been developed to transfer MEMS from silicon to a ceramic substrate containing RF circuits [5]. Using this technology, [4] reported a capacitor array design, which is shown in Fig. 2.12(a) and Fig. 2.12(b). The plates of the array snap down one-by-one, theoretically. However, this capacitor array needed improvement for the following reasons: a) Fig. 2.13(a) shows the effect of the variation in bond height on the capacitive performance. b) the standoffs were not initially in contact with the substrate, the capacitive plates were forced to bend before pull-in. c) Finally, only 11% of the area of this 30

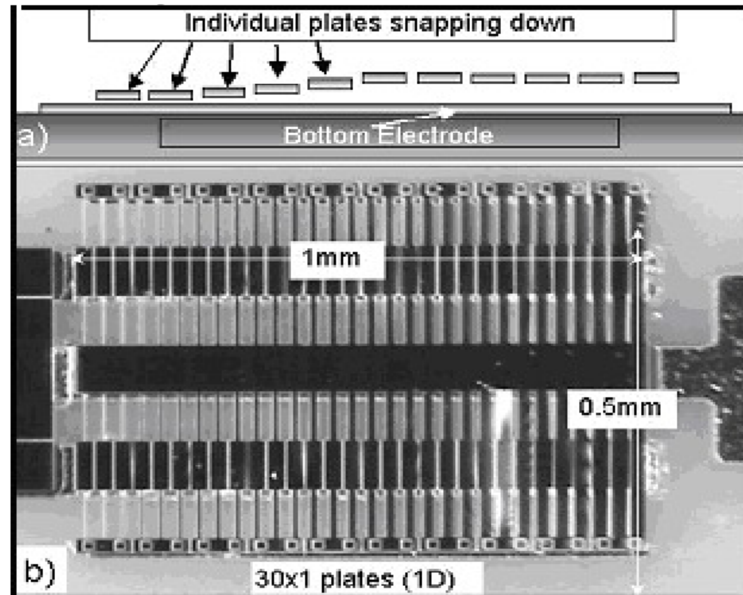


Figure 2.12 1-D flip-chip digital parallel-plate varactor: (a) principle of digital pull-in in MEMS varactors, and (b) SEM top view of the varactor [4]

plate one-dimensional (1-D) array was related to the capacitance change. Another design option for a 1-D varactor array of fixed-fixed beam, is shown in Fig. 2.13(b). However, this design also has disadvantages. For example, capacitance values can vary from plate to plate due to warpage caused by a coefficient of thermal expansion (CTE) mismatch. A 2-D array MEMS varactor was reported in [5]. The capacitor's array is assembled using flip-chip bonding with tethers on the donor substrate [5] and is illustrated in Fig. 2.14. The receiving substrate contains micro-strip transmission lines with indium bumps. In addition, a thin layer of alumina layer is deposited by atomic layer deposition (ALD) coating techniques [6] to prevent creating a short circuit when the collapse occurs. Before bonding, the MEMS chip is released in hydrofluoric acid (HF) followed by a CO_2 critical-point drying process to prevent sticktion. The MEMS varactor array is still connected to the silicon substrate by tethers. These tethers are then broken during the bonding process, leaving behind the top plate of the varactor. The schematic diagram of the assembled capacitor is shown in Fig. 2.15. The side-view illustrates how the capacitor plates maintain a

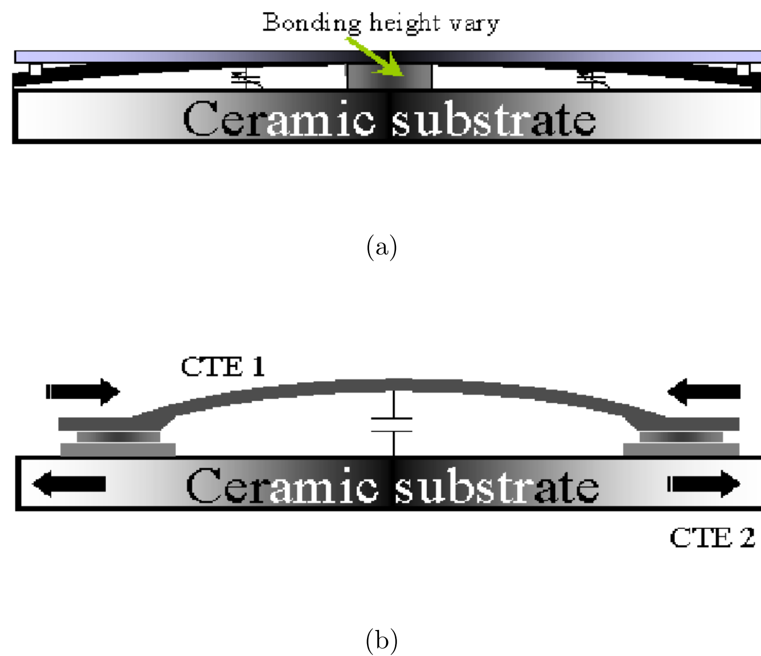


Figure 2.13 Problems in the reported MEMS varactor [4]: (a) residual stress effect in the reported 1-D array capacitor , and (b) thermal mismatch warpage that existed in the reported 1-D array varactor

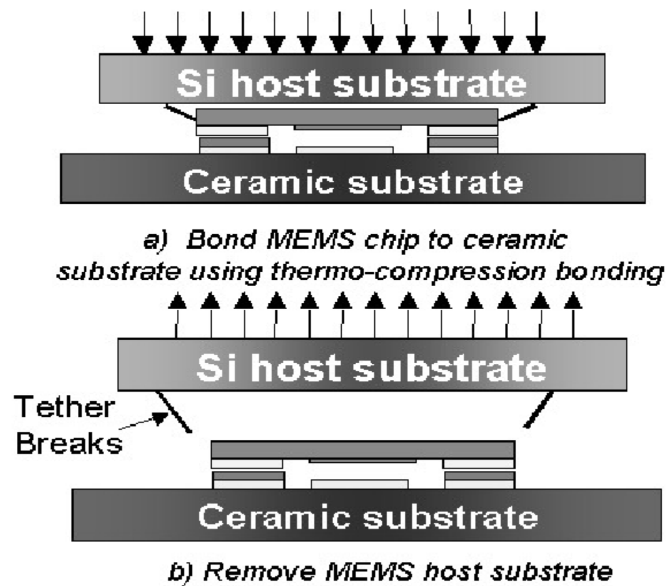


Figure 2.14 The flip-chip assembly of the 2-D array MEMS varactor [5]

uniform air gap with the substrate. Such a gap is achieved by the use of posts, which are critical to the precision flip-chip assembly process. In addition to maintaining a uniform air gap, the posts carry the vertical load during electrostatic actuation. The maximum capacitance, measured at 74 V with three plates snapped down, was

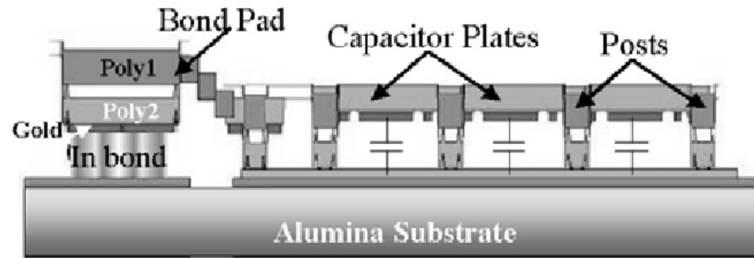


Figure 2.15 Side-view of 3 capacitor plates in the up position after flip-chip assembly [6]

C_{down}= 1.5 pF, as seen in Fig. 2.16. With more plates snapped down, the capacitance would be further increased. At present, the applied voltage is limited to the breakdown voltage of the dielectric coating on the substrate. In addition, the digital increments of the capacitance are clearly shown in Fig. 2.16. The loss of the digital increments in the previous 1-D array reported in [4] was eliminated by the use of the precision flip-chip assembly process used in the 2-D array varactor. A comparison between the 1-D array varactor reported in [4] and the 2-D varactor reported in [5] which is an enhancement of the 1-D capacitor is included in Table 2.1.

2.6 Interdigitated "Comb" Varactor

An interdigitated varactor that demonstrated a tuning range between 1 pF and 5 pF, which is in the excess of 300%, was reported by [7]. The capacitor was made from a single crystal silicon, released then sputter coated with a higher conductive thin metal film to improve the electrical performance.

The interdigitated "comb" structure displacement relies on the electrostatic force

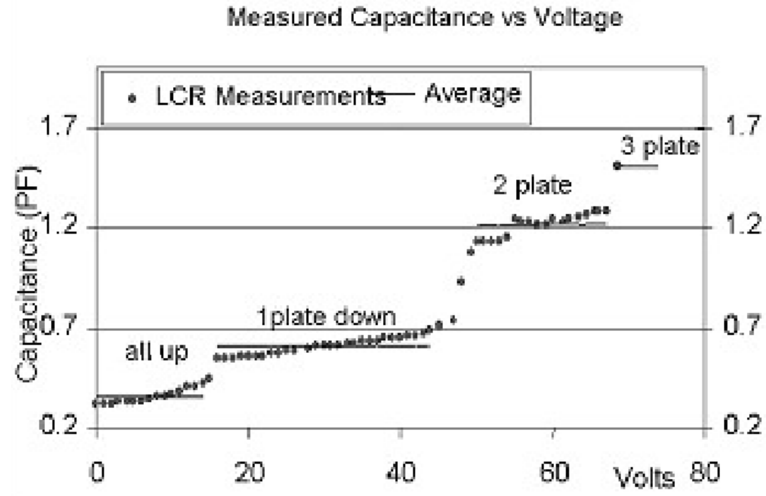


Figure 2.16 Capacitance measurements of a 3x3 array resulted in a tuning range of 4.7:1, achieved between 0.32 pF and 1.5 pF [5]

Table 2.1 Comparison between the 1-D array varactor and the 2-D array capacitor

	Hoivik *etal* (2001)	Faheem *etal* (2002)
RF Comparison		
Tuning Ratio	3:1	4.7:1
Q-Factor	140 at 745 MHz	$>$ 200 at 936 MHz
Capacitance	Continuous	Digital Steps
Integration with RF circuit	2-terminal device	Mounted on CPW, Micro-strip, 2-terminals
Mechanical Comparison		
Array Type	30x1 (1-D)	3x3 (2-D)
Overall Size Space Used For	0.5 mm x 1.0 mm	0.345 mm x 0.55 mm
Capacitance Ratio	11%	63%
Gap Height	almost 2 μm	2-4.75 μm as designed

generated by fringing fields at the ends of the "comb" structure, and thus is independent of and not limited by the gap spacing between the two electrodes. This configuration allows a large motion on the order of 10's μm with a relatively small actuation voltage, providing a large tuning range for the varactor. The independence of the maximum one third distance does not have the 50% tuning-range limitation. However, it occupies a huge area of the silicon substrate in comparison with the parallel-plate varactor. Moreover, the high aspect ratio of such devices which goes up to 30 μm in height, produces huge structural capacitors. The SEM photograph of the fabricated comb varactor is shown in Fig. 2.17 whereas Fig. 2.18 illustrates the obtained S_{11} for the measured capacitor. It is clear from Fig. 2.18(a) that the capacitor suffered a huge parasitic disturbance in the S_{11} response. A second fabricated capacitor was tested but this time a portion of the silicon substrate was etched away. The obtained response in Fig. 2.18(b) shows the enhancement in the RF response up to 6 GHz.

2.7 Integrated MEMS/CMOS Varactor and its Implementation in a BPF

Diode varactors with high capacitance ratios can be fabricated in CMOS processes. These varactor diodes exhibit high non-linearity, and extreme loss at high frequency and over their tuning range. An alternative device for this diode that promises superior performance is a MEMS varactor. Also, these MEMS varactors can be built monolithically in CMOS chips which solves other loss and coupling issues by replacing the off chip varactors with the on chip ones [8]. Fig. 2.19 shows a CMOS/MEMS varactor built using Carnegie Mellon University (CMU) post-processing technique that is reported in [9, 22]. The metallization layers that are used to make interconnects in CMOS process is employed to construct the comb varactor that is laterally actuated. The exposed oxide layers are etched anisotropically by dry etch and the

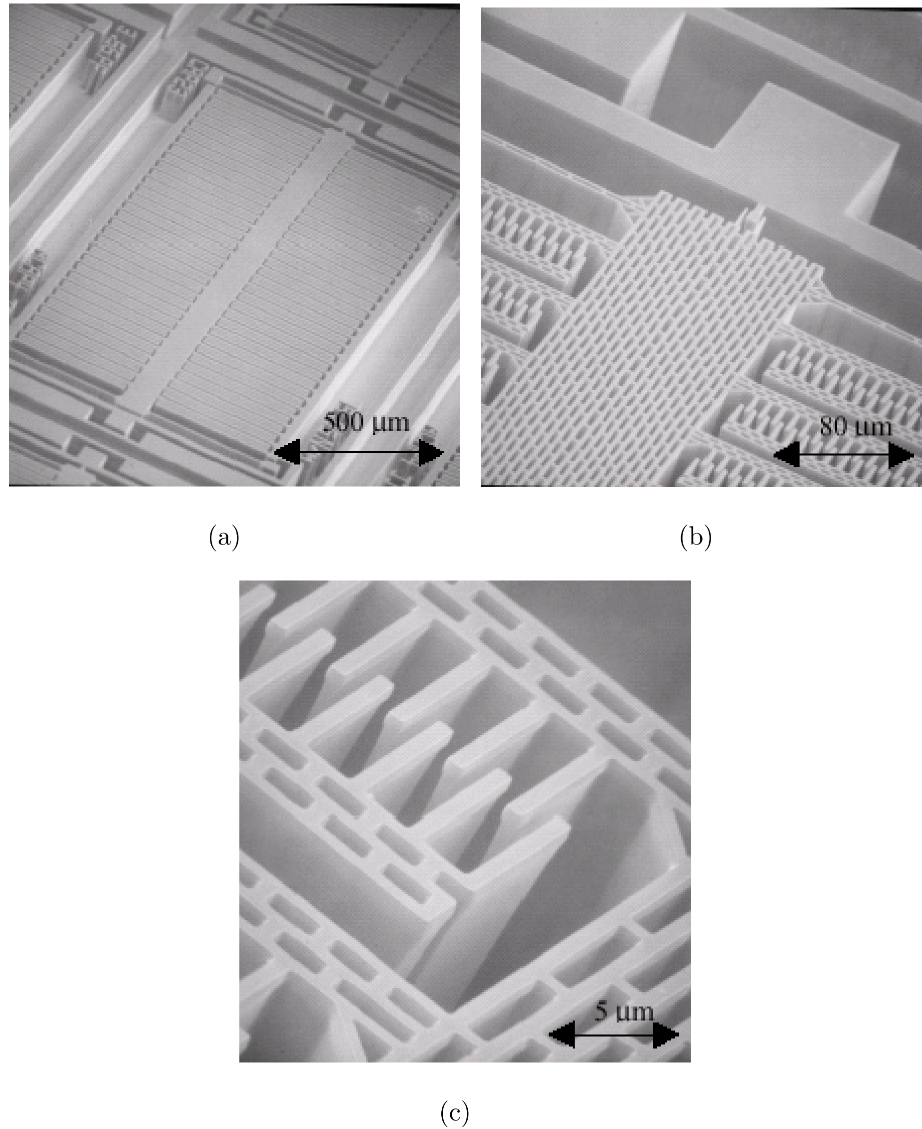
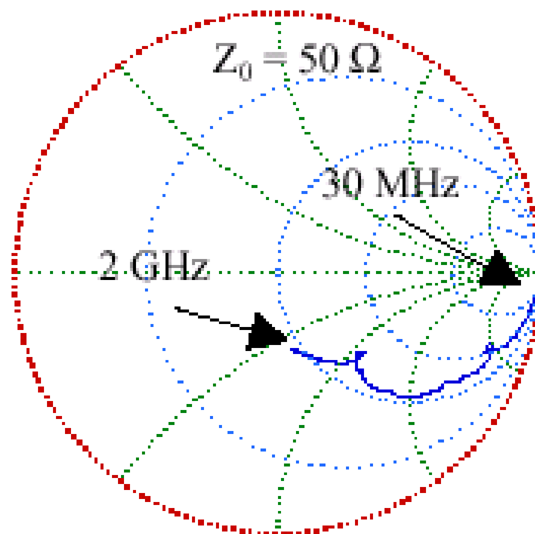
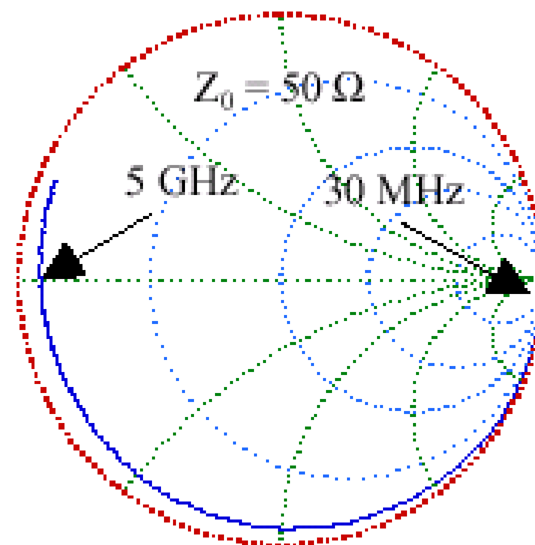


Figure 2.17 SEM graph of the interdigitated MEMS varactor [7]: (a) the overall capacitor, (b) zoomed SEM showing the arrays of the interdigitated combs, and (c) zoomed SEM showing the fingers of the comb



(a)



(b)

Figure 2.18 The return loss response S_{11} shows , (a) strong parasitic effects with silicon substrate intact, and (b) minimal parasitic effects with portions of the silicon substrate removed [7]

silicon substrate was etched away by anisotropic and then isotropic dry etch [8].

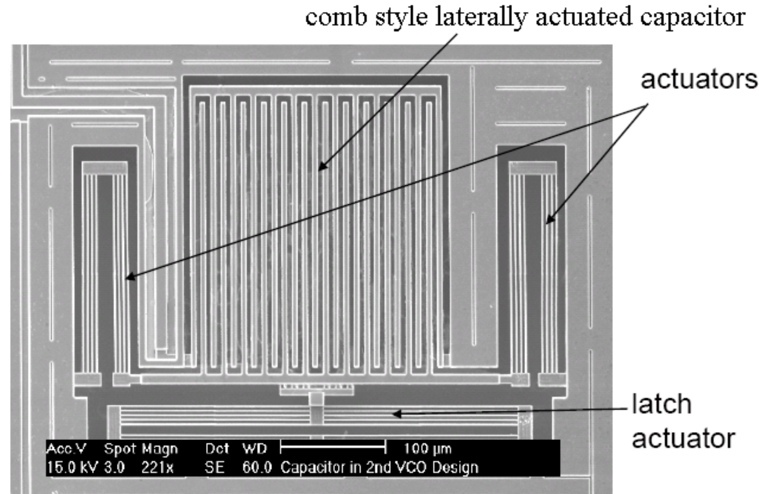


Figure 2.19 SEM picture of the released capacitor in TSMC 0.35 μm CMOS process [8]

MEMS tunable filters have the potential to replace off chip filters in RFICs. The high miniaturization, that MEMS tunable filters have, opens exciting possibilities to build one chip solution transceivers for multi-standard wireless bands in cell phones and wireless applications. Tunable filter using the CMU CMOS/MEMS post-processing technique were implemented and reported in [10]. The filter tunes from 1.87GHz up to 2.36GHz. The worst measured insertion loss is as high as 17dB in a fully integrated passive lumped element filter. Fig. 2.21 shows the fabricated filter and the measured insertion loss.

Higher quality factor MEMS varactor that has a Q of 65 at 1.5 GHz was reported by the Center for Integrated RF Engineering (CIRFE) at University of Waterloo [11]. The varactor was built using parallel-plate topology by dry etching oxide, and wet etching the silicon, metal 2 and metal 4 as depicted in Fig. 2.22. These etched metal layers work as a sacrificial layer and a mask layer, respectively. The etched sacrificial layer creates an air gap of 0.6 μm which is the thickness of metal 2. The maximum achieved trench depth for the reported varactor did not exceed 75 μm. The obtained

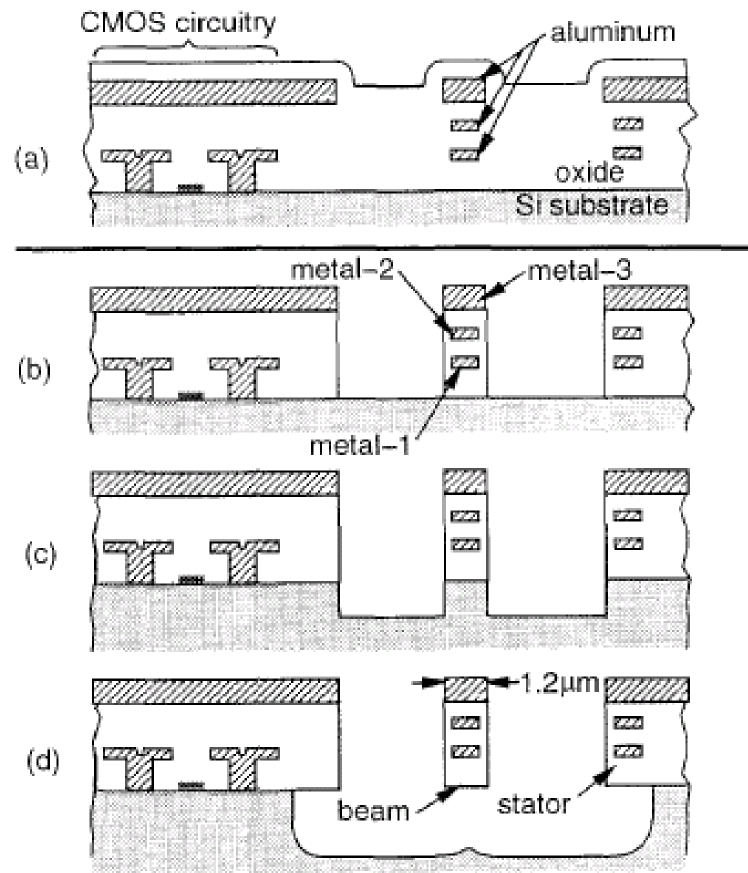
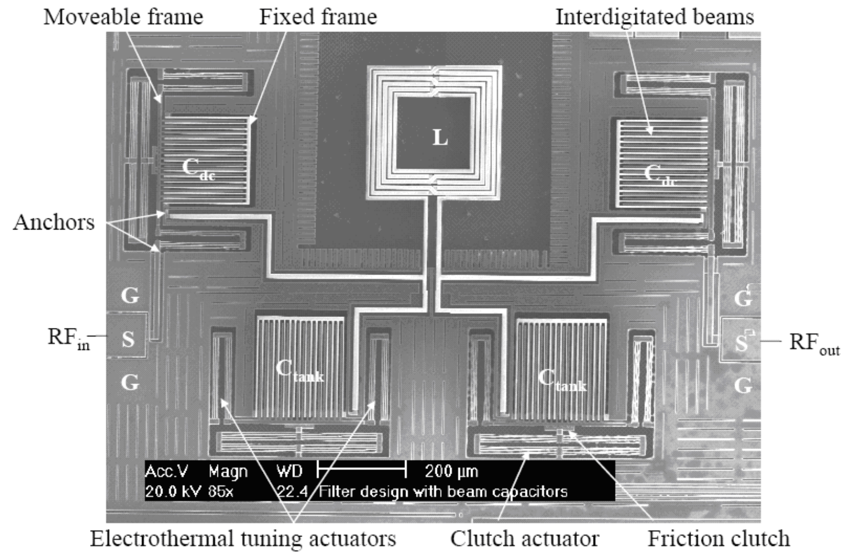
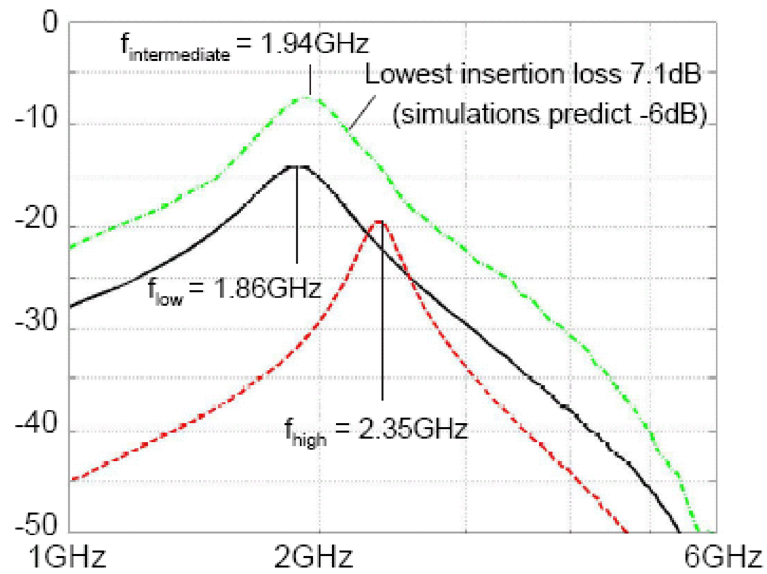


Figure 2.20 The flow of the post-processing steps performed at CMU: (a) before applying the post-processing, (b) after the anisotropic dry etch of the oxide, (c) after the anisotropic dry etch of the silicon substrate, and (d) after the isotropic dry etch of the silicon substrate to fully release the structures [9]



(a)



(b)

Figure 2.21 The MEMS tunable filter in BiCMOS technology: (a) an SEM picture of the fabricated MEMS tunable filter, and (b) the measured insertion loss of the MEMS tunable filter using lumped element topology [10]

trench in the silicon substrate limit the measured quality factor. The fabricated varactor is shown in Fig. 2.23.

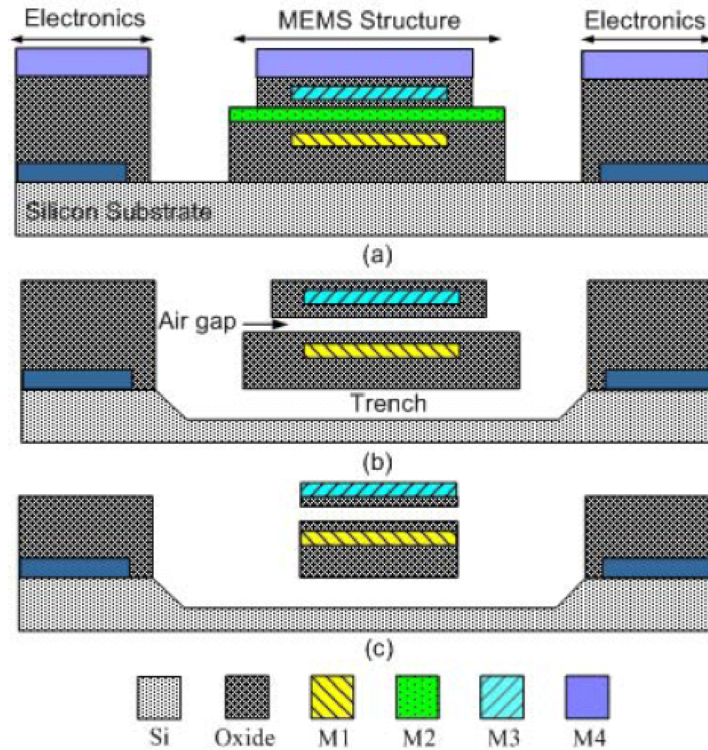


Figure 2.22 Cross-sectional view of the reported MEMS/CMOS post-processing technique in TSMC 0.35 μm CMOS process [11]

The reported MEMS varactor was implemented in a tunable two pole coupled resonators at a center frequency of 9.5 GHz and a bandwidth of 9%. The measured insertion loss of the reported filter was 5.66 dB and demonstrated a tuning ratio of 17% on the center frequency with a constant bandwidth as shown in Fig. 2.24.

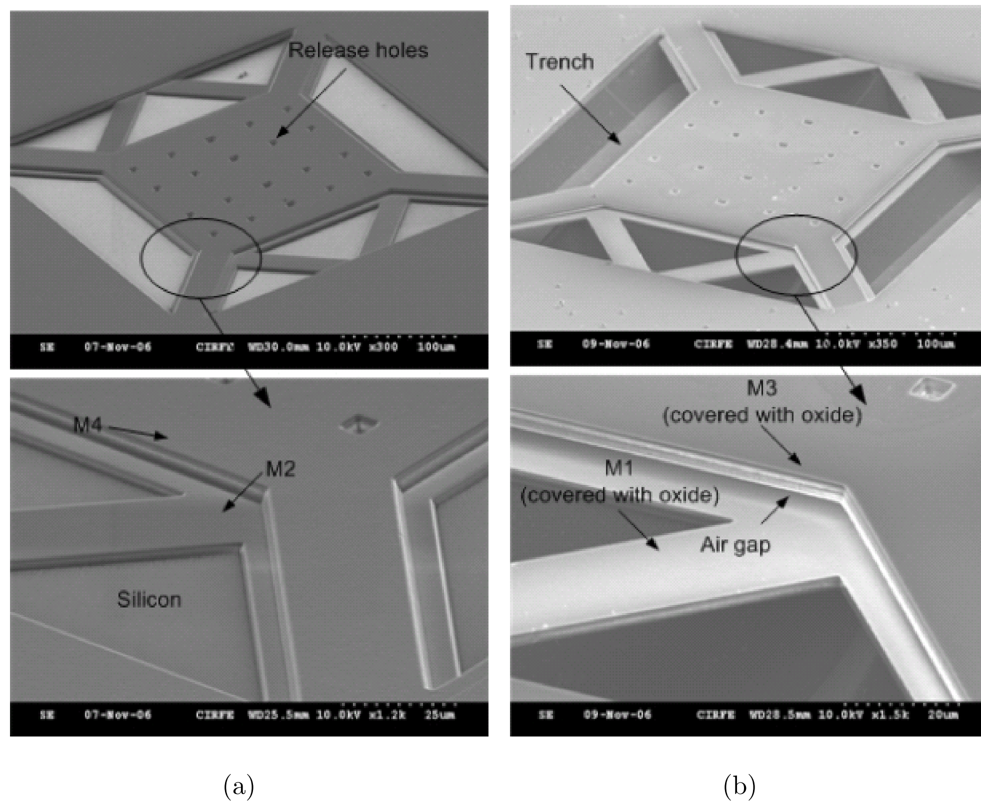


Figure 2.23 SEM image of the reported capacitor, (a) after the anisotropic dry etch of oxide, and (b) after the wet etch of the sacrificial layer and the silicon substrate at CIRFE [11]

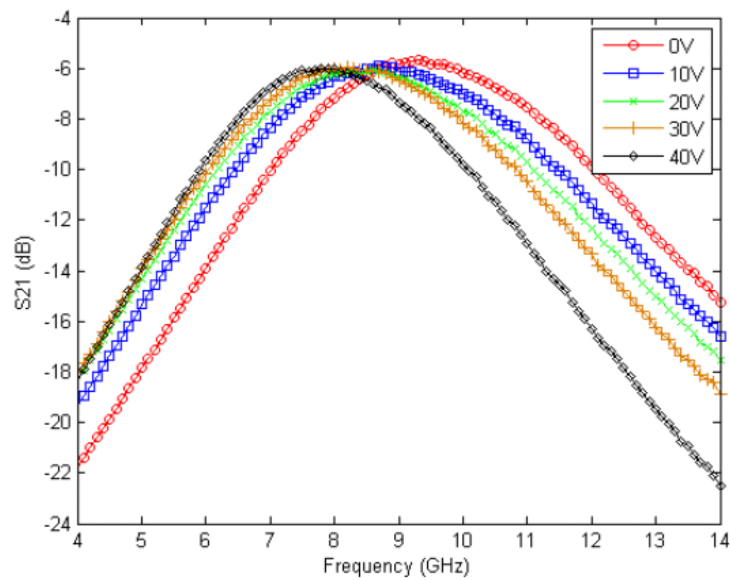


Figure 2.24 Measured response of the two pole tunable bandpass MEMS filter built in TSMC 0.35 μm CMOS process at different biasing voltages [11]

Chapter 3

Analog Continuous Parallel-Plate MEMS Variable Capacitors with High Tuning Capacitance Ratio

3.1 Introduction

MEMS variable capacitors have the potential to replace conventional varactor diodes in many applications such as phase shifters, oscillators and tunable filters. While there are various configurations to realize MEMS variable capacitors, the parallel plate configuration exhibits a relatively high Q value and is very convenient to build due to simplicity of its fabrication [1, 2]. However, such types of MEMS capacitors have a maximum theoretical tuning range of 50% due to the collapse of the capacitor structure as the voltage is increased beyond the pull-in voltage [1]. While interdigitated MEMS capacitors do not suffer from the pull-in voltage limitation, they exhibit low Q volumes and a low self resonance frequency [7, 23, 24] in comparison with the parallel plate capacitors.

A MEMS parallel plate capacitor with a wider tuning range was proposed in [2] by spacing the actuation electrodes differently from the capacitor's plates. Such an

approach has yielded a theoretical 100% tuning range. However, in practice, the capacitor demonstrated a tuning range of only 69.8%. There has been therefore a need to develop MEMS parallel plate variable capacitors with a much wider tuning range.

3.2 Two Movable-Plate Nitride-Loaded MEMS Variable Capacitor

In this section, we introduce the Two Movable Plate Nitride Loaded MEMS Variable Capacitor. The proposed configuration has three unique features that make it possible to achieve a superior performance in comparison with traditional parallel plate MEMS capacitors. These features are: the use of two movable plates, the use of a nitride layer between the two plates and the use of a trench underneath the capacitor's bottom plate. The capacitor is built using the MetalMUMPs process which has been recently released by MEMSCAP [25] for commercial use. We present theoretical and measured results that verify the validity of the proposed approach.

3.2.1 Proposed MEMS capacitor design

Fig. 3.1 illustrates a schematic diagram of the proposed capacitor. It consists of two movable plates with an insulation dielectric layer on top of the bottom plate. With the two plates being flexible, makes it possible for the two plates to attract each other. The capacitor demonstrated an extended tuning range even after the two plates touched each other.

The capacitor is constructed using two structural layers, three sacrificial layers, and two insulating layers of nitride. The top plate is fabricated from nickel with a thickness of 26 μm covered by a gold layer of 2 μm thickness, while the bottom plate is made of polysilicon covered by a nitride layer of a thickness of 0.35 μm.

Fig. 3.2 illustrates the different layers used to construct the capacitor using the

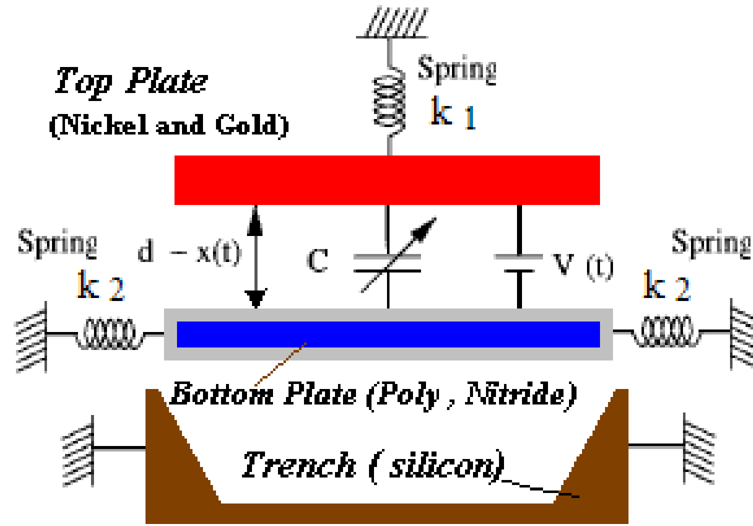


Figure 3.1 A schematic diagram of the proposed capacitor.

MetalMUMPs process [25]. The 2-D layers given in this figure are generated using CoventorWare [26]. First, a layer of 2 μm of oxide is deposited on the silicon substrate to form an isolation layer as illustrated in Fig. 3.2(a). Then a 0.5 μm oxide is deposited and patterned as illustrated in Fig. 3.2(b). This oxide layer outlines the area that will be used to etch a trench in the silicon substrate. The first nitride layer of 0.35 μm thickness is deposited and patterned as illustrated in Fig 3.2(c). This nitride layer forms the bottom cover of the polysilicon layer and is used as a part of the capacitor's bottom plate. On top of the first nitride layer, a 0.7 μm layer of polysilicon is deposited and patterned to form the bottom conductive plate of the variable capacitor as shown in Fig. 3.2(d). The last step in building the bottom plate of the variable capacitor is to deposit the second nitride layer on top of the polysilicon layer to form the isolating area that prevents any electrical contact between the two plates as illustrated in Fig. 3.2(e).

A 1.1 μm layer of second oxide is then deposited and patterned as illustrated in Fig. 3.2(f). The second oxide layer is etched so that the metal layer is anchored on the nitride and a physical contact between the bottom electrode (polysilicon) and the

two outer pads is ensured.

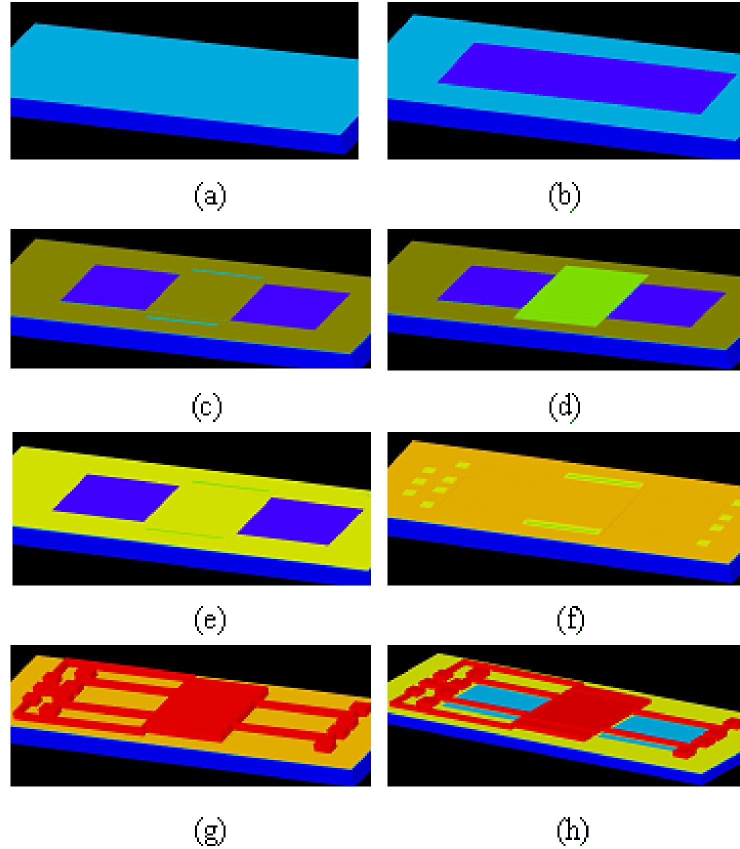


Figure 3.2 The fabrication process of the MetalMUMPs that used to build the proposed variable capacitor: (a) silicon substrate, (b) a deposited layer of oxide, (c) first nitride layer, (d) poly layer is deposited and patterned, (e) second nitride layer is deposited and both nitride layers are patterned, (f) second oxide layer is deposited, (g) nickel layer is then electroplated and the mold is removed, and (h) the MEMS varactor is released.

The last layer is the metal layer, which is composed of 26 μm of nickel with 2 μm of gold on top of it. The nickel layer is deposited and patterned as shown in Fig. 3.2(g). The capacitor is then released using a wet etchant and the trench is formed by etching the silicon substrate as illustrated in Fig. 3.2(h). The last step is to etch out the sacrificial layers as well as to etch a trench in the silicon substrate. The trench etch of the substrate is determined by the first oxide layer. Once the first

oxide is etched away by opening holes through the nitride layer, the solvent will etch the isolation layer underneath. The silicon substrate is then etched to form a trench of a depth of 25 μm. The total depth from the bottom plate of the variable capacitor is 27.5 μm. Fig. 3.3 shows the top and cross section views of the proposed MEMS variable capacitor.

In order to get a reasonable value for the beams restoring forces that suspend the heavy nickel top plate, the pull in voltage was chosen to be 24 V. A T-type suspension was used to design the anchors [1]. The calculated K value was found to be 344 N/m for each beam, leading to a beam length of 610 μm. The Young's modulus of nickel is assumed to be 202 Gpa.

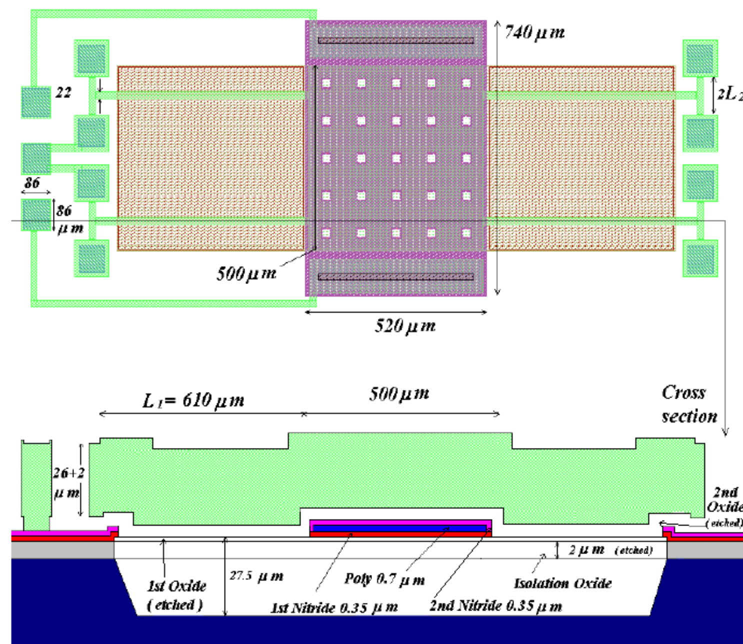


Figure 3.3 The top and cross section views of the proposed variable capacitor.

3.2.2 A General Lumped Element Modeling Of The Parallel-Plate Capacitors

A general lumped element modeling for parallel plate variable capacitors requires that both plates are movable. In this case, the induced electrostatic force between the two plates moves them toward each other. Fig. 3.4 is a schematic diagram of a general case, of a MEMS parallel-plate variable capacitor, with movable plates. To verify the proposed model, a variable capacitor that has plates of different thicknesses is characterized by using the analytical model and ANSYS. The capacitor's plates are assumed to be rigid in both models. To find the displacement of each plate, the two moving plates are formulated as follows:

$$F_e = \left[\frac{\epsilon_o \cdot A \cdot V_{in}^2}{2 \cdot d^2} \right], \tag{3.1}$$

$$F_{x1} = K_1 \cdot X_1, \tag{3.2}$$

$$F_{x2} = K_2 \cdot X_2, \tag{3.3}$$

and

$$g_o = d + X_1 + X_2, \tag{3.4}$$

where

F_e : induced electrostatic force

ϵ_o : dielectric constant of air

A : overlapping area

g_o : initial air gap

V_{in} : input voltage

d : air gap

K_1 : spring constant for the top plate

K_2 : spring constant for the bottom plate

X_1 : displacement of the top plate (downward)

X_2 : displacement of the bottom plate (upward)

F_{x1} : restoring force for the top plate

F_{x2} : restoring force for the bottom plate

At equilibrium and after applying the dc bias voltage, $F_e = F_{x1} = F_{x2}$. From this equation, X_1 in terms of X_2 is computed as follows:

$$X_1 = (K_2/K_1) \cdot X_2 \tag{3.5}$$

Then, by substituting (3.5) in (3.4) yields:

$$g_o = d + (K_2/K_1) \cdot X_2 + X_2 \tag{3.6}$$

or

$$g_o = d + r \cdot X_2 + X_2 \tag{3.7}$$

where $r = K_2/K_1$. Then, X_2 is found in terms of d as follows:

$$X_2 = (g_o - d)/(r + 1) \tag{3.8}$$

By substituting (3.8) in (3.3),

$$F_{x2} = K_2 \cdot (g_o - d)/(r + 1) \tag{3.9}$$

By solving (3.1) and (3.9) numerically for d, the gap between the two plates is calculated. From (3.5) and (3.8), the maximum displacement for both plates is found. An arbitrarily chosen conventional capacitor with plates 210 μm X 230 μm with four

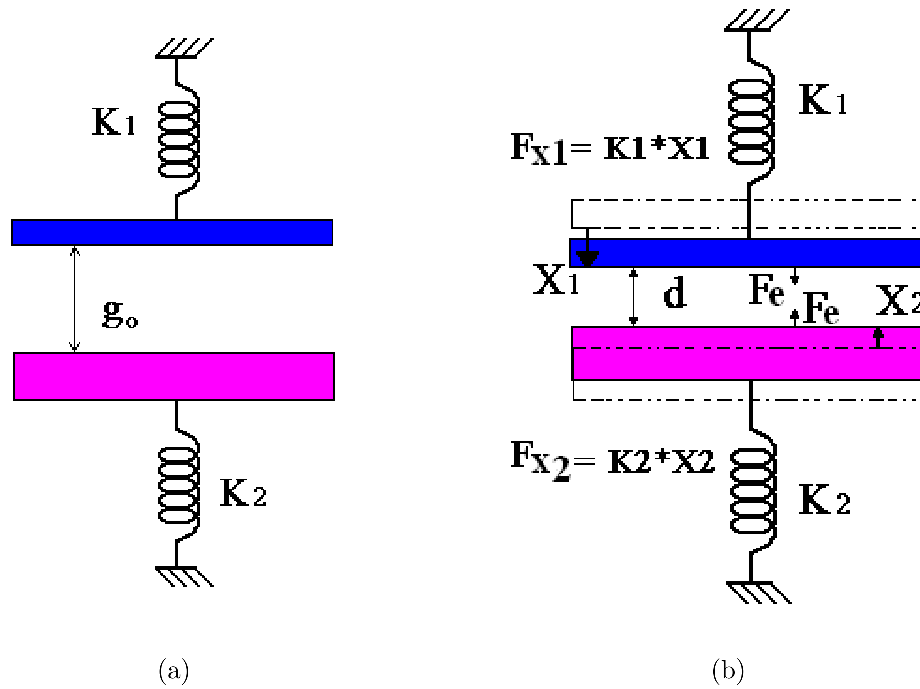


Figure 3.4 A schematic diagram for a typical parallel-plate variable capacitor: (a) at equilibrium before applying *dc* bias voltage, and (b) at equilibrium after applying *dc* bias voltage between the two plates.

guided beams for each plates, is selected. These beams have a width of 10 μm, a length of 107 μm, and a Young's modulus of 170 GPa with an air gap of 2 μm, as depicted in Fig. 3.5. These dimensions are chosen in our analytical lumped element model and the ANSYS model. The plates in ANSYS model are made rigid as well. The spring constant for the top plate is fixed at K_1=18.62 N/m for a thickness of t_1=1.5 μm, whereas the thickness of bottom plate t_2 is swept from 1.5 μm up to 4.17 μm.

Fig. 3.6 illustrates a comparison between the lumped element model and the AN-

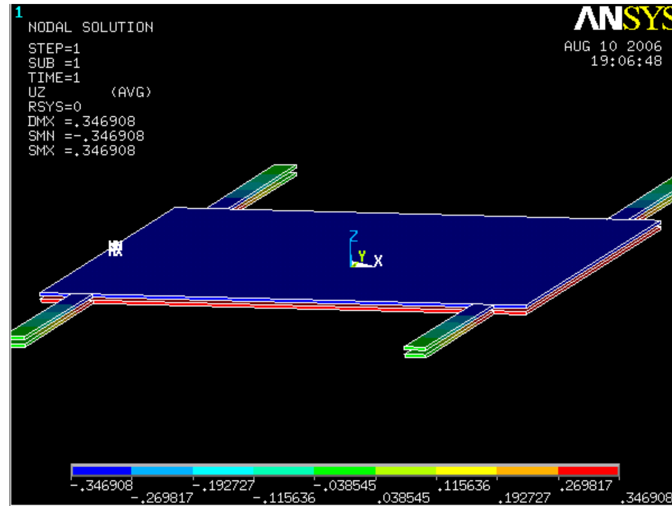


Figure 3.5 A 3-D structure of the FEM model deformed in ANSYS software.

SYS model for the same variation in the thickness of the bottom plate with its beams. A maximum deviation of 0.7 volt is observed at the maximum thickness which is t_2=4.17 μm, corresponding to a spring constant of K_2=400 N/m that is relatively rigid to K_1=18.62 N/m. The maximum error obtained between both models is 7%. In addition, the model in ANSYS requires a higher actuation voltage than the analytical model. This is expected since the analytical model uses a lower order function to calculate the deflections of the suspension system. Table 3.1 indicates displacements X_1 and X_2 of the top and bottom plates, respectively, and the beam's thickness and the pull-in voltage for the ANSYS model. Table 3.2 indicates the same parameters for the lumped element model.

There are two special cases of this general model. The first case is observed when the bottom plate is anchored to the substrate,(K_2=400 N/m in Fig. 3.6), and the top plate is released and movable, whereas the second case is observed when both plates are suspended and movable with identical spring constants (K_1=18.62 N/m and K_2=18.62 N/m in Fig. 3.6). As seen in Fig. 3.6, the required *dc* bias voltage to achieve the pull-in for the ANSYS model is 10.7 volts when the top plate is fixed, and the required *dc* bias voltage, when both plates are suspended and spring constants

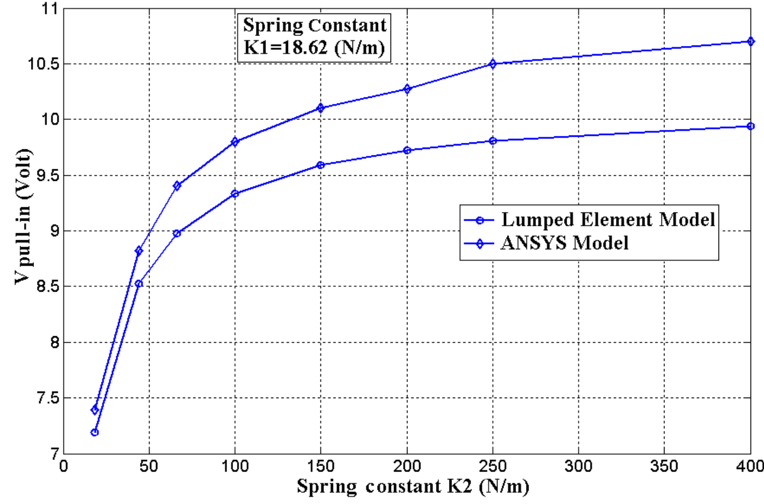


Figure 3.6 A comparison between the analytical model and the FEM model showing Pull in voltage for different spring constants of the bottom plate while fixing the spring constant of the top plate at K_1 =18.62 N/m.

are identical in the same model, is 7.4 volts. By comparing the two cases, it is evident that the *dc* bias voltage for the case in which both plates are moving and identical is 44% less than for the case with one fixed plate and one moving plate.

This method is useful for predicting the bottom plate displacement which, typically, is hidden by the top plate. Once the displacement of the top plate is measured, that of the bottom plate can be calculated by (3.5). For example, if a capacitor has a top plate thickness of t_1=1.5 μm and a bottom plate thickness of t_2=2.63 μm, to find the displacement of the bottom plate, then, only the top plate displacement needs to be measured. For this case, the corresponding displacement from Table 3.2 for the top plate is X_1=0.5566 μm. This means from (3.5), X_2=0.103 μm, which is the same derived displacement of the analytical model for t_2=2.63 μm.

The extracted displacement from the ANSYS model for the previous example is X_2=0.112 μm. The movable plates not only reduce the actuation voltage but also the vibration noise response, since both plates should exhibit the same response. This noise can be further mitigated, if plates of identical thickness and material are used, a situation that also means the spring constants are identical.

Table 3.1 Max. displacement of the two plates for different thicknesses and their corresponding spring constants for the ANSYS model for t_1=1.5 μm and K_1 = 18.62 N/m.

$t_2(m)$	$K_2(N/m)$	$X_1(m)$	$X_2(m)$	$V_{pull-in}V$
1.5	18.62	0.325	0.325	7.39
2.0	44.145	0.456	0.204	8.82
2.3	66.00	0.543	0.164	9.40
2.63	100.00	0.548	0.112	9.8
3.0	150.00	0.565	0.078	10.10
3.31	200.00	0.574	0.059	10.27
3.57	250.00	0.661	0.056	10.50
4.17	400.00	0.690	0.037	10.70

Table 3.2 Max. displacement of the two plates for different thicknesses and their corresponding spring constants for the lumped element model for t_1=1.5 μm and K_1 = 18.62 N/m.

$t_2(m)$	$K_2(N/m)$	$X_1(m)$	$X_2(m)$	$V_{pull-in}V$
1.5	18.62	0.331	0.331	7.191
2.0	44.15	0.464	0.195	8.527
2.3	66.00	0.516	0.145	8.979
2.63	100.00	0.557	0.104	9.33
3.0	150.00	0.588	0.073	9.59
3.31	200.00	0.604	0.056	9.72
3.57	250.00	0.617	0.046	9.81
4.17	400.00	0.636	0.029	9.94

3.2.3 Mechanical Modeling

CoventorWare was used to simulate the mechanical behavior of the proposed capacitor as the *dc* voltage was varied from $V_{dc} = 0.0\ V$ to $32\ V$ in steps of $2\ V$.

The CoventorWare software is based on Finite Element Analysis (FEM) which is very computationally intensive. In order to reduce the computation time, the structure was simplified as shown in Fig. 3.7. The anchors were clipped and the beams' lengths were compensated to have the same length from the anchoring points. This approximation helps to considerably reduce the mesh density of the simulated structure. The mechanical behavior of the proposed capacitor is expected to agree with the case before applying the simplification since the existence of the anchors can be replaced by applying mechanical boundary conditions at the clipping planes. It is noticeable from Fig. 3.7 that the bottom plate has deformed upward and touched the top plate of the variable capacitor. The bottom plate which is considered as a membrane, has a low restoring force K_2 that makes the bottom plate collapses at a relatively low voltage in comparison with the top plate.

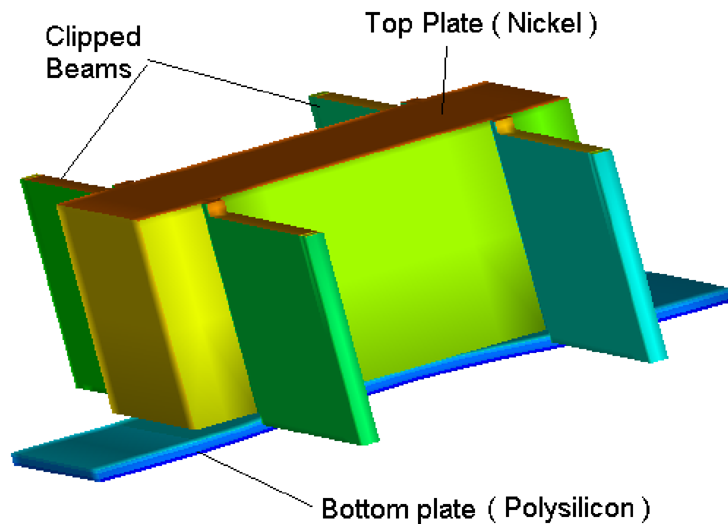


Figure 3.7 The deformation of the two movable plate nitride loaded MEMS variable capacitor simulated using CoventorWare and scaled 10 times in the Z-axis.

3.2.4 HFSS RF Simulation

The variable capacitor was transferred to HFSS and simulated as a one port network connected to a co-planar waveguide port of 50 Ω as shown in Fig. 3.8. A silicon substrate of 525 μm was used in the analysis.

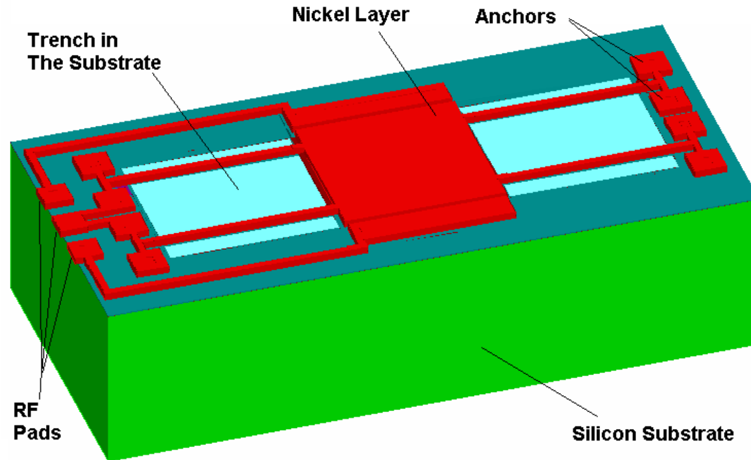


Figure 3.8 The two movable plate nitride loaded MEMS variable capacitor in HFSS.

The S_{11} response on the Smith chart was obtained over a frequency range from 1 GHz up to 6 GHz as illustrated in Fig. 3.9. The HFSS simulation results show that the capacitance at 1 GHz is 3.65 pF while the electrostatic theoretical value ($\epsilon A/x$) is 1.92 pF. The difference between the theoretical capacitance and the simulated RF capacitance, when zero *dc* voltage is applied, is due to the parasitic capacitances coming from the RF pads and the coupling between the top plate and the silicon substrate.

Fig. 3.10 shows the HFSS simulation of the capacitance assuming different gap values between the two plates. These simulations were conducted using gaps of 1.45, 0.95, 0.79, 0.65 and 0.55 μm including the 0.35 μm Nitride layer.

The capacitor was also simulated on HFSS as a two port network by adding a second set of RF pads on the other side of the capacitor as illustrated in Fig. 3.11.

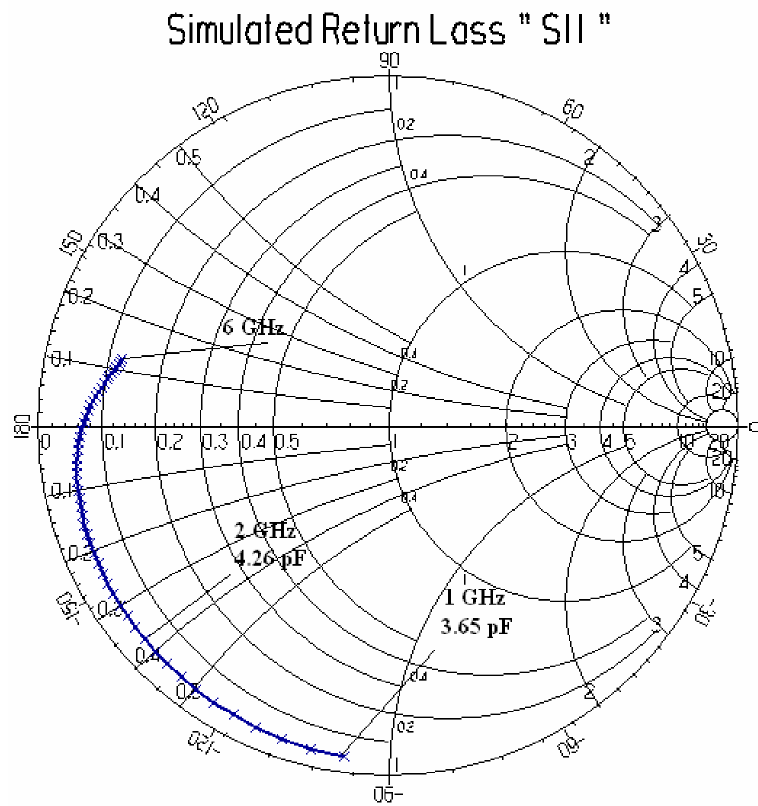


Figure 3.9 Simulated return loss on Smith chart.

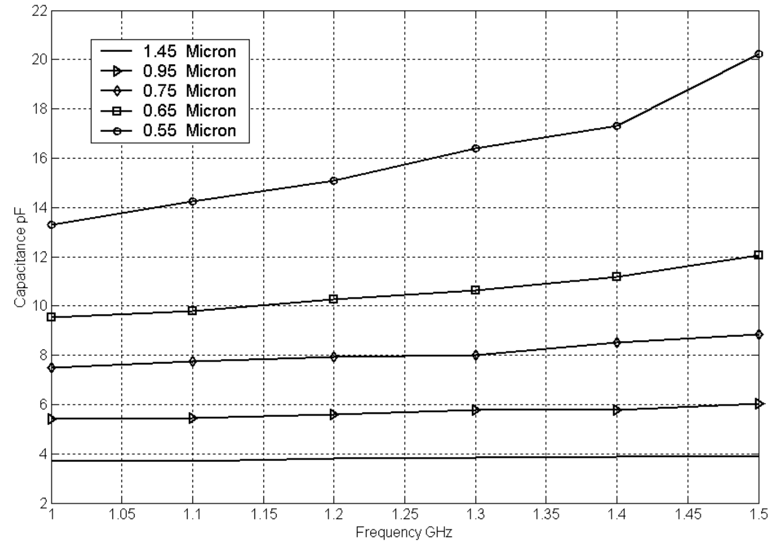


Figure 3.10 Simulated capacitance vs. frequency on deferent displacements.

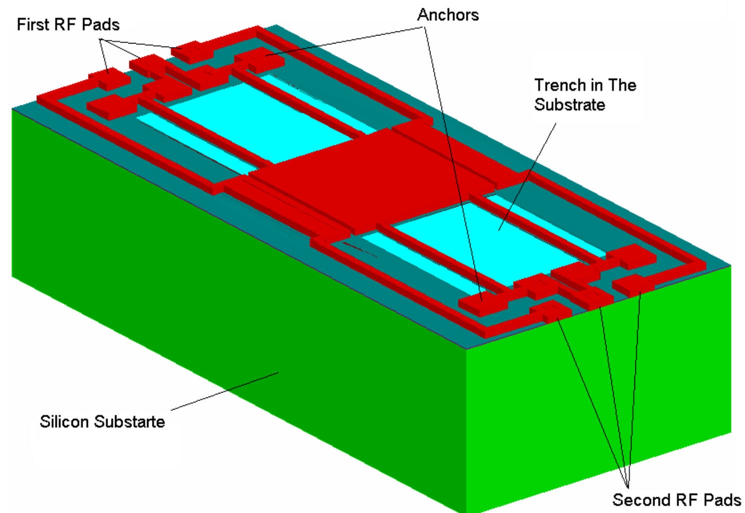


Figure 3.11 The two movable plate nitride loaded MEMS variable capacitor in HFSS as a two port network.

The detailed equivalent circuit of the proposed capacitor as a two-port network is shown in Fig. 3.12. The capacitance C_1 is the extracted capacitance that varies between the two plates due to the *dc* bias voltage applied. The capacitance C_2 is the coupling capacitance between the silicon substrate and the top plate of the variable capacitor which also varies due to the variation in the distance between the top plate and the substrate. The capacitance C_3 represents a parasitic component that comes from the RF pads which is illustrated in Fig 3.13. R_2 represents the loss due to the coupling to the silicon substrate. Finally, L_1 and R_1 are the inductance and resistance associated with the connections from the RF pads to the capacitor.

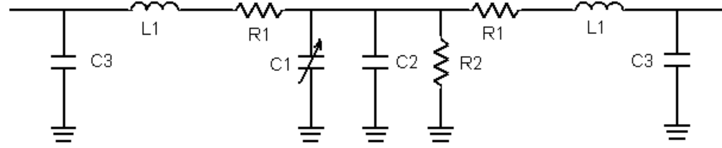


Figure 3.12 The equivalent circuit of the simulated proposed variable capacitor as a two-port network.

In order to extract the equivalent circuit, the proposed capacitor was simulated with different configurations. First, the capacitor was simulated as a one-port network and the total capacitance was obtained. Other simulations were conducted as well. In the first simulation, the RF pads were taken off and the capacitance was obtained and plotted against the original capacitance as illustrated in Fig. 3.14.

The dimensions of the RF pads are 87 μm *X* 87 μm built using a nickel layer. This is the second conductive layer which is anchored on the second nitride layer. The extracted RF pad capacitance is found to be 0.108 pF at 1 GHz.

There are three layers between the nickel and the silicon substrate. The RF pads are composed of: the isolation oxide, and the two nitride layers as shown in Fig. 3.13. The dielectric constant of the isolation oxide is taken as 4 while that of nitride is assumed to be 7. The thickness of the isolation oxide is 2 μm and the thickness of the

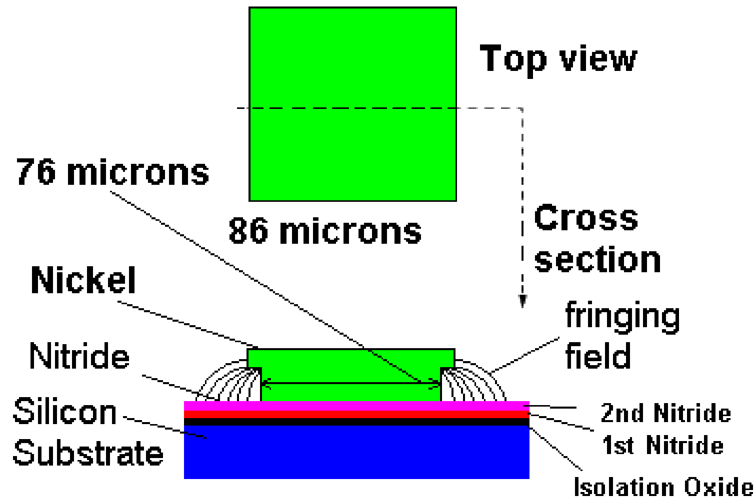


Figure 3.13 The top view and the cross section of the RF pad.

two nitride layers is 0.7 μm. The theoretical pad capacitance ($\epsilon A/x$) is found to be $C_{pad} = 0.0852$ pF. The extracted capacitance seems to be higher than the theoretical value due to the fringing field since the area of the nickel that touches the nitride is less than the original size of the pad as shown in Fig. 3.13. The outer dimension of the pad is 87 μm X 87 μm while the inner part that touches the nitride layer is 76 μm X 76 μm due to the fabrication rules. It is noticeable from the simulation conducted on the RF pads alone that the outer two pads which are connected to the ground have no effect on the obtained simulations. The simulated parasitic capacitance is then only for the signal pad.

In the second simulation, the silicon substrate was omitted. Fig. 3.15 shows the simulation results for the extracted capacitance without the substrate and with the silicon substrate that has a trench. The parasitic capacitance due to the lossy silicon substrate was obtained and plotted against the response of the capacitor with the silicon substrate that has a trench. This capacitance was found to be 1.35 pF at 1 GHz.

The low conductivity of the silicon substrate, which is 100 S/m, explains the

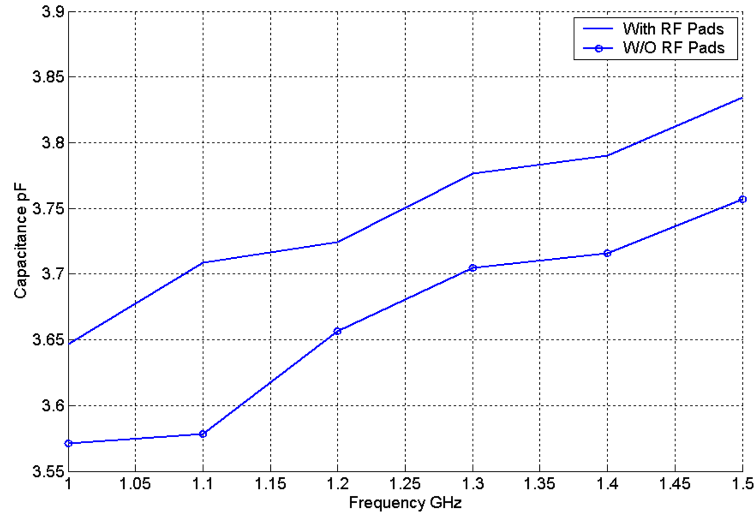


Figure 3.14 The extracted capacitance with and without the RF pads.

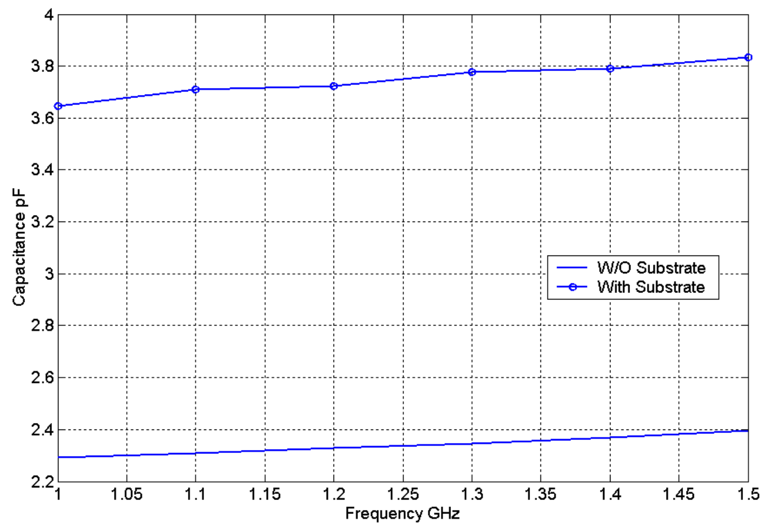


Figure 3.15 The extracted capacitance with the silicon substrate that has a trench vs. the extracted simulated capacitance without the substrate.

high losses obtained from the simulation. The trench that was etched underneath the proposed capacitor helps to reduce the effects of the silicon substrate. Since it won't be practical to completely omit the substrate, the trench in the silicon substrate helps to decrease the parasitic capacitance coming from the silicon substrate. Fig. 3.16 illustrates the parasitic capacitance that would exist if the trench underneath the two plates had not been used.

The inductance of the variable capacitor was extracted from the two port network simulation. The inductance was found to be 0.4 nH. The self resonance frequency of the proposed capacitor was almost 4.35 GHz as shown in the simulated S_{11} in Fig. 3.9 and this occurs when the *dc* bias voltage equals zero.

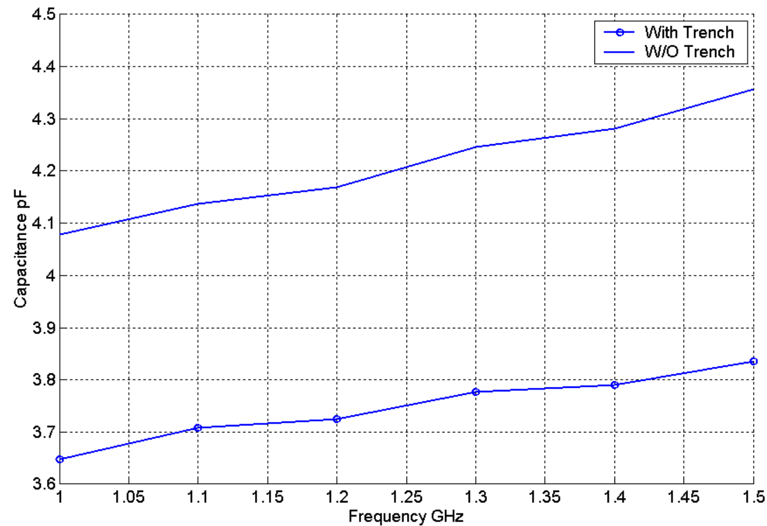


Figure 3.16 The simulated capacitance with the trench in the silicon substrate vs. the simulated capacitance when the trench is not there.

This self resonance frequency will increase when the *dc* bias voltage is applied and the capacitor's plates deform toward each other. The extracted capacitance of the two port network structure that is shown in Fig. 3.12 is plotted against the total capacitance of the one port network capacitor, which is represented by a capacitor, inductor and resistor in series, as shown in Fig. 3.17. It is clear from the results that the capacitance obtained in the two port network case is higher than that of the one

port case. This is attributed to the inductance of the beams and the connections between the RF pads and the capacitor's plates.

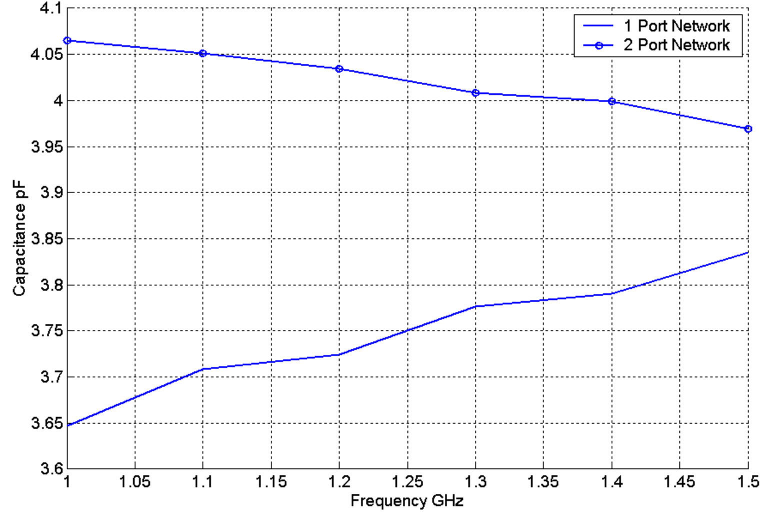


Figure 3.17 The extracted simulated capacitance for the two port network vs. the extracted simulated capacitance for the one port network.

3.2.5 The Quality Factor

The polysilicon is a lossy material. The quality factor Q is expected to be relatively low. This is due to the fact that the skin depth far exceeds the thickness of the 0.7 μm polysilicon bottom plate used in the MetalMUMPs process. Assuming a conductivity σ of $8.23 \cdot 10^4$ S/m at 1 GHz, the $\sigma/\omega\epsilon$ ratio for the polysilicon and the skin depth are given by:

$$\frac{\sigma}{\omega\epsilon} = 1.24 \cdot 10^4 \gg 100 \tag{3.10}$$

$$\delta = 55.5\ \mu m \tag{3.11}$$

The calculated Q in the fabricated capacitor at 1 GHz is obtained as $Q = 1/\omega RC$. Where $R = 3.9336\ \Omega$ is the resistance obtained from the measurement of the capacitor as a one port network. As illustrated in Fig. 3.18, ω is the frequency and C is the capacitance at the calculated frequency. The quality factor is then calculated and

found to be 8.784 at 1 GHz. As will be seen in Section 3.2.6, the quality factor Q can be improved by adding some slight modifications to the capacitor's structure.

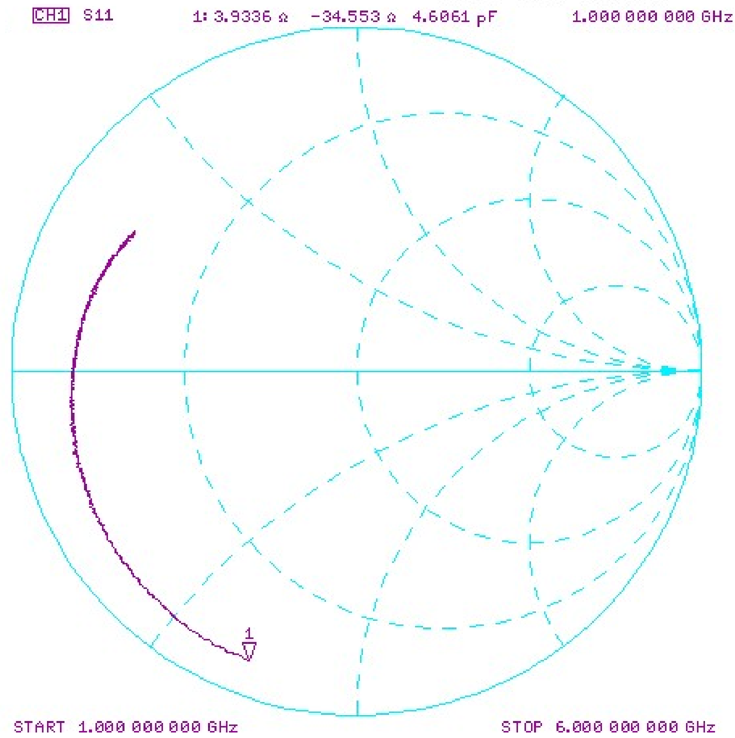


Figure 3.18 The measured return loss on Smith chart.

3.2.6 The Measurement

The measurements were done over the same frequency range of 1-6 GHz when a zero *dc* voltage is applied to the capacitor. The measured S_{11} response on the Smith Chart at $V_{dc} = 0\ V$ is given in Fig 3.9. At 1 GHz the measured capacitance value was found to be 4.6 pF. The difference between the HFSS results and the experimental results is attributed to the deformation of the top plate. Fig. 3.19 shows a SEM picture of the fabricated capacitor. A slight deformation is observed. The gravity effect of the relatively heavy 26 μm thick nickel top plate, which is 67.6 μg, causes initial deformation. The initial displacement of the top plate can be calculated using the

following equation [1]:

$$X_g = \frac{m \cdot g}{k} \tag{3.12}$$

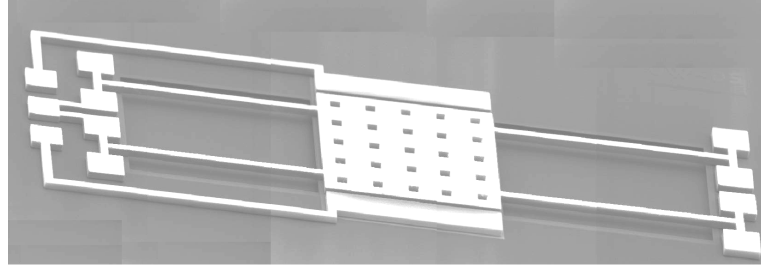


Figure 3.19 An SEM picture of the fabricated variable capacitor.

Where X_g is the initial displacement after releasing the variable capacitor, m is the mass of the plate, and g is the acceleration due to gravity $g = 9.80665\ m/s^2$. The calculated initial displacement is 0.5 μm. This reduces the spacing between the top and the bottom plate to 0.95 μm including the nitride layer. By taking such deformation into consideration in the HFSS simulation, the zero *dc* bias capacitance was found to be 5.4 pF. The difference between the measured and the simulated capacitance, in the zero *dc* bias case, is due to the residual stress and the accuracy of the electrical specifications of the materials used in the HFSS simulations.

A *dc* voltage sweep from 0 V *to* 39 V is applied to the variable capacitor. Fig. 3.20 illustrates the measured capacitance value for *dc* voltage steps over the frequency range of 1 - 1.5 GHz. At 1 GHz, the achievable tuning of the proposed capacitor is found to be 280% while the variable capacitor reached a higher tuning range of 495% at 1.5 GHz. The tuning response at 1 GHz is plotted in Fig. 3.21. The two plates came in contact with each other (with the nitride layer in between) at around 21.2 V.

It was observed however, that the capacitance still increases with applied *dc* voltages beyond 21.2 V. A zero *dc* current was observed even at 39 V. It is worth mentioning that the capacitor demonstrated the same performance when the test was repeated several times.

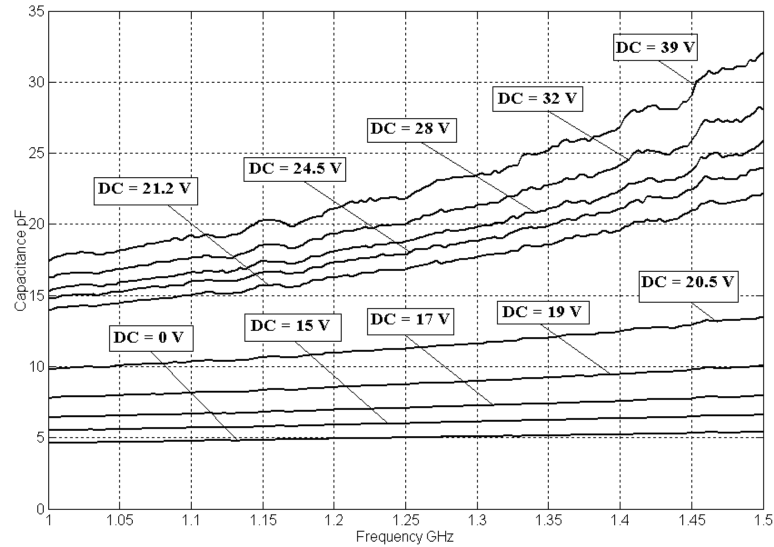


Figure 3.20 The measured capacitance vs. frequency at different *dc* voltages.

Before the collapse of the capacitor's plates, it is obvious from Fig. 3.21 that the capacitor demonstrated a tuning range of 117% at 1 GHz. The relaxation behavior of the capacitor and the non-linearity of the fixed-fixed beams in this case have extended the 50% tuning range limit of the traditional parallel plate MEMS capacitor [1]. Above 21.2 V the top plate and the bottom plate relaxed on each other due to the increase of the electrostatic force, which was induced by increasing the *dc* bias voltage. The tuning range of the proposed variable capacitor increased till it reached 280% at 1 GHz for a *dc* bias voltage of 39 V. Another variable capacitor with a smaller plate area (300 μm X 300 μm) was designed and fabricated. Several modifications were introduced to this capacitor in order to reduce the parasitic capacitances and to improve its Q value. A SEM picture of this capacitor is shown in Fig. 3.22. The parasitic capacitance coming from the anchors was reduced by using smaller anchors and by eliminating two anchor pads through the use of the center anchor as common anchor for the right and left beams. The dimensions of the beams were also redesigned to fit the smaller size plates. These beams have a width of 12 μm and a length of

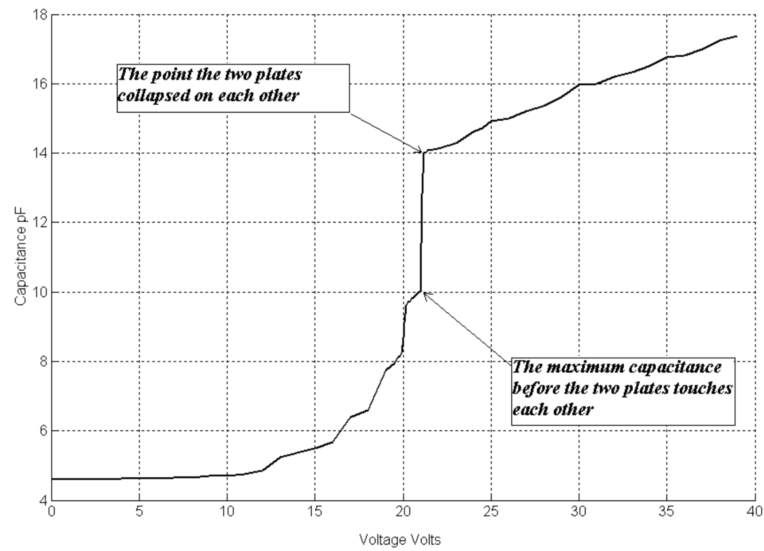


Figure 3.21 The measured tuning characteristics of the proposed capacitor at 1 GHz.

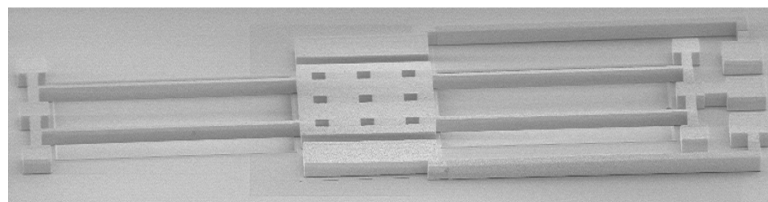


Figure 3.22 An SEM picture of the smaller fabricated variable capacitor.

566 μm. The heights of the beams were 20 μm nickel plus 0.5 μm gold. Fig. 3.23 illustrates the variation of the capacitor with the applied *dc* bias voltage.

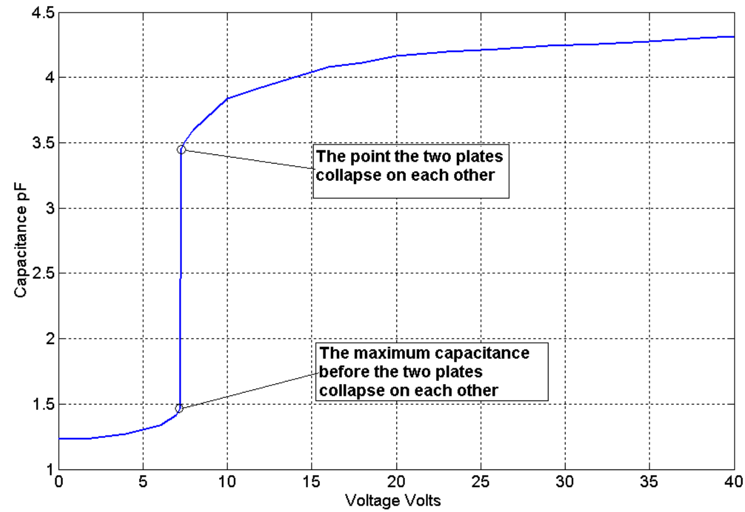


Figure 3.23 The measured tuning characteristics of the proposed capacitor at 1 GHz.

The small variable capacitor demonstrated a less smooth increment in the capacitance. We believe that the smaller dimensions used in this capacitor increased the rigidness of the top plate which caused a decrease in the strain on the plate before the collapse occurs. The quality factor of the small capacitor was calculated and found to be 13. The measured resistance of this capacitor $R = 14.83\ \Omega$ and the capacitance was 1.16 pF as illustrated in Fig. 3.24.

3.3 A High-Tuning-Range MEMS Varactor Using Carrier Beams

Over the past four years, several papers have reported improvements to the tuning range of such capacitors [3–5, 27–29]. References [3] and [28] have proposed a parallel-plate MEMS variable capacitor in which the actuation electrodes are spaced differently from the plates of the capacitor. Their approaches have yielded tuning

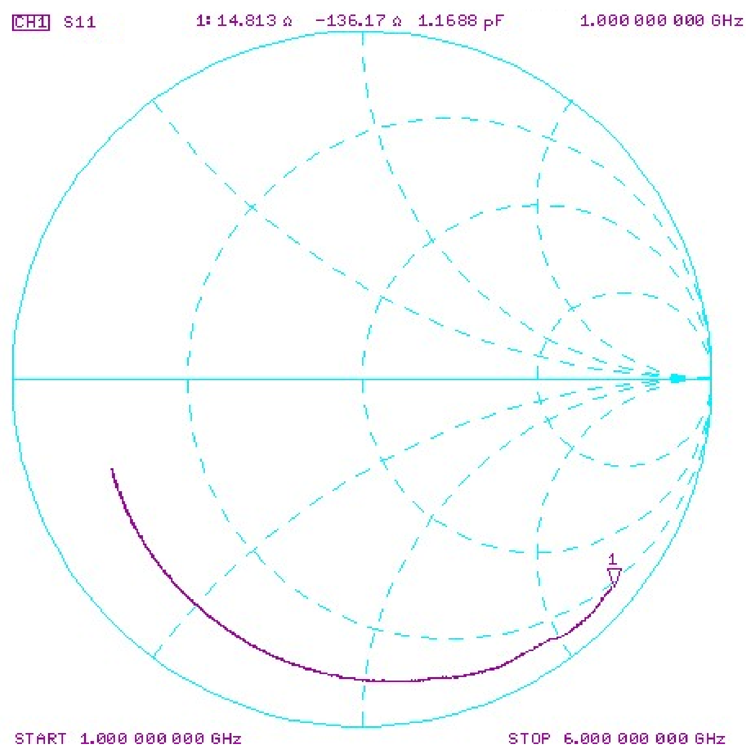


Figure 3.24 The measured return loss on Smith chart.

ranges of 300% and 443%, respectively. However, the latter suffers from low self-resonance. In [4] and [5], an array of parallel-plate capacitors with different beam sizes that demonstrates a tuning range of 370% has been proposed. A two-movable-plates MEMS variable capacitor with a nitride layer between the two plates has been proposed in [27]. Such a capacitor has a demonstrated tuning range of 280%. Finally, a parallel-plate MEMS variable capacitor using additional carrier beams has been reported in [30].

In the following section, we introduce a novel MEMS parallel-plate variable capacitor that is capable of achieving a tuning range of 410%. The proposed structure consists of a simple parallel-plate capacitor with four additional beams (carrier beams) placed between the two plates. The proposed structure is analyzed both theoretically and experimentally. Several capacitors have been built and tested. A detailed RF model of the capacitor, which takes into consideration all parasitic effects, is presented. The results obtained from this model agree well with measured data for various *dc* bias voltages. Consistent measured results are obtained for several sample capacitors.

3.3.1 Proposed MEMS Capacitor Design

Fig. 3.25 presents a schematic diagram of the proposed capacitor. The capacitor consists of one fixed plate (E_2), one movable plate (E_1) held by four attached supporting beams, and four carrier beams with their tips inserted between the two main plates of the capacitor. The carrier beams are built in such a way that free-standing cantilevers are formed. Since their tips are underneath the top plate, these beams are able to carry the top plate when it deflects downward toward the bottom plate. They prevent the top plate from collapsing onto the bottom plate when the traditional 50% [1] tuning point is reached. The capacitor is built using the PolyMUMPs [20] process, which consists of three structural layers and two sacrificial layers. E_2, which represents the bottom plate, was constructed using the poly0 layer. The carrier beams were built

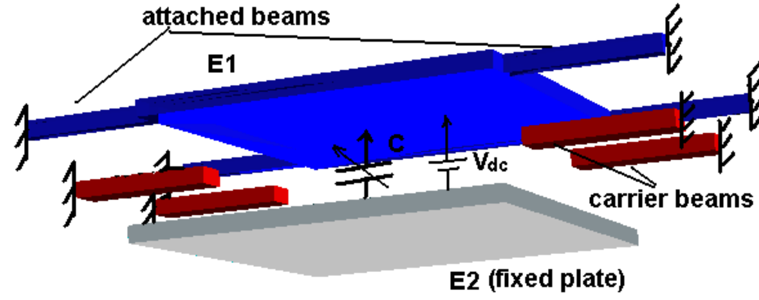


Figure 3.25 A schematic diagram of the proposed capacitor.

using the second structural layer (poly1). Finally, the top plate with the attached supporting beams was made from the last layer (poly2) with gold on top. Fig. 3.26 shows the top and cross-section views of the proposed MEMS variable capacitor, created with MEMSPro software. As mentioned, the carrier beams were built using the poly1 layer, and a vertical gap of 1.25 μm was achieved by using poly1-poly2-via, which etched away the second oxide and over-etched the first oxide by 0.75 μm as well. The space between the tip of the carrier beams and the top plate is equal to the thickness of the second oxide (0.75 μm).

3.3.2 Steady-State Response

With the carrier beams added, the electrostatic force, F_e, generated from an applied voltage V_{dc} is

$$F_e = \frac{1}{2}\frac{CV_{dc}^2}{(x_o - x)} = k_1 x, \quad 0 \leq x \leq x_o \tag{3.13}$$

$$F_e = \frac{1}{2}\frac{CV_{dc}^2}{(gap - x)} = k_1 x + k_2(x - x_o), \quad x_o \leq x \leq gap, \tag{3.14}$$

where C is the capacitance between the top and the bottom plates, x_o is the distance between the top plate and the carrier beams (0.75 μm), x is the variable distance between the top plate and the bottom plate, k_1 is the spring constant of the attached supporting beams, k_2 is the spring constant of the carrier beams, gap is the theoretical distance between the top plate and the bottom plate at zero dc bias

voltage (1.25 μm), and F_e is the induced electrostatic force. When the top plate is displaced downward, the suspension produces a restoring force represented as F_m. The magnitude of F_m is related to x by $F_m = k_m x$, where k_m is equal to k_1 before the top plate touches the carrier beams, and takes the form $k_m = k_1 + k_2.(x - x_o)$ after the top plate touches the carrier beams. Solving for the steady-state response, we find, at equilibrium, that the magnitudes of F_e and F_m are equal. In order to find the equilibrium point, the two functions F_e and F_m are plotted as illustrated in Fig. 3.27. Two solutions are observed for voltages less than the pull-in voltage, as shown in Fig. 3.27.

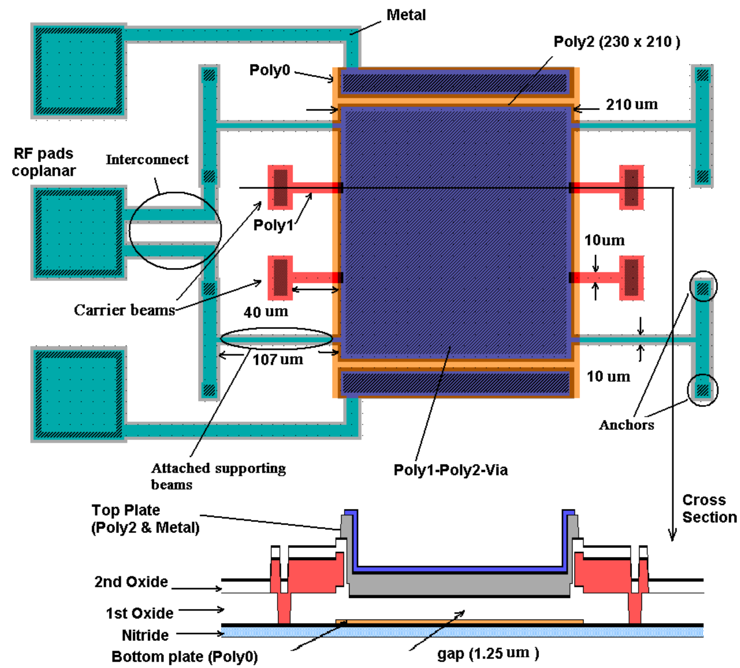


Figure 3.26 The top and cross-section views of the proposed variable capacitor.

The higher-displacement solution is an unstable solution, while the smaller displacement solution is stable [31]. As long as we have an intersection between the two curves, an equilibrium state is obtained and collapse is avoided. If we assume that no carrier beams exist in the capacitor, a maximum displacement of 0.417 μm (50%) is

expected to result when we apply a V_{dc} value of 4.73 V, as illustrated in Fig. 3.27. After this virtual collapse point is passed, the top plate touches the carrier beams. These beams add additional restoring force and oblige F_e to intersect with the new F_m, as shown in (3.14). The spring constant of the carrier beams must be much higher than that of the attached supporting beams in order to oppose the large electrostatic force that is induced when the distance between the two plates of the capacitor is reduced. This will allow F_e and F_m to achieve equilibrium solutions again. The new maximum displacement obtained from the lumped element modeling is 0.91 μm, and the new pull-in voltage is 7.4 V. Fig. 3.27 shows the new maximum displacement which occurs at 0.91 μm. This extended displacement is achieved because of the carrier beams added to the variable capacitor, which generate a spring-constant behavior to compensate for the nonlinear electrostatic force demonstrated by the applied voltage across the capacitor's plates.

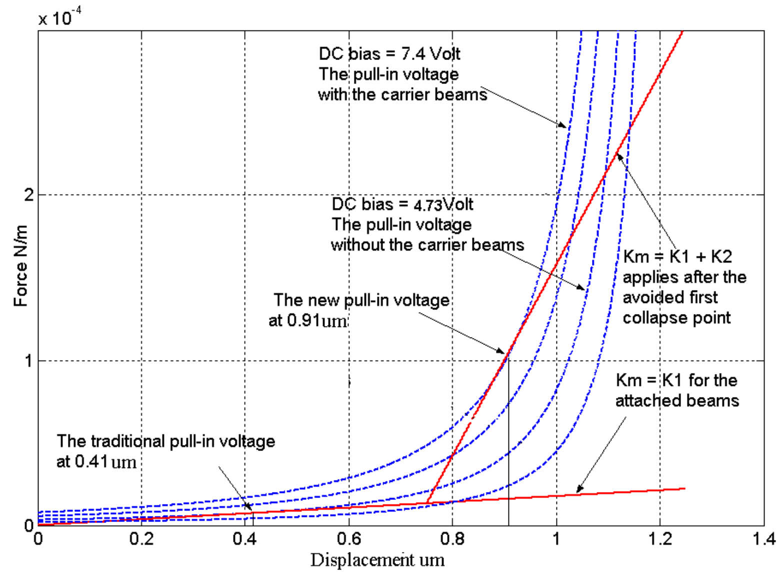


Figure 3.27 The lumped element analysis of the proposed capacitor with the carrier beams.

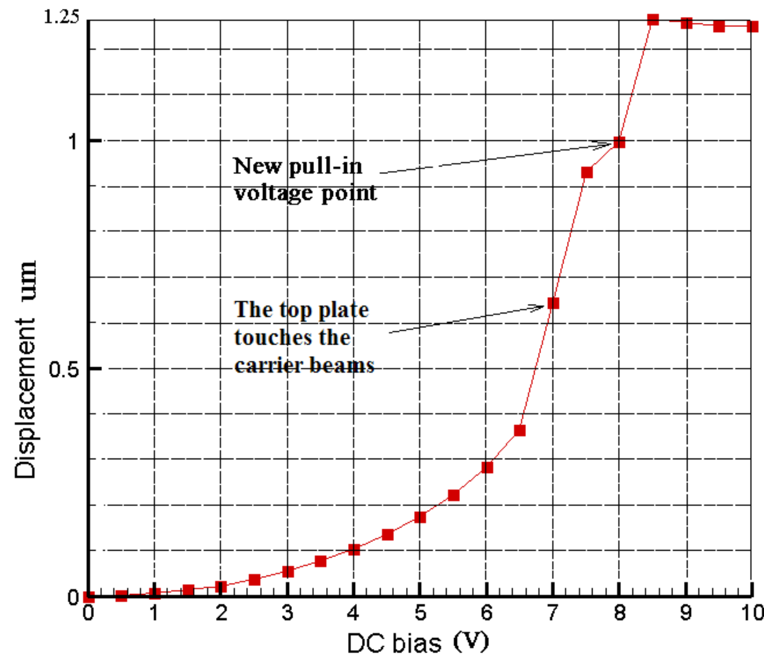


Figure 3.28 The simulated tuning range of the proposed capacitor.

3.3.3 The Electromechanical Simulation

CoventorWare software was used to simulate the mechanical behavior of the proposed MEMS variable capacitor as the *dc* bias voltage was increased from 0.0 V to 10 V in 0.5 V steps, as shown in Fig. 3.28. The new pull-in voltage was found to be between 8 V and 8.5 V, and the new simulated maximum displacement obtained was 1 μm with the added carrier beams. The achievable maximum simulated tuning range was 400%. Fig. 3.29 illustrates the deformed structure of the proposed capacitor. To simplify the structure, the attached supporting beams and the carrier beams were clipped at the contact planes, and the anchors and release holes were removed from the simulated capacitor. The figure illustrates the final collapse of the top plate when it touches the bottom plate. One can observe that the carrier beams have deflected downward as shown in Fig. 3.29; this deflection is due to the electrostatic force that keeps growing as the *dc* bias voltage is increased. The deformed structure is scaled up five times in the Z-axis for illustration purposes.

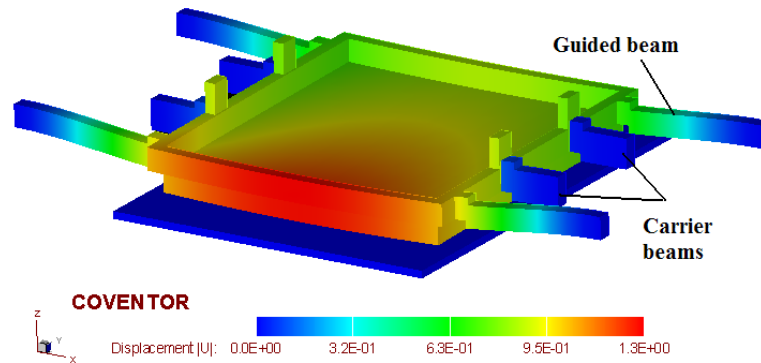


Figure 3.29 The simulated deformation in CoventorWare, exaggerated five times in the Z-axis.

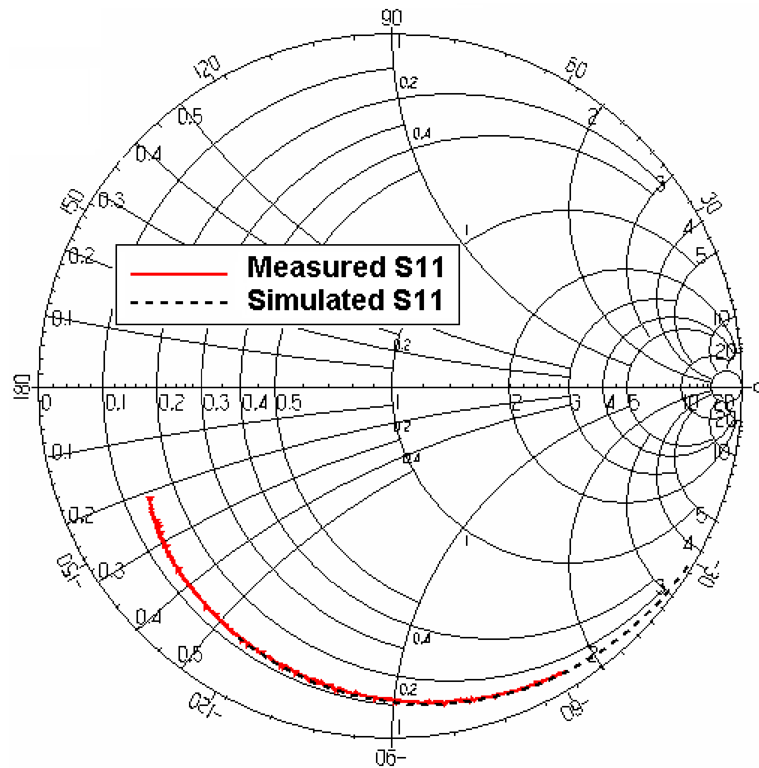


Figure 3.30 The simulated and measured return loss on a Smith chart at $V_{dc} = 0$ V.

3.3.4 HFSS Simulation and Measured Results

The variable capacitor was first built in CoventorWare and then transferred to a high-frequency structure simulator (HFSS) for RF simulation. The one-port return loss S_{11} responses of the simulated and measured data are plotted on a Smith chart over a frequency range of 1 GHz to 6 GHz. Fig. 3.30 shows the simulated and the measured S_{11} results for $V_{dc} = 0V$ when the initial deformation is not considered in HFSS (ideal case).

The difference between the theoretical and the measured results, when zero *dc* bias voltage is applied, is due to three major factors, as reported in [27]: (1) the residual stress that causes the initial deformation of the suspended top plate; (2) the parasitic capacitance that comes from the lossy silicon substrate; and (3) the parasitic capacitances that come from the RF pads and the anchors. The third factor does not contribute to the inconsistency between the simulation results and the measured results at zero *dc* bias voltage since the entire capacitor with the RF pads was simulated in HFSS.

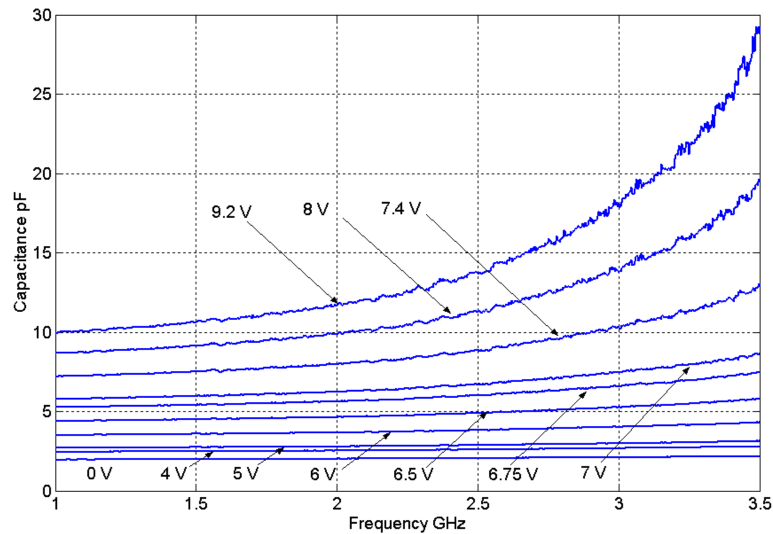


Figure 3.31 Measured capacitance versus frequency at different *dc* voltages.

A *dc* bias voltage sweep from 0 V up to 10 V was applied to the variable capacitor.

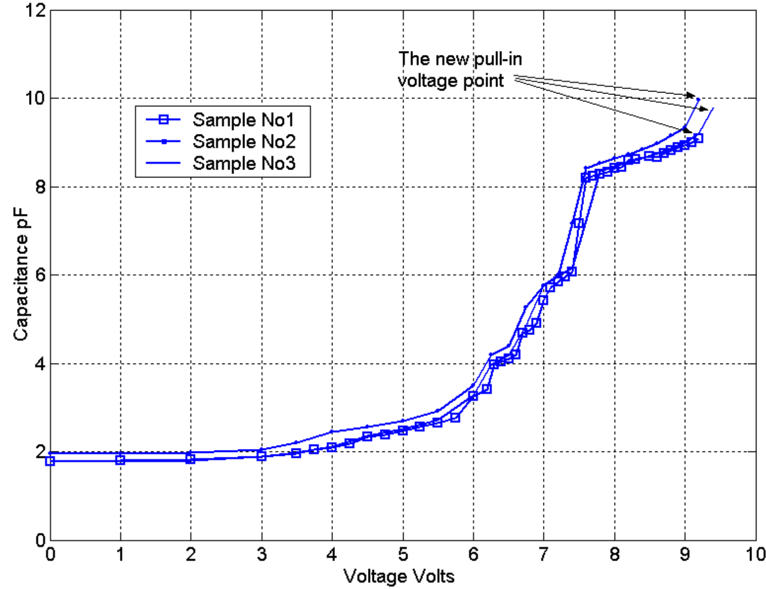


Figure 3.32 Measured tuning characteristics of the proposed capacitor at 1 GHz.

Fig. 3.31 illustrates the measured capacitance value for *dc* voltage steps over the frequency range of 1 GHz to 3.5 GHz. At 1 GHz, the achievable tuning of the proposed capacitor was found to be 410% for the first sample. The second sample has a tuning range of 450%, while the third sample has a tuning range of 410%. The measured tuning responses at 1 GHz for the three samples are plotted in Fig. 3.32. The presence of the carrier beams, which are positioned 0.75 μm below the top plate, prevented the top plate from collapsing at 0.41 μm. This extends the tuning range beyond the 50% limit of traditional parallel-plate MEMS capacitors [1].

The equivalent circuit of the proposed variable capacitor is shown in Fig. 3.33. The top plate and the bottom plate of the capacitor are represented in the equivalent circuit by C_3, R_3, and L_3. The capacitance, resistance, and inductance of the substrate are C_5, R_5, and L_5 respectively. L_1, C_6, and R_1 are the inductance, capacitance, and resistance associated with the attached supporting beams that are connected to the top plate. C_2 and R_2 are the capacitance and the resistance that come from the anchors on either side of the capacitor. L_2 and C_1 are the inductance and the capaci-

tance of the wires that form a connection between the center RF pad and the anchors of the beams. Finally, C_4 and R_4 are the capacitance and the resistance generated by the RF pads. These elements are determined by parameter extraction from the HFSS simulations at zero *dc* bias voltage in the case of a deflected structure, as will be explained later. Fig. 3.34 shows an SEM picture of the fabricated capacitor. A slight deformation is observed in the center of the top plate.

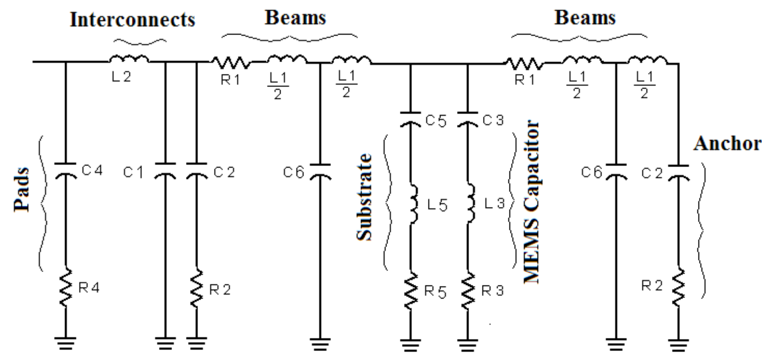


Figure 3.33 The equivalent circuit of the simulated proposed variable capacitor as a one-port network.

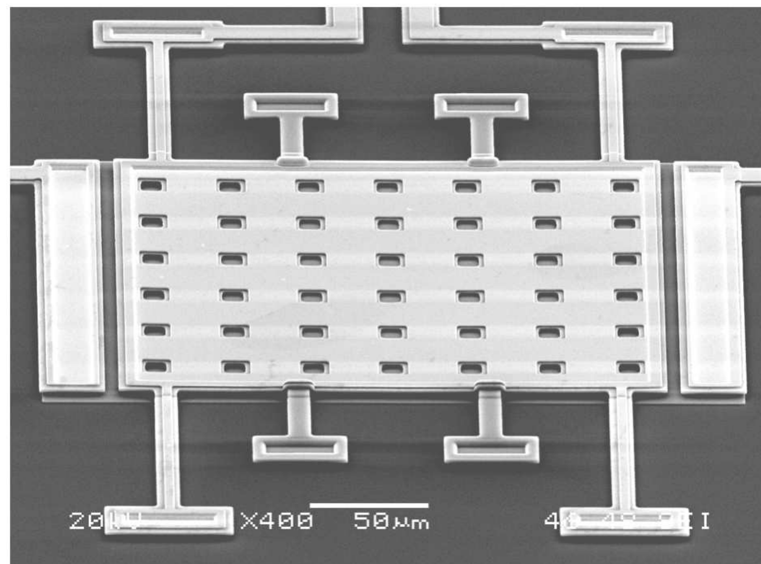


Figure 3.34 An SEM picture of the fabricated variable capacitor.

In MEMS technology, the mechanical domain plays a major role in the modeling of the RF MEMS devices because of the residual stress that causes initial deformation of the free-standing structures. This effect makes the modeling more complex because it requires additional software, not currently available, to simulate the initial deflection and to allow these structures to be exported from the finite element software such as CoventorWare and imported into HFSS.

In our technique, HFSS was used to simulate the capacitor, while the structure was manually deflected to match the measured results at zero *dc* bias voltage. Once the dominant elements were extracted using HFSS, an optimization procedure using Hewlett-Packard's HP Advanced Design System HPADS was developed to match the measured results at zero and at the remaining *dc* bias voltages. The extracted elements of the modeled capacitor yield very good agreement with the measured results, as will be shown later. Once the model is obtained, we can use it in designing circuits that integrate many of the proposed capacitors. The extracted elements of the equivalent circuit shown in Fig. 3.33 are obtained as follows:

Three deflected structures are implemented in order to match the measurements of the proposed capacitor. Fig. 3.35 illustrates the simulated capacitance of these three structures compared with the non-deflected structure. A deflection of 0.9 μm, which represents a gap of 0.35 μm, is found to be in good agreement with the measured equivalent capacitance at $dc = 0$ V. Fig. 3.36 illustrates the return loss, S_{11}, on a Smith chart for the initially deformed structure obtained in HFSS versus the measured results.

In order to extract all the parameters of the proposed capacitor, two HFSS simulations are carried out as a two-port network which can be looked at as the same circuit in Fig. 3.33 with the interconnects and pads components, C_1, L_2, C_4 and $R4$, on the right side as well. Using such simulations, the series inductance, series resistance, shunt capacitance, and shunt resistance can be obtained for the equivalent T-type circuit. In the first simulation, the silicon substrate is included, while in the second simulation, the silicon substrate is excluded. In both simulations, the attached

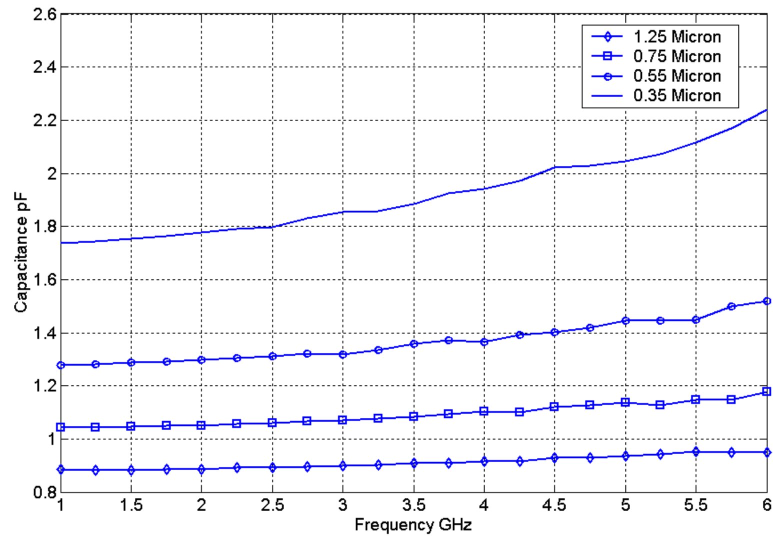


Figure 3.35 Simulated capacitance versus frequency at different gaps for the entire capacitor, including the RF pads.

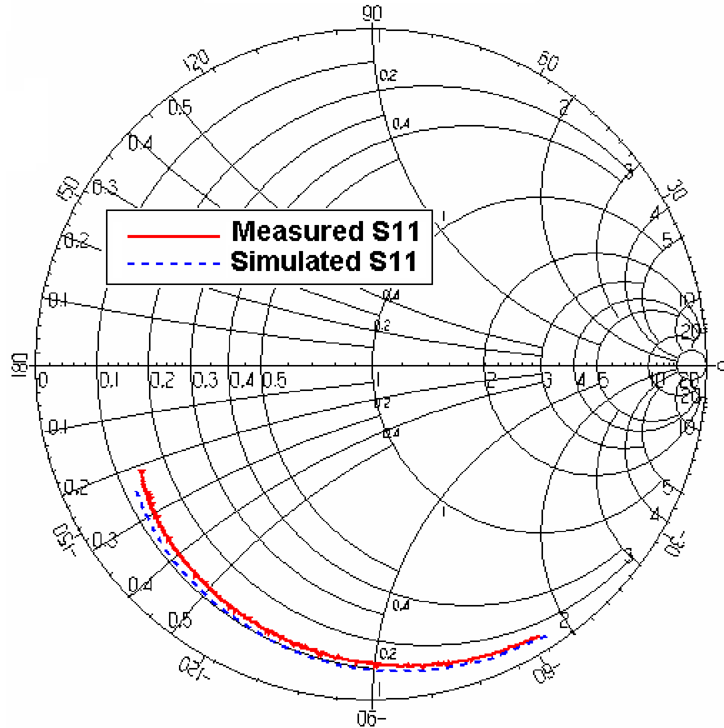


Figure 3.36 The simulated and measured return loss on a Smith chart, with the initial deformation included in HFSS.

supporting beams, anchors, and RF pads are excluded. The series components are extracted from the series impedance, Z_{11}–Z_{12}, while the shunt elements are extracted from the shunt impedance, Z_{12}, of the same T-type equivalent circuit. Fig. 3.37 shows a comparison between the capacitance calculated using CoventorWare and that in HFSS for the structure shown in Fig. 3.38. In this structure, only the two plates were simulated in both softwares. The results obtained from the simple formula $\epsilon A/d$ are also shown in Fig. 3.37. For the HFSS results, we have included simulations with and without the lossy silicon substrate. It can be noted from the HFSS simulations with and without the silicon substrate that the substrate contributes an additional capacitance of 0.04 pF at 1 GHz. The effects of the substrate on resistance are shown in Fig. 3.39 and Fig. 3.40 for the structure shown in Fig. 3.38. The extracted shunt resistance imposed by the silicon substrate is illustrated in Fig. 3.39. In this figure, the limited resistance of the doped layer at the top of the silicon substrate is responsible for the difference between the losses in the two simulations. This layer is created by heavily doping the silicon substrate with phosphorus [20]. Also, the extracted series resistance causes an increase in the equivalent resistance induced by the substrate, as shown in Fig. 3.40. The extracted capacitance between the top plate and the bottom plate from HFSS is found to be $C_3 = 1.134$ pF when the substrate is removed, as shown in Fig. 3.41.

The RF pads are simulated in HFSS. They contribute a parasitic capacitance of $C_2 = 0.23$ pF at 1 GHz, as illustrated in Fig. 3.42. The theoretical pad capacitance ($\epsilon A/x$) is found to be $C_{pad} = 0.1$ pF. The higher extracted capacitance compared to the theoretical value is due to anchoring of the pad on the nitride layer and to the fringing field, as shown in Fig. 3.43. Extracting the parasitic components of the RF pads gives us the ability to exclude these parasitic elements when the proposed capacitor is required to be integrated with other circuits.

The supporting beams are modeled from L_1 and C_6 (as shown in Fig. 3.33) by running one two-port network simulation. The extracted capacitance of the simulated beams in HFSS is found to yield $C_6 = 0.03$ pF at zero *dc* bias voltage.

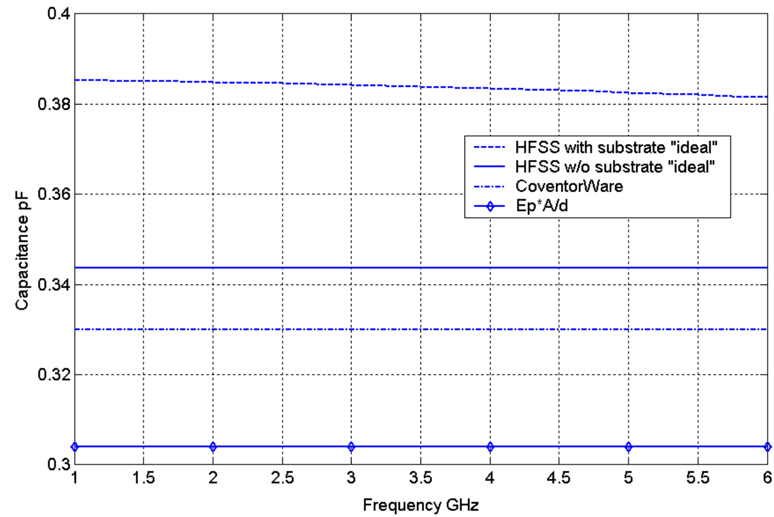


Figure 3.37 A comparison of the capacitance between the top and bottom plates as calculated using CoventorWare, $\epsilon A/d$, and HFSS with and without silicon substrate.

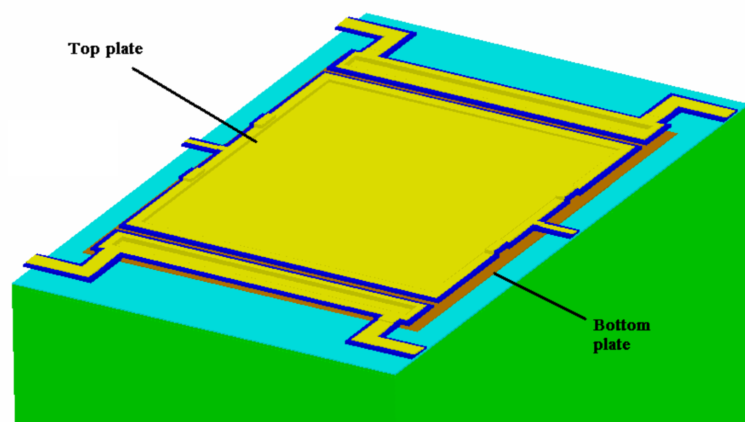


Figure 3.38 A 3D image of the simulated two plates as a two-port network in HFSS.

In order to determine the parasitic capacitance contributed by the anchors, the same method of performing two simulations as a two-port network is employed in HFSS. The silicon substrate is included in the first simulation and is excluded in the second simulation. The capacitances obtained for both cases are shown in Fig. 3.44. The extracted capacitance is then calculated and found to be $C_2 = 0.045$ pF which represents the parasitic capacitance coming from two anchors out of the four anchors as shown in Fig. 3.33.

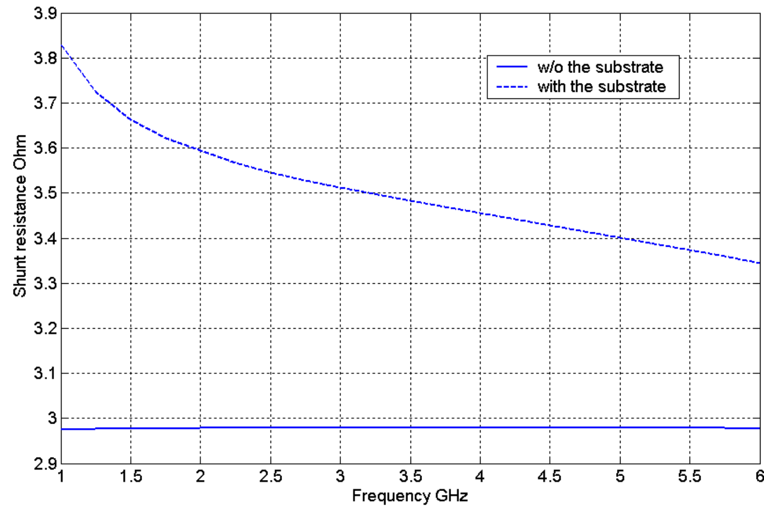


Figure 3.39 The extracted resistance from the shunt impedance of the two plates with and without silicon substrate as shown in Fig. 3.33.

HPADS optimization tools are used to extract the component values of the detailed equivalent circuit as given in Table 3.3. First, the extracted values of the equivalent circuit's elements obtained by HFSS above are used in the simulated circuit model. These elements are C_3, C_5, C_2, C_4, and C_1, corresponding to the capacitance between the two plates, the parasitic capacitance caused by the substrate, the capacitance of the anchors, the capacitance of the RF pads, and the capacitance of the interconnect between the anchors and the RF pad, respectively. Fixing the values of C_5, C_2, C_4, and C_1 and optimizing for the other elements in the circuit model achieves the optimal solution for our model. Fig. 3.45 and Fig. 3.46 show excellent agreement between the

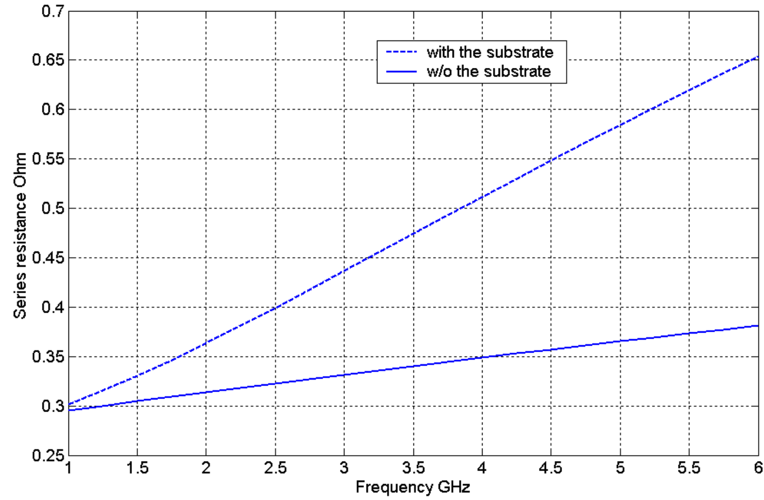


Figure 3.40 The extracted resistance from the series impedance of the two plates with and without silicon substrate as shown in Fig. 3.33.

electrical model of the proposed capacitor and the measured results for the magnitude and phase responses at $V_{dc} = 0$ V, $V_{dc} = 5.5$ V, and $V_{dc} = 9.2$ V. The first and the third *dc* bias points represent the starting and the ending points of the applied *dc* bias range. An error of less than 0.1 dB is observed between the developed model and the measured results in the magnitude response at $V_{dc} = 9.2$ V. It is worth mentioning that the key elements in obtaining the matching response from the circuit model are C_3, L_3, R_3, R_1, C_6, L_1, L_5, and R_5. These elements are associated with the moving structures, namely, the top plate and the supporting beams. It is noted that when the top plate with the attached supporting beams deforms downward, these elements are the only elements that change in the model.

The self-resonance frequency of the proposed capacitor was measured and found to be almost 11 GHz at the zero *dc* bias voltage. The self-resonance decreases to $f = 4.37$ GHz when the *dc* bias voltage equals 9.2 V. The extracted model is able to give the self-resonance frequency of the proposed capacitor, which is a product of all the capacitor's components, both wanted and parasitic. The ability to change these parameters in the circuit model is important in designing the capacitor, especially

in terms of compensating for the low actuation voltage with low self-resonance. For example, lower actuation voltage means longer attached supporting beams, which means higher parasitic inductance. Increasing the parasitic inductance of the attached supporting beams results in lower self-resonance frequency. The quality factors for the three samples were calculated from the measured data at 1 GHz. The quality factor, Q, is 14.6 for the first sample, 13.6 for the second sample, and 15.8 for the third sample.

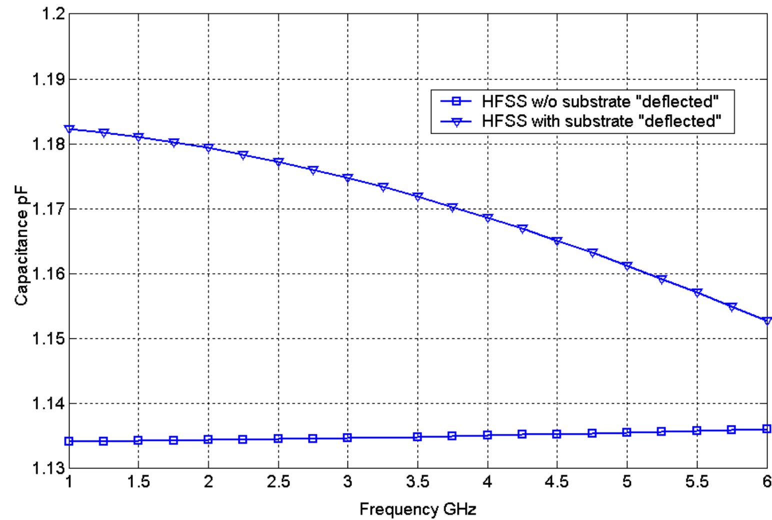


Figure 3.41 The extracted capacitance of the simulated top and bottom plates as a two-port network with the equivalent initial deformation included.

3.4 A High Tuning Range MEMS Varactor With Arrays Of Carrier Beams

Over the past three years, several techniques have been reported to increase the tuning range of parallel plate MEMS capacitors [3, 5, 27]. More recently, a parallel plate MEMS variable capacitor was proposed by the same authors in [30] employing carrier beams to hold the top plate from collapsing yielding a tuning range of 400%.

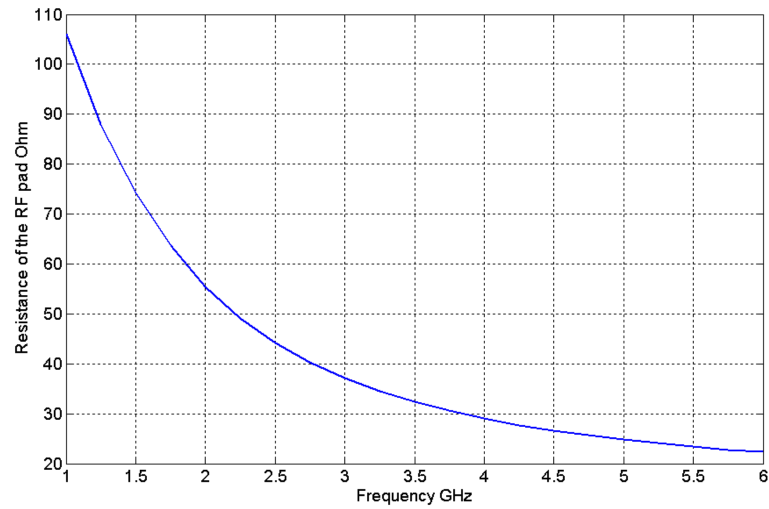


Figure 3.42 The extracted resistance of the RF pads simulated as a one-port network.

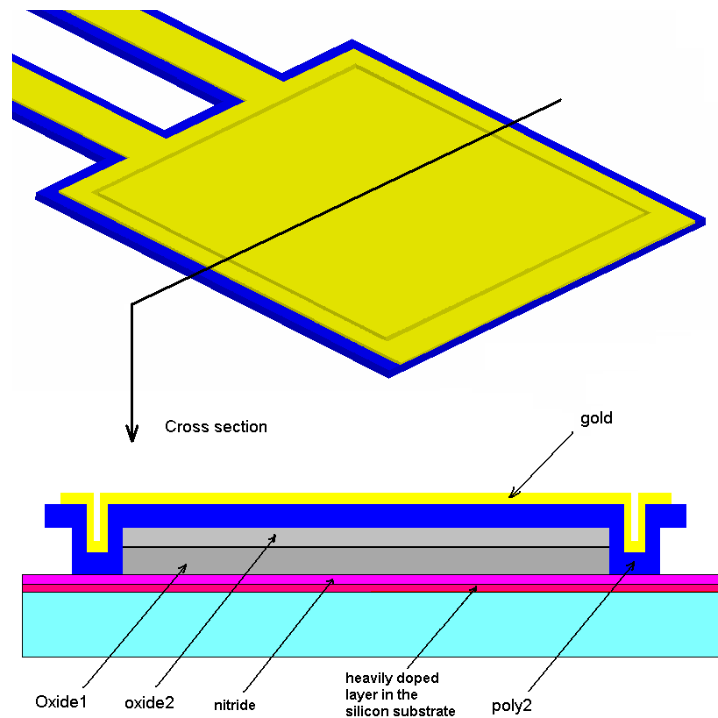


Figure 3.43 A 3D image and cross-section of the center RF pads in HFSS.

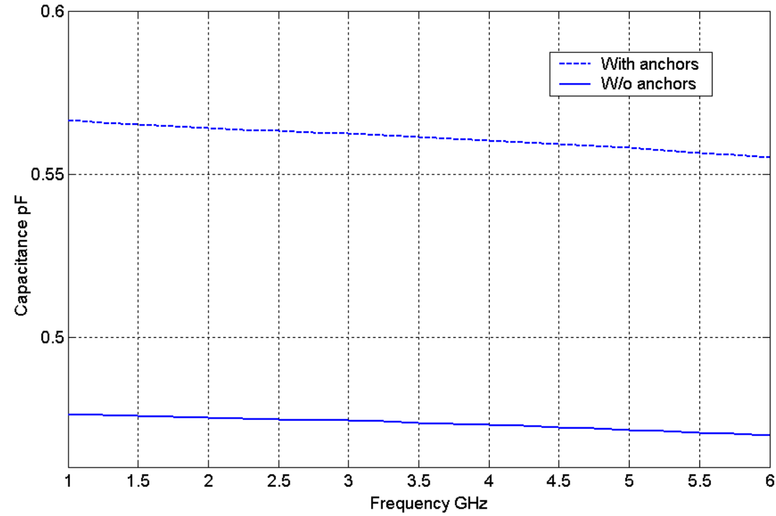


Figure 3.44 The extracted capacitance of the anchors simulated as a two-port network.

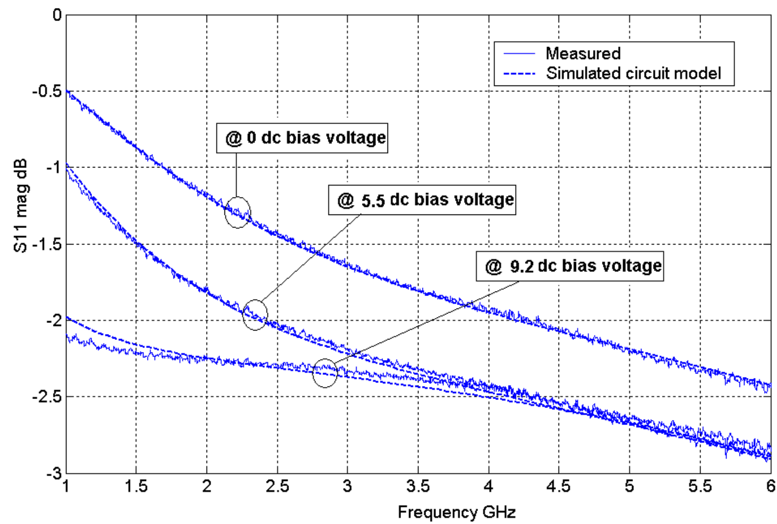


Figure 3.45 The simulated-circuit-model response versus the measured response of the magnitude for $dc = 0\ V$, $5.5\ V$, and $9.2\ V$.

Table 3.3 Values of elements in equivalent circuit of proposed capacitor extracted using HPADS optimization tools

$V_{dc} = 0V$	$V_{dc} = 5.5V$	$V_{dc} = 9.2V$
$L_1 = 0.107\,\text{nH}$	$L_1 = 0.066\,\text{nH}$	$L_1 = 0.0012\,\text{nH}$
$L_2 = 0.0047\,\text{nH}$	$L_2 = 0.0047\,\text{nH}$	$L_2 = 0.0047\,\text{nH}$
$L_3 = 0.132\,\text{nH}$	$L_3 = 0.145\,\text{nH}$	$L_3 = 0.182\,\text{nH}$
$L_5 = 0.21\,\text{nH}$	$L_5 = 0.187\,\text{nH}$	$L_5 = 0.012\,\text{nH}$
$C_1 = 0.069\,\text{pF}$	$C_1 = 0.069\,\text{pF}$	$C_1 = 0.069\,\text{pF}$
$C_2 = 0.055\,\text{pF}$	$C_2 = 0.055\,\text{pF}$	$C_2 = 0.055\,\text{pF}$
$C_3 = 1.212\,\text{pF}$	$C_3 = 2.039\,\text{pF}$	$C_3 = 8.064\,\text{pF}$
$C_4 = 0.23\,\text{pF}$	$C_4 = 0.23\,\text{pF}$	$C_4 = 0.23\,\text{pF}$
$C_5 = 0.05\,\text{pF}$	$C_5 = 0.05\,\text{pF}$	$C_5 = 0.05\,\text{pF}$
$C_6 = 0.045\,\text{pF}$	$C_6 = 0.049\,\text{pF}$	$C_6 = 0.052\,\text{pF}$
$R_1 = 0.235\,\Omega$	$R_1 = 1.433\,\Omega$	$R_1 = 2.67\,\Omega$
$R_2 = 4.84\,\Omega$	$R_2 = 4.84\,\Omega$	$R_2 = 4.84\,\Omega$
$R_3 = 11.91\,\Omega$	$R_3 = 9.24\,\Omega$	$R_3 = 4.52\,\Omega$
$R_4 = 14.78\,\Omega$	$R_4 = 14.78\,\Omega$	$R_4 = 14.78\,\Omega$
$R_5 = 28.48\,\Omega$	$R_5 = 40.5\,\Omega$	$R_5 = 59.12\,\Omega$

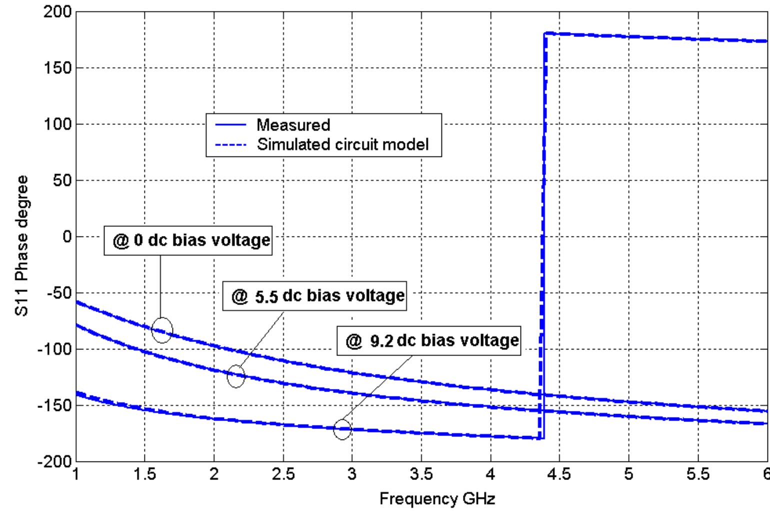


Figure 3.46 The simulated-circuit-model response versus the measured response of the phase for $V_{dc} = 0$ V, 5.5 V, and 9.2 V.

In this section we introduce a novel technique which further increases the tuning range up to 470%.

Two novel capacitors are introduced. The first proposed capacitor consists of a parallel plate capacitor with arrays of carrier beams (32 beams in total). The tips of these beams are placed under the attached beams (the four beams that are holding the capacitor) in a way to gradually add restoring forces to the total restoring force of the capacitor's spring system. The various level of restoring forces are induced as the attached beams deflect toward the array of carrier beams. The proposed capacitor has been tested demonstrating consistent measured results.

The second proposed capacitor combines the technique proposed in this section with the technique reported in [30] to further extend the tuning range of the capacitor to 470%. With a proper choice of the array configuration a higher tuning range can be potentially achieved.

3.4.1 The First Proposed MEMS Capacitor Design

Fig. 3.47 displays a schematic diagram of the proposed capacitor. The capacitor consists of two parallel-plates, one fixed plate and a second movable plate. Four arrays of carrier beams are placed under the attached beams and are supported by four anchors.

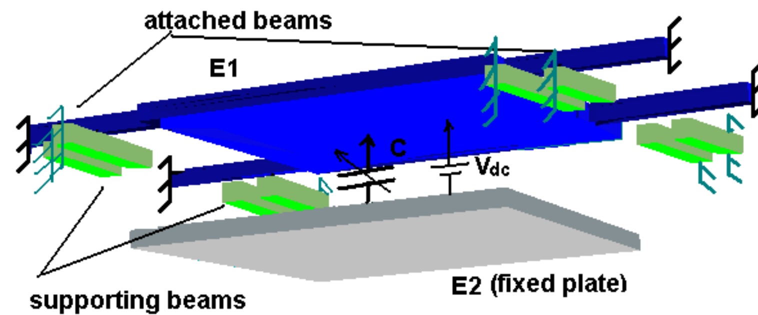


Figure 3.47 A schematic diagram of the proposed capacitor.

The capacitor is built using PolyMUMPs [32] process which consists of three structural layers and three sacrificial layers. E_2 which represents the bottom plate is constructed using poly0, the array of the carrier beams are built using the second structural layer (poly1) while the top plate with the attached supporting beams are made of the last layer (poly2) with the gold on top of it. Fig. 3.48 shows the top and cross section views of the proposed MEMS variable capacitor obtained using MEMSPro [32] software. The array of the carrier beams are built using poly1 and a gap of 1.25 μm is achieved by using poly1-poly2-via which etched away the second oxide and over etched the first oxide by 0.75 μm as well. The space between the tip of the array of carrier beams and the top plate is the thickness of the second oxide which is 0.75 μm.

3.4.2 Lumped Element Modeling of The First Proposed Capacitor For The Steady State Response

In order to understand the nature of our proposed technique, we should look at the deflection behavior of a conventional beam (cantilever). To extract the gaps between the attached deflected beam and the arrays of carrier beams we assume that the function of the deflected beam is a polynomial of a third degree as follows [31]: $W(X) = C_3X^3 + C_2X^2 + C_1X + C_o$. After applying the boundary conditions, the final formula will take the form [31]:

$$W(X) = \frac{Fa}{2EI}x^2 - \frac{Fa}{6EI}x^3 \tag{3.15}$$

where F is the applied force at the free end of the cantilever, a is the length of the cantilever, E is the young modulus, x is the distance from the anchor to the tested point, and I is the moment of inertia. An approximation is used to find the force F. The force, F, is calculated by obtaining the electrostatic force induced between the two plates and then dividing by four, which splits the force between the four attached beams.

The carrier beams consist of four arrays of beams. Each array consists of eight beams that are different in lengths and 3 μm separated from each other. The width is the same and equal to 4 μm.

Solving the previous equation for our attached beam gives a gap difference of 0.075 μm in Z-axis between the attached beam and any two sequential beams of the carrier beams. i.e. the attached beam will touch the closest beam of the array of carrier beams to the top plate first then will touch the next beam to it after a deflection of 0.075 μm more. The total restoring force K_t consists of eight carrier beams that are contacting the attached beams at different deflection positions.

Solving for the steady state response, at equilibrium, the magnitude of electrostatic force and total restoring force are equal. In order to find the equilibrium point, the two functions are plotted as illustrated in Fig. 3.49. As long as we have an intersection between the two curves, an equilibrium state is obtained and the collapse is not

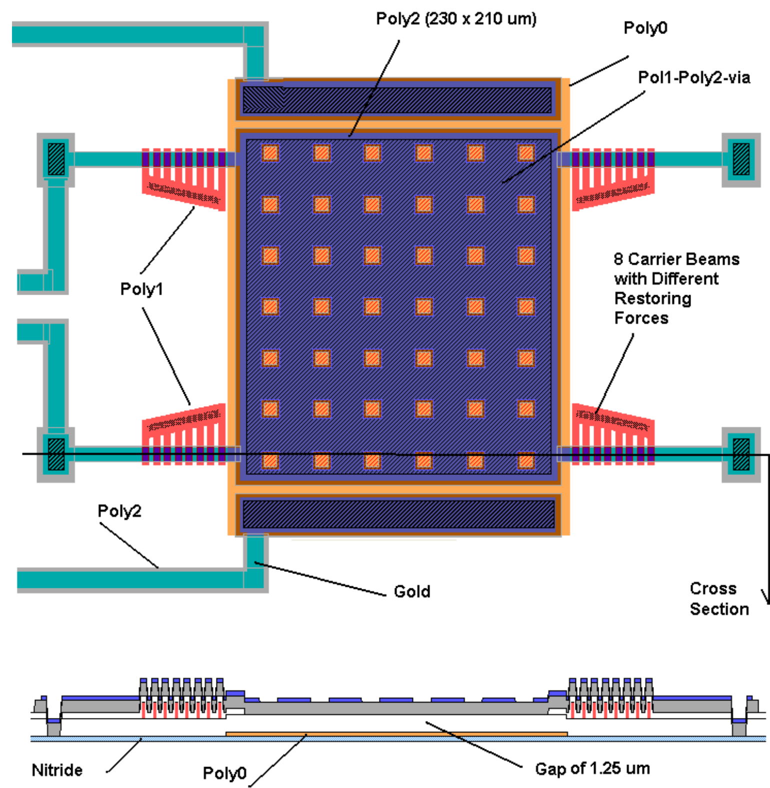


Figure 3.48 The top and cross section views of the proposed variable capacitor.

reached. The maximum displacement obtained from the lumped element modeling is 1.02 μm which gives an approximate tuning range of 440%.

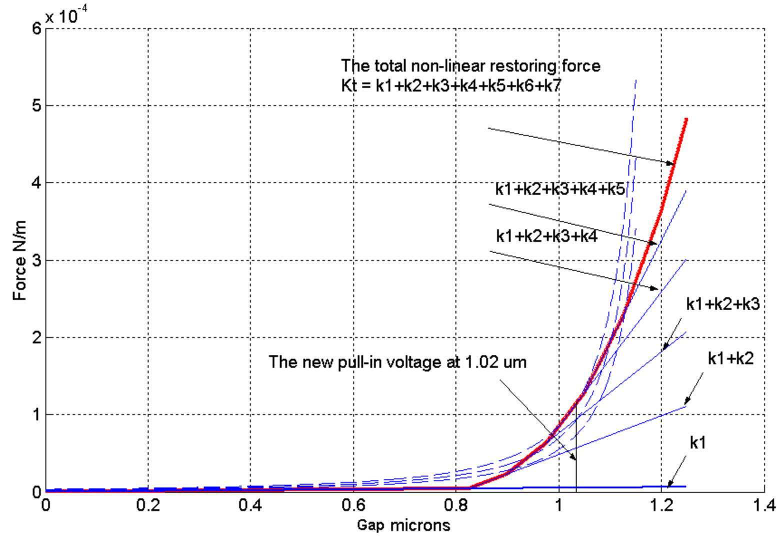


Figure 3.49 The lumped element analysis of the first proposed capacitor.

3.4.3 The Electro-Mechanical Simulation

CoventorWare [26] is used to simulate the mechanical behavior of the proposed MEMS variable capacitor as shown in Fig. 3.50. As expected, the attached beam is noticed to touch the closest beam to the top plate of the array of carrier beams then the next one to it and so on. The deformed structure is scaled up five times in the Z-axis for illustration purposes. The gap differences between the attached beam and the second and third beams of the array are 0.075 μm and 0.15 μm, respectively. Note that the attached beam is touching the first beam of the array.

3.4.4 Measured Results

The S11 response of the measured data is plotted on Smith chart over a frequency range from 1 GHz to 8 GHz. The electrostatic theoretical capacitance of the de-

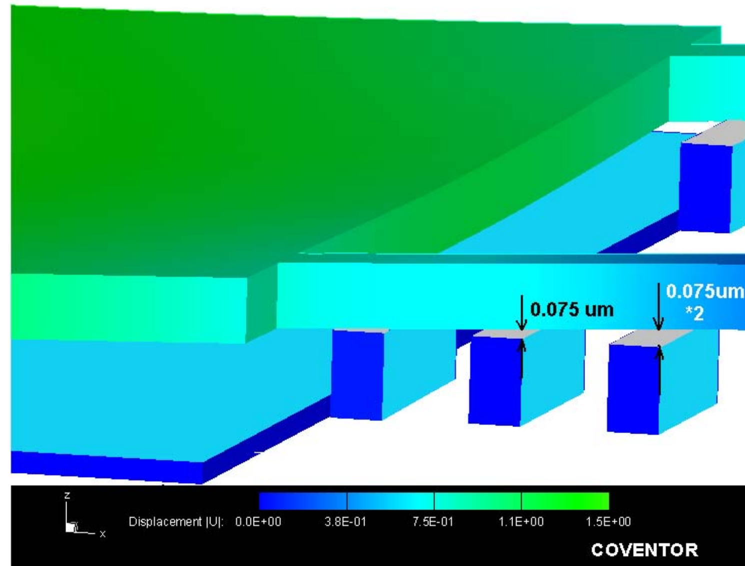


Figure 3.50 The simulated deformation in Coventorware.

signed capacitor ($\epsilon A/x$) is 0.3 pF. The measured capacitance at the same frequency is 1.83 pF. Fig. 3.51 shows the measured S_{11} for $V_{dc} = 0\ V$. The difference between the theoretical value and the measured results at $V_{dc} = 0\ V$ is due to the residual stress, and the parasitic capacitance that comes from the RF pads and the silicon substrate [27]. Fig. 3.52 shows a SEM picture of the fabricated capacitor. The capacitor is released using HF then dried using CO_2 drying process. Fig. 3.53 illustrates the array of carrier beams. The initial gap between the attached beam and the carrier beams is 0.75 μm at $V_{dc} = 0\ V$. After applying the *dc* voltage, the attached beam starts to deflect toward the carrier beams but different gaps start to appear as explained in Section 3.4.2.

A *dc* voltage sweep from 0 V to 10 V is applied to the variable capacitor. Fig. 3.54 illustrates the measured capacitance value for *dc* voltage steps over the frequency range of 1 - 4.5 GHz. At 1 GHz, the achievable tuning range of the proposed capacitor is found to be 400%. The measured tuning response at 1 GHz is plotted in Fig. 3.55.

The quality factor of the proposed capacitor from the measured data at 1 GHz is

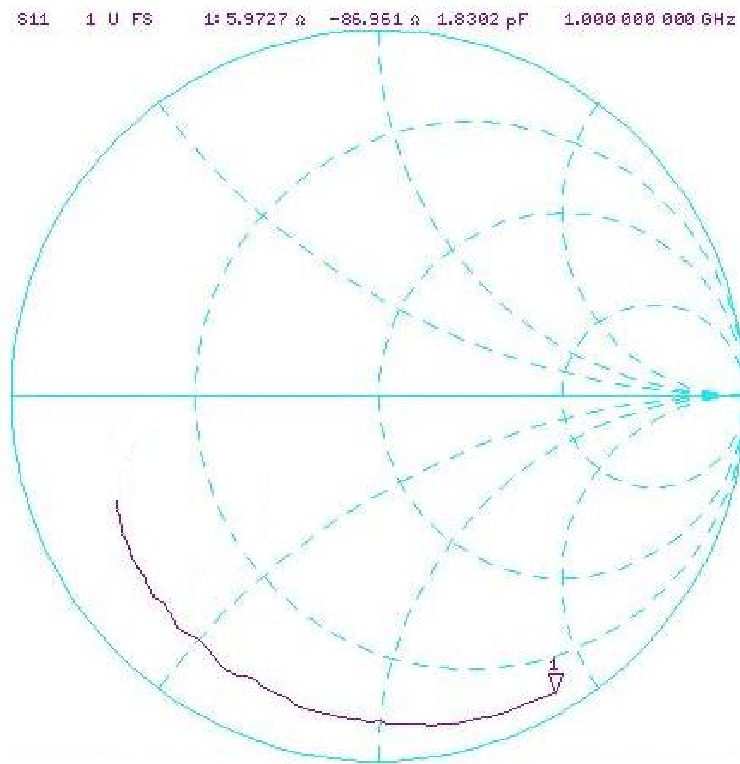


Figure 3.51 The Measured Return Loss on Smith chart at $V_{dc} = 0\ V$.

found to be 15. The capacitance is 1.48 pF, and the resistance is 5.9 Ω at the same frequency .

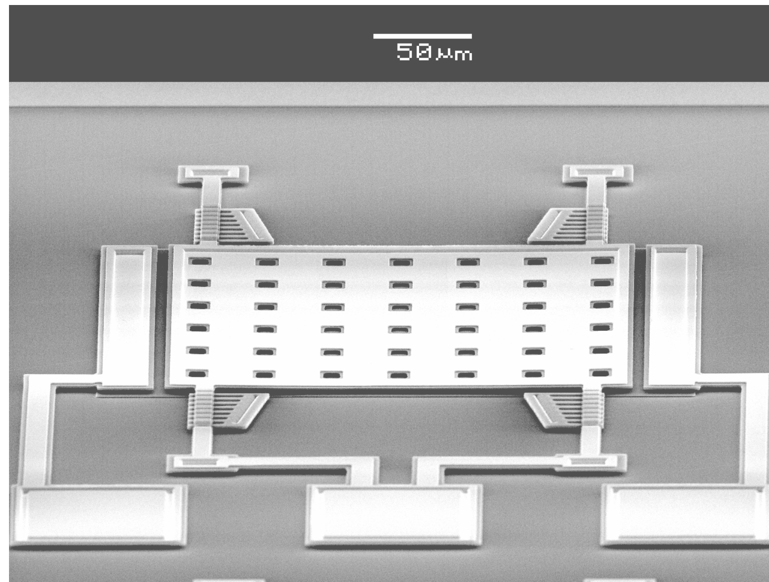


Figure 3.52 A SEM picture of the fabricated variable capacitor.

3.4.5 The Second Proposed MEMS Capacitor Design

The tuning range can be further increased by combining the arrays of carrier beams presented in the previous sections with the carrier beams used in [30]. Fig. 3.56 depicts the SEM picture of the second proposed capacitor. Two samples are measured and a tuning range of 470% is obtained for the first one and a 420% of tuning range is obtained for the second sample as illustrated in Fig. 3.57.

3.5 Summary

A two movable plate nitride loaded MEMS variable capacitor has been introduced in this chapter. In comparison with conventional parallel MEMS capacitors, the proposed capacitor exhibits three unique features, namely: the movable two plates,

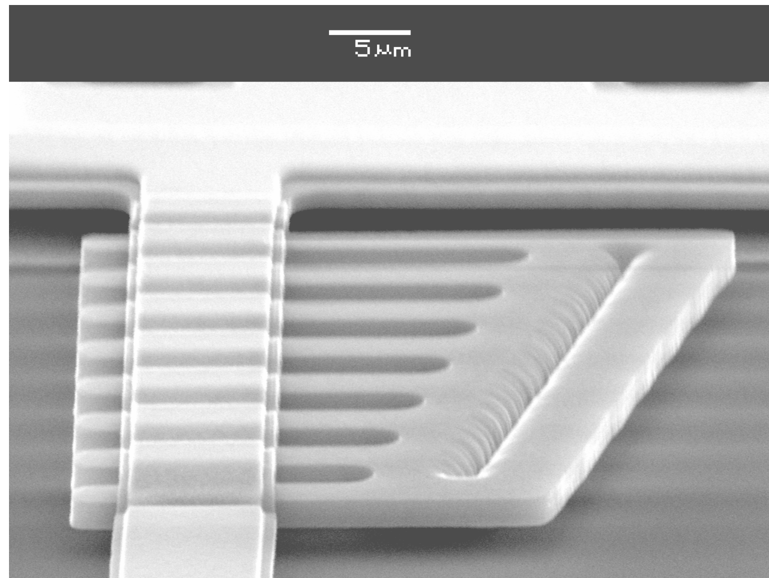


Figure 3.53 A SEM picture of the fabricated variable capacitor which shows the array of carrier beams.

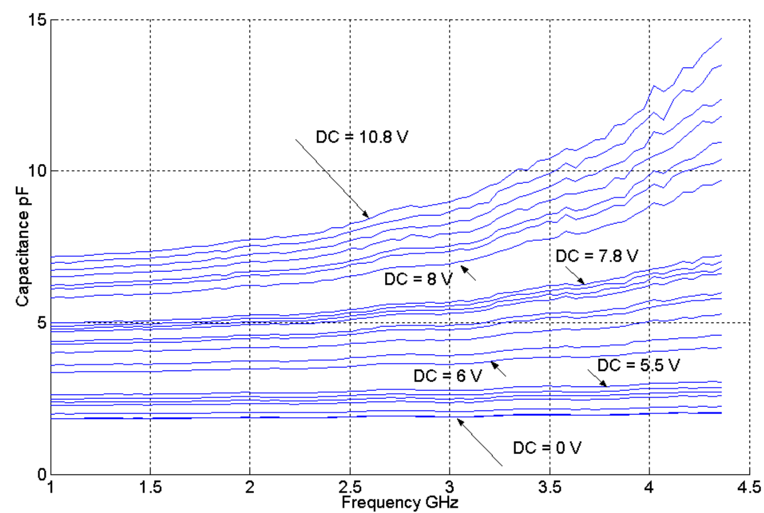


Figure 3.54 The measured capacitance vs. frequency at different *dc* voltages.

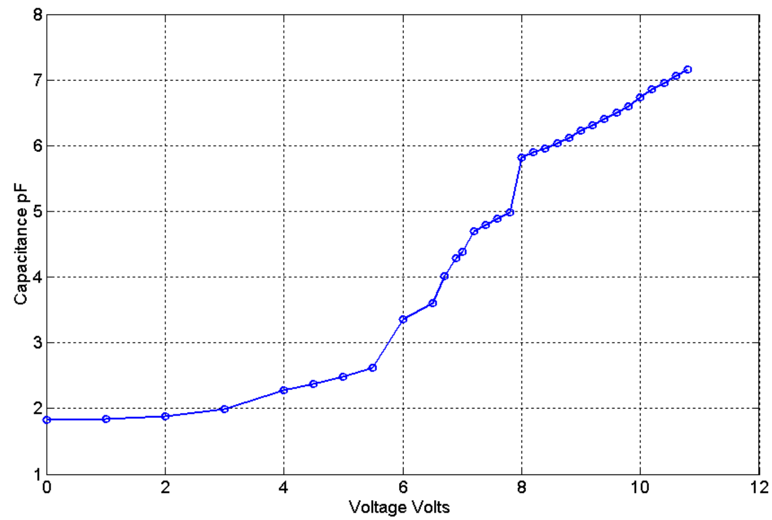


Figure 3.55 The measured tuning characteristics of the proposed capacitor shown in Fig 3.52 at 1 GHz.

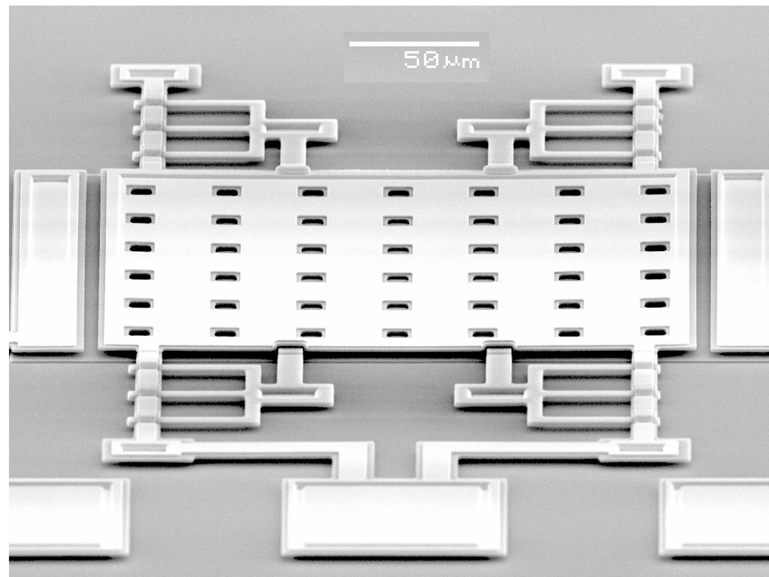


Figure 3.56 A SEM picture of the fabricated variable capacitor.

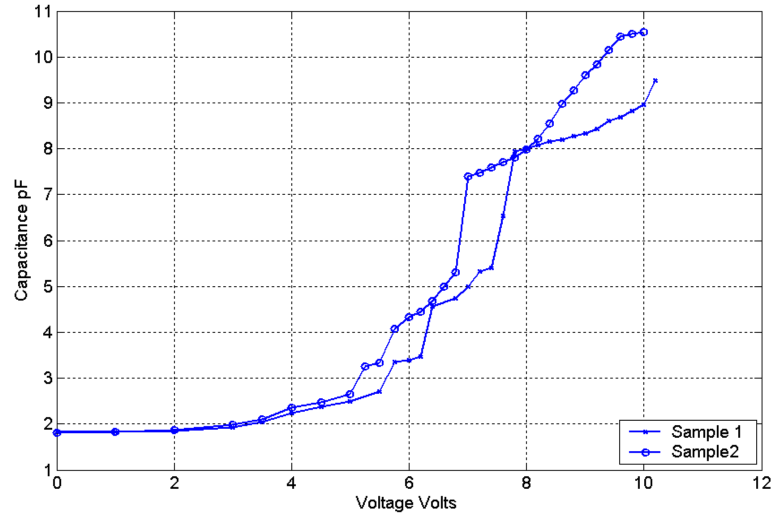


Figure 3.57 The measured tuning characteristics of the proposed capacitor shown in Fig 3.56 at 1 GHz.

the nitride layer between the two plates and the trench underneath the capacitor. Several simulations have been conducted to extract the parasitic components of the capacitor. The capacitor has been simulated as one port network, two port network, with/without RF pads and with/without the silicon trench.

Two variable capacitors having different capacitance values are fabricated and tested. The tuning range of traditional parallel plate MEMS capacitors is limited to 50%, while the measured tuning range of the proposed MEMS capacitor is found to be 250% - 280%, i.e. more than 5 times improvement in tuning range has been achieved by the proposed capacitor configuration which is fabricated through MetalMUMPs process from MEMSCAP.

The second configuration of the presented variable capacitors is built in Poly-MUMPs process from MEMSCAP with two sets of beams: attached supporting beams and carrier beams. The attached supporting beams hold the top plate at zero V_{dc} V, while the carrier beams prevent the top plate from collapsing onto the bottom plate by imposing an additional restoring force. The equivalent spring constant of the new suspension system creates a nonlinear restoring force that attempts to maintain a

solution with the induced nonlinear electrostatic force. The measured tuning range is 410%, which far exceeds the 50% tuning range of traditional parallel-plate MEMS capacitors. The lumped element model is developed, and a steady-state response is demonstrated. Consistent measured results are achieved for three capacitor samples.

The third and fourth structures of the presented capacitors in this section are built with attached beams and arrays of carrier beams. The maximum measured tuning range obtained is 470%. The capacitors are fabricated through PolyMUMPs process from MEMSCAP.

Chapter 4

Linear Parallel-Plate MEMS Varactors with High Tuning Capacitance Ratio

4.1 Introduction

Parallel-plate variable capacitors with electrostatic actuation [3,5,27,29,30,33,34] are preferable due to their high self-resonance, high quality factor, and low power consumption. However, the capacitors are prone to non-linear displacement. A second type is the interdigitated capacitors [24,35] that have a linear response, but exhibit a low self-resonance and low quality factor. In this section, two approaches are used to obtain linear capacitance response. The first one is by which the vertical comb actuation technique is combined with the conventional parallel-plate topology, is proposed. As a result, the tuning ratio is 7:1. The second approach employs the residual stress in the bi-layer thin film to create a unique curl up structures that demonstrate linear capacitance response versus the applied *dc* bias voltage.

4.2 A Parallel-Plate MEMS Varactor with Vertical Thin-Film Comb Actuators

The first proposed capacitor consists of horizontal parallel-plates facing each other. They are suspended by support beams and have the capability to vertically deform toward each other. The two plates of the proposed variable capacitor are mechanically connected to the actuator's two electrodes, yet these electrodes are electrically isolated from the capacitor's plates.

4.2.1 Proposed MEMS Capacitor Design

Fig. 4.1 is a schematic diagram of the newly developed capacitor. It consists of two parallel plates which are movable. The capacitor is fabricated by the MetalMUMPs

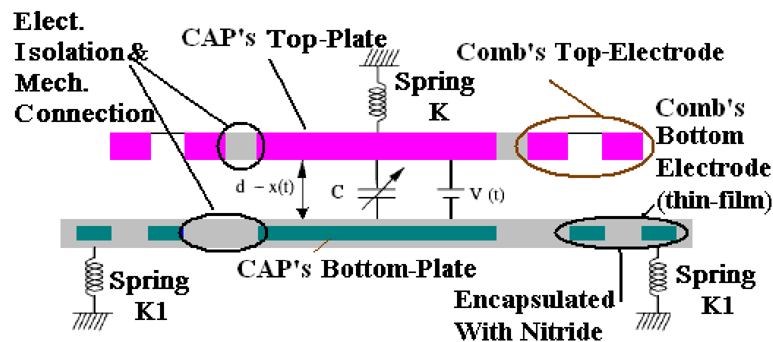


Figure 4.1 A schematic diagram of the proposed capacitor.

process [25]. It involves the use of a 26 μm nickel structural conductive layer on top of a second conductive layer that are suspended, one dielectric layer that can be suspended, and two sacrificial layers are used to trench the silicon substrate under the device. In this process, the silicon substrate is replaced with a highly resistive silicon substrate to enhance the RF performance of the fabricated devices.

In Fig. 4.1, both the capacitor's bottom plate and the actuator's bottom plate are constructed from the first conductive structural layer which is the poly layer

in Fig. 4.2. The top plate of the capacitor and the top electrode of the vertical comb actuator are fabricated from the second conductive structural layer which is the nickel, as illustrated in Fig. 4.3. Fig. 4.4 depicts the top and the cross-section views of the proposed MEMS variable capacitor at the mechanical-electrical-bonding point illustrated in MEMSPro software [32]. This bonding point has two functions. It is responsible for the mechanical connection between the top plate of the capacitor with the top electrode of the comb actuator. At the same time they are still electrically isolated. Secondly, the bonding point connects the two outer parts and the middle part of the top electrode of the comb actuator, mechanically and electrically, that are separated by the capacitor's top plate beams.

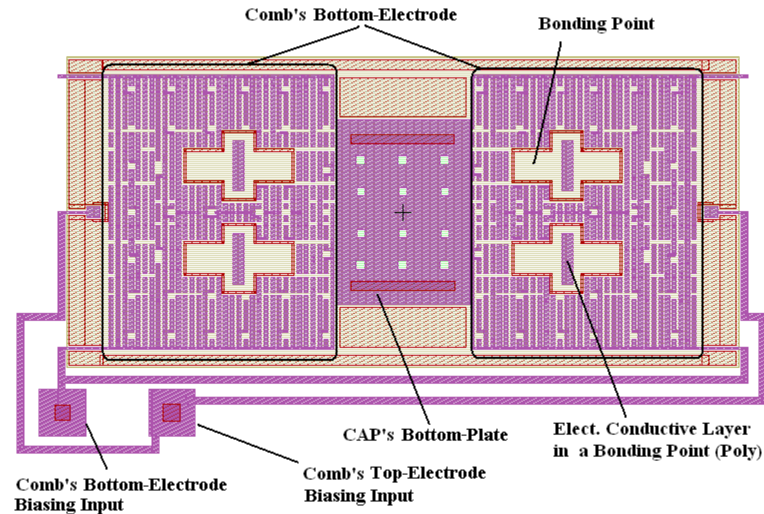


Figure 4.2 A top view of the variable capacitor showing the bottom plate of both the capacitor and the actuator, built from the poly layer.

As shown in Fig. 4.4, the bonding point consist of two layers on nitride encapsulating a strip of poly layer. This point is suspended and has four pads of nickel anchored on it. Two of these pads are part of the capacitor's top plate beams while the other two pads are from the comb's top electrode. The mechanical connection between the capacitor's top plate and the comb's top electrode is then formed. The poly layer creates an electrical connection between the comb's top electrode pads.

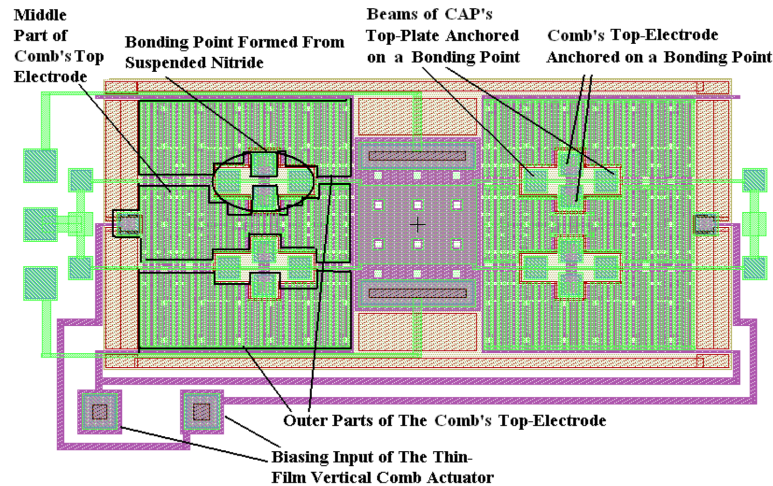


Figure 4.3 A top view of the entire variable capacitor, showing the top plate of both the capacitor and the actuator built from nickel layer.

When the actuator's electrodes attract each other, the top electrode forces the top plate of the capacitor to deform downward because of the bonding point. The bottom plate of the capacitor deforms upward, when the bottom electrode of the comb actuator moves upward. This behavior is the result of the mechanical bonding between the bottom plate of the capacitor and the bottom electrode of the comb caused by the nitride layers 1&2 which are encapsulating both and still suspended over the trench. As a result of this bonding, the bottom plate of the capacitor and the bottom electrodes of the comb actuator move as one piece.

4.2.2 The Thin Film Vertical Comb Actuator Design

Fig. 4.5 displays the layout and the cross-section of the thin-film vertical comb actuator design of the proposed capacitor. The bottom plate of the capacitor and the bottom electrodes of the comb actuator are encapsulated with the nitride layer 1 and the nitride layer 2 that are used in the MetalMUMPs process. Both layers provide the insulation that prevents the top plate of the capacitor and the top electrode of the comb actuator from contacting the bottom plate of the capacitor and the bottom

electrode of the comb actuator, respectively. These insulation layers, that are low-

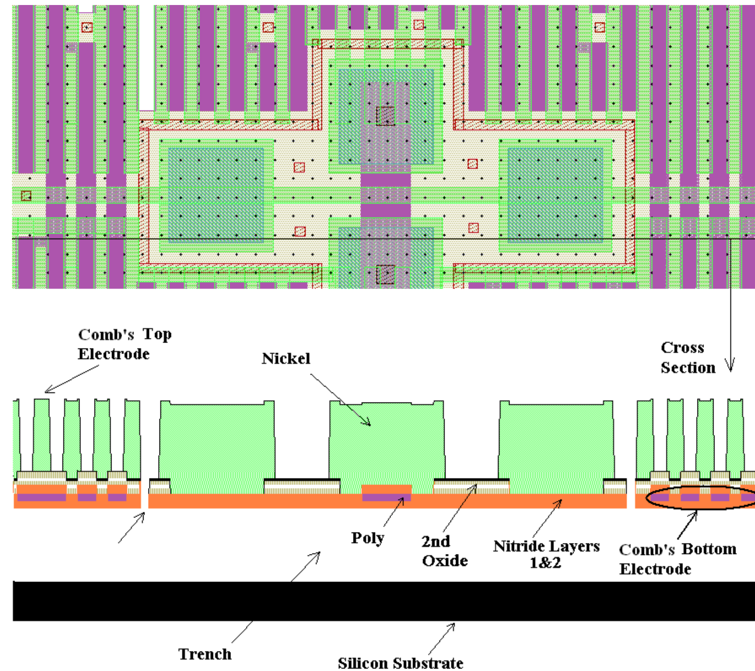


Figure 4.4 A top view and the cross-section of the mechanical-electrical-bonding point in the proposed variable capacitor.

stress silicon nitride layer 1 and nitride layer 2, have a total thickness of 0.7 μm forms the bonding point, responsible for the mechanical bonding between the top plate of the capacitor and the top electrode of the comb, and the layers that encapsulate the bottom plate of the capacitor and the bottom electrode of the comb. The thickness of the poly layer that forms the bottom plate of the capacitor and the bottom electrode of the comb actuator is 0.7 μm as well.

The capacitor's actuation mechanism depends primarily on the fringing field that is induced between the two electrodes as displayed in Fig. 4.5. This generated electrostatic force is more linear than the conventional electrostatic force, produced by the parallel-plate actuator, as the *dc* bias is increased. Moreover, this technique eliminates the pull-in behavior of the conventional parallel-plate capacitors, since the induced force from the overlap regions is smaller than the force from the fringing field.

As portrayed in Fig. 4.5, the top fingers and the bottom fingers of the proposed

thin-film vertical comb actuator do not interdigitate due to the nitride layer which covers all the bottom fingers and the gaps between them of the comb's bottom electrode. As soon as the top fingers of the comb's top electrode contact the nitride layer, the top plate of the capacitor touches the nitride layer that covers the bottom plate of the capacitor.

The maximum capacitance that can be obtained from the parallel-plate capacitance occurs when the top plate contacts the nitride layer 2 on the capacitor's bottom plate. In this case, no interdigitating behavior is required from this type of vertically displaced comb actuator since the maximum displacement is already achieved. The two actuators, one on each side of the parallel-plate capacitor, are mechanically connected to the four beams that are carrying the top plate of the capacitor. The actuators assist in pushing the capacitor's plates against each other so that a higher capacitance is achieved. The only limiting factors to obtaining a higher capacitance in this type of capacitor are the surface roughness of the nickel layer and the nitride layer 2 which is on top of the capacitor's bottom plate.

4.2.3 Measured Results

The S_{11} response of the measured data is plotted on the Smith chart over a frequency range of 1 GHz to 10 GHz. The electrostatic capacitance for the designed capacitor, computed by the simple equation ($\epsilon \cdot A/x$) is 0.462 pF. The measured capacitance at 1 GHz is 0.58 pF. Fig. 4.6 signifies the measured S_{11} for $V_{dc} = 0\ V$. The difference between the theoretical value and the measured results, where $V_{dc} = 0\ V$, is due to the parasitic capacitance, caused from the capacitive coupling between the comb's top plate and the capacitor's top plate. This coupling comes from the relatively thick nickel layer, which is normally 26 μm [25], and a small separation gap which is 8 μm between the top plate beam and the top electrode of the actuator. Also, the residual stress might have caused some deflection of either the capacitor's plates.

Fig. 4.7 and Fig. 4.8 display SEM pictures of the fabricated capacitor and the

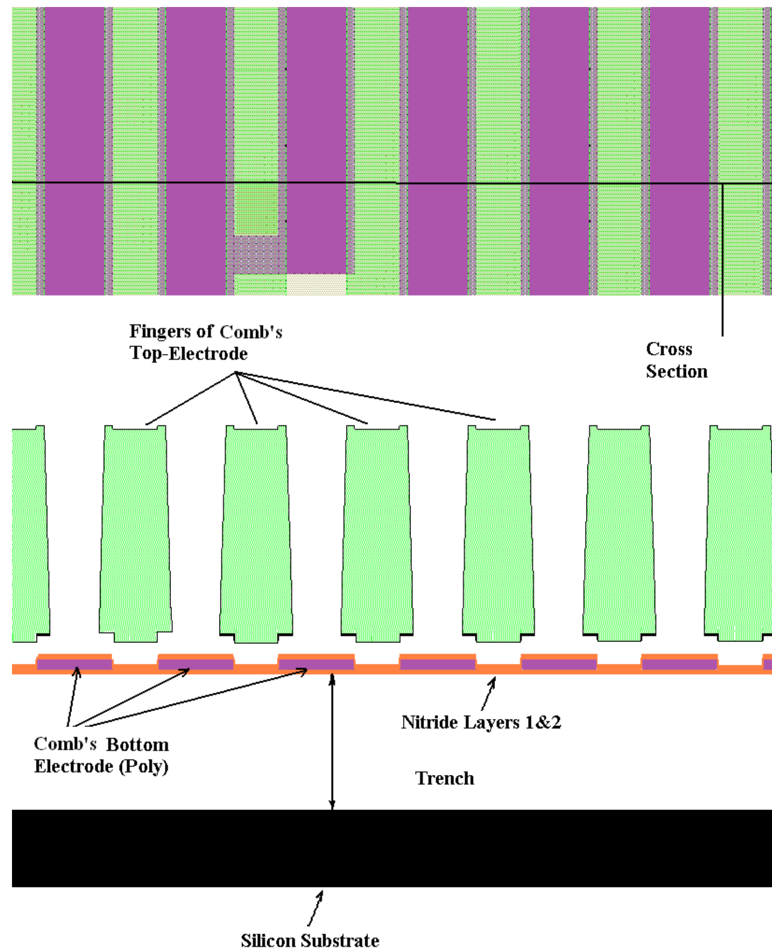


Figure 4.5 A top and a cross-section views of the proposed thin-film bottom electrode layer of the vertical comb actuator.

mechanical-electrical-bonding point, respectively. The two electrodes of the comb actuator consists of a thin tri-layer film of nitride, poly, and nitride as the bottom electrode and a thick electroplated layer of nickel as the top electrode. The initial gap between the capacitor's top plate and the nitride layer 2 is 1.1 μm. Fig. 4.9 exhibits the SEM of the top and bottom plates of the capacitor. It is obvious that both plates are suspended such that the bottom plate is supported by two beams, and the top plate is supported by four beams. The measured tuning response at 1 GHz is plotted

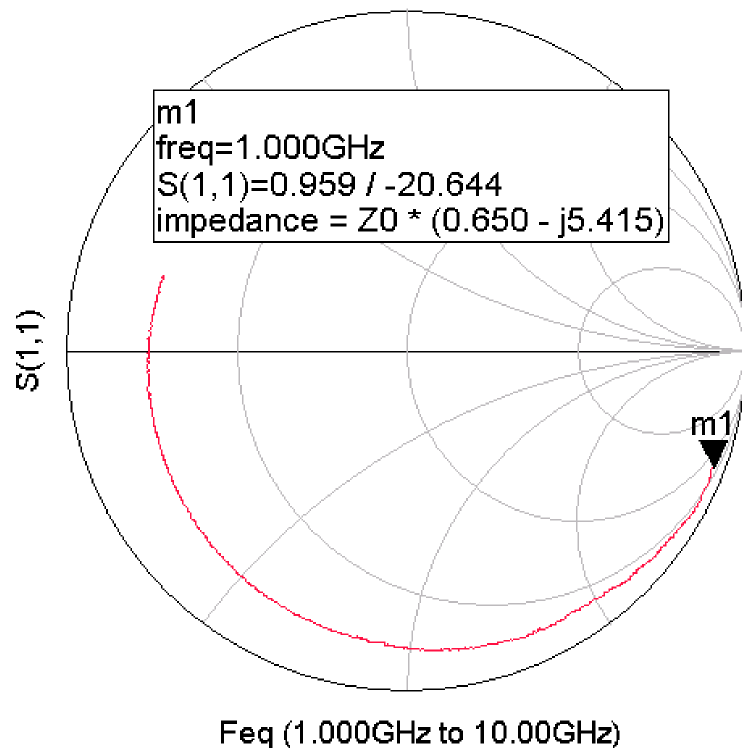


Figure 4.6 The Measured Return Loss on the Smith chart at $V_{dc} = 0\ V$.

in Fig. 4.10. The resultant tuning range of the variable capacitor is 600%.

The quality factor of the proposed capacitor from the measured data at 1 GHz is found to be 8.3, the capacitance is 0.588 pF, and the resistance is 32.5 Ω at the same frequency. The low quality factor obtained from the measurement at 1 GHz is due to the fact that the poly layer of 0.7 μm thickness, which is the first structural layer in

the MetalMUMPs process, is the bottom layer in the proposed capacitor.

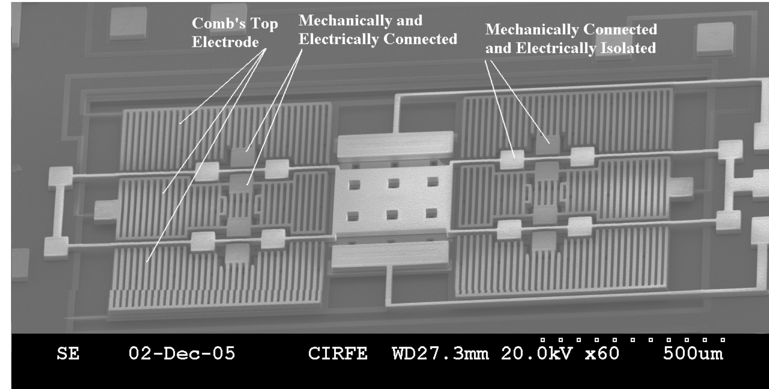


Figure 4.7 A SEM picture of the fabricated variable capacitor.

4.3 Linear Bi-Layer ALD Coated MEMS Varactor With High Tuning Range

Various MEMS varactors have been developed for RF and microwave applications. These varactors, built by different fabrication processes [8, 24, 27, 34, 36–40], exhibit high tuning ranges. The varactors, reported in [24, 27, 34, 37, 38], exhibit a non-linear C-V response, whereas, in [24, 39], interdigitated varactors with comb structures are described but they are prone to a low self resonance and relatively low quality factor. PolyMUMPs [20] is one of several commercially available fabrication processes which are used in designing MEMS devices in standard IC fabrication processes [30, 34, 38]. PolyMUMPs features three structural poly-silicon layers: poly0, poly1, and poly2, with good mechanical specs and a fourth layer of 0.5 μm gold on top of poly2. The advantage of a bi-layer with two different thermal conductivities in this case is for the residual stress to have a visible effect on the initial warpage of the top plate after the removal of the sacrificial layer.

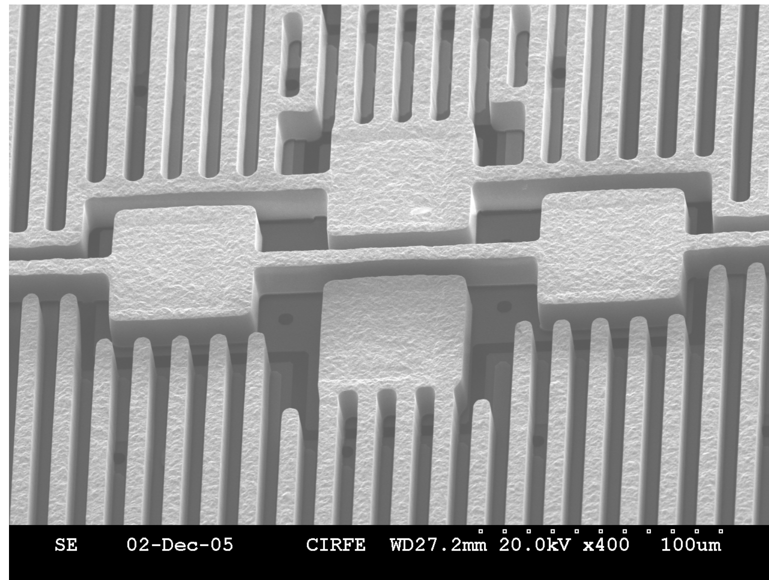


Figure 4.8 An SEM picture of the mechanical-electrical-bonding point.

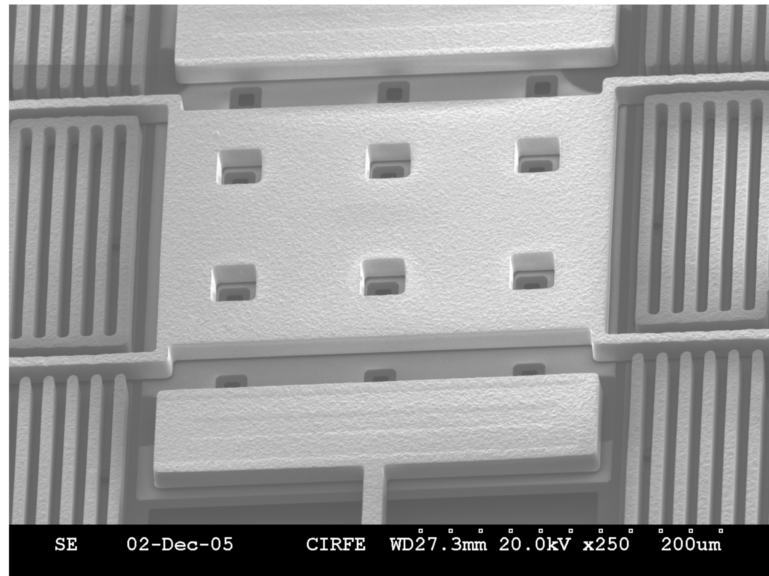


Figure 4.9 The SEM of the top and bottom plates of the capacitor.

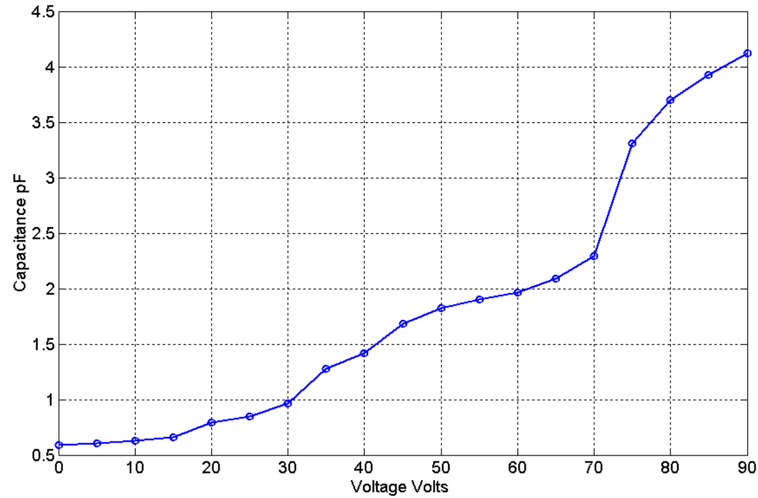


Figure 4.10 The measured tuning characteristics of the proposed capacitor in Fig. 4.7 at 1 GHz.

4.3.1 Proposed MEMS Capacitor Design

Fig. 4.11 is a schematic diagram of the proposed varactor. The capacitor, fabricated in PolyMUMPs process [20], consists of two parallel-plates connected to four guided beams with a spring constant of F_{x1}. This capacitor employs residual stress to create curled up plates. This warpage results from the residual stress's bending moment in which the top plate is deformed and relaxes on the bottom plate. The bottom plate has a relatively much higher spring constant, represented by $2F_{x2}$, than the top plate, as illustrated in Fig. 4.11. Also, the variable capacitor uses eight unanchored cantilever beams , with a spring constant of $2F_{x3}$, which introduce additional higher spring constants when the beams touch the nitride layer. The equivalent stiffness of the curled up bi-layer top plate in the proposed parallel-plate variable capacitor is a non-linear restoring force that opposes the non-linear electrostatic force. Fig. 4.12 shows the top and cross-sectional views of the proposed MEMS variable capacitor obtained by MEMSPro software [32]. As observed in these figures, the top plate is held by four guided beams which all are made of a poly2 layer with a layer of metal on top of it. The eight unanchored cantilever beams work as additional spring

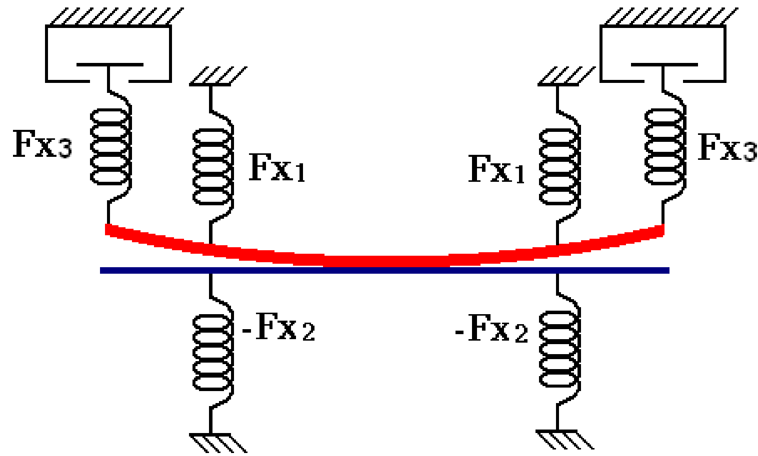


Figure 4.11 A schematic diagram of the proposed linear bi-layer capacitor.

constants that touch the nitride layer as the top plate moves downward due to the electrostatic force, applied between the two plates. These beams are made relatively stiff to prevent the top plate from collapsing on the bottom plate. They also function as stoppers, when they allow the guided beams to rotate around the beams' axials, as depicted in Fig. 4.13. To create a difference in the height between the tips of the unanchored cantilever beams and the guided beams, a time-controlled etching of the oxide layer is initiated. This is achieved by applying the poly1-poly2-via mask, fabricated in PolyMUMPs, right at the tips of the unanchored beams.

After the varactor is coated with a thin layer of alumina by the Atomic Layer Deposition (ALD) technique [6, 41, 42], the top plate touches the bottom plate in the center. This technique is useful to create an insulator layer that prevents a short circuit between the top and the bottom plates, after they come in contact. The adopted temperature for coating the capacitor with ALD is 120° Celsius and is relatively low by choice so that the temperature does not cause excessive curl up to the top plate, as reported in [41]. The top plate exhibits a smaller curvature before the ALD technique is used.

Figure 4.12 A cross-sectional view of the proposed capacitor built in MEMSPro: (a) two cross sectional views of the proposed capacitor showing the opened windows in the silicon, the different heights of the top plate and the un-anchored cantilever beams and (b) a cross section of the capacitor after the Tetramethylammonium hydroxide (TMAH) etch and the Hydrofluoric acid (HF) release.

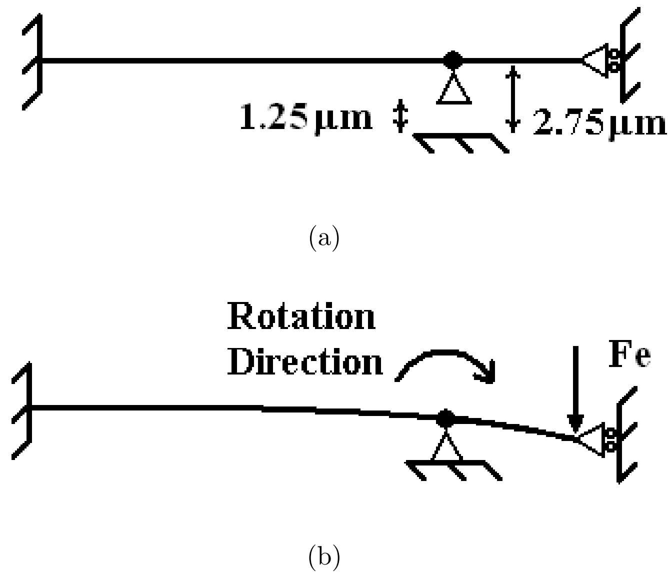


Figure 4.13 A schematic diagram of one novel guided beam in the proposed linear bi-layer capacitor: (a) the state of the proposed beam at zero *dc* bias voltage, and (b) the state of the proposed beam after the unanchored beams touch the nitride layer, when a *dc* bias voltage is applied.

4.3.2 Post-Processing

In this work, two post-processing steps are performed on the fabricated chips to improve the tuning ratio. The first step involves the wet etching of the silicon substrate to reduce the parasitic effects, including the parasitic capacitance formed between the top plate and the low resistive silicon substrate [43]. The elimination of this parasitic capacitance enhances the tuning ratio of the newly fabricated capacitor since the initial capacitance is less than the initial capacitance with the existence of the silicon substrate. This step is a maskless post-processing technique which has been specifically introduced for PolyMUMPs as investigated in [43]. The second post-processing step is called ALD and is applied to deposit a very thin layer of insulating alumina between the two parallel plates. Since there is no insulator between the top and bottom plate through the typical fabrication process, the ALD technique makes it possible to obtain a higher capacitance range, when the top plate relaxes down on the bottom plate.

1. **Maskless Wet Etch**

   The objective of wet etching is to eliminate the lossy silicon substrate that is used in standard IC fabrication processes. This allows the reduction of the parasitic coupling between the substrate and the plates of the MEMS variable capacitor due to the fringing field. This post-processing step enhances the quality factor of the MEMS variable capacitor, and, as a result, yields a better RF performance. The 0.6 μm nitride layer which is deposited on the silicon substrate, as shown in Fig. 4.12, works as a mask for the later wet etching of the silicon. The openings throughout the thin nitride film are created by overexposing the nitride layer to the oxide RIE etching through by three etching steps: anchor 1, anchor 2 and poly1-poly2-via masks in PolyMUMPs without any poly layers to cover the openings.

   The PolyMUMPs design technology allows the three aforementioned masks to

be stacked so that the silicon substrate can be exposed in order to deposit the poly2 layer on top of the substrate for grounding. However, in this work, the poly2 layer is not deposited over the silicon so that the silicon substrate can be eventually wet etched. Since poly0 does not exist under the anchor1 mask, it causes the RIE to etch away the oxide1 layer and slightly etches the nitride layer so that the oxide2 layer is deposited on top of the nitride layer. The poly1-poly2-via mask allows the RIE to etch the oxide2 layer, and further attacks the nitride layer. Finally, the anchor2 mask continues to attack the nitride layer till it disappears, and then etches some of the silicon substrate. With these aforementioned sequences of masks, it is possible to etch the oxide1, oxide2, and the nitride layer.

After the protective photoresist is removed, the entire whole chip is placed in the TMAH solution to etch the silicon substrate under the varactor, wherever there is an opening in the silicon substrate. The wet etchant is an electronic grade 5% diluted Tetramethylammonium hydroxide (TMAH). It is an anisotropic silicon etchant which etches silicon in the <100> direction and stops at (111) plane without etching the nitride layer.

To protect the poly2 layer from being etched by the wet etchant, the metal layer must cover the poly2 layer. It is observed that there is a mechanical damage and etching to the poly2 layer wherever it is not covered by the metal layer. The optimized etch parameters with the lowest damage to the poly2 structural layer are discussed in [43]. Under these conditions, the etch rate of the silicon is almost 0.5 μm/min. By choosing a higher temperature, a higher etch rate can be attained, reducing the post-processing time. However, by increasing the temperature, the higher reaction rate, the hydrogen bubbles are released faster, resulting in mechanical damage to devices with smaller feature sizes.

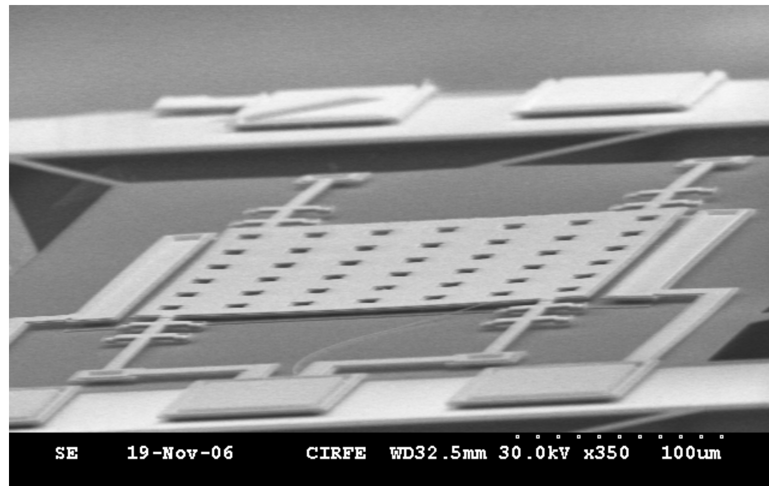
The HF release is performed after the wet etching step. The oxide1 and oxide2 layers cover the poly0 and poly1 layers protect poly0 and poly1 layers from being

attacked by the wet etchant due to the high selectivity in the TMAH between oxide and silicon. Since there is no oxide layer on the poly2 layer, the poly2 layer should be covered with the metal layer. Even though the metal does not completely cover the poly2 layer, the poly2 layer survives the attack of the wet etchant by using the optimized etch parameters. Fig. 4.14 offers SEM pictures of the capacitor after the TMAH and HF etching before applying the ALD. The top bi-layer plate of the novel MEMS varactor hangs above the bottom plate of the capacitor. When the poly2 layer is not covered by the metal layer, the poly-silicon layer almost disappears after the TMAH etching.

2. **Atomic Layer Deposition (ALD)**

An ALD technique that coats the sides of the proposed varactor with a very thin layer of 500 Angstroms alumina is used for the proposed variable capacitor. The objective of using the ALD is to obtain a high capacitance density, when the two plates come in contact with each other. This increases the capacitance between the two plates, especially with the extremely thin dielectric layers, obtained by these atomically controlled deposited layers. The only limiting factor in applying such thin ALD films is the breakdown voltage which is 1 volt/nm alumina layer in this investigation.

In order to leave a safe margin, 2 volt/nm is applied to the newly developed varactor. The samples are grown at 120° Celsius yielding about 500 Angstroms on each side of the plate. The total dielectric thickness between the two plates, after applying the ALD, is almost 100 nm. In the approach in, [6], the ALD technique is applied on the cantilever beams and flipped-chip parallel-plate variable capacitors. In our work, the ALD is used on the fully released capacitors that are built monolithically. The existence of the tensile metal layer over the compressive poly layer allows for the top plate to deform upward to facilitate the deposition of the alumina layer on the top and bottom plates during the



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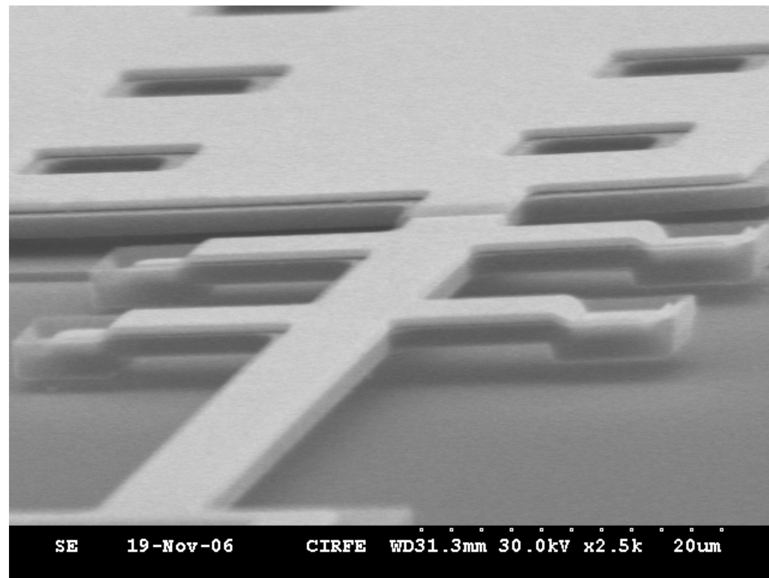


(b)

Figure 4.14 The SEM pictures of the proposed capacitor after the TMAH, HF release, and before the ALD: (a) the SEM of the full capacitor after the wet etch and (b) the unanchored cantilever beams.

application of the ALD at relatively high temperature, rather than the room temperature. As a result, the bi-layer built in this way obliges the top plate to deform laterally away from the bottom plate to avoid any contact between them, which occurred in [6], when the ALD technique is applied. In our proposed approach, the top plate can deform downward and stick to the bottom plate during the ALD approach, since the gap is relatively small with respect to the dimensions of the capacitor. This is achieved by constructing the top plate with bi-layers of the tensile stressed layer on top of the compressive stressed layer. Fig. 4.15 is an SEM picture of the capacitor after the ALD technique. It is noticeable that the top bi-layer plate is touching the bottom plate in the center of the plate due to the curvature that is greater than that of the prior ALD.

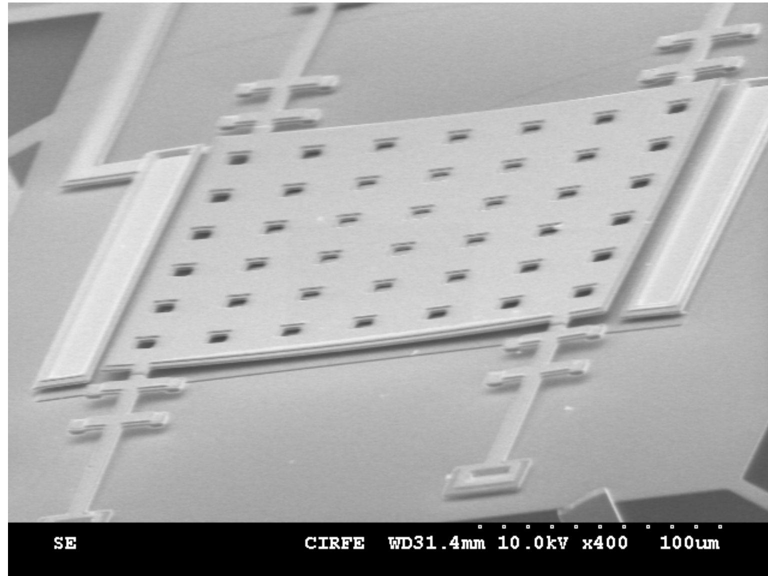


Figure 4.15 The SEM of the proposed capacitor after implementing ALD.

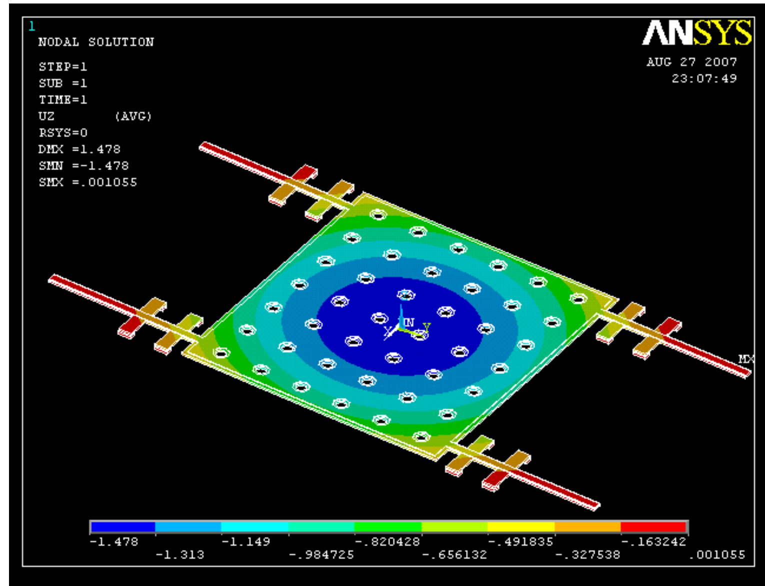
4.3.3 Simulation Results

After the mechanical behavior of the proposed varactor is simulated by the Finite Element Method (FEM) by using ANSYS and Coventorware [26], the results are compared. In addition, the High Frequency Structure Simulator (HFSS) is used to obtain the RF performance of the proposed capacitor for the initial state, when the warpage is included.

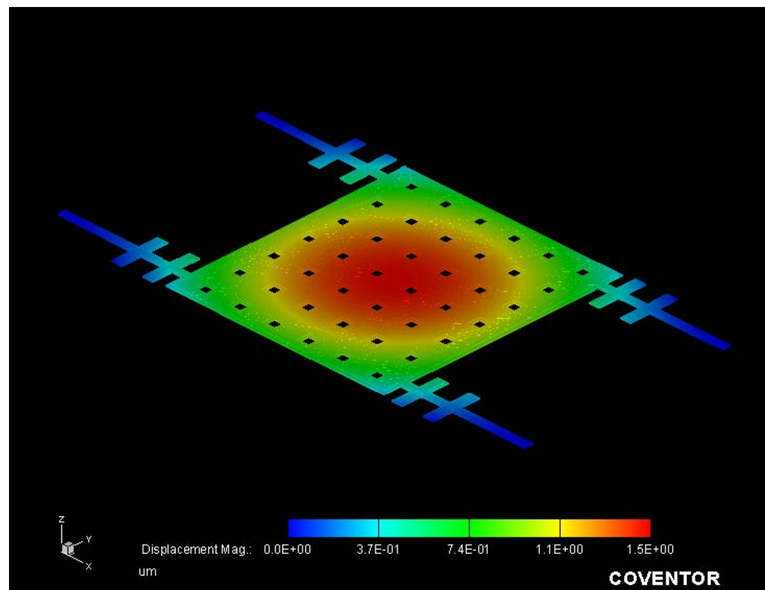
1. **Finite Element Simulations**

   The previous software is used to simulate the deformation due to the residual stress for the proposed capacitor at room temperature at zero *dc* bias voltage. The stress data, provided by MEMSCAP for the PolyMUMPs are 7.6C MPa for the poly2 and 23.7T MPa for the metal layer.

   Fig. 4.16 denotes the 3-D results of the deformed structures in ANSYS and CoventorWare. The maximum deformation in ANSYS is 1.48 μm, whereas the maximum deformation in CoventorWare is 1.5 μm after the wet etch and before the ALD is applied. The results of the curl up obtained in ANSYS and CoventorWare, due to the initial stress after the release of the proposed capacitor, are in good agreement. Before applying the ALD technique on the novel varactor, the varactor is simulated in ANSYS to obtain the proper temperature for the ALD deposition to ensure there is enough deflection away from the bottom plate at the temperature in the ALD chamber. 120° Celsius degrees is found to be sufficient and meets the minimum acceptable temperature for the ALD to be successful. Fig. 4.17 depicts the 3-D result, obtained from ANSYS, of the top plate deflection due to the temperature of 120° Celsius degree that is used in the ALD step. As expected, the top plate deflects upward and away from the bottom plate, and the alumina coated layer is successfully uniformly deposited on the capacitor. The maximum displacement achieved by the deflected top plate is 6.8 μm. After the ALD, the device is cooled down to room tempera-



(a)



(b)

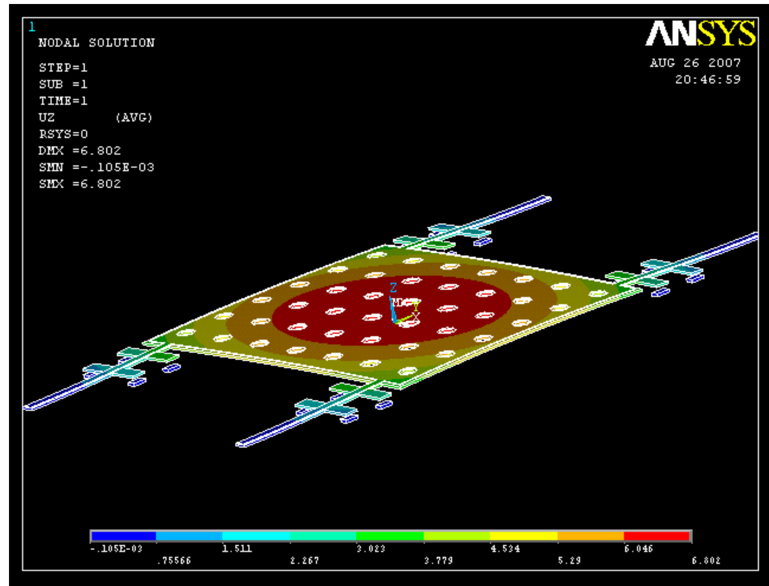
Figure 4.16 The 3-D results of the FEM simulations. (a) using ANSYS, (b) using Coventorware.

ture. The capacitor is found to exhibit a greater curvature, and the center of the top plate touches the bottom plate.

The *dc* bias voltage is then swept from 0 V to 60 V in 2 V steps by ANSYS. To reduce the time required for these simulations, including the residual stress and the release holes, two symmetries are applied on the simulated capacitor which means that only a quarter of the capacitor is required to simulate the displacement versus the *dc* bias voltage. Fig. 4.18 illustrates the 3-D results from ANSYS. The varactor exhibits the relaxation of the top plate on the bottom plate after the initial curl up of the top plate. The relaxation behavior occurs when the *dc* bias voltage is increased, leading to the increase in the equivalent restoring force by increasing the touching area. This allows a non-linear restoring force for the top plate that opposes the non-linear electrostatic force, induced by the *dc* bias voltage applied between both plates. This behavior results in almost a linear increase in the capacitance, until the curvature of the plate becomes relatively straight and then, a pull-in can occur. To prevent the pull-in, unanchored cantilever beams are used to stop the top plate. These beams come in touch with the nitride layer and introduce restoring forces that oppose the increasing electrostatic force. The higher the *dc* bias voltage, the more relaxation the top plate undergoes. The advantage of having these beams unconstrained at their tips allows the the guided beams to easily rotate around the unanchored cantilever beams' long axis. This allows the top plate to continue to relax on the bottom plate without a pull-in.

2. **HFSS Simulations**

The simulated deformed capacitor is then transferred to the HFSS to simulate the RF response. Fig. 4.19 portrays the 3-D structure of the capacitor in HFSS, including the suspended nitride layer and the trench in the silicon substrate. The simulated capacitance, extracted from the s-parameters, are compared with



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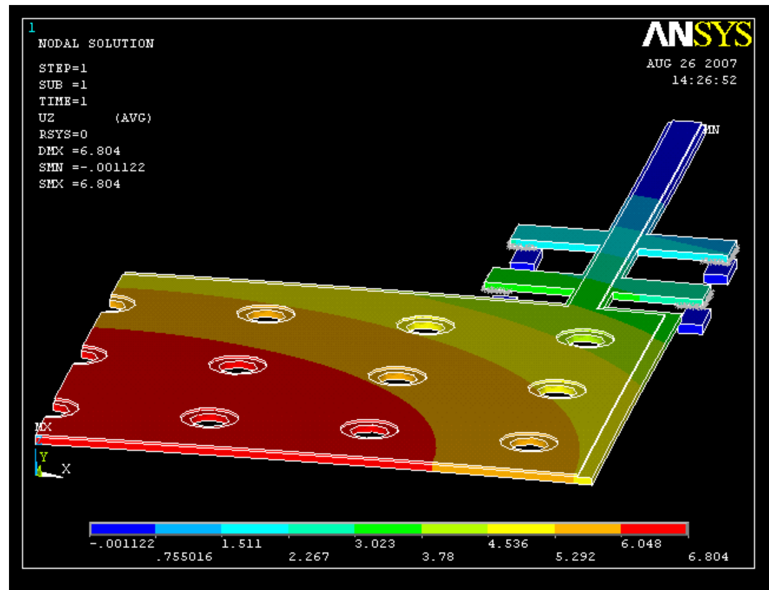


(b)

Figure 4.17 The simulated displacement results of the 3-D structure of the proposed linear Bi-layer capacitor obtained in ANSYS for high temperature: (a) the entire capacitor before the ALD deposition and (b) a quarter of the capacitor before the ALD deposition after applying symmetry.

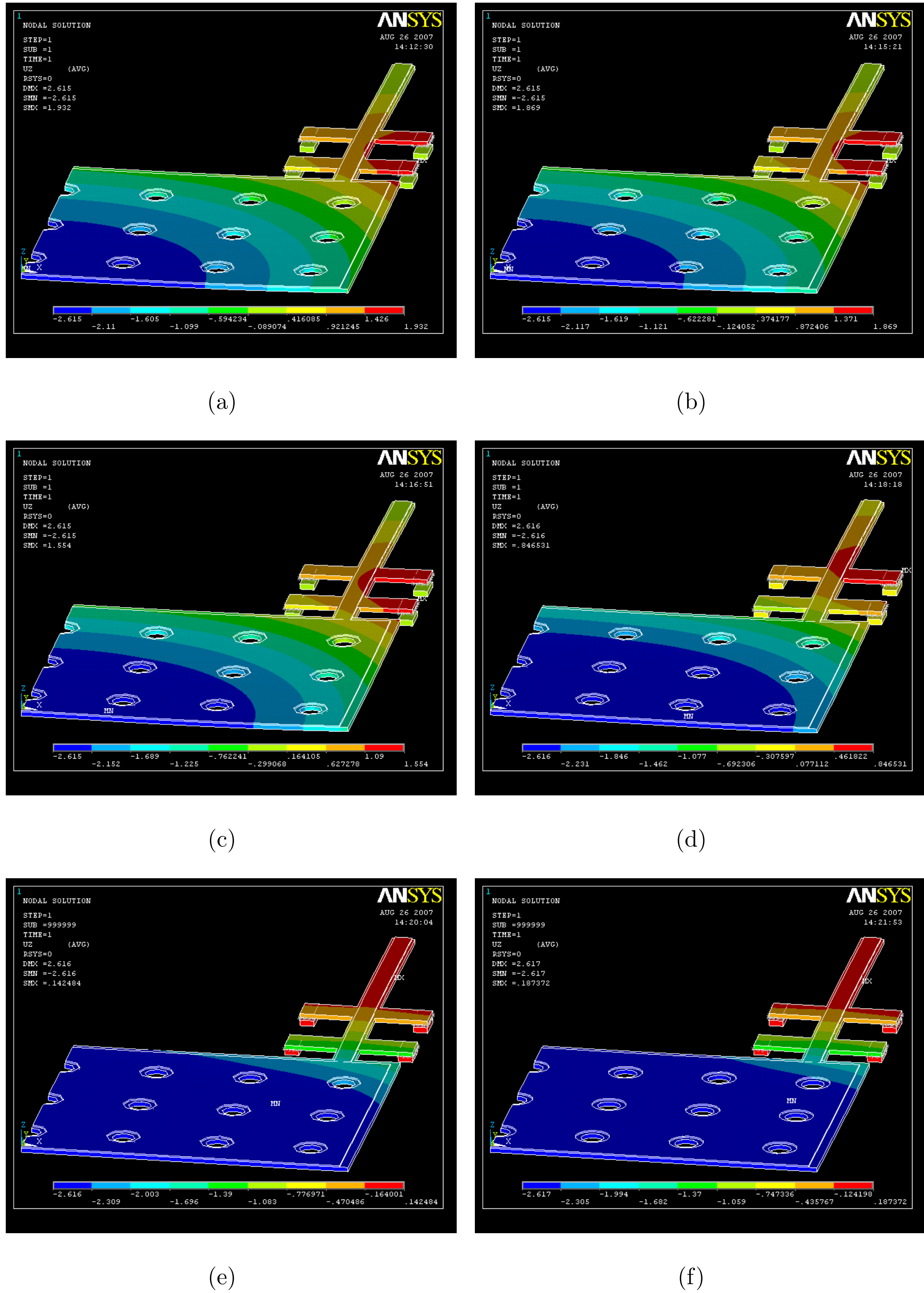


Figure 4.18 The simulated displacement results of the 3-D structure of the proposed linear bi-layer capacitor obtained in ANSYS after depositing 50 nm of ALD, showing the six positions of the capacitance: (a) at 0 V, (b) at 10 V, (c) at 20 V, (d) at 30 V, (e) at 40 volts, and (f) at 50 V.

the measured extracted capacitance in Fig. 4.20. It is evident that the simulated and measured capacitance results are in good agreement up to 4 GHz with a maximum error of 17% at 10 GHz. Surface optical profilometer test is carried out investigate this discrepancy.

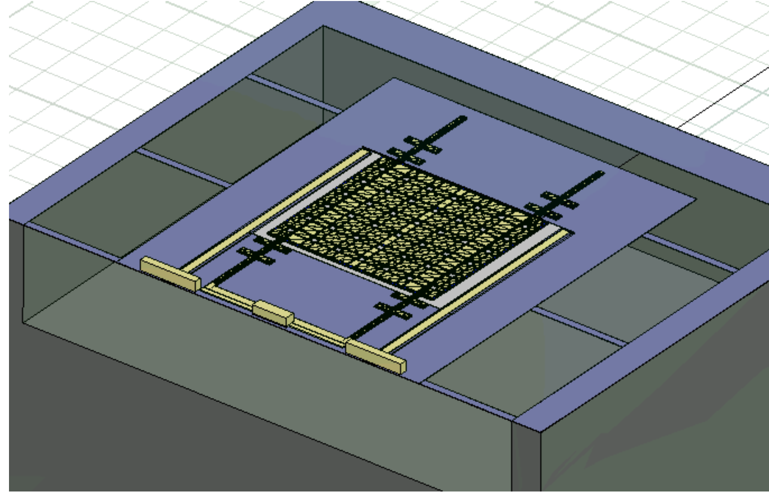


Figure 4.19 The 3-D structure of the proposed MEMS varactor in HFSS.

4.3.4 Measured Results

A surface optical profilometer is used to obtain the 2-D cross sections of the capacitors by measuring the length and width, as depicted in Fig. 4.21. The capacitor exhibits a maximum curl up of 3 μm in the y-profile and 2 μm in its x-profile. This curl is a result of the ALD and the residual stress due to the difference in the thermal expansion coefficients of the metal and poly2 that construct the top plate of the capacitor. The 3-D structure that is obtained from the surface profilometer is illustrated in Fig. 4.22 as well. ANSYS is used to simulate the curvature of the proposed capacitor by using the fit-to-measurement approach. The maximum curl up obtained for the y-profile is found to be 3.08 μm, and the maximum curl up for the x-profile is 1.36 μm. The discrepancies between the measured and the simulated capacitances in Fig. 4.20 exist because of the non-symmetrical warpage that is observed in the x-profile of the

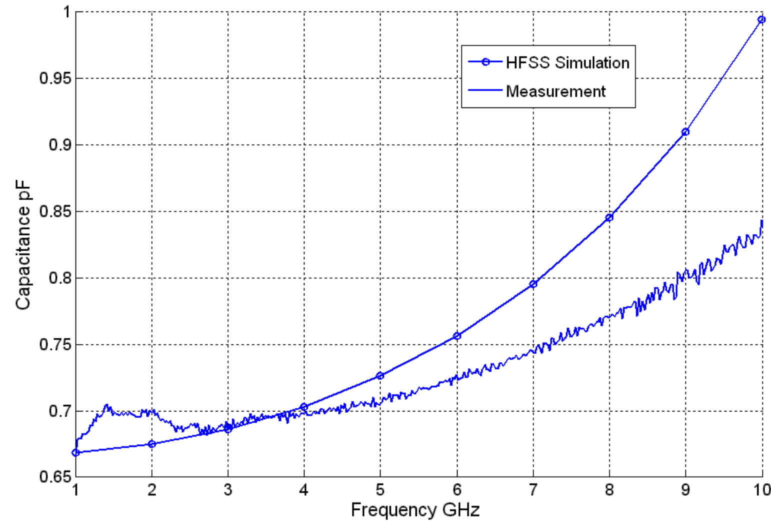


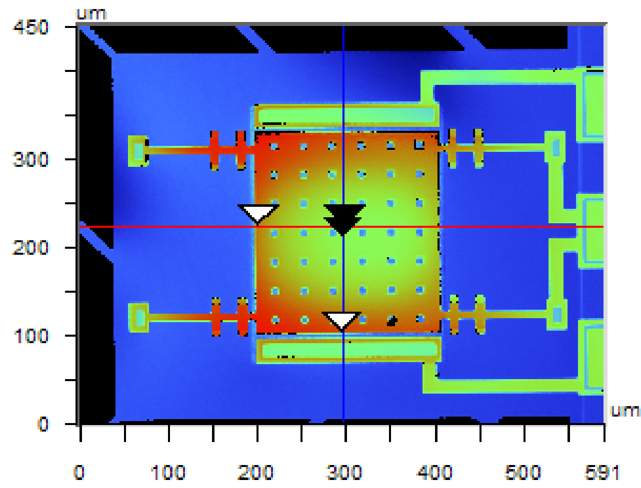
Figure 4.20 Simulation versus measurement of the proposed MEMS varactor.

proposed capacitor in Fig. 4.21.

The extracted measured capacitances versus the applied *dc* bias voltages at 1 GHz is shown in Fig. 4.23. The capacitor exhibits a linear capacitance response due to the bending moment caused by the residual stress and the ability to relax the top plate on the bottom plate without any pull-in due to the unanchored cantilever beams.

4.4 Summary

The first half of this chapter introduces a MEMS capacitor that exhibits three main features: it combines the thin tri-layer film vertical comb actuator with a conventional parallel-plate variable capacitor, the top and the bottom electrodes of the comb actuators are suspended and capable of deforming toward each other as *dc* bias voltage is increased and the comb's electrodes are electrically isolated from the capacitor's plates. The proposed capacitor is built in the MetalMUMPs process by employing two structural layers and one sacrificial layer with a trench under the proposed capacitor. The achieved measured tuning range is 7:1. The authors are working toward opti-



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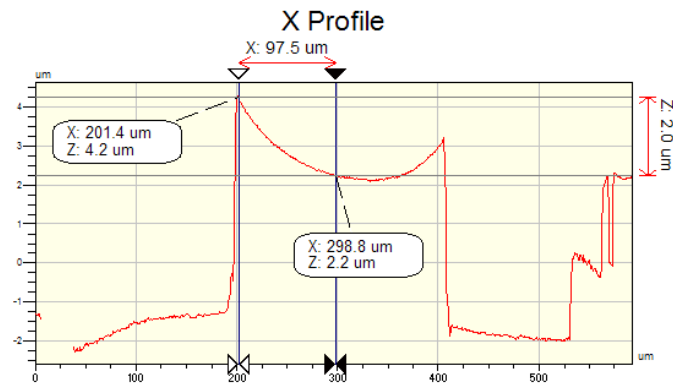

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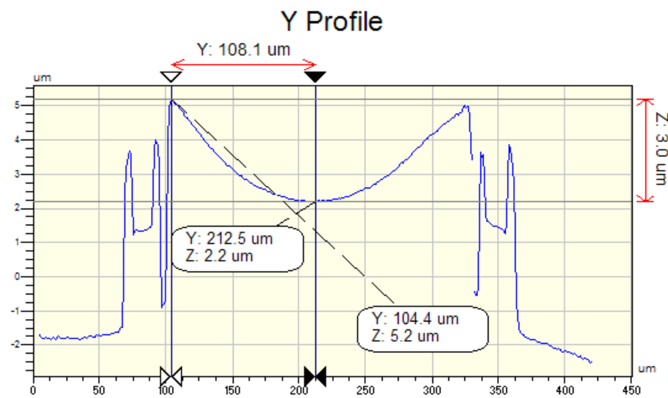


(c)

Figure 4.21 The measured profile of the curl up in the capacitor: (a) The top view of the capacitor, (b) the 2-D x-profile of the capacitor, and (c) the 2-D y-profile of the capacitor.

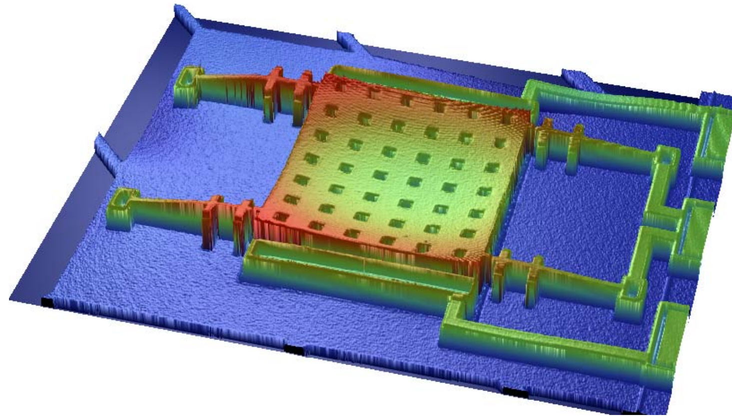


Figure 4.22 A 3-D view of the proposed capacitor obtained in the Surface Optical Profilometer (Veeco).

mizing the mechanical design to allow the capacitor to operate under lower actuation voltages.

A MEMS varactor with linear high tuning ratio, is introduced in the second half of this chapter. This capacitor takes advantage of the residual stress in a bi-layer of gold and poly-silicon. The residual stress that causes the curl up to the bi-layer top plate helps the top plate to relax on the bottom plate, resulting in a linear capacitance response. The spring constant of the unanchored cantilever beams prevents the top plate of the capacitor from collapsing on the bottom plate. The removal of the silicon substrate during the first post-processing step results in lowering the parasitic capacitance and achieving a lower minimum capacitance at zero *dc* bias voltage. Finally, the thin dielectric layer, obtained by the ALD technique in the second step of the post-processing, increases the maximum capacitance at the highest applied actuation voltage, and prevents a short circuit between the top and the bottom plates. All the techniques are utilized to obtain a considerably linear capacitance response with a high tuning ratio for the proposed MEMS variable capacitor that is fabricated in PolyMUMPs technology.

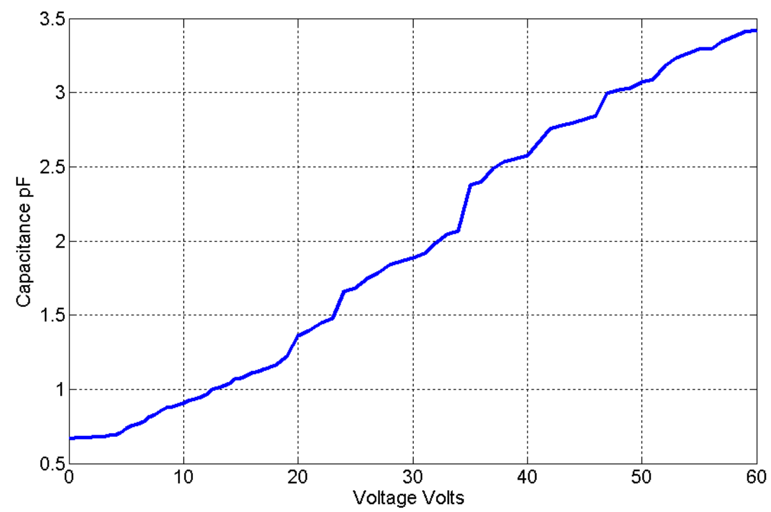


Figure 4.23 The extracted measured tuning behavior of the proposed linear bi-layer capacitor at 1 GHz over a *dc* bias voltage from 0 - 60 V.

Chapter 5

Novel Curled-plate of Analog Continuous and Digital MEMS Variable Capacitors in CMOS technology

5.1 Introduction

The fabrication of Microelectromechanical Systems (MEMS) devices in commercially available CMOS technology, with a minimum feature size of a few hundred nanometers, can push MEMS technology to higher integration. It improves performance of RF integrated circuits and results in the elimination of bulky off-chip components.

MEMS variable capacitors can be used as tuning elements in several RF systems, such as voltage-controlled oscillators (VCOs), tunable filters, and impedance matching networks. Their size and RF response significantly affect the performance of the system. Recently, several MEMS variable capacitors have been reported with different structures and fabrication technologies [8, 24, 27, 34, 36–40, 44–47]. These capacitors are classified as either lateral interdigital or parallel-plate capacitors. Lateral

interdigital MEMS capacitors demonstrate a better linear tuning characteristic than parallel-plate capacitors, whereas parallel-plate capacitors exhibit a higher quality factor and lower parasitic inductance.

Lateral MEMS variable capacitors, fabricated of single crystalline silicon in SOI technology and interconnect layers in CMOS technology, have been described in [24] and [8, 10, 15, 48, 49], respectively. These capacitors exhibit a low quality factor and a low self-resonance frequency and occupy a relatively large area.

Parallel-plate capacitors are simple to fabricate and can be designed for higher capacitance values with a smaller area [33, 34]. In this chapter, novel MEMS/CMOS curled-plate variable capacitors for RF and microwave applications are presented. These capacitors are manufactured in 0.35 μm CMOS technology from Taiwan Semiconductor Manufacturing Company (TSMC), and then post-processed by optimizing the technique presented in [11] at the CIRFE lab at the University of Waterloo. The advantage of choosing CMOS is that MEMS capacitors can be monolithically integrated with active CMOS devices on the same chip to exploit their higher quality factor, smaller area, and higher self-resonance frequency, to create highly integrated RFICs. The two novel structures, proposed in this chapter, have the potential to replace conventional digital and analog continuous capacitors, especially for circuits designed in CMOS technology.

5.2 Designed Capacitors

The new curled-plate MEMS variable capacitors are fabricated in 0.35 μm CMOS technology. The capacitors are built by using metal interconnect layers shown in Fig. 5.1. Four metal layers and two poly-silicon layers are available through this CMOS technology. The top metal layer, metal #4, serves as a mask in the first dry etching stage in the proposed post-processing technique. The top and bottom plates of the parallel-plate capacitors consists of metal #3 and metal #1 layers, respectively. Metal #2 is offered as a sacrificial layer to create an air gap between the capacitor's

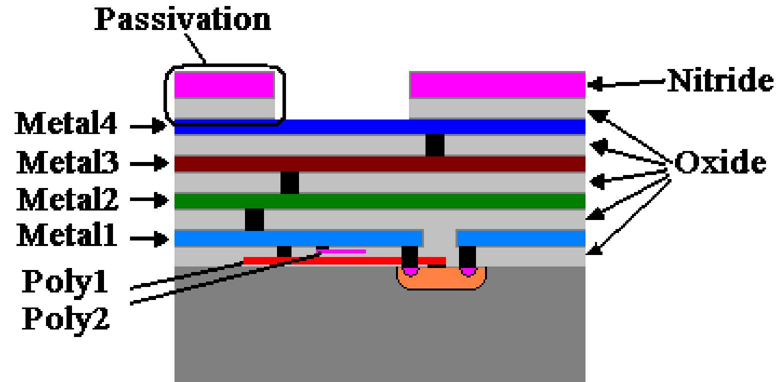


Figure 5.1 A cross sectional view of the layer stack in 0.35 μm CMOS technology from TSMC.

plates. With this approach, the total distance between the top and bottom plates is typically 2.64 μm, including a 1 μm of oxide on both plates and a 0.64 μm air gap. The oxide dielectric layers prevent the capacitor from short circuiting, when the two plates touch each other.

In this chapter, two structures of capacitors, based on a newly designed spring system and curl action due to residual stress, are proposed. The top plate of the capacitor consists of two layers, one on top of the other. The oxide layer of the top plate is found to be 0.65 μm thick and reveals compressive stress, whereas the top layer of the top plate is aluminum and has a tensile stress [50]. Both the top and bottom plates of the capacitors are movable. However, unlike the two movable plate capacitors in [27], the proposed capacitors are integrated monolithically in a commercially available CMOS technology, and their plates are intentionally curled upward to control the capacitors' tuning performance.

5.2.1 Tri-State Curled-Plate Capacitor Design

The first capacitor is a tri-state type capacitor, composed of an eight-beam spring system with four beams for the top plate and four beams for the bottom plate. These are called the main beams. Fig. 5.2 denotes a top view of the tri-state capacitor.

These main beams function not only as electrical paths for the RF signal, but also as

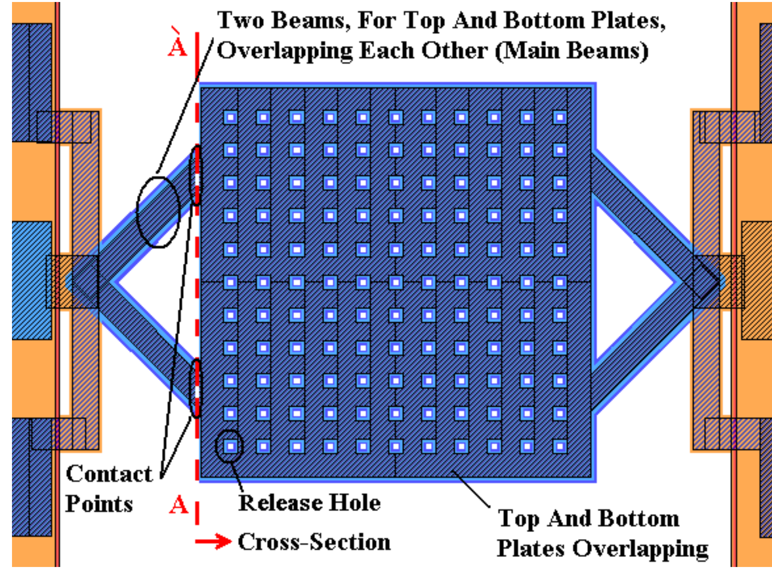


Figure 5.2 A 2-D layout of the tri-state type capacitor built in L-edit.

mechanical supports that control the curl up of the plates (see Fig. 5.2). The beams force both plates to adopt different curvatures, because the beams pull the plates down at the contact points opposing the moment induced from the residual stress. As a result, both plates display non-uniform curvatures that are divided into four top sections and four bottom sections, as depicted in Fig. 5.3. The schematic diagram of the tri-state capacitor can be understood by looking at the cross-section $A\grave{A}$ in Fig. 5.2. In Fig. 5.3, the top sections, TS_4 and TS_2, exhibit different curvatures than those of TS_1 and TS_3. The bottom sections, BS_4 and BS_2, show different curvatures than the bottom sections BS_1 and BS_3. The bottom plate curvatures are relatively smaller than the top plate curvatures due to the thicker oxide layer.

As illustrated in Fig. 5.3, each top plate and each bottom plate consists of four sections with two different curvatures. Both plates of the capacitor touch each other at the initial state, where the *dc* bias voltage is zero (1st capacitance level). After the first collapse voltage, the second state, TS_1 and TS_3 that display a curvature of ρ_1, collapse on their overlapping sections, BS_1 and BS_3, which have a curvature of ρ_3

(2nd capacitance level). At the third state, TS_2 and TS_4, which have a curvature of ρ_2, collapse on BS_2 and BS_4 of the bottom plate, which have a curvature of ρ_4, when the second collapse voltage is attained (3rd capacitance level). Fig. 5.4 is a schematic

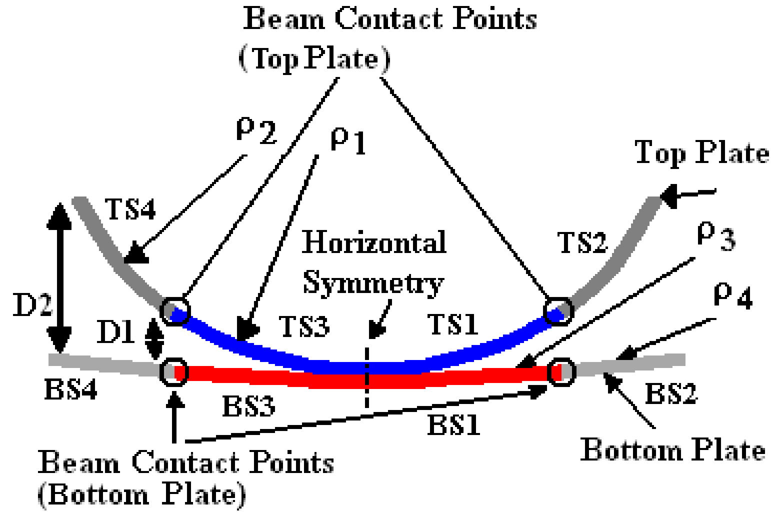


Figure 5.3 A schematic diagram of the novel tri-state capacitor.

diagram for the three previous states of the proposed tri-state capacitor. Fig. 5.4(a) is a schematic diagram of the new capacitor at the initial state at zero *dc* bias voltage. Fig. 5.4(b) depicts the capacitor after TS_1 and TS_3 collapse on BS_1 and BS_3, and Fig. 5.4(c) shows the capacitor after TS_2 and TS_4 collapse on BS_2 and BS_4. The fact that the main beams prevent the top and bottom plates from curling up and having a uniform curvature causes the capacitor to collapse in two steps. This occurs because TS_2 and TS_4 overlaps BS_2 and BS_4 undergo a higher restoring force than that of TS_1 and TS_3 that overlaps BS_1 and BS_3. The difference in the restoring force prevents top sections, TS_2 and TS_4, from collapsing on bottom sections, BS_2 and BS_4, until a *dc* bias voltage is increased and a second collapse voltage point is achieved.

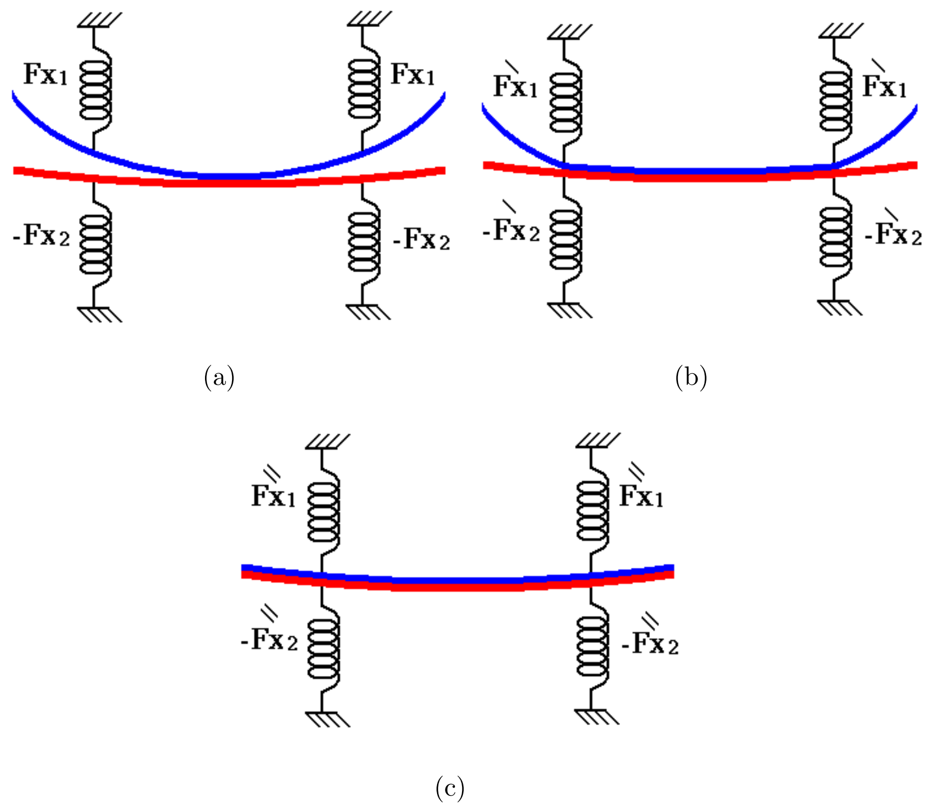


Figure 5.4 A schematic diagram of the proposed tri-state capacitor showing the three main states: (a) the capacitor at zero *dc* bias voltage, (b) the capacitor after the first collapse point, and (c) the capacitor after the second collapse point.

5.2.2 Analog Continuous Curled-Plate Capacitor Design

The second proposed capacitor, a continuous capacitor, has eight main beams and eight additional corner beams that mechanically connect the top and the bottom plates of the capacitor to the silicon substrate. These long and narrow corner beams do not contribute a meaningful spring constant in the transverse direction; however, they do portray the high restoring forces in plane, where the corner beams attempt to prevent the top and bottom plates from curling up as high as the ones in the novel tri-state capacitor. Fig. 5.5 illustrates the layout of the continuous capacitor. The 16-beam spring system that is connected to both plates of the continuous capacitor is shown in the same figure. A schematic diagram of the second proposed capacitor is illustrated in Fig. 5.6. For this capacitor, the corner beams can control the curl of

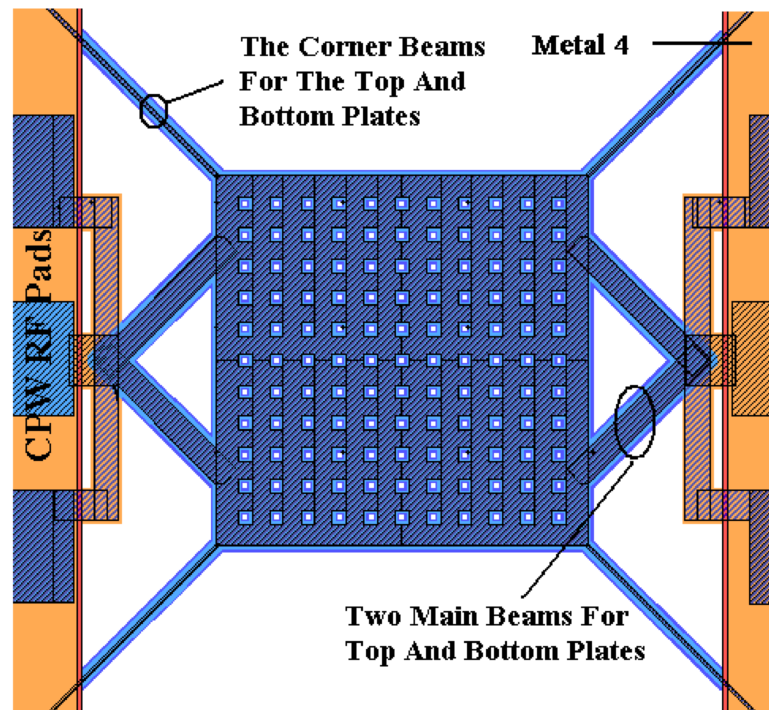


Figure 5.5 A 2-D layout of the proposed curled continuous MEMS/CMOS variable capacitor built in L-edit.

both plates from deflecting too far from one another. The equivalent restoring force of these deflected beams, caused by the moment induced from the residual stresses,

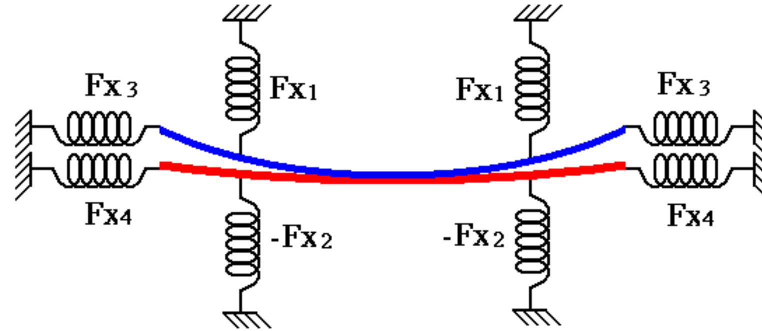


Figure 5.6 A schematic diagram of the proposed curled continuous MEMS/CMOS variable capacitor.

results in a non-linear restoring force that opposes the non-linear electrostatic force, generated by the *dc* bias voltage in parallel-plate capacitors.

5.3 Post-Processing and The Fabrication of The Proposed Capacitors

A maskless post-processing technique is used to release the MEMS curled-plate capacitors. This technique consists of three stages: dry etching, wet etching, and lastly, dry etching. The first stage is the same as that in the dry etching, in [51] for a lateral interdigitated capacitor. In this chapter, the addition of a wet etching stage and a final dry etching stage are proposed to realize the curled-plate capacitors. In this technique, the objective is to etch the sacrificial layer, which is metal #2, create a deep trench in the substrate, decrease the thickness of each oxide layer, etch away the mask layer, metal #4, and finally, expose the RF pads and the top capacitor plate metal layer #3.

The process is developed to integrate the novel MEMS curled-plate capacitors with RFICs that can be implemented in CMOS technology. A schematic view of the post-processing stages is presented in Fig. 5.7. The first dry etching stage consists of three steps: The anisotropic etching of the silicon oxide by using RIE with CHF_3

Table 5.1 Dry Etching Steps

Etching Stage	Etching Method	Etching Step	Gas Content	Gas (sccm)
1	Dry etching	Anisotropic etching in oxide	CHF_3 and O_2	47:3
		Anisotropic etching in silicon	SF_6 and O_2	50:12.5
		Isotropic etching in silicon	SF_6 and O_2	50:5
2	Wet etching	See Table 5.2		
3	Dry etching	Anisotropic etching in oxide	CHF_3 and O_2	47:3

and O_2 plasma, the anisotropic etching of the silicon substrate by employing DRIE with SF_6 and O_2, and the isotropic etching of the silicon substrate by using SF_6 and O_2 [51]. The first dry etching stage that involves the removal of the silicon oxide and the silicon substrate, around the MEMS structure, is signified in Fig. 5.7(b). Since the wet etchants are not selective regarding silicon and aluminum, it is critical to keep an oxide layer around the structural metal layers (metal #1 and metal #3) to protect the aluminum from being etched by the wet etchants. This is accomplished by extending metal #4, over the top of the structural metal layers. Therefore, the metal #2, which must be exposed after the RIE step, should be extended beyond the metal #4 layer. As shown in the cross-sectional view of the new capacitor in Fig. 5.7, metal #4 extends over metal #1 and metal #3 by 2 μm, an extension sufficient to protect the capacitor's two plates from being exposed to non-ideal anisotropic etching.

Table 5.1 lists the parameters and the etch recipe for the first and third dry etching

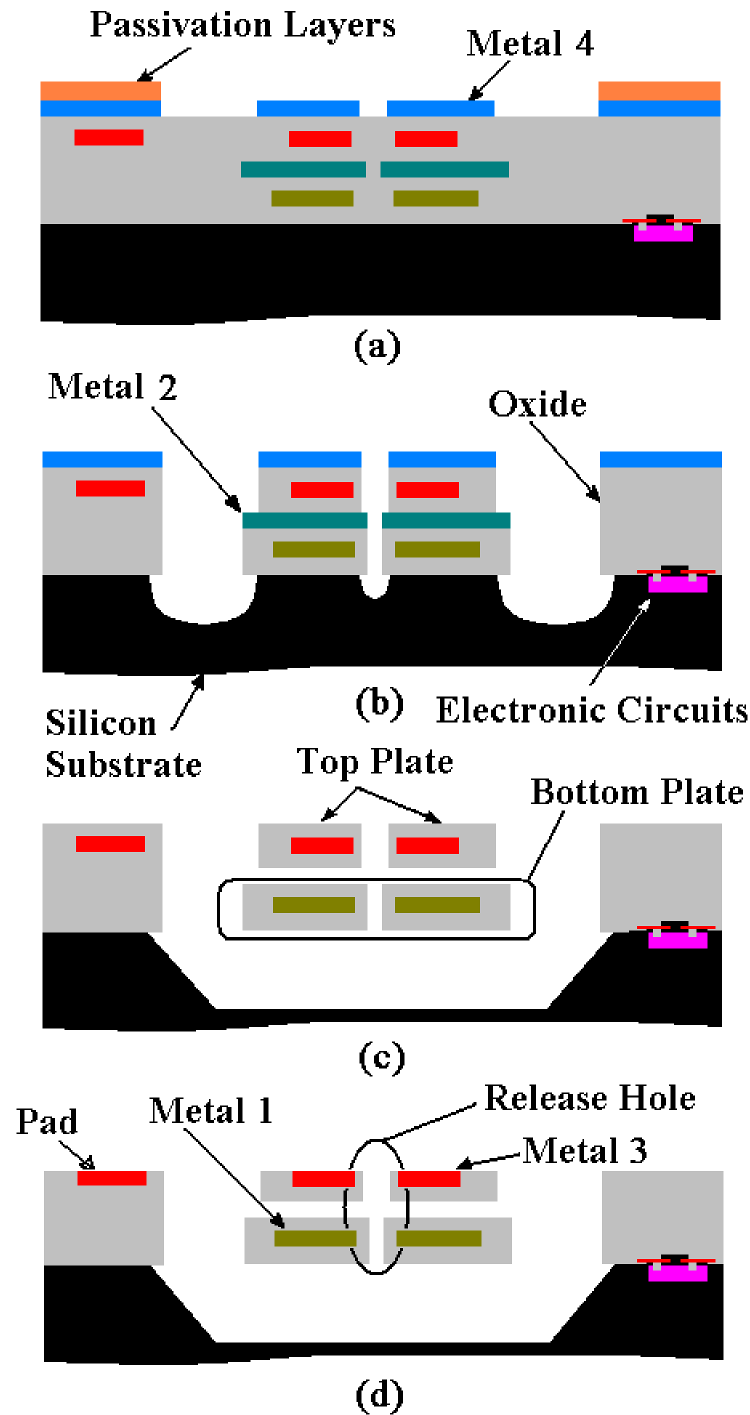
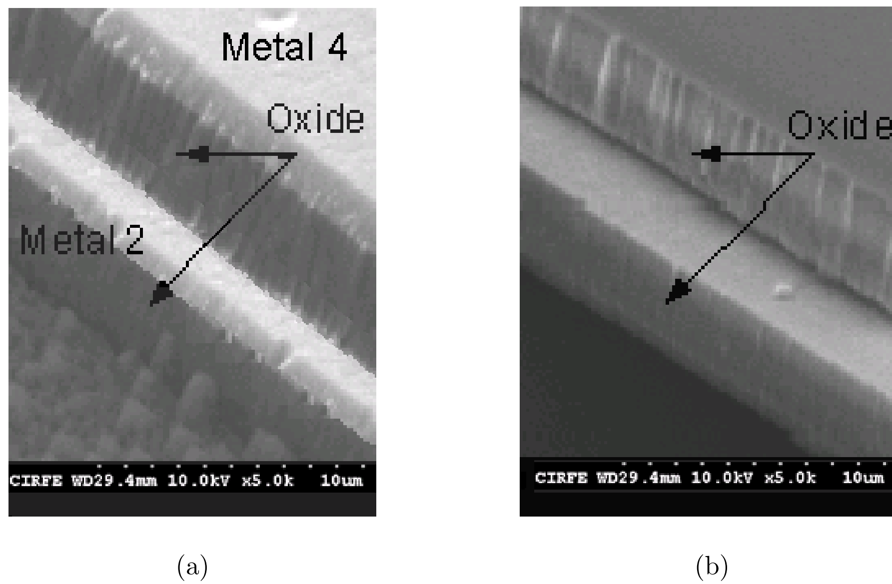


Figure 5.7 The post-processing steps for the new technique of RF MEMS/CMOS integrated circuits: (a) a chip after being fabricated and delivered, (b) after the first dry etching (stage #1) that includes the anisotropic etching of oxide, anisotropic, and isotropic on the silicon substrate, (c) after the wet etching (stage #2) that consists of isotropic etching of aluminum and anisotropic etching of silicon, and (d) after the second dry etching (stage #3).



(a) (b)

Figure 5.8 An SEM picture of the capacitor: (a) after dry etching of oxide, before the wet etching and (b) after the wet etching of aluminum.

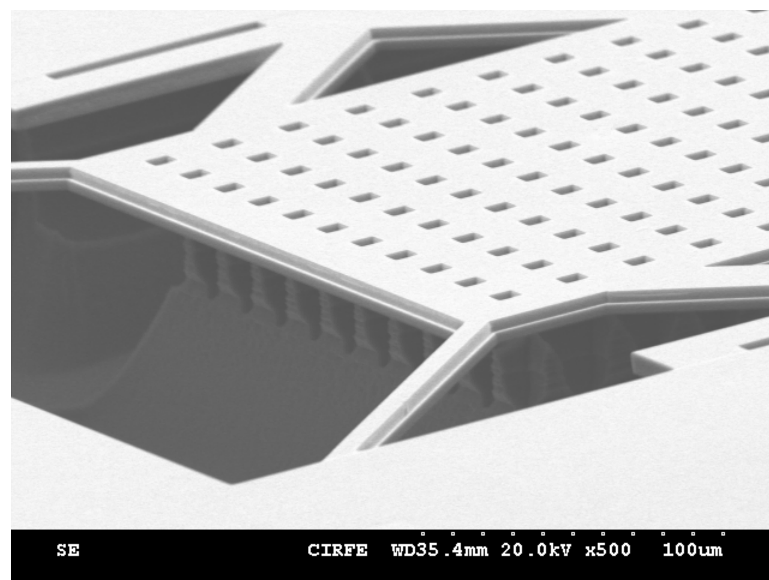


Figure 5.9 The capacitor after the first dry etching stage.

stages. The measured anisotropic etch rate of oxide is 670 Å/min. Fig. 5.8(a) reflects an SEM image of the capacitor after the anisotropic dry etching step of oxide. Then, the substrate is etched by using anisotropic dry etching, isotropic dry etching, and wet etching. Fig. 5.8(b) displays the chip after the wet etching of the aluminum and the silicon substrate. The wet etching achieves the six objectives simultaneously: 1) releases the top plate of the variable capacitor from the bottom plate; 2) etching away the mask layer (metal #4); 3) etching away the lossy silicon substrate underneath the capacitor, which releases the bottom plate; 4) cleans the trench underneath the released structure by etching away the remaining piles of silicon, left after the isotropic dry etching, as shown in Fig. 5.9 and resulting, of course, in a deeper trench in the silicon substrate, compared with using dry etching alone; 5) eliminates the under-etching of the silicon substrate underneath the electronic circuits for the same trench depth; and 6) decreases the thickness of the oxide layers, resulting in lower equivalent stiffness, in order to reduce the actuation voltage between the top and bottom plates and enhance the curl up.

The combination of wet and dry etching of the silicon substrate in the proposed post-processing technique is more desirable than dry etching alone [51] or wet etching alone [11]. The combination requires the same safety distance the dry etching needs from the electronics, and creates deeper trench caused by the wet etching, at least 2.5 times deeper than previously published techniques [11, 51], improving RF performance. Fig. 5.7(c) is a schematic diagram of the released capacitor after the first dry and wet etching stages. The top plate of the variable capacitor is released by etching the exposed sacrificial metal layer which, in this case, is metal #2, as signified in Fig. 5.7(c). The lossy silicon substrate is etched to improve the quality factor, and in turn, enhancing the RF performance.

Etching away the mask layer (metal #4) is a vital step for the new technique because the etching eliminates the huge parasitic capacitance that might be induced in the other three interconnect metal layers and metal #4. The wet etching stage is conducted by a phosphoric-acetic-nitric acids (PAN) etch for 40 minutes at 60 ^{o}C to

etch the aluminum. To etch the adhesion layer, a sulfuric acid (H_2SO_4/H_2O_2) etch for 30 minutes at 60 ^{o}C is sufficient. Finally, potassium hydroxide (KOH) is applied for 10 minutes at 80 ^{o}C at a silicon etching rate of 8.33 μm/min [52] and an oxide etching rate of 38 nm/min [53]. The new technique allows a slight etching of the oxide layer that protects the metal layer. Then, tetra methyl ammonium hydroxide (TMAH) is used for 85 minutes at 90 ^{o}C to continue etching the silicon substrate. The wet etching stage is summarized in Table 5.2.

Etching away the encapsulating oxide layers results in thinner oxide layers, enhancing the curl up of the top and bottom plates, decreasing the total equivalent stiffness and lowering the actuation voltage. The measured oxide layer after the KOH etching is 0.65 μm, indicating that the KOH etched away 0.45 μm from the oxide. TMAH etches the (100) and (110) silicon planes and stops at the (111) plane. The concentration of TMAH used at 90 ^{o}C leads to an etch rate of 0.25 μm/min.

After 95 minutes of wet etching in KOH and TMAH, the total measured depth of the trench is more than 125 μm. Release holes are required to etch the sacrificial metal layer and etch through the silicon substrate so that the lossy silicon substrate underneath can be etched in a shorter period of time. These release holes are created in the metal #4 and metal #2 mask layers, shrinking metal #3 and metal #1, and extending metal #2 farther outward, as shown in Fig. 5.7. Now, the top plate and the bottom plate are readily released without affecting the buffer distance for the electronics on the chip. Moreover, the wet etching stage allows us to release the proposed capacitors with fewer release holes. The size of the hole in metal #2 is 5 μm, and the spacing between two adjacent holes is 20 μm.

Table 5.2 Wet Etching Recipes

Etched Material	Etchant	Recipe	Time
Aluminum	PAN Etch	14:2:1:3	40min@60 ^{o}C
TiN	H_2SO_4/H_2O_2	3:1	30min@60 ^{o}C
Silicon (110) and oxide	PSE200 (KOH)	60%	10min@80 ^{o}C
Silicon (100)	TMAH	25%	85min@90 ^{o}C

5.4 Simulations and Measured Results of The Curled-Plate Capacitors

In the proposed process, the maximum curl up of the MEMS/CMOS capacitors is controlled as follows: 1) the location and number of springs in the design of capacitors that control the curling of the aluminum and oxide layers; 2) the temperature these devices are exposed to during the post-processing stages; and 3) the combination of the different layers of materials used to build the plates of the capacitor. For example, the bottom plate consists of an oxide-aluminum-oxide tri-layer that demonstrates less curling than the top plate, which is a bi-layer of aluminum-oxide.

5.4.1 Tri-State Curled-Plate Variable Capacitor Analysis

For the proposed tri-state capacitor, both plates touch each other at zero *dc* bias voltage. After the *dc* bias voltage is applied, the plates begin to relax on each other

without any significant change in capacitance despite their minimal overlapping areas. Fig. 5.10 shows a schematic diagram of half of the tri-state capacitor after the symmetrical boundary is applied. The new tri-state capacitor is simulated in AN-

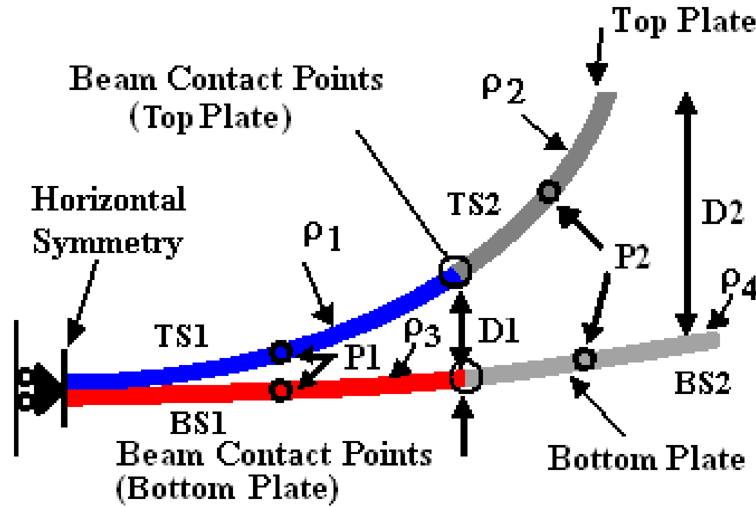


Figure 5.10 A schematic diagram of half of the proposed tri-state capacitor with the applied symmetry line.

SYS. The capacitor's model is simplified by applying two symmetries on one quarter of the capacitor, as depicted in Fig. 5.11. The notations and dimensions of the curled sections are also reflected in Fig. 5.11. The curled sections collapse down step by step at the center of their curvatures, P_1 and P_2 as illustrated in Fig. 5.10 and Fig. 5.11, because of their warped shapes. This is due to the stiffness of the main beams that causes the difference in curvature in the different curled sections. These beams are tilted 45° in plane to impose a force in the direction of the beam, F_t, as conveyed in Fig. 5.11, at the contact points with the plates when the plates curl up due to the induced moment by the residual stress. Also, these beams create bending moments as a reaction at the contact points with the plates that oppose the direction of the moment in the top and bottom plates. The main equivalent force from this bending moment is a vertical force that is applied at the contact points with the plates. As a result of this vertical force, non-uniform curvature is created in the top and bottom

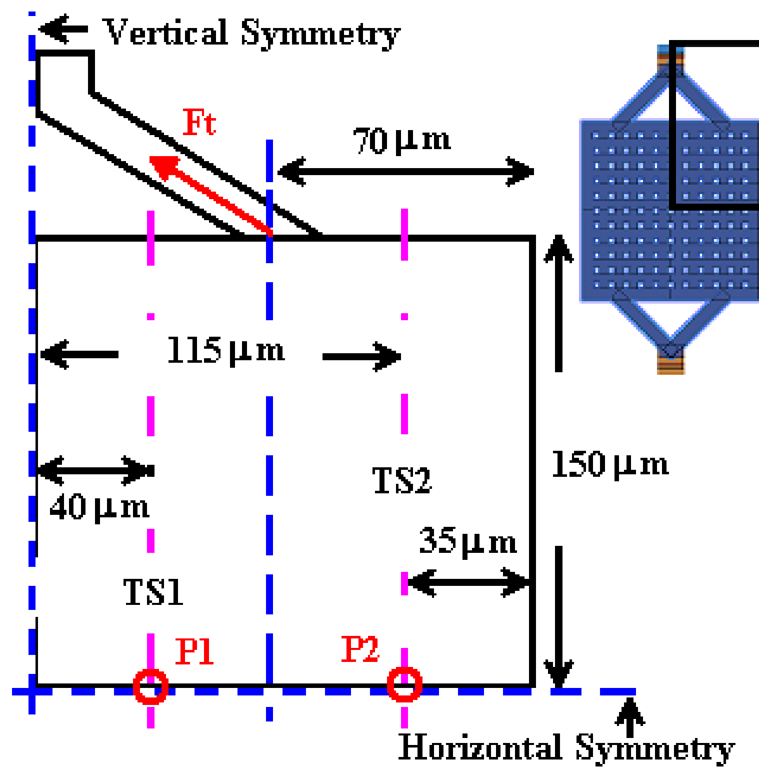


Figure 5.11 A quarter of the tri-state capacitor for both the top and bottom plates, after applying the two symmetry lines

plates.

Fig. 5.12 represents the SEM photography of the tri-state capacitor. The capacitor is analyzed by surface optical profilometer (Veeco) software, and its measured x-axis profile is obtained. The measured maximum curl up of the top plate for the tri-state capacitor is almost 42.7 μm as illustrated in Fig. 5.13. The maximum simulated curl up at zero *dc* bias voltage, obtained using fit to measured curl up data in ANSYS, is 42 μm. From the direction of the measured curl up, the net stress is a tensile stress, caused by the aluminum layer [31]. To verify the measured results, the

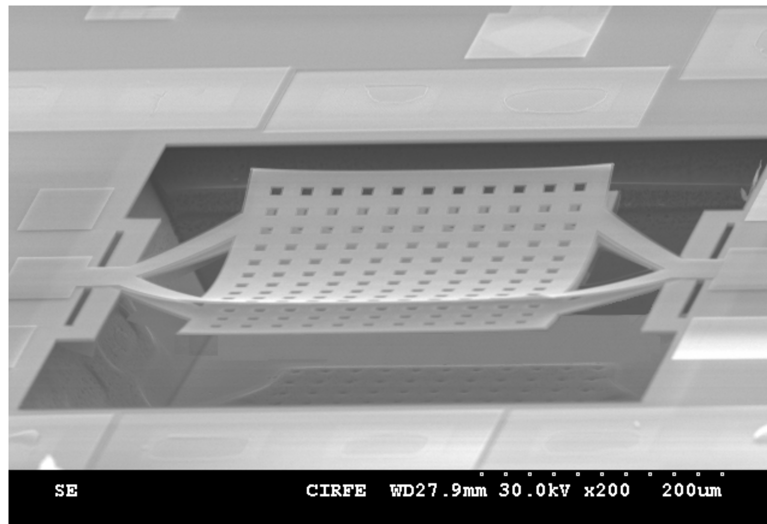


Figure 5.12 An SEM photograph of the fabricated tri-state capacitor post processed at CIRFE.

tri-state capacitor is then simulated in ANSYS using a *dc* bias voltage range from 0-60 V. The used Young's modulus for aluminum and oxide are 49 GPa and 56 GPa, respectively [54]. Both plates, the top and the bottom, attract each other due to the applied electrostatic force. Fig. 5.14 denotes the simulated displacement for the tri-state capacitor at four voltages. The simulated displacement results for the tri-state capacitor demonstrate that the first collapse occurs between 42 and 44 V, and the second collapse occurs between 54 and 56 V. The extracted displacement and the *dc* bias voltages for the locations P_2 and P_1 in the top and bottom plates

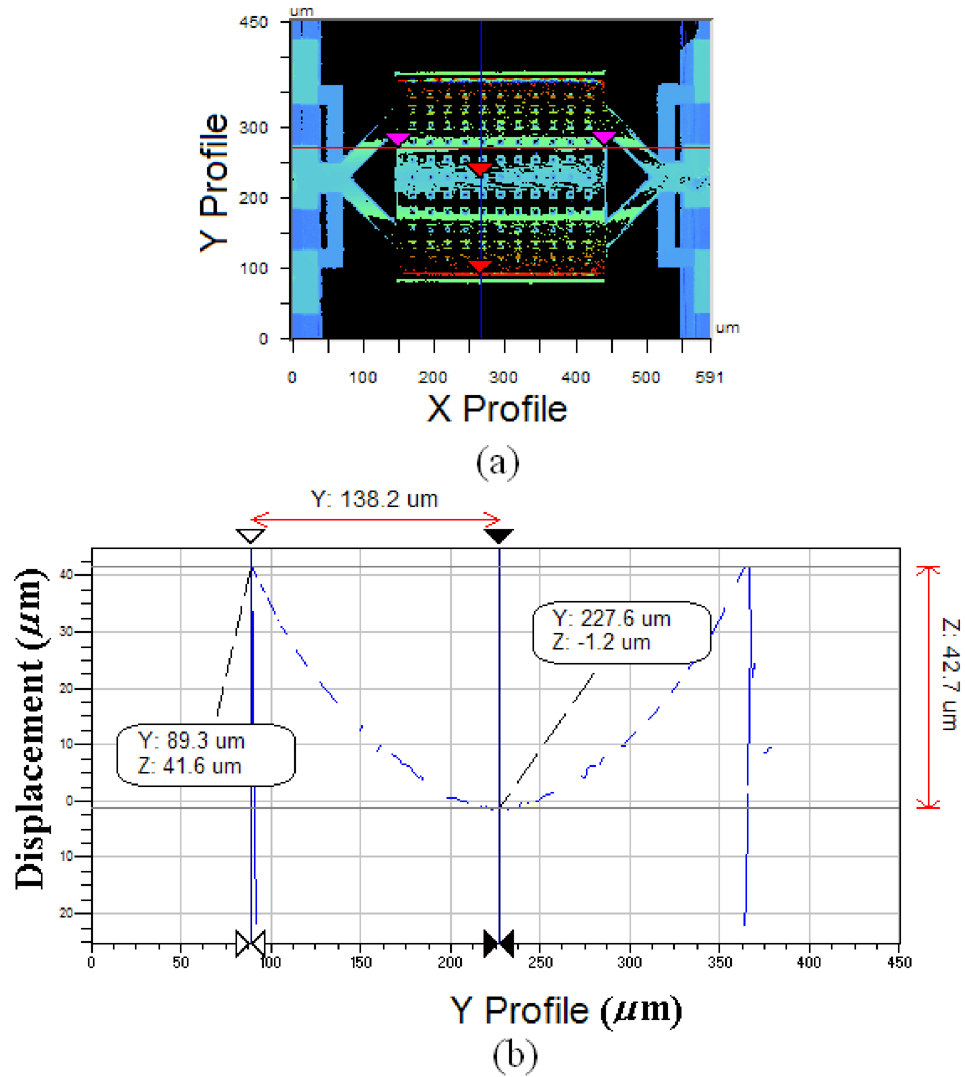
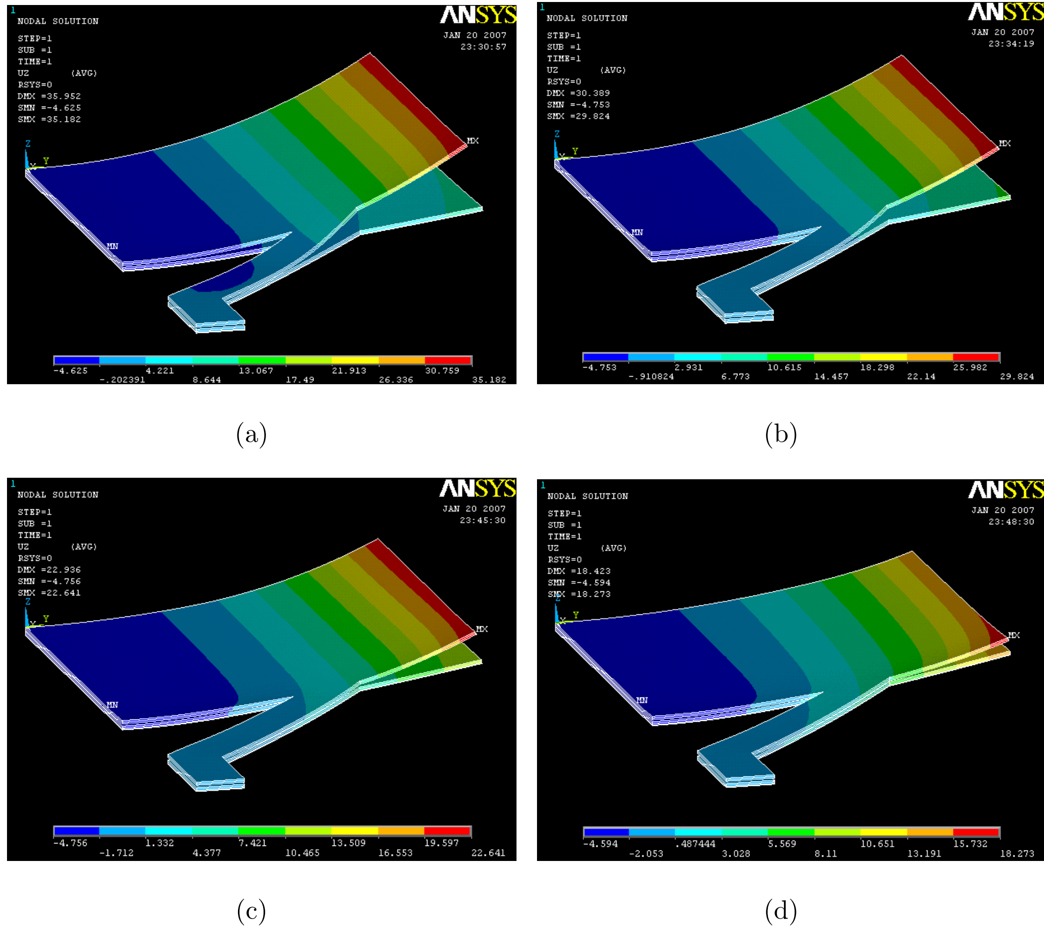


Figure 5.13 The measured profile of the curl up in the capacitor: (a) The top view of the tri-state capacitor, and (b) the 2-D profile of the tri-state capacitor.



(a) (b)

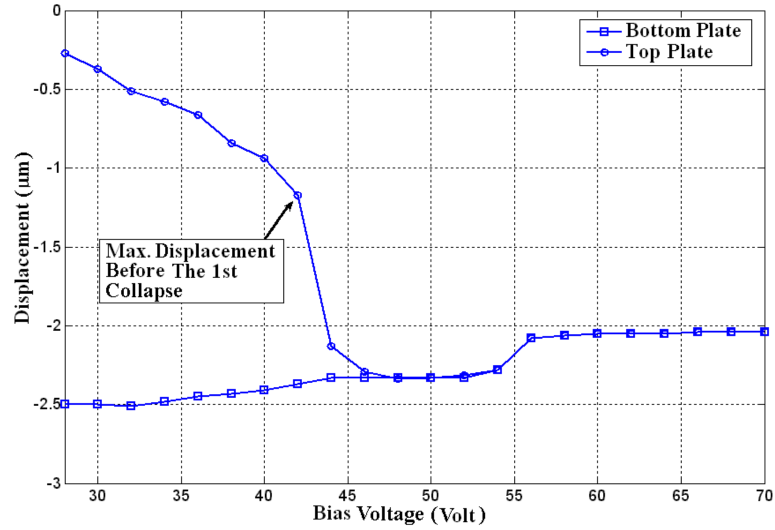
(c) (d)

Figure 5.14 The simulated displacement results of the 3-D structure of the proposed tri-state capacitor obtained in ANSYS, showing the four main positions. (a) the capacitor at 42 V before the first collapse point, (b) the capacitor at 44 V after the first collapse point, (c) the capacitor at 54 V before the second collapse point, and (d) the capacitor at 56 V after the second collapse point.

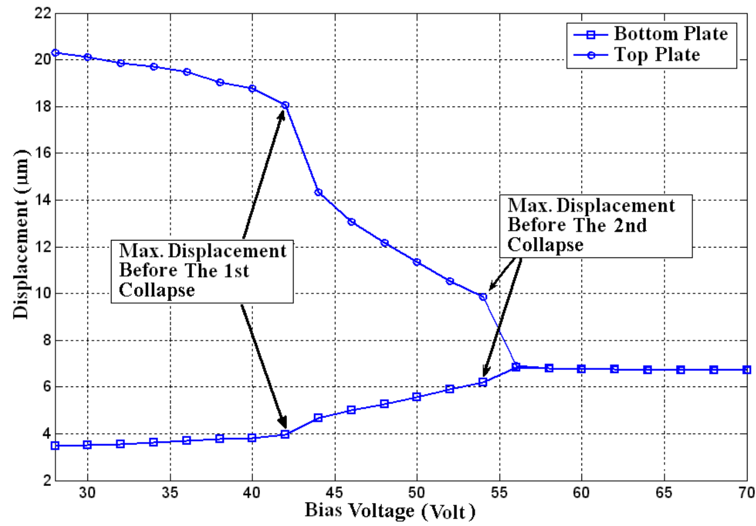
(see Fig. 5.11) are illustrated in Fig. 5.15(a) and in Fig. 5.15(b) in a range of 28 to 70 V, respectively. Fig. 5.15(a) illustrates the maximum displacement before TS_1 collapse on BS_1 at the location P_1. Fig. 5.15(b) reveals that the location P_2 on both plates exhibits two different points of collapse. To model the tri-state curled-plate capacitor, a technique, derived from the method of moments, is developed to theoretically simulate the capacitance between the two plates of the capacitor [55]. In Fig. 5.16, it is assumed that the top plate and the bottom plate areas are divided into subareas where the top plate and bottom plate have N subareas. The capacitance is then calculated by implementing the simulated displacement results obtained in ANSYS, as shown in Fig. 5.15(a) and Fig. 5.15(b) in the newly developed method of moments model. Because of the oxide layers, the equivalent dielectric constant [56] at each subarea is used to obtain the simulated capacitance. This capacitance and the capacitance extracted from the measurement results, after de-embedding the RF testing pads at 1 GHz, are plotted in Fig. 5.17. The measurement and the simulated capacitance are in good agreement. The difference between the extracted simulated and measured capacitance is due to the non-ideal collapse at the edges of the plates, and the fact that the method of moments does not include the RF effect and release holes. The extracted measured self-resonance of the tri-state capacitor is better than 20 GHz at a *dc* bias voltage of 70 V.

After the post-processing technique and the release process, the capacitors are placed in a CO_2 critical point drying system to avoid surface stiction. The residual stress forces the top and the bottom plates to curl upward because of the net tensile stress [42,50,57] while the main beams attempt to oppose this moment at the contact points. This action increases the curvature ρ_2 and ρ_4 compared with that of ρ_1 and ρ_3, respectively, for the top and bottom plates of the tri-state capacitor.

The advantage of using curled-plate sections that collapse at different voltages is that the sections provide a compact structure that has a higher self-resonance, higher quality factor, and less capacitance variation than those of conventional digital capacitors. This occurs because no narrow beams are needed for the arrays of



(a)



(b)

Figure 5.15 The extracted simulated displacement response of the proposed tri-state capacitor in ANSYS model: (a) the extracted simulated results at location P_1, and (b) the extracted simulated results at location P_2.

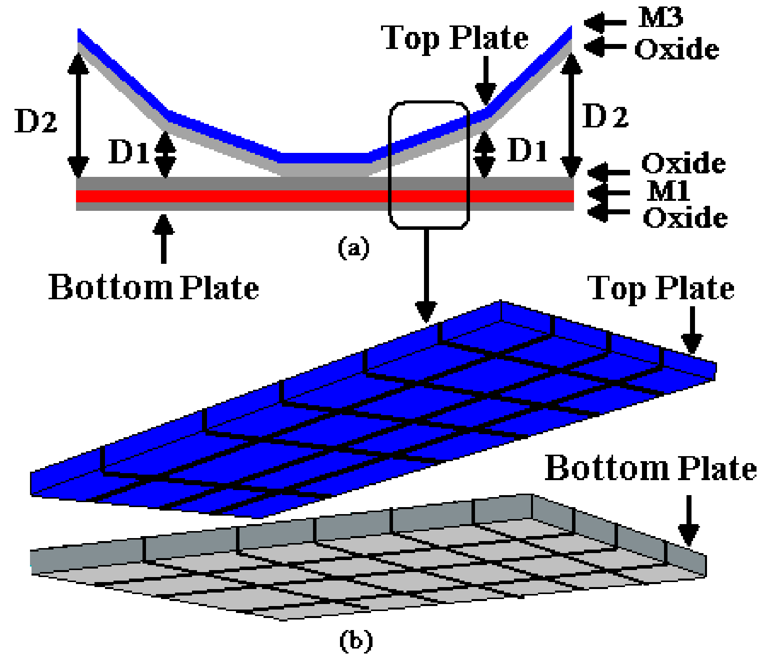


Figure 5.16 A schematic diagram of the MEMS variable capacitor being divided into subareas for both plates.

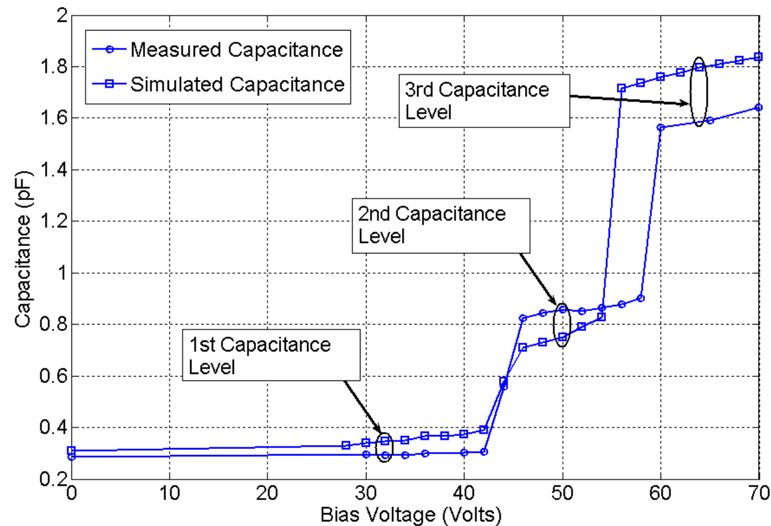


Figure 5.17 The simulated capacitance of the proposed tri-state capacitor using the method of moments based on the displacement results obtained in ANSYS and the measured tuning response of the fabricated tri-state type curled plate capacitor at 1 GHz.

capacitors.

The conventional digital capacitor, reported in [4, 40] yields a continuous performance. The modified version of [4], as described in [37], includes larger plates. However, the beams are narrow for their arrays of capacitors [4, 24, 37]. The 50% maximum tuning range of these plates of the conventional digital capacitor in [37] leads to a measured capacitance variation of 28%, 36%, and 20% for the first, second, and third capacitance levels, respectively. This is due to the effect of the *dc* bias voltage on the other capacitors that should not deform.

The proposed tri-state capacitor exhibits three stable capacitance ranges, based on the novel integrated mechanical tuning system that functions according to the applied *dc* bias voltages. As illustrated in Fig. 5.17, a measured maximum capacitance variation of 9% is obtained at the 2nd capacitance level. The first capacitance level has a variation of 7% over a *dc* bias voltage range of 0-42 V, the second capacitance level has a variation of 9% over a *dc* bias voltage of 46-58 V, and the third capacitance level has a variation of 5% over a *dc* bias voltage range of 60-70 V. The tri-state capacitor exhibits a flatter response and better variation than conventional digital capacitors, as shown in Fig. 5.17. The capacitor's hysteresis is not measured at this stage, but, it might slightly shift the measured response in the voltage axis. This should not affect the maximum variation. The tri-state capacitor is compact with an area of only 500 μm by 500 μm.

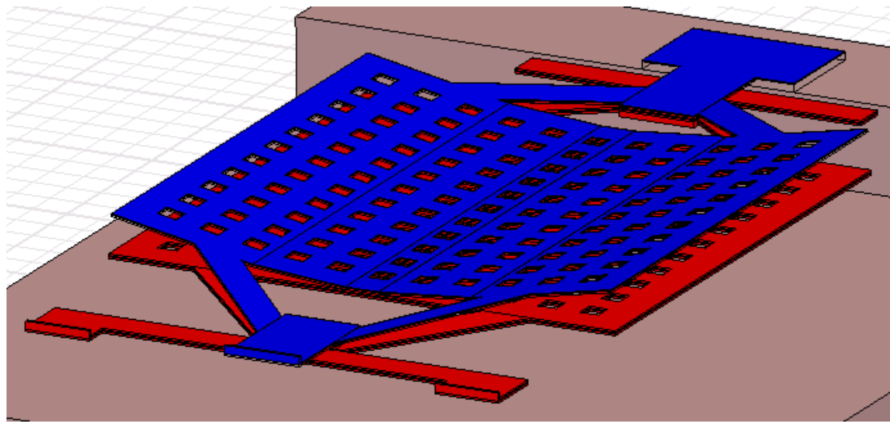
The maximum deflection of the tip of a curled cantilever before collapse with a fixed bottom electrode is reported to be 33% [58] of the total distance between the free end tip and the bottom electrode. Also, the maximum reported capacitance change at the pull-in voltage for a conventional curled cantilever beam is 20% [59]. In conclusion, the curled beams have fewer capacitive variations compared with unstressed beams. However, the tri-state capacitor has capacitive variations that are at least 50% less than those of conventional curled beams. This value results in 75% less variation than that of conventional digital capacitors [37].

The analytical model for the conventional curled structure in [60] assumes a curled

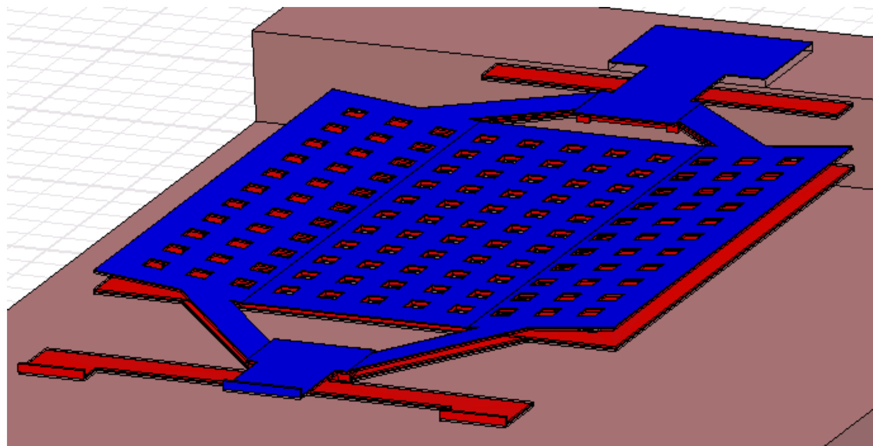
cantilever on top of a fixed electrode. The analyses in [58–60] are not applicable to the proposed structure, since each plate curls up with two different curvatures and the plates attract each other such that the top plate deforms downward, while the bottom plate deforms upward. Moreover, the sections of both plates that touch result in vertical movement, whereas the conventional cantilever is anchored at the corresponding end.

To study the capacitance extracted at high frequencies, the tri-state capacitor is built in HFSS, as reflected in Fig. 5.18. Three HFSS simulations are carried out. The first simulation is for the first state of the tri-state capacitor in which the two plates slightly touch each other in the initial position at zero *dc* bias voltage. In the second simulation, TS_1 and TS_3 collapse on BS_1 and BS_3 due to the applied *dc* bias voltage that exceeds the first collapse point. In the third simulation, the entire top plate collapses on the bottom plate.

Fig. 5.18 shows the 3-D structures of the proposed tri-state capacitor for the zero *dc* bias voltage and after the first collapse voltage. In all the HFSS simulations, the RF pads are excluded, and the trench in the silicon substrate is included. The one port network topology is adapted to extract the capacitance from the S-parameters simulated in HFSS. Fig. 5.19 provides a comparison between the extracted capacitance from HFSS and the extracted capacitance from the measurements. The results of the extracted capacitances from HFSS are in good agreement with the measurements for the zero *dc* bias voltage and the 46 V *dc* bias voltage. The error is 34% at 5 GHz for a *dc* bias voltage of 70 V. This error is due to the remaining oxide in the release holes under the mask layer metal #4 and the sacrificial layer metal #2. This oxide, that has a dielectric constant of four, creates higher parasitic capacitance due to the fringing field in comparison with air that has a dielectric constant of one.



(a)



(b)

Figure 5.18 The proposed capacitor simulated in HFSS: (a) the capacitor after being deflected due to the residual stress before applying *dc* bias (1st state), and (b) the simulated capacitor after the first collapse point (2nd state)

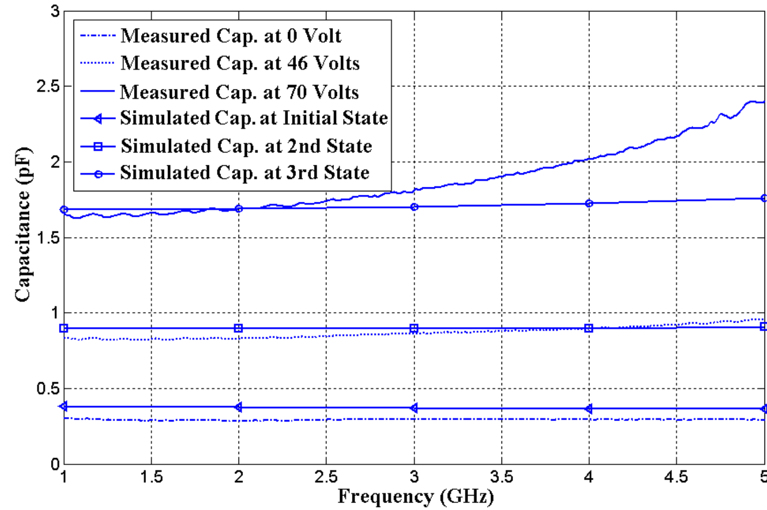


Figure 5.19 A comparison between the simulated capacitances in HFSS and the measured capacitance from 1 GHz up to 5 GHz for the tri-state capacitor.

5.4.2 Analog Continuous Curled-Plate Variable Capacitor Analysis

The analog continuous capacitor in Fig. 5.5 has corner beams, which are relatively low in their spring constants in the transverse direction, connecting the corners of the capacitor to the substrate. The existence of these corner beams prevents the top plate and the bottom plate from curling up too high and moving away from each other.

The capability of these corner beams to limit the plates of the analog continuous capacitor from curling upward to the same height as that of the tri-state capacitor, induces high stress in the corner beams' axial directions. However, the corner beams are thinner than the main beams to allow the corners of the capacitor to curl upward relatively more than the curl up at the contact points of the main beams. This facilitates the creation of a non-linear equivalent spring constant in both the top and bottom plates that results in a non-linear restoring force. This force opposes the induced non-linear electrostatic force from the applied *dc* bias voltage, and as a result, deforms both plates without discontinuities from collapsing.

Fig. 5.20 presents a top view of the schematic diagram of one quarter of the analog continuous capacitor. The in plane restoring force from the corner beam axial direction is decomposed to two forces in the guided beams [61]. F_1 and F_2 are the projections of the force caused by the corner narrow beam, whereas F_3 and F_4 are the projections of the force caused by the main wide beam. To measure the initial

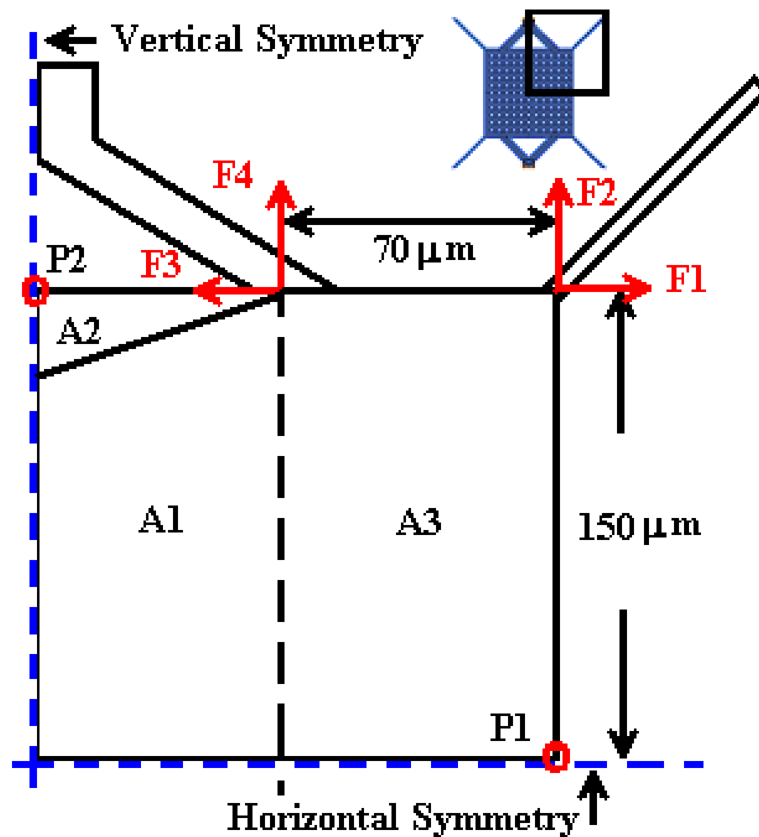


Figure 5.20 The top view of a schematic diagram of a quarter of the curled analog continuous capacitor for both plates, top and bottom, illustrating the induced tensile force.

curl up of the analog continuous capacitor, an optical surface profilometer (Veeco) is used. Fig. 5.21 shows the SEM photography of the analog continuous capacitor. Fig. 5.22 provides the 2-D profile. The maximum curl up between the edges of the top plate and the center of the capacitor is measured by the surface profilometer and found to be 15.8 μm, as depicted in Fig. 5.22.

In addition, the proposed analog continuous capacitor is simulated in ANSYS. The portion of the capacitor in Fig. 5.20 is used after two symmetry lines are applied. The maximum simulated curl up using fit to measured curl up data in ANSYS, which occurs at the location P_1, is found to be 14.51 μm at zero *dc* bias voltage. The maximum simulated curl up of the hidden bottom plate of the capacitor is then obtained from ANSYS and found to be 5.8 μm at the location P_1 as well. Because of the oxide-aluminum-oxide tri-layer, there is less curl up in the bottom plate. The capacitor is simulated over a *dc* bias range from 0 V to 70 V. Fig. 5.23 illustrates the 3-D results at four different *dc* bias voltages. The simulated results of the displacement

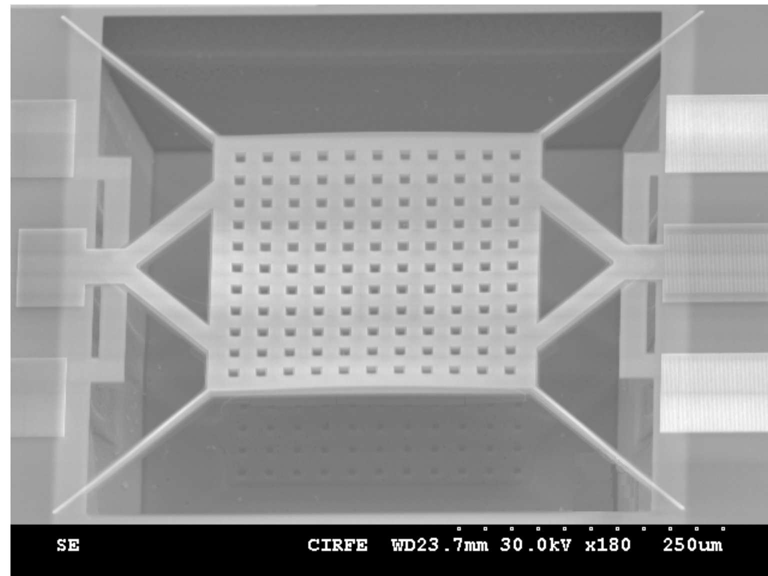


Figure 5.21 An SEM photograph of the fabricated curled analog continuous capacitor.

in ANSYS, in relation to the *dc* bias voltage of the location P_1 for the area A_3 (see Fig. 5.20) are shown in Fig. 5.24(a). A small area of the analog continuous capacitor A_2 on Fig. 5.20 indicates a jump in displacement at 46 V, as shown in Fig. 5.24(b). This jump occurs because of F_3 and its symmetrical force from the vertical symmetry line, causing these sections of the capacitor to collapse, as a cause of buckling, on each other and cause a capacitance jump [31]. It is clear from the simulated results

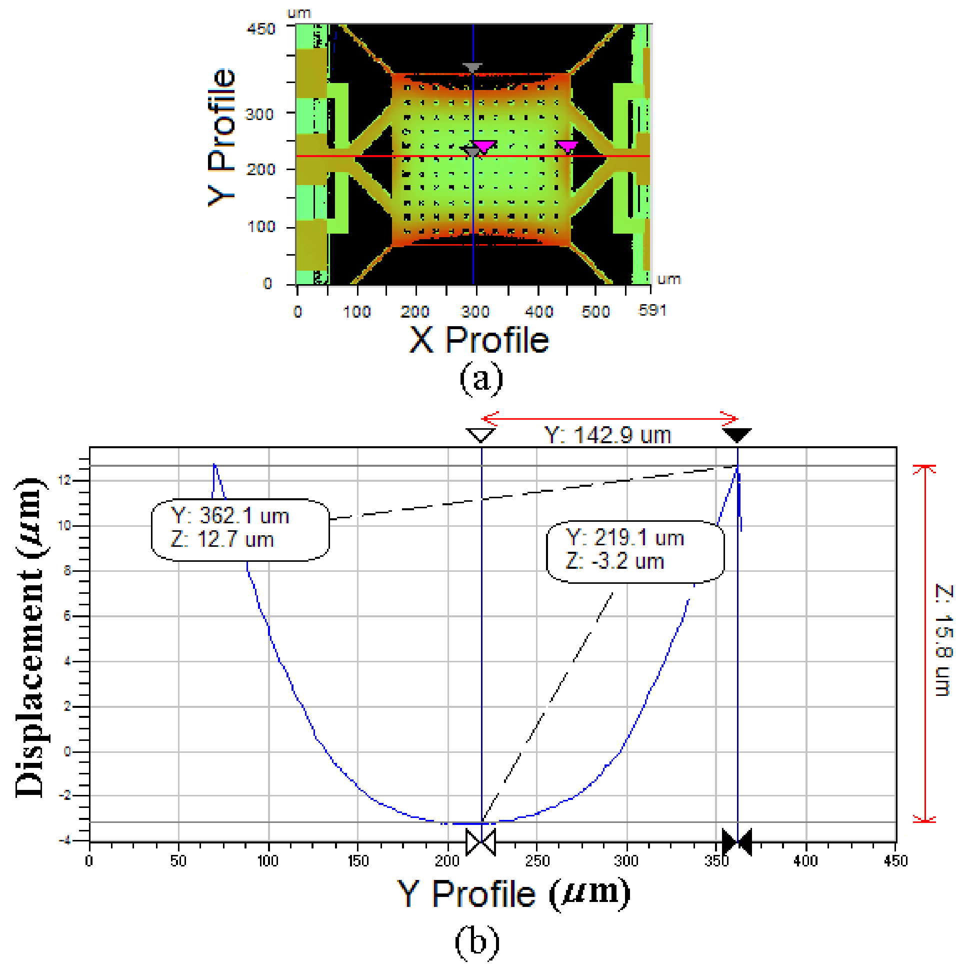


Figure 5.22 The measured profile of the curl up in the capacitor: (a) the top view of the curled analog continuous capacitor, and (b) the 2-D profile of the of the Y axis of the capacitor.

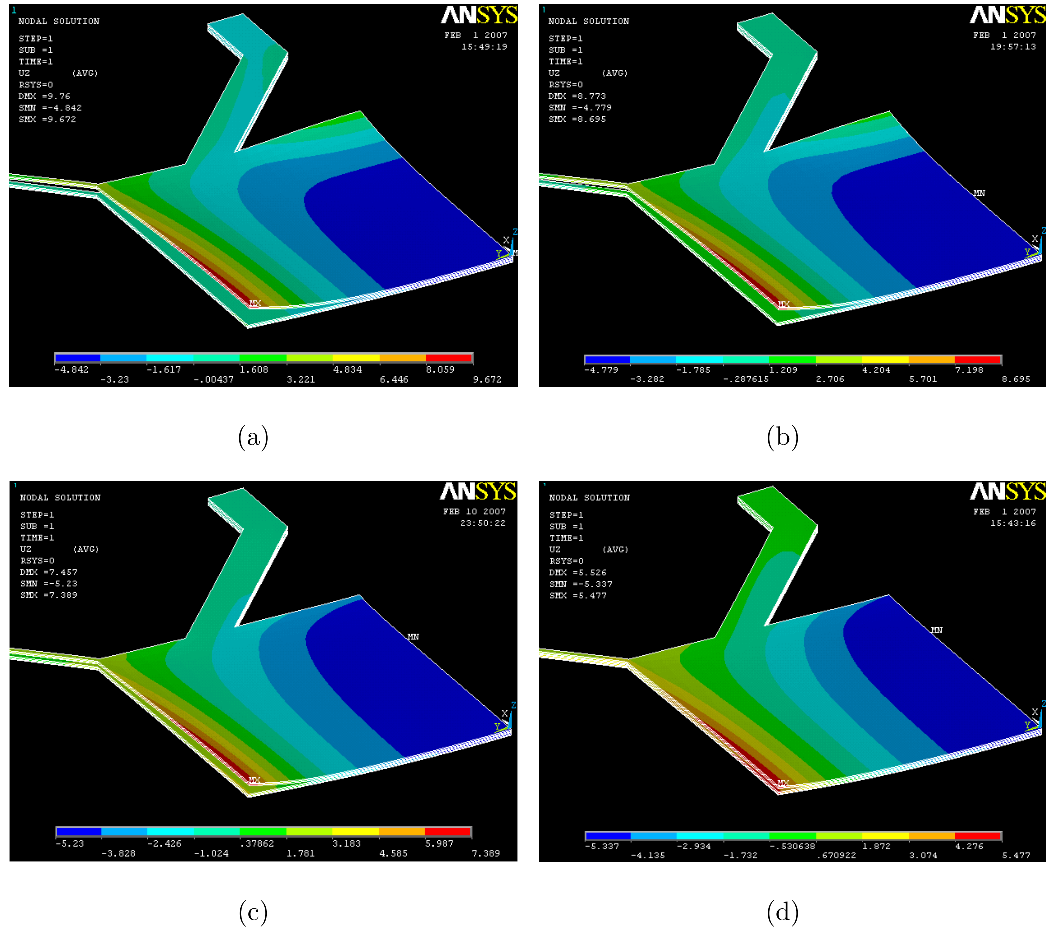
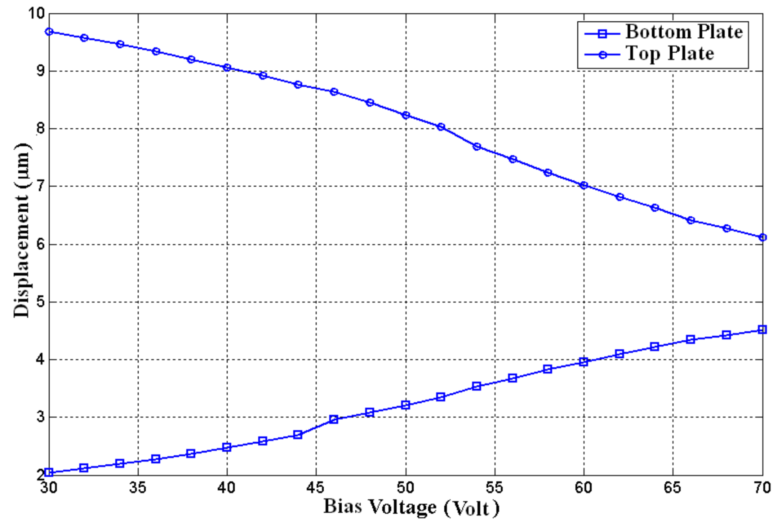
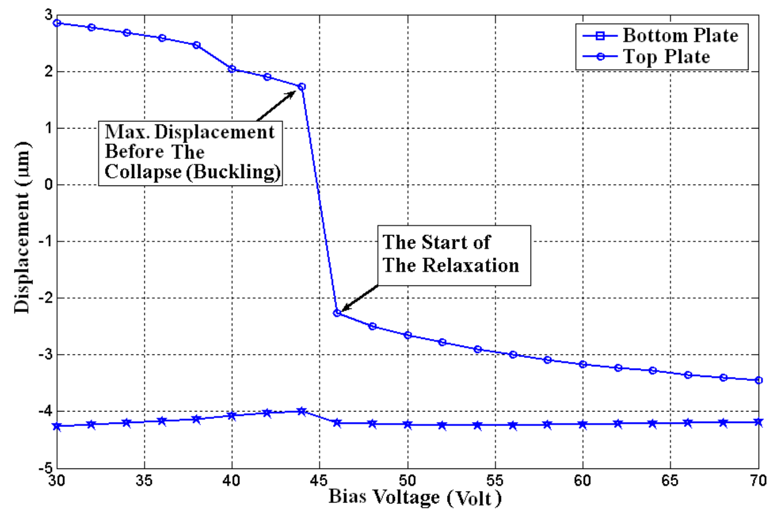


Figure 5.23 The 3-D displacement results of the proposed curled analog continuous capacitor showing four obtained results: (a) the capacitor at zero *dc* bias voltage, (b) the capacitor at a 36 *dc* bias voltage, (c) The capacitor at 52 *dc* bias voltage, and (d) the capacitor at 70 *dc* bias voltage.



(a)



(b)

Figure 5.24 The simulated displacement versus *dc* bias voltage of the curled analog continuous capacitor obtained in ANSYS, (a) the displacement results for both plates of location P_1 that is shown in Fig. 5.20, and (b) the displacement results for both plates at location P_2 shown in Fig. 5.20.

for the displacement versus *dc* bias that both plates move toward each other.

The extracted measured capacitance at 1 GHz and the theoretically simulated capacitance of the method of moments model over a *dc* bias voltage from zero up to 70 V is illustrated in Fig. 5.25. The measurement indicates that the capacitor changes its slope at 44 V, due to the small jump in area A_2 for both plates. The difference between the measured and simulated results is due to the complexity of the curled plate of the proposed capacitor that was approximated in the method of moments model and the fringing field that is not included in the same model. The capacitance

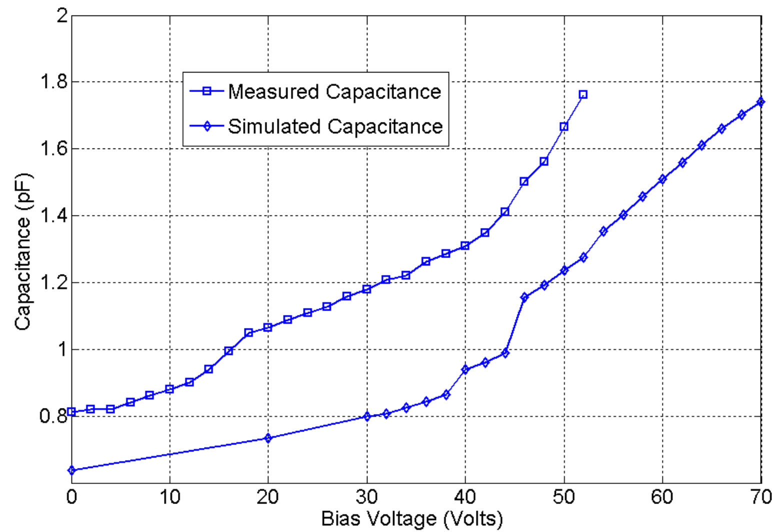


Figure 5.25 The measured tuning response of the fabricated analog continuous curled-plate capacitor at 1 GHz and the simulated tuning response using the method of moments model.

extracted from the measurement over a frequency range of 1 GHz to 5 GHz is plotted in Fig. 5.26. The proposed analog continuous capacitor demonstrates a continuous tuning response for two ranges of the measurements; the first is from 18 V to 42 V and the second range is from 42 V to 52 V.

Unlike the conventional capacitor that is reported in [11] which has a 50% tuning range before the pull-in, the proposed analog continuous capacitor is not prone to the pull-in voltage for the following two reasons: 1) the top plate is already touching the

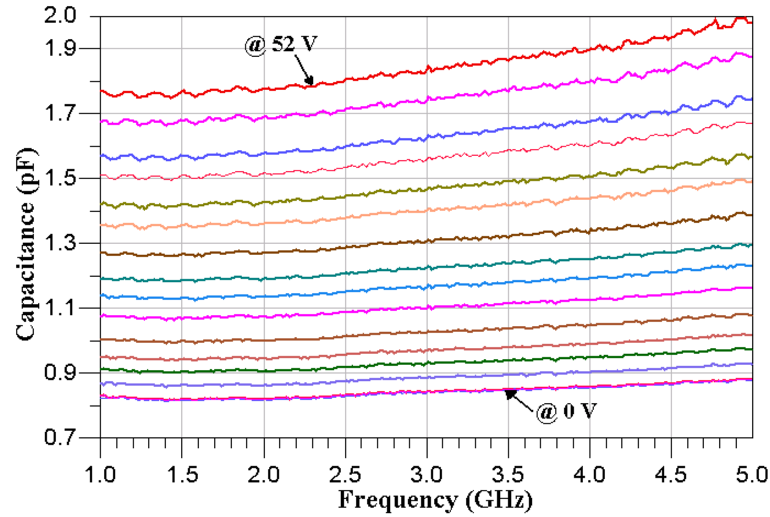


Figure 5.26 The measured extracted capacitance of the curled-plate analog continuous MEMS/CMOS variable capacitor from zero *dc* bias voltage up to 52 *dc* bias voltage for a frequency from 1 GHz up to 5 GHz.

bottom plate with an area A_1 (see Fig. 5.20). The contact is due to the initial curling upward, initiated by the residual stress on both plates and 2) the equivalent restoring force for the spring constant system is non-linear due to the existence of the residual stress, the corner beams, and the main beams.

The measured quality factor of the capacitors is extracted from the S-parameters (S_{11}) that are illustrated in Fig. 5.27 for both capacitors, after the RF pads are de-embedded. Fig. 5.28 illustrates the measured quality factor for both capacitors. The quality factor of the analog continuous capacitor is better than 300 at 1.5 GHz at zero *dc* bias voltage, which is at least 4.6 times better than the quality factor of the conventional parallel-plate capacitor, reported in [11] due to the deeper trench obtained by the combination of the dry and wet etching of the silicon substrate. The jumps and fluctuations in the measured quality in Fig. 5.28 may have been caused by external vibrations from the environment.

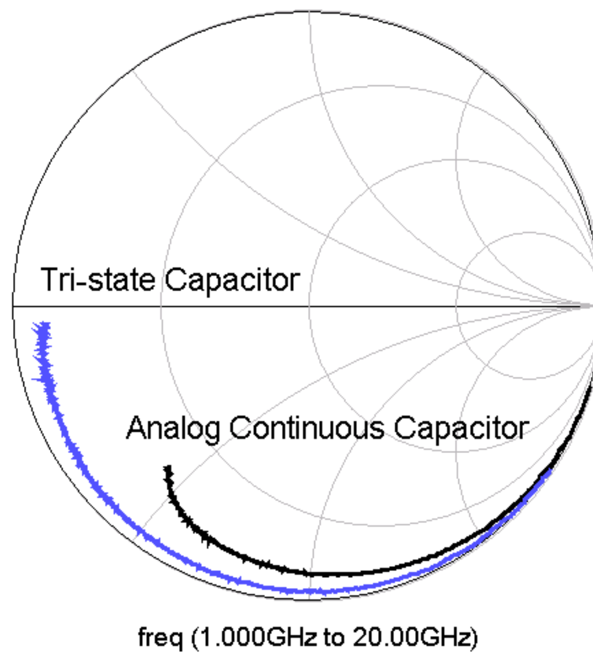


Figure 5.27 The measured S_{11} of the tri-state and the analog continuous MEMS varactors before de-embedding the RF pads.

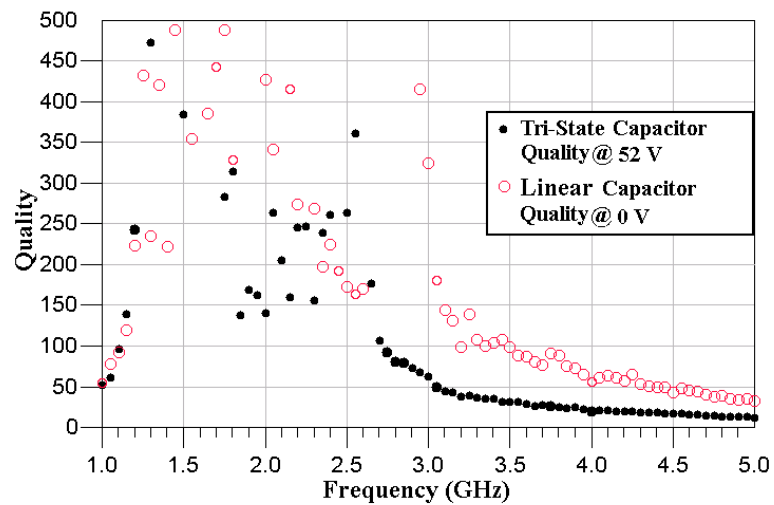


Figure 5.28 The measured quality factor of the proposed analog continuous and tri-state MEMS/CMOS variable capacitors at zero *dc* bias voltage and 52 *dc* bias voltage, respectively.

5.5 A Tunable BPF Employing MEMS Varactor in 0.18 μm CMOS Technology

A tunable band-pass filter that utilities a novel parallel-plate MEMS variable capacitor that has its electrostatic actuators electrically separated from the capacitive parallel plate MEMS varactor whereas they are still bonded together is proposed. In order to build a tunable filter that has efficient occupied area on CMOS technology, lumped element approach should be the topology to adopt. This section describes a novel topology of tunable band-pass filter at a center frequency of 5GHz with a relative bandwidth of 10% and a tuning range of 50%.

Recently, [11] reported a post-processing technique to build parallel plate MEMS varactor in 0.35 μm CMOS technology. This technique allows obtaining relatively high quality factor and high self resonance MEMS varactors that can be monolithically integrated in CMOS technology. The reported filter [11] exhibits a center frequency of 10GHz and a bandwidth of 10% with a tuning range of 17% and occupies an area of 2x1.7 mm^2. In order to build tunable band-pass filter that can work at Wi-Fi operating range, lumped element topology is utilized in order to maintain small real estate on CMOS chip. The proposed tunable filter consists of three shunt resonators that are coupled with capacitors as illustrated in Fig. 5.29. The tunable filter has been fabricated in TSMC 0.18 μm CMOS process and post-processed in CIRFE at University of Waterloo. The cross sectional view of the TSMC 0.18 μm CMOS

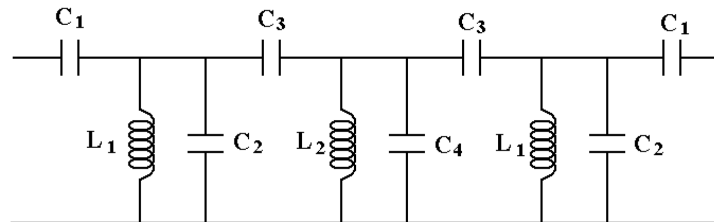


Figure 5.29 A schematic diagram of the proposed capacitor.

technology is shown in Fig. 5.30. This process consists of 6 metallization layers plus 1 polysilicon layer that can have two different resistivities. The schematic diagram and

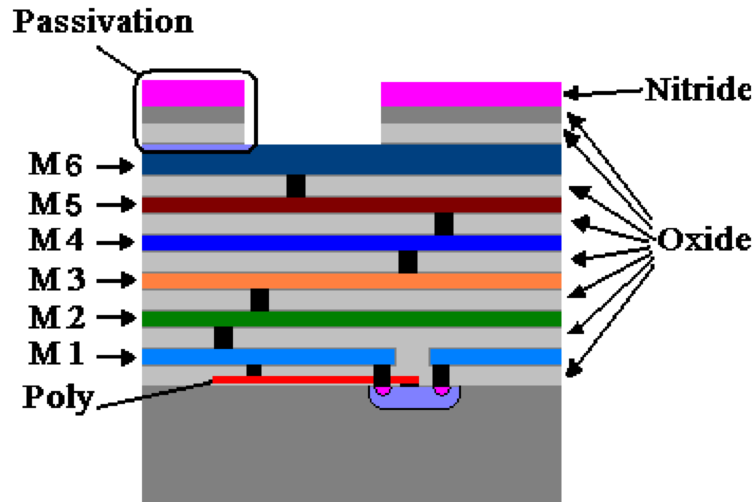


Figure 5.30 The top view and the cross section of the mechanical-electrical-bonding point in the variable capacitor before release.

the cross sectional view of the capacitor's structure in the proposed tunable band-pass filter is depicted in Fig. 5.31. The 2-D layout of the proposed tunable band pass filter is illustrated in Fig. 5.32. Two different sizes of MEMS variable capacitors are implemented in the filter with a same size inductor. Metal-insulator-metal (MIM) fixed capacitors are used for the coupling capacitors between the three resonators. M6 is used as the mask layer during the RIE etching of the silicon oxide and the silicon. In order to protect the capacitor's plates and the actuators' plates, the mask layer M6 is extended 3 μm beyond these plates. In order to avoid using the relatively lossy vias in the signal metallization layer in the fabricated tunable filter, different layers are used for the capacitor's and the actuators' electrodes. The MEMS varactor in the center uses M5 and M3 as the top and bottom plates of the capacitor's electrodes and the actuators' electrodes whereas M4 is used as the sacrificial layer. The MEMS varactors on the left and right sides use M4 and M2 as their top and bottom plates of the capacitor's electrodes and the actuator's electrodes where as M3 is used as a

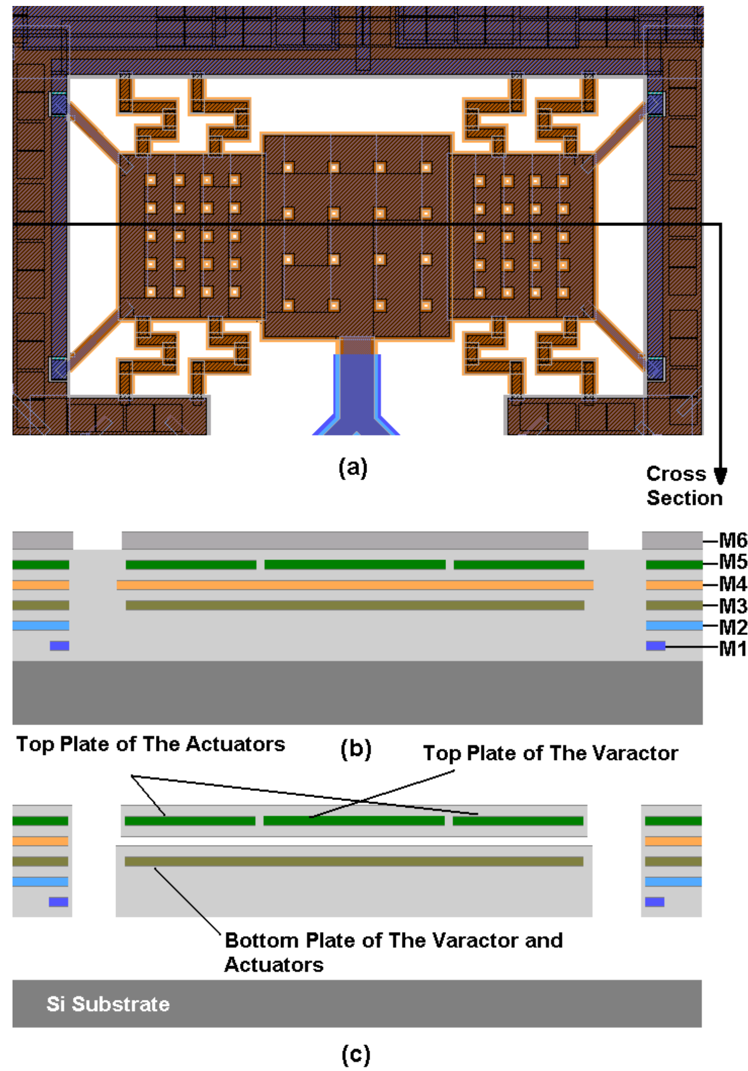


Figure 5.31 The proposed MEMS variable capacitor in 0.18 μm: (a) top view of the capacitor in L-edit, (b) a cross sectional view of the proposed capacitor before post-processing, and (c) a cross sectional view of the proposed capacitor after post-processing.

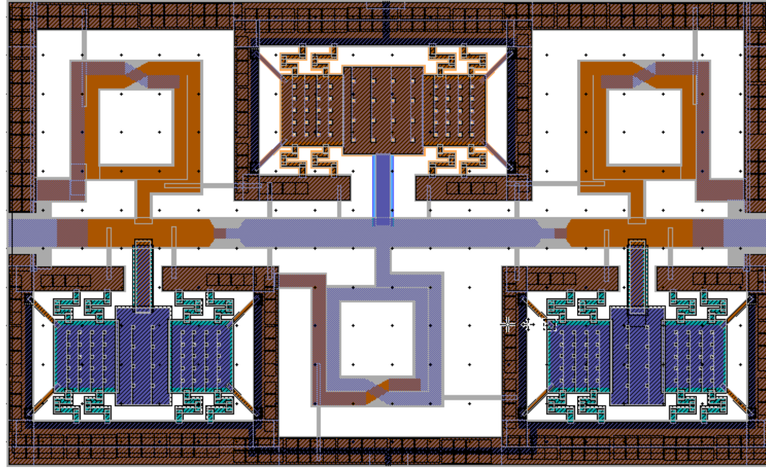


Figure 5.32 The top view and the cross section of the mechanical-electrical-bonding point in the variable capacitor before release.

sacrificial layer. The sacrificial layers are extended even beyond the mask layer M6 to ensure that they get exposed during the RIE etch in order to be etched away later during the wet etch.

A post processing recipe was characterized for the 0.18 μm using pure CHF_3 gas. A 3-D profile of 0.18 μm TSMC CMOS chip is shown in Fig. 5.33. Built up were observed in the output hose of the roughing pump. The recipe had to be re-characterized using CF_4 gas. Pure CF_4 and CF_4 with O_2 have to be used in our RIE. Fig. 5.34 are the SEM pictures of the fabricated tunable filter before and after applying the new post-processing technique. Fig. 5.35 are the zoomed SEM pictures of the fabricated tunable filter after applying the post-processing technique. The tunable filter is modeled in hpADS to obtain the maximum tuning range as shown in Fig. 5.36. The tunable filter is then built and simulated in HFSS as shown in Fig. 5.37 and the results are compared with the modeled result at a center frequency of 5 GHz in Fig. 5.38 for the lossless case. The simulated insertion and return losses after including the metallization and the substrate losses are depicted in Fig. 5.39. The simulated results show that an insertion loss of 4.2 dB is achieved at 5 GHz with a return loss of better than 14 dB. The filter is tuned by applying a *dc* bias voltage

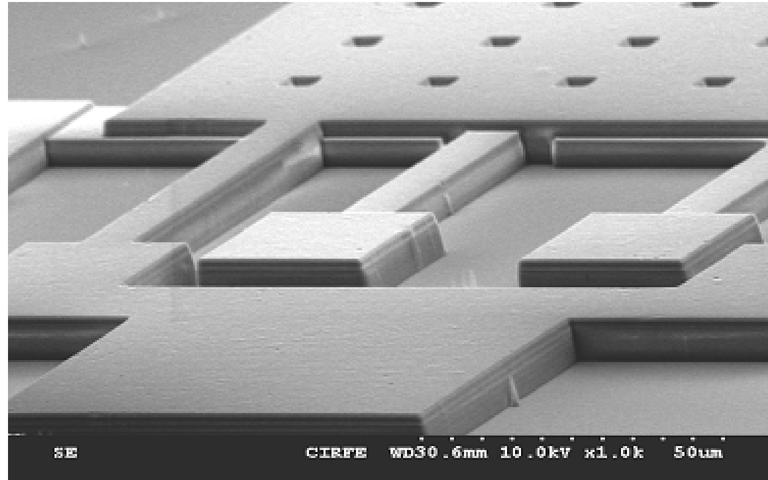
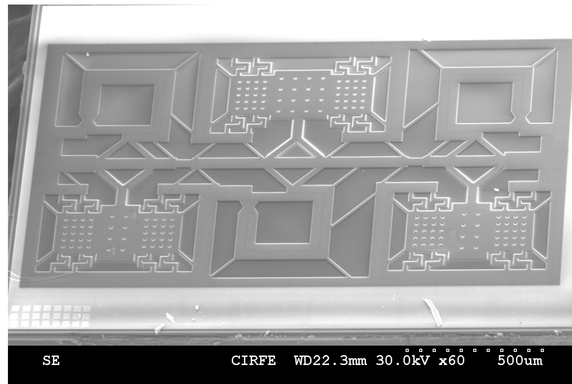


Figure 5.33 A 3-D profile of the 0.18 μm CMOS technology from TSMC.

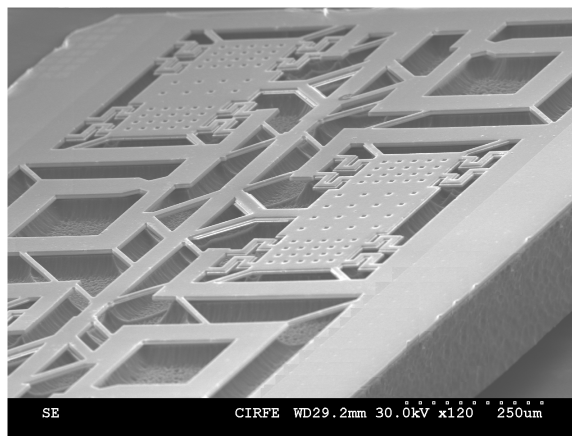
on all three capacitors. The filter could not be measured due to the following reason. During the final step of post processing 0.18 μm chips, debris of the dirts from the RIE shower head fell on the chips and caused pin holes through the mask layer and the oxide underneath it. This caused the the wet etchant to penetrate the oxide layer under the mask layer and as a result attacked the protected aluminum layers. A solution to this problem could be running the clean recipe of SF_6 and O_2 in the middle of the process to ensure cleanness of the RIE shower head.

5.6 Summary

A maskless MEMS, CMOS-compatible, post-processing technique that enables the fabrication of parallel-plate capacitors type for RF and microwave circuits is introduced. Two structures of curled-plate MEMS variable capacitors are proposed: a tri-state curled-plate capacitor and an analog continuous curled-plate capacitor. Both capacitors are fabricated by using a commercially available 0.35 μm CMOS technology. The residual stress of the CMOS fabrication process is adopted as a feature to tailor the tuning performance of the capacitors.



(a)



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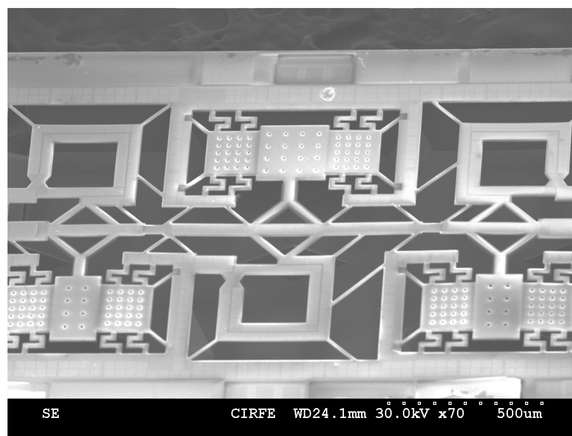
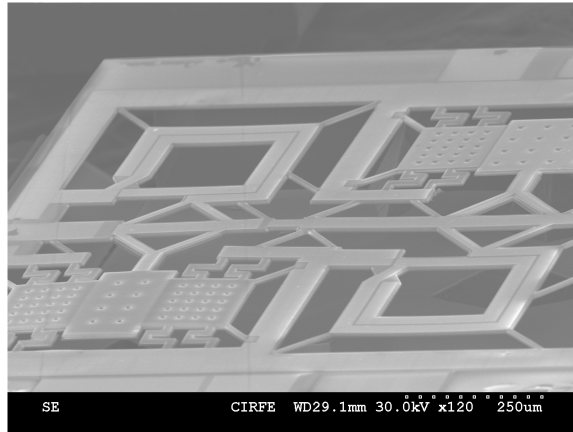
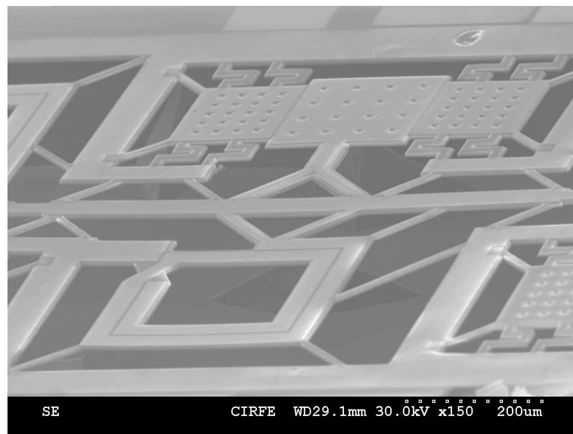


(c)

Figure 5.34 The SEM pictures of the fabricated BPF: (a) the BPF before applying the post-processing, (b) the BPF after the oxide and silicon dry etching (c) the BPF after the wet etching that include sacrificial layer and silicon etching.



(a)



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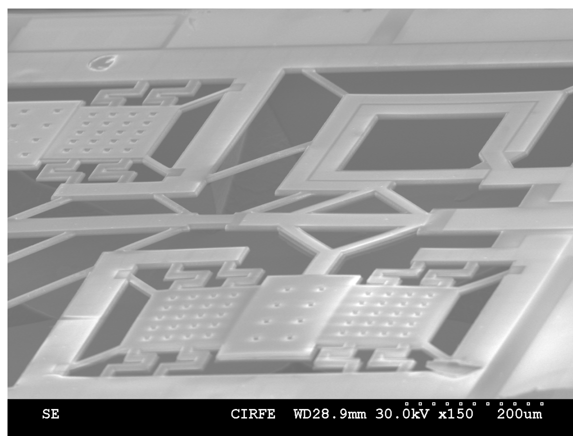
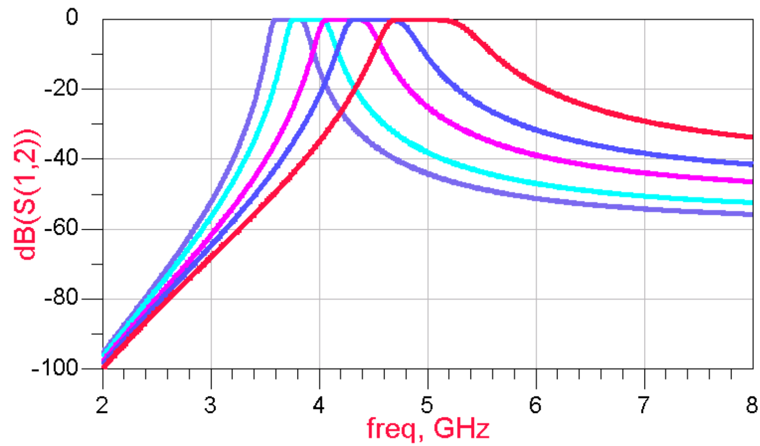
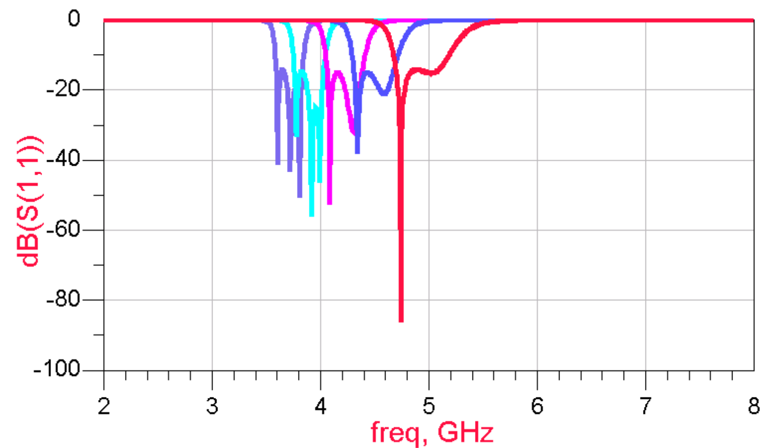


(c)

Figure 5.35 Zoomed SEM pictures of the fabricated BPF after applying the post-processing: (a) the first resonator of the BPF, (b) the second resonator, and (c) the third resonator.



(a)



(b)

Figure 5.36 The tuning range of the modeled tunable filter in hpADS: (a) the S_{12} response of the modeled filter showing a tuning from 5 GHz to 3.7 GHz, and (b) the S_{11} response of the modeled filter showing a tuning from 5 GHz to 3.7 GHz.

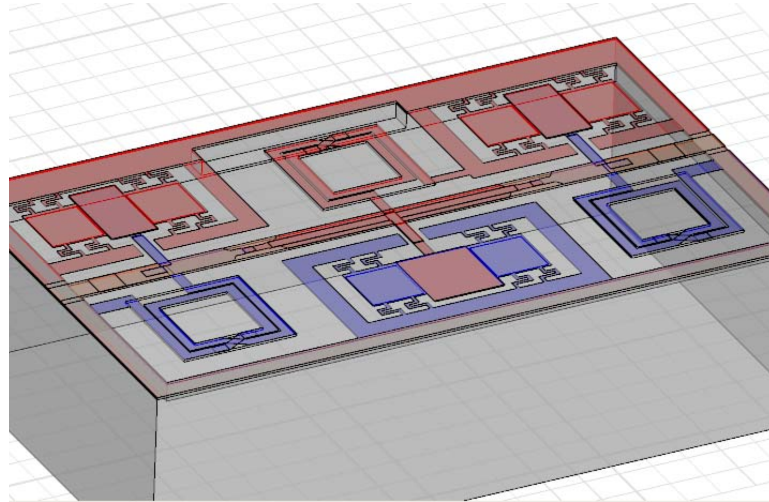


Figure 5.37 The 3-D structure of the 3 pole tunable filter built of the metalization of the 0.18 μm CMOS technology from TSMC in HFSS.

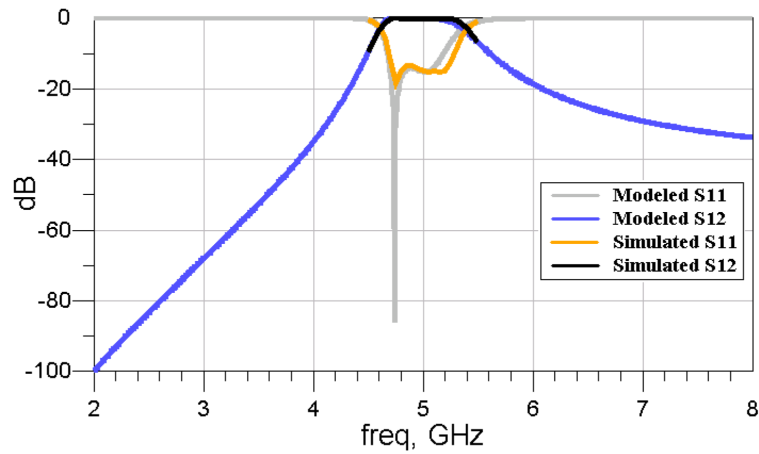


Figure 5.38 A comparison between the modeled and simulated return loss and insertion loss of the proposed BPF for the lossless case.

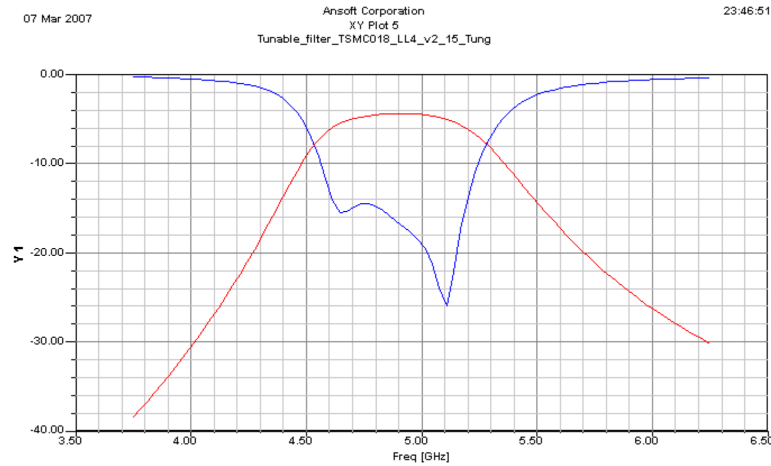


Figure 5.39 The simulated insertion and return losses after including the metallization and the substrate losses.

The tri-state parallel-plate capacitor exhibits three levels of measured capacitance whose values can be controlled by a set of beams. The proposed analog continuous capacitor does not suffer from the pull-in voltage effects and exhibits an almost linear measured tuning range of 115%. These MEMS capacitors exhibit the highest quality factor of MEMS variable capacitors built in CMOS.

Finite element method software, ANSYS is used to simulate the mechanical behavior of the curled-plate capacitors versus the applied voltage. A fit to measured curl up data is implemented to simulate the curl up at zero bias voltage. The ANSYS mechanical solution is coupled to an analysis, based on the method of moments to determine the capacitance value versus the voltage for the proposed curled-plate capacitors. The approach has provided theoretical results that are in good agreement with the measured data.

The post-processing technique is maskless and involves dry etching and wet etching stages. The proposed integrated MEMS/CMOS variable capacitors have the potential to be useful as tuning elements in compact RF subsystems such as impedance tuners, VCOs, and miniaturized integrated tunable filters for SoC.

A tunable band-pass filter that utilities a MEMS varactor in 0.18 μm is designed

and fabricated. The fabricated band pass filter of the third order has three parallel-plate MEMS variable capacitors that have their electrostatic actuators electrically isolated from the MEMS varactor while being mechanically connected.

Chapter 6

Conclusions

6.1 Thesis Contributions

The major contributions of the thesis can be summarized as follows:

Several configurations and novel topologies for analog continuous MEMS varactors are investigated, designed, fabricated and tested. A novel model for the two movable plate configuration is developed. This model is applied to reduce the actuation voltage by as much as 40%, compared with conventional MEMS varactors and capacitive switches. This leads to better reliable devices, since the contact forces and trapped charges are reduced significantly due to the decrease in the actuation voltages. The technique can be readily implemented to build a MEMS varactor and a capacitive switch where both plates can deform. The tuning capacitance ratio of the measured two movable-plate nitride-loaded capacitor is found to be between 250% and 280%. The proposed capacitor is built by the MetalMUMPs process. The other three configurations of the new variable capacitors are built by PolyMUMPs process with two sets of beams: guided beams and carrier beams. The carrier beams prevent the top plate from collapsing onto the bottom plate by imposing an additional restoring force on the capacitor with the carrier beams. Moreover, the arrays of carrier beams extends the tuning capacitance ratio further by imposing a gradual restoring force. The

equivalent spring constant of the new suspension system creates a nonlinear restoring force that pushes the "pull-in" voltage point farther. The measured tuning capacitance ratios of these three capacitors are 410%, 400% and 470% respectively, which far exceeds the 50% tuning range of traditional parallel-plate MEMS capacitors.

Two linear analog continuous MEMS variable capacitors with a high tuning capacitance ratio are designed, fabricated, and tested. The fifth capacitor combines a novel vertical comb actuator with a conventional parallel-plate variable capacitor. The top and the bottom electrodes of the comb actuators are suspended and capable of attracting each other. The capacitor exhibits a measured tuning capacitance ratio of 7:1 (600%) and built by the MetalMUMPs process. The sixth capacitor employs the residual stress, Atomic Layer Deposition (ALD) and bulk etching of the silicon substrate below the capacitor to come up with a novel topology of a MEMS capacitor that exhibits a linear capacitance change in term of the *dc* bias voltage. The measured tuning capacitance ratio of this capacitor is 5.7 (470%). The suspended spring constant that comes from the unanchored cantilever beams prevents the top plate of the capacitor from collapsing on the bottom plate, and as a result, avoids the pull-in phenomenon.

Two novel structures of curled-plate MEMS variable capacitors, integrated monolithically in CMOS technology, are proposed: a tri-state curled-plate capacitor and a analog continuous curled-plate capacitor. Both capacitors exploit the residual stress in the deposited layers in CMOS technology. The seventh capacitor, tri-state parallel-plate capacitor, exhibits three levels of measured capacitance whose values can be controlled by a set of beams, and exhibits a tuning capacitance ratio of 460%. The eighth proposed capacitor is an analog continuous capacitor exhibiting a linear measured tuning range of 115% with an eliminated pull-in voltage. These MEMS capacitors demonstrate the highest quality factor of MEMS variable capacitors built in CMOS. The measured quality factor is in excess of 300 at 1.5 GHz.

A tunable band-pass filter that utilities a MEMS varactor in 0.18 μm is designed and fabricated. This filter is of the third order that has three parallel-plate MEMS

variable capacitors. Appendix B summarizes the performance of our proposed MEMS varactors in comparison with commercially available varactor diodes.

6.2 Future Work

The newly developed MEMS variable capacitors in Chapter 5 should be tested in terms of their thermal stability and reliability issues due to the dielectric charging. Also, the hysteresis needs to be carefully investigated for the digital tri-state type capacitor.

The novel post-processing technique, proposed in this thesis, reduces the CMOS occupied area. This allows the realization of miniature micro-scale RF passive devices such as varactors, capacitive switches, and tunable filters. The miniaturization achieved with the integration of MEMS sensors and actuators offers exciting possibilities for building an intelligent SoC. The evolving Nanotechnology which uses MEMS as an interface can lead to even higher levels of monolithic integration between nano-scale MEMS and CMOS electronics.

These systems have low mass, high-speed, small occupied area and a low power consumption. Using integrated MEMS devices in CMOS technology, intelligent system-on-chip (SoC) transceivers can be built by integrating MEMS sensors and actuators, that exhibit a large stroke and high tuning speed, with CMOS electronics on one chip.

The use of the proposed MEMS/CMOS technique reduces the area by developing varactors with parallel-plate actuators. This allows the realization of miniature micro-scale RF passive devices such as varactors, capacitive switches, and tunable filters.

To build intelligent SoC systems, first, intelligent MEMS, long stroke, linear actuators should be developed by using feedback control integrated into CMOS platforms. In order to achieve the targeted repeatability, the feedback control design issues in those actuators are critical. Secondly, highly linear sensors should be developed. Thirdly, the electronics of the transceiver with the developed sensors and actuators should be used to build the intelligent SoC transceiver. Finally, intelligent SoC in RF

and biomedical applications should be used in the following applications:

1. Phase shifters and impedance tuners

2. Superconductive MEMS varactors and switches

3. Tunable Bandpass filters (BPF)

4. Chemical analysis

5. Embedded biomedical systems: pace-making and deep brain stimulation

6. Miniaturized endoscope equipment: micro-level surgical

Bibliography

[1] A. Dec and K. Suyama, "Micromachined electro-mechanically tunable capacitors and their applications to rf ic's," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 46, no. 12, pp. 2587–2596, Dec. 1998.

[2] J. Zou, C. Liu, J. Schutt-Aine, J. Chen, and S.-M. Kang, "Development of a wide tuning range mems tunable capacitor for wireless communication systems," in *Electron Devices Meeting, 2000. IEDM Technical Digest. International*, 10-13 Dec. 2000, pp. 403–406.

[3] D. Peroulis and L. Katehi, "Electrostatically-tunable analog rf mems varactors with measured capacitance range of 300%," in *Microwave Symposium Digest, 2003 IEEE MTT-S International*, vol. 3, 8-13 June 2003, pp. 1793–1796.

[4] N. Hoivik, M. Michalicek, Y. Lee, K. Gupta, and V. Bright, "Digitally controllable variable high-q mems capacitor for rf applications," in *Microwave Symposium Digest, 2001 IEEE MTT-S International*, vol. 3, 20-25 May 2001, pp. 2115–2118vol.3.

[5] F. Faheem, N. Hoivik, Y. Lee, and K. Gupta, "Post-enabled precision flip-chip assembly for variable mems capacitor," in *Microwave Symposium Digest, 2003 IEEE MTT-S International*, vol. 3, 8-13 June 2003, pp. 1927–1930vol.3.

[6] N. Hoivik, J. Elam, S. George, K. Gupta, V. Bright, and Y. Lee, "Atomic layer deposition (ald) technology for reliable rf mems," in *Microwave Symposium Digest, 2002 IEEE MTT-S International*, vol. 2, 2-7 June 2002, pp. 1229–1232.

[7] S. P. J. Jason Yao and J. DeNatale, "High tuning-ratio mems-based tunable capacitors for rf communications applications," in *Technical Digest-Solid State Sensor and Actuator Workshop*, Hilton Head Island, SC, June 1998, pp. 124–127.

[8] A. Oz and G. Fedder, "CMOS-compatible RF-MEMS tunable capacitors," in *Microwave Symposium Digest, 2003 IEEE MTT-S International*, vol. 1, 8-13 June 2003, pp. A97–A100.

[9] G. Fedder, S. Santhanam, M. Reed, S. Eagle, D. Guillou, M.-C. Lu, and L. Carley, "Laminated high-aspect-ratio microstructures in a conventional cmos process," in *Micro Electro Mechanical Systems, 1996, MEMS '96, Proceedings. 'An Investigation of Micro Structures, Sensors, Actuators, Machines and Systems'. IEEE, The Ninth Annual International Workshop on*, 11-15 Feb. 1996, pp. 13–18.

[10] G. Fedder and T. Mukherjee, "Tunable rf and analog circuits using on-chip mems passive components," in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, 6-10 Feb. 2005, pp. 390–391Vol.1.

[11] S. Fouladi, M. Bakri-Kassem, and R. R. Mansour, "An integrated tunable band-pass filter using mems parallel-plate variable capacitors implemented with 0.35um cmos technology," in *Microwave Symposium, 2007. IEEE/MTT-S International*, 3-8 June 2007, pp. 505–508.

[12] C. Liechti and G. Epprecht, "Controlled wideband differential phase shifters using varactor diodes," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 15, no. 10, pp. 586–589, Oct. 1967.

[13] B. Ulriksson, "A low-cost continuous l-band phase shifter/attenuator for low power applications," in *European Microwave Conference, 1979. 9th*, Oct. 1979, pp. 475–479.

[14] F. Chen, J. Brotz, U. Arslan, C.-C. Lo, T. Mukherjee, and G. Fedder, "Cmos-mems resonant rf mixer-filters," in *Micro Electro Mechanical Systems, 2005. MEMS 2005. 18th IEEE International Conference on*, 30 Jan.-3 Feb. 2005, pp. 24–27.

[15] D. Ramachandran, A. Oz, V. Saraf, G. Fedder, and T. Mukherjee, "Mems-enabled reconfigurable vco and rf filter," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2004. Digest of Papers. 2004 IEEE*, 6-8 June 2004, pp. 251–254.

[16] Y.-C. W. I.-C. O. K. Hung, C.-M. Ho, "High-q capacitors implemented in a cmos process for low-power wireless applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 46, no. 5, pp. 505–511, May 1998.

[17] J. A. Shu, Yong-Hui. Navarro and K. Chang, "Electronically switchable and tunable coplanar waveguide-slotline band-pass filters," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 36, no. 3, pp. 548–554, March 1991.

[18] A. Presser, "High-speed, varactor-tunable microwave filter element," in *Microwave Symposium Digest, 2003 IEEE MTT-S International*, vol. 79, no. 1, April 1979, pp. 416–418.

[19] S. Saeedi, T. Heidari, M. Hafezi, and J. Baabuei, "Design, simulation and fabrication of a varactor tunable combline microwave filter," in *Microwave Conference Proceedings, 2005. APMC 2005. Asia-Pacific Conference Proceedings*, vol. 1, 4-7 Dec. 2005, p. 3pp.

[20] A. S. D.A. Koester, R. Mahadevan and K. Markus, *SmartMUMPs Design Handbook Including MUMPs Introduction and Design Rules*, 4th ed., Research Triangle Park, N.C.: MEMS Technology Applications Center, July 1996.

[21] [Online]. Available: http://www.sonnetusa.com/

[22] G. Fedder, "Mems fabrication," in *Test Conference, 2003. Proceedings. ITC 2003. International*, vol. 1, Sept. 30-Oct. 2, 2003, pp. 691–698.

[23] I. Borwick, R.L., P. Stupar, J. DeNatale, R. Anderson, C. Tsai, and K. Garrett, "A high q, large tuning range, tunable capacitor for rf applications," in *Micro Electro Mechanical Systems, 2002. The Fifteenth IEEE International Conference on*, 20-24 Jan. 2002, pp. 669–672.

[24] I. Borwick, R.L., P. Stupar, J. DeNatale, R. Anderson, and R. Erlandson, "Variable mems capacitors implemented into rf filter systems," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 51, no. 1, pp. 315–319, Jan. 2003.

[25] S. J. Allen Cowen, Ramaswamy Mahadevan and B. Hardy, *MetalMUMPs Design Handbook, a MUMPs process*, 2nd ed., MEMSCAP.

[26] [Online]. Available: http://www.coventor.com/

[27] M. Bakri-Kassem and R. Mansour, "Two movable-plate nitride-loaded mems variable capacitor," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 52, no. 3, pp. 831–837, March 2004.

[28] T. Tsang and M. El-Gamal, "Very wide tuning range micro-electromechanical capacitors in the mumps process for rf applications," in *VLSI Circuits, 2003. Digest of Technical Papers. 2003 Symposium on*, 12-14 June 2003, pp. 33–36.

[29] J.-M. Kim, S. Lee, J.-M. Kim, C.-W. Baek, Y. Kwon, and Y.-K. Kim, "Mechanically reliable mems variable capacitor using single crystalline silicon (scs) structure," in *Solid-State Sensors, Actuators and Microsystems, 2005. Digest of Technical Papers. TRANSDUCERS '05. The 13th International Conference on*, vol. 1, 5-9 June 2005, pp. 1080–1083Vol.1.

[30] M. Bakri-Kassem and R. Mansour, "An improved design for parallel plate mems variable capacitors," in *Microwave Symposium Digest, 2004 IEEE MTT-S International*, vol. 2, 6-11 June 2004, pp. 865–868Vol.2.

[31] S. D. Senturia, *Microsystem Design*, F. Printing, Ed. Kluwer Accademic Publishers, 2002.

[32] [Online]. Available: http://www.softmems.com/

[33] T. Rijks, J. van Beek, P. Steeneken, M. Ulenaers, J. De Coster, and R. Puers, "Rf mems tunable capacitors with large tuning ratio," in *Micro Electro Mechanical Systems, 2004. 17th IEEE International Conference on. (MEMS)*, 2004, pp. 777–780.

[34] M. Bakri-Kassem and R. Mansour, "High tuning range parallel plate mems variable capacitors with arrays of supporting beams," in *Micro Electro Mechanical Systems, 2006. MEMS 2006 Istanbul. 19th IEEE International Conference on*, 22-26 Jan. 2006, pp. 666–669.

[35] H. Nguyen, D. Hah, P. Patterson, R. Chao, W. Piyawattanametha, E. Lau, and M. Wu, "Angular vertical comb-driven tunable capacitor with high-tuning capabilities," *Microelectromechanical Systems, Journal of*, vol. 13, no. 3, pp. 406–413, June 2004.

[36] G. Rebeiz, *RF MEMS: Theory, Design, and Technology*, 1st, Ed. John Wiley & Sons , Ltd, 2003.

[37] F. Faheem, K. Gupta, and Y.-C. Lee, "Flip-chip assembly and liquid crystal polymer encapsulation for variable mems capacitors," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 51, no. 12, pp. 2562–2567, Dec. 2003.

[38] M. Bakri-Kassem and R. Mansour, "A high-tuning-range mems variable capacitor using carrier beams," *Electrical and Computer Engineering, Canadian Journal of*, vol. 31, no. 2, pp. 89–95, Spring 2006.

[39] C. Tsai, P. Stupar, I. Borwick, R.L., M. Pai, and J. DeNatale, "An isolated tunable capacitor with a linear capacitance-voltage behavior," in *TRANSDUCERS,*

Solid-State Sensors, Actuators and Microsystems, 12th International Conference on, 2003, vol. 1, 8-12 June 2003, pp. 833–836vol.1.

[40] J. Muldavin, C. Bozler, S. Rabe, and C. Keast, “Large tuning range analog and multi-bit mems varactors,” in *Microwave Symposium Digest, 2004 IEEE MTT-S International*, vol. 3, 6-11 June 2004, pp. 1919–1922Vol.3.

[41] N. Hoivik, J. Elam, R. Linderman, V. Bright, S. George, and Y. Lee, “Atomic layer deposition of conformal dielectric and protective coatings for released micro-electromechanical devices,” in *Micro Electro Mechanical Systems, 2002. The Fifteenth IEEE International Conference on*, 20-24 Jan. 2002, pp. 455–458.

[42] M.-A. Eyoum, N. Hoivik, C. Jahnes, J. Cotte, and X.-H. Liu, “Analysis and modeling of curvature in copper-based mems structures fabricated using cmos interconnect technology,” in *Solid-State Sensors, Actuators and Microsystems, 2005. Digest of Technical Papers. TRANSDUCERS ’05. The 13th International Conference on*, vol. 1, 5-9 June 2005, pp. 764–767Vol.1.

[43] S. Fouladi, M. Bakri-Kassem, and R. Mansour, “Suspended on-chip rf mems components fabricated using polymumps technology,” *Electrical and Computer Engineering, Canadian Journal of*, vol. 31, no. 2, pp. 105–109, Spring 2006.

[44] J. Rizk and G. Rebeiz, “Digital-type rf mems switched capacitors,” in *Microwave Symposium Digest, 2002 IEEE MTT-S International*, vol. 2, 2-7 June 2002, pp. 1217–1220.

[45] D. Mercier, K. Van Caekenberghe, and G. Rebeiz, “Miniature rf mems switched capacitors,” in *Microwave Symposium Digest, 2005 IEEE MTT-S International*, 12-17 June 2005, p. 4pp.

[46] S. He and R. Ben Mrad, “A novel mems tunable capacitor,” in *MEMS, NANO and Smart Systems, 2004. ICMENS 2004. Proceedings. 2004 International Conference on*, 25-27 Aug. 2004, pp. 550–554.

[47] J. De Coster, R. Puers, H. Tilmans, J. van Beek, and T. Rijks, "Variable rf mems capacitors with extended tuning range," in *TRANSDUCERS, Solid-State Sensors, Actuators and Microsystems, 12th International Conference on, 2003*, vol. 2, 8-12 June 2003, pp. 1784–1787vol.2.

[48] A. Oz and G. Fedder, "Rf cmos-mems capacitor having large tuning range," in *TRANSDUCERS, Solid-State Sensors, Actuators and Microsystems, 12th International Conference on, 2003*, vol. 1, 8-12 June 2003, pp. 851–854vol.1.

[49] V. Saraf, D. Ramachandran, A. Oz, G. Fedder, and T. Mukherjee, "Low-power lc-vco using integrated mems passives," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2004. Digest of Papers. 2004 IEEE*, 6-8 June 2004, pp. 579–582.

[50] H. Xie, Y. Pan, and G. Fedder, "A cmos-mems mirror with curled-hinge comb drives," *Microelectromechanical Systems, Journal of*, vol. 12, no. 4, pp. 450–457, Aug. 2003.

[51] G. Fedder, S. Santhanam, M. Reed, S. Eagle, D. Guillou, M.-C. Lu, and L. Carley, "Laminated high-aspect-ratio microstructures in a conventional cmos process," in *Micro Electro Mechanical Systems, 1996, MEMS '96, Proceedings. 'An Investigation of Micro Structures, Sensors, Actuators, Machines and Systems'. IEEE, The Ninth Annual International Workshop on*, 11-15 Feb. 1996, pp. 13–18.

[52] C.-T. Ko, J.-P. Wu, W.-C. Wang, C.-H. Huang, S.-H. Tseng, Y.-L. Chen, and M.-C. Lu, "A highly sensitive cmos-mems capacitive tactile sensor," in *Micro Electro Mechanical Systems, 2006. MEMS 2006 Istanbul. 19th IEEE International Conference on*, 22-26 Jan. 2006, pp. 642–645.

[53] K. Williams, K. Gupta, and M. Wasilik, "Etch rates for micromachining processing-part ii," *Microelectromechanical Systems, Journal of*, vol. 12, no. 6, pp. 761–778, Dec. 2003.

[54] C.-L. Dai, "In situ electrostatic microactuators for measuring the youngs modulus of cmos thin films," *Journal of Micromechanics and Microengineering*, vol. 13, pp. 563–567, Sept. 2003.

[55] R. F. Harrington, *Field Computation by Moment Methods Book*, 1st, Ed. John Wiley & Sons Canada, Ltd., Aug 30 2001.

[56] Y. Yoon and B. Kim, "A new formula for effective dielectric constant in multi-dielectric layer microstrip structure," in *Electrical Performance of Electronic Packaging, 2000, IEEE Conference on.*, 23-25 Oct. 2000, pp. 163–167.

[57] G. Zhang, H. Xie, L. de Rosset, and G. Fedder, "A lateral capacitive cmos accelerometer with structural curl compensation," in *Micro Electro Mechanical Systems, 1999. MEMS '99. Twelfth IEEE International Conference on*, 17-21 Jan. 1999, pp. 606–611.

[58] R. Legtenberg, J. Gilbert, S. Senturia, and M. Elwenspoek, "Electrostatic curved electrode actuators," *Microelectromechanical Systems, Journal of*, vol. 6, no. 3, pp. 257–265, Sept. 1997.

[59] L. C. Wei, A. Mohammad, and N. Kassim, "Analytical modeling for determination of pull-in voltage for an electrostatic actuated mems cantilever beam," in *Semiconductor Electronics, 2002. Proceedings. ICSE 2002. IEEE International Conference on*, 19-21 Dec. 2002, pp. 233–238.

[60] Y.-C. Hu, "Closed form solutions for the pull-in voltage of micro curled beams subjected to electrostatic loads to electrostatic loads," *Journal of Micromechanics And Microengineering*, vol. 16, pp. 648–655, March. 2006.

[61] G. K. Fedder, "Simulation of microelectromechanical systems," Ph.D. dissertation, University of California at Berkeley, 1994.

Appendix A

Thesis Publication List (As of Dec. 2007)

Refereed Journal Papers:

1. M. Bakri-Kassem and R. Mansour "Linear Bi-Layer ALD Coated MEMS Varactor with High Tuning Capacitance Ratio" *Microelectromechanical Systems, Journal of*, Submitted.

2. M. Bakri-Kassem, S. Fouladi, and R. Mansour "Novel High-Q MEMS Curled-Plate Variable Capacitors Fabricated in 0.35 μm CMOS Technology" *IEEE MTT Trans. Microwave Theory & Tech.*, Accepted (12 pages).

3. M. Bakri-Kassem and R. Mansour, "A high-tuning-range mems variable capacitor using carrier beams," *Electrical and Computer Engineering, Canadian Journal of*, vol. 31, no. 2, pp. 89-95, March 2006.

4. S. Fouladi, M. Bakri-Kassem, and R. Mansour, "Suspended on-chip rf mems components fabricated using polymumps technology," *Electrical and Computer Engineering, Canadian Journal of*, vol. 31, no. 2, pp. 105-109, March 2006.

5. M. Bakri-Kassem and R. Mansour "Two Movable Plate Nitride Loaded MEMS Variable Capacitor" *IEEE MTT Trans. Microwave Theory Tech.* Vol. 52, No. 3, pp. 831-837, March 2004.

Refereed Conference Papers:

1. M. Bakri-Kassem, R. R. Mansour "A Parallel Plate MEMS Variable Capacitor with Vertical Thin Film Comb Actuators ", *IEEE Microwave Conference, 2007. 37th European*, 8-12 Oct. 2007, Munich, Germany, pp. 1349-1352.

2. S. Fouladi, M. Bakri-Kassem and R. R. Mansour "An Integrated Tunable Band-Pass Filter Using MEMS Parallel-Plate Variable Capacitors Implemented with 0.35 μm CMOS Technology", IEEE MTT-S, 105–109 June 2007, Hawaii, USA, pp. 505-508.

3. M. Bakri-Kassem and R. Mansour, "High tuning range parallel plate mems variable capacitors with arrays of supporting beams", in Micro Electro Mechanical Systems, 2006. MEMS 2006 Istanbul, 19th IEEE International Conference on, 22–26 Jan. 2006, pp. 666-669.

4. M. Bakri-Kassem and Raafat Mansour "An Improved Design for Parallel Plate MEMS Variable Capacitors", *IEEE MTT-S Int. Microwave Symposium Digest*, Texas, USA, June 2004. pp. 865–868.

5. M. Bakri-Kassem, R. R. Mansour "Modeling, Design And Analysis Of The Two Movable Plate Nitride Loaded MEMS Variable Capacitor" *10th International Symposium on Antenna Technology and Applied Electromagnetics*, Ottawa, Canada. pp. 17–20. ANTEM 2004.

6. M. Bakri-Kassem and Raafat Mansour "The Design and Modeling of Wide Tuning Range MEMS Variable Capacitor for Wireless Applications", *Workshop on Nanotechnology and Microtechnology*, Damascus, Syria, Oct. 2003 (Best Paper)

7. R. R. Mansour, M. Bakri-Kassem, M. Daneshmand and N. Messiha "RF MEMS DEVICES " *The IEEE 2003 International Conference on MEMS, NANO, and Smart Systems*, Alberta, Canada, July 20–23, 2003 (INVITED)

8. M. Bakri-Kassem and Raafat Mansour "Two Movable Plate Nitride Loaded MEMS Variable Capacitor", *IEEE MTT-S Int. Microwave Symposium Digest*, Philadelphia, USA June 2003. pp.483–486.

9. M. Bakri-Kassem, R. R. Mansour "Two Level Beam MEMS Variable Capacitor and its Characterizations", *9th International Symposium on Antenna Technology and Applied Electromagnetics*, Montreal, Canada, pp. 596–599, ANTEM 2002.

Posters:

1. M. Bakri-Kassem, and R. Mansour "A Parallel Plate MEMS Variable Capacitor with Vertical Thin Film Comb Actuators" Canadian Workshop on MEMS, Ottawa, August 2007.

2. S. Fouladi, M. Bakri-Kassem, and R. Mansour "CMOS-MEMS Post-Processing Technique Developed for Integrated RF MEMS Devices", *Canadian Workshop on MEMS*, Ottawa, August 2007.

3. M. A. E. Mahmoud, M. Bakri-Kassem, E.F. El-Saadany and R.R. Mansour (2007) "Surface Micro-machined Capacitive Transducer for Electrostatic Vibration Energy Harvesters", *Canadian Workshop on MEMS*, Ottawa, August 2007.

4. M. Bakri-Kassem, and R. Mansour "A High Tuning Range MEMS Variable Capacitor Using Carrier Beams", *Canadian Workshop on MEMS*, Ottawa, August 2005.

5. M. Bakri-Kassem, R. Mansour "A Wide Tuning Range MEMS Variable Capacitor" *Canadian Workshop on MEMS*, Ottawa, August 2003.

6. M. Daneshmand, D. Yan, M. Bakri-Kassem, M. Motiee, R. Mansour, "RF MEMS For Wireless Communication System", *CITO Innovators Showcase*, Toronto, Ontario, Nov. 2004, (Best Student Presentation Award).

7. M. Bakri-Kassem, R. R. Mansour "A Novel Two Level Beam MEMS Variable Capacitor and Its Characterization", *Centre for Research in Earth and Space Technology CRESTech*, Toronto, Oct. 2002.

Appendix B

A Comparison Between Varactor Diodes and MEMS Diodes

Table B.1 A summary of the Diode Varactors available in the market

Model Number	Manufacturer	Cap. (pF) MIN	Cap. Ratio	Q	Package Size
ATV1000	ASI	2.7@ 1MHz @4 V	4.5	2000 @50MHz@4V	SOT-23 2.1x2.8 mm
MA46600	M/A Comm	0.3	1.9	8000 @50MHz@4V	SOD-323 1.9x1.45 mm
MP6301	M-Pulse	0.4@1MHz @4 V	5@1MHz @0-30 V	5000 @50MHz	Chip 0.038 x 0.038 mm
BB141	Philips	4	1.76	211@470MHz @1V	SOD-523 1.3x0.9 mm
SMTV3001	Metelics	1	3.5	3000 @50MHz@4V	SOD-323 2.3x0.15 mm
MGV-075-10	Metelics	0.5@4V	2.8 (2-12 V)	4000 @50MHz@4V	1.078x1.25 mm
1SV147	Toshiba	11.7	2.6	353@50MHz @C=30pF	1.078x1.25 mm N/A
GC1500A	Microsemi	0.4	4.2	5000 @50MHz	Style 30 Package
STVD901J	STMicro-electronics	4@0.25V	2	1273 @100MHz@1V	SOD-323 1.11x2.3 mm
MV20001	Microwave Device Tech.	0.3	2.4	8000 @50MHz@4V	Chip 0.028 x0.028 mm
BBY53-03W	Siemens	2.4	2.2	78 @1GHz@1V	SOD-323 1.25x2.5 mm

Model Number	Manufacturer	Cap. (pF) MIN	Cap. Ratio	Q	Package Size
BBY53	Infineon	2.4	2.2	60 @1GHz@1V	SOT-23 3x3.3 mm
HVC355B	Renesas	2.55	2.2	80 @470MHz@1V	UFP 0.8x1.6 mm
GMV7821 -000	SkyWorks	0.4	3.3	4000 @50MHz@4V	Chip 0.25 x0.25 mm
BBY31	Zetex	1.8	5	31 @470MHz@9pF	SOT-23
HVC355B	Aeroflex	0.4	3.5	6300 @50MHz@4V	Chip 0.018 x0.018 mm

Table B.2 A summary of the proposed MEMS Varactors that are reported in this thesis

MEMS Parallel Plate Capacitors	Foundry	Cap. (pF) MIN	Cap. Ratio	Q @0V	Expected Q, Same Thickness but Different Materials
Two movable plate nitride loaded capacitor (cap.# 1)	MEMSCAP USA	2	3.8 (280%)	15 @1GHz	400@1GHz
Carrier beam capacitor (cap.# 2)	MEMSCAP USA	2	3.8 (280%)	15 @1GHz	400@1GHz

MEMS Parallel Plate Capacitors	Foundry	Cap. (pF) MIN	Cap. Ratio	Q @0V	Expected Q, Same Thickness but Different Materials
Two movable plate nitride loaded capacitor (cap.# 1)	MEMSCAP USA	2	3.8 (280%)	15 @1GHz	400@1GHz using gold
Carrier beam capacitor (cap.# 2)	MEMSCAP USA	1.7	5 (400%)	14 @1GHz	300@1GHz using gold
Arrays of carrier beams capacitor (cap.# 3&4)	MEMSCAP USA	1.2	5.7 (470%)	15 @1GHz	500@1GHz using gold
Tri-state MEMS/CMOS Digital type	0.35 μm TSMC	0.3	5.6 (460%)	300 @1.5GHz @52V	-
Analog continuous MEMS/CMOS Analog type	0.35 μm TSMC	0.8	2.15 (115%)	300 @1.5GHz @0V	-