Novel MEMS Tunable Capacitors with Linear Capacitance-Voltage Response Considering Fabrication Uncertainties

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisiosn, as accepted by my examiners.

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Abstract

Electrostatically actuated parallel-plate MEMS tunable capacitors are desired elements for different applications including sensing, actuating and communications and RF (radio frequency) engineering for their superior characteristics such as quick response, high Q-factor and small size. However, due to the nature of their coupled electrostatic-structural physics, they suffer from low tuning range of 50% and have nonlinear capacitance-voltage (C-V) responses which are very sensitive to the voltage change near pull-in voltage. Numerous studies in the literature introduce new designs with high tunability ranging from 100% to over 1500%, but improvement of the nonlinearity and high sensitivity of the capacitor response have not received enough attention.

In this thesis, novel highly tunable capacitors with high linearity are proposed to reduce sensitivity to the voltage changes near pull-in. The characteristic equations of a perfectly linear capacitor are first derived for two- and three-plate capacitors to obtain insight for developing linear capacitance-voltage responses. The devices proposed in this research may be classified into three categories: designs with nonlinear structural rigidities, geometric modifications and flexible moving electrodes.

The concept of nonlinear supporting beams is exploited to develop parallel-plate capacitors with partially linear C-V curves. Novel electrodes with triangular, trapezoidal, butterfly, zigzag and fishbone shapes and structural/geometric nonlinearities are used to increase the linearity and tuning ratio of the response. To investigate the capacitors' behavior, an analytical approximate model is developed which can drastically decrease the computation time. The model is ideal for early design and optimization stages. Using this model, design variables are optimized for maximum linearity of the C-V responses. The results of the proposed modeling approach are verified by ANSYS® FEM simulations and/or experimental data. When the fabrication process has dimensional limitations, design modifications and geometric enhancements are implemented to improve the linearity of the C-V response. The design techniques proposed in this thesis can provide tunabilities ranging from 80% to over 350% with highly linear regions in resulting C-V curves. Due to the low sensitivity of the capacitance to voltage changes in new designs, the entire tuning range is usable.

Furthermore, the effect of fabrication uncertainties on parallel-plate capacitors performance

is studied and a sensitivity analysis is performed to find the design variables with maximum impact on the C-V curves. An optimization method is then introduced to immunize the design against fabrication uncertainties and to maximize the production yield for MEMS tunable capacitors. The method approximates the feasible region and the probability distribution functions of the design variables to directly maximize the yield. Numerical examples with two different sets of design variables demonstrate significant increase in the yield. The presented optimization method can be advantageously utilized in design stage to improve the yield without increasing the fabrication cost or complexity.

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To my father

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Chapter 1

Introduction

1.1 Overview

MEMS-based capacitive elements have a wide range of applications from medical research to communication engineering. They are also used as sensors to measure different parameters, such as chemical properties [4], displacement and force [5, 6, 7]. Among capacitive devices, tunable capacitors are the most commonly used ones in RF integrated circuits like tunable filter and oscillators. These elements have superior characteristics such as simple and small structure, quick response and low energy consumption. However, they suffer from low tunability up to 50% due to structural instability at pull-in and also have sensitive capacitance-voltage (C-V) responses near their pull-in.

Although extensive research works have been dedicated to the improvement of tuning ratio [8, 9, 10], due to the nature of such capacitors, they exhibit high sensitivities and the "quality" of their responses has not received enough attention. Therefore, the enhancement of the C-V responses in different ways, including linearization of the curves or reduction of the high sensitivity of the responses near pull-in, is a valuable task in development of tunable capacitors.

1.2 Motivation

This research is motivated by the fact that the designs introduced in the literature provide high tuning ratio, but their responses are very sensitive to the voltage changes near pull-in which in

turn divides the C-V response into tuning and switching regions. Therefore, a major portion of the tunability, obtained in switching part, is lost. On the other hand, the applicability of linearly tunable capacitors, as efficient elements different circuits have not yet been well established. The existing designs have limited tunabilities with no systematic approach to improve the linearity or the tuning ratio of the response. The lack of analytical/numerical models in general limits the capabilities of MEMS tunable capacitors with high tunabilities and Q-factors already presented in the literature.

In addition to improvement of the quality of the capacitors response, analysis of fabrication uncertainties and their effects on the final product is of great importance and should be performed when a MEMS device is designed. For example, Chen *et al.* [11] reported different tunabilities ranging from 45% to 70% for five identical two-gap capacitors fabricated on the same chip. The discrepancy reported in this research highlights the importance of analysis of fabrication inaccuracies in development of tunable capacitors. A thorough understanding of dimensional inaccuracies and their effects on the performance of a tunable capacitor helps a designer to develop new devices with expected characteristics in mass production. The tolerances of different different steps in MEMS fabrication processes are relatively wide leading to a higher number of inacceptable devices in mass production. Tightening these tolerance ranges is not always possible due to technological challenges and this may severely affect the production yield. Although the analysis of fabrication inaccuracies and their effect on final output is a vital task and should be performed at the design stage, it has not been established for MEMS tunable capacitors. However, various such approaches have been developed in fabrication of ICs [12, 13, 14] which are similar to MEMS processes.

1.3 Objectives

The objectives of this research are categorized into three main topics:

Modelling of Electrostatically Actuated MEMS-based Elements: An approximate analytical model is developed to solve the governing coupled electrostatic-structural equations. The model takes into account the structural and geometric nonlinearities, including large deformations and mechanical contact, and numerically obtains the characteristic curves for different

structures. As a very time efficient formulation, the approximate model is ideal for investigation of the behavior of new electrostatically actuated elements and also for optimization purposes.

Development of Linearly Tunable Capacitors: Novel structures with different features including asymmetric geometries, flexible electrodes, geometric nonlinearity and dimensional optimization are utilized to enhance the capacitance-voltage response for different applications. The focus of this thesis is to increase response linearity and improve tunability of MEMS capacitors. The techniques presented in this thesis provide a powerful design tool to develop capacitors for applications. The new capacitors are developed, simulated and optimized for maximum linearity and tunability. The fabrication limitations are also taken into account to develop realistic designs. The capacitors are simulated by ANSYS® software for verification and whenever possible, the designs are modified to be fabricated with standard processes. The fabricated samples are tested to validate the results of analytical and FEM simulations and to evaluate the linearity of the measured C-V responses.

Analysis of Fabrication Uncertainties and Yield Maximization: Large dimensional tolerance ranges and limited fabrication processes drastically affect the performance of a MEMS device in mass production. To address these fabrication challenges, the effects of dimensional tolerances on the performance of parallel-plate capacitors are studied. The parameters which highly alter the C-V curve are extracted by performing a sensitivity analysis. A probabilistic design optimization method for tunable capacitors under existing fabrication uncertainties is introduced. The method maximizes the production yield in design stage without increasing the fabrication cost and complexity. The proposed method also finds the tolerance ranges corresponding to 100% yield which can be used for possible process modifications.

1.4 Thesis Organization

This thesis is divided into seven chapters. The present chapter is designed to outline the overview, motivations and objectives of this research. Chapter 2 presents a review of MEMS tunable capacitors introduced in the literature, the basic equations of a conventional parallel-plate tunable capacitor and the definitions used throughout the thesis.

A systematic structure-based design methodology is introduced through Chapters 3 to 5 to develop linearly tunable capacitors. In Chapter 3, an ideally linear capacitor is studied and based on its characteristics, a linearly tunable parallel-plate capacitor with geometric nonlinearity is developed. The capacitor is modeled by an approximate analytical formulation. The new design is then simulated using ANSYS®-based FEM to verify the results of the analytical model. Capacitors fabricated with PolyMUMPs are tested and the measured C-V responses validate that weak geometric nonlinearity enhances the performance of a parallel-plate capacitor.

Chapter 4 presents analytical models which simulate the behavior of asymmetric designs such as capacitors with trapezoidal and triangular electrodes. The geometric and structural asymmetries are used to modify conventional two-gap and three-plate tunable capacitors and to achieve high tunability and linearity. The results of numerical simulations display highly linear C-V responses with high tunabilities for capacitors designed for PolyMUMPs. The sensitivity of the response to the voltage change is reasonably low and therefore, the entire tuning range is usable.

In Chapter 5, structural nonlinearity and geometric modifications presented in Chapter 3 and 4 are combined to develop linear capacitors with flexible electrodes. The capacitors are divided into segmented-plate designs (with lumped flexibility) and flexible-plate structures (with continuous flexibility). A set of rigid or flexible steps placed between two electrodes generate structural nonlinearity and delay (or eliminate) the pull-in and provide a combination of high linearity and tunability. Geometric modifications leading to novel structures are also used to further enhance the linearity of the responses.

The fabrication uncertainties and their effects on the C-V curve are studied in Chapter 6. A sensitivity analysis is performed to find the design parameters which produce the highest deviations in the response. A probabilistic design optimization method for tunable capacitors is then introduced which maximizes the yield for a fabrication process with given tolerance ranges. The method can be implemented to variables with any distribution functions. Numerical simulations of a parallel-plate capacitor with two different sets of design parameters demonstrate the capabilities of the proposed method in improving the production yield prior to fabrication stage.

In Chapter 7, a summary of contributions achieved in this thesis is presented and some suggestions for future work are provided.

Chapter 2

Background and Literature Review

2.1 Definitions

2.1.1 Tuning Ratio, Tunability and Linear Tunability

Tuning ratio for a capacitor is the ratio of its maximum capacitance to its minimum capacitance, $\frac{C_{\max}}{C_{\min}}$. This parameter can also be expressed in percentage as:

$$\text{Tunability} = \frac{C_{\max} - C_{\min}}{C_{\min}} \times 100 \tag{2.1}$$

which is called tunability. The defined tunability may reach values higher than 100% as will be discussed later. In this thesis both tuning ratio and tunability are used to define the working range of a tunable capacitor. As it will be seen, for a conventional parallel-plate capacitor, tuning ratio and tunability are 1.5 and 50%, respectively.

For linear capacitors presented in this thesis the linear tunability is defined as the tunability in linear region as:

$$\text{Linear Tunability} = \left(\frac{C_{\max} - C_{\min}}{C_{\min}}\right)_{\text{in linear region}} \times 100 \tag{2.2}$$

2.1.2 Ideally Linear Capacitor

An ideally linear capacitor is assumed to have a mathematically (perfect) linear C-V response. Development of such capacitor may not be physically possible, however, its characteristics will

be used in this thesis to design capacitors with similar behavior and to improve the linearity and tunability of the device.

2.1.3 Linearity Factor

Developing a tunable capacitor with a perfect linear C-V response is very challenging, if not impossible. Thus the linear capacitors already presented in the literature or the ones proposed in this research exhibit different levels of linearization. To quantify the quality of linearization for a given C-V response, a linearity factor, LF, representing the coefficient of linear correlation between capacitance and voltage [15], is defined as:

$$LF = \frac{n\sum C_i V_i - \sum C_i \sum V_i}{\sqrt{\left[n\sum C_i^2 - (\sum C_i)^2\right]\left[n\sum V_i^2 - (\sum V_i)^2\right]}} \tag{2.3}$$

where each C_i is obtained at the corresponding applied voltage V_i and n is the number of voltage samples. The linearity factor is positive for ascending responses and negative for descending ones. Its magnitude varies between zero and one and $|LF|$ approaches one as the curve approaches a line,. The advantage of the defined LF is that it does not depend on the number of samples and changes only if there is a change in the shape of the response. For example, for a conventional parallel-plate tunable capacitor (Figure 2-2) the linearity factor is 0.865 and if the curve is stretched to the left- or right-hand-side, LF will remain constant.

2.1.4 Production Yield

production yield (or simply yield) is an index to quantify the quality of a production line, and is defined as the ratio of the number of devices which meet the product requirements to the total production.

$$\text{Yield} = \frac{\text{number of accepted devices}}{\text{number of total devices produced}} \tag{2.4}$$

Yield is often expressed in percent and the maximum yield for an ideal process is 100%.

Table 2.1: Material properties of polysilicon used in analytical and FEM simulations

Parameter	Value
Young's modulus	160 GPa
Poisson ratio	0.22

2.1.5 Material Properties

The capacitors presented in this thesis are designed for a polysilicon-base process such as PolyMUMPs. The mechanical properties of polysilicon used in analytical and FEM simulations in this thesis are presented in Table 2.1, and are extracted from PolyMUMPs Design Handbook [16]. Wherever applicable, the dimensional limitation are also based on design rules presented in [16].

2.2 MEMS Tunable Capacitors

Microelectromechanical systems (MEMS) have two main characteristics: they are made in micro scale and they combine electrical and mechanical properties to enhance or modify the performance of a device [17]. In the past decades, MEMS technology has rapidly grown and is expected to continue to do so in response to the market demand for such integrated circuits. MEMS devices are used in a wide range of applications from medical research [18, 19] to aerospace technology [20, 21, 22] and communication systems [9, 23, 24].

Electrostatically actuated capacitive elements are among the most common elements used in MEMS technology. A capacitive element consists of two conductive electrodes which can store electrical energy when a DC voltage is applied. If the distance between two electrodes or their effective area changes, the capacitance of the device changes accordingly. Capacitive elements are used as sensors to measure a wide range of chemical [25]and physical properties [4, 26, 27]. For example, they are utilized as pressure sensors [7, 28] or displacement sensors [5, 6, 29].

In addition to capacitive sensors and actuators, CMOS (Complementary Metal-Oxide-Semiconductor) compatible tunable capacitors with applications in communications and radio frequency (RF) engineering are well-known elements integrated in tunable filters and resonators [8, 9, 10]. A vast amount of research works have been dedicated to the performance enhancement

of such elements including increasing the maximum tunability and Q-factor [30, 31, 32].

Different actuation mechanisms, for instance, piezoelectric [33, 34, 35] or thermal [36, 37, 38] actuations are available for tunable capacitors, but the electrostatic actuation is the most common and convenient method due to its inherent speed and low power consumption [39, 40, 41]. Tunable capacitors are categorized based on their geometries into multi-finger [42, 43, 44] and parallel-plate [45, 46, 47], as displayed in Figures 2-1-a, 2-1-b and 2-1-c. In the first category, the capacitor consists of two electrodes with parallel fingers, where each pair of fingers forms a small capacitor. The gap between the fingers is constant and the actuation of the electrodes causes a relative displacement of two sets of fingers and changes the effective area of the small capacitors which consequently changes the total capacitance. These tunable capacitors, in general, have complex geometries and fabrication processes, higher maximum tunabilities and lower Q-factors comparing to parallel-plate capacitors. In a parallel-plate capacitor, the electrode surface area is constant and the capacitance changes as the distance between them varies:

$$C = \frac{\epsilon_r \epsilon_0 A}{d} \tag{2.5}$$

A is the area of the electrodes, d is the gap between them and ϵ_0 and ϵ_r are the permittivity of free space and the dielectric, respectively. For MEMS capacitors without dielectric layer $\epsilon_r = 1$.

An electrostatically actuated parallel-plate capacitor is constructed based on two electrodes moving relative to each other as the electrical potential is generated between them. The moving electrode is suspended by supporting beams (see Figure 2-1-c), and the electrostatic force, F_e, produced by electrical potential, V, is obtained from:

$$F_e = \frac{\epsilon_0 A V^2}{2d^2} \tag{2.6}$$

When a DC voltage is applied, the beams deform to balance the electrostatic force and therefore, the distance between electrodes changes. The equation of static equilibrium, in this case, is written as:

$$\frac{\epsilon_0 A V^2}{2d^2} - k_{eq}(d_0 - d) = 0 \tag{2.7}$$

where k_{eq} is the equivalent stiffness coefficient of all beams modeled as parallel springs and d_0

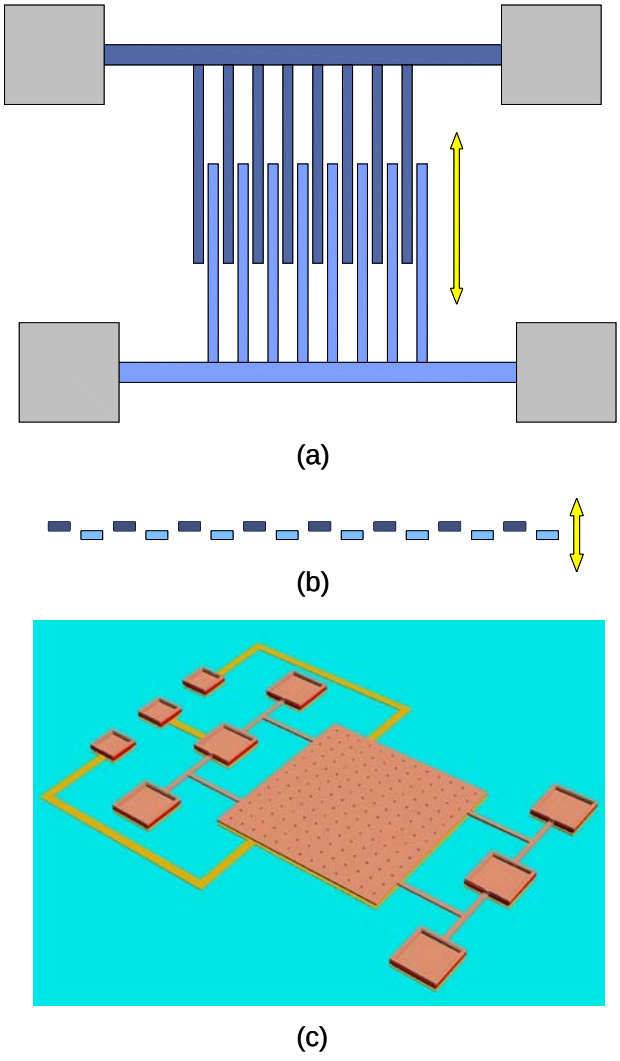


Figure 2-1: Finger-type capacitors with (a) inplane displacement and (b) out of plane displcamenets; (c) A parallel-plate tunable capacitor.

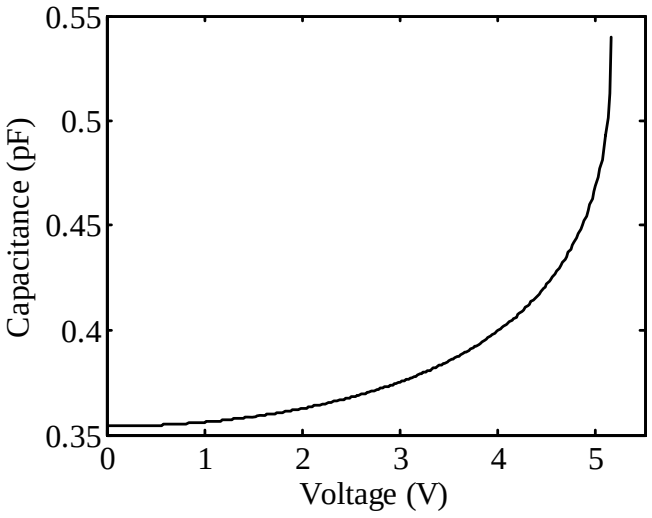


Figure 2-2: The capacitance-voltage (C-V) response of a MEMS parallel-plate tunable capacitor.

is the initial gap between two electrodes. Equation (2.7) is numerically solved for d at each bias voltage V and then the capacitance-voltage (C-V) curve is obtained from (2.5), as presented in Figure 2-2. A conventional parallel-plate capacitor has limited tunability of 50% at the pull-in voltage, where the electrostatic force overcomes the beams resistive force leading to the structural instability [48]. At this moment, the moving electrode collapses on the fixed one. For parallel-plate capacitors, pull-in occurs at $d = \frac{2}{3}d_0$ and the corresponding voltage is obtained from:

$$V_{pull-in} = \sqrt{\frac{8k_{eq}d_0^3}{27\epsilon_0 A}} \tag{2.8}$$

2.3 Highly Tunable Capacitors

Due to limited tuning ratio of conventional parallel-plate capacitors with electrostatic actuation, many research works have been focused on developing devices with higher tunabilities. One of the most common techniques is to adopt different gaps for the actuation and sense, as illustrated in Figure 2-3 [49, 50]. In this design, the distance between the sense electrodes is less than that of the actuation electrodes; therefore, at the pull-in voltage, the sense gap decreases to less

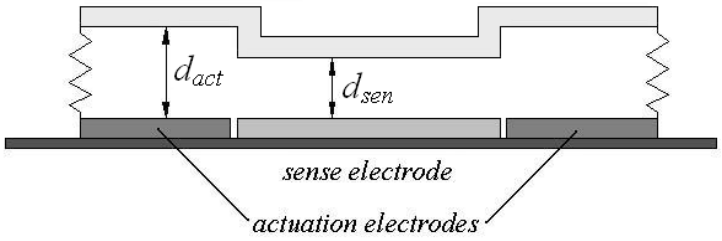


Figure 2-3: A two-gap capacitor; d_{sen} and d_{act} are the initial sense and actuation gaps, respectviely.

than 2/3 of its initial value leading to higher tunability. If the initial sense gap is chosen to be 1/3 of initial actuation gap, then the capacitor can provide infinite tuning ratio. Rijks *et al.* [1, 51] developed designs with tuning ranges of 700% to over 1700%. The C-V curves for these devices have three different regions as shown in Figure 2-4. In the first part before the pull-in voltage, capacitance increases because the air gap reduces gradually. At the pull-in, there is a jump in the capacitance, where the upper sense electrode collapses on the insulator layer. After this point, the capacitance increases linearly due to the deformations at the contact surface. Similar designs provide tunability as high as 500%, where the ratio of the actuation gap and sense gap are different [52]. The main drawback for these designs is the high sensitivity of their C-V curves to the voltage changes, especially at the pull-in voltage. At this point, the device behaves like a capacitive switch and loses its fine tunability. Larger sense gaps lead to less sensitive responses and lower tunabilities [11]. Similar concept (i.e., separation of actuation and sense electrodes) has been used in three-plate capacitors [45], where a higher tunability with a less sensitive C-V curve is achieved.

There are also other techniques to improve the maximum tunability. Bakri-Kassam and Mansour [46] proposed a 2-DOF varactor, where two electrodes can move relative to one another. In this design, the mobility of the second electrode changes the governing equations of the system. The capacitor has a 117% tunability before the pull-in voltage, and then, at pull-in voltage, a jump in the capacitance occurs. At the pull-in voltage, the electrode covered by a nitride layer touches the other one in a small area. After this point, further deformation of flexible electrode increases the capacitance in a linear fashion. The final tunability is as high as

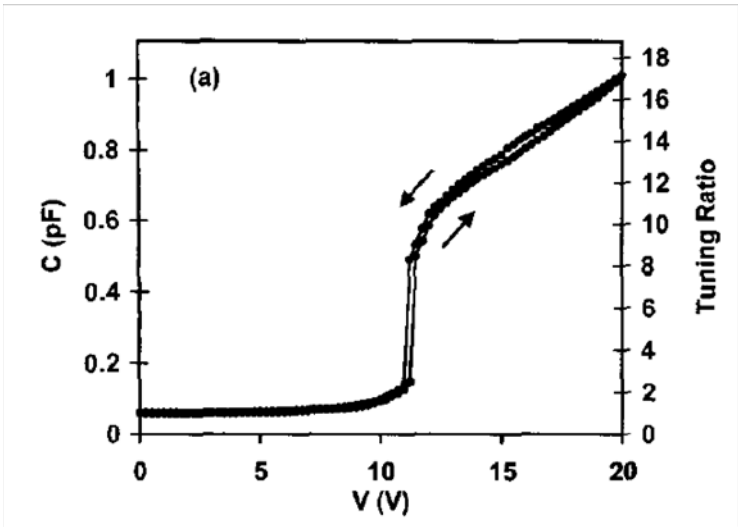


Figure 2-4: The C-V response of a Two-gap highly tunable capacitor [1].

280%. In this design, the instability (pull-in) happens at a tunability higher than 50% with no mathematical modeling or explanations. Additional tunability obtained after the pull-in is the result of the deformations of the contact surfaces, leading to a linear response in this region.

Some research works addressed the enhancement of structural stiffness to increase the tunability. Gray *et al*. [48] proposed a capacitor with two-layer supporting beams. The top layer is constructed with stressed hard gold, whereas the bottom layer is made of stress-free soft gold. Residual stress in the beam's layers causes stress gradients in the thickness and length of the cantilever beam. These gradients produce a pre-deformation in the beam that, in turn, increases the pull-in voltage. The profile of the top layer determines the maximum tunability. The experimental results demonstrated 30 to 45% improvement in the tunability. Bakri-Kassam and Mansour [47] also introduced a design with two sets of beams: attached beams and carrier beams. The attached beams hold the top plate up to the pull-in voltage, and then the moving electrode collapses on the the carrier beams which provide an additional resisting force until the second collapse occurs and additional beams improve the tunability to 410%. Adding an array of carrier beams under the supporting beams improves the tunability and generates a linear region at higher voltages before pull-in [2] (see Figure 2-5).

Due to the nature of parallel-plate structures, many of design techniques used by different

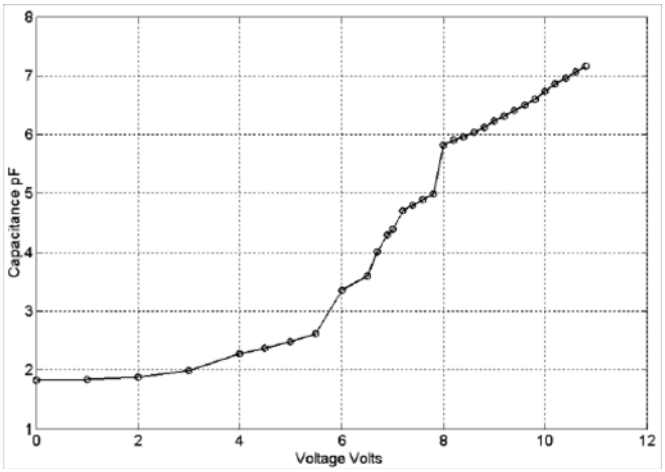


Figure 2-5: The C-V response of a capacitor with enhanced structural stiffness and partial linear respinse [2].

researchers to improve the tunability result in highly sensitive C-V responses, where a major portion of the tuning range is obtained. For this reason, it is important to develop low-sensitive response capacitors, where the entire tunability is usable.

2.4 Linear Capacitors

The C-V response of existing highly tunable capacitors, as discussed before, are either very sensitive to the voltage changes close to pull-in or have two distinct tuning and switching regions and consequently a major portion of their tunabilities are lost. Theoretically, the ideal response for a capacitor is a linear one, where due to constant variability of capacitance to the voltage change, the entire tuning range can be utilized. Moreover, the linear C-V response eliminates a separate circuitry, needed for conventional nonlinear devices, to relate the input and output. Another important advantage of linear systems is their reaction to uncertainties. Nonlinear systems, for instance conventional tunable capacitors, are usually very sensitive to deviations of design parameters from their nominal values, which notably alter the output (as will be discussed later in Chapter 6). In a linear device, the output and input deviations are linearly related which simplifies the operations.

Comparing to the numerous innovative highly tunable designs found in the literature, there

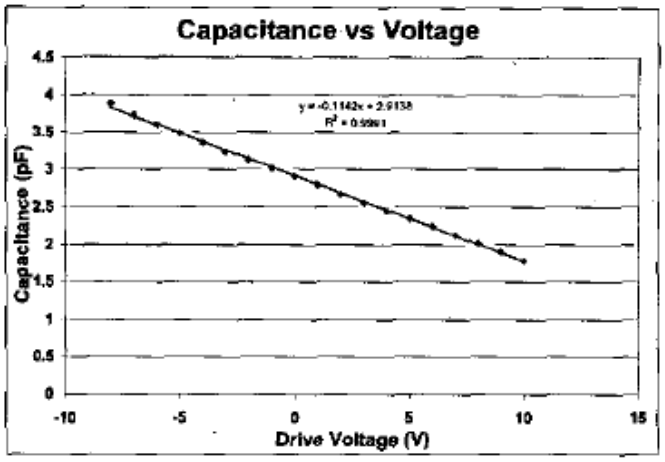


Figure 2-6: A comb-drive linearly tunable capacitor using linear actuators [3].

are limited research works dedicated to the enhancement of the C-V response by decreasing the sensitivity or linearization of the response. Seok *et al.* [24] and Dai *et al.* [44] reported finger-type designs with linear responses and low tunabilities. Tsai *et al.* [3] developed a comb-drive capacitor with highly linear response and tunability of 118%, as shown in Figure 2-6. In this design, linear actuators move the electrodes and since the capacitance and electrodes displacements are proportional, a linear C-V response is obtained. One of the limited parallel-plate-based designs with linear response is a curled-plate pull-in free capacitor introduced by Bakri-Kassem *et al.* [53]. This device utilizes the curvature of the electrodes and has relatively linear response with 115% tunability and since two electrodes are in contact even before the actuation voltage is applied, the pull-in is eliminated.

In this thesis, analytical models and different design techniques are presented which can be used to develop capacitors with high tunabilities and linear C-V responses. A systematic design approach including development of the main idea, modeling, simulation, optimization and verification of the results is exploited to enhance the capacitors performance.

2.5 MEMS Fabrication Uncertainties

One of the major obstructions in development of new MEMS devices is the fabrication uncertainties which are quite noticeable in different processes such as deposition and etching and may produce large deviations in design variables. Therefore, thicknesses, feature sizes and mechanical properties (i.e., Young's modulus and residual stress) of MEMS structures may face considerable variation from one device to another and create a large discrepancy in the device performance. Fabrication uncertainties for IC's and CMOS-based circuits have been well studied and different approaches for yield optimization have been reported in the literature [54, 55, 56]. Despite the similarities between CMOS and MEMS processes, there are limited investigations on MEMS process variations. The focus of some researches is the analysis of uncertainties [57, 58, 59]. Mawardi and Pitchumani [60] and Wittwer *et al.* [61] studied the effect of material and dimensional variations in fabrication of force gauges to develop an optimal design. There are also design optimizations which reduce the sensitivity of design parameters to dimensional deviations to achieve a higher performance. For example, Han and Kwak [62] proposed an optimization method which improves the yield for a vibratory microgyroscope, by considering the fabrication uncertainties. Fan *et al.* [63] used a multi-objective genetic algorithm to minimize the deviations of resonance frequency in a resonator, where the design variables are the lengths and widths of different elements of the resonator. In this optimization problem, the dimensions are modified such that their sensitivities to fabrication uncertainties decrease. As a result, the differences between initial and optimized dimensions may become very large. Moreover, this method cannot include the thickness of the device into consideration, because the nominal thickness of the structural layer is usually fixed.

Due to technological limitations, tightening the tolerance range of feature sizes or layer thicknesses to increase the yield is not always possible and it may drastically increase the fabrication cost. Ponnambalam *et al.* [64, 65, 66] introduced a probabilistic design optimization for electrical elements which increases the yield for a given set of tolerance ranges and distribution functions of corresponding design parameters. The method searches for the nominal design variables which produce the highest yield for the fabrication process. Since the tolerance ranges before and after optimization are the same, then the process complexity and the device topology do not change. Therefore, it is a useful technique for yield maximization of MEMS devices such

as tunable capacitors and resonators. This optimization method is used in this research to maximize the yield for a tunable capacitor with different level of fabrication inaccuracies. The effect of process uncertainties are also studied and the design parameters which produce the highest inaccuracies are found to be used for yield maximization and possible process modifications.

Chapter 3

Application of Nonlinear Springs in Development of Linearly Tunable Capacitors

3.1 Introduction

Conventional parallel-plate MEMS capacitors are modeled as two rigid plates, one fixed to the substrate and the other one suspended by supporting beams. The beams are modeled as springs with constant stiffness coefficients which reflect their bending rigidities. Such a capacitor has two main characteristics: maximum tunability of 50%, and nonlinear C-V response which is very sensitive to the voltage changes near pull-in.

In this chapter, a new design for parallel-plate capacitors is introduced. An ideally linear capacitor is studied and its force-displacement (F-d) curve is used to develop supporting beams with nonlinear stiffness. An analytical model is employed to study the effect of geometric nonlinearity on the device response. The numerical analysis shows that nonlinear structural stiffness can increase the tunability to 150% and partially linearize the C-V curve if the beams are thin and the initial air gap is relatively large. The FEM simulations and experimental results verify the performance enhancement in new designs and demonstrate the applicability of the proposed model developed for numerical simulations.

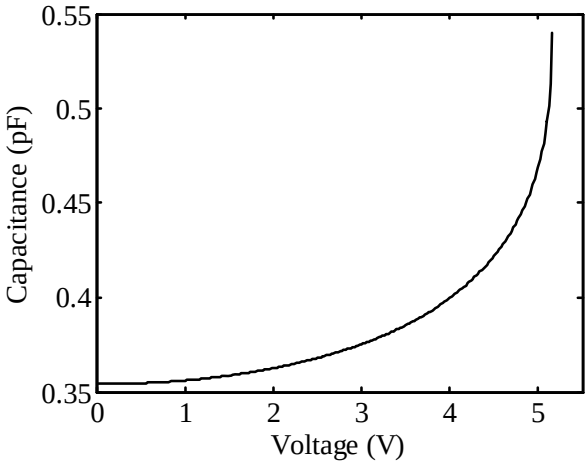


Figure 3-1: The C-V curve of a conventional parallel-plate capacitor.

3.2 Linear Capacitors with Nonlinear Spring

In a MEMS parallel-plate capacitor, the capacitance is a function of electrodes area and the gap in between:

$$C = \frac{\varepsilon_0 A}{d} \tag{3.1}$$

As it was explained before, the actuation voltage changes the capacitance leading to a nonlinear capacitance-voltage curve as shown in Figure 3-1. The dimensional parameters are: $A = 400 \times 400\ \mu m^2$ and $d_0 = 4.0\ \mu m$.

For an ideally linear capacitor, the capacitance-voltage relation is obtained from:

$$C = C_0 \left[1 + (a-1)\frac{V}{V_{\max}}\right] \tag{3.2}$$

where a is the assumed tuning ratio, $\frac{C_{\max}}{C_0}$, and V_{max} is the maximum applied voltage corresponding to $C_{\max}$. Substituting C from (3.1) into (3.2), the air gap for the ideally linear capacitor is expressed in terms of actuation voltage as:

$$d = \frac{V_{\max}}{[V_{\max} + (a-1)V]} d_0 \tag{3.3}$$

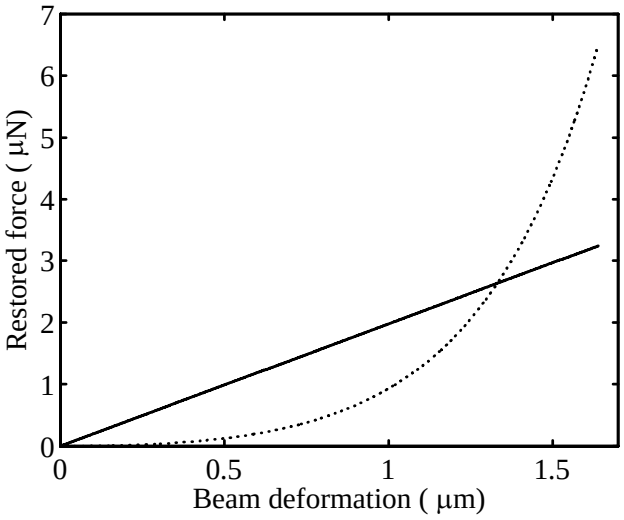


Figure 3-2: The force-deformation curves of an ideally nonlinear beam (dashed line) and a linear spring (solid line).

It should be noted that the displacement-voltage expression (3.3) can only exist if the stiffness coefficients of supporting beams vary in a nonlinear manner. By eliminating the voltage in the equation of static equilibrium (2.7) and substituting the electrodes displacement from (3.3), the nonlinear stiffness coefficient of the ideal supporting beams is obtained as:

$$k_{eq}(d) = \epsilon_0 A V_{\max}^2 \left(\frac{d_0 - d}{2(a-1)^2 d^4} \right) \tag{3.4}$$

Figure 3-2 compares the force-deformation characteristics of an ideally nonlinear stiffness coefficient to that of a linear beam used to obtain C-V response of Figure 3-1. The tunability for both cases is 50% and $V_{max} = V_{pull-in} = 5.16\ V$. As depicted in this figure, the ideal spring provides small resistive force at low voltages and as the bias voltage increases, the stiffness coefficient increases to balance larger electrostatic force and to maintain the capacitance growth.

The closest mechanical element to an ideally nonlinear spring is a bar element which can bear only axial (tensile) force, as shown in Figure 3-3. In static equilibrium, the vertical component

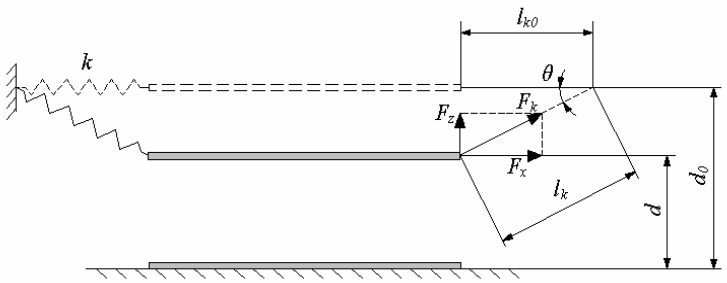


Figure 3-3: A tension spring and the components of force acting on the moving electrode.

of the spring force, F_z, balances the electrostatic force, where

$$F_z = \frac{EA_S}{L_{S0}} \left(1 - \frac{L_{S0}}{\sqrt{(d_0 - d)^2 + L_{S0}^2}} \right) (d - d_0) \tag{3.5}$$

and A_S and L_{S0} are the cross-sectional area and initial length of the beam, respectively. The equivalent stiffness coefficient of a truss beam, k_T, is then obtained from:

$$k_T = \frac{EA_S}{L_{S0}} \left(1 - \frac{L_{S0}}{\sqrt{(d_0 - d)^2 + L_{S0}^2}} \right) \tag{3.6}$$

If the beam dimensions are optimized, the nonlinear stiffness coefficient obtained from the tensile force becomes very similar to that of an ideally nonlinear spring. Figure 3-4 represents the stiffness coefficient of a beam with dimensions: $L_{S0} = 100\ \mu m$, $w = 3\ \mu m$ and $t = 1\ \mu m$. For displacements below $1.2\ \mu m$, the two stiffness coefficients are very close, however, at higher deformations the ideal nonlinear stiffness coefficient grows faster than that of a pure tension spring.

An ideal truss element bears no lateral force or bending moment and is pivoted at both ends (to the anchor and the plate). In practice, it is difficult (if not impossible) to fabricate a pure tension spring with pivoted ends. Therefore, a design modification is considered to simplify the fabrication. In the modified design, the beam is assumed to have fixed-fixed boundary conditions with vertical displacement at one end, as shown in Figure 3-5. This is possible if the

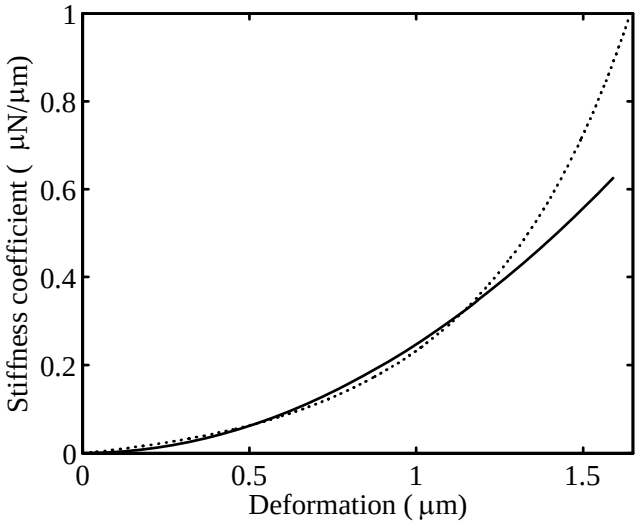


Figure 3-4: Stiffness coefficients of a tension spring (solid line) and the ideal nonlinear spring (dotted line).

capacitor's geometry is symmetric and therefore, the end of beams connected to the moving electrode move vertically. Constraining the axial displacement of the beam at the moving end produces a horizontal force and bending moment in the beam. The governing equations of the beam shown in Figure 3-5 for axial and lateral deformations are nonlinear and coupled [67]. To simplify the analytical simulation of a parallel-plate capacitor equipped with such supporting beams, an uncoupled model for stiffness coefficients of the beams is considered. In this model, it is assumed that the axial and bending deformations are uncoupled, and the stiffness of the beam is simply obtained by adding the tensile and bending stiffness coefficients, k_T and k_B, respectively:

$$k = k_B + k_T = \frac{12EI}{L_{S0}^3} + \frac{EA_S}{L_{S0}} \left(1 - \frac{L_{S0}}{\sqrt{(d_0 - d)^2 + L_{S0}^2}} \right) \tag{3.7}$$

If the thickness of the beam decreases, then k_B reduces with higher rate than k_T. To investigate the effect of beam thickness on the behavior of a capacitor, the air gap-voltage (d-V) and capacitance-voltage curves for a capacitor with three different beam models are compared to those of an ideally linear capacitor (see Figures 3-6-a and 3-6-b). The beam length, width and

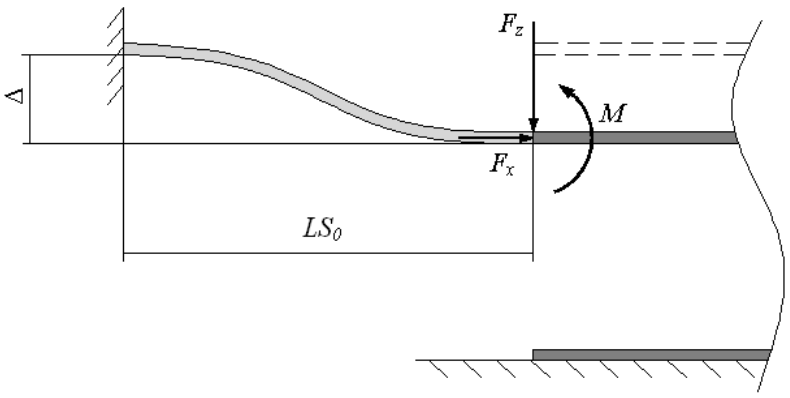


Figure 3-5: The applied forces and deformations of a coupled tensile-bending beam.

thickness are 100 μm, 3 μm and 1 μm, respectively. The initial gap is $d_0 = 4$ μm and the plate dimensions are $A = 400 \times 400$ μm^2. As shown in Figure 3-6-a, the d-V curve of a capacitor with tension beams is similar to that of the linear capacitor (3.3) at low voltages and adding bending stiffness to this beam (the uncoupled model) does not improve the linearity of the C-V response. Moreover, using the uncoupled model, one can see that for small displacements the bending rigidity is dominant and as displacement increases, the geometric nonlinearity generates axial deformations leading to a nonlinear stiffness coefficient. Therefore, to design a beam with structural nonlinearity, the bending stiffness should decrease to achieve higher linearity in the C-V curve. A parallel-plate capacitor with the same dimensions ($A = 400 \times 400$ μm^2 and $d0 = 4$ μm) and different beams is simulated for the demonstration of this observation. The beams are modeled as nonlinear springs with uncoupled bending and tensile stiffness coefficients. The resulting C-V curves for three supporting beams with the same length and width and different thicknesses are presented in Figure 3-7. This figure displays that the geometric nonlinearity increases the maximum tunability of the capacitor because when the voltage increases, the structural stiffness increases accordingly, which, in turn, delays the pull-in. The tunability for capacitors with Beam I, Beam II and Beam III (in Figure 3-7) are 120%, 132% and 143%, respectively. Furthermore, decreasing the thickness of the beam drastically reduces the bending rigidity and therefore a C-V curve with higher linearity is achieved.

To compare the linearity of C-V curves presented in Figure 3-7 to that of a conventional

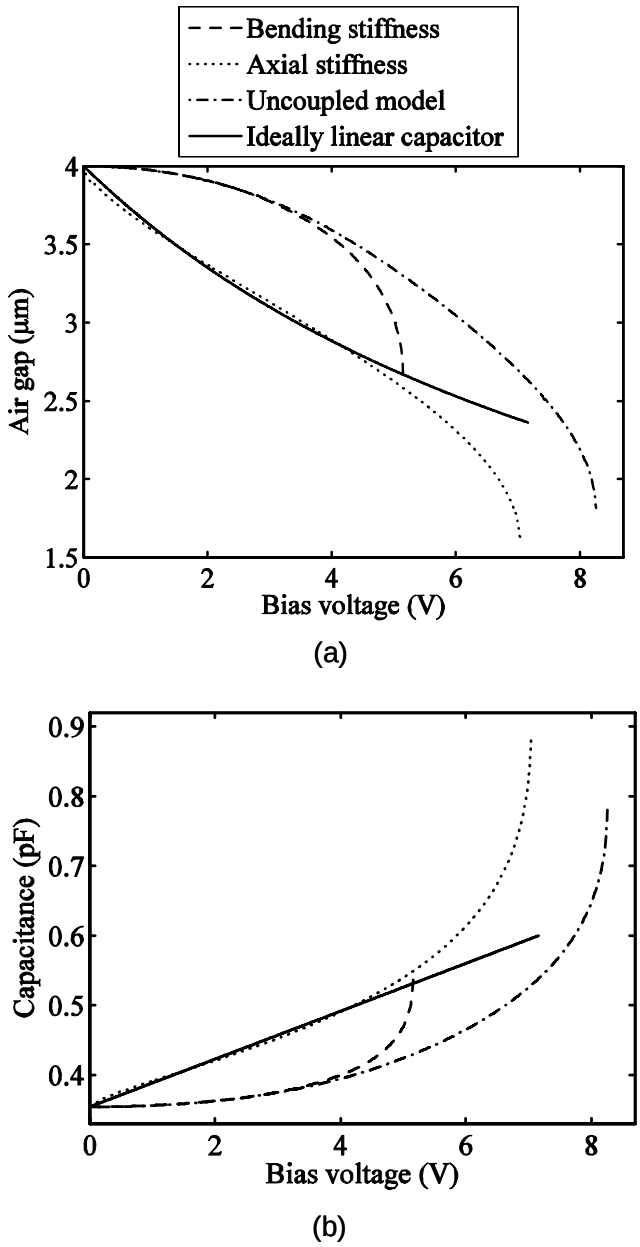


Figure 3-6: The characteristic curves of capacitors with different beam models: (a) Air gap-voltage (b) Capacitance-voltage.

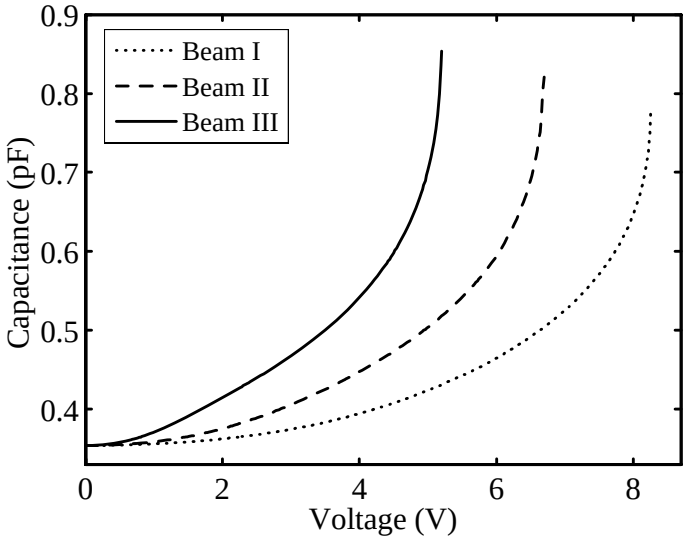


Figure 3-7: The C-V responses for a capacitor with three different beams. Beam I: $L_{S0} = 100$ μm, $w = 3$ μm, $t = 1$ μm; Beam II: $L_{S0} = 100$ μm, $w = 3$ μm, $t = 0.75$ μm; Beam III: $L_{S0} = 100$ μm, $w = 3$ μm, $t = 0.5$ μm.

parallel-plate capacitor, a 50% tuning range in linear regions of each response is considered. For the capacitor with Beam I, the tunability for the voltage interval 2.5 V$< V <$ 7.3 V is 50% and the linearity factor, LF, for this part of the curve is 0.975. Similarly, for the capacitor with Beam II and the voltage interval 1.5 V$< V <$ 5.6 V, the tunability is 50% and LF is 0.986. As expected, the best result is obtained for the capacitor with Beam III which has the lowest thickness. In this case, for voltage interval 0.7 V$< V <$ 4.0 V with 50% tunability, the linearity factor reaches 0.994, displaying a significant improvement.

In addition to the beam thickness, the nonlinear tensile stiffness coefficient, k_T in (3.7), depends also on the initial air gap. Larger air gap causes larger axial deformation in the beam, resulting in higher stiffness at higher voltages. Figure 3-8 portrays this fact where a capacitor with large air gap $d_0 = 7$ μm, beam dimensions: $l = 100$ μm, $w = 3$ μm and $t = 0.5$ μm (Beam III) and the plates size $A = 400 \times 400$ μm^2 is simulated. The tunability in linear region, named linear tunability is $\frac{C(V=10)-C(V=2)}{C(V=2)} \times 100 = 30\%$ with $LF = 0.9997$ and total tunability reaches 147%. As illustrated in this figure, if the beams dimensions and air gap are optimized, a highly linear C-V response with reasonably high tunability is achieved (in Figure 3-8 the C-V curve

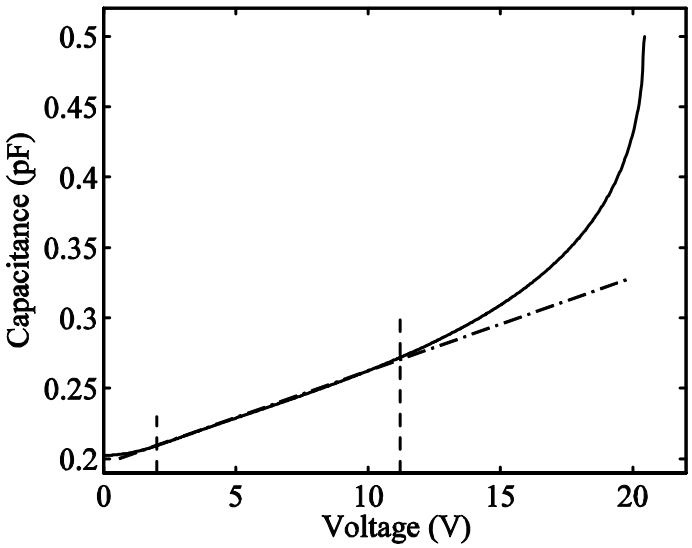


Figure 3-8: A highly linear capacitor with large air gap and thin supporting beams.

and its linear interpolation are hardly separable in the linear region (2.0 V $< V <$ 11.2 V). On the other hand, large initial air gaps result in smaller capacitances and require higher actuation voltages, therefore, for practical reasons they may not be always preferred.

3.3 FEM Analysis

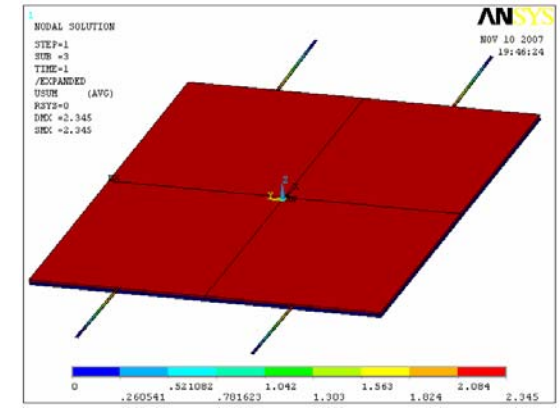
The applicability of the analytical uncoupled model and the effect of nonlinear structural rigidities on the linearization of the C-V response are verified by an ANSYS®-based FEM analysis, as presented in Figures 3-9-a and 3-9-b. ESSOLV macro, a solver for coupled electrostatic and structural fields, was used for simulation which iteratively solves the electrostatic and structural physics to converge to a static equilibrium. In this macro, two electrostatic and structural models are developed at the same time and are meshed in separate physics with different element types. The electrostatic model includes the air around the electrodes and their surfaces, and the electrodes construct the structural model. The electrostatic solver calculates the nodal forces acting on the surface of the electrodes and structural solver calculates nodal displacements of the electrodes. The nodal forces and displacements are iteratively transferred between electro-

static and structural solvers, and iteration continues up to the point that the errors in both solvers reduce to less than defined values. The electrostatic boundary conditions (electrical potential) are defined on the surface of the electrodes and structural boundary conditions are defined in structural model.

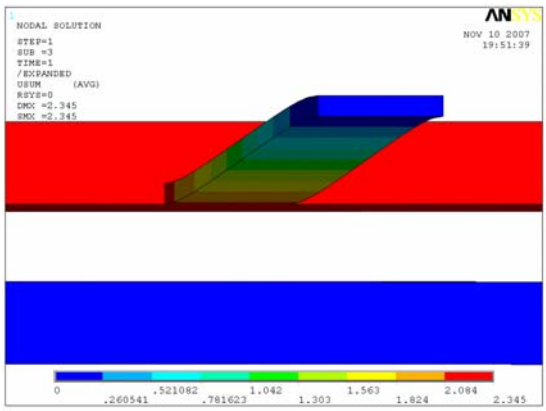
The capacitor used for this simulation has dimensions similar to those of Figure 3-7 ($A = 400 \times 400\ \mu m^2$ and $d_0 = 4\ \mu m$) and the plates thickness 2 μm. The beams dimensions are: $l = 100\ \mu m$, $w = 3\ \mu m$ and $t = 0.5\ \mu m$ (Beam III). The structural and electrostatic physics are meshed with SOLID186 and SOLID122 elements, respectively, and the nonlinear geometry mode is activated. Material properties are the same as those presented in Table 2.1.

The ANSYS simulation results are compared to those of uncoupled beam model in Figure 3-9-c. The maximum tunability for analytical and FEM models are 143% and 125%, respectively. The pull-in voltages, $V_{pull-in}$, obtained by uncoupled beam and ANSYS® models are 5.19 V and 5.03 V, respectively, displaying a good agreement between two models. Similar simulation (with the same element types) were also conducted for a capacitor equipped with linear beams (i.e., the nonlinear geometry was set to zero) and the maximum tunability of 49.9% was obtained for the ANSYS® model.

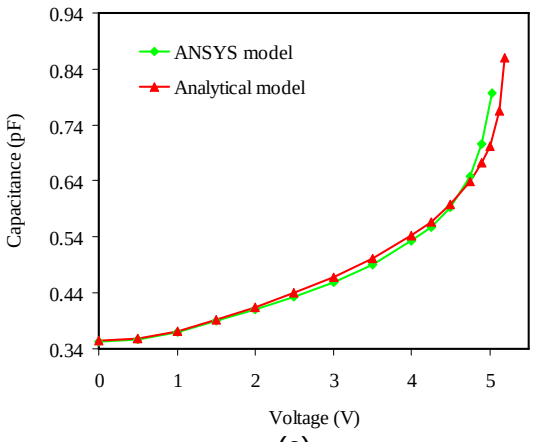
Considering ANSYS® simulations as the reference, the error of uncoupled model is quite negligible. The average error for voltage interval 0.0 V $< V <$ 4.75 V is 1.13%. The maximum capacitance for FEM and analytical models are 0.796 pF and 0.859 pF, respectively, exhibiting 7.9% error. Similar analyses for capacitors with different plate and beam sizes display that the uncoupled model is quite reliable and produces negligible error for capacitors with thin and long beams and small plate sizes. For a capacitor with stiffer beams ($l = 100\ \mu m$, $w = 5\ \mu m$ and $t = 0.5\ \mu m$), the moving electrode underwent deformations leading to a lower tunability and pull-in voltage (see Figure 3-10-a). As shown in Figure 3-10-b, at low voltages the analytical model in this case produces accurate results, but at higher voltages the moving electrode exhibits notable deformations which reduces the tunability and pull-in voltage leading to larger error.



(a)



(b)



(c)

Figure 3-9: FEM simulation of a parallel-plate capacitor with large gap and thin beams. (a) The ANSYS® model; (b) Deformation of a supporting beam; (c) C-V response for analytical and ANSYS® models.

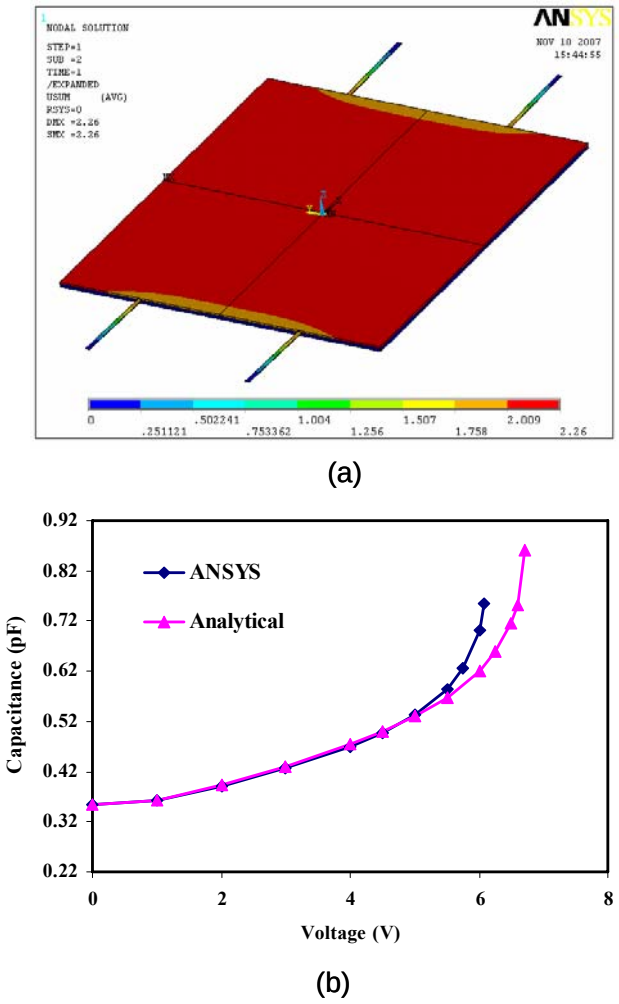


Figure 3-10: (a) ANSYS® simulation of a capacitor with stiffer beams. (b) The C-V responses obtained from ANSYS® and analytical models.

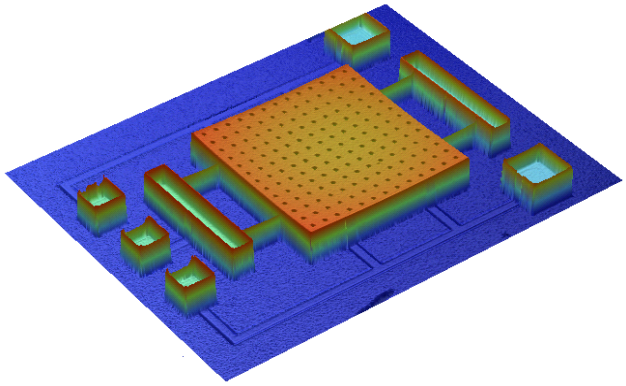
3.4 Fabrication and Experiments

As elucidated in this chapter, to develop a capacitor with highly linear response, the fabrication process should be able to provide large initial air gap and thin structural layer for the supporting beams. In this thesis, PolyMUMPs [16] is considered as the fabrication process and capacitors with different sizes are fabricated and tested to validate the effect of structural nonlinearity on the capacitor performance. It should be mentioned that PolyMUMPs is not an optimum process for linear capacitors because of its thick structural layers and thin sacrificial layers. Nevertheless, capacitors fabricated with this process exhibit "weak geometric nonlinearity" which increases the tunability and verifies the proposed idea that structural nonlinearity can enhance the performance of a parallel-plate tunable capacitor.

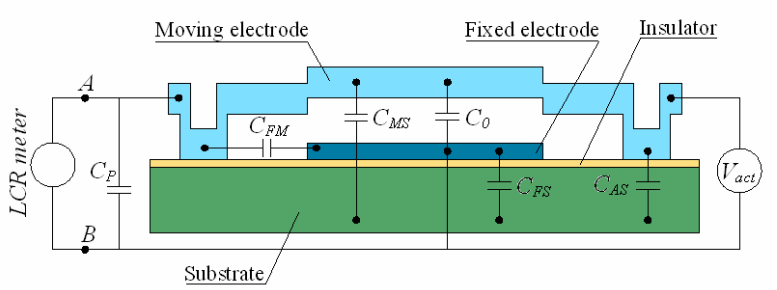
The device fabricated by PolyMUMPs is shown in Figure 3-11-a. The plates have dimensions of $A = 400 \times 400\ \mu m^2$ with 2 μm initial gap. The thickness of moving plate and beams is 2 μm and the beams length and width are 100 and 3 μm, respectively.

Due to intrinsic properties of PolyMUMPs, the silicon substrate and thin dielectric (silicon nitride) layer produce large parasitic capacitances [68]. Different models have been developed to take the parasitic effects into account (for example, see [47] and [69]). In this thesis, a simple model is used to calculate the parasitic terms as presented in Figures 3-11-b and 3-11-c. In the model, C_P, C_{FM}, C_{MS}, C_{AS} and C_{FS} represent parasitic capacitances of measurement probes, fixed plate-moving plate, moving plate-substrate, anchors-substrate and fixed plate-substrate, respectively, and C_0 is the capacitance between two electrodes. The parasitic capacitances and C_0 are extracted from C-matrix obtained by CoventorWare^{TM} simulations and the results are summarized in Table 3.1. The total parasitic capacitance measured at A-B terminals is calculated as $C_{par} = 5.477$ pF. This value must be subtracted from the capacitance measured by LCR meter to obtain C_0. The initial capacitance obtained by CoventorWare^{TM}, $C_0 = 0.7078$ pF, is comparable to 0.7083 pF obtained from analytical model.

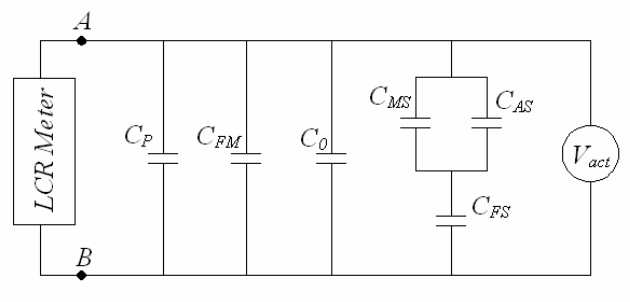
The capacitance-voltage response for the device shown in Figure 3-11-a was measured by Agilent E4890A Precision LCR meter. For more accurate measurement, sample averaging mode in LCR meter was activated and each reading is the result of averaging of 16 to 32 samples calculated by the LCR meter. The resulting tunability ($\Delta C = C - C_0$) curve is compared to the analytical and ANSYS® models in Figure 3-12. The error between calculated and measured



(a)



(b)



(c)

Figure 3-11: A parallel-plate MEMS capacitor fabricated by PolyMUMPs. (a) The image created by WYKO NT1100 Optical Profiler; (b) Cross-view of the device with parasitic capacitances; (c) The equivalent circuit.

Table 3.1: The parasitic capacitances obtained from CoventorWare simulation

Capacitance	Value (pF)
C_0	0.708
C_P	1.166
C_{FM}	0.027
C_{MS}	4.743
C_{AS}	1.031
C_{FS}	16.605

initial capacitance (after subtracting the parasitic capacitance) is 4%. The measured tunability is 67% which is comparable to 63% theoretical value obtained from uncoupled beam model. The test was repeated four times in a row after each pull-in and the results were identical for both capacitance and pull-in voltage. Similar results were also obtained for a capacitor with smaller plate size, $A = 300 \times 300\ \mu m^2$, initial gap $d_0 = 2.75\ \mu m$ and the same supporting beams, where the maximum measured and calculated tunabilities, ΔC_{max}, are 0.299 pF and 0.212 pF, respectively. The resulting C-V curves for this capacitor are presented in Figure 3-13. This figure illustrates an intensified difference between simulations and experimental data.

The pull-in voltages obtained from analytical model, ANSYS® simulations, experiments and that of a conventional model $\left(V_{pull-in} = \sqrt{(8k_{eq}d_0^3)/(27\epsilon_0 A)}\right)$ are 5.32 V, 4.07 V, 1.85 V and 5.15 V, respectively, for the capacitor of Figure 3-12, and 11.19 V, 8.16 V, 2.086 V and 10.05 V, respectively, for that of Figure 3-13. Comparing the theoretical pull-in voltage with values obtained from analytical model supports the idea of small structural stiffening in the beams since analytical model predicts the pull-in voltage slightly larger than that of a conventional device with linear springs. The difference between experimental and simulation results can be attributed to different sources. For example, the fabrication uncertainties and over-etching which decrease the thickness of the beams can be two factors in reducing the actual pull-in and increasing tunability obtained from measurements. It is also possible that the residual stress in the moving electrode creates a curvature which may reduce the average gap between the plates and decrease the pull-in.

To investigate the effect of fabrication uncertainties on discrepancy between simulations and experimental results, a capacitor model with smaller initial air gap and beam thickness ($d_0 = 1.5\ \mu m$ and $t = 1.4\ \mu m$ and the plate size is $A = 300 \times 300\ \mu m^2$) is studied. The analytical and

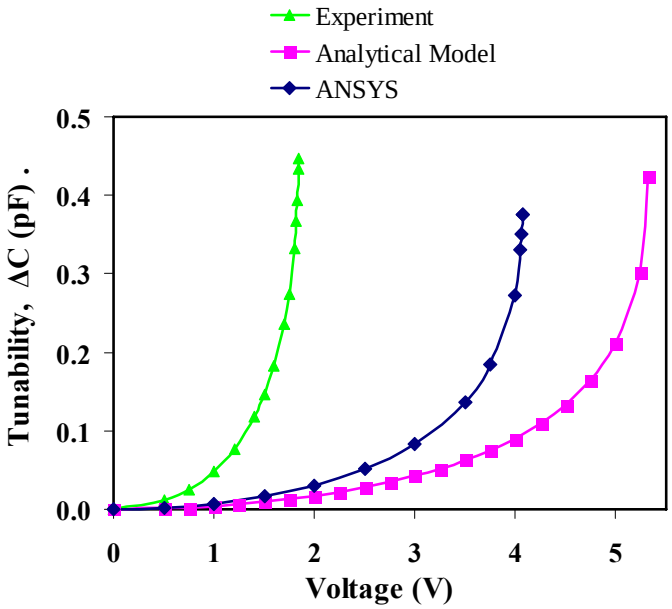


Figure 3-12: The measured ΔC-V response of a MEMS parallel-plate capacitor with nonlinear beams compared to the results of analytical and ANSYS® simulations.

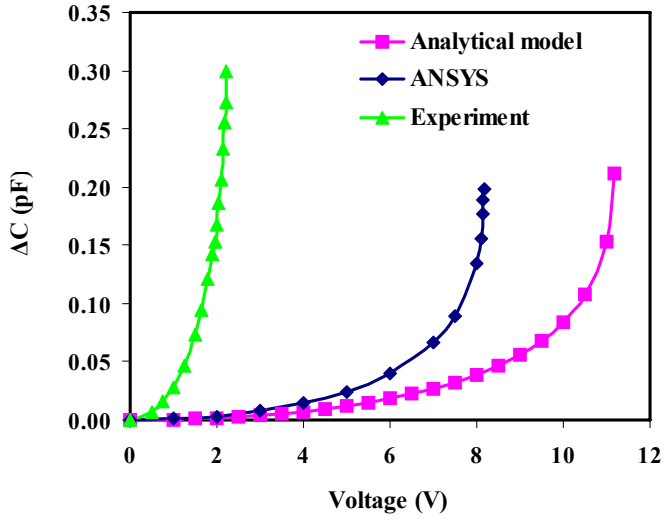


Figure 3-13: The ΔC-V responses for a 300×300 μm^2 capacitor and intial gap $d_0 = 2.75$ μm, obtained from experiment and simulations.

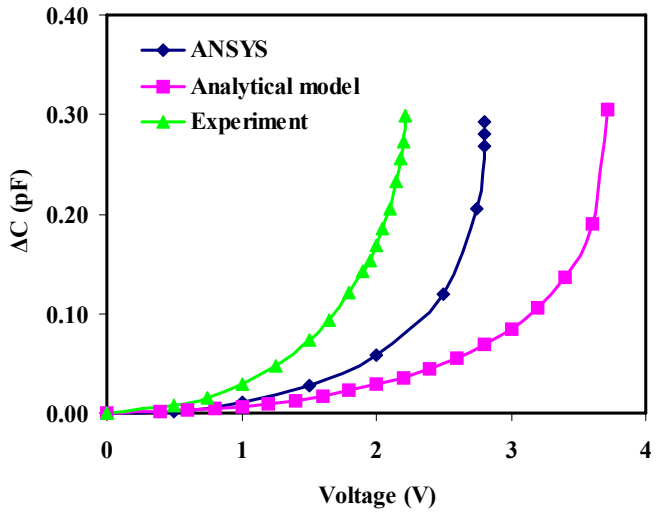


Figure 3-14: The ΔC-V responses for a capacitor with deviations from nominal design values, obtained by ANSYS® and analytical models, compared to the experimental results.

ANSYS® models result in closer pull-in voltage and maximum capacitance to measurement data as displayed in Figure 3-14. One should note that if actual initial air gap is less than the nominal value (2.75 μm), the initial capacitance and maximum tunability changes. The tunabilities obtained from ANSYS® and analytical models are 53.5% and 57.5%, respectively. If the actual initial air gap decreases, then the effect of weak structural nonlinearity may not affect the capacitance or may have negligible effect. Therefore, as explained before, to obtain a highly linear and tunable capacitor, the fabrication process should be modified to build thin beams with large initial air gaps.

It is important to note that the analytical uncoupled beam model introduced in this chapter provides an efficient tool that can be used in early design stages for development and optimization of electrostatically actuated devices. The computation time for C-V responses obtained by analytical uncoupled beam models is only few seconds (depending on the number of voltage samples), while the convergence time at each voltage sample and for a relatively course mesh ANSYS® model varies from 10 minutes at low voltages to over two hours at voltages near pull-in. For example, at $V = 5.03$ V (the last point on C-V curve in Figure 3-9-c), the convergence takes over two hours.

3.5 Summary and Conclusion

The characteristic force-displacement curve of an ideally linear capacitor was analyzed. Based on this curve, supporting beams with similar nonlinear stiffness coefficients were developed to be integrated in a parallel-plate tunable capacitor. The beam's nonlinear stiffness coefficient incorporates bending and axial rigidities. Analytical and FEM analyses of capacitors with relatively large gap, $d_0 \geq 4.0\ \mu m$, and thin beams, $t \leq 1.0\ \mu m$, verify that nonlinear supporting beams increase the tunability and linearity of C-V curves. For devices fabricated by PolyMUMPs, with relatively thick beams and small air gap, weak geometric nonlinearity increases the tunability. When the fabrication process is flexible, it is possible to optimize the capacitor's design parameters to maximize the linearity factor of the C-V response or the maximum tunability. Different examples presented in this chapter also demonstrate that the analytical uncoupled beam model produces negligible error for small deformations. This model can be advantageously exploited in early design stage to save computational time and cost in development of electrostatically actuated elements.

Chapter 4

Development of Highly Tunable and Linear Capacitors with Asymmetric Geometries

4.1 Introduction

Conventional MEMS capacitor designs have rectangular-shape plates and symmetric geometries which maintain the parallelness of the electrodes. If the device structural symmetry is altered or electrode shapes other than rectangle are used, the plates lose the parallelness and consequently the capacitance-voltage response changes. Such techniques are exploited in this chapter to enhance the capacitors performance. First, a non-parallel-plate capacitor with asymmetry in one direction is studied and the effect of different design parameters on C-V response is investigated. Then, two conventional designs, two-gap and three-plate capacitors, are modified using the non-parallel-plate structures and geometric nonlinearity. Finally, a novel triangular-plate capacitor model, based on structural and geometric asymmetry, is developed to provide a combination of high tunability and linearity in the C-V response.

4.2 Non-Parallel-Plate Capacitors

In a parallel-plate capacitor if the electrode geometry is asymmetric or supporting beams are not the same, then after applying a DC voltage the two electrodes lose their parallelness, as shown in Figure 4-1-a. In this case, the resultant electrostatic force deviates from the center of plates, causing an uneven deflection in the beams. The electrostatic force and the moment about z axis for a capacitor with uneven springs, $k_1 \neq k_2$, are obtained by integration over the area of the electrodes (see Figure 4-1-b):

$$F = \int_A \frac{\epsilon_0 V^2 dA}{2d(x)^2} = \frac{\epsilon_0 V^2 A}{2d_1 d_2} \tag{4.1}$$

$$X_0 F = \int x dF = \frac{\epsilon_0 V^2 A}{2} \left[\frac{l}{(d_2 - d_1)^2} \ln\left(\frac{d_2}{d_1}\right) - \frac{l}{d_2(d_2 - d_1)} \right] \tag{4.2}$$

The nodal positions of the moving plate, d_1 and d_2, are obtained from the equations of static equilibrium (each side is considered as a node):

$$\frac{\epsilon_0 V^2 A}{2d_1 d_2} - k_1(d_0 - d_1) - k_2(d_0 - d_2) = 0 \tag{4.3}$$

$$\frac{\epsilon_0 V^2 A}{2} [\frac{l}{(d_2 - d_1)^2} \ln(\frac{d_2}{d_1}) - \frac{l}{d_2(d_2 - d_1)}] - k_2(d_0 - d_2)l = 0 \tag{4.4}$$

Nonlinear equations (4.3) and (4.4) are numerically solved for d_1 and d_2. The capacitance is then obtained from:

$$C = \int dC = \frac{\epsilon_0 A}{(d_2 - d_1)} \ln(\frac{d_2}{d_1}) \tag{4.5}$$

These equations are solved for a capacitor with plate size $A = 350 \times 350\ \mu m^2$, air gap $d_0 = 2.75\ \mu m$, and different stiffness ratios $r = k_2/k_1$. The results of numerical simulations are shown in Figure 4-2. As depicted in this figure, increasing the stiffness ratio, r, increases the pull-in voltage and decreases the maximum tunability. If the shape of electrodes changes to a trapezoid, then the relations for electrostatic force and moment and capacitance is derived by direct integration as:

$$F = \frac{\epsilon_0 V^2}{2} (\frac{\alpha}{\beta} \ln\left(\frac{d_2}{d_1}\right) + \frac{L_1 l}{d_1 d_2} - \frac{\alpha l}{\beta d_2}) \tag{4.6}$$

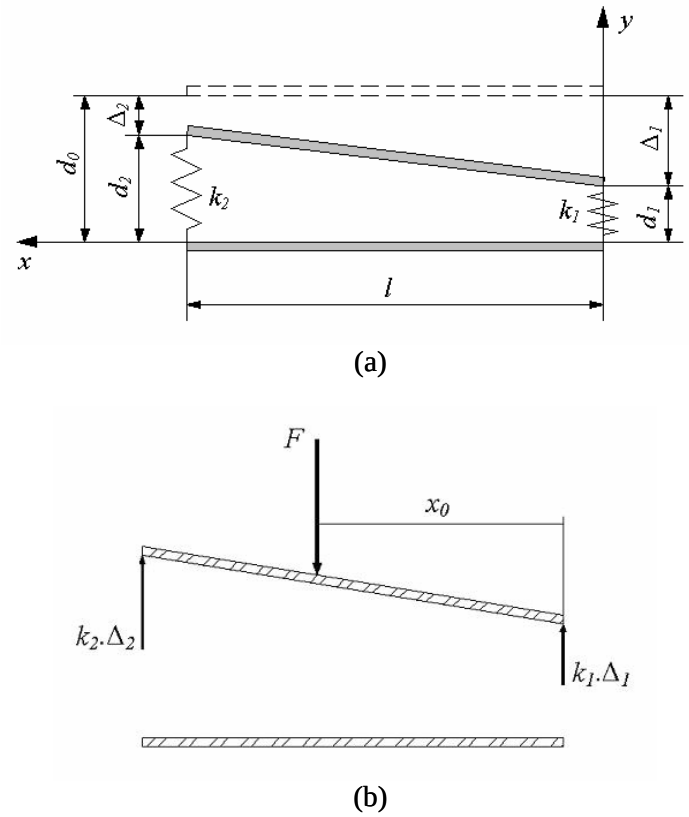


Figure 4-1: The geometry and forces acting on a non-parallel-plate tunable capacitor.

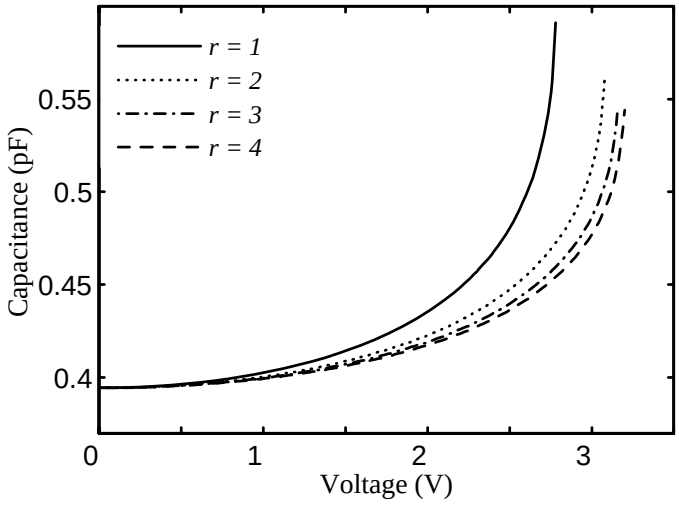


Figure 4-2: The C-V responses of an asymmetric capacitor with different stiffness ratios, $r = \frac{k_2}{k_1}$.

$$X_0 F = \frac{\epsilon_0 V^2}{2 d_2 \beta^3}[d_2 \ln(\frac{d_2}{d_1})(\beta L_1 - 2\alpha L_1) + \alpha\beta l(d_1 + d_2) - \beta^2 L_1 l] \tag{4.7}$$

$$C = \epsilon_0[\frac{\alpha}{\beta} l + \ln(\frac{d_2}{d_1})(\frac{L_1}{\beta} + \frac{\alpha}{\beta} d_1)] \tag{4.8}$$

where

$$\alpha = \frac{L_2 - L_1}{l} \tag{4.9}$$

$$\beta = \frac{d_2 - d_1}{l} \tag{4.10}$$

and L_1 and L_2 are the width of the electrode at nodes 1 and 2, respectively, as displayed in Figure 4-3.

A design parameter, $a = L_2/L_1$, is defined to study the effect of geometric asymmetry on the capacitance-voltage response, and different C-V responses are plotted for different values of a in Figure 4-4. As shown in this figure, the maximum tunability increases as a increases, however, for $a = 100$ where the electrode approaches a triangular shape, the maximum tunability is still less than that of a conventional design. Figures 4-2 and 4-4 illustrate that asymmetric designs do not generate high tunability or linearity; however, as will be discussed later, these geometric modifications are useful tools in developing highly tunable or highly linear capacitors.

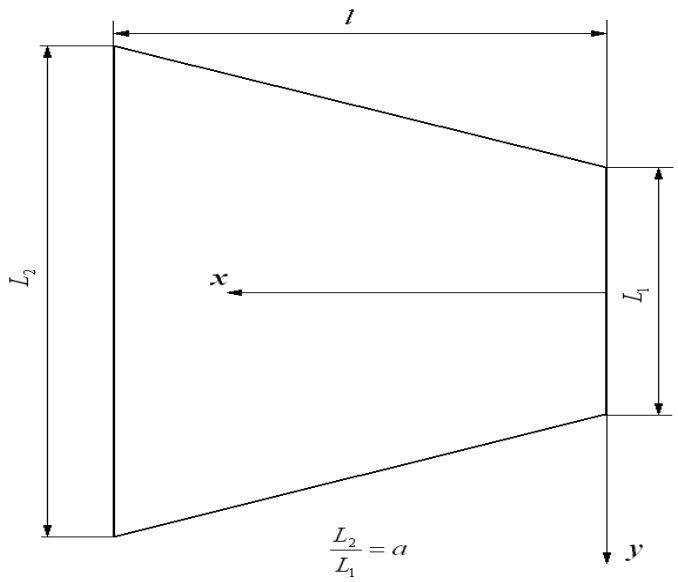


Figure 4-3: A trapezoidal electrode.

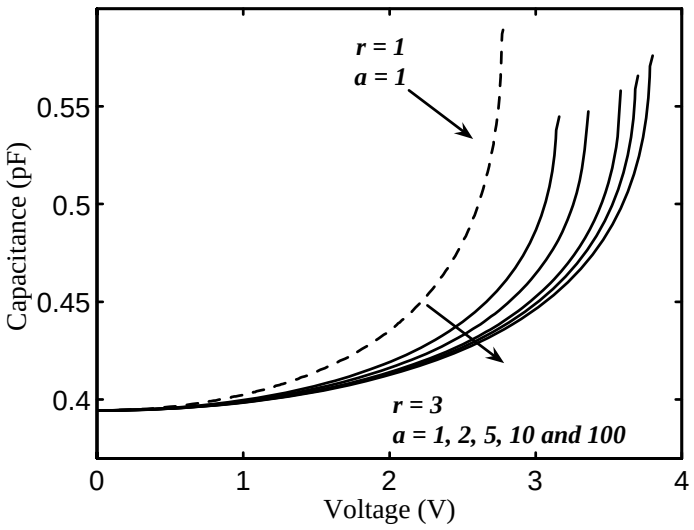


Figure 4-4: The C-V responses of asymmetric capacitors with trapeziodal electrodes and uneven beams.

4.3 Highly Tunable Two-Gap Capacitors

Two-gap parallel-plate tunable capacitors with separate actuation and sense gaps (see Figure 4-5) have been well-established in the literature [11, 49, 50]. As shown in Figure 4-5, the fixed plate in such capacitors is separated into actuation and sense electrodes where a one-piece moving plate is used for both actuation and sense. Since the pull-in occurs at two-third of initial actuation gap, for $d_{sen} < d_{act}$ the capacitor exhibits tuning ratio higher than 1.5 [51, 52]. It is potentially possible to reach infinite tunability if $d_{sen} = d_{act}/3$. In a two-gap capacitor, the capacitance is obtained from:

$$C = \frac{\epsilon_0 A_{sen}}{d_{sen}} \tag{4.11}$$

where A_{sen} is the area of the sense electrodes. When the bias voltage is applied to the actuation electrodes, the gap between them, d_{act}, is obtained by solving the following equation of static equilibrium:

$$\frac{\epsilon_0 A_{act} V^2}{2 d_{act}^2} - k_{eq} \left(d_0 - d_{act}\right) = 0 \tag{4.12}$$

where k_{eq} represents the stiffness coefficients of all supporting beams, A_{act} is the area of actuation electrodes, V is the bias voltage and d_0 is the initial actuation gap. The numerical solutions of (4.12) for a conventional parallel-plate and a two-gap capacitor, designed for PolyMUMPs, are shown in Figure 4-6. The electrodes dimensions are: $A_{sen} = 300 \times 400\ \mu m^2$, $A_{act} = 200 \times 400\ \mu m^2$ and initial sense and actuation air gap are 2.0 μm and 2.75 μm, respectively. For the conventional parallel-plate capacitor initial actuation and sense gaps are the same, $d_0 = 2\ \mu m$. As presented in this figure, the two-gap capacitor provides higher tunability of 91%.

Two-gap capacitors are highly sensitive to the voltage change near pull-in where a notable portion of the tunability is produced. In the next two sections, two design modifications are introduced that can enhance the performance of the two-gap capacitors by increasing the tunability and decreasing the sensitivity of the response to the voltage change.

4.3.1 Capacitors with Structural Nonlinearity

It was shown in Chapter 3 that if the beam's force-deformation relation changes to a stiffening regime, then electrostatic and structural forces both grow and larger stable displacement is achievable. This modification improves the tunability of the device by delaying the pull-in

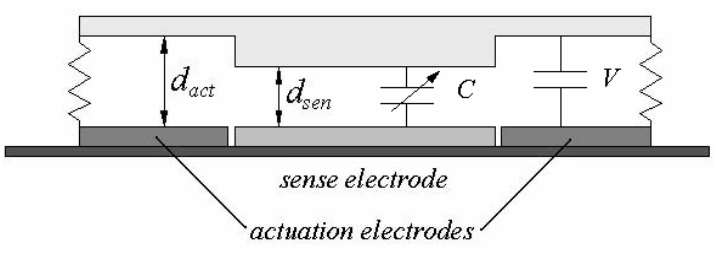


Figure 4-5: A two-gap parallel-plate capacitor with separate actuation and sense electrodes

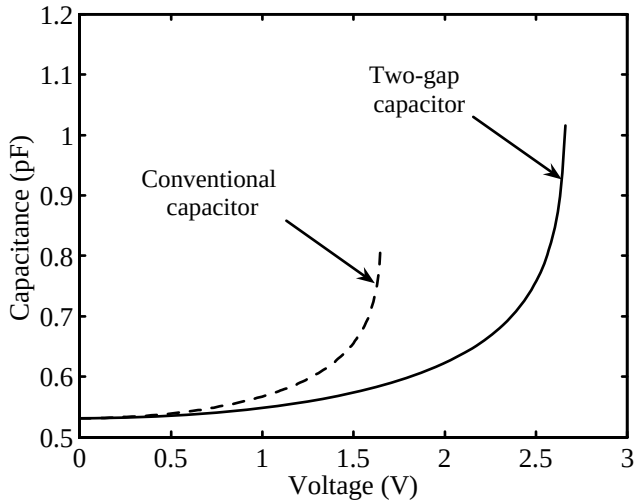


Figure 4-6: C-V curves for conventional and two-gap parallel-plate tunable capacitors.

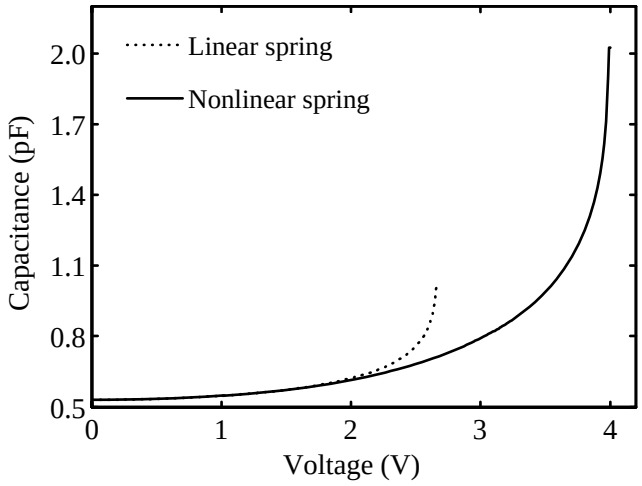


Figure 4-7: C-V curves for two-gap parallel-plate tunable capacitors with linear and nonlinear springs.

effect. Using the uncoupled nonlinear beam model, the C-V response of two-gap capacitors with and without structural nonlinearity are compared in Figure 4-7. The electrodes dimensions for both capacitors are the same as the ones shown in Figure 4-6 with the ratio of sense gap to actuation gap: $\frac{d_{sen}}{d_{act}} = \frac{2.0}{2.75} = 0.727$. The modified capacitor displays 281% tunability which is over three times higher than that of a conventional two-gap capacitor.

It is possible to obtain the same tunability for a conventional capacitor by changing the gap ratio, for example, if $\frac{d_{sen}}{d_{act}} = \frac{2.0}{4.425} = 0.452$, then for a capacitor with linear springs the tunability reaches up to 281%. However, the shape of the response is different from that of the modified design, because in a capacitor with nonlinear beams when actuation voltage increases, the structural resistive force also increases, and therefore, the electrode's displacement changes with a slower rate. To compare the responses of a conventional two-gap capacitor and a modified one with nonlinear stiffness, two normalized curves are presented in Figure 4-8. As depicted in this figure, for a conventional capacitor, the rate of capacitance change is very low up to the point where voltage reaches about $0.9V_{pull-in}$, and then there is a sudden increase in the capacitance for the last part of the curve. In the modified device, the capacitance increases with higher rate at low voltages, but close to pull-in, it has lower sensitivity to the voltage change

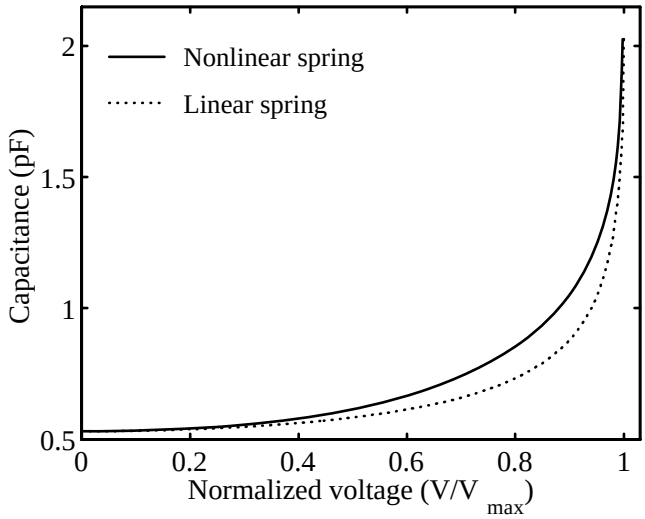


Figure 4-8: A comparison between C-$(V/V_{\max})$ responses of conventional and modified highly tunable two-gap capacitors.

comparing to the response of a conventional capacitor. This is the main advantage of nonlinear structural stiffness over conventional linear beams and can increase the "usable tunability" of the capacitor. Furthermore, when fabrication process is limited and $\frac{d_{sen}}{d_{act}}$ cannot be reduced to any desired value, the nonlinear springs can advantageously provide higher tuning ratio.

4.3.2 Capacitors with Asymmetric Geometries

As the second modification, the geometric symmetry of the capacitor is altered. For a trapezoidal-shape capacitor with uneven beams the actuation voltage causes uneven deformations in beams and alters the parallelness of the two plates (see Figure 4-9). The capacitance in this case is obtained from:

$$C = \epsilon_0[\frac{\alpha}{\beta}L_{sen} + \ln(\frac{d_3}{d_2})(\frac{L_1}{\beta} + \frac{\alpha}{\beta}d_2)] \tag{4.13}$$

where $\alpha = (L_2 - L_1)/L_{sen}$, $\beta = (d_3 - d_2)/L_{sen}$ and L_1 and L_2 are the width of the sense electrode corresponding to end positions d_2 and d_3, respectively, as shown in Figures 4-9-a and 4-9-b.

By integrating electrostatic force and moments over the length of actuation electrodes, the

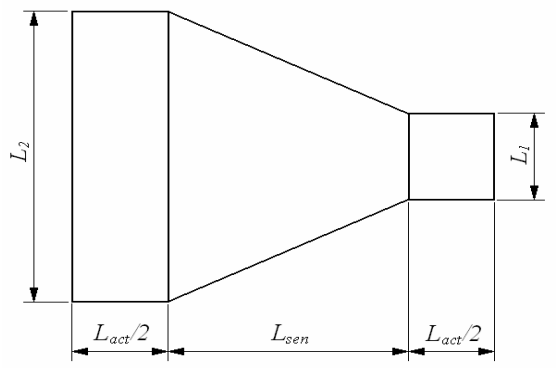
following expressions for resultant electrostatic forces and moments are obtained:

$$F_i = \frac{\epsilon_0 A_i V^2}{2 d_{i+1} d_i} \quad , \quad i = 1, 3 \tag{4.14}$$

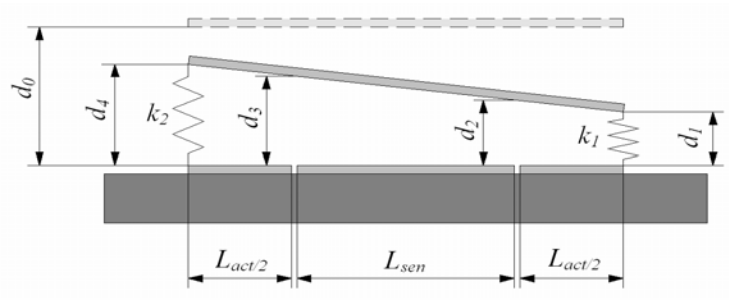
$$x_i F_i = \frac{\epsilon_0 A_i V^2 L_{act}}{4(d_{i+1} - d_i)^2} \left[\ln(\frac{d_2}{d_1}) - (1 - \frac{d_i}{d_{i+1}}) \right] \quad , \quad i = 1, 3 \tag{4.15}$$

Equations (4.14) and (4.15) are used in the static equilibrium to calculate d_2 and d_3 for any input voltage and the capacitance is calculated from (4.13). To study the effect of asymmetry, two design parameters, $a = L_2/L_1$ and $r = L_{S2}/L_{S1}$, are defined, where L_{S1} and L_{S2} are the length of supporting beams corresponding to k_1 and k_2, respectively. If these parameters change, then the tunability and the shape of C-V response change accordingly. Figure 4-10 compares the C-V curves of different capacitors designed for PolyMUMPs with actuation and sense gaps of 2.75 μm and 2.0 μm, respectively. Cap I and Cap II are the conventional parallel-plate and two-gap capacitors, with tunability of 50% and 91%, respectively. As presented in this figure, the modified designs, Cap III with nonlinear springs and Cap IV with nonlinear springs and asymmetric geometry, can provide much higher tunabilities. One can see that in Cap IV with design parameters $a = 15$ and $r = 2$, the tunability is improved to 344% comparing to 281% of Cap III.

The pull-in voltages for modified designs, shown in Figure 4-10, are higher than conventional ones, therefore, to quantify the improvement of sensitivity a criterion for maximum allowable slope for the normalized response, C-$(V/V_{\max})$, is considered as: $\Delta C/\Delta(V/V_{\max}) \leqslant 2.0$ pF, i.e., for a 0.01 increment in normalized actuation voltage, the capacitance increases by less than 0.02 pF. Using this criterion the maximum low sensitive tunability for Cap I, Cap II, Cap III and Cap IV are obtained as 29%, 44%, 77% and 80%, respectively. Similar values for absolute slope criterion, $\Delta C/\Delta V \leqslant 1.0$, are 33%, 51%, 115% and 164%, respectively. The analysis of response sensitivity and numerical simulations demonstrate the improvement of capacitor's performance for modified two-gap designs as the tunability notably increases and the response sensitivity to voltage change decreases.



(a)



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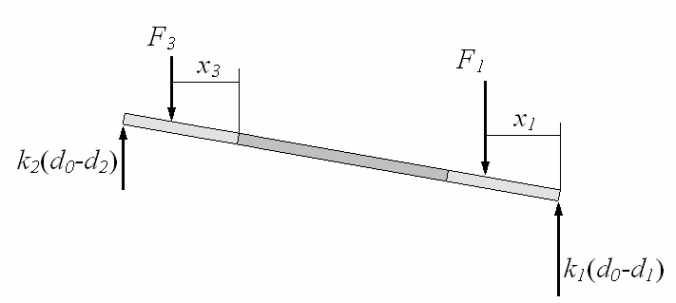


(c)

Figure 4-9: A modified asymmetric two-gap tunabel capacitor: (a) The electrode shape; (b) Displacements under electrostatic actuation; (c) Forces acting on the moving electrode.

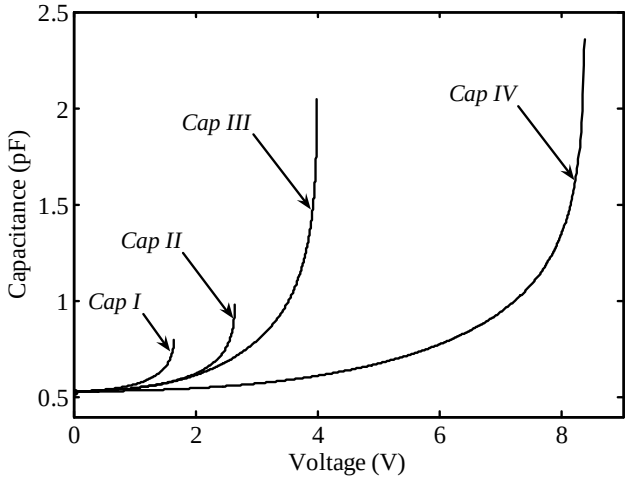


Figure 4-10: C-V curves for different designs: Cap I, Cap II, Cap III and Cap IV represent conventional parallel-plate capacitor, conventional two-gap capacitor, modified two-gap capacitor with nonlinear springs and modifed asymmetric capacitor with nonlniear springs, respectively.

4.4 Three-Plate Linear Capacitors

4.4.1 Analysis and Design optimization

The design introduced in Chapter 3 uses the characteristic force-displacement curve of an ideally linear capacitor to develop nonlinear elements and linearize the capacitance-voltage response. In this section, a similar approach is followed considering air gap-voltage (d-V) curve of an ideally linear device, expressed by:

$$d = \frac{d_1}{1 + \frac{1-a}{a}\left(\frac{V-V_1}{V_2-V_1}\right)} \tag{4.16}$$

where $V_1 \leq V \leq V_2$, d_1 and d_2 are the initial and final gaps at V_1 and V_2, respectively, $a = \frac{C_1}{C_2}$ is the tuning ratio, C_1 and C_2 are the capacitance at V_1 and V_2, respectively, and $C_1 > C_2$. In this model, the C-V response is descending and can be generated by a three-plate model shown in Figure 4-11. In this capacitor, the bias voltage is applied to the actuation electrodes and the sense electrodes are used to measure the capacitance [45]. When the voltage is applied, the middle plate moves toward the bottom fixed plate and the distance between two sense plates,

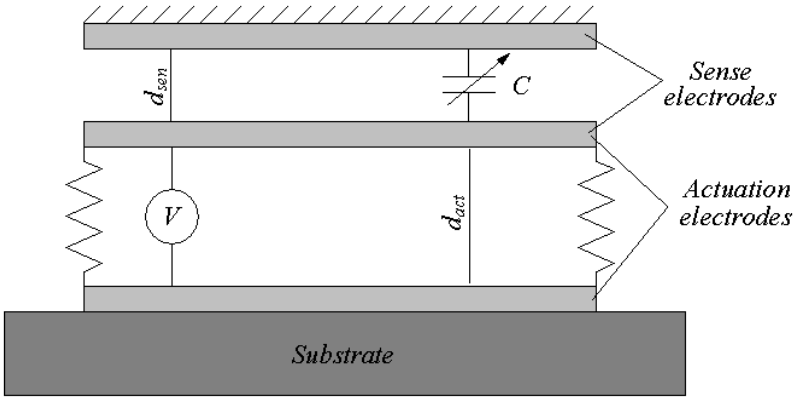


Figure 4-11: A simplified model of a three-plate tunable capacitor.

d_{sen}, increases. In a three-plate capacitor, the pull-in occurs at 2/3 of the initial actuation gap, d_{act}, and therefore, for $d_{sen} < d_{act}$ the capacitor provides tunability higher than 50%. Figure 4-12 compares the behavior of an ideally linear capacitor to that of a three-plate capacitor. The capacitor's dimensions are: $A = 350 \times 350\ \mu m^2$, $d_{sen} = 0.75\ \mu m$ and $d_{act} = 2\ \mu m$. For the ideal capacitor the parameters used in (4.16) are: $V_1 = 0$ and $V_2 = V_{pull-in} = 1.88$ V, $C_1 = 1.446$ pF, and $C_2 = 0.770$ pF. C_1 and C_2 are chosen to be the initial and final capacitances of the three-plate capacitor, respectively. The tuning ratio for both capacitors is $a = 1.88$. The linearity factor of the C-V curve is $LF = -0.959$ (negative sign implies that the curve is descending) which is higher than that of a conventional parallel-plate capacitor.

As shown in Figure 4-12, at low voltages the change in the gap for three-plate capacitor is slower than that of ideally linear one and close to the pull-in, the rate of displacement change in three-plate capacitor exceeds that of the ideal one. Numerical simulations reveal that when the ratio of the two gaps, d_{sen}/d_{act}, decreases, three-plate and ideally linear capacitors exhibit similar behavior at the middle of the gap-voltage (d-V). For a capacitor with $A = 350 \times 350$ μm^2, $d_{sen} = 0.3\ \mu m$ and $d_{act} = 2.45\ \mu m$ and for voltage interval $V_1 = 0.8$ V and $V_2 = 2.4$ V, the C-V and d-V curves are compared to those of ideally linear capacitor in Figure 4-13. Since the d-V curves for the real and ideal devices are very similar, the linearity is considerably improved and reaches $LF = -0.9995$.

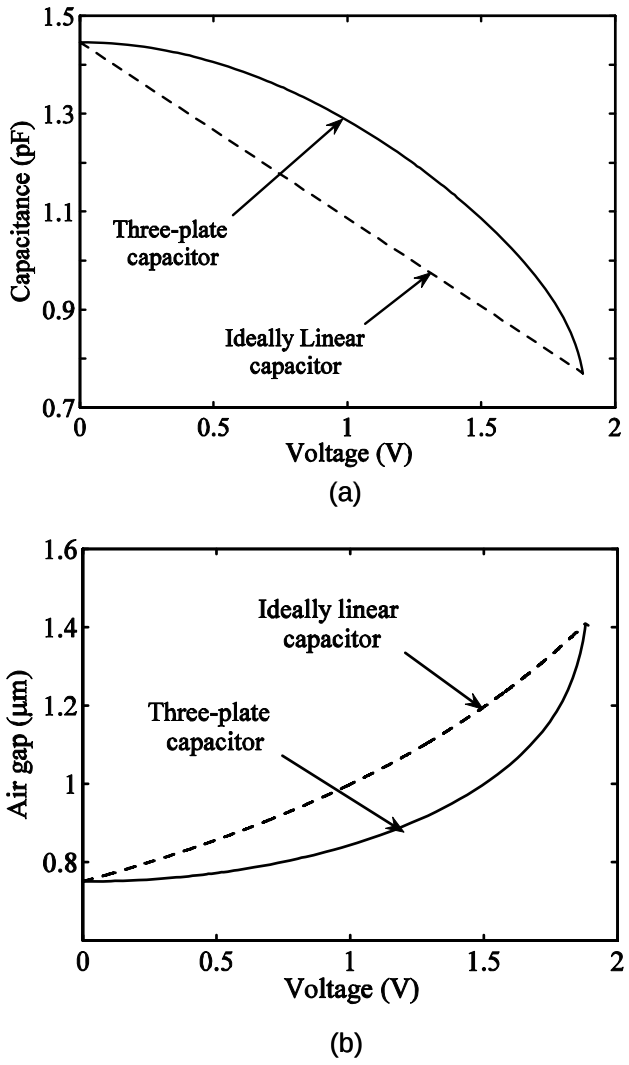


Figure 4-12: A comparison between an ideally linear capacitor and a three-plate tunable capacitor designed for PolyMUMPs: (a) C-V response; (b) d-V curve.

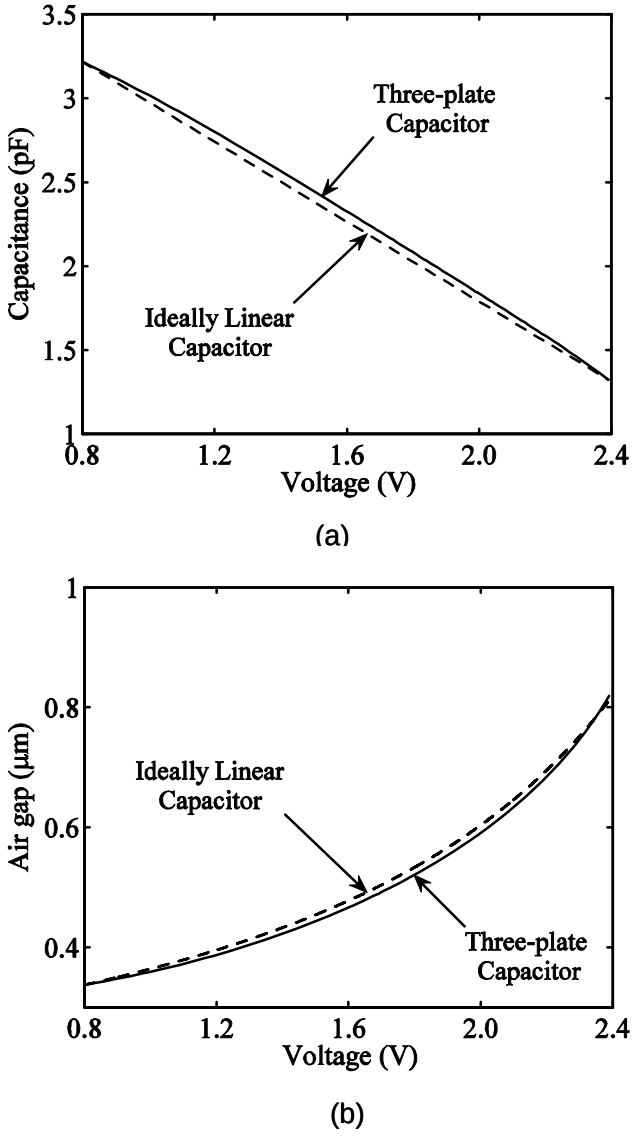


Figure 4-13: A highly linear three-plate tunable capacitor; (a) C-V response; (b) d-V curve.

Figure 4-13 also demonstrates major improvement in tunability. As already explained, when the sense gap to actuation gap ratio, d_{sen}/d_{act}, decreases, the tunability increases. For the C-V curve shown in this figure, for the voltage interval 0.8 V $< V <$ 2.4 V, the tunability is 143% (this tunability is called linear tunability), where the total tunability for $0 < V < V_{pull-in}$ is 275%. When fabrication process is flexible and capable of depositing and etching sacrificial layers with arbitrary thicknesses, then d_{sen}/d_{act} can be optimized to obtain the best linear response. For example, a capacitor with the same plates dimensions and actuation and sense gaps $d_{act} = 2.5\ \mu m$ and $d_{sen} = 0.25\ \mu m$, respectively, provides $LF = -0.99997$ with 146% linear tunability for the voltage interval 0.9 V$< V <$ 2.4 V. The total tunability is 346% and the actual and ideal C-V and d-V responses are hardly separable in linear region. When highly precise linear C-V response is not required, then the upper and lower voltage limits may vary for the best combination of linearity and tunability. For example, the voltage limits 0.6 V $< V <$ 2.6 V provides $LF = -0.9997$ and linear tunability 262%.

In general, an optimization problem which includes the fabrication limitations (minimum possible gaps) and design preferences (maximum tunability and linearity and minimum pull-in voltage) can obtain the best design parameters. If fabrication limitations restrict the minimum thickness for deposition and etching, one can get similar results by increasing the actuation gap (and the pull-in voltage). Figure 4-14 represents a capacitor with similar behavior and different gap, where $d_{act} = 5\ \mu m$, $d_{sen} = 0.5\ \mu m$. The maximum and linear tunabilities for this design are 332% and 168%, respectively, with $LF = 0.99997$ in the linear region.

4.4.2 Design Modifications

A tunable capacitor may be integrated in a circuit where different elements are fabricated on the same chip and it is not possible to customize the process for each element. Therefore, it is important to modify the design for a standard processes with fabrication limitations such as fixed thickness for sacrificial layers. To demonstrate the capability of the design modifications, in what follows PolyMUMPs is considered as a standard process.

The C-V response of a three-plate capacitor designed for PolyMUMPs was already presented in Figure 4-12-a, where the thickness of sacrificial layers Oxide1 and Oxide2 are 2 μm and 0.75 μm, respectively, and the response is nonlinear. To obtain a higher linearity, the symmetry of

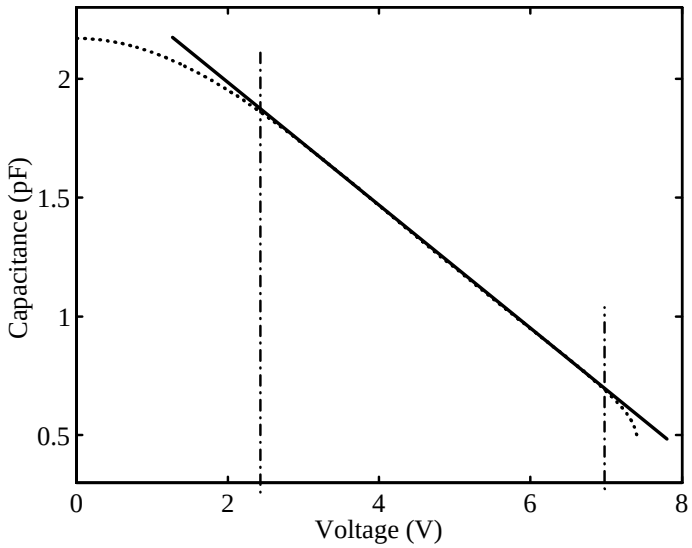


Figure 4-14: The C-V response of a highly linear three-plate MEMS capacitor (dotted line) and its interpolation in linear region (solid line).

the capacitor is altered using both uneven springs and trapezoidal plate shape. The supporting beams are also designed to exhibit nonlinear stiffness coefficients. This modifications stretch the C-V curve to the right-hand-side of the voltage axis. The capacitance, in this case, is obtained from:

$$C = \epsilon_0[\frac{\alpha}{\beta_{sen}}l + \ln(\frac{d_{sen2}}{d_{sen1}})(\frac{L_1}{\beta_{sen}} + \frac{\alpha}{\beta_{sen}}d_{sen1})] \tag{4.17}$$

where l is the length of electrodes, $\alpha = (L_2 - L_1)/l$, $\beta_{sen} = (d_2 - d_1)/l$, L_1 and L_2 are the width of the sense electrode corresponding to d_{sen1} and d_{sen2}, the distance between sense electrodes at their two ends, respectively (see Figure 4-15). The electrostatic force and moment acting on the moving electrode are obtained from expressions similar to (4.6) and (4.7), respectively.

The results of these modifications are presented in Figure 4-16. The total tunability for the new design is 82% which is slightly less than conventional design (88%). For the voltage interval 1.5 V$< V <$ 3.2 V, the linear tunability is 52% and the C-V curve exhibits high linearity, $LF = -0.999$. If this response is substituted by its linear interpolation, the maximum error in linear region is less than 1%.

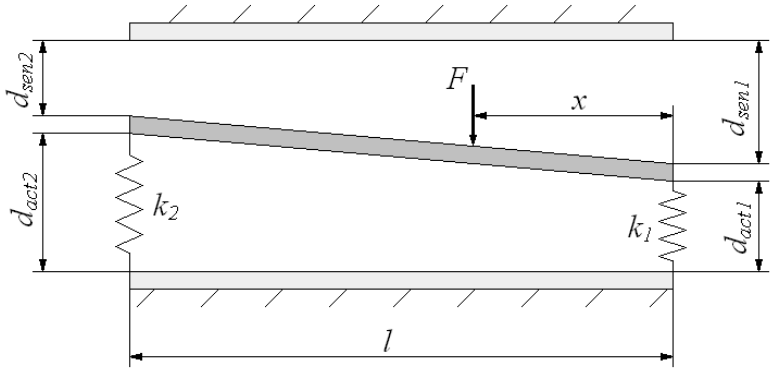


Figure 4-15: The displacements of an asymmetric three-plate capacitor.

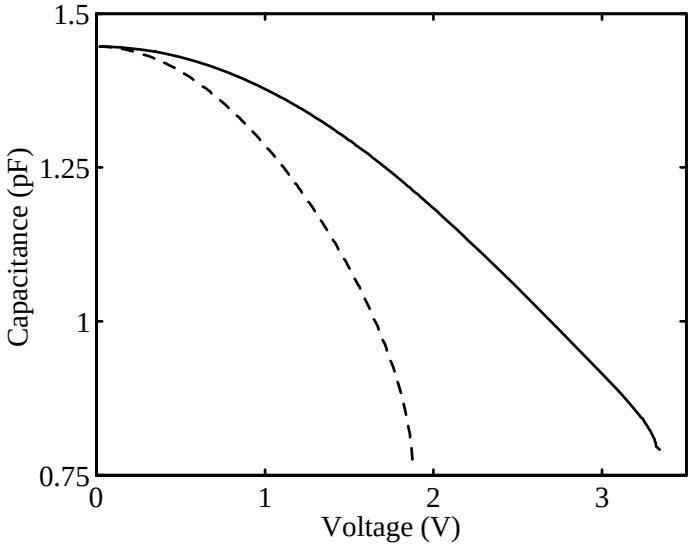


Figure 4-16: C-V responses of a conventional three-plate tunable capacitor (dashed line) and an optimized asymmetric design with nonlinear springs (solid line).

4.5 Triangular-Plate capacitor

4.5.1 Governing Equations

The modified non-parallel-plate designs introduced in this chapter (two-gap and three-plate capacitors) have a symmetric axis and an asymmetric one. Therefore, the moving electrode has two independent nodal displacements. In a triangular-plate capacitor with three uneven supporting beams, the moving plate has three independent nodal displacements, as shown in Figure 4-17-a. The moving plate is assumed to be rigid and suspended by three beams connected to its three nodes (nodes 1, 2 and 3). Using the model presented in Figures 4-17-a, 4-17-b and 4-17-c, the governing equations of the capacitor is obtained as follows.

The displacement of the moving plate after applying a bias voltage is expressed in terms of its nodal positions d_1, d_2 and d_3. When a voltage is applied, the beams deform to balance the electrostatic force. If the three side lengths l_1, l_2 and l_3 or the stiffness coefficients k_1, k_2 and k_3 are not the same, the two electrodes lose their parallelness. The equations of static equilibrium, in this case, are written as:

$$F - k_1(d_0 - d_1) - k_2(d_0 - d_2) - k_3(d_0 - d_3) = 0 \tag{4.18}$$

$$X_1 F - k_1(d_0 - d_1) l_3 \sin\theta_2 = 0 \tag{4.19}$$

$$X_3 F - k_3(d_0 - d_3) l_2 \sin\theta_2 = 0 \tag{4.20}$$

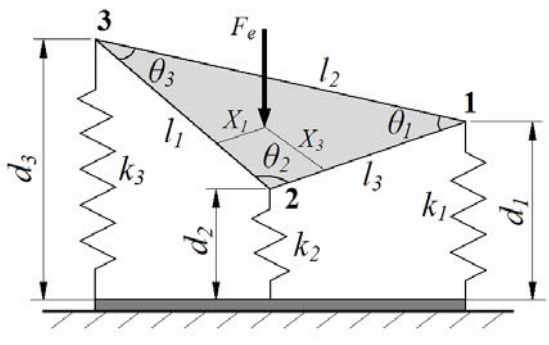
where d_0 is the initial gap between two electrodes. The electrostatic force, F, in (4.18) is obtained from :

$$F = \int_0^{l_3 \sin\theta_2} \frac{\epsilon_0 V^2 l_1(x)}{2 d_1(x) d_2(x)} dx \tag{4.21}$$

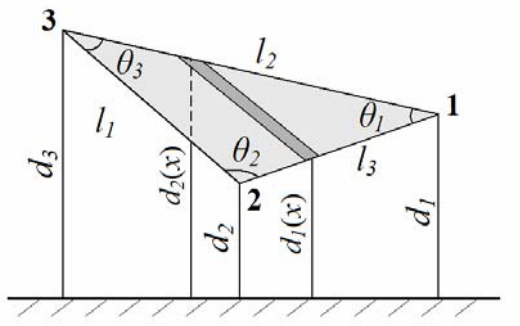
$d_1(x)$ and $d_2(x)$ are expressed in terms of nodal positions as follow (see Figure 4-17-b):

$$d_1(x) = d_2 + \frac{d_1 - d_2}{l_3 \sin\theta_2} x \tag{4.22}$$

$$d_2(x) = d_3 + \frac{d_1 - d_3}{l_3 \sin\theta_2} x \tag{4.23}$$



(a)



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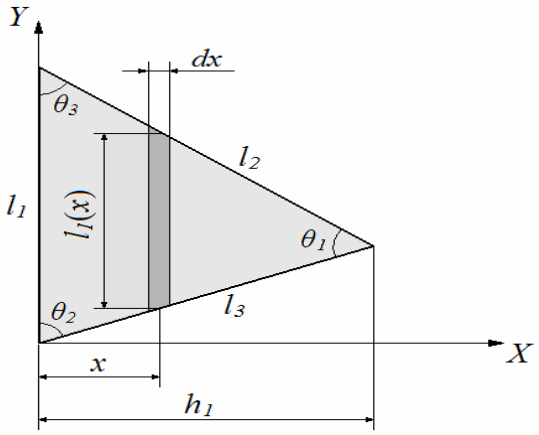


(c)

Figure 4-17: (a) A simplified model of a triangular-plate capacitor; (b) The differential element and its end positions; (c) The top view of the electrode.

and as shown in Figure 4-17-c, the length of differential element is obtained from:

$$l_1(x) = l_1\left(1 - \frac{x}{l_3 \sin\theta_2}\right) \tag{4.24}$$

Therefore:

$$F = \epsilon_0 V^2 A \frac{d_1 \ln\left(\frac{d_3}{d_2}\right) + d_2 \ln\left(\frac{d_1}{d_3}\right) + d_3 \ln\left(\frac{d_3}{d_1}\right)}{(d_1 - d_2)(d_2 - d_3)(d_3 - d_1)} \tag{4.25}$$

where A is the area of the plate. The electrostatic moments X_1F and X_3F are obtained from:

$$X_1F = \int_0^{l_3 \sin\theta_2} \frac{\epsilon_0 V^2 l_1(x)}{2 d_1(x) d_2(x)} x dx \tag{4.26}$$

$$X_3F = \int_0^{l_2 \sin\theta_1} \frac{\epsilon_0 V^2 l_3(x)}{2 d_1'(x) d_2'(x)} x dx \tag{4.27}$$

where $d_1'(x)$ and $d_1'(x)$ are obtained form expressions similar to (4.22) and (4.23).

Equations (4.18) to (4.20) are highly nonlinear and should be numerically solved at each voltage to obtain the nodal positions d_1, d_2 and d_3. Once the nodal positions are known, the capacitance is calculated from:

$$C = \int_A \frac{\epsilon_0 dA}{d(x)} = \int_0^{l_3 \sin\theta_2} \frac{\epsilon_0 l_1(x) x}{d_2(x) - d_1(x)} \ln\left(\frac{d_2(x)}{d_1(x)}\right) dx \tag{4.28}$$

As an example, consider an equilateral triangular-plate capacitor with $l_1 = l_2 = l_3 = 400$ μm and the initial gap $d_0 = 2.75$ μm, designed for PolyMUMPs. All supporting beams are assumed to have the same length, width and thickness of $L = 120$ μm, $w = 5$ μm and $t = 1.5$ μm, respectively. The stiffness coefficient of each beam reflects its bending rigidity. The corresponding C-V response is presented in Figure 4-18 and since all side lengths and beams stiffness are the same, the three nodal displacements are equal and electrodes remain parallel. Therefore, the tunability of the capacitor is limited to 50%.

By changing the stiffness of three supporting beams one can obtain a higher tunability. For example, if the beams lengths for a capacitor of Figure 4-18 changes to $l_1 = 100$ μm, $l_2 = 130$ μm and $l_3 = 200$ μm, the tunability increases to 64% with a nonlinear and sensitive curve.

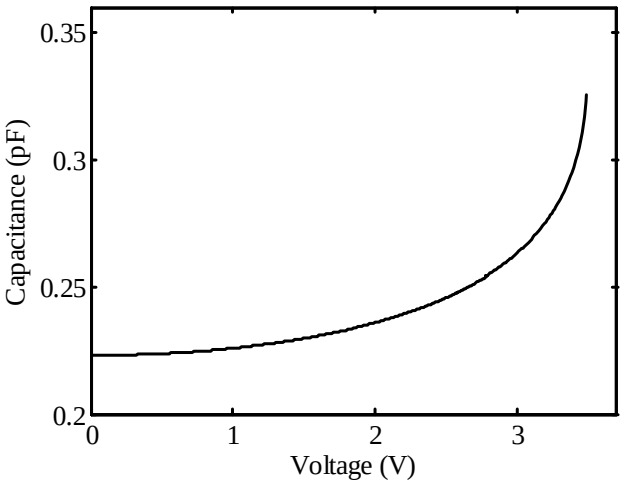


Figure 4-18: The C-V response of a symmetric triangular-plate tunable capacitor.

4.5.2 Linear Triangular-Plate Capacitors

It was shown that asymmetric triangular-plate capacitors slightly increase the tunability but do not improve the sensitivity or linearity of the C-V response. To improve the linearity of the response, a new design displayed in Figures 4-19-a and 4-19-b is introduced, where a flexible step (a lateral beam named middle beam) with initial height of h_i is added under node i, $i = 1, 2, 3$. When the bias voltage increases, the nodes touch the corresponding middle beams and their stiffness are added to the system. The equations of static equilibrium for this capacitor are the same as (4.18) to (4.20). The nodal stiffness coefficient before and after contact is k_i and $(k_i + k_i')$, respectively, where k_i' is the stiffness of the ith middle beam.

To investigate the effect of middle beams on linearity of the C-V response, a capacitor designed for PolyMUMPs is considered. The initial air gap is $d_0 = 2.75\ \mu m$ and the heights of three flexible steps are the same: $h = [2.0, 2.0, 2.0]\ \mu m$. The length and width of all supporting and middle beams are 120 μm and 5 μm, respectively, where their thicknesses are 1.5 μm, and 2.0 μm, respectively. The electrodes are equilateral triangles, $l_1 = l_2 = l_3 = 400\ \mu m$. The resulting C-V response for this capacitor is presented in Figure 4-20, where due to geometric symmetry, the plates remain parallel and all nodes contact the middle beams at the same time. The figure depicts that when the nodes touch the middle beams, the total stiffness of the

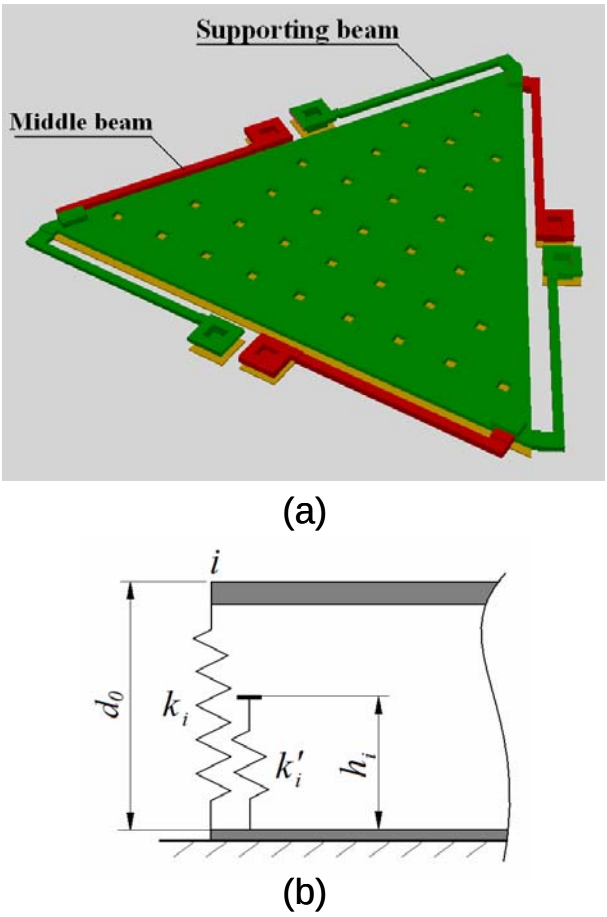


Figure 4-19: (a) A modified triangular-plate capacitor; (b) The simplified model of the middle nodal beam.

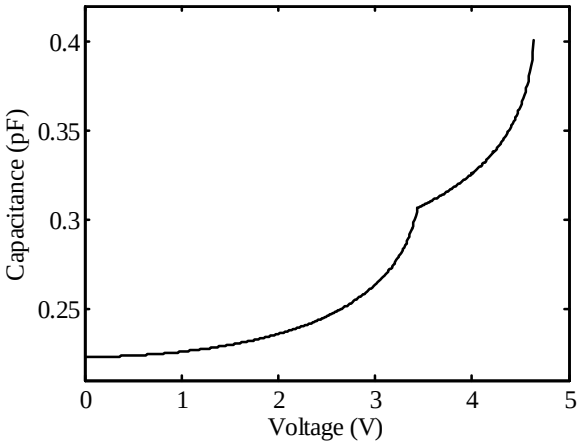


Figure 4-20: The C-V response of a modified triangular-plate capacitor with even supporting and middle beams.

system suddenly increases. This reduces the rate of nodal displacements and consequently, a discontinuity in the C-V curve is created. Adding stiffness of the system increases the resistive force and delays the pull-in and the maximum tunability (for this design) increases to 81% with $LF = 0.9176$.

If the supporting beams are not the same, the stiffness coefficients of three middle beams, k_1', k_2' and k_3', will be added to the system at different voltages. Hence, the overall structural stiffness of the capacitor gradually increases. This results in a smoother and more linear C-V response and reduces the sensitivity of the curve. To maximize the linearity of the response the following optimization problem is defined:

$$\begin{aligned} \max \ & LF(k_1, k_2, k_3, k_1', k_2', k_3') \qquad (4.29) \\ & \text{subject to} \quad : \\ & k_3 \ < \ k_2 \\ & k_2 \ < \ k_1 \\ & k_{low} \ \leqslant \ k_i \leqslant k_{up} \\ & k_{low}' \ \leqslant \ k_i' \leqslant k_{up}' \end{aligned}$$

Table 4.1: The results of design optimization for a triangular-plate capacitor

Design	L_1	L_2	L_3	L'_1	L'_2	L'_3	LF	Lin. Tun.	Max. Tun.
Cap I	120	120	120	120	120	120	0.9176	-	81%
Cap II	110	120	210	100	50	200	0.9936	78%	152%
Cap III	110	130	290	150	70	160	0.9932	104%	142%
Cap IV	100	120	290	140	70	150	0.9944	102%	136%

Li and $L'i$ are the lengths of supporting and middle beams, respectively.

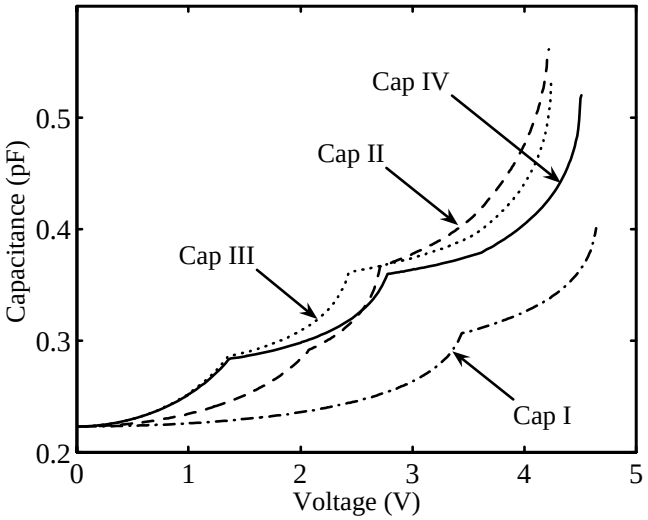


Figure 4-21: C-V responses for triangular-plate capcitors with different design parameters.

where k_{up} and k_{low} and k'_{up} and k'_{low} are the upper and lower limits for supporting and middle beams, respectively. The first two constraints in (4.29) guarantee that the three nodes touch the middle beams at different voltages and increase the maximum tunability. For simplicity, the width of all beams is set to $w = 5\ \mu m$, and only their lengths change. It should be mentioned that due to high level of nonlinearity of the governing equations, different initial guesses for the lengths of beams may result in different final values, and several trials may be needed to obtain the optimum set of supporting and middle beams. Table 4.1 and Figure 4-21 show the results of numerical simulations for different sets of beam lengths, where Cap II provides 150% and Cap III and Cap IV generate 100% linear tunabilities.

In order to illustrate the level of linearity of the new design, the C-V response of Cap

IV and its linear interpolation with upper and lower bounds are plotted in Figure 4-22-a. The linear region is in voltage interval 0.2 V$< V < (V_{pull-in} - 0.2)$ V. The upper and lower bounds specify a $\pm 4\%$ margin, meaning that if the real C-V curve is substituted by its linear interpolation, the maximum possible error is 4%. The nodal positions are plotted in Figure 4-22-b and as explained before, the high linearity is obtained because the three nodes touch the middle beams at three different voltages. Figures 4-22-a and 4-22-b verify that the separation of contact points in the new design considerably enhances the response of a parallel-plate-based capacitor by linearizing the curve, increasing the tunability and reducing the sensitivity of the curve to the voltage changes.

4.6 Summary and Conclusion

It was demonstrated that geometric and structural modifications presented in this chapter can notably improve the tunability and linearity of a parallel-plate tunable capacitor. Altering the parallelness of the electrodes decreases the sensitivity of the C-V response to the voltage change and adding structural nonlinearity increases the resulting resistive force and therefore, improves the linearity and tunability. Using these techniques, conventional two-gap and three-plate capacitors were modified for higher tunability and linearity.

The novel triangular-plate design, presented in this chapter, also verifies that a combination of geometric and structural modifications can drastically enhance the capacitor's performance. These modifications may also be implemented to rectangular-shape electrodes to achieve high linearity and tunability.

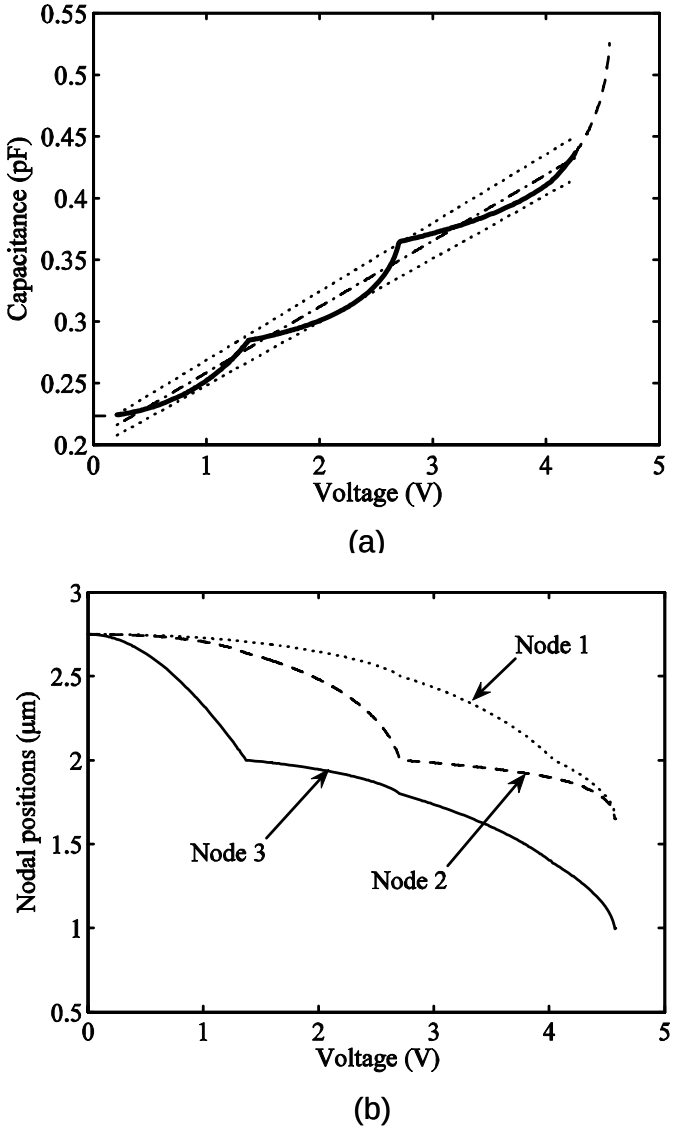


Figure 4-22: (a) The C-V response of a triangular-plate capacitor (dashed line), its linear region (solid line), the linear interpolation (dash-dotted line) and upper and lower bounds (dotted lines); (b) The nodal displacement of the same capacitor.

Chapter 5

Linearly Tunable Capacitors with Flexible Electrodes

5.1 Introduction

In a conventional parallel-plate tunable capacitor, the moving electrode is assumed to be rigid. The accuracy of such an assumption depends on the size of the plate and stiffness of the supporting beams and may produce error for a thin moving electrode and stiff beams as discussed in Chapter 3. Therefore, taking the flexibility of the plate into account can increase the accuracy of a model. Moreover, if the displacement of a flexible moving electrode is controlled, capacitance-voltage responses with different shapes can be obtained. This provides a strong design tool for the development of highly tunable and linear capacitors. In this chapter, different design techniques such as segmentation of moving electrodes and geometric modifications with nonlinear structural stiffness are used to develop linear capacitors with high tunabilities.

5.2 Analysis of Moving Plates Flexibility

To study the flexibility of the moving electrode of a parallel-plate tunable capacitor, an analytical approximate lumped model is developed. The moving plate is divided into rigid segments and each segment is connected to the neighboring segments by torsional springs as shown in Figure 5-1. In this model, the moving plate consists of n nodes, and $n-1$ segments connected

together with n torsional springs, kt_i (the stiffness coefficient of first and last torsional springs are zero, $kt_1 = kt_n = 0$). At each node there is a linear spring, k_i, as shown in Figure 5-1-b, where the first and the last linear springs represent the supporting beams and the others along with the torsional springs simulate the plate rigidity. The distance of node i from fixed plate is d_i. The equations of static equilibrium for this model are obtained using the energy method. The potential energy due to deformations of torsional and linear springs is expressed in terms of segments displacements as:

$$U = \sum_{i=1}^{n} \left[\frac{kt_i}{2}(\theta_{i-1} - \theta_i)^2 + \frac{k_i}{2}(d_0 - d_i)^2 \right] \tag{5.1}$$

where d_0 is the initial air gap between the two electrodes and θ_i is the slope of each segment. Nodal displacements, d_i, are much smaller than segments length, $d_i - d_{i+1} \ll l_i$ and hence, θ_i can be approximated as (θ_i in Figure 5-1-b are exaggerated):

$$\theta_i = \frac{d_i - d_{i+1}}{l_i} \tag{5.2}$$

The potential energy is then written as:

$$U = \sum_{i=1}^{n} \left[\frac{kt_i}{2} \left(\frac{d_{i-1} - d_i}{l_{i-1}} - \frac{(d_i - d_{i+1})}{l_i} \right)^2 + \frac{k_i}{2}(d_0 - d_i)^2 \right] \tag{5.3}$$

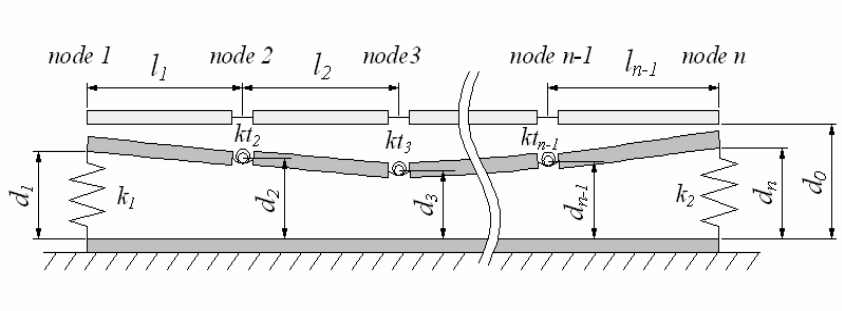
The work done by external electrostatic force, W, is expressed in terms of nodal displacements as follows:

$$W = \sum_{i=1}^{n-1} \left(d_0 - d_i + \frac{(d_{i+1} - d_i)}{l_i} x_i \right) F_i \tag{5.4}$$

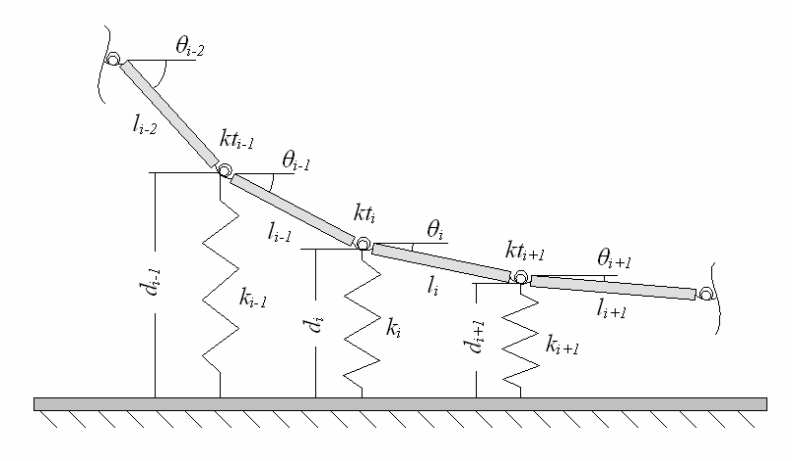
where x_i is the distance of resultant electrostatic force, F_i, from i^{th} node. F_i and x_i are nonlinear functions of nodal displacements of the i^{th} segment and are obtained from the equations of non-parallel electrodes (Chapter 4):

$$F_i = \frac{\epsilon_0 V^2 A_i}{2 d_i d_{i+1}} \tag{5.5}$$

$$x_i = l_i d_i d_{i+1} \left[\frac{1}{(d_{i+1} - d_i)^2} \ln \left(\frac{d_{i+1}}{d_i} \right) - \left(1 - \frac{d_i}{d_{i+1}} \right) \right] \tag{5.6}$$



(a)



(b)

Figure 5-1: (a) The lumped model for a parallel-plate capacitor with flexible movign plate; (b) Deformation of the i^{th} segment and corresponsing nodal springs and dispalcements (nodal linear springs are not shown in (a)).

The equations of static equilibrium are obtained from:

$$\frac{\partial(U-W)}{\partial d_i}=0 \quad , \quad i=1,...,n \tag{5.7}$$

Rearranging (5.7) in terms of nodal displacements results in a set of n nonlinear equations for n nodal displacements, d_i, as follows:

$$\begin{aligned}
&\left(\frac{kt_{i-1}}{l_{i-1}l_{i-2}}\right)d_{i-2}-\left[\frac{kt_i}{l_{i-1}}\left(\frac{1}{l_{i-1}}+\frac{1}{l_i}\right)+\frac{kt_{i-1}}{l_{i-1}}\left(\frac{1}{l_{i-2}}+\frac{1}{l_{i-1}}\right)\right]d_{i-1}\\
&+\left[kt_i\left(\frac{1}{l_{i-1}}+\frac{1}{l_i}\right)^2+\frac{kt_{i-1}}{l_{i-1}^2}+\frac{kt_{i+1}}{l_i^2}\right]d_i\\
&-\left[\frac{kt_i}{l_i}\left(\frac{1}{l_{i-1}}+\frac{1}{l_i}\right)+\frac{kt_{i+1}}{l_i}\left(\frac{1}{l_i}+\frac{1}{l_{i+1}}\right)\right]d_{i+1}+\left(\frac{kt_{i+1}}{l_il_{i+1}}\right)d_{i+2}+k_i\left(d_0-d_i\right)\\
=\;& F_i\left(\frac{x_i}{l_i}-1\right)-F_{i-1}\left(\frac{x_{i-1}}{l_{i-1}}\right) \qquad , \qquad i=1,...,n
\end{aligned} \tag{5.8}$$

Equations (5.8) can also be expressed in the following matrix form:

$$[K]\{d\}-d_0\{k\}-\{F(d)\}=0 \tag{5.9}$$

where $[K]$ represents the stiffness matrix including torsional and linear stiffness terms, $\{k\}$ represents the vector of nodal linear springs and $\{F(d)\}$ represents the vector of external electrostatic forces. Equation (5.9) is numerically solved for $\{d\}$ at any given voltage, V. The total capacitance is obtained from the summation of capacitances of $n-1$ segments:

$$C=\sum_{i=1}^{n-1}\frac{\epsilon_0 A_i}{d_{i+1}-d_i}\ln\left(\frac{d_{i+1}}{d_i}\right) \tag{5.10}$$

For a capacitor modeled by three segments of equal length ($l_1=l_2=l_3=l$ and $kt_1=kt_2=kt$), the stiffness matrix, $[K]$, and the vector of electrostatic nonlinear force, $\{F\}$, are (see Figure 5-2):

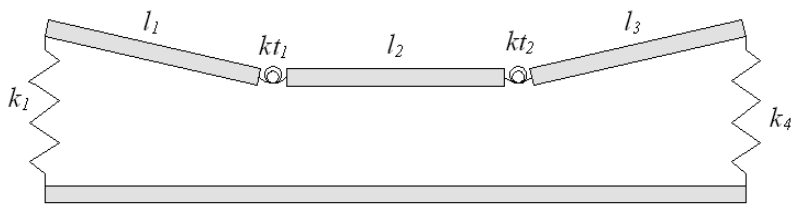


Figure 5-2: Three-segmented model of a flexible plate tunable capacitor.

$$[K] = \begin{bmatrix} \frac{kt}{l^2} + k_1 & -2\frac{kt}{l^2} & \frac{kt}{l^2} & 0 \\ -2\frac{kt}{l^2} & 5\frac{kt}{l^2} + k_2 & -4\frac{kt}{l^2} & \frac{kt}{l^2} \\ \frac{kt}{l^2} & -4\frac{kt}{l^2} & 5\frac{kt}{l^2} + k_3 & -2\frac{kt}{l^2} \\ 0 & \frac{kt}{l^2} & -2\frac{kt}{l^2} & \frac{kt}{l^2} + k_4 \end{bmatrix} \tag{5.11}$$

$$\{F\} = \begin{Bmatrix} F_1 - \frac{F_1 x_1}{l} \\ F_2 - \frac{F_2 x_2}{l} + \frac{F_1 x_1}{l} \\ F_3 - \frac{F_3 x_3}{l} + \frac{F_2 x_2}{l} \\ \frac{F_3 x_3}{l} \end{Bmatrix} \tag{5.12}$$

As an example, a parallel-plate capacitor with flexible moving electrode and following specifications is considered: $A = 400 \times 400\ \mu m^2$, $d_0 = 3\ \mu m$, $l = 133.3\ \mu m$, $kt = 7000\ \mu N.\mu m/rad$, $k_1 = k4 = 2.56\ N/m$ and for simplicity $k_2 = k_3 = 0$. The C-V response for this capacitor is compared to that of a similar capacitor with rigid plate in Figure 5-3. For the conventional capacitor, torsional rigidities are set to very large numbers (theoretically $kt_i = \infty$ for a rigid plate).

Figure 5-3 illustrates that in a flexible-plate capacitor, the applied voltage deforms the plate producing an uneven gap between two electrodes at different points. This causes earlier pull-in and decreases the overall capacitance at pull-in voltage leading to a lower tunability (39% for this example). If the torsional rigidities increase, the curve will be stretched to the right showing

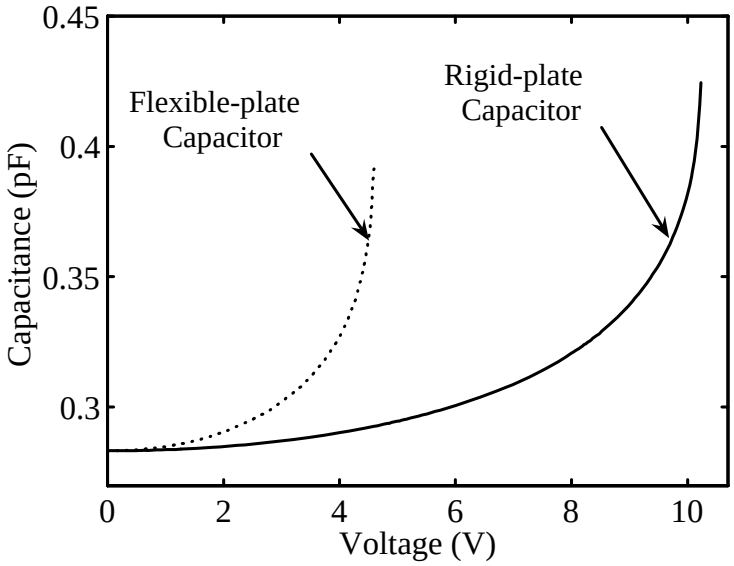


Figure 5-3: C-V responses for parallel-plate MEMS capacitors with flexible and rigid plates.

higher tunability. The C-V curve of the rigid-plate (conventional) capacitor is an asymptote for the family of curves as $kt \to \infty$.

5.3 Segmented-Plate Capacitors with Rigid Steps

5.3.1 Analytical Model and Design Optimization

Flexibility of the moving plate decreases the pull-in voltage and tunability, and it does not affect the linearity of the C-V response. However, the linearity of the C-V curve of a segmented-plate capacitor can be improved if the nodal displacements are constrained. Figure 5-4 shows the schematic representation of a capacitor with a three-segmented moving plate and rigid steps located under middle nodes, where the nodes are restricted to move vertically up to the corresponding steps. The segments are assumed to be rigid and each two adjacent segments are connected by torsional springs. The supporting beams have nonlinear stiffness due to axial deformations which are, in this case, higher than those of a parallel-plate capacitor (Chapter 3), because when the electrode displacement increases, the moving end of the beam has both vertical and horizontal displacements, as shown in Figure 5-5. The stiffness coefficient of each

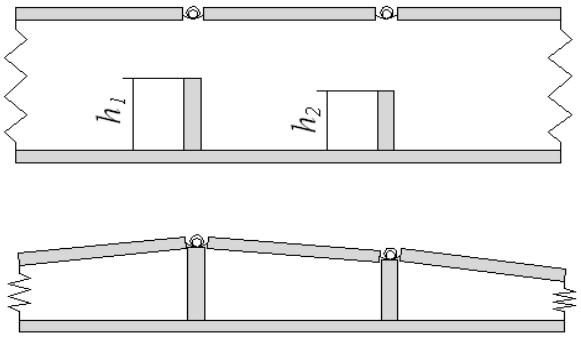


Figure 5-4: A three-segmented-plate tunable capacitor with rigid nodal steps.

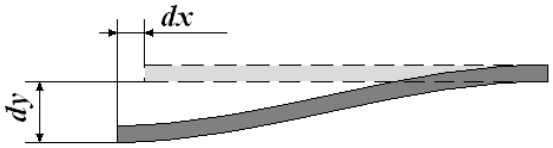


Figure 5-5: Horizontal and vertical displacements of the supporting beams in a segmented-plate capacitor.

supporting beam (uncoupled model), k, and connecting beam, kt, are obtained from:

$$k = k_B + k_T = \frac{12EI}{L_{S0}^3} + \frac{EA_S}{L_{S0}}\left(1 - \frac{L_{S0}}{\sqrt{dy^2 + (L_{S0} + dx)^2}}\right) \tag{5.13}$$

$$kt = \frac{Ew_t t^3}{12(1-\nu^2)l_t} \tag{5.14}$$

where l_t and w_t, shown in Figure 5-6, are the length and width of the connecting beams, respectively.

To study the capacitor's response to the actuation voltage, the steps are modeled as linear springs with stiffness coefficients equal to zero and infinity (10,000 $\mu N/\mu m$ in this thesis) before and after contact between node and step, respectively. Therefore, the equations of static equilibrium for this model are the same as (5.9). This equation is solved numerically to calculate nodal displacements and capacitance at each voltage. When the heights of steps change, the

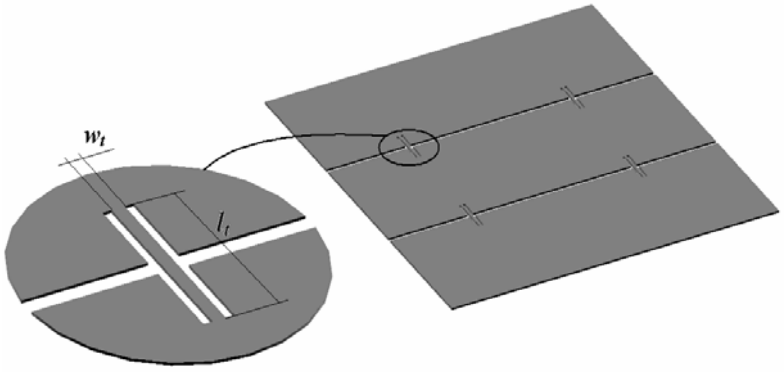


Figure 5-6: The segments and connecting beams with torsional stiffness.

shape of C-V curve, its linearity and maximum tunability also change. By solving an optimization problem, the best set of step heights, providing the highest linearity, is obtained. For the three-segmented-plate capacitor shown in Figure 5-4, the optimization problem is defined as:

$$\begin{aligned} \max \quad & LF(h_1, h_2) \\ \text{subject to} \quad & : \\ & h_1 \leq d_0 \\ & h_2 \leq d_1 \end{aligned} \tag{5.15}$$

where the step heights, h_1 and h_2, are the optimization variables and the constraints in (5.15) guarantee that higher linearity and tunability is achieved. The result of optimization for a silicon-based capacitor with elastic modulus $E = 165$ GPa is presented in Figure 5-7. The electrode size is $A = 200 \times 400\ \mu m^2$, the initial gap is $d_0 = 3\ \mu m$, the thickness of moving electrode is $2\ \mu m$. One can also add the stiffness coefficients to the optimization variables of (5.15), but this increases the number of iterations and several initial guesses may be required. In this thesis, the stiffness coefficients are separately optimized to avoid the complexity in the main optimization problem. The length and width of supporting beams are $100\ \mu m$ and $5\ \mu m$, respectively, and a set of two identical connecting beams, $l_t = 30\ \mu m$ and $w_t = 10\ \mu m$, are used

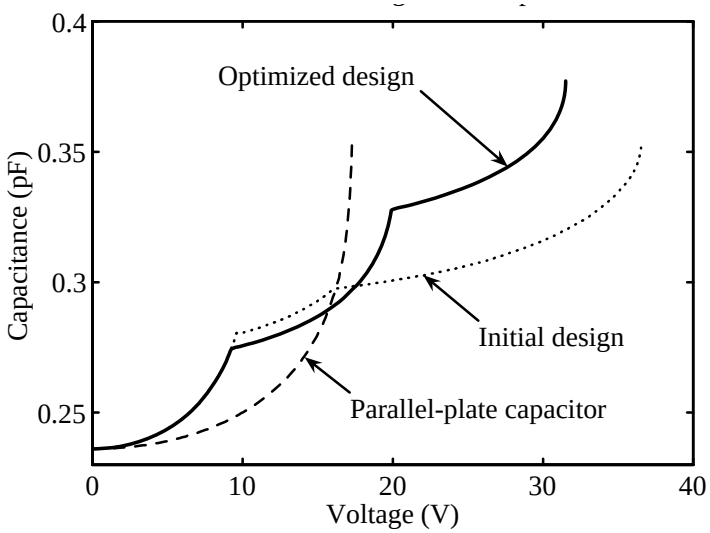


Figure 5-7: C-V responses for the three-segmented-plate capacitor before and after optimization compared to a conventional design.

to connect each two segments.

Due to the high level of nonlinearity of the governing equations (5.9) and (5.10), different initial guesses for h_i in the optimization problem may result in different final values. In Figure 5-7, the initial and optimized values for step heights are $h_0 = [2.4, 2.1]$ μm and $h = [2.46, 1.65]$ μm, respectively. The maximum tunabilities before and after optimization are 50% and 60%, respectively. The linearity factor, LF, has increased from 0.965 before optimization to 0.992 after optimization.

In order to investigate the effect of the number of segments on improving the linearity or tunability of a C-V curve, a symmetric six-segmented-plate capacitor with three independent step heights, h_1, h_2 and h_3, is modeled (see Figure 5-8-a). To maintain the high tunability of the final response, some constraints similar to those of (5.15), $h_0 > h_1$, $h_1 > h_2$ and $h_2 > h_3$, are added to specify the order of step heights. For a six-segmented-plate capacitor with plate size $A = 200 \times 400$ μm^2, the initial air gap $d_0 = 3$ μm and the plate thickness $t = 2$ μm, the results of design optimization are displayed in Figure 5-8-b. The supporting and connecting beams dimensions are $L_S = 100$ μm, $w = 5$ μm, $l_t = 40$ μm and $w_t = 15$ μm and there are two connecting beams between each two segments.

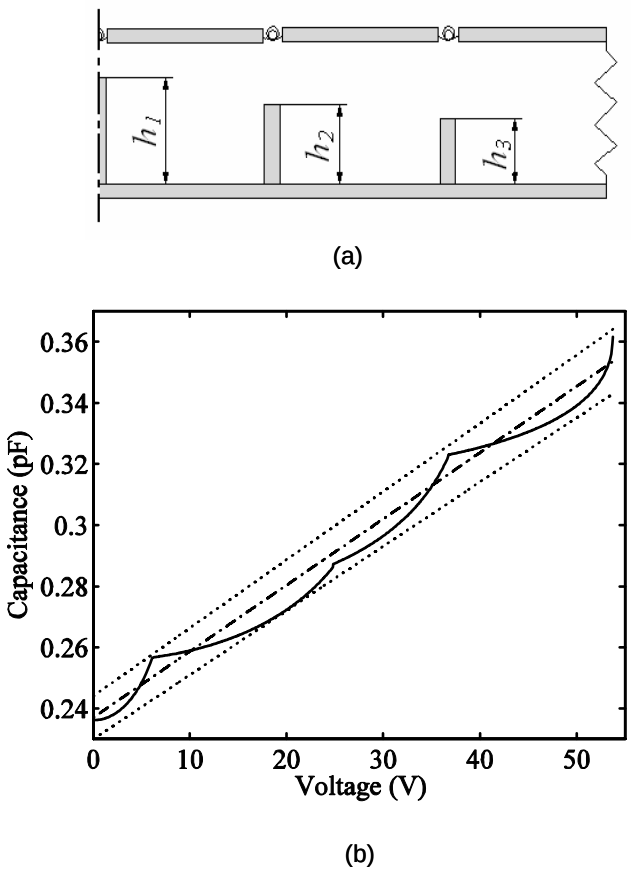


Figure 5-8: A symmetric six-segmented-plate capacitor: (a) The $\frac{1}{2}$ model; (b) The optimized C-V response (rigid line), its linear interpolation (dash-dotted line) and upper and lower bounds (dotted lines).

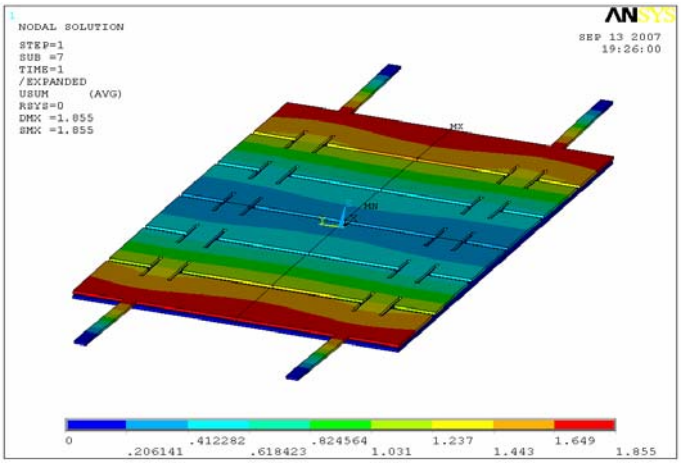
The linearity factor for the optimized design is found to be 0.994 and the upper and lower bounds which completely enclose the curve exhibit $\pm 3\%$ deviation from the linear interpolation presented in Figure 5-8-b. In this design, the tunability is also slightly improved from 50% to 53%. As shown in these examples, using segmentation technique and dimensional optimization leads to linear C-V curves while the tunability remains as high as that of a conventional parallel-plate capacitor.

5.3.2 Finite Element Analysis

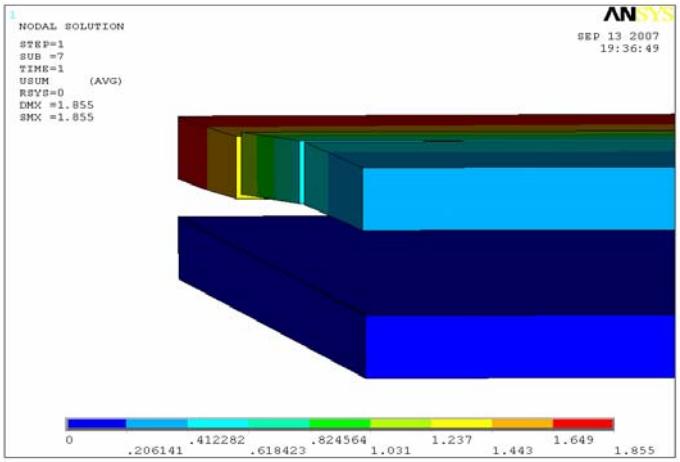
The applicability of the segmentation technique and the results of the analytical model are verified by performing a finite element analysis (FEA). The symmetric six-segmented-plate capacitor presented in the last section is modeled and the step heights $h_0 = [1.97, 2.47, 2.66, 2.47, 1.97]$ μm obtained from the analytical optimization are considered as the initial input for FEA. The beams length and width are 100 μm and 5 μm, respectively. The capacitance at each voltage is obtained using ANSYS® structural-electrostatic solver, ESSOLV, and SOILD186 and SOLID122 elements are used to model structural and electrostatic fields, respectively. The nonlinear geometry mode is activated which enables the model to include large deformations. Young's modulus and Poisson ratio are the same as those listed in Table 2.1.

The optimum step heights $h = [1.75, 2.47, 2.66, 2.47, 1.75]$ μm are obtained after three iterations and the results of simulations are presented in Figure 5-9 and 5-10. The linearity factor for the optimized dimensions is $LF = 0.994$ with maximum tunability of 58% (see Figure 5-10).

It should be mentioned that there are some differences between ANSYS® simulation results and those of the analytical (lumped) model, as illustrated in Figure 5-11. For example, the capacitance values extracted from FEM model are slightly higher than those of analytical calculations. This discrepancy may be associated, in part, with the fringing effect included in ANSYS® simulation. The difference between initial capacitance of two models is 0.0294 pF or 12.5%. The fringing effect for a conventional parallel-plate capacitor has been investigated using similar ANSYS® simulations. This can be done by changing the size of air box that models the electrostatic field and surrounds the capacitor. The results display 2 to 9 percent increase in initial capacitance (for different sizes of air box) comparing to the analytical value obtained from $C = \epsilon_0 A/d$. Considering the fact that each segment has four open edges producing extra fringing capacitance not included in the lumped model, and adding parasitic capacitances of connecting beams (i.e., torsional springs), 12.5% difference between ANSYS® and analytical model is consistent with the results of a conventional parallel-plate capacitor. If 0.0294 pF is added to the values obtained by analytical model to approximate the fringing effect, then this model will produce reasonably small error. Furthermore, the segments flexibility in ANSYS® model (see Figure 5-9-a) slightly increases the total capacitance, whereas the segments in the lumped model are assumed to be rigid. Even though these error sources may affect the precision of the



(a)



(b)

Figure 5-9: ANSYS® simulation for a six-segmented-plate capacitor; (a) The deformed moving segments; (b) Deformations of segments edges.

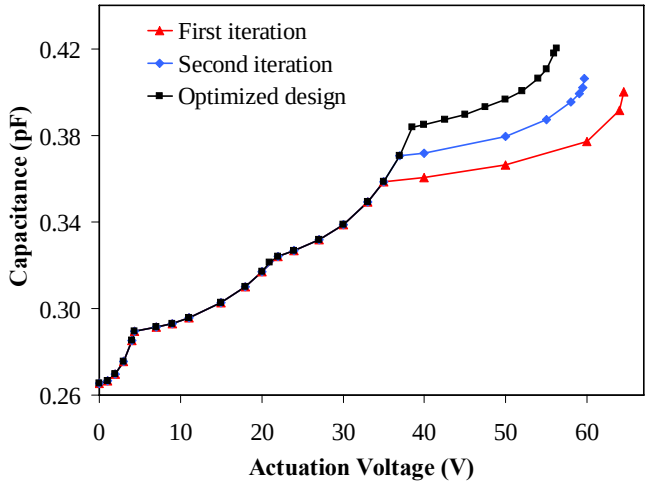


Figure 5-10: C-V responses for two iterations and optimized design.

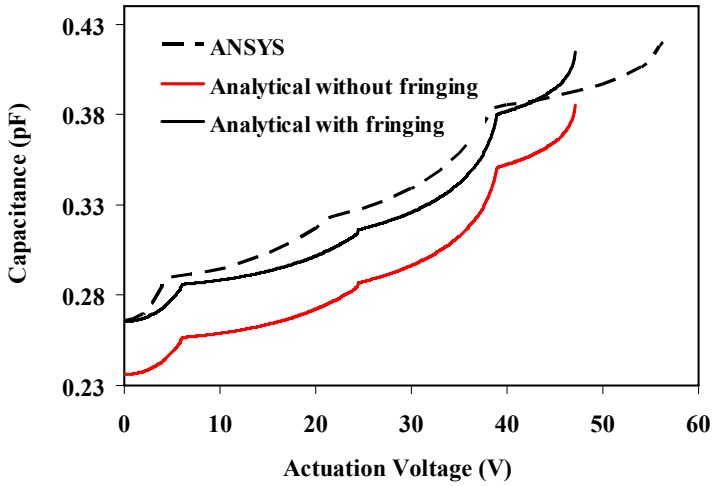


Figure 5-11: A comparison between the results of ANSYS® simulations and those of the analytical model for a set of step heights: $h = [1.75, 2.47, 2.66, 2.47, 1.75]$ μm (FEM optimized values).

analytical formulation, it is very time-efficient and fairly accurate for preliminary optimization stage. As presented in this section, the results of analytical optimization can be chosen as the input for FEM design, thus the computation time reduces drastically. The analytical simulation is over a thousand times faster than FEA. For example, the time required to obtain the C-V response presented in Figure 5-8-b for more than 1000 voltage samples is only few seconds, while using the same computer processor, ANSYS® simulations requires several hours to obtain the C-V response of Figure 5-10 with only 31 voltage samples.

5.3.3 The effect of fabrication uncertainties on capacitor performance

Conventional parallel-plate capacitors are highly sensitive to the deviation of the initial air gap and the thickness of supporting beams from the nominal values and as a result, small changes in these parameters cause large variations in C-V curves (this will be comprehensively discussed later in Chapter 6). In a segmented-plate capacitor, the linearity of the C-V response and the maximum tunability depend on the heights of the steps and therefore, it is important to study the effect of fabrication uncertainties on the capacitor performance. If the grey-tone mask is properly designed and calibrated, the main sources of deviations are over/underexposure during the photolithography, over/underetching or inaccuracies in thickness of different layers. In all these cases, the fabrication uncertainties have similar impact on all step heights, meaning that all steps are either longer or shorter than their nominal values and thus, the design parameters are correlated.

To examine the effect of fabrication tolerances on the segmented-plate capacitors responses, the six-segmented-plate capacitor of Figure 5-8 is studied. For simplicity of the analysis and in order to concentrate on the steps, it is assumed that the initial air gap and beams are accurate and take their nominal values. Two possible scenarios, Model I and Model II, are proposed to take the fabrication inaccuracies into account. In Model I, it is assumed that the deviations of step heights are proportional to the nominal values. This model is suitable to investigate the effect of inaccuracies in photolithography and RIE on the C-V response. The results of numerical simulations for cases of $\pm 5\%$ and $\pm 10\%$ deviations in step heights are presented in Figure 5-12-a. As portrayed in this figure, smaller step heights improve the maximum tunability, but reduce the curve linearity. In Model II, a constant value is added to all steps. This happens

if the thicknesses of photoresist or dielectric layers deviate from their nominal values. The same capacitor with two different level of inaccuracies is simulated and the results are presented in Figure 5-12-b. The dimensional deviations for steps heights are considered to be $\pm 0.15\ \mu m$ and $\pm 0.30\ \mu m$. As shown in this figure, similar behavior is observed for the second model. The tunability for capacitors with different level of inaccuracy (for both models) varies from 37% for largest set of steps to 74% for the shortest ones. The linearity factor also varies between 0.989 and 0.994 exhibiting small changes for different cases. As demonstrated by these numerical examples, the linearity of segmented-plate capacitors exhibit low sensitivity to the deviation of step heights from their nominal values.

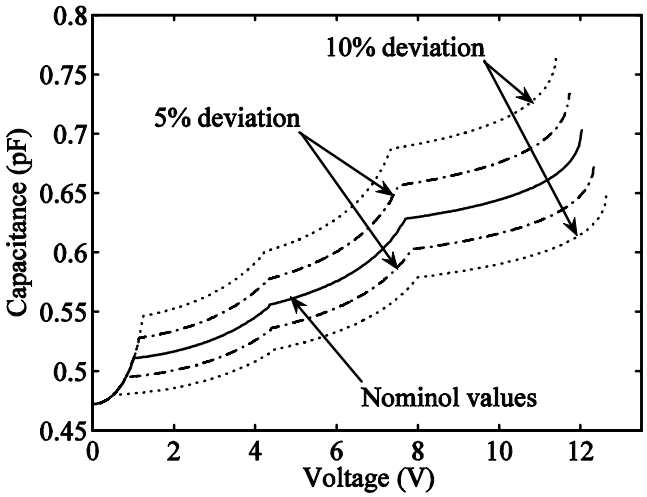
5.4 Segmented-Plate Capacitors with Flexible Steps

5.4.1 Two-Segmented-Plate Capacitors

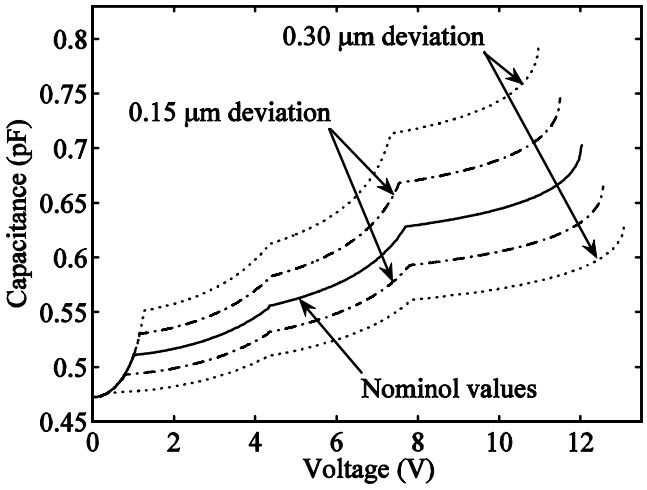
The use of segmentation technique and nonlinear springs improve the linearity of a MEMS tunable capacitor, but require a customized fabrication process. To be able to utilize this technique in a standard process, a new design with simpler geometry (using only two segments) and a modified "flexible" step is developed as shown in Figure 5-13. The middle spring has an initial distance, h, from the fixed plate, and after the middle node touches the step, it will continue to move downward with a slower rate providing smoother C-V response and higher tunability. The equation of static equilibrium in matrix form for this device is written as:

$$\begin{aligned}
&\begin{bmatrix}
\frac{kt}{l_1^2}+k_1 & -\frac{kt}{l_1}\left(\frac{1}{l_1}+\frac{1}{l_2}\right) & \frac{kt}{l_1 l_2} \\
-\frac{kt}{l_1}\left(\frac{1}{l_1}+\frac{1}{l_2}\right) & kt\left(\frac{1}{l_1}+\frac{1}{l_2}\right)^2+k_2 & -\frac{kt}{l_1}\left(\frac{1}{l_1}+\frac{1}{l_2}\right) \\
\frac{kt}{l_1 l_2} & -\frac{kt}{l_1}\left(\frac{1}{l_1}+\frac{1}{l_2}\right) & \frac{kt}{l_2}\left(\frac{1}{l_1}+\frac{1}{l_2}\right)+k_3
\end{bmatrix}
\begin{Bmatrix} d_1 \\ d_2 \\ d_3 \end{Bmatrix} \\
= \; & d_0 \begin{Bmatrix} k_1 \\ k_2 \\ k_3 \end{Bmatrix} - \begin{Bmatrix} F_1 - \frac{x_1 F_1}{l_1} \\ F_2 - \frac{x_2 F_2}{l_2} + \frac{x_1 F_1}{l_1} \\ \frac{x_2 F_2}{l_2} \end{Bmatrix}
\end{aligned} \tag{5.16}$$

where $k_2 = 0$ for $d_2 \geq h$. All three springs have nonlinear stiffness coefficients. For a capacitor with dimensions: $A_{total} = 400 \times 400\ \mu m^2$, $d_0 = 2.75\ \mu m$, $h = 2\ \mu m$ and $l_1 = l_2$ (see Figure



(a)



(b)

Figure 5-12: The effect of fabrication inaccuracies on C-V response of a six-segmented-plate capacitor: (a) Model I, (b) Model II.

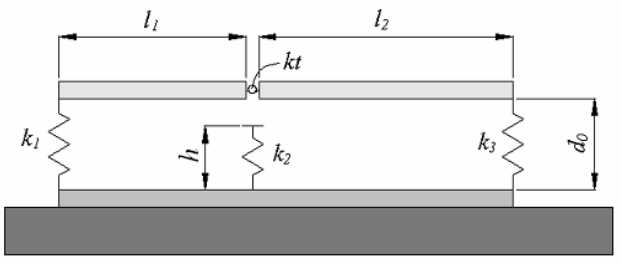


Figure 5-13: A modified two-segmented-plate capacitor with a flexible step.

5-13), the C-V response is shown in Figure 5-14. The total tunability of the capacitor is 99%, where the low sensitive part (solid line) has 47% tunability with linearity factor of $LF = 0.970$. The dash-dot line represents the linear interpolation of the low sensitive region.

Although the linearity of C-V response for this design is less than three- or six-segmented-plate capacitors introduced before, it can be used as a highly tunable, low sensitive capacitor. It is also possible to optimize design parameters including the length of segments, the stiffness coefficients of the springs or the height of middle spring, h, to achieve higher linearity within the low sensitive region of the curve. The optimization problem is then defined as follows:

$$\begin{aligned} \max \ & LF(a, r, d) \\ \text{subject to} \ & : \\ & a \leq 1 \\ & r \geq 1 \\ & d \leq d_0 \end{aligned} \tag{5.17}$$

where a is the ratio of the segments length, $a = l_2/l_1$, and r is the ratio of supporting beams length, $r = L_{S3}/L_{S1}$. Figure 5-15-a presents the response of a capacitor with optimized design parameters: $a = 0.6$, $r = 1.3$ and $h = 2.1\ \mu m$. The LF for this capacitor in linear-like low sensitive region (solid line) is 0.987 with 51% tunability, where the total tunability is increased to 108%. The design exhibits higher tunability and the linear part has a tunability as high as a conventional parallel-plate capacitor. If h is assumed to be fixed (as is the case in standard

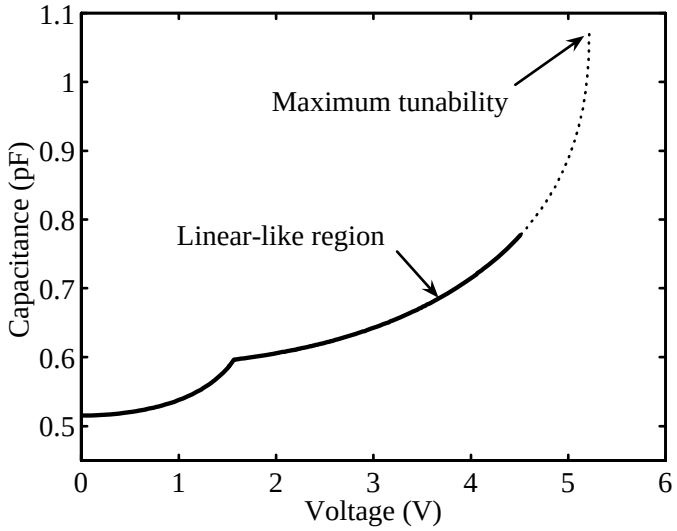


Figure 5-14: The C-V curve for a two-segmented-plate capacitor with flexible middle step. The dotted and solid lines respresnt the maximum and linear-like tunability, respectively.

processes like PolyMUMPs), then k_2 can be replaced in the optimization problem as the new design parameter. Solving the problem for the new set of design variables results in a higher linear tunability, where for the low sensitive region $LF = 0.990$ and the tunability is 57%. The total tunability for this design is 108% and the C-V curve is displayed in Figure 5-15-b.

5.4.2 Butterfly-Shape Linear Capacitors

Design Development

The idea of placing a flexible step under central node in two-segmented-plate capacitors improved the maximum tunability, because it allows larger segments displacements. However, the low sensitive part of response is not highly linear yet. As shown in aforementioned sections, when the number of steps increases, the C-V response is broken into smaller curves leading to higher linearity. Therefore, if similar steps are added under the first and last nodes of a two-segmented plate capacitor, then higher tunability and linearity are expected. Furthermore, one can optimize the geometry of the capacitor to further improve the linearity of the response by changing the shape of the electrodes from rectangular to trapezoidal, where the width of

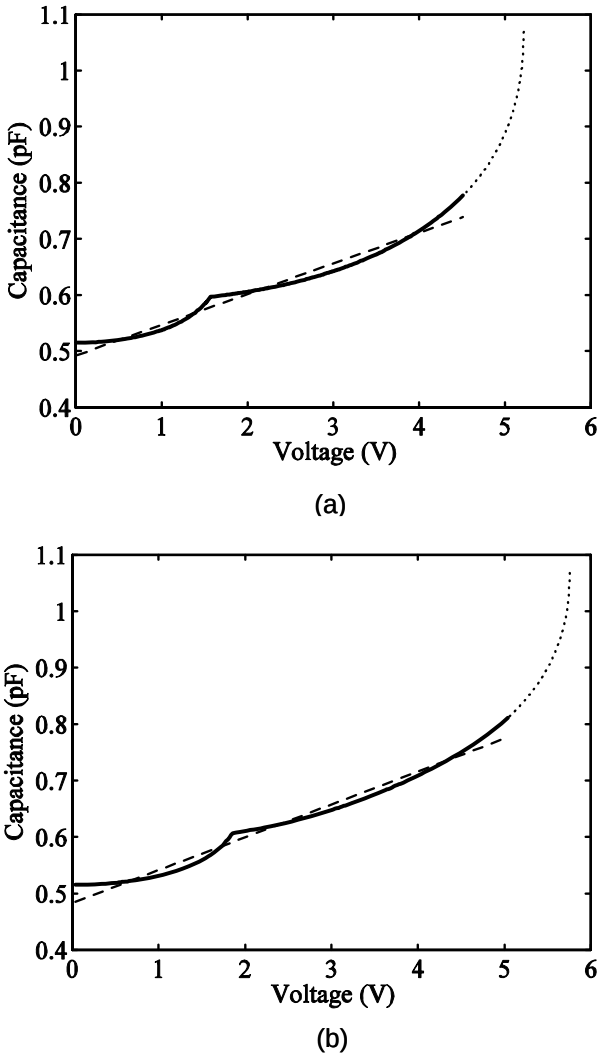


Figure 5-15: C-V curves for optimized two-segmented-plate capacitors with different optimization scenarios. (a) The height of the middle step is a design variable; (b) Middle spring's stiffness is a design variable (Dashed, solid and dotted lines represent the linear interpolations, linear region and the end part of the curves, respectively).

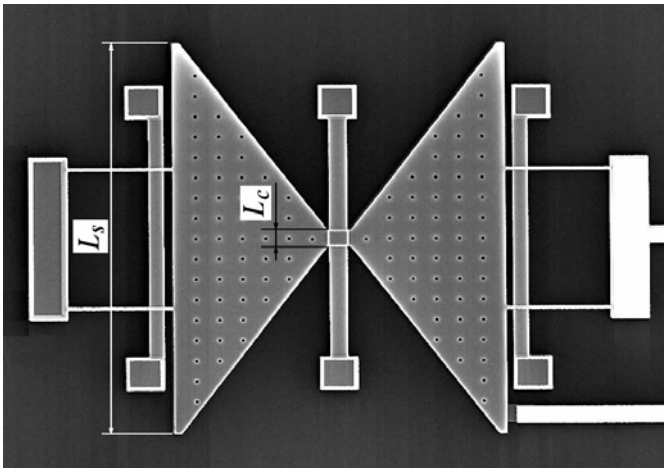


Figure 5-16: SEM image of a butterfly-shape MEMS tunable capacitor fabricated with Poly-MUMPs.

segments at sides are larger than center. The capacitor then looks like a butterfly as depicted in Figure 5-16. For this capacitor, the equations of static equilibrium is the same as (5.16), where the electrostatic forces and moments acting on the segments are obtained from (4.6) and (4.7) as:

$$F_i = \frac{\varepsilon_0 V^2}{2}\left[\frac{\alpha}{\beta_i}\ln\left(\frac{d_{i+1}}{d_i}\right) + \frac{L_i l_i}{d_i d_{i+1}} - \frac{\alpha l_i}{\beta_i d_{i+1}}\right] \quad , \quad i = 1, 2 \tag{5.18}$$

$$x_i F_i = \frac{\varepsilon_0 V^2}{2 d_{i+1}\beta_i^3}\left[d_{i+1}\ln\left(\frac{d_{i+1}}{d_i}\right)(\beta_i L_i - 2\alpha L_i) + \alpha\beta_i l_i\,(d_i + d_{i+1}) - \beta_i^2 L_i l_i\right] \quad , \quad i = 1, 2 \tag{5.19}$$

Here, $\beta_i = (d_{i+1} - d_i)/l_i$, $\alpha = (L_s - L_c)/l_i$, $L_1 = L_3 = L_s$, $L_2 = L_c$ and L_s and L_c are the width of the segments at sides and center of the electrodes, respectively, as shown in Figure 5-16. The device has dimensions: $d_0 = 2.75\ \mu m$, $h = 2\ \mu m$, $L_s = 575\ \mu m$, $L_c = 25\ \mu m$ and $l_1 = l_2 = 200\ \mu m$. The C-V response for this butterfly-shape capacitor is presented in Figure 5-17. The total tunability is 97%, where the linear tunability (i.e., the tunability of linear-like region specified by solid line in the figure) is 70% and the linearity factor, LF, is 0.994 displaying a reasonable improvement comparing to segmented-plate capacitors.

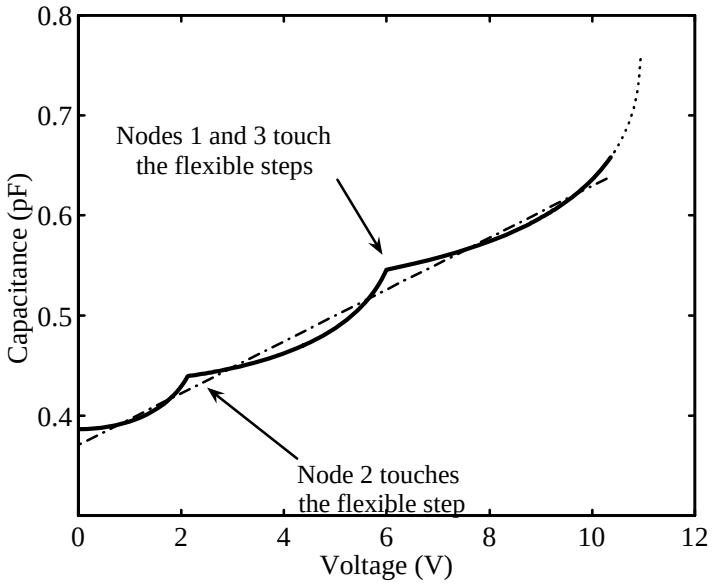


Figure 5-17: C-V curve for a butterfly-shape MEMS capacitor. Dash-dotted line represents the linear interpolation of linear-like low sensitive region.

Fabrication and Test

A butterfly-shape capacitor fabricated with PolyMUMPs is presented in Figure 5-16. The fixed electrode, flexible steps and segments are made by Poly0, Poly1 and Poly2 layers, respectively. The electrodes dimensions are: $L_s = 575\ \mu m$, $L_c = 25\ \mu m$ and $l_1 = l_2 = 200\ \mu m$.

The intrinsic parasitic capacitances are extracted from the model shown in Figure 5-18. The terms C_P, C_{MB}, C_{FB}, C_{MS}, C_{AS} and C_{FS} represent parasitic capacitances of measurement probes, moving plate-beams, fixed plate-beams, moving plate-substrate, anchors-substrate and fixed plate-substrate, respectively, and C_0 is the capacitance between two electrodes. Each parasitic term is extracted from C-matrix obtained from ANSYS® and CoventorWare^{TM} and the results are summarized in Table 5.1. The overall simulated parasitic capacitance is calculated as: $C_{par} = 9.902\ pF$ which must be subtracted from the measured values to obtain the capacitance between two electrodes at each voltage.

As presented in Table 5.1, the effect of silicon nitride (insulator) layer in parasitic capacitances C_{AS} and C_{FS} is quite noticeable and hence, the total parasitic capacitance is sensitive to

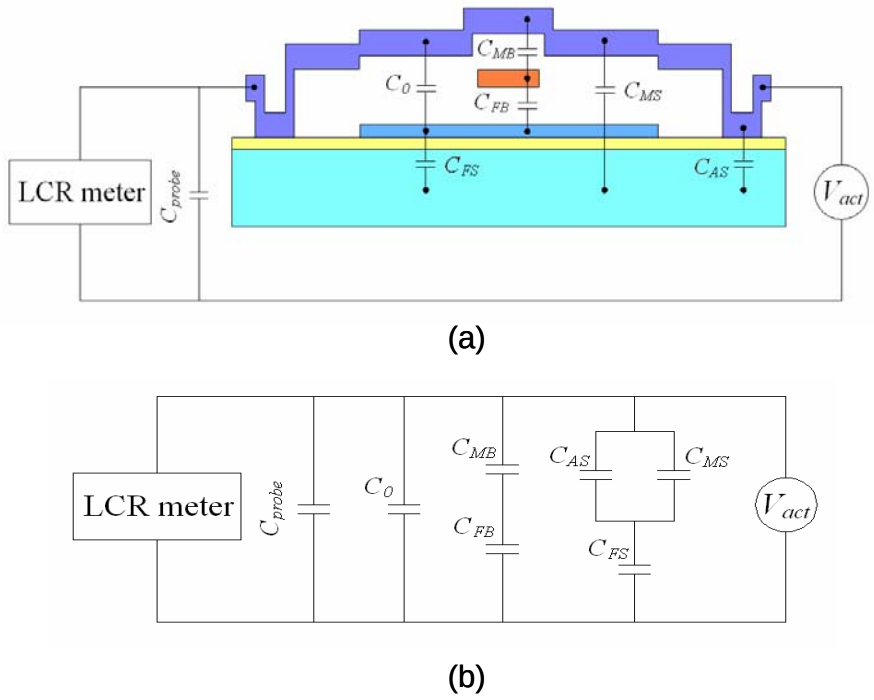


Figure 5-18: (a) The parasitic capacitances for a butterfly-shape capacitor fabricated with PolyMUMPs; (b) The equivalent circuit.

Table 5.1: The parasitic capacitances extracted from FEA simulations

Capacitance	Value (pF)
C_P	1.820
C_{MB}	0.047
C_{FB}	0.034
C_{MS}	0.366
C_{AS}	11.314
C_{FS}	25.514

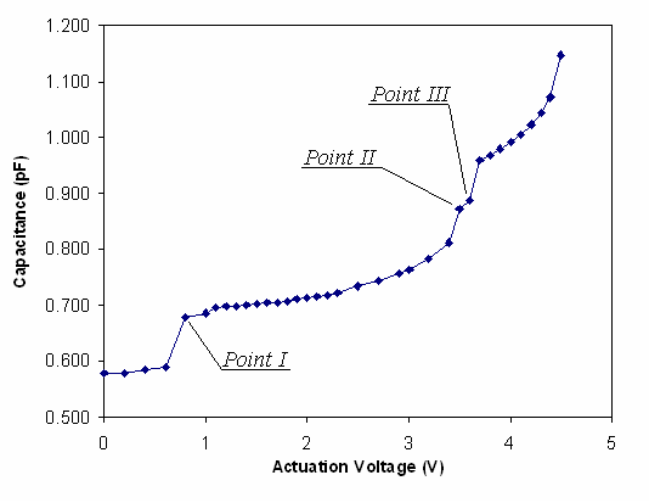


Figure 5-19: C-V response for a butterfly-shape capacitor measured by the LCR meter; Points I, II and III, represent the contact between segments and lateral beams at node, 2,1 and 3 respectively.

the thickness of this layer. The capacitance-voltage response was measured by Agilent E4890A Precision LCR meter. For the capacitor shown in Figure 5-16, the C-V response is presented in Figure 5-19. The total tunability is 99% which is comparable to 97% of the analytical model.

The measured initial capacitance after subtracting the parasitic values is 0.577 pF, where the initial capacitance obtained from analytical equation is 0.386 pF. The 3D image of the capacitor before applying actuation voltage created by WYKO NT1100 Optical Profiler is used to investigate the difference between analytical and measured values (see Figures 5-20-a and 5-20-b). The theoretical thickness of Poly0 and Poly2 are 0.5 μm and 1.5 μm, respectively, and the gap between Poly0 and Poly2 layers is 2.75 μm. The actual gap between two electrodes was observed to vary from 2.8 μm at the edges to 1.9 μm close to the central node assuming that the layers thicknesses are the same as designed values. As one can see in Figure 5-19, the gap between electrodes for most of the electrodes area is less than 2 μm which increases the initial capacitance. Using the average actual initial gap $d_0 = 2.0$ μm the theoretical initial capacitance is obtained as $C_0 = 0.531$ pF which is comparable to the measured value, 0.577 pF, and exhibits small difference of 9% which, as explained before, can be attributed to the neglected fringing effect. The difference between the actual and theoretical initial gaps may be

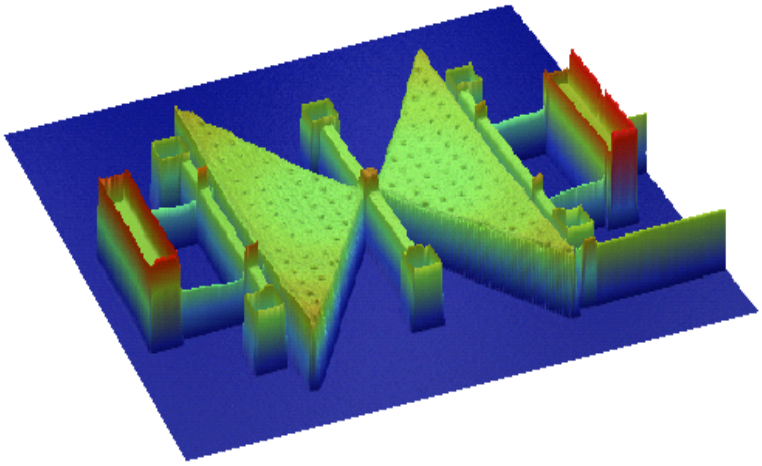
associated with residual stresses that bend the segments and decrease the gap.

Design Optimization for a highly Linear C-V Response

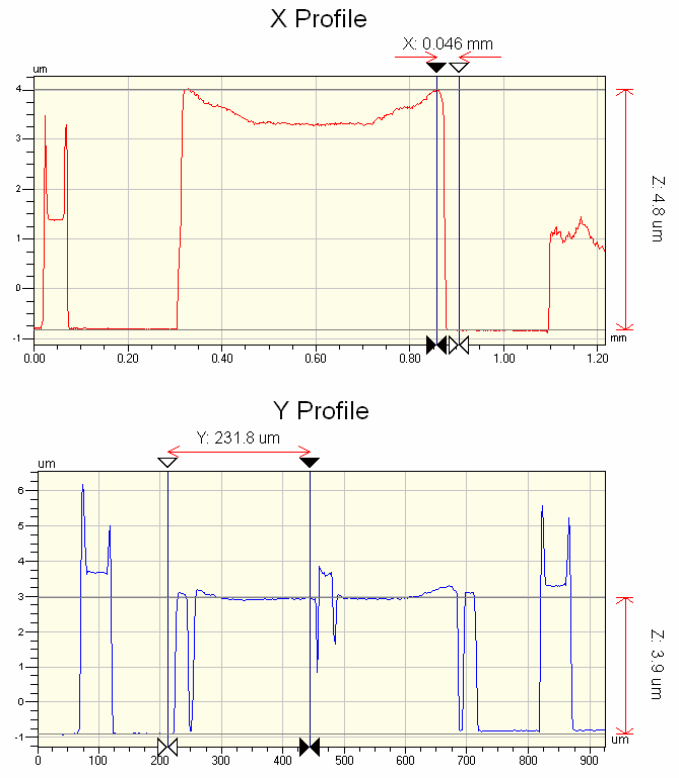
A closer look at the C-V response in Figure 5-19, suggests that node 1 and 3 do not touch the corresponding steps at the same time due to fabrication tolerances which alters the symmetry of the capacitor (see distinct Point II and Point III in Figure 5-19, which must be the same for a perfectly symmetric structure). This characteristic can be advantageously exploited to increase the number of discontinuities in C-V response and to improve its linearity. If the two segments and corresponding supporting beams have different dimensions, then after applying the bias voltage, the nodal positions d_1 and d_3 will not be the same. Consequently, the flexible steps at nodes 1 and 3 are not added to the structural stiffness at the same time and as a result, the resulting curve will have three discontinuities. An asymmetric design can be achieved by setting $l_1 \neq l_2$ and $k_1 \neq k_3$. In this case, the electrostatic and resistive forces for two segments are different causing uneven nodal deformations d_1 and d_3. To maximize the linearity, an optimization problem with parameters: $a = l_2/l_1$, $r = k_3/k_1$, kt and k_2 is solved as follows:

$$\begin{aligned} \max \ & LF(a, r, kt, k_2) \\ \text{subject to} \ & : \\ a &\leq 1 \\ r &\leq 1 \\ k_2 &\leq k_0 \\ kt &\leq kt_0 \end{aligned} \tag{5.20}$$

where k_0 and kt_0 are the upper limits of optimization parameters k_2 and kt, respectively. The optimized parameters are: $a = 0.8$, $r = 0.8$, $k_2 = 12.16\ \mu N/\mu m$ and $kt = 3200\ \mu N.\mu m/rad.$ The characteristic d-V and C-V responses of the new optimized design are shown in Figure 5-21. As displayed in this figure, the asymmetric geometry causes different nodal displacements at two sides which results in a highly linear C-V response. The total tunability (dotted curve in Figure 5-21-b) is 89% where the linear region exhibits high linearity of $LF = 0.998$ and tunability of 68%.



(a)



(b)

Figure 5-20: (a) 3D image of the butterfly-shape capacitor created by WYKO NT1100 Optical Profiler; (b) Profile of the moving electrode in two perpendicular directions.

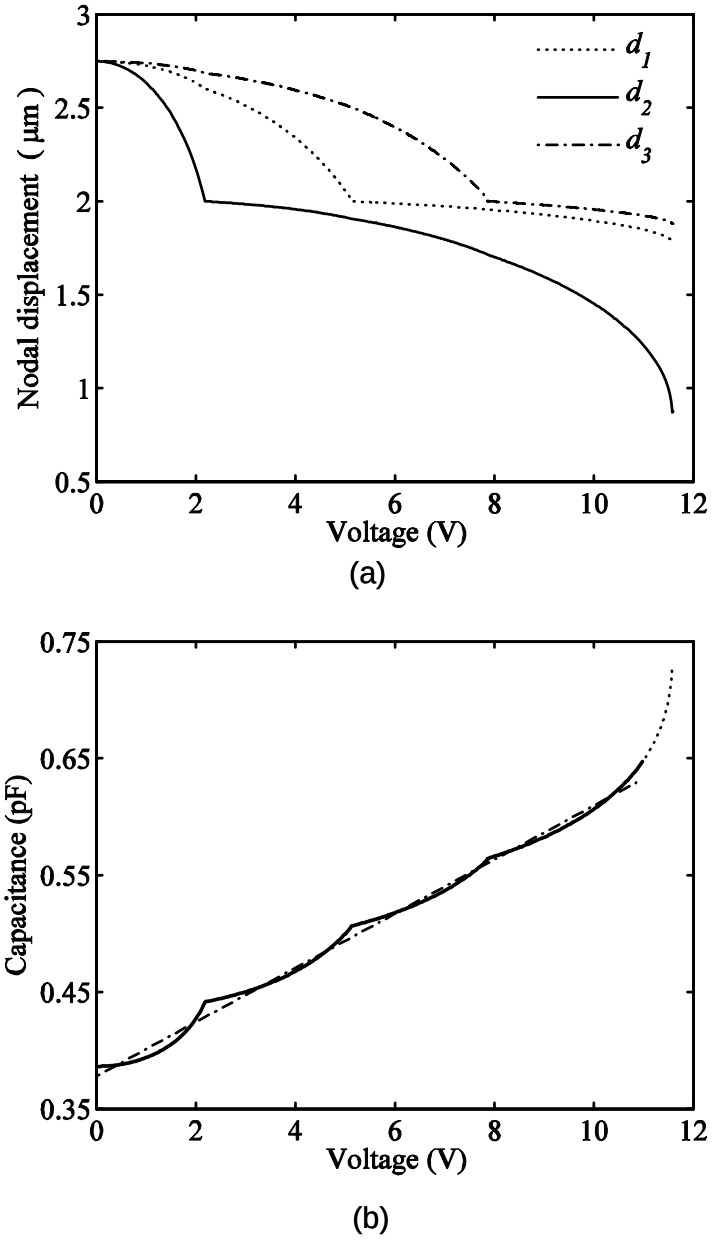


Figure 5-21: Characteristic curves of an optimized butterfly-shape capacitor: (a) Nodal displacment-voltage response; (b) Capacitance-voltage response.

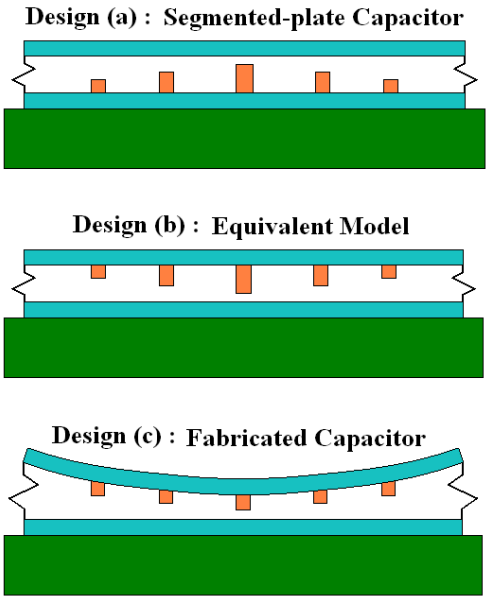


Figure 5-22: (a) A segmented-plate capacitor; (b) its equivalent model and (c) a teeth-equipped capacitor.

5.5 Linearly Tunable Capacitors with Flexible Plates

5.5.1 Linear Capacitors with Bent Plates

The rigid steps used in segmented-plate capacitors restrict the displacement of the moving electrodes and linearize the C-V responses. Increasing the number of steps improves the linearity of the curve and on the other hand, it creates more complexity in the fabrication process. Using the effect of residual stress on the moving plate, a new design with conceptual similarity to segmented-plate capacitors and a simpler fabrication process is developed.

As portrayed in Figure 5-22, the gap between each step and the electrode for segmented design (a) and its equivalent design (b) is the same and therefore, the two designs are expected to have similar C-V responses. Since fabrication of design (b) has the same challenges of the segmented-plate one, a capacitor with similar (and not exactly the same) behavior is introduced which can be fabricated with PolyMUMPs. The curvature of the moving plate is created by residual stress in Poly2 layer, where the steps are built using DIMPLE layer. The image created by optical profiler (Figure 5-23) shows that the moving plate has two different radii

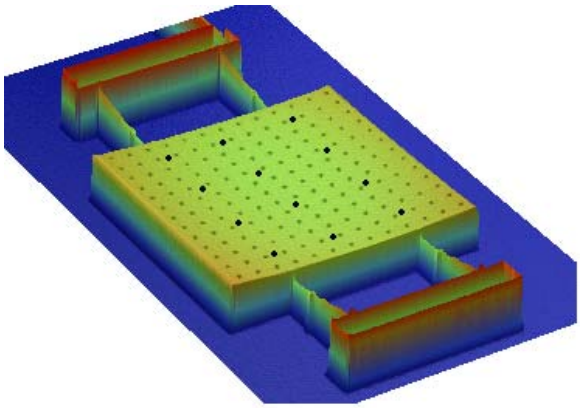
of curvature in two directions. Therefore, adding an array of teeth in two directions, instead of steps, increases the linearity of the response because the initial distances between the teeth and fixed electrode vary in two directions (see Figure 5-23-a). Therefore, when the bias voltage increases each tooth touches the fixed plate at a different voltage. This modification is the key advantage of the modified design over a segmented-plate capacitor.

The ΔC-V responses of four similar teeth-equipped capacitors are compared with ANSYS simulations in Figure 5-24. The ANSYS model was built based on the surface profile of the capacitor shown in Figure 5-23 and the results of simulation are presented in Figure 5-25. The deformations of the The parasitic capacitances are calculated and subtracted from measured values, $C_{par} = 8.652$ pF, and an average initial gap of 1.8 μm for all samples is considered in the calculation of parasitic term C_{MS} (moving plate-substrate). The tunability of four samples vary from 55% to 68% as shown in Figure 5-24 and the curves exhibit high linearity ranging from 0.9904 to 0.9967.

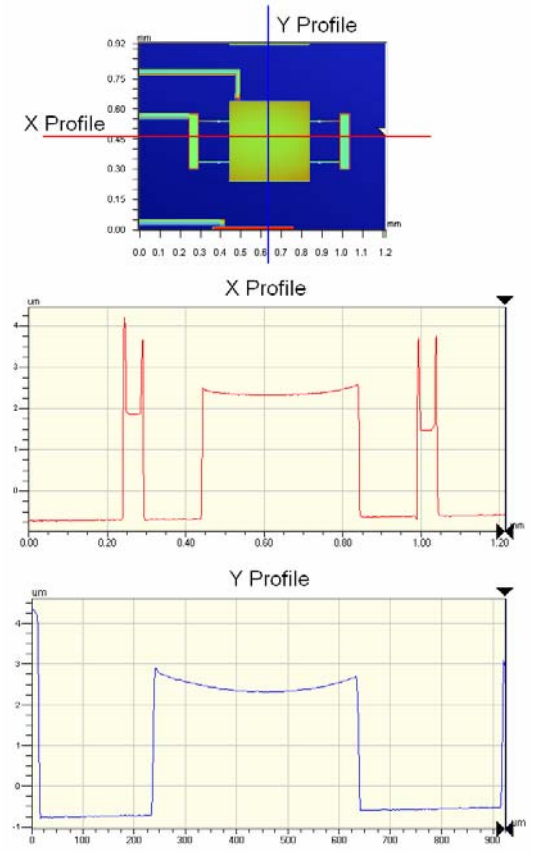
It is worth mentioning that fabricated capacitors may have different radii of curvature since the residual stress in the plate varies from one chip to another. Even though the simple structure and fabrication process is a major advantage of teeth-equipped capacitors over segmented-plate ones, however, developing a process with accurate residual stress and electrode curvature is a challenging task. It is possible to deposit a highly stressed layer (e.g., Metal layer in PolyMUMPs) on top of the moving electrode to increase the stress gradient and the curvature of the plates. The shape of the Metal layer on top of the moving electrode and the positions of the teeth can then be optimized to produce a desired curvature and to provide high linearity. This requires a complex FEM modeling to include the residual stress and contact in a multi-layer-electrode electrostatic-structural coupled filed.

5.5.2 Capacitors with Fixed-Edge Flexible Electrodes

The assumption of rigid moving plates and beams with constant stiffness coefficients in conventional parallel-plate capacitors produces negligible error for soft beams and small plate sizes and displacements. If the size of moving electrode increases or its boundary conditions (B.C.) are changed to fixed-edge, the distributed electrostatic force causes deformations in the plate [67] as depicted in Figure 5-26. The coupled electrostatic-structural governing equations,in this



(a)



(b)

Figure 5-23: (a) The image of a teeth-equiped capacitor and different radii of curvature in two directions. The teeth are shown by black spots. (b) The curvature of the electrode in two directions.

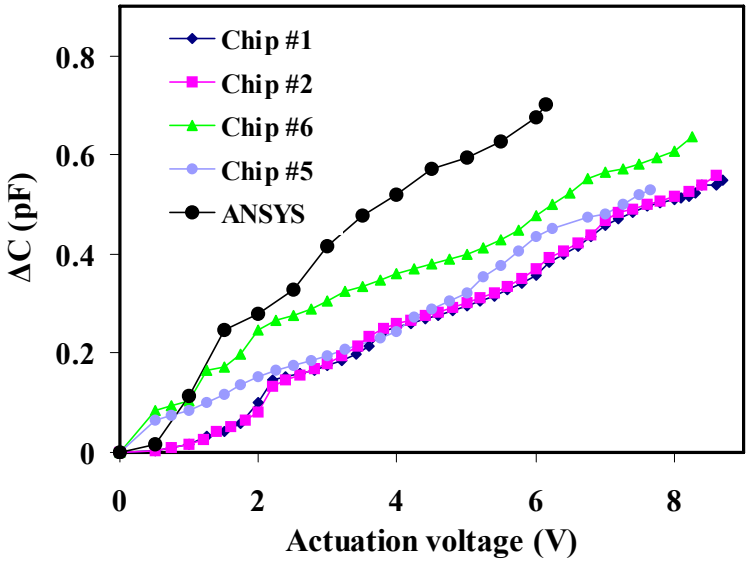
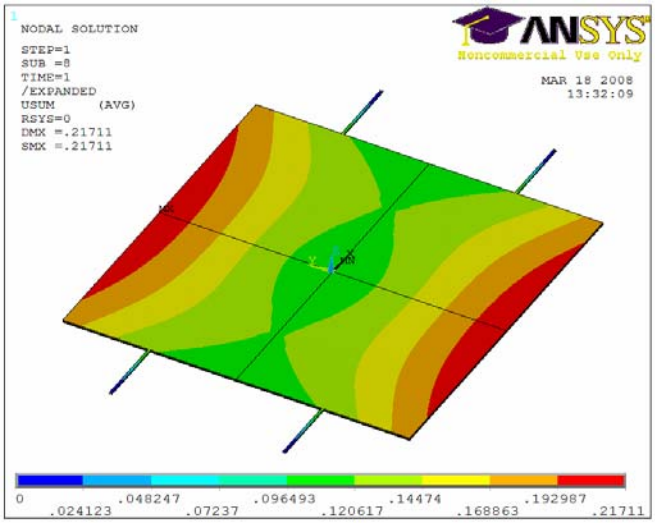


Figure 5-24: The measured tunability reponses (ΔC-V) of four identical teeth-equipped capacitors with curved moving plate compared with the ANSYS model.

case, do not have closed-form solutions and should be solved numerically.

Figure 5-27 displays the C-V response of a capacitor with rectangular moving electrode fixed at its two ends. The dimensions of fixed and moving plates are 630×200 μm^2 and 830×200 μm^2, respectively, with 2.75 μm initial air gap. The capacitance at each bias voltage is obtained using ANSYS® ESSOLV macro and element types for structural and electrostatic fields are SOLID186 and SOLID 122, respectively. A $\frac{1}{4}$ model (with symmetric boundary conditions) is used to reduce the simulation time. Young's modulus and Poisson ratio are: $E = 160$ GPa and $\nu = 0.22$, respectively (obtained from Table 2.1). Since the governing equations of this capacitor are different from those of a conventional rigid-plate model, the maximum tunability increases to 65%. As shown in Figure 5-27, the curve is highly nonlinear and very sensitive to voltage changes near pull-in. For instance, 12% of the total tunability is obtained by only 0.061 V change in actuation voltage.

To examine the convergence rate of ESSOLV, a convergence test was performed and initial capacitance of the C-V response was obtained from a model with different element sizes. In this analysis, the size of elements is fixed along the electrode width and changes lengthwise by



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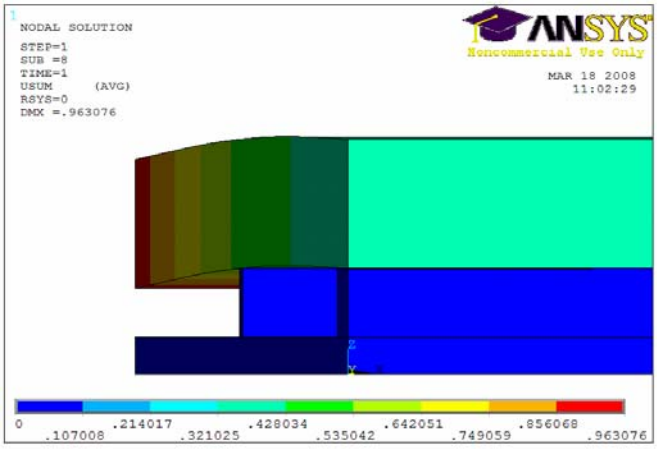


(b)

Figure 5-25: ANSYS simulations of a teeth-equipped capacitor with curved electrode. (a) The moving electrode deformations; (b) Contact between teeth and fixed electrode.

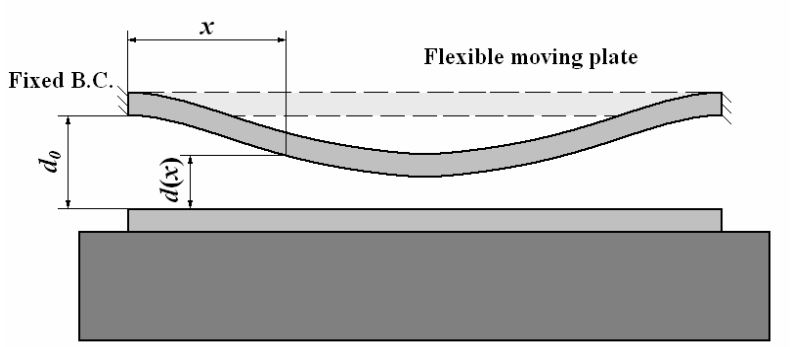


Figure 5-26: A parallel-plate tunable capacitor with flexible moving electrode and fixed-fixed boundary conditions.

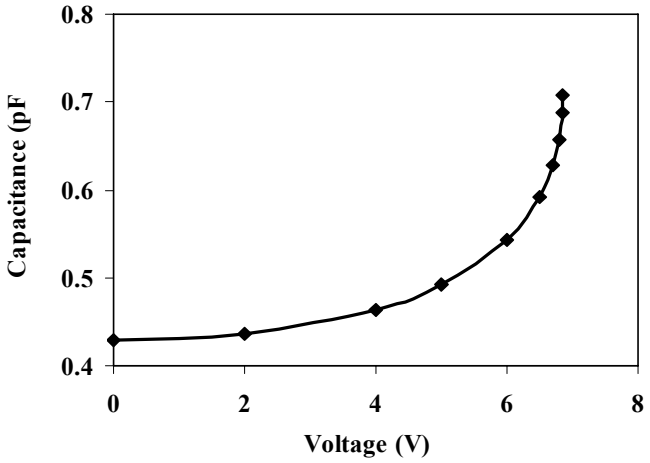


Figure 5-27: The C-V response of a capacitor with flexible rectangular plate obtained from ANSYS® FEM modeling.

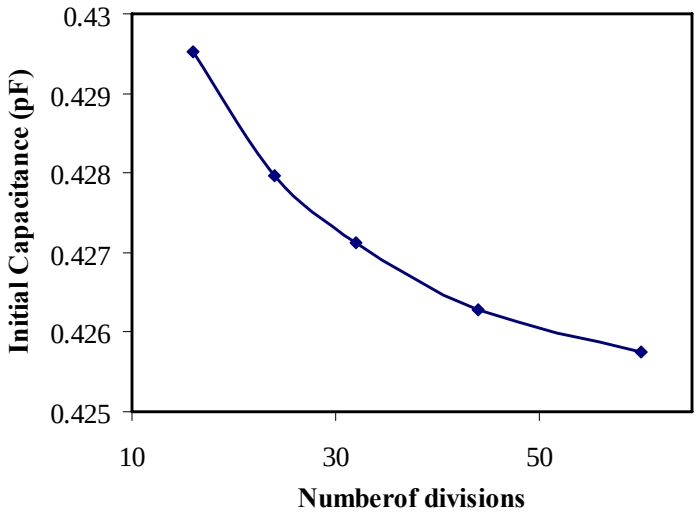


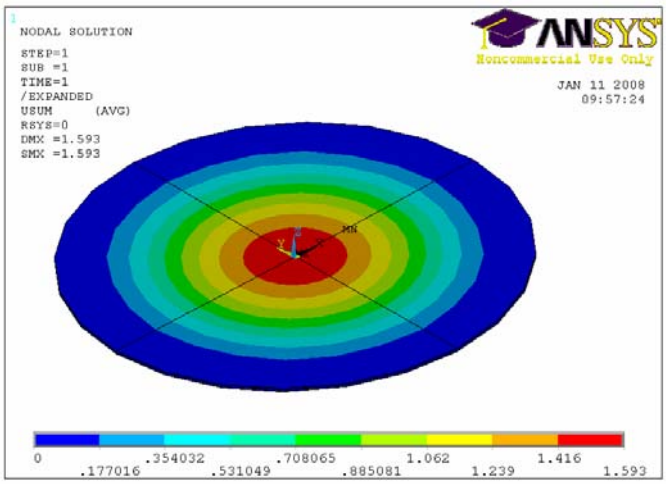
Figure 5-28: The result of convergence test for a rectangular-plate capacitor with different element sizes.

increasing the number of element divisions. The results are presented in Figure 5-28. As shown in this figure, the initial capacitance reduces with the size of element. The maximum error observed in thsis study is less than 1%.

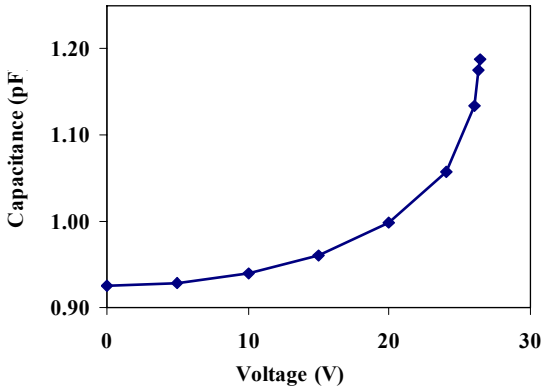
A circular-plate capacitor with fixed B.C. (Figure 5-29-a) was then modeled and the higher structural stiffness of this design (compared to rectangular electrode) increases the actuation voltage and the maximum tunability reduces to 28% as displayed in Figure 5-29-b. The radius of both fixed and moving electrodes is 300 μm and the initial gap is 2.75 μm. This example demonstrates the fact that higher structural stiffness in a capacitor increases the actuation voltage but does not necessarily improve tunability.

Linearly Tunable Capacitors

Flexibility of the moving electrode may change the tunability of a capacitor; nevertheless, the C-V curve remains nonlinear and highly sensitive to the voltage change near the pull-in. In order to reduce the sensitivity and to linearize the response, a novel design is developed. PolyMUMPs, with its dimensional constraints, is considered as the fabrication process to demonstrate the capabilities of the proposed design approach.



(a)



(b)

Figure 5-29: (a) Deformation of a circular moving electrode with fixed B.C. before pull-in; (b) The corresponding C-V response.

Figure 5-30: CoventorWare^{TM} simulation of three gaps which can be fabricated with PolyMUMPs.

Table 5.2: Tunability and linearity for flexible-plate capacitors with different design parameters

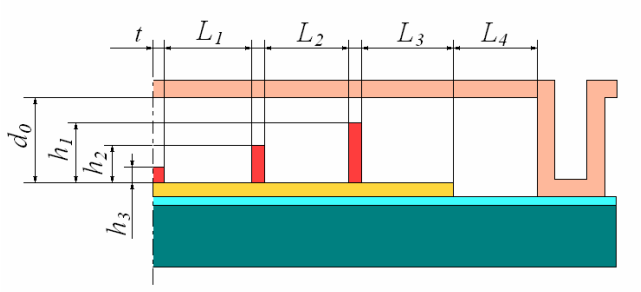
Design	L_1	L_2	L_3	L_4	t	h_1	h_2	h_3	LF	Tunability
Design I	100	100	100	100	5	0	0	0	0.863	65%
Design II	110	90	100	150	5	2.0	0.75	1.5	0.975	134%
Design III	100	100	100	100	5	2.0	0.75	1.5	0.992	130%

In the new design, different steps are placed between two electrodes to control the deformations of the moving one. Based on PolyMUMPs, steps with three different gaps of 0.75 μm, 1.25 μm and 2.0 μm can be fabricated (see Figure 5-30), where the fixed and moving electrodes are made of Poly0 and Poly2, respectively, resulting in an initial gap of $d_0 = 2.75$ μm.

An ANSYS® model is created using three different step heights, 2.0 μm, 1.5 μm and 0.75 μm, corresponding to the three possible gaps between two plates. Depending on the number of steps, their heights and locations, C-V responses with different shapes and tunabilities are obtained. Figures 5-31-a, 5-31-b and 5-31-c display the results of FEM simulations for a capacitor with symmetric rectangular design and five steps (three independent step heights, i.e., steps one and five and also two and four have the same heights). L_i and h_i are design variables and three sets of variables, presented in Table 5.2, are examined.

As explained before, Design I confirms that the flexibility of the moving plate alone does not improve LF. The new Design II and III capacitors exhibit notably improved linearity, and since the rigid steps allow larger displacements of the moving plate, the total tunability is also increased without intensifying the sensitivity of the capacitance to the voltage change.

To further improve the linearity, the same technique is applied to a circular-plate capacitor. The higher structural stiffness of a circular plate with fixed-edge boundary conditions prevents



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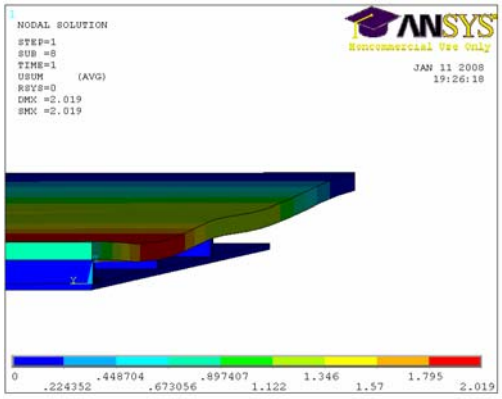

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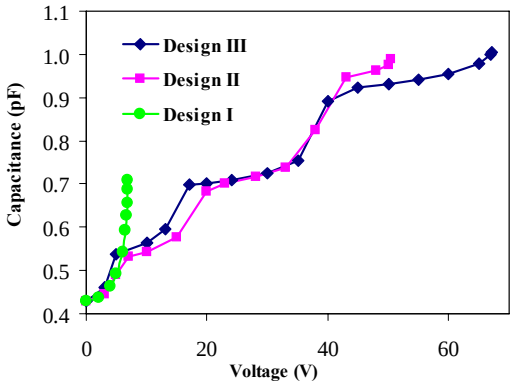


(c)

Figure 5-31: The results of ANSYS® simulations for a flexible-plate capacitor: (a) The simplified model; (b) Deformations of the plate after contact with steps; (c) The C-V response for three designs.

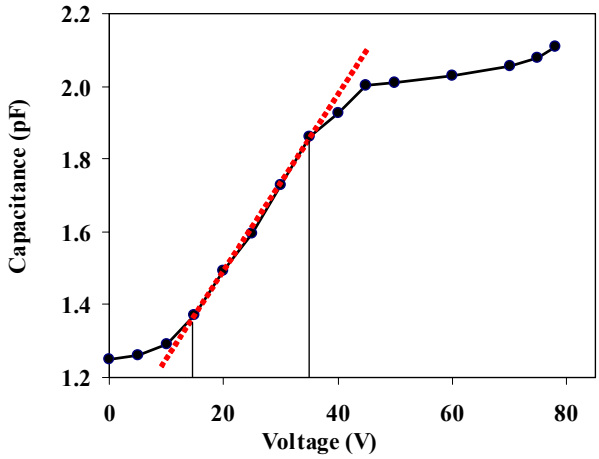


Figure 5-32: The C-V response (solid line) and its linear interpolation inlinear region (dotted line) for an optimized circular-plate capacitor.

rapid increment in the plate displacements and increases the linearity and also the actuation voltage. Similar steps are added to a circular-plate capacitor and the dimensions are optimized to improve the linearity of the response. The steps in this design are circular stripes with different radii. The C-V response of the resulting linear circular-plate capacitor is presented in Figure 5-32. As displayed in this figure, for a voltage range 15 V $< V <$ 35 V, the capacitor exhibits high linearity of $LF = 0.999$ with 36% tunability, where the maximum tunability reaches 69% at pull-in.

Design Modification

The rigid steps added to the capacitor's structure prevent the pull-in each time the moving electrode is about to collapse on the fixed one. This is observed in Figure 5-31-c, where the C-V curves of Design II and Design III are broken into four sub-regions. For a capacitor equipped with more steps, the C-V curve will be divided into more sub-regions leading to higher linearity and tunability. Each region is the result of a local pull-in for the part of plate with higher rate of displacement. To prevent the local jumps in the curve and obtain a smoother response, the geometry of the plates is modified to a (symmetric) zigzag shape as depicted in Figure 5-33.

The plate shown in Figure 5-33 is connected to the anchor at edge E, and as the bias voltage

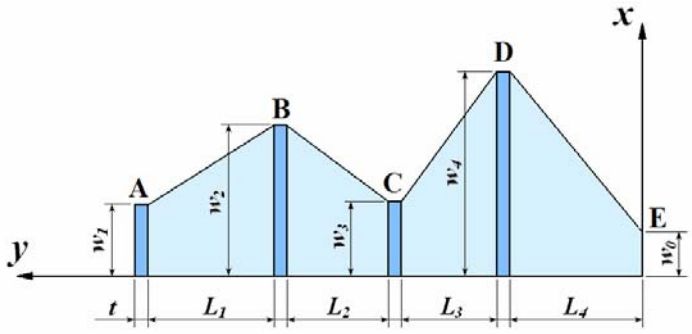


Figure 5-33: The top view of a zigzag-shape electrode and the design variables (the contact surfaces are shown by darker stripes).

increases, stripes A, B, D and C, respectively, touch the corresponding steps. Due to the zigzag shape of the plate, once actuation voltage is applied, the two electrodes lose their parallelness in lateral (x) direction. It means that first points B and D touch the steps and then, the rest of the stripes gradually contact the corresponding steps. This is the key idea to eliminate the jumps in the C-V curve and to improve the linearity of the response as illustrated in Figures 5-34-a and 5-34-b. For a capacitor with zigzag-shape electrodes, the resulting C-V response depends on the design variables, L_i, w_i and h_i, which can be optimized for maximum linearity or tunability. Figure 5-35 shows the C-V curve of a capacitor with a set of optimum design parameters. For this device, $LF = 0.997$ and the maximum tunability reaches 125% at $V = 33.5$ V displaying remarkable improvement over a conventional parallel-plate capacitor.

5.5.3 Fishbone-Shape Linear Capacitors

Zigzag-plate capacitors provide high tunabilities and highly linear C-V curves. To further benefit the flexibility of the electrode in lateral direction, a further modification is applied to design, by increasing the number of triangular areas and decreasing their width. The electrode in this case looks like a fishbone as portrayed in Figure 5-36 and the length and width of each step is the same as the corresponding beam. When a DC voltage is applied, the longitudinal beam deforms due to the electrostatic force and each lateral beam also deflects. Since the lateral beams have different lengths, they touch the corresponding steps at different voltages which

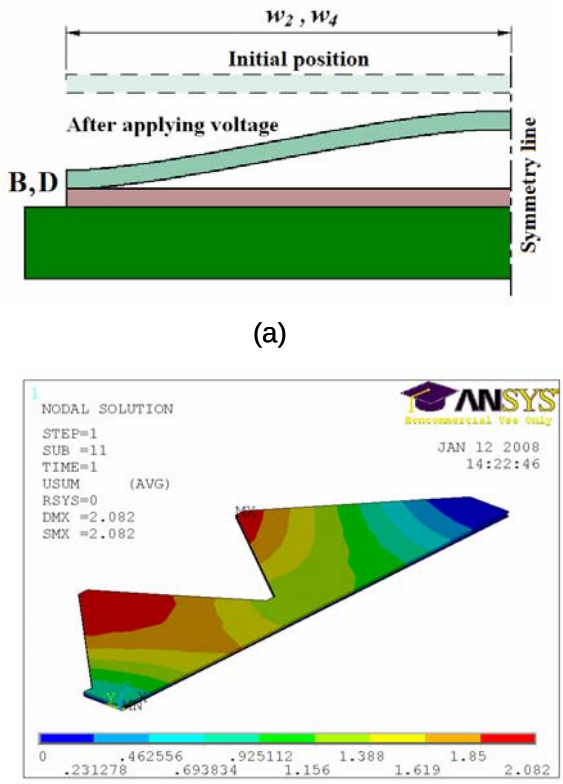


Figure 5-34: (a) Lateral deformations (in x direction) of a zigzag-shape electrode at B and D; (b) The result of ANSYS® simulations.

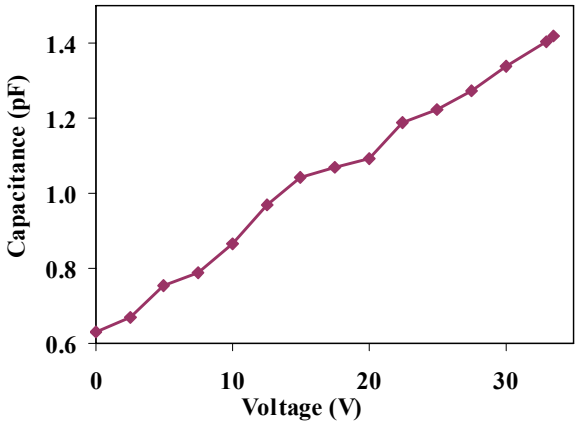


Figure 5-35: The C-V response for the optimized zigzag-shape flexible-plate capacitor obtained from ANSYS simulations.

improves the linearity. Due to variable flexibility of each beam, there is no need to use different step heights. Therefore, this design is suitable for fabrication processes with two conductive layers and an isolator (dielectric) layer on top of the fixed electrode, which is its main advantage over zigzag-shape capacitors.

To examine the behavior of a fishbone-shape tunable capacitor, a $\frac{1}{4}$ model of a symmetric design with three lateral beams is studied. Capacitors with different lateral beam lengths and locations are simulated with ANSYS® and the results of simulations are presented in Figures 5-37 and 5-38. As shown in Figure 5-38, the capacitors display high linearity in two separate regions. In contrary to conventional parallel-plate designs, due to structural stiffening of the longitudinal beam at larger deformations, the rate of capacitance increment decreases at higher voltages and the pull-in does not occur. The maximum tunability of the capacitor exceeds 200%, and for the linear region (voltage interval 2 V $< V <$ 9 V) up to 150% tunability and $0.992 < LF < 0.998$ are obtained. A closer look at the C-V responses (Figure 5-38) reveals that in different designs the beams touch the contact surfaces at different voltages. Therefore, if the number of beams is increased or the symmetry of the capacitor is altered, then a higher linearity may be achieved. In both cases, the ANSYS® model should include more contact pairs which drastically increases the number of structural iterations and the computation time. To study the effect of asymmetric design, an approximation is applied to the model. If the C-V curves of

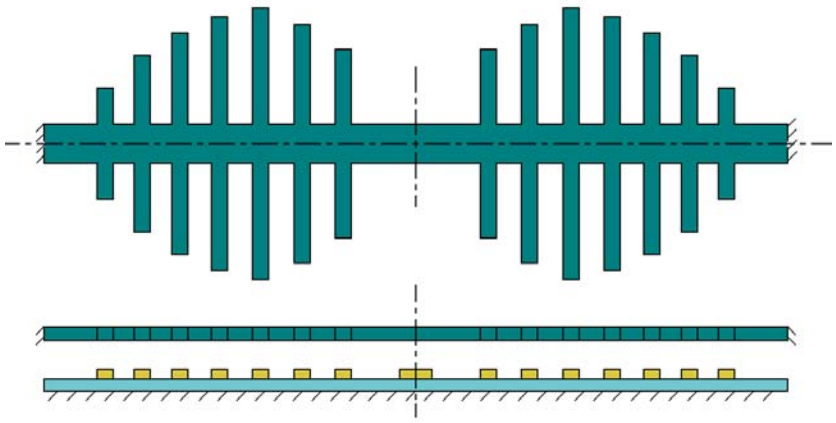


Figure 5-36: A fishbone-shape capacitor with symmetric electrodes. The moving electrode is connected to anchor at its two ends, and under each lateral beam there is a step to prevent contact between two electrodes.

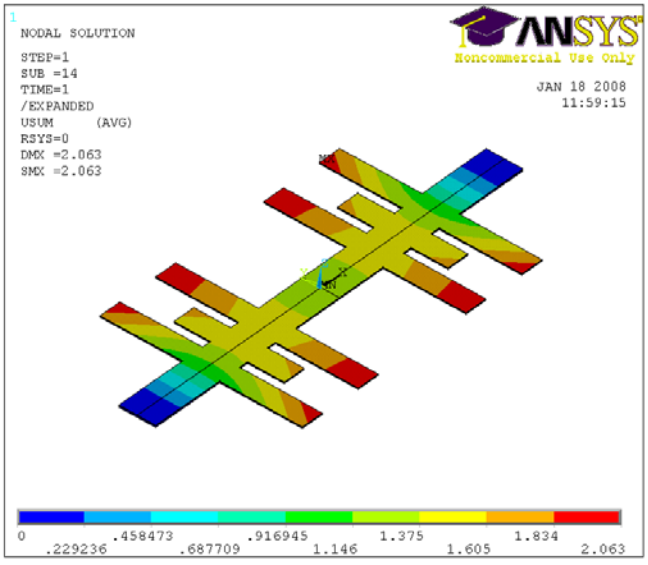


Figure 5-37: Beams deformations at $V = 7.0$ V for a symmetric fishbone-shape design.

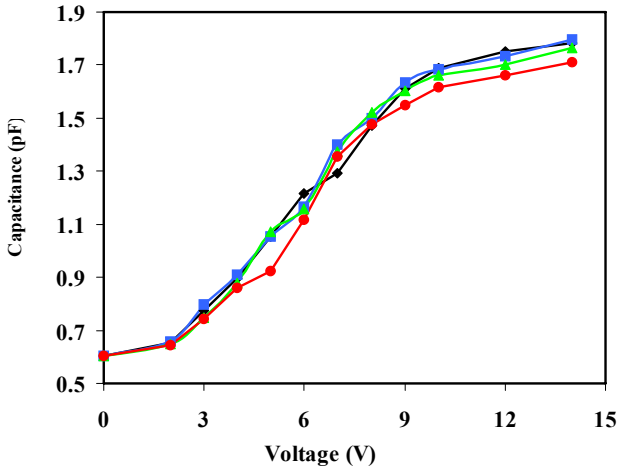


Figure 5-38: The C-V curves for fishbone-shape capacitors with three lateral beams of different dimensions, obtained from ANSYS simulations.

four $\frac{1}{4}$ models, presented in Figure 5-38, are added, the resulting C-V response in linear region becomes very smooth as shown in Figure 5-39. Since the actual design is asymmetric and the capacitance values used in this C-V curve are obtained from models with symmetric boundary conditions, the results may incorporate some error. However, the error can be minimized if the electrode areas of all $\frac{1}{4}$ section are the same which reduces the difference between components of electrostatic force in each section. The C-V curve displayed in Figure 5-39 has a linearity factor $LF = 0.998$ with 145% tunability and if the curve is replaced by its linear interpolation, $C = 0.1407V + 0.3436$, the average error is less than 2%.

5.6 Summary

The lumped and continuous structural flexibilities of the moving plates in parallel-plate-based tunable capacitors were studied. The capacitor performance is improved by adding steps to the device structure. The segmented-plate capacitors with fixed and flexible steps and geometric modifications exhibit high linearity up to $LF = 0.998$ and total tunability over 100%. Similar design technique in capacitors with flexible plates lead to higher linear tunability up to 150% with $LF = 0.998$. The geometric optimization and controllable structural flexibility (such as

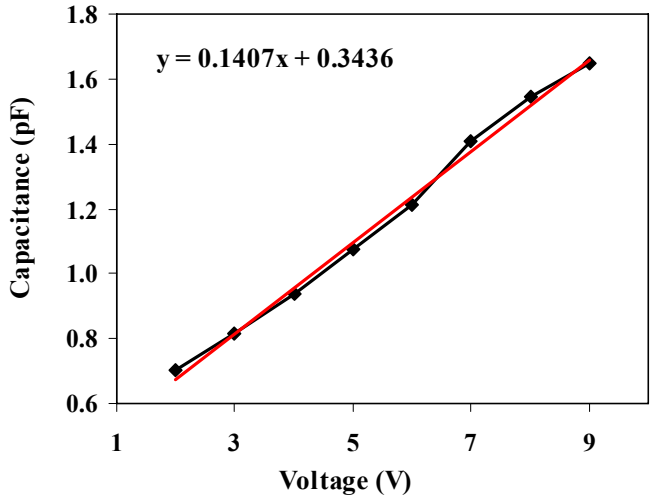


Figure 5-39: The approximate C-V response of an asymmetric fishbone-shape capacitor with high tunability and linearity.

zigzag-plate or fishbone capacitors) are key ideas to enhance the performance of the device and to eliminate the pull-in. All capacitors presented in this chapter (except optimized three-segmented and six segmented-plate designs) can be fabricated by a two- or three-conductive-layer process such as PolyMUMPs which demonstrates the potential of this methodology to the development of highly linear and tunable capacitors.

Chapter 6

Development of a MEMS Probabilistic Design Methodology Immune to Process Uncertainties

6.1 Introduction

MEMS fabrication processes display physical, chemical and operational uncertainties which affect the properties of the fabricated devices. Regardless of the sources of uncertainties, the results usually appear as deviations of the actual parameters from the nominal values within their tolerance ranges. Consequently, various uncertainties are taken into account by adding appropriate tolerances to the nominal values. In MEMS processes, dimensional tolerance are relatively large and may lead to a wide output (performance) range in fabricated devices, where many of the final products may fail to meet desired specifications. Tightening the tolerances usually is not an option, as it creates technical or cost challenges. Therefore, it is very important to develop a design methodology that take into account the process tolerances and make the fabricated devices immune to process uncertainties. This will immune the design to any fabrication inaccuracies and consequently improve production yield of MEMS devices. For development of this methodology, the production yield is considered as an index in this thesis and higher yield corresponds to higher process immune design. In general, the analysis of

fabrication uncertainties and their effects on the device performance is a vital task before finalizing the design. If the performance is severely affected by fabrication inaccuracies, it is essential to optimize the design to minimize these effects to maximize the yield.

In this chapter, the fabrication uncertainties are briefly reviewed and their effects on performance of MEMS parallel-plate tunable capacitors are addressed. Then, a probabilistic design optimization method is introduced that improves the yield for a given fabrication process and is "immunized" to the large tolerance ranges. for improving the yield. The optimization can be conducted in two steps: finding the nominal design variables which maximizes the yield (design optimization), or finding a tolerance range which provides 100% yield (process optimization).

6.2 MEMS Fabrication Uncertainties

One of the main obstacles in commercialization of MEMS devices is the fabrication uncertainties which are quite noticeable in different processes such as deposition and etching. These uncertainties may produce tolerances higher than $\pm 10\%$ of the nominal values. Therefore, thicknesses, feature sizes and mechanical properties (Young modulus and residual stress) of MEMS structures may face large deviations from one device to another and generate a notable discrepancy in the device performance. Moreover, tightening the tolerances to obtain more accurate dimensions is not always possible, since it imposes higher costs to micro-fabrication processes. As a result, the analysis of fabrication uncertainties and their effects on the device output are very important and should be performed at the design stage.

Inaccuracy exists in all steps of a MEMS fabrication process such as mask alignment, deposition, photolithography, etching, drying and even packaging. To study fabrication uncertainties, PolyMUMPs is considered as a pilot process. The deposition tolerances in this process are listed in Table 6.1 [16].

As presented in this table, the thickness tolerances are quite large and will greatly affect the device performance. In addition to layer thicknesses, the mask alignment, photolithography and etching also produce dimensional variations in feature sizes, where comparing to the thickness variation, the feature size "normalized" tolerances are usually negligible if the dimensions are larger than 10 μm. For example, in PolyMUMPs the feature size deviation, created by mask

Table 6.1: Deviations of thickness of different layers (tolerance) in PolyMUMPs

Layer	Thickness (μm)			Normalized
	minimum	nominal	maximum	tolerance
Nitride	0.53	0.6	0.67	$\pm$12%
Poly0	0.47	0.5	0.53	$\pm$6%
Oxide1	1.75	2.0	2.25	$\pm$13%
Poly1	1.85	2.0	2.15	$\pm$8%
Oxide2	0.67	0.75	0.83	$\pm$11%
Poly2	1.4	1.5	1.6	$\pm$7%
Metal	0.46	0.52	0.58	$\pm$12%

alignment, photolithography and etching is found to be less than ± 0.5 μm. Figure 6-1 shows the result of misalignment in a two-segmented-plate capacitor fabricated with PolyMUMPs. The designed gap between central beam and two segments, g, is 3 μm, where the actual gaps after fabrication are $g_1 = 2.45$ μm and $g_2 = 3.75$ μm or 18.3% and 25% error, respectively. As one may notice $g_1 + g_2 > 2g$, because the beam and plates are overetched which increases the distance between them.

The dimensional deviations are not constant for a process and changes from one device to another. Therefore, design parameters varying within tolerance ranges can be considered as random variables. The device performance then becomes a random variable and if the tolerances are not within certain ranges, the final output may fail to meet the defined criteria. This raises the question that how to modify the process or design to increase the yield. Tighter tolerances lead to higher yields, but they involve extra cost or technical challenges. This question will be answered later in this chapter by introducing a yield optimization method which directly maximizes the yield.

6.3 The Effects of Fabrication Uncertainties on Parallel-Plate Capacitors

The capacitance-voltage response for a parallel-plate tunable capacitor is a nonlinear function of electrode and beams dimensions and the applied voltage. It also depends on Young's modulus which changes the structural rigidity. Moreover, residual stress may change the response by pre-bending the moving plate and beams and changing the initial air gap as demonstrated in

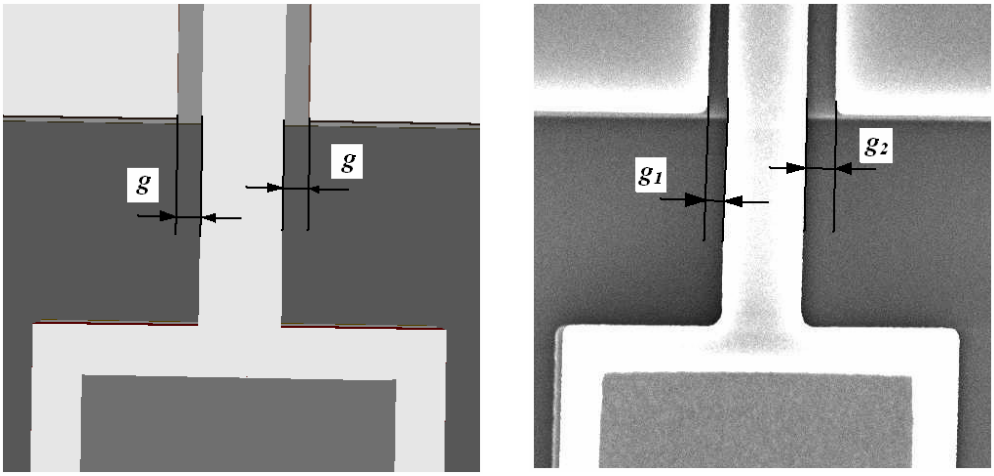


Figure 6-1: The fabrication error due to misalignment of masks; (a) 3D model produced by CoventorWare, b) the SEM image of the fabricated device. $g = 3$ μm, $g_1 = 2.45$ μm, $g_2 = 3.75$ μm.

the previous chapters. In mass production of a tunable capacitor, the value of each parameter randomly deviates from the designed value within its tolerance range. Because the C-V curve has a nonlinear relation with design parameters, small deviations in dimensions of the structure causes large difference between designed and actual responses. If the beams dimensions are not equal at two sides of the capacitor due to fabrication uncertainties, the electrodes lose their parallelness. Recall the governing equations of a non-parallel-plate capacitor,

$$C = \frac{\epsilon_0 A}{(d_2 - d_1)} \ln(\frac{d_2}{d_1}) \tag{6.1}$$

$$\frac{\epsilon_0 V^2 A}{2 d_1 d_2} - k_1(d_0 - d_1) - k_2(d_0 - d_2) = 0 \tag{6.2}$$

$$\frac{\epsilon_0 V^2 A}{2}[\frac{l}{(d_2 - d_1)^2} \ln(\frac{d_2}{d_1}) - \frac{l}{d_2(d_2 - d_1)}] - k_2(d_0 - d_2)l = 0 \tag{6.3}$$

one can see that as the plates and beams dimensions change, the capacitance at each actuation voltage changes accordingly. Therefore, random deviations of the dimensions cause a random C-

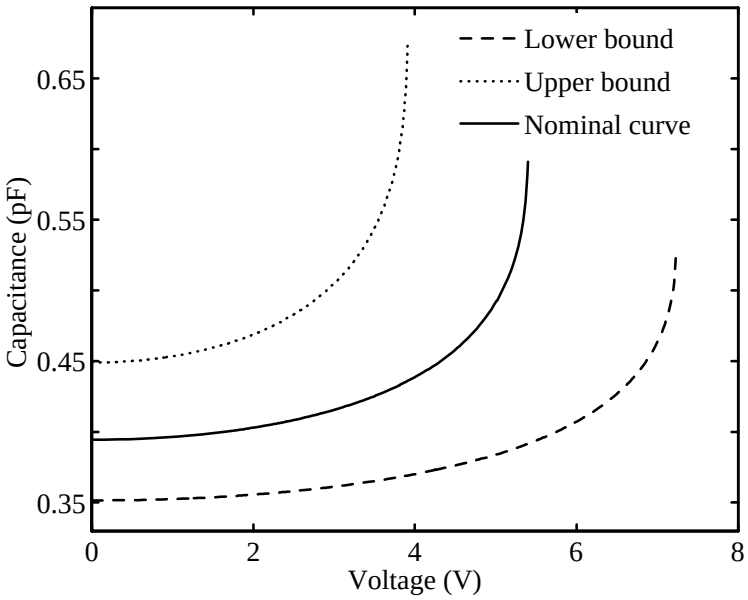


Figure 6-2: The nominal C-V curve and its upper and lower limits obtained from maximum/minimum dimensional deviations of PolyMUMPs.

V response for each device, where the dimensional uncertainties change both initial capacitance, C_0, and pull-in voltage, $V_{pull-in}$. To illustrate this fact, a parallel-plate tunable capacitor designed for PolyMUMPs is considered. The fixed and moving plates are made by Poly0 and Poly2 layers, respectively, and the initial air gap is $d_0 = 2.75$ μm. The plates' dimensions are, $A = 350 \times 350$ μm^2 and the thickness, width and length of beams are $t = 1.5$ μm, $w = 8$ μm and $L = 150$ μm, respectively. Figure 6-2 shows the capacitor's nominal C-V response and its upper and lower bounds, where all parameters take their maximum or minimum values from Table 6.1.

As shown in this figure, the deviations are very large. For example, the nominal pull-in voltage is 5.3 V, while its upper and lower bounds are 3.94 V and 7.19 V, respectively, exhibiting -26% to 35% error. Maximum initial capacitance, C_0, is 30% higher than the minimum value which means one should expect at least 30% variations in product's output. Chen *et al.* [11] reported a similar discrepancy for C-V response of a two-gap capacitor. The measured tunability varies from 44.7% to 69.8% displaying 36% variation in the maximum

tunability, where the C-V responses were measured for five identical capacitors fabricated on the same chip. These examples explain why the analysis of fabrication uncertainties at the design stage is very important. In the analysis, two main issues should be addressed: For a multi-parameter device like a tunable capacitor, which design variables create the highest deviations in the device output, and how the design parameters can be optimized to obtain the highest possible yield.

6.4 Sensitivity Analysis for Parallel-Plate Capacitors

The analysis of uncertainty may involve different level of complexity. It is possible to include all design parameters such as plates' and beams' dimensions, air gap and even elastic modulus and residual stresses, but this will complicate the analysis and interpretation of the results. To simplify the problem and reduce the number of variables without sacrificing the accuracy, a sensitivity analysis is performed. Using the relative sensitivity, the parameters with major impact on the C-V response are found.

The relative sensitivity of a performance characteristic function y to the change of an element x is defined as [70]:

$$S_x^y = \frac{\partial y}{\partial x}\frac{x}{y} \tag{6.4}$$

For a tunable capacitor the performance function y in (6.4) is the capacitance, C, where the element x can be stiffness coefficient, initial capacitance or any dimension. For a multi-parameter function, Y, the change in Y due to small deviations in all variables is obtained from:

$$dY = \sum_{i=1}^{n} \frac{\partial Y}{\partial x_i} dx_i \tag{6.5}$$

Using (6.4), the multi-parameter sensitivity measure is then defined as:

$$\frac{dY}{Y} = \sum_{i=1}^{n} S_{x_i}^{Y} \frac{dx_i}{x_i} \approx \sum_{i=1}^{n} S_{x_i}^{Y} \delta_i \tag{6.6}$$

Here, δ_i is the relative tolerance, $\delta_i = \Delta x_i / x_i$, and x_i and Δx_i are the nominal design values and corresponding tolerances, respectively. Equation (6.6) explains that the deviation of a multi-parameter function from its nominal value depends on the fabrication tolerance of each

design variable and the relative sensitivity of the performance function to the change of that variable.

For simplicity of the analysis, the parameters are divided into two groups: the parameters which affect the stiffness coefficient of beams, k, and those which change the initial capacitance, C_0. This separation has a physical meaning because initial capacitance defines the starting point of the C-V curve and k determines the pull-in voltage. Using (6.6) this can be expressed as:

$$\left|\frac{\Delta C}{C}\right| \approx \left|S_{C_0}^{C}\frac{\Delta C_0}{C_0}\right| + \left|S_{k_{eq}}^{C}\frac{\Delta k_{eq}}{k_{eq}}\right| \tag{6.7}$$

where $S_{C_0}^{C}$ and $S_{k_{eq}}^{C}$ depend on the capacitor's governing equations and do not change by fabrication tolerances. The initial capacitance is a function of initial air gap and plates' dimensions and k is a function of Young modulus and beams' dimensions:

$$k_{eq} = 4 \times \frac{12EI}{L_S^3} = 4\frac{Ewt^3}{L_S^3} \tag{6.8}$$

where w, t, L_S and E are width, thickness, length and elastic modulus of the beams, respectively, and k_{eq} is the equivalent stiffness coefficient of four supporting beams. The change of initial capacitance in terms of normalized tolerances of initial gap, d_0, and surface area, A, is written as:

$$\left|\frac{\Delta C_0}{C_0}\right| \approx \left|S_{d_0}^{C_0}\delta_{d_0}\right| + \left|S_{A}^{C_0}\delta_{A}\right| \tag{6.9}$$

where δ_{d_0} and δ_A are normalized tolerances of the initial gap and surface area, respectively.

The plates' feature tolerances (length and width of plates) depend on photolithography and etching and for PolyMUMPs it is estimated to be less than ± 0.50 μm. Using Table 6.1, for initial capacitance: $d_0 = 2.75$ μm, $A = 350 \times 350$ μm^2, and the normalized tolerances are $\delta_{d_0} = 0.12$ and $\delta_A = 0.003$ and relative sensitivities, $S_{d_0}^{C_0}$ and $S_{A}^{C_0}$, are -1 and 1, respectively:

$$S_{d_0}^{C_0} = \frac{\partial C_0}{\partial d_0}\frac{d_0}{C_0} = -\frac{\epsilon_0 A}{d_0^2}\frac{d_0}{\frac{\epsilon_0 A}{d_0}} = -1 \tag{6.10}$$

$$S_{A}^{C_0} = \frac{\partial C_0}{\partial A}\frac{A}{C_0} = \frac{\epsilon_0}{d_0}\frac{A}{\frac{\epsilon_0 A}{d_0}} = 1 \tag{6.11}$$

From (6.9), the total relative deviation of initial capacitance is obtained as $\left|\frac{\Delta C_0}{C_0}\right| = 12.3\%$,

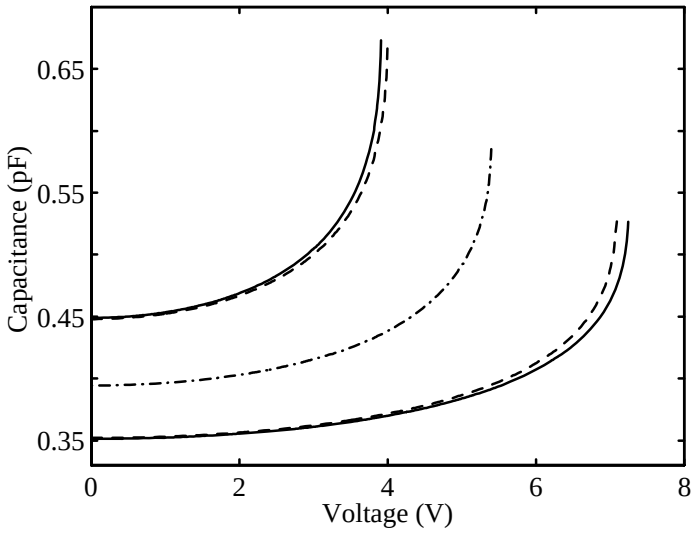


Figure 6-3: C-V curves for different sets of uncertain variables; Solid line: All tolerances; Dashed line: Two main tolerances obtained by sensitivity analysis; Dash-dotted line: Nominal design values.

12% of which is generated by the thickness of sacrificial layers, d_0. Similarly, the deviation of stiffness coefficient in terms of fabrication uncertainties is obtained from:

$$\left|\frac{\Delta k_{eq}}{k_{eq}}\right| \approx \left|S_t^{k_{eq}}\delta_t\right| + \left|S_w^{k_{eq}}\delta_w\right| + \left|S_{L_S}^{k_{eq}}\delta_{L_S}\right| \tag{6.12}$$

For supporting beams: $t = 1.5$ μm, $w = 8$ μm and $L_S = 150$ μm, the normalized tolerances δ_t, δ_w and δ_{L_S} are 0.07, 0.038 and 0.003, and the relative sensitivities are obtained from equations similar to (6.10) and (6.11) as 3, 1 and -3, respectively. The approximated relative deviation obtained from (6.12) is $\left|\frac{\Delta k_{eq}}{k_{eq}}\right| = 25.36\%$, 21% of which is generated by Poly2 thickness variations. This means that the variables with the most impact on C-V deviations are expected to be the thicknesses of Poly2 and sacrificial layers (Oxide1 plus Oxide2). Figure 6-3 presents C-V curves with different level of uncertainty. As shown in the figure, the error of considering the tolerances of d_0 and t and neglecting the other tolerances is quite negligible which verifies the result of sensitivity analysis. It should be mentioned that if the design parameters change, the normalized tolerance will change which affect the results of sensitivity analysis. For exam-

ple, if the width of beam decreases to $w = 3$ μm, then the corresponding normalize tolerance δ_w increases to 0.167 and has higher impact on deviation of capacitance from its nominal value.

6.5 Yield Optimization

The quality of a manufacturing process is interpreted by different parameters such as production yield. A Higher yield indicates more acceptable products and less losses. Increasing the yield can decrease the production costs, rendering a product more competitive in the market. Therefore, yield optimization is a decisive step in the development of a new device. In this section, a method for yield optimization is introduced which involves three steps: approximation of the constraint region (defined by the performance functions and bounds on the design parameters), approximation of joint cumulative distribution functions of the random design variables to calculate the yield and the yield maximization that combines the above two steps [71, 72].

6.5.1 Polyhedral Approximation of the Constraint Region

Let $\Re^n$ be the space of design variables x. The feasible region, F, containing the acceptable output is defined over $\Re^n$ as:

$$F = \{x \in \Re^n \mid \ h_i(x) \geqslant 0, \quad i = 1, 2, ..., m\} \tag{6.13}$$

Here, the real-valued functions $h_i(x) : \Re^n \longrightarrow \Re$ are measures of the system performance and act as the mathematical constraints for F and index i represents the i^{th} constraint. The vector x represents a sample of the random variable X with arbitrary joint probability distribution function in the space of design variables. Because the analytic form of $h_i(x)$ may not be available (for example, the capacitance is an implicit function of design variables), the method constructs a polyhedral approximation of the feasible region by taking first-order approximation of each $h_i(x)$ at the expansion point x^*:

$$h_i(x) \approx h_i(x^*) + g_i(x^*)^T(x - x^*) \tag{6.14}$$

where $g_i(x^*)$ is the gradient vector of h (if the explicit gradient function cannot be derived then, the gradient vector, $g_i(x^*)$, should be calculated numerically). The point x^* is on the surface $h_i(x) = 0$ and has the minimal distance from the center of the initial tolerance box, x^c. The shortest distance to the constraint is found by solving the minimization problem:

$$\begin{aligned} \min\ \beta &= [(x - x^c)^T (x - x^c)]^{\frac{1}{2}} \\ \text{subject to} &: h_i(x) = 0 \end{aligned} \tag{6.15}$$

An iterative formula, developed by Madsen *et al.* [73], is employed to solve this optimization problem, where the Lagrangian of β in (6.15) with a fixed-point method, is given by:

$$x^{k+1} = x^c - \frac{g_i^k[(g_i^k)^T(x^c - x^k) + h_i^k]}{(g_i^k)^T g_i^k} \tag{6.16}$$

The superscripts k and $k+1$ refer to the index of iteration. This formula attempts to solve $h_i(x) = 0$ indirectly. Convergence of (6.16) depends on continuity and convexity of $h_i(x)$ and the solution may not be unique. For each constraint, the method finds a linear approximation in the form of (6.14). Such approximations, together with upper and lower bounds on the design variables form a polyhedral feasible region. The polytope P, an approximation for F, is defined by:

$$P = \{x \mid Ax \geqslant C, \quad x_j^{\min} \leqslant x_j \leqslant x_j^{\max}\} \tag{6.17}$$

The i^{th} row of A is g_i^T, where all the partial derivatives are evaluated at x^*, found by (6.16), and $C_i = (g_i^*)^T x_i^*$. The lower and upper bounds of x_j are denoted by $x_j^{\min}$ and $x_j^{\max}$, respectively, where index j represents the j^{th} design variable.

6.5.2 Modeling Arbitrary Distributions

If the random variables are independent and have uniform distributions, then the yield optimization problem reduces to the worst-case design and is solved by searching for the maximum volume box contained in the feasible region. On the other hand, there are cases in which the probability density function (PDF) is not symmetric. For example, the distribution of width deviation from nominal values for 75 stripes (supporting beams and transmission lines) with 3,

5, 10 and 20 μm width is shown in Figure 6-4. The stripes were fabricated by PolyMUMPs on a 5×5 mm^2 chip and etched for five minutes. As explained before, the feature tolerance for PolyMUMPs is less than ± 0.50 μm. If the effect of etching is added, then the actual dimensions will be smaller after etching and whole distribution will be shifted to the left-hand-side of nominal value and the results are considered as non-symmetrical distributions.

If a PDF is non-symmetrical, the maximum volume box does not necessarily correspond to maximum yield and thus the yield should be maximized directly by the following step. For each component the Kumaraswamy's distribution [74], a double-bounded probability density function (DB-PDF) appropriate for physically bounded variables, with the following form is defined :

$$f(z) = abz^{a-1}(1-z^a)^{b-1} \tag{6.18}$$

where z is a normalized variable defined as:

$$z = \frac{x - x^{\min}}{x^{\max} - x^{\min}} \quad , \quad x^{\min} \leq x \leq x^{\max} \tag{6.19}$$

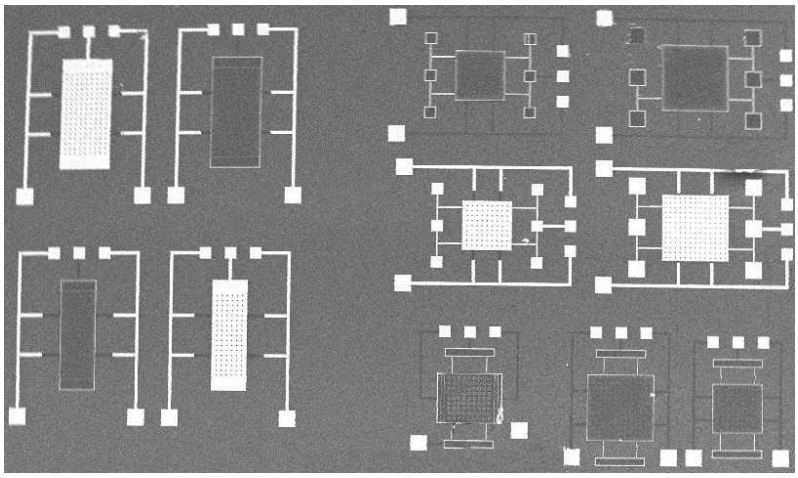
Depending on the choice of parameters a and b, DB-PDF takes various shapes. It can be used to approximate uniform, triangular, tail and many other single modal distributions. Another advantage of DB-PDF is that its integral, needed for yield evaluation, is available in closed form:

$$F(z) = 1 - (1-z^a)^b \tag{6.20}$$

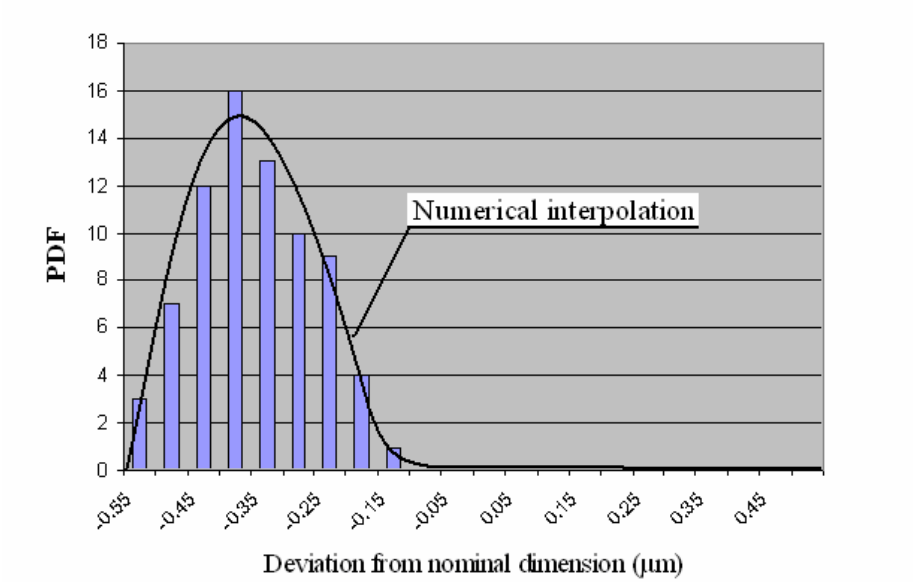
The DB-PDFs for some of the commonly used distribution functions (produced by different values of a and b) are presented in Figure 6-5.

6.5.3 Yield Maximization

Given a convex and bounded polytope P defined by (6.17), the yield maximization is performed in the space of design variables. This means that no extra evaluations of performance functions are needed once P is constructed. Because the original constrained region, F, could be non-convex, several iterations may be required, each with a different starting point and different polyhedral approximation.



(a)



(b)

Figure 6-4: The distribution of width deviation for stripes with different width and a numerical interpolation; (a) SEM image of the chip; (b) Probability distribution function (PDF).

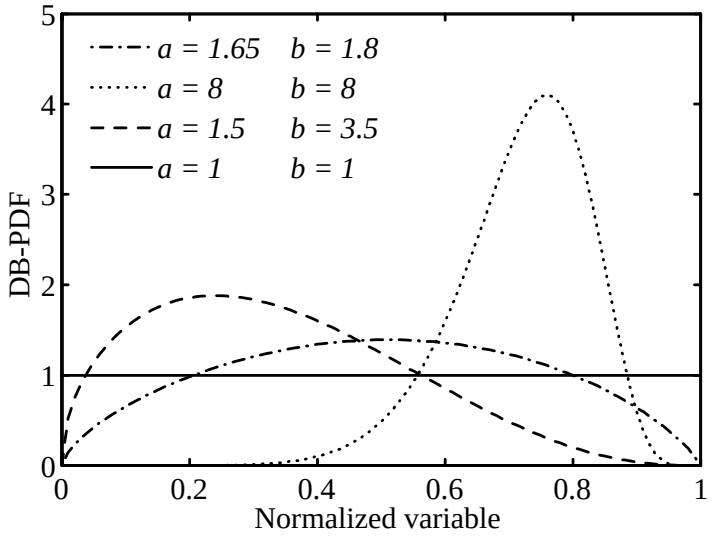


Figure 6-5: Double-bounded probability density functions for different values of a and b.

As previously mentioned, uniform distributions lead to the worst-case design which can be handled by searching for the maximum volume of the rectangular n-dimensional cube (box) contained in the feasible region. For a non-symmetrical PDF, this maximum volume does not correspond to maximum yield and the yield function must be maximized directly. The problem then reduces to the search for a box, contained in the polytope P, over which the yield is maximized and is defined by:

$$R(x^l, x^u) = \{x \in \Re n \mid x^l \leqslant x \leqslant x^u\} \tag{6.21}$$

$R(x^l, x^u)$ is the box, and x^l and x^u are lower and upper bounds of the box, respectively. The containment requirement, $R \subseteq P$, is equivalent to:

$$A^+ x^u - A^- x^l \leqslant C \tag{6.22}$$

Recall that A_i is the transpose of the gradient vector, g_i, obtained from the linearization of the performance constraint, h_i, and a given x. A^+ and A^- are the upper and lower bounds of

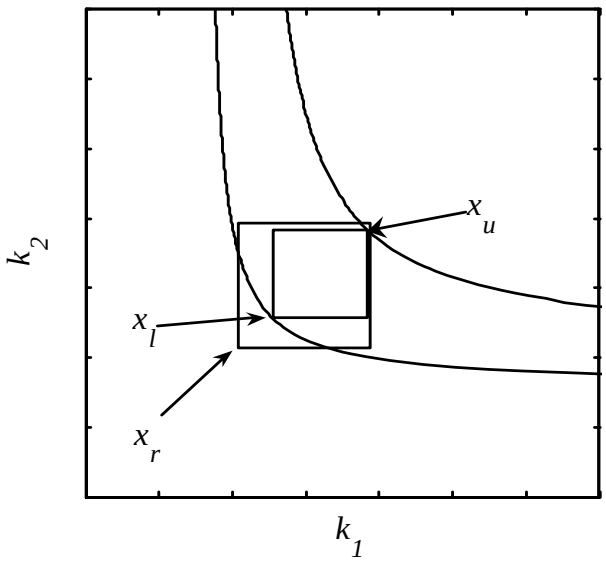


Figure 6-6: The optimzation parameters in the space of design variables; the large rectangle represents the tolerance box, and small rectangle represents the optimzed box correcponding to Yield = 1.0.

the performance constraint, and C refers to the constant term in the linearization. A reference point, x^r, $x^r \geqslant x^{\min}$, defines the location of the larger tolerance box shown in Figure 6-6. The left bottom corner is x^r, the top right corner is $x^{r+\Delta}$ and the range Δ is given for the j^{th} width by $\Delta_j = x_j^{\max} - x_j^{\min}$. The variables x^l and x^u define the bottom left corner and the top right corner of the smaller box, respectively, and specify the location and size of the optimal box that corresponds to the maximum yield. The optimization variables are x^r, x^l, and x^u, and the yield function is given by:

$$\begin{aligned} \text{Yield}(x^r, x^l, x^u) &= \prod_{j=1}^{n} \Pr\{x_j^l \leqslant x_j \leqslant x_j^u\} \\ &= \prod_{j=1}^{n} \left[F\left(\frac{x_j^u - x_j^r}{\Delta_j}\right) - F\left(\frac{x_j^l - x_j^r}{\Delta_j}\right) \right] \end{aligned} \tag{6.23}$$

The yield model (6.23), estimates the yield for the given values of x^r, x^l, and x^u. The estimated yield may have errors, depending on the shape of the feasible region, but the design is usually quite good, as discussed later in numerical examples. The objective of the yield

optimization problem is to move the tolerance box such that the yield is maximized:

$$\begin{aligned} \max\ & \text{Yield}(x^r, x^l, x^u) \\ & \text{subject to} \quad : \\ A^+x^u - A^-x^l &\leqslant C \\ x^r &\geqslant x^{\min} \\ x^l &\geqslant x^r \\ x^u - x^l &\leqslant \Delta \\ x^r + \Delta &\leqslant x^{\max} \end{aligned} \tag{6.24}$$

The problem can be extended in many ways. For example, the ratios of the tolerances of some of the components can be fixed, or (6.24) can be used in an inner optimization, while the outer optimization can include cost functions considering the tolerance, Δ, as the optimization variable.

6.5.4 Numerical Simulations and Results

To illustrate the capability of the proposed method, a parallel-plate tunable capacitor with two different sets of design variables is studied. For the first case, it is assumed that the initial gap is accurate enough and the fabrication uncertainties only deviate the stiffness of the beams. If the tolerances of deposition, mask alignment, photolithography and etching are taken into account, then the beams may have different dimensions, i.e., the summation of the stiffness coefficient of beams at two sides of the device are different leading to a non-parallel-plate configuration. The capacitance is then obtained from (6.1). Figure 6-7 displays the C-V curves of a capacitor with dimensions: $A = 350 \times 350\ \mu\text{m}^2$ and $d_0 = 2.75\ \mu$m (solid line). The nominal stiffness coefficients at two sides, k_1 and k_2, are the same, $k_1 = k_2 = 1.6$ N/m (corresponding to $L_S = 150\ \mu$m, $w = 10\ \mu$m and $t = 1.5\ \mu$m).

The upper and lower limits of the capacitance at voltage $V = 3.5$ V, C_{up} and C_{low}, respectively, are considered as design criteria for performance functions, $C_{up} = 0.49$ pF and $C_{low} = 0.44$ pF. An upper bound for design variables k_1 and k_2 ,$k_{max} = 3.0$ N/m, is considered

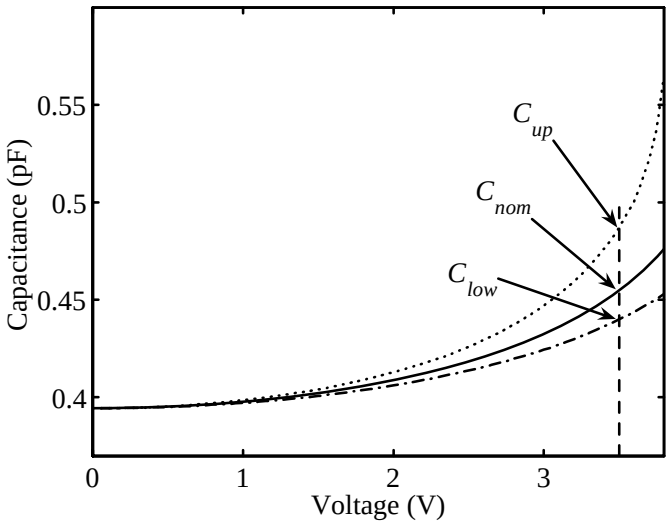


Figure 6-7: The C-V response for a capacitor with different stiffness coefficients. Dotted line, dash-dotted line and solid line represent upper bound, lower bound and nominal curve, respectively.

to enclose the feasible region. The tolerance box for stiffness coefficients is: $\Delta = [1.1, 1.1]$ N/m, corresponding to $\pm 35\%$ deviation from nominal values. The performance functions of the problem are:

$$\begin{aligned} \frac{\epsilon_0 A}{d_2 - d_1} \ln(\frac{d_2}{d_1}) &\leqslant C_{up} \\ \frac{\epsilon_0 A}{d_2 - d_1} \ln(\frac{d_2}{d_1}) &\geqslant C_{low} \\ k_1 &\leqslant k_{\max} \\ k_2 &\leqslant k_{\max} \end{aligned} \tag{6.25}$$

where d_1 and d_2 are the distance between two electrodes corresponding to k_1 and k_2, respectively, and the first two expressions in (6.25) are implicit functions of k_1 and k_2. The feasible area in the space of design variables and its linear approximation are shown in Figure 6-8. The dotted curves are the performance functions, $h_i(x) = 0$. The dashed-dotted lines represent linear approximation and depend on the center point x^c in (6.15). Dashed lines represent extra lower bounds to reduce the error of linearization. The dark grey area, enclosed by solid lines,

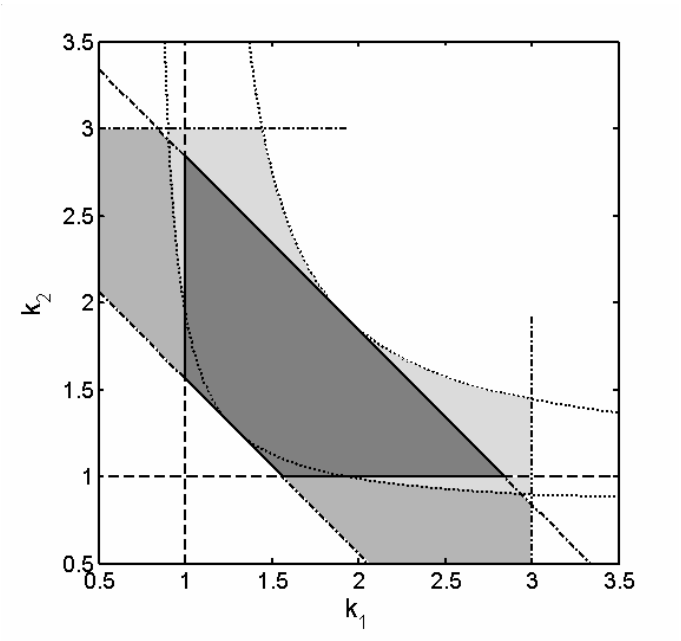


Figure 6-8: The feasible area corresponding to the performance functions, $h_i \geqslant 0$ (light grey area) and its linear approximation (dark grey area).

represents the approximated feasible region.

The results of yield optimization for different tolerance boxes and double-bounded probability density functions, DB-PDFs, are presented in Table 6.2 and Figure 6-9. The method also finds the tolerance box which corresponds to the yield equal to 1.0 (small rectangle in Figure 6-9-a and 6-9-b). That means if the process can be modified in such a way that it provides the optimum tolerances, then the final products will be 100% within the designed range. As shown in Table 6.2, the result of optimizations displays significant increase in yield for nonsymmetrical distributions from 31% to over 90%. The improvement for symmetrical (normal) distribution is also satisfactory. One can also see that the error between approximated yield and the reference Monte-Carlo (M-C) simulations is negligible.

As the second example, the tolerances of all dimensions are taken into account and the results of sensitivity analysis are used to find the most effective design variables. Using these results, the initial air gap, d_0, and beams' thickness, t, the main sources of inaccuracy in capacitance, are the new design variables in the yield optimization problem. Consequently, the

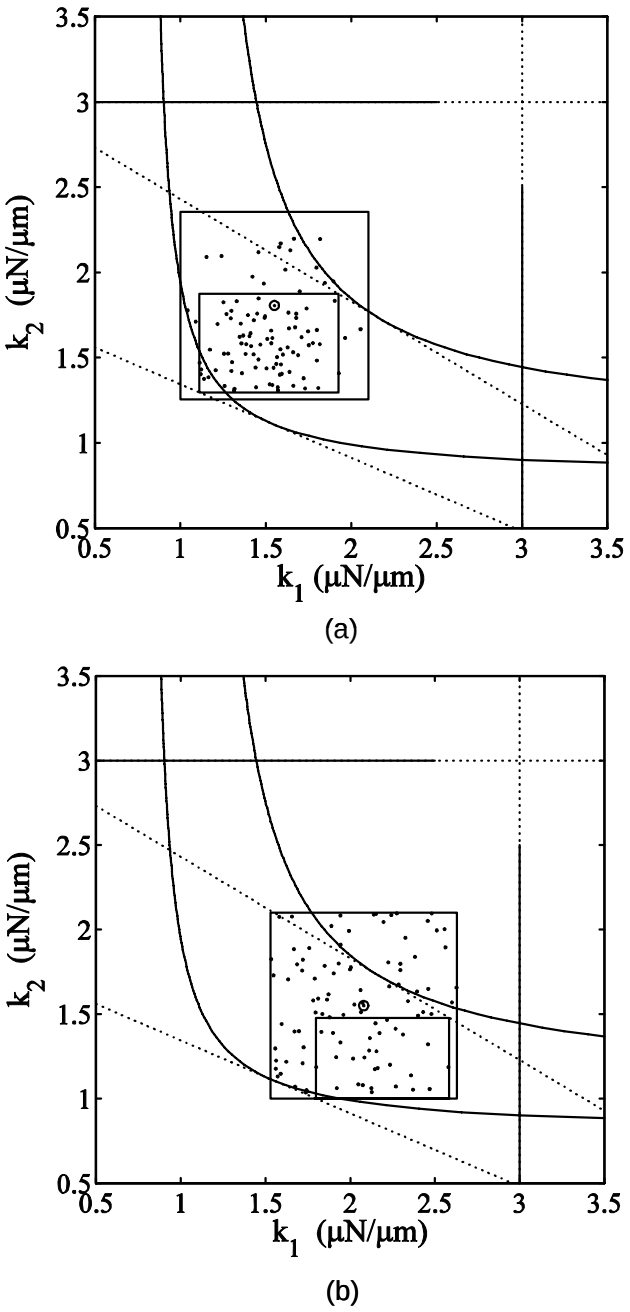


Figure 6-9: The result of yield optimization: (a) Skewed joint distribution functions ($a = [2, 1.5]$, $b = [2.5, 3.5]$); (b) Normal joint distribution functions ($a = [1, 1]$, $b = [1, 1]$); large and small rectangles represent existing and optimized tolerance boxes.

Table 6.2: Yield optimization for different DB-PDF and tolerance boxes

Parameters		Tol. Box	Yield			Remarks
a	b	(δ)	Initial M-C	Final M-C	Estimated	(distribution)
[2,1.5]	[2.5,3.5]	[1.1,1.1]	0.31	0.92	0.93	Skewed
[1,1]	[1,1]	[1.1,1.1]	0.54	0.74	0.75	Uniform
[1,1]	[1,1]	[0.8,0.8]	0.59	0.89	0.89	Uniform

a and b are the parameters used in (6.18).

performance functions, $h_i(x)$, should be re-defined in terms of the new variables:

$$\begin{aligned} \frac{\epsilon_0 A}{d} &\leqslant C_{up} \\ \frac{\epsilon_0 A}{d} &\geqslant C_{low} \\ t &\leqslant t_{\max} \\ d_0 &\leqslant d_{0_{\max}} \end{aligned} \tag{6.26}$$

where d is an implicit function of d_0 and t. For the capacitor introduced in Figure 6-2, the upper and lower limit of the capacitance at $V = 3.5$ V are the new design criteria for performance functions: $C_{up} = 0.53$ pF and $C_{low} = 0.37$ pF. The nominal capacitance at the same voltage is: $C_{nom} = 0.43$ pF. The results of yield optimization are presented in Table 6.3 and Figure 6-10. The numerical results of this problem display superior improvements in the yield, where for skewed joint distribution function the initial and optimized yield are 34% and 100%, respectively, and the error between estimated yield and Monte-Carlo simulation is only 1%.

It is worth to mention that the CPU time for yield calculated from (6.23) is much lower than M-C simulations due to the fact that M-C requires large number of random samples to provide high accuracy. This will increase the M-C computation time specifically for design optimizations where several iterations and a large number of function evaluation are needed to find the optimum design variables. For example, the elapsed time for M-C simulations with 100 random simulations and that proposed method (6.23) are 12.53 sec and 9.1×10^{-5} sec, respectively. In general, Monte-Carlo is an accurate simulation method to evaluate the results of random design parameters and includes more comprehensive details in modeling, but it is extremely time consuming for design optimization.

Comparing the results of two different problems (the device is the same, but the design

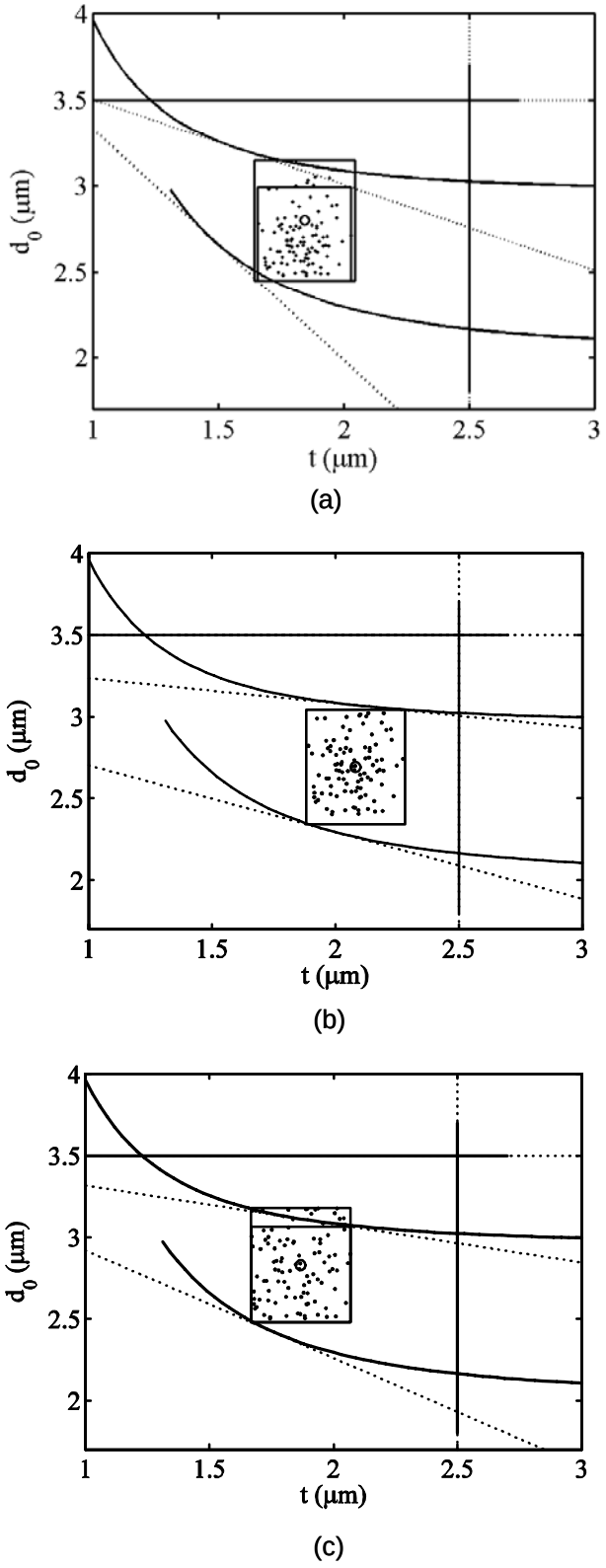


Figure 6-10: Yield optimization for: (a) skewed, (b) normal, and (c) uniform joint distribution functions.

Table 6.3: The results of yield optimization for design variable obtained from sensitivity analysis

Parameters		Tol. Box	Yield			Remarks
a	b	(δ)	Initial M-C	Final M-C	Estimated	(distribution)
[2,1.5]	[2.5,3.5]	[0.4,0.7]	0.34	0.99	1.00	Skewed
[1.6,1.6]	[1.8,1.8]	[0.4,0.7]	0.58	1.00	1.00	Normal
[1,1]	[1,1]	[0.4,0.7]	0.55	0.88	0.89	Uniform

a and b are the parameters used in (6.18).

parameters and performance functions are different) verifies that the proposed method can be advantageously used to improve the yield in the design stage without changing the design structure of increasing the process accuracy.

6.6 Summary

In this chapter, the uncertainties in MEMS fabrication processes and their effects on the performance of fabricated devices were addressed. It was also shown that process uncertainties can severely alter the output of a tunable capacitor from the designed values. A sensitivity analysis was then performed to find the design parameters with the most impact on the capacitor performance. After analyzing the fabrication uncertainties, a method for yield optimization of MEMS tunable capacitors was introduced. The optimization results in a set of optimum design variables and tolerance box, where the optimum tolerance ranges may be used for process modification to obtain 100% yield. As shown by numerical examples, the proposed method can drastically improve the yield in design stage without extra technological challenges for both symmetrical and nonsymmetrical distributions. This method is not limited to tunable capacitors and can be extended to other MEMS devices.

Chapter 7

Concluding Remarks

7.1 Thesis Contributions

In this thesis, analytical approximate models and novel parallel-plate-based MEMS tunable capacitors were developed. Also the fabrication challenges were addressed. The contributions of this research are categorized into the following topics:

1. Development of analytical models for electrostatically actuated parallel-plate-based devices: The analytical models developed in Chapters 3, 4 and 5 solve the coupled structural-electrostatic governing equations of a capacitive device with electrostatic actuation. The models include the flexibility of the electrodes and structural and geometric nonlinearities such as large deformations and mechanical contact. A comparison between the results of the proposed models and FEM analyses reveal that the error associated with approximations included in the analytical formulations are quite negligible for small deformations, where the computation time is over a thousand times less than that of FEM simulations. The models can be used in preliminary design stage to study the behavior of parallel-plate-based capacitors, sensors or actuators. They can also be used for optimization purposes since the response calculation for a device with a set of design variables takes only few seconds.

2. Development of linearly tunable capacitors: Different techniques were introduced for the design of parallel-plate-based MEMS tunable capacitors with linear capacitance-voltage

responses. The proposed designs were modeled, simulated, fabricated and tested. Using the geometric nonlinearity discussed in Chapter 3, a parallel-plate capacitor with maximum tunability up to 147% and highly linear regions with 30-50% tunabilities was introduced. The linearity factor, LF, for these designs varies from 0.975 to 0.9997. Geometric modifications and design optimizations proposed in Chapter 4 resulted in extremely linear three-plate capacitors with over 350% tunability, more than 250% of which is linear with $LF = -0.9997$. A triangular-plate capacitor equipped with middle beams was also designed and simulated which provided over 100% linear tunability with $LF = 0.9944$.

In Chapter 5, the flexibility of the moving electrodes was employed to design different capacitors with novel shapes and high tunability and linearity. The maximum tunability for these devices varied from 50% for segmented-plate capacitors to over 200% for fishbone-shape capacitors, where their linearity factor reached 0.999. Flexible-plate capacitors with rigid steps, and modified electrode shapes such as zigzag-shape were also introduced. The electrodes can be made of metal layers and a dielectric layer on top of the fixed plate prevents short circuit after pull-in or when the two electrodes touch one another. Therefore, the design technique developed in this thesis is a powerful tool to develop capacitors with high Q-factor for RF purposes. The technique can be used to systematically design capacitors with a smooth C-V response and without pull-in.

The optimizations and modifications applied to different designs such as trapezoidal shape for two-gap capacitors, butterfly shape for two segmented-plate and zigzag shape for flexible-plate designs are also implemented for the first time in this thesis. The results are quite satisfactory and standard fabrication processes can be used for their fabrication. Using the analytical models developed in this thesis and the optimization approaches discussed, one can design tunable capacitors based on pre-defined characteristics. The analytical models along with modification techniques and design optimization generate an efficient and powerful design package for MEMS capacitive elements and electrostatically actuated sensors and actuators.

Table 7.1 displays the summary of performances of eleven novel capacitors presented in this thesis.

Table 7.1: The summary of performances of new designs introduced in Capters 3 , 4 and 5

Capacitor Description	Max. tunability	Linear Tunability	Linearity factor, $\|LF\|$
Nonlinear-spring	$120\% - 147\%$	$30\% - 50\%$	$0.986 - 0.9997$
Modified two-gap	344%	–	–
Optimized three-plate	346%	$52\% - 262\%$	$0.999 - 0.99997$
Triangular-plate	152%	$78\% - 104\%$	$0.9932 - 0.9944$
Six-segmented-plate	58%	58%	0.994
Two-segmented-plate	108%	57%	0.990
Butterfly-shape	$89\% - 97\%$	$68\% - 70\%$	$0.994 - 0.998$
Teeth-equipped	$55\% - 68\%$	$55\% - 68\%$	$0.9904 - 0.9967$
Flexible-plate	$60\% - 130\%$	$36\% - 130\%$	$0.992 - 0.999$
Zigzag-shape	125%	125%	0.997
Fishbone-shape	200%	$145\% - 150\%$	$0.992 - 0.998$

3. Analysis of fabrication uncertainties and yield optimization: The effects of fabrication inaccuracies on the outcome of parallel-plate capacitors were addressed and a sensitivity analysis was performed to finds the most dominant parameters. The existing yield optimization method developed by Ponnambalam *et al.* was re-formulated for parallel-plate capacitors and the production yield was maximized in the design stage, without changing the topology of the device. Since the method can be implemented to cases with implicit performance functions, it can be utilized for different designs such as triangular-plate or segmented-plate capacitors, presented in this thesis, or be extended to other MEMS devices.

7.2 Thesis publications

The novel Linear designs and yield optimization method presented in this thesis resulted in 16 publications including 5 refereed journal papers, 8 refereed conference papers and 3 conference papers accepted for draft submission. The list of papers are as follow:

7.2.1 Journal Papers

1. **Shavezipur, M.,** Khajepour, A., and Hashemi, S. M., "The application of structural nonlinearity in development of linearly tunable MEMS capacitors", J. of Micromech. and Microeng., 18 (3), 2008, (In press).

2. **Shavezipur, M.,** Khajepour, A., and Hashemi, S. M., 2007, "Development of Novel

Segmented-Plate Linearly Tunable MEMS Capacitors", J. of Micromech. and Microeng., 18 (3), 2008, (In press).

3. **Shavezipur, M.,** Khajepour, A., and Hashemi, S. M., 2008, "A Novel Linearly Tunable Butterfly-Shape MEMS Capacitor", Microelectronics J., (In press).Type the first equation.

4. **Shavezipur, M.,** Ponnambalam, K., Khajepour, A., and Hashemi, S. M., 2007, "Fabrication Uncertainties and yield optimization in MEMS Tunable Capacitors" Sensors and Actuators A: Physical, June 2007, (Accepted).

5. **Shavezipur, M.,** Ponnambalam, K., Hashemi, S. M., and Khajepour, A., 2008, "A Probabilistic Design Optimization for MEMS Tunable Capacitors" Microelectronics J. (Accepted).

7.2.2 Conference Papers

1. **Shavezipur, M.,** Khajepour, A., and Hashemi, S. M., 2007, "Design and Optimization of a New Highly Linear Tunable MEMS Capacitor", Proc. of IMECE-2007, IMECE-42556, pp. 1-7.

2. **Shavezipur, M.,** Khajepour, A., and Hashemi, S. M., 2007, "A low sensitive, highly tunable butterfly-type MEMS capacitor", Proc. of IMECE-2007, IMECE-42556, pp. 1-6.

3. **Shavezipur, M.,** Hashemi, S. M. and Khajepour, A., 2007, "Novel highly tunable MEMS capacitors with flexible structure and linear C-V response", Proc. of IDETC-2007, DETC2007-35908, pp. 1-6.

4. **Shavezipur, M.,** Khajepour, A., and Hashemi, S. M., 2007, "Design Optimization of a Novel Two-Segmented-Plate MEMS Tunable Capacitor for Linear Capacitance-Voltage Response", Proc. of 21st Canadian Congress of Applied Mechanics, Toronto, ON, June 3-7, 2007, pp. 1-2.

5. **Shavezipur, M.,** Ponnambalam, K., Khajepour, A., and Hashemi, S. M., 2006, "Sensitivity Analysis in Yield Optimization of MEMS Tunable Capacitors", Proc. of IMECE-2006, IMECE-14752, pp. 1-8.

6. **Shavezipur, M.,** Khajepour, A., and Hashemi, S. M., 2006, "Design and Modeling of Novel Linearly Tunable Capacitors", Proc. of IMECE-2006, IMECE-14765, pp. 1-8.

7. **Shavezipur, M.,** Hashemi, S. M. and Khajepour, A., "Novel Linearly Tunable MEMS Capacitors with Flexible Moving Electrodes", ASME International Design Engineering Technical Conferences, DETC2008-49272. (Accepted)

8. **Shavezipur, M.,** Hashemi, S. M. and Khajepour, A., "A Novel Linear MEMS Capacitor with Triangular Electrodes and Nonlinear Structural Stiffness", ASME International Design Engineering Technical Conferences, DETC2008-49270. (Accepted)

9. **Shavezipur, M.,** Khajepour, A., Hashemi, S. M., and Nieva, P., 2008, "A Linearly Tunable MEMS Capacitor with Segmented Electrode and Enhanced Structural Stiffness", ASME International Mechanical Engineering Congress and Exposition, IMECE2008-68081 (Abstract accepted).

10. **Shavezipur, M.,** Khajepour, A., Hashemi, S. M., and Nieva, P., 2008, "Development of a Linearly Tunable Modified Butterfly-Shape MEMS Capacitor", ASME International Mechanical Engineering Congress and Exposition, IMECE2008-68090 (Abstract accepted).

11. **Shavezipur, M.,** Hashemi, S. M., Khajepour, A., and Nieva, P., 2008, "A Novel Fishbone-Shape MEMS Tunable Capacitor with Linear Capacitance-Voltage Response", ASME International Mechanical Engineering Congress and Exposition, IMECE2008-68092 (Abstract accepted).

7.3 Future Work

Some of the extensions of the presented research work are presented as follow:

- Extending the analytical model to flexible structures with initial curvature as a general case for electrostatically actuator devices with flexible structures.

- Combination of different design techniques to achieve high linearity and tunability, such as using rigid and flexible steps and teeth under the electrode at the same time.

- Development of linear capacitors using a dielectric layer with variable thickness and modified electrode shape for higher tunability and linearity.
- Development of an RF compatible process for fabrication of capacitors proposed in this thesis, using a metal-base fabrication process.
- Linearization of capacitive sensors and electrostatically actuated actuators using the same design techniques used in this thesis.
- Analysis of the effects of fabrication uncertainties on performance of sensors and actuators and maximizing yield.

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