Thin-Film Transistor Integration for Biomedical Imaging and AMOLED Displays

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

Thin film transistor (TFT) backplanes are being continuously researched for new applications such as active-matrix organic light emitting diode (AMOLED) displays, sensors, and x-ray imagers. However, the circuits implemented in presently available fabrication technologies including poly silicon (poly-Si), hydrogenated amorphous silicon (a-Si:H), and organic semiconductor, are prone to spatial and/or temporal non-uniformities.

While current-programmed active matrix (AM) can tolerate mismatches and non-uniformity caused by aging, the long settling time is a significant limitation. Consequently, acceleration schemes are needed and are proposed to reduce the settling time to 20 μs. This technique is used in the development of a pixel circuit and system for biomedical imager and sensor. Here, a metal-insulator-semiconductor (MIS) capacitor is adopted for adjustment and boost of the circuit gain. Thus, the new pixel architecture supports multi-modality imaging for a wide range of applications with various input signal intensities. Also, for applications with lower current levels, a fast current-mode line driver is developed based on positive feedback which controls the effect of the parasitic capacitance. The measured settling time of a conventional current source is around 2 ms for a 100-nA input current and 200-pF parasitic capacitance whereas it is less than 4 μs for the driver presented here.

For displays needed in mobile devices such as cell phones and DVD players, another new driving scheme is devised that provides for a high temporal stability, low-power consumption, high tolerance of temperature variations, and high resolution. The performance of the new driving scheme is demonstrated in a 9-inch fabricated display intended for DVD players. Also, a multi-modal imager pixel circuit is developed using this technique to provide

for gain-adjustment capability. Here, the readout operation is not destructive, enabling the use of low-cost readout circuitry and noise reduction techniques.

In addition, a highly stable and reliable driving scheme, based on step calibration is introduced for high precision displays and imagers. This scheme takes advantage of the slow aging of the electronics in the backplane to simplify the drive electronics. The other attractive features of this newly developed driving scheme are its simplicity, low-power consumption, and fast programming critical for implementation of large-area and high-resolution active matrix arrays for high precision.

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Dedication

To my lovely wife and kind parents

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Chapter 1

Introduction

We are witnessing a new generation of applications of thin-film transistors (TFTs) for flat panel imaging [1, 2, 3] and displays [4, 5, 6]. Unlike the active matrix liquid crystal display (AMLCD) where TFTs act as simple switches [7], in recent applications, the TFTs operate as analog components [3, 6].

1.1 Organic Light Emitting Displays

OLEDs have demonstrated promising features to provide a high-resolution, potentially low-cost, and wide-viewing angle displays. More importantly, OLEDs require a small current to emit light along with a very low operating voltage (3-10 V), leading to a very power efficient light emitting devices [4-6].

OLEDs are fabricated either by organic (small molecule) or polymeric (long molecule) materials. Small molecule OLEDs are produced by an evaporation technique in a high vacuum environment [8], whereas, polymeric OLEDs are fabricated by spin-coating or inkjet printing [9]. However, the efficiency of small molecule OLEDs is much higher than that of polymeric OLEDs.

To increase the efficiency of the OLED, an engineered band structure is adopted [8]. A typical multi-layer OLED and its corresponding banding diagram are illustrated in Figure 1.1. The indium tin oxide (ITO) layer is the anode contact. The hole-transport layer (HTL), a p-doped layer, provides holes for the emission layer (EML), and also prevents electrons from

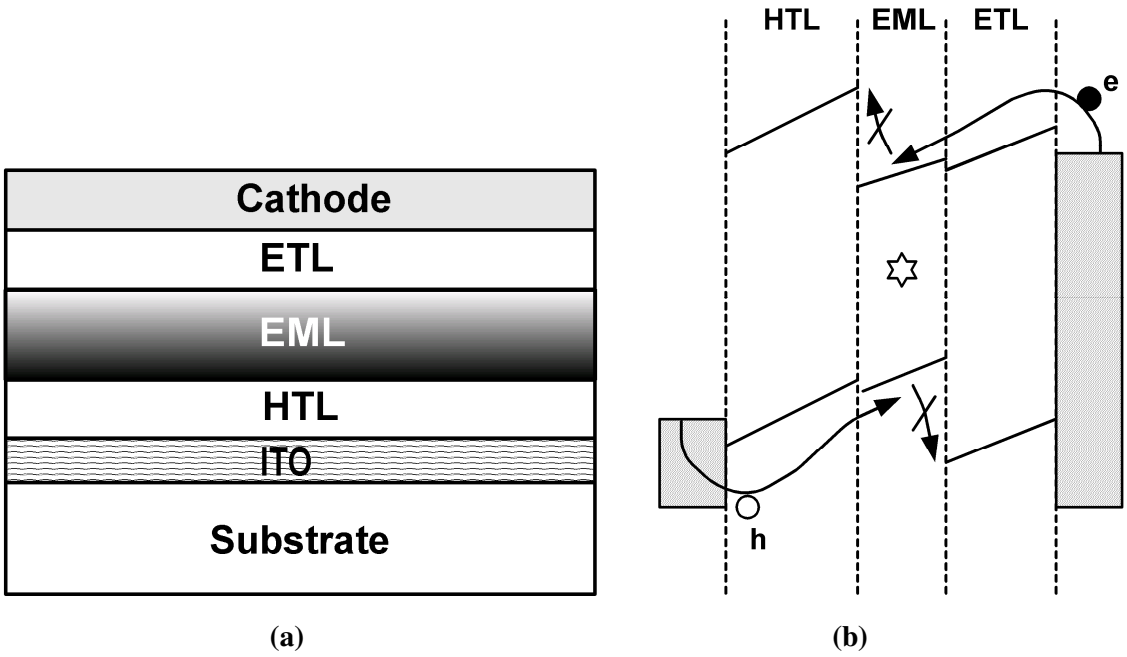


Figure 1.1: (a) Multi-layer OLED stack structure and (b) OLED banding diagram [8, 10].

traveling to the anode because of the band offset with the adjacent layers. For the cathode, the electron transport layer, an n-doped layer, provides electrons for the EML, and prevents the holes from traveling to the cathode. Then, the electrons and holes are recombined in the EML layer, resulting in the generation of photons [8, 10].

The luminance of OLEDs is linearly proportional to their current at low-to-mid current densities, and saturates at higher current densities. Also, the voltage of OLEDs increases over time due to crystallization, chemical reaction at the boundaries, changes in the charge profile of the layers, and oxidation due to the existence of oxygen and moisture [11, 13]. Consequently, most of the proposed driving schemes are designed to provide a constant current for OLEDs to eliminate the effect of shifts in the OLEDs' voltage.

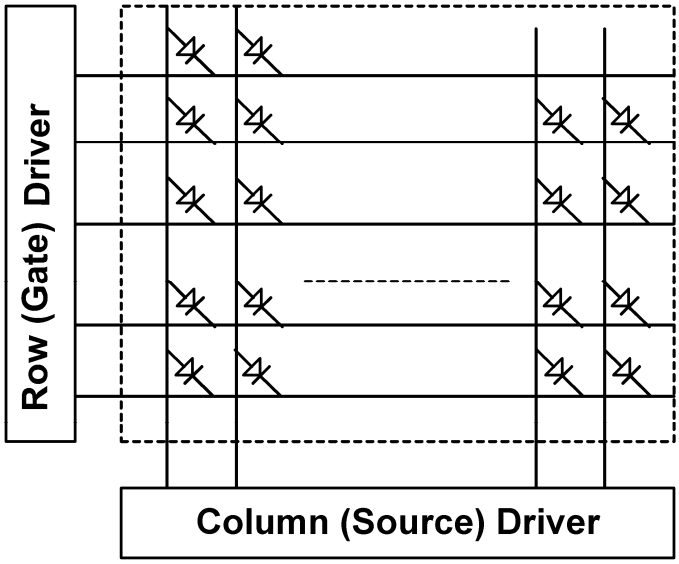


Figure 1.2: Passive matrix OLED display structure [16].

OLEDs offer great promise in either passive or active formats. Figure 1.2 portrays a passive matrix OLED (PMOLED) architecture. By applying a voltage across the appropriate row and column contacts, a specific pixel is addressed. Thereby, a current flows through the organic layers at the intersection of these contacts to light up the pixel. In this architecture, the luminance during the programming is averaged for the entire frame rate. Thus, the pixel should be programmed for NxL where N is the number of rows and L is the desired luminance for a frame [15, 16]. Thus, the OLED current density increases significantly, especially for higher resolution displays [5, 17]. Since the OLED efficiency drops at high current densities [18], to increase the display resolution, the current increases by a power law instead of linearly. Thus, the power consumption increases and the OLED ages faster. As a result, the actual applications of PMOLED displays are limited to small displays that have a low resolution [5].

To increase the resolution and area of the displays, active matrix addressing is selected [5]. A simplified active matrix OLED (AMOLED) display structure is illustrated in Figure

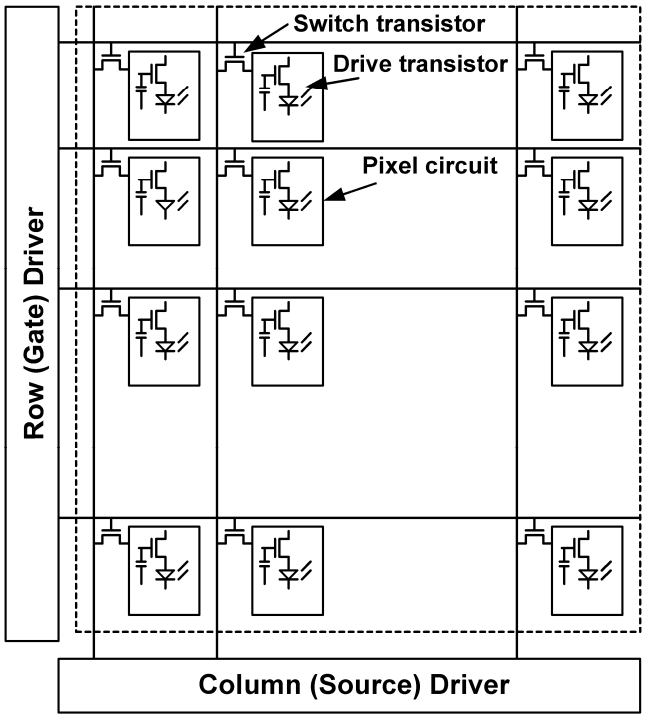
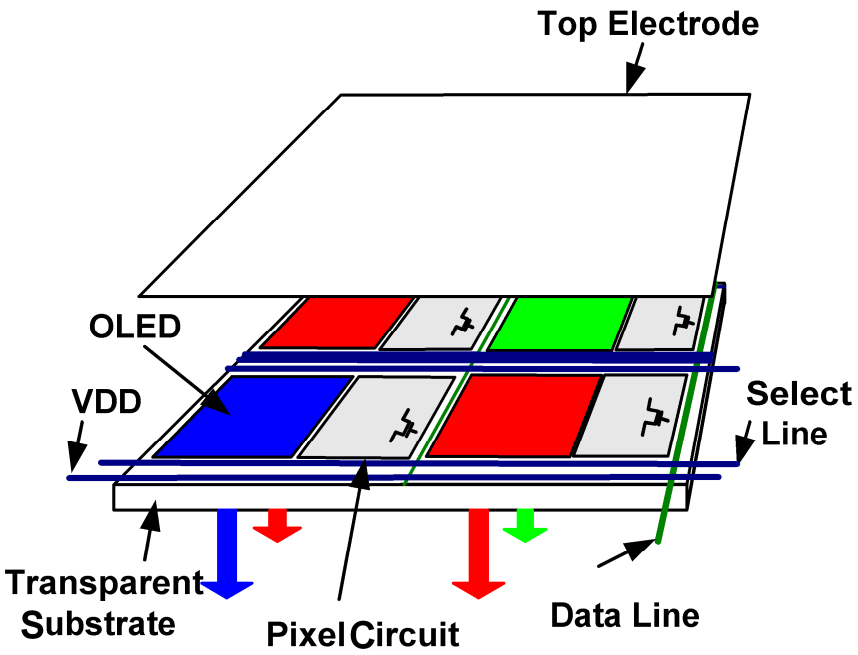


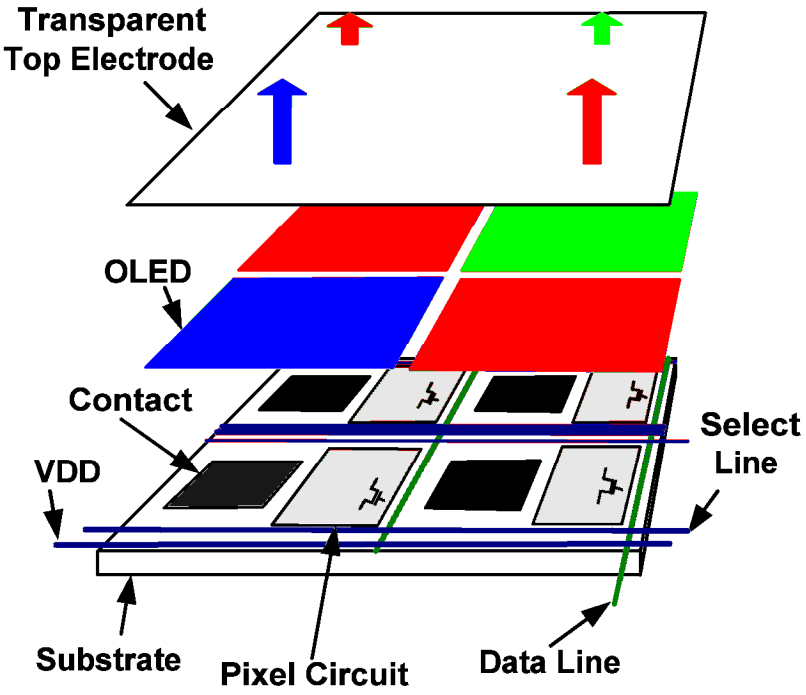
Figure 1.3: Active matrix OLED (AMOLED) display structure.

1.3, where the pixel current is controlled by a drive transistor. During the programming cycle, the switch TFT is ON, and the pixel data is stored in the storage capacitor. During the driving cycle, a current, related to the stored data voltage, is provided to the OLED. Since the pixel current is smaller in the AMOLED displays, they have longer lifetimes than PMOLED displays.

Figure 1.4 (a) reflects the structure of a bottom-emission AMOLED display in which the light passes through the substrate [19]. Thus the substrate is limited to transparent materials, and the aperture ratio is diminished by the area lost to the pixel circuitry, resulting in a higher current density. Moreover, the aperture ratio becomes more critical when considering a more complex pixel circuit to compensate for both spatial and temporal non-uniformities. Hence, top-emission displays are preferred (see Figure 1.4 (b)). It provides for more than a 80% aperture ratio, and the substrate is not required to be transparent [20].



(a)



(b)

Figure 1.4: Bottom and top emission AMOLED pixel structure [19, 20].

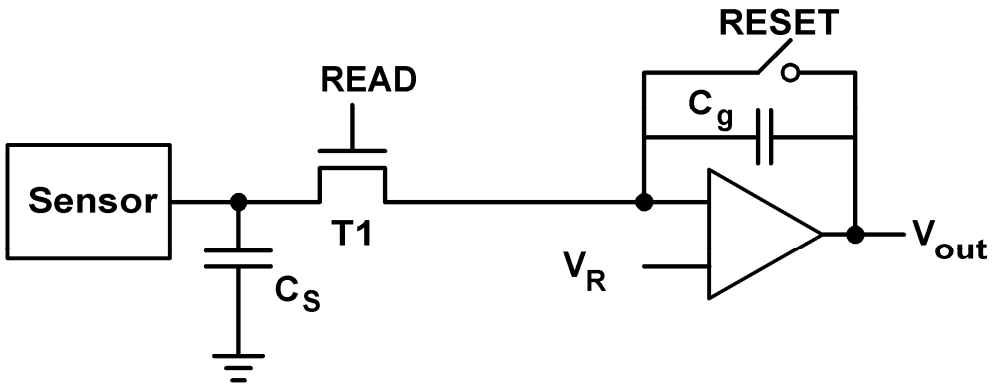


Figure 1.5: PPS imager pixel circuit [1, 2].

1.2 Flat-Panel Biomedical Imagers

Large-area flat panel digital imaging has been valued for its advantages, including the separation of detector, image storage, and display, which facilitates independent improvement by isolating the complexity of the different parts from each other. Moreover, it enables the use of digital processing of the captured images to improve visual quality and to make feasible, the use of computer-aided diagnostics [2]. The basic blocks of a flat panel imager include a sensor and a readout circuitry using transistors which act either as a switch or as an amplifier. The sensor, commonly used in these applications, is a PIN or a MIS diode in the case of indirect detection (in which x-rays are converted to optical signals by phosphor layers) or amorphous selenium for direct detection (whereby the incident x-rays are directly converted to electrical charge).

Figure 1.5 shows a passive pixel sensor (PPS) architecture in which the pixel consists of a switch TFT and a capacitor. The charge generated by the sensor is integrated into the storage capacitor which is read out by a charge-pump amplifier, while the switch TFT is ON. The gain of the PPS pixel is given as

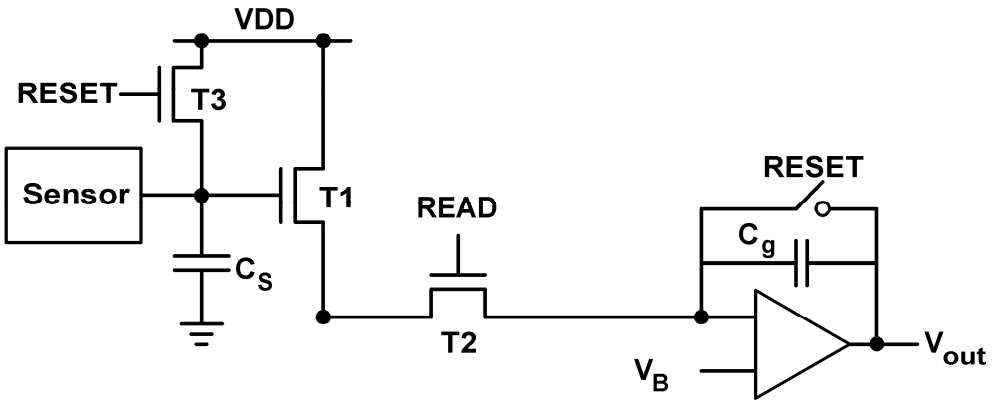


Figure 1.6: 3-TFT APS imager pixel circuit [3].

$$V_{out} = Q(t)t_{\text{int}} / C_g . \tag{1.1}$$

Here, Q(t) is the charge generated by the sensor and t_{int} the integration time. However, due to non-uniformities such as noise and leakage currents, the minimum level, detectable by PPS pixel, is limited.

To improve the sensitivity to small intensity signals, an active pixel sensor (APS) was introduced by Matsuura [3] (see Figure 1.6). Here, the storage capacitor is charged to a reset voltage. Then, the collected sensor charge into the storage capacitor modulates the current of the amplifier TFT (T1) as

$$I_{px} = g_m Q(t)t_{\text{int}} / C_s \text{ and } V_{out} = I_{px} t_{read} / C_g , \tag{1.2}$$

in which g_m is the transconductance of T1, and t_{read} the time associated with the readout cycle. However, for high intensity input signals, the on-pixel gain saturates the readout circuitry. In particular, for bio-medical x-ray imaging applications, the significant contrast in the signal intensity of the different imaging modalities mandates unique pixel design.

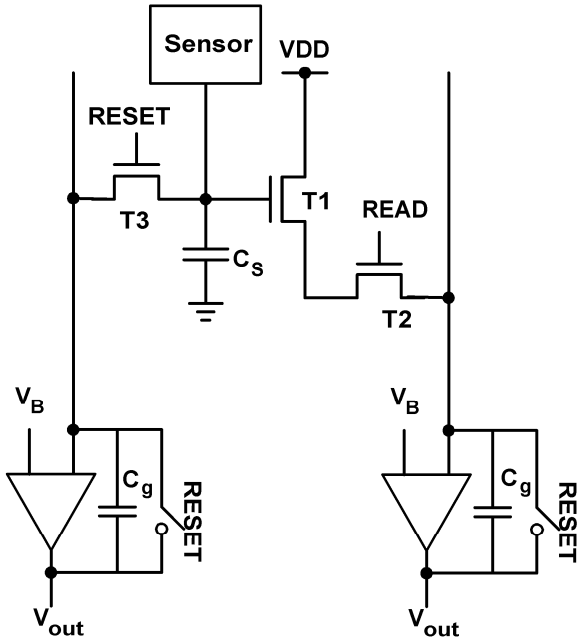


Figure 1.7: Hybrid active-passive imager pixel circuit [23].

Recently, hybrid mode pixel circuits have been reported that can operate between the passive and active readout for modalities employing high and low x-ray intensities, respectively. Figure 1.7 shows the 3-TFT hybrid pixel circuit presented in [23]. The issue with this type of a circuit is that it can be optimized for only active or passive operation. For example, in the active readout mode, a small storage pixel is required to improve the SNR [23], whereas, in the passive readout, a large storage capacitor is needed to avoid saturation, improving the maximum detectable signal intensity. Also, a high resolution (2-TFT) version of this pixel has been reported [24]. In addition to a limited dynamic range, this circuit suffers from cross talk and accelerated aging of TFTs. In particular, during the readout cycle of a row, the amplifier TFTs in pixels of inactivated rows are in the linear regime resulting in relatively high cross talk and accentuated aging [25]. Moreover, to achieve linear sensitivity,

Table 1.1: Comparison of TFT backplane technologies for large-area electronics [26].

Attribute	**a-Si:H**	**poly-Si**	**mc/nc-Si:H**	**organic**
Circuit type	n-type	n-type/p-type	n-type/p-type	p-type
Mobility *(cm2/Vs)*	< 1	10~100	~1 to 10	~ 1
Temporal Stability (ΔV_T)	issue	more stable than a-Si:H	more stable than a-Si:H	improving
Initial Uniformity	high	low	potentially high	low
Manufacturability	mature	Developing	Research	Reseach
Cost	low	high	low	potentially low

the amplifier TFT is biased in the linear regime, which makes it very susceptible to IR drop and ground bouncing.

1.3 Backplane Technologies

The pixel circuits discussed above can be fabricated using different technologies, notably, poly silicon (poly-Si) [27, 28, 29] and hydrogenated amorphous silicon (a-Si:H) [3, 6, 30]. Poly-Si technology offers high-mobility and complementary (n-type and p-type) TFTs [28, 29], but has an undesirable large range of mismatched parameters over an array [31, 32]. This is due to the random distribution of the grain boundary in the material [31].

In contrast, a-Si:H provides low mobility TFTs and does not provide p-type devices [33]. Also, the threshold voltage of TFTs increases (V_T-shift) under prolonged bias stress due to the inherent instability of a-Si:H material [34, 35]. Despite these issues, the technology provides good uniformity over a large area. More importantly, a-Si:H technology's industrial accessibility, by virtue of its usage in the AMLCD [7], provides for low-cost large-area electronics. In particular, an a-Si:H TFT backplane has the benefit of all the desirable attributes of the well established a-Si:H technology, including low-temperature fabrication

on plastic for eventual flexible electronics. Table 1.1 lists the attributes of different possible fabrication technologies.

In addition, promising research has been carried out on new materials such as hydrogenated nano/micro crystalline (nc/mc) silicon [36, 37, 38], and organic semiconductors [39, 40]. The nc/mc-Si:H technology provides higher temporal stability [37, 38] and mobility [36] compared to a-Si:H technology. On the other hand, organic semiconductor has demonstrated extremely low cost fabrication including inkjet printing. However, this technology suffers from bias-induced [41, 42] and environment-induced instabilities [43] and poor uniformity [44].

1.4 Thesis Outline

Chapter 2 presents the challenges and design considerations for imaging and display applications in which we discuss the principle of different driving schemes, including voltage and current programming. The major drawback of these driving schemes is settling time which is investigated for both voltage and current programming; the proposed solution for improving voltage programming is presented in Appendix A.

A simple acceleration technique for current programming is detailed in Chapter 3. An imager/sensor pixel circuit is discussed, followed by short-term stressing to improve the temporal stability; a more detailed description of this technique is presented in Appendix B. Also, presented is a pixel circuit for implementation of a 16x12 biomedical sensor. To improve the pixel dynamic range, a variable capacitor is used to mitigate the integration of the charge generated by the sensor, and also to improve the gain for very low intensity input signals. The acceleration technique is also demonstrated for stabilizing AMOLED displays.

Here, measurement and simulation results are presented for extreme spatial and temporal instability are presented.

Chapter 4 discusses the use of a positive feedback to improve the settling time for very small programming currents (~100 nA). Since the system is non-linear, the stability of the system is investigated using the Lyapunov approach. The operation and stability of a circuit implementation of the driving scheme is also detailed. Measurement results for the circuit and the offset-leakage cancelation technique, developed for small current levels, are discussed.

For applications where cost is critical including small area displays, a new charge based compensation technique is presented in Chapter 5. Here, the cost of implementation is reduced by simplifying the external driver requirements. Moreover, a novel relaxation technique is introduced to improve the stability of the AMOLED pixel circuit. The implementation of 9-inch and 2-inch displays is discussed, followed by stability measurement results for the 9-inch displays. The charge-leakage technique is also adopted in the development of extremely high dynamic range biomedical imager pixel circuit. The gain-adjustability measurement results of the circuit are presented and the noise performance of the pixel circuit is analyzed.

To meet the specification for high resolution applications such as large-area AMOLED displays, a highly accurate compensation technique is required to reduce the effect of temporal/spatial mismatches to less than 0.5%. To achieve 0.5% uniformity, a successive calibration technique is proposed in Chapter 7. Its implementation using a single-bit current comparator is reviewed. Measurement results for the current comparator and successive calibration are discussed. This method can control the non-uniformities in other components

such as sensor and OLED. Calibration of the OLED with this technique is described in Appendix C.

Chapter 7 concludes this thesis.

Chapter 2

Specifications and Considerations

As described in Chapter 1, technologies such as poly-Si, a-Si:H, and organic semiconductors are available for the fabrication of pixel circuits. Figure 2.1 demonstrates three most used TFT structures. Since the bi-layer staggered bottom-gate structure requires fewer mask sets and processing steps, it is highly adapted in an industrial scaled a-Si:H fabrication. However, this structure is prone to a higher leakage current, since the back-side of a-Si:H layer is damaged during the process. An alternative solution to this structure is tri-layer structure in which an etch stopper layer is used to preserve the a-Si:H layer. However, tri-layer structure has more mask layers and process steps compared to the bi-layer structure which makes the industry resilient to adopt the tri-layer structure. For poly-Si TFTs, the coplanar top-gate structure is the most common structure. This structure enables recrystallization of amorphous silicon layer after deposition. Also, it supports self-alignment, resulting in smaller design rules and TFT sizes.

2.1 Temporal and Spatial Non-Uniformity

Each of these fabrication technologies is associated with drawbacks for circuit design. However, the key challenge in using the available technologies is the temporal or spatial non-uniformities. In a-Si:H technology, the threshold voltage of the TFTs tends to shift (V_T-shift) under prolonged bias stress condition (denoted in Figure 2.2). Considering that each pixel in most applications experiences different biasing conditions, the V_T-shift will increase the non-

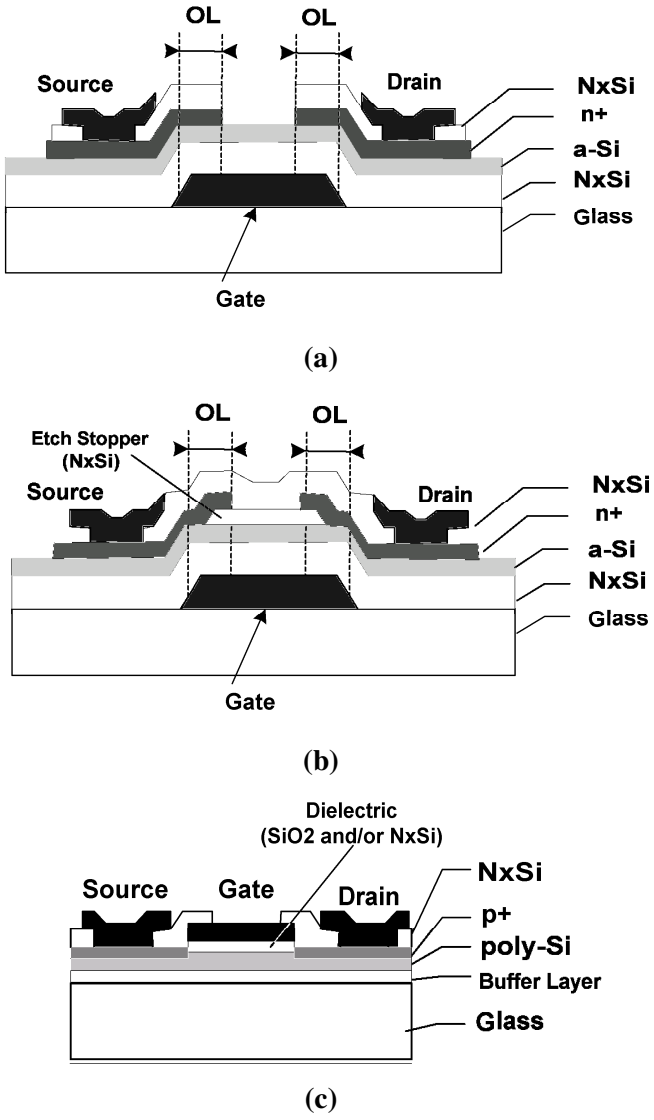


Figure 2.1: Different TFT structures: (a) bi-layer inverted staggered, (b) tri-layer inverted staggered, and (c) coplanar.

uniformity across the panel over time. This phenomenon occurs due to charge trapping and/or defect state creation [45, 46]. The V_T-shift has been modeled under different conditions including constant voltage [45, 46], constant current [47], and pulsed stress conditions [48, 49]. Depending on different applications, one of these models can be applied to extract the aging of the pixel. However, in the applications that TFT is under a constant

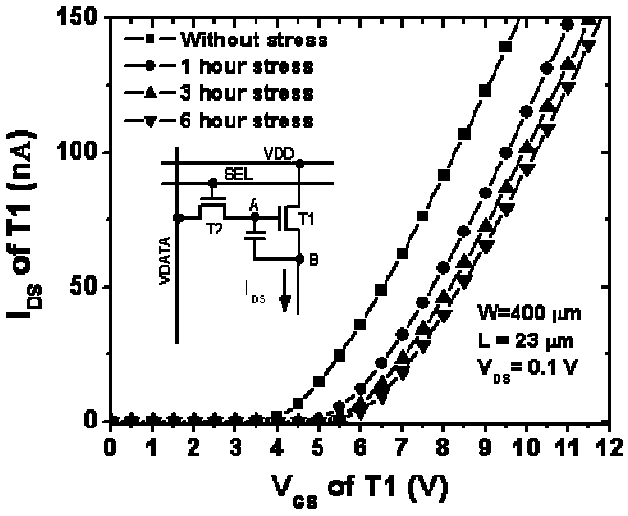


Figure 2.2: Biased induced V_T-shift (stress condition: V_{GS} = 10 V, V_{DS} = 0.1 V).

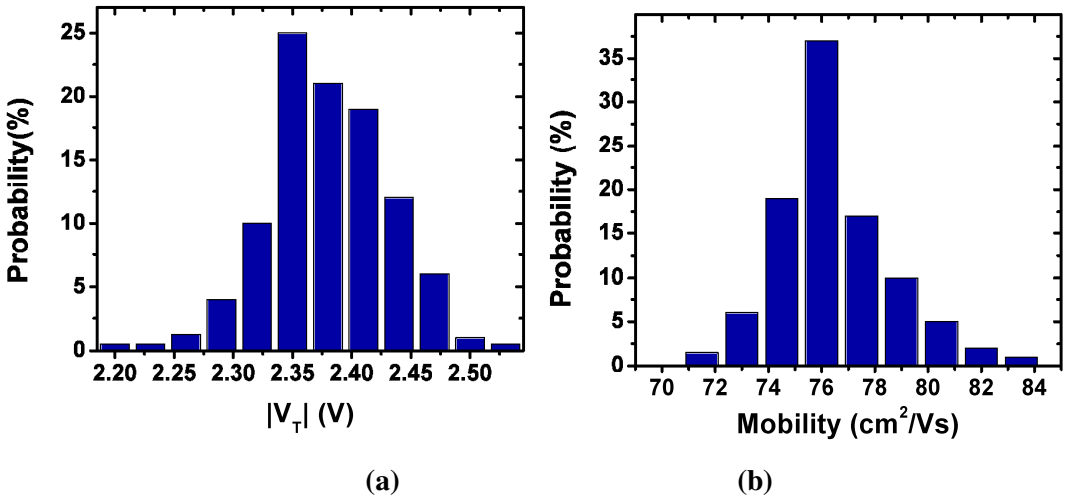


Figure 2.3: (a) V_T and (b) mobility variation in poly-Si TFTs (adapted from [32]).

current stress, the V_T-shift is severe [47] and unlike the TFT under constant voltage stress, the V_T shifts tends to increase forever.

Also, poly-Si TFTs are more stable but suffer from initial non-uniformities caused by recrystallization methods [31, 32]. Since the channel of a TFT consists of several randomly oriented crystalline grains, the interface of these grains (grain boundaries) can manipulate the

mobility and V_T. Figure 2.3 shows the stochastic results gather from a set of 600 poly-Si TFTs. It is evident that both V_T and mobility are prone to mismatch.

2.2 Compensation Schemes

Although, the initial spatial mismatches results in an after-fabrication non-uniformity reducing the yield significantly, the temporal instability increases the non-uniformity over time, and shortens the lifetime of the device. However, the initial spatial mismatches and temporal instability tend to cause the same effect in the pixel circuit. As a result, most of the compensation techniques control both spatial and temporal non-uniformity. The two primary compensation techniques, introduced to improve the yield/lifetime and panel quality, are current and voltage driving schemes [6].

2.2.1 Current Driving Scheme

Current-programmed active matrix (AM) architectures are attractive for displays and sensors independent of the fabrication technology because of their ability to tolerate mismatches and non-uniformity caused by aging.

Figure 2.4 illustrates two different pixel circuits, based on the current cell and current mirror. Two current programmed pixel circuits (CPPCs) for AMOLED displays and flat-panel imagers are depicted in Figure 2.5. Here, a shared data line is connected to the I_{in} port of the pixels in one column and a current source is used as part of peripheral circuitry to program the pixels row by row. Figure 2.6 (a) shows a detailed model of the data line, in which R_i (i= 1 to n) stems from the sheet resistance of the metal, C_i (i= 1 to n) the parasitic capacitances stemming from the line and pixels, and I_{Li} (i= 1 to n) the leakage current contribution of the i^{th} pixel. In addition, the switches, used to form the pixel circuits, are not ideal, adding resistance (R_s) to the path of the programming current. It is noteworthy that the

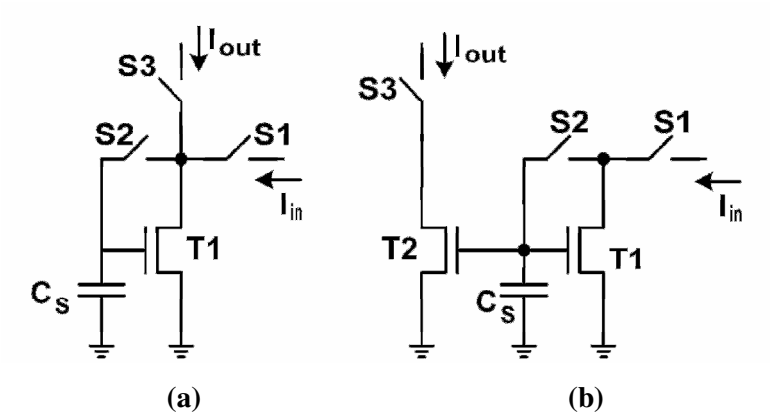


Figure 2.4: Current programmed pixel circuits; (a) current cell and (b) current mirror.

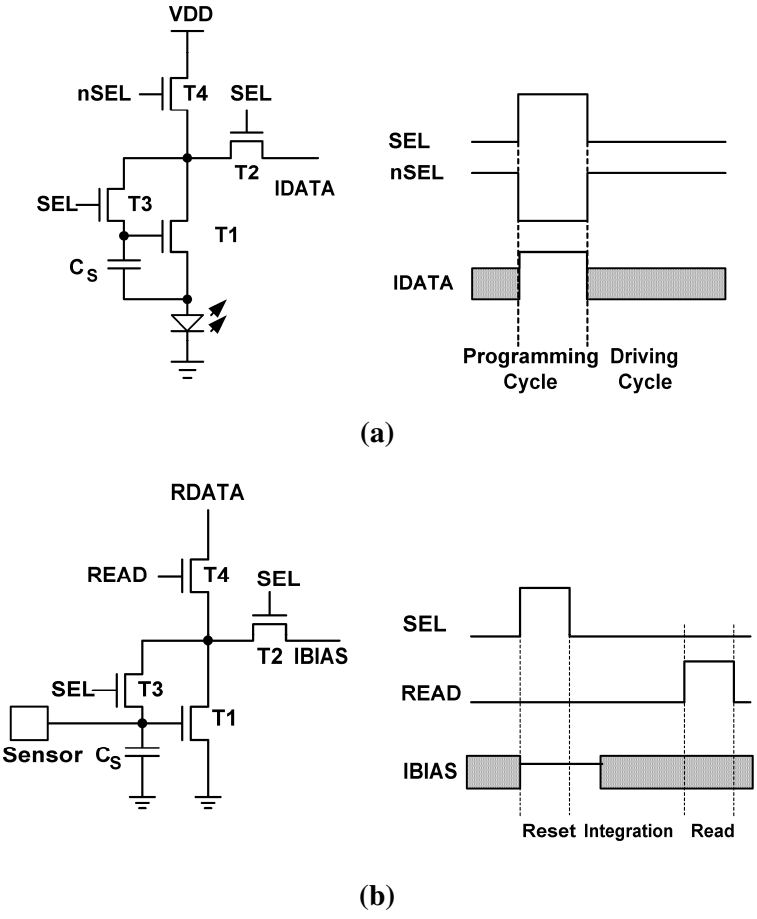


Figure 2.5: Current programmed pixel circuit (CPPC) for (a) AMOLED displays (adapted from [50]) and (b) flat-panel imagers (adapted from [51]).

value of Ri (i= 1 to n) is a few ohms whereas the Rs can be as high as few 100 KΩ. To simplify the analysis, the first order model in Figure 2.6 (b) [9] is selected. Here, C_P and I_L

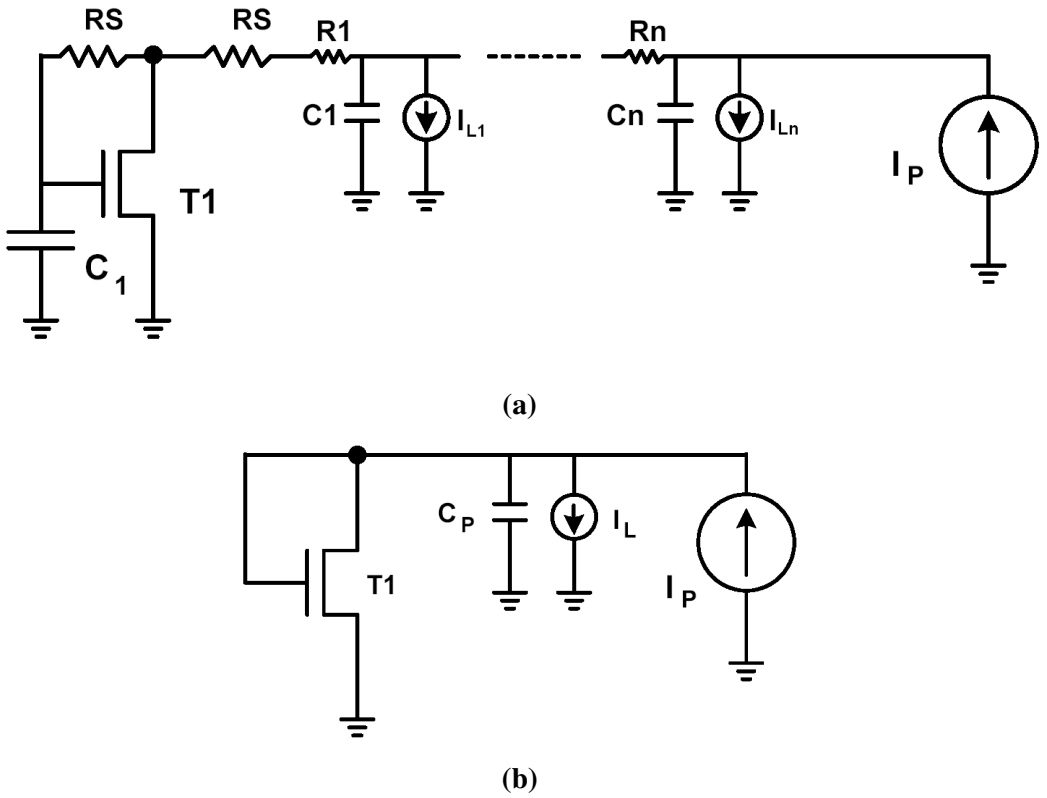


Figure 2.6: (a) Line model for a column during the programming cycle and (b) its simplified equivalent.

represent the effective parasitic capacitance and leakage current, respectively. As discussed in [6], assuming that T1 is in the saturation regime and $I_L = 0$, the behavior of the pixel based on Figure 2.6 (b) is given by

$$V(t) = \sqrt{\frac{I_P}{K}} \cdot \left(\frac{1 - v_a \exp\left(-\frac{t}{\tau}\right)}{1 + v_a \exp\left(-\frac{t}{\tau}\right)} \right)^2 \text{ and } V_a = \frac{\sqrt{\frac{I_P}{K}} - (V_0 - V_T)}{\sqrt{\frac{I_P}{K}} + (V_0 - V_T)}. \quad (2.1)$$

Here, $V(t)$ is the line voltage, I_P the programming current, V_0 the pre-charged voltage of the data line, V_T the threshold voltage of T1, K the gain in the I-V characteristics of *T1* ($I_{DS} = K(V_{GS}-V_T)^2$) [52], and $\tau = 2C_P/(K.I_P)^{0.5}$. Considering the fact that C_P is large and K is small, the settling time becomes longer.

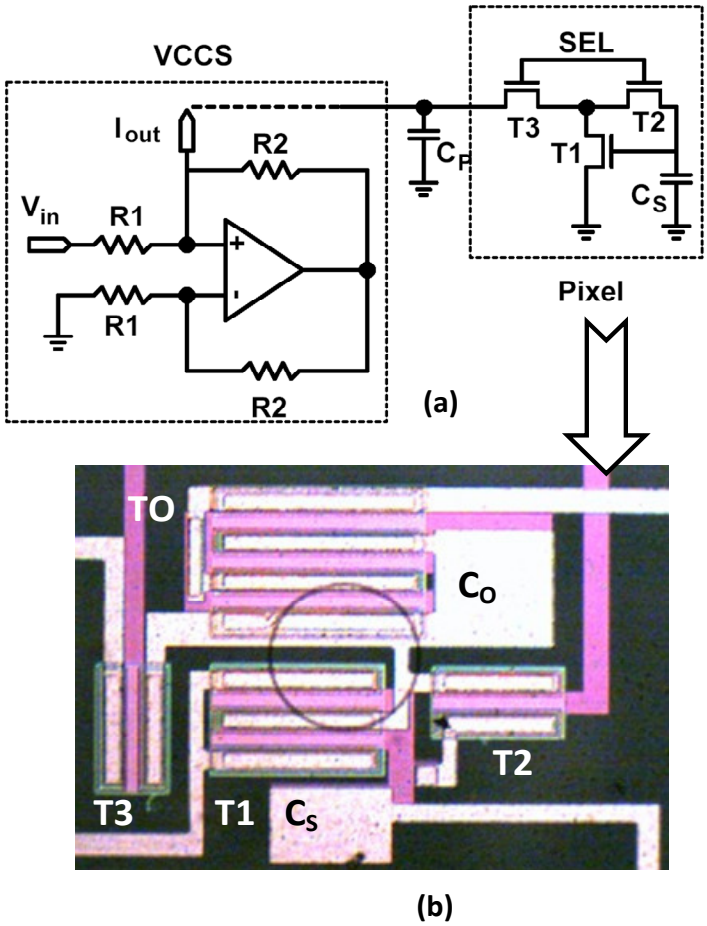


Figure 2.7: (a) Discrete VCCS and (b) photomicrograph of fabricated current cell in amorphous silicon technology.

To investigate the actual settling time, an a-Si:H pixel circuit, based on Figure 2.4 (b), is used with an external parasitic capacitance, along with a voltage controlled current source (VCCS), in which $I_{out} = V_{in}/R1$ (see Figure 2.7(a)). A photomicrograph of the pixel circuit is depicted in Figure 2.7 (b) and its parameters are listed in Table 2.1. Since the pixel is fabricated for the AMOLED display, the components TO and C_O are used to emulate the OLED and its intrinsic capacitance. It is noteworthy that to generalize the analysis for imaging and display applications, the effect of the OLED capacitance in equation (2.1) must be eliminated. Thus the second terminal of TO and C_O is left unconnected for the settling

time measurements to be consistent with the analysis. The 5% settling time of the drain-source current (I_{DS}) of T1 is measured by Tektronix TDS 5054 5 GS/s oscilloscope. Figure 2.8 indicates that the settling time increases linearly with parasitic capacitance (C_P) as predicted in (2.1). Considering a 240-row array structure with a 60-Hz frame rate, the programming time for each row is less than 70 μs. As shown in Figure 2.8, the settling time is higher than 70 μs and becomes even more severe for larger parasitic capacitances, which is true in the case of large-area devices such as displays and x-ray imagers.

Table 2.1: Parameters of the amorphous silicon current cell.

Name	Description	Value
W/L(T1)	Aspect ratio of T1 (μm)	400/23
W/L(T2)	Aspect ratio of T2 (μm)	100/23
W/L(T3)	Aspect ratio of TFT used for OLED (μm)	100/23
C_S	Storage capacitance (pF)	1

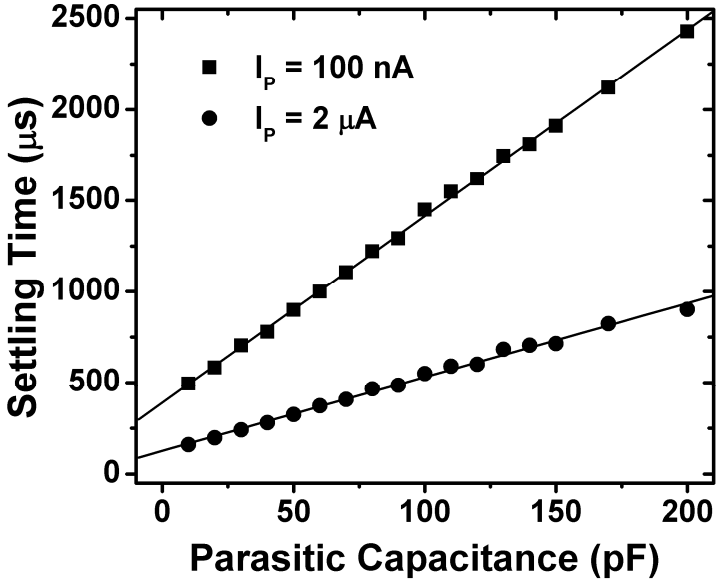


Figure 2.8: Measured settling time as a function of parasitic capacitance for large and small programming currents.

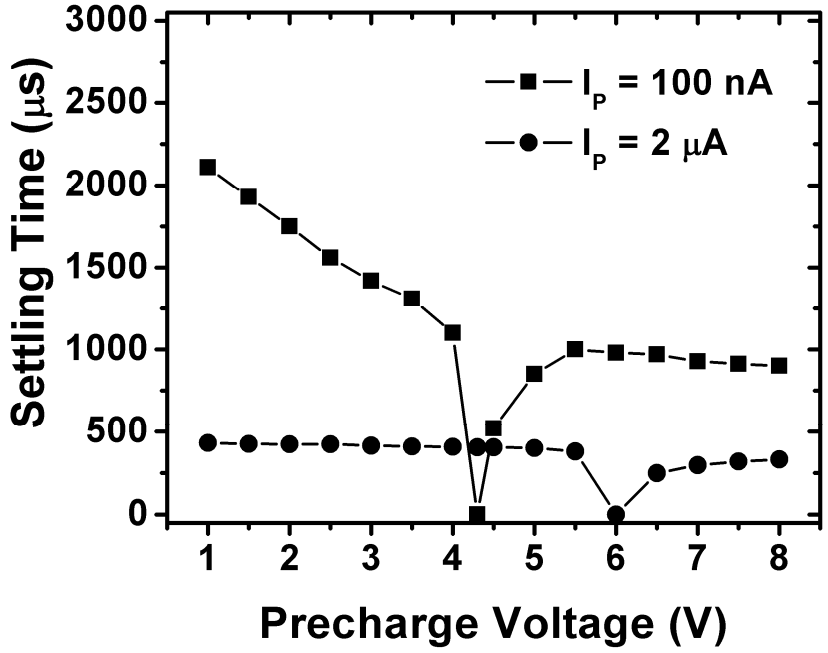


Figure 2.9: As in Figure 2.8, but settling time is as a function of the pre-charge voltage.

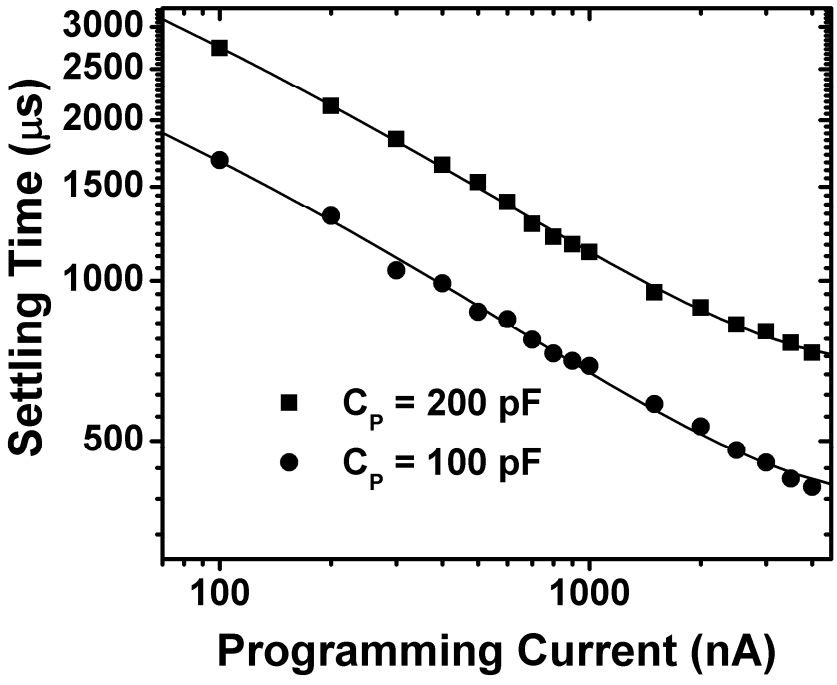


Figure 2.10: Settling time as a function of the programming current for different parasitic capacitances.

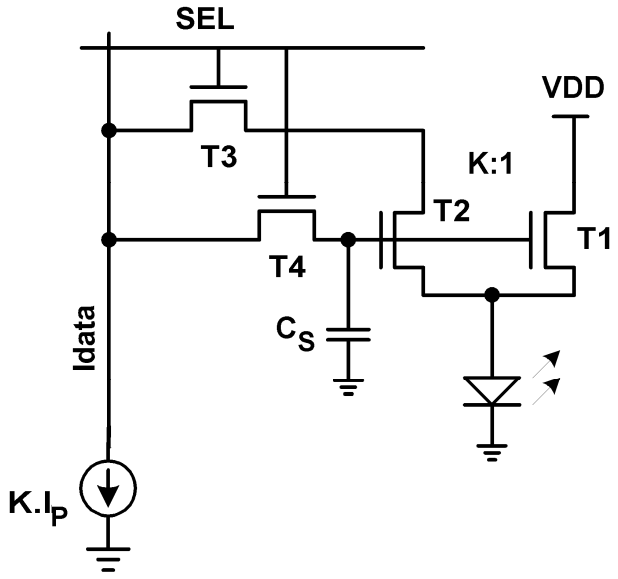
The effect of the pre-charging voltage (V_0) on the settling time is demonstrated in Figure 2.9. As the pre-charging voltage gets closer to the final voltage (V_f) characteristic for a specific programming current, the settling time drops significantly. However, due to the high level of mismatch, a priori selection of a suitable pre-charging voltage is not practical. Figure 2.10 shows the effect of programming current (I_P) on the settling time, where the V_0-V_f is 1 V. As (2.1) predicts, the settling time should drop linearly on a logarithmic scale as the programming current increases. However, the measurement results do not show the presence of perfect correlation at large current levels. This could be due to the resistance of the switch transistors. Assuming that the V_{DS} of the switches is small, the resistance of the switches is a given by

$$R_S \approx \frac{1}{K_S (V_H - V_L - V_{TS})}. \tag{2.2}$$

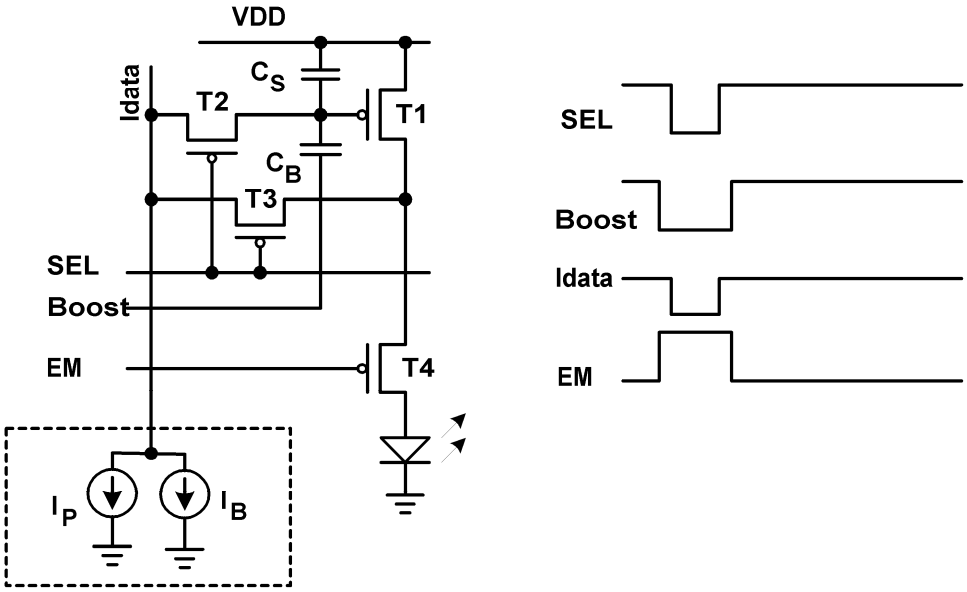
Here, K_S is the gain in the IV characteristics of switches, V_H the select voltage, V_L the voltage on the data line, and V_{TS} the threshold voltage of switches. Thus, for a given select voltage, the resistance of the switches increases as the voltage of the data line increases due to larger currents. As a result, the actual settling time deviates from that predicted by the first order model shown in Figure 2.6 (b).

Although, several solutions have been proposed to accelerate the settling time [14, 53, 54, 55], the effectiveness of those solutions, coupled with power consumption and/or circuit overhead, is a lingering issue.

2.2.1.1 Scaling Acceleration



(a)



(b)

Figure 2.11: Acceleration driving scheme: (a) scaling (adapted from [14]) and (b) additive (adapted from [53]).

Acceleration techniques, based on scaling, have been used in current mirror and current cell architectures for settling time reduction [14]. Figure 2.11 (a) denotes a current-mirrored

current-scaling pixel circuit. Here, the programming current is *k* times larger than the actual current required for the pixel circuit and the current is scaled down at the pixels. In particular, for very low currents, of the order of 100 nA, *k* should be several hundred.

2.2.1.2 Additive Acceleration

The other solution is additive acceleration in which bias current (I_B) is added to the actual current and is subtracted locally at the pixel [53, 54, 55] (illustrated in Figure 2.11 (a)). This method is more effective for low current levels compared with the scaling method, and is applicable to both current mirror and current cell pixel architectures [17]. However, the bias current can be large, leading to high power consumption. This can be a major concern in portable devices such as small displays, and more importantly, the subtraction of this bias current potentially reduces the immunity to mismatches and temperature fluctuations.

2.2.2 Voltage Driving Scheme

The voltage driving schemes have been mostly adapted in the AMOLED pixel circuits [6, 56]. In voltage driving schemes in order to compensate for the V_T-shift in a-Si:H or V_T-mismatch in poly-Si TFTs, the gate-source voltage (V_{GS}) of drive TFT must include the programming voltage and the V_T of the drive TFT. Here, the major operating cycles are V_{comp}-generation, V_T-generation, programming, and driving [57, 58]. In the pre-charging cycle, a compensating voltage is stored in the storage capacitor. During the V_T-generation cycle, the voltage stored in the storage capacitor discharges through the diode-connected drive TFT until it turns off, so the gate-source voltage is equal to the V_T of the drive TFT. In the current-regulation cycle, a programming voltage (V_P) is added to the generated V_T, resulting in a gate-source voltage as V_P+V_T. Therefore, during the driving cycle, the pixel current is given by

$$I_{pixel} = K(V_P)^{\alpha}. \quad (2.3)$$

Based on the method used to add a programming voltage (V_P) to the generated V_T, the voltage-programmed pixel circuits (VPPCs) can be divided into four different categories: stacked, parallel-compensation, boot-strapping, and mirror VPPCs.

2.2.2.1 Stacked Voltage Programming

Figure 2.12 shows the simplified circuits for a typical stacked VPPC during different operating cycles [59, 60]. Here, C_S is the storage capacitor, and C_{OLED} the OLED capacitor. During the pre-charge cycle, node B is charged to $-V_{comp}$. During the V_T-generation cycle, node B is discharged until T1 turns OFF so that the voltage at node B becomes $-V_T$ of T1. In the current-regulation cycle, node A is charged to V_P. Considering that C_{OLED} is large, the voltage at node B stays at $-V_T$, resulting in the V_{GS} of T1 as V_P+V_T.

Two pixel circuits, based on this driving scheme, are depicted in Figure 2.13. In the 3-TFT pixel circuit [59], T3 and T1 reduce to the diode-connection configuration during the V_T-generation cycle (third operating cycle). Also, the programming voltage is written into storage capacitor (C_S) through T2. Here, the OLED should be patterned to enable changes to *Vca* of each row without affecting the other rows in the matrix structure. In the 2-TFT pixel circuit presented by Reza [60] (Figure 2.13 (b)), during the V_T-generation cycle (second operating cycle), the gate terminal of i is connected to V_{ref} through T2, and the drain terminal is connected to a high positive voltage (VDD). Also, T2 is used to write the programming voltage into storage capacitor C_S.

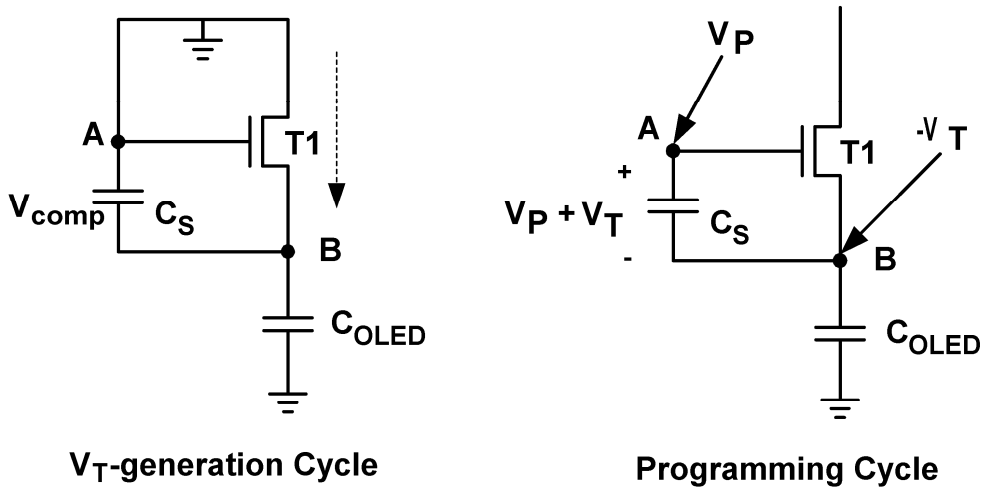


Figure 2.12: Stacked VPPC configurations during different operating cycles.

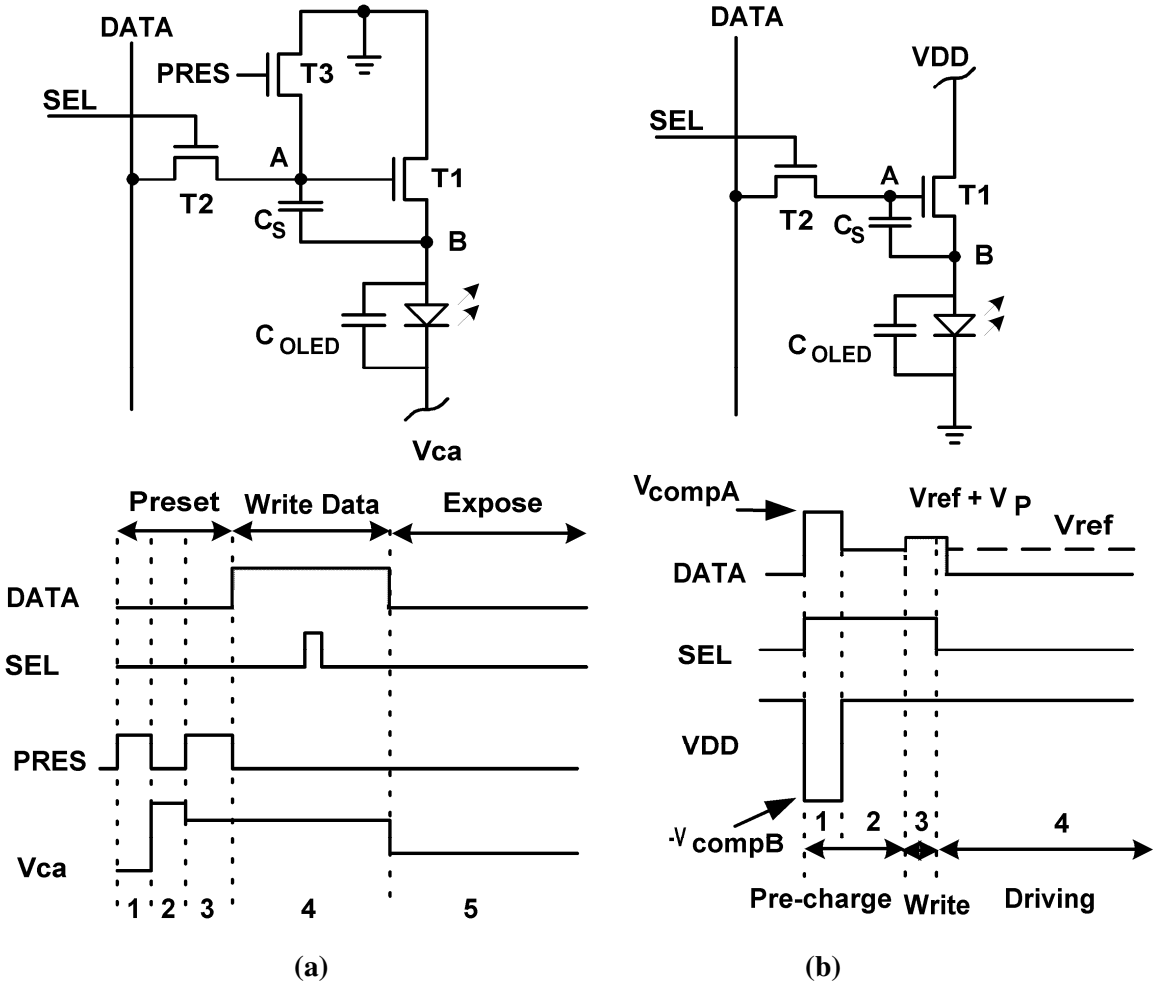


Figure 2.13: Stacked VPPCs; (a) 3-TFT pixel circuit (adapted from [59]) and (b) 2-TFT pixel

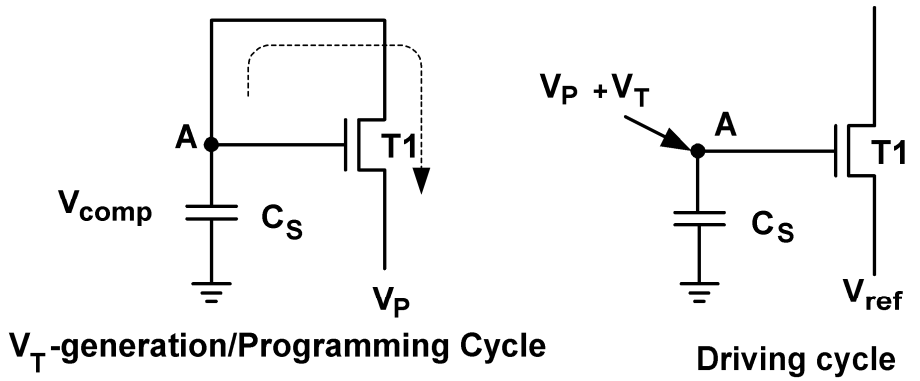


Figure 2.14: Parallel-compensation VPPC configurations during different operating cycles.

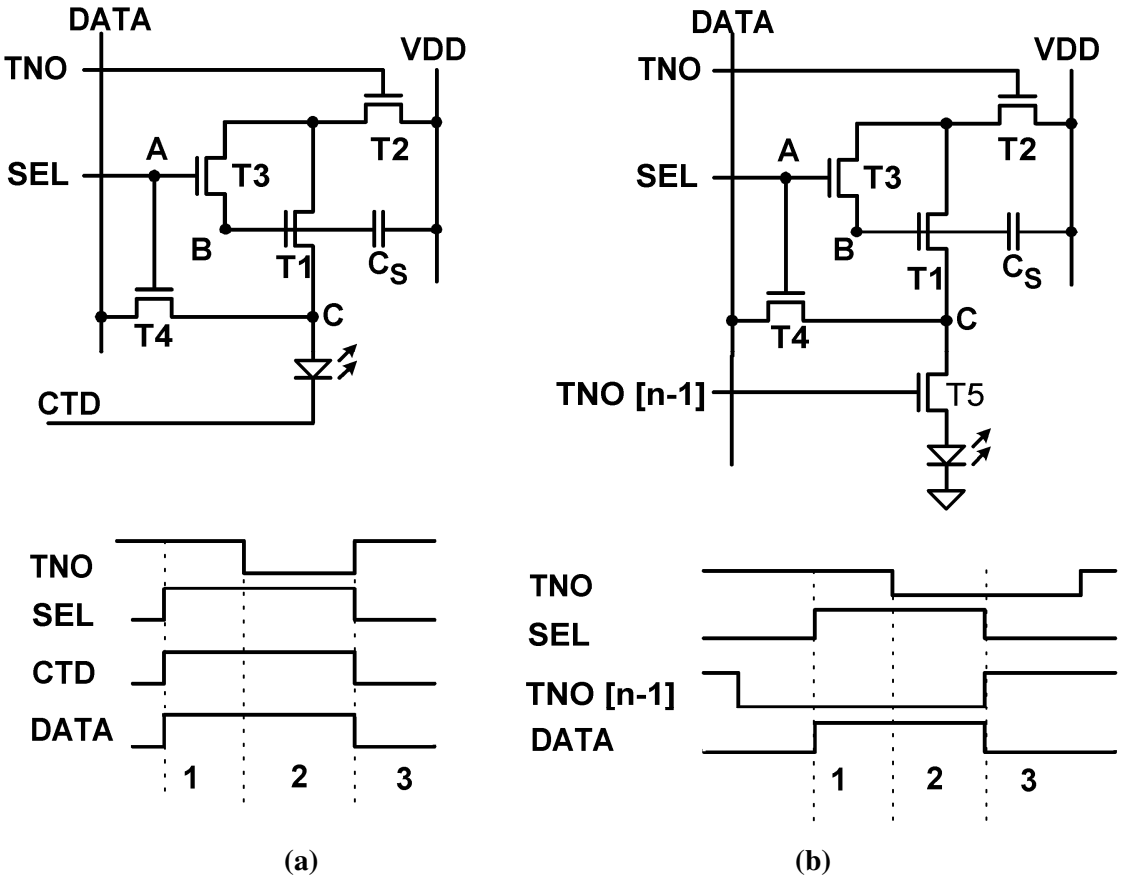


Figure 2.15: Parallel-compensation VPPCs: (a) 4-TFT pixel circuit (adapted from [61]) and (b) 5-TFT pixel circuit (adapted from [62]).

2.2.2.2 Parallel-Compensation Voltage Programming

Figure 2.14 shows simplified circuits for a generic parallel-compensation VPPC by using n-type TFTs during different operating cycles. In the pre-charge cycle, node A is charged to V_{comp}. Here, V_T generation and current regulation occur simultaneously. At the beginning of the V_T-generation/current-regulation cycle, the source voltage of T1 goes to the programming voltage (V_P). During this cycle, node A is discharged until T1 turns OFF, so that the voltage at node A becomes V_P+V_T of T1. During the driving cycle, source voltage of T1 goes to V_{ref}, such that the V_{GS} becomes $V_P+V_T-V_{ref}$.

Figure 2.15 demonstrates two parallel–compensation VPPCs [61, 62]. Here, the compensation and programming occur in the second operating cycle. In the pixel circuit of Figure 2.15 (a), $V_{ref} = V_{DS5}+V_{OLED}$, where V_{DS5} is the drain-source voltage of T5, but V_{ref} is equal to V_{OLED} in the other pixel circuit.

2.2.2.3 Bootstrapping Voltage Programming

Figure 2.16 shows a typical bootstrapped VPPC by using n-type TFTs during different operating cycles [6]. During the V_T-generation cycle, the voltage at node A (V_{comp}) is discharged through the diode connected drive TFT (T1) until T1 turns off. Thus, the voltage stored in C_S is the threshold voltage of T1. Then a programming voltage (V_P) is added to the stored V_T by boot-strapping, resulting in V_{GS} of T1 as V_P+V_T. Therefore, the V_T-shift/V_T-mismatch of the drive TFT does not affect the OLED current.

Two bootstrapped VPPCs are demonstrated in Figure 2.17 [63, 64]. At the end of the programming cycle of the pixel circuit shown in Figure 2.17 (a), the voltage at node C (V_C) is equal to V_P, the voltage at node A (V_A) V_P+V_T, and V_{ref} equal to *VDD* [63]. V_A and V_C of

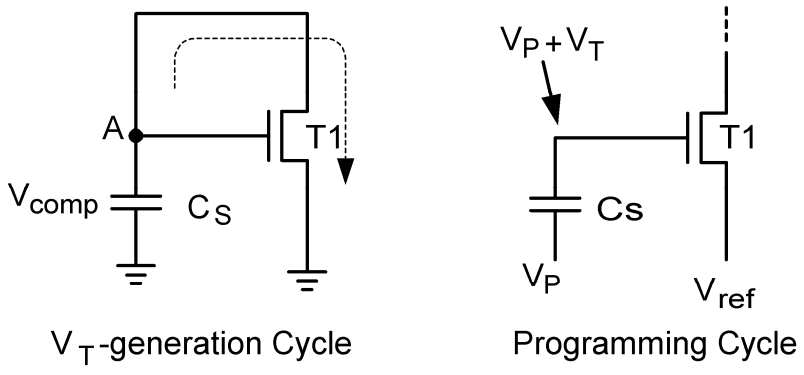


Figure 2.16: Bootstrapped VPPCs during different operating cycles.

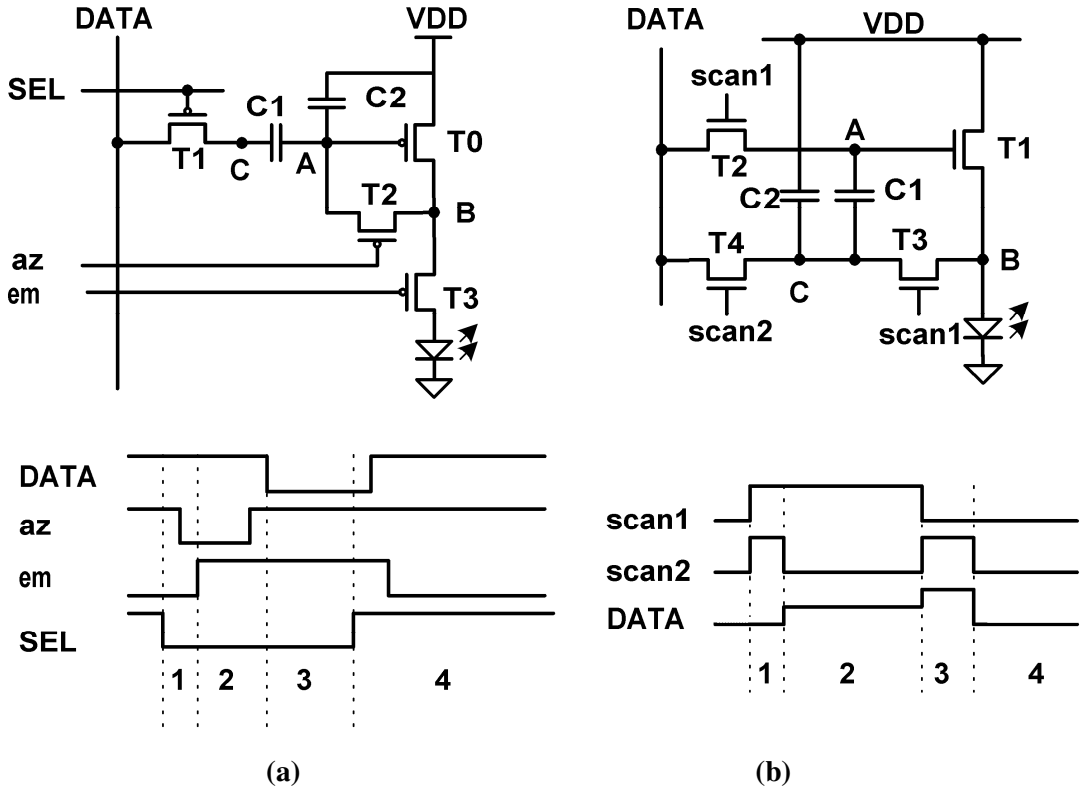


Figure 2.17: Bootstrapped VPPCs; (a) p-channel pixel circuit (adapted from [63]) and (b) n-channel pixel circuit (adapted from [64]).

the pixel shown in Figure 2.17 (b) are the same as those in previous pixel. However, V_{ref} is equal to V_{OLED} in this pixel circuit [64].

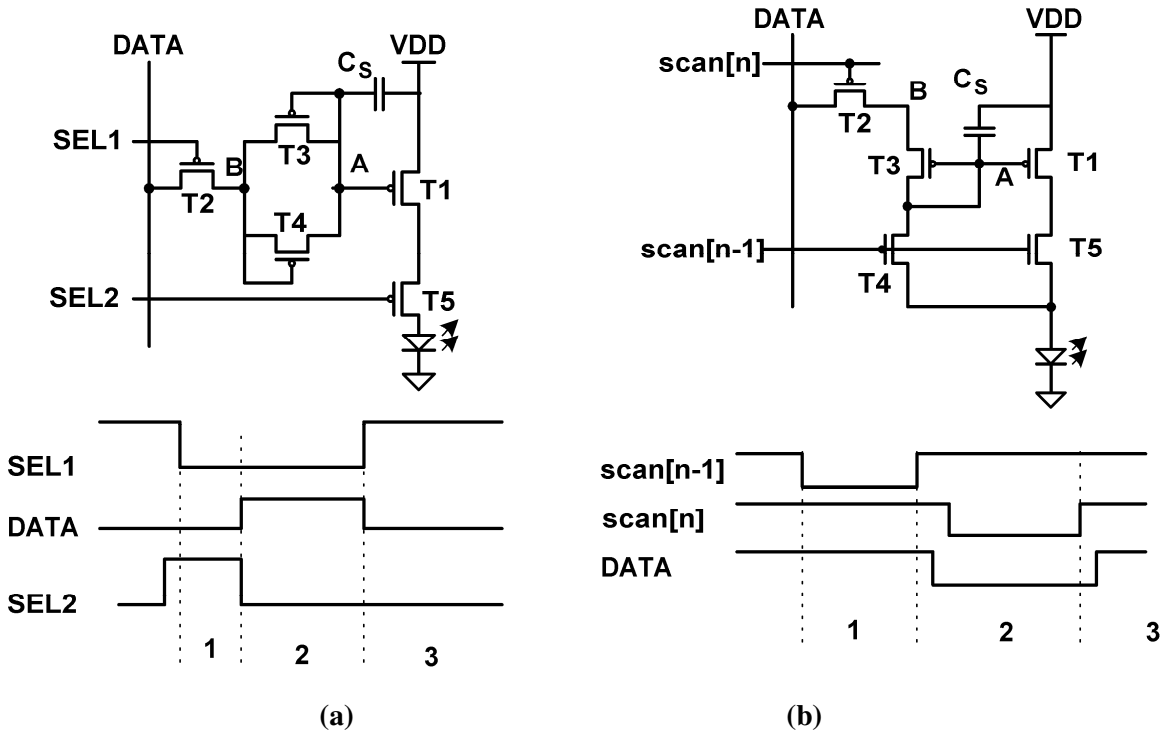


Figure 2.18: Mirror VPPCs; (a) p-channel pixel circuit (adapted from [65]), (b) complementary pixel circuit (adapted from [66]).

2.2.2.4 Mirror Compensation Voltage Programming

This family of pixel circuits is a combination of mirror topology and one of the aforementioned driving schemes. Here, instead of compensating the V_T-shift/V_T-mismatch in the drive TFT, the V_T-shift/V_T-mismatch in the mirror TFT is compensated. In poly-Si technology, the principal assumption for these circuits is that the short range mismatch is negligible. However, in a-Si:H technology, the drive and mirror TFTs must have the same biasing conditions in order to have the same V_T-shift.

Two mirror VPPCs, based on parallel-compensation, are shown in Figure 2.18. In the pixel circuit of Figure 2.18 (a), the pre-charging occurs through T4. The mirror TFT is T3, and so the voltage at node A is V_P-V_{T3} during the drive cycle. If V_{T3} and V_{T1} are identical, this can compensate the V_T-mismatch of T1. The role of T5 is to prevent unwanted emission

during the first operating cycle (pre-charging). In the complimentary pixel circuit, T4 pre-charges the node A, and T3 is used to generate the V_T. Here, complementary technology is required.

2.2.2.5 Spatial Mismatch and Temperature Variation

The drawback of the voltage driving scheme is the high level of sensitivity to spatial mismatch, and environmental parameter variations. Therefore, employing voltage-programmed pixel circuit with poly-Si technology is an area of concern due to a large spatial mismatch. Following (2.3), K is a function device geometry and mobility. Therefore, any change in the geometry due to spatial mismatch directly affects the pixel current. Also, since the TFT mobility is a strong function of temperature, any temperature change results in pixel current variation.

However, the stacked voltage-programmed pixel circuits are less sensitive to mismatch and temperature variation. In the pixel circuit shown in Figure 2.13 (b), since T1 is ON during the third operating cycle, the stored gate-source voltage of T1 reduces. The V_{GS} of T1 can be written as [67]

$$V_{GS} \approx V_P \exp(-\frac{K\tau_{CR}}{C_S + C_{OLED}}) + V_T , \tag{2.4}$$

where τ_{CR} is the timing budget of the current-regulation cycle. This indicates that the stored V_{GS} of *T1* depends on K. Furthermore, a change in K due to spatial mismatch, temperature variation, and mechanical stress changes the stored V_{GS} of T1 in the reverse direction. Although, the current of T1 depends on both V_{GS} and K, this reverse variation makes the pixel less sensitive to mismatch. Figure 2.19 demonstrates the pixel current for the stacked VPPC and conventional 2-TFT driving schemes. The pixel current surpasses close to 300%

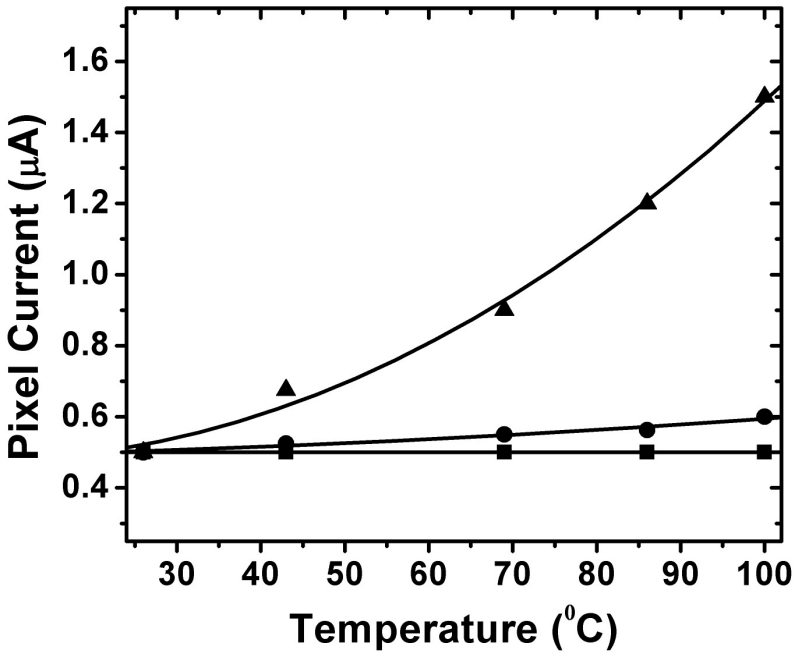


Figure 2.19: Temperature stability measurement results for stacked VPPC (circles for C_{OLED} = 6 pF and squares for C_{OLED} = 8 pF) and conventional (triangles) driving schemes [68].

for the latter after 70 ˚C, whereas the current changes less than 40% for the compensation driving scheme [68].

2.2.2.6 Imperfect Compensation

The principle obstacle in using voltage-programmed pixel circuits in large-area devices is the imperfect compensation during the V_T-generation cycle [57, 58]. Considering that the drive TFT is in the saturation region during the V_T-generation cycle, the overdrive voltage of the drive TFT at the end of the V_T-generation is

$$V_{OV}(\tau_{GC}) = \frac{V_{comp} - V_T}{\frac{K}{C_T}(V_{comp} - V_T)\tau + 1}, \tag{2.5}$$

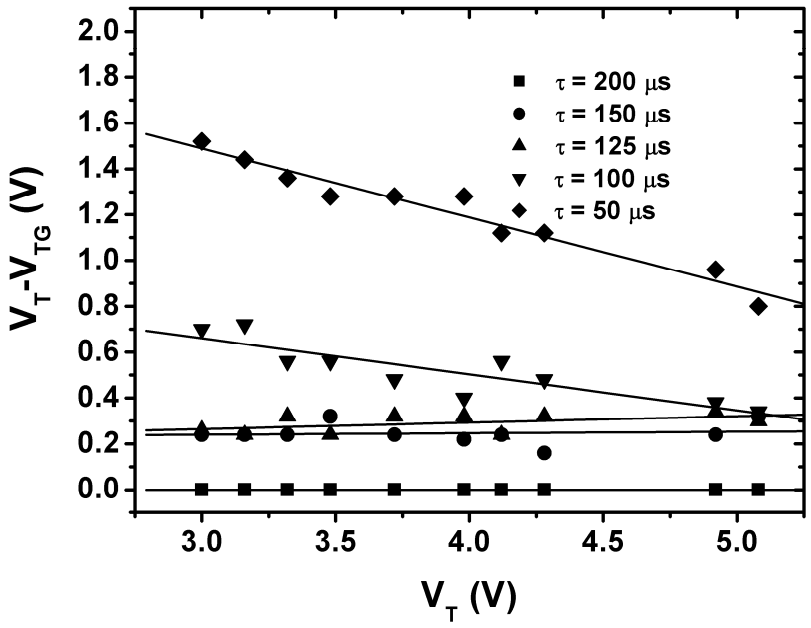


Figure 2.20: Effect of limited timing budget on V_T generation.

where C_T is the total capacitance that is effective during the V_T-generation cycle, and τ the timing budget of the V_T-generation cycle. For perfect compensation, the overdrive voltage should be zero at the end of this cycle. Following (2.5) since τ is limited, the overdrive voltage is not zero, inducing a V_T-dependent error in the pixel current. In the stacked voltage-programmed pixel circuits, C_T is C_S+C_{OLED}, and in other pixel circuits C_T is C_S. Since C_{OLED} is larger than the storage capacitor (C_S), the imperfect compensation can be more severe in the stacked voltage-programmed pixel circuit. Measurement results for the different between threshold voltage (V_T) and generated threshold voltage (V_{TG}) with different timing budgets assigned to the V_T-generation cycle are shown in Figure 2.12. While V_{TG} and V_T are exactly the same for a 200-μs V_T-generation, V_{TG} has a fixed error for medium V_T-generation cycles (τ = 150 μs and 125 μs), becoming more severe for short V_T-generation cycles (τ = < 125 μs). Consequently, the errors in the generated V_T (V_{TG}) for small timing budgets preclude the use

of voltage compensating techniques in AMOLED displays. The experiments are carried out by using a TFT with an aspect ratio 400 µm/ 23 µm.

2.3 Design Considerations for AMOLED Displays

In addition to current and voltage driving schemes, several other driving schemes have been proposed for AMOLED displays including optical feedback [68], electrical (current or voltage) feedback [69, 70], and digital [71] (time based) driving schemes. In optical feedback, a photo diode/TFT is used to monitor the OLED luminance, and adjust the gate voltage of the drive TFT accordingly [68]. Thus, the optical feedback can theoretically compensate for all the undesirable effects such as V_T shift/mismatch, temperature variation, and OLED aging. However, the problem with this driving scheme is the instability of the sensor, high susceptibility to cross talk, and complex pixel circuits. On the other hand, electrical feedback has more stable operation, but comes with the cost of higher cost driver and lower resolution pixel circuit. Also, despite the simplicity of the digital driving schemes [71], they suffer from the contrast ratio due to missing low gray scales. Also, the number of gray scale is limited in this type of driving scheme.

In order to design a suitable driving scheme for different AMOLED displays, one needs to know the major design considerations which can be listed as lifetime, differential aging and mura, power consumption, aperture ratio, IR drop, and implementation cost.

2.3.1 Lifetime and Yield

Display lifetime is when the display luminance is dropped to half of its initial value. This occurs due to OLED luminance degradation and TFT degradation. For simplicity, it is assumed that in a-Si:H AMOLED display, TFT is the only source of aging and the compensation scheme can perfectly manage the effect of aging. However, the compensation

is limited to the given headroom between maximum overdrive voltage and the operating voltage of the driver. To find out the limitation due to the operating voltage, the V_T shift model for constant current is used. The shift in threshold voltage under constant current is given by [47]

$$\Delta V_T = \frac{\left(I_{DS}/K\right)^{\frac{\gamma}{\alpha}}}{\left(1+\frac{1}{\alpha}\right)^{\gamma}}\left(\frac{t}{\tau}\right)^{\beta}, \tag{2.6}$$

where τ, β, γ are process/device dependent parameters [47]. The time required to reach some maximum allowable level can be expressed as

$$t = \tau\left(\frac{\Delta V_{T\max}\left(1+\frac{1}{\alpha}\right)^{\gamma}}{\left(I_{DS}/K\right)^{\frac{\gamma}{\alpha}}}\right)^{\frac{1}{\beta}}. \tag{2.7}$$

For convenience, the current-voltage characteristic of the drive TFT is written, in the following form, by assuming operation is in the saturation regime

$$I_{DS} = K(V_{GS} - V_T)^{\alpha}, \tag{2.8}$$

where $K \propto (W/L)\mu$ where μ is mobility.

$$V_{GS\max} - V_{T\max} = \left(I_{DS}/K\right)^{\frac{1}{\alpha}}, \tag{2.9}$$

where

$$V_{T\max} = V_{T0} + \Delta V_{T\max}. \tag{2.10}$$

Here, V_{T0} is the initial threshold voltage. Failure occurs when V_{GSmax} reaches V_{DD}-V_{OLED} ($\equiv V_{dd}$) then the maximum allowable V_T-shift is then given as

$$\Delta V_{T\max} = V_{dd} - V_{T0} - \left(I_{DS}/K\right)^{\frac{1}{\alpha}}. \tag{2.11}$$

Therefore the lifetime following (2.7) can be estimated as

$$t_{lifetime} = \tau\left(1+\frac{1}{\alpha}\right)^{\frac{\gamma}{\beta}}\left(\left(V_{dd}-V_{T0}\right)\left(\frac{\mu_{FE}C_iW}{2LI_{DS}}\right)^{\frac{\gamma}{\alpha}}-\left(\frac{\mu_{FE}C_iW}{2LI_{DS}}\right)^{\frac{\gamma-1}{\alpha}}\right)^{\frac{1}{\beta}} \quad (2.12)$$

Following (2.12), the maximum allowable V_T-shift for a given V_{dd} increases with the larger size of drive TFT. However, the size of drive TFT is limited by aperture ratio and pixel size. The required lifetime varies in different applications. For a smaller display with less area for large drive TFT, the lifetime is also smaller (~3000 hours). On the other hand, for larger displays, the required lifetime is around 50000 hours. As it is explained in Chapter 5, the size of drive TFT is limited by other factors such as the OLED current density. Thus, achieving such a lifetime without suppressing the aging can be challenging.

Although poly-Si backplane is more stable, the level of mismatch, which can be compensated, is limited to the V_{dd} and maximum required current, resulting in limited yield.

2.3.2 Differential Aging and Mura

Due to different non-idealities such as charge injection (see Chapter 6), the compensation techniques are not perfect. As a result, after compensation, the luminance different across the panel may increase which is called differential aging (for temporal non-uniformity) or mura (for spatial non-uniformity). The amount of acceptable differential aging (or mura) changes, based on applications. For example, the amount of differential aging for mobile application is approximately 2% after aging the display with a white-and-black checker board for 120-hour. On the other hand, it should be less than 0.5% for a display intended for TV application.

2.3.3 Power Consumption

Power consumption in a display consists of two distinct parts: panel and the driver. Also, the power consumption of an AMOLED panel stems for the programming and the driving power consumption. The power consumption, during driving cycle, is mostly due to charging and discharging different parasitic capacitors, particularly in VPPCs. The power consumption, during driving cycle, stems from the current passing through the OLED and drive TFT. Thus for a given OLED, to reduce the power consumption of the panel, the voltage drop across the TFT needs to be reduced which is limited by the size of TFT, required brightness and required lifetime. However, as a rule of thumb, the number of TFTs, within the active path during the driving cycle, should be as low as possible (e.g. one or two) to reduce the power dissipation.

2.3.4 Aperture Ratio

The aperture ratio is the area of the OLED to the total area of the pixel. Since the OLED degradation is a function of the current density [68], for a given brightness (resulting in a required current), the OLED lifetime increases as the aperture ratio increases. To improve the aperture ratio, fewer TFTs in a pixel and an improved layout is required.

2.3.5 IR Drop and Ground Bouncing

Although the current level for each individual pixel is low (around few μA), the total current which passes through the common electrode can be significant due to the high number of pixels in a display. As a result, the effective ground (or VDD) voltage can be different for each pixel resulting in luminance gradient across the panel. This effect is simulated using finite element method for different structures (denoted in Figure 2.21). It is clear that by connecting more sides of the common electrode to the voltage source, the

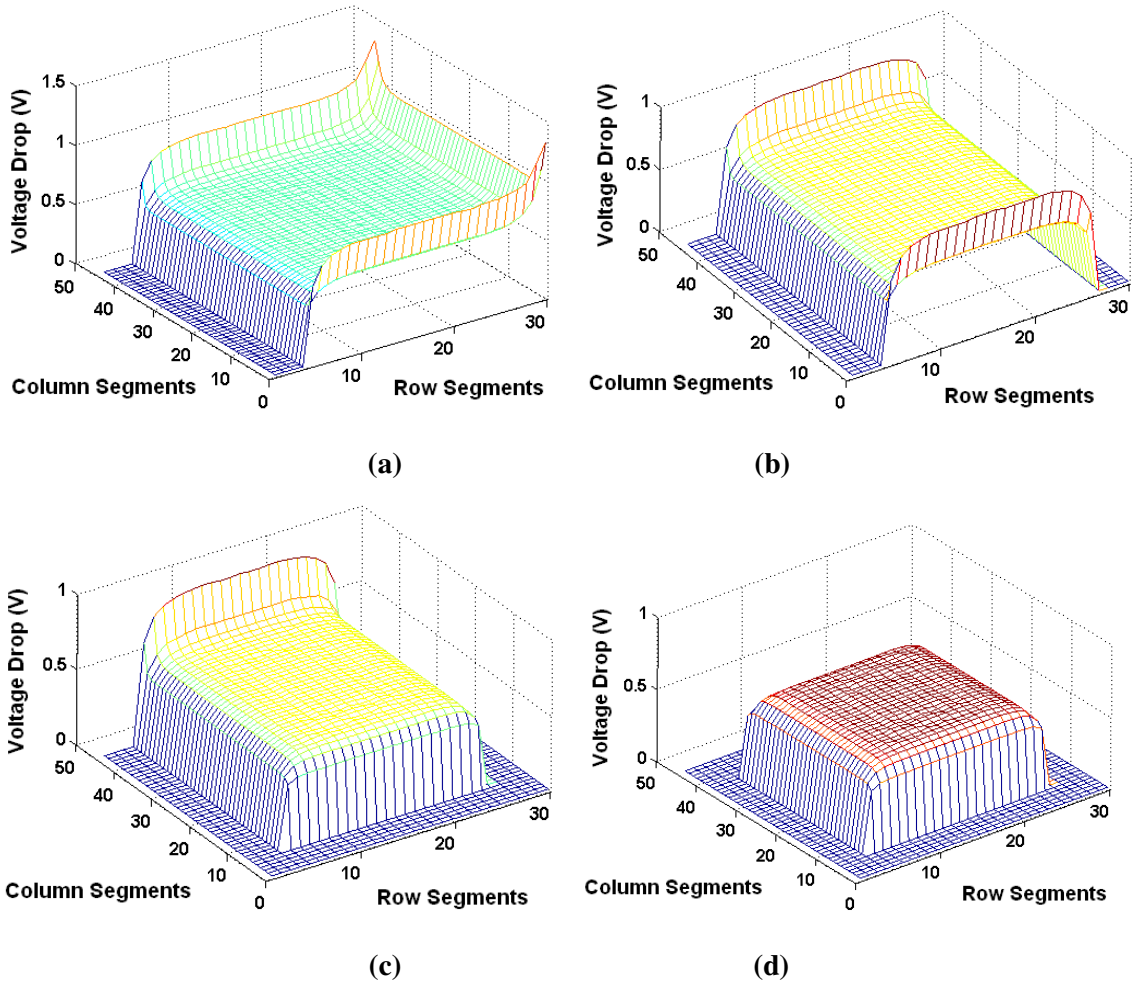


Figure 2.21: Voltage gradient across the common electrode based on different sides connected to the voltage source: (a) one side, (b) two sides, (c) three sides and (d) four sides.

voltage drop can be reduced and the voltage gradient becomes smoother. However, the pixel circuit and driving scheme should be able to tolerate the ground-bouncing and IR drop, since they change as the current density varies with different pictures shown on the display.

2.3.6 Implementation Cost

Another important aspect of the design is the cost, in particular for small area displays for portable applications. In a display structure, the cost is enforced by yield and driver components. To improve the yield, a more stable pixel circuit with fewer TFTs is required. In

addition, the driving scheme should not increase the complexity of the drivers. In particular, the number of controlling or data signals required for each column and row should be reduced. For example, if a driving scheme needs a data line and a monitor line for each column, the number of source driver pads increases dramatically. Considering that the source drive is mostly pad-limited, two lines per column doubles the size of the driver leading to a higher cost.

2.4 Design Considerations for Flat Panel Imager

Most of the discussions in the previous section about lifetime, uniformity, and power consumption can be applied to the imaging application, as well. However, some design considerations are more important for imaging including input dynamic range, input refereed noise, resolution, and cost.

2.4.1 Input Referred Noise and Dynamic Range

The noise model for the 3-TFT APS pixel circuit during different operating cycles is depicted in Figure 2.20. Here, it is assumed that the output of the pixel is virtual ground. The input referred noise (V_{Rn}) during the reset cycle is given by

$$V_{Rn} = V_{n3} = \frac{i_{n3}}{C_T s + 1/R3} \text{ and } C_T = C_s + C_{gs}. \tag{2.13}$$

in which $R3$ and i_{n3} is the channel resistance and noise of T3, respectively. Since T2 and T1 are independent noise sources, the input referred noise associated with the readout cycle is given by

$$V_{Rdn1} = \frac{i_{n1}}{C_T s + g_m} \text{ and } V_{Rdn2} = \frac{i_{n2}}{C_T s + g_m}. \tag{2.14}$$

The total input referred noise can be given as:

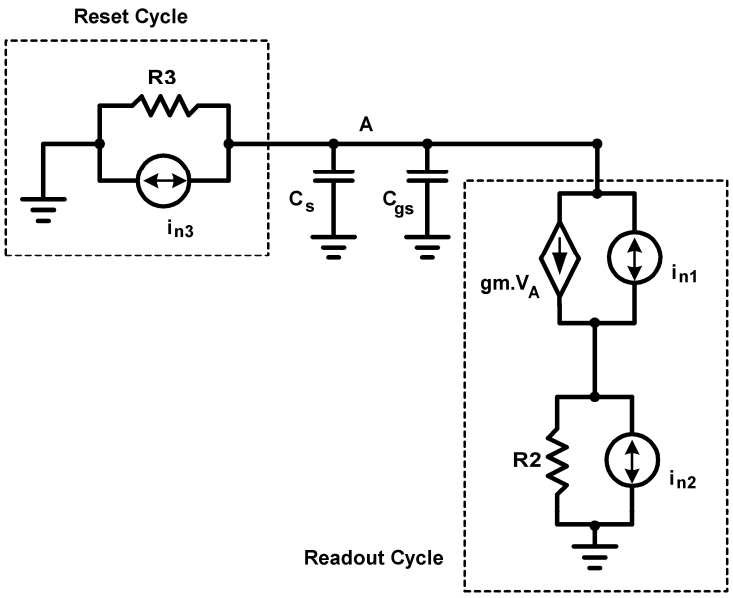


Figure 2.22: Noise model for 3-TFT APS imager pixel circuit [3].

$$|V_{n-in}|^2 = \left(|V_{Rdn1}|^2 + |V_{Rdn1}|^2 + |V_{Rn}|^2\right)^{0.5} = \frac{i_{n1}^2 + i_{n2}^2}{C_T^2\omega^2 + g_m^2} + \frac{i_{n3}^2}{C_T^2\omega^2 + 1/R_3^2}. \tag{2.15}$$

The low end of a dynamic range is defined by the maximum input referred noise of the system.

$$q_{\min} > (q_n + q_s) \text{ and } q_{\min} \propto \frac{I_{\min}}{\eta} \tag{2.16}$$

in which, I_{min} is the minimum input signal intensity, η the conversion efficiency of the sensor, q_s is the noise associated with sensor, q_n the total input referred noise in terms of number of electron. Following (2.16) and (2.17), the sensitivity of the pixel sensor is limited by input referred noise and conversion efficiency of the sensor. On the other hand, the high end of input signal is determined by the dynamic range of readout circuitries.

$$q_{\max} = \frac{V_{HS}}{A_T} \text{ and } q_{maz} \propto \frac{I_{\max}}{\eta}. \tag{2.17}$$

Here, A_T is the total system gain and V_{HS} is the maximum output voltage of the readout circuit. Considering using a charge-pump amplifier as readout circuitry with a capacitance of C_g, A_T can be written as

$$A_T \propto \frac{C_S g_m t_{Rd}}{C_g} \tag{2.18}$$

where g_m is the transconductance of the amplifier TFT in case of active mode. Also, t_{Rd} is the readout time. Thus to increase the high end of the dynamic range one can use a larger C_g or smaller C_S.

2.4.2 Implementation Cost

Due to the need for low volume of biomedical imagers, their cost is very high. A multi-modal platform can improve the overall cost by sharing the device between several applications. However, due to the high contrast between the dynamic ranges of the different applications, the multi-modal platform must be able to handle a wide dynamic range.

2.5 Summery

Spatial and temporal uniformity is the major concern in development of AMOLED displays and flat panel imagers. Although current programming can improve the uniformity and reduce the pixel sensitivity to device variation, it suffers from long settling time. Voltage programming, however, is faster but it is prone to imperfect compensation. To implement stable and uniform devices using the existing technologies, new compensation techniques, improving the uniformity, lifetime, and yield, are required.

Also, the new driving scheme should provide for low power consumption, low implementation cost, high resolution for AMOLED display. In addition to low cost and low

power consumption, the proposed driving schemes should results in improving the dynamic range and lowering the effect of input referred noise.

As result, the design strategy during the course of this research has been based on the fact that stability and uniformity has the highest priority. Moreover, seeking optimized solution for each application instead of a universal solution has been the other principle of the design strategy.

Chapter 3

Hybrid Voltage-Current Programming

As described in Chapter 2, the settling time in current programming depends strongly on the V_T of T1 and initial line voltage (V_0). Figure 3.1 shows the settling time of the pixel circuit depicted in Figure 2.5 (a) as a function of the initial voltage. It is evident that the settling time changes as the initial voltage changes. As a result, since the voltage of the previous pixel remains on the data line, the programming of the new pixel is affected. Pre-charging the data lines to a specific voltage can control the effect of the initial voltage, but this can increase the power consumption considerably. Moreover, initial voltage is a function of the V_T. Thus, the settling time cannot be managed by a fixed pre-charging voltage, because the value of V_T is varying.

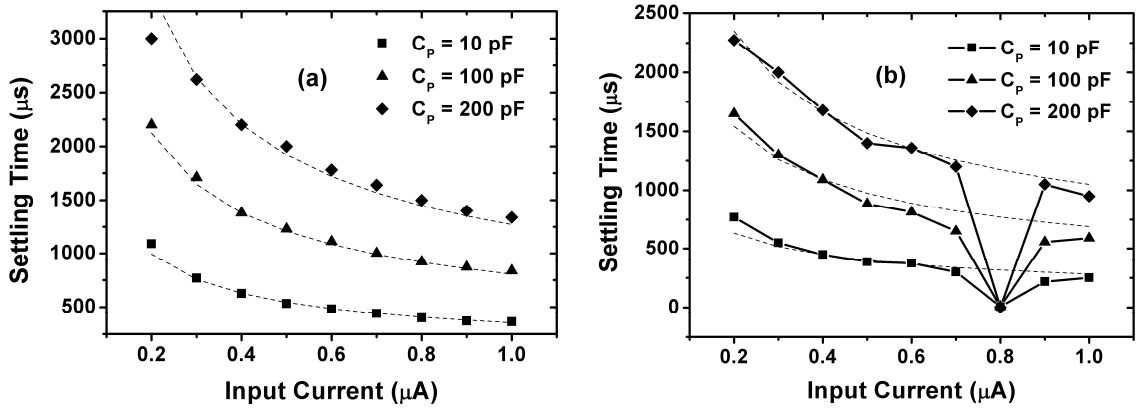


Figure 3.1: Settling time of current programming as a function of initial voltage: (a) $V_0 = 0$ V and (b) $V_0 = 4$ V.

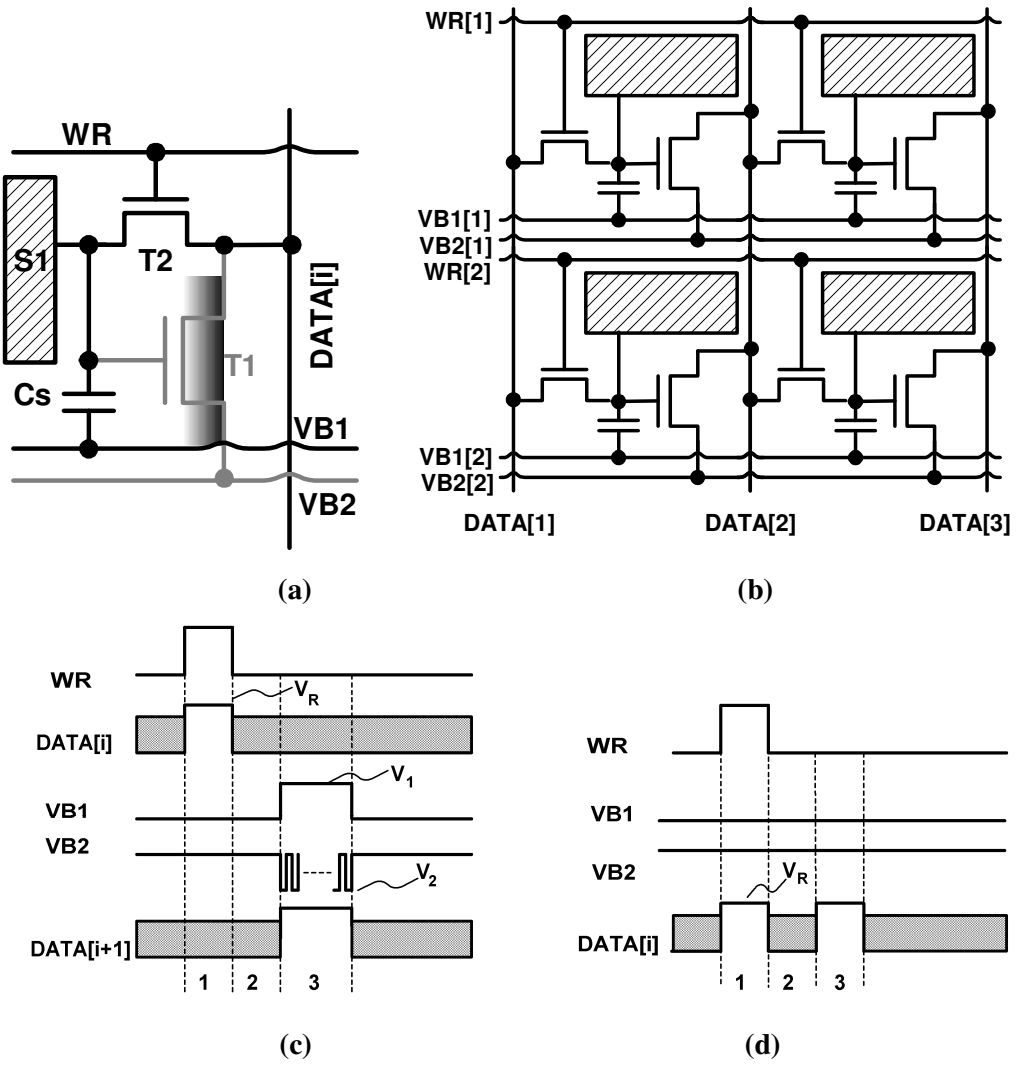


Figure 3.2: 2-TFT hybrid active-passive pixel sensor circuits: (a) 2-TFT hybrid pixel circuit and (b) its corresponding array structure along with (c) signal diagrams for active readout (low intensity sensor signals) and (d) passive readout (high intensity sensor signals) mode signal diagram. The gray components are used only in the active readout mode.

Thus, a dynamic line pre-charging scheme, coupled with a large current, is required to improve the settling time. To develop this driving scheme, a fix current is required to program the pixels so that the initial voltage becomes independent of the pixel content. Also, in-pixel current reduction/division is used to adjust the pixel current accordingly. This driving scheme is called the current-biased voltage-programmed (CBVP) scheme [73, 74].

3.1 Multi-Modal Biomedical Imaging Pixel Circuit

Figure 3.2 (a) demonstrates multi-modal pixel circuits for bio-medical imaging [74]. It operates in active readout mode for low intensity sensor signals such as fluoroscopy in x-ray imaging, and in passive readout mode for high intensity sensor signals such as digital radiography. In these circuits, T1 is the amplifier and T2 is the reset switch transistor. But, T1 also performs the function of a readout switch for the active readout. The corresponding array structure is depicted in Figure 3.2 (b). Figure 3.2 (c) describes the active mode operation of the pixel circuits. Initially, during the reset cycle, the gate voltage of T1 is charged to a reset current (I_R). During the programming, I_R is larger than the required current to accelerate the settling time. Figure 3.3 shows the settling time of the pixel circuit using 4 μA where $V_T[n]$ and $V_T[n-1]$ represent the threshold voltage of the two adjacent pixel circuits in the array. It is clear that the settling time is below 20 μs for a wide range of threshold

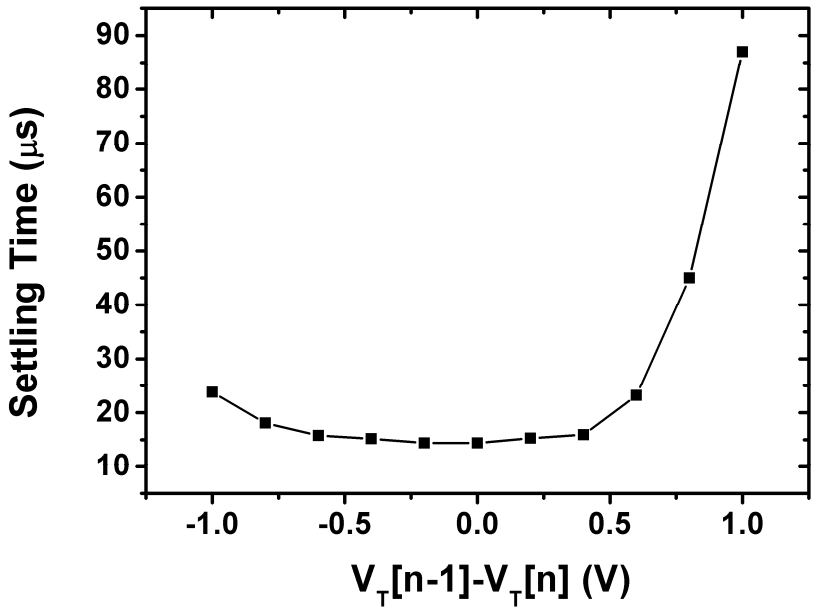


Figure 3.3: Settling time of CBVP pixel circuit.

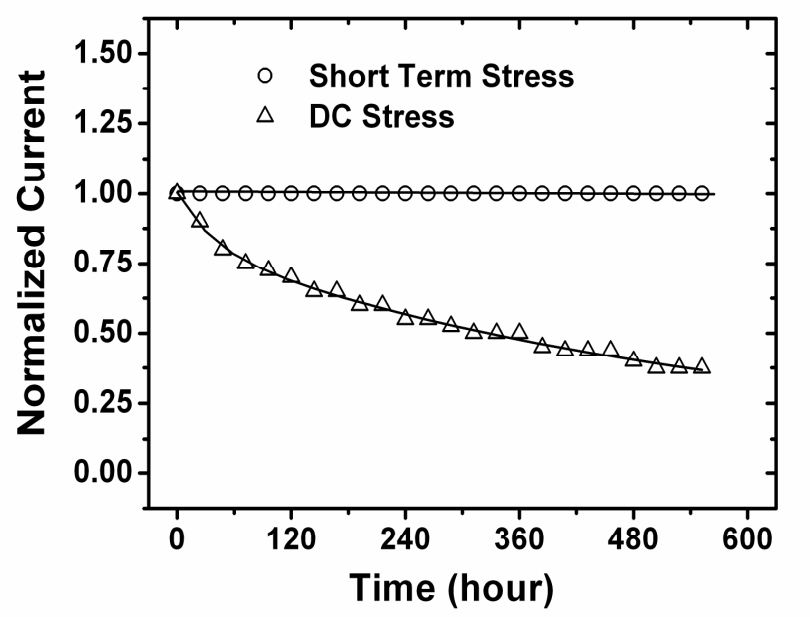


Figure 3.4: Stability of the pixel current (here, voltage programming is used for DC biasing).

voltage variation. This is the case for sensor application since the pixel ages almost identical. Also, since the short-term stress condition introduced in [75, 76] is adopted, the aging of the pixel is limited significantly.

During the integration cycle, where T1 is not under stress (V_{GS} = V_{DS} = 0), the sensor signal is integrated into the storage capacitor and generates a voltage (V_{gen}), which modifies the reset current (I_R) and changes the output current accordingly. The change, associated with the output current, is given by

$$\Delta I = g_m V_{gen},\ g_m = 2\sqrt{KI_R},\ V_{gen} = \frac{Q}{C_S}, \text{ and } Q = \eta\, t_{\text{int}} \tag{3.1}$$

where K is the gain parameter in the I-V characteristics of the TFT [52], Q the charge generated by the sensor, t_{int} integration time, and η the conversion rate which is a function of the conversion efficiency of the sensor, input signal intensity, and sensor area. The current of T1 can be read out through the same data line (DATA[i]) by a trans-resistance or charge

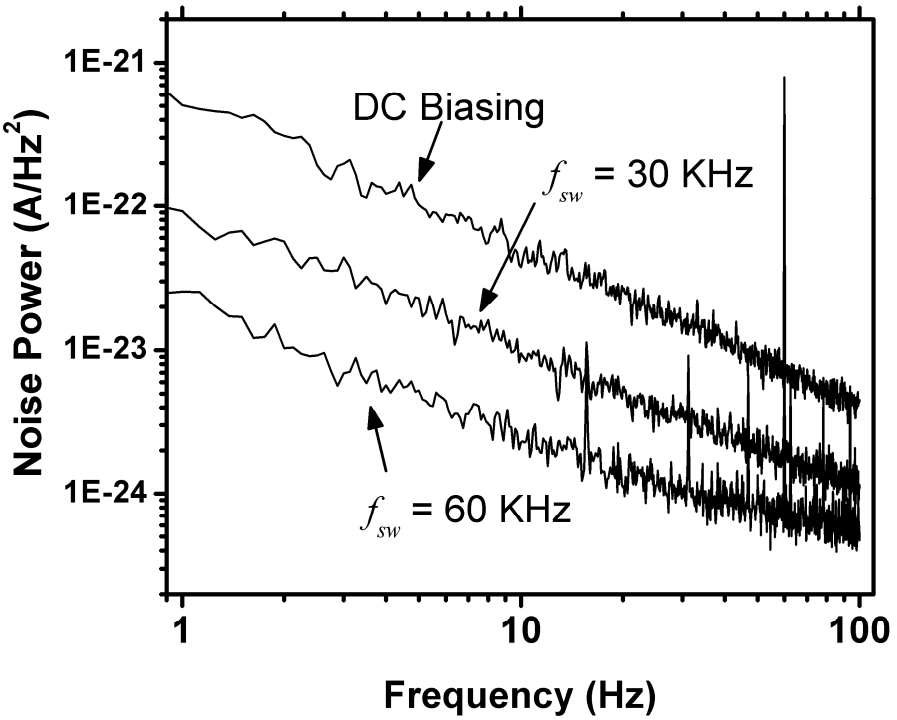


Figure 3.5: Pixel output current noise using different biasing techniques.

amplifier while VB1 and VB2 are at V_1 and V_2 voltages, respectively. These voltages should be chosen in such a way that T1 is turned on during the readout cycle. For example, VB1 can be connected to ground during all the operating cycles ($V_1 = 0$). Also, VB2 has the reset voltage (V_R) during the reset and integration cycles and zero ($V_2 = 0$) during the readout cycle.

Since, T1 is ON only during the readout cycle, minimizing the effect of the leakage current on the operation of the pixel circuits in the same column. More significantly, since T1 is ON for only a fraction of the frame-time, it remains stable for longer of time [76]. Figure 3.4 signifies the pixel current stability for a over 500-hour operation.

During the readout cycle, a periodic pulse is applied to either VB1 or VB2, turning T1 on and off periodically. Since the flicker noise at low frequencies stems from the large time

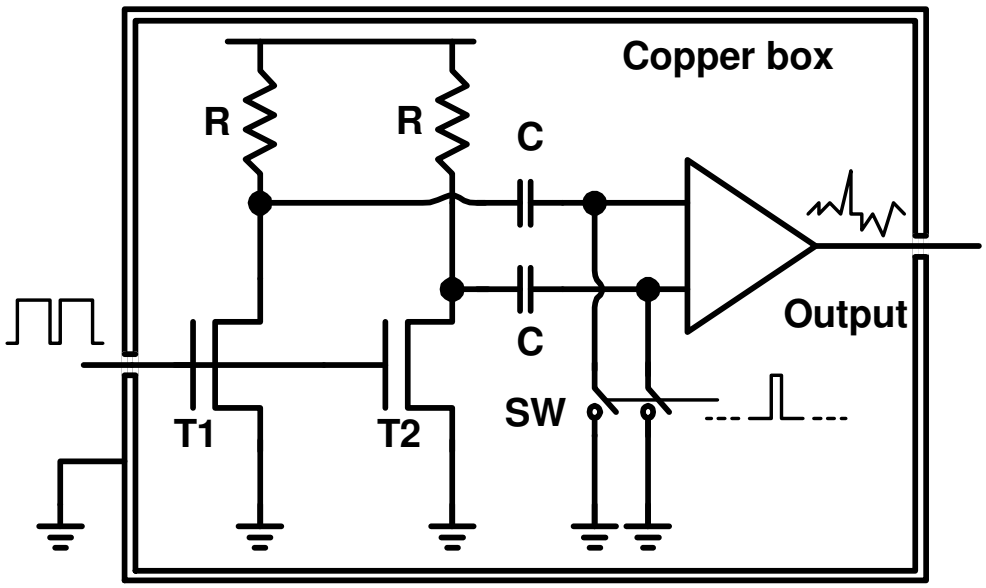


Figure 3.6: Noise measurement setup.

constant trapping-detrapping events, the applied pulse, depending on the pulse width, amplitude, and frequency, serves to reduce the noise at lower frequencies similar to what has been observed in the transistors in CMOS technology [77, 78]. Considering the fact that flicker noise is one of the most important limiting factors of the performance in readout circuits, the switched biasing technique can improve the noise performance of the pixel significantly. The noise performance of the pixel is depicted in Figure 3.5. Although, the noise during a normal readout (30 KHz readout) is smaller than DC biasing, it is larger than the switched biasing technique with two pulses per readout cycle (60 KHz). The setup used for measurement of the flicker noise is shown in Figure 3.14. Here a 8013B HP pulse generator is used for the biasing signal. The entire setup is placed in a double-shielded copper box to reduce external noise coupling, while a differential structure is deployed for further reduction in the input noise associated with a pulse generator. The switches (SW) are used to compensate for the offset caused by any mismatch in the resistors and TFTs. Before measurement, the switches are turned on, such that the offset is stored in the capacitors,

resulting in the balanced inputs at the low-noise amplifier (pre-amplifier 5006 Brookdeal). Since the capacitors are large, the stored voltages for the offset are preserved after the switches are turned off. The output of the low-noise amplifier is fed to a HP 3562A dynamic signal analyzer to extract the power spectral density of the amplified signal. The size of the TFTs used in the measurement is 800 μm/23 μm, and the source and drain terminals are connected to 0 V and 12.5 V, respectively.

The configuration of the pixel circuits in passive readout is exhibited as black in Figure 3.2 (a). In the passive readout mode, VB1 and VB2 remain at levels that turn off T1 (e.g. VB1 = 0 and VB2 = V_R) as depicted in Figure 3.2 (d). Here, the storage capacitor is charged to reset voltage (V_R) during the first operating cycle, and following the integration cycle, the generated voltage is read back through T2.

3.2 Multi-Modal Biomedical Sensor Array

A complete system is developed according to the proposed pixel circuit. Also, sensor is a biomedical sensor in which a sensing pad is surrounded by four reference pads [79]. Figure 3.7 shows the block diagram of the micro-array biosensor, including the sensing area and peripheral circuitry. The readout and biasing circuitries are shared among the columns and pixel circuits provides for a first stage gain and access to the sensing pads. After the pixels are biased with the initial current, the modulated current is read back by the operational trans-resistance amplifier (OTRA).

The pixel circuit used in this array is represented in Figure 3.8 along with the corresponding signal diagram for different modes of detection. The pixel circuit is connected to a sensing pad which is surrounded by reference pads. For the detection modes, associated with faint signals such as amperometric or voltammetry [78, 79], integration overtime is used

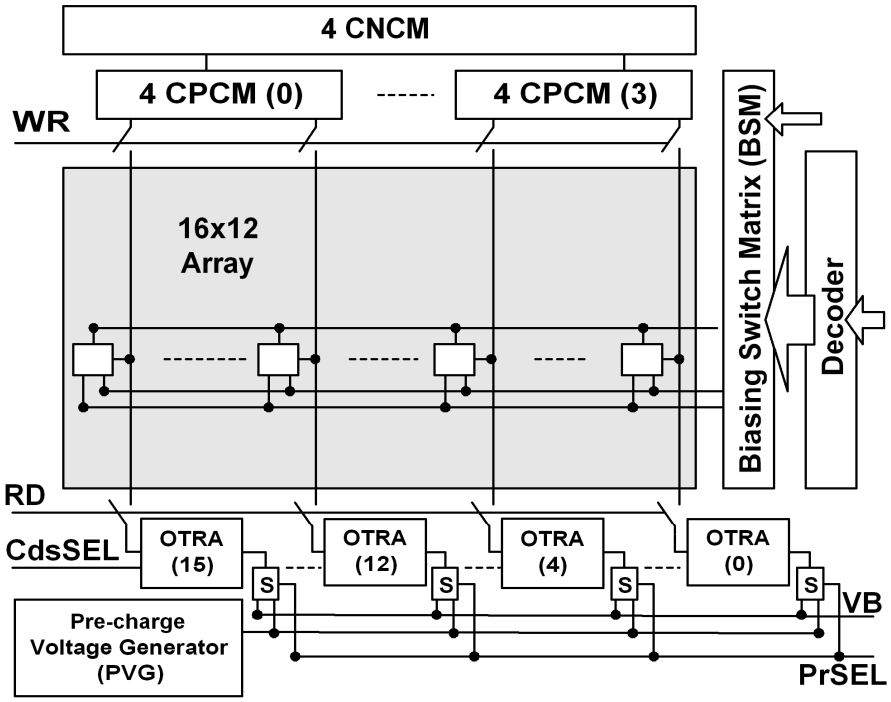


Figure 3.7: Block diagram of the micro-array biosensor.

to amplify the input signal (see Figure 3.8 (b)). The pixel is biased with a constant current during the reset cycle. To accelerate the biasing, the line is pre-charged, and a larger current is employed to bias the circuit. By bootstrapping, the pixel current is dropped to the required level at the end of the reset cycle [74]. During the readout cycle, the current of n1 is read by the corresponding OTRA, connected to the column line. Figure 3.8 (c) signifies the operation of the pixel circuit for detection modes with larger signals such as impedance spectroscopy (IS) [79]. Here, n1 is OFF and the OTRA is directly connected to the sensing pads for reading the current caused by the time-variant voltage applied to the reference pads. The OTRA is reset by a reference current that can be a sensing pad which is not covered by any bio-acceptor material. Thus, the effect of the current caused by electrolyte is subtracted from the final output signals. Although the pixel circuit has been implemented in CMOS for easier

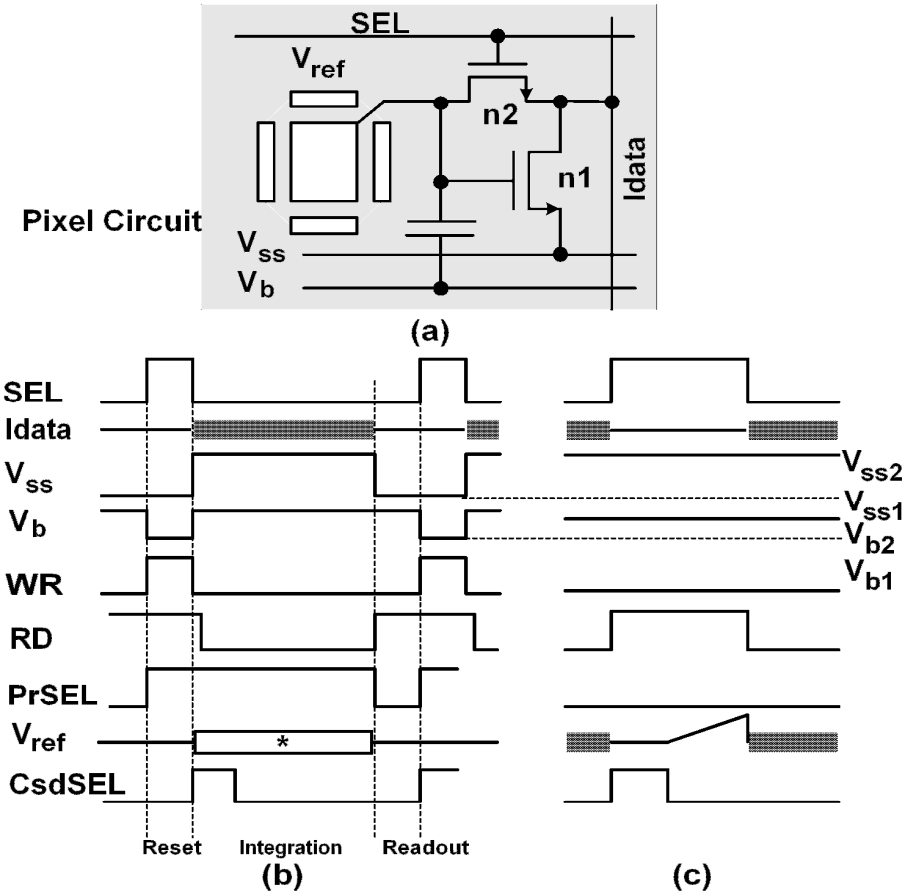


Figure 3.8: Pixel circuit and corresponding signal diagram for different detection modes (* for some detection modes such as voltammetry a time variant voltage should be applied to V_{ref}).

integration, the pixel circuit can be easily replaced with the TFT-based pixel circuit demonstrated in Figure 3.2.

3.2.1 Peripheral Circuitries

The biasing switch matrix (BSM) block, switching the biasing configuration of the pixels, is shown in Figure 3.9. When a row is selected for the reset cycle, $V_{b\text{-}en}$ and $V_{ss\text{-}en}$ are high such that V_b and V_{SS} of the pixels in that row are connected to V_{b1} and V_{ss1}, respectively. Here, the pixels are reset with larger current to accelerate the settling. After the reset cycle terminated over, the V_b of the pixels are switched back to V_{b2}. As a result, the pixels' current

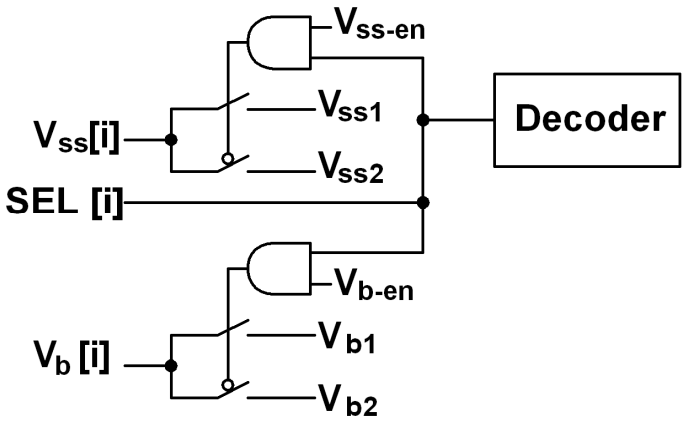


Figure 3.9: Biasing switch matrix (BSM) circuit diagram.

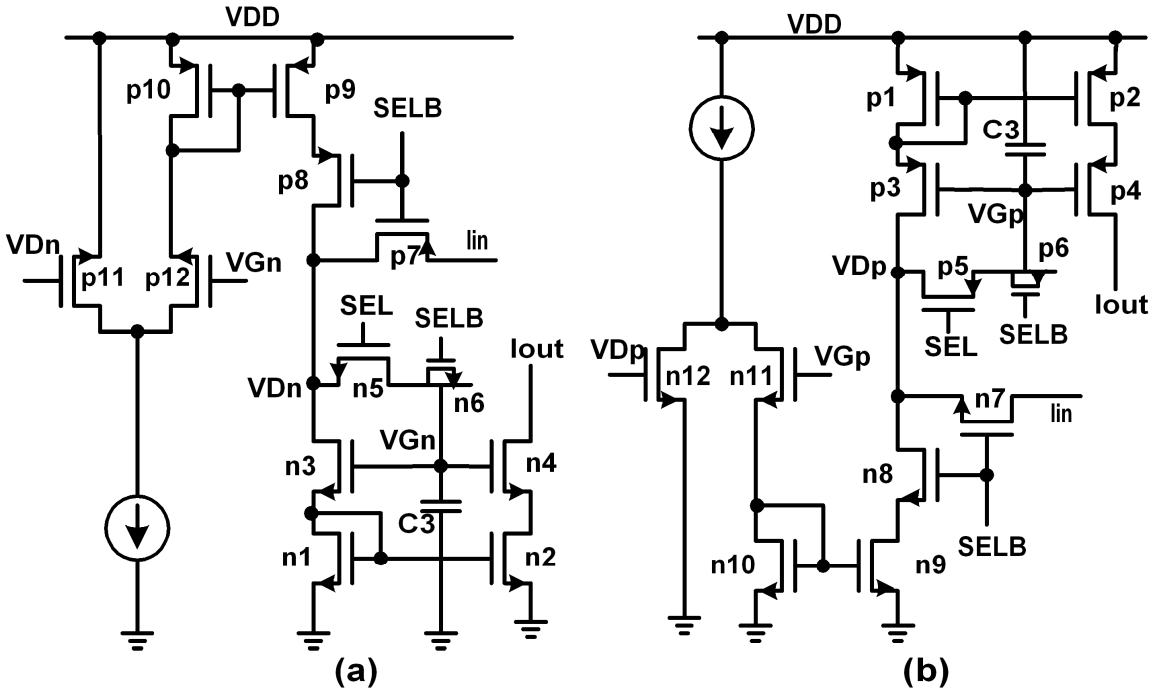


Figure 3.10: (a) NMOS and (b) PMOS calibrated current sources.

is reduced. If a row is selected for the read cycle, the $V_{SS\text{-}en}$ is high so that the V_{SS} of the pixels is connected to V_{SS1}, allowing the modulated current to pass through n1.

To bias the pixel circuits, a two-level calibrated current mirror is adopted. The first level consists of four NMOS current mirrors (CNCMs) which are calibrated, in turn, with a

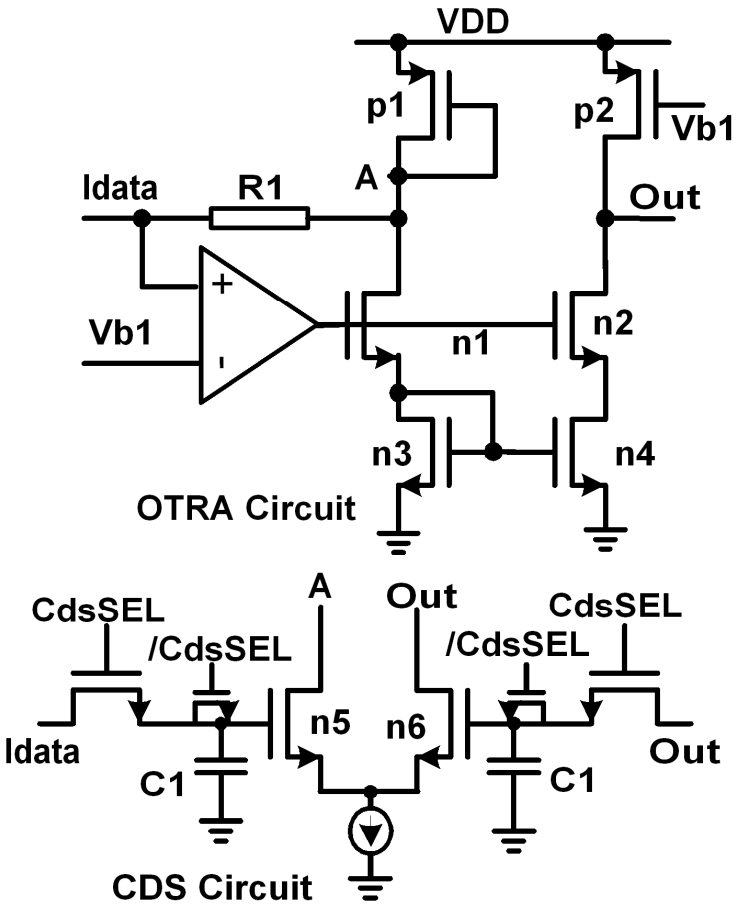


Figure 3.11: OTRA circuit diagram.

single input current as observed in Figure 3.10 (a). To stabilize the output current of the calibrated current sources over time, a feedback loop is used to set the V_{DS} of p7 to zero. As a result, the leakage current of p7 drops significantly preserving the stored voltage in C3 for a longer time. Each of the CNCMs is used to calibrate four PMOS current mirrors (CPCMs) which are connected to a column line through a write switch. As shown in Figure 3.10 (b), the same feedback mechanism is used to reduce the effect of leakage current in CPCMs.

An OTRA is used at each column to read out the modulated current of the pixel circuit and also assisting the current sources with pre-charging the column line during the reset cycle, apparent in Figure 3.11. To improve the offset, mismatch, and noise performance of the

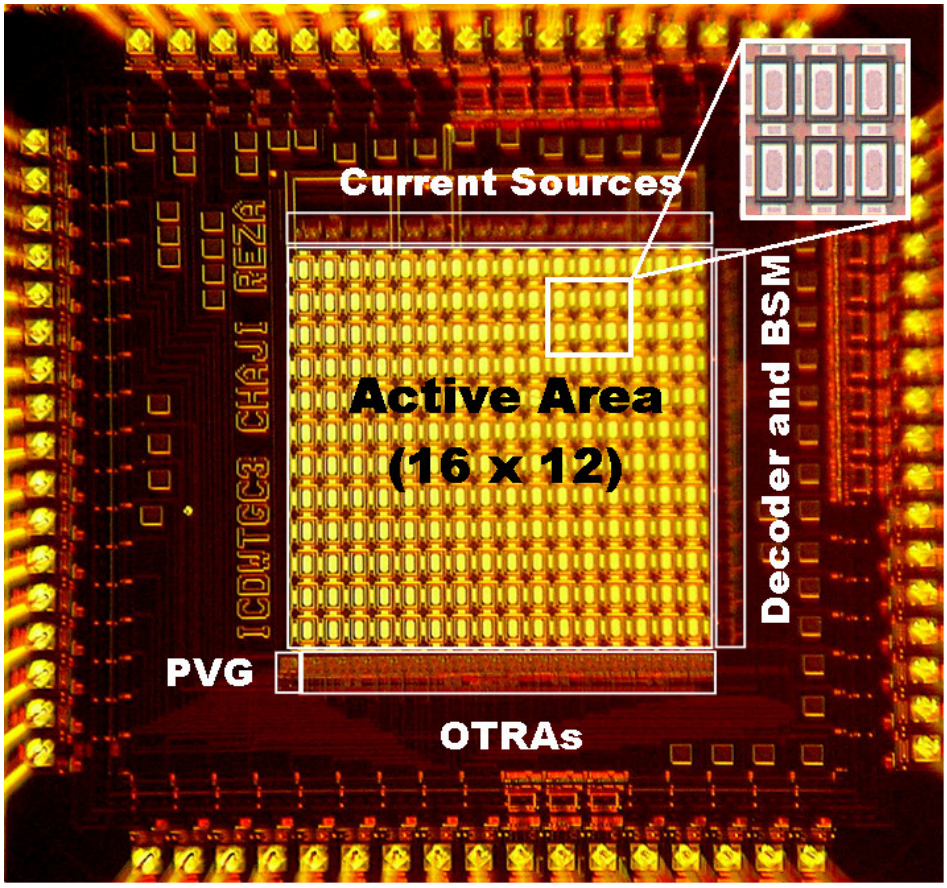


Figure 3.12: Photomicrograph of the micro-sensor and a 3x2 magnified pixel pads surrounded by reference pads.

micro-array, a sample and hold circuit is used for the OTRA biasing (correlated double sampling (CDS) circuit). Before reading out the pixel signal, the CDS circuit samples a reference current which is the reset current of the pixel. As a result, the leakage current of the pixels, connected to a column line (Idata); mismatch current of CPCM and/or pixel circuits; offset of the OTRA; and *1/f* noise of the circuits are sampled and deducted from the final readout signal. Moreover, if the select line of the pixel circuit goes to zero before the CDS circuit finishes the sampling; the charge injection effect associated with the switching is also compensated (see Chapter 6 for more details).

3.2.2 Measurement Results

Figure 3.12 is the photomicrograph of the fabricated chip in 0.35-μm TSMC CMOS technology. The electrical performance of the array is listed in Table 3.1. Because several test pads are used for verifications; the size of the chip is larger than the actual size of the array.

Table 3.1: Electrical performance of the fabricated chip

chip	**Values**
Technology	0.35 μm (4 metal) at 3.3 V
Power consumption	15 mW
Die Size	3.8 mm x 3.8 mm (it is pad limited due to the use of several test pads)
External components	OTRA resistor (R1)
Array	Values
Size	16x12
Area	1.71 mm x 1.65 mm
Pixel pitch	140 μm x 100 μm (size depends on the sensor technology)
Operation mode	Impedance spectroscopy, amperometric, cyclic voltammetry,
Power Consumption	0.4 mW
Peripheral Circuitry	Values
OTRA	Power (0.7 mW), area (102 μm x 107 μm), gain (0.2 MΩ), output mismatch (< 24 mV), 3db bandwidth (7.5 MHz), and output dynamic range (2 V)
Calibrated Current Sources	Power (1.5 mW for 16 CPCMs 4 CNCMs) and area (58 μm x 54 μm), mismatch (21 nA at 4.5 μA)

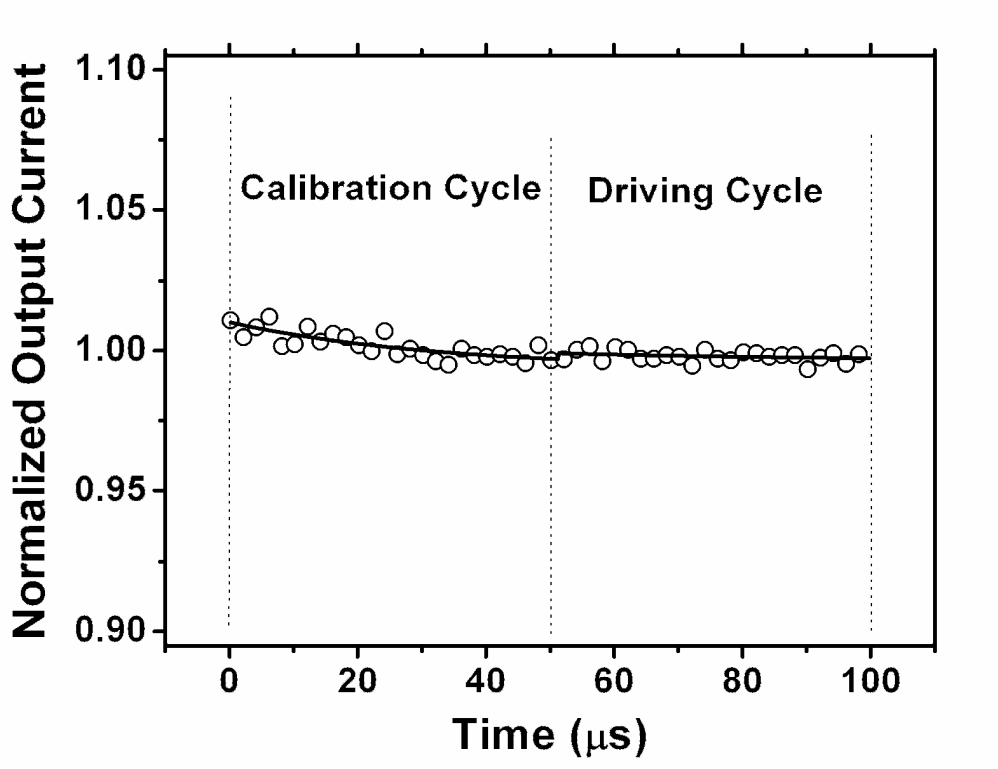


Figure 3.13: Current stability measurement for the calibrated current sources.

Since the readout circuits, used here are simple and shared among the columns, the total power consumption is substantially reduced which allows the up-scaling of the array for higher throughput without the risk of increasing the surface temperature. Also, the power consumption, associated with the sensing area, is very low (0.4 mW), since only one row is activated at a time. Also, the mismatch in the output of the OTRAs is exceptionally low (< 24 mV) due to the use of CDS circuit.

Figure 3.13 highlights the stability of the calibrated current sources over time. During the calibration cycle, the current settles to its final value. After n7 turns off, the source driver contains its current for the driving cycle. The drop in the pixel current, due to the leakage, is less than 0.3 %. Also, since a dummy transistor and large storage capacitor (C3 = 350 fF) is

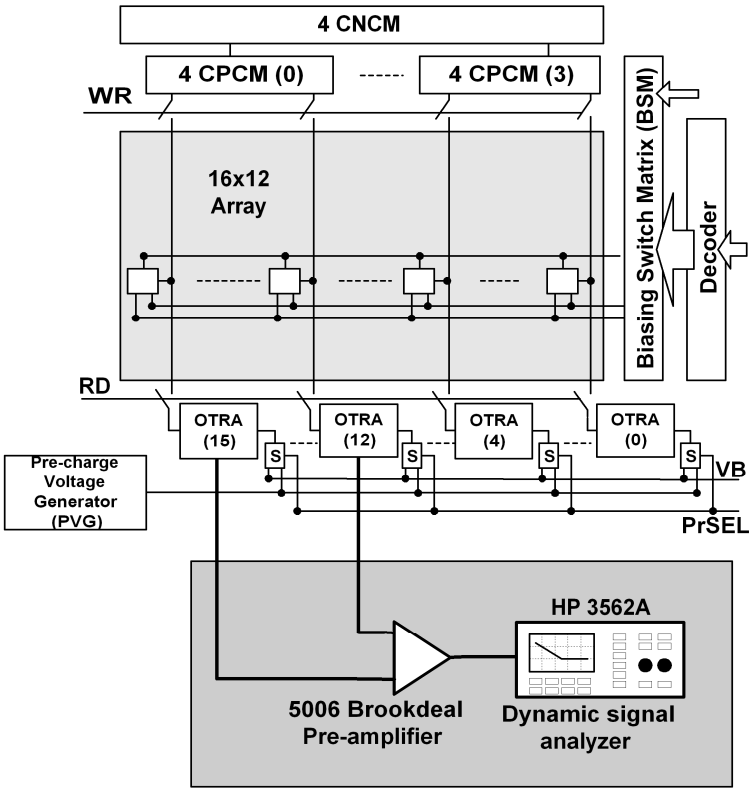


Figure 3.14: Noise measurement setup used for the biomedical sensor array.

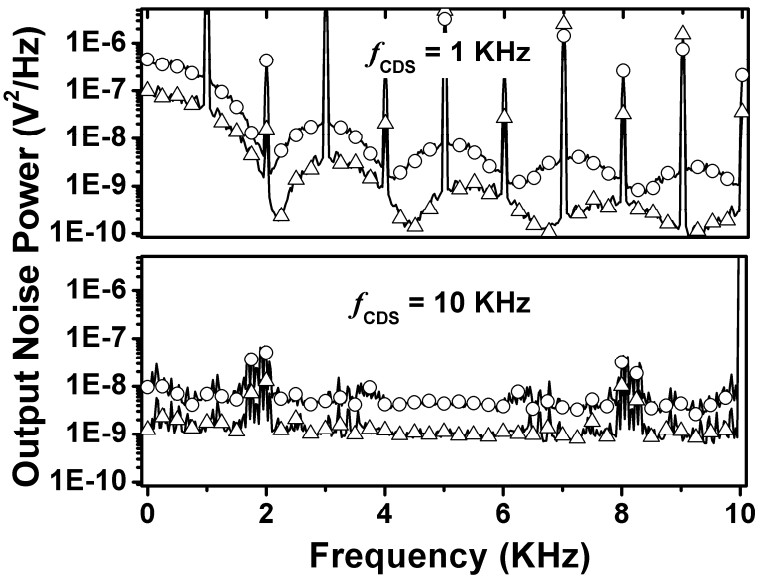


Figure 3.15: Measured noise performance of the micro-array with different noise reduction techniques (circles indicate the DC bias of the pixel circuit and triangles show the switching bias technique of the pixel circuit).

used to compensate for the charge injection effect of n5 (Figure 3.10 (a)), the change in the output current is negligible.

Since the signal in the amplification mode is DC, having a low noise power at the vicinity of DC is crucial. Thus, both the CDS and switching bias (SB) techniques are utilized in this micro-array for *1/f* noise reduction. To implement the SB technique, a pulse is applied to the source of n1 during the readout cycle. The noise measurement setup is depicted in Figure 3.14 in which a differential amplifier is used to reduce the correlated noises induced by crosstalk (such as 60 Hz). Figure 3.15 emphasizes the noise performance of the circuit using both the SB and CDS techniques. Due to the existence of a small mismatch (<24 mV) among the OTRAs, some pulses appear at the harmonics of the CDS frequency. The higher the CDS frequency is, the lower the *1/f* noise is. However, this would reduce the integration time thus limiting the frequency of the CDS. The noise power at the vicinity of the DC is reduced to -83 dB by means of the CDS and SB.

The impedance characteristics of the sensing pads changes in the presence of an analyte [79]. Such changes can be measured by applying a sinusoidal signal to the reference pads and tracing the change in the current between the reference and sensor pads. Measurement results for the two different concentrations of bovine serum albumin (BSA) are depicted in Figure 3.16. The result indicates that the impedance consists of a significant capacitance, which changes with the concentration of the BSA. However, the pixel circuit and data line forms a low pass filter which reduces the input signal as the stimulus frequency increases, which in turn, saturates the output of the OTRA at high stimulus frequencies. According to Figure 3.16, the chosen frequency must be less than 60 KHz.

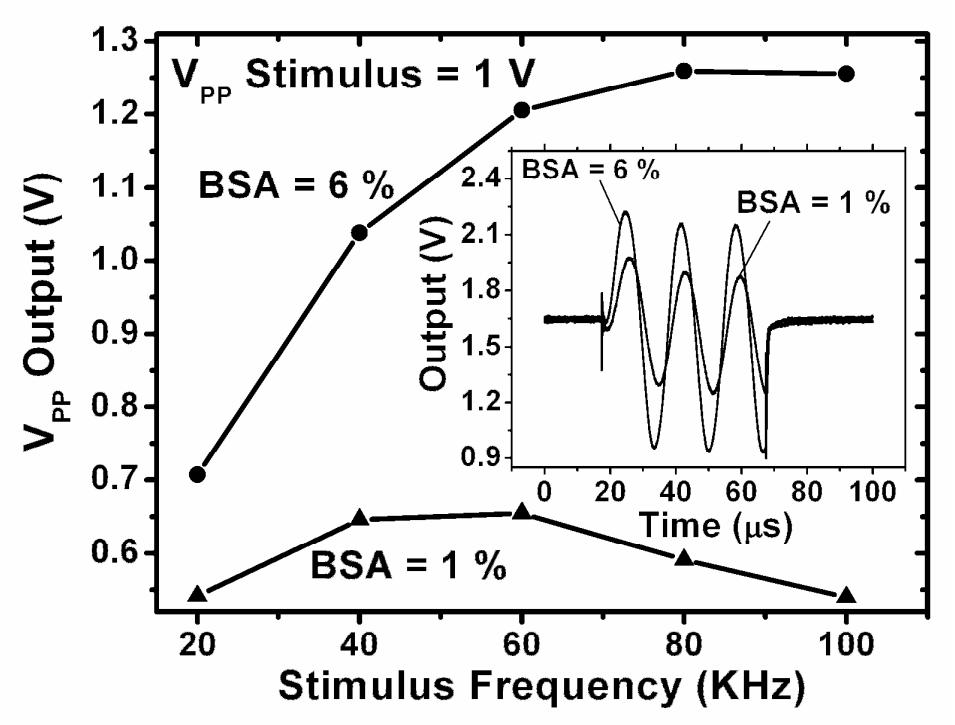


Figure 3.16: Measurement results for impedance spectroscopy.

For a low intensity of BSA, however, the pixel is configured in the active readout mode signified in Figure 3.17. A ramp voltage is applied to the reference pads, and the current is integrated in C_S. Here, the pixel remains connected to the OTRA to display the transient of the active readout measurement. As described, the CDS circuit can reduce the leakage and charge injection effects of the pixels. During the reset cycle of the gray curve, the select of the pixel circuit is turned off before the CDS circuit finishes the sampling. As a result, the output voltage of the OTRA settles back to its original voltage (see Figure 3.17). However, for the black curves, the select lines of the pixel and CDS circuits are turned off at the same time. Thus, the OTRA output jumps up at the beginning of the integration cycle (the SB technique is turned off in this measurement for more clarity).

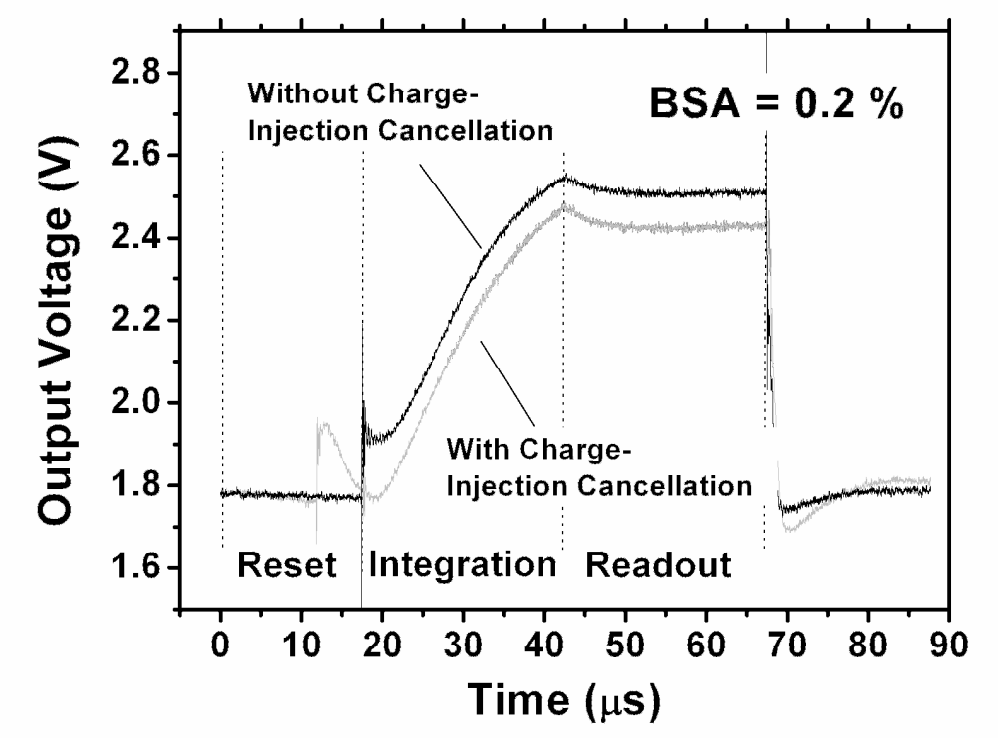


Figure 3.17: Measurement results for the effect of charge injection on the output of OTRA.

3.2.3 Improved Dynamic Rage

As explained in (1.1), the generated voltage is a reverse function of the storage capacitor. Consequently, it is desirable for the low intensity signal to have a small storage capacitor to improve the signal-to-noise ratio (SNR) [81]. On the other hand, for a high intensity signal, the capacitor should be large to avoid saturating the readout circuitry.

Since the pixel, depicted in Figure 3.2, provides access to the capacitor, a metal-insulator-semiconductor (MIS) structure is employed to change the capacitor value for the different measurement modes. The capacitance-voltage (CV) characteristics of a MIS structure are demonstrated in Figure 3.18. As highlighted, the MIS capacitor can accommodate the need for variable capacitor in a multi-modal imaging/sensor structure. Moreover, the MIS capacitor can provide for gain-boosting for detecting extremely low

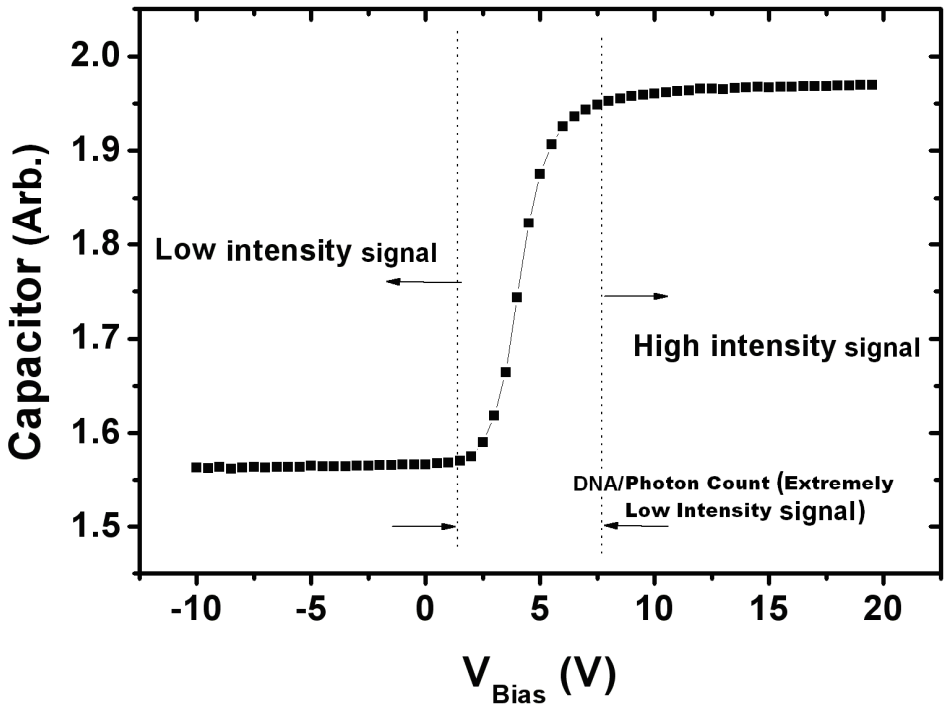


Figure 3.18: Measured CV characteristics of an a-Si:H MIS structure.

intensity signals. Figure 3.19 (b) represents the simulation results for the gain of the proposed pixel circuit with and without MIS capacitor gain. To employ the MIS gain, the V_T of the MIS should be extracted carefully, to bias the MIS capacitor in an adequate point. Chapter 6 describes a method for extracting the V_T of drive/amplifier TFT. The same technique can be used to detect the edge of the MIS capacitor.

3.2.4 Noise Analysis of CBVP Pixel Circuit

Figure 3.20 shows the small circuit model used to analyze the input referred noise caused by the pixel components. During the reset cycle, node B is assumed to be float since it is connected to a current source. The reset noise associated with T1 and T2 is calculated as

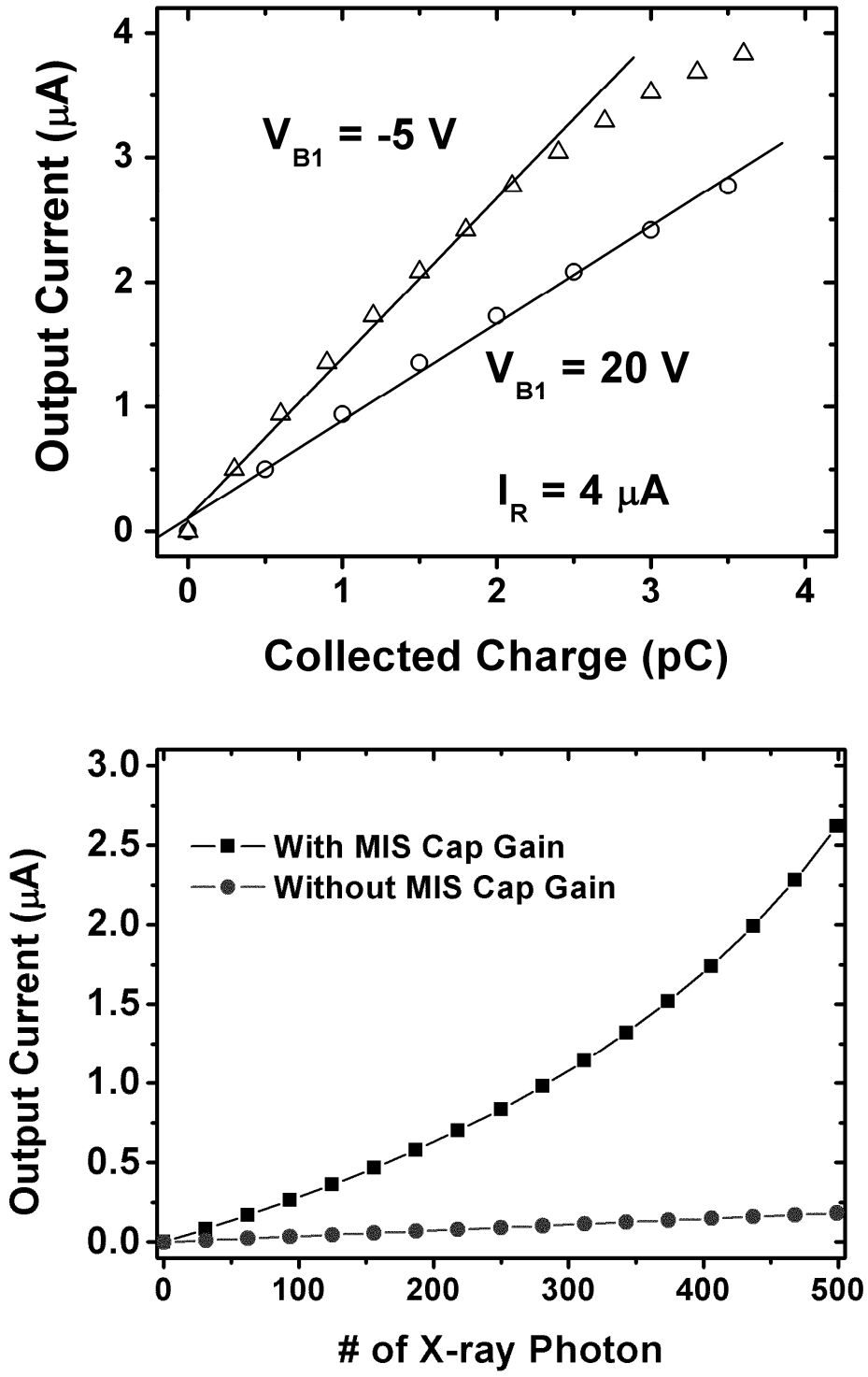


Figure 3.19: (a) Active mode gain adjusting with MIS capacitor and (b) pixel sensitivity with and without MIS capacitor gain.

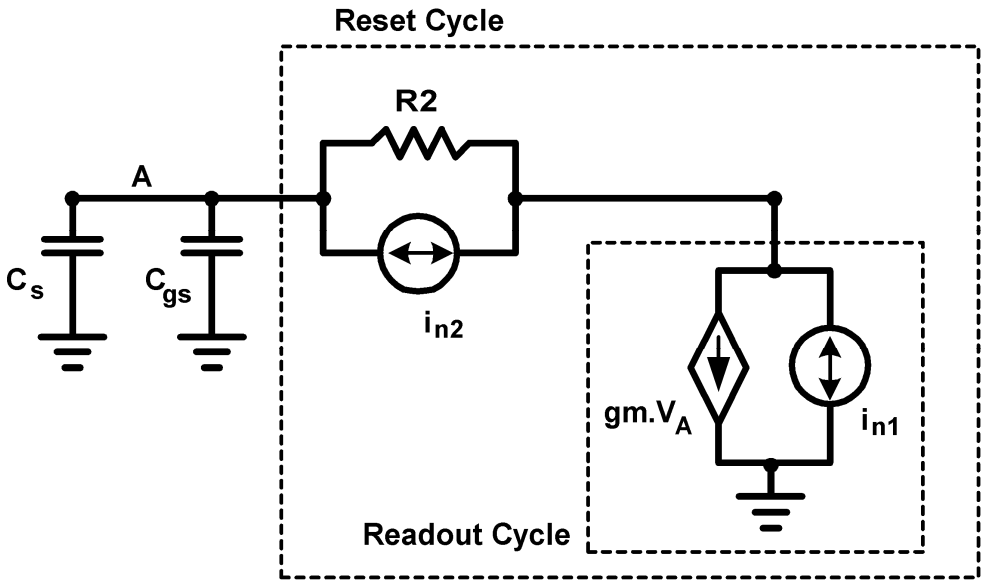


Figure 3.20: Noise model of CBVP imager pixel circuit during different operating cycles.

$$V_{Rn1} = \frac{i_{n1}}{(C_T s + g_m)} \quad \text{and} \quad V_{Rn2} = \frac{R_2}{r_d} \frac{i_{n2}}{\left((1 + \frac{R_2}{r_d}) C_T s + (g_m + \frac{1}{r_d}) \right)} \tag{3.2}$$

where, r_d is the drain-source resistance of T1, and R_2 the switch resistance of T2. Assuming that $r_d/R_2 << 1$, the effect of T2 is attenuated significantly.

During the readout cycle, we assume that node B is connected to a resistive load. Also, the effect of C_{gd} of T1 becomes important during the readout cycle. The input referred noise during the readout cycle can be calculated as

$$V_{Rdn1} = \frac{i_{n1}}{\left(\frac{C_T + C_{gd}}{R_L C_{gd}} + g_m + C_T s \right)}. \tag{3.3}$$

Here, the R_L is the output load. Considering that the input referred noise of 3-TFT APS (see Section 2), (3.2), and (3.3), it can be concluded that the input referred noise of CBVP

pixel circuit can be smaller than that of 3-TFT APS, since there is no switch TFT in series with T1. Also, using the switch biasing technique the noise of CBVP pixel circuit is reduced more significantly.

3.3 CBVP AMOLED Pixel Circuit

For a technology, such as poly-Si, in which mobility experiences variations as well as threshold voltage mismatches [32], a current programming is prerequisite for high yield. Since the CBVP benefits from advantages of both current and voltage programming, the CBVP pixel circuit is a suitable candidate for the above mentioned technology.

Figure 3.21 offers the proposed CBVP pixel circuits [82], providing for large-area high-resolution AMOLED displays. Here a fixed large bias current (I_{bias}) is used to compensate for the aging and mismatches. Since the current levels required by OLED are around 1 μA, the bias current is divided inside the pixel by a bootstrapping technique. During the biasing cycle, SEL[n] which is the address line of the n^{th} row is high and the voltage at node A adjusts to $V_{bias}+V_T$ where $V_{bias}=(I_{bias}/K)^{0.5}$. The OLED needs to be OFF during the biasing cycle, and so $V_{DD}-V_{bias}-V_T$ should be smaller than the ON voltage of the OLED. Since For the pixel circuit in Figure 3.21 (a), node B is charged to $V_{bias}-V_P$ where V_P is related to the pixel luminance, and so the programming and biasing occur in parallel. However, for the circuit in Figure 3.21 (b), node B is charged to zero during the biasing cycle, thus the biasing is independent of V_P. During the programming cycle, SEL[n] is low and SEL[n+1] which is the address line of the $n+1^{th}$ row is high. Thus, node B is charged to zero or V_P-V_{bias} for the pixel circuits in Figure 3.21 (a) and (b), respectively, changing the voltage at node A to V_P+V_T. During the driving cycle, the current of T1 which is controlled by its gate voltage drives the OLED independent of the V_T of T1. While both pixel circuits operate essentially

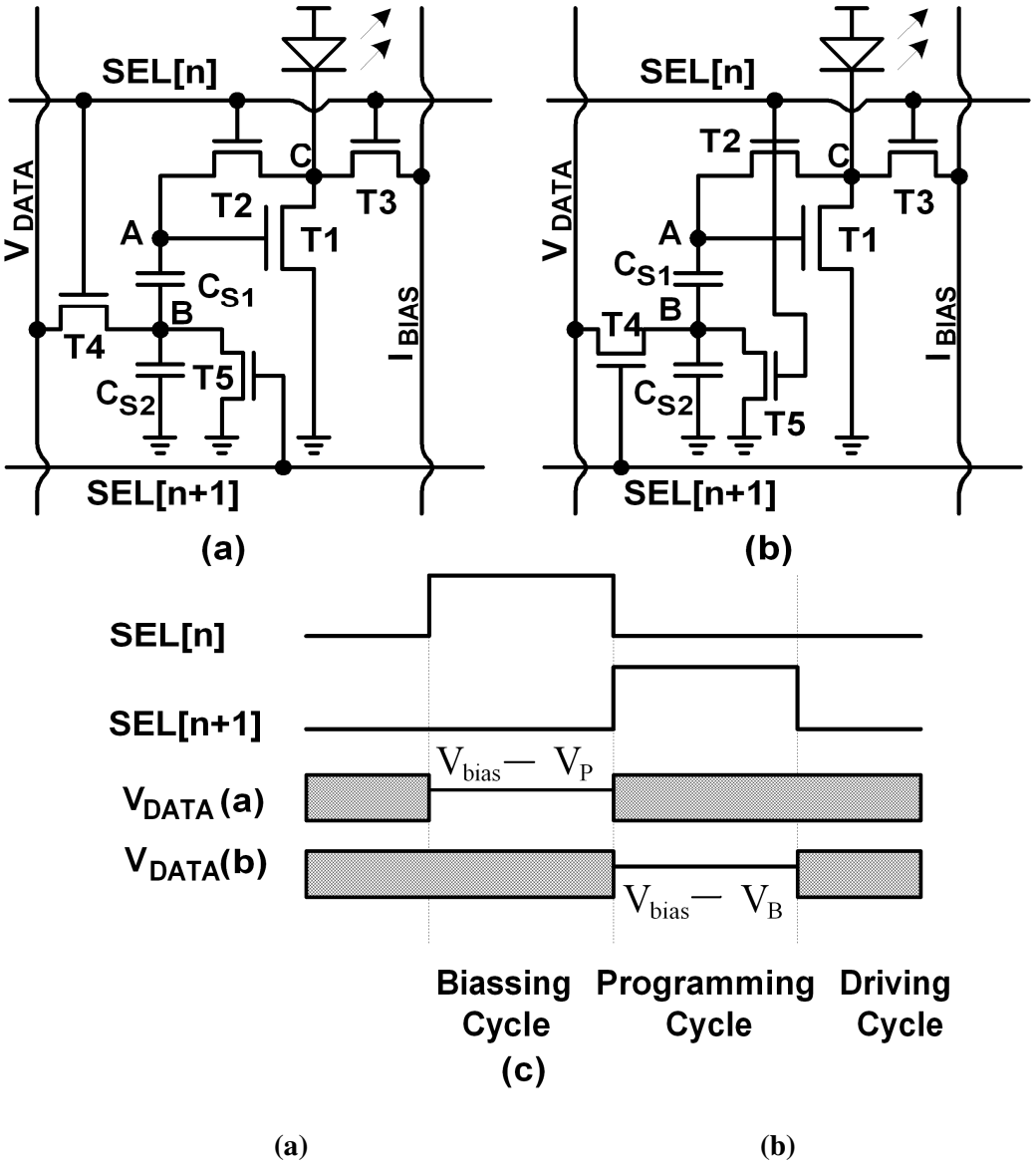
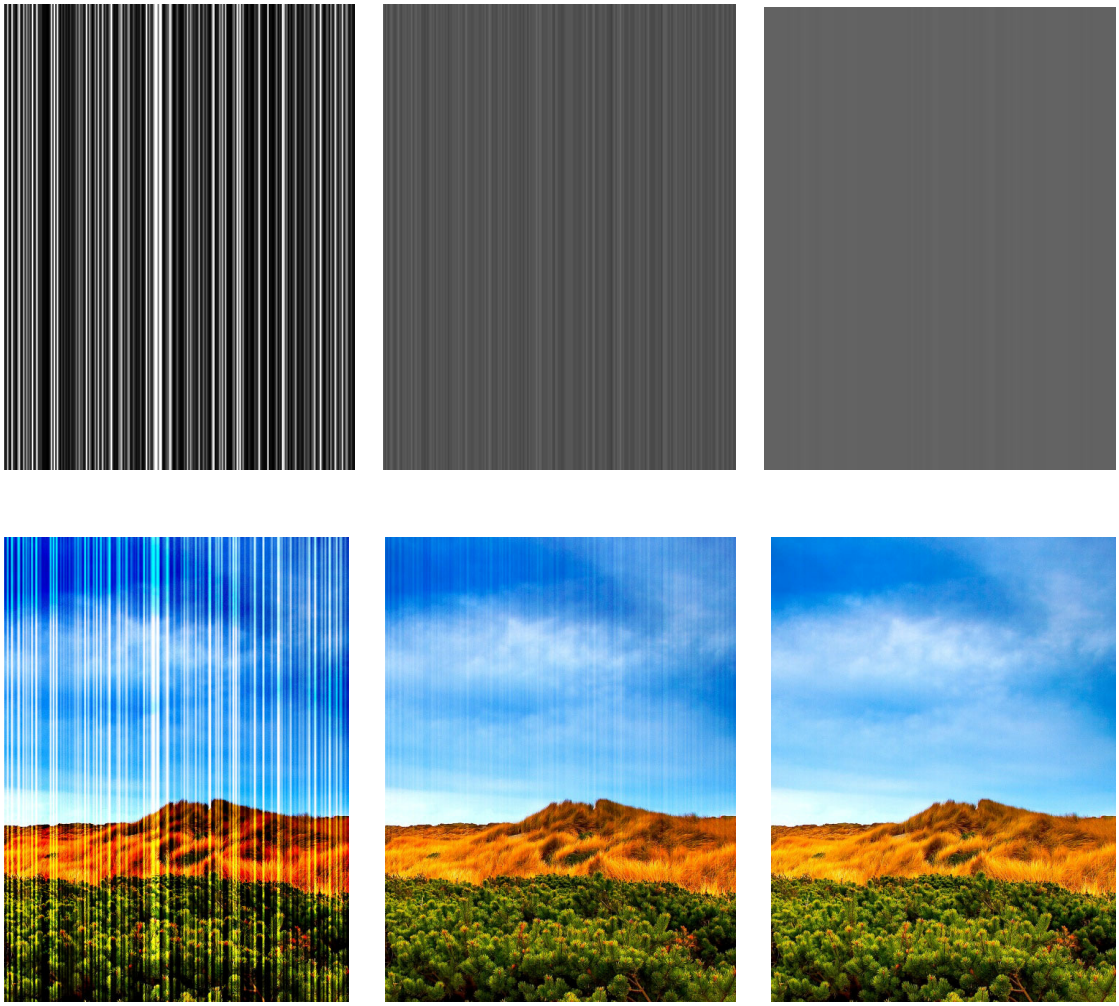


Figure 3.21: CBVP AMOLED pixel circuit along with the corresponding signal diagram.

the same way, each of them has its own advantages. If T5 is ON for the entire frame time except during the biasing cycle, C_{S2} can be removed from the parallel biasing circuit leading to higher aperture ratio. On the other hand, independent biasing provides for a separate storage capacitor for V_T and V_P-V_{bias}. Since, the leakage current of the a-Si:H TFTs is low (of

Table 3.2: Process variation in a typical poly-Si technology [32]

Process Parameter	Average	Standard Deviation (sd)
Mobility	**80 (cm2 /V s)**	**3.3**
Threshold Voltage	**1 (V)**	**0.1**



(a) **(b)** **(c)**

Figure 3.22: Mont-Carlo simulation results: (a) conventional 2-TFT, (b) voltage programmed, and (c) CBVP pixel circuits

the order of 10^{-14} A) [52], it is possible to store the V_T in C_{S1} and use it for several consecutive frames which can improve the power consumption [57].

To verify the tolerance of the pixel circuit, a Gaussian distribution for the mobility and V_T variation typical for poly-Si (depicted in Table 3.2) [32] and Mont-Carlo simulation is used. Simulation is carried out for 240 pixels resembling a row in a QVGA display (240x3x320). Also, the simulations are conducted for a pure voltage programmed pixel circuit [83]. Figure 3.22 demonstrates the simulation results as a visual artifact on the display quality. Tthe simple 2-TFT pixel suffers from both V_T and mobility variation and the voltage programmed pixel circuit cannot handle mobility variation, whereas the CBVP compensates for both variations.

Also, to investigate the effectiveness of the new CBVP pixel circuits, the circuits are assembled from a pre-fabricated pixel circuit and a discrete TFT (see Figure 3.23). To test a single pixel, T4 and T5 can be the same TFT. Thus, to reduce the effect of parasitic capacitance induced by discrete TFTs, a single TFT is used for T4 and T5. The pixel parameters are listed in Table 3.3, the aspect ratio of the discrete TFT is 300 μm/ 23 μm, and I_{bias} is 4 μA. A diode-connected TFT (T_{OLED}) and a capacitor (C_{OLED}) are used to emulate the OLED.

The I-V characteristic of the CBVP pixel circuits is depicted in Figure 3.24. The pixel circuit with the independent biasing technique requires negative voltages while the other circuit works with positive voltages. As seen, the hold current is smaller than the programming current (the current during programming cycle) which is a consequence of charge injection and clock feed through. More importantly, the slope of the hold currents for the two pixel circuits is different which can be explained by the charge injection effect of *T4*

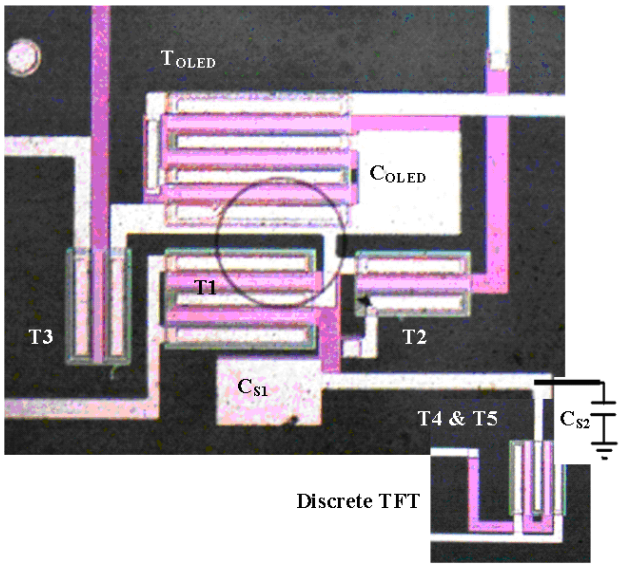


Figure 3.23: Photo micrograph of the fabricated AMOLED CBVP pixel circuit.

Table 3.3: AMOLED CBVP pixel circuit parameters

Name	Description	Values
W/L(T1)	Aspect ratio of T1	400/23
W/L(T2)	Aspect ratio of the TFT used for S1	100/23
W/L(T3)	Aspect ratio of the TFT used for S2	100/23
W/L(T4)	Aspect ratio of the TFT used for S3	100/23
C_S	Storage capacitance	1 pF
V_H	ON voltage of the switches	30 V
V_{DD}	Operating voltage	20 V

and T5. Using the model presented in [84], the effect of charge injection and clock feed-though of T5 can be written as (see Chapter 6 for more detail analysis)

$$V_5 = \frac{C_{S1}}{2C_{OV1} + C_{OV2} + C_{S1}} \left(\frac{C_{ov5}}{2(C_{OV5} + C_{S2})} V_H - \frac{C_{gs5}}{C_{OV5} + C_{S2}} (V_H - V_{B2} - V_{T5}) \right) \quad (3.4)$$

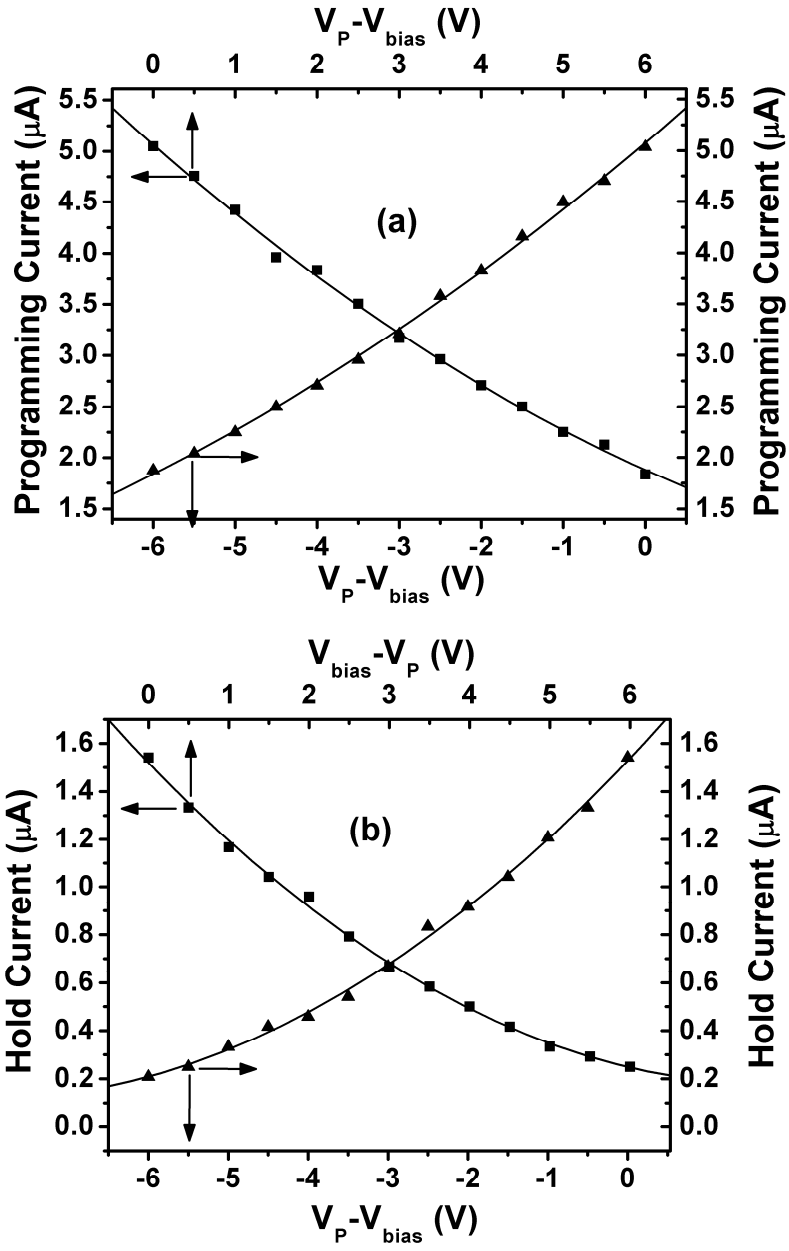


Figure 3.24: Measurement resuts of the (a) programming current and (b) hold current (squres denotes prallel biasing and triangles are the resutls of independent biasing).

where, $C_{ov1,}$ $C_{ov2,}$ and C_{ov5} are the overlap capacitances between gate and source (drain) of T1, T2 and T5, respectively. C_{gs5} is the gate capacitance of T5, V_{T5} the threshold voltage of T5 and V_{B2} the voltage at node B at the end of the programming cycle. For the parallel biasing

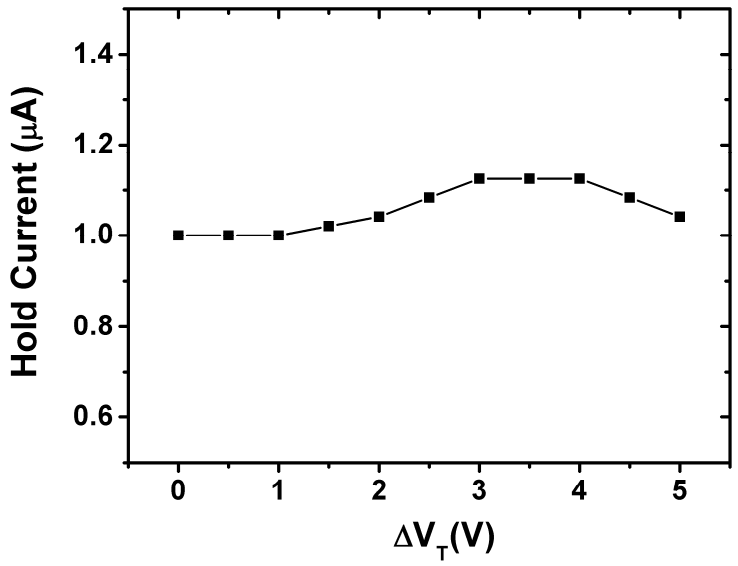


Figure 3.25: Lifetime measurement of the a-Si:H CBVP AMOLED pixel circuit.

technique, V_{B2} is zero, and so the charge injection of T5 is independent of the programming voltage (V_P), whereas for the independent biasing technique, V_{B2} is V_P-V_B resulting in V_P dependent charge injection, which in turns leads to two slightly different hold-current slopes for the CBVP circuits.

Lifetime measurement result of the AMOLED CBVP pixel circuits is shown in Figure 3.25. Here, the source voltage of T1 is increased to emulate the V_T-shift. The increase in the current is due to the charge injection as discussed in Chapter 6. However, drop in the current is due to the channel length modulation [52] since the drain-source voltage (V_{DS}) is decreased by the artificial aging. This will not be the case in a real aging experience since V_{DS} is fixed.

3.4 Summary

The CBVP driving scheme can improve the settling time and benefits from the simplicity of the voltage programming and accuracy of current programming. The CBVP driving scheme can compensate for all process variations including mobility and V_T

mismatches leading to higher yield especially in poly-Si. The driving scheme is easily adapted in high resolution multi-modal biomedical imager. Here, in pixel gain is used for low-intensity signals whereas high-intensity signals are detected in the passive mode. Also, the pixel accommodates a variable capacitor by using a MIS structure for further dynamic range improvement. For low-intensity signals, the capacitor is biased to provide a lower capacitance resulting in a higher SNR. For, high-intensity signals, the capacitor is biased for higher capacitance value preventing saturation of the external driver.

The CBVP driving scheme is also used in the AMOLED pixel circuit. Here, the settling time fits most of application but for larger displays, there is a need for faster settling driving schemes which are discussed in next chapter.

Chapter 4

Enhanced-Settling Current Programming

Although the current mode active matrix provides an intrinsic immunity to mismatches and differential aging, the long settling time at low current levels and large parasitic capacitance is a lingering issue. As explained in Chapter 2, the major source of the settling time in current programming is the large parasitic capacitance. Although, using small switch transistors can reduce the parasitic capacitance to some extent [17], the optimized settling time still cannot fit the programming time required for most of applications. In addition, the acceleration techniques cannot improve the settling time significantly, particularly if low mobility technologies are used. As a result, external driver assistance is required.

4.1 Positive Feedback

To overcome the settling-time issue in current programming, a new fast current driver is proposed that controls the effect of the parasitic capacitance by positive feedback [85, 86] (as seen in Figure 4.1). Here, a band pass (BP) filter is used as the feedback function. At the beginning of the programming cycle, the voltage of the line changes rapidly, and the current source pumps more current into the current line. As the voltage of the current line settles, the current of the source moves to a programming current. Also, the band-pass filter prevents the high-frequency noise of the line to influence the output current of the source driver.

The feedback system cannot be implemented by using a sophisticated filter circuit,

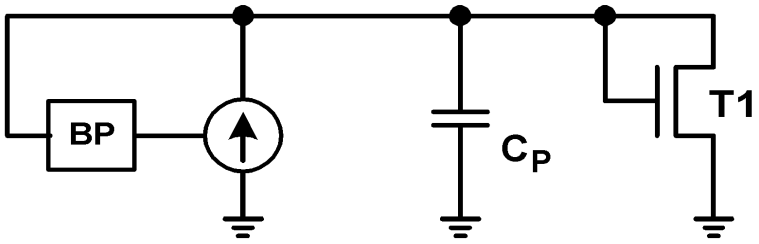


Figure 4.1: Fast current driver based on positive feedback.

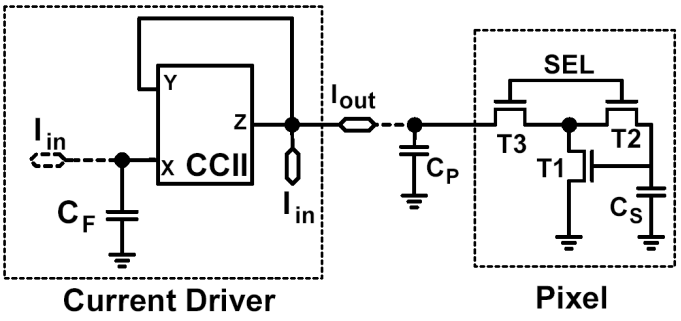
because it should fit within the pitch of the pixels (<< 100 μm). As a result, the BP filter is implemented as a one-pole low-pass Butterworth filter and a differentiator. As depicted in Figure 4.2 (a) and (b) the driver can be implemented based on a simple current conveyer type II (CCII) [87, 88] with the following I-V characteristics

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ A & 0 & 0 \\ 0 & M & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}. \tag{4.1}$$

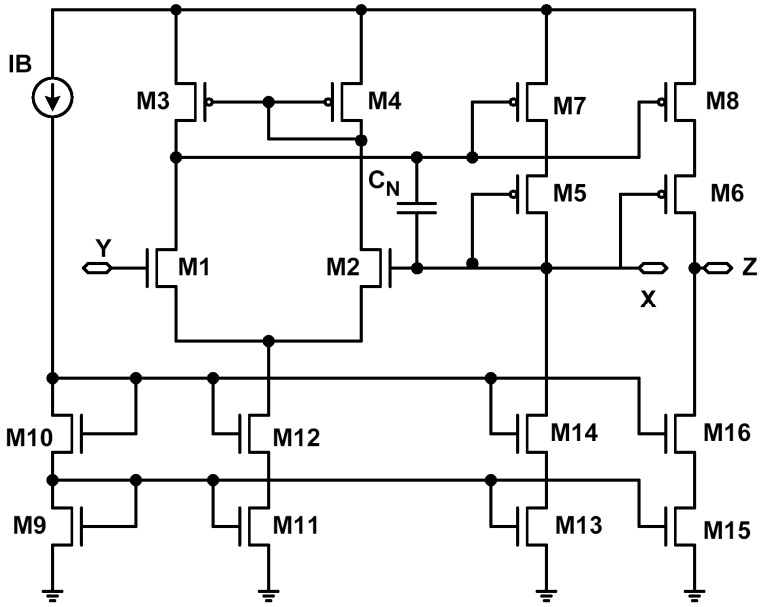
The amplitudes of A and M can be approximated as the unity and independent of the input values for small signals. However, since active matrix devices deal with large signals, A and M become input signal dependent. The voltage at the X terminal is controlled by the voltage at Y, which is equal to the voltage at the Z terminal ($V_X = AV_Z$ where $|A| \leq 1$). The programming current (I_P) can be either applied to the X- or to Z-terminals. Considering the case in which the programming current is directly connected to the Z terminal, the current at the X terminal is given by

$$I_X = -AC_F \frac{d}{dt} V_Z, \tag{4.2}$$

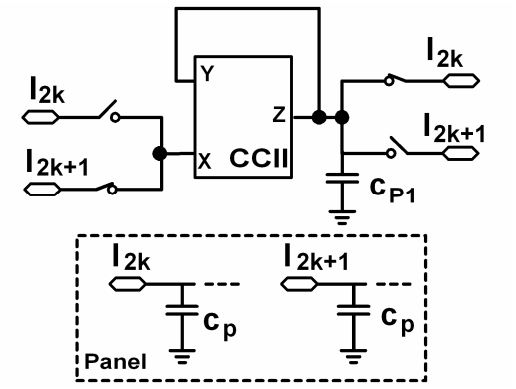
where C_F is the feedback capacitor, and V_Z the voltage at the Z terminal. The current at the Z terminal can be defined by that of the X terminal (I_Z=MI_X) Therefore, the behavior of the system can be written as



(a)



(b)



(c)

Figure 4.2: Fig. 8: (a) Fast current driver, (b) circuit diagram of the current conveyor II, and (c) implementation method for C_F using column parasitic capacitance.

$$I_P = (C_P - AMC_F)\frac{d}{dt}V_Z + \beta(V_Z - V_T)^2 . \quad (4.3)$$

Thus, the time constant becomes $\tau = 2(C_P - AMC_F)/(\beta.I_P)^{0.5}$. As a result, choosing AMC_F close to C_P reduces the effect of the parasitic capacitance significantly. Since C_P can be large (of the order of 100 pF), having M larger than one leads to smaller C_F, which can be implemented inside the driver chip. A larger C_F can be implemented externally with a MIM capacitor at the edge of the panel during the panel fabrication with no extra cost, or with the parasitic capacitance of the data line. Figure 4.2 (c) shows a proposed architecture for using the parasitic capacitance as C_F. C_{P1} is a small integrated compensation capacitance to stabilize the driver and the switches can be shared with offset cancellation circuit as discussed further in the next sections. Since, by using the fast current driver, the settling time can be smaller than the required programming time, it is possible to divide a frame into two sub-frames and program the odd and even columns during each sub-frame. Thus, the parasitic capacitance of the columns that are not programmed during each sub-frame can be used as the C_F for the other columns. For example; the odd columns can be programmed first while using the parasitic capacitance of the even columns as the C_F, and vice versa during the next sub-frame. Thus, C_F is not integrated into the driver, and the number of current sources is reduced by half, resulting in a smaller die area.

4.2 Stability and Noise Analysis

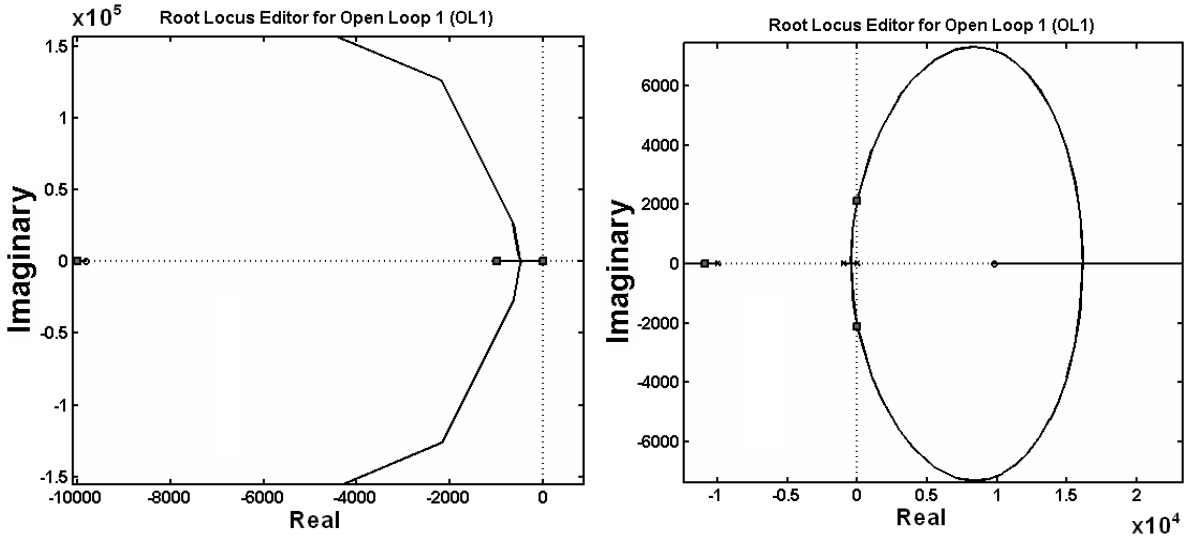
To investigate the stability of the system, two distinct approaches are taken. When the operating condition (involving large currents) cannot be approximated by small signal analysis, the Lyapunov approach [89] is selected to define the stability region for the driver. The settling point of (4.3) is moved to zero as following

$$\frac{d}{dt}x = \frac{x}{(C_P - AMC_F)}\left(-\beta x - \sqrt{\beta I_P}\right);$$
$$x = V_Z - \sqrt{\frac{I_P}{\beta}}\,. \tag{4.4}$$

By defining the energy function as $E(t)=x^2$, the derivative of E can be written as

$$\frac{d}{dt}E = \frac{2x^2}{(C_P - AMC_F)}\left(-\beta x - \sqrt{\beta I_P}\right). \tag{4.5}$$

Based on the Lyapunov approach, it can be concluded that the driver is stable if (4.5) is negative which means that AMC_F should be positive and smaller than the overall parasitic capacitance. To investigate the stability of the driver in the presence of noise, cross talk, and small current levels, a small signal analysis is employed. Figure 4.3 shows the root-locus plot for the circuit with two different feedback capacitors. The circuit is unconditionally stable for C_F = 90 pF (< C_P). On the other hand, to stabilize the circuit with C_F =110 pF (> C_P), the close loop gain between V_Y and V_X should be smaller than 1.



(a) **(b)**

Figure 4.3: Root locus plot for (a) C_F = 90 pF and (b) C_F = 110 pF.

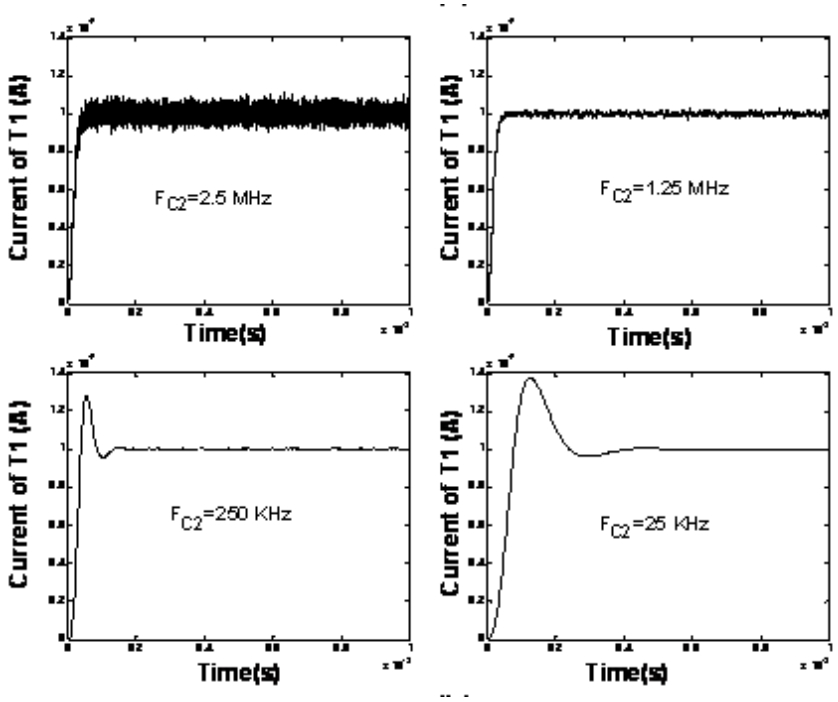


Figure 4.4: Transient waveforms of the positive feedback current source with different cut-off frequencies in the presence of noise.

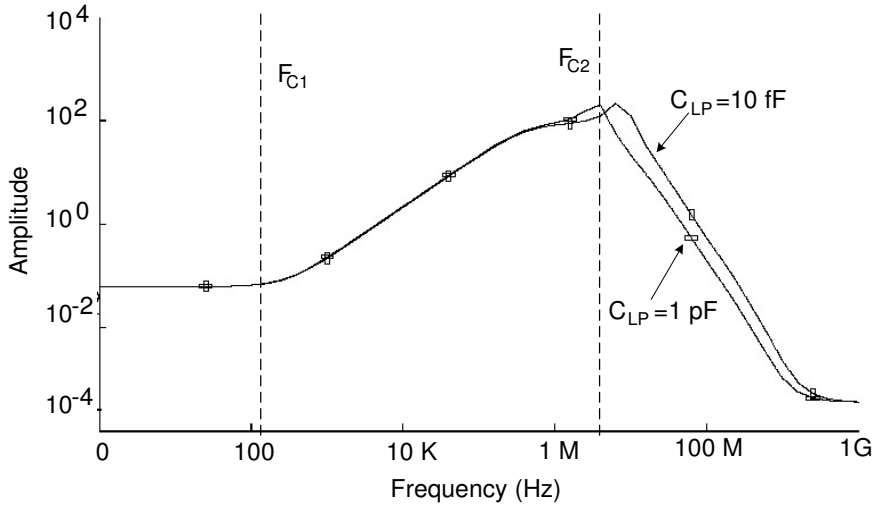


Figure 4.5: Frequency response of the CCII current source for different values of C_{LP}.

Also, a MATLAB model is used to investigate the characteristics of the new current source. Figure 4.4 emphasizes the effectiveness of the filter on the noise performance. It is evident that increasing the cut-off frequency of the LP filter makes the driver more sensitive to the noise of the current line. However, as the cut-off frequency increases, the speed

increases as well. The Butterworth filter is implemented by simply adding a capacitor between the output of the voltage feedback and X terminal (C_{LP}). As it is shown in Figure 4.5, increasing the C_{LP} results in a smaller F_{C2}. Also, the circuit acts as a differentiator between F_{C1} and F_{C2}. The slop of the differentiator is defined by the value of C_F.

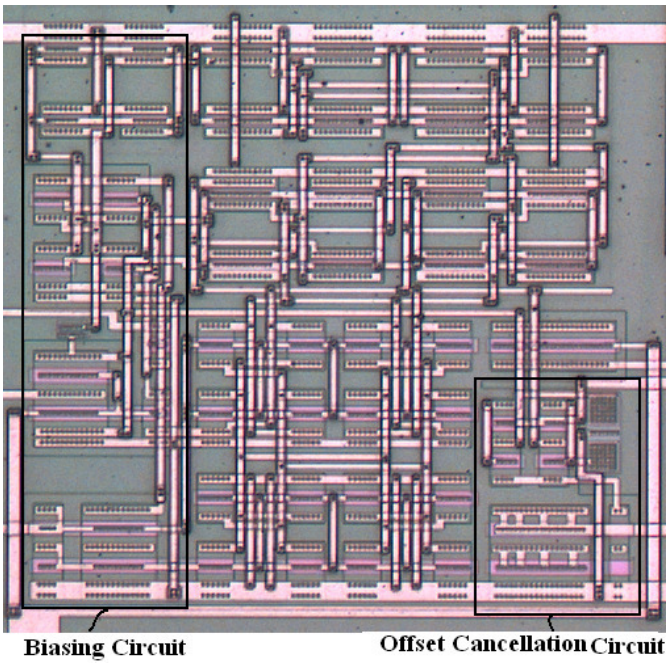


Figure 4.6: Photomicrograph of the fabricated current driver.

Table 4.1: Parameters of fabricated current driver

Name	Description	Value
$(W/L)_{1,2}$	Aspect ratio of M1 and M2	30 µm /6 µm
$(W/L)_{3,4}$	Aspect ratio of M3 and M4	40 µm /6 µm
$(W/L)_{5,8}$	Aspect ratio of M5 to M8	120 µm /6 µm
$(W/L)_{9,10}$	Aspect ratio of M9 and M10	12 µm /6 µm
$(W/L)_{13,16}$	Aspect ratio of M13 to M16	60 µm /6 µm
$(W/L)_{19,20}$	Aspect ratio of M19 and M20 used in	10 µm /6 µm
C_N	Noise reduction capacitance	1 pF
C_F	Feedback capacitor	10-200 pF
C_P	Parasitic capacitance	10-200 pF

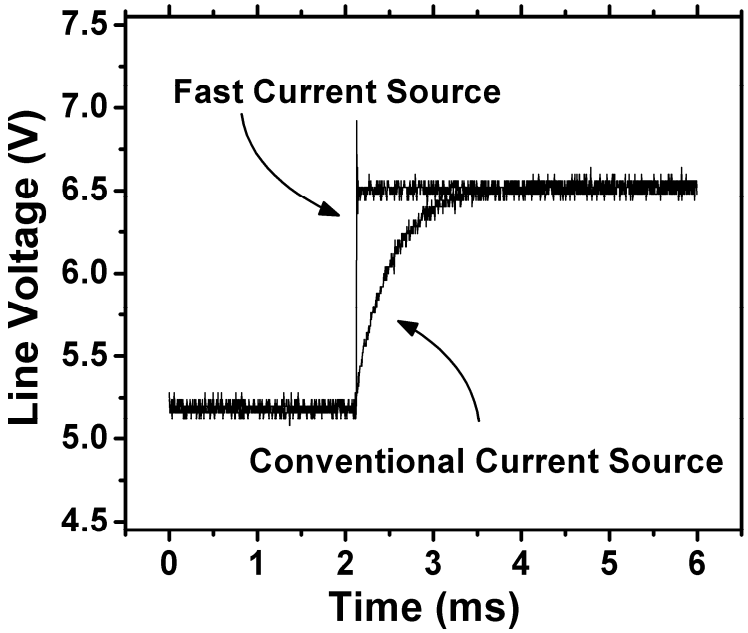


Figure 4.7: Transient line voltage waveform for the fast and conventional and fast current driver.

4.3 Measurement Results and Discussion

The photomicrograph of the driver fabricated in a high voltage CMOS process (the 0.8-μm process of DALSA semiconductor) is given in Figure 4.6. The parameters of the fabricated driver are listed in Table 4.1. Figure 4.7 demonstrates the settling time of the pixel circuit for a step current of 100 nA in the presence of parasitic and feedback capacitances of 100 pF. It is clear that the fast current driver can manage the effect of parasitic capacitance and reduce the settling time significantly.

The I-V characteristics of the current driver are extracted by using a Keithley 236 source measurement unit (SMU). For the results shown in Figure 4.8, the output is connected to a fixed voltage (7 V), while the input current is swept. The output current closely follows the input current at a fixed input voltage of 7 V. However, the voltage dynamic range does not stretch from rail-to-rail (as observed in Figure 4.9). Here, the input current is 1 μA, and

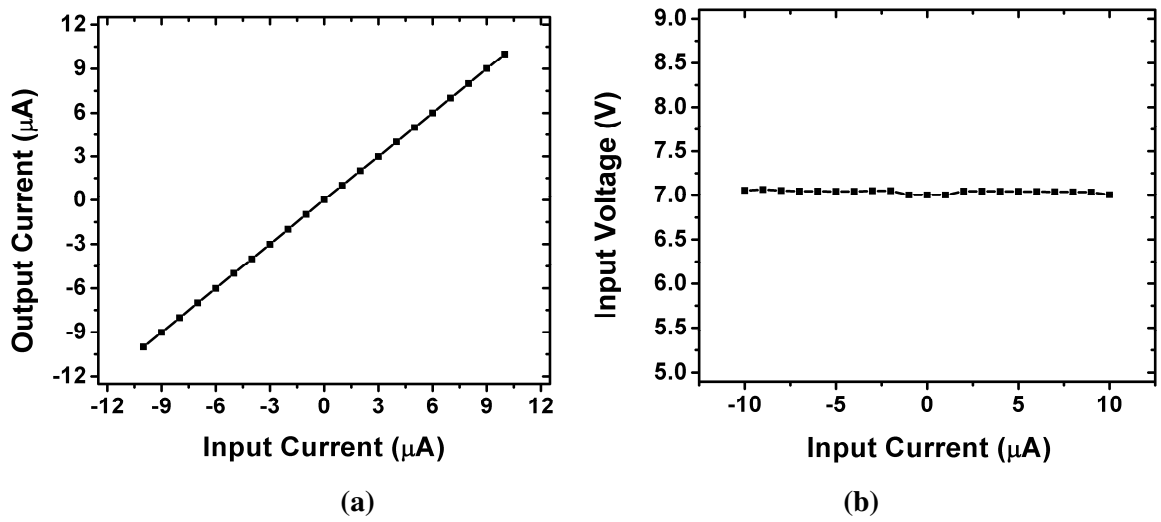


Figure 4.8: (a) Output current and (b) input voltage for a fixed output voltage as a function of input current.

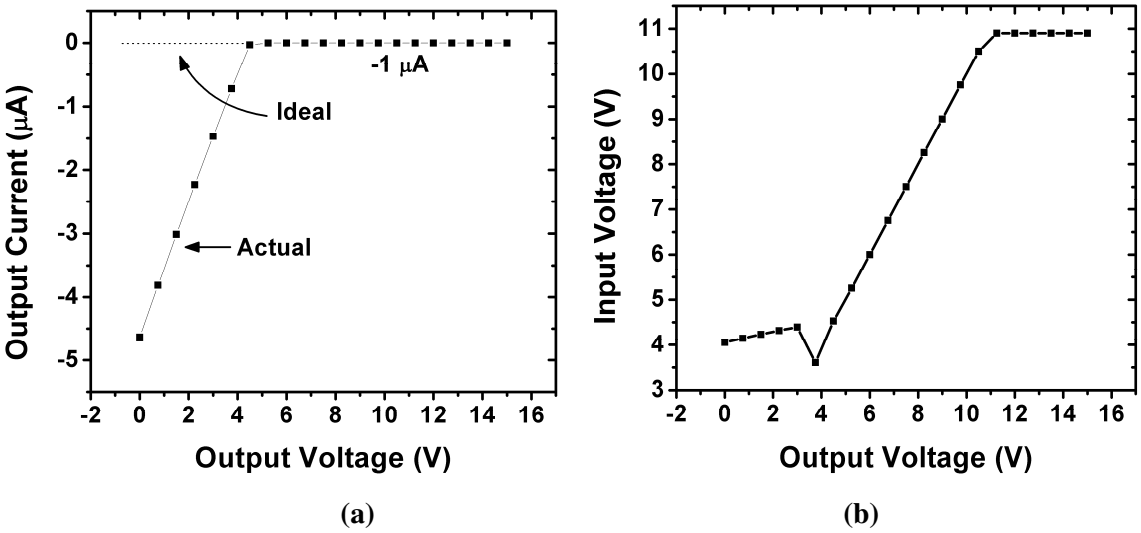
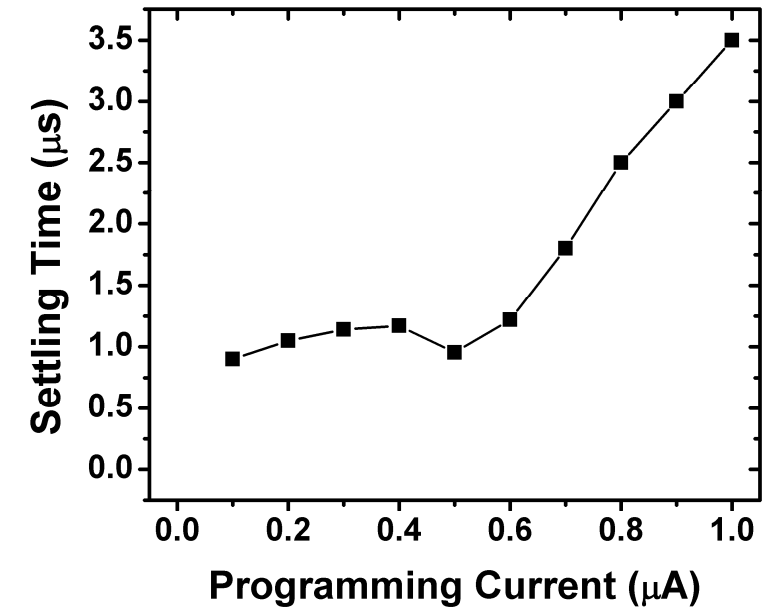


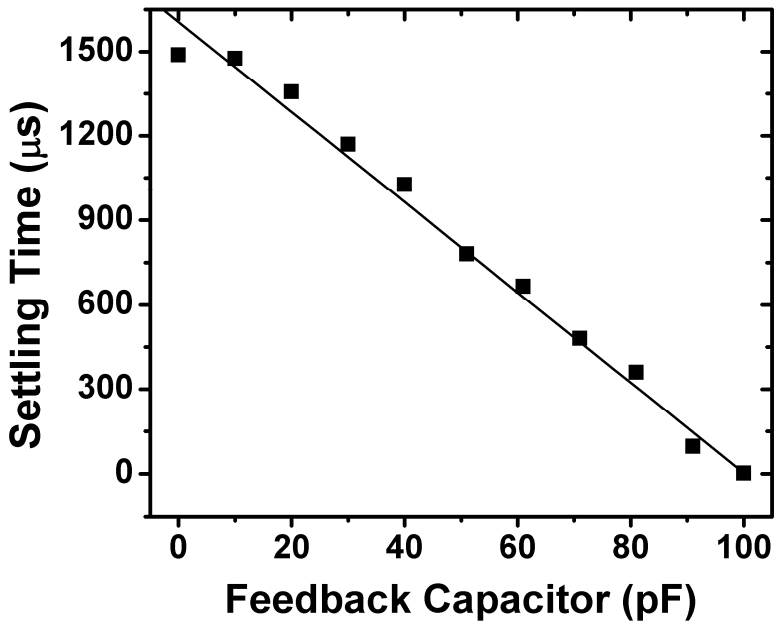
Figure 4.9: (a) Output current and (b) input voltage for a fixed output voltage as a function of input voltage.

the output voltage is swept from 0 to V_{DD} = 15 V. This can result in different settling times for different programming currents, as discussed in the following.

Figure 4.10(a) shows the settling time extracted for a 200-pF parasitic and feedback capacitance for the current cell demonstrated in Figure 2.2 (a). Here, V_f-V_0 is set to 1 V throughout the entire measurement range. Since the programming time for large-area and



(a)



(b)

Figure 4.10: Settling time as a function of (a) programming current and (b) feedback capacitor.

high resolution active matrix devices is larger than 10 μs, it is clear that the driver presented here can meet the requirements of a vast range of applications since the settling time is less

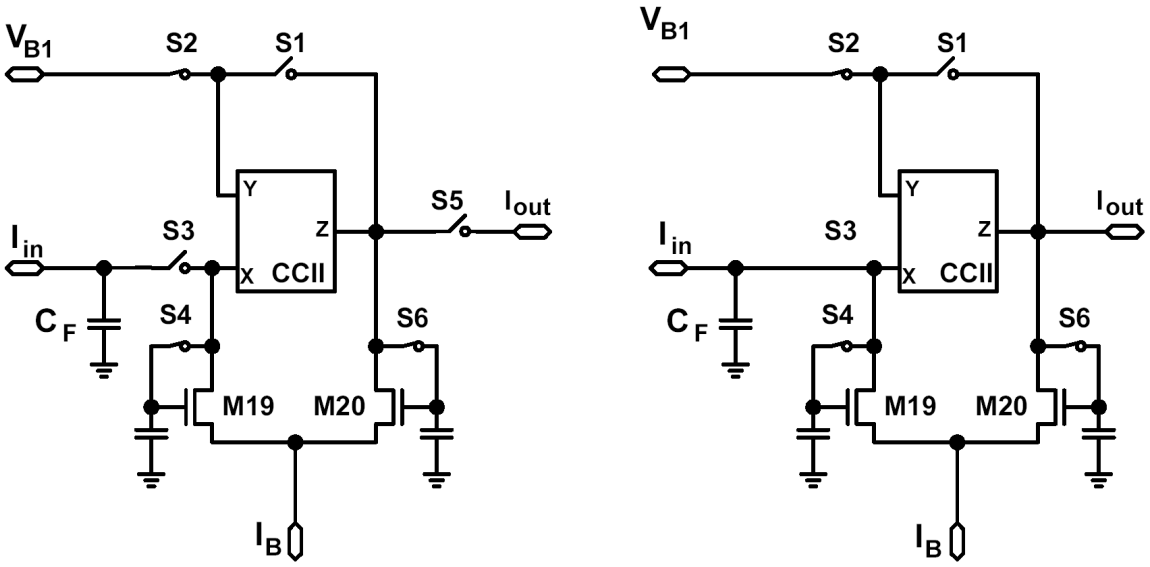


Figure 4.11: (a) Circuit schematics for offset cancellation and (b) offset-leakage cancellation.

than 4 μs. While it is expected that the settling time drops as the programming current increases, the measurement results exhibit a reverse trend. This occurs because the closed-loop voltage gain reduces for large voltages, as depicted in Figure 4.9(b), mitigating the effectiveness of the driver in accordance to (4.3).

The effect of the feedback capacitance is shown in Figure 4.10 (b). The input current is 1 μA and the parasitic capacitance is 100 pF. The settling time decreases linearly, as the feedback capacitance increases, again corroborating with (4.3).

4.4 Self-Calibration of the Current Source

In applications for which the current driver is intended, the current levels are small (of the order of 1 μA) which compounds the effect of the offsets mandating an effective offset cancellation technique. Figure 4.11 demonstrates two different configurations for the offset

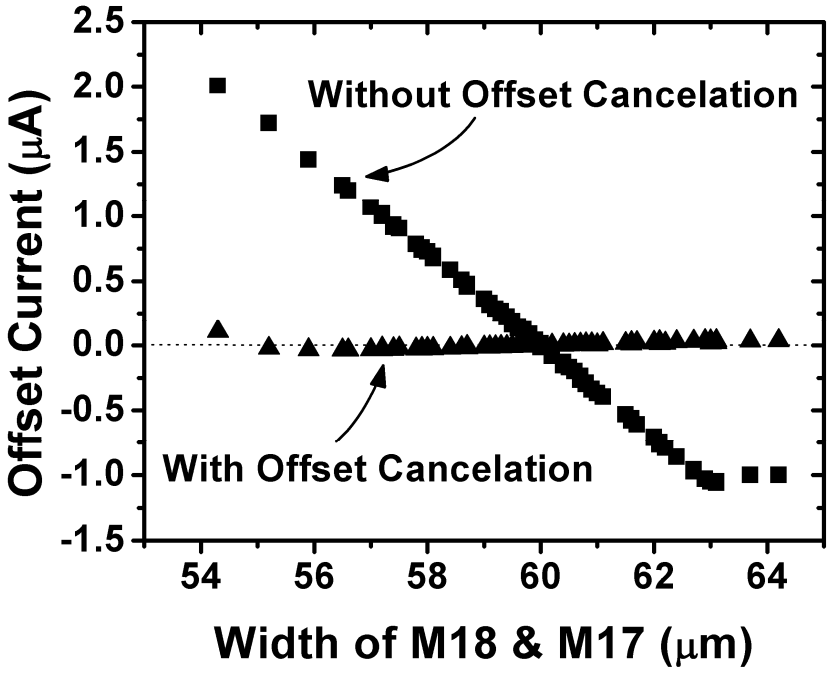


Figure 4.12: Monte Carlo simulation of the offset current as a function of transistor mismatch with and without offset cancellation.

cancellation. A differential circuit is adopted in both configurations to reduce the effects of the charge injection and clock feed-through leading to small storage capacitors. In case I (Figure 4.11 (a)), the circuit is disconnected from the input current and output load during the cancellation process. If there is an offset between the current of the X and Z terminals, M19 and M20 stores the offset, alleviating its effect [84]. Since the statistics of the process variations for the technology is not available, the offset is emulated by variations in the width of the paired transistors. Figure 4.12 shows Monte Carlo simulation results for variation in the width of M17 and M18. The offset current varies from -1 μA to 2 μA for the circuit without cancellation. In contrast, the offset current remains smaller than 10 nA for case I. Although this technique can control the offset associated with the driver, the technique is

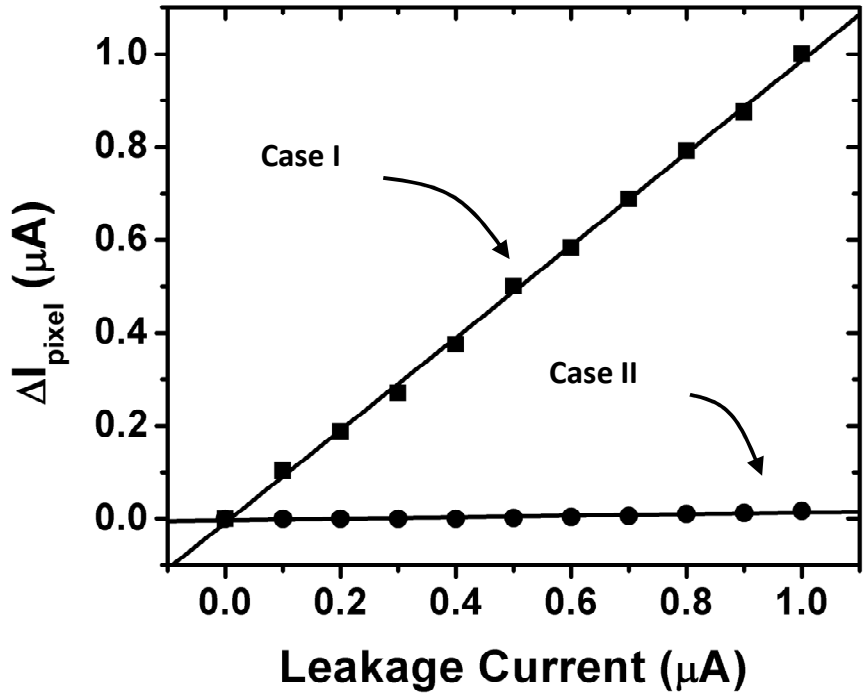


Figure 4.13: Effect of leakage on the output of case I and II of cancellation techniques.

prone to offsets, stemming from the input and leakage currents caused by the pixels connected to the output.

Figure 4.11 (b) shows a configuration that compensates for the aforementioned issues in addition to the driver offset. Here, the input and output terminals are connected to the current source and output load, respectively, during the cancellation process. Therefore, any output leakage or source offset is stored by M19 and M20 rendering the circuit offset-immune. Figure 4.13 demonstrates measurement results for which a current source is connected to the output of the driver to emulate the leakage current, and the output of the current cell connected to the driver is monitored. In case I, the leakage current is conveyed to the cell output current, whereas, for case II, the output current is independent of the leakage current. Moreover, this circuit can perform the CDS reducing the reset and programming

noises. Since the reset noise is the most significant portion of the input referred noise in sensors and imagers, the noise performance improves significantly. This can be seen in Figure 4.5 where, the gain for low frequency signal is around -40 dB.

4.5 Summary

The current driver, introduced in this chapter, controls the effect of parasitic capacitance and improves the settling time substantially. The settling time for a 100 nA current, in the presence of a 200 pF parasitic capacitance, is less than 4 μs for the proposed current driver. Also, the novel offset-leakage cancellation technique can manage the effect of driver offset, besides the effect of the leakage and offset currents from the pixels connected to the data line. Therefore, the new driver can further extend the applications of current programming to enable scaling to large area active matrix devices, and yet maintain high refresh rates.

Chapter 5

Charge-Based Driving Scheme

Considering all the design considerations, an ideal driving scheme for a-Si:H AMOLED displays should not only prevent additional complexity in the simple voltage programming (2-TFT pixel circuit [6]) but also compensate for the instability (or mismatches) of the backplane without compromising the aperture ratio. Thus, a new driving

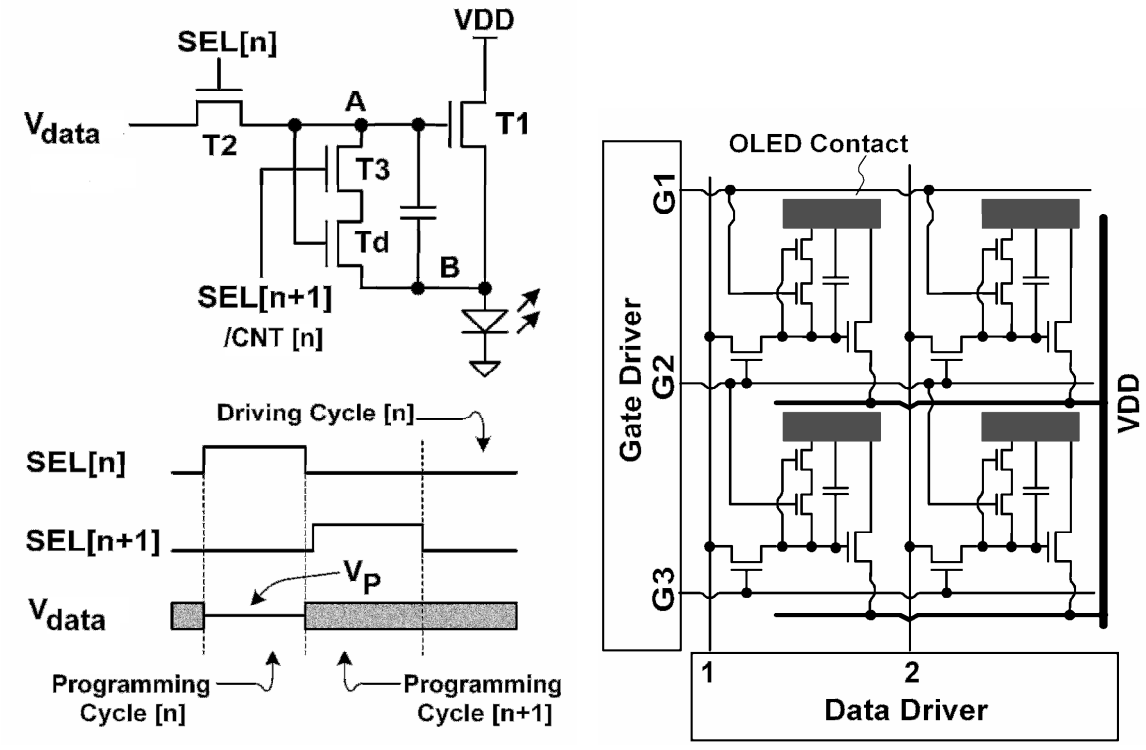


Figure 5.1: AdMo™ AMOLED (a) pixel circuit and (b) array structure based on charge-based compensation.

scheme is proposed where the pixel aging is compensated based on discharged voltage [89, 90]. Here, the amount of the leaked charge from the gate voltage of the drive/amplifier transistor changes as the TFT ages and compensates for the aging.

5.1 Advance Mobile Technology (AdMo™)

Figure 5.1 (a) demonstrates the proposed simple voltage-programmed pixel circuit. During the programming cycle of the n^{th} row, node A of the pixel circuits in that row are charged to a programming voltage (V_P), related to the pixels' image data. During the programming cycle of the $(n+1)^{th}$ row, a part of the voltage, stored at node A, is discharged through Td. The amount of discharged voltage (eliminating the effect of OLEDs), ΔV_A, is controlled by the channel resistance of Td which is defined by the aspect ratio, mobility, and threshold voltage of Td, given by

$$\Delta V_A = \frac{(V_P - V_{OLED} - V_T)^2}{(V_P - V_{OLED} - V_T) + \frac{\tau}{t}} \quad \text{and} \quad \tau = \frac{C_S}{(W/L)_{Td} K}. \tag{5.1}$$

Here, V_T is the threshold voltage of Td, V_{OLED} the OLED voltage, $(W/L)_{Td}$ the aspect ratio of *Td*, K a function of mobility and gate capacitance, and C_S the storage capacitor. More importantly, since Td and T1 are physically adjacent and have the same biasing condition, Td represents T1 in the discharging process. For example, electrical aging causes correlated shifts in the threshold voltages of T1 and Td. Also, a shift in the threshold voltage of Td results in higher channel resistance for a given voltage, and so the discharged voltage is reduced in a given discharge time. Therefore, the gate-source voltage of T1 becomes larger, and so compensates for the V_T shift. Figure 5.1(b) shows the array structure, based on the proposed pixel circuit. As shown, an extra address line SEL[m+1] is required for the entire display, where m is the number of rows in the display.

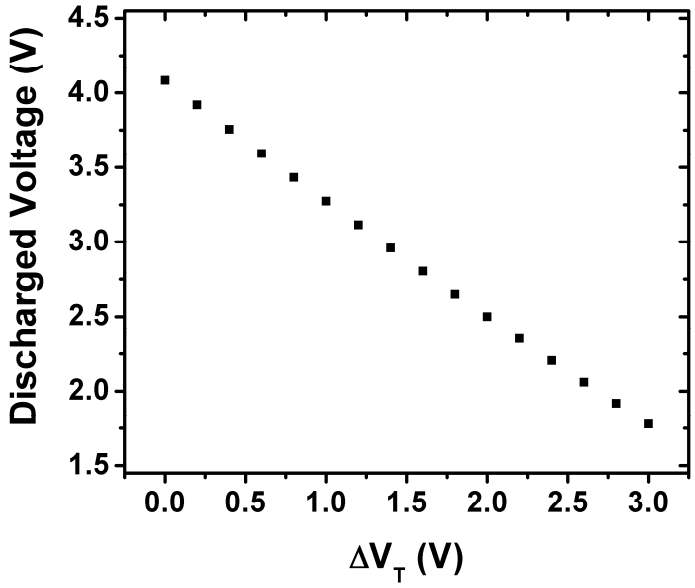


Figure 5.2: The discharged voltage for different shifts in the threshold voltage of T1.

Figure 5.2 shows the discharged voltage for a different V_T-shift (ΔV_T). It is clear that as ΔV_T increases the discharged voltage decreases linearly. Here, C_S is 350 fF, T1 is 180 µm/3 µm, T2 is 20 µm/3 µm, T3 is 18 µm/3 µm, and Td is 4.5 µm/4 µm. Besides the V_T-shift, the shift in the OLED voltage, any spatial mismatches and/or temperature variations can be compensated by the discharged voltage.

5.1.1 Measurement Results

To investigate the effectiveness of the proposed driving scheme, the pixel circuit is fabricated and tested under electrical stress. A micro-controller is used to generate the required signals for a programming time of 20 µs and frame rate of 60 Hz.

Figure 5.3 shows the current passing through T1 during different operating cycles. In this experiment, some delays are added between each operating cycle to exhibit the role of each cycle. During the n^{th} programming cycle, a large current passes through T1 as node A charges to a programming voltage (V_P). The pixel current drops, as T2 turns off at the end of

this cycle, due to the charge injection effect of T2. During the $(n+1)^{th}$ programming cycle, the voltage at node A starts discharging through Td, and so the pixel current drops to the desired current levels. This current is preserved during the driving cycle since the voltage is stored in the storage capacitor.

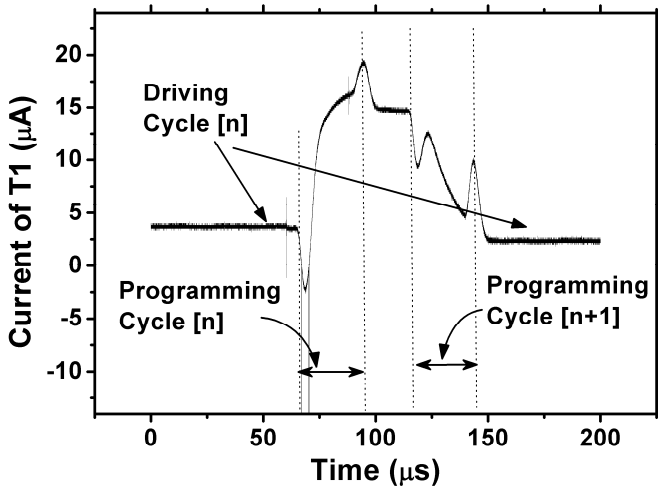


Figure 5.3: Measured current of T1 during different operating cycles.

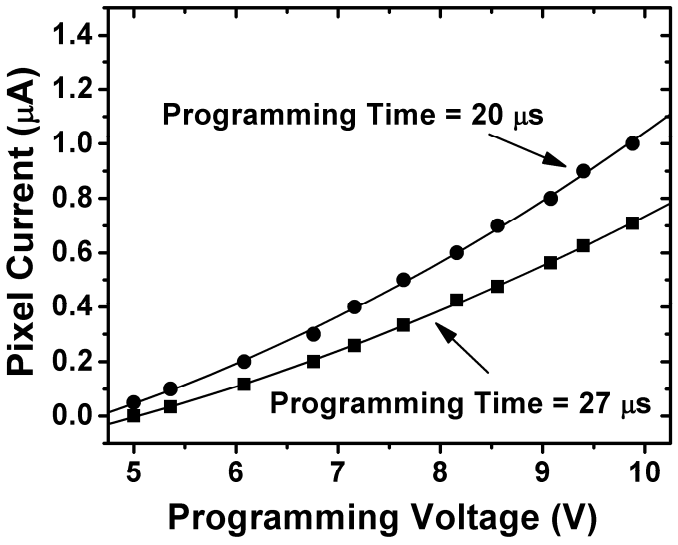


Figure 5.4: Measured IV characteristics of the AdMo™ pixel circuit.

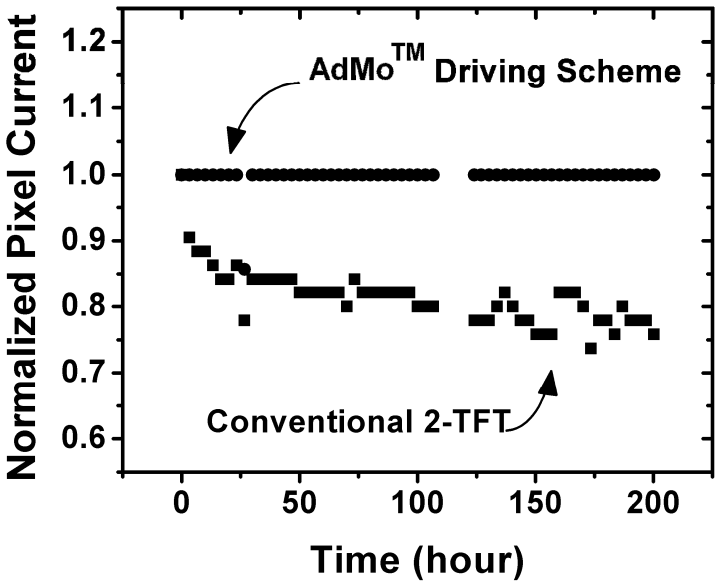
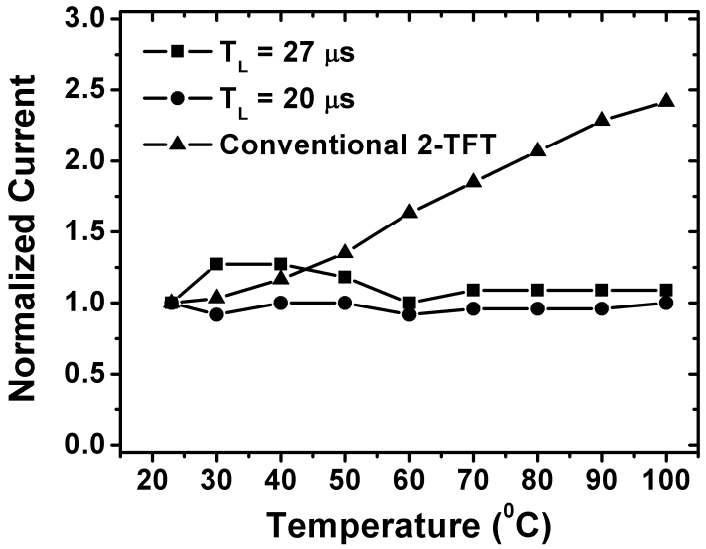


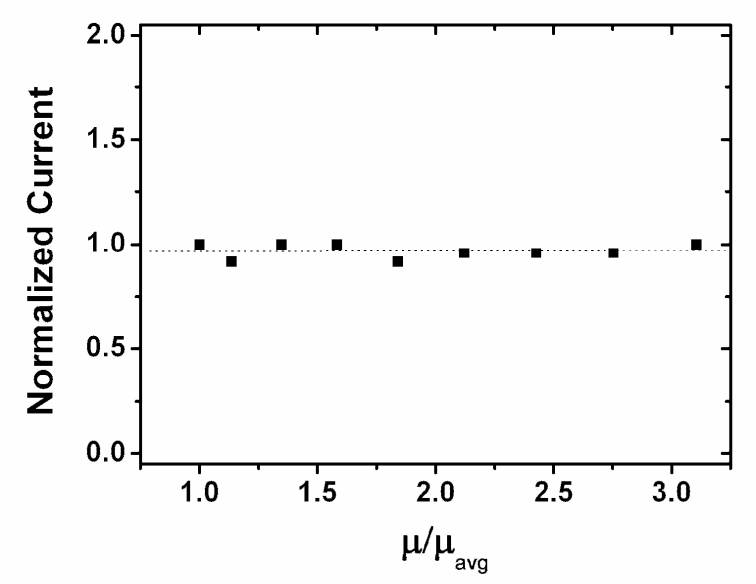
Figure 5.5: Lifetime measurement of AdMo™ and conventional 2-TFT pixels.

As shown in Figure 5.4, the level of the pixel current (current passing through the OLED during the driving cycle) drops as the timing of the programming cycle increases.

To test the lifetime of the pixel circuit, it is subject to a bias stress which emulates the worst case of operation condition. During each frame time, the pixel is programmed by the maximum programming voltage which results in an initial current of 1.17 μA, and its current is measured. Figure 5.5 compares the lifetime test results of the conventional 2-TFT pixel circuit versus the proposed new driving scheme. The current of the 2-TFT pixel circuit drops by 25% whereas the current of the proposed pixel circuit is significantly more stable. The fluctuation in the current of the conventional 2-TFT pixel circuit is due to the variation in ambient temperature. Since the results for the proposed and 2-TFT pixel circuits have been extracted in the same environment and time, the results indicate that the proposed driving scheme is stable under temperature variations as predicted earlier.



(a)



(b)

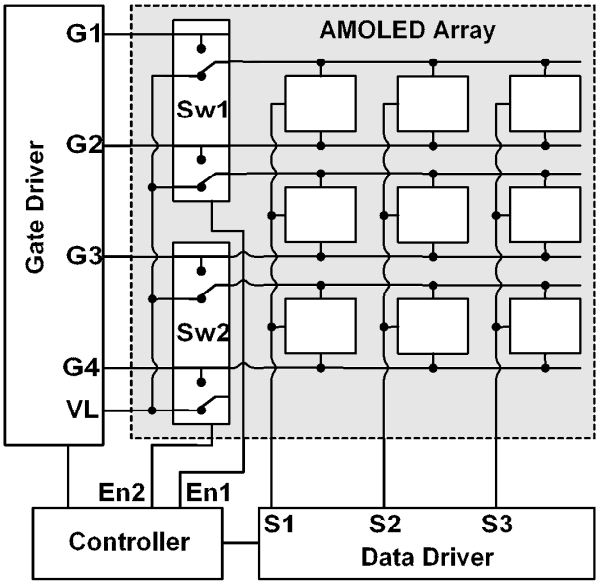
Figure 5.6: Measured pixel current under (a) temperature and (b) mobility variation.

The effect of temperature variation is measured as well. The results are shown in Figure 5.6 (a) verifying the temperature stability of the AdMo^{TM} pixel circuit. Here, the T_L is the leakage time, and $T_L = 0$ represents the conventional 2-TFT pixel circuit. As suggested in (5.1) increasing the mobility increases the discharged voltage, resulting in smaller gate-

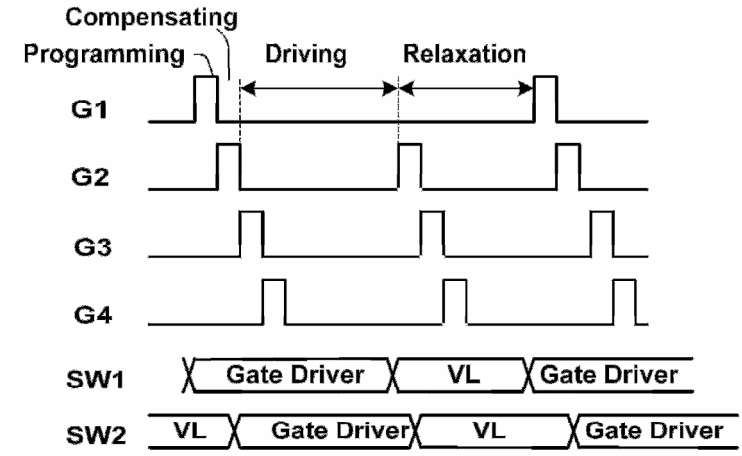
source voltage. Thus, the pixel current becomes constant despite the higher mobility. Temperature effects mobility, V_T, and power parameter in IV-characteristics of the a-Si:H TFTs [91]. Figure 5.6 (b) represents the measurement results against the mobility variations (temperature variations are translated to mobility variations using the model presented by C. NG [91]). This result indicates that the pixel current is stable despite the mobility variations independent of the cause. As a result, this pixel can be adopted in flexible electronics in which the mobility varies by mechanical stress.

5.1.2 Implementation of the Relaxation Technique

To further extend the lifetime of the display, a new timing scheme is adapted which suppresses the threshold voltage shift. The frame time is divided into programming, compensating, driving and relaxation cycles [67, 90]. During the relaxation cycle, the gate-source voltage of the drive TFT is discharged to zero. Thus, the drive TFT is not under stress, and moreover, the trapped charges are released preventing an accumulation of the aging. Figure 5.7 (a) shows the proposed array structure for the relaxation technique. The outputs of the gate driver are directly connected to the CNT lines while being connected to the SEL lines through a dual switch (SW1 and SW2). Figure 5.7 (b) indicates that during the programming cycle, switches are connected to the gate driver. For the relaxation, the dual switches are connected to VL, which is the OFF voltage of the switch TFTs. As a result, T2 in the pixel circuit in Figure 5.1 (a) remains OFF, while T3 is ON discharging the gate voltage of T1. To compensate for the loss in luminance caused by relaxation, the pixel must be programmed for a brighter luminance.



(a)



(b)

Figure 5.7: Relaxation driving scheme: (a) array architecture and (b) timing diagram.

For a larger array in which there is not enough blanking time for discharging the gate voltage, the discharging and programming occurs in parallel. The use of dual switches ensures that there is no conflict between the programming and discharging operations. While, one row of a dual switch (e.g. SW2) is programmed, the corresponding row of the other dual switch (i.e. SW1) is discharged. Since switch transistors T2 of the row in discharging mode

are connected to VL and they are OFF, no cross talk occurs. The number of dual switches determines the ratio of the relaxation in a frame time. For example, if there are two dual switches, the relaxation cycle can be 50% of the frame time. To reduce the relaxation to 30% three dual switches are used. In this case, the programming and discharging operations occurs in SW(i) and SW(i-2) respectively. More importantly, the dual switches can be fabricated with a-Si:H TFTs placed at the edge of panel.

5.1.3 9-Inch AMOLED Display

The AdMo™ is adapted in the design of a 2.2-inch QVGA (240x3x320) and a 9-inch WXGA (800x3x480) displays. Here, each pixel consists of red, green, and blue sub-pixels. To design each sub-pixel, it is necessary to calculate the brightness share of each color for a targeted white point in the tristimulus or CIE coordination [93]. Since each color of the OLED is not pure meaning it covers a wide range of the spectrum, a 3x3 matrix (T_{SP}) is used to present the color contents of each OLEDs assuming they light up at 1 nit/m^2. As a result, the brightness share for each sub-pixel is calculated by the following:

$$B = T_{SP}^{-1} W \,. \tag{5.2}$$

B is a 1x3 matrix containing the brightness share of each sub-pixel, T_{SP}^{-1} the inverse of T_{SP}, and W is the tristimulus of desired whit point. Knowing the brightness share for each sub-pixel and the efficiency of each OLED, the maximum current required for each sub-pixel is expressed as

$$I_i = B_i . \eta_i \,, \; i = R, G, B, \tag{5.3}$$

where, I_i, B_i, and η_i are the maximum required current, a value in matrix B, and efficiency, respectively, corresponding to OLED *'i'*, respectively. The maximum overdrive voltage of

drive TFT (T1) is kept constant and required aspect ratio of drive TFT is obtained through simulation. This assures that the drive TFT of each sub-pixel ages at the same rate, preserving the white balance point during the display's lifetime. The switch TFTs are designed based on the required settling time.

Moreover, the aperture ratio is adjusted according to the efficiency of each OLED and their brightness share for the white point. As a result the three different OLEDs ages at the same rate avoiding any color shift in the white balance. The optimize aperture ratio is given by the following,

$$Ri = \frac{B_i \eta_i}{B_G \eta_G} \quad \text{and } i = \text{R or B}, \tag{5.4}$$

where, R_i is the ratio of the blue (or red) aperture ratio to the green's aperture ratio. Since green is normally the highest efficiency, green OLED is selected as the reference but any of the other OLEDs can be the reference. The sub-pixel is designed based on (5.3) and during the layout is optimized to achieve the aperture ratios listed in (5.4). The goal is to have the smallest possible overdrive voltage for the TFT and the largest possible aperture ratio for OLED in order to get the best lifetime for the TFT and OLED. Thus, the design of the pixel is an iterative process between selecting an overdrive voltage and obtaining the aperture ratio to get the optimum point for a display lifetime.

Figure 5.8 shows the layout of the RGB pixel for the two display sizes. The maximum front-screen brightness (FSB) for the 2.2-inch display is 200 nit/m^2 (after a 45% efficient polarizer) and it is 150 nit/m^2 for the 9-inch display. The achieved aperture ratios for the 2.2-inch display are 21%, 20.5%, and 30.5% for red, green and blue sub-pixels, respectively. Also, 34.5%, 30%, and 35% aperture ratios are achieved for red, green, and blue sub-pixels of the 9-inch display, respectively.

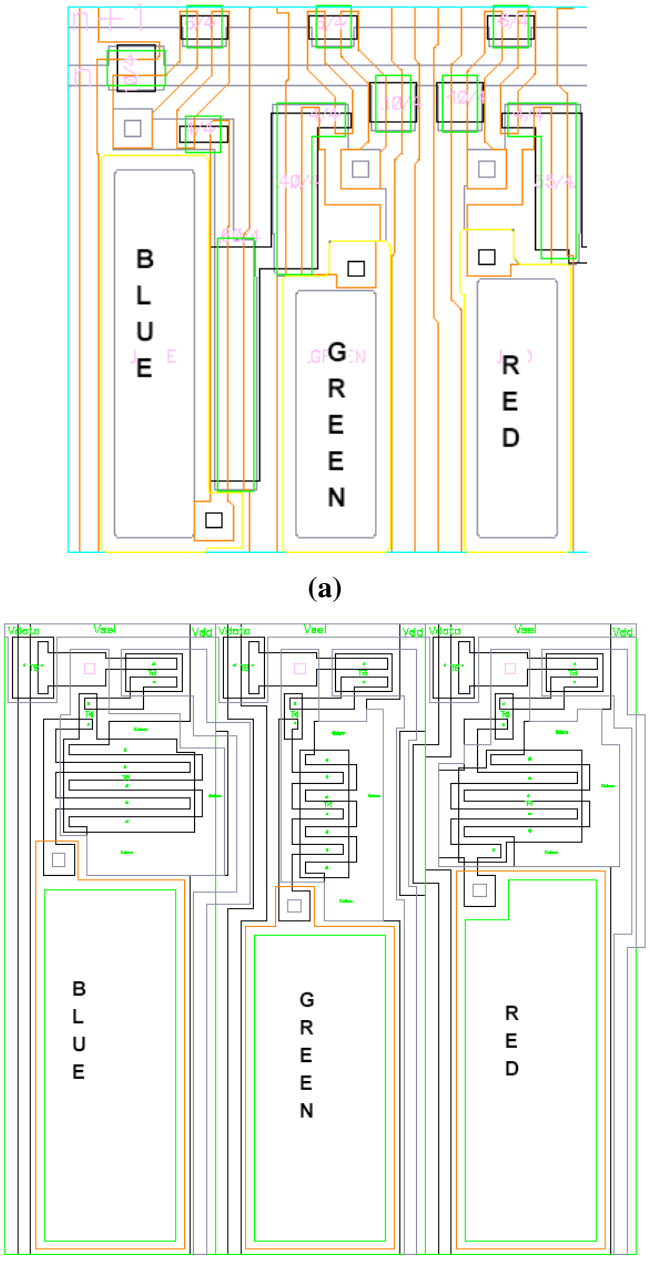
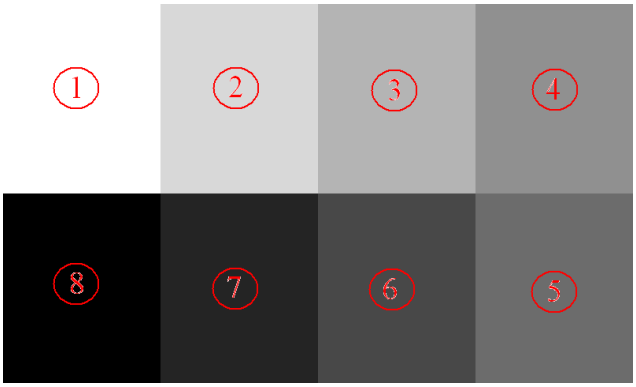
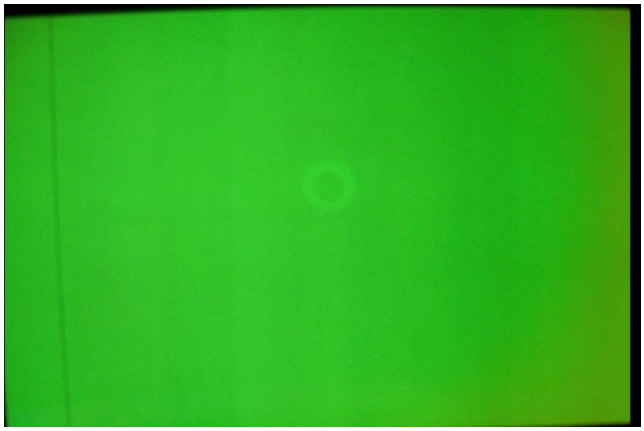


Figure 5.8: RGB pixel layout for (a) 2.2-inch QVGA and (b) 9-inch WXGA displays.

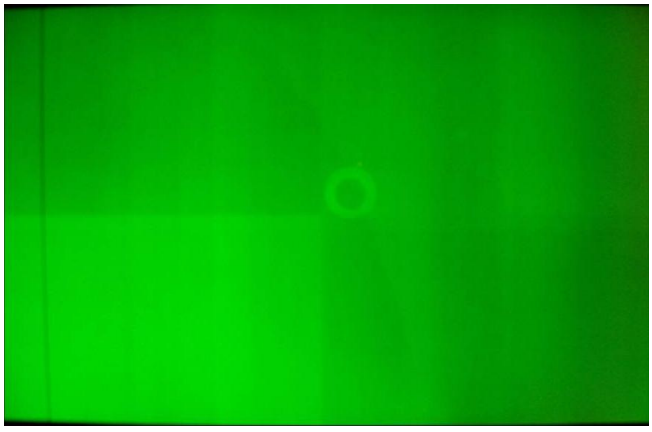
The fabricated display is measured for the differential aging effect using the gray scale pattern, depicted in Figure 5.9 (a). The image sticking issue is obvious in the conventional 2-TFT display whereas the image is clear for the AdMo™ display.



(a)



(b)



(c)

Figure 5.9: (a) gray scale used for 200-hour differential aging measurement along the measurement result for (b) AdMo™ and (c) conventional 2-TFT.

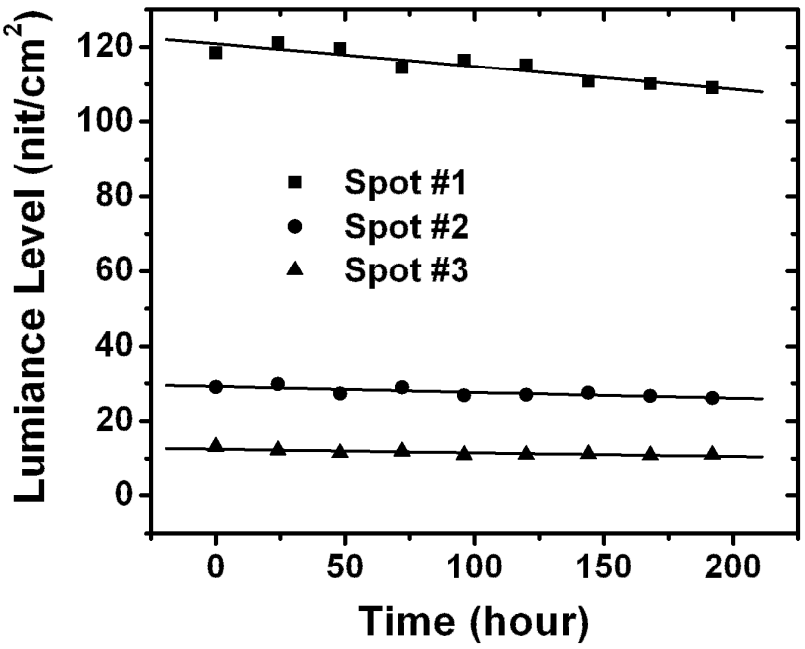


Figure 5.10: Measured luminance stability for different stress levels.

Also, the brightness of each spot shown in Figure 5.9(a) is measured everyday by using a luminance meter (Konica Minolta LS-100). The measured luminance results for the spot numbers 1,3, and 5 are depicted in Figure 5.10. The total error for the maximum stressed part (spot 1) is less than 5% after 200 hours of stress. Since the pixel current is stable, the loss in the brightness can be due to the degradation in OLED brightness.

Figure 5.11 provides two pictures of the display after prolonged operation. Since the aging is more rapid at the beginning of the panel life, the results signify the potential of the new driving scheme in fulfilling the lifetime specs for most applications, in particular for portable devices such as cell phones, digital cameras, and DVD players.

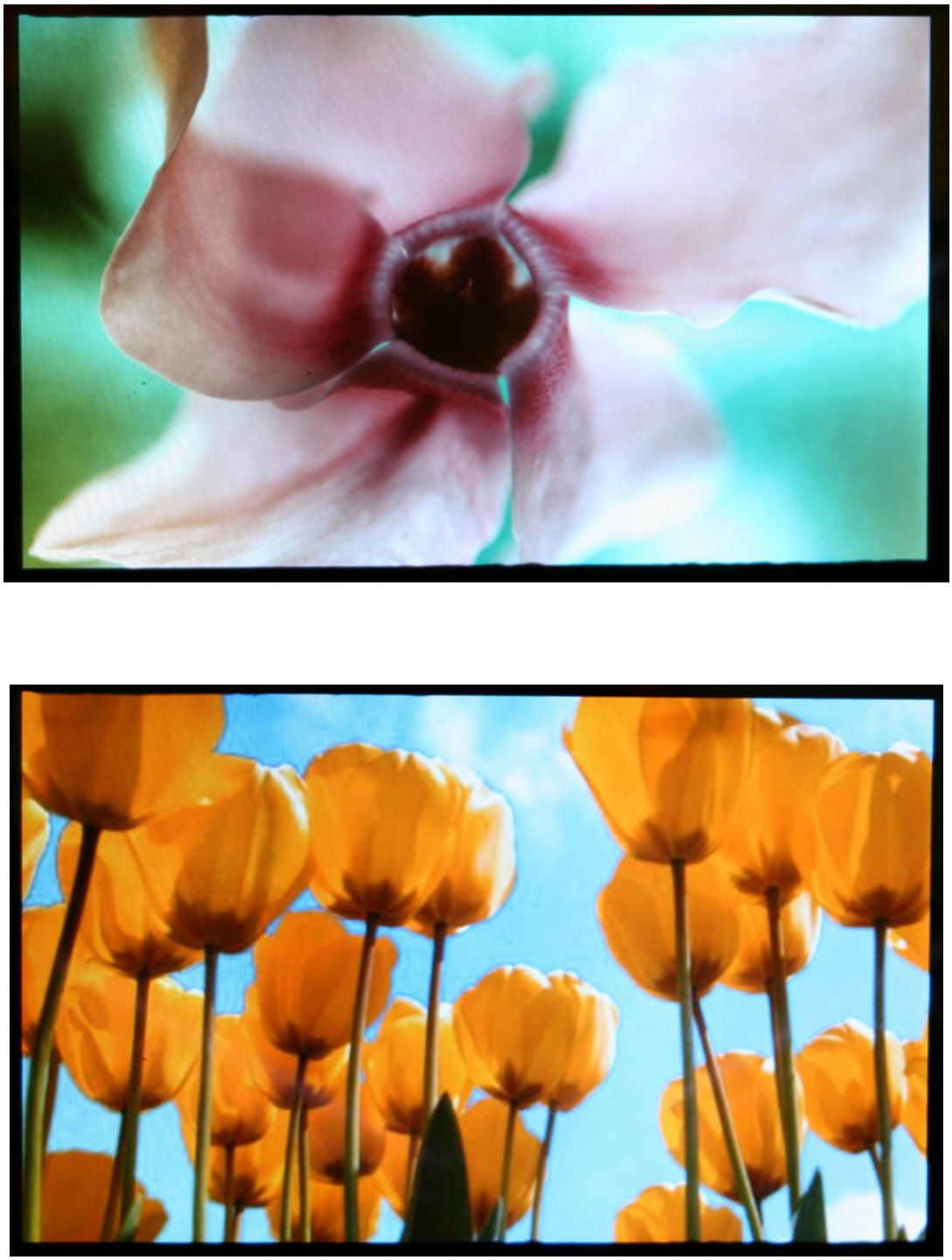


Figure 5.11: Real images from the 9-inch AdMo™ display.

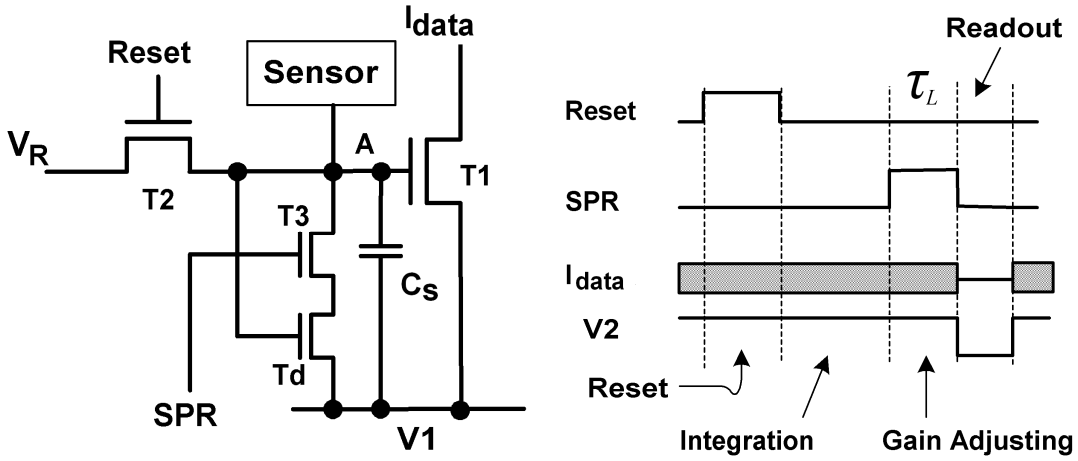


Figure 5.12: Gain-adjustable biomedical imager pixel circuit.

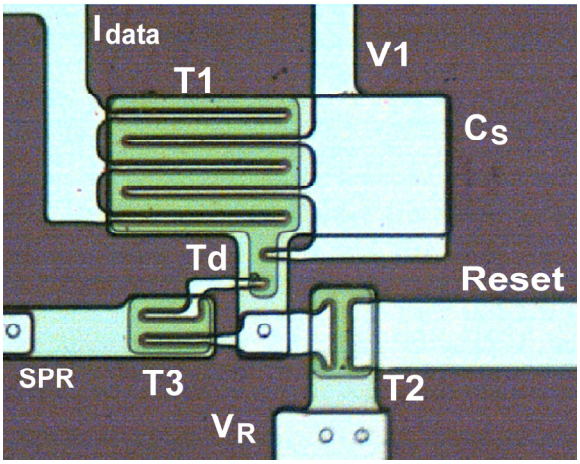


Figure 5.13: Photomicrograph of the gain-adjustable pixel circuit.

5.2 Real-Time Biomedical Imaging Pixel Circuit

The charge-based compensation driving scheme is used in the design of a real-time imager pixel circuit. Not only does the discharging path compensate for the aging and mismatches, but also it adjusts the gain of the pixel for different applications. The pixel circuit and corresponding signal diagram are demonstrated in Figure 5.12. During the reset cycle, node A is charged to a reset voltage (V_R). The next cycle can be the discharging for compensation. However, since the short term stress condition is used for the pixel operation,

Table 5.1: Parameters of the fabricated pixel circuit

Name	Description	Value
$(W/L)_1$	Aspect ratio of T1	180 µm /3 µm
$(W/L)_2$	Aspect ratio of T2	20 µm /3 µm
$(W/L)_3$	Aspect ratio of T3	18 µm /3 µm
$(W/L)_d$	Aspect ratio of T4	4.5 µm /4 µm
C_S	Storage capacitor	350 fF

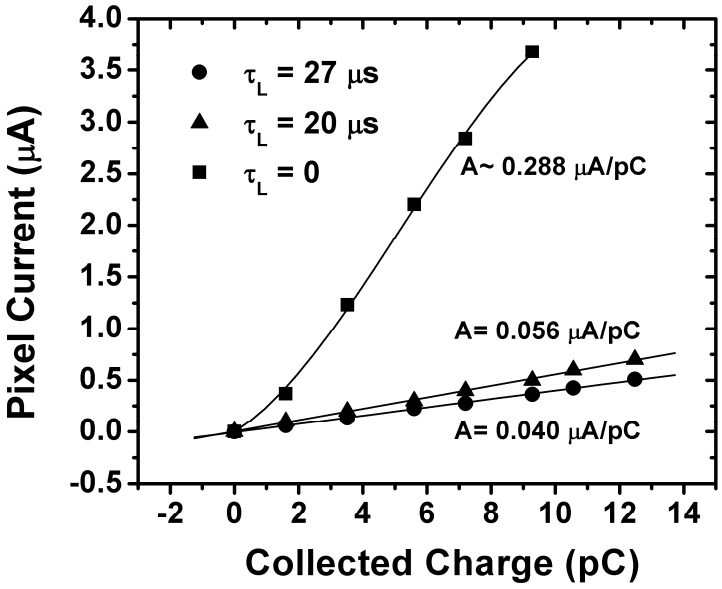


Figure 5.14: Gain-adjustment results using charge-leakage technique.

this cycle is ignored. During the integration, the sensor signal is collected by the storage capacitor. During the gain-adjusting cycle, the voltage of the gate leaks out through Td. Leakage time (τ_L) can be adjusted for different application since it controls the gain of the pixel. During the readout cycle, the pixel current is read through I_{data}. Unlike the hybrid PPS-APS pixel circuit [23], the read operation is not destructive, since the proposed pixel circuit operates only in the active mode.

Based on (5.1), the remaining voltage (V_{dmp}) at node A after the gain adjusting cycle is given by

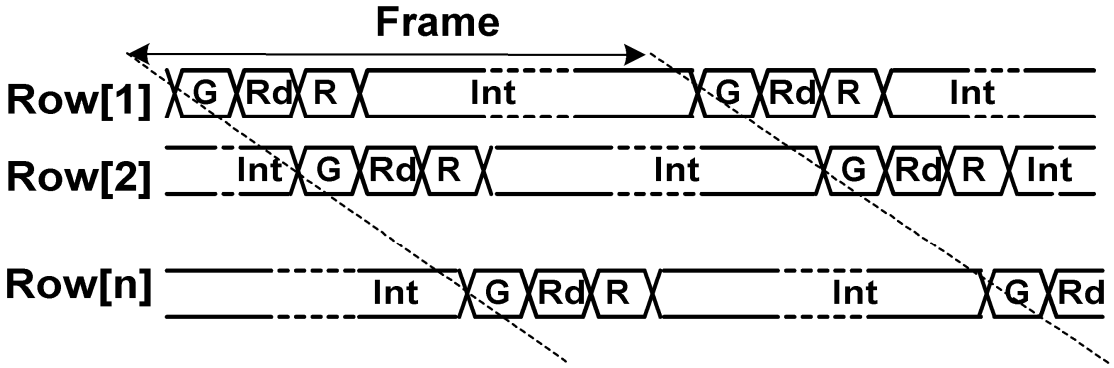


Figure 5.15: Timing schedule for real-time imaging.

$$V_{dmp} = V_R - V_{gen} - \frac{(V_R - V_{gen} - V_T)^2}{(V_R - V_{gen} - V_T) + \tau / \tau_L} \quad . \tag{5.5}$$

Here, V_{gen} is the generate voltage due to the collected charge. By assuming that V_{gen} is much smaller than V_R, the linear approximation is employed to calculate the damping effect (A_{dmp}) as the following:

$$A_{dmp} = \frac{1}{1 + \frac{\tau_L (V_R - V_T)}{\tau}} \quad . \tag{5.6}$$

Figure 5.13 portrays the photomicrograph of the pixel circuit used for the measurement. Measurement result for different leakage time is shown in Figure 5.14. The pixel parameters are listed in Table 5.1. It is obvious that the gain of the pixel can be adjusted for various applications. For example for very low intensity input signals (e.g. fluoroscopy) the leakage time can be close to zero to get the maximum gain. On the other hand the leakage time can be increased (e.g. 27 μs) for higher intensity input signals (e.g. radiology). More importantly, the pixel response to the collected charge is significantly linear.

The pixel circuit can provide for parallel operation of reset and readout cycles for different rows. As a result, it can be used for real-time imaging applications such as

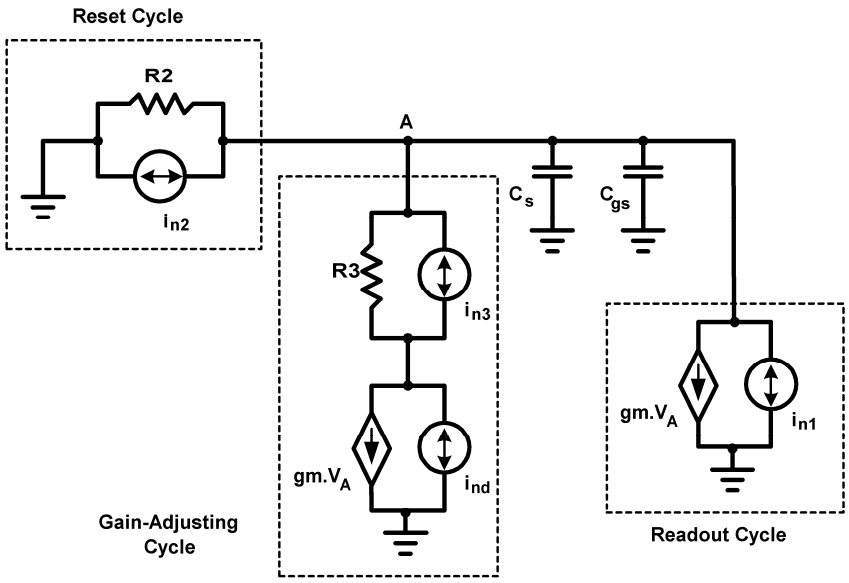


Figure 5.16: Noise model of the pixel circuit during the reset and gain adjusting cycle.

fluoroscopy. Figure 5.15 shows the timing schedule for an array intended for real-time imaging.

5.2.1 Noise Analysis of Charge-Based Pixel Circuit

To investigate the effect of gain-adjusting branch (T3 and Td) on the noise performance of the pixel, the reset noise of the pixel is calculated with and without the path (the gain-adjusting path does not affect the readout cycle). Figure 5.16 shows the noise model used to evaluate the reset noise of the pixel circuit. The reset noise without considering the gain-adjusting branch is given as

$$V_{n\_2T} = V_{n2} = \frac{i_{n2}}{C_T s + 1/R2} \text{ and } C_T = C_s + C_{gs}. \tag{5.7}$$

in which $R2$ and i_{n2} is the channel resistance and noise of T2, respectively.

If the gain adjusting branch is used, the noise of T2 is damped. T2 noise effect can be written after damping based on (5.6)

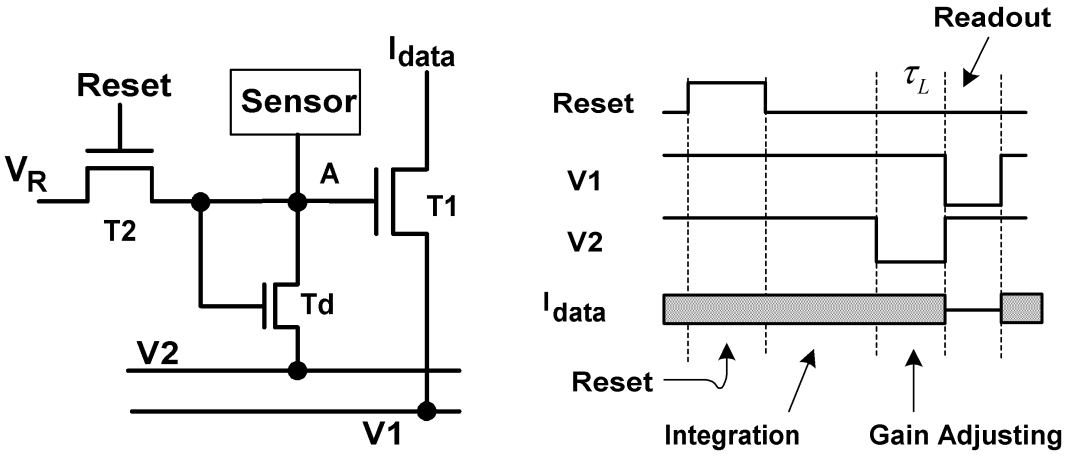


Figure 5.17: 3-TFT gain-adjustable biomedical imager pixel circuit.

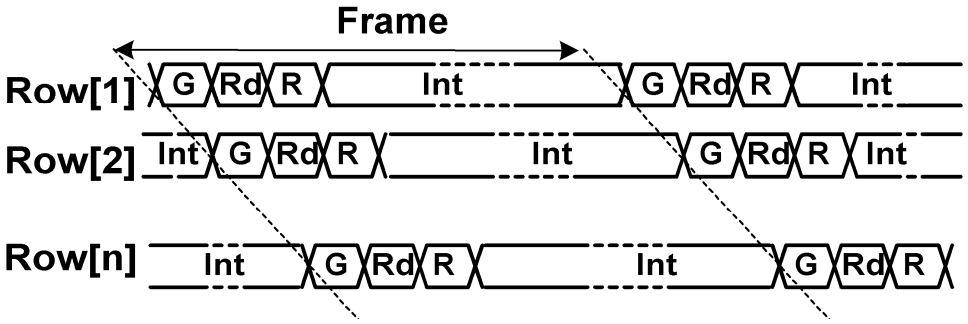


Figure 5.18: Timing schedule for 3-TFTgain-adjustable pixel circuit.

$$V_{n2-dmp} = \frac{i_{n2}}{C_T s + 1/R2} \frac{1}{\left[1 + \frac{\tau_L (V_R - V_T)}{\tau}\right]}. \tag{5.8}$$

Noise of Td is the dominant noise source in the gain-adjusting branch (cascade branch) [94]. Thus, the noise effect of this branch is given as

$$V_{nd} = \frac{i_{nd}}{C_T s + g_{md}}. \tag{5.9}$$

in which g_{md} and i_{nd} is the transconductance and noise of Td, respectively. The total noise of the pixel with gain-adjusting branch is

$$V_{n-dmp} = \frac{i_{nd}}{C_T s + g_{md}} + \frac{i_{n2}}{C_T s + 1/R2} \frac{1}{\left[1 + \frac{\tau_L (V_R - V_T)}{\tau}\right]}. \quad (5.10)$$

Since A_{dmp} can be very small, the noise effect of T2 becomes negligible. Thus, by proper aspect ratio of Td, the noise performance can be almost the same as the one without the gain-adjusting branch.

To improve the resolution, T3 and Td can be merged and also Td can replace the storage capacitor. Figure 5.17 demonstrates the 3-TFT gain-adjustable pixel circuit. Also, the pixel provides a separate path for gain adjusting, reset and readout; thus, the timing schedule can be improved for more parallelism as shown in Figure 5.18. Here, while the pixels in one row are being reset, the next adjacent row's pixels are tuned for the gain, and the row after that is readout. As a result, it can provide for a fast refresh rate suitable for high frame rate real-time imaging.

5.3 Summary

The charge-based compensation driving scheme presented here preserves the cost advantage of a-Si:H technology without increasing the implementation complexity. Moreover, it compensates for the instabilities of the backplane. While the aging error for the conventional 2-TFT pixel circuit is more than 25% for 200 hours of operation, the charge-based compensation pixel circuits is significantly more stable. Moreover, measurement results and analysis reveal that the new driving scheme presented here can control any spatial mismatch and temperature variation without compromising the settling time. The image quality of the 9-inch panel after prolonged continuous operation demonstrates the potential of this driving scheme for different applications.

Also, this technique is adapted in a biomedical imager to adjust the gain for different modalities with different signal intensities. Unlike other proposed high-dynamic range pixel circuit [23], the readout is not destructive. Hence, it enables the use of OTRA for the entire dynamic range including high intensity signals (e.g. radiology). Moreover, since the gain of OTRAs is independent of the readout time (unlike charge-pump amplifiers), it enables faster readout leading to higher frame rate for real-time imaging.

Chapter 6

High Resolution Architectures

For some application such as high resolution AMOLED displays for TV and monitor, and highly sensitive imaging such as radiotherapy, the backplane should compensate for all the effects caused by the aging or mismatches to achieve the intended accuracy (e.g. less than %0.5 differential aging for a TV screen). While the entire proposed driving scheme compensate only for the static effect of V_T-shift (i.e. drop in the pixel current/gain), the transient effects such as charge injection and clock-feed through can cause up to 10% error in the pixel characteristics. To solve this issue, we introduce a calibration technique capable of controlling the transient effects as well as the static effect of the V_T-shift (mismatches).

6.1 Time Dependent Charge Injection and Clock Feed-Through

To compensate for the V_T-shift/mismatch, the compensation techniques [51, 54] lead to a modification in the gate voltage of the drive TFT to provide a constant overdrive voltage. However, as a consequence of this change in the gate voltage, clock feed-through and charge injection associated with the parasitic capacitances change overtime. Since the storage capacitor cannot be large due to the mandated frame time and aperture ratio, the parasitic capacitances stemming from the overlap of the gate over the drain and source become comparable. Moreover, the threshold voltage of the switch TFTs decreases since they are under negative bias stress during most of the frame time [45]. Consequently, the charge

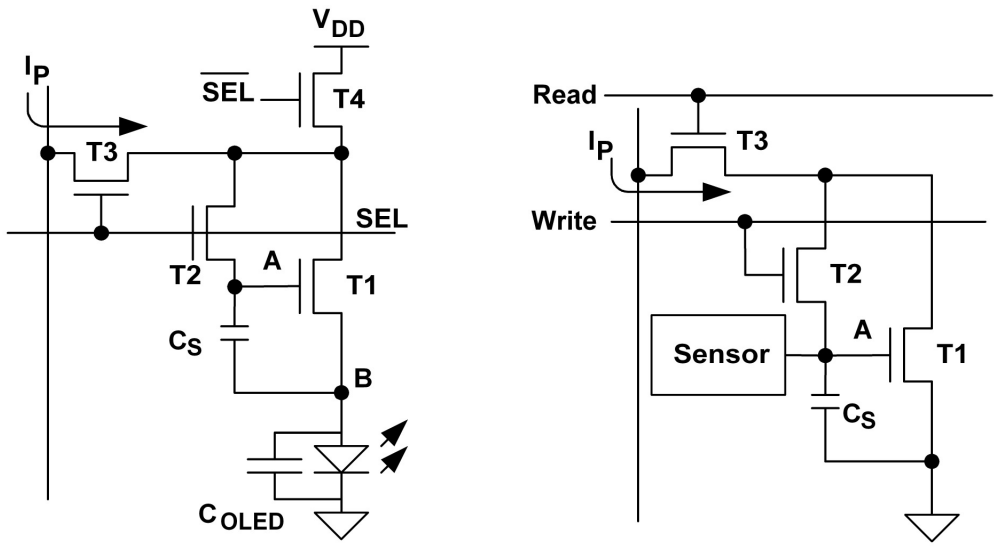


Figure 6.1: Gate-programmed pixel circuit for (a) AMOLED display [59] and (b) APS [96].

profile of their channels changes for a given programming voltage inducing a time dependent error.

The transient shifts including charge injection and clock feed-through can either increase or deceases the pixel current overtime depending on the circuit topology and driving scheme. The two most probable topologies used in the design of pixel circuits, in particular for AMOLED displays, are gate-programmed (GP) and source-programmed (SP) [95]. Figure 6.1 demonstrates two GP pixel circuits for AMOLED and APS applications, respectively. In the GP pixel circuits, the source voltage is fixed and the gate voltage changes during the programming cycle. Whereas, in the SP pixel circuits, the gate voltage is fixed and the source voltage changes during the programming cycle.

In the GP pixel circuits shown in Figure 6.1, a programming current (I_P) flows through the switches T3 and T2, adjusting the gate voltage of T1 to $V_{OLED}+V_P+V_{T1}$ for the AMOLED pixel and V_P+V_{T1} for the APS pixel circuit, where V_P is $(I_P/K)^{1/2}$ and K the gain coefficient in

the I-V characteristic TFTs. The transient shifts in the gate voltage of the GP pixel circuit is given by

$$\Delta V_{gp} = -\frac{C_{g2}}{2 \cdot C_S}(V_H - V_{T2} - V_{g1}) - \frac{C_{ov2}}{C_S}(V_H) + \frac{C_{ov1}}{C_S}(V_{DD-eff} - V_{g1}) \tag{6.1}$$

where C_{g2} is the gate capacitance of T2, C_S the storage capacitor, V_H the ON voltage of switch TFTs (OFF voltage is assumed to be zero), V_{T1} and V_{T2} the threshold voltage of T1 and T2, respectively, and V_{g1} the gate voltage if T1 which is $V_{OLED}+V_{T1}+V_P$ for Figure 6.1 (a) and $V_{T1}+V_P$ for Figure 6.1 (b). Here, C_{ov1} and C_{ov2} are the overlap capacitances of T1 and T2, respectively, and $V_{DD\text{-}eff}$ is the effective voltage at the drain of T1 during the driving cycle (in AMOLEDs, $V_{DD\text{-}eff} = V_{DD} - V_{DS4}$) or the readout cycle (in APSs, $V_{DD\text{-}eff}$ is a biasing voltage). The time dependence of (6.1) can be calculated as

$$\begin{aligned} \frac{d}{dt}\Delta V_{gp} &= K_1 \frac{\partial}{\partial t} V_{T1} + K_2 \frac{\partial}{\partial t} V_{T2} + K_3 \frac{\partial}{\partial t} V_{OLED} \\ K_1 &= \frac{\partial}{\partial V_{T1}} \Delta V_{gp} = \frac{1}{2 \cdot C_S}(C_{g2} - 2 \cdot C_{ov1}) \\ K_2 &= \frac{\partial}{\partial V_{T2}} \Delta V_{gp} = \frac{C_{g2}}{2 \cdot C_S} \\ K_3 &= \frac{\partial}{\partial V_{OLED}} \Delta V_{gp} = \begin{cases} \frac{1}{2 \cdot C_S}(C_{g2} - 2 \cdot C_{ov1}) & \text{Figure 6.1 (a)} \\ 0 & \text{Figure 6.1 (b)} \end{cases} \end{aligned} \tag{6.2}$$

According to (6.2), the current of the GP pixel circuits increases as it ages. Moreover, the major effect is due to C_{g2}, which is representative of charge injection component. Figure 6.2 displays the effect of transient shifts on the current (I_{pixel}) of the GP pixel circuit in Figure 6.1 (a). Cadence and a model presented by Servati [52] are used for the simulations unless a different simulator is noted. Clearly, the transient shifts include a fix offset, and a time

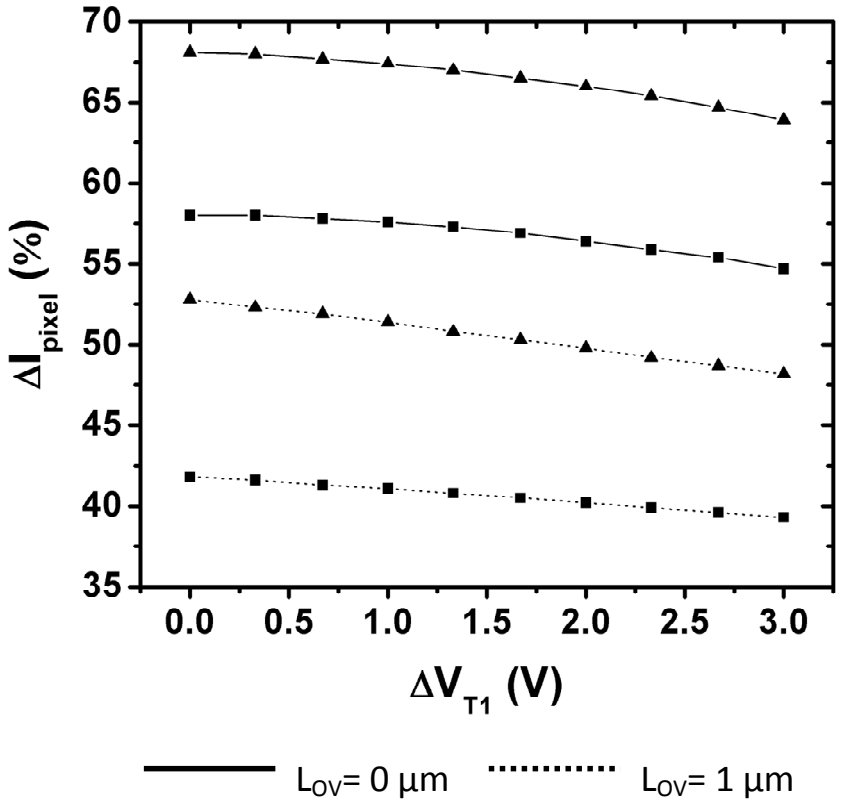
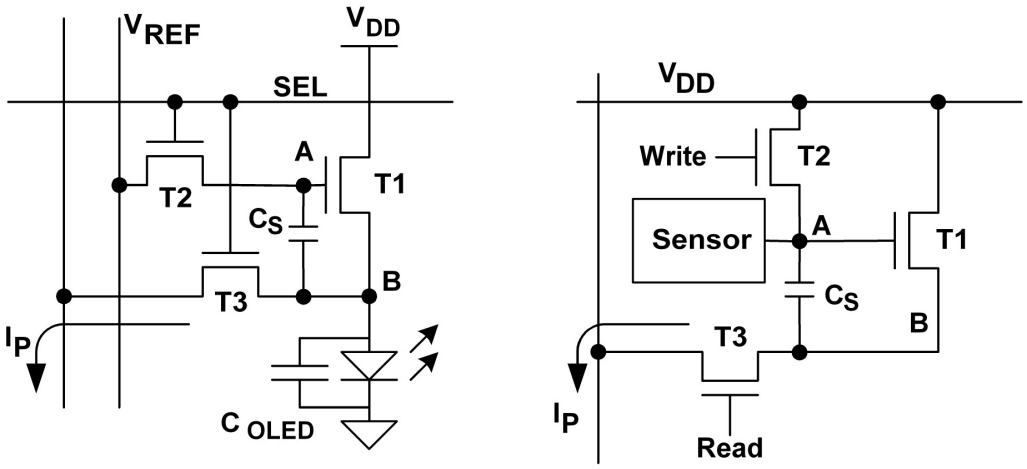


Figure 6.2: Effect of charge injection and clock feed through on the current of the GP pixel circuit for W_{T2}=100 µm (squares) and W_{T2}=120 µm (triangles).

dependent component. Since increasing the width of T2 (W_{T2}) results in a larger parasitic capacitance, a larger T2 boosts both components of the transient effects. As indicated in (6.2) and Figure 6.2, the charge injection and clock feed-through components can compensate each other. Thus, the transient effects can be controlled significantly by increasing C_{ov1}, properly.

In the SP pixel circuits, demonstrated in Figure 6.3, a programming current (I_P) flows from T2, and adjusts the source voltage of T1 to V_{REF}-V_P-V_{T1}. Here, V_{REF} is the gate voltage of T1 during the programming cycle. The transient shifts in the gate voltage of the SP pixel circuit is given by [100]



(a) **(b)**

Figure 6.3: Source-programmed pixel circuit for (a) AMOLED display [97] and (b) APS [96].

$$\Delta V_{ch-sp} = -\frac{C_{g2}}{2 \cdot C_S}(V_H - V_{T2} - V_{REF}) - \frac{C_{ov2}}{C_S}(V_H + V_{OLED} + V_{T1}) - \frac{C_{ov1}}{C_S}(V_{SS-eff} + V_{T1}) \qquad (6.3)$$

where C_{ov2} is the overlap capacitances of T2, and $V_{SS\text{-}eff}$ the effective voltage at the source of *T1* during the driving cycle (in AMOLEDs, $V_{SS\text{-}eff} = V_{OLED}$) or the readout cycle (in APS, $V_{SS\text{-}eff}$ is a biasing voltage). The time dependence of (6.3) can be calculated as

$$\begin{aligned}
\frac{d}{dt}\Delta V_{sp} &= K_1 \frac{\partial}{\partial t} V_{T1} + K_2 \frac{\partial}{\partial t} V_{T2} + K_3 \frac{\partial}{\partial t} V_{OLED} \\
K_1 &= \frac{\partial}{\partial V_{T1}} \Delta V_{sp} = -\frac{1}{C_S}(C_{ov1} + C_{ov2}) \\
K_2 &= \frac{\partial}{\partial V_{T2}} \Delta V_{sp} = \frac{C_{g2}}{2 \cdot C_S} \\
K_3 &= \frac{\partial}{\partial V_{OLED}} \Delta V_{sp} = \begin{cases} -\dfrac{1}{C_S}(C_{ov1} + C_{ov2}) & \text{Figure 6.3 (a)} \\ 0 & \text{Figure 6.3 (b)} \end{cases}
\end{aligned} \qquad (6.4)$$

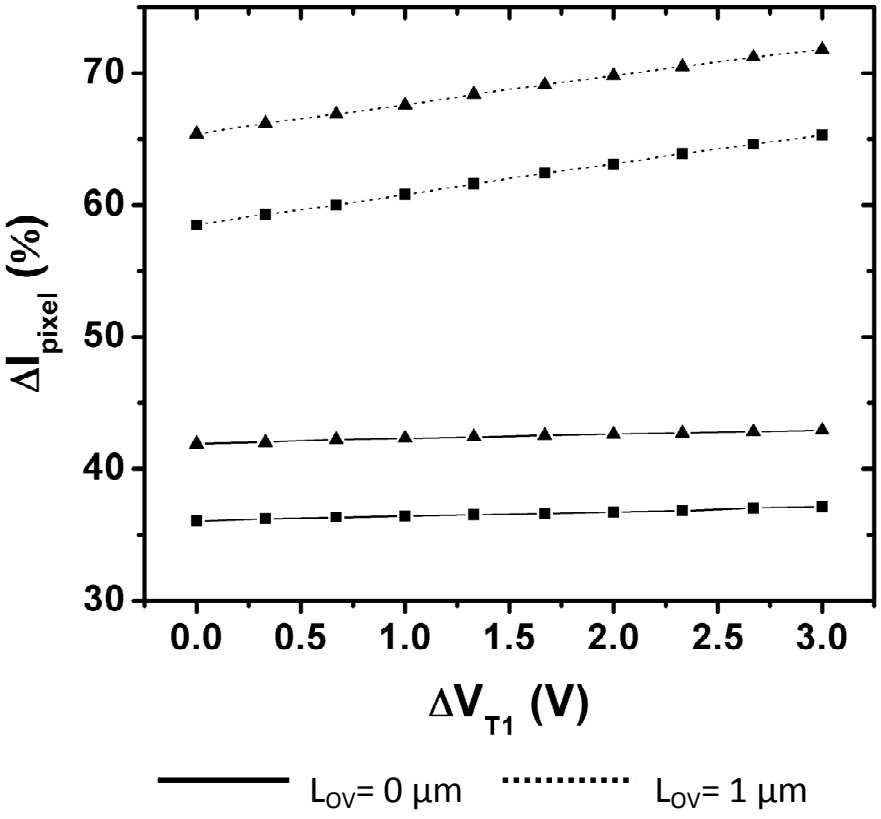


Figure 6.4: Effect of charge injection and clock feed through on the current of the SP pixel circuit for W_{T2}=100 µm (squares) and W_{T2}=120 µm (triangles).

According to (6.4), the current of the SP pixel circuit decreases as it ages. Unlike the GP pixel circuit, the dominant time-dependent component stems from the overlap capacitance. However, the V_{T2}-dependent part of the transient shifts is the same for both GP and SP pixel circuits. Simulation results for Figure 6.3 (a) are depicted in Figure 6.4 highlighting the impact of transient shifts on the current of the SP pixel circuit. Table 6.1lists the parameters used in the simulations. Although increasing the width of T2 increases the fixed offset, its affect on the time dependent component is negligible since T1 is much larger than T2 and so its overlap capacitance (C_{OV1}) is dominant. Moreover, as is predicted by (6.4), if the overlap capacitances are zero, the time-dependent component of the error becomes zero.

Table 6.1: Parameters of GP, SP, and 3-TFT step-calibration pixel circuits used in simulations and measurement

Name	Description	Values
W/L(T1)	Size of T1	400/23
W/L(T2)	Size of T2	100/23
W/L(T3)	Size of T3	100/23
W/L(T4)	Size of T4	400/23
W/L(T_{OLED})	Size of T4	750/23
C_S	Storage capacitance	2 pF
C_{OLED}	OLED capacitance	5 pF
I_P	Programming current	1 μA

Even though, most of compensating schemes proposed to date try to compensate for the DC shift in V_T, the previous analysis shows that the transient shifts stemming from the charge injection and clock feed-through can induce significant error in the pixel current. Following the analysis, the dynamic effects can be reduced by using either a larger storage capacitor or a smaller switch TFT. However, the size of switch TFT determines the settling time [17], and the size of storage capacitor is limited by the aperture ratio and pixel area.

6.2 Successive Calibration

The V_T-shift (ΔV_T) in the a-Si TFT under constant current stress is given by [47]

$$\Delta V_T = \frac{\left(\frac{I_{DS}}{K}\right)^{\frac{\gamma}{\alpha}}}{(1+1/\alpha)^{\gamma}}\left(\frac{t}{t_0}\right)^{\beta} \tag{6.5}$$

where, I_{DS} is the current in the TFT, K and α are the gain and power parameters in the TFT I-V characteristic, respectively, β the power law index of hydrogen escape rate, and γ the

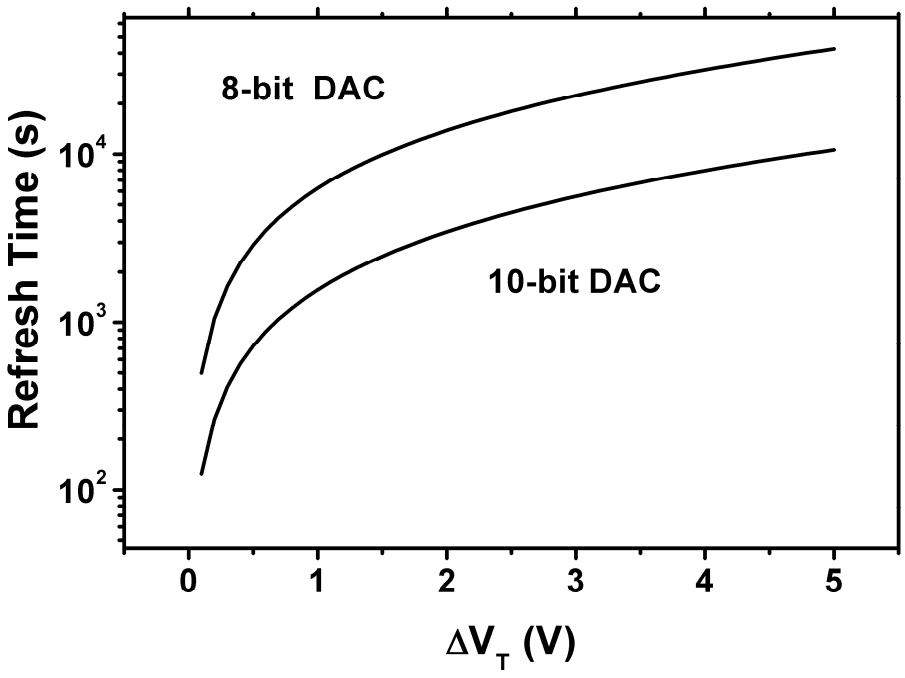
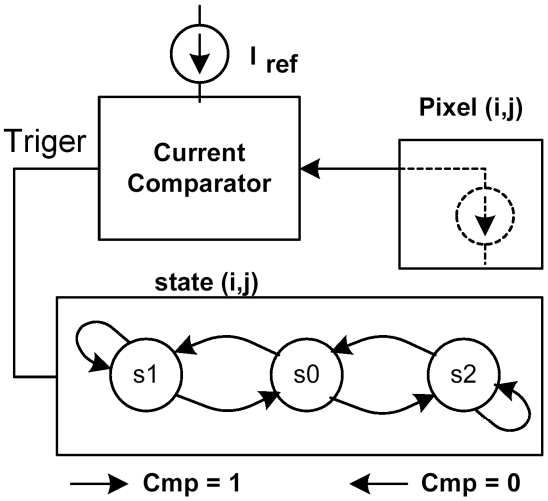


Figure 6.5: The maximum refresh time for digital calibration.

power parameter relating dangling bond creation to the band tail states [45]. Assuming that the maximum achievable accuracy of the system is set by the digital to analog converters (DACs) of the source driver, the refresh time of any individual pixel must be smaller than the time required for the V_T-shift to become larger than a voltage-step of the driver DAC. Thus, using the linear approximation around ΔV_T, the maximum refresh time can be written as

$$t_r = \frac{V_S\left(\frac{t_\Delta}{t_0}\right)}{\beta \Delta V_T} \tag{6.6}$$

Here, V_S is a voltage step of the driver DAC, t_Δ the corresponding time of ΔV_T, and t_r the maximum refresh time. The simulation results for two different driver DACs are shown in Figure 6.5. For γ, β, α, and t_0, the values listed in [47] are used and the aspect ratio of the TFT



$$if\ \ state(i,j) = s1 \qquad V_{cal}(i,j) = V_{cal}(i,j) - V_s$$
$$if\ \ state(i,j) = s2 \qquad V_{cal}(i,j) = V_{cal}(i,j) + V_s$$

Figure 6.6: Digital calibration using a single-bit current comparator.

is set to 400 μm/ 27 μm with a mobility of 0.5 cm^2/Vs and I_{DS}=1.5 μA. It is clear that the refresh time is larger than 100 s, and it increases as the TFT ages. Also, the non-linear part of the curves can be avoided by pre-stressing the TFT, to get a slower refresh rate. Moreover, Figure 6.5 signifies that the V_T-shift is a very slow process. Thus, by knowing the previous V_T, a single-bit ADC can follow the aging to acceptable accuracies. To do so, the pixel is programmed with a voltage as

$$V_{ref}(i,j) = V_{ref0} + V_{cal,n-1}(i,j). \tag{6.7}$$

in which, $V_{ref}(i,j)$ is the reference voltage of the pixel at the i^{th} row and j^{th} column and $V_{cal,n-1}(i,j)$ the previous calibration voltage of pixel (i,j). Then, the current of each pixel is compared with a reference current, which can be the current of a reference pixel that is not under stress thus remaining stable. The calibration voltage is updated based on the state machine shown in Figure 6.6. Unlike the successive approximation ADC [98], the calibration

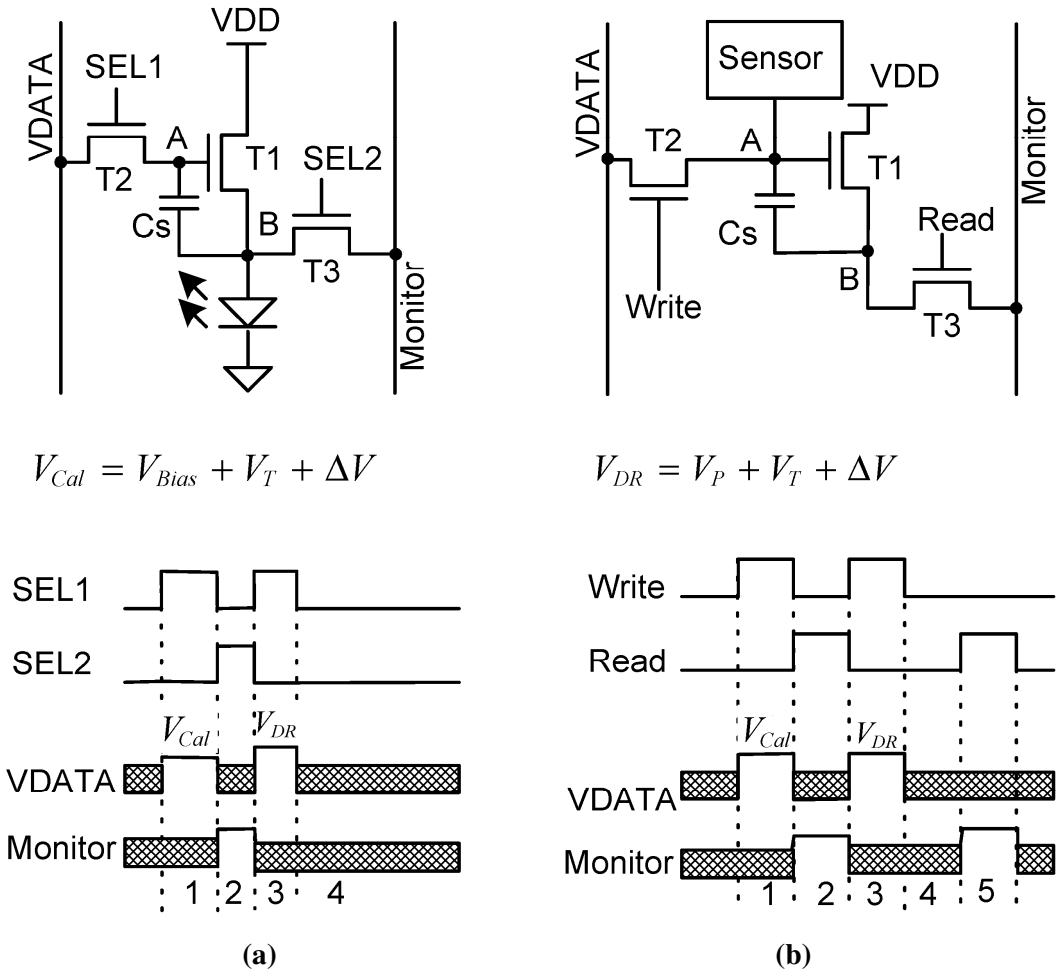


Figure 6.7: (a) 3-TFT AMOLED and (b) AMI pixel circuits for the step-calibration driving scheme.

voltage of each pixel is updated by only one step voltage (V_S) during each calibration turn. If Cmp is one (the estimated V_T is smaller than the real V_T), state machine goes to *S1*. If Cmp is zero (estimated V_T is bigger than the real V_T), the state machine goes to *S2*. The small refresh time for the display ensures that the driver does not lose any aging data. For example, to calculate the refresh time, we assume that there is a comparator for each display column. During the blanking time (of the order of 500 μs) which is the free time at the end of a frame, we can extract the aging of at least 10 rows considering that the programming of each row

with a reference voltage takes less than 20 μs. Hence, the refresh time for a high definition display (1920xRGBx1080) with a 60 Hz frame rate is around 2 s which is much smaller than the needed 100 s.

Moreover, this technique can resolve any offset associated with the source driver since the offset has the same effect as the V_T-shift. Also, to control the offset associated with the current comparator and reference current, one can calibrate all the comparators and reference pixels with a fixed current at the beginning. For this calibration, the pixel current is replaced with a fixed current and the same algorithm shown in Figure 6.6 is used to calibrate the comparator and reference pixel circuits. Thus, V_{ref0} in (6.7) is replaced with $V_{ref0}(j)$, which is for the comparator at the j^{th} column. To avoid increasing the source driver size, the state machine can be implemented as a firmware at the controller. To pass the results of the comparators to the controller, the shift register chain that exists in the source driver for writing the row data can be used. However, the remaining issue is the size of comparators that can result in a significant increase in the die area. Figure 6.7 displays two pixel circuits based on the step-calibration driving scheme applied to AMOLED displays and APSs. Here, the pixel current is observed through the Monitor line to extract the shift in V_T of T1.

The step-calibration proposed in Figure 6.6 benefits from simple implementation but it does not follow abrupt changes in the V_T. While the V_T shifts gradually due to aging, it changes sharply due to temperature variations. Thus, for applications in which the temperature varies abruptly, a new driving scheme is required. A modified version of the step-calibration presented here that can follow any sharp variation in V_T. To improve the algorithm, two gain stages are added to the state machine (see Figure 6.8). When the system is in state *E*, the previous extract V_T, $V_T(i,j)$, is applied to the pixel in the i^{th} row and j^{th}

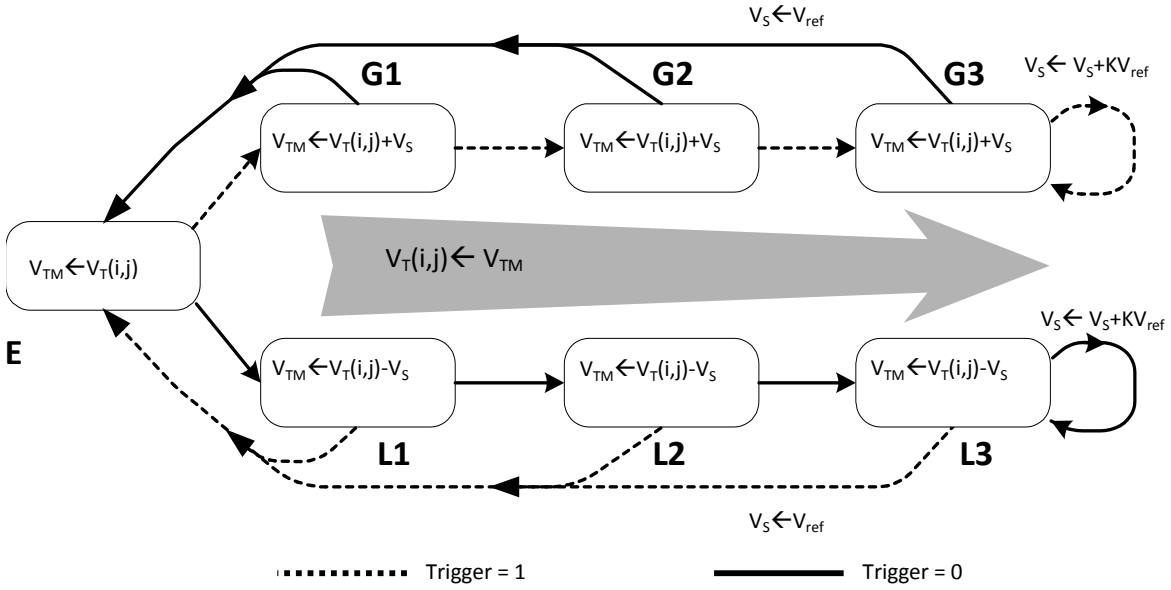


Figure 6.8: State diagram used for gained step calibration.

column. If the Trigger is zero, the system changes its state to G1, which means the actual V_T is larger than $V_T(i,j)$. At the state G1, the predicted V_T is increased by V_S. The states G2 and G3 operate similarly as G1. The only difference is that state G2 changes the operational mode to G3 if Trigger is zero, and state G3 increases V_S intelligently to expedite the extraction of V_T-shift. States L1, L2, and L3 are the counterparts of G1, G2, and G3 for negative V_T-shift and are used when the actual V_T is smaller than the previously calculated one. Simulation results for the number of required iterations to extract the different V_T-shifts are depicted in Figure 6.9. While the number of iterations increases linearly using the algorithm of Figure 6.6, the gained algorithm reduces the required number of iteration significantly.

The proposed driving scheme inherently cancels the offset associated with the different components including drivers, pixel circuits, and up to the current comparator. Figure 6.10 shows simulation results for the conventional 2-TFT and the 3-TFT step-calibration pixel

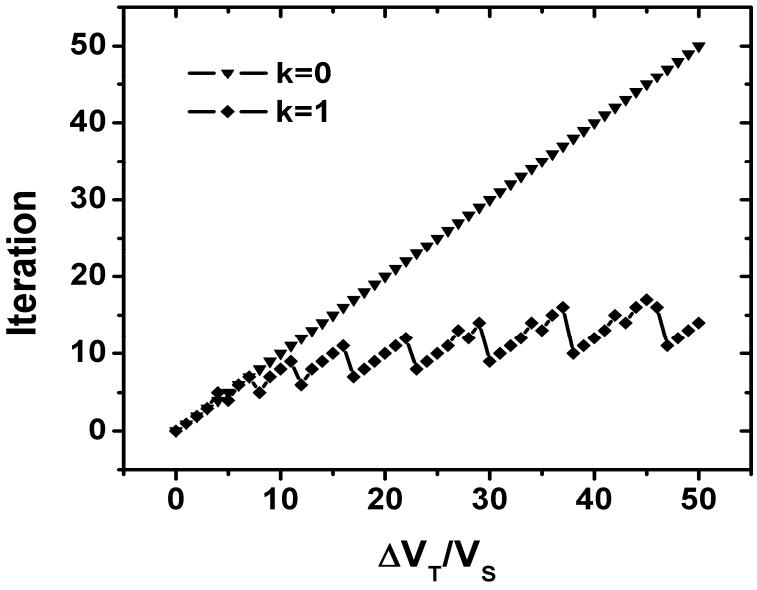


Figure 6.9: Number of iterations required for detecting ΔV_T.

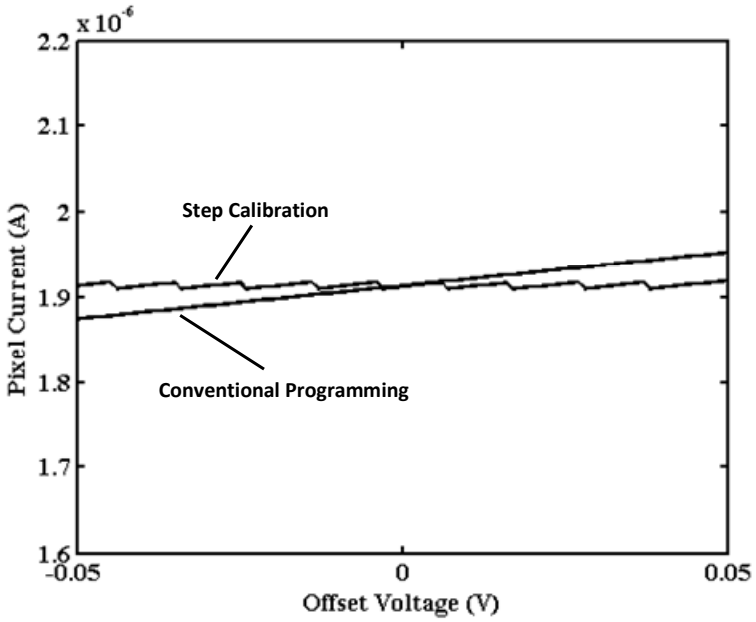


Figure 6.10: Effect of driver offset on the pixel current.

circuits. While the error in the pixel current due to 0.1 V offset is over 5% for the conventional 2-TFT, it is around 0.5% for the new driving scheme.

6.3 Arrays Structure and Timing

Figure 6.11 (a) presents the integration method for the new pixel circuit along with the required blocks. The extraction procedure occurs in two different stages of device lifetime. First, the panel is put under calibration after fabrication and the data is stored inside the extraction memory. At this stage, timing is not an issue since the normal operation of the display is halted. The second calibration is performed during the normal operation of the display. Here, the calibration should be done without affecting the frame rate and timing of the display during normal operation. Thus, the extraction can be done in two different ways: blanking-time or simultaneous extraction.

6.3.1 Blanking-time extraction

As Figure 6.11 (b) shows, only one extraction procedure occurs during a frame time and the V_T extraction of the pixel circuits in the same row is performed at the same time. Therefore, the maximum time required to refresh a frame is

$$\tau_F = n \cdot \tau_P + \tau_E . \tag{6.8}$$

Here, τ_F is the frame time, τ_P the time required to write the pixel data into the storage capacitor, τ_E the extraction time, and n the number of rows in the display. In normal operation, assuming $\tau_E = m.\tau_P$, the frame time can be rewritten as

$$\tau_F = (n + m)\tau_P . \tag{6.9}$$

Following (6.9), there will be $m \cdot \tau_P$ blanking time at the end of each frame that can be used for calibration. For example, for a QVGA display (240x320) with a frame rate of 60Hz, if $m=10$, the programming time of each row is 66 µs, and the extraction time is 0.66 ms.

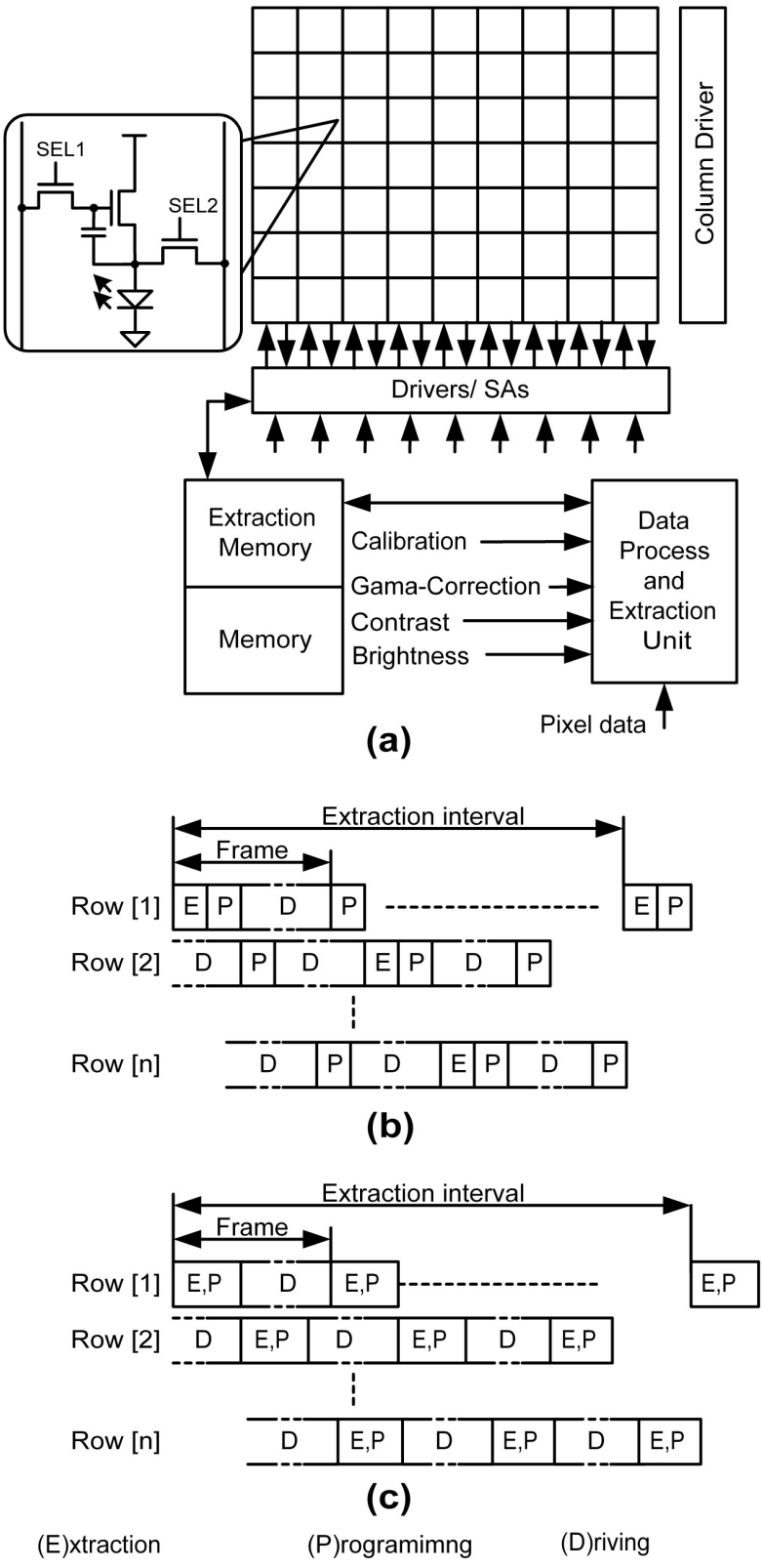


Figure 6.11: Arrays structure and proposed timing for calibration.

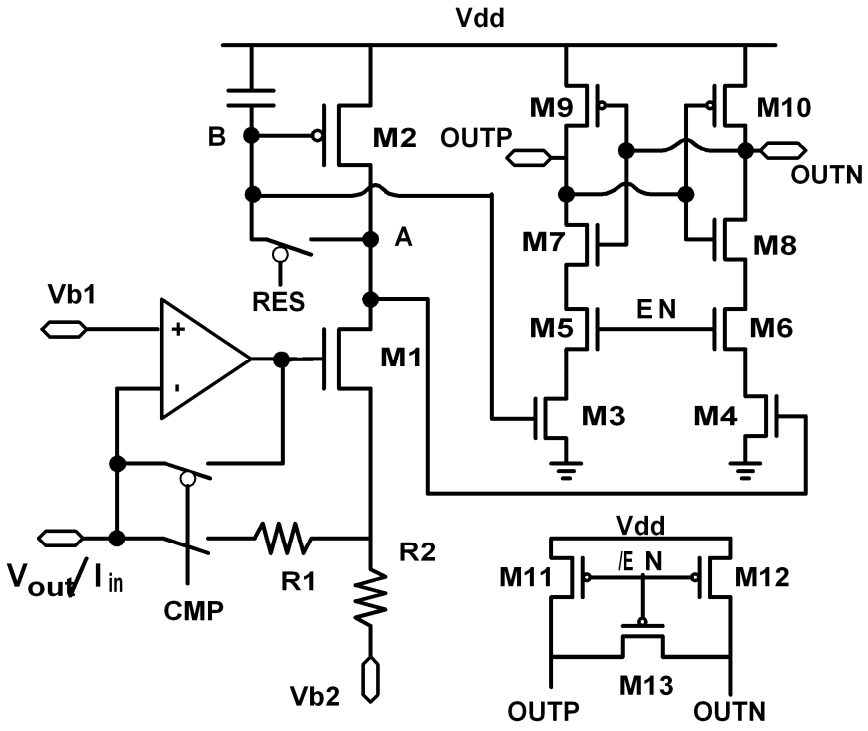
Here, the reference current is duplicated for each pixel at the row using a current mirror. Thus, the reference current sources do not occupy too much area.

6.3.2 Simultaneous extraction

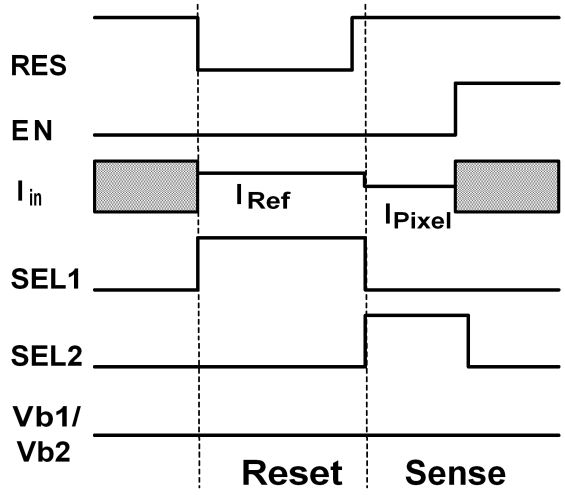
Another method is simultaneous extraction in which the extraction can be performed during the programming cycle (see Figure 6.11 (c)). In this case, the pixel current is compared to a programming current instead of a fixed reference current. Therefore, the frame time is $n \cdot \tau_P$, which fits in the timing budget of large-area displays easily. In this case, it is hard to duplicate the current using a current mirror since the reference current is different for each pixel. Thus, a complicated programmable current source is required at each comparator to provide the reference current. To reduce the number of programmable current sources at the source driver IC, the extraction occurs for one or few columns at each frame time, and so the current sources are shared between the pixels.

6.4 Configurable Current Comparator

Figure 6.12 (a) shows a configurable current comparator [99], which operates as the output buffer and current comparator. To act as an output buffer, Vb1 which is connected to the corresponding DAC at the source driver has the pixel luminance data, Vb2 is Vdd, and CMP is zero. Therefore, the pixel is programmed through the V_{out}/I_{in} port. For comparing the current, CMP is one, and V_{out}/I_{in} port conveys the reference and pixel currents to the current comparator. To improve the comparator resolution, the input current is amplified by *(R1+R2)/R2*. Since the ratio of these resistors is important, their value can be low, thus reducing the input referred noise and die area. The signal diagram of Figure 6.12 (b) is used to test the operation of the comparator.



(a)



(b)

Figure 6.12: (a) Configurable current comparator and (c) signal diagram for comparator operation.

During the reset cycle, the current of a reference pixel, which is programmed by $V_{ref0}(j)$, is conveyed into the current comparator. As a result the gate voltage of M2 is self-adjusted to allow the reference current to pass. The internal nodes of the latch (M3-M12) are also set to Vdd. During the sense cycle, the normal pixel circuit is connected to the current comparator through monitor port of the pixel and Vout/Iin port of the current comparator. Therefore, the change in the voltage at node A (ΔV_A) can be written as

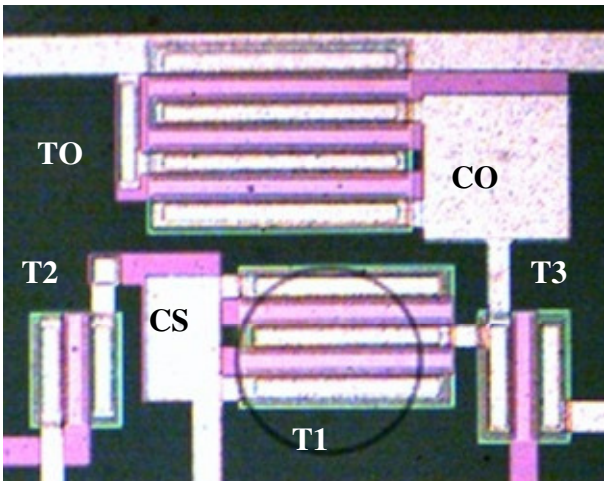
$$\Delta V_A = \frac{R1 + R2}{R2} r_{o2}(I_{ref} - I_{pixel}) . \quad (6.10)$$

Here, r_{o2} is the output resistance of M2. Then, the latch is activated and its state changes according to the difference between voltages at nodes A and B. The output of the latch can be used to adjust the calibration voltage.

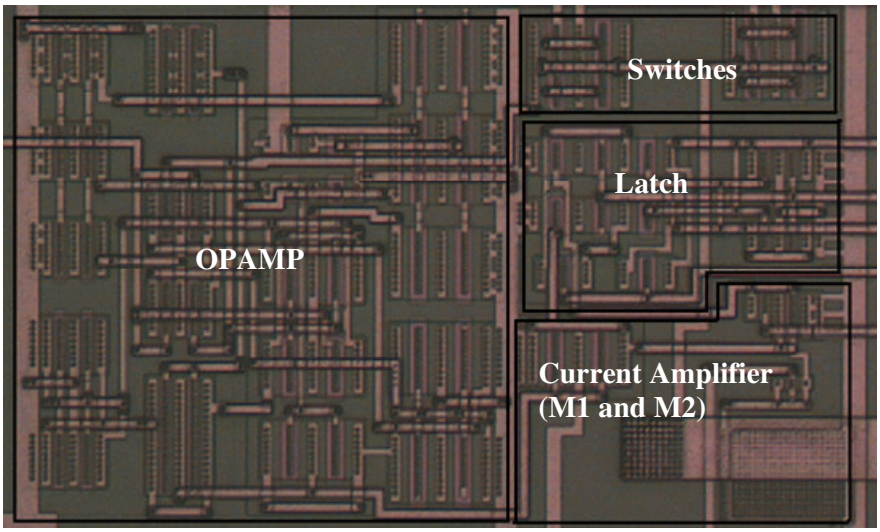
During normal operation, the gate voltage of T1 is charged to $V_P+V_{T0}+\Delta V_T$ where V_P is the programming voltage and V_{T0} the initial threshold voltage of T1. Then T2 is turned off thus affecting the gate voltage of T1 by charge injection [84]. The effect of charge injection (ΔV_2) of T2 on the gate voltage of T1 can be written as

$$\Delta V_2 = -\frac{C_{gs2}}{2C_S}(V_H - V_P - V_{T0} - \Delta V_T) . \quad (6.11)$$

Here, V_H is the ON voltage of SEL1. Thus, as ΔV_T increases, the magnitude of ΔV_2 reduces. As a result the voltage remains on the gate of T1 after turning of T2 increases, and so the pixel current increases. However, If T2 of the normal pixel circuit turns off during the sense cycle, the comparator will compare the pixel current affected by charge injection, and so this effect can be compensated by calibration. This is further explained in the next section by measurement results.



(a)



(b)

Figure 6.13: Photomicrograph of (a) fabricated pixel circuit and (b) configurable current comparator.

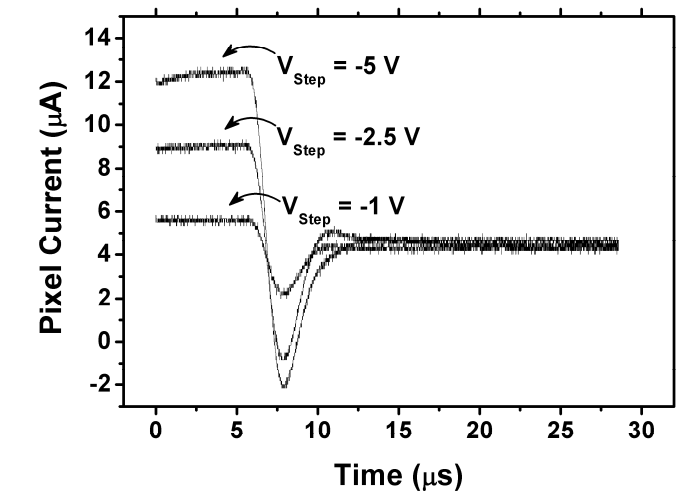
6.5 Measurement Results and Discussions

Figure 6.13 shows the photo-micrograph of the fabricated pixel circuit and the current comparator in amorphous silicon and 0.8-μm high voltage CMOS technologies, respectively. The diode connected transistor TO and the capacitor CO in the pixel emulates the OLED. A micro controller (PIC16F628) is used to implement the firmware and to generate the signals.

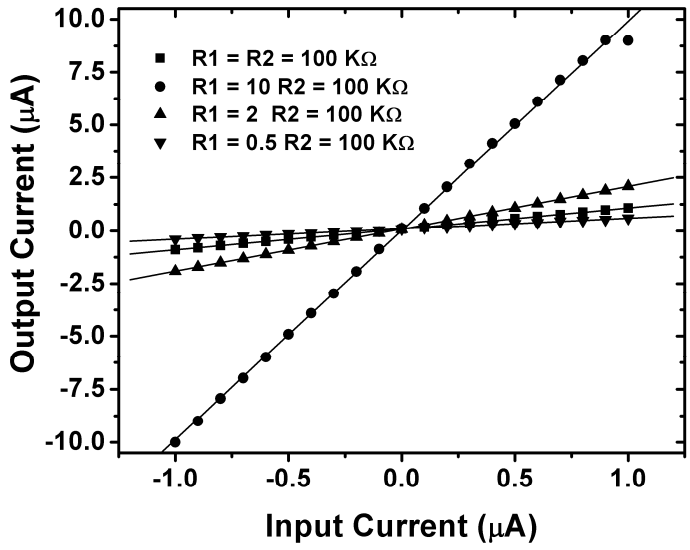
Also, level shifters are used for converting the low-voltage signals to high voltage signals. The Vdd and Vss of the current comparator are 18 V and 0V, respectively, while Vdd and *Vss* of the pixel are 10 V and -10 V. Vb1 and Vb2 are set at 10 V (Vb1=Vb2 results in lower power consumption). For R1 and R2, 100 KΩ and 100 Ω external resistors are used, respectively. The frame rate is 60 Hz, and the programming and calibration time is 20 μs. Here a 1x2 array is integrated with the discrete pixels where one pixel is used as reference pixel and the other one as working pixel. The current of working pixel is measured by using a trans-resistance amplifier connected between the ground and source of T1. Also two 100-pF external capacitors are used to emulate the parasitic capacitance of the Monitor and Vdata lines in a real panel.

Figure 6.14 (a) shows the response of the pixel current to a step voltage applied to the gate of the drive TFT. As it is clear, the current settles in less than 10 μs, which means that the current comparator is not a limiting factor for the refresh time. Moreover, the settling time is independent of the load at the monitor line since the monitor line is virtually grounded. Figure 6.14(b) shows the gain of the current between input and that of passing through Vb2, which follows the ratio of R1 and R2.

To emulate the V_T-shift for the next measurement, the ground voltage of the pixel circuit is increased. The extracted calibration voltage (V_{cal}) is depicted in Figure 6.15 (a) for both cases with charge injection compensation (case 1: turning off T2 during the sense cycle) and without charge injection compensation (case 2: T2 is ON during the sense cycle). The calibration voltage is used to compensate for the aging during the programming cycle. Here, a programming voltage is added to the calibration voltage and applied to the gate of T1 while T2 is ON (the current of T1 at this cycle is called programming current). Then T2 turns off



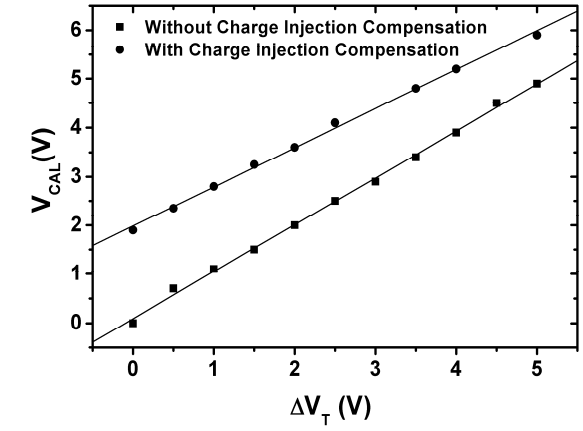
(a)



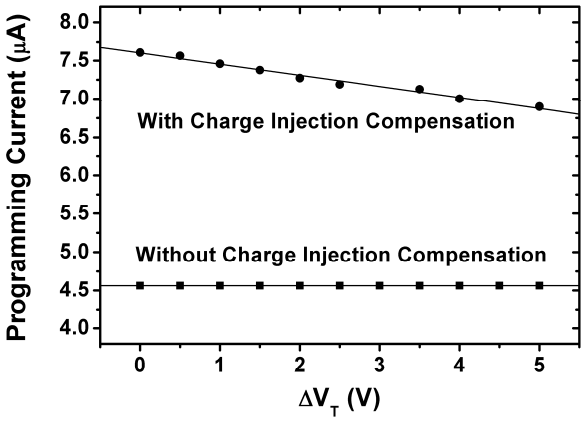
(b)

Figure 6.14: (a) Settling time for different step voltages and (b) gain of configurable current comparator.

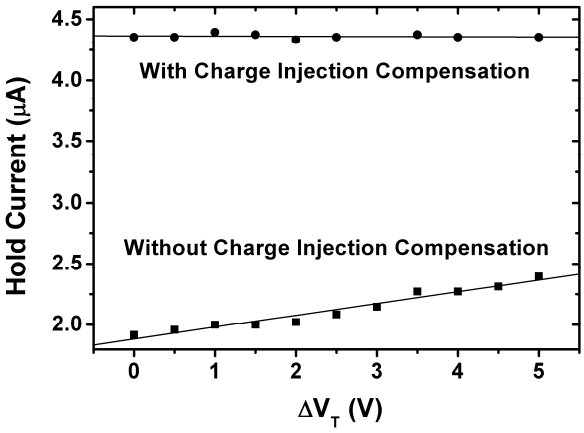
and T1 provides a current called hold current to the OLED for the rest of the frame time. The calibration voltage for case 1 is larger than that of case 2 but the slope of case 1 is 0.8 whereas the slope for case 2 is 0.96. As a result, the programming current of case 1 starts dropping as V_T shifts while the programming current of case 2 is stable (see Figure 6.15 (b)).



(a)



(b)



(c)

Figure 6.15: Measurement results of (a) calibration voltage (b) programming current and (c) hold current for calibration with and without charge injection compensation.

On the other hand, as shown in Figure 6.15 (c) the hold current of case 1 is stable, but the hold current for case 2 increases. Also, the hold current of case 1 is larger than that of case 2 since the total effect of charge injection is compensated. These results corroborate with the conclusions arising from (6.7). As predicted, the error in the pixel current is 0.47 % which is within the range of the quantization error of DACs at the source driver.

The successive calibration can be used to compensate for the other components of the pixel such as the OLED [101].

6.6 Summary

The driving scheme proposed in this section reduces the aging effects down to 0.5% by controlling the DC and transient shifts in the V_T and gate voltage of drive/amplifier TFT. Moreover, the algorithm presented here can inherently manage the offset associated with different driving components reducing the complexity of the driver IC. Adding gain states to the extraction algorithm enables tracing of sharp variation in V_T using a single bit comparator with reasonable number of iterations. Taking advantage of the slow aging rate of a-Si TFTs and fast settling of voltage programming, a single-bit current-mode comparator is designed for digital calibration. The refresh time of the proposed calibration can be as low as 2 s for a high definition panel (1920 x 3 x 1080). Measurement results presented here show that the error in the pixel current after a 5-V shift in the threshold voltage of the drive TFT is less than 0.47 %, which is in the range of the quantization error of the source driver.

Chapter 7

Conclusion

Despite the spatial and temporal non-uniformities, associated with the thin-film transistor (TFT), implementation of stable and uniform backplanes in which the TFTs serve as analog components is investigated in this thesis. The development of stable driving schemes for different applications is a critical step toward the realization of reliable and practical imagers and displays. In addition to high stability, the implementation cost, power consumption, and additive noise must be mitigated. To maximize the performance of various applications, different solutions are required since the specifications vary substantially. Thus, a set of driving schemes that can cover a wide range of intended applications for TFT backplanes is proposed.

Although the current mode active matrix has an intrinsic immunity to mismatches and differential aging, the long settling time at low current levels and large parasitic capacitance is a lingering issue, particularly for large area applications. Consequently, a current-biased voltage-programmed (CBVP) pixel circuit that benefits from the high immunity of current programming yet has a fast settling time, low implementation cost, and low power consumption is proposed. In particular, the CBVP driving scheme is adequate for technologies which are prone to mobility as well as V_T variations. A 16x12 sensor array is fabricated with CBVP pixel circuit that demonstrates a low noise. The array uses operational trans-resistance amplifier (OTRA) as the readout circuitry. This enables a faster readout

process and therefore real time operation. In addition, and unlike the hybrid PPS-APS driving schemes, a gain-boosting technique based on a MIS capacitor is developed that can improve the input dynamic range from extremely low to high input signal intensities.

For very low current levels and large area applications, a fast current driver is also developed. The settling time for a 100 nA current in the presence of a 200 pF parasitic capacitance is more than 2 ms for the conventional current source, whereas the settling time is less than 4 μs for the proposed current driver. This block can be used in a hybrid driving scheme in which current programming is used to extract the non-uniformity of the panel, while the normal operation is according to voltage programming.

For low-cost small-area AMOLED displays, a charge-based compensation technique is designed. Since on-pixel compensation is used and no change in driver requirement, the implementation cost is minimum. Measurement results of a fabricated 9-inch WXGA display show a high uniformity, despite the aging the panel with a gray-sclae pattern for almost 200 hours.

For high resolution devices, a driving scheme is required that provides less than a 1% non-uniformity. As a result, all the secondary effects such as charge-injection and clock feed-through becomes important. Also, a successive calibration using a current comparator is proposed. This driving scheme can provide for 0.5 % uniformity despite a 5-V shift in the V_T of the drive (amplifier) TFT. Also, this technique can be used in calibrating other component of the pixel such as the OLED and/or sensor.

The driving schemes presented in this thesis enable the use of TFT backplanes in a wide range of applications with different specifications. A quantitative comparison of these driving schemes is presented in Tables 7.1 and 7.2.

Table 7.1: Performance comparison of different AMOLED driving schemes.

	Compensation Ability					Settling time	Power Consumption	Implementation Cost	Application
	V_T shift	**V_T Variation**	**Mobility Variation**	**Temperature Variation**	**OLED Degradation**				
2-TFT	- -	- -	- -	- -	- -[1]	~ 10 µs	Low	Low	No application
VPPC	+	+	- -	- -	-[2]	> 20 µs	Medium	Medium[3]	Small displays
CPPC	+	+	+	+	-[2]	~ 1ms	Low	High[4]	No application
Scaling CPPC	+	+	+	+	-[2]	> 200 µs	Medium	High[4]	No application
Additive CPPC	+	+	-	-	-[2]	> 50 µs	High	High[4]	Small displays
CBVP	+	+	+	+	-[2]	~ 20 µs	Low	Low	Small-medium displays
Fast Current Source	+	+	+	+	-[2]	~ 4 µs	Low	Medium/High[5]	Large
AdMo™	+	+	+	+	-[2]	~ 10 µs	Low	Low	Small-medium displays
Successive Calibration	+ +	+ +	+ +	+ +	+ +	~ 10 µs	Low	Medium[3]	Large
Relaxation	Reduced[6]	NA	NA	NA	NA	NA	NA	Low	All

Here "- -" is very poor, "-" poor, "+" good, and "+ +" very good.

[1] It does not compensate for OLED voltage shift as well as OLED luminance degradation.

[2] It compensates for only OLED voltage shift.

[3] It requires slightly modified drivers.

[4] It requires new drivers.

[5] It can be used in hybrid driving schemes in which only one current source is required to calibrate the entire display.

[6] Threshold voltage shift in TFTs is reduced and becomes saturated even under constant current operation.

Table 7.2: Performance comparison of different biomedical driving schemes.

	Compensation Ability				Dynamic Range	Input Referred Noise	Implementation Cost
	V_T shift	**V_T Variation**	**Mobility Variation**	**Temperature Variation**			
3-TFT APS	-	-	-	-	Low intensity input signals	Low	High[1]
Hybrid APS-PPS	-	-	-	-	Medium to high intensity input signals[1]	Low	Medium[2]
CBVP	+	+	+	+	Medium to high intensity input signals[1]	Lower than 3-TFT APS	Medium[2]
Gain-Boosted CBVP	+	+	+	+	Very low to high intensity input signals	Lower than 3-TFT APS	Low[3]
Gain-Adjusted APS	+	+	+	+	low to high intensity input signals	Low	Low[3]
Short term stress	Controlled[4]	NA	**NA**	NA	NA	NA	NA

Here "- -" is very poor, "-" poor, "+" good, and "+ +" very good.

[1] It covers a narrow range of the applications.

[2] The cost is shared in a wider range of applications than that of 3-TFT APS.

[3] The cost is shared for most of the possible applications. Also, the driving scheme allows the use of lower cost driving circuitry such as OTRA for all range of input signal intensities.

[4] The TFTs tend to be stable under this driving scheme.

Appendix A

Enhanced Voltage Driving Schemes

Design of the VPPCs that provides the required configurability for voltage programming is hindered by several issues: complexity (a lower yield and aperture ratio), extra controlling signals (more complex external drivers), and extra operating cycles (overhead in power consumption). Moreover, the limited time provided for V_T-generation by the conventional addressing scheme, results in imperfect compensation.

A. 1 Interleaved Addressing Scheme

The interleaved addressing scheme depicted in Figure A.1 is based on V_T generation for several rows simultaneously. The rows in a panel are divided into few segments and the V_T- generation cycle is carried out for each segment. As a result, the time assigned to the V_T-generation cycle is extended by the number of rows in a segment leading to more precise compensation. Particularly, since the leakage current of a-Si:H TFTs is small (of the order of 10^{-14}), the generated V_T can be stored in a capacitor and be used for several other frames (see Figure A.1). As a result, the operating cycles during the next post-compensation frames are reduced to the programming and driving cycles similar to the operation of conventional 2-TFT pixel circuit [6]. Consequently, the power consumption associated with the external driver and with charging/discharging the parasitic capacitances is divided between the same few frames. In Figure A.1, the number of frames per segment is denoted as '*h*' and the

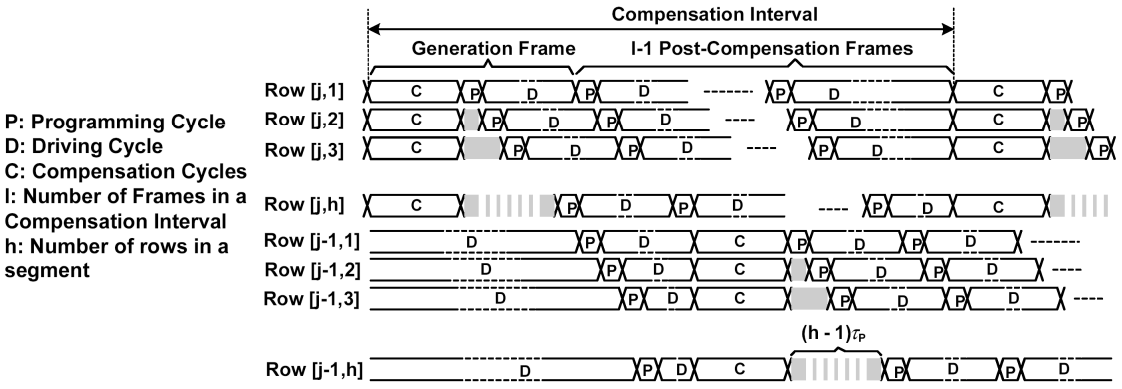


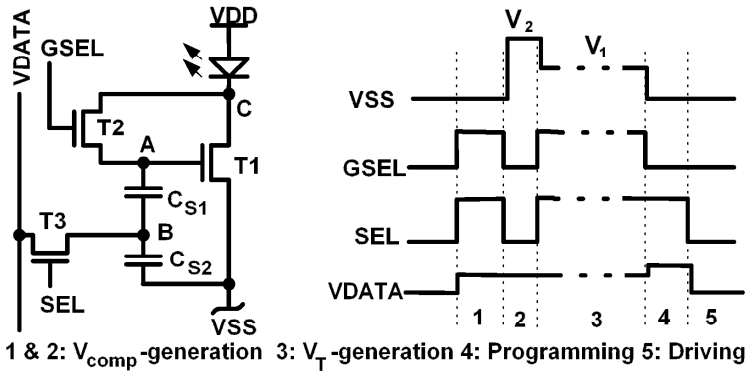
Figure A.1: Interleaving addressing scheme for low-power low-cost applications.

number of frames per compensation interval as '*l*'. As seen, the driving cycle of each row starts with a delay of τ_P from the pervious row, which is the timing budget of the programming cycle. Since τ_P (of the order of 10 µs) is much smaller than the frame time (of the order 16 ms), the latency effect is negligible. However, to improve the brightness accuracy, one can either change the programming direction each time, so that the average brightness lost due to latency becomes equal for all the rows or takes into consideration this effect in the programming voltage of the frames before and after the compensation cycles.

A.1. 1 3-TFT Pixel Circuit

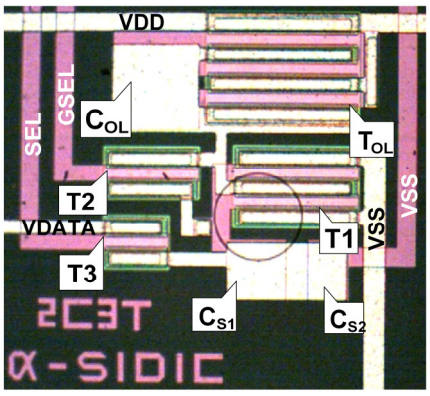
Figure A.2(a) demonstrates a 3-TFT pixel circuit designed for the interleaved addressing scheme. During the first operating cycle, node A is charged to a compensating voltage. To turn off the OLED, the voltage at node A and C are charged to a higher voltage at the second operating cycle.

During the third operating cycle, node A and C are discharged through T1 until the voltage reaches V_T of T1. A programming voltage is added to the generated V_T by bootstrapping during the fourth operating cycle. Thus, the current in the pixel during the fifth operating (driving) cycle becomes independent of V_T shift. Figure A.2 (b) shows the



(a)

W/L(T1)	400/23
W/L(T2)	150/23
W/L(T3)	100/23
W/L(T_{OL})	750/23
C_{OL}	6 pF
C_{S1}	2pF
C_{S2}	1pF

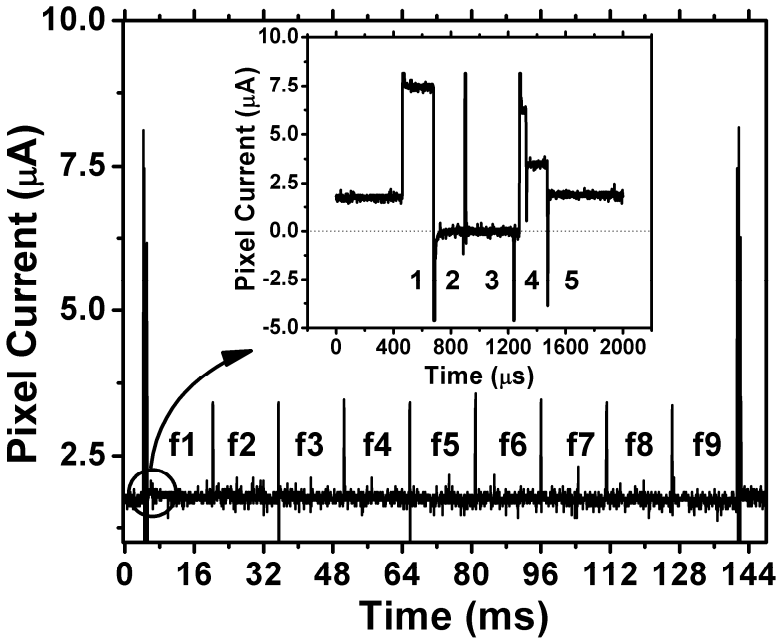


(b)

Figure A.2: A-Si:H 3-TFT voltage-programmed pixel circuit, and (b) photomicrograph of the fabricated pixel circuit (TFT sizes are denoted in μm).

macrograph of the fabricated 3-TFT pixel using a-Si:H technology. Here a diode connected TFT (T_{OL}) and a capacitor (C_{OL}) is used to emulate the OLED and its intrinsic capacitance respectively.

The extracted waveform for the operation of the pixel circuit using the interleaved addressing scheme is depicted in Figure A.3 (a), in which the number of frames in the compensation interval is 9. The inset plot denotes the different operating cycles including the compensation cycles. The transient cycle is explained in the next section. It is evident that the pixel current remains constant during the generation and post-compensation frames.



(a)

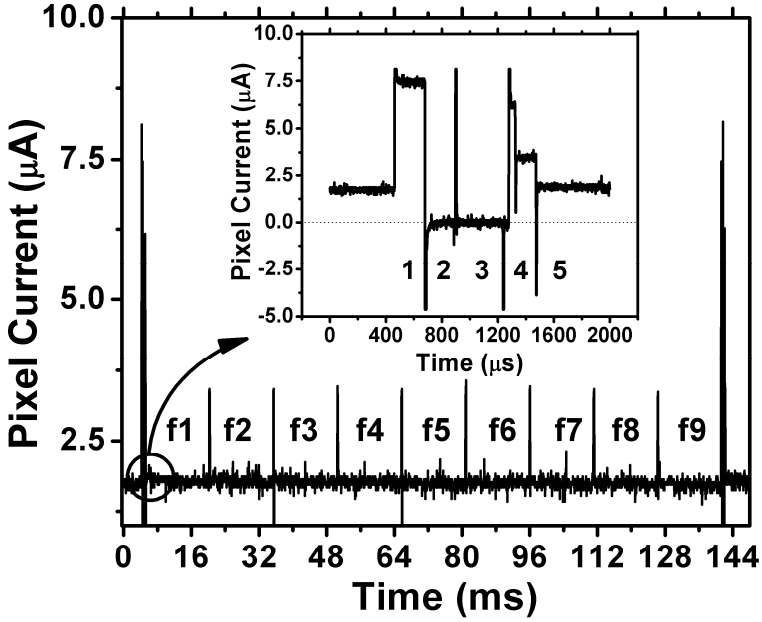


Figure A.3: (a) Measured pixel current for the interleaved addressing scheme, and (b) pixel current for different frames in the compensation interval.

Table A.1: Power and complexity of different driving schemes

Type	Power Consumption at 1μA	Number of IOs	
		Controlling	Data
2-TFT	230 mW	240	960
Compensated	446 mW	720	960
Interleaved	250 mW	290	960

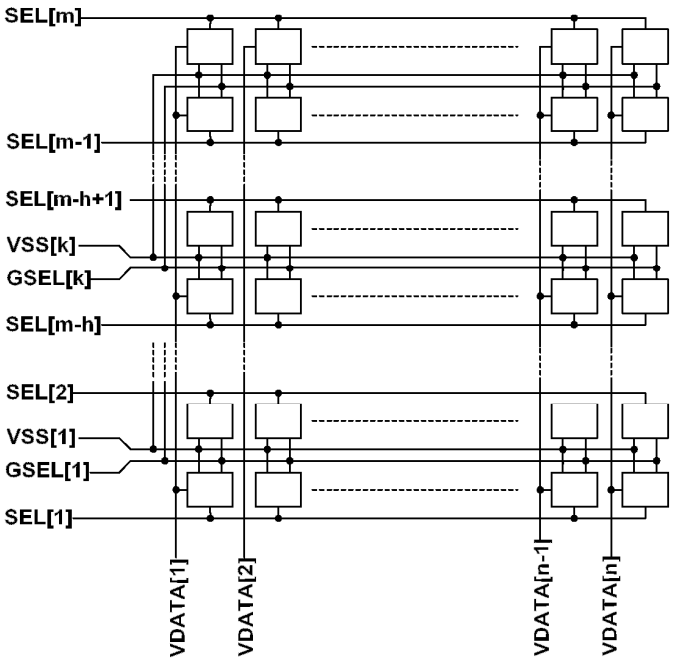


Figure A.4: Array structure sustaining the interleaved addressing scheme.

Figure A.3 (b) signifies the average pixel current for the frames in a compensation interval. The current drops by only a few percent due to the existence of leakage. However, this can be compensated during the programming cycle of post-compensation frames with a slightly larger current.

As listed in Table A.1, the power consumption of a 2-TFT RGB QVGA panel power consumption is 230 mW. The power consumption is calculated based on the current passing through a single pixel during different operating cycles for maximum brightness (1 μA) and the current of the source driver used to charge/discharge the storage/parasitic capacitance.

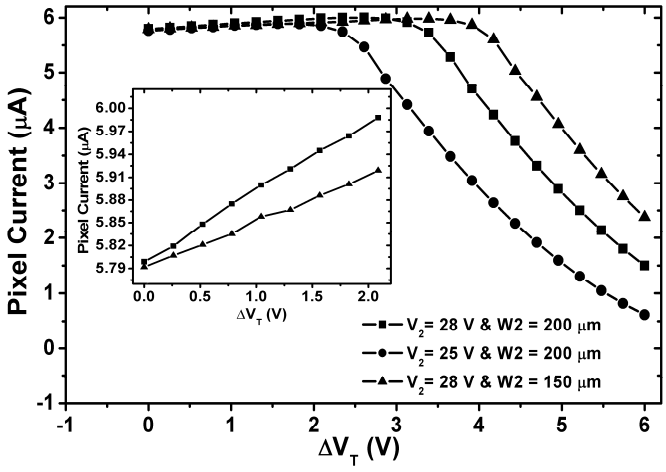


Figure A.5: Influence of non-idealities on the pixel current.

However, the compensation cycles increases the power consumption for the voltage programming to 446 mW whereas it is reduced to 250 mW by the 9-frame interleaved addressing, reducing the overhead in power consumption by approximately 90%.

Generally, compensation schemes add at least two more controlling signals to each row [83] resulting in a larger and more complex external driver. As indicated in Table A.1, this issue is well controlled by the interleaved addressing scheme and with the array structure presented in Figure A.4. The proposed array structure diminishes the wasted area caused by extra GSEL signal by sharing VSS and GSEL signal between two physically adjacent rows. Moreover, VSS and GSEL of each row in the same segment are merged together and form the segment GSEL and GVSS lines. Consequently, the controlling signals are reduced to 290 from 720 and approach to 240 by including more rows in each segment. Moreover, the number of blocks driving the signals is also reduced resulting in lower power consumption and lower implementation cost.

Figure A.4 shows a set of simulation results for different values of V_2 and sizes of T2 (W2). As depicted in the inset, the larger the T2 the higher the charge injection effect and so

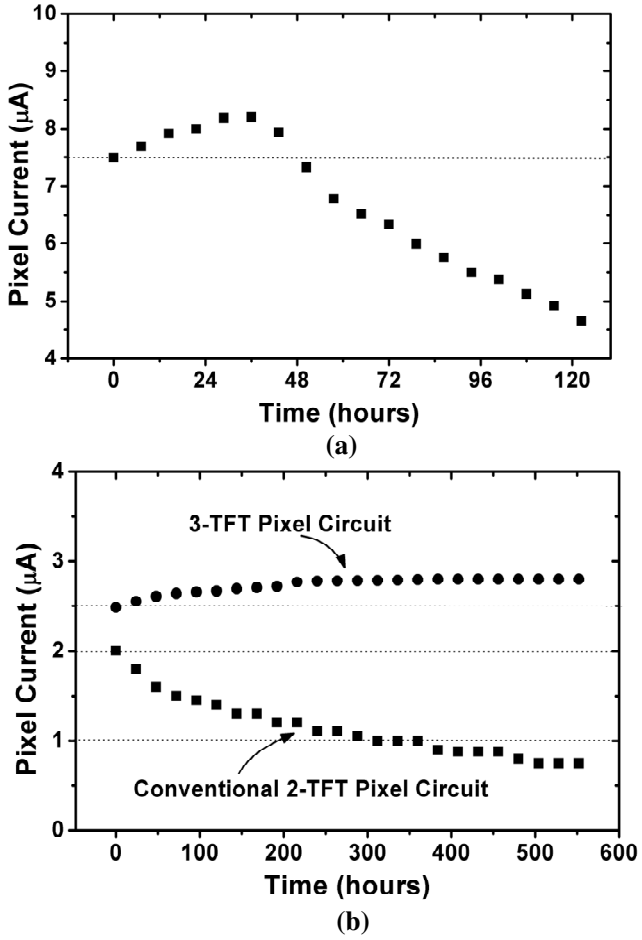


Figure A.6: Measurement results for (a) accelerated and (b) normal lifetime tests.

the current rises faster due to the V_T shift (see Chapter 6). Consequently, this can be used to compensate for OLED luminance degradation. However, a larger T2 reduces the compensating voltage developed at the gate of T1 during the third operating cycle due to higher charge injection and clock-feed through effects. This results in a smaller turn around voltage, which means the pixel current starts dropping for smaller V_T shift.

The measurement results depicted in Figure A.6 (a) highlight the significance of issues discussed above while supporting the simulation results shown in Figure A.5. To magnify the effects, the pixel is programmed at high current and a small voltage is used for V_2 (24 V), while V_1 is 17 V. Consequently, the circuit reaches its turn around voltage sooner. It is

evident that the current increases at the beginning due to the charge injection effect. However, after 30 hours the current drops, since the pixel cannot compensate for any larger V_T-shift. However, the maximum current required by an OLED is approximately 1 μA resulting in smaller V_T-shift overtime, and so the pixel continues to operate at realistic operating conditions for longer time, even with small V_2.

The measurement results in Figure A.6 (b) are based on a moderated current stress level and larger V_2 (28 V). The conventional 2-TFT pixel current drops by over 70% whereas the 3-TFT pixel current increases by 9% which can partially compensate for OLED luminance degradation. It is expected that pixel stability can meet requirements for mobile applications ranging from cell phones to digital cameras.

Appendix B

Short-Term Stress Driving Scheme

Until recently, circuits in a-Si:H technology have employed steady-state (dc) bias conditions in which the thin film transistors (TFTs) suffer from threshold voltage shift (VT-shift) over time. Here, an a-Si:H local current source (LCS) [75. 76] is used to adjust the circuit current bias. Since the LCS circuit is under stress for a small fraction of operation time, its current remains stable. The measurement and analysis of the LCS circuit indicate that the a-Si:H TFT is stable under short-term bias stress for over 50000 hours.

B. 1 Stability Analysis of Short-Term Stressed TFTs

The most appealing application of the a-Si:H technology is the large-area active matrix structure for display and imaging applications. In these applications, the programming time is a small fraction of the frame time; i.e. for a 320x240 matrix structure with a frame rate of 60 Hz (frame time is 16.7 ms) the programming time is less than 70 μs. As a result, if a TFT is used for the programming cycle, it is under stress for less than 1% of the frame time. The analysis and measurement results show that such a stress condition leads to a stable operation of the TFT. The V_T-shift of the TFT is given by [47]

$$\Delta V_T = \frac{[V_{GS} - V_{T0}]}{\left(1+\frac{1}{\alpha}\right)}\left(\frac{t_{sh\_st}}{t_0}\right)^{\beta} \tag{B.1}$$

where V_{GS} is the gate-source voltage of the TFT, V_{T0} the initial threshold voltage, t_0 the time constant, β measure of time dependence of hydrogen dispersion, and α the power index in the I-V characteristics of the TFT, where the I-V characteristics is given by $I_{DS} = K(V_{GS}-V_T)^{\alpha}$. Here, K is the gain parameter. Also, t_{sh_st} is the stress time of the TFT. The stress time of the short-term stressed TFT can be written as

$$t_{sh\_st} = \frac{t_p}{t_f} t_{life1} \quad . \tag{B.2}$$

Here, t_p is the programming time, t_f the frame time, and t_{life1} the anticipated life time of the circuit. Substituting (B.2) into (B.1), we can calculate the life time of the circuit based on an acceptable shift in the V_T.

$$t_{life1} = \frac{t_0 \cdot t_f}{t_p} \frac{\Delta V_T^{\frac{1}{\beta}} \left(1 + \frac{1}{\alpha}\right)^{\frac{\gamma}{\beta}}}{\left[V_{GS} - V_{T0}\right]^{\frac{\gamma}{\alpha\beta}}} \quad . \tag{B.3}$$

For example, if a shift of 0.5 V is acceptable for an application, the lifetime of the circuit will be higher than 50000 hours. Here, we use the values listed by S. M. Jahinuzzaman 2005 [47].

More importantly, the relaxation process during the time in which the TFT is not under stress is ignored in the lifetime calculation. During this time, any possible shift in the V_T of the TFT is partially annealed; thus, the lifetime will be higher than the one calculated in (B.3).

To investigate the effectiveness of the short-term biased stability of a-Si:H TFTs, a long term measurement was conducted. The same TFT as the one used for Figure 1 was used for this experiment after annealing at 170 ˚C. We put a TFT under stress with V_{GS}=V_{DS}=15 V for a small time during 16 ms frame time, and repeated for a test time interval. The measurement results are for an inverted staggered a-Si:H TFT structure that was fabricated

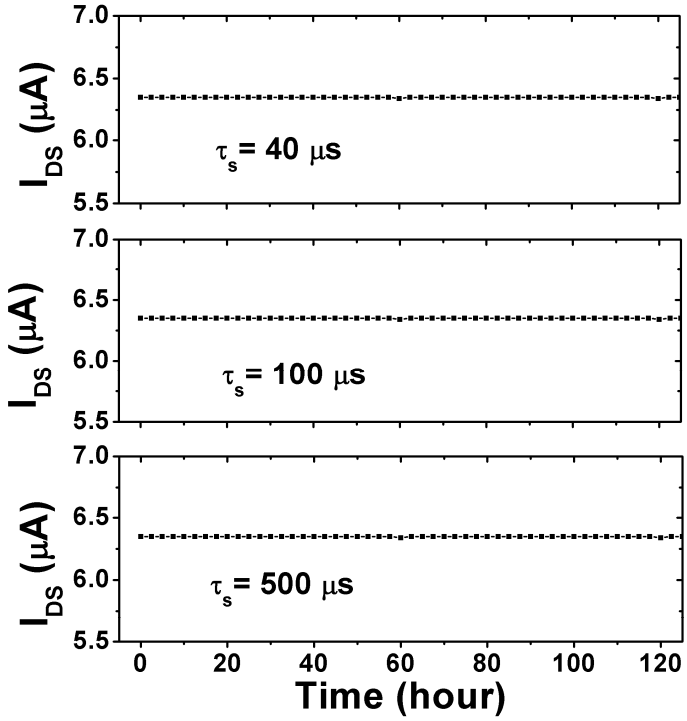


Figure B.1: Stability of the a-Si:H TFT under short-term stress.

using Standard plasma enhanced chemical vapor deposition (PECVD) at the temperature of 300 ◦C. Also, the thickness of a-SiN layer is 300 nm. The TFT current was measured during the stress condition (VGS=VDS=15 V). Figure B.1 demonstrates the result for different duty cycles. It is evident that the current of the TFT is stable after 120 hours of operation for even 0.5 ms stress time within a 16 ms frame time.

B. 2 Stable Circuit Design

The short-term stressed stability of the a-Si:H TFTs is used to implement a stable driving circuit for active matrix applications such as AMOLED displays. Figure B.2 (a) presents a circuit that provides a bias voltage that compensates for the V_T-shift in the current of the drive TFTs.

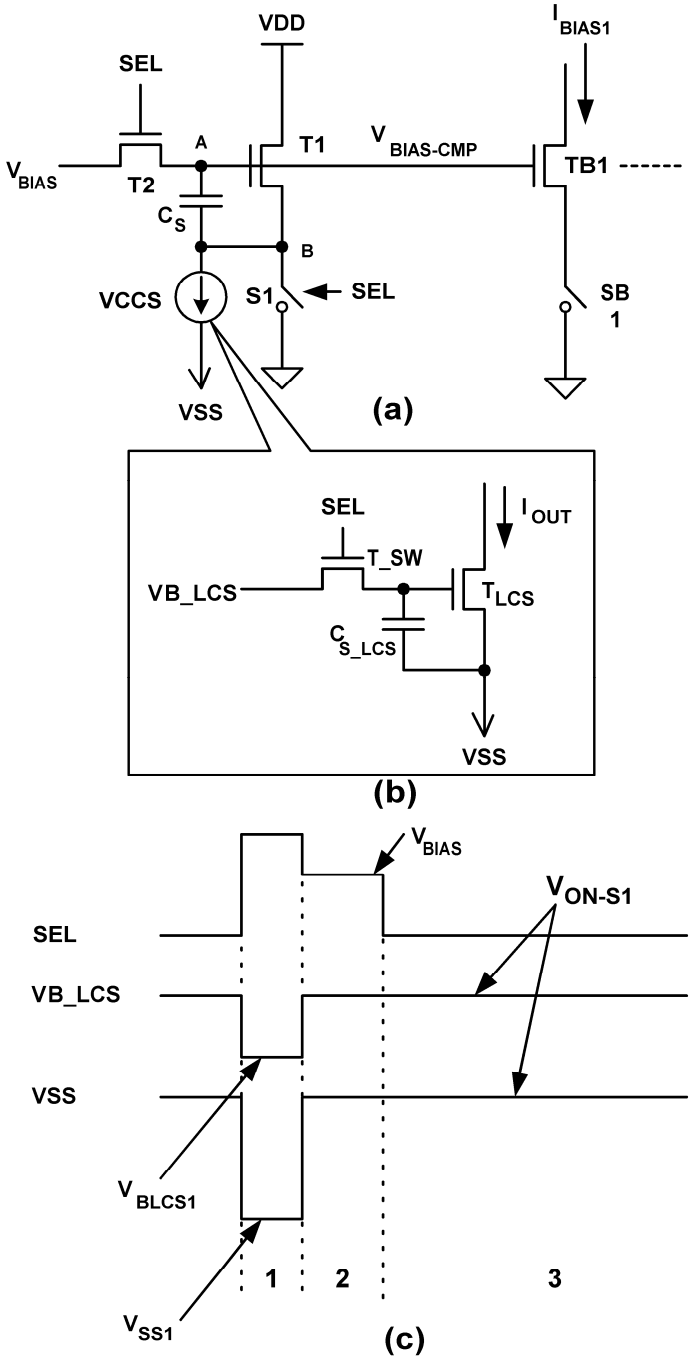


Figure B.2: Stable circuit design based on the stability of a-Si:H TFT under short-term stress.

During the first operating cycle, S1 is open, and SEL is high. As a result, node A is charged to V_{BIAS}, and node B goes to an appropriate voltage that allows all the current of the

voltage-control current source (VCCS) to pass through T1. The voltage at node *B* at the end of this driving cycle is

$$V_B = V_{BIAS} - V_T - \left(\frac{I_B}{K}\right)^{\alpha} \tag{B.4}$$

where I_B is the current of VCCS. In the next operating cycle, SEL goes to a low voltage, and S1 is closed, and so voltage at node A goes to $V_{ON\_S1}+V_T+(I_B/K)^{1/\alpha}$ where V_{ON_S1} is the ON voltage of S1.

Figure B.2 (b) is an implementation of VCCS with a-Si:H TFTs as a local current source (*LCS*). During the first operating cycle, the gate-source voltage of T_{LCS} goes to $V_P = V_{BLCS1} - V_{SS1}$. Considering the fact that T_{LCS} is in saturation region, its current is given by $K(V_P-V_{TLCS})^{\alpha}$ where V_{TLCS} is the threshold voltage of T_{LCS}. During the second operating cycle, the gate and source voltages of T1 go to $V_{ON\text{-}S1}$ so that T_{LCS} is not under stress. The voltage on the V_{BIAS_COMP} line becomes $V_P+V_{T1}-V_{TLCS}+V_{ON\_S1}$, and so the current of T1 stays at $K(V_P-V_{TLCS})^{\alpha}$. If the timing of the proposed circuit and driving scheme is the same as the measurement condition, T_{LCS} will be stable. As a consequence, since the current of T1 is adjusted by the T_{LCS} current, the current of T1 remains stable.

Figure B.3 displays the simulation results for the circuit in Figure B.2(a). Here, the size of T1 and TB1 is 400 μm/ 23 μm and the C_S is 4 pF. The simulation results are based on a physical model in which the parameters are extracted from a set of fabricated TFTs. It is evident that the V_{BIAS_CMP} includes the threshold voltage of T1. Thus, if we use this voltage to bias another TFT such as TB1 which has the same bias conditions as T1's, the current of that TFT remains stable.

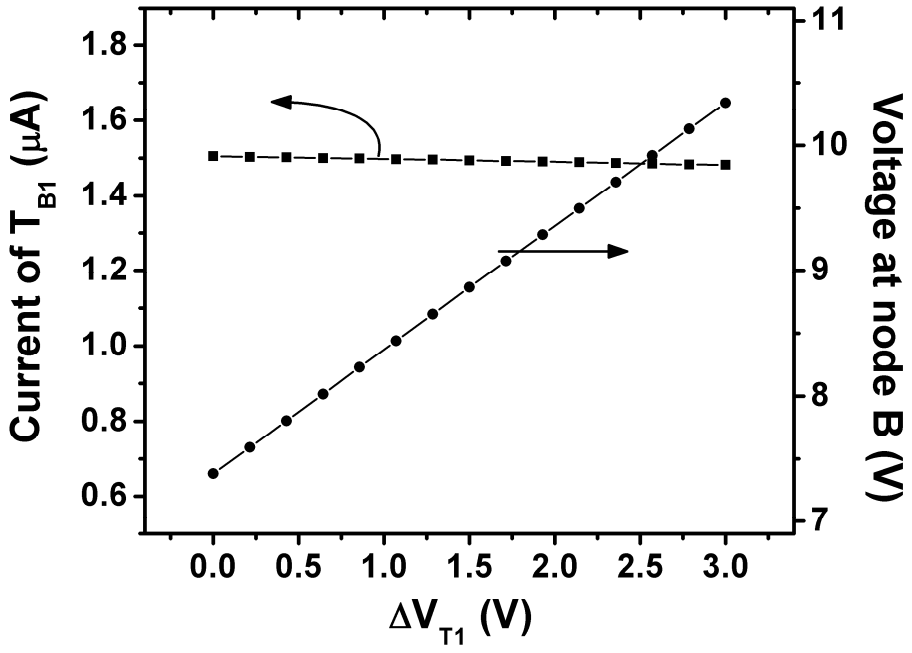


Figure B.3: Simulation results of the circuit depicted in Figure B.2.

To have a stable current provided by T_{LCS}, it should be in saturation regime of operation. However, following (B.4), the drain voltage of T_{LCS} drops as the V_T of T1 increases, which moves TLCS to the linear regime of operation. Therefore, the lifetime of the circuit is limited also by the saturation condition of TLCS. Considering that the initial threshold voltages of T1 and TLCS are the same, the maximum acceptable VT-shift that do not violate the saturation condition of TLCS is calculated as

$$\Delta V_{T1}(\max) = V_{BIAS} - V_{SS1} - 2V_P \,. \tag{B.5}$$

Since the current of T1 is constant, its V_T-shift follows the constant current stress model [47].

$$t_{life2} \leq \left[\frac{\left(1 + \frac{1}{\alpha}\right)^{\gamma} \left(V_{BIAS} - V_{SS1} - 2V_P\right)}{(V_P - V_{TLCS})^{\gamma}} \right]^{\frac{1}{\beta}} t_0 \tag{B.6}$$

where γ is a power parameter having a value in range of 1.5-1.9 [47]. According to (B.6), we can fit the circuit lifetime for a specific application by using appropriate values for V_{SS1} and V_{BIAS}. Following (B.6) and (B.3), the lifetime of the circuit is defined as $t_{life} \leq \min(t_{life1}, t_{life2})$.

Appendix C

OLED Electrical Calibration

This section presents a stable compensation scheme for AMOLED displays based on the strong interdependence observed between the luminance degradation of OLED and its current drop under bias stress [100]. This feedback based compensation provides 30% improvement in the luminance stability under 1600-hour of accelerative stress. To employ this scheme in AMOLED displays, a new pixel circuit is presented that provides on-pixel electrical access to the OLED current without compromising the aperture ratio.

C. 1 Interdependence Between Electrical and Luminance Degradation

Figure C.1 shows the lifetime results of a 4-mm^2 PIN-OLED with a red phosphorescent emitter for a constant luminance of 1500 nits/cm^2. A constant voltage of 3 V is applied to the OLED and the current and luminance are measured every 10 minutes. As seen, the ratio between luminance and current degradation is almost constant for the entire range. Here, ΔL and ΔI are the degradation in the OLED luminance and current, respectively, and L_0 and I_0 are the respective initial values. From the observed interdependence, it appears very likely that both luminance degradation and drop in the drive current in the OLED have a common source, and that may be the charge trapping/de-trapping at the interface of the different layers [12]. Thus, it is possible to control the aging of OLED using its output electrical signals. Although, there is a deviation at degradation levels higher than 60 %, we adopt a linear

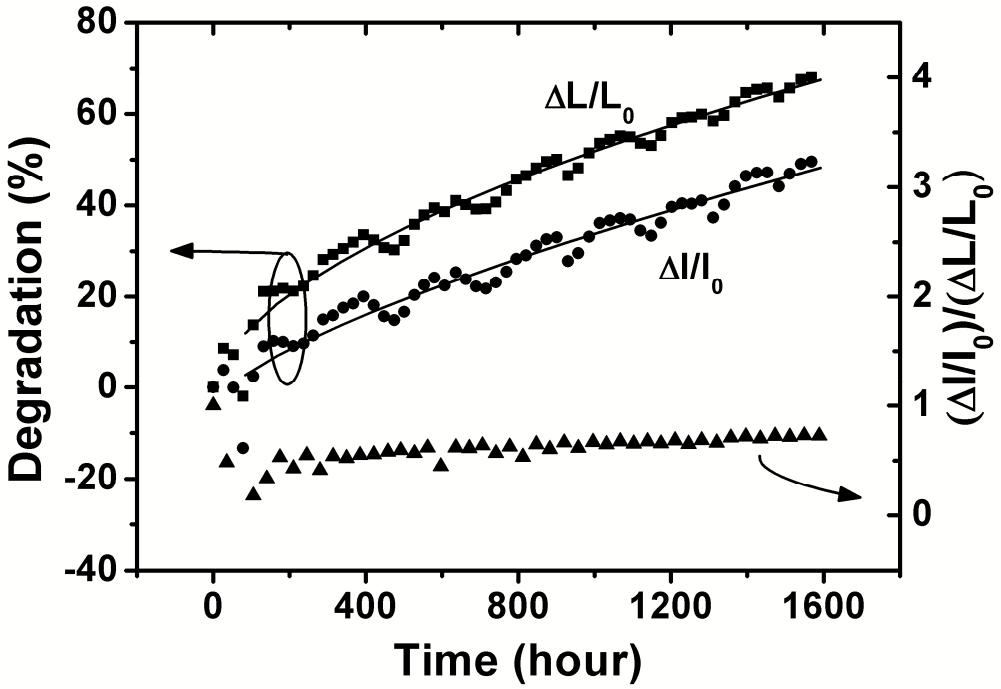


Figure C.1: Interdependence between current and luminance degradation of the OLED.

approximation for the compensation scheme.

C. 2 Electrical Compensation of OLED Degradation

To investigate the effectiveness of the electrical feedback, an OLED sample is put under constant luminance stress of 1500 nits/cm^2. Every 30 minutes, a 3-V bias is applied to the OLED and its current is measured. Using a simple linear approximation, the OLED current stabilizing the luminance can be calculated as

$$I_P(n) = I_P(0)\left(1 + K\,\frac{I_B(0) - I_B(n)}{I_B(0)}\right) \tag{C.1}$$

in which K is the correction factor, $I_P(0)$ the initial programming current, $I_B(0)$ the initial biasing current following the 3-V bias, and $I_B(n)$ and $I_P(n)$ the biasing and programming currents after n/2 hours, respectively. Here, the current of an unstressed OLED at 3-V bias is used as I_B (0) during each measurement interval. Then, the new programming current, $I_P(n)$,

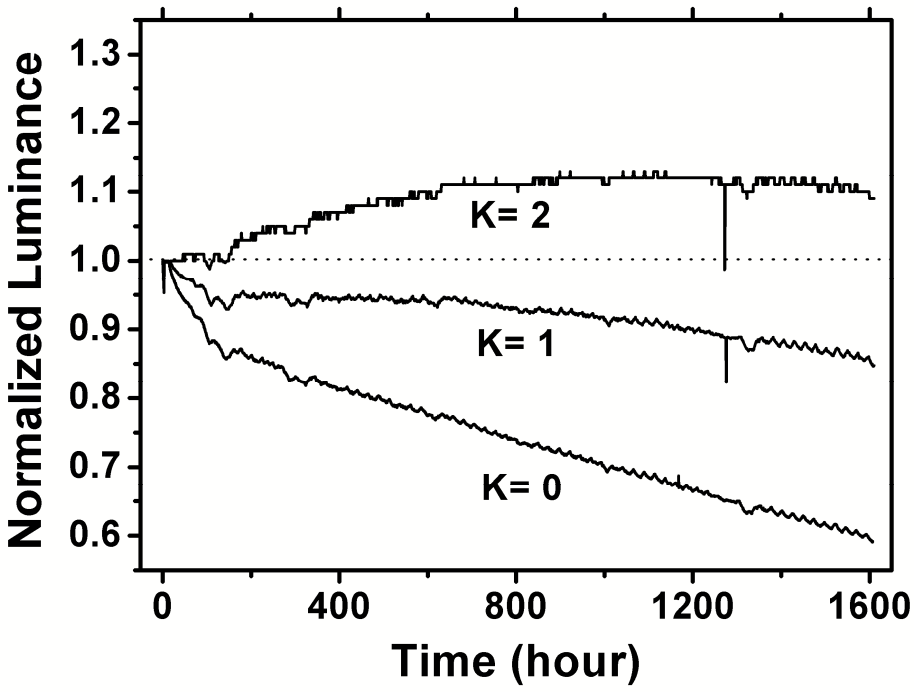


Figure C.2: Electrical feedback measurement data for (a) OLED current and (b) OLED luminance at constant current (i.e. for K=0).

is applied to the OLED and its luminance is measured. Measurement results depicted in Figure C.2 show that electrical feedback compensates for the degradation by 30%. The constant current (i.e. when K=0) results in 40 % luminance drop whereas the degradation when K= 1 and *K =2* is less than 10 %. Here, the initial luminance is 300 nits. The correction factor and the linear approximation may vary for different OLED technologies. Nevertheless, the method shows promising improvement when the degradation in OLED current and luminance exhibit strong interdependence for a given biasing voltage.

C. 3 Pixel Circuit for OLED Compensation

To adopt this technique in an AMOLED display, the pixel circuit shown in Figure C.3 (a) is designed to provide electrical access to compensate both the drive TFT (*T1*) and OLED instability. The select lines of adjacent rows (SEL[i] and SEL[i+1]) and the data lines of

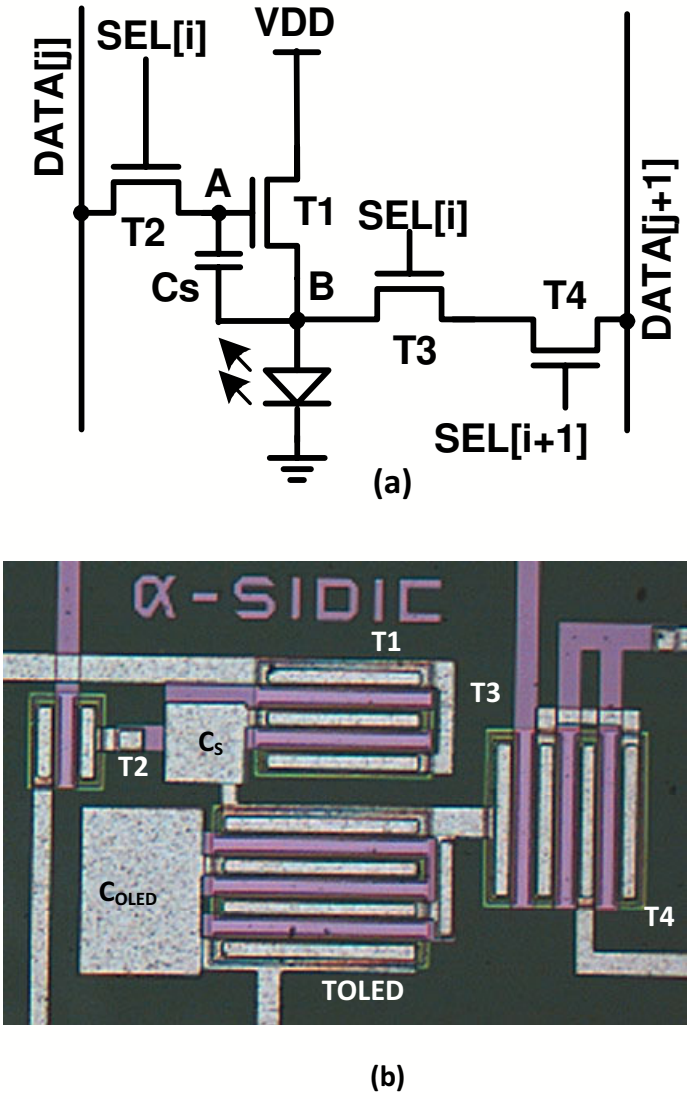


Figure C.3: : (a) Proposed pixel circuit to control OLED degradation using electrical feedback and (b) photo micrograph of the fabricated pixel circuit in which T1 = 400/23, T2=100/23, T3 =200/23, T4=400/23, TOLED=750/23, C_S=2 pF, and C_{OLED} =6 pF (the sizes are in μm).

adjacent columns (DATA[j] and DATA[j+1]) are shared to not compromise the aperture ratio and to enable use of simpler external drivers. To extract the TFT instability, SEL[i] and SEL[i+1] is high and node *A* is charged to a calibration voltage while node *B* is set to VSS. Therefore, OLED is OFF and the current through *T1* can be read through *T3* and *T4*. Here,

the calibration voltage increases over time by a step voltage until the current becomes equal to a reference current, and so the number of steps determines the threshold voltage shift (ΔV_T) [99]. Also, by charging node A to zero and applying a biasing voltage to node B, the OLED current can be read back so as to manage the OLED luminance degradation following (1). During the normal operation, SEL[i] is high and node A is charged to a programming voltage modified according to the extracted ΔV_T and luminance degradation.

To investigate the stability of the current of TFT pixel, a test circuit was fabricated using standard plasma enhanced chemical vapor deposition (PECVD) for a-SiN, a-Si:H, and passivation layers at the temperature of 300 ˚C (see Figure C.3(b)). In the fabricated pixel circuit, a diode connected TFT is used to emulate the OLED. Measurement results of TFT stability compensation are presented in Figure C.4. The current is stable, despite a 2-V shift in the threshold voltage of T1.

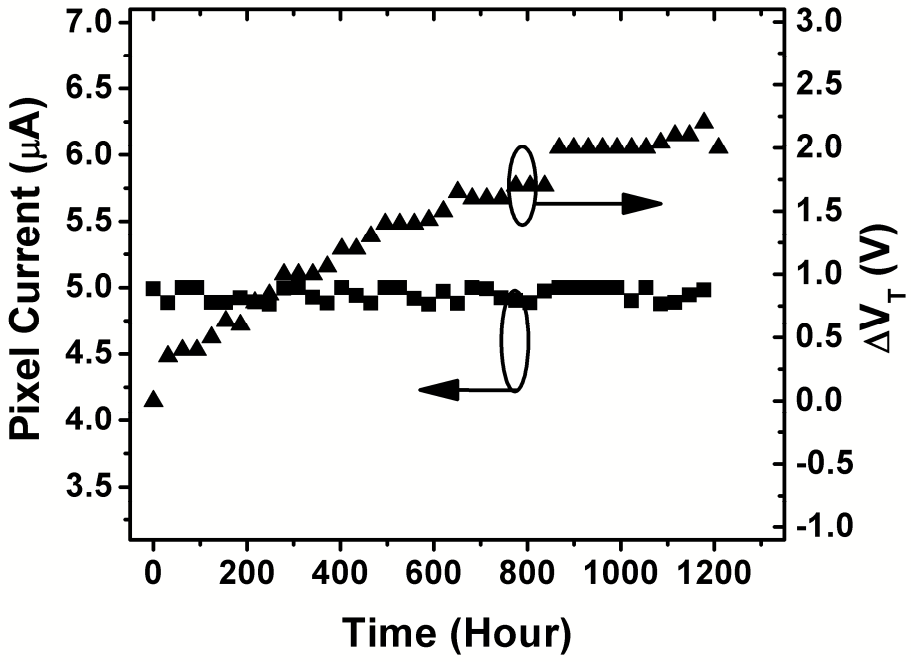


Figure C.4: Measurement results of compensating for TFT instability.

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