

# **Transparent Oxide Semiconductors: Fabrication, Properties, and Applications**

by

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A thesis  
presented to the University of Waterloo  
in fulfillment of the  
thesis requirement for the degree of  
Doctor of Philosophy  
in  
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2008

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## **AUTHOR'S DECLARATION**

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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## Abstract

Transparent oxide semiconductors (TOSs) are materials that exhibit electrical conduction and optical transparency. The traditional applications of these materials are transparent conducting oxides in flat-panel displays, light-emitting diodes, solar cells, and imaging sensors. Recently, significant research has been driven to extend state-of-the-art applications such as thin-film transistors (TFTs). A new and rapidly developing field is emerging, called transparent electronics. This thesis advances transparent electronics through developing a new technique to fabricate TOSs and demonstrating their applications to active semiconductor devices such as diodes and TFTs.

Ion beam assisted evaporation (IBAE) is used to deposit two common TOSs: zinc oxide (ZnO) and indium oxide ( $\text{In}_2\text{O}_3$ ). The detailed material study is carried out through various characterization of their electrical properties, chemical composition, optical properties, crystal structure, intrinsic stress, topology, and morphology, as well as an investigation of thin-film property as a function of the deposition parameters: ion flux and energy, and deposition rate. The study proves that IBAE technique provides the capability for fabricating TOSs with controllable properties.

By utilizing the newly developed semiconducting ZnO, p-NiO/i-ZnO/n-ITO and n-ITO/i-ZnO/p-NiO heterostructure photodiodes with a low leakage are proposed and assessed. Analysis of their current-voltage characteristics and current transient behaviour reveals that the dominant source of leakage current stems from the deep defect states in the intrinsic zinc oxide layer, where its dynamic response at low signal levels is limited by the charge trapping. The exploration of the photoconduction mechanism and spectral response confirms that such photodiodes are potentially

applicable for ultraviolet (UV) sensors. The comparative study of both device structures provides further insights into the leakage current mechanisms, p-i interface properties, and quantum efficiency.

Secondly, with the novel semiconducting  $\text{In}_2\text{O}_3$ , TFTs are fabricated and evaluated. The device performance is optimized by addressing the source/drain contact issue, lowering the intrinsic channel resistance, and improving the dielectric/channel interface. The best n-channel TFT has a high field-effect mobility of  $\sim 30 \text{ cm}^2/\text{Vs}$ , a high current ON/OFF ratio of  $\sim 10^8$ , and a sub-threshold slope of 2.0 V/decade. More important, high-performance indium oxide TFTs here are integrated with the silicon dioxide and silicon nitride gate dielectrics by conventional plasma-enhanced chemical vapour deposition, which makes indium oxide TFT a competitive alternative for next generation TFTs to meet the technical requirements for flat-panel displays, large area imager arrays, and radio frequency identification tags. The stability study shows that indium oxide TFTs are highly stable with a very small threshold voltage shift under both a long-term constant voltage and long-term current stress. The dynamic behaviour indicates factors that affect the operation speed of such TFTs. A descriptive model is proposed to link the material properties and the processing issues with the device performance to facilitate further research and development of TOS TFTs.

The research described in this thesis is one of the first investigations of the fabrication of TOSs by the IBAE and their applications to a variety of thin-film devices, particularly UV sensors and TFTs.

## Acknowledgements

I would like to express my sincere thanks to my advisor, Dr. Arokia Nathan for his vision, supervision and guidance. He has supported me throughout my doctoral program and often encouraged me to dig deeper into my research. Words cannot express my gratitude to him.

I am indebted to my mentor, Dr. Yuriy Vygranenko for training me in equipment usage, device fabrication and characterization, and analysis. This work would not have been completed without his direction and help.

Many thanks go to Flora Li and Hyun Jung Lee for their advice and fruitful discussion on device physics during countless coffee breaks. I am grateful to my colleagues, Reza Chaji and Afrin Sultana, for their help with the stress tests, Hassan El-Gohary for his assistance in rapid thermal annealing, and Richard Barber and Robert Mullins for their equipment trouble-shooting. Thanks are also given to many other colleagues: Mohammad R. Esmaili Rad, Maryam Moradi, Dr. Majid Gharghi, Dr. Isaac Chan, Dr. Yichun Luo, former group members Dr. Dennis Striakhilev, Dr. Sheng Tao, Dr. Jeff Chang, Dr. Jackson Lai, Dr. Kyung Ho Kim, Saeed Fatholouloumi, and my officemate, Arash Fomani.

I also want to thank some professors and staff from the department: Dr. Andrei Sazonov, Dr. Siva Sivoththaman, Dr. Hany Aziz, Dr. Dayan Ban, Dr. M. P. Anantrum, Dr. Sherman Shen, Annette Dietrich, Wendy Boles, Lisa Hendel, Karen Schooley, and Eliza Ho for their help.

Special thanks to Gloria Ichim for her endless encouragement and support. I am grateful to my landlady, Maria Alice Seviara and her family, Lakhena Sam, Donna

Armborst, Uncle Dexu Sun and his family, my roommate, Yunwei Dong, and my good friends: Raymond Zhu, Wei Li and Xiaoling Ling, Dr. Shude Xiao, Yanqiao Zhang, Dr. Xiaogang Li and his family, Dr. Humphrey Rutagemwa, Dr. Henghua Deng, Fanlong Ning and Yi Zhou for their encouragement and friendship during my years in Canada. I appreciate Jing Fu for her listening to my stories and sharing laughter which I needed most.

Lastly and most important, my everlasting gratitude goes to my father, Min Wang and my mother, Shumin Yang, for their continuous and unconditional support and love. This thesis is dedicated to them.

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# Chapter 1

## Introduction

Metal oxides are very interesting materials which can behave as insulators, superconductors, and semiconductors. Some of them exhibit electrical conductivity and visible transparency such as transparent oxide semiconductors (TOSs). Traditionally, the semiconductors such as indium-tin oxide (ITO), doped tin oxide ( $\text{SnO}_2\text{:F}$ ;  $\text{SnO}_2\text{:Sb}$ ), and doped zinc oxide ( $\text{ZnO:Al}$ ;  $\text{ZnO:Ga}$ ;  $\text{ZnO:In}$ ) are widely used as transparent conducting oxides (TCOs) in flat-panel displays, light-emitting diodes, solar cells, and imagers [2]. Recently, thin-film transistors (TFTs) based on TOSs have attracted a great deal of attention.

This thesis addresses materials, processing, and devices regarding TOSs with a focus on diodes and TFTs. The purpose of this chapter, in particular, is to review this group of materials, focusing on ZnO and  $\text{In}_2\text{O}_3$ , to describe the challenges of the emerging transparent electronics.

### 1.1 Overview of TOSs

This section contains a brief introduction of TOSs from fundamental material physics to industrial applications, a review of two well-known TOSs: ZnO and  $\text{In}_2\text{O}_3$ , including their crystal and electronic structures, and the research challenges in the field of transparent electronics.

TOSs are a series of metal oxides, composed of heavy metal cations (HMCs) with an outside shell electronic configuration of  $(n-1)d^{10}ns^0$  ( $n>4$ ) and oxygen anions [3].

In terms of this definition, the candidates of HMCs to form TOSs can be sorted out from the chemical periodic table and their electronic configurations are in Table 1.1.

Table 1.1: Candidates for HMCs with the electronic configuration

<b>Cu</b> [Ar]3d <sup>10</sup> 4s <sup>1</sup>	<b>Zn</b> [Ar]3d <sup>10</sup> 4s <sup>2</sup>	<b>Ga</b> [Ar]3d <sup>10</sup> 4s <sup>2</sup> 4p <sup>1</sup>	<b>Ge</b> [Ar]3d <sup>10</sup> 4s <sup>2</sup> 4p <sup>2</sup>	<b>As</b> [Ar]3d <sup>10</sup> 4s <sup>2</sup> 4p <sup>3</sup>
<b>Ag</b> [Kr]4d <sup>10</sup> 5s <sup>1</sup>	<b>Cd</b> [Kr]4d <sup>10</sup> 5s <sup>2</sup>	<b>In</b> [Kr]4d <sup>10</sup> 5s <sup>2</sup> 5p <sup>1</sup>	<b>Sn</b> [Kr]4d <sup>10</sup> 5s <sup>2</sup> 5p <sup>2</sup>	<b>Sb</b> [Kr]4d <sup>10</sup> 5s <sup>2</sup> 5p <sup>3</sup>
<b>Au</b> [Xe]4f <sup>14</sup> 5d <sup>10</sup> 6s <sup>1</sup>	<b>Hg</b> [Xe]4f <sup>14</sup> 5d <sup>10</sup> 6s <sup>2</sup>	<b>Tl</b> [Xe]4f <sup>14</sup> 5d <sup>10</sup> 6s <sup>2</sup> 5p <sup>1</sup>	<b>Pb</b> [Xe]4f <sup>14</sup> 5d <sup>10</sup> 6s <sup>2</sup> 5p <sup>2</sup>	<b>Bi</b> [Xe]4f <sup>14</sup> 5d <sup>10</sup> 6s <sup>2</sup> 6p <sup>3</sup>

[Ar]: 1s<sup>2</sup>2s<sup>2</sup>2p<sup>6</sup>3s<sup>2</sup>3p<sup>6</sup>

[Kr]: 1s<sup>2</sup>2s<sup>2</sup>2p<sup>6</sup>3s<sup>2</sup>3p<sup>6</sup>3d<sup>10</sup>4s<sup>2</sup>4p<sup>6</sup>

[Xe]: 1s<sup>2</sup>2s<sup>2</sup>2p<sup>6</sup>3s<sup>2</sup>3p<sup>6</sup>3d<sup>10</sup>4s<sup>2</sup>4p<sup>6</sup>4d<sup>10</sup>5s<sup>2</sup>5p<sup>6</sup>

TOSs have wide bandgaps in which the ns orbitals of the HMCs primarily constitute the bottom part of the conduction band and the oxygen 2p orbitals form the top of the valence band. Uniquely, the spatial spreading of the outside ns orbitals with a spherical symmetry in the HMCs is much larger than that in light metal cations such as aluminium, leading to a wider conduction band. Since the carrier mobility is proportional to the width of the conduction band, TOSs are electrically active and differ from light metal oxides such as MgO and Al<sub>2</sub>O<sub>3</sub> which are typical insulators. The metal ion radius, metal and oxygen bond length and angle are among the critical parameters that determine the carrier mobility of these oxide semiconductors. Table 1.2 lists these critical parameters of the common HMCs and TOSs, and their ns orbital overlap integrals [1].



Table 1.2: Critical parameters of HMCs and TOSs [1]

HMC	TOS	ion radius (pm)	M-O length (Å)	M-O-M angle	Overlap
<b>Zn 4s</b>	<b>ZnO</b>	<b>1.16</b>	<b>1.976</b>	<b>108.2<sup>0</sup></b>	<b>0.6045</b>
Ga 4s	$\beta$ -Ga <sub>2</sub> O <sub>3</sub>	0.88	1.978	100.4 <sup>0</sup>	0.4632
Ge 4s	GeO <sub>2</sub>	0.71	1.738	130.0 <sup>0</sup>	0.2848
Cd 5s	CdO	1.25	2.348	90.0 <sup>0</sup>	0.6905
<b>In 5s</b>	<b>In<sub>2</sub>O<sub>3</sub></b>	<b>0.95</b>	<b>2.180</b>	<b>98.2<sup>0</sup></b>	<b>0.5613</b>
Sn 5s	SnO <sub>2</sub>	0.77	2.052	101.9 <sup>0</sup>	0.4523

As seen from this table, the Zn-Zn 4s and the In-In 5s orbitals have large overlap integrals compared with the other HMCs. As a result, ZnO and In<sub>2</sub>O<sub>3</sub> should have a high carrier mobility. This has already been proven by Hall-effect measurements: single crystalline n-type ZnO has a Hall mobility of around 200 cm<sup>2</sup>/Vs, and single crystalline n-type In<sub>2</sub>O<sub>3</sub> has a Hall mobility as high as ~ 160 cm<sup>2</sup>/Vs [1]. Moreover, the large ns-ns orbital overlap makes the mobility less sensitive to any angular variation or bond stretching in the M-O-M bonds; that is, the mobility of TOSs is immune to the structural disorder because of such ionic bonding. Thus, amorphous TOSs still display a considerable carrier mobility comparable to their crystalline counterparts. This characteristic cannot be found in other types of semiconductor materials. For instance, the mobility of polycrystalline silicon (covalent bonding) is 2~3 orders of magnitude higher than that of amorphous silicon (a-Si:H).

## 1.2 Two Common TOSs: $\text{In}_2\text{O}_3$ and $\text{ZnO}$

As discussed in the previous section, both  $\text{In}_2\text{O}_3$  and  $\text{ZnO}$  are non-toxic and have relatively large overlap integrals, leading to a high mobility that is desirable for device applications. In this section, an introduction of these two vital TOSs is given.

### 1.2.1 Crystal Structure

$\text{In}_2\text{O}_3$  has a bixbyite crystal structure that is inherently a cubic-type rare earth, vacancy-defect oxide. Bixbyite has an 80 atom unit cell with the  $\text{Ia}\bar{3}$  space group and a 1 nm lattice constant in an arrangement, based on the stacking of the  $\text{MO}_6$  coordination groups [2]. The bixbyite structure is similar to that of fluorite and has a face-centred cubic array of indium atoms with all the tetrahedral interstitial positions filled with oxygen atoms. The primary difference between fluorite and bixbyite is the  $\text{MO}_8$  coordination units in the bixbyite structure (the oxygen position is on the corners of a cube and the indium atom is located at the centre of the cube) are replaced by units with oxygen atoms missing from either the body or the face diagonally as depicted in Figure 1.1. The removal of two oxygen atoms from the  $\text{MO}_8$  to form the  $\text{MO}_6$  coordination units forces the displacement of the indium from the centre of the cube. Thus, indium is distributed in two nonequivalent sites with one-quarter of the indium atoms positioned at the centre of a trigonally distorted oxygen octahedron (diagonally missing O), and the remaining three-quarters positioned at the centre of a more distorted and less symmetric octahedron that results from the removal of two oxygen atoms from the same face of the octahedron. The resulting  $\text{MO}_6$  coordination

units are then stacked such that one-quarter of the oxygen atoms are missing from each {100} plane in the fluorite structure [4].

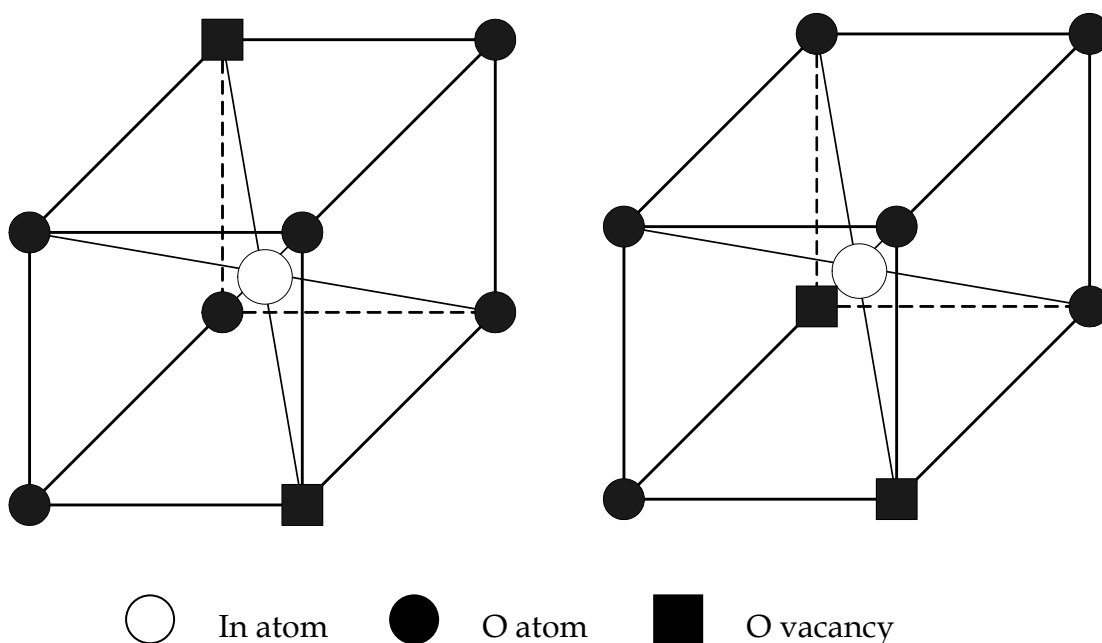


Figure 1.1: Schematic illustration of atomic arrangement in crystalline  $\text{In}_2\text{O}_3$

Zinc oxide crystallizes in the hexagonal wurtzite lattice in Figure 1.2. The zinc atoms are nearly in the position of hexagonal close packing. Each oxygen atom lies within a tetrahedral group of four zinc atoms, which are in the same direction along the hexagonal axis. ZnO lattice has space group  $P6_3mc$ , with the lattice constants of  $a = b = 3.24 \text{ \AA}$ ,  $c = 5.19 \text{ \AA}$  [2]. Three of the oxygen atoms in the distorted  $\text{ZnO}_4$  tetrahedron are placed in one close-packed  $ab$  plane, whereas the fourth oxygen atom is located in the adjacent plane. As a result, the structure contains an array of vertical Zn-O vectors along the  $c$  axis, resulting in a classical polar structure.

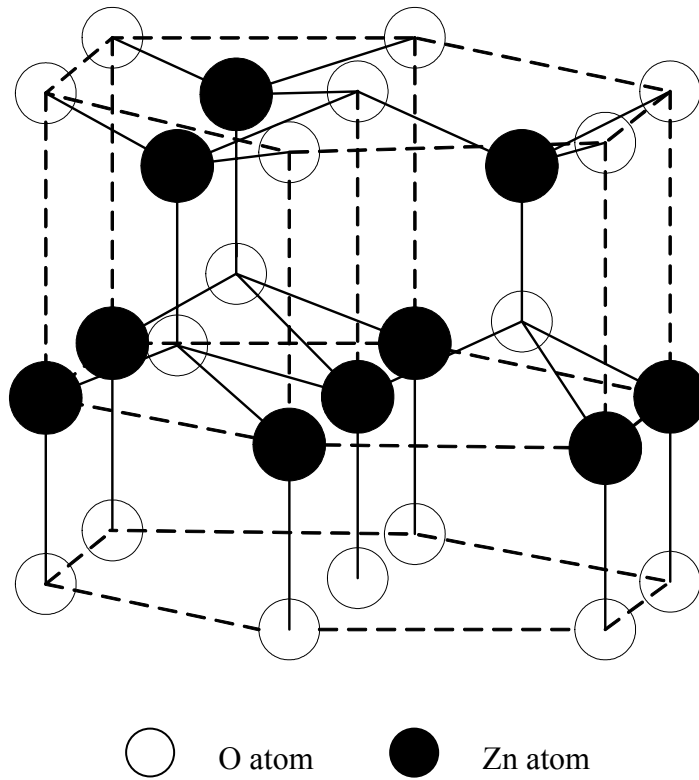


Figure 1.2: Wurtzite structure of ZnO lattice

## 1.2.2 Electronic Structure

$\text{In}_2\text{O}_3$  has a cubic bixbyite structure in which  $\text{O}^{2-}$  ions occupy, in an ordered manner, three-quarters of the tetrahedral interstices of a faced-centered-cubic  $\text{In}^{3+}$ -ion array. Consequently,  $\text{In}_2\text{O}_3$  should consist of a filled  $\text{O}^{2-}:2p$  valence band that is primarily oxygen 2p in character [5]. The In: 3d core lies below the valence band edge ( $E_v$ ). The conduction band is the In: 5s band with an band edge ( $E_c$ ) approximately 3.75 eV above  $E_v$ . As discussed in Section 1.2.1,  $\text{In}_2\text{O}_3$  is usually oxygen-deficient. At high oxygen vacancy concentration, an oxygen vacancy band forms and overlaps  $E_c$  at the bottom of the conduction band such that  $\text{In}_2\text{O}_3$  becomes a degenerated semiconductor [6]. Hereby, the oxygen vacancies act as doubly ionized donors and contribute a

maximum of two electrons to the conduction band. Electrons can also be generated by doping tin into indium oxide to form tin-doped  $\text{In}_2\text{O}_3$ . Since indium has a valence of three, the tin substitution results in an n-type doping by providing an extra electron to the conduction band to preserve the overall charge neutrality.

The second semiconductor of interest is ZnO. The electronic structure of ZnO has been calculated by many researchers. The lowest two valence bands correspond to the  $\text{O}^{2-}$ : 2s core-like states. The next six valence bands correlate to the  $\text{O}^{2-}$ : 2p bonding states. The first two conduction band states are strongly localized on zinc and correspond to the unoccupied  $\text{Zn}^{2+}$ : 4s levels. The higher conduction bands are free-electron-like. The fundamental bandgap, calculated by using band structure models, is  $\sim 3.4$  eV at room temperature [2]. The undoped ZnO is slightly an n-type wide and a direct bandgap semiconductor. The n-type conduction is attributed to the deviation from the stoichiometry. The free carriers are created from the self-donors, associated with the oxygen vacancies and/or interstitial zinc [7, 8]. The donor levels are also produced by the incorporation of foreign atoms such as hydrogen, indium, aluminium, and gallium. It is necessary to fabricate both p-type and n-type ZnO in order to realize bipolar devices from ZnO. However, wide bandgap semiconductors generally have an asymmetric doping problem; that is they can be easily doped to either an n-type or a p-type, but not both. For example, ZnO is easily doped to an n-type with a very high carrier density and low resistance by group III elements [9]. However, p-type doped ZnO is very difficult to achieve [10]. Group V elements such as nitrogen have been considered as acceptor dopants.

## 1.3 Transparent Electronics

In 2003, the invention of the first transparent TFTs with ZnO as channels, marked the birth of transparent electronics [11-13]. Immediately, transparent electronics represented by transparent TFTs becomes one of the most nascent and attractive research areas in thin-film electronics. Continuous efforts have been made to fabricate TFTs with many TOSs including zinc oxide [14, 15], tin oxide [16], indium oxide [17-19], as well as binary or ternary oxide compounds such as zinc-tin oxide [20, 21], zinc-indium oxide [22], zinc-indium-tin oxide [23], and indium-gallium-zinc oxide [24-27]. The field-effect mobility of these TFTs is generally in the range of 10~30  $\text{cm}^2/\text{Vs}$ . Compared with their silicon and organic counterparts, TOS TFTs have much higher field-effect mobility, leading to a higher drain current density which is well suited for current-driven organic light-emitting diode (OLED) displays. Furthermore, low temperature process renders TOS TFTs compatible with future generation of large area electronics that require flexible substrates [24].

Table 1.3 summarizes the available TFT technologies. Compared with amorphous silicon and organic TFTs, TOS TFTs demonstrate the potential for better device characteristics in terms of mobility, leakage current, processing temperature, and transparency as a bonus. With the continuous research and development efforts, TOS TFT technology is believed to be an attractive alternative to existing TFT technologies.

Table 1.3: Comparison of available TFT technologies

	<b>Poly-Si TFT</b>	<b>uc-Si TFT</b>	<b>a-Si:H TFT</b>	<b>Organic TFT</b>	<b>TOS TFT</b>
<b>Circuit Type</b>	CMOS	NMOS	NMOS	PMOS	NMOS
<b>Device Performance</b>					
-Mobility	Good	Good	Poor	Poor	Good
-Leakage Current	Medium	High	Low	Medium	Low
-Uniformity	Poor	Good	Good	Good	Good
-Stability	Good	NA	Poor	Poor	NA
<b>Cost</b>	High	Low	Low	Very low	Medium
<b>Processing Temperature</b>	High	Low	Low	Very low	Very low
<b>Flexible Substrate</b>	Alternative	Promising	Promising	Promising	Promising
<b>Transparent</b>	No	No	No	Can be	Can be

Besides the research on TOS TFTs, some work has been conducted in TOS-based thin-film diodes. The primary application is for ultraviolet (UV) sensors. Wide bandgap semiconductors, including GaN, ZnS, and SiC are commonly used to form solar-blind UV sensors [28]. However, the integration of these devices with CMOS circuits is a complex technological issue. UV sensors based on oxide semiconductors such as ZnO can overcome this obstacle and offer significant advantages in terms of fabrication cost and processing simplicity [29].

### 1.3.1 Research Challenges

The advancement of transparent electronics largely depends on an in-depth understanding of oxide semiconductor physics and chemistry, material and device processing issues, and more important, device physics. In this section, several challenges in transparent electronics are addressed and some of them are the focus of this thesis work.

As discussed previously, most TFTs use ZnO-based oxide semiconductors as channel materials. Very few attempts have been made to fabricate singular indium oxide TFTs. However, the indium oxide TFTs exhibit the highest field-effect mobility of  $\sim 180 \text{ cm}^2/\text{Vs}$ , one order of magnitude higher than the other TOS competitors, and looks promising for TFT applications [18].

The reason for the unpopularity of  $\text{In}_2\text{O}_3$  TFT research is mainly due to the challenge of producing semiconducting indium oxides. Conventional sputtering techniques have been employed as an appropriate technology to prepare most oxide semiconductors including ZnO,  $\text{SnO}_2$ , and other multi-component oxides such as In-Ga-Zn-O. However, it is difficult to deposit semiconducting indium oxide with a low background carrier concentration. Since as a doubly-charged donor, oxygen vacancy doping in indium oxide is more efficient than that in Zn- and Sn-oxide systems [2], it becomes difficult to effectively control the oxygen vacancies in indium oxides and thereby the free carrier density. Consequently, new techniques are pivotal to prepare semiconducting indium oxides for active devices.

Apart from this, a gate dielectric with a low defect density, a high break down voltage, and a highly packed density is another vital factor to achieve high-performance TOS TFTs. To date, a few gate dielectrics have been used in TOS TFTs, including thermally grown  $\text{SiO}_2$  [12, 22], sputtered  $\text{SiO}_2$  [30], laser-ablated  $\text{Y}_2\text{O}_3$  [24], e-beam evaporated  $\text{Al}_2\text{O}_3$  [31], atomic layer deposited  $\text{Al}_2\text{O}_3$  and hafnium oxide [32],  $\text{Al}_2\text{O}_3$  and  $\text{TiO}_2$  superlattices [14, 20], and self-assembled organic polymers [18]. The most commonly-used gate dielectrics in modern TFTs,  $\text{SiO}_x$  and  $\text{SiN}_x$ , deposited by plasma-enhanced chemical vapour deposition (PECVD) are not that popular in TOS



TFTs and the viability of PECVD dielectrics in TOS TFTs remains unproven. There are very few reports on the fabrication of TOS TFTs with PECVD-derived gate dielectrics. Presley et al. have reported indium-gallium oxide TFT circuits with PECVD SiO<sub>x</sub> [33]. Carcia et al. have conducted a comparative study of zinc oxide TFTs with PECVD SiO<sub>x</sub> and SiN<sub>x</sub> dielectrics [34]. Recently, it has been demonstrated at the University of Waterloo, the stable indium oxide TFTs with a PECVD SiO<sub>x</sub> gate dielectric [19]. However, to our knowledge, high-mobility TOS TFTs with PECVD dielectrics have not been reported.

Besides device performance, two other concerns: device stability and dynamic characteristics, have also not well addressed for these TFTs. Even though some preliminary studies on oxide TFTs has been conducted by several groups [19, 35, 36], information on these two issues is sparse and a more detailed study is necessary. Thus, one part of this thesis is dedicated to device stability and dynamic behaviour.

With regards to TOS-based diodes, one serious problem is the imperfection and interfacial defects which cause a very high leakage current. Therefore, the task is to fabricate TOS-based diodes with a decreasing leakage current. In addition to this, an investigation of leakage mechanism in TOS-based diodes is also required.

## **1.4 Organization of the Thesis**

This section describes the organization of this thesis. First, Chapter 2 is a discussion of IBAE as the fabrication technique in this research. After the introduction of the deposition system, some key deposition parameters are described.

In Chapter 3, a detailed material study for both ZnO and In<sub>2</sub>O<sub>3</sub> is conducted. The electrical properties, chemical composition, optical properties, crystal structure, intrinsic stress, topology, and morphology, are measured in order to fully examine the material properties by the IBAE.

Thin-film devices are demonstrated by employing optimized semiconducting oxide thin films. In Chapter 4, ZnO-based heterostructure diodes are fabricated and characterized. The device analysis including current-voltage characteristics, current transients, leakage current, and spectral response, is followed.

Chapter 5 details indium oxide TFTs with gate dielectrics by PECVD. The device analysis includes transfer and output characteristics, device stability, and dynamic behaviour.

Lastly, Chapter 6 concludes this thesis and summarizes its contribution to the field of transparent electronics.

# Chapter 2

## Fabrication Technique

This chapter describes the fabrication technique for developing TOSs. After a brief introduction of the IBAE technique, the schematic structure of the system is presented. Since the ion source is a very important unit in such a system, one section is devoted to the working principle of the ion source. In the last section, a discussion of the deposition parameters is given.

### 2.1 Introduction

IBAE deals with the use of energetic ions to assist the growth of thin films. It combines a traditional evaporation technique with an independent ion source, providing more capability in thin-film growth and processing.

Generally, the bombardment of a growing film with energetic particles has been recognized to produce significant modification such as improved adhesion, densification, texture, grain size, crystallinity, and morphology in thin-film properties [37]. Here, the energetic particles refer to those with kinetic energies that are typical of ion beam assistance processing; that is from a few tens to approximately one thousand electron volts (eV). For the purpose of substrate pretreatment or precleaning, a few tens of eV is enough to remove most of the physical and chemical adsorbed contaminants and moisture. Regarding the assistance of thin-film growth, a kinetic energy as much as one thousand eV is suitable and avoids plasma damaging and etching. Since most particles are ions and radicals, throughout this thesis, the term,

ion, is used for the impinging particles that assist thin-film growth. However, it is noteworthy that ion refers to two particles: ions and radicals. An independent ion source also offers the possibility of realizing reactive evaporation. For instance, in the preparation of oxides, an oxygen ion source can provide reactive oxygen ions during the oxide growth. Compared with a conventional reactive evaporation, immersed in an oxygen atmosphere, reactive IBAE is more feasible for low temperature deposition and more effective control in the stoichiometry.

## **2.2 Ion Beam Assisted Evaporation**

The IBAE technique can be realized in several experimental configurations. In general, it consists of an independent ion source and a traditional evaporator. The ion source can be in different types such as Kaufman-type ion source, End-Hall ion source, and plasma-based ion source [38]. Evaporation can be carried out either by the resistive heating of a crucible or more efficiently, by the electron beam (e-beam) bombardment of a bulk solid.

### **2.2.1 Schematic Configuration of the IBAE system**

A typical IBAE system is illustrated schematically in Figure 2.1. It consists of dual chambers: the main vacuum chamber and the loadlock chamber. An evaporator and ion source are housed in the main chamber. The roughing pump and cryopump serve the system with a base pressure down to  $\sim 10^{-6}$  torr. The gas introduced into the system generates a desirable range of working pressure of approximately  $10^{-3} \sim 10^{-4}$  torr. The loadlock chamber separates the sample holder and main chamber by a loadlock gate

to facilitate an efficient pumping to attain the base pressure. The equipped quartz crystal sensor is used to in-situ monitor the thickness and evaporation rate during film growth. In some systems, the Faraday cup is employed to measure the ion beam flux and energy simultaneously. An independent ion source allows the independent control of the ion type, energy, and flux, which ultimately provides the capability to deposit different kinds of materials.

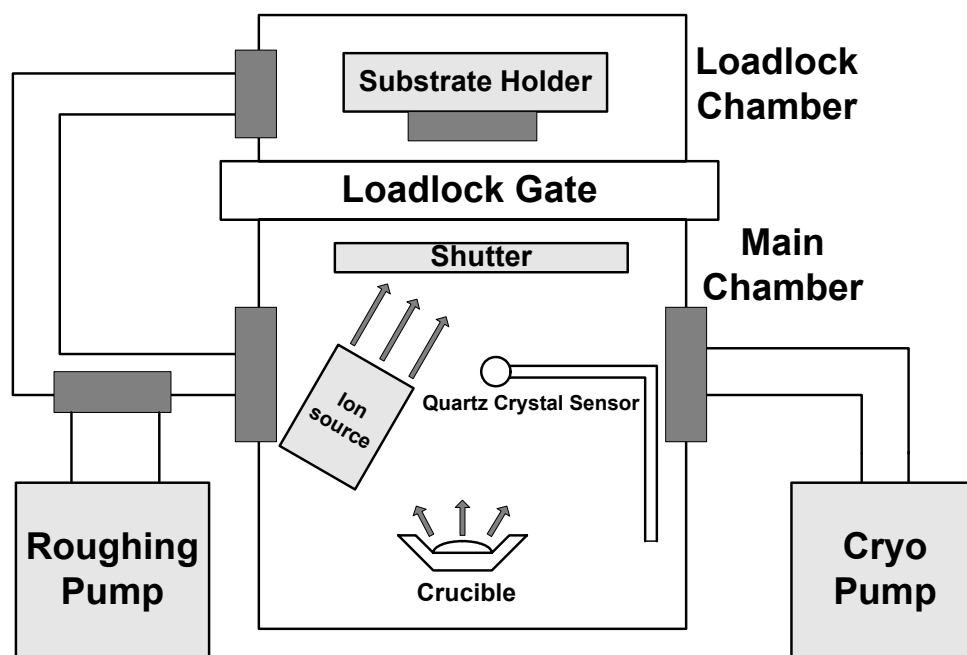


Figure 2.1: Schematic structure of a typical IBAE system

### 2.2.2 Reactive IBAE

Thanks to more reliable ion sources, reactive IBAE technique is developing rapidly in thin-film fabrication, particularly in the low temperature deposition of oxides and nitrides. A high portion of ion beam processing deals with an inert gas such as Ar, He, and Ne. The ion effects are mainly physical. In a traditional reactive evaporation, oxygen or nitrogen gas is introduced into the vacuum chamber. It can be less efficient,

since the oxygen or nitrogen is in the form of atom, not as radical and reactive as oxygen or nitrogen plasma. Reactive ion assisted evaporation, however, uses oxygen or nitrogen ions as reactants and it is a technique that is emerging for the fabrication of many oxide or nitride compounds at low temperatures.

The system adopted in this research includes a typical e-beam evaporator and an independent oxygen ion source. The distance between the substrate and evaporation source is fixed at 35 cm. The oxygen ion source module is located 20 cm below the substrate with an incident angle of  $60^{\circ}$ . The water-cooling coils surrounding the sample holder maintains a substrate temperature below  $40^{\circ}\text{C}$ , principally coming from the oxygen plasma heating during deposition. Figure 2.2 and Figure 2.3 are photographs of the IBAE system and the main chamber during deposition.



Figure 2.2: IBAE system used in this research

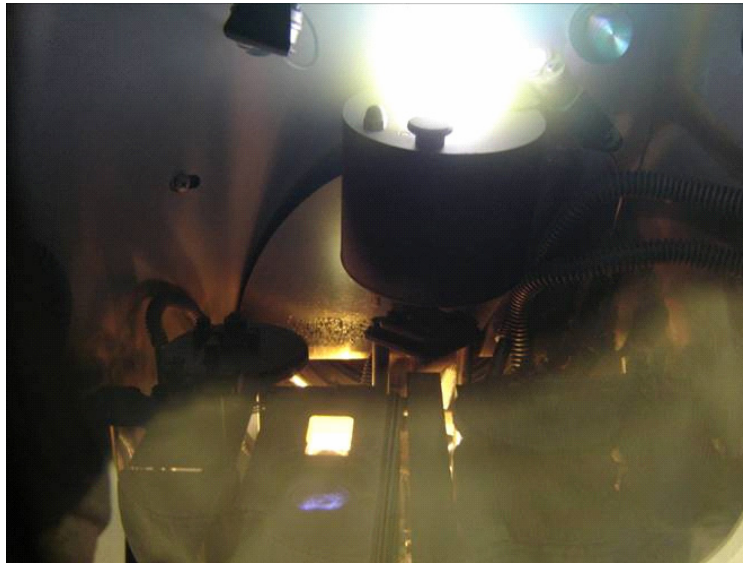


Figure 2.3: Main chamber during deposition

### **2.2.3 Oxygen Ion Source**

The ion source plays a very important role in the reactive IBAE. Several commercially-available ion sources exist for different applications. The most commonly-used ion sources include the Kaufman-type ion source, End-Hall ion source, and filament-less ion source. The difference between each ion source lies in the mechanism and set-up of its plasma generator. The oxygen ion source in our IBAE system is the Kaufman-type ion source. Figure 2.4 is a schematic diagram of the oxygen ion source. The module includes a hollow cathode electron source, where the keeper tube generates a high voltage between the cathode tip and the keeper to ionize the Ar gas. The keeper first initiates the discharge of the Ar gas into the hollow cathode electron source. Once the bias voltage is applied, electrons flow toward the anode, but are prevented from flowing directly to the positive anode by the magnetic

field. The electrons bombard the oxygen gas to create the oxygen ions. They are then accelerated by the discharge voltage and reach the substrate.

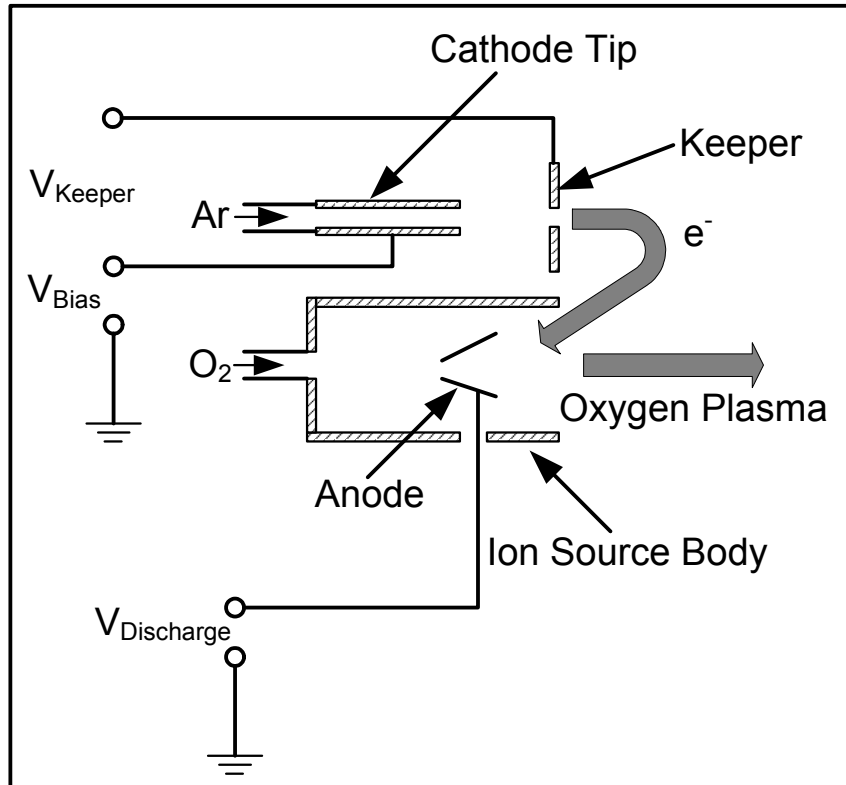


Figure 2.4: Schematic diagram of oxygen ion source

## 2.3 Deposition Parameters

The deposition rate, ion beam energy and flux, dynamic pressure, and substrate temperature are among the deposition parameters, determining the film properties. Table 2.1 gives the deposition parameters of the IBAE technique used in this research.

Since the material properties such as resistivity and transparency correlate to the composition of the films, the ratio between the ion flux and arrival atoms from the evaporation source becomes the most important factor in the reactive IBAE.



Therefore, in the material development, the idea is to control the film properties by simply modifying the oxygen ion beam flux, ion beam energy, and metal evaporation.

Table 2.1: Deposition parameters of the IBAE technique

<b>Parameters</b>	<b>Typical Range</b>	<b>Comments</b>
Deposition Rate	0.5 ~ 4 Å/s	It varies with the metal evaporation and oxygen ion flux.
Discharge Current	0.5 ~ 3.0 A	It is proportional to the ion flux with a density ranging from 0.025 mA/cm <sup>2</sup> to 0.1 mA/cm <sup>2</sup> .
Discharge Voltage	80 ~ 180 V	It is proportional to the ion beam energy with a range of 50 to 130 electron volts.
Substrate Temperature	30 ~ 40 <sup>0</sup> C	It is due to plasma heating during deposition.
Dynamic Pressure	0.1 ~ 1 mTorr	It is adjusted with a flow rate of O <sub>2</sub> (5 ~ 20 sccm); The flow rate of Ar stays at 10 sccm during deposition.

# Chapter 3

## Material Study

This chapter describes the preparation, characterization, and optimization of TOSs. Two widely-used TOSs are fabricated. One is ZnO and the other is In<sub>2</sub>O<sub>3</sub>. The correlations between deposition conditions and thin-film properties are also investigated.

### 3.1 Zinc Oxide

#### 3.1.1 Introduction

Zinc oxide thin films are deposited by the reactive IBAE [39]. A high-purity zinc metal is chosen as the evaporation source, and the oxygen reactants are introduced in the forms of oxygen ions, generated by the oxygen ion source. The discharge voltage and current of the ion source are proportional to the oxygen ion energy and flux, respectively. The electrical and optical properties of IBAE-derived ZnO thin films are examined in the following sections.

#### 3.1.2 Deposition Rate

In the reactive IBAE, the deposition rate depends on the number of arrival atoms and their migration on the substrate. The arrival mass and migration are determined by the evaporation rate of zinc, the oxygen ion flux, and the oxygen ion energy. The IBAE system has a deposition controller and quartz crystal sensor to set the deposition rate

while the actual evaporation is monitored. The measured deposition rate can differ from the set deposition rate. Therefore, the first thing that should be done is to calibrate the deposition rate before each deposition.

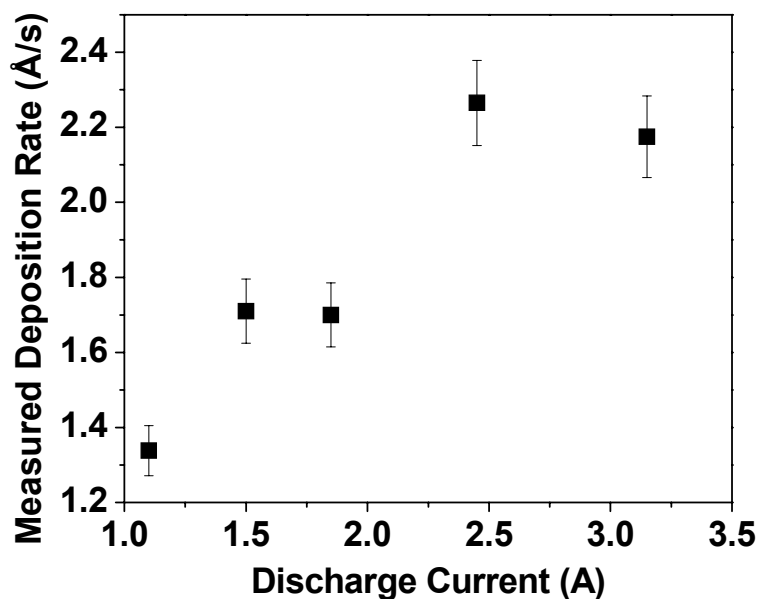


Figure 3.1: Deposition rate calibrated in terms of the discharge current

Figure 3.1 denotes the calibration of the deposition rate in terms of the discharge current. The measured deposition rate varies slightly from the deposition rate (1.5 Å/s) set in the deposition controller. The measured deposition rate increases with the discharge current, which is reasonable because the greater the ion beam flux, the greater the film growth.

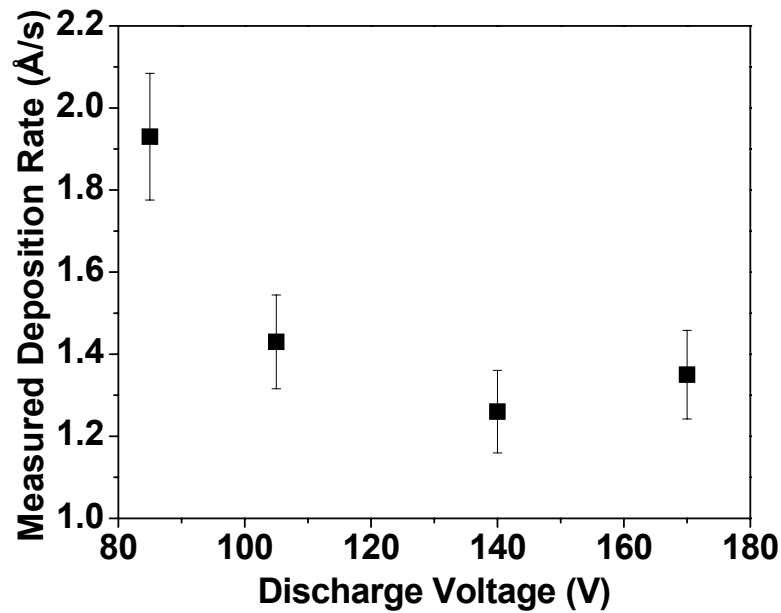


Figure 3.2: Deposition rate calibrated in terms of the discharge voltage

Similarly, the deposition rate is also calibrated in relation to the discharge voltage, which is proportional to the ion beam energy as observed in Figure 3.2. The set deposition rate is 1.5 Å/s. Here, the measured deposition rate decreases with the discharge voltage due to the atom peening effects which high-energy ions usually display [38]. Therefore, a low or modest discharge voltage is preferred in order to avoid any plasma damaging during deposition.

### 3.1.3 Electrical Properties

Since the primary goal of this chapter is to develop semiconducting ZnO thin films for active device applications, the first priority is to study the electrical properties: the resistivity of IBAE-derived ZnO thin films and the dependence of resistivity on the deposition parameters.

The ZnO films are deposited on Corning 1737 glass substrates for resistivity evaluation. All the films have a thickness of approximately 100 nm. The resistivity measurements are performed by sputtering Molybdenum (Mo) on the top of the ZnO films through a shadow mask on which the electrode patterns are defined by different widths and lengths. The resistivity of ZnO films is then extracted from the current-voltage curves by microprobing the electrodes.

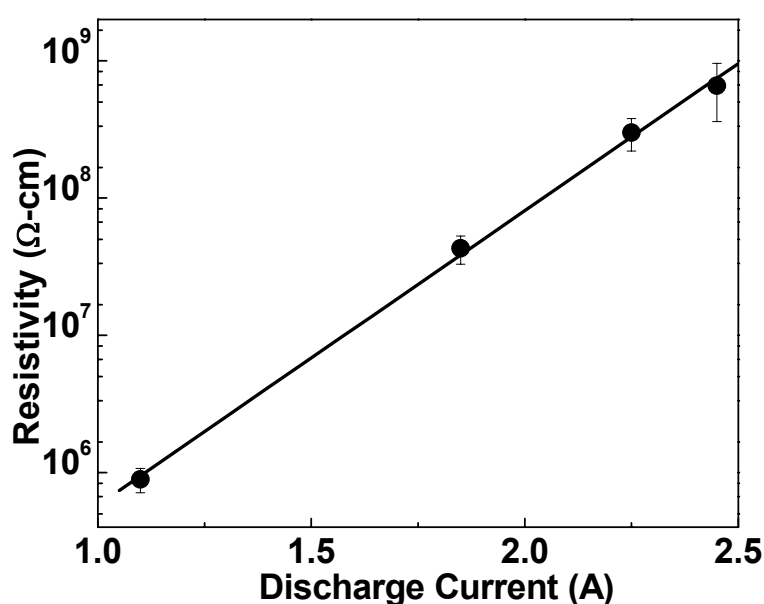


Figure 3.3: Resistivity of the ZnO films as a function of the discharge current

Figure 3.3 illustrates the dependence of the ZnO resistivity on the discharge current. The deposition rate and discharge voltage are maintained at the constants of 1.5 Å/s and 120 V, respectively. By increasing the discharge current, the resistivity of the ZnO films increases from  $9 \times 10^5$  Ω-cm to  $7 \times 10^8$  Ω-cm. Since the discharge current is proportional to the ion beam flux, the oxygen vacancy concentration inside ZnO films also rises with the discharge current.

Figure 3.4 depicts the resistivity of the ZnO films as a function of the discharge voltage. The deposition rate and discharge current are fixed at 1.5 Å/s and 2.5 A, respectively. The resistivity does not change when the discharge voltage is in the range of 80 V to 180 V, suggesting that the discharge voltage is not a determining parameter, in particular, for the resistivity.

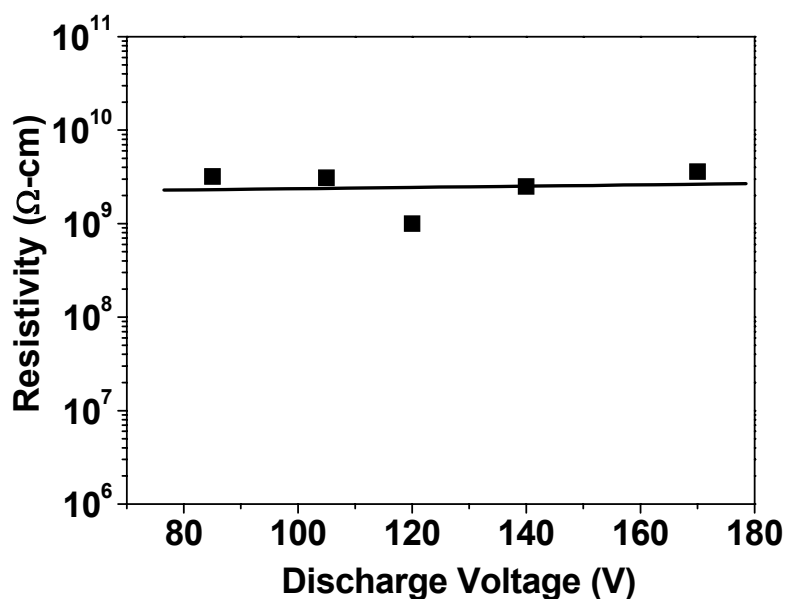


Figure 3.4: Resistivity of the ZnO films as a function of the discharge voltage

Active semiconductor devices such as TFTs require semiconducting films with a low background carrier concentration and high carrier mobility. The experimental results in this thesis indicate that by simply modifying the discharge current, it is possible to achieve semiconducting ZnO thin films with a resistivity ranging from  $10^6$  Ω-cm to  $10^8$  Ω-cm that is appropriate for device applications. To avoid high-energy ion damage, a modest discharge voltage of 100~120 V should be chosen for the following semiconducting film deposition.

### 3.1.4 Optical Properties

In this section, the optical properties of the IBAE-derived ZnO thin films are investigated. After the optical transmittance and optical constants of the ZnO films are measured, the optical bandgaps of the ZnO thin films are extracted from an absorption model. The optical transmittance is measured by a Shimadzu UV/Vis spectrometer (UV-2501PC) in a wavelength range of 300 to 800 nm with a measurement resolution of 1 nm. The film thickness for the transmittance measurements is around 100 nm.

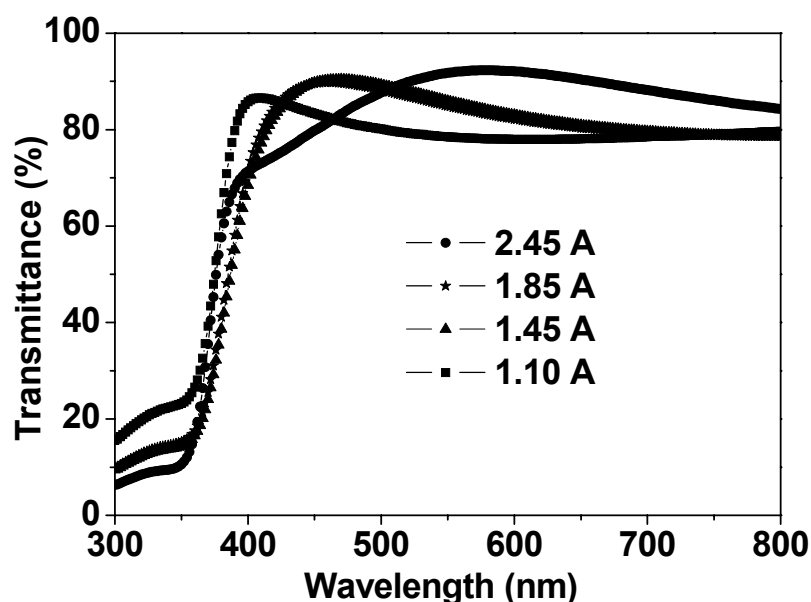


Figure 3.5: Transmittance spectra of the 100 nm ZnO films deposited at different discharge currents

Figure 3.5 plots the transmittance spectra of the 100 nm ZnO thin films, deposited at different discharge currents. The discharge voltage and deposition rate are set at 120 V and 1.5 Å/s, respectively. Figure 3.6 displays the transmittance of the 100 nm

ZnO films, deposited at different discharge voltages. The deposition rate and discharge current are kept constants at 1.5 Å/s and 2.25 A, respectively.

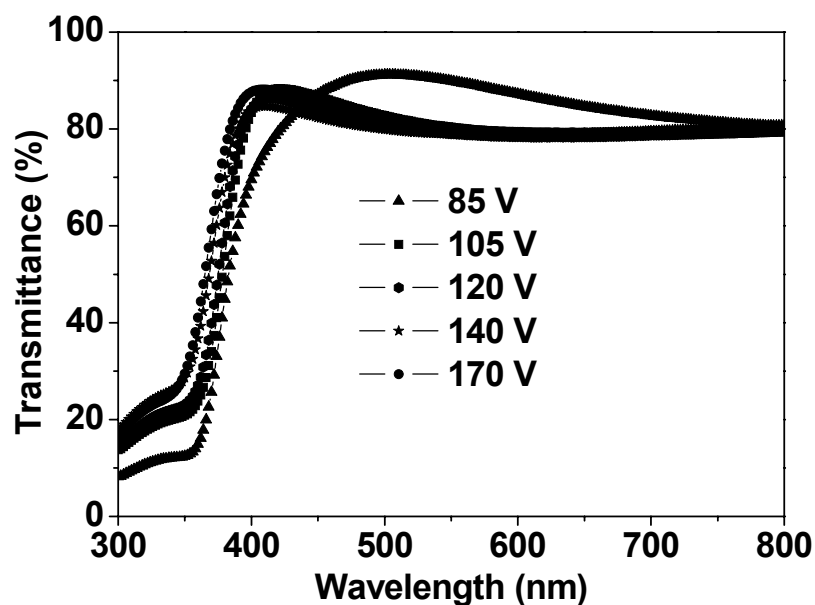


Figure 3.6: Transmittance spectra of the ZnO films deposited at different discharge voltages

In the visible region, with a wavelength ranging from 400 to 700 nm, all the ZnO films are highly transparent with an average transmittance of more than 85%, and the transmittance spectra are not very dependent on either the discharge current or the discharge voltage.

Another optical parameter, refractive index ( $n$ ) as a function of the visible wavelength, is also evaluated. The refractive index is measured by a spectroscopic ellipsometer, produced by J. A. Woollam Co.. The value of  $n$  should slightly increase with the decrease of the wavelength in the visible region due to dispersion effects [2].



The best fit for the refractive index as a function of the wavelength is to use the following three-term Cauchy equation [29]:

$$n(\lambda) = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4}, \quad (3-1)$$

where A, B, and C are parameters that fits the Cauchy model.

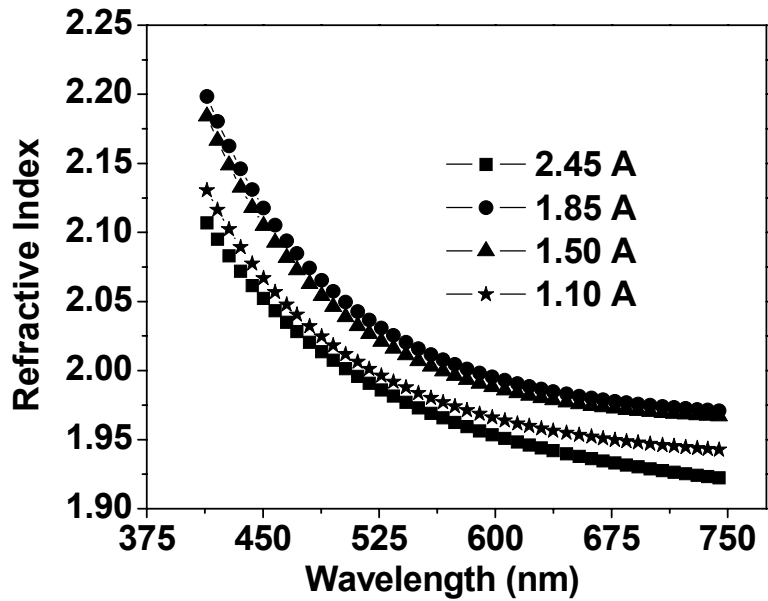


Figure 3.7: Variation of the refractive index with the wavelength of the ZnO films deposited at different discharge currents

Figure 3.7 presents the variation of the refractive index with the wavelength of the ZnO films, deposited at different discharge currents with a fixed deposition rate of 1.5 Å/s and a discharge voltage of 120 V. Figure 3.8 gives the refractive index as a function of the wavelength of the ZnO deposited at different discharge voltages, whereas the deposition rate and discharge current are selected as 1.5 Å/s and 2.25 A, respectively. As observed, the refractive index depends very little on the discharge

current or discharge voltage. The index ranges from 1.90 to 2.20 in the visible region, which is consistent with the results in the literature, and is close to the refractive index of the bulk ZnO [2]. In this wavelength range, the extinction coefficient can be negligible because all the films are highly transparent with very weak absorption.

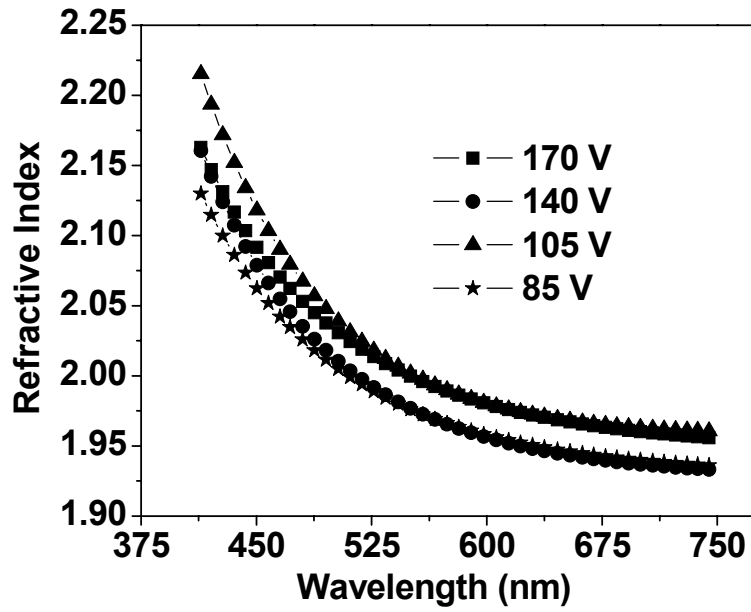


Figure 3.8: Dependence of the refractive index on the wavelength of the ZnO films deposited at different discharge voltages

The optical bandgap of the ZnO films can be extracted according to the direct band-to-band transition model [2]:

$$(h\nu\alpha)^2 = \alpha_0(h\nu - E_{gap}), \quad (3-2)$$

where  $h\nu$  is the photon energy,  $\alpha$  is the absorption coefficient,  $\alpha_0$  is approximately a constant that is independent of the photon energy, and  $E_{gap}$  is the optical bandgap.

The curve  $(hv\alpha)^2$ , in terms of  $hv$  extrapolated to zero, yields the value of  $E_{gap}$ .  $\alpha$  is obtained from the transmittance by the relation [2]:

$$T = (1 - R)^2 \exp(-\alpha t), \quad (3-3)$$

where  $T$  is the transmittance,  $R$  is the reflectance, and  $t$  is the film thickness. By assuming  $R \ll 1$  in the absorption region of the ZnO films, the absorption coefficient is simplified to:

$$\alpha = \frac{1}{t} \ln\left(\frac{1}{T}\right). \quad (3-4)$$

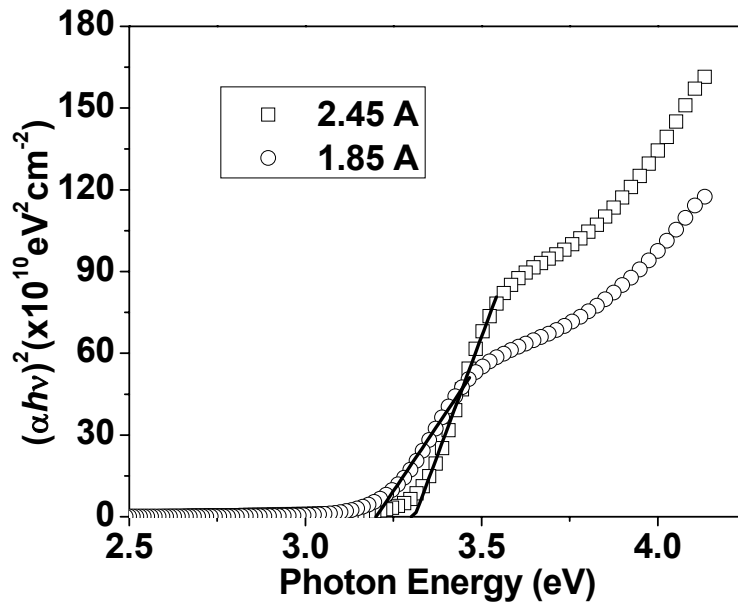


Figure 3.9: Representative absorption curves of the ZnO films deposited at the discharge of 2.45 A and 1.85 A for the optical bandgap extraction

Figure 3.9 sketches two representative absorption curves of the ZnO films for the optical bandgap extraction. The 100 nm films are deposited at a deposition rate of 1.5 Å/s and discharge voltage of 120 V, and the two discharge currents of 1.85 A and

2.45 A, respectively. The extracted optical bandgap is around 3.2 eV for the 1.85 A film and 3.3 eV for the 2.45 A film, both very close to those reported undoped ZnO films in the literature [2].

### 3.1.5 Crystal Structure

The crystal structure of the deposited semiconducting ZnO film is obtained by performing x-ray diffraction (XRD) measurements with a Rigaku D/MAX 2000 x-ray diffractometer (Source: Cu  $K\alpha_1$  with a wavelength of 1.54056 Å; Tube voltage: 50 kV; and Tube current: 40 mA).

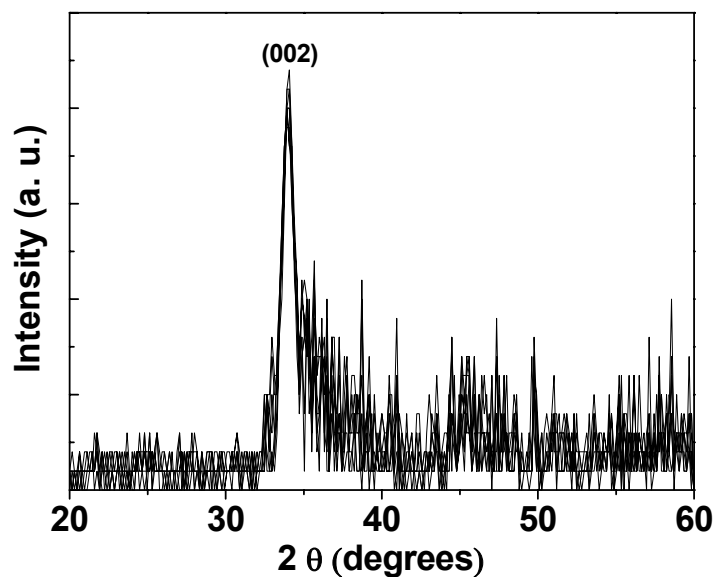


Figure 3.10: XRD patterns of the semiconducting ZnO film

Figure 3.10 reflects the XRD patterns with  $2\theta$ , ranging from  $20^\circ$  to  $60^\circ$  of the semiconducting ZnO film, fabricated at a discharge current of 2.25 A, discharge voltage of 120 V, and deposition rate of 1.5 Å/s. Only the (002) peak at  $2\theta \approx 34^\circ$  is

observed, identifying the formation of the ZnO film with a hexagonal structure and a preferred orientation with the c-axis perpendicular to the substrate. Calculated from the Scherrer formula:

$$D = \frac{K\lambda}{B_{1/2} \cos \theta}, \quad (3-5)$$

in which  $D$  is the average grain size,  $\lambda$  is the wavelength of the incident x-ray,  $K$  is a numerical constant from 0.95 ~ 0.98,  $\theta$  is the Bragg angle, and  $B_{1/2}$  is the full-width half-maximum, the estimated average grain size is around 13 nm.

## 3.2 Indium Oxide

Indium oxides are also fabricated by the reactive IBAE [40]. A high-purity indium is used as the evaporation source. The electrical properties are first characterized, followed by the chemical composition, optical properties, crystal structure, intrinsic stress, topology, and morphology.

### 3.2.1 Electrical Properties

In the reactive IBAE, in order to achieve semiconducting indium oxides for the active device applications, the oxygen vacancy concentration must be restrained as discussed in Section 1.2.2. Therefore, the indium and oxygen atom arrival ratio to the substrate are modified by adjusting two most important deposition parameters: deposition rate and oxygen ion flux.

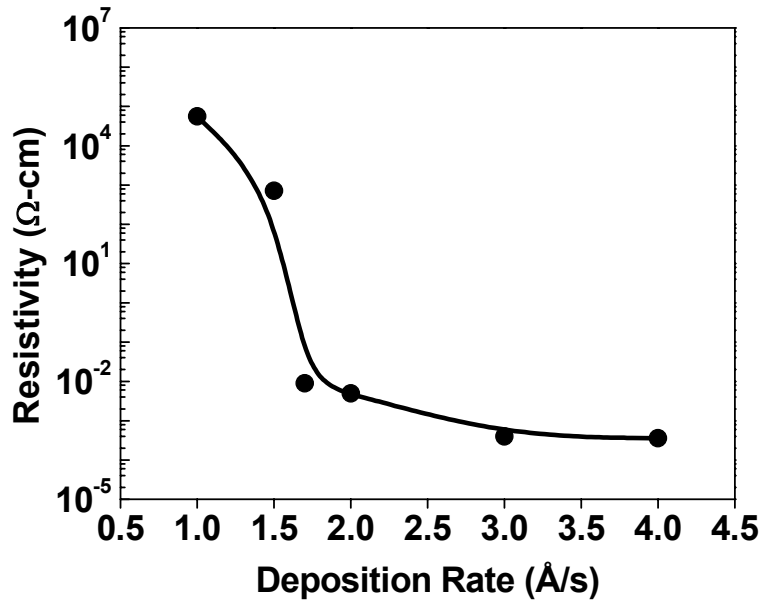


Figure 3.11: Dependence of the resistivity of the indium oxide films on the deposition rate

Figure 3.11 illustrates the dependence of the resistivity on the deposition rate. All the indium oxide films are deposited on Corning 1737 glass substrates with a thickness of  $\sim 100$  nm. The discharge voltage and current of oxygen ion source are kept at 100 V and 1.0 A, respectively. As seen in Figure 3.11, the resistivity of the indium oxide films can be tuned from  $10^5$   $\Omega\text{-cm}$  down to  $10^{-4}$   $\Omega\text{-cm}$  by simply increasing the deposition rate. At a deposition rate higher than 3  $\text{\AA}/\text{s}$ , the resistivity approaches a stable value of  $5 \times 10^{-4}$   $\Omega\text{-cm}$ , on par with the current TCOs for flat-panel displays [2]. At lower deposition rates, the resistivity undergoes a sharp transition from the conducting ( $\sim 10^{-2}$   $\Omega\text{-cm}$ ) to the semiconducting states ( $\sim 10^3$   $\Omega\text{-cm}$ ), suggesting a critical oxygen vacancy concentration that causes a shift of the Fermi-energy level from close to the conduction band down to close to the mid-bandgap.

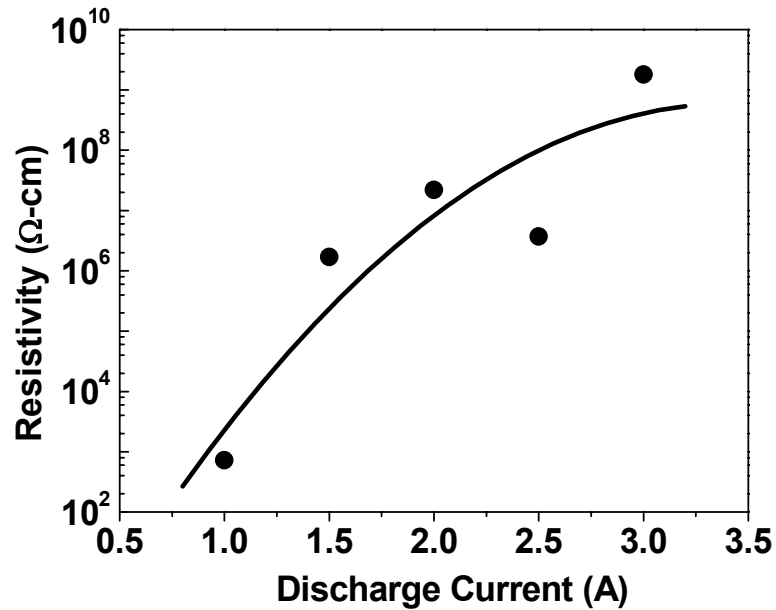


Figure 3.12: Variation of the resistivity of the indium oxide films with the discharge current

Figure 3.12 exhibits the variation of the resistivity of the indium oxide films with the discharge current. The deposition rate and discharge voltage are set at 1.5 Å/s and 100 V, respectively. In non-stoichiometric indium oxides, the oxygen vacancies act as doubly-charged donors [2]. Therefore, a small discharge current: that is less oxygen ions, tends to generate a high population of oxygen vacancies, and consequently, a low resistivity. In contrast, a large discharge current helps decrease the population of the oxygen vacancies, leading to an increased resistivity. Moreover, it is found that the resistivity of the indium oxide films can reach values as high as  $10^9$  Ω-cm, which is difficult to achieve with conventional sputtering or evaporation. Thus, the IBAE allows the engineering of the resistivity of indium oxides from metallic to insulating. Such a wide range of variation in the resistivity also indicates that the defect density

in these films is not that high, and the Fermi-energy level is not pinned, such that it can be shifted from the conduction band edge to close to the mid-bandgap.

### 3.2.2 Compositional Analysis

To verify that the oxygen concentration inside the films changes with the deposition conditions and to identify how the concentration depends on the oxygen ion flux, x-ray photoelectron spectroscopy (XPS) measurements are performed in a multiple-technique ESCA microprobe system (VG ESCALab 250). In addition, XPS can be used to identify the chemical bonding states of the indium oxides.

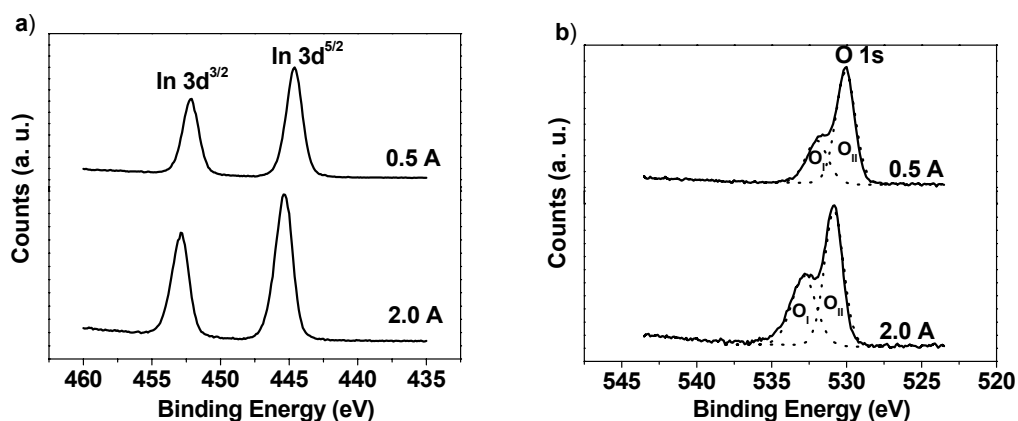


Figure 3.13: XPS spectra of (a) In 3d and (b) O 1s of the indium oxide films deposited at two different discharge currents of 0.5 A and 2.0 A

Figure 3.13 depicts the XPS spectra of In 3d and O 1s of the indium oxide films, deposited at the two different discharge currents of 0.5 A and 2.0 A for comparison. The binding energy of In 3d<sup>5/2</sup> and In 3d<sup>3/2</sup> is located at 444.6 eV and 452.2 eV for the 0.5 A film, similar to that of ITO reported elsewhere [5, 41]; and 445.3 eV and 452.9 eV for the 2.0 A film. A shoulder peak appears adjacent the main peak of the O



1s spectra in both samples, as shown in Figure 3.13 (b). Two Gaussian functions with variable positions and intensities are used to deconvolute each spectrum, where the two resolved peaks in the O 1s spectrum are located at 530.1 eV and 531.9 eV for the 0.5 A film, and 530.8 eV and 532.7 eV for the 2.0 A film. Both the In 3d and O 1s spectra shift towards the lower binding energy by decreasing the oxygen ion flux. It is indicated that the oxygen bonding states depend more strongly on the discharge current compared with the In bonding states. Also from the XPS spectra, two types of  $O^{2-}$  ions are distinguished:  $O_I$  and  $O_{II}$ . The main peak of  $O_{II}$  is related to the O-In state, where the In atoms with the six closet  $O^{2-}$  ions form the  $InO_6$  octahedra. The subpeak of  $O_I$  with a higher binding energy is associated with an O-In binding state in the oxygen-deficient region [5]. Consequently,  $O_I$  is more sensitive to the loss of oxygen. Compared with the integrated areas of the In  $3d^{5/2}$  and O 1s peaks, the relative atomic ratio between indium and oxygen can be calculated. This ratio is 0.61 for the 0.5 A film and 0.53 for the 2.0 A film. Thus, by tuning the oxygen ion flux, the stoichiometry of indium and oxygen inside the film can be varied. The more oxygen-deficient film is obtained at a smaller discharge current and the more oxygen-rich film is achieved at a larger discharge current, which is also in line with the resistivity results. For the TCO applications, the more oxygen-deficient film with a high conductivity is needed, whereas for the device applications, oxygen-rich films with a low electron density are desirable.

### 3.2.3 Optical Properties

The visible transmittance, the refractive index, and the extracted optical bandgap of indium oxides are presented. The measurements and extraction are similar to those for the ZnO films. The details are found in Section 3.1.4.

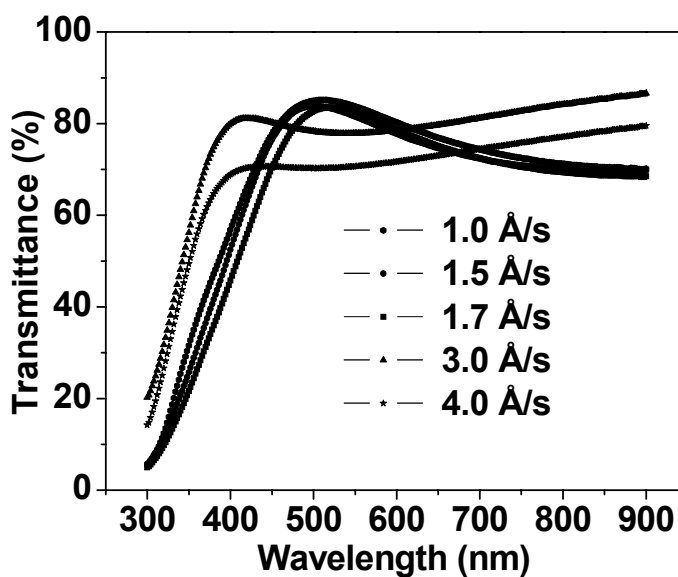


Figure 3.14: Transmittance spectra of the indium oxide films deposited at different deposition rates

Figure 3.14 shows the transmittance of the indium oxide films, deposited at different deposition rates. The discharge voltage and current are fixed at 100 V and 1.0 A, respectively. The film thickness is approximately 100 nm. The wavelength ranges from 300 to 900 nm. An average visible transmittance of more than 80 % is achieved for all the derived indium oxide films. The strong near-UV absorption is observed due to the band-to-band transition. Also, it is found that the transmittance spectra of the indium oxide films, fabricated at a higher deposition rate demonstrate

the blue shift: that is the transmittance spectrum shifts towards short wavelengths.

This can be due to Burstein-Moss effect described as [2]:

$$E_g - E_{g0} = \frac{(\pi\hbar)^2}{2m_r^*} \left(\frac{3N}{\pi}\right)^{2/3} \quad (3-6)$$

where  $E_g$  is the optical bandgap,  $E_{g0}$  is the intrinsic optical band gap,  $m_r^*$  is the effective mass, and  $N$  is the free carrier density. The shift towards shorter wavelengths is caused by the increased free carrier density in the films with the deposition rates of 3 Å/s and 4 Å/s.

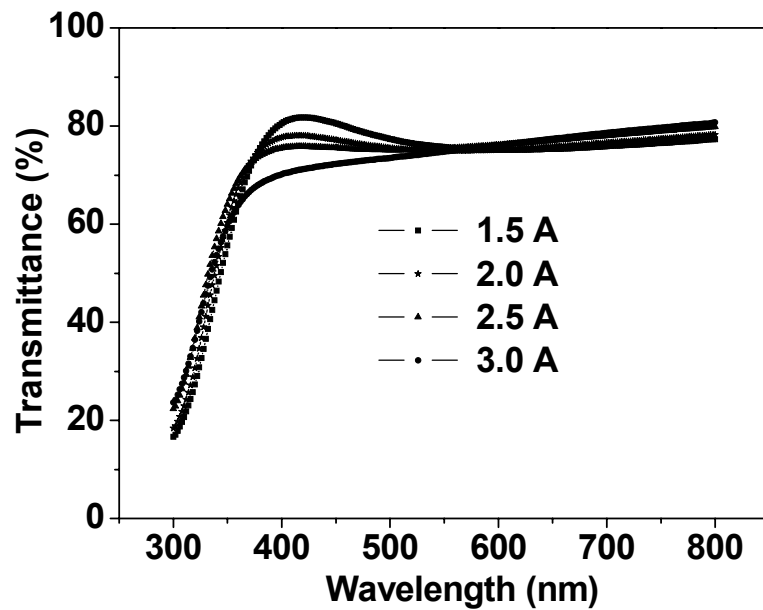


Figure 3.15: Transmittance spectra of the indium oxide films deposited at different discharge currents

Figure 3.15 illustrates the transmittance of the indium oxide films, deposited at different discharge currents. The deposition rate and discharge voltage are kept constants at 1.5 Å/s and 100 V, respectively. The thickness of all the deposited films

is approximately 100 nm. The transmittance varies little with the discharge current for the semiconducting indium oxides with an overall average visible transmittance of around 80%. The blue shift is not observed since the indium oxides, deposited under these conditions, are not degenerated and the free carrier density is not that high.

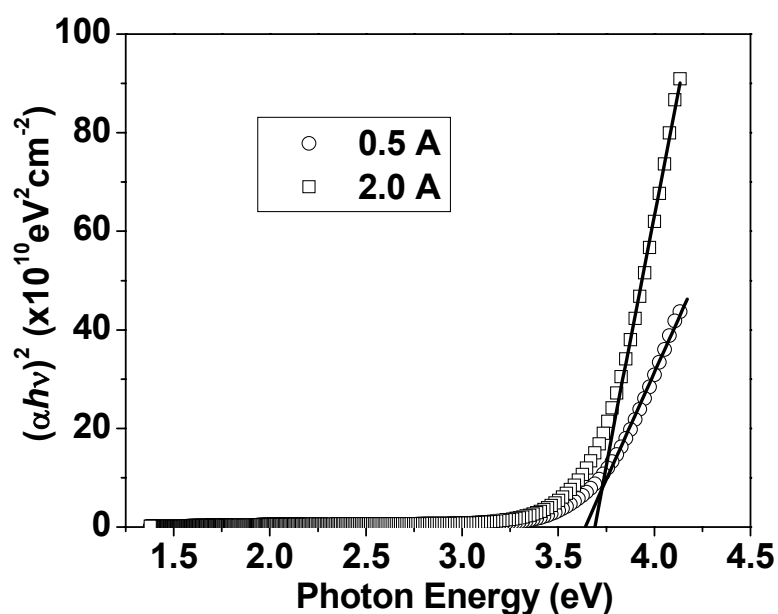


Figure 3.16: Representative absorption curves of the indium oxides deposited at the discharge currents of 0.5 A and 2.0 A for the optical bandgap extraction

Figure 3.16 conveys the direct optical bandgap extraction for the indium oxides, deposited at the discharge currents of 0.5 A and 2.0 A, while the deposition rate and discharge voltage remain at 1.5 Å/s and 100 V, respectively. The bandgap is retrieved from the transmittance data by extrapolating the linear part of the  $(\alpha h\nu)^2$  versus the photon energy  $h\nu$  plot to the absorption coefficient,  $\alpha = 0$ , as seen in Figure 3.16, yielding 3.6~3.7 eV for both the conducting and semiconducting indium oxides. This value is also close to that reported in the literature [2].

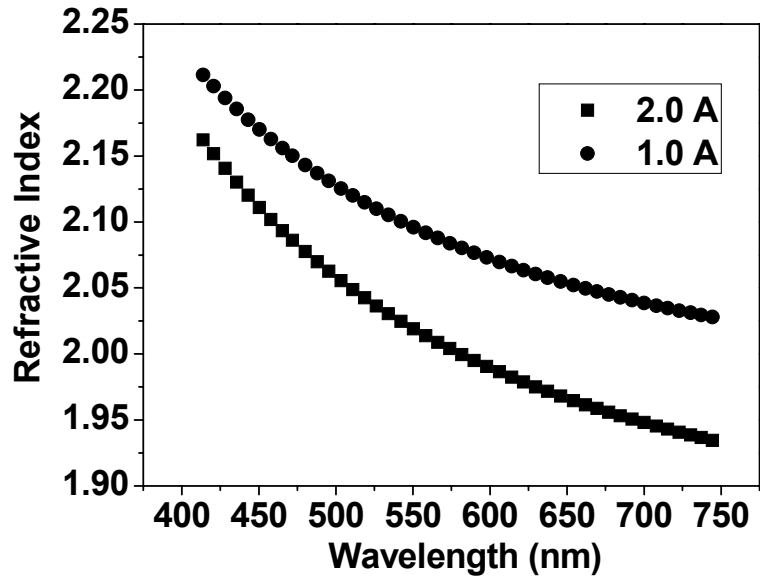


Figure 3.17: Refractive index of the indium oxides fabricated at two different discharge currents

The refractive index in the relation to the wavelength curves of the indium oxides fabricated at two different discharge currents are shown in Figure 3.17. The deposition rate and discharge voltage are chosen as  $1.0 \text{ \AA/s}$  and  $100 \text{ V}$ , respectively. Figure 3.18 presents the refractive index as a function of the wavelength of the indium oxides deposited at two different deposition rates. The discharge voltage and current are kept at  $100 \text{ V}$  and  $1.0 \text{ A}$ , respectively. The refractive index ranges from 2.30 to 1.95. The value slightly varies with the deposition conditions. Since the discharge current and deposition rate in the reactive IBAE affect the chemical composition of indium oxides, it is anticipated that the refractive index is dependent on the oxidation: that is more oxidized samples have the relatively smaller refractive index.

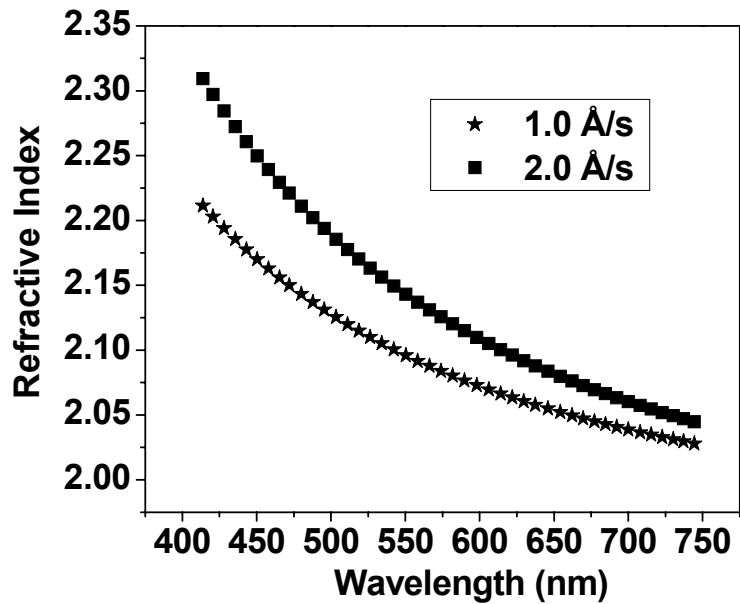


Figure 3.18: Refractive index of the indium oxides deposited at two different deposition rates

### 3.2.4 Crystal Structure

The crystal structure of the indium oxides are evaluated by the XRD technique performed by the same diffractometer described in Section 3.1.5. The structural order of the films is significantly dependent on the discharge current. Figure 3.19 signifies the XRD patterns of the indium oxide films, deposited at different discharge currents: 0.5 A, 1.5 A, and 2.0 A. The deposition rate and discharge voltage are kept constants at 1.5 Å/s and 100 V. The 1.5 A and 2.0 A films are polycrystalline with a dominant (222) orientation, whereas the 0.5 A film is amorphous in nature. As observed from the increased number of diffraction peaks, a large discharge current helps improve the structural ordering. The estimated grain size for the 2.0 A film is around 12 nm from the Scherrer formula.

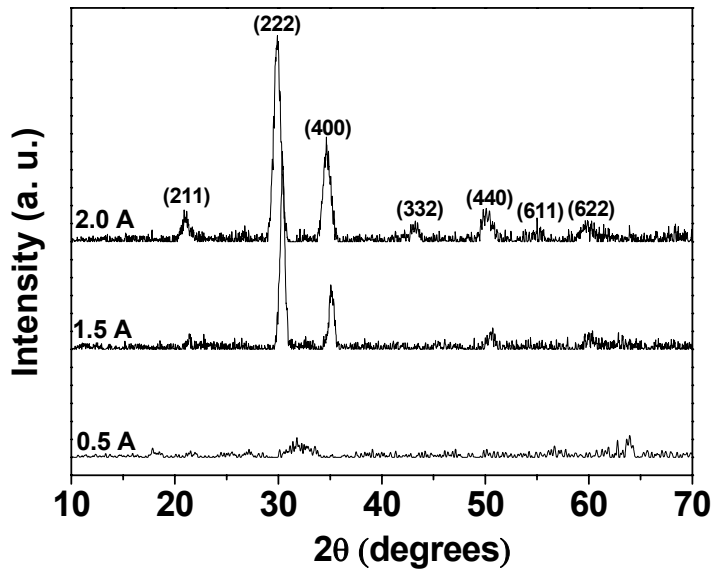


Figure 3.19: XRD patterns of the indium oxide films deposited at different discharge currents: 0.5 A, 1.5 A, and 2.0 A

The reactive IBAE is proven a versatile technique that allows for modifying the crystal structure of the indium oxide films from amorphous to polycrystalline simply by adjusting the discharge current of the oxygen ion source.

### 3.2.5 Intrinsic Stress

The obvious shift of the XRD peaks in Figure 3.19 is most likely caused by the intrinsic stress, generated from the growth process. To identify this, the intrinsic stress under different deposition conditions is measured. The stress measurements are performed by using a mechanical stress gauge from Ionic Systems. It is also crucial to study the film stress issue, especially for applications on flexible substrates. Excessive stress can cause the delamination of the film from the substrate. The film stress can be from thermal stress and intrinsic stress. The thermal stress arises from the difference

in the growth temperature and the thermal expansion coefficients between substrate and the grown film. The intrinsic stress is generated during the growth process varied with deposition technique and deposition conditions. Since all the films were grown at low temperature on water-cooled glass substrates ( $\sim 40^{\circ}\text{C}$  due to plasma heating during deposition), the thermal stress can be negligible, and therefore, the key stress would be intrinsic stress.

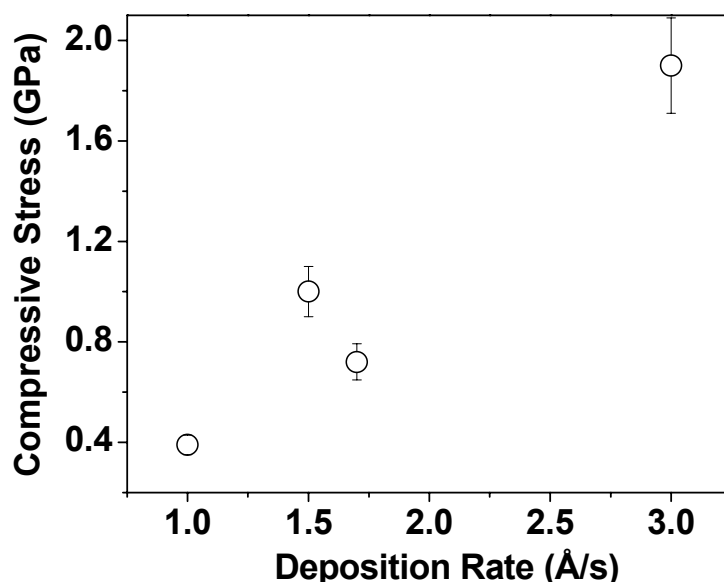


Figure 3.20: Intrinsic stress of the indium oxide films as a function of the deposition rate

Figure 3.20 displays the intrinsic stress of the indium oxide films as a function of the deposition rate. The discharge current and voltage are 1.0 A and 100 V. Figure 3.21 presents the dependence of the intrinsic stress on the discharge current, whereas the discharge voltage and deposition rate are kept constants at 100 V and 1.0 Å/s. Due to the atom peening effects [38], compressive stress generally occurs, when the



growing film is bombarded by ions with an energy of tens to hundreds of eV. In these figures, all the films have compressive stress ranging from 0.4 GPa to 1.8 GPa, slightly higher than that in the low-stress sputtered ITO films. The intrinsic stress increases with deposition rate and discharge current. This implies that the stress is proportional to the arrival mass, suggesting that a low deposition rate and low discharge current facilitates the realization of the low-stress films by the IBAE.

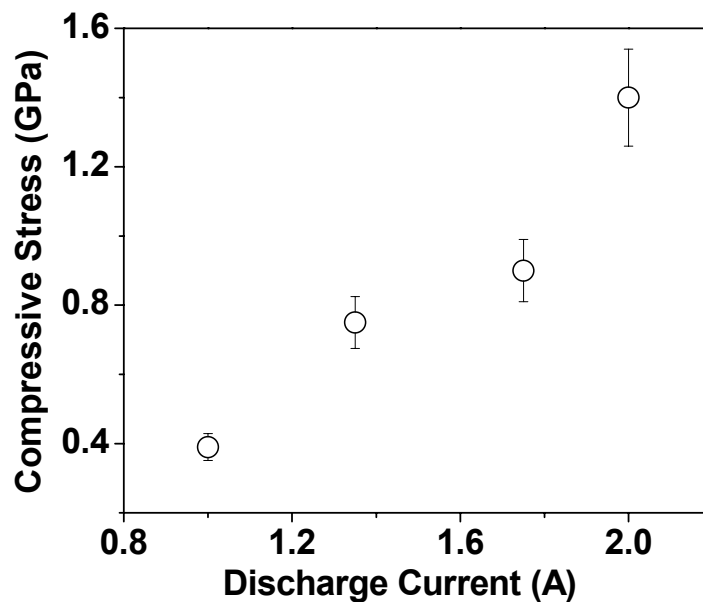


Figure 3.21: Intrinsic stress of the indium oxide films as a function of the discharge current

### 3.2.6 Topology

To examine the topology of the deposited films, the surface roughness is evaluated by a Veeco WYKO NT1100 optical profiler. The three surface roughness evaluation parameters are the average roughness, which is defined as the arithmetic mean or

average of the absolute distances of the surface points from the mean plane; the root mean square roughness, which is the root mean square of the surface departures from the mean plane within the sampling area; and the peak to valley roughness, which is defined as the sum of the largest peak height value and the largest valley depth from the mean plane within the sampling area.

Figure 3.22 and Figure 3.23 show the image of the topology and representative surface profiles scanned in both the x- and y-directions. The 200-nm-thick film on a single crystalline silicon wafer is deposited at a discharge current of 2.0 A, discharge voltage of 100 V, and deposition rate of 1.5 Å/s. The calculated peak to valley roughness is around 4.0 nm for an area of 200 μm×200 μm. The calculated root mean square roughness and average roughness are ~ 1.0 nm and ~ 0.8 nm, respectively, comparable to those of the best ITO films by sputtering.

Figure 3.24 and Figure 3.25 are the image of the topology and the scanned surface profiles in both x- and y-directions for the 200 nm highly-conducting films, deposited at a rate of 3.0 Å/s. The discharge current is 1.0 A, and the discharge voltage is 100 V. The calculated peak to valley roughness is approximately 10.3 nm for the area of 200 μm×200 μm. The calculated root mean square roughness and average roughness are ~ 1.4 nm and ~ 1.2 nm, respectively.

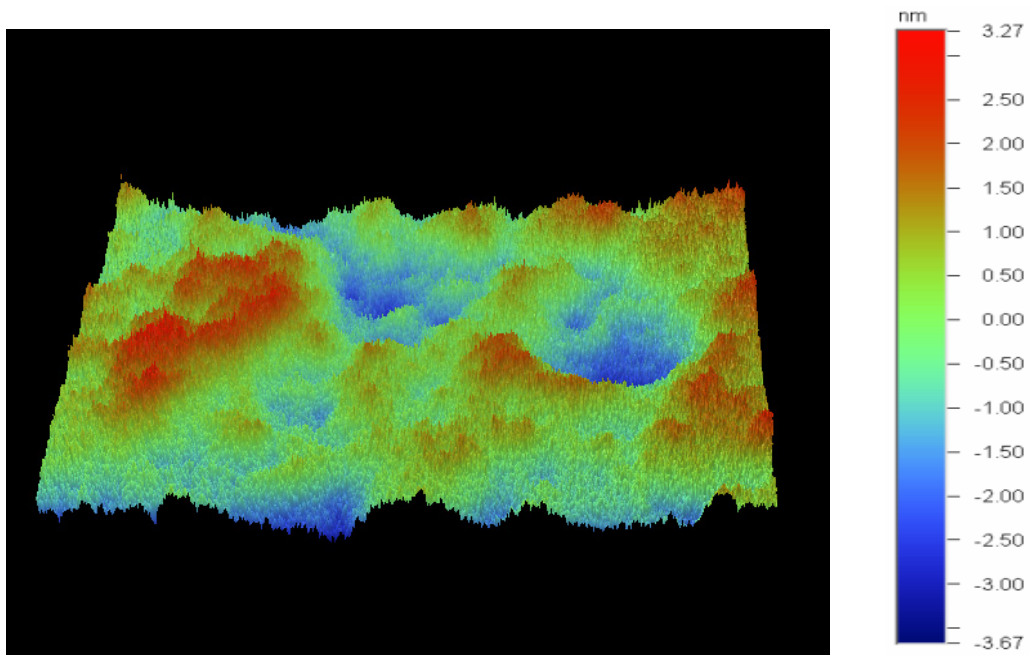


Figure 3.22: Topological image of the semiconducting indium oxide

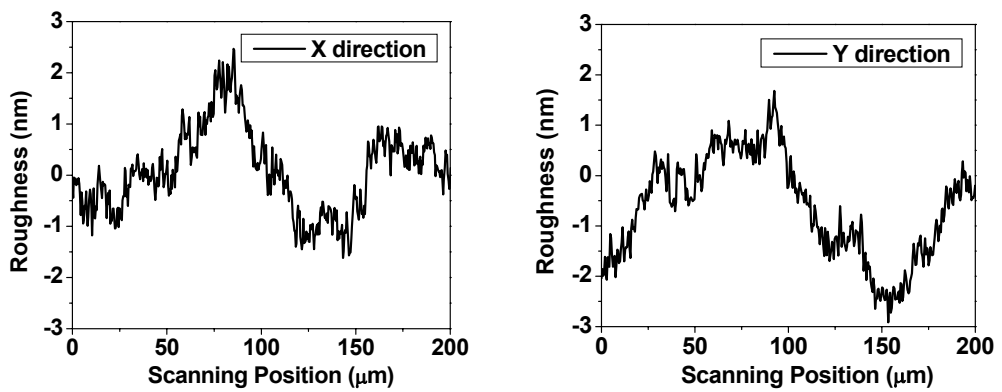


Figure 3.23: Representative surface profiles scanned in both the x- and y- directions for the semiconducting indium oxide

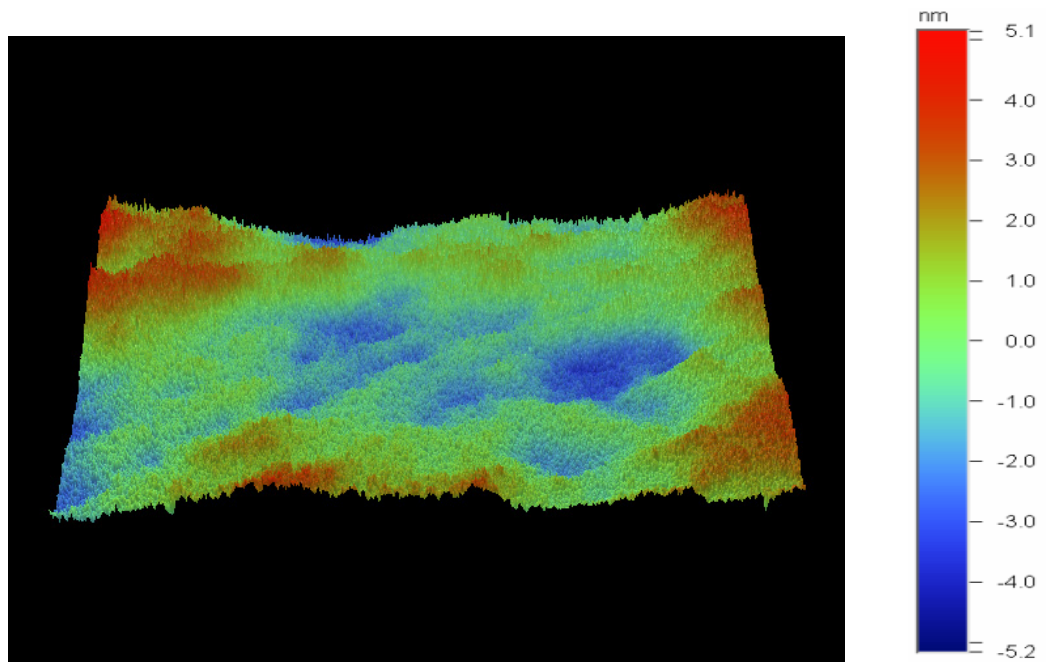


Figure 3.24: Topological image of the highly-conducting indium oxide

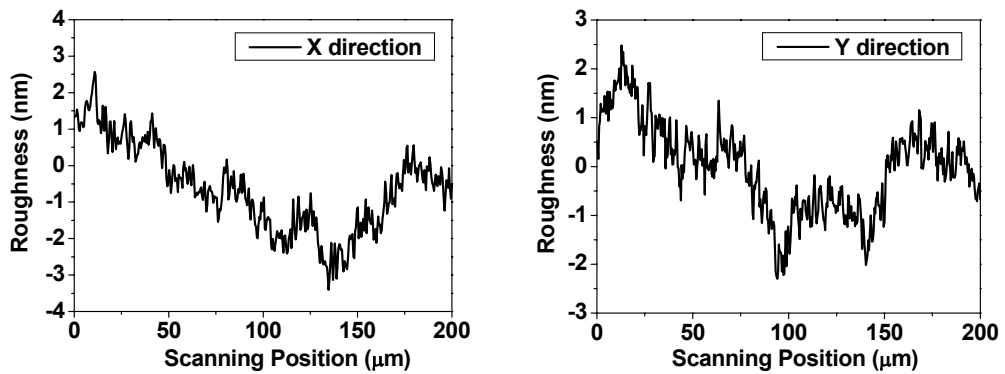


Figure 3.25: Representative surface profiles scanned in both the x- and y- directions for the highly-conducting indium oxide

The IBAE-derived films are smoother and more uniform than those deposited by conventional evaporation, since the incident ions physically promote the migration of the atoms, which is one of the main physical effects of the IBAE technique [38].

### 3.2.7 Morphology

The scanning electron microscopy (SEM) images are attained by a LEO 1530 FE-SEM with an operating voltage of 15 KV and an amplification factor of 50 K. Figure 3.26 reflects the fractured cross-sectional SEM images of the semiconducting indium oxide film, deposited on a bare single crystalline silicon wafer. The film thickness is about 200 nm. The left image is captured from a secondary electron detector and the right image is from a back scattering electron detector. The column structures are identified in the cross-sectional morphology images, typical for most thin films, deposited by physical vapour deposition at low substrate temperatures [42].

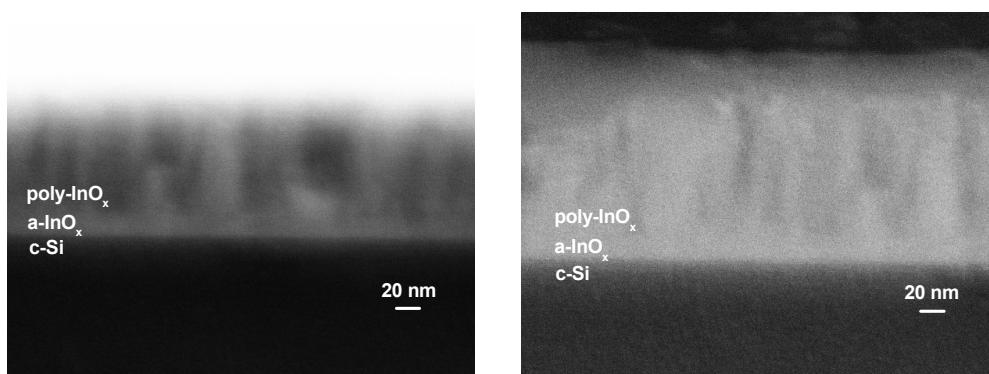


Figure 3.26: Cross-sectional SEM images of the semiconducting indium oxide film on a single crystalline Si wafer

Interestingly, the SEM images further reveals that the film growth by the IBAE can be divided into two consecutive processes: at the initial stage of the growth, a very thin indium oxide (around 20 nm in this case) with an amorphous phase is grown at the interfacial region as marked in Figure 3.26, followed by a polycrystalline growth of the column structure to the top. Thus, from growth process point of view, ion assisted deposition is quite different from conventional evaporation or sputtering,

which is typically an island-mode growth. It is believed that the ion assistance enhances the adatom diffusion length, along the substrate surface, and tends to break up the three-dimensional islands so that the column structure growth less likely occurs at the bottom. After a certain thickness, the growth becomes normal due to cluster aggregation and the change in the surface conditions.

### **3.3 Summary**

In this chapter, a comprehensive material study of the zinc oxide and indium oxide thin films, prepared by the oxygen ion assisted reactive IBAE at low temperatures. The focus is on the investigation of the correlations between deposition conditions and film properties. The electrical properties, chemical composition, optical properties, crystal structure, intrinsic stress, topology, and morphology as a function of the deposition conditions are studied. The process windows for achieving the semiconducting zinc and indium oxides are eventually figured out. In addition, the work in this chapter demonstrates that as a versatile technique, IBAE can effectively control the TOS thin film properties to meet the technical requirements of a variety of applications, including TCOs, TFTs, and optical coatings.

# Chapter 4

## ZnO-based UV Sensors

This chapter includes a review of the ZnO-based thin-film UV sensor technology, a description of the device fabrication and processing, and the details on the device characterization and analysis, including the current-voltage characteristics, current transients, leakage mechanisms, and spectral response.

### 4.1 Introduction

Undoped zinc oxide is transparent at visible wavelengths, has a direct and wide bandgap of  $\sim 3.3$  eV at room temperature, and a large exciton binding energy ( $\sim 60$  meV at room temperature) [29]. Doped zinc oxides such as ZnO:Al and ZnO:In are well-known for many optoelectronic device applications, including TCOs in flat-panel displays and solar cells. Recently, ZnO-based UV sensors and light-emitting diodes have been reported [43, 44]. Among these applications, ZnO-based UV sensor technology offers definite advantages due to its direct and wide bandgap, strong UV-response, simple and low-cost processing, and capability of working in harsh environments [45-47].

The Schottky and p-n junction have been widely-adopted for structuring ZnO-based UV sensors. Since the growth of reproducible and reliable p-type ZnO films are still under development, Schottky diodes and a number of p-n heterojunctions have been developed by combining n-type ZnO with metal Ag [46] and other p-type material such as Si [47], SiC [48], SrCu<sub>2</sub>O<sub>2</sub> [49], NiO [43], ZnMgO [50], and ZnRh<sub>2</sub>O<sub>4</sub> [51]. A

high leakage current, due to the imperfection of the heterojunction interface, is a serious technical issue for these devices as UV sensors. The lowest level of leakage current to date is  $2 \times 10^{-4}$  A/cm<sup>2</sup> at -10 V for n-ZnO/p-SiC heterojunction diodes, grown by plasma-assisted molecular-beam epitaxy [48]. As for the other materials, the p-n heterojunction performance is far inferior because of the lattice mismatch of the used materials and electronic defects.

To take advantage of the development of the semiconducting ZnO, the approach in this thesis is to fabricate a p-i-n heterostructure instead of a p-n heterojunction by using semiconducting ZnO as the intrinsic layer, and p-NiO and n-ITO as the contacts. The property and thickness of the intrinsic layer is critical for the device performance. Generally, it is perceived that in order to absorb the light at a certain wavelength, the thickness of the absorption layer should be thicker than  $\alpha_{bandedge}^{-1}$ , where  $\alpha_{bandedge}$  is the absorption coefficient at the particular wavelength, referring to the optical bandgap [2]. By applying this simple rule and taking the wavelength corresponding to the ZnO optical bandgap of 3.2 eV as a reference, the minimal thickness for the ZnO absorption layer is approximately 140 nm, which means the ZnO absorption layer must be thicker than this value in order to efficiently absorb the photons.

In ZnO-based diodes, NiO with a bandgap of ~3.7 eV is used as a p-type contact. Non-stoichiometric NiO is p-type conductive due to the presence of Ni<sup>3+</sup> ions, resulting from the appearance of nickel vacancies and/or interstitial oxygen in the NiO crystallites [52]. The details of the NiO films, fabricated by the IBAE can be found in the literature [53].



## 4.2 Device Fabrication and Processing

Both p-i-n and n-i-p structures are achieved by simply changing the deposition sequence. Figure 4.1 is a schematic diagram of the p-i-n and n-i-p heterostructures. Semiconducting i-ZnO and p-NiO are fabricated by the reactive IBAE and n-ITO is deposited by a conventional radio frequency sputtering technique. For the p-i-n configuration, first, a 20 nm NiO layer is deposited by using the IBAE, followed by a 200 nm ZnO deposited by the IBAE. Finally, a 50 nm ITO is sputtered through a shadow mask with a contact area of  $0.025 \text{ cm}^2$  to form the top transparent electrodes. Similarly, the n-i-p diodes are constructed by the following deposition steps. A 200 nm i-ZnO film is prepared on a commercial ITO-coated glass substrate. Then, a 20 nm p-NiO layer is deposited through the same shadow mask to form the top contact. All the deposition steps are performed at low temperatures without heating the substrate and post-deposition annealing.

The deposition rate is maintained at  $0.3 \text{ \AA/s}$  for the NiO films and  $1.5 \text{ \AA/s}$  for the ZnO films. The optimized discharge voltage and current are 120 V and 2.25 A and 100 V and 1.45 A for the ZnO and NiO, respectively. The resistivity of the 20 nm p-NiO is around  $1 \text{ }\Omega\text{-cm}$  on the glass substrate. The amorphous ITO films are sputtered in an Ar plasma at a working pressure of 5 mTorr and a deposition rate of  $1.1 \text{ \AA/s}$ . The sheet resistance of the ITO layer is  $\sim 70 \text{ }\Omega/\text{sq}$ .

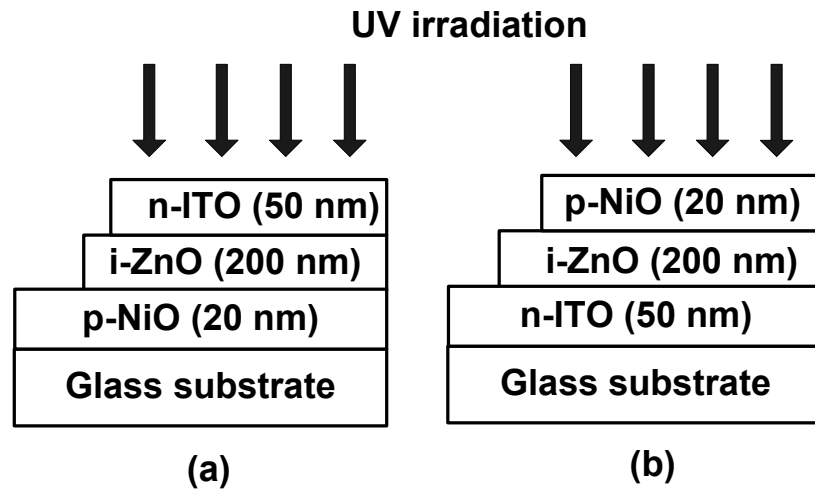


Figure 4.1: Schematic diagram of the (a) p-i-n and (b) n-i-p heterostructures

## 4.3 Device Characterization and Analysis

### 4.3.1 Current-Voltage Characteristics

The current-voltage (J-V) characteristics of both diodes are measured in a 4200 Semiconductor Characterization System from Keithley instruments. Figure 4.2 shows the typical J-V characteristics of the as-deposited p-i-n and n-i-p diodes. The measurements are performed by changing the bias voltages from -5 V to +2 V and vice versa. The voltage increment and delay time are set to 25 mV and 2 s, respectively. Both diodes exhibit clear diode-like behaviour with a current rectification ratio as high as  $10^4 \sim 10^5$  at the bias voltages of +/- 2 V. The reverse dark leakage current is  $\sim 10$  nA/cm<sup>2</sup> for the p-i-n structure and  $\sim 100$  nA/cm<sup>2</sup> for the n-i-p structure at -5 V, which is orders of magnitude lower than that reported for the ZnO-based diodes prepared by other techniques [43, 48, 51, 53]. This is the lowest leakage current recorded for ZnO-based diodes to date. The observed hysteresis in Figure 4.2

is similar to that in a-Si:H p-i-n diodes and is attributed to a time-dependent current component, induced by the depletion of the charge from the intrinsic layer [54].

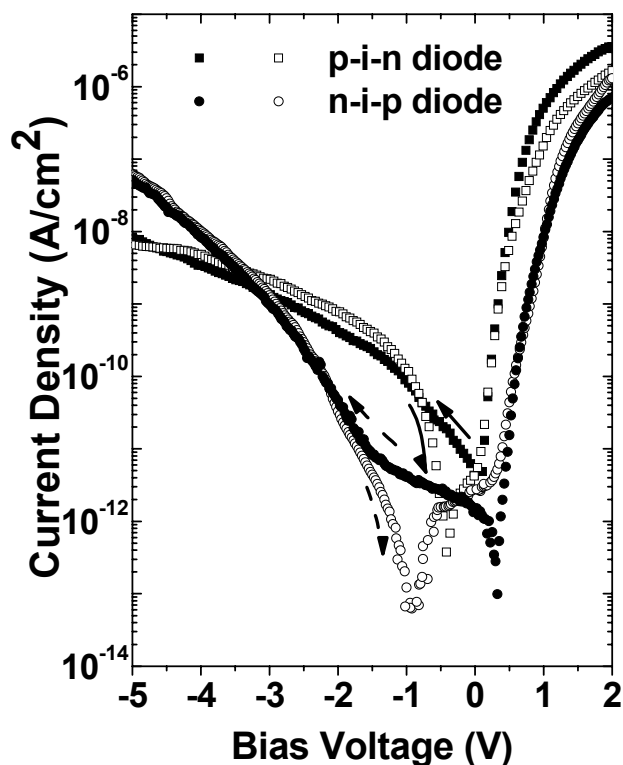


Figure 4.2: Typical J-V characteristics of the ZnO-based p-i-n and n-i-p diodes

### 4.3.2 Leakage Current Mechanisms

Since a UV sensor works under reverse bias conditions, it is crucial to decrease leakage current as much as possible, particularly for low-level UV detection. The lowest leakage current ( $\sim 10$  nA/cm<sup>2</sup> at -5 V) is achieved in the diode with a p-i-n configuration, whereas the sample with a n-i-p structure has a one order of magnitude higher leakage current at the same reverse bias. However, at reverse biases, lower

than 3 V, the n-i-p diode has a lower leakage current than the p-i-n diode in Figure 4.2.

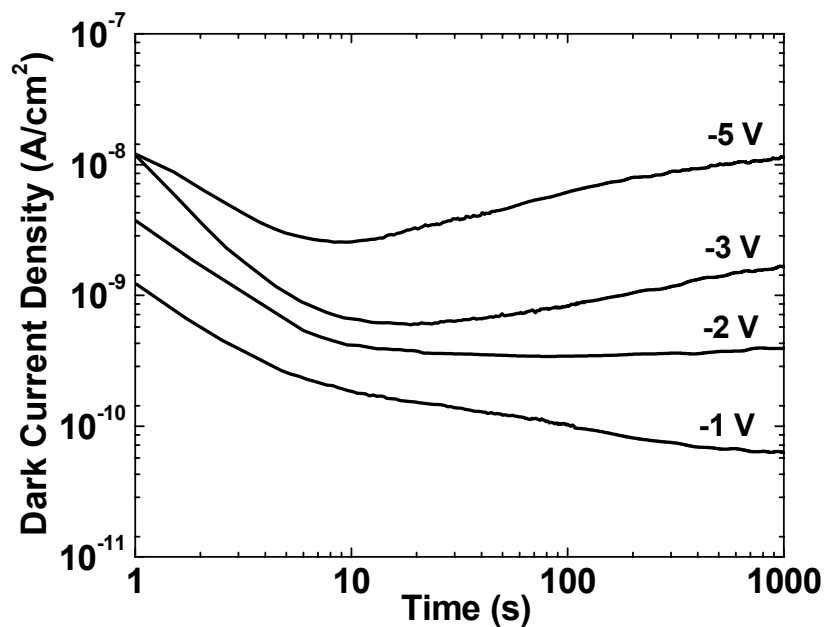


Figure 4.3: Time dependence of the dark current at different bias voltages for the p-i-n diode

There are bulk and contact components to the leakage current. The large value of the leakage current may be due to the increased charge generation through the defect states in the i-layer bulk and at the interfaces. To identify the dominant source of the leakage current, the time dependence of the dark current measurements are carried out at different reverse biases.

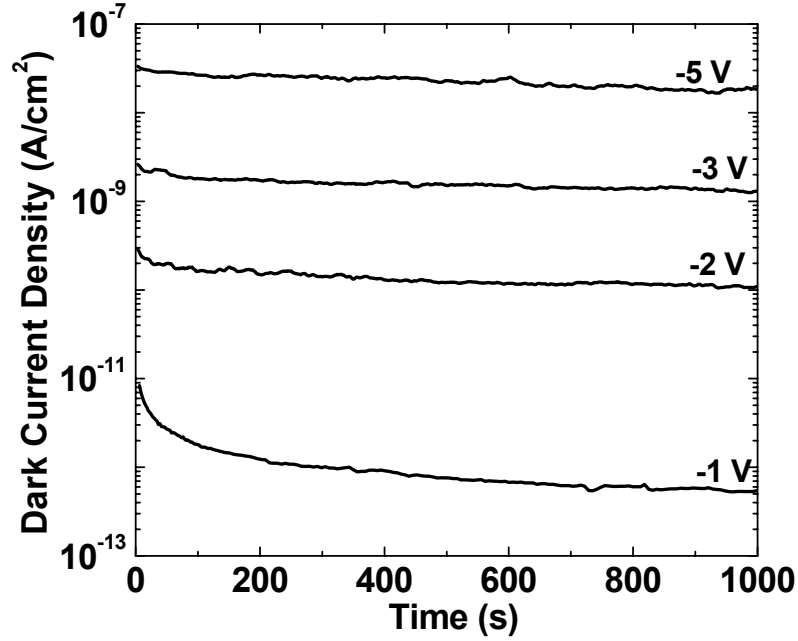


Figure 4.4: Time dependence of the dark current at different bias voltages for the n-i-p diode

Figure 4.3 and Figure 4.4 present dark current transient curves of the p-i-n and n-i-p diodes. At a low reverse bias of 1 V, a slow decrease in the dark current is observed in both diodes over a period of 1000 s. Such a current decay is attributed to the depletion of the charge from the deep defect states in the i-ZnO layer. The time taken for the depletion ( $\tau_D$ ) is

$$\tau_D = \nu_0^{-1} \exp[(E_c - E_{qF})/kT], \quad (4-1)$$

where  $\nu_0$  is the excitation rate prefactor,  $k$  is the Boltzmann constant,  $T$  is the absolute temperature in Kelvin,  $E_c$  and  $E_{qF}$  are the conduction band energy and the quasi Fermi energy [55]. For wide bandgap semiconductors such as ZnO, the depletion time can be very lengthy when the quasi Fermi-energy level approaches the

mid-bandgap. Since at low reverse biases, the leakage current originates primarily from the thermal generation of the carriers from the defect states and is proportional to the defect density, the expectation is that the ZnO-based n-i-p diode has a smaller thermal generation current than that of the p-i-n diode.

At reverse biases within the range of 1.5 V and 5 V, the leakage current of both diodes increases with the applied reverse bias and exhibits strong field-dependence, evident in the J-V characteristics and dark current transients.

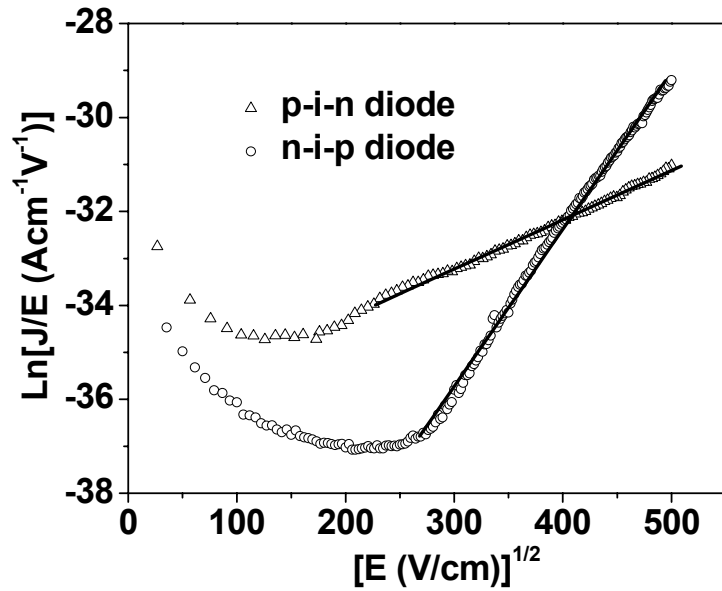


Figure 4.5:  $\ln(J/E)$  as a function of  $E^{1/2}$ , obeying the Poole-Frenkel model, accounts for the leakage current mechanism at a reverse bias higher than 1.5 V

Figure 4.5 reveals that both the J-V characteristics at this reverse bias range follow:

$$J \propto E \exp(\beta \sqrt{E}), \quad (4-2)$$

where  $\beta = \frac{\beta_{P-F}}{\xi kT}$  is a constant and  $E$  is the electric field strength under a reverse bias, assuming  $E = \frac{V_R}{d}$ , where  $V_R$  is the applied reverse bias and  $d$  is the thickness of the i-ZnO film. This increasing leakage current is likely caused by a field-enhanced carrier generation mechanism, matching well with the Poole-Frenkel model [56]. The Poole-Frenkel constant,  $\beta_{P-F}$ , is given by

$$\beta_{P-F} = \sqrt{\frac{e^3}{\pi \epsilon_0 \epsilon_r}}, \quad (4-3)$$

where  $e$  is the elementary charge,  $\epsilon_0$  is the permittivity of the free space and  $\epsilon_r$  is the optical dielectric constant of the ZnO film, which should satisfy  $\epsilon_r = n^2$  ( $\sim 4$ ), and  $n$  is the refractive index of the ZnO film.

The coefficient ( $\xi$ ) is introduced to reflect the modification of the normal Poole-Frenkel effect, where  $\xi$  is unity. A large value of  $\xi$  ( $1 < \xi < 2$ ) is agreeable if the material contains a non-negligible number of traps [57, 58]. Since the deposited ZnO is not fully compensated, the Fermi-energy level lies above the mid-bandgap and the depletion of the i-ZnO layer causes a larger increase in the electric field strength at the p-i interface, compared to that of the n-i interface (i.e. the charge injection is more probable from the p-layer than from the n-layer). Furthermore, the p-i interface on the top of the i-ZnO (the n-i-p configuration) favours even a larger electric field enhancement than the p-i interface on the bottom (p-i-n configuration) due to surface condition that is rougher on the top. However, the early assumption on the electric field strength in Eq. (4-2) does not consider this situation. Therefore, the larger field

enhancement at the p-i interface can lead to a smaller value of  $\xi$ , which explains well that the leakage current of the n-i-p diode has a stronger field-dependence than that of the p-i-n diode.

In addition to the generation currents: thermal and Poole-Frenkel, contact leakage is another mechanism. The principal observable effect of the contact leakage is a dark current increase over time, after the reverse bias is applied [54]. As seen in Figure 4.3, the dark current transient of the p-i-n diode (at -2 V, -3 V and -5 V) exhibits two stages of time dependence: the current decay at the beginning corresponds to the charge depletion, and the current slowly increases afterwards, which can be due to the contact leakage. For an ideal Schottky barrier, the contact leakage is the saturation current,  $J_0$ , which is associated with the Schottky barrier height,  $\Phi_B$  and the absolute temperature, T [59]:

$$J_0 = A^* T^2 \exp(-e\Phi_B / kT), \quad (4-4)$$

where  $A^*$  is the effective Richardson constant. For a non-ideal Schottky barrier, tunneling across the barrier reduces the barrier height and the contact leakage current,  $J_{contact}$  is expressed by [59]:

$$J_{contact} = A^* T^2 \exp[-e(\Phi_B - E_t R_t) / kT], \quad (4-5)$$

where  $R_t$  is an effective tunnelling length and  $E_t$  is the field at the contact. Therefore, the slow leakage current increase in the p-i-n diode at high reverse biases is attributed to the depletion of the i-ZnO layer. The depletion slowly increases the electrical field at the p-i interface, and consequently, augments the contact leakage. However, such a



current tendency does not appear in the n-i-p diode in Figure 4.4. The possible reason is that the n-i-p diode has a higher  $\Phi_B$  than that of the p-i-n diode.

### 4.3.3 Forward-Bias Analysis

The forward-bias J-V characteristics can be fitted by a typical diode model [60]:

$$J_F(V_F) = J_0 \exp\left(\frac{eV_F}{nkT}\right), \quad (4-6)$$

where  $J_F(V_F)$  is the forward-bias current at a forward-bias of  $V_F$  and  $n$  is the ideality factor.

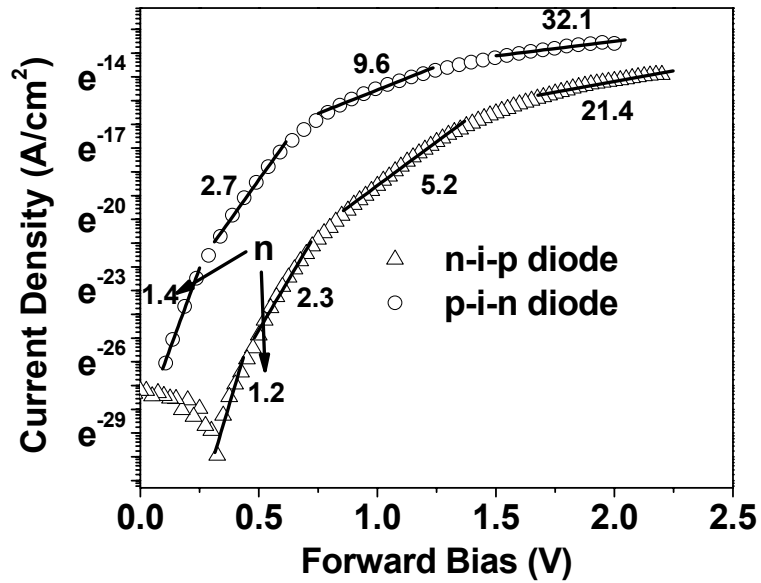


Figure 4.6: Forward-bias  $\ln(J)$ -V characteristics of the p-i-n and n-i-p diodes

With Eq. (4-4), the Schottky barrier height,  $\Phi_B$ , can be determined. Calculated from the forward-bias J-V characteristics presented in Figure 4.6, the Schottky barrier

energy  $e\Phi_B$  of the n-i-p diode is approximately 0.34 eV higher than that of the p-i-n diode, which can explain why the contact leakage of the n-i-p diode is greatly suppressed. The ideality factor ( $n$ ) is greater than unity in both diodes, suggesting that the carrier recombination and generation in the depletion layer and the interfacial states exist in both diodes. Fewer interfacial states of the n-i-p diode yield smaller ideality factors, consistent with the results in the thermal generation current.

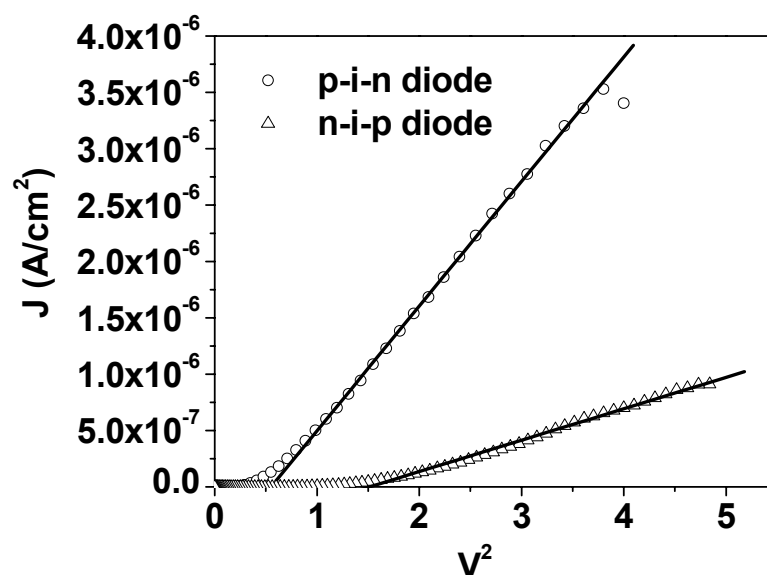


Figure 4.7: At higher biases, the current depends on  $V^2$ , fitting well with the space-charge-limited current model

At forward biases higher than the turn-on voltage, a large value for  $n$  (2~30) violates the exponential J-V relationship, and  $J \propto V^2$  in Figure 4.7 indicates that the Space-Charge-Limited current accounts for the carrier transport [59]. Therefore, the forward-bias J-V characteristics undergo a transition from the recombination and generation current at low bias voltages to the space-charge-limited current at higher bias voltages.

### 4.3.4 Photocurrent Transient

The photocurrent transient measures the current's response to the pulse light illumination, describing how the current changes dynamically with and without the light illumination. The measurements of the transient photocurrent are performed by using a 1.8 mW GaN-based LED as a light source to provide a uniform photogeneration within the diode. The current measurements are conducted by the Keithley 4200 Semiconductor Characterization System.

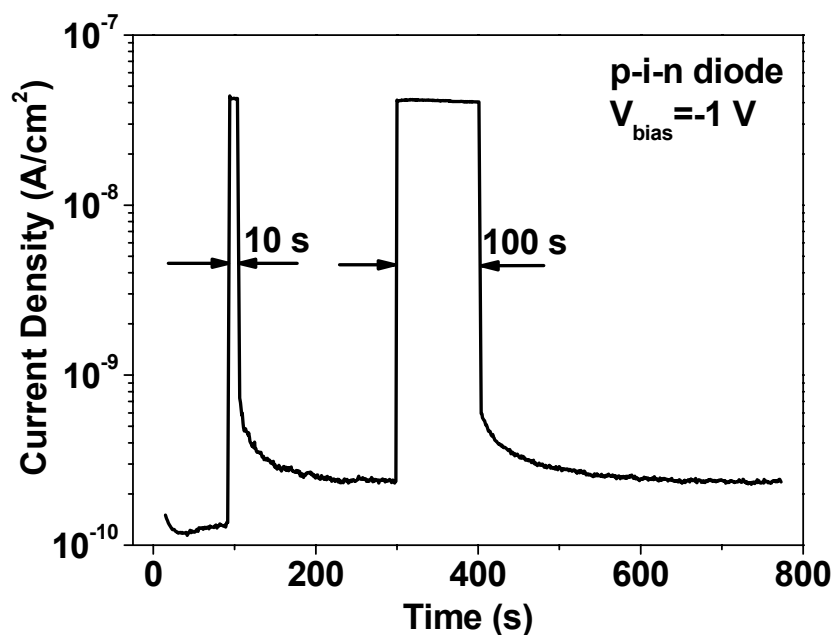


Figure 4.8: Photocurrent transient of the p-i-n diode under the reverse bias of 1 V

Figure 4.8 displays the transient photoresponse of the p-i-n diode at the reverse bias of 1 V. After the light pulse, the current first decreases rapidly from the steady-state level of  $4 \times 10^{-8}$  A/cm<sup>2</sup> to about  $7 \times 10^{-10}$  A/cm<sup>2</sup>, and then decays exponentially due to

the continuous charge release. The trapped charge density, estimated for a pulse width of 100 s yields a value of  $\sim 3 \times 10^{16}$  electrons/cm<sup>3</sup> [61].

### 4.3.5 Spectral Response and Linearity

To demonstrate the UV sensing performance, spectral response measurements are conducted by using the Oriel monochromator. Also the linearity results are also presented to examine the photosensitivity. Both quantum efficiency (QE) and spectral responsivity ( $R_\lambda$ ) are functions of the photon's wavelength. To convert from the  $R_\lambda$  to the QE:

$$QE(\lambda) = \frac{R_\lambda}{\lambda} \times \frac{hc}{e}, \quad (4-7)$$

where  $\lambda$  is the photon's wavelength in nm,  $h$  is the Planck constant,  $c$  is the speed of light in a vacuum, and  $e$  is the elementary charge.

Figure 4.9 illustrates the QE of the p-i-n and n-i-p diodes with a wavelength between 300 and 450 nm. The transmittance spectrum of the ZnO absorption layer is also plotted for reference. Both diodes are sensitive to UV irradiation with a wavelength range of 320 to 400 nm. It is also found that the p-i-n diode has a larger QE than the n-i-p diode for most of the wavelengths. The long wavelength component of the QE spectrum is associated with the optical interband transition in the i-ZnO. The QE reaches a maximum of 18% and 6% at the wavelength of 380 nm for the p-i-n and n-i-p diodes, respectively, and then decreases at shorter wavelengths due to the absorption in the top electrode.

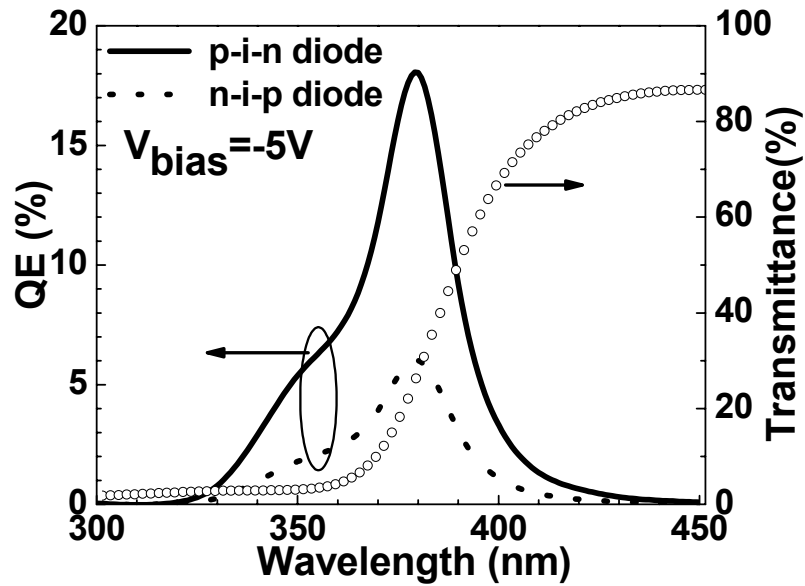


Figure 4.9: Comparison of the quantum efficiency between the p-i-n and the n-i-p diodes; transmittance spectrum of the ZnO intrinsic layer at wavelengths from 300 to 450 nm is also included

Figure 4.10 provides a comparison of the transmittance spectra between the 20 nm p-NiO and the 50 nm ITO films at wavelengths ranging from 300 to 450 nm. For most wavelengths, the ITO top contact in the p-i-n diode has an optical loss that is less than the NiO contact in the n-i-p diode, such that the p-i-n diode has larger values of the QE than the n-i-p diode.

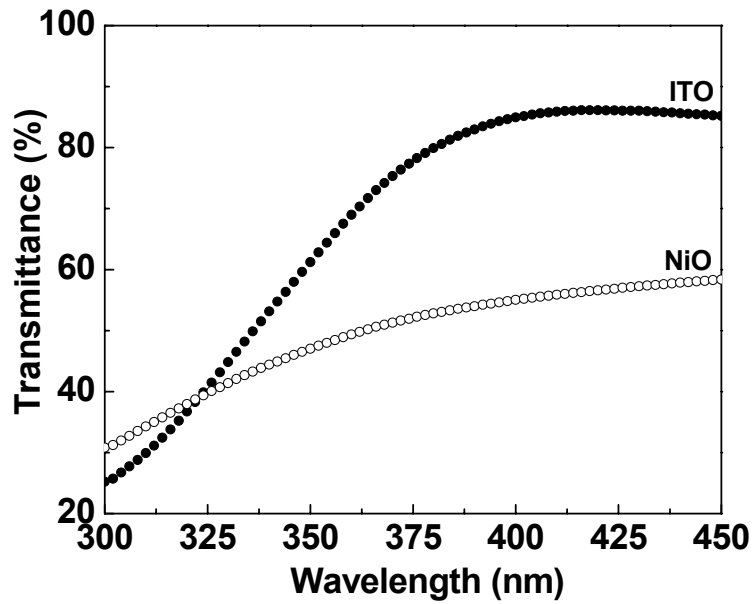


Figure 4.10: Transmittance spectra of the 50 nm ITO and 20 nm NiO in the wavelength range of 300 to 450 nm

Under the uniform illumination of the 1.8 mW GaN-based UV light-emitting diode, the photocurrent density increases linearly with the light intensity over five decades as portrayed in Figure 4.11, and as such, meets most of application requirements for the UV sensors. The p-i-n diode has a photocurrent density that is roughly three-times larger than the n-i-p diode under the same light density, consistent with the results in the QE.

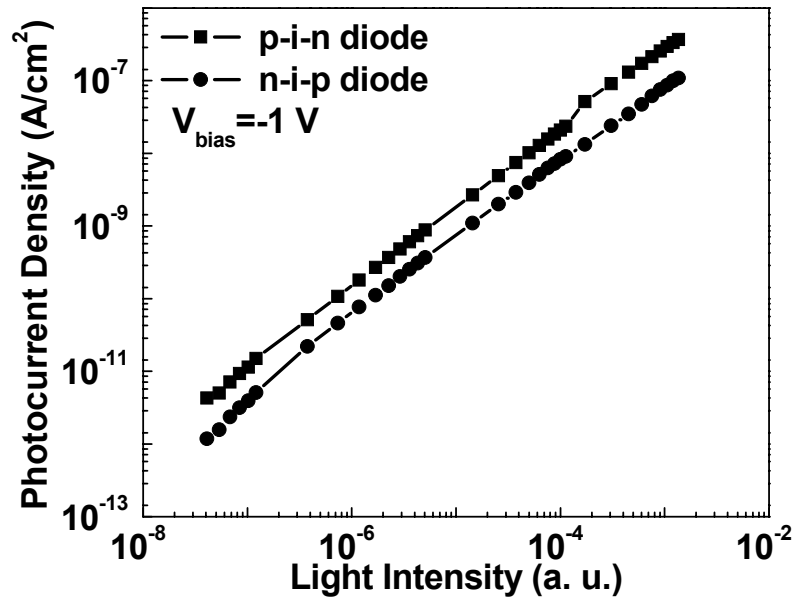
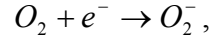


Figure 4.11: Photocurrent density as a function of the light intensity for both the p-i-n and n-i-p diodes

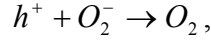
#### 4.3.6 Photoconduction Mechanisms

The sensitivity of the heterostructure photodiode stems from the photoconduction of the i-layer ZnO. An understanding of the photoconduction mechanisms is pivotal to guide material optimization and device design in the future.

The photoconduction in the nanocrystalline i-ZnO films may be due to the following. First, the photo-induced desorption of the oxygen, primarily accumulated at the grain boundaries [62]. In the absence of the UV light, excess oxygen is adsorbed by taking a free electron from the grain boundary of the ZnO crystallite to form a chemically adsorbed surface state, leaving behind a depletion region near the surface, expressed as:



under illumination, when the photon energy is higher than the fundamental absorption bandgap of ZnO (~3.2 eV), holes are produced by the light absorption near the grain boundary surface, discharging the negatively-charged oxygen ions, represented by:



and simultaneously producing electrons that increase the conductivity. Thus, nanocrystalline ZnO can have larger photocurrent because of the larger specific surface area or surface to volume ratio, which can adsorb more oxygen at the grain boundaries. Secondly, UV illumination lowers the barrier height of the grain boundary which enhances the mobility [63]. For polycrystalline semiconductor materials, the mobility  $\mu$  has the relationship of

$$\mu^{-1} = \mu_0^{-1} + [\mu_{gb} \exp(-E_b / kT)]^{-1} , \quad (4-8)$$

and is related to the mobility of a ZnO crystalline grain,  $\mu_0$ , and  $\mu_{gb} \exp(-E_b / kT)$  is the contribution, accounting for the grain boundary scattering. Here  $E_b$  is the barrier height of the grain boundary,  $k$  is the Boltzmann constant, and  $T$  is the absolute temperature in Kelvin [64]. The lowered barrier height  $E_b$  by UV illumination, enhances the carrier mobility from Eq. (4-8). Lastly, an increase of free carriers due to photovoltaic effects. The photogenerated carrier density  $n_{phg}$  and  $p_{phg}$  is the charge integration of generation rate in the entire depletion region,

$$n_{phg} = p_{phg} = \int_0^W G(x) dx , \quad (4-9)$$



where  $W$  is the width of the depletion layer, and  $G(x)$  is the carrier generation rate, given by

$$G(x) = \Phi_{ph} T_{TCO}(\lambda) \alpha(\lambda) e^{-\alpha(\lambda)x}, \quad (4-10)$$

where  $\Phi_{ph}$  is the photon flux reaching the device,  $T_{TCO}(\lambda)$  is the transmittance of the top-contact NiO or ITO, and  $\alpha(\lambda)$  is the absorption coefficient of the ZnO, a function of the penetration depth [28, 65].

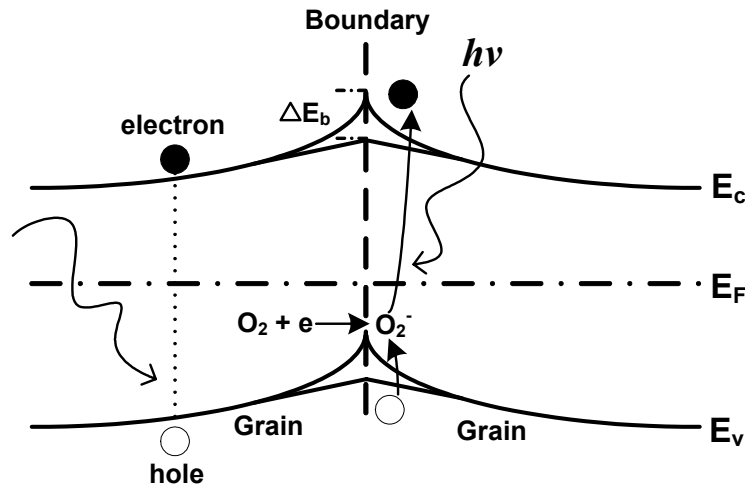


Figure 4.12: Photoconduction mechanisms of the nanocrystalline ZnO thin film

Figure 4.12 illustrates these three photoconduction mechanisms of the nanocrystalline ZnO thin film in a schematic band diagram. The ZnO thin films, derived by the IBAE can have a strong UV photosensitivity due to its nanocrystalline structure.

## 4.4 Summary

Both p-i-n and n-i-p heterostructure photodiodes are fabricated with the optimized semiconducting ZnO as the intrinsic absorption layer. The diodes exhibits a low

leakage current level and a high current rectification ratio, compared with those reported for the ZnO-based Schottky and p-n heterojunction diodes. A comparative study between two heterostructures is conducted with an in-depth analysis of current-voltage characteristics, leakage current mechanisms, current transients, spectral response, and linearity. Both diodes are sensitive to UVA (320-400 nm) irradiation and might be promising for low levels of UVA detection. A discussion on photoconduction mechanisms is also presented.

# Chapter 5

## Indium Oxide TFTs

This chapter reports on fabrication, characterization, and analysis of indium oxide TFTs. The focus is on the optimization of the device performance along with the detailed study of device characteristics, stability and dynamic behaviour.

### 5.1 Introduction

After the successful fabrication of semiconducting indium oxides by the IBAE, the possibility of applying semiconducting indium oxides to TFTs is considered. Even though indium oxide TFTs have been demonstrated with different gate dielectrics, as discussed in Chapter 1, the interest here is indium oxide TFTs with  $\text{SiN}_x$  or  $\text{SiO}_x$  gate dielectrics, deposited by conventional PECVD, which seems more attractive for large area fabrication and low-cost industrial practice.

### 5.2 TFTs with a Silicon Dioxide Gate Dielectric

#### 5.2.1 First-Run Indium Oxide TFTs

The first-run indium oxide TFTs are constructed with a  $\text{SiO}_x$  gate dielectric by PECVD. The bottom-gate staggered TFT test structure is shown in Figure 5.1. The device fabrication steps are described as follows. First, a 200 nm  $\text{SiO}_x$  layer is deposited on heavily doped p-type single crystalline silicon wafers. Then, a 100 nm indium oxide layers are grown by the IBAE and patterned by traditional

photolithography and wet etching. The semiconducting  $\text{In}_2\text{O}_3$  channel layer is deposited at a discharge current of 2.0 A and deposition rate of  $1.7 \text{ \AA/s}$ . Before the deposition of the indium oxide channel, the  $\text{SiO}_x$  surface is treated by a beam of low-energy  $\text{O}_2$  plasma to remove contaminants and moisture. Finally, a 70 nm amorphous ITO with a sheet resistance of  $70 \text{ \Omega/sq}$ . is sputtered in an Ar plasma at a working pressure of 5 mTorr and a deposition rate of  $1.1 \text{ \AA/s}$ . The ITO layer is patterned by the lift-off technique to form source and drain contacts. Al is sputtered on the back side of silicon wafer to form a common gate electrode.

The TFT performance, transfer characteristics and output characteristics are characterized by the 4200 Semiconductor Characterization System from Keithley instruments. The sweeping time and holding time are selected as 1 s and 2 s, respectively. The sweep voltage increment is set to 0.5 V.

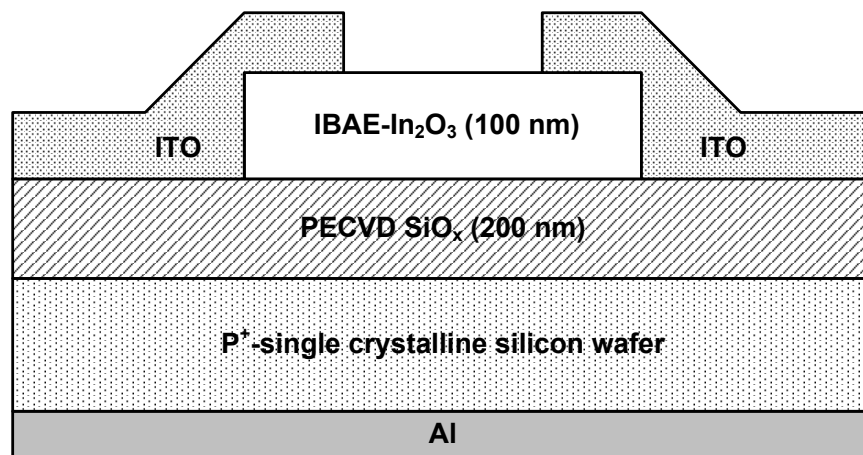


Figure 5.1: Cross-sectional schematic diagram of the indium oxide TFT test structure

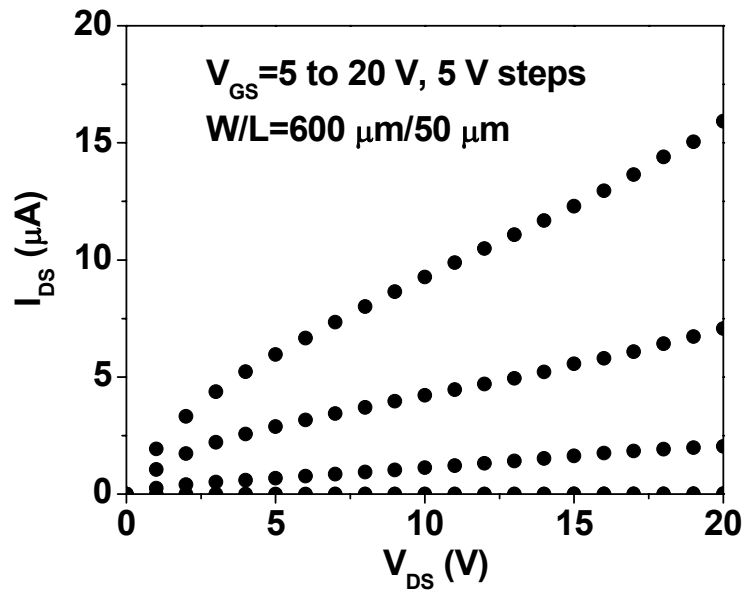


Figure 5.2: Output characteristics of the first-run indium oxide TFT with the PECVD  $\text{SiO}_x$  gate dielectric

Figure 5.2 depicts the output characteristics of the first-run indium oxide TFT with the PECVD  $\text{SiO}_x$  gate dielectric.  $W$  and  $L$  refer to the channel width and length, respectively ( $W/L = 600 \mu\text{m} / 50 \mu\text{m}$ ). The output characteristics shown here are very poor and there is no clear pinch off or “hard” saturation observed in the studied voltage range.

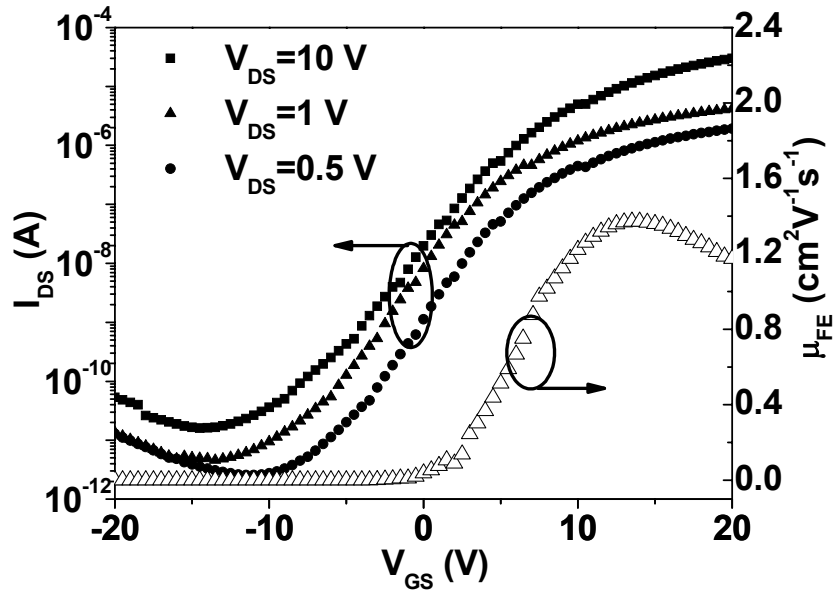


Figure 5.3: Transfer characteristics and field-effect mobility dependence on the gate voltage of the first-run indium oxide TFT with the PECVD SiO<sub>x</sub> gate dielectric

Figure 5.3 presents the transfer characteristics of the same indium oxide TFT. An current ON/OFF ratio of  $2 \times 10^6$  is achieved at  $V_{DS} = 10$  V and  $V_{GS}$ , ranging from -15 V to 20 V. The gate leakage current is below 1 pA under bias conditions. The threshold voltage  $V_T$  of this TFT is around 5.7 V, extracted from the linear extrapolation plot of the transfer characteristics at  $V_{DS} = 1$  V. Also, the field-effect mobility  $\mu_{FE}$  as a function of  $V_{GS}$  is included in Figure 5.3. The details of the field-effect mobility and threshold voltage extraction can be found in Appendix of this thesis. The field-effect mobility strongly depends on the gate bias. It increases with the gate bias due to the fact that the traps at the interface and/or in the “bulk” of the channel layer are continuously filled by increasing the  $V_{GS}$ . In an ideal case, the mobility should saturate at a certain  $V_{GS}$ . However, as observed here, the mobility drops with a continuous increase in the  $V_{GS}$  that might be caused by series resistance,

channel mobility degradation, and/or interface scattering [66]. The peak value of the field-effect mobility is  $1.4 \text{ cm}^2/\text{Vs}$  at  $V_{GS} = 15 \text{ V}$ , much lower than start-of-the-art TOS TFTs reported elsewhere. Another important device parameter, the sub-threshold slope defined by  $S = (d \log_{10} I_{DS} / dV_{GS})^{-1}$ , can be calculated from the logarithmic scale transfer characteristics, and yields a value of  $2.9 \text{ V/decade}$ .  $S$  is quantified by:

$$S = \frac{qk_B T (N_t t_c + D_{it})}{C_{ox} \log(e)} \quad (5-1)$$

where  $C_{ox}$  is the equivalent capacitance per unit area of the  $\text{SiO}_x$  ( $\sim 19 \text{ nF/cm}^2$ ), retrieved from measurement of capacitance-voltage characteristics of the TFT,  $q$  is the electron charge,  $k_B$  represents Boltzmann's constant,  $T$  is the absolute temperature in Kelvin, and  $t_c$  is the channel layer thickness [67]. The value of  $S$  depends on the trap density in the bulk channel layer ( $N_t$ ) and at the  $\text{In}_2\text{O}_3/\text{SiO}_x$  interface ( $D_{it}$ ). If  $N_t$  or  $D_{it}$  is set to zero, the maximum values of  $N_t$  and  $D_{it}$  are  $5.7 \times 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$  and  $5.7 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ , respectively. The large values of  $N_t$  and  $D_{it}$  suggests that either the semiconductor channel and/or interface needs to be further optimizing.

## 5.2.2 Problem Identification and Proposed Solutions

The first-run TFTs with the PECVD dielectrics  $\text{SiO}_x$  are demonstrated in the last section. The TFTs work as field-effect devices, but the device performance is poor, and far from meeting the technical needs of practical applications such as active matrix OLED displays.

The principal problems in such TFTs are two-fold. One is that the output characteristics have a “soft” saturation, showing the ineffective gate control. The other is that the large values of sub-threshold slope signifies the large amount of interfacial traps and/or defect states in the indium oxide bulk and the TFTs are prone to a low field-effect mobility with degradation.

To solve these problems and improve the device performance, three solutions are proposed: (1) Replace ITO with Mo to diminish the contact resistance between the source/drain (S/D) and channel. In indium oxide TFTs, Mo can be slightly doped into the indium oxide surface layer during the Mo sputtering so as to enhance the contact conduction; (2) Shrink the channel layer thickness in order to decrease the intrinsic channel resistance. The thicker channel is detrimental to the device performance, particularly field-effect mobility due to the grain boundary scattering from polycrystalline indium oxide layer. As noted in Section 3.2.7, the indium oxide channel layer consists of a very thin amorphous interfacial layer at the bottom and a thicker polycrystalline layer on the top, where carriers injected from the S/D contacts are most likely scattered by a large number of grain boundaries in this polycrystalline layer. Therefore, a thinner channel layer with an amorphous nature is preferred to avoid grain boundary scattering.

### **5.2.3 TFTs with the Improved Device Performance**

The goal of this section is to implement the strategies previously mentioned and examine if these strategies work effectively to improve the device performance.



A schematic cross section and a micrograph of the fabricated bottom-gate staggered TFT are denoted in Figure 5.4. The TFT is produced by a four-mask photolithographic process. First, an 80 nm Mo is sputtered and patterned on Corning 1737 glass substrate to form gate electrodes (Mask #1). Then after a 200 nm SiO<sub>x</sub> dielectric layer is deposited at 300<sup>0</sup>C by conventional PECVD, the deposition of 30 nm indium oxide by the IBAE is carried out. The indium oxide film is deposited at the discharge current of 2.0 A, discharge voltage of 100 V, and deposition rate of 1.7 Å/s. The channel layer is patterned by traditional photolithography and wet etching (Mask #2). Then, the SiO<sub>x</sub> layer is patterned to open via under the gate contact pads (Mask #3). Finally, a 100 nm Mo film is sputtered and patterned by the lift-off technique to form the source and drain contacts as well as the contact pads (Mask #4).

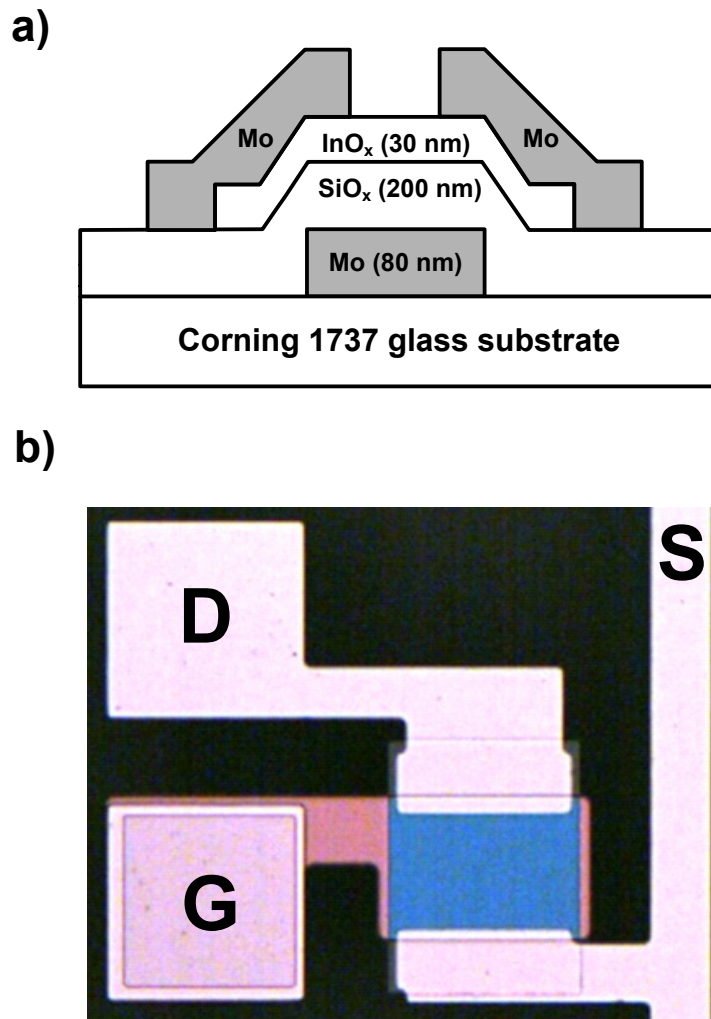


Figure 5.4: (a) Schematic cross section of the fabricated bottom-gate indium oxide TFT with the PECVD SiO<sub>x</sub> dielectric and (b) micrograph of the fabricated TFT

Figure 5.5 depicts the output characteristics of the indium oxide TFT with the PECVD SiO<sub>x</sub> dielectric. The obvious saturation and pinch off are observed. The drain current increases with the gate bias level, indicating that the electrons are accumulated under the gate biases. There is no current crowding at the low drain-source biases, suggesting that the Mo source/drain electrodes and indium oxide channel forms a reasonably good Ohmic contact.

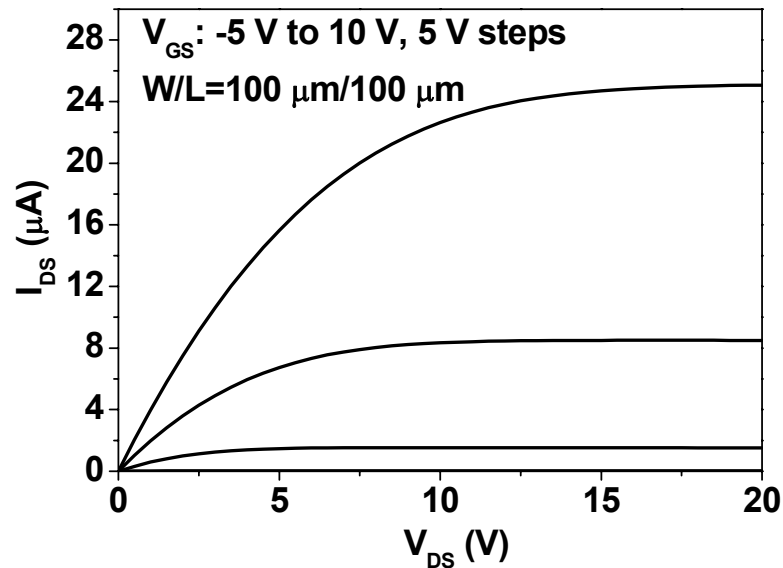


Figure 5.5: Output characteristics of the indium oxide TFT with the PECVD SiO<sub>x</sub> dielectric

Figure 5.6 conveys the transfer characteristics of the same indium oxide TFT at the drain-source voltages of 10 V, 1 V and 0.1 V, respectively. The high current ON/OFF ratio of  $10^7 \sim 10^8$  with a very low OFF current of  $\sim 10^{-13}$  A is obtained. The extracted threshold voltage of  $\sim 2.0$  V is achieved from the linear transfer characteristics at  $V_{DS} = 1$  V. From the dependence of the field-effect mobility on the gate-bias voltage curve, the value of the field-effect mobility can reach as high as  $33 \text{ cm}^2/\text{Vs}$  at  $V_{GS} = 20$  V, one of the highest mobility achieved in TOS-based TFTs. More important, the field-effect mobility does not indicate any degradation at the higher gate biases.

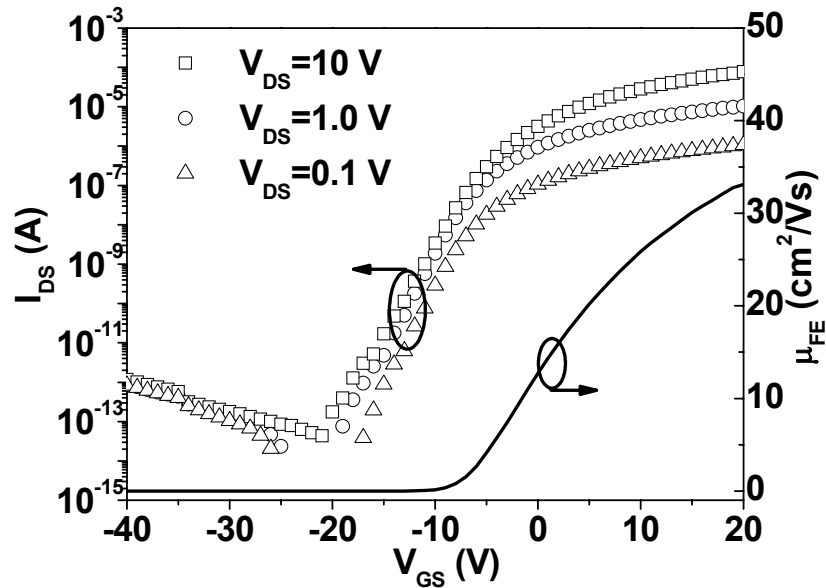


Figure 5.6: Transfer characteristics of the indium oxide TFT with the PECVD SiO<sub>x</sub> dielectric; the field-effect mobility as a function of the gate bias is also included

Another critical device parameter, the sub-threshold slope is around 2.0 V/decade, still much higher than the required value of several tens mV/decade for practical applications. From Eq. (5-1), the large value of the sub-threshold slope can be due to either large trap density at the interface or the large defect density in the channel. Since the interface condition does not change much with the thickness of the channel, the large defect density in the bulk is the most plausible reason. In order to identify this, a TFT with a 100 nm indium oxide channel is fabricated and characterized for the purpose of comparison.

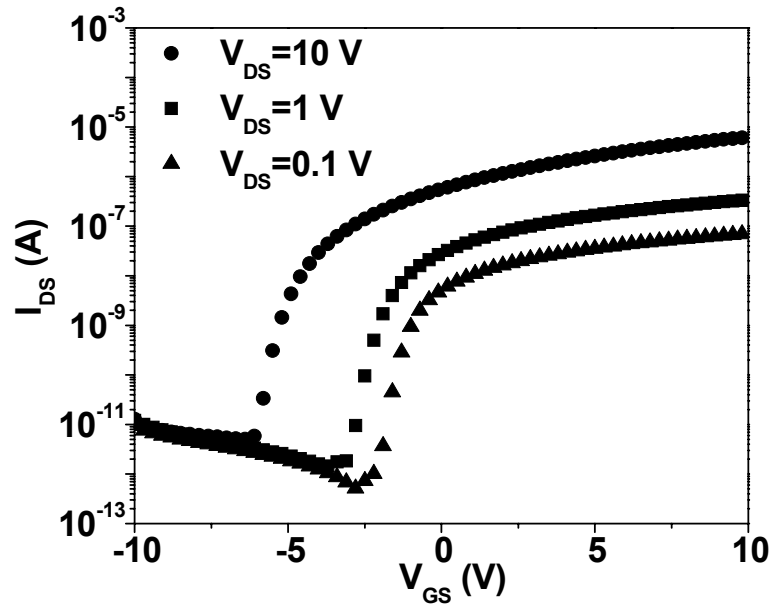


Figure 5.7: Transfer characteristics of the indium oxide TFT with the 100 nm channel layer

Figure 5.7 presents the transfer characteristics of the indium oxide TFT with the 100 nm channel layer. It is evident that the sub-threshold slope improves up to 0.5 V/decade, about four-times smaller than that of the previous TFT with a 30 nm indium oxide channel layer, suggesting that the sub-threshold slope is more dependent on the defect density in the indium oxide bulk than the trap density at the interface. Nevertheless, the field-effect mobility in this TFT is much lower ( $\sim 3 \text{ cm}^2/\text{Vs}$  at  $V_{GS} = 10 \text{ V}$ ) than the one in the previous TFT with the thinner channel layer. The intrinsic channel resistance, mainly coming from grain boundary scattering in the polycrystalline indium oxide layer, increases with the channel thickness. Therefore, the “actual” drain voltage applied to the conduction channel decreases, resulting in a lower drain current as well as a lower extracted field-effect mobility [68]. This

implies that the thick amorphous indium oxide channel is preferable in achieving TFTs with a high field-effect mobility, as well as a small sub-threshold slope.

### **5.3 TFTs with a Silicon Nitride Gate Dielectric**

The TFT with a PECVD SiN<sub>x</sub> gate dielectric is also fabricated and characterized. Figure 5.8 and Figure 5.9 illustrate the output and transfer characteristics of the first-run indium oxide TFT with the PECVD SiN<sub>x</sub> gate dielectric. Similar to the first-run TFTs with the PECVD SiO<sub>x</sub> gate dielectric, the TFT shown here also exhibits poor output characteristics and transfer characteristics. For example, the current crowding and concave shape of the I<sub>DS</sub>-V<sub>DS</sub> curves indicate that an improved source/drain contact with a low contact resistance is required. The extracted threshold voltage is around 10.5 V from the linear transfer characteristics curve at V<sub>DS</sub> = 1 V. The peak field-effect mobility is very low, around 0.18 cm<sup>2</sup>/Vs at V<sub>GS</sub> = 15 V. It also drops at the higher gate biases, indicating the same degradation as that occurred in the TFT with the PECVD SiO<sub>x</sub> gate dielectric.

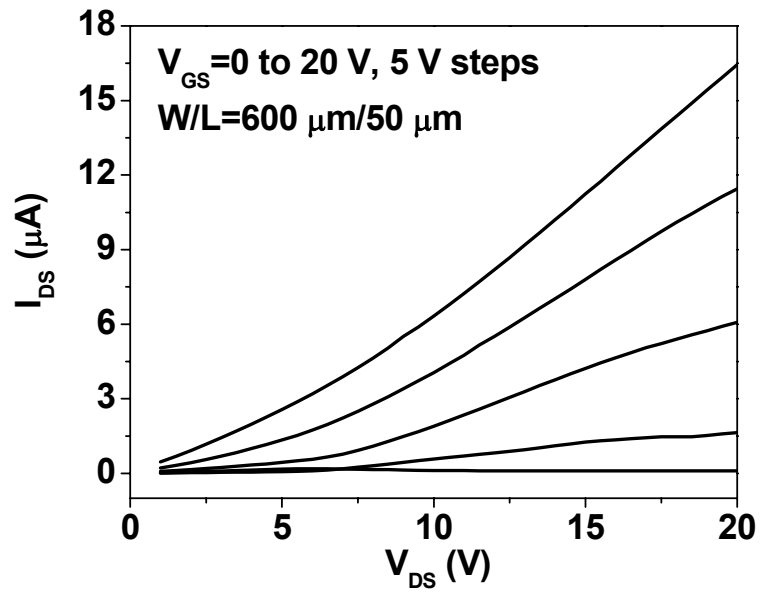


Figure 5.8: Output characteristics of the first-run indium oxide TFT with the PECVD

SiN<sub>x</sub> gate dielectric

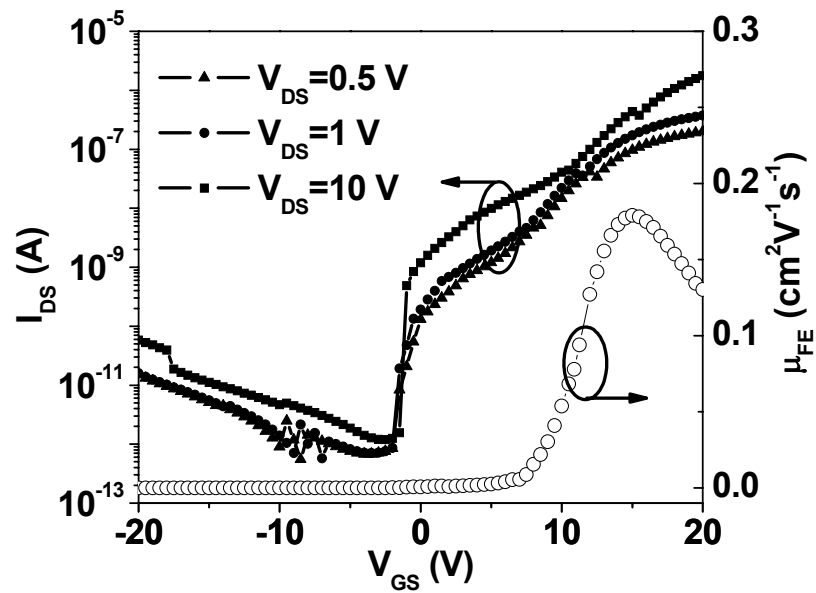


Figure 5.9: Transfer characteristics of the first-run indium oxide TFT with the

PECVD SiN<sub>x</sub> dielectric

By addressing the series resistance issues in the first-run TFTs and applying the same strategies as in Section 5.2.2, the second-run TFTs with the improved performance are fabricated and characterized. Figure 5.10 and Figure 5.11 give the output and transfer characteristics of the second-run indium oxide TFTs. Compared with the TFT performance in Figure 5.8 and Figure 5.9, both the output and transfer characteristics are substantially enhanced. The output characteristics have an obvious “hard” saturation and there is no current crowding at the low bias drain voltages. The transfer characteristics demonstrate a low OFF current of  $10^{-12}\sim 10^{-13}$  A, an ON/OFF current ratio of  $10^7\sim 10^8$ , and a field-effect mobility of  $\sim 30$   $\text{cm}^2/\text{Vs}$  at  $V_{\text{GS}} = 20$  V. The field-effect mobility does not degrade with the gate bias in the range that is investigated.

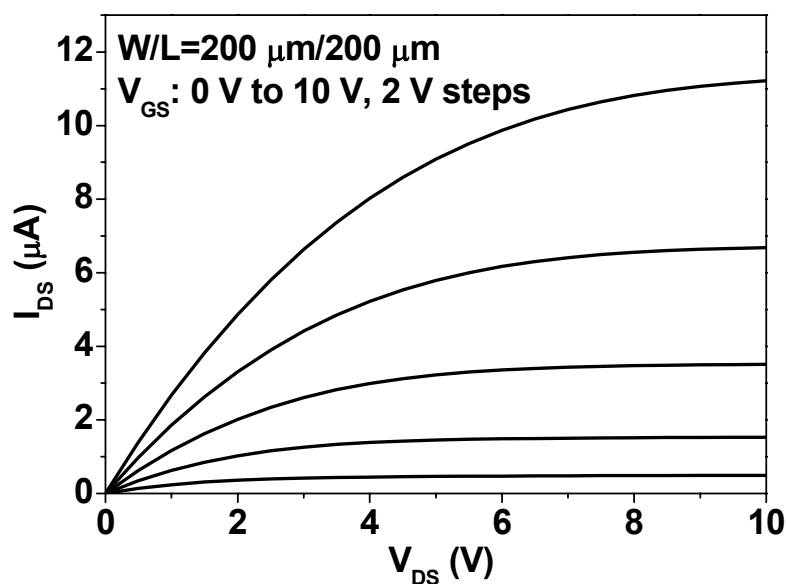


Figure 5.10: Output characteristics of the second-run indium oxide TFT with the PECVD  $\text{SiN}_x$  dielectric



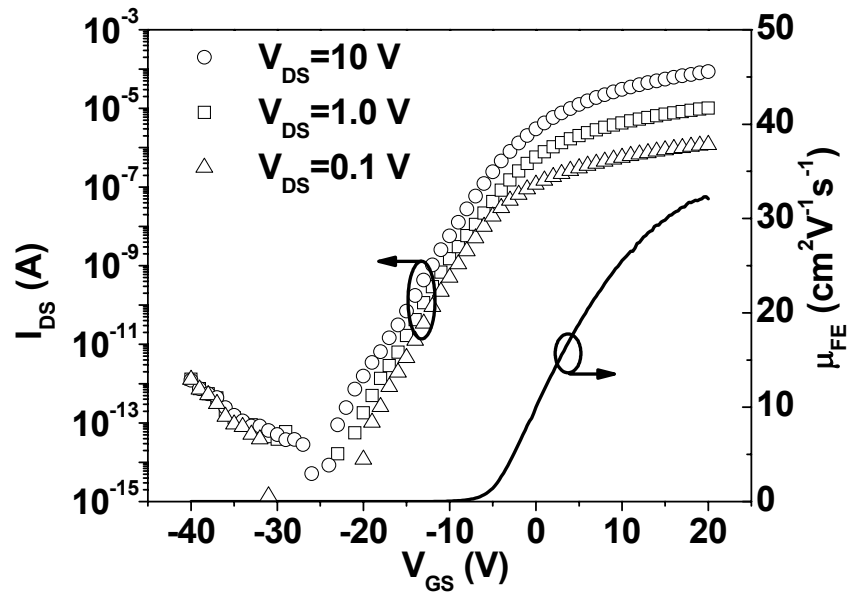


Figure 5.11: Transfer characteristics of the second-run indium oxide TFT with the PECVD SiN<sub>x</sub> dielectric

In conclusion, the effectiveness of the proposed solutions is examined by studying the transfer and output characteristics of the indium oxide TFTs. It is evident that the channel layer thickness and S/D contact resistance are two critical factors that affect the device performance. The output characteristics can be improved by decreasing the contact resistance. The sub-threshold slope and the field-effect mobility are mainly dependent on the channel layer thickness, which is related to the intrinsic channel resistance. The study also implies that the device performance of the indium oxide TFTs seems insensitive to the choice of the gate dielectric. High-performance indium oxide TFTs can be achieved with both the silicon dioxide and the silicon nitride gate dielectrics by conventional PECVD.

## **5.4 Threshold Voltage Stability**

Device stability is another concern of the indium oxide TFTs. This section is devoted to the study of the threshold voltage shift of the indium oxide TFTs under long-term constant voltage and long-term current stress modes, and to identify the mechanisms underlying the TFT instability.

### **5.4.1 Stability under Constant Voltage Stress**

To examine the threshold voltage stability, long-term stress tests are executed. The measurements are performed in the constant voltage bias stress mode, where different gate biases are applied and the drain and source are kept grounded [19]. The rapid sweeps of the transfer characteristics at the drain voltage of 1 V are carried out during the stress with an interval time of 600 s. Thus, the threshold voltages are extracted from the linear transfer characteristics.

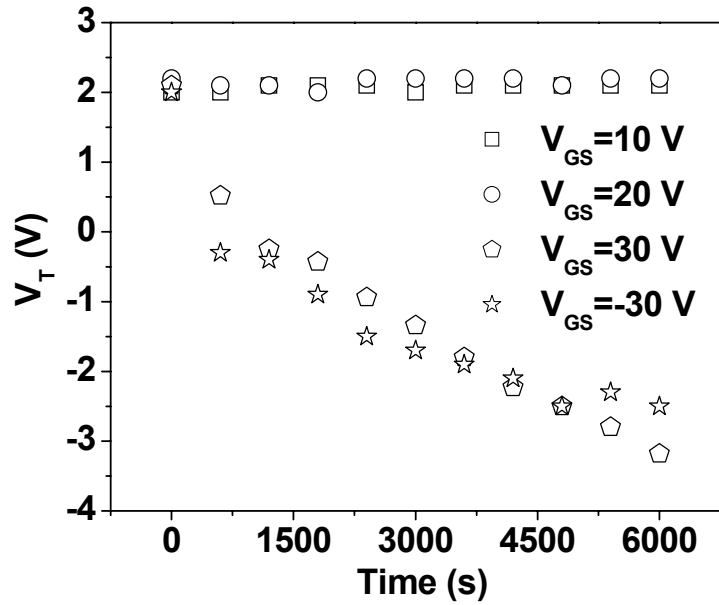


Figure 5.12: Threshold voltage of the indium oxide TFT with the PECVD SiO<sub>x</sub> dielectric as a function of the stress time

Figure 5.12 illustrates the dependence of the threshold voltage on the gate bias stress time for the indium oxide TFT with the PECVD SiO<sub>x</sub> gate dielectric. The threshold voltage is kept constant at a 10 V and 20 V gate voltage stress for 6000 s, suggesting that the TFT is highly stable under low gate bias stress conditions. However, at a high gate bias stress of 30 V and -30 V, the  $V_T$  shifts significantly towards the negative direction from 2 V to -3 V after a 6000 s stress.

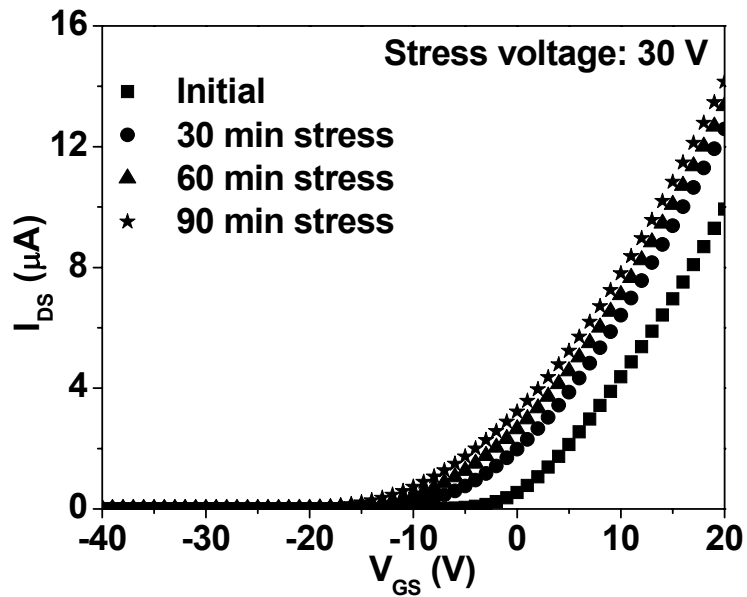


Figure 5.13: Shift in transfer characteristics of the TFT due to a stress gate bias of 30 V for different stress time

A constant voltage of 30 V stress induces a parallel shift in the transfer characteristics of the TFT, as seen in Figure 5.13. Typically, two mechanisms cause the TFT instability: defect creation in the channel and charge trapping in the gate dielectric and/or at the dielectric/channel interface [69]. It has been reported that in the a-Si:H TFTs, a positive shift of the threshold voltage under positive gate bias stress and a negative shift under a negative gate bias stress are the evidence to distinguish charge trapping from the defect generation mechanism [70]. Another distinction between these two mechanisms is the required energy level to fill and/or release the trapped charges: usually defects are located at deep energy level, and therefore, require a high energy to fill and/or release the trapped charges by means of heating and/or a high electric field; the charged traps are in the shallow energy level and are easily filled and/or released by simply relaxing the device [71].

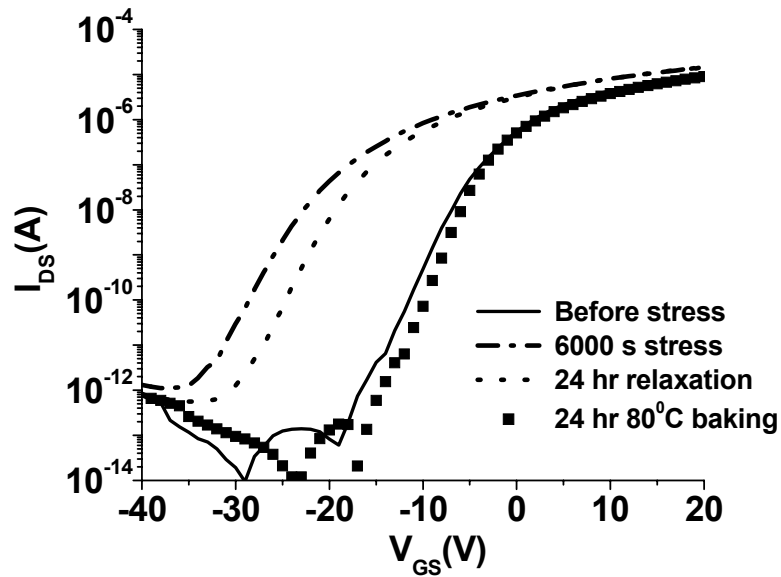


Figure 5.14: Transfer characteristics of the indium oxide TFT measured before stress, after 6000 s stress, after 24 hr relaxation, and after 80<sup>0</sup>C baking for 24 hours (stress voltage: 30 V)

The  $V_T$  here shifts towards the negative direction under a positive and negative 30 V gate bias stress, indicating that the charge trapping at the interface is less likely the cause of the observed  $V_T$  shift in the indium oxide TFT. It is also found that the transfer characteristics of the indium oxide TFT are extremely difficult to recover by itself for a long period of relaxation after the 30 V gate voltage stress. After baking the device at 80<sup>0</sup>C for 24 hours, the characteristics return to their original status, as shown in Figure 5.14. The findings strongly support the arguments that the defect creation as in a-Si:H TFTs does not likely occur in TOS TFTs, because of the absence of covalent bonds [19, 35]. Additionally, after a 30 V gate bias stress, the field-effect mobility remains the same, implying that the defects are not likely generated in the indium oxide channel. Deep-level traps, created in the gate dielectric under a high

electric field stress and the hydrogen motion from the PECVD gate dielectric to the interface are possible causes. The role of hydrogen in the oxide semiconductors are addressed theoretically [72, 73]. Unlike the hydrogen in amorphous silicon materials that plays a positive role in passivating the dangling bonds, the hydrogen in the oxide semiconductors acts as shallow donors, as well as interstitial atom. They are very small, easily activated, and become mobile in the film. Under an electric field across the gate dielectric layer, the chemical potential of hydrogen should be lower to facilitate the interlayer diffusion of the hydrogen from the gate dielectric into the active semiconductor channel [74]. The increase in the electrically active hydrogen concentration in the active channel leads to the increase in the carrier density through hydrogen doping. In addition, the defect density can be increased through the interlayer diffusion of mobile hydrogen atoms. At present, it is still too early to conclude the instability mechanisms for TOS TFTs and more research work needs to be carried out in the future.

#### **5.4.2 Stability under Current Stress**

To better evaluate the device stability, the threshold voltage shift under a long-term constant current stress mode is performed. Instead of applying a constant bias voltage to the gate, a constant current signal is applied to the drain, while keeping the gate and drain remain connected. Also, the source is grounded so that the stress current flows only through the channel [75].

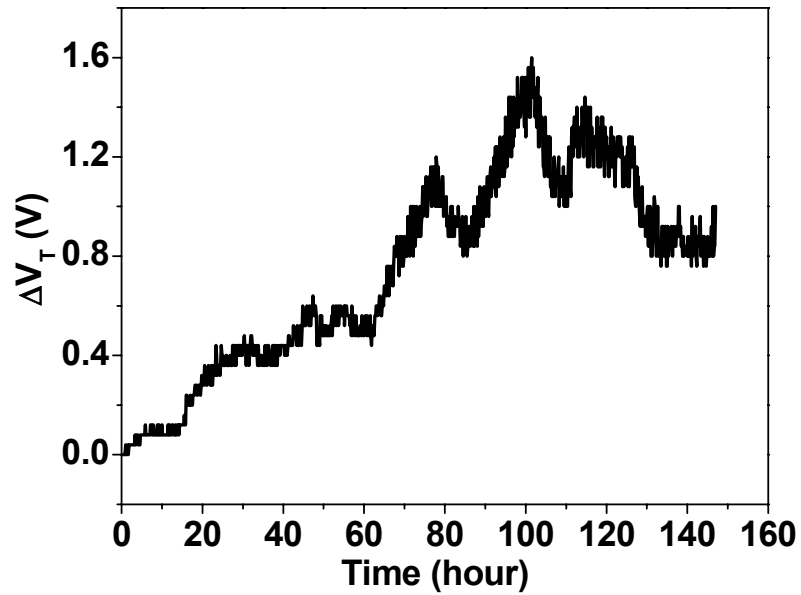


Figure 5.15: Threshold voltage shift of the indium oxide TFT with the PECVD SiO<sub>x</sub> gate dielectric under constant current stress

Figure 5.15 plots the threshold voltage shift of the indium oxide TFT as a function of the stress time under the constant current of 1  $\mu\text{A}$ . The device is highly stable and exhibits a very small  $V_T$  shift of 0.8 V after a constant current stress of approximately 150 hours. The fluctuation patterns seen in this plot are possibly due to the variation of the ambient temperature during tests.

Figure 5.16 reflects the threshold voltage shift of the TFT under a constant current stress with relaxation. In this case, the stress current signal is divided into a 13-ms driving cycle of 1.2  $\mu\text{A}$  and a 3-ms relaxation cycle of 0  $\mu\text{A}$ . During the relaxation cycle, the TFT is not under stress [76].

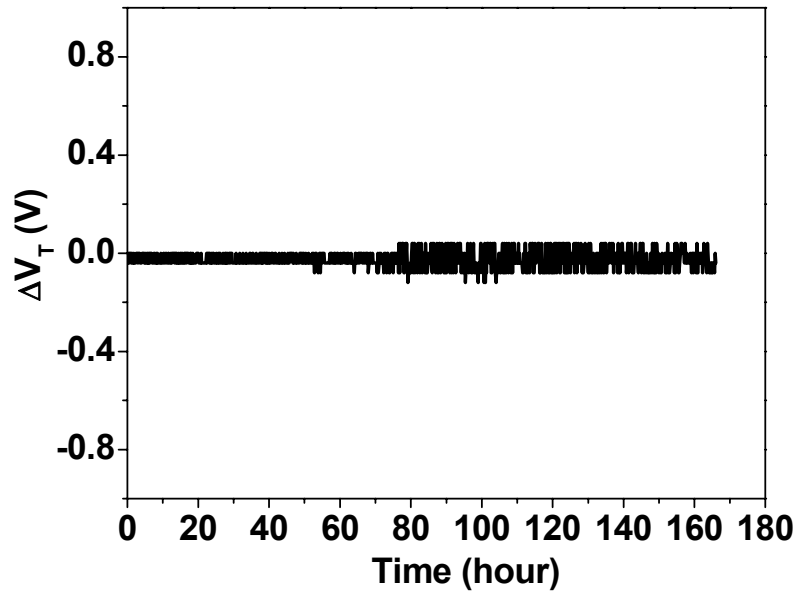


Figure 5.16: Threshold voltage shift of the indium oxide TFT under the current stress with relaxation

It is obvious that the  $V_T$  shift under the long-term constant current stress can be compensated by applying the relaxation cycle in the stress current, and there is no obvious threshold voltage change after a 160 hour stress. It is further suggested that the  $V_T$  shift in Figure 5.15 is mostly likely caused by temporary charge trapping.

In summary, the TFT reported here is highly stable under both long-term constant voltage and long-term current stress conditions. The deep-level traps, created in the gate dielectric and/or hydrogen motion from the gate dielectric to the interface, are possible mechanisms for causing the  $V_T$  shift under a high gate bias stress and the temporary charge trapping is the mechanism, accounting for the small  $V_T$  shift under a long-term constant current stress.



## 5.5 Dynamic Characteristics

Since a TFT is commonly used as a “switch” to drive active matrix displays, it is necessary to identify the operation speed and study the TFT’s dynamic behaviour. To our knowledge, such a study has not yet been reported for TOS-based TFTs in the literature.

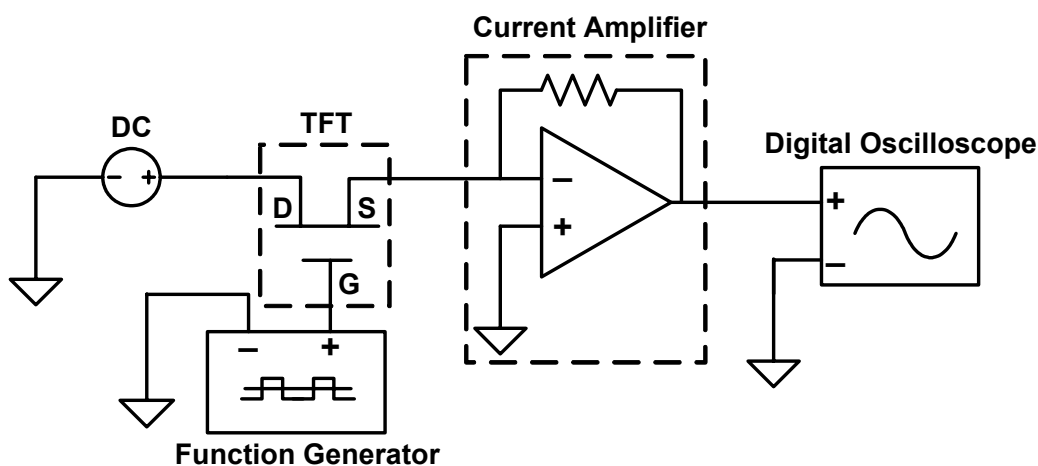


Figure 5.17: Set up for the dynamic behaviour test

The test set up for the dynamic behaviour is illustrated in Figure 5.17. The drain is biased by using a DC voltage power supply (Keithley 6430 Sourcemeter). Voltage pulses with a controllable amplitude, frequency, and duty cycle, generated by a functional signal generator (Wavetek 40MS/s Universal Waveform Generator Model 195)) are applied to the gate. A current amplifier (Keithley 427) transfers the input drain current into the voltage level, and the output signal is measured and stored in a digital form by a digital oscilloscope (Tektronix TDS5054).

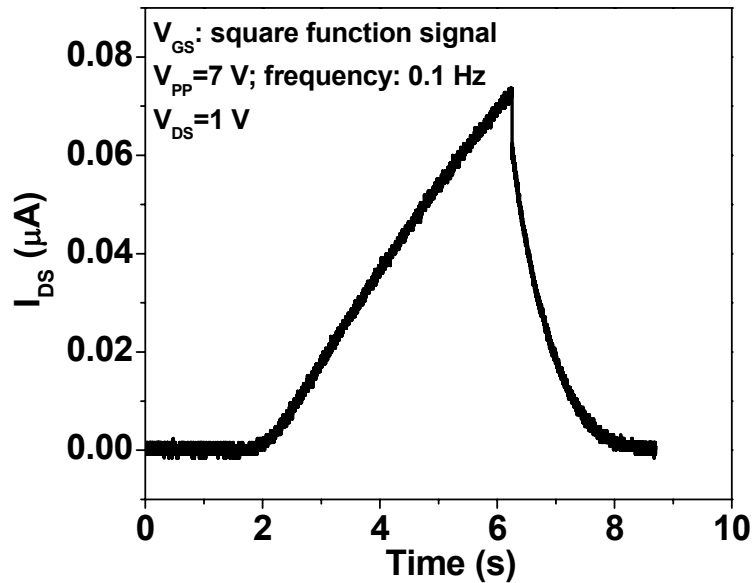


Figure 5.18: Switching waveform of the TFT with the 100 nm indium oxide channel layer

The TFT with the 100 nm indium oxide channel layer ( $W/L = 200 \mu\text{m}/ 200 \mu\text{m}$ ) is first tested. The gate dielectric in this TFT is PECVD  $\text{SiO}_x$ . Figure 5.18 sketches the switching waveform. The applied gate bias is a square function signal with a frequency of 0.1 Hz and a peak to peak voltage ( $V_{pp}$ ) of 7 V. The drain-source voltage is kept at 1 V. As observed in Figure 5.18, it is difficult to completely turn ON/OFF this TFT even under a gate bias signal with a very low frequency of 0.1 Hz. The drain current continuously increases with time and also undergoes a slow current decay when the device is turned off.

It might be attributed to the cutoff. The maximum operating frequency ( $f_{max}$ ), also called the cutoff frequency of the TFT which can be estimated from [60]:

$$f_{\max} = \frac{\mu_{FE} V_D}{2\pi L^2} \quad \text{if } V_D \leq V_{Dsat} \quad (5-2)$$

The calculated cutoff frequency is around 1 KHz for the fabricated indium oxide TFT with the 100 nm channel layer. Therefore, the very slow switching behaviour observed here cannot be explained by the cutoff.

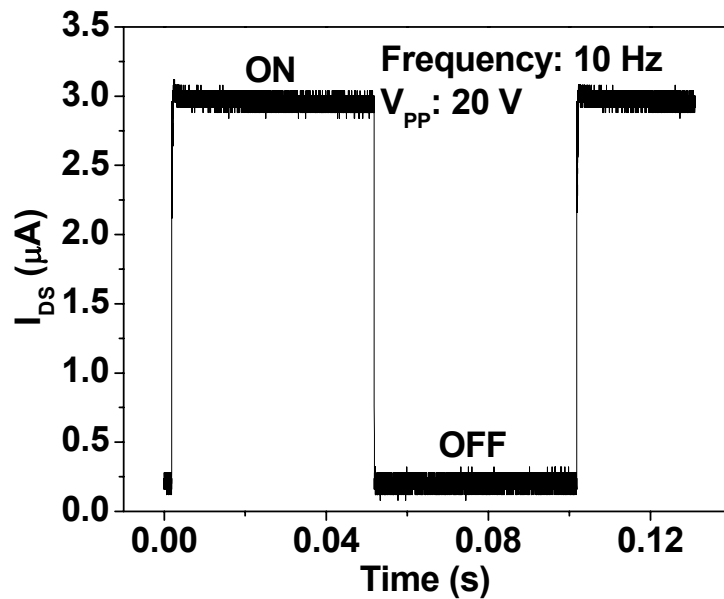


Figure 5.19: Switching waveform of the indium oxide TFT with the 30 nm channel layer

It is found that the TFT with the thinner indium oxide channel layer exhibits a much faster switching characteristic. Figure 5.19 represents the switching waveform of the indium oxide TFT with the 30 nm channel layer. The W/L ratio of this TFT is 100  $\mu\text{m}/100 \mu\text{m}$ . The applied gate bias is also a square function signal with a frequency of 10 Hz and a  $V_{pp}$  of 20 V. The TFT can be switched ON/OFF to respond to the continuous 10 Hz square function gate bias signal.

Consequently, the channel thickness plays a very critical role in the TFT operation and the TFT with a thick channel layer has an undesirable “memory” phenomenon. Together with the morphological structure, observed in Section 3.2.7, it is anticipated that such a ‘memory’ effect stems from the top polycrystalline indium oxide layer due to the charge storage in the polycrystalline layer, where a large amount of grain boundaries exist. From this perspective, amorphous indium oxide is preferred as a semiconductor channel instead of its polycrystalline counterpart for TFTs. Here, the research results of the dynamic behaviour provide more evidence to support the view that amorphous TOSs are superior to polycrystalline TOSs, as channel materials in TOS TFTs [77].

## 5.6 Summary

In this chapter, device processing, device performance and stability, and dynamic characteristics of the indium oxide TFTs with the PECVD gate dielectrics are presented and discussed. Three goals of this research work in this chapter are achieved: the demonstration of the TFT with the semiconducting indium oxide channel; the device optimization through addressing the contact issue and shrinking channel layer thickness; and the detailed investigation of device physics, instability mechanisms, and the dynamic characteristics of the fabricated indium oxide TFTs.

Here, a descriptive model in Figure 5.20 is proposed to summarize those factors that affect the device performance of TOS TFTs with PECVD dielectrics in general. These factors include the contact resistance between source/drain and semiconductor channel ( $R_C$ ); the intrinsic resistance of the semiconducting layer ( $R_i$ ); the intrinsic



# Chapter 6

## Conclusions and Contributions

In this thesis, the capability of using the IBAE to fabricate TOSs, in particular, zinc oxides and indium oxides is demonstrated. It is believed that this technology is also applicable to other oxide systems.

A detailed material study of zinc oxides and indium oxides is conducted. The electrical, optical, structural, mechanical, topological, and morphological properties of the developed films are examined. The achieved performance of semiconducting oxide films enables the use for active device applications.

The core parts of this thesis address the device applications of TOSs. Most of this research proves concepts, demonstrates the working devices, investigates device processing issues to further optimize device performance, and explores device performance including long-term device stability and dynamic characteristics.

The contributions of this research to the field of transparent electronics are summarized.

- One of the first investigations of the use of IBAE to fabricate transparent oxide semiconductors and devices.
- The successful fabrication and characterization of ZnO-based p-i-n and n-i-p heterostructure diodes with the lowest reported leakage current that can be implemented for low-level UV detection.

- The study of current-voltage characteristics, dark current transients, spectral response, and linearity to identify the leakage current mechanisms, and determine the quantum efficiency and photosensitivity of ZnO-based photodiodes.
- The fabrication and study of indium oxide TFTs with PECVD gate dielectrics to find solutions for device processing issues and identify factors that affect device performance.
- The proof that high-performance indium oxide TFTs can be achieved with PECVD gate dielectrics.
- The achievement of highly stable indium oxide TFTs with a very small  $V_T$  shift under both a long-term constant voltage and long-term current stress conditions and the preliminary investigation of instability mechanisms.
- The first report on dynamic characteristics of TOS TFTs.

# Appendix

## TFT Parameter Extraction

The TFT parameters, including threshold voltage ( $V_T$ ), sub-threshold slope (S), and field-effect mobility ( $\mu_{FE}$ ) are extracted according to the square-law theory [60]. An explicit  $I_{DS}$ - $V_{DS}$  relationship in the linear operation of the TFT is expressed as:

$$I_{DS} = \frac{W\mu_{FE}C_{ox}}{L} [V_{GS} - V_T]V_{DS} - \frac{V_{DS}^2}{2} \quad (V_{DS} \leq V_{GS} - V_T).$$

The field-effect mobility is deduced from the transconductance:

$$g_m = \frac{dI_{DS}}{dV_{GS}} = \frac{C_{ox}\mu_{FE}W}{L} V_{DS}.$$

By knowing the gate capacitance ( $C_{ox}$ ), W/L ratio, and a certain  $V_{DS}$  in the linear operation of the TFT, the field-effect mobility which is a function of the  $V_{GS}$  is calculated.

The threshold voltage can be extracted by two methods: (1) from the transfer characteristics in the linear operation of the TFT and (2) from the transfer characteristics in the saturation operation of the TFT. In the linear transfer characteristics, where  $V_{DS} \leq V_{GS} - V_T$ ,  $V_T$  is given as the intercept of the line that is extrapolated on the  $V_{GS}$  axis. The  $V_T$  is also extracted from the following saturation operation of the TFT:

$$I_{DS} = \frac{C_{ox}\mu W}{2L} (V_{GS} - V_T)^2 \quad (V_{DS} > V_{GS} - V_T).$$



The intercept of the  $I_{DS}^{1/2} - V_{GS}$  plots is the extracted  $V_T$ . It is noteworthy that in this thesis, the first method is used to extract the  $V_T$ .

The sub-threshold slope is defined as the voltage that is required to enhance the drain current in the sub-threshold regime by a factor of ten and it is given by:

$$S = \frac{dV_{GS}}{d(\log I_{DS})} \quad (V_{GS} \leq V_T).$$

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