Fabrication and Analysis of Bottom Gate Nanocrystalline Silicon Thin Film Transistors

by

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Author’s Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners. I understand that my thesis may be made electronically available to the public.

Abstract

Thin film transistors (TFTs) have brought prominent growth in both variety and utility of large area electronics market over the past few decades. Nanocrystalline silicon (nc-Si:H) TFTs have attracted attention recently, due to high-performance and low-cost, as an alternative of amorphous silicon (a-Si:H) and polycrystalline silicon (poly-Si) TFTs. The nc-Si:H TFTs has higher carrier mobility and better device stability than a-Si:H TFTs while lower manufacturing cost than poly-Si TFTs. However, current nc-Si:TFTs have several challenging issues on materials and devices, on which this thesis focuses.

In the material study, the gate quality silicon nitride (a-SiNx) films and doped nc-Si:H contacts based on conventional plasma enhanced chemical vapor deposition (PECVD) are investigated. The feasibility of a-SiNx on TFT application is discussed with current-voltage (I-V)/capacitance-voltage(C-V) measurement and Fourier Transform Infrared Spectroscopy (FTIR) results which demonstrate 4.3 MV/cm, relative permittivity of 6.15 and nitrogen rich composition. The doped nc-Si:H for contact layer of TFTs is characterized with Raman Spectroscopy and I-V measurements to reveal 56 % of crystalinity and 0.42 S/cm of dark conductivity.

Inverted staggered TFT structure is fabricated for nc-Si:H TFT device research using fully wet etch fabrication process which requires five lithography steps. The process steps are described in detail as well as adaptation of the fabrication process to a backplane fabrication for direct conversion X-ray imagers. The modification of TFT process for backplane fabrication involves two more lithography steps for mushroom electrode formation while other pixel components is incorporated into the five lithography step TFT process.

The TFTs are electrically characterized demonstrating 7.22 V of threshold voltage, 0.63 S/decade of subthreshold slope, 0.07 $cm^2/V \cdot s$ of field effect mobility, and 10^6 of on/off ratio. The transfer characteristics of TFTs reveal a severe effect of parasitic resistance which is induced from channel layer itself, a contact between channel layer and doped nc-Si:H contact layer, the resistance of doped nc-Si:H contact layer, and a contact between the doped nc-Si:H layer and source/drain metal electrodes. The parasitic resistance effect is investigated using

numerical simulation method by various parasitic resistances, channel length of the TFT, and intrinsic properties of nc-Si:H channel layer. It reveals the parasitic resistance effect become severe when the channel is short and has better quality, therefore, several further research topics on improving contact nc-Si:H quality and process adjustment are required.

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Lastly, I must express my sincere appreciation to my parents and my little sister, Rachel Shin, for their endless support and encouragement on the study.

To my parents, and my little sister, Rachel Shin

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Chapter 1
Introduction

Hydrogenated amorphous silicon (a-Si:H) is still most popular technology in Thin Film Transistors (TFTs) for large area electronics such as X-ray imagers, and it is also heavily utilized in photovoltaic applications. a-Si:H TFTs have low off current and sufficient on/off current ratio for current large area applications; however, their field effect mobility and stability of threshold voltage. The low mobility limits not only pixel size but also prohibits complementary circuit implementation using a-Si:H. Since the hole mobility in a-Si:H is several orders lower than electron mobility, p-type transistor implementation is not practical which makes designing usable complementary circuit impossible. On the other hand, the drifting threshold voltage means that a-Si:H TFTs cannot be implemented in column multiplexor and row shift register circuits [1]. Polycrystalline silicon (Poly-Si) had been proposed to resolve these problems and replace a-Si:H. However, Poly-Si technology has drawbacks on production side since it requires a large and expensive laser annealing system.

Nanocrystalline silicon (nc-Si:H) was proposed as a strong candidate to replace current a-Si:H with higher field effect mobility in top gate TFTs [2] and stable threshold voltage in bottom gate TFTs [3]. Moreover, nc-Si:H can be deposited by conventional plasma enhanced chemical vapor deposition (PECVD) which is the mainstream of a-Si:H production technology. In theory, nc-Si:H has higher or equivalent carrier mobility and stable threshold voltage due to its higher crystallinity than a-Si:H counterpart.

In this thesis, the electrical (field effect mobility, transconductance) characteristics bottom gate nc-Si:H TFT, and structural (crystallinity, chemical composition) information of silicon nitride and n+ nanocrystalline silicon films grown by PECVD will be presented and discussed. Moreover, numerical analysis method of the bottom gate nc-Si:H TFT will be introduced to estimate performances in various conditions, i.e. different channel length, parasitic resistance and nc-Si:H defect states, using Atlas TCAD simulation tool from Silvaco Corporation.

1.1 Direct Conversion X-ray Image Sensor

A large area active matrix flat panel digital X-ray imagers based on a-Si:H technology have been developed over the past decade. Recently, a-Si:H active matrix flat panel digital X-ray imager using sensor-and-switch architecture with areas of 30 × 40 cm^2 were demonstrated for diagnostic medical chest radiography [4]. The motivation for implementation of the active matrix flat panel X-ray imagers includes improved image quality, large area X-ray imaging capability, a compact flat panel structure, low storage cost, better waste management, and digitalized handling/storage of sensory information. The basic imaging unit of active matrix flat panel X-ray imagers is the pixel. The pixel is addressed by a matrix of gate and data lines, and operates in storage (or integration) mode. During the off-period, the sensor charge is integrated, and when the switch is turned on, the charge in the sensor is transferred to the data line where it is detected by readout circuitry. There are two detection schemes for X-rays: direct conversion, where the X-rays are directly absorbed and converted to electrical charge in the detector, i.e. amorphous selenium (a-Se); and indirect conversion, where the X-rays are first converted into visible light by a phosphor layer, which in turn is converted to electrical charge in the photodetector. In both cases, the electrical charge is readout by active matrix TFT array. The direct conversion type has superior image quality, cheaper and easier to manufacture due to its simpler structure [5]. Figure 1.1 illustrates schematics of direct conversion X-ray imager.

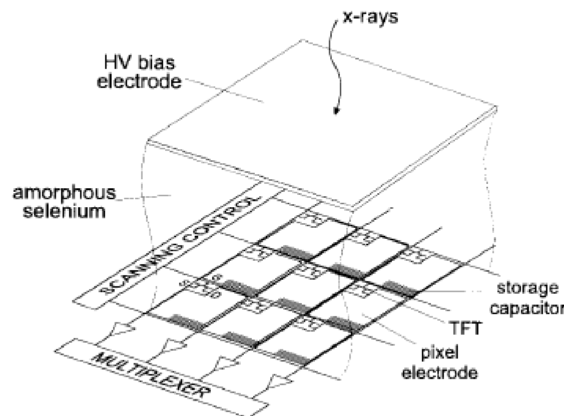


Figure 1.1 Schematic of Direct Conversion X-ray Imager using a-Si:H TFT active matrix array, from [6]

1.2 Motivation

As the nc-Si:H was proposed as one of candidates to replace a-Si:H technology [2,3], direct implementation of nc-Si:H to current a-Si:H process technology using the bottom gate a-Si:H TFT process which was already developed by University of Waterloo [7]. The main objective of this thesis is the implementation of the bottom gate nc-Si:H TFT to the a-Si:H TFT process technology, fabrication of backplane for direct conversion X-ray imager, and characterizing the TFT performance using computational numerical analysis method without fabricating various types of TFTs into actual samples.

1.3 Overview of the Thesis

In this thesis the electrical properties of bottom gate nc-Si:H TFT will be studied as well as fabrication process and film characterizations. The fabrication process will be shown with step by step with illustrations. The film characteristics of the TFT dielectrics and contact layer will be extracted with FTIR, Raman Spectroscopy, I-V and C-V measurements. To study the electrical properties of TFTs, conventional performance factor extraction method using square root model and numerical analysis using Atlas TCAD simulation will be demonstrated.

Chapter 2
Background

2.1 Thin-Film Materials

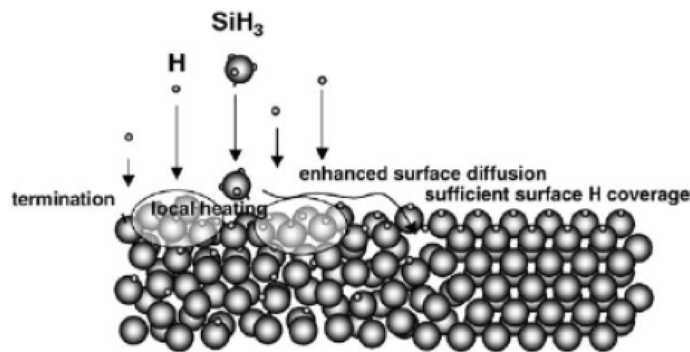
2.1.1 Amorphous Silicon

Amorphous silicon began to be used as a semiconductor in 1960s. The first amorphous silicon was prepared by sputtering a silicon target or by thermal evaporation and it had poor characteristics. Sterling and Swann [8] were the first to use plasma enhanced chemical vapor deposition (PECVD) to grow a-Si:H and amorphous silicon nitride (a-SiN) from silane (SiH_4) gas in 1965. The use of SiH_4 caused hydrogen to be incorporated into films and they passivated defects dangling bond defects leading better quality material. The first devices utilizing a-Si:H in a practical way were solar cells. Sanyo first commercialized calculators powered by a-Si:H solar cells in 1979. The TFT concept was pioneered by Weimer [9]. Research on TFTs was not concentrating on a-Si:H but other materials such as cadmium sulfide (CdS) for channel layer. The first TFTs made using a-Si:H reported from Le Cromber et al. [10] in 1979. Today, a-Si:H incorporated flat panel displays surpassed display market share that of cathode ray tube (CRT) displays. The a-Si:H TFTs are now being used as switching elements in X-ray imagers [11] and with further research, a-Si:H could be a promising alternative to c-Si for large-area, low-cost, and possibly flexible solar cells [12].

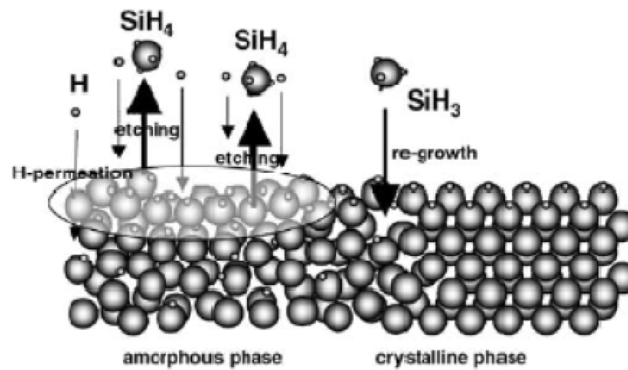
However, a-Si:H TFT has a few drawbacks. Due to its amorphous nature, carriers in a-Si:H device cannot travel fast since the excessive trapping and detrapping process in localized states and scattering. The usual field effect mobility of a-Si:H TFT is 0.1 to 1 $cm^2/V\cdot s$ [25]. Although it is sufficient for current LCD applications, the performance is significantly lower than crystalline silicon transistors. Also, instability of a-Si:H TFT is one of noticeable drawbacks. When a-Si:H TFT is subjected to a prolonged gate voltage, the drain current gradually decreases over time as well as shift in threshold voltage. Although the instability is not a serious issue for X-ray imager implementation, it prevents a-Si:H TFTs from being used for Organic Light Emitting Diode (OLED) display applications [45].

2.1.2 Nanocrystalline Silicon

Nanocrystalline silicon (nc-Si:H) is a close relative of polysilicon. Polysilicon has long been used as a gate conductor for metal oxide field effect transistors (MOSFETs). This particular polysilicon is processed at high temperature and also heavily doped so that it can be used as a "polysilicon" gate. At low temperatures, the only options are to a-Si:H into polysilicon using laser crystallization [39] which require high manufacturing cost, complex fabrication process and have poor uniformity [40]. However, nc-Si:H can be grown by PECVD with a plasma heavily diluted with hydrogen (H_2) or other etchant gases such as SiF_4 or $SiCl_2H_2$ [13]. The most convenient way to fabricate nc-Si:H films using current a-Si:H techniques is to use PECVD with high (at least 95%) hydrogen dilution. nc-Si:H has many promising advantages over a-Si:H while having cheaper manufacturing cost. One is that it have increased stability since it has lower hydrogen concentration than a-Si:H [41]. However, most important advantages are that it can have higher field effect mobility due to the presence of silicon crystallites [42] as well as increased doping efficiency [43]. In addition, the device non-uniformity in the nc-Si:H TFTs is significantly lower than polysilicon counterparts due to smaller but uniformly-distributed crystalline grains in nc-Si:H.



(a)



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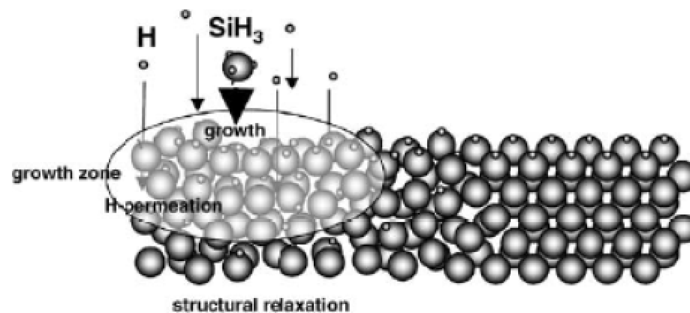


(c)

Figure 2.1 Growth models for nc-Si:H: (a) surface-diffusion model, (b) etching model, and (c) chemical annealing model, from [14].

There are several theories describing the mechanisms of nc-Si:H film growth. Matsuda [14] suggests three models of nc-Si:H growth: the "surface-diffusion model," the "etching model," and the "chemical annealing model." In the surface-diffusion model, large amount of hydrogen atoms fully cover the film-growing surface as well as producing local heating through hydrogen exchange reactions, enhancing the surface diffusion of film precursors (SiH_3). The film precursors adsorb on the surface, leading to the nucleus formation. As a result, epitaxial-like crystal growth takes place. In the etching model, atomic hydrogen breaks weak Si–Si bonds in the amorphous network. Each broken bond is replaced with a

new film precursor (SiH_3) to create a new Si–Si bond leading to crystalline structure. The chemical annealing model has been proposed to explain a layer-by-layer growth of nc-Si:H films by simplifying the growth as a repetition of a-Si:H growth and hydrogen plasma treatment. During hydrogen plasma treatment, lots of hydrogen atoms are incorporated into the film, leading to a crystallization of amorphous phase through the formation of a flexible network without noticeable removal process of silicon atoms. The three models are illustrated in Figure 2.1.

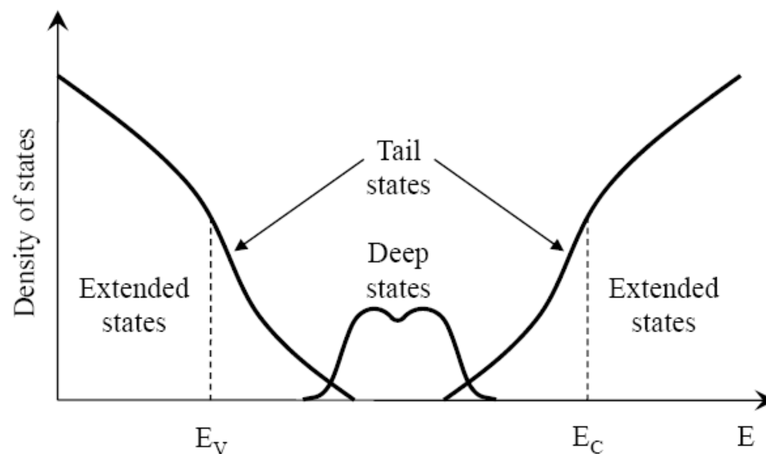


Figure 2.2 Density of states within the band gap of disordered materials such as nc-Si:H, polysilicon and a-Si:H [15]

The defects in nc-Si:H (as well as in polysilicon and a-Si:H) can be described as a typical density of defect states (DOS) distribution [15]. Figure 2.2 illustrates the typical DOS in a-Si:H/polysilicon/nc-Si:H material. Here, each half of the gap is divided into two sections: deep and tail states. States in upper half of the band gap are acceptor-like (positively charged when unoccupied and neutral when occupied by electrons), and states in the lower half of the gap are donor-like (neutral when unoccupied and negatively charged when occupied by electrons) [15]. The two types of deep states can be modeled by using a Gaussian distribution expressed by,

$$g_{GA}(E) = NGA \exp\left[-\left(\frac{EGA - E}{WGA}\right)^2\right] \quad (2.1)$$

$$g_{GD}(E) = NGD \exp\left[-\left(\frac{E - EGD}{WGD}\right)^2\right] \quad (2.2)$$

where E is the trap energy, and subscripts G, A, and D stands for Gaussian, acceptor and donor states, respectively. For Gaussian distributions, density of states is described by its total density of states (NGA and NGD), its characteristic decay energy (WGA and WGD), and its peak energy/peak distribution (EGA and EGD) [16]. Two tail states can be modeled using exponential distribution as,

$$g_{TA}(E) = NTA \exp\left(\frac{E - E_C}{WTA}\right) \quad (2.3)$$

$$g_{TD}(E) = NTD \exp\left(\frac{E_V - E}{WTD}\right) \quad (2.4)$$

where the subscript T stands for tail states, E_C is the conduction band energy, and E_V is the valence band energy. For exponential tail distributions, the density of states is described by its conduction and valence band edge intercept densities (NTA and NTD), and by its characteristic decay energy (WTA and WTD) [16]. The total density of states in the bandgap is the sum of above four distributions, shown below.

$$g(E) = g_{GA}(E) + g_{GD}(E) + g_{TA}(E) + g_{TD}(E) \quad (2.5)$$

Table 2.1 summarizes typical values of these parameters (NTA, NTD, NGA and etc.) for a-Si:H and polycrystalline silicon materials.

Table 2.1 Summary of typical values for the density of states (DOS) in amorphous and polysilicon [16]

Parameter	a-Si:H	Poly-Si
NTA (cm^{-3})	1×10^{21}	1.12×10^{21}
NTD (cm^{-3})	1×10^{21}	4×10^{21}
NGA (cm^{-3})	4.5×10^{21}	1×10^{18}
NGD (cm^{-3})	4.5×10^{21}	3×10^{18}
EGA (eV)	0.62	0.4
EGD (eV)	0.78	0.4
WTA (eV)	0.033	0.025
WTD (eV)	0.049	0.05
WGA (eV)	0.15	0.1
WGD (eV)	0.15	0.1

2.1.3 Silicon Nitride

Silicon Nitride was first developed in 1960s in a search for high density, high strength and high toughness materials. The development was primarily aimed to replace metals with ceramics in advanced turbines and reciprocating engines to achieve higher operating temperatures and efficiencies [44]. For electrical applications, the Silicon nitride was also developed for electronic purposes such as TFT gate dielectric, device passivation, diffusion and oxidation barriers, interlevel isolation, and photolithographic masks [17]. To adopt the silicon nitride to low temperature (around 260-300 ^{o}C) technology, PECVD method has been researched from 1970s [18]. PECVD silicon nitrides (a-SiNx) are typically deposited using silane (SiH_4) and ammonia (NH_3) or ammonia/nitrogen (NH_3/N_2) mixtures. Usually, nitrogen rich a-SiNx is preferred for TFT gate dielectric. It can be characterized with conventional

thin film analytical tools such as FTIR, ESR, Auger, ESCA, SIMS and I-V/C-V measurements. In this thesis, FTIR and I-V/C-V measurements are used to characterize a-SiNx which was deposited in home facility.

2.1.4 n+ Nanocrystalline Silicon

It has been long known that the nanocrystalline silicon (nc-Si:H) can be doped, as evidenced by the use of doped nc-Si:H layers in solar cells. The crystalline content in nc-Si:H allows substitutional doping by creating donor or acceptor states inside of the crystalline area. Doping in a-Si:H is very inefficient since dopant atoms mostly bond in their lowest energy configuration which does not lead to a donor state. Doped n+ nc-Si:H is currently the state-of-the-art in highly conductive source and drain contacts for TFTs [19] and was studied extensively by Kanicki et al. [20]. Recently, top-gate nc-Si:H TFTs with silicon oxide dielectric have demonstrated field effect mobility [13,19]. The source/drain contact n+ nc-Si:H can be characterized by crystalinity and dark conductivity. To measure crystalinity of n+ nc-Si:H film, Raman spectroscopy can be used while conventional I-V measurement method can be applied to extract dark conductivity.

2.2 Thin Film Transistor

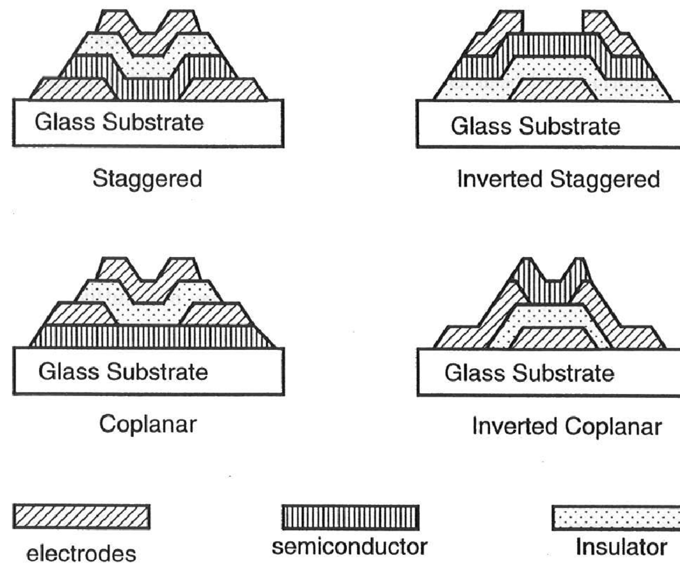


Figure 2.3 Illustration of four different types of TFTs: Staggered, inverted staggered, coplanar, and inverted coplanar. From [21]

Unlike crystalline silicon MOSFET's, there are many different device geometries possible for thin film transistors. Top-gate, bottom-gate (also known as "inverted") are two classes of devices. The latter has its gate electrode and gate dielectric below a-Si:H or nc-Si:H active layer and the former has above the active layer. These two cases subdivided into coplanar and staggered devices, giving a total of four types of basic structures illustrated in Figure 2.3. The term coplanar/staggered describes the location of source and drain contacts relative to the gate. In coplanar case, the source and drain contacts are on the same side of the active region as the gate contact while the source and drain contacts are on the opposite side of the gate contact in staggered case. The most popular configuration for a-Si:H is inverted staggered. The bottom-gate, or inverted staggered, is a widely used process for a-Si:H TFTs, and it is the best TFT structure to adopt nc-Si:H TFT for most of current a-Si:H TFT applications without modification of production lines. In this chapter, basic concepts on TFT operations and parameter extraction methods will be described.

2.2.1 Basic Operation

In terms of electrical operation, TFTs are similar to MOSFETs. Therefore, same I-V relationship can be applied to describe their operation. However, density of states in channel layer, which are illustrated in Figure 2.2, make difference. Figure 2.4 shows basic operation of TFT when gate and drain bias is applied. Applying a positive gate bias induces charges near the channel layer/gate dielectric interface by forming electron accumulation layer. Thus, the positive gate bias increases conductivity between source and drain as well as the positive bias between source and drain. The magnitude of drain current in TFTs is usually much smaller than that in MOSFETs, due to the defects in the channel layer.

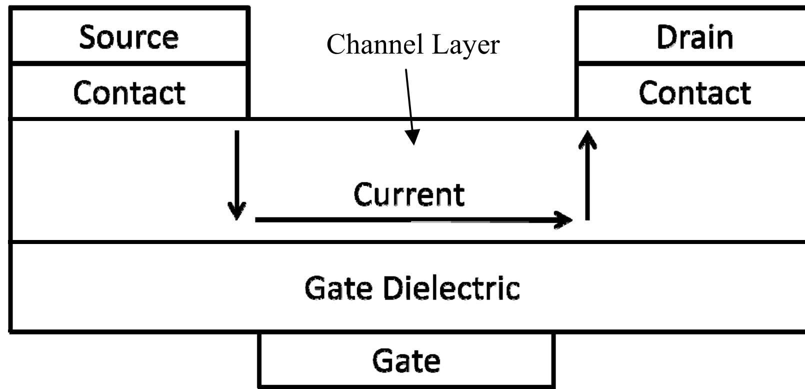


Figure 2.4 Illustration of TFT basic operation

In the channel layer, the tail states act as temporary traps for conduction electrons. The electrons may experience frequent trapping and release events into or from various energy levels within the band gap during their journey in the channel layer. In the presence of the trapping/detrapping events, the field effect mobility (μ_{EF}) can be expressed as

$$\mu_{EF} = \mu_0 \frac{\tau_{free}}{\tau_{free} + \tau_{trapped}} \tag{2.6}$$

where μ_0 is the field effect mobility of electrons without trapping, and τ_{free} and $\tau_{trapped}$ are the time intervals that electrons are free and trapped, respectively [22]. Usually, the trapped interval is larger than free interval which degrades actual field effect mobility significantly.

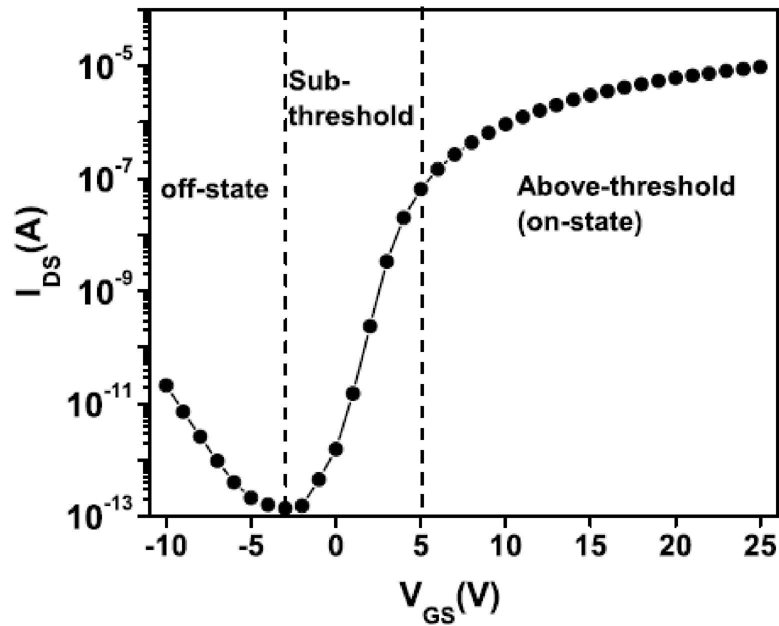


Figure 2.5 A typical transfer characteristic of a bottom gate nc-Si:H or a-Si:H TFT [25]

The operation of a TFT is illustrated in Figure 2.5 as drain current versus gate bias: transfer characteristic. It can be seen that there are three regions of operation. For small gate voltages, the Fermi level lies in the deep states (Figure 2.2) and it can be assumed that the energy bands are close to flat-band condition. By increasing the positive gate bias, band bending close to the gate dielectric interface occurs, meaning the Fermi level moves up through the deep states and towards the band tail states [23,24]. In this state, most of induced electrons are trapped in deep defect states; a small but negligible amount of electrons may occupy tail states yield a small amount of drain current. This operation region is called the subthreshold region shown in Figure 2.5. The subthreshold region continues until the deep states are filled up with electrons and the concentration of electrons in tail states exceeds that of trapped electrons in deep states. As the gate bias continues to increase, it finally exceeds a threshold voltage (V_{th}) which implies the Fermi level now lies in the tail states [23,24]. For gate-source bias (V_{gs}) higher than V_{th}, the TFT is operating in the above-threshold regime, i.e. on-state. To simplify characterization, the square root equation which is used for MOSFET characterization can be adopted. In linear region, where the source-drain bias (V_{ds}) is equal or

lower than $V_{gs} - V_{th}$, the source-drain current (I_{ds}) is linearly proportional to V_{ds}, which can be expressed as:

$$I_{ds} = \mu_{EF} C_{gate} \frac{W}{L} \left[(V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right] \tag{2.7}$$

where W, L and C_{gate} are the TFT channel width, length and gate capacitance, respectively.

When $V_{ds} = V_{gs} - V_{th}$, the accumulation channel is pinched off near the drain and drain current saturates and becomes independent from V_{ds}. For $V_{ds} \geq V_{gs} - V_{th}$, TFTs operate in saturation regime. The I_{ds} in the saturation regime is written by

$$I_{ds} = \frac{1}{2} \mu_{EF} C_{gate} \frac{W}{L} (V_{gs} - V_{th})^2 \tag{2.8}$$

The third operation region is the off-state when negative gate voltages are applied. In this case, the drain current (I_{ds}) is called off-current or drain leakage current. The mechanisms of off-current have not yet fully confirmed in nc-Si:H TFTs, although there are several researches to investigate the drain leakage current mechanism for inverted bottom gate structure [25] and inverted top gate structure [26].

2.2.2 Parameter Extraction Method

Extraction of performance factors from experimental data will be demonstrated in this section. The field effect mobility, threshold voltage, subthreshold slope, on/off ratio and transconductance can be obtained from the TFT transfer characteristics.

To extract field effect mobility and threshold voltage, a linear fit on square root of the linear scale data is required as shown in Figure 2.6. The threshold voltage can be determined by extrapolating the linear fit down to the x-intercept. To obtain the field effect mobility, first, the slope of the linear fit must be drawn from the most accurate linear fit data. The slope can be interpreted analytically from (2.8):

$$\text{slope} = \frac{d\sqrt{I_{ds}}}{dV_{gs}} = \sqrt{\frac{1}{2} \mu_{EF} C_{gate} \frac{W}{L}} \tag{2.9}$$

Therefore, the field effect mobility can be determined by

$$\mu_{EF} = \text{slope}^2 \left(\frac{2L}{WC_{gate}}\right) \tag{2.10}$$

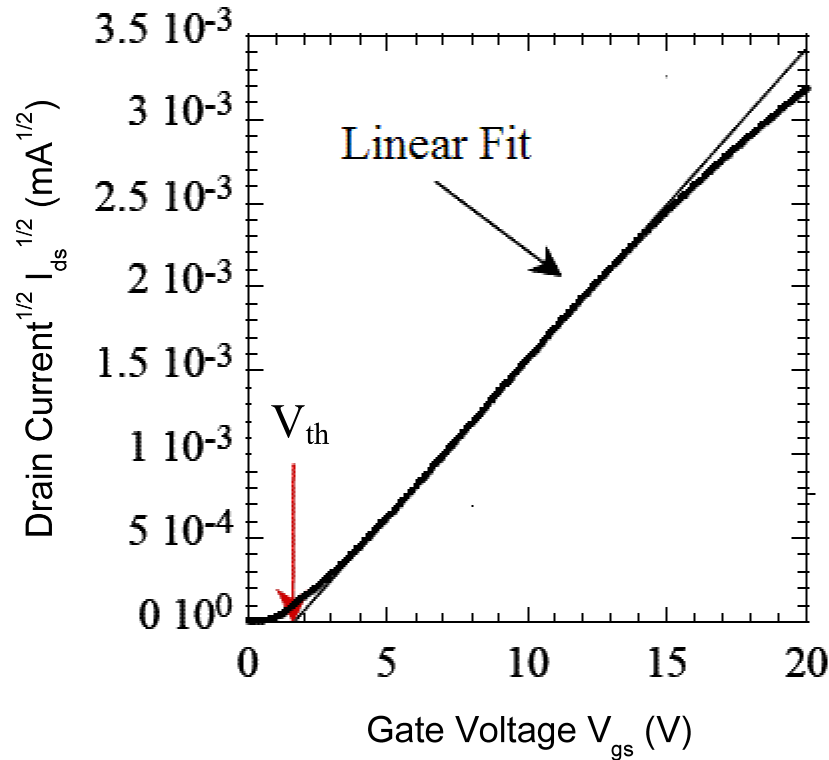


Figure 2.6 Linear fit on square root of transfer characteristics of a TFT, adopted from [27]

The subthreshold slope and on/off ratio can be obtained from log scale plot of transfer characteristics. The subthreshold slope which can be easily extracted by applying an apparent linear fit in subthreshold regime is a measure of the increase in gate voltage needed to switch the TFT from off-state regime to above-threshold regime. By taking the inverse of the apparent linear fit, the subthreshold slope can be determined with units V/decade since the subthreshold slope is defined by

$$S = \frac{dV_{gs}}{d(\log I_{ds})} = \ln 10 \frac{dV_{gs}}{d(\ln I_{ds})} \tag{2.11}$$

The smaller value corresponds to faster switching performance. The on/off ratio can be determined from the minimum/maximum current value of the transfer characteristics by taking maximum to minimum current ratio.

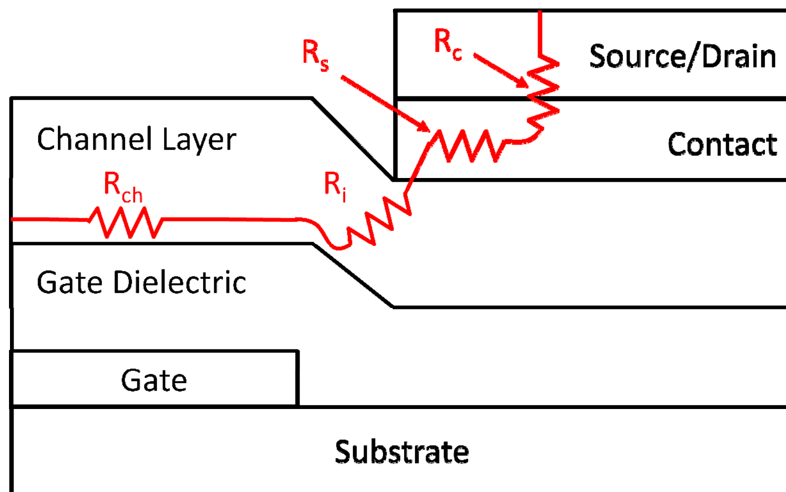
Finally, the transconductance can be obtained from the differentiation of transfer characteristics of experimental data since definition of the transconductance in saturation region is given by

$$g_m = \frac{dI_{ds}}{dV_{gs}} = \mu_{EF} C_{gate} \frac{W}{L} \left(V_{gs} - V_{th}\right) \tag{2.12}$$

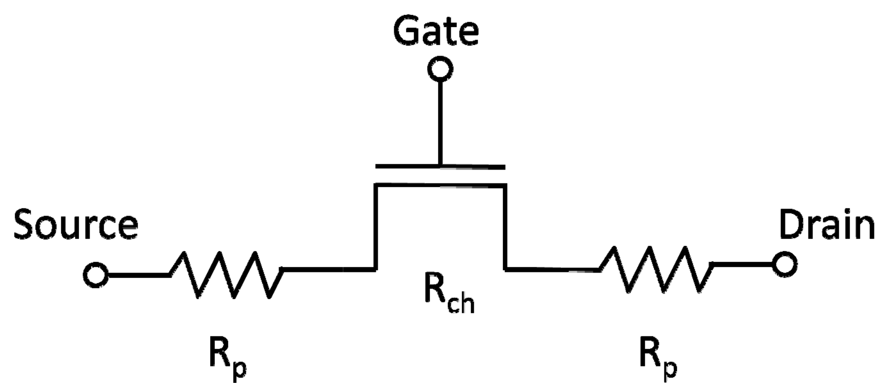
2.2.3 Parasitic Resistance

There are many factors, including channel length, channel layer thickness, and quality of source/drain contact layers, that have influence on TFT performances [28]. The effect of these factors is revealed by parasitic resistance in TFTs. For example, if the parasitic resistance is too large, ohmic contact cannot be achieved. It leads to the current crowding behavior which can be observed near the origin of the TFT output characteristics [29]. The parasitic resistance also affects on the transconductance degradation at high gate bias which limits the on-state performance of the TFTs [30].

Figure 2.7 (a) illustrates components of parasitic resistance that are reside in the bottom gate TFTs. The components include: contact resistance between n+ nc-Si:H source/drain contact layers and metal electrodes, series resistance of the contact layers, and series resistance of the nc-Si:H channel layer. In staggered structure, the series resistance component can be most significant part of the parasitic resistance since electrons must travel through an intrinsic nc-Si:H region on their way to/from the channel [31]. Figure 2.7 (b) shows equivalent circuit for TFT including parasitic resistance effect. Three resistance components, two parasitic resistances (R_p) and a channel resistance (R_{ch}) , are connected in series from source to drain. The channel resistance component is the resistance of accumulated electron conduction layer which is affected by gate/drain bias and defect state profile of channel layer.



(a)



(b)

Figure 2.7 (a) Parasitic components in staggered bottom gate nc-Si:H TFT and (b) equivalent circuit for parasitic resistance analysis

Chapter 3 Characterization and Fabrication

This chapter will demonstrate the experimental part of research. Silicon Nitride dielectric and n+ nc-Si:H contact layers will be characterized first, and fabrication of bottom gate nanocrystalline TFT will be described. Subsequently, the electrical characteristics of the fabricated TFT will be illustrated and discussed as well as performance factor extraction: threshold voltage, field effect mobility, subthreshold slope and on/off ratio. Along with description on sample preparation for material characterization, the test apparatus and methods will be described in detail. Finally, fabrication sequence for direct conversion X-ray detector array backplane and its mask design will be illustrated.

3.1 Material Characterization

3.1.1 Silicon Nitride Characterization

Fourier Transform Infrared (FTIR) spectroscopy, I-V and C-V measurements were performed to characterize our current silicon nitride. In preparation of the FTIR spectroscopy and C-V measurements, we deposited silicon nitride in multi chamber PECVD system which was manufactured by MVSystems Inc. For FTIR spectroscopy and C-V measurement, we prepared 3” lightly doped p-type crystalline silicon wafer as substrate while 3” heavily doped p-type crystalline silicon wafer was used for I-V measurement. The substrate wafers were cleaned by RCA1 cleaning process followed by HF dip process to remove native oxide prior to the PECVD process. The PECVD process was performed in 260-300 ^{o}C, 400 mTorr chamber pressure and 2 W RF power. We used SiH_4 and Ammonia (NH_3) for silicon nitride deposition using 20 sccm flow rate for SiH_4 and 100 sccm for NH_3. The deposition time was 1800 seconds to prepare 300-nm-thick sample. For I-V and C-V measurements, we deposited aluminum on top of the silicon nitride sample to form MIS structure using shadow mask depicted in Figure 3.1.

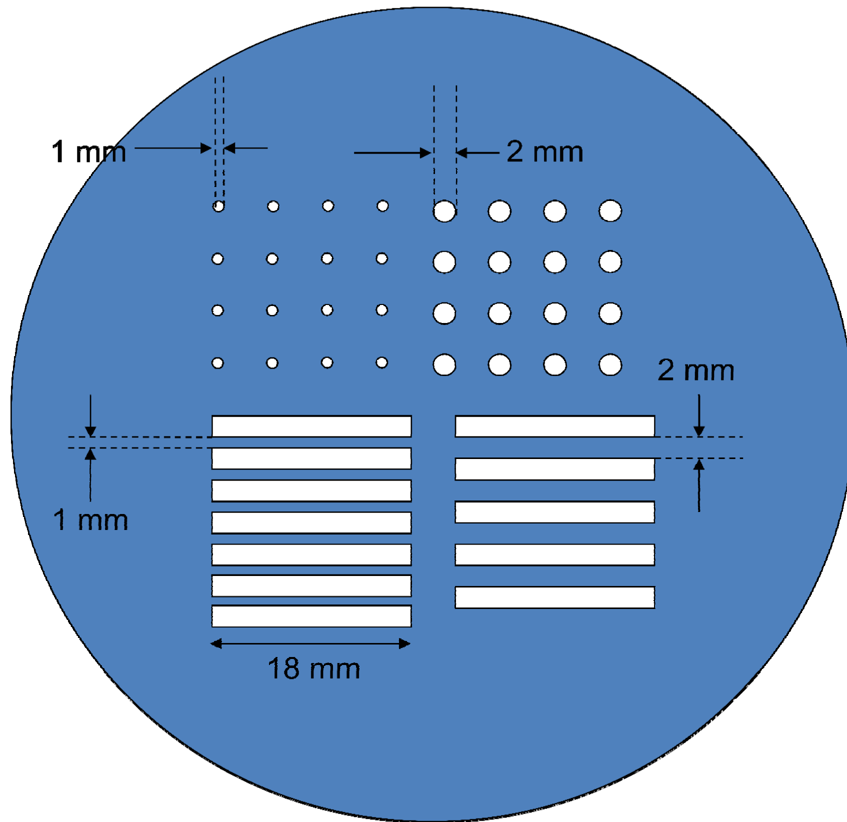


Figure 3.1 Top view of the shadow mask schematic used for I-V and C-V Characterization

The FTIR spectra are obtained using FTIR-8400S spectrophotometer from Shimadzu Corporation. A bare intrinsic crystalline silicon wafer was measured first to provide background spectra information for silicon nitride absorption spectra data processing prior to 300-nm-thick silicon nitride sample measurement. The FTIR spectra of silicon nitride sample are displayed in Figure 3.2.

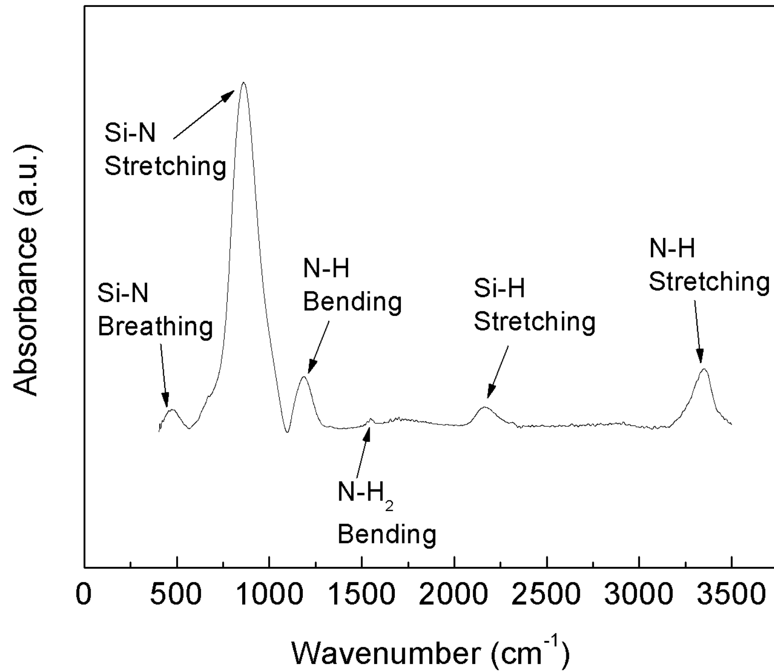


Figure 3.2 FTIR spectra of silicon nitride sample

The absorption peaks in Figure 3.2, are due to Si–N Breathing, Si–N Stretching, N–H Bending, N–H_2 Bending, Si–H Stretching, and N–H Stretching modes, which are located at 430–490, 880–900, 1180–1190, 1550, 2150–2180, and 3340 cm^{-1}, respectively [33, 17]. The relatively higher peak due to N–H bonds indicates that silicon nitride is nitrogen rich which is desirable for gate dielectric for thin film transistor application [36]. In high temperature LPCVD, the Si–H Stretching mode is observed around 840-850 cm^{-1}. However, in our measurement, it was observed in 880–900 cm^{-1} range. The shift of Si–H Stretching mode to higher wavenumbers indicates that the silicon nitride sample is hydrogen rich. The sharp and symmetrical shape of Si–H Stretching mode represents both nitrogen and hydrogen rich situation which is common in PECVD silicon nitride deposited using ammonia gas in deposition process [17].

The I-V characteristics of silicon nitride sample are obtained by using Keithley 4200 Semiconductor characterization system. To observe breakdown voltage, the metal pattern on

the sample which is formed by shadow mask deposition was biased up to 200 V while the substrate chuck bias remained ground. The compliance of current was set to 10^{-3} A. The I-V characteristic obtained is illustrated in Figure 3.3.

Relatively low leakage current level in low bias range (< 3 MV/cm) [17], indicates that the sample silicon nitride is nitrogen rich. The sharp increase of current around 4.3 MV/cm range indicates the breakdown of silicon nitride dielectric. Usually, high quality passivation silicon nitride has > 7 MV/cm breakdown voltage. However, since the TFT bias range we used in characterization was around 30 V(less than 2 MV/cm), the relatively low breakdown voltage does not bring serious TFT operation range constrains.

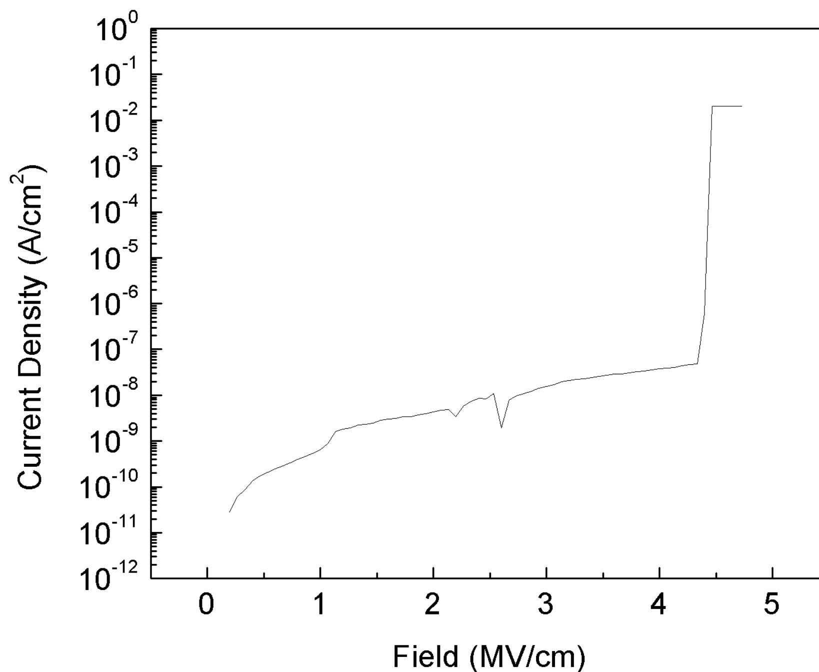


Figure 3.3 I-V characteristics of silicon nitride sample

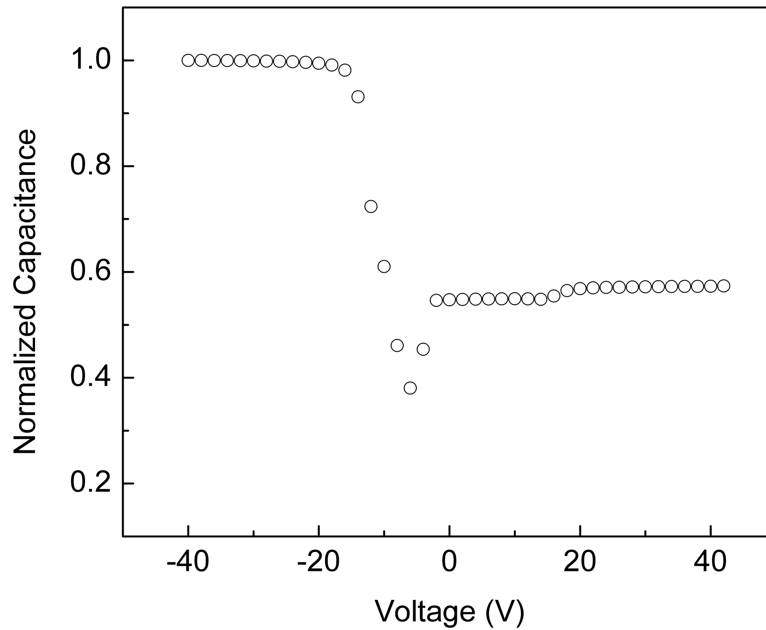


Figure 3.4 C-V Characteristics of silicon nitride sample

The C-V characteristics (illustrated in Figure 3.4) are obtained using Agilent 4184A LCD Meter. The voltage applied on the silicon nitride sample was -40 to 40 V range at 1 MHz frequency of 50 mV AC signal while the chuck bias remained ground. In -40 to -10 V range, evacuation of accumulated charge at the silicon nitride/crystalline silicon surface can be observed. From -10 V range to 40 V, a slight increase of capacitance can be observed at -10 to 0 V range and fast state charge presence from 0 to 40 V range. The increase of capacitance in -10 to 10 V range can be originated from fixed inversion layer [38]. Since the top electrode (dot pattern in the shadow mask) is relatively smaller than bottom electrode (3” silicon wafer substrate), the AC current will be spread out from the gate electrode to outer region due to lower resistance of inversion layer. This spread of AC current establishes low pass filter network which increases the measured capacitance.

Finally, relative permittivity of silicon nitride was obtained as shown in Figure 3.5. Capacitance measurement data from five randomly selected dots were collected and averaged to obtain permittivity of 6.15 which is relatively low compared to typical silicon nitride value;

6.3 ~ 7. This low relative permittivity also indicates nitrogen rich composition of current silicon nitride sample.

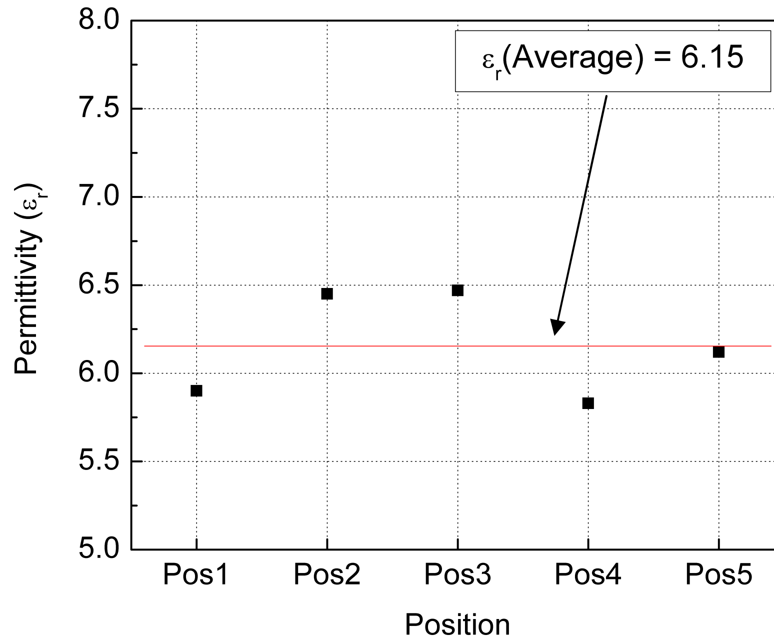


Figure 3.5 Relative permittivity obtained from 5 randomly picked points resulting average permittivity as 6.15

3.1.2 n+ Nanocrystalline Silicon Characterization

The n+ nanocrystalline silicon (n+ nc-Si) is characterized by Raman spectra and Dark conductivity. The samples are prepared on RCA1 processed Corning 1737 3" glass wafers using multi chamber PECVD system manufactured by MVSystem Inc. The PECVD process was performed in 260-300 ^{o}C, 1800 mTorr chamber pressure and 2 W RF power. We used Phosphine (PH_3) gas to provide dopants on nanocrystalline silicon film. The gas flow rate was 1 sccm, 1 sccm, and 250 sccm for PH_3, SiH_4 and H_2, respectively. The deposition time was 3600 seconds to prepare 85-nm-thick sample. For Dark conductivity measurements, we deposited 100-nm-thick Aluminum using the shadow mask depicted in Figure 3.1.

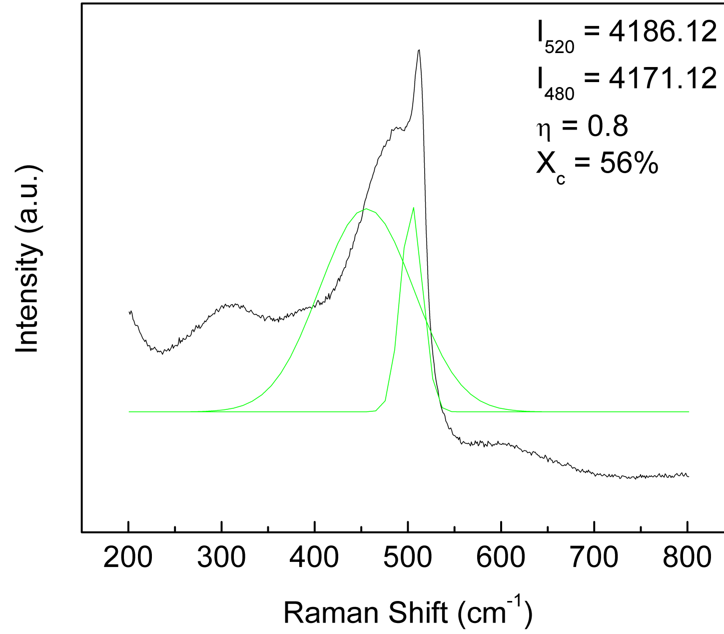


Figure 3.6 Raman spectra of n+ nanocrystalline silicon Film

The film crystallinity X_C was extracted from Raman spectra measured in the backscattering geometry using a Renishaw micro-Raman 1000 spectrometer with a 633 nm He-Ne laser source. The incident beam power was kept below 50 mW to prevent the crystallization of the nc-Si:H films. The crystallinity was deduced from the integrated Raman intensity ratio,

$$X_C = \frac{I_{520}}{I_{520} + \eta I_{480}} \tag{3.1}$$

where I_{520} and I_{480} are the deconvoluted intensities of the Raman spectra in Gaussian approximated crystalline silicon transverse optical (TO) (~520 cm^{-1}) and amorphous silicon TO (~480 cm^{-1}) peaks, respectively, and η is the ratio of the back scattering cross-sections, being set to be 0.8 here [34]. The Raman spectra of 56% crystallinity n+ nanocrystalline silicon sample is illustrated in Figure 3.6.

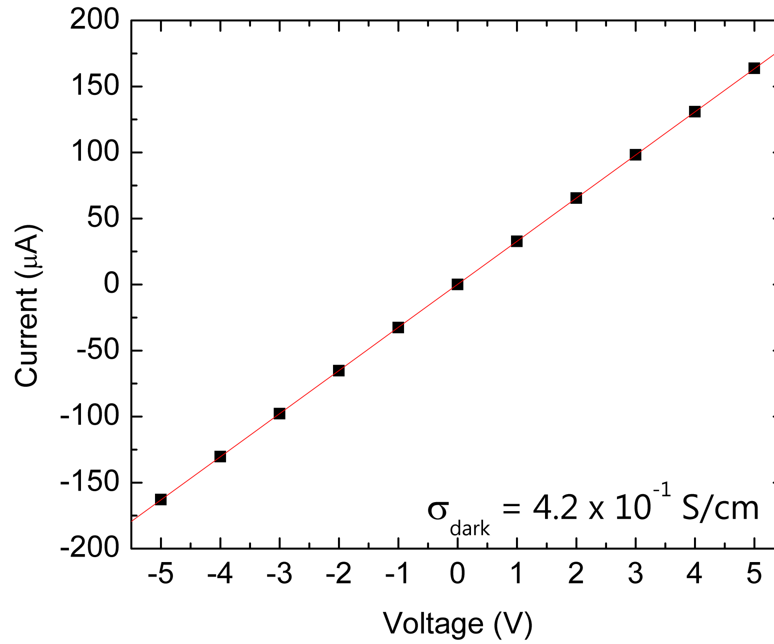


Figure 3.7 Dark conductivity measurement

The dark conductivity (σ_{dark}) was measured using the stripe patterns in the shadow mask pattern. The measurement was performed under dark condition using Keithley 4200 Semiconductor Characterization System. The voltage bias between two metal stripes was ranged from -5 to 5 V while measuring current between two metal stripes. To extract dark conductivity, simple resistance definition was used.

$$R_{dark} = \frac{L_{S-S}}{\sigma_{dark} W_S t_{n+}} \tag{3.2}$$

The L_{S-S}, W_S, and t_{n+} represent the spacing between two stripes in the shadow mask pattern, width of the stripe pattern and the thickness of n+ nanocrystalline silicon film, respectively. Applying Equation (3.2), the dark conductivity was observed as 0.42 S/cm.

3.2 Fabrication of Bottom Gate Staggered TFTs

A 5 mask mask set is used for bottom gate TFT sample fabrication. The mask set includes 50 um gate length and 300 um gate width design with several process monitoring patterns. The bottom gate process requires two metal sputtering processes, two PECVD depositions, and five lithographic processes. Each step in the fabrication will be described.

3.2.1 Substrate Preparation

Corning 1737 3” glass wafers are prepared for fabrication process with RCA1 cleaning process.

3.2.2 Gate Metal Deposition

The gate metal is the first layer to be deposited. In this process, molybdenum (Mo) was used and it was deposited using the Three Target Sputtering System which was manufactured by MV Systems Inc. Deposition temperature was kept at room temperature while using AC RF power as 300 W, argon (Ar) pressure of 5.6 mTorr, and deposition time as 1800 second with 200 nm per hour deposition rate.

3.2.3 Gate Metal Patterning

This is the first lithography step (mask 1) to define the TFT’s gate. Mo was wet-etched using a Phosphoric Acetic Nitric acid (PAN) solution, and after etching, the wafer looks as shown in the Figure 3.8. The etching process was monitored by bare eye and microscope during wet etch process and the etch rate was about 80 nm per minutes.

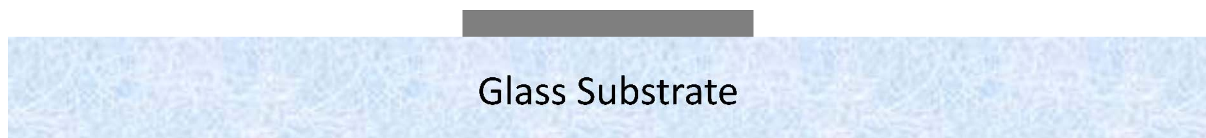


Figure 3.8 Mask 1 lithography which defines the TFT gate

3.2.4 Depostion of Tri-Layer

A tri layer of silicon nitride/BiLayer/silicon nitride was grown by PECVD using the Multi-Chamber PECVD System manufactured by MVSystems Inc. The whole process was

performed under 260-300 ^{o}C. The first silicon nitride layer was deposited by SiH_4/NH_3 dilution ratio of 1/20 under 2 W RF power setup with 400 mTorr chamber pressure. To yield 300 nm thickness, the deposition time was set to 1800 seconds due to 10 nm per minute growth rate.

Before the deposition of the Bilayer performed, we employed a plasma treatment step to improve channel interface [35]. Hydrogen plasma was used under 2 W RF power and 900 mTorr chamber pressure. The hydrogen flow rate was 200 sccm for the five-minute plasma treatment process.

The Bilayer channel was deposited immediately after the plasma treatment. It consisted of 15 nm nanocrystalline silicon and 35 nm amorphous silicon layer. The SiH_4/H_2 dilution ratio for nanocrystalline silicon layer was 1/100 with 2 W RF power under 900 mTorr chamber pressure. The process took 15 minutes to achieve 15 nm-thick film. For amorphous silicon layer, the SiH_4/H_2 dilution ratio was 1/10 with the same RF power as the nanocrystalline silicon process under 400 mTorr chamber pressure. The deposition took 10 minutes to achieve 35 nm amorphous silicon layer. The passivation silicon nitride layer was deposited right after the BiLayer deposition. The wafer schematic of the Tri-Layer deposition is described in Figure 3.9.

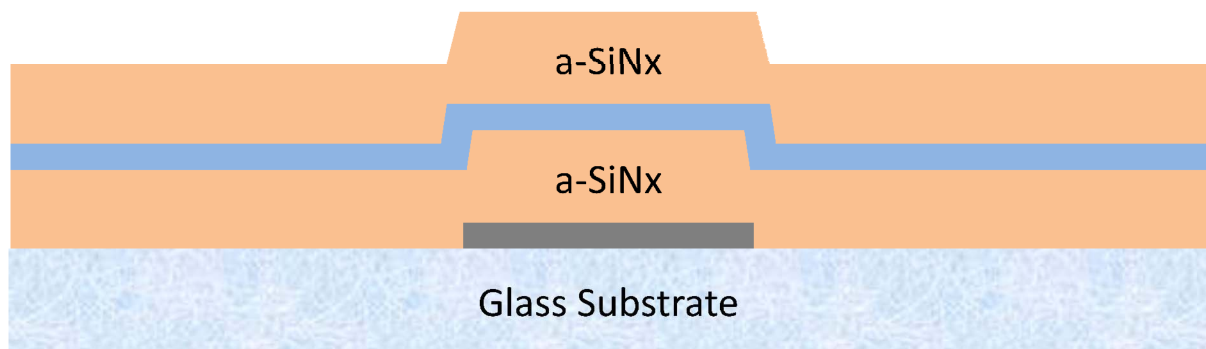


Figure 3.9 The deposition of Tri-Layer

3.2.5 Patterning of Source/Drain Openings

In this lithography process (Mask 2), source and drain contacts are opened with BHF solution in the top silicon nitride passivation layer, which defines the effective channel length as well

as gate overlap. The wet etching process took 75-90 seconds to completely etch the 300 nm silicon nitride layer. Figure 3.10 shows the sample after patterning process is finished.

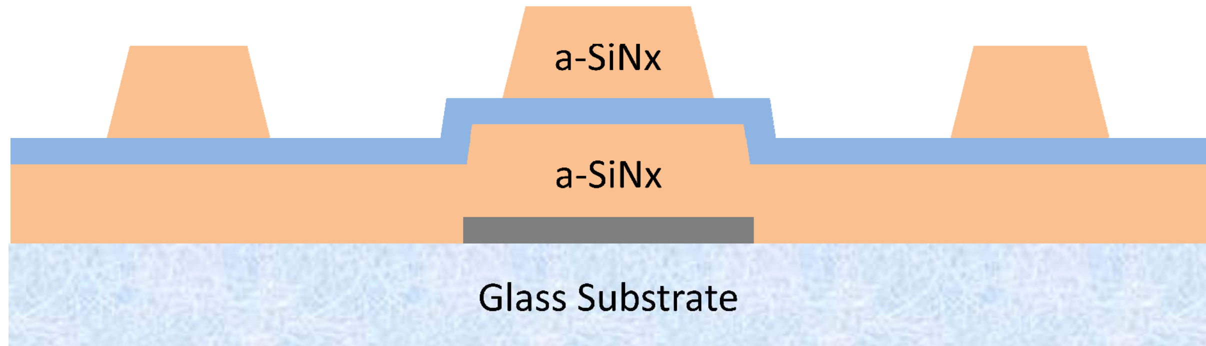


Figure 3.10 Patterning of Source/Drain Openings

3.2.6 Deposition of n+ nanocrystalline silicon and Protection silicon nitride layer

n+ nanocrystalline silicon layer and Protection silicon nitride layer are deposited for source and drain contacts using PECVD process. The Protection silicon nitride layer is needed as a mask for the etching of n+ nanocrystalline silicon by potassium hydroxide (KOH). Photoresist cannot be used as an etching mask when etching silicon since KOH also damage the Photoresist. The thickness of n+ nanocrystalline silicon was 60 nm and the silicon nitride was again 300 nm. We used Phosphine (PH_3) as the dopant for n+ nanocrystalline silicon layer with 99.6% Hydrogen dilution. The n+ nanocrystalline silicon deposition performed using 2 W RF power under 1900 mTorr chamber pressure. The deposition time was 45 minutes for 60 nm n+ nanocrystalline silicon film.

3.2.7 Defining n+ nanocrystalline silicon Source/Drain Regions

Third lithography step (Mask 3) is now performed to define the source and drain regions. Part of uppermost silcon nitride was etched using a BHF wet etch and the resulting device is shown in Figure 3.11. The leftover silicon nitride will serve as the mask for Si layer etching.

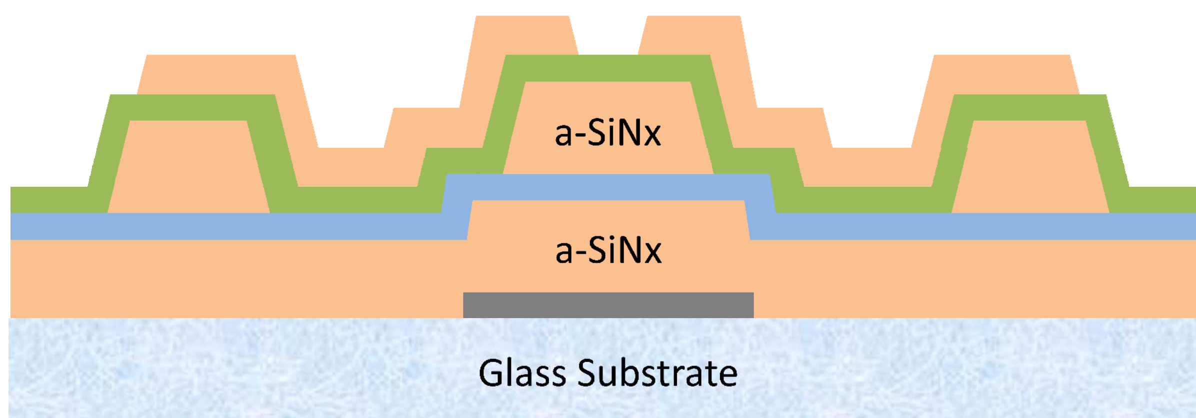


Figure 3.11 Defining silicon nitride mask by wet etching

3.2.8 Etching of n+ nanocrystalline silicon and BiLayer Channel

To etch n+ nanocrystalline silicon and BiLayer, KOH is used. This etching step defines TFT islands (isolate the BiLayer channel regionis). Since the wet etching process is an isotropic process, n+ nanocrystalline silicon will be etched laterally while 50 nm BiLayer is being etched. However, the thickness of films has much less dimensions than lateral dimensions (a few tens of µm) so this is not a problem. The resulting device is depectied in Figure 3.12.

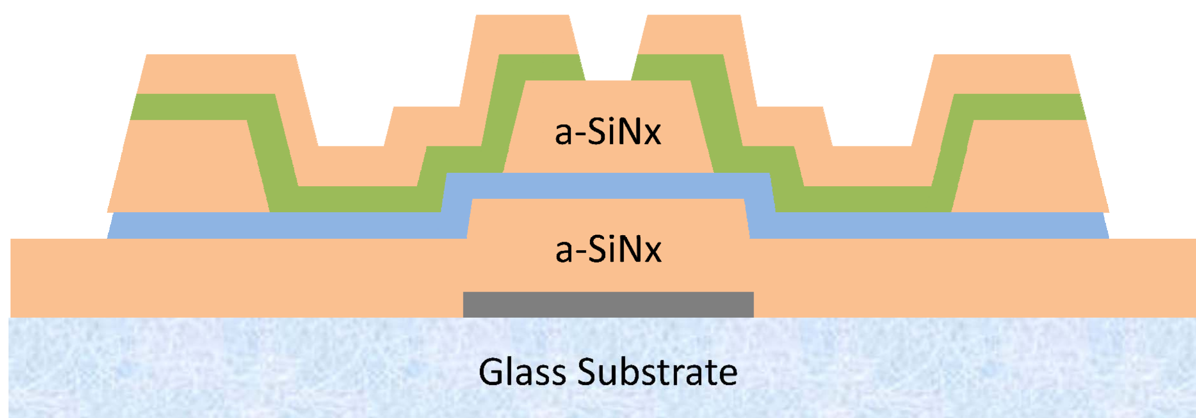


Figure 3.12 Etching step to remove n+ nc-Si:H and BiLayer to define island

3.2.9 Etching of the Protection silicon nitride to open Gate, Source, and Drain Vias

After patterning using mask 4, the silicon nitride was etched with BHF to open gate contacts and the drain and source contacts. The resulting device is described in Figure 3.13.

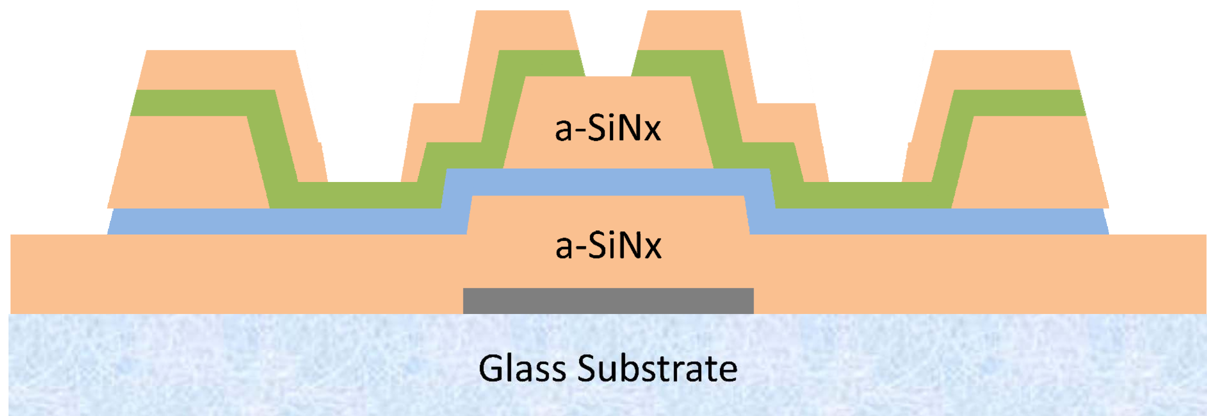


Figure 3.13 Defining opening for gate, source, and drain contacts

3.2.10 Molybdenum Deposition

A few seconds of HF dip was performed before Molybdenum deposition to remove oxidized silicon layer on the n+ nanocrystalline silicon, which was formed during previous process steps, to improve contact with metal contacts. 100-nm-thick molybdenum was deposited to form actual metal contacts for TFT Gate, source and drain.

3.2.11 Patterning of Final Molybdenum Metallization Layer

In this step (mask 5), the metal contacts are patterned. Molybdenum was etched using PAN solution in room temperature. The final device is illustrated in Figure 3.14.

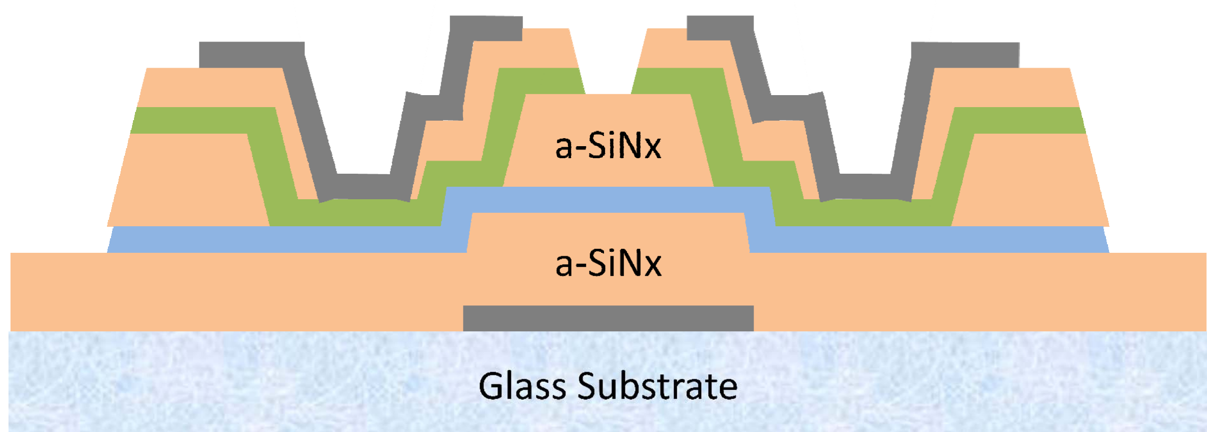


Figure 3.14 Finalized Bottom Gate TFT after patterning mask 5

3.3 TFT Characterization

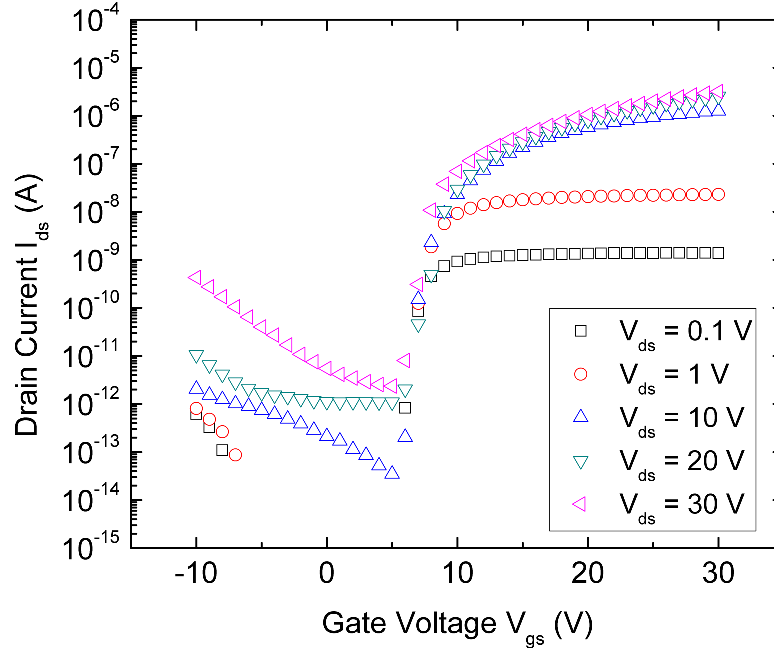


Figure 3.15 Transfer Characteristics of fabricated TFTs

The fabricated TFT samples were characterized electrically by measuring transfer and output characteristics using Keithley 4200 Semiconductor Characterization System. To measure transfer characteristics, the voltage sweep was applied from -10 to 30 V for gate bias (V_{gs}) while collecting current at drain electrode. The voltage sweep was performed five times with different drain bias (V_{ds}) conditions: 0.1, 1, 10, 20, and 30 V. The transfer characteristics of fabricated TFTs are depicted in Figure 3.15. The output characteristics are obtained by biasing drain voltage from 0 to 30 V while measuring drain current for different gate bias conditions: 10, 15, 20, 25, and 30 V. The output characteristics are illustrated in Figure 3.16.

In the transfer characteristics (Figure 3.15), we can observe that the drain current in the above threshold region does not increase noticeably by increasing drain bias from 10 to 30 V while the drain leakage current under 5 V gate bias keeps increasing. In output characteristics (Figure 3.16), the saturation current does not increase following square root model when the gate bias is higher than 20 V. It can be noted that the channel is affected by lateral electric

field induced by drain bias. Charge sheet approximation which assumes the channel is not affected by lateral electric field is used in the derivation of square root model. However, in short channel field effect transistors, the lateral electric field causes the channel to be spread from bulk/dielectric interface to bulk region resulting in degradation of field effect mobility [37].

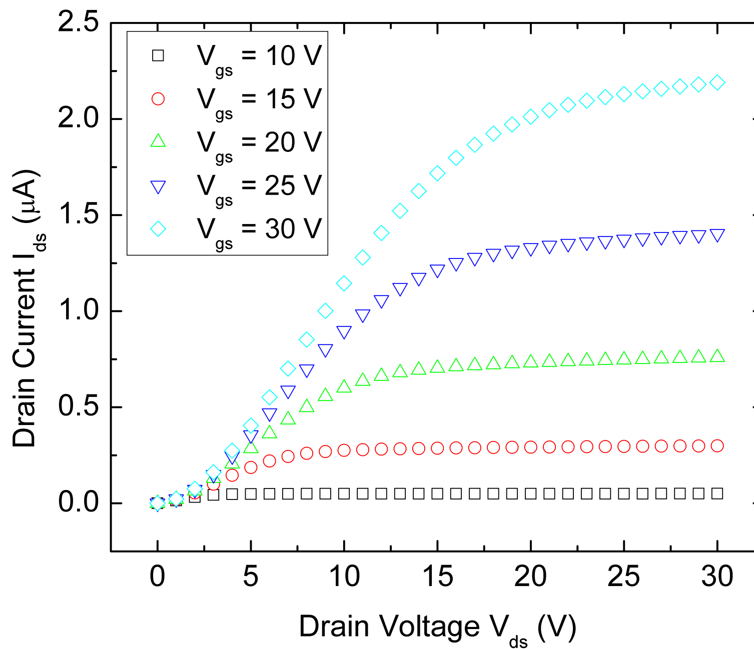


Figure 3.16 Output Characteristics of fabricated TFTs

Again, in the output characteristics, the drain current at less than 5 V drain bias does not increase linearly as described in square root model. This can be explained by current crowding effect which is caused by poor contact between contact layer and metal. The current crowding effect also contributes to parasitic resistance increase which eventually causes the transconductance degradation. The transconductance degradation is shown in Figure 3.17. The transconductance was extracted from the transfer characteristics by taking differentiation of drain current at drain voltage bias 10 V. The transconductance decreases when the gate bias is larger than 20 V where it must remain constant according to the square root model.

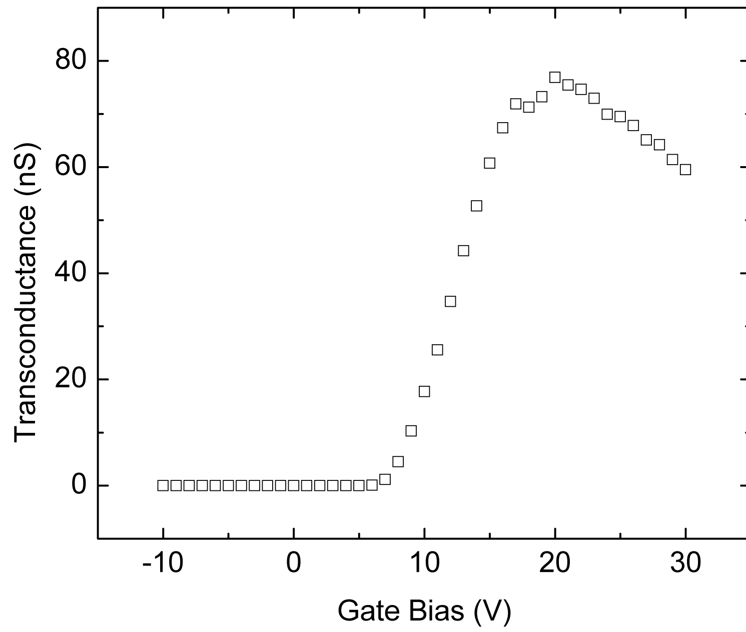


Figure 3.17 Transconductance of V_{ds} = 10 V condition

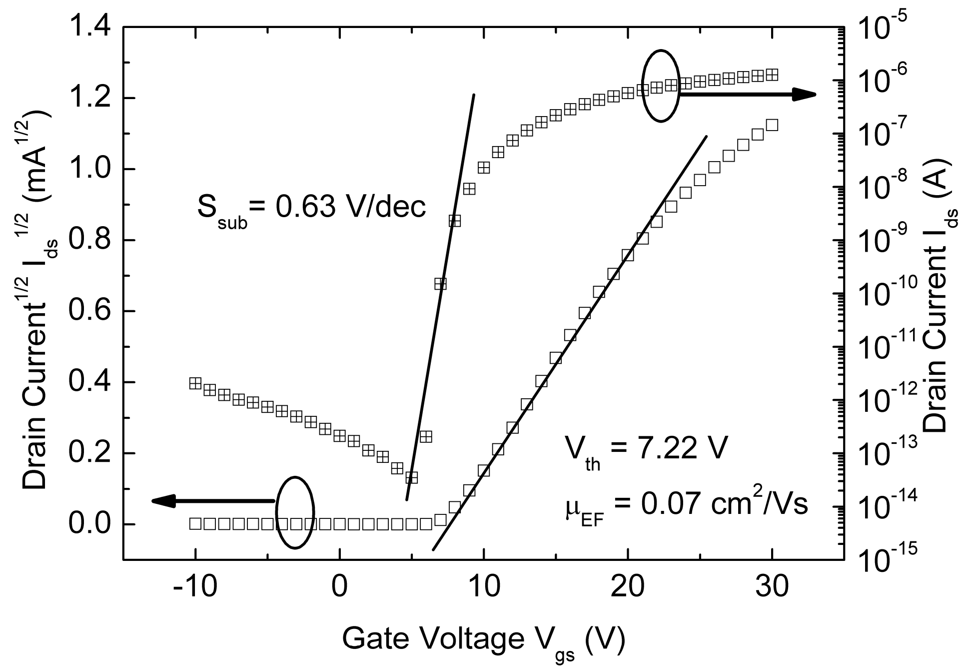


Figure 3.18 Performance factors extraction scheme

The TFT performance factors extracted from transfer characteristics at drain bias 10 V is illustrated in Figure 3.18. The threshold voltage and field effect mobility were extracted from linear plot by performing linear fit on square root drain current dependence on the gate bias range 6 V to 20 V. The subthreshold slope was extracted from a linear fit on log scale part. The TFT demonstrated a threshold voltage of 7.22 V, a field effect mobility of 0.07 $cm^2/V\cdot s$, and subthreshold slope of 0.63 V/decade. The on/off ratio was calculated by taking the minimum point at 5 V in the log scale part, resulting in the value of 10^6.

3.4 Implementation of Direct Conversion X-ray Detector Array

To implement direct conversion X-ray detector array using current TFT fabrication process, we need two additional mask sets for TFT passivation silicon nitride patterning and mushroom electrode formation. The mushroom electrode serves both TFT protection underneath from X-ray photons and as bottom contact for photodetector material. A charge storage capacitor implementation, however, does not require additional process steps but can be included within current TFT fabrication step. The bottom electrode pattern of a charge storage capacitor was included in Mask 1 while the top electrode part was realized in Mask 5. The entire fabrication sequence of Direct Conversion X-ray Detector Array Backplane is illustrated in Figure 3.19.

The TFT passivation silicon nitride was deposited using the multi chamber PECVD system manufactured by MVSystems Inc. with the gate dielectric silicon nitride process condition followed by a patterning process (Mask 6) to open contact hole for mushroom electrode. Subsequently, 300-nm-thick Aluminum was sputtered for mushroom electrode formation. The patterning process (Mask 7) was performed with PAN solution etching to finalize the backplane fabrication process. An optical micrograph of a pixel component in the completed array backplane is displayed in Figure 3.20.

The pixel was designed to fit our TFT dimension: 300/50 μm. The pixel area, mushroom electrode size, designed as 500 × 500 μm^2. The charge storage capacitor pattern was composed as four rectangular regions, each rectangle of 30 × 80 μm^2 area, to ease aligning process.

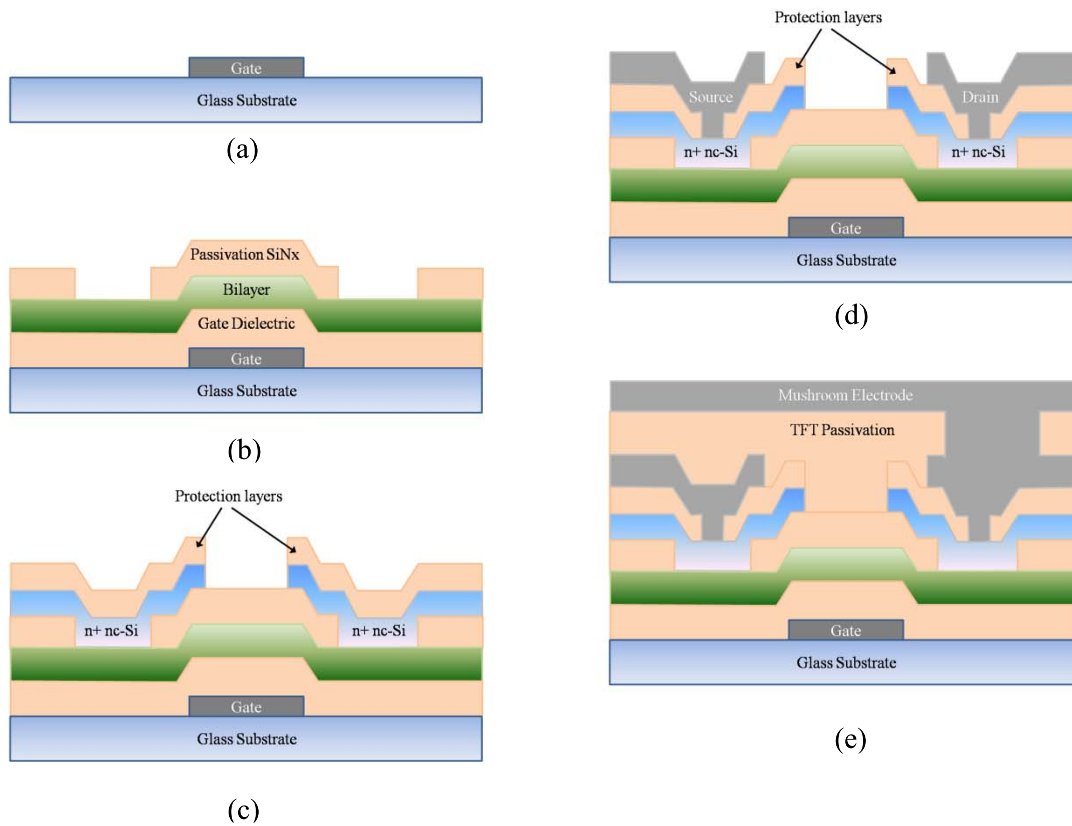


Figure 3.19 Fabrication sequence of the direct conversion X-ray detector array: (a) gate electrode formation, (b) tri-layer deposition followed by source/drain contact hole formation, (c) n+ nanocrystalline silicon contact formation, (d) source/drain electrode formation, and (e) TFT passivation followed by mushroom electrode formation.

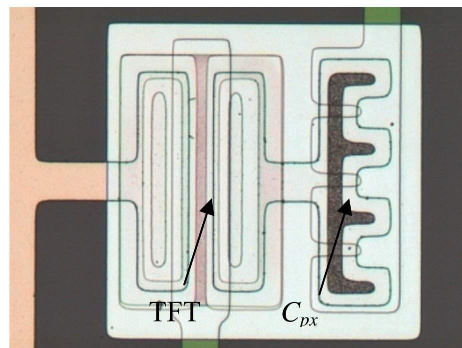


Figure 3.20 Optical micrograph of a pixel structure in the finalized backplane

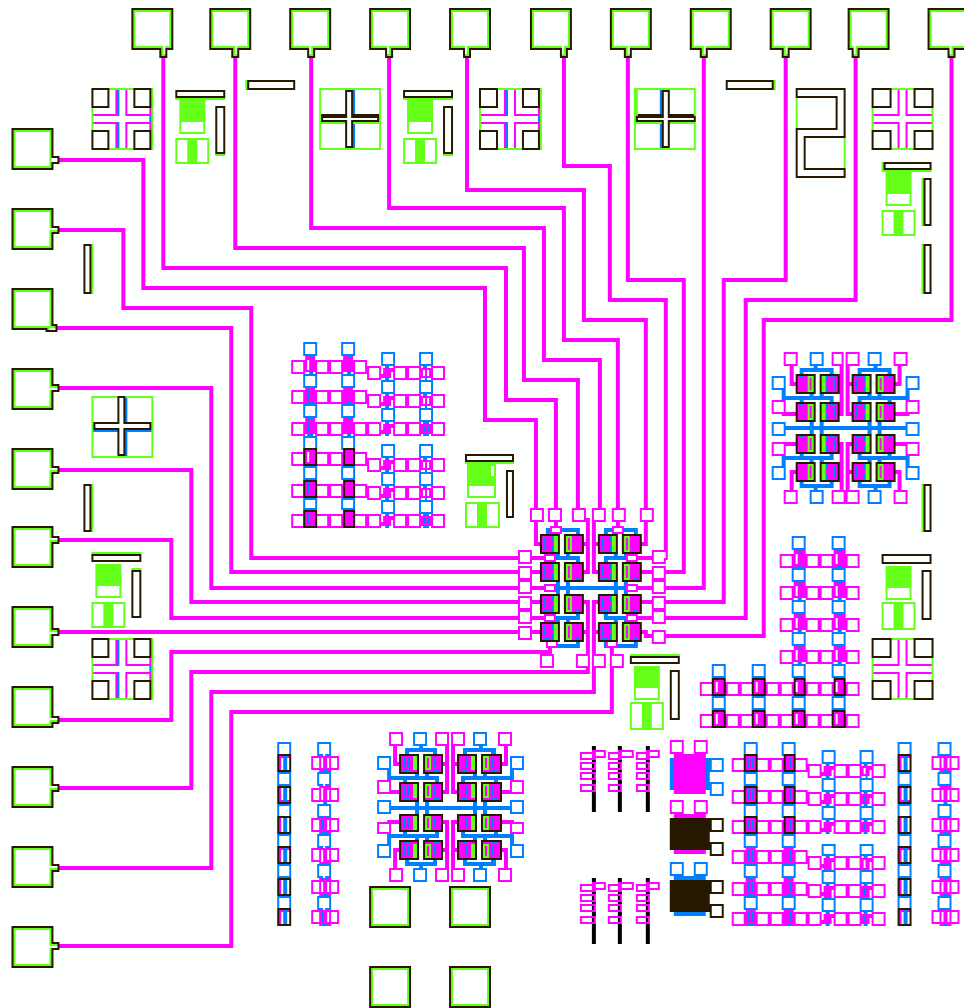


Figure 3.21Snapshot of Entire Array Backplane Design

The snapshot of the array backplane design is illustrated in Figure 3.21. The entire die area is 1” × 1” to fit constraints of the alignment system. We implemented four 2 by 2 array in the middle of the die while securing the array from pads which are located at top and left edge of the die by 1 cm. It was inevitable to place such large space (1 cm) since a photoconductor which should be deposited on top of the array is biased by a few kV for X-ray photon collection. The lines between the pads and the arrays have 50 μm of width and designed to avoid crossing between gate and source/drain connections. TFT samples and alignment marks are located between the lines and right/bottom side spaces.

Chapter 4
Numerical Analysis of Parasitic Resistance

In this chapter, analysis of parasitic resistance effect by numerical simulation method will be demonstrated. The simulation setup for current bottom gate nanocrystalline silicon TFT will be presented followed by results on various simulation conditions: parasitic resistance component, channel length and tail states in nc-Si:H channel layer. To analyze effects of parasitic resistance on these various conditions, we used series resistance network model which was presented in Figure 2.7 (b).

4.1 Simulation Scheme

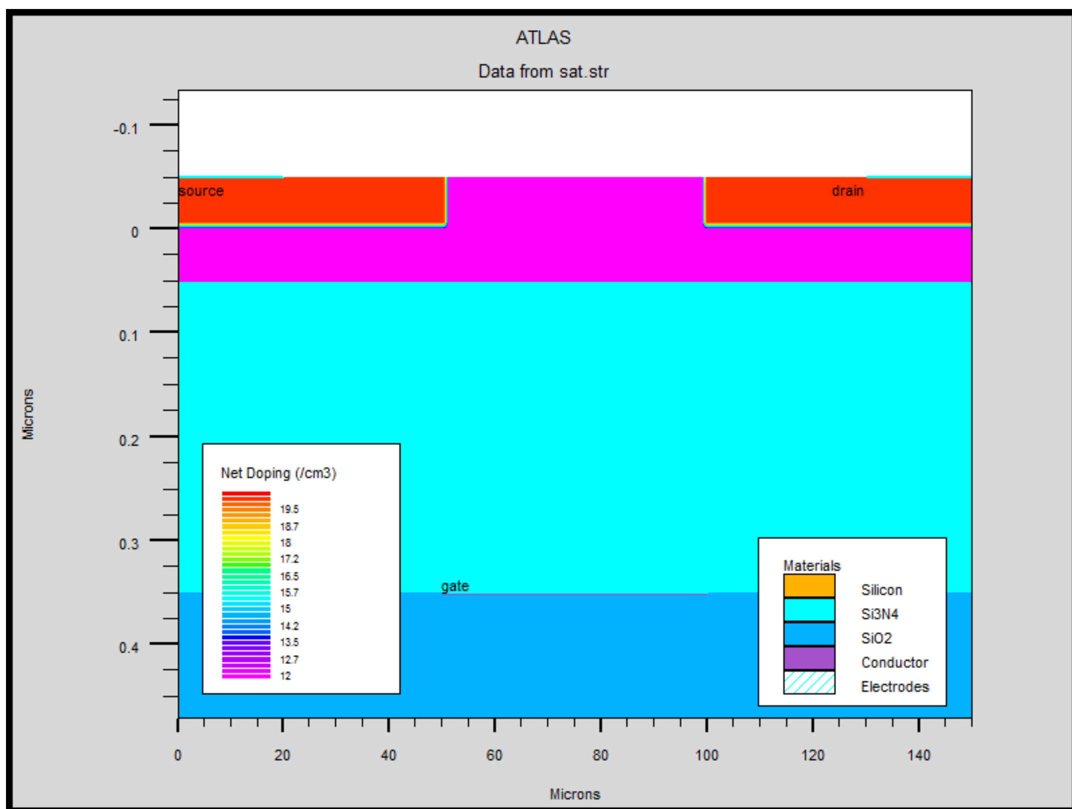
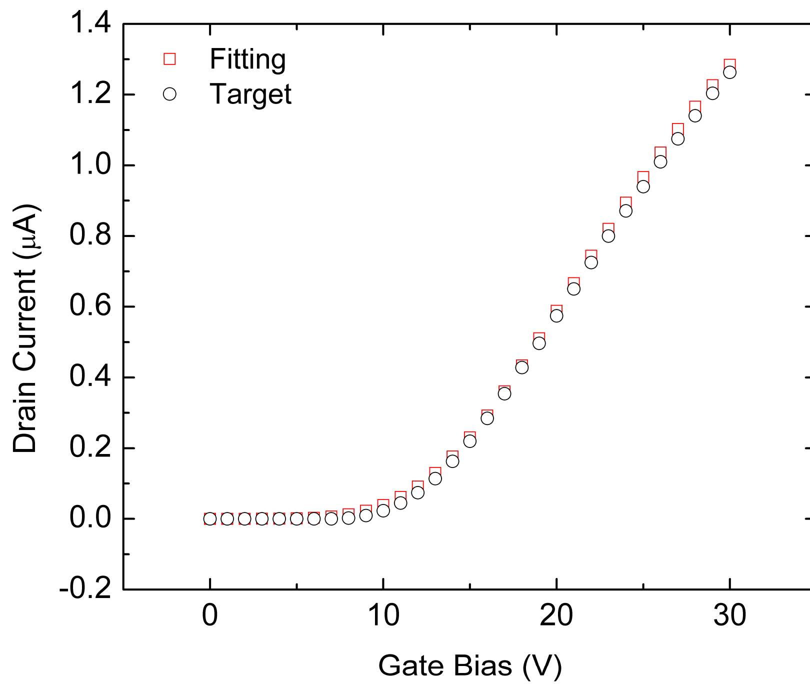


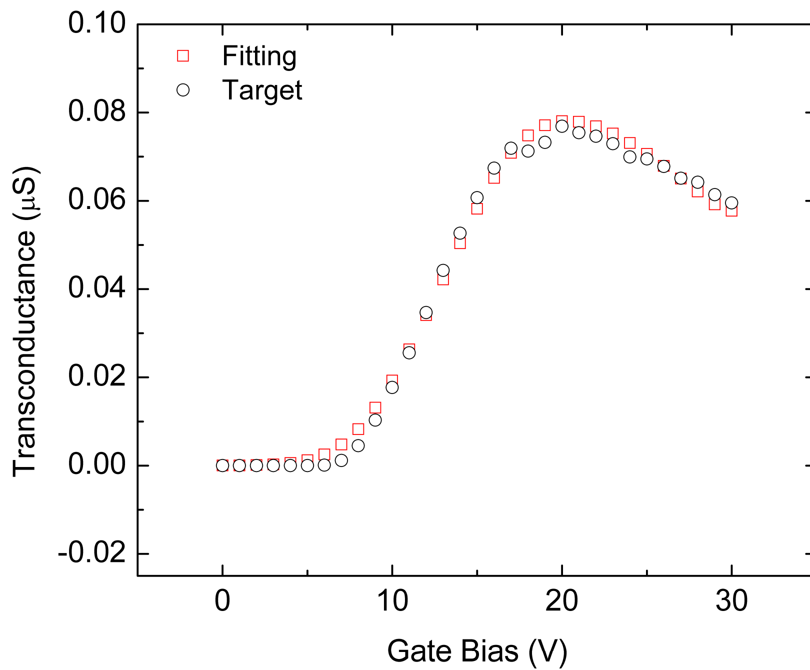
Figure 4.1 Bottom gate TFT mesh structure for simulation input

To perform numerical analysis on TFT, Atlas TCAD package from Silvaco Corporation was used. Prior to set up material parameters and simulation models, we defined a TFT mesh structure which reflects current bottom gate nanocrystalline TFT as close as possible. The TFT mesh structure for simulation is illustrated in Figure 4.1.

The source/drain region is difficult to implement perfectly with Atlas mesh structure. Therefore, instead of defining a new layer for source/drain contacts, we introduced a highly doped n+ regions and metal contacts on top of them. The doping concentration was set to 10^{20} /cm^{3} to achieve highest conduction while avoiding degenerate semiconductor implementation in simulation. The parasitic resistance components were not defined in the mesh structure directly since they can be implemented as lumped element in simulation input deck separately. The material parameters which were predefined in the simulation package had to be adjusted since the initial values were prepared for crystalline silicon. In addition, we employed DOS model which was provided by TFT module in the package to realize tail states and deep defect states in nanocrystalline silicon properly. The parameters for nanocrystalline silicon, defect states, and lumped parasitic resistance component were extracted by obtaining a best fit to experimental data as shown in Figure 4.2. The transfer characteristic and transconductance of 10 V drain bias condition was used as the experimental data. The input deck which includes all fitting parameters is provided in Appendix A.



(a)



(b)

Figure 4.2 (a) The best fit of transfer characteristics, and (b) transconductance

4.2 Simulation Results

4.2.1 Parasitic Resistance Variation

The impact of parasitic resistance is studied by changing the lumped parasitic element value. The fitting was established at 1.733 MΩ. The results including fitting condition (experimental data labeled as 'Target') are presented in Figure 4.3 and Figure 4.4. As shown here, the parasitic resistance effect diminishes at 100 kΩ, which is about one order of magnitude lower than original fitting value. Vice versa, as the parasitic resistance increases, transconductance degradation becomes more prominent than experimental case. Also, severe reduction of drain current is observed due to higher net resistance which is a series connection of parasitic resistance components and TFT channel resistance. When the parasitic resistance decreased to 1 kΩ range, transconductance increases rather than saturates. This behavior was already reported elsewhere [32].

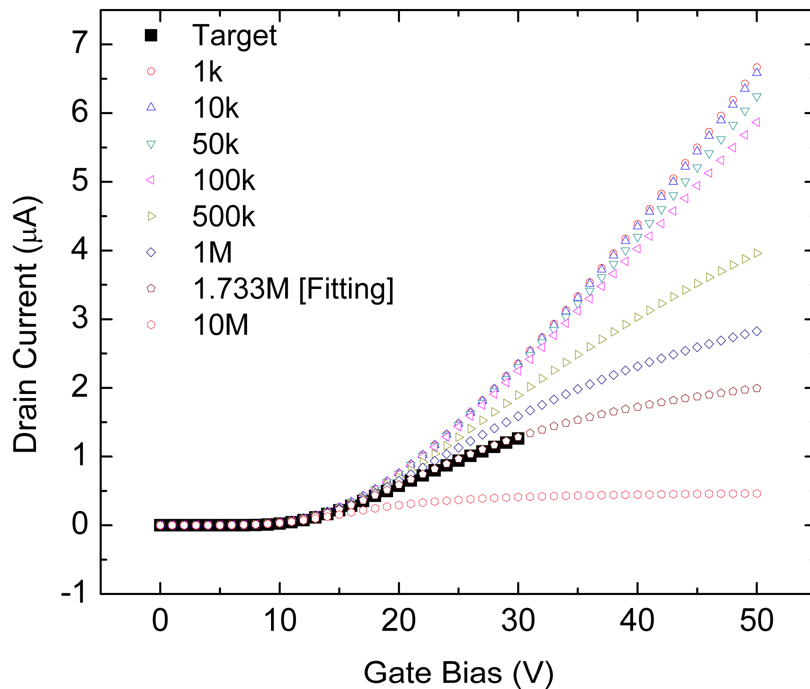


Figure 4.3 Simulated transfer characteristic of various parasitic resistances

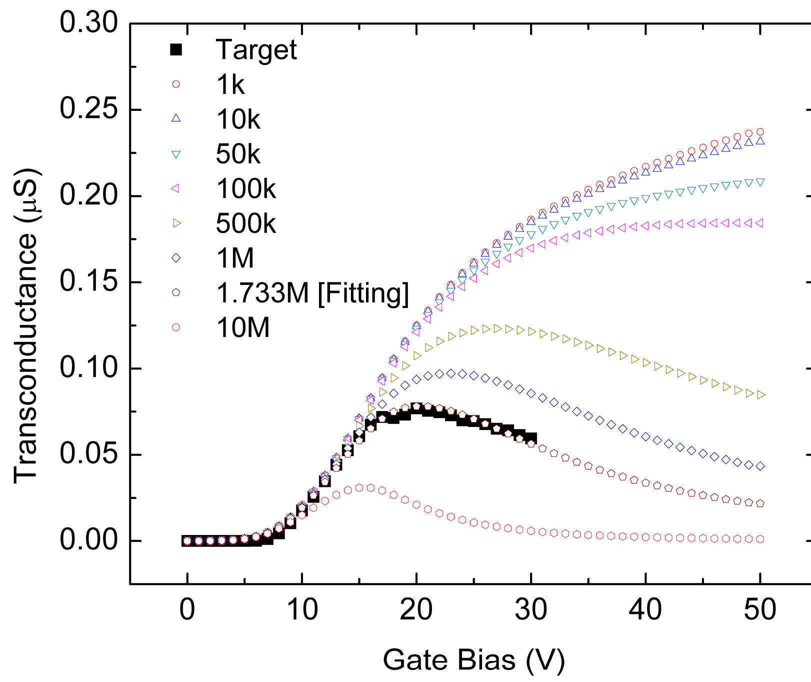


Figure 4.4 Simulated transconductance of various parasitic resistances

4.2.2 Channel Length Variation

The dependence of channel length is investigated for channel length varied from 10 to 200 um while keeping lumped parasitic resistance parameter and DOS parameters constant at initial fitting values. To implement various channel length, a TFT mesh structure for each gate length conditions are prepared. The resulting transfer characteristics and transconductance are illustrated in Figure 4.5, and Figure 4.6, respectively.

As the channel length decreases, the drain current level increases from 0.4 μA to 2 μA range due to reduction of total resistance of the series resistance network described in Figure 2.7 (b) while transconductance degradation becomes prominent. The maximum value of normalized transconductance decreases drastically from 6.8 to 1.4 μS/μm as the channel length decreases.

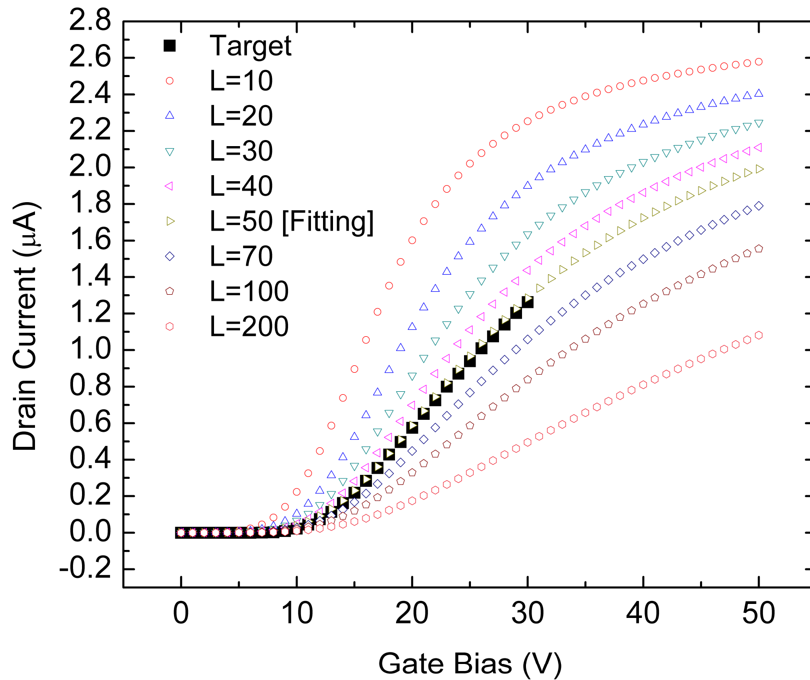


Figure 4.5 Simulated transfer characteristics of channel length

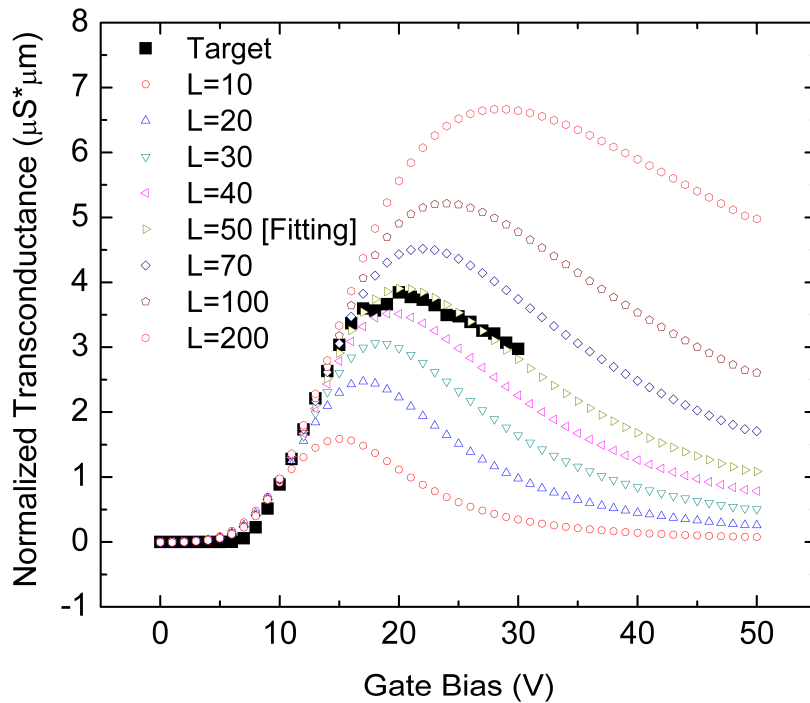
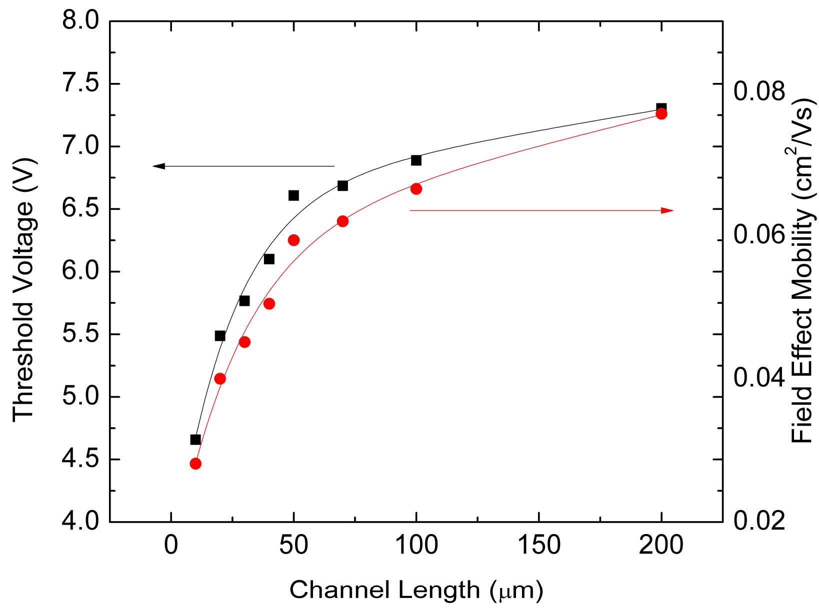
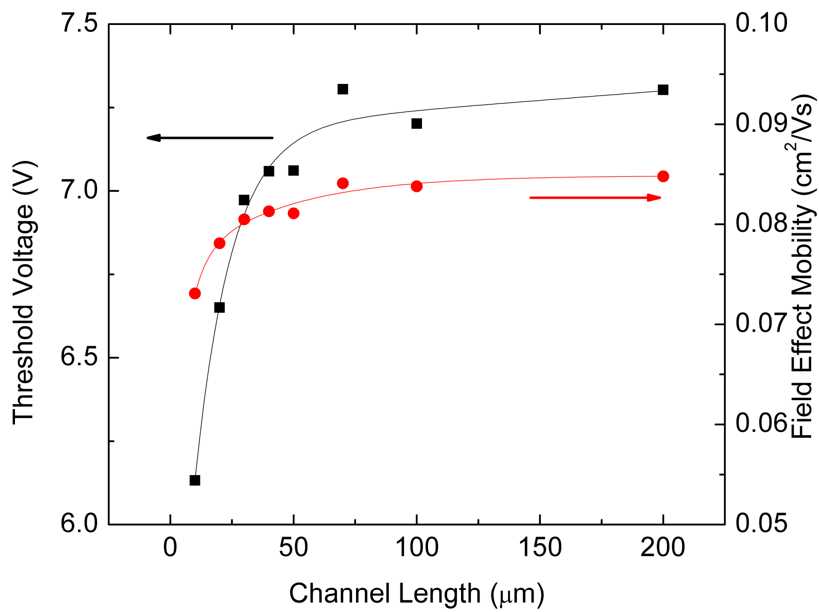


Figure 4.6 Simulated transconductance (normalized) of channel length

As a result, threshold voltage and field effect mobility, illustrated in Figure 4.7 (a), reduction by 36 % and 60 %, respectively. The observations above can be explained due to the increase of channel resistance weight in the series resistance network [28]. Figure 4.7 (b) shows the threshold voltage/field effect mobility relation to channel length at the parasitic resistance component was 1 kΩ. The decrease of threshold voltage and field effect mobility in the 1 kΩ case is 16 % and 11%, respectively.



(a)



(b)

Figure 4.7 Threshold voltage and field effect mobility extracted from simulation data: (a) Parasitic resistance value at 1.733 MΩ and (b) 1 kΩ

4.2.3 Tail State Variation Effect

Effects of material properties of nc-Si:H channel layer on parasitic resistance can also be investigated using simulation. As explained in Chapter 2, the DOS can be mathematically illustrated by sum of Gaussian deep states and Exponential tail states. The wider tail corresponding to higher tail characteristic decay energy indicates that the film has more amorphous states [32], thus resulting in higher resistance of the channel layer. Therefore, we investigated the influence of nc-Si:H properties on transconductance degradation by varying the characteristic decay energy. The simulated transfer characteristics and transconductance on various WTA are depicted in Figure 4.8 and Figure 4.9, respectively.

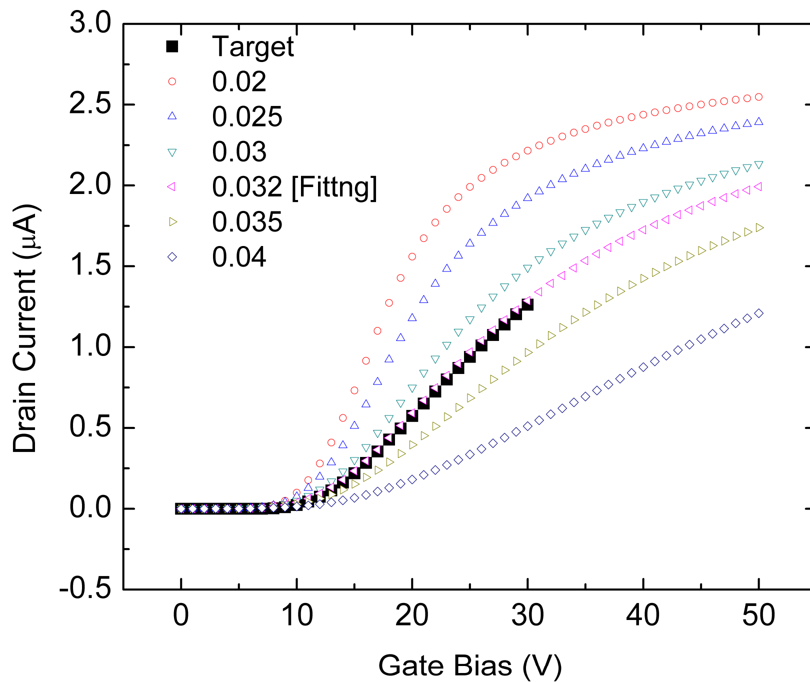


Figure 4.8 Simulated transfer characteristics at various WTA

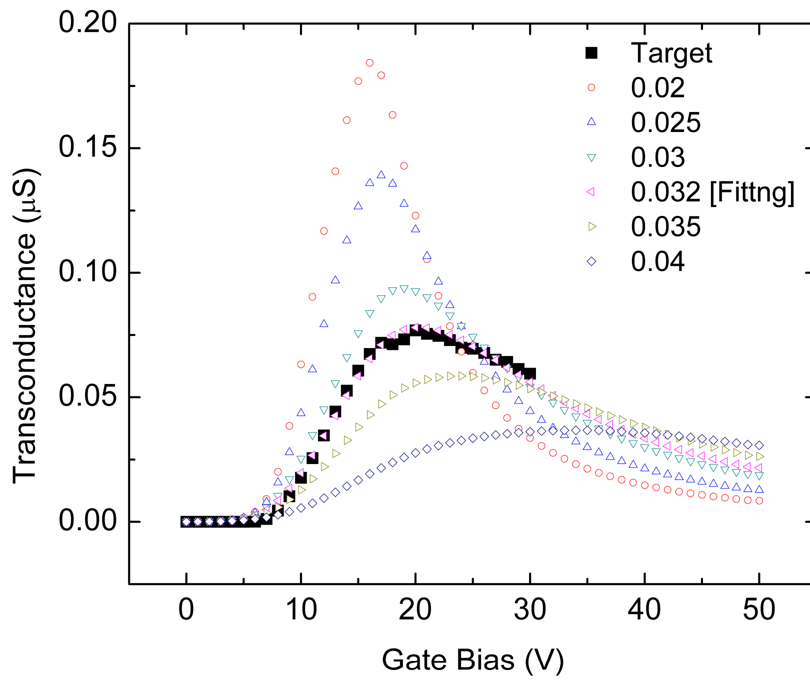


Figure 4.9 Simulated transconductance at various WTA

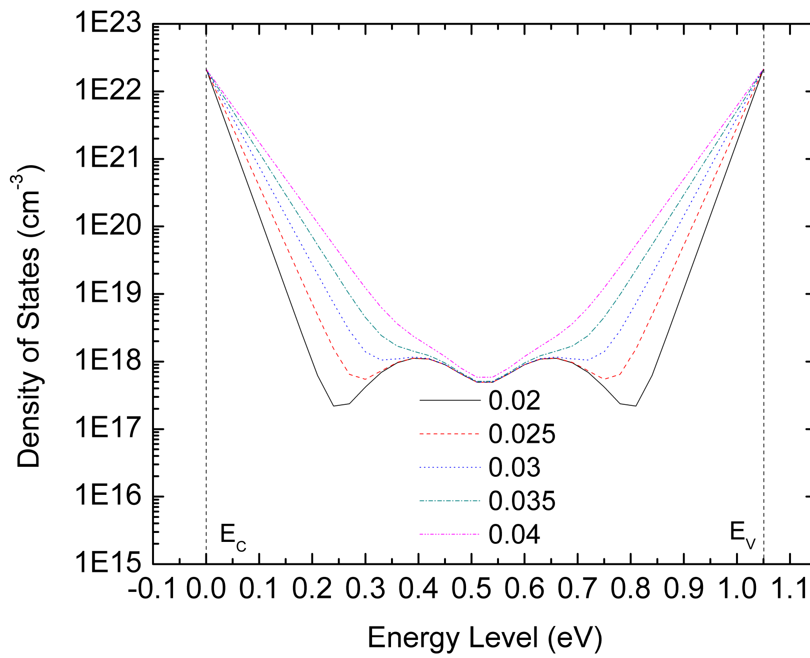


Figure 4.10 DOS profile of various WTA settings

The DOS distributions are illustrated in Figure 4.10. The energy level was quantized to 36 points for computerized process to achieve simulation accuracy and running time. Usually, the more quantized points result in better accuracy on experimental data, however, the more running time required.

The effect of wider characteristic decay energy can be explained by decrease of channel resistance weight according to Figure 4.8 and Figure 4.9. The drain current decreases due to increase of total series resistance network which can be observed in Figure 4.8 while the channel resistance weight decreases as shown in Figure 4.9.

4.3 Summary and Discussions

The effect of parasitic resistance has been investigated in this chapter using numerical simulation method. It is clearly seen that the transconductance degradation effect was originates from parasitic resistance regarding various parasitic resistance, channel length simulation results. The weight of channel resistance in the series resistance network is the key of the parasitic resistance effects. When the weight of channel resistance is relatively low, most of the voltage applied between source and drain will be distributed across parasitic resistance components. In other words, the actual voltage applied to the TFT component become significantly lower than that across parasitic resistances. It implies inferior performance compared to low parasitic resistance devices. To eliminate the transconductance degradation, increasing the channel resistance weight by implementing longer channel length device or more amorphous like nanocrystalline silicon channel can be possible solutions. However, employing larger device or reducing crystalinity of nanocrystalline silicon is not preferable since the former require more space and the latter implies returning to amorphous technology. Therefore, the only way to resolve detrimental parasitic resistance effect is reducing the parasitic resistance at least up to 100 kΩ range. It can be achieved by improving n+ nc-Si conductivity and reducing contact resistance at source/drain. Furthermore, by resolving high parasitic resistance problem, it can be possible to achieve higher field effect mobility, since the field effect mobility was also affected by high parasitic resistance component according to Figure 4.7.

Chapter 5
Conclusions

5.1 Summary

In this thesis, several material properties and device aspects for bottom bate staggered nc-Si:H TFT has been covered.

In material properties research, we characterized a-SiNx for gate dielectric purpose for the bottom gate nc-Si:H TFT and n+ nc-Si:H for contact layers. We used FTIR and I-V/C-V measurements for a-SiNx gate dielectric revealing its nitrogen rich composition, breakdown field 4.3 MV/cm, electron accumulation behavior at -10 to -40 V range and relative permittivity as 6.15. Although, the a-SiNx was not ideally acceptable for TFT passivation purpose due to low breakdown field, its nitrogen rich composition made acceptable for TFT gate dielectric purpose. In n+ nc-Si:H characterization, we adopted Raman spectroscopy and I-V measurement, revealing 56 % of crystalinity and 0.42 S/cm of dark conductivity which imply the film maintained its crystalinity enough to be called nanocrystalline film.

In device aspects for nc-Si:H TFT, we introduced fully wet etch fabrication process, TFT performance factors from the fabrication, and numerical analysis for parasitic resistance effect. Also, we have shown possibility of the wet etch process can be adopted for direct conversion X-ray imager array manufacture with a few modifications. The fabrication process required 5 lithography steps and a single or a couple of wet etch steps are involved to each lithography steps. The modification of the process for X-ray imager revealed 7 lithography steps required and circuitry components can be integrated into current 5 mask process except the mushroom electrode.

To extract performance factors and analyze the electrical characteristics of TFTs, we used conventional I-V measurement methods. In transfer characteristics, it revealed performance factors: the threshold voltage of 7.22 V, subthreshold slope of 0.63 V/decade, field effect mobility of 0.07 $cm^2/V\cdot s$, and on/off ratio of 10^6. Also, transconductance degradation and field effect mobility degradation from parasitic resistance effect has been observed. In output

characteristics, the field effect mobility degradation and current crowding effect was found as well due to severe parasitic resistance component.

To analyze the parasitic resistance effect, we utilized a TCAD simulation using a simple device structure and parasitic resistance equivalent circuit model. The simulation involved variation of parasitic resistance component of equivalent circuit model, channel length of the bottom gate nc-Si:H TFT, and intrinsic attribute of the nc-Si:H channel layer. In the variation of parasitic resistance simulation results, the parasitic resistance can be told as 1.733 MΩ with our series resistance network model and the parasitic resistance effect can be remedied by reducing the parasitic resistance component to 100 kΩ. In channel length variation part, the parasitic resistance component degrades 36 % in threshold voltage and 60 % in field effect mobility when the channel length decrease from 200 μm to 10 μm in current 1.733 MΩ case while the degradation was reduced to 16 % and 11 %, respectively, in 1 kΩ case. Lastly, in variation of intrinsic properties of channel layer, the transconductance degradation effect become severe even if we improve the channel by reducing defects while not improving, or reducing, the parasitic resistance components. Therefore, to improve TFT performance, the parasitic resistance effect must be the first to be remedied.

5.2 Future Research

According to results demonstrated in this thesis, we can provide a few suggestions to remedy parasitic resistance effect and to improve the TFT performance.

- To analyze parasitic resistance effect in deeper details, one can adopt a more complicated structure for simulation by using a process simulation module. It will enable to divide the lumped parasitic resistance component to its origins: contact resistance between n+ nc-Si:H source/drain contact layers and metal electrodes, series resistance of the contact layers, and series resistance of the nc-Si:H channel layer.
- It is obvious that, we have high contact resistance in source/drain area of TFTs. It can be avoided by performing BHF dip before source/drain metal contact deposition carefully and moving the wafers from etching facility to metal deposition facility as

fast as possible. However, it requires human skill and perfect process environment to be performed. Therefore, adjusting and simplifying the process by employing reactive ion etching (RIE) while removing protection silicon nitride and mask 3 and 4.

- The improvement of n+ nc-Si:H layer can be one of important future research topic. The recipe for higher dark conductivity n+ nc-Si:H which covers the wafer surface uniformly should be researched not only to improve electrical properties of n+ nc-Si:H quality, but also to realize implementation of large area application with current devices.
- Finally, passivation purpose silicon nitride can be researched for large area X-ray imager applications. It can be achieved by reducing hydrogen component in current silicon nitride by adjusting gas flow ratio and introducing dilution gas such as nitrogen.

More future research topics can be introduced to amplify performances of TFT and simplify the fabrication process. However, reducing the parasitic resistance effect is the most important topic at this point.

Appendix A

Input Deck of the Simulation

- **Structure Definition Part**

```
go atlas
# Kyung-Wook Shin
# G2N Centre, University of Waterloo
# Jan. 07, 2008
#

# TFT structure: standard (Loff = 0), L = 50 um, t_ch = 50 nm, tsinx = 300 nm
mesh
x.m     l=0       spac=2.
x.m     l=20      spac=3.
x.m     l=35      spac=5.
x.m     l=50      spac=0.25
x.m     l=75      spac=3.
x.m     l=100     spac=0.25
x.m     l=115     spac=5.
x.m     l=130     spac=3.
x.m     l=150     spac=2.

y.m     l=-0.05   spac=0.05
y.m     l=0       spac=0.0075
y.m     l=0.05    spac=0.0075
y.m     l=0.35    spac=0.25
y.m     l=10.     spac=5.
# Regions
```

```
# 3=nitride, 1,2=silicon, 4=oxide
region          num=1          y.min=-0.05  y.max=0      silicon
region          num=2          y.min=0.     y.max=0.05   silicon
region          num=3          y.min=0.05   y.max=0.35   nitride
region          num=4          y.min=0.35   oxide
# Electrodes
# 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate electrode
elec      num=1      x.min=50      x.max=100    y.min=0.35    y.max=0.35
    name=gate
elec      num=2      x.min=0.      x.max=20.    y.min=-0.05   y.max=-0.05
    name=source
elec      num=3      x.min=130.    x.max=150.   y.min=-0.05   y.max=-0.05
    name=drain
# Doping
doping          reg=2  uniform      conc=1.e11   n.type
doping          reg=2  uniform      conc=1.e11   n.type
doping          reg=1  gauss        conc=1.e20   n.type       x.right=50
    char=0.3
doping          reg=1  gauss        conc=1.e20   n.type       x.left=100
    char=0.3
save outf="STD_STR_L=50.str"
#tonyplot    "STD_STR_L=50.str" -set "doping.set"


go atlas
# TFT structure: L=200
mesh
x.m       l=0        spac=2.
x.m       l=20       spac=3.
x.m       l=35       spac=5.
```

```
x.m         l=50        spac=0.25
x.m         l=150       spac=3.
x.m         l=250       spac=0.25
x.m         l=265       spac=5.
x.m         l=280       spac=3.
x.m         l=300       spac=2.

y.m         l=-0.05     spac=0.05
y.m         l=0         spac=0.0075
y.m         l=0.05      spac=0.0075
y.m         l=0.35      spac=0.25
y.m         l=10.       spac=5.
# Regions
# 3=nitride, 1,2=silicon, 4=oxide
region          num=1           y.min=-0.05  y.max=0      silicon
region          num=2           y.min=0.     y.max=0.05   silicon
region          num=3           y.min=0.05   y.max=0.35   nitride
region          num=4           y.min=0.35   oxide
# Electrodes
# 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate electrode
elec        num=1       x.min=50     x.max=250.   y.min=0.35   y.max=0.35
    name=gate
elec        num=2       x.min=0.     x.max=20.    y.min=-0.05  y.max=-0.05
    name=source
elec        num=3       x.min=280.   x.max=300.   y.min=-0.05  y.max=-0.05
    name=drain
# Doping
doping          reg=2  uniform      conc=1.e11   n.type
```

```
doping      reg=2  uniform   conc=1.e11   n.type
doping      reg=1  gauss     conc=1.e20   n.type     x.right=50
    char=0.3
doping      reg=1  gauss     conc=1.e20   n.type     x.left=250
    char=0.3
save outf="STD_STR_L=200.str"
#tonyplot   "STD_STR_L=200.str" -set "doping.set"


go atlas
# TFT structure: L=400
mesh
x.m     l=0       spac=2.
x.m     l=20      spac=3.
x.m     l=35      spac=5.
x.m     l=50      spac=0.25
x.m     l=250     spac=3.
x.m     l=450     spac=0.25
x.m     l=465     spac=5.
x.m     l=480     spac=3.
x.m     l=500     spac=2.

y.m     l=-0.05   spac=0.05
y.m     l=0       spac=0.0075
y.m     l=0.05    spac=0.0075
y.m     l=0.35    spac=0.25
y.m     l=10.     spac=5.
# Regions
# 3=nitride, 1,2=silicon, 4=oxide
region      num=1            y.min=-0.05  y.max=0     silicon
```

```
region          num=2           y.min=0.        y.max=0.05      silicon
region          num=3           y.min=0.05      y.max=0.35      nitride
region          num=4           y.min=0.35      oxide
# Electrodes
# 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate electrode
elec     num=1     x.min=50      x.max=450.    y.min=0.35     y.max=0.35
    name=gate
elec     num=2     x.min=0.      x.max=20.     y.min=-0.05    y.max=-0.05
    name=source
elec     num=3     x.min=480.    x.max=500.    y.min=-0.05    y.max=-0.05
    name=drain
# Doping
doping          reg=2  uniform     conc=1.e11     n.type
doping          reg=2  uniform     conc=1.e11     n.type
doping          reg=1  gauss       conc=1.e20     n.type      x.right=50
    char=0.3
doping          reg=1  gauss       conc=1.e20     n.type      x.left=450
    char=0.3
save outf="STD_STR_L=400.str"
tonyplot     "STD_STR_L=400.str" -set "doping.set"


go atlas
# TFT structure: L=100
mesh
x.m      l=0       spac=2.
x.m      l=20      spac=3.
x.m      l=35      spac=5.
x.m      l=50      spac=0.25
```

```
x.m       l=100     spac=3.
x.m       l=150     spac=0.25
x.m       l=165     spac=5.
x.m       l=180     spac=3.
x.m       l=200     spac=2.

y.m       l=-0.05   spac=0.05
y.m       l=0       spac=0.0075
y.m       l=0.05    spac=0.0075
y.m       l=0.35    spac=0.25
y.m       l=10.     spac=5.
# Regions
# 3=nitride, 1,2=silicon, 4=oxide
region          num=1          y.min=-0.05  y.max=0      silicon
region          num=2          y.min=0.     y.max=0.05   silicon
region          num=3          y.min=0.05   y.max=0.35   nitride
region          num=4          y.min=0.35   oxide
# Electrodes
# 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate electrode
elec      num=1     x.min=50    x.max=150   y.min=0.35   y.max=0.35
    name=gate
elec      num=2     x.min=0.    x.max=20.   y.min=-0.05  y.max=-0.05
    name=source
elec      num=3     x.min=180.  x.max=200.  y.min=-0.05  y.max=-0.05
    name=drain
# Doping
doping          reg=2  uniform      conc=1.e11   n.type
doping          reg=2  uniform      conc=1.e11   n.type
```

```
doping          reg=1  gauss       conc=1.e20   n.type       x.right=50
    char=0.3
doping          reg=1  gauss       conc=1.e20   n.type       x.left=150
    char=0.3
save outf="STD_STR_L=100.str"
#tonyplot    "STD_STR_L=100.str" -set "doping.set"


go atlas
# TFT structure: L=10
mesh
x.m       l=0         spac=2.
x.m       l=20        spac=3.
x.m       l=35        spac=5.
x.m       l=50        spac=0.25
x.m       l=55        spac=3.
x.m       l=60        spac=0.25
x.m       l=75        spac=5.
x.m       l=90        spac=3.
x.m       l=110       spac=2.

y.m       l=-0.05     spac=0.05
y.m       l=0         spac=0.0075
y.m       l=0.05      spac=0.0075
y.m       l=0.35      spac=0.25
y.m       l=10.       spac=5.
# Regions
# 3=nitride, 1,2=silicon, 4=oxide
region          num=1             y.min=-0.05  y.max=0      silicon
region          num=2             y.min=0.     y.max=0.05   silicon
```

```
region          num=3           y.min=0.05   y.max=0.35   nitride
region          num=4           y.min=0.35   oxide
# Electrodes
# 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate electrode
elec      num=1     x.min=50     x.max=60     y.min=0.35    y.max=0.35
    name=gate
elec      num=2     x.min=0.     x.max=20.    y.min=-0.05   y.max=-0.05
    name=source
elec      num=3     x.min=90.    x.max=110.   y.min=-0.05   y.max=-0.05
    name=drain
# Doping
doping          reg=2  uniform    conc=1.e11   n.type
doping          reg=2  uniform    conc=1.e11   n.type
doping          reg=1  gauss      conc=1.e20   n.type       x.right=50
    char=0.3
doping          reg=1  gauss      conc=1.e20   n.type       x.left=60
    char=0.3
save outf="STD_STR_L=10.str"
#tonyplot    "STD_STR_L=10.str" -set "doping.set"


go atlas
# TFT structure: L=20
mesh
x.m       l=0        spac=2.
x.m       l=20       spac=3.
x.m       l=35       spac=5.
x.m       l=50       spac=0.25
x.m       l=60       spac=3.
x.m       l=70       spac=0.25
```

```
x.m         l=85          spac=5.
x.m         l=100         spac=3.
x.m         l=120         spac=2.

y.m         l=-0.05       spac=0.05
y.m         l=0           spac=0.0075
y.m         l=0.05        spac=0.0075
y.m         l=0.35        spac=0.25
y.m         l=10.         spac=5.
# Regions
# 3=nitride, 1,2=silicon, 4=oxide
region            num=1              y.min=-0.05  y.max=0       silicon
region            num=2              y.min=0.     y.max=0.05    silicon
region            num=3              y.min=0.05   y.max=0.35    nitride
region            num=4              y.min=0.35   oxide
# Electrodes
# 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate electrode
elec        num=1         x.min=50     x.max=70     y.min=0.35   y.max=0.35
    name=gate
elec        num=2         x.min=0.     x.max=20.    y.min=-0.05  y.max=-0.05
    name=source
elec        num=3         x.min=100.   x.max=120.   y.min=-0.05  y.max=-0.05
    name=drain
# Doping
doping            reg=2  uniform     conc=1.e11   n.type
doping            reg=2  uniform     conc=1.e11   n.type
doping            reg=1  gauss       conc=1.e20   n.type       x.right=50
    char=0.3
```

```
doping          reg=1  gauss      conc=1.e20   n.type      x.left=70
    char=0.3

save outf="STD_STR_L=20.str"

#tonyplot    "STD_STR_L=20.str" -set "doping.set"


go atlas

# TFT structure: L=30

mesh

x.m       l=0        spac=2.

x.m       l=20       spac=3.

x.m       l=35       spac=5.

x.m       l=50       spac=0.25

x.m       l=65       spac=3.

x.m       l=80       spac=0.25

x.m       l=95       spac=5.

x.m       l=110      spac=3.

x.m       l=130      spac=2.


y.m       l=-0.05    spac=0.05

y.m       l=0        spac=0.0075

y.m       l=0.05     spac=0.0075

y.m       l=0.35     spac=0.25

y.m       l=10.      spac=5.

# Regions

# 3=nitride, 1,2=silicon, 4=oxide

region          num=1           y.min=-0.05  y.max=0      silicon

region          num=2           y.min=0.     y.max=0.05   silicon

region          num=3           y.min=0.05   y.max=0.35   nitride

region          num=4           y.min=0.35   oxide
```

```
# Electrodes
# 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate electrode
elec        num=1       x.min=50      x.max=80      y.min=0.35     y.max=0.35
      name=gate
elec        num=2       x.min=0.      x.max=20.     y.min=-0.05    y.max=-0.05
      name=source
elec        num=3       x.min=110.    x.max=130.    y.min=-0.05    y.max=-0.05
      name=drain
# Doping
doping            reg=2  uniform      conc=1.e11    n.type
doping            reg=2  uniform      conc=1.e11    n.type
doping            reg=1  gauss        conc=1.e20    n.type         x.right=50
      char=0.3
doping            reg=1  gauss        conc=1.e20    n.type         x.left=80
      char=0.3
save outf="STD_STR_L=30.str"
#tonyplot    "STD_STR_L=30.str" -set "doping.set"


go atlas
# TFT structure: L=40
mesh
x.m         l=0         spac=2.
x.m         l=20        spac=3.
x.m         l=35        spac=5.
x.m         l=50        spac=0.25
x.m         l=70        spac=3.
x.m         l=90        spac=0.25
x.m         l=105       spac=5.
x.m         l=120       spac=3.
```

```
x.m       l=140      spac=2.

y.m       l=-0.05    spac=0.05
y.m       l=0        spac=0.0075
y.m       l=0.05     spac=0.0075
y.m       l=0.35     spac=0.25
y.m       l=10.      spac=5.
# Regions
# 3=nitride, 1,2=silicon, 4=oxide
region          num=1          y.min=-0.05  y.max=0      silicon
region          num=2          y.min=0.     y.max=0.05   silicon
region          num=3          y.min=0.05   y.max=0.35   nitride
region          num=4          y.min=0.35   oxide
# Electrodes
# 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate electrode
elec      num=1      x.min=50      x.max=90      y.min=0.35    y.max=0.35
    name=gate
elec      num=2      x.min=0.      x.max=20.     y.min=-0.05   y.max=-0.05
    name=source
elec      num=3      x.min=120.    x.max=140.    y.min=-0.05   y.max=-0.05
    name=drain
# Doping
doping          reg=2  uniform      conc=1.e11   n.type
doping          reg=2  uniform      conc=1.e11   n.type
doping          reg=1  gauss        conc=1.e20   n.type       x.right=50
    char=0.3
doping          reg=1  gauss        conc=1.e20   n.type       x.left=90
    char=0.3
save outf="STD_STR_L=40.str"
```

```
#tonyplot    "STD_STR_L=40.str" -set "doping.set"

go atlas
# TFT structure: L=70
mesh
x.m         l=0          spac=2.
x.m         l=20         spac=3.
x.m         l=35         spac=5.
x.m         l=50         spac=0.25
x.m         l=85         spac=3.
x.m         l=120        spac=0.25
x.m         l=135        spac=5.
x.m         l=150        spac=3.
x.m         l=170        spac=2.

y.m         l=-0.05      spac=0.05
y.m         l=0          spac=0.0075
y.m         l=0.05       spac=0.0075
y.m         l=0.35       spac=0.25
y.m         l=10.        spac=5.
# Regions
# 3=nitride, 1,2=silicon, 4=oxide
region          num=1          y.min=-0.05  y.max=0     silicon
region          num=2          y.min=0.     y.max=0.05  silicon
region          num=3          y.min=0.05   y.max=0.35  nitride
region          num=4          y.min=0.35   oxide
# Electrodes
# 1=gate, 2=source, 3=drain
```

```
# To give gate offset, change x.max of gate electrode
elec     num=1    x.min=50     x.max=120    y.min=0.35    y.max=0.35
    name=gate
elec     num=2    x.min=0.     x.max=20.    y.min=-0.05   y.max=-0.05
    name=source
elec     num=3    x.min=150.   x.max=170.   y.min=-0.05   y.max=-0.05
    name=drain
# Doping
doping        reg=2  uniform    conc=1.e11   n.type
doping        reg=2  uniform    conc=1.e11   n.type
doping        reg=1  gauss      conc=1.e20   n.type     x.right=50
    char=0.3
doping        reg=1  gauss      conc=1.e20   n.type     x.left=120
    char=0.3
save outf="STD_STR_L=70.str"
#tonyplot   "STD_STR_L=70.str" -set "doping.set"

Quit
```

- **Calculation Part**

```
go atlas

TITLE Bottom gate TFT at Vds=10V

#**************************************************************************************#
#
# Use this file for curve fitting
#
# - General rules of thumb
#
```

```
# 1. Make a 10 (V) foler dated today under the ATLAS folder
# 2. Replace 'master' in the file name with today, e.g. '11-16-2007' for Nov 16, 2007.
# 3. Stick to the current names for data extraction
# 4. Save tonyplot using JPG format.
#
#*********************************************************************************#

mesh inf=../../../str/STD_STR_L=50.STR

# Set parameters for nc-Si:H

material material=silicon mun=65 mup=3

# numa and numd are 12 initially but change them to 36 when fitting is done
# initial fitting parameter is based on polycrystalline example
defects nta=2.15e22 ntd=2.15e22 wta=0.032 wtd=0.032 \
  nga=1.125e18 ngd=1.125e18 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
  sigtae=1.e-16 sigtah=1.e-14 sigtde=1.e-14 sigtdh=1.e-16 \
  siggae=1.e-16 siggah=1.e-14 siggde=1.e-14 siggdh=1.e-16 \
  dfile=donors.dat afile=acceptors.dat \
  numa=12 numd=12

interface qf=3e11

# Define parameters for contacts
# initial contact resistance is 50kOhm == 1.5e7 Ohm_um
contact num=1 alum
contact num=2 alum resistance=5.2e8
```

```
contact num=3 alum resistance=5.2e8

# Define models

models srh print trap.coulombic

method newton
#itlimit=100
solve init
solve prev vdrain=0.1
solve prev vdrain=0.2
solve prev vdrain=0.5
solve vdrain=1 vfinal=10 vstep=1 name=drain

log outf=forward_10.log
solve vgate=0 vstep=1 vfinal=50 name=gate
go atlas
extract init infile="forward_10.log"
extract name="forward_10" curve(v."gate", i."drain") outf="forward_10.dat"
extract name="gm_10" curve(v."gate",dydx(v."gate", i."drain")) outf="gm_10.dat"

tonyplot -overlay forward_10.dat ../../../target/sep/target.dat
tonyplot -overlay gm_10.dat ../../../target/sep/target_gm.dat

quit
```

Bibliography

1. I. D. French, S. C. Deane, and P. Roca I Cabarrocas, “Microcrystalline si tfts for integrated multiplexers and shift registers,” Proceedings of 21st International Display Conference and 8th International Display Workshops, pp. 367, Japan, 2001
2. I-C. Cheng and S. Wagner, “Nanocrystalline sililicon thin film transistors,” IEE Proc.-Circuits Devices Syst., Vol. 150, No. 4, August 2003.
3. Mohammad R. Esmaeili-Rad, Flora Li, Andrei Sazonov, and Arokia Nathan, “stability of nanocrystalline silicon bottom-gate thin film transistors with silicon nitride gate dielectric,” J. Appl. Phys., Vol. 102, 06452, September 2007.
4. R. L. Weisfield, “Amorphous silicon TFT X-ray image sensors,” IEEE International Electron Devices Meeting (IEDM 1998) Technical digegst, pp. 21-24, 1998.
5. S.O. Kasap and J.A. Rowlands, “Direct-conversion flat-panel X-ray image detectors,” IEE Proc.-Circuits Devices Syst., Vol. 149, No. 2, April 2002.
6. J. A. Rowlands, “Current Advances and Future Trends in X-Ray Digital Detectors for Medical Applications,” IEEE Transactions on Instrumentation and Measurement, Vol. 47, No. 6, December 1998.
7. A. M. Miri and S. G. Chamberlain, “A totally wet etch fabrication technology for amorphous silicon thin film transistors,” Proceedings of Material Research Society Symposium, Vol. 377, pp. 737-742, 1995.
8. H. F. Sterling and R. C. G. Swann, “Chemical vapour deposition promoted by r.f. discharge,” Solid-State Electronics, Vol. 8, pp. 653-654, 1965.
9. Paul K. Weimer, “The TFT - a new thin-film transistor,” Proceedings of the IRE, Vol. 50, pp. 1462-1469. IRE, June 1962.
10. P. G. Le Comber, W. E. Spear, and A. Ghaith, “Amorphous silicon Field-effect device and possible application,” Electronics Letters, Vol. 15(6), pp. 179-181, March 1979.
11. Karim Sallaudin Karim, “Pixel Architectures for Digital Imaging Using Amorhpous Silicon Technology,” PhD thesis, Universitiy of Waterloo, Waterloo, 2002.
12. D. E. Carlson. Monolithic amorphous silicon alloy solar modules. Solar Energy Materials and Solar Cells, Vol. 78(1-4), 627-645, July 2003.

13. R.B. Min and S. Wagner, Nanocrystalline silicon thin-film transistors with 50-nm-thick deposited channel layer, 10 cm2 $cm^2/V\cdot s$ electron mobility and 10^8 on/off current ratio. Applied Physics A, Vol. 74, pp. 541-543, 2002.
14. Akihisa Matsuda, “Growth mechanism of microcrystalline silicon obtained from reactive plasmas,” Thin Solid Films, Vol. 337, pp. 1-6, January 1999.
15. J. G. Shaw and M. Hack, “An analytic model for calculating trapped charge in amorphous silicon,” J. Appl. Phys., Vol. 64, pp. 4562-4566, 1988.
16. ATLAS user’s manual, Silvaco Int’l, Santa Clara, USA, 2007.
17. G. N. Parsons, J. H. Souk, and J. Bately, “Low hydrogen content stoichiometric silicon nitride films deposited by plasma-enhanced chemical vapor deposition,” J. Appl. Phys., Vol. 70 (3), pp. 1553-1560, August 1991.
18. E. A. Taft, “Characterization of Silicon Nitride Films,” J. Electrochem. Soc., Vol. 118, pp. 1341, August 1971.
19. I-Chun Cheng and Sigurd Wagner, “Hole and electron Field effect mobilities in anocrystalline silicon deposited at 150 ^{o}C,” Applied Physics Letters, Vol. 80(3), pp. 440-442, January 2002.
20. J. Kanicki, E. Hasan, D.F. Kotecki, T. Takamori, and J.H. Griffith, “Properties and application of undoped hydrogenated microcrystalline silicon thin films,” A. Madan, M.J. Thompson, P. C. Taylor, Y. Hamakawa, and P. G. LeComber, editors, Amorphous Silicon Technology-1989 Symposium, pp. 173-179. Materials Research Society, 1989.
21. Amir Masoud Miri, “Development of a Novel Wet Etch Fabrication Technology for Amorphous Silicon Thin-Film Transistors,” PhD thesis, University of Waterloo, Waterloo, Canada, 1996.
22. D. W. Greve, “Field Effect Devices and Applications: Devices for Portable, Low-Power, and Imaging Systems,” Prentice-Hall, Englewood Cliffs, NJ, 1998.
23. M. J. Powell, “The physics of amorphous-silicon thin-film transistors,” IEEE Transactions on Electron Devices, vol. 36, pp. 2753-63, 1989.
24. M. Shur and M. Hack, “Physics of amorphous silicon based alloy field-effect transistors,” Journal of Applied Physics, vol. 55, pp. 3831-42, 1984.

25. Mohammad-Reza Esmaeili-Rad, “Nanocrystalline Silicon Thin Film Transistor,” PhD thesis, University of Waterloo, Waterloo, Canada, 2008.
26. Hyun Jung Lee, “Top-Gate Nanocrystalline Silicon Thin Film Transistors,” PhD thesis, University of Waterloo, Waterloo, Canada, 2008.
27. Ke Long, “Towards Flexible Full-Color Active Matrix Organic Light-Emitting Displays: Dry Dye Printing For OLED Integration and 280°C Amorphous-Silicon Thin-Film Transistors on Clear Plastic Substrates,” PhD thesis, Princeton University, New Jersey, 2006.
28. S. Luan and G. W. Neudeck, “An experimental study of the source/drain parasitic resistance effects in amorphous silicon thin film transistors,” J. Appl. Phys., vol. 72, pp. 766-772, 1992.
29. M. J. Thompson, N. M. Johnson, M. D. Moyer, and R. Lujan, “Thin-film transistors on a-Si:H,” IEEE Trans. Electron Devices, vol. ED-29, pp. 1643-1646, 1982.
30. A. Valletta, L. Mariucci, G. Fortunato, and S. D. Brotherton, “Surface-scattering effects in polycrystalline silicon thin-film transistors,” Appl. Phys. Lett., vol. 82, pp. 3119-3121, 2003.
31. J. Kanicki, F. R. Libsch, J. Griffith, and R. Polastre, “Performance of thin hydrogenated amorphous silicon thin-film transistos,” J. Appl. Phys., vol. 69, pp. 2339-2345, 1991.
32. Dosi Dosev, “Fabrication, characterisation and modelling of nanocrystalline silicon thinfilm transistors obtained by hot-wire chemical vapor deposition,” Ph.D. thesis, Universitat Politecnica de Catalunya, 2003.
33. D. Striakhilev, A. Sazonov, and A. Nathan, “Amorphous silicon nitride deposited 120 ^{o}C for organic light emitting display-thin film transistor arrays on plastic substrates,” J. Vac. Sci. Technol. A, Vol. 20(3), May/June 2002.
34. C.-H. Lee, D. Striakhilev, and A. Nathan, “Highly conductive n+ hydrogenated microcrystalline silicon and its application in thin film transistors,” J. Vac. Sci. Technol. A, Vol. 22(3), May/June 2004.
35. B. C. Lim, Y. J. Choi, J. H. Choi, and J. Jang, “Hydrogenated Amorphous Silicon Thin Film Transistor Fabricated on Plasma Treated Silicon Nitride,” IEEE Trans. Electron

Devices, Vol. 47 (2), pp. 367, February 2000.

36. N. Lustig and J. Kanicki, “Gate dielectric and contact effects in hydrogenated amorphous silicon nitride thin-film transistors,” J. Appl. Phys. Vol. 65 (10), May 1989.
37. K. Yamaguchi, “Field-Dependent Mobility Model for Two-Dimensional Numerical Analysis of MOSFET’s,” IEEE Trans. Electron Devices, Vol. ED-26 (7), pp. 1068, July 2000.
38. E. H. Nicollian and A. Goetzberger, “Lateral AC Current Flow Model for Metal-Insulator-Semiconductor Capacitors”, IEEE Trans. Electron Devices, Vol. 12 (3), pp. 108-117, March 1965.
39. T Nishimura, Y Akasaka, H Nakata, A Ishizu, and T Matsumoto, “Characteristics of TFT fabricated in laser-recrystallized polysilicon for active LC display,” SID Int. Symp. Digest Tech. Papers, p. 36, 1982.
40. A. W. Wang and K. C. Saraswat, “A strategy for modeling of variations due to grain size in polycrystalline thin-film transistors,” IEEE Trans. Electron Devices, Vol. 47, pp. 1035-1043, 2000.
41. P. Roca i Cabarrocas, “Plasma enhanced chemical vapor deposition of silicon thin films for large area electronics,” Curr. Opin. Solid State Mater. Sci., vol. 6, pp. 439-444, 2002.
42. A. Matsuda, “Microcrystalline silicon. Growth and device application,” J. Non-Cryst. Solids, Vol. 338-340, pp. 1-12, 2004.
43. P. Alpuim, V. Chu, and J. P. Conde, “Doping of amorphous and microcrystalline silicon films deposited at low substrate temperatures by hot-wire chemical vapor deposition,” J. Vac. Sci. Technol. A, Vol. 19, pp. 2328-2334, 2001.
44. A to Z Materials, http://www.azom.com/details.asp?ArticleID=53
45. M. Hack, A. Chwang, Y.-J. Tung, R. Hewitt, J. Brown, J. P. Lu, C. Shih, J. Ho, R. A. Street, L. Moro, X. Chu, T. Krajewski, N. Rutherford, and R. Visser, “Status and opportunities for high efficiency OLED displays on flexible substrates.,” Proceedings of Material Research Society Symposium, Vol. 870E, pp. H3.1.1-10, 2005.