Vertical Thin Film Transistors for Large Area Electronics

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

The prospect of producing nanometer channel-length thin film transistors (TFTs) for active matrix addressed pixelated arrays opens up new high-performance applications in which the most amenable device topology is the vertical thin film transistor (VTFT) in view of its small area. The previous attempts at fabricating VTFTs have yielded devices with a high drain leakage current, a low ON/OFF current ratio, and no saturation behaviour in the output current at high drain voltages, all induced by short channel effects. To overcome these adversities, particularly dominant as the channel length approaches the nano-scale regime, the reduction of the gate dielectric thickness is essential. However, the problems with scaling the gate dielectric thickness are the high gate leakage current and early dielectric breakdown of the insulator, deteriorating the device performance and reliability.

A novel ultra-thin SiN_x film suitable for the application as the gate dielectric of short channel TFTs and VTFTs is developed. The deposition is performed in a standard 13.56MHz PECVD system with silane and ammonia precursor gasses diluted in nitrogen. The deposited 50nm SiN_x films demonstrate excellent electrical characteristics in terms of a leakage current of 0.1 nA/cm^2 and a breakdown electric field of 5.6MV/cm.

Subsequently, the state of the art performances of 0.5um channel length VTFTs with 50 and 30nm thick SiN_x gate dielectrics are presented in this thesis. The transistors exhibit ON/OFF current ratios over 10^9, the subthreshold slopes as sharp as 0.23 V/dec, and leakage currents in the fA range. More significantly, a high associated yield is obtained for the fabrication of these devices on 3-inch rigid substrates.

Finally, to illustrate the tremendous potential of the VTFT for the large area electronics, a 2.2-inch QVGA AMOLD display with in-pixel VTFT-based driver circuits is designed and fabricated. An outstanding value of 56% compared to the 30% produced by conventional technology is achieved as the aperture ratio of the display. Moreover, the initial measurement results reveal an excellent uniformity of the circuit elements.

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Chapter 1

Introduction

The enormous growth of microelectronics has greatly affected the modern-day lifestyle due to the availability of sophisticated hardware ranging from health and entertainment to communication and space products. In particular, the advancements in microelectronics have led to production of large area electronic circuits owing to the low-cost deposition of silicon-based thin films over large surfaces [1]. At present, the applications of large area electronics include flat panel displays, thin film solar cells, and x-ray imagers, which are collectively generating an ever-growing multi-billion dollar business [2].

The basic building block of large area electronics is the thin film transistor (TFT), which is employed as an active and/or switching element. To enhance the performance in terms of speed, resolution, or sensitivity, the dimensions of the TFT must be scaled down in a manner similar to the trend followed in the very large-scale integration (VLSI) industry [3]. However, critical issues related to the small geometrical dimensions of the transistor

channel, widely known as short channel effects, emerge thus limiting the performance and reliability of the TFT [4].

To overcome the problems, which deteriorate the functionality of the TFT especially when the channel length approaches the nano-scale regime, a proper choice for TFT configuration, structure, and topology are mandatory. Moreover, an in-depth material study and optimization of the various layers employed in the fabrication of the TFT is essential. This thesis specifically addresses these issues and presents device fabrication and material development for non-conventional TFT architectures suitable for high performance and high-resolution large area electronics.

1.1 Active Matrix Pixelated Arrays

The backplane electronics for any active matrix display or imager consists of an array of pixels and associated programming lines running in rows and columns [5]. The basic unit in each array is a pixel, and each pixel consists of a sensor or light-emitting device and one or more TFTs. Therefore, as the demand on the performance of the system increases, requirements on the TFT characteristics become more challenging to satisfy.

Among the different display technologies, the active matrix liquid crystal displays (AMLCD) is the most mature [6]. Figure 1.1 (a) illustrates an 82-inch AMLCD TV produced by Samsung Company. Another rapidly growing technology is the active matrix organic light emitting diode (AMOLED) display. OLED displays have gained significant attention because of their potentially faster response time, larger viewing angles (>150°), higher contrast, lower power consumption, and lighter weight compared to the AMLCD [7], [8]. Figure 1.1(c) shows the images of Sony's recently marketed 11-

inch AMOLED display. Other important application of active matrix arrays is in imaging particularly for modalities such as radiography and fluoroscopy (Figure 1.1(b)). High image quality, large area imaging capability, low storage cost, and computerized handling/storage of sensory information constitute the ever-growing demands, pushing the imaging technology to new limits.

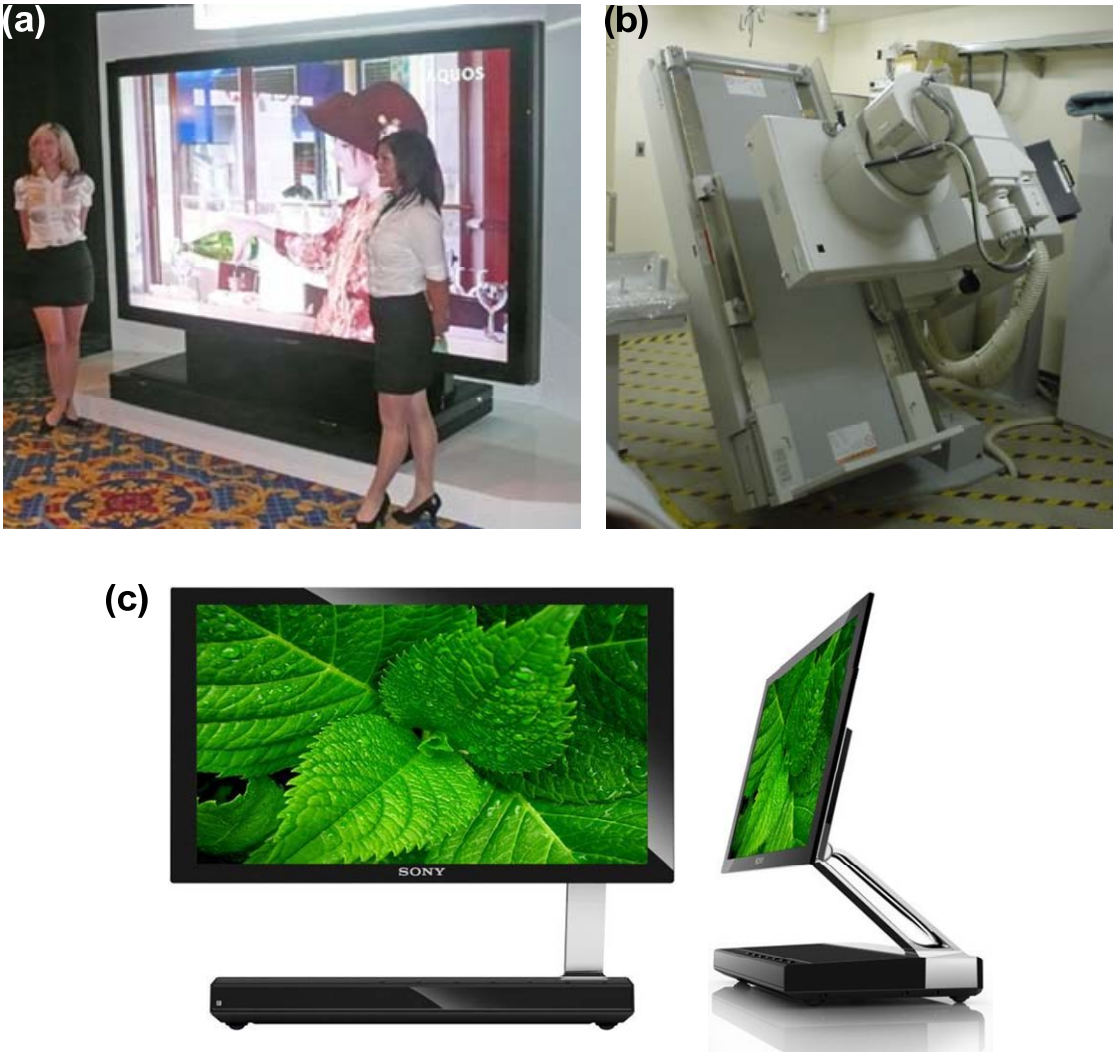

Figure 1.1: (a) Samsung's 82-inch LCD TV [9], (b) flat-panel medical imager [10], and (c) Sony's 11-inch AMOLED display [11].

Despite the differences in the functionality of TFTs in the pixel, the architecture of all active matrix arrays is similar as illustrated in Figure 1.2. The address and data lines run

horizontally and vertically between the pixels and connect each pixel to external circuitry. Typically, the vertical lines provide the data and bias connections, and the horizontal address lines are connected to the gates of TFTs.

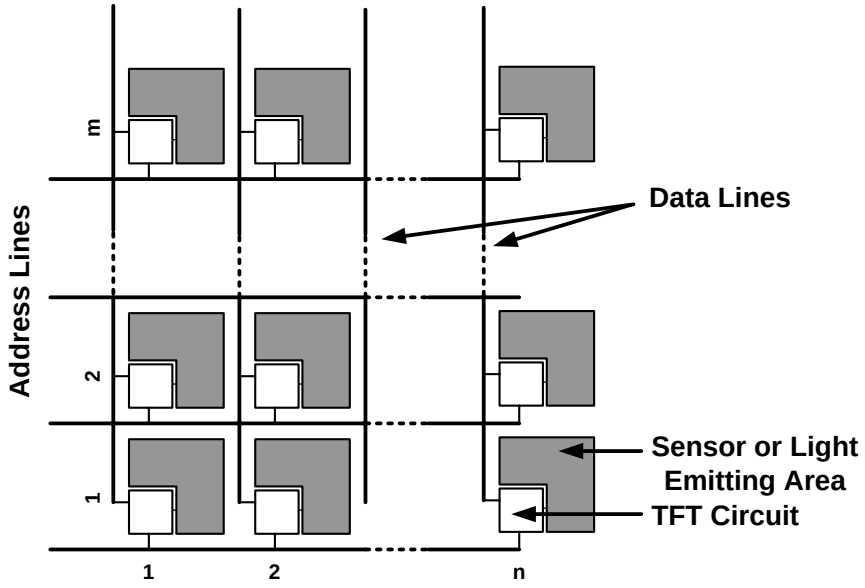

Figure 1.2: Schematic of active matrix array.

Depending on the function of the TFT in the circuit, the requirements on the performance specifications of the device vary. This, in turn, dictates the complexity and the cost of the fabrication process. The role of TFTs displays can be divided into two categories. For applications such as AMLCDs, the TFT acts as a switch. In AMOLED displays, the TFTs are used as linear integrated circuit elements, i.e. as switches, pass transistors, and drivers. As an example, the equivalent circuits for possible pixel architectures of an active matrix liquid crystal display (AMLCD) and an active matrix organic light emitting diode (AMOLED) display are depicted in Figure 1.3.

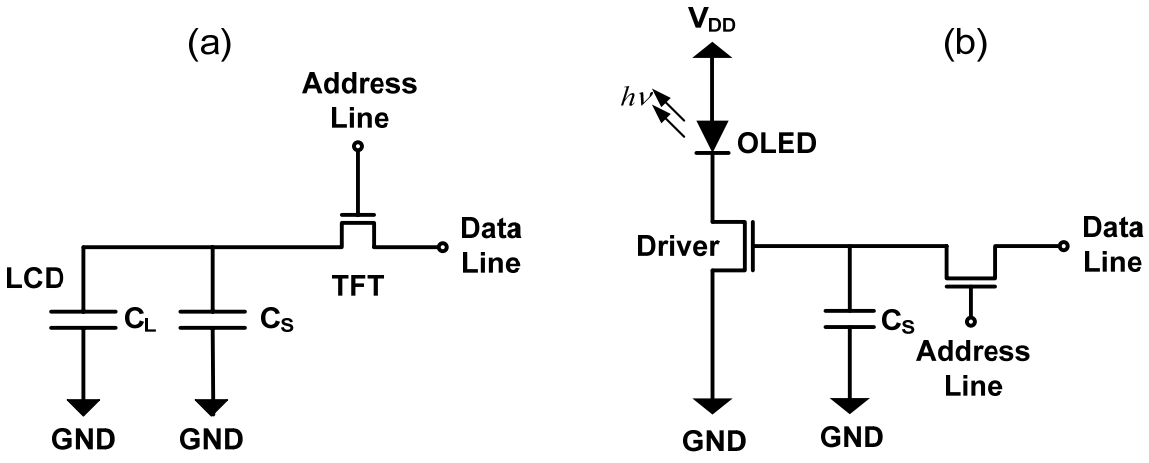

Figure 1.3: Basic circuit pixel for (a) AMLCD and (b) AMOLED display.

The history of the present TFT begins with the work of P. K. Weimer at RCA laboratories in 1962 [12]. From then on, TFTs have evolved in materials and structures to match different application requirements and this development is still going on.

Hydrogenated amorphous silicon (a-Si:H), nanocrystalline (nc)-, microcrystalline (μc)-, and poly-crystalline (poly)- Si are used as an active layer in the TFT depending on the application. Among the different family of materials, a-Si:H TFTs are popular for the large area electronics such as AMLCDs, AMOLED displays, and active matrix image sensors employed in document scanners and x-ray imagers. a-Si:H TFTs gain their reputation mainly due to the ability of low-cost high uniformity deposition over large areas (more than 1 meter in linear dimension) at low temperature (<300°C), which allows fabrication on a wide range of substrates. However, the most serious issue related to the present a-Si:H TFT is the operating speed due to low field effect mobility of electrons in the material (0.1-1 cm^2/V-s) [13].

One feasible solution to increase the operation speed of the a-Si:H TFT is to reduce its channel length, since the switching time is proportional to the channel length. Short channel TFTs have a shorter transit time for carriers to cross the channel. However, in

conventional TFTs, shortening the channel length is limited by fabrication issues associated with lithography and etching. Thus, for high-resolution matrix addressing and high-density TFT integration applications, alternative TFT configurations have to be considered where shrinking of TFTs dimensions are not limited by the above issues.

The focus of this thesis is on reducing the dimensions of TFTs for active matrix addressed pixelated arrays in order to advance the performance of flat panel applications. The remaining part of this chapter includes a brief introduction of vertical thin film transistors and the objectives of the conducted research.

1.2 Vertical Thin Film Transistors (VTFTs)

Figure 1.4 shows the simplified cross section of the vertical thin film transistors structure. The active channel in this device is deposited vertically and the channel length in the VTFT is defined by the intermediate SiN_x layer thickness between the drain and source islands. Therefore, the channel length can be accurately controlled and reduced down to nanometer-range by scaling the thickness of the insulator layer. Moreover, the area occupied by the TFT is not a function of the aspect ratio (W/L) [14]. Since the channel length (L) can be 1μm or less, the channel width W can be reduced accordingly to maintain the same W/L ratio as in the lateral TFT, resulting in a further significant reduction in TFT size.

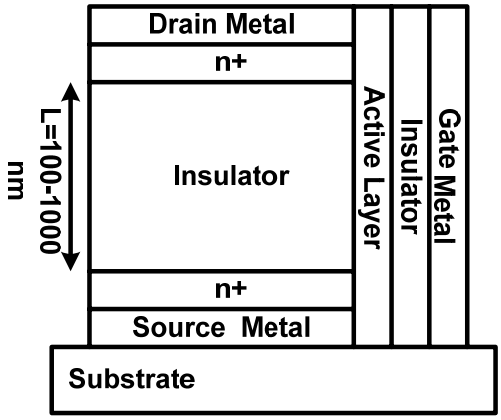

Figure 1.4: Schematic cross section of the vertical TFT structure.

Using small area transistors, the fill factor (defined as the ratio of light sensing area to the total pixel area) or aperture ratio (defined as the ratio of light emitting display area to the total pixel area), which determines the performance attributes in imagers or displays (such as dynamic range, brightness, contrast ratio, etc.), can be significantly enhanced. The VTFT offers an excellent platform due to its inherent structural characteristics of short channel length and small device area, enabling a new generation of low-cost, high-speed, and high-resolution applications. However, while the device holds great promise, there are severe issues related to its performance and reliability because of the scaled-down TFTs geometries. As the channel length shrinks, undesirable effects (so-called short channel effects), arise undermining the functionality of the TFTs. These adversities and the solution to alleviate their effects will be addressed in this thesis in detail.

1.3 Objectives of the Thesis

This doctoral study focuses on the fabrication of the vertical thin film transistors and the challenges related to the functionality and reliability of short channel lengths and small areas, in an attempt to make feasible high performance, high-resolution large area arrays.

The biggest challenge lies in dealing with short channel effects, which induce high drain leakage current, low on/off current ratio, and absence of the saturation behavior at high drain voltages. To overcome these adversities, which become prevail as the channel length approaches the nano-scale regime, reduction of the gate dielectric thickness is mandatory. However, the main problem that arises is the high gate leakage current and, more importantly, early dielectric breakdown, which undermines device reliability [15]. Hence an important goal of this thesis was to develop of an ultra thin silicon nitride insulator layer (SiN_x) as the gate dielectric. We report here for the first time, SiN_x with thicknesses as low as 30 nm, which has been employed as the VTFT gate dielectric providing the fabricated transistors with good performance and reliability.

1.4 Thesis Organization

A brief introduction to large area electronics and its applications is presented in Chapter 1. Here, different applications of TFTs serving as the building blocks of active matrix arrays are addressed. Lastly, the motivation for research on VTFTs and their potentially superior performance over conventional TFTs is discussed.

Chapter 2 reports the basics of lateral and vertical TFTs with a brief literature review. This chapter covers the detailed fabrication process of VTFTs and related issues. The challenges in formation of the vertical structure and associated process and solutions, in particular, deposition and etching techniques/conditions are discussed, along with initial electrical characteristics of the devices. Here, the underlying reasons for poor VTFT performance, particularly short channel effects, are reviewed.

Chapter 3 describes the impact of film thickness on leakage current and electrical breakdown of plasma enhanced chemical vapor deposited (PECVD) silicon nitride dielectrics. We consider SiN_x films of various thicknesses, in the range 50 to 300 nm, deposited on both planar and vertical sidewalls in resemblance to the structural topology of the vertical thin film transistor (VTFT). Both physical and electrical characteristics of the SiN_x with different thicknesses have been examined from the standpoint of performance characteristics and device reliability.

Chapter 5 focuses on development of sub-50 nm silicon nitride layers suitable for short channel TFTs. A systematic study on the relation between the material properties and the process conditions has been conducted to develop functional ultra-thin nitrides. The electrical, physical, and chemical properties of this nitride characterized using different techniques are reviewed in chapter 5.

Chapter 6 reports results of a-Si:H VTFTs fabricated using the ultra-thin SiN_x gate dielectric. VTFTs with different gate dielectric thickness are presented. The effect of the thin gate nitride on OFF current, ON current, and sub-threshold slope has been studied and compared VTFTs with conventional SiN_x gate dielectric. Also discussed is the impact of substituting the a-Si:H active layer with nc-Si on VTFT characteristics.

Chapter 7 discusses the applications of VTFTs in large area electronics. As a proof of concept, a 2.2-inch AMOLD array has been fabricated using optimized VTFTs as the building block for a two-transistor pixel circuit.

Chapter 8 concludes the thesis and outlines future work.

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Chapter 2

Thin Film Transistors and Integration Considerations

It is necessary to have a basic understanding of the thin film transistors (TFTs) since these devices serve as the building block of imagers or display panels. This chapter provides the reader with a concise description of both lateral and vertical TFTs. Following the introduction of the amorphous silicon TFT structure and its electrical characteristics, the motivation for the application of the vertical thin film transistors (VTFTs) is outlined. Then a brief literature review of VTFT is presented.

In this chapter the detailed fabrication process of the VTFT and the related issues are discussed. The challenges through the formation of the vertical structure and the developed processes and solutions are addressed. The details of the processing conditions for the deposition and etching techniques are reported along with the initial device

characteristics of VTFT constructed in University of Waterloo. At the end, the short channel effects will be introduced to explain the poor electrical behavior of the devices.

2.1 Lateral TFTs

Lateral hydrogenated amorphous silicon (a-Si:H) TFTs are the most popular active devices used in current large area electronics [1]. The a-Si:H TFT was first demonstrated in 1981 by Spear and LeComber's research group [2], [3]. The reproducible device characteristics and simple low-cost fabrication process renders a-Si:H TFT-based circuits very attractive for large area electronics [4].

Although a variety of configurations can be used for producing a-Si:H TFT's, the most popular structure is the inverted-staggered structure [3], [5]. Most researchers employ an inverted staggered structure due to its performance that is better than a top-gate structure where the gate insulator is deposited on the a-Si:H. On the contrary, in and inverted staggered structure, the a-Si:H film is deposited on the gate dielectric layer in a single vacuum-pump down process. This sequence of deposition is one of the best methods to achieve a high interface quality. Therefore, the field effect mobility of the inverted staggered devices is typically about 30% higher than that for the staggered type [6].

In amorphous silicon devices integrated circuit (a-SiDIC) laboratory at the University of Waterloo, the inverted staggered a-Si:H TFTs is fabricated using a five-mask process [7], [8]. As depicted in Figure 2.1, the fabrication process begins with the deposition of 100nm-Cr or Mo on the substrate to form the gate electrode of the device (Mask 1). The next step is the deposition of silicon nitride (SiN_x) as the gate insulator, a-Si:H as the active channel, and a second SiN_x film as the passivation layer in one vacuum-pump-

down cycle to minimize the density of defect states at the interfaces. Although other dielectric materials such as SiO_2 have been used, silicon nitride is by far the most recognized choice as the gate dielectric, giving a superior performance than that of other materials [9]. The three layers are deposited in a plasma enhanced chemical vapor deposition (PECVD) system with thicknesses of 250nm, 50nm, and 250nm for SiN_x, a-Si:H and SiN_x layers, respectively. Then, the passivation SiN_x is patterned using mask 2 to define the source and drain regions. Next, a 300nm heavily-doped nano-crystalline (n^+ nc-Si:H) layer and a 250nm passivation silicon nitride film are deposited, and patterned with mask 3. Consequently, the mask 4 is employed to open the contact windows at the source and drain doped layer through the second SiNx passivation layer. Finally, the aluminum layer is deposited and patterned to form the contact metal pads.

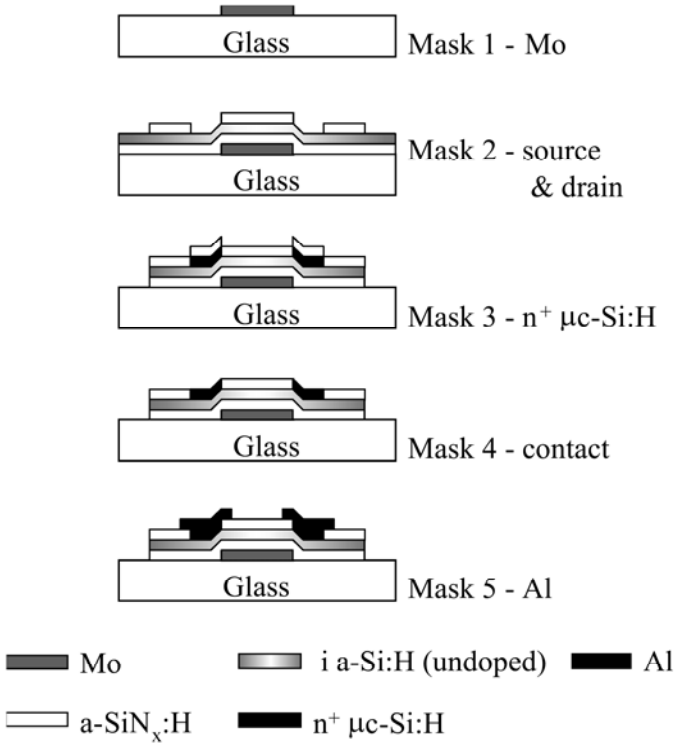

Figure 2.1: Fabrication sequence of an inverted staggered TFT (adapted from [7], [8]).

The transistor current-voltage characteristics of a device fabricated in the a-SiDIC laboratory are displayed in Figure 2.2. The TFT demonstrates an ON/OFF current ratio of around 10^8, a good saturating behavior at the high drain voltages, and a low leakage current of ~10 fA at the drain-source voltage of -5V [10], [11]. No evidence of the current crowding at low drain-source voltages (V_{DS}) indicates the good contact properties achieved through the application of the highly conductive n+ nc-Si:H source-drain contact layers.

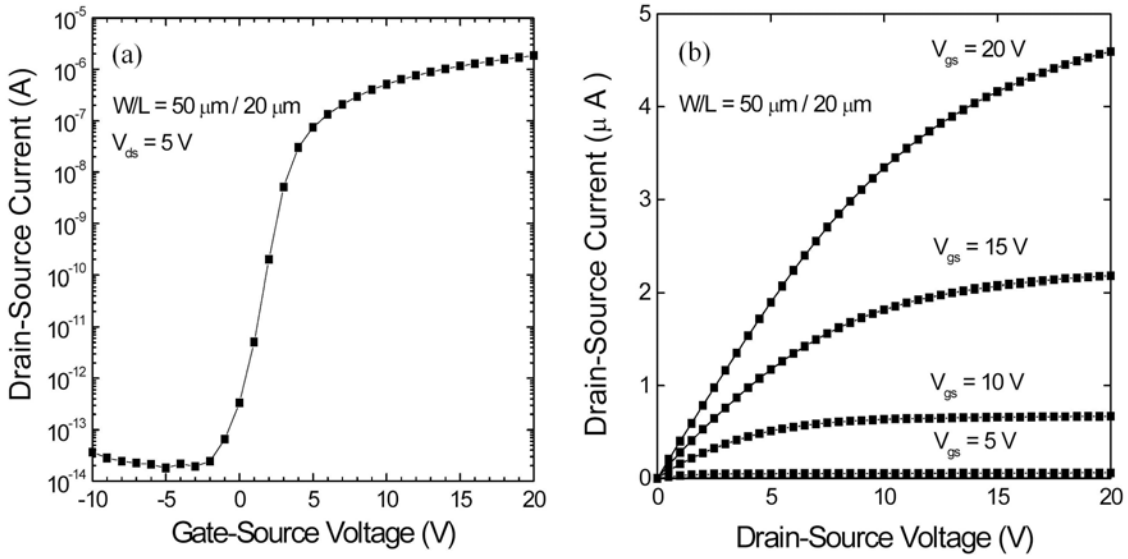

Figure 2.2: (a) Transfer and (b) output characteristics of a lateral TFT (adapted from [11]).

2.2 Motivation for VTFTs

VTFTs have the most appealing structure for high quality active matrix arrays due to the inherent short channel length of the transistor and the small area of the device. The ever-growing high quality panels require TFTs with dimensions as small as possible to preserve the aperture ratio or the fill factor. For example, in imagers, the pixel fill factor,

which represents the percentage of the photosensitive area to the entire pixel area, is a critical parameter that determines the image brightness, contrast ratio, dynamic range, and other factors of a high-quality image [12]. Although scaling the TFT size is possible, the reduction in the channel length and other dimensions of the conventional TFT is not possible without employing the expensive nano-lithography process. Therefore, for high resolution imaging or display applications, wherein an adequate fill factor must be preserved despite the pixel scaling or high-density TFT integration, an alternative TFT configuration is required in which the dimensions of the TFT is not limited by the fabrication issues associated with lithography or etching [13].

The most promising configuration of the TFT is the vertical structure where the channel length is defined independent of photolithographic patterning. Consequently, sub-micron channel-length VTFT is easily achieved without the need for a critical lithography process. In VTFTs, the channel length is defined by an intermediate dielectric layer, placed between the source and drain contact layers. Therefore, the channel length is accurately reduced down to sub-micron scales by controlling only the thickness of the intermediate dielectric layer.

The device structures for conventional inverted staggered TFTs and VTFTs are provided in Figure 2.3. From this figure, it can be concluded that a significant reduction in the device area can be obtained with the vertical TFT structure, since it does not spread laterally. Although the lateral TFT structure currently meets performance requirements, the device consumes a considerable portion of the pixel area, undermining the fill factor. For example, in digital mammography that requires a small pixel size to satisfy the spatial resolution requirement [14], the fill factor is reduced to 37% for the 50-μm pixel

pitch (*Lp*) arrays, with a lateral TFT area of 20 × 15 μm^2 (*L* × *W*) and photoactive size (L_a) of 35 μm based on the 5-μm lithography process according to:

$$f = \frac{L_a^{\,2} - (L \times W)}{L_p^{\,2}}. \tag{2.1}$$

By employing VTFT with an area of 5 × 5 μm^2 for the same pixel pitch, the fill factor increases to 48%. Moreover, it is possible to hide the VTFT under the signal lines to further boost the fill factor or aperture ratio. In Chapter 7, this architecture, which is used in the pixel drivers of an AMOLED display array, is explained.

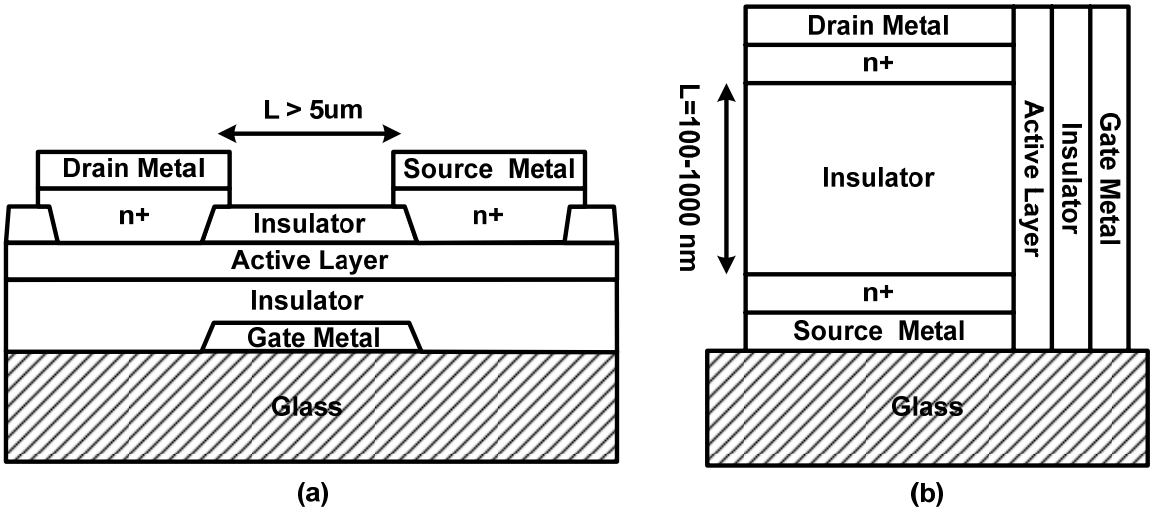

Figure 2.3: Schematic cross section of the (a) lateral and (b) vertical TFT.

Low operational speed and low drive current are the other concerns of the present a-Si:H TFTs due to the low field effect mobility of the amorphous silicon. For instance, in AMOLED displays, the OLED emits light that is proportional to the passing current. Application of a high mobility poly-Si material seems to be a straightforward approach to increase the drive current and switching speed of TFTs. However, the fabrication of poly-Si TFTs usually requires extra processing steps such as excimer laser annealing (ELA) for crystallization of the deposited a-Si:H material that adds to the cost and complexity of

the production [15]. High leakage current and poor uniformity of the device characteristics are the other concerns involving the poly-Si TFTs that usually lower the throughput of the production line [16].

To attain a satisfactory speed, the transit time of the electrons across the channel of the TFT should be decreased. Scaling down the channel length (L) is an effective way to increase the switching speed of the TFT, since the time delay (t_d) of the TFT response to the input signal is proportional to L^2, expressed as follows [17]:

$$t_d \propto \frac{L^2}{\mu_{eff}} \tag{2.2}$$

Here, μ_{eff} is the mobility of the electron in the active layer. Therefore, VTFTs can achieve a fast switching speed, since the channel length can be easily reduced to the nano-scale regime.

Furthermore, to increase the ON current of the transistors in both the linear and saturation regions, reducing the channel length is effective according to the following [3]:

$$I_{DS} = \frac{W}{L}\mu_{eff}C_i\left[(V_{GS}-V_{Th})V_{DS}-\frac{1}{2}{V_{DS}}^2\right] \qquad V_{DS} < V_{GS}-V_{Th} \tag{2.3}$$

$$I_{Ds} = \frac{1}{2}\frac{W}{L}\mu_{eff}C_i\left(V_{GS}-V_{Th}\right)^2 \qquad V_{DS} \geq V_{GS}-V_{Th} \tag{2.4}$$

In the previous equations, W, C_i, V_{th}, $V_{GS,}$ and V_{DS} represent the channel width, gate capacitance, threshold voltage, gate-source voltage, and drain-source voltage, respectively.

Finally, the immediate benefit of this short channel, minimal size, and self-aligned structure, is the very low overlap gate capacitances. Consequently, a short turn-on time for the TFT and a read-out time for the signal detection are achieved [18].

2.3 Early Works on VTFTs

In 1984, the first vertical-type hydrogenated amorphous silicon (a-Si:H) VTFT was fabricated [19]. The channel length of the device was 1μm, and demonstrated promising results that drew attention to its application potential in AMLCDs [19] [20]. In this device, as shown in Figure 2.4 (a), the gate electrode is at the right-hand side and the source and drain electrodes are the upper and lower metals. The channel is formed vertically at the gate SiN_x/a-Si:H interface, the channel length being defined by the thickness of the SiN_x, separating the drain-source region. The rationale for this structure is to provide an easy way to reduce the channel length L to the sub-micron scale in order to increase the switching speed of a-Si:H TFTs inversely proportional to L^2, according to (2.2) [19].

A conventional TFT limits in the reduction of the channel length, not by the device physics, but by the added complexity of the photolithography process for delineating the source and drain. Instead, in the vertical structure, the channel length is defined by the film thickness, which is controlled by the precise timing of the deposition process [21], [22]. The literature discusses various transistor topologies for VTFT, as seen in Figure 2.4; however, most of the designs are still in the experimental stage and are not defined as a standard VTFT process. The physical properties and electrical characteristics of these devices are summarized in Table 2.1 [22] - [26].

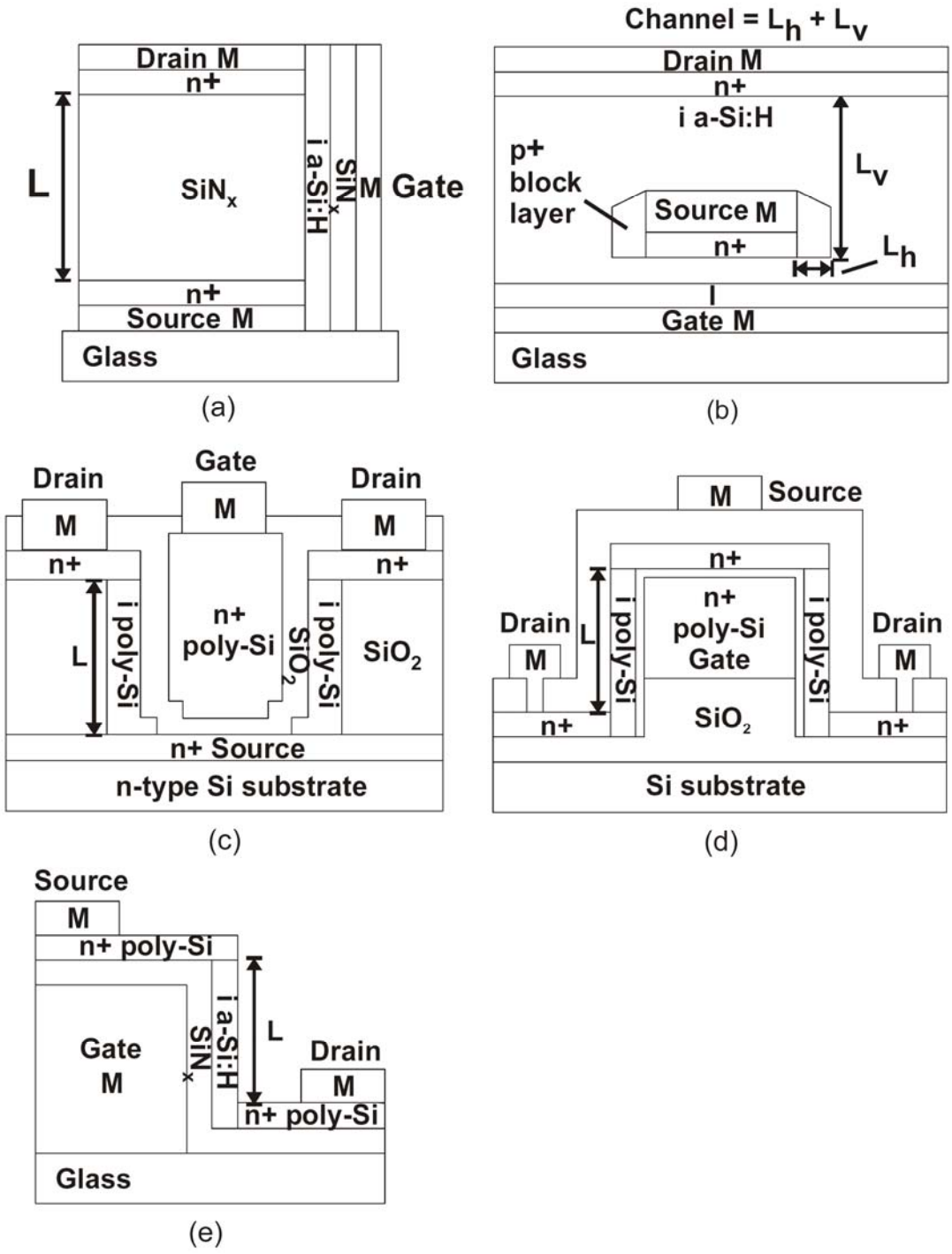

Figure 2.4: Different topologies of the VTFT structure (adapted from [22] - [26]).

Table 2.1: Summary of the VTFT electrical and physical characteristics from literature [22]-[26].

TFT characteristics	Performance range	Comments
Channel Length (L)	0.5-1.5 μm	
W/L Ratio	14~1000	
ON/OFF Current ratio	10^4~10^5	At $V_D \approx 5$ V
Leakage Current (I_{OFF})	10^{-6}~10^{-10} A	At $V_D \approx 5$ V
Threshold Voltage (V_T)	1~3 V	At $V_D \approx 5$ V
Subthreshold Slope (S)	1.25-4 V/dec	
Propagation Delay (t_d)	95 ns/stage	From a 7-stage ring oscillator

The a-Si:H VTFT fabrication process, carried out in the a-SiDIC laboratory of University of Waterloo, includes five photolithography steps, initially developed by Dr. I. Chan [27]. The VTFTs are fabricated on a Corning 1737 glass substrate. The details of the fabrication process and issues related that will be addresses in the following sections.

2.4 Device Fabrication

The fabrication of the VTFT in the Giga-2-nano (G2n) laboratory is a five-mask process illustrated in Figure 2.5. First, a Cr layer with a thickness of 100nm is sputter deposited, followed by the deposition of n^+ nc-Si:H layer and SiN_x layer using PECVD with thicknesses of 300nm and 20nm, respectively. The last two layers are patterned in reactive ion etching (RIE) employing CF_4/H_2 gas mixture, then Cr is wet-etched to form the source metal (Mask 1). The next step is related to the reverse deposition of SiN_x/n^+

nc-Si:H/Cr by applying the same conditions as the first step. The thicknesses of these three layers are 500nm, 300nm, and 100nm, respectively. Again, the top Cr is patterned (Mask 2) and wet-etched to form the drain metal. Now the patterned Cr layer is used as a mask for the layers underneath. Another RIE is conducted for dry-etching of the n^+ nc-Si:H/SiN_x layers. This is the most critical step of the fabrication as defines the vertical sidewall of the device where channel lays. Any roughness or contamination, induced by the RIE etching process, deteriorates the VTFT performance.

The thickness of the intermediate nitride between the source and drain n^+ films defines the channel length. It is note worthy that the n^+ and SiN_x layers are self-aligned with the drain Cr. After this step, a-Si:H and SiN_x layers with thickness of 50nm and 250nm are deposited by PECVD in a single vacuum pump-down as the active and gate insulator layers, respectively. Then, Cr is deposited by sputtering, and patterned (Mask 3) as the gate metal and masking layer for the active and insulator films. The dry etch of these layers stops at the source and drain metal. Next, a SiN_x layer with a thickness of 250nm is deposited by PECVD to passivate the entire sample and patterned (Mask 4) to specify the contact vias. Lastly, to form the source, drain, and gate contact pads, a 1 μm Al layer is sputter deposited and patterned (Mask 5).

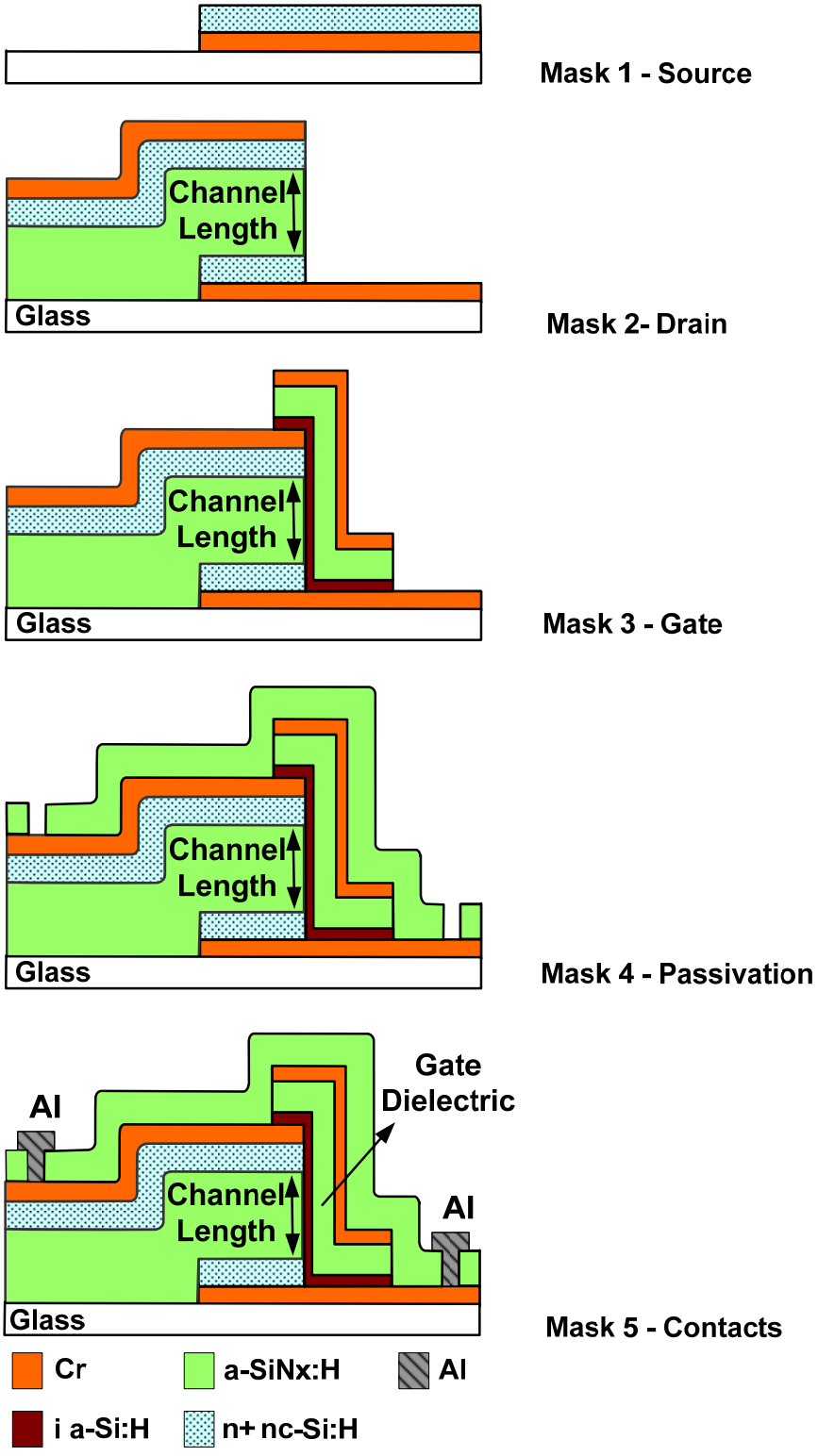

Figure 2.5: Fabrication sequence of the VTFT process (not to scale).

In the fabrication of the VTFT, the formation of the vertical sidewall is the most critical part of the process determining the performance of the device. The vertical sidewall formation and the related challenges are detailed in the following sections. Before that, PECVD, which is the principal deposition method in the fabrication of VTFT, is reviewed to give the reader a concise information on the deposition steps.

2.4.1 Deposition Techniques

In this work, PEVCD is used for the deposition of silicon-based materials such as intrinsic Si, n- and/or p-doped Si, silicon nitride, and silicon oxide films. For the deposition of the chromium and aluminium metals, RF sputtering is employed. A summary of the deposition techniques and conditions for the a-Si:H VTFT fabrication is presented in Table 2.2.

A variety of plasma-assisted deposition methods for Si-based thin films have been reported including radio-frequency (RF) PECVD, direct current (DC) PECVD, very high frequency (VHF) PECVD, and electron cyclotron resonance (ECR) CVD. Among them, the 13.56 MHz RF PECVD is the industrial standard and is used in this doctoral research for the fabrication of the VTFT.

Table 2.2: Summary of the deposition conditions for a-Si:H VTFT fabrication.

Film	Application	Deposition Technique	Deposition Conditions
a-Si:H	Active Layer	PECVD	20 sccm (SiH_4), 2 W, 400 mTorr, 300 °C, ~ 9 nm/min
n^+ nc-Si:H	Source and Drain	PECVD	$SiH_4/PH_3/H_2$ (1/1/250 sccm), 10 W, 1900 mTorr, 300 °C, ~1.5 nm /min
SiN_x	Gate Dielectric, Passivation Layer, Intermediate Dielectric Layer	PECVD	NH_3 / SiH_4 (100/5), 2W, 400 mTorr, 300 °C, ~10 nm/min
Cr	Source, Drain, and Gate Metal	RF Sputtering	Ar (30 sccm), 400 W, 5 mTorr, room temp.(22 °C), ~11 nm/min
Al	Contact Pads	RF Sputtering	Ar (30 sccm), 400 W, 5 mTorr, room temp. (22 °C), ~12 nm/min

The cluster multi-chamber PECVD/Sputtering system, manufactured by MVSystems Inc., is employed for the deposition of the various thin film semiconductor materials [28]. A schematic top-view of the PECVD cluster multi-chamber system and chamber layout are displayed in Figure 2.6. The reactor consists of a gas inlet, a deposition reactor, an RF power system, and a gas outlet. Two parallel-plate electrodes with a size of 6" × 6" are separated by a specified distance in the reactor, where the top electrode is grounded and the bottom one is RF powered. The system consists of four isolated chambers for the deposition of intrinsic Si film, n- and/or p-doped Si film, dielectric film, and ITO films to prevent any cross-contamination. Here, the deposition method for the ITO films is RF sputtering, and for all the other materials, is RF PECVD. The central chamber is used to

transfer the substrate between the deposition chambers, and the substrate is loaded and unloaded via a load lock by using a robotic arm that operates in vacuum.

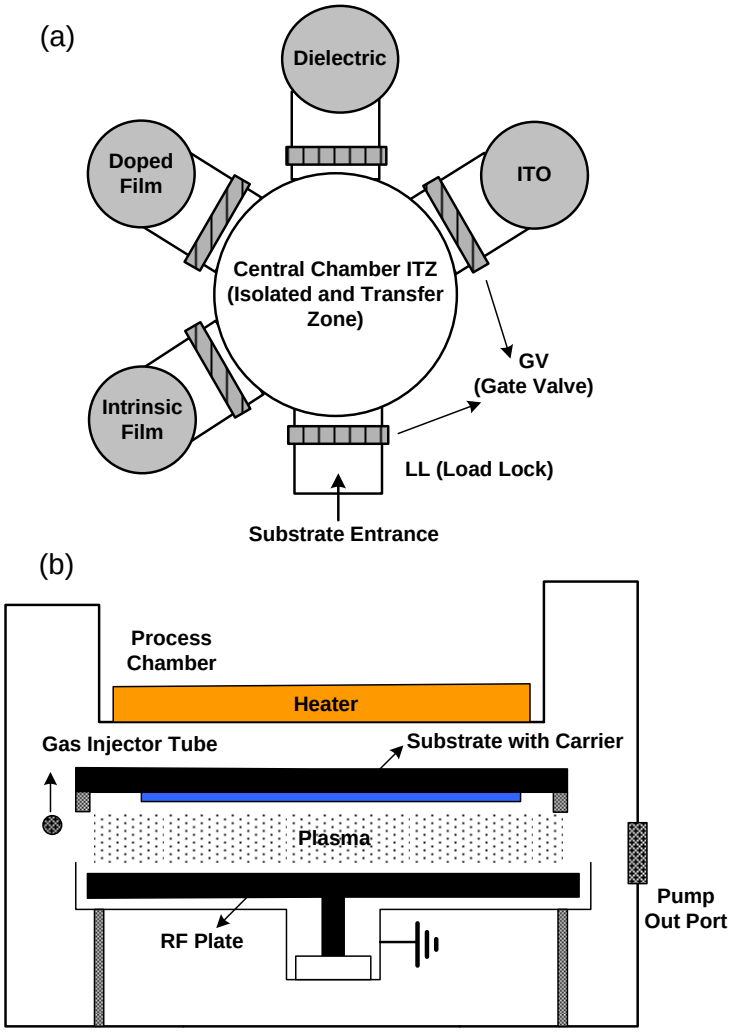

Figure 2.6: (a) MVS cluster PECVD equipment and (b) the chamber configuration.

The pumping system is composed of the combination of a corrosion resistant turbo-molecular pump and a rotary vane pump. Prior to deposition, the background vacuum is kept at a base pressure below 10^{-7} Torr. The samples are placed on the ground electrode, and the substrate temperature is controlled by a resistive heater. The plasma is created between the two electrodes in the reactor, when the RF power is applied. The flow of each gas and the chamber pressure are set by the mass flow controllers and a controllable

throttle valve, respectively. For the silicon-based materials, SiH_4 is used as the main source gas. The electrical and physical characteristics of the deposited film are dependent on the deposition conditions such as gas pressure, gas flow rate, deposition temperature, and RF power density.

2.4.2 Etching Techniques

The goal of any etch process is to reproduce the image of a mask with a high degree of integrity. The characteristics of the etching process can be either isotropic or anisotropic. In an isotropic etching, the etch proceeds at the same rate for each direction, creating an undercut, equal to the film thickness beneath the mask. In anisotropic etching, the horizontal etch component is very small, resulting in a faithful pattern transfer, observed in Figure 2.7.

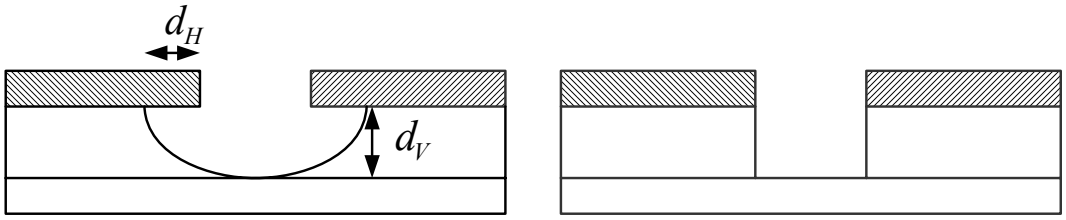

Figure 2.7: (a) Isotropic and (b) anisotropic etching pattern.

The degree of isotropic etching (IE) and anisotropic etching (AE) is defined as:

$$IE = \frac{d_H}{d_V} \tag{2.5}$$

and

$$AE = 1 - IE = \frac{(d_V - d_H)}{d_V} \tag{2.6}$$

where, d_H and d_V are the lateral and vertical etch rate, respectively. For the completely isotropic etching, $d_H = d_V$ which translates into $IE = 0.5$, and for a fully anisotropic etching, $d_H = 0$ or $AE = 1$.

Typically wet etching processes result in an isotropic profile of etching with some exceptions in the etching of crystalline materials where the etch rate depends on the crystalline orientation. However, in dry etching, it is possible to achieve anisotropic etching, since the etching can proceed by both physical sputtering and ion-assisted mechanisms. In the fabrication of the VTFT, RIE is used for the anisotropic etching of the Si-based layers. The summary of the etching conditions for the fabrication of the VTFTs is shown in Table 2.3.

Table 2.3: Summary of the etching conditions in VTFT fabrication.

Film	Application	Etching Technique	Etching Conditions
a-Si:H	Active Layer	RIE	CF_4 (20 sccm), Pr 10 mT, RIE 60W
n^+ nc-Si:H	Source and Drain	RIE	CF_4/H_2 (17/3 sccm), Pr 10 mT, RIE 100W
SiN_x	Gate Dielectric, Passivation Layer,	RIE	CF_4/H_2 (17/3 sccm), Pr 10 mT, RIE 100W
Cr	Source, Darin, and Gate Metal	Wet	$(NH_4)_2Ce(NO_3)_6$: 120g, CH_3COOH: 100 cc, H_2O: 500cc, 40°C, etch rate: ~40nm/min
Al	Contacts	Wet	H_3PO4: 465cc, CH3COOH: 36cc, HNO_3: 18cc, H_2O: 90cc, 30°C, etch rate: ~40nm/min

2.4.2.1 Anisotropic Dry Etching

Dry etching employs an electrically generated plasma environment, consisting of energetic gas molecules, ions, and/or free radicals to remove the surface material from the wafer [29]. The term commonly applies to the following processes [29]:

- Plasma etching
- Reactive ion etching
- Ion milling
- Sputter etching

Reactive ion etching is based on a combination of the chemical activities of the reactive species, generated in the plasma, and the physical effects, caused by the ion bombardment. The impinging ions damage the surface, thereby increasing its reactivity. The primary processes, occurring in RIE can be summarized as follows:

- Active species generation
- Transport of plasma-generated reactant from the bulk of the plasma to the surface of the material being etched
- Adsorption step
- Reaction step
- Desorption of the volatile reaction products
- Pump-out of the volatile reaction products

In the fabrication of the VTFT, the formation of a vertical sidewall on the drain-source structure, consisting of a Cr/n^+ nc-Si:H/SiN_x/n^+ nc-Si:H/Cr multilayer, is the most critical step. The requirement for a vertical sidewall implies a precise self-alignment of the top Cr layer and the n^+/SiN_x/n^+ trilayer. This self-alignment can be accomplished by reactive

ion etching of the trilayer using a wet etch patterned Cr layer as a masking layer. However, because of the different material composition of the n^+ and SiN_x layers, any lateral etching of the stacked layers (given the unequal etch rates) leads to film misalignment, giving rise to a sidewall with zig-zag profile. This outcome can undermine the integrity of the subsequent channel layers deposited on the sidewall.

Figure 2.8 (a) is a cross-section SEM image of the fabricated device using a non-optimized dry etching process. It is evident that the channel profile is not vertical, a problem that arises because of the undercutting on the top part of the channel during the RIE etching. The channel lies on a slanted sidewall with a portion of the drain metal hanging over the channel. Because of the shadowing effect of the overhanging drain metal, the flux of the gate metal is possibly blocked from reaching the upper part of the channel region during the deposition process.

Hence, a high gate voltage is needed to enhance the conduction in the un-gated region. This part of the channel behaves as a high-resistance region between the n^+ drain and the gated channel (Figure 2.8 (b)). This issue causes poor subthreshold characteristics and a low ON current of the transistor [30],[31].

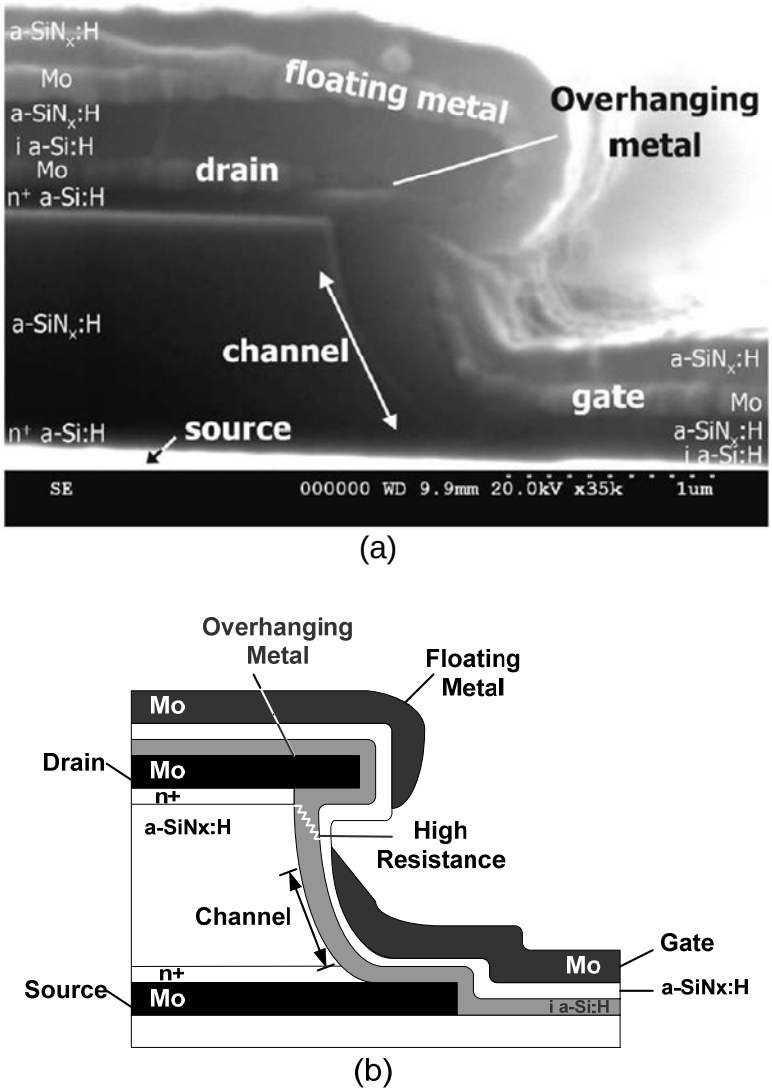

Figure 2.8: (a) Cross-sectional SEM image of the fabricated VTFT and (b) schematic cross-section of the device showing the parasitic resistance near the drain contact (adapted from [27]).

Therefore, the development of a dry-etching process for $n^+/SiN_x/n^+$ trilayer that can provide a high degree of anisotropic etching is critical for the fabrication of the VTFT [21]. In this work, a gas mixture of CF_4/H_2 is used to form the vertical sidewall of the channel. Fluorocarbon molecules in the ground state are inert towards the silicon, silicon oxide, and silicon nitride surfaces [32]. Etching starts only after the reaction gas has been

dissociated to ions in the plasma environment. The subsequent etching of Si in CF_4 plasma can be described according to the following chemical processes:

$$CF_4 \rightarrow 2F + CF_2 \tag{2.7}$$

$$Si + 4F \rightarrow SiF_4 \tag{2.8}$$

$$Si + 2CF_2 \rightarrow SiF_4 + 2C \tag{2.9}$$

Typically, only the atomic fluorine and difluorocarbene react with silicon to form silicon tetrafluoride as a volatile product.

Even when there is no ion bombardment, the atomic fluorine reacts easily with silicon [32]. The reaction between the fluorine atoms and silicon is highly exothermic (negative heat of reaction) generating volatile products at room temperature. The ion bombardment increases the reaction rate between F and Si only slightly, therefore does not significantly affect the characteristics of the process. This is the reason behind the isotropical etching of silicon in most fluorine-based plasma systems.

The role of H_2 in CF_4 is to reduce the concentration of F atoms by forming HF, according to the following reactions:

$$H_2 \rightarrow 2H \tag{2.10}$$

$$H + F \rightarrow HF \tag{2.11}$$

These HF gas molecules are not reactive in a high vacuum environment. The experimental results also demonstrate that adding H_2 to a CF_4 glow discharge lowers the Si etch rate [33]. Fluorocarbon species are strongly chemisorbed on silicon surfaces, but react only slowly without ion bombardment. Consequently, the addition of hydrogen to the gasses reduces the density of the discharge fluorine ions and suppresses the plasma etching in favor of fluorocarbon polymerization as the F/C ratio drops,

$$nCF_2 \rightarrow [CF_2]_n \tag{2.12}$$

However, constant ion bombardment on the bottom surface sputters the polymer material from the surface of the material, which allows the etching to proceed in the vertical direction. The sidewalls, though, are not subjected to the ion bombardment and polymerization occurs on their surface, inhibiting further lateral etching [30], [34].

At high flux density and energy level, the impinging ions damage the surface layers and provide the possibility for reaction of the adsorbed fluorocarbon species with the substrate. If the substrate is silicon oxide, oxygen is available to form volatile carbon oxide with fluorocarbon compounds. Simultaneous to this chemical reaction, F is released to remove the Si atoms [32] as follows:

$$SiO_2 + 2CF_2 \rightarrow SiF_4 + 2CO \tag{2.13}$$

A similar mechanism is not available for silicon, and a carbon-rich film, called an inhibitor polymer, is formed on the sidewall, based on (2.12). The low sputter yield of the carbon materials then suppresses further Si removal. The characteristic of silicon nitride etching is between that of silicon and of silicon oxide [34]. Silicon nitride reacts faster with fluorine ions than oxide does due to the Si-N bonds being weaker than the Si-O bonds. Moreover, it is proposed that the silicon nitride reacts with the CF_2 species, since it is etched in CF_4/H_2 at approximately the same rates of silicon oxide. This suggests the surface carbon may be removed as CN in analogy with equation (2.13).

Figure 2.9 demonstrates a good alignment of the drain metal with the trilayer in CF_4/H_2 (18%) gas mixture. Although this CF_4/H_2 gas mixture can provide a vertical channel profile, an immediate concern is the potential effects of the inhibitor polymer on the device performance. This polymer might physically hinder the electrical contact between

the n^+ and the intrinsic a-Si:H layer. In addition, the polymer might act as a defect creation site at the back interface between the intrinsic a-Si:H and the sidewall of the trilayer, which can, in turn, lead to an increase in the leakage current of the TFT [27]. Therefore, it is necessary to remove this polymer film formed on the vertical sidewall of the sample. One possible approach is to immerse the wafer in a photoresist stripper solution with an ultrasonic activation to mechanically remove this polymer, followed by the exposure of the sample to an oxygen plasma.

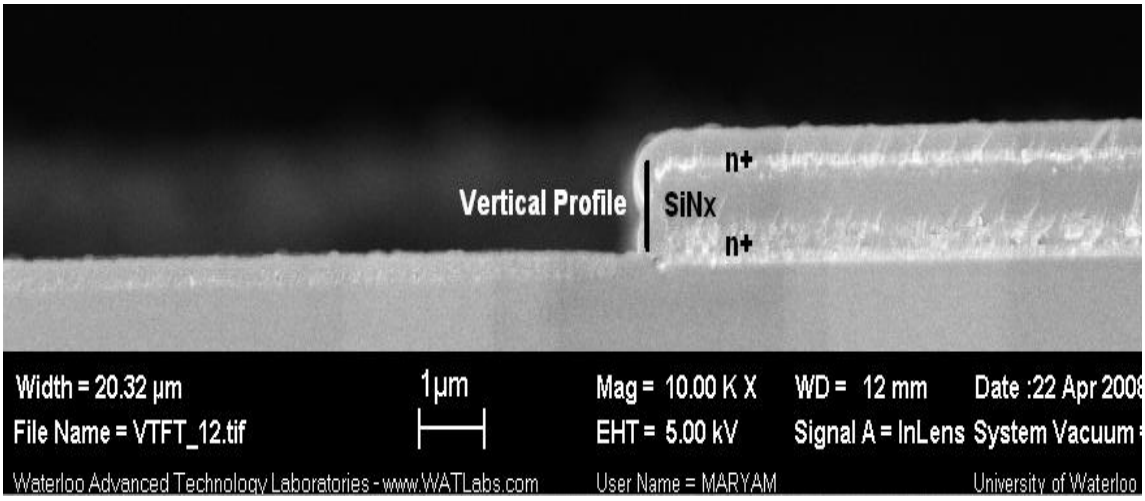

Figure 2.9: $n^+/SiN_x/n^+$ trilayer profile obtained after RIE etching by using CF_4/H_2 gas mixture and polymer removal process.

2.4.2.2 Masking Materials

During the dry etching of the n^+ /SiN / n^+ trilayer, it is crucial to choose a mask material that has no influence on the plasma chemistry and the etch result. The mask should be deposited without complicating the fabrication process. For instance, photoresist (PR) is the most common mask for patterning. However, the PR/Si selectivity is not high enough due to the presence of the fluorine and oxygen content in the plasma, which can react to

the carbon content of the PR. Moreover, during the etching of the Si, PR can be sputtered and redeposited on the silicon, where it's not protected with the mask. This phenomenon gives rise to the formation of the nano-pillar on the silicon surface. Figure 2.10 is the SEM image of the 500nm silicon nitride step structure with PR as the mask. It is evident that, the development of the fully vertical sidewall has failed by virtue of the nano-pillar formation.

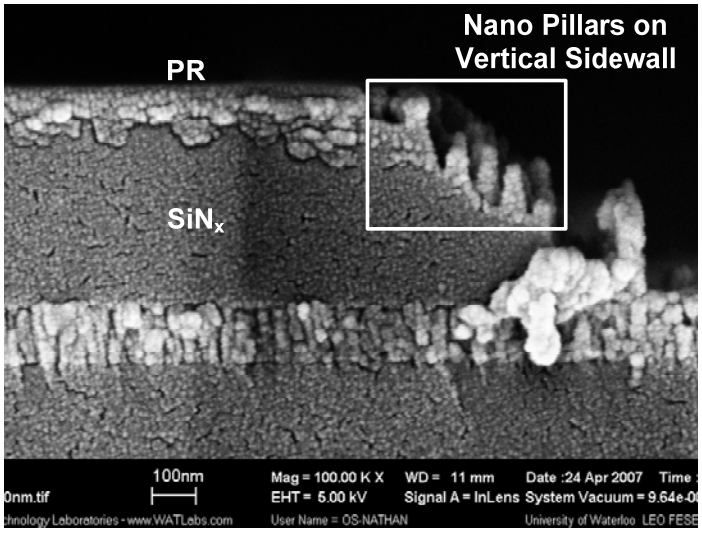

Figure 2.10: SEM image of the slanted sidewall and the generated nano-pillar on its surface in the RIE etching of SiN_x using a PR mask.

Any metal can also be used as the mask, and at the same time, serve as the drain metal contact. However, the mask erosion is an undesirable phenomenon that deteriorates the etching profile. In general, if the mask is retarded or etched during the process, the trench profile is influenced and the result is not fully vertical. Figure 2.11 shows the slanted sidewall of the a-Si:H with a height of 500nm, when Al is used as the mask. Al is an IC compatible metal; however, even impinging ions with a low energy (40eV) can attack the mask by means of sputtering the material. This effect roughens or etches the Si adjacent

to the A1 protected regions [35]. The erosion may be explained by the existence of eddy currents in aluminum [35].

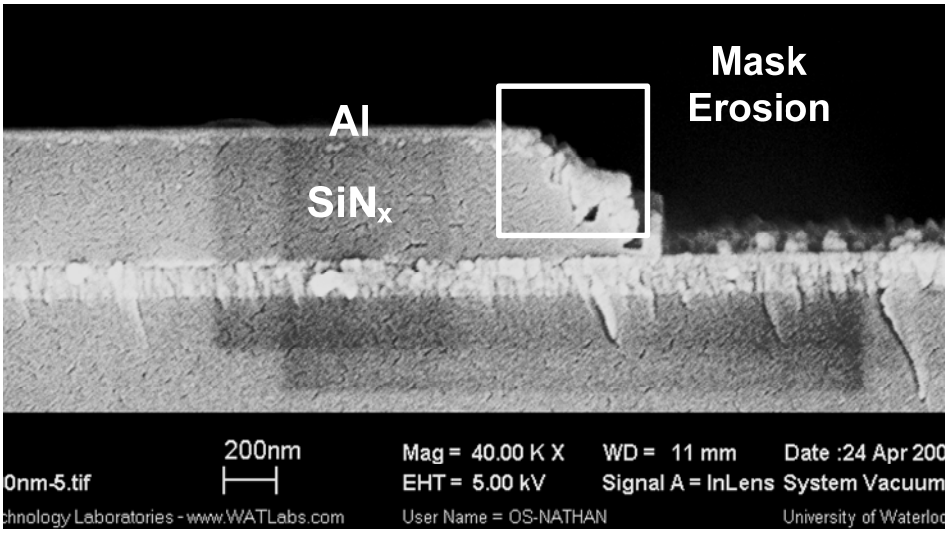

Figure 2.11: SEM image of the slanted sidewall due to the mask erosion in RIE.

Among the different metals, Cr is an appropriate choice for the masking purpose in RIE processes. A 10 nm Cr layer as a mask is enough to etch over 400μm height of the Si, because of its low physical sputtering and low volatility of the fluoride compounds [35]. It is reported that Cr is not sputtered even at ion energies as high as 200eV. Figure 2.9 demonstrates that Cr is an appropriate masking material in the fabrication of VTFTs.

2.4.3 Thin Film Step Coverage

The step coverage of the active layer, gate dielectric, and the gate metal is the next critical issue in determining the device performance and success of the VTFT fabrication. Although the deposition process parameters have been optimized for lateral electronic devices, the plasma kinetics responsible for the step coverage of those films on a topographical surface are not well understood. To develop a clear understanding of thin

film step coverage, a new study on the material deposition for VTFT fabrication is required.

Sputter deposition for metal films is a physical vapor deposition (PVD) technique. The directionality of the metal atoms from the metal target to the substrate surface, the surface diffusivity of the physiosorbed metal atoms, and the substrate step angels, all determine the step coverage of the deposited metal [34]. In sputter deposition, because of the directionality of the incident atoms, the number of atoms arriving at the horizontal surface is more than those reaching the vertical surface. In fact, there are more possible angles for the incident atoms to reach the horizontal surface than the vertical surface (Figure 2.12); therefore, the metal film thickness should follow the same scale on these surfaces.

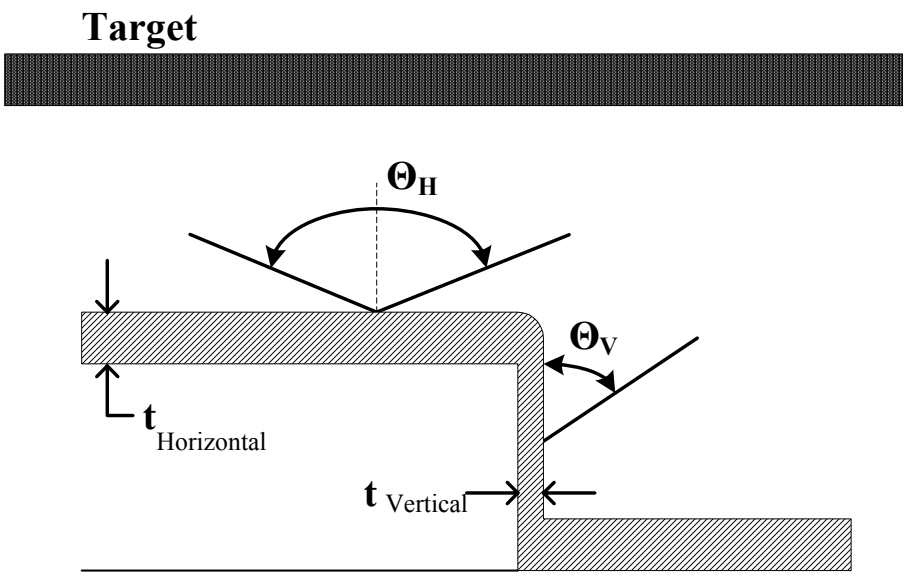

Figure 2.12: Schematic illustrating the possible arriving angles for metal atom flux and the film coverage on a horizontal and a vertical surface.

Figure 2.13 reflects the step coverage of the Cr film on the vertical sidewall. The SEM results confirm that the Cr thickness on the vertical sidewall is half of that on the horizontal surface.

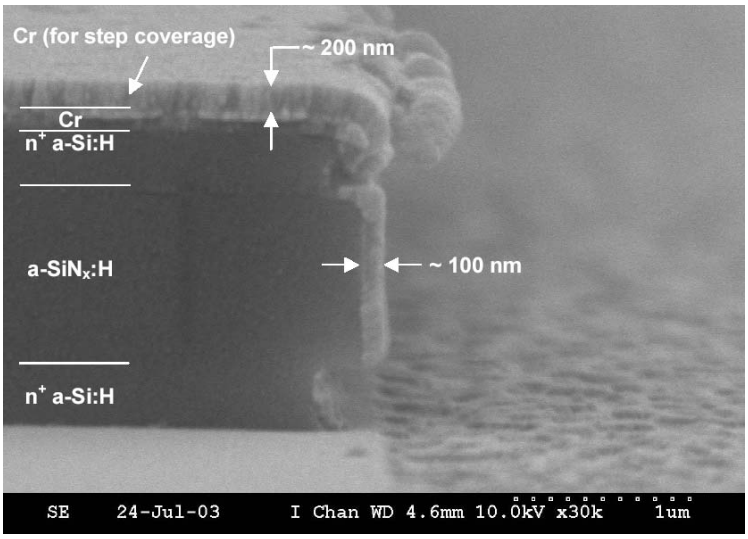

Figure 2.13: Step coverage of sputter-deposited Cr metal film [27].

PECVD is the typical deposition technique for a-Si:H and SiN_x films. Despite the common belief that PECVD films have the property of a conformal step coverage (deposited film thickness on the vertical surface equals that on the horizontal surface), it is not true in practice. For instance, in the PECVD deposition of a-Si:H film, previous studies [27] have shown that ion bombardment enhances the film growth rate by turning more passivated silicon surface sites (no silicon dangling bond) into activated sites (at least one silicon dangling bond) to adsorb more gas-phase SiH_3 radicals from the glow discharge of the SiH_4 gas [27]. The SEM image in Figure 2.14 demonstrates that the conformality of the step coverage for PECVD films is similar to that of sputter-deposited films [27]. The thicknesses of the PECVD and sputter-deposited films on the vertical sidewall are approximately half of those on the horizontal surface, verifying the step

coverage behavior governed by the plasma kinetics. This aspect must be taken into account in the VTFT process design for the intended film thickness on the sidewall.

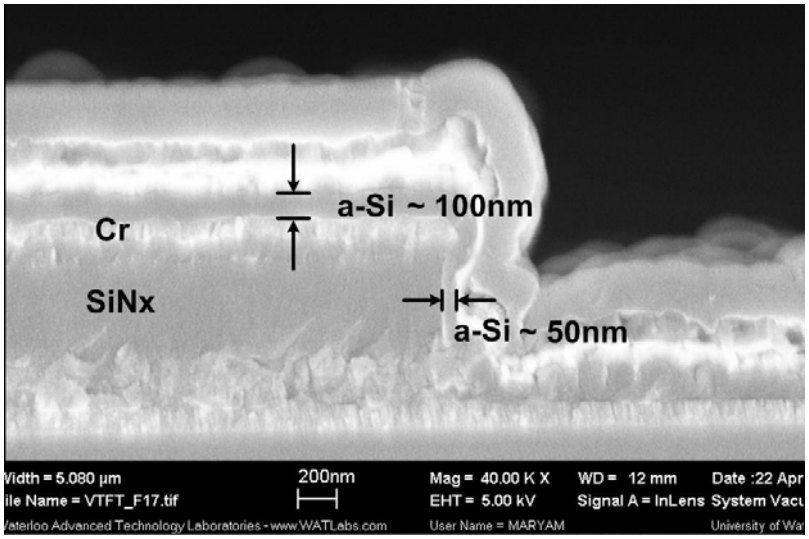

Figure 2.14: Step coverage of the PECVD-deposited a-Si:H film.

2.5 Preliminary Results

Prior to measurement, the fabricated VTFTs were annealed at 150-170 °C for 2 hours in a nitrogen ambient to improve the contact properties [36], [37]. The current-voltage measurements of the VTFTs were performed at room temperature using a Keithley 4200 semiconductor characterization system.

The transfer characteristics of an a-Si:H VTFT with a W/L ratio of 31/0.1 (µm) for different drain voltages are shown in Figure 2.15. The ON/OFF current ratio of this device is approximately 10^6, and the leakage current is in the order of 0.1 pA at a gate voltage of -5V. The subthreshold slope is approximately 2 V/dec at low drain voltages; thus a high gate voltage is required to turn on the device. It is noticeable that the ON/OFF current ratio is lower at the higher drain voltages due to a rapid increase of the device

OFF current. The high drain electric field, caused by the drain voltage, is deemed to be responsible for the observed behavior of this short channel transistor [38].

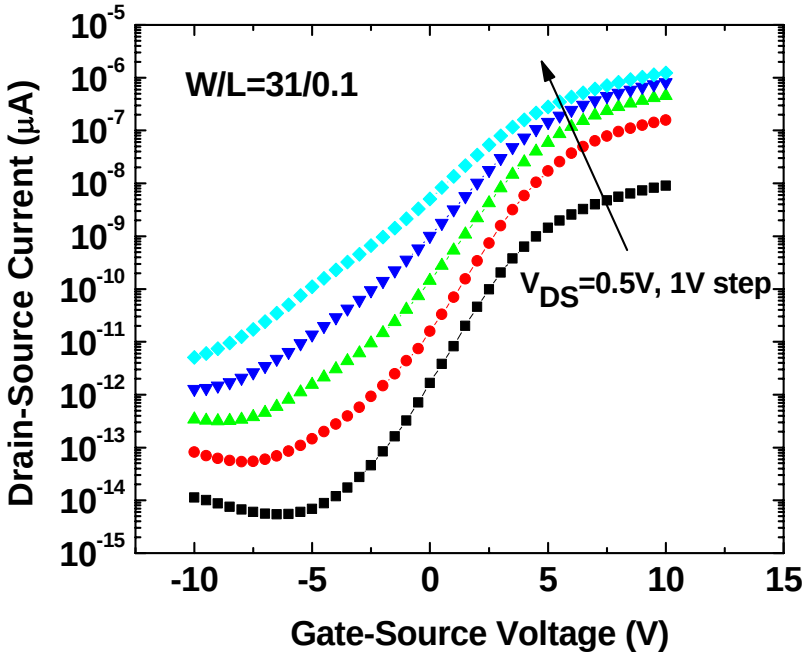

Figure 2.15: Transfer characteristics of the a-Si:H VTFT with 0.1μm channel length at different drain voltages.

The VTFT output characteristics of the fabricated VTFT are plotted in Figure 2.16 at the different gate voltages. The graph demonstrates very low output currents in the small drain voltages and non-saturating behavior with increasing drain voltage. This non-saturating behavior of the I_{DS}-V_{DS} characteristics, which is evident in Figure 2.16, is historically the first short channel effect studied in small channel transistors [39].

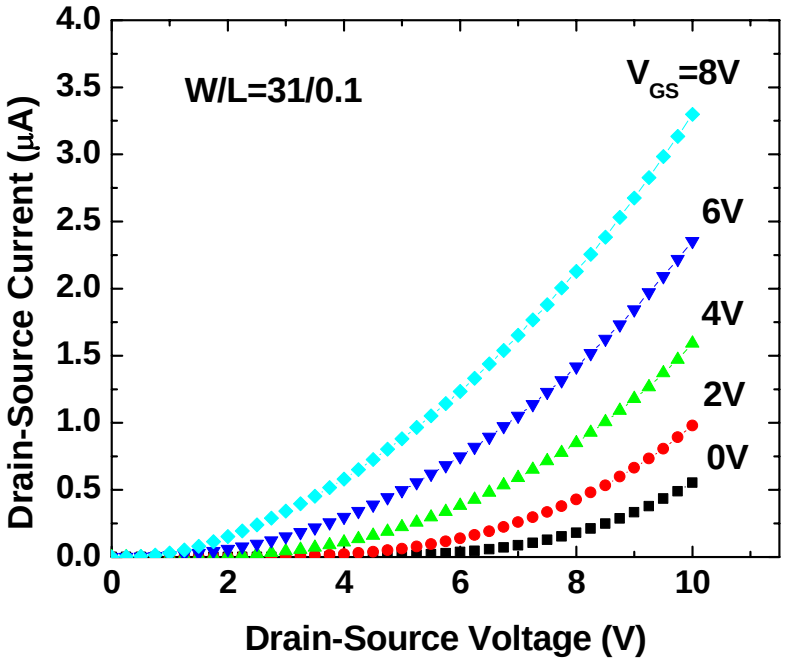

Figure 2.16: I_{DS} - V_{DS} characteristics of the a-Si:H VTFT with 0.1μm channel length at different gate voltages.

The high contact resistance and aggressive short channel effect are easily observed in the transfer and output characteristics of the VTFT. To study these effects, the electron transport mechanisms in the a-Si:H VTFTs with channel lengths below 1 μm are reviewed.

2.6 Short Channel Effects

The short channel effects are the deviation of the device characteristics from normal transistor behavior when the channel length of transistor is scaled. These adversities are the consequence of the dramatic enhancement of the transverse electric field along the channel. When the source and drain regions are sufficiently apart, the electric field in the active region is mainly generated by the gate; therefore it is perpendicular to the surface

of the channel. Under this condition, a one-dimensional analysis, called the gradual-channel approximation, can accurately predict the device characteristics [39]. When the channel length shrinks, the electric field can no longer be assumed unidirectional, and has a comparable component transverse to the gate dielectric/active region interface. The later portion of the electric field is responsible for most of the short channel effects [39]. Since the channel length of the VTFT is in the nanometer scale, the VTFT is considered as a short channel device. Three possible sources of the short channel effects, graphically depicted in Figure 2.17, are considered for VTFTs [27]:

1- Back gate effect (BGE)

2- Space charge limited current (SCLC)

3- Drain induced barrier lowering (DIBL)

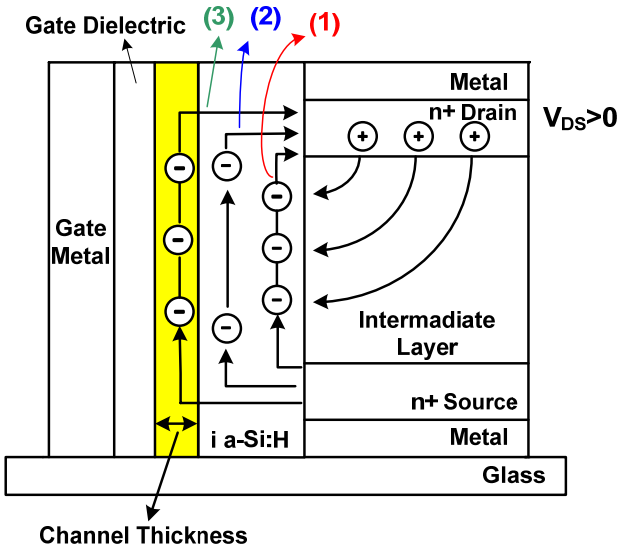

Figure 2.17: Short channel effect in VTFTs (1) Back gate effect (2) Space charge limited current and (3) Drain induced barrier lowering.

2.6.1 Back Gate Effect (BGE)

Because of the VTFT structure, the drain electric field can penetrate the back interface of the active region by capacitive coupling through the intermediate dielectric. This phenomenon causes electron accumulation in the vicinity of the drain region and improves the current conduction from drain to source through the back interface at high drain biases. Although this current is negligible in the above threshold region and in TFTs with long channel lengths, it is a dominant mechanism in the OFF state of the short channel VTFT [40].

2.6.2 Space Charge Limited Current (SCLC)

The SCLC, mechanism 2 in Figure 2.17, stems from the conduction of the injected charge carriers (electrons) from the n^+ regions into the bulk of an intrinsic (i a-Si:H) semiconductor [41]. Under a high transverse electric field, these injected carriers can be collected at the drain terminal, contributing to the leakage current. This current component is negligible in long channel lateral TFTs, since the electric field from drain to source is too weak to generate a significant current unless the drain voltage is very high. However, it cannot be ignored in short channel VTFTs, because the electric field becomes significant [42]. This is similar to the punch-through condition in the short channel crystalline Si (c-Si) MOSFET, in which the source and drain depletion widths merge and the conduction mechanism becomes dominated by the SCLC with a V_D^2 dependence [42]. Since this component of the leakage current is a bulk effect, the gate bias cannot effectively control the SCLC, and the suggested solution is to reduce the active-layer thickness of the device [43].

2.6.3 Drain Induced Barrier Lowering (DIBL)

The other consequence of shortening the channel length is DIBL. This phenomenon is used to describe the effect of the drain potential on the energy barrier that carriers encounter when traveling through the channel. In the long channel, the drain bias does not affect the source to channel potential barrier [44] and only the gate bias affects this potential barrier. However, in short channel devices, as the drain bias is raised, the conduction band edge in the drain is pulled down and the source-channel potential barrier is lowered [44]; that is, for $V_{DS} > 0$, the field lines penetrate from drain to source, thereby lowering the potential barrier for the current conduction, as illustrated in Figure 2.18 [45]. Once the source channel barrier is lowered by DIBL, the drain current is significantly influenced by the drain voltage.

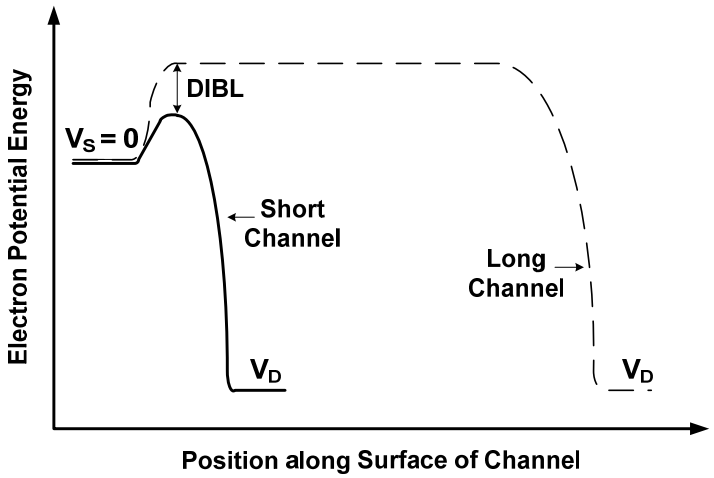

Figure 2.18: DIBL in MOSFETs; potential distribution along the channel for a long and short channel device (adapted from [44]).

One practical approach to minimize the short channel effects is to maintain the long channel behavior by simply reducing all the dimensions and applied voltages by a scaling factor α (α >1) (Figure 2.19). Therefore, the internal electric fields remain the same as

those of the long channel transistors, and the device characteristics kept reasonably unchanged [46].

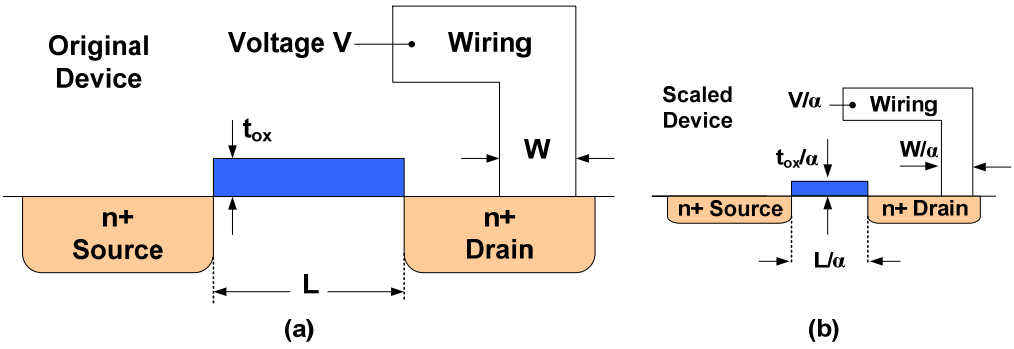

Figure 2.19: Principle of scaling for MOS transistors and integrated circuits (adapted from [47]).

The most effective and also challenging part of this approach is to reduce the gate dielectric thickness [39], [47]. Although scaling the channel length tends to deteriorate the short channel effects, decreasing the gate dielectric thickness alleviates the adverse effects [39]. The rational behind this approach is to enhance the gate control over the channel charge [39].

2.7 Summary

In this chapter the motivation for the application of VTFTs is detailed. The immediate benefits of this structure are the inherently small size and short channel characteristics of this device. The VTFT is well suited for the high-resolution large area electronics providing display or imaging equipment with a high fill factor or a high aperture ratio. Moreover, due to the short channel length of the device, the electron transit time is reduced, offering a high switching speed and high driving currents. However, despite the

aforementioned advantages of the VTFT, the short channel effects undermine the performance of the device.

The details of the vertical thin film transistors fabrication are then reported. In the five-mask process, the main challenge is the formation of the vertical sidewall of the device structure. The optimization of the RIE process and choosing the proper masking material are two critical issues determining the profile of the vertical sidewall. The combination of CF_4/H_2 (18%) is used for the anisotropic etching of the trilayer with a 100nm Cr layer serving as the mask. During the RIE process, an inhibitor polymer layer is formed on the sidewall that prevents the etching from proceeding laterally. After this etching step, the inhibitor layer must be removed to reduce the contact resistance between the n+ contact layer and the active layer of the transistor. Finally, the step coverage of the sputtered gate metal and PECVD deposited dielectric/active layer on the vertical sidewall of the device are investigated.

Finaly, the electrical characteristics of the initial VTFT fabricated at the University of Waterloo and the related short channel effects are described. The back gate effect, space charge limited current, drain induced barrier lowering are deemed to be responsible for the poor VTFT performance. The decrease in the gate ability to control the channel charge is accountable for most of the short channel effects; and scaling the gate dielectric thickness can provide an effective solution.

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Chapter 3

Silicon Nitride (SiN_x) Gate Dielectric

Plasma enhanced chemical vapor deposited (PECVD) SiN_x is widely employed in very large scale integrated circuits (VLSICs), thin film transistors (TFTs), and electronic packages as intermediate dielectric layer, gate dielectric, passivation layer, etc. [1], [2]. The structural and electrical properties of the silicon nitride greatly depend on the deposition conditions, and must be tailored according to the device requirements. The film density and mechanical stress can also vary, depending on the conditions of the deposition [3].

In chapter 2, it is discussed that to overcome the short channel effects, the reduction of the silicon nitride thickness, serving as the transistor gate dielectric, is the most effective solution. However, the main problem with this approach is the high gate leakage current

and, more importantly, early dielectric breakdown deteriorating the performance and reliability of the device [4], [5] .

To investigate the underlying reasons behind the above-mentioned adversities, particularly limiting the operation of devices with nanometer-thick gate dielectrics, the electrical and physical characteristics of the SiN_x with thicknesses ranging from 50nm to 300nm are studied, and the results are presented in this chapter. First, a brief introduction is given on the deposition of the silicon nitride using the PECVD method. Then, the impact of the thickness on the electrical and physical properties of silicon nitride is addressed with an emphasis on the mechanisms of the film degradation. Furthermore, the sources of a high leakage current and a low breakdown voltage of the SiN_x with thickness below 50nm are presented.

3.1 Conventional SiN_x

Since PECVD is a low temperature process (below 300 °C), it is a popular deposition method for TFT fabrication, especially on a flexible substrate. Moreover, the deposition can be carried out over a large area substrate with a good uniformity and a high yield. For the PECVD deposition of the silicon nitride, typically, the process is performed at temperatures, ranging form 200 ºC to 400 ºC, with silane and ammonia as the main feeding gases [3], [6]. To achieve the proper stoichiometry of the silicon nitride film, an excess of ammonia, often by the ratio of 20 over the silane, is used. Significant amounts of hydrogen are incorporated in the films, bonded to both the Si and N [3]. According to

(3.1), silane reacts with ammonia to form the hydrogenated silicon nitride film on the substrate and the volatile hydrogen gas as the reaction byproduct.

$$3SiH_4 + 4NH_3 \rightarrow Si_xN_y : H + xH_2 . \quad (3.1)$$

In this work, the SiN_x films are deposited by a multi-chamber 13.56MHz PECVD system. The SiN_x films are deposited at an RF power of 2 W, chamber pressure of 400 mTorr, deposition temperature of 300 ºC, and gas mixture of SiH_4/NH_3 with a 5/100 ratio. The film growth rate is around 10 nm/min and the process conditions guarantee the insulator characteristics of the silicon nitride. To monitor the bonding composition of the deposited SiN_x film, the FTIR measurement is conducted. The FTIR spectra of the SiN_x are consistent with those in the literature; the main peaks associated with the Si-N bending bonds occur at 880-900 cm^{-1}, N-H bending bond at 1160 cm^{-1}, Si-H and N-H stretching bonds at 2150–2180 cm^{-1} and 3340 cm^{-1}, respectively (see Figure 3.1). This material is extensively used as the gate dielectric and the passivation layer providing an excellent film quality in terms of low leakage current and high breakdown voltage at the film thicknesses above 250nm [7]-[9]. In the remainder of this thesis, the films deposited by the aforementioned recipe are referred to as conventional SiN_x.

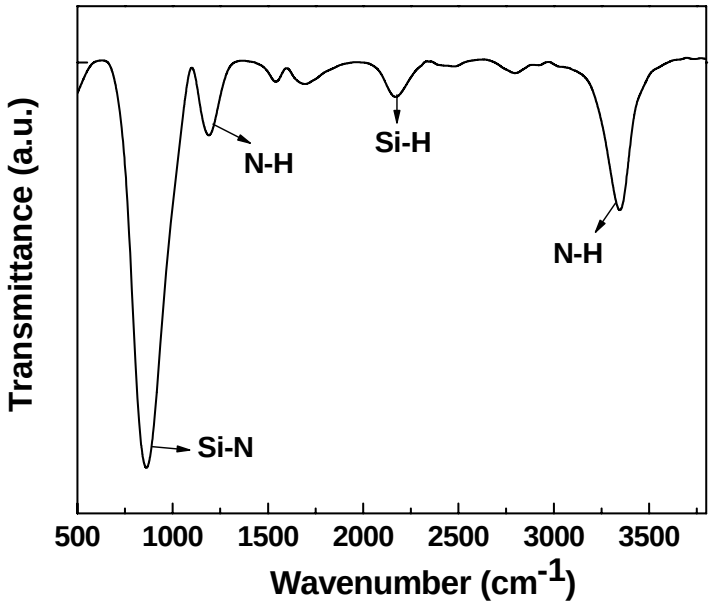

Figure 3.1: FTIR spectra of the conventional silicon nitride.

3.2 Thickness Dependence

3.2.1 Electrical Characteristics

To examine the impact of the thickness on the electrical characteristics of SiN_x, Metal/Insulator/Metal (MIM) structures are considered. The SiN_x is sandwiched between bottom Chromium (Cr) and top Aluminum (Al) electrodes. The dependence of the leakage current on the film thickness is investigated for the SiN_x layers of different thicknesses in the range of 50-300nm. The associated current-voltage characteristics are shown in Figure 3.2. The experimental results demonstrate that the electrical breakdown strength for 150-300nm thick films is approximately 6-7 MV/cm, whereas the value drops to ~2.4 MV/cm for 50nm thick films, deposited under the same process conditions.

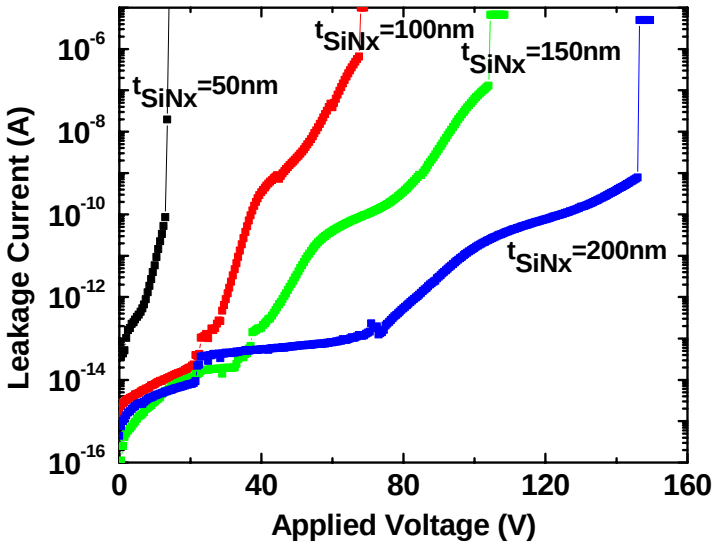

Figure 3.2: Current-voltage characteristics of the SiN_x films with different thicknesses.

The calculated breakdown electric field, as a function of the film thickness, is depicted in Figure 3.3. The breakdown field is calculated from the breakdown voltage in which an abrupt rise in the leakage current of the device is observed.

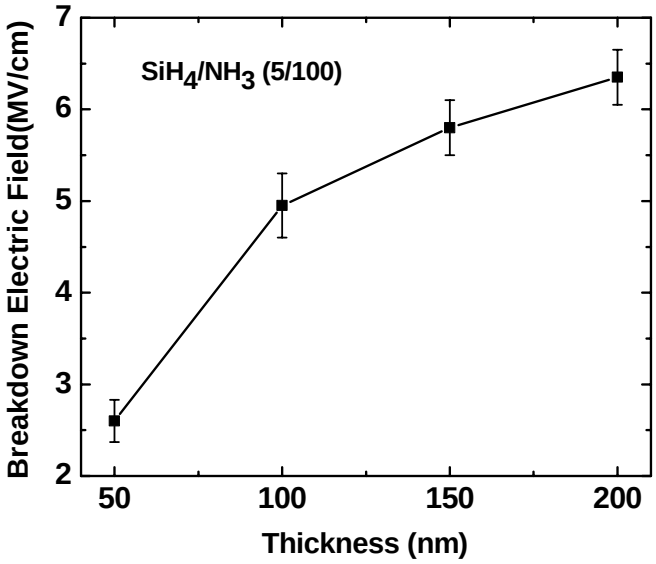

Figure 3.3: Breakdown electric field as a function of SiN_x thickness.

3.2.2 Physical Properties

The silicon oxide breakdown is divided into three modes: the A-mode failure is related to the oxide breakdown at very low electric fields of 1-2MV/cm; the B-mode is associated with the breakdown in the range of 2-8 MV/cm; and the C-mode is defined as the breakdown in the field range of 9-12 MV/cm [10]. In the literature, the A-mode breakdowns are attributed to pinholes, scratches, and other gross defects, the B-mode is related to dielectric thinning, and defects, and the C-mode is caused by the intrinsic nature of the dielectric (Figure 3.4).

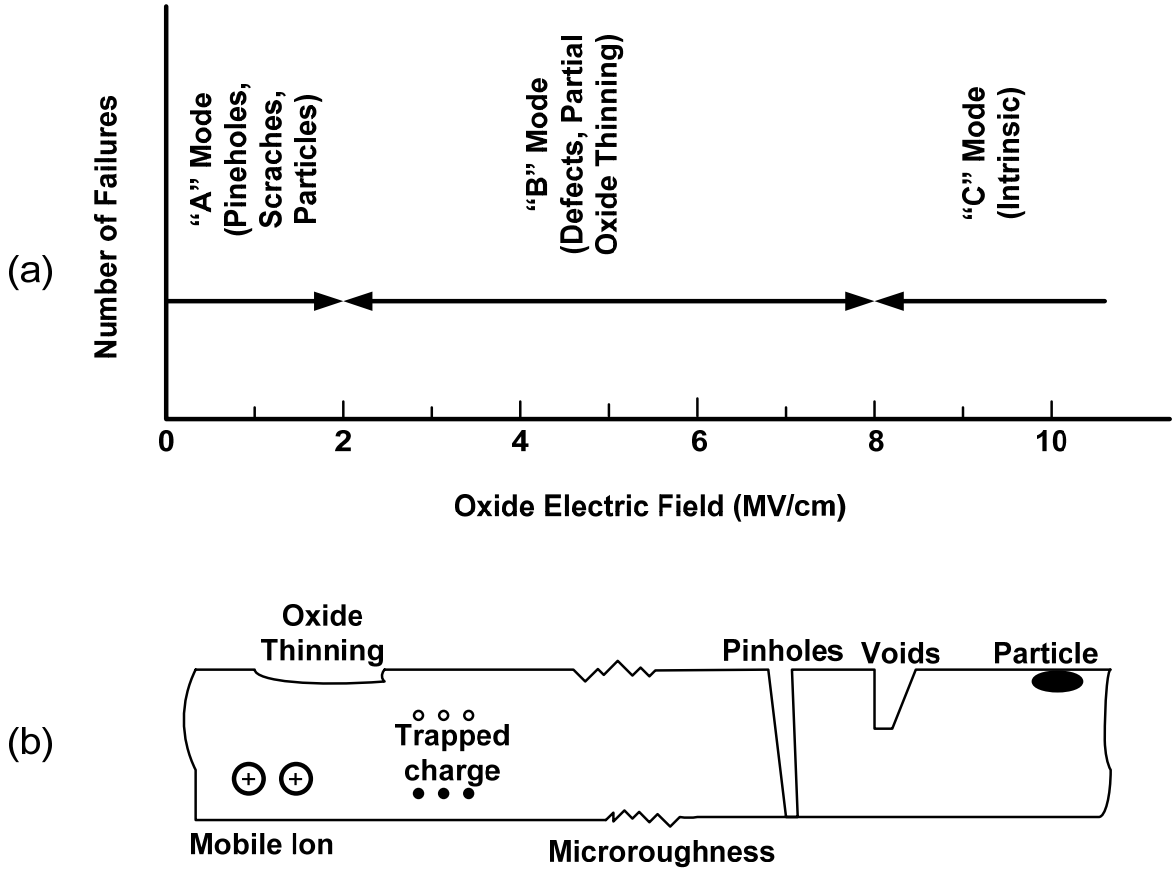

Figure 3.4: (a) Oxide breakdown mode and (b) Oxide defects (adapted from [10]).

In analogy with the oxide, the early failure (2.4 MV/cm) of the film, with thicknesses below 100nm led us to search for the possible presence of gross defects in the silicon nitride film. To examine the existence of pinholes, a selective etching method in which the etchant enters the pinholes and/or cracks of the SiN_x to etch the underlying metal layer, is used. By using this method, a rough estimate of the film pinhole density is achieved. To further characterize the SiN_x films, atomic force microscopy (AFM) measurements are employed to characterize the surface roughness of the material with different thicknesses.

To measure the density of the pinholes, SiN_x films with different thicknesses are deposited on metallized substrates and subjected to the selective etching method. The spots where the metal is etched are easy to distinguish and can be counted to provide a rough estimate of the defect pinhole density [11]. To increase the accuracy of the measurement, the observation field is magnified by a factor of 20. It is observed that while the pinhole density of the silicon nitride with a 50nm thickness is $8.6\times10^3/cm^2$, this value is reduced to $3\times10^2/cm^2$ for the 200 nm thickness films.

It is noticed that the lower breakdown field is accompanied by a pinhole density that is larger by 20 folds. High pinhole density of the thin SiN_x can be explained by the nature of the thickness evolution during the deposition. At the initial stages of the deposition, there is formation of islands or nuclei, which subsequently merge to form a continuous film [12]. As a result, at the vicinity of the substrate, the nitride is more defective than in the bulk [13].

The surface morphologies of the silicon nitride film with various thicknesses are measured using the tapping mode atomic force microscopy (AFM) with a scan size of 3μm. The representative morphologies for the 300, 100, 50 nm films are shown in Figure 3.5. The surface roughness of the silicon nitride reduces from 36% to 2.8% when the film thickness goes from 50 nm to 300 nm. Indeed the higher surface roughness at the lower film thicknesses is expected because of nucleation and islanding at the initial stages of the PECVD deposition.

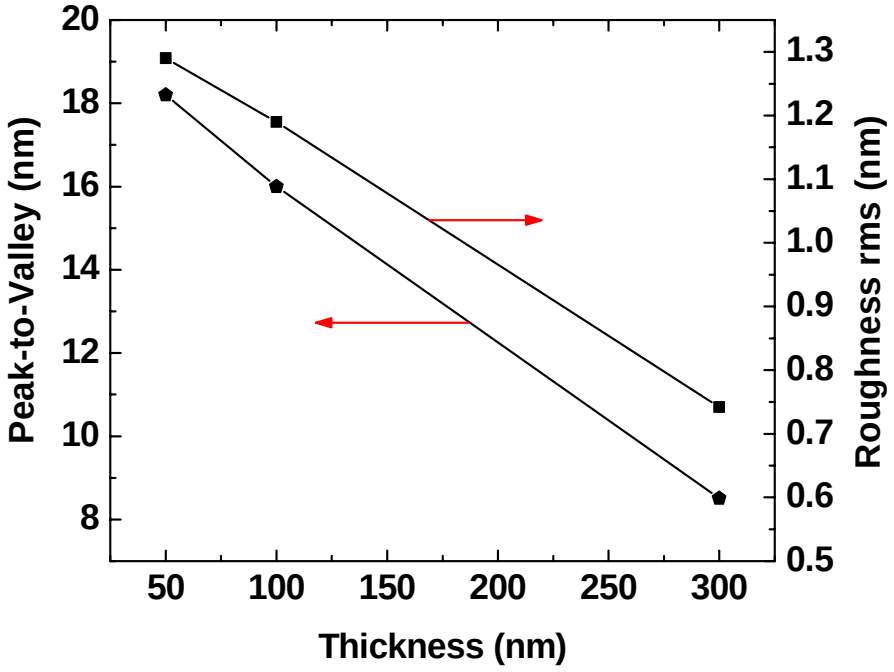

Figure 3.5: Surface morphology of the SiN_x layers as a function of film thickness.

3.3 Vertical Topology

To examine the impact of the vertical sidewall on the electrical characteristics, SiN_x films deposited on both planar and vertical surfaces are considered. The latter resembles the topology of the vertical thin film transistor. Figure 3.6 shows the schematic diagrams of the planar and vertical structures.

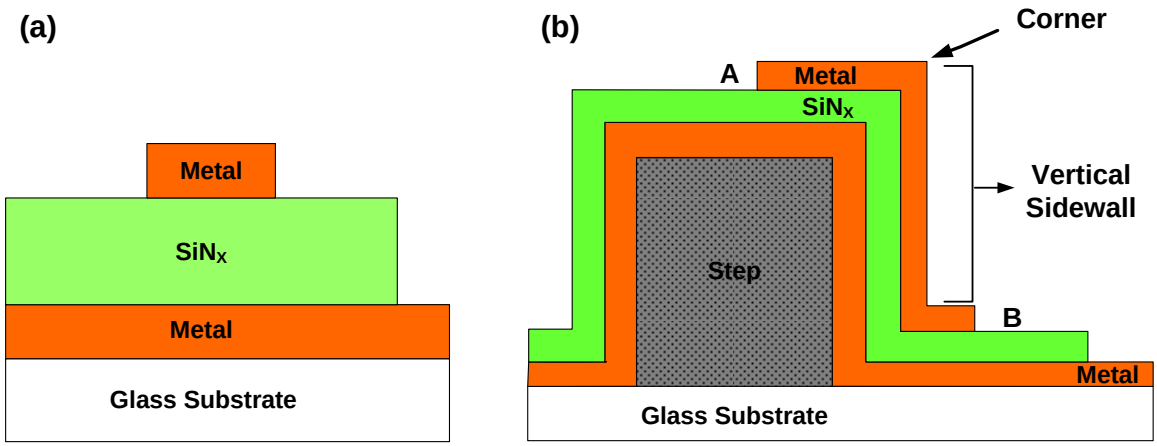

Figure 3.6: Schematic cross section of the (a) planar and (b) vertical structures used in this study (not to scale).

Figure 3.7 indicates that, the 200nm-thick silicon nitride films, deposited on a metallized planar substrate (Figure 3.6(a)) have a lower leakage current and higher breakdown strength, compared to those deposited on the vertical sidewalls (Figure 3.6(b)) at the same deposition conditions. The data reveals that for VTFTs whose gates have both planar and vertical areas, the latter section is responsible for the three orders of magnitude higher leakage current.

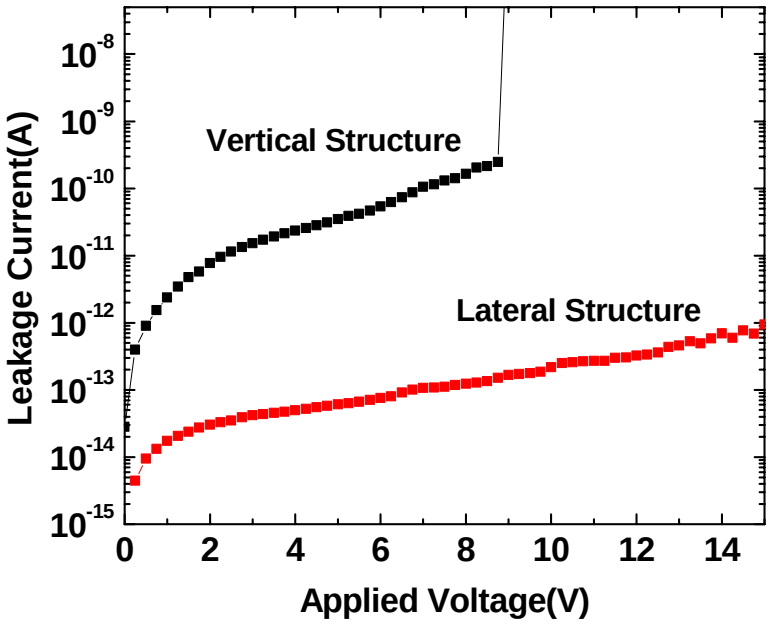

Figure 3.7: Current-voltage characteristics of vertical and lateral structures.

Intuitively there are two possible causes for the high leakage and the low breakdown of the vertical structures. The first might be the high electric field at the corners of the vertical structure. The other possible reason for the high leakage current and early breakdown might be related to the material differences or inhomogeneities in the material deposited on the vertical sidewalls. These two possibilities are discussed in the following sections.

3.3.1 Electric Field Effects

Figure 3.8 shows the electric field distribution of the vertical structure, numerically simulated using Medici software. Here, the step height is 500nm, and the thickness of the SiN_x is 200nm. The horizontal axis on the plot corresponds to the distance from A to B,

shown in Figure 3.6 (b). The two noticeable areas in Figure 3.8 with the highest magnitude of the electric field are related to the corners of the vertical structure. The electric fields at those regions are ~ 40% higher than that of the middle of the sidewall.

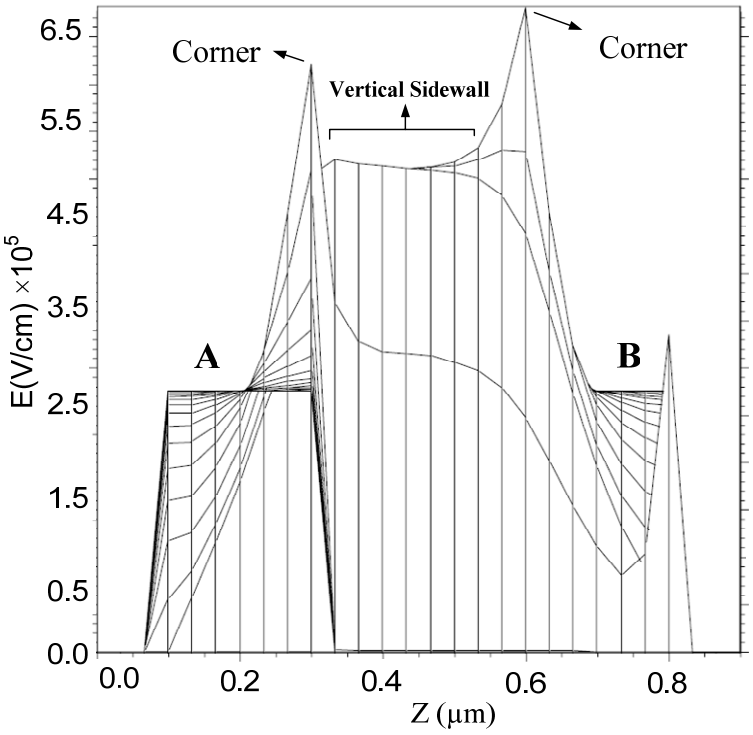

Figure 3.8: Simulated electric field distribution of the vertical structure; the horizontal axis corresponds to the distance from A to B shown in Figure 3.6 (b).

To verify the effect of the high corner electric field on the leakage current and breakdown behavior, several structures that feature a variable number of corners are examined. The associated current-voltage characteristics are illustrated in Figure 3.9. Contrary to the intuitive predictions, the current-voltage characteristics show no clear certainty in the breakdown voltage values, i.e. there is no systematic effect of the number of corners on the breakdown voltage.

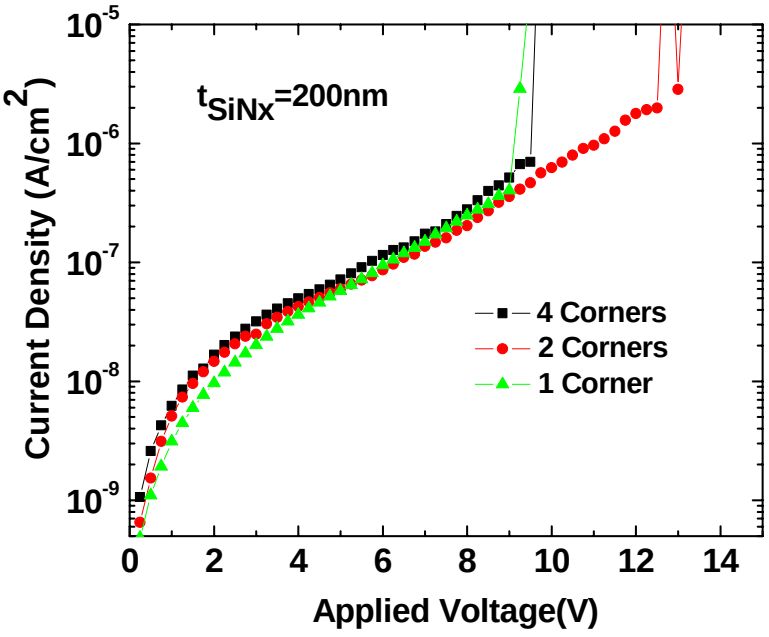

Figure 3.9: Current density of the vertical structures with different numbers of corners.

3.3.2 Material Inhomogeneity Effects

The other possible reason for the high leakage current and early breakdown of the non-planar device is the inhomogeneities in the deposited silicon nitride. In chapter 2, It is demonstrated that the thickness of PECVD films on the vertical sidewalls are approximately half of those on the horizontal surface due to the nature of plasma kinetics which govern the step coverage behavior [14]. Hence, in vertical structures, due to the poor step coverage, the thickness of the deposited film on the vertical sidewall is thinner than that of the horizontal area, inevitably leading to material inhomogeneities. This is believed to be the primary cause of the high gate leakage current and early breakdown voltages of the non-planar structures. It is also shown that the early failure of the thinner

SiN_x films is accompanied with the higher pinhole density in the layer. Therefore, VTFTs breakdown at low electric filed are attributed mostly to the high density of pinholes in the thin silicon nitride layer that lays on the vertical sidewall of the device.

3.4 Dry Etching Effects

To study the impact of dry etching on the electrical characteristics of the silicon nitride, two types of capacitor structures are investigated. In one form of the device, a continuous SiN_x dielectric layer is sandwiched between two metal layers where the top metal is patterned to define several different size capacitors (Figure 3.10 (a)). In another type, the SiN_x dielectric is patterned by means of the RIE process to construct capacitors with the isolated dielectric islands (Figure 3.10 (b). In order to produce analogous structures to those of the VTFT source-drain island, a similar dry-etch process with CF_4/H_2 (18%) used for the fabrication of VTFT devices is performed.

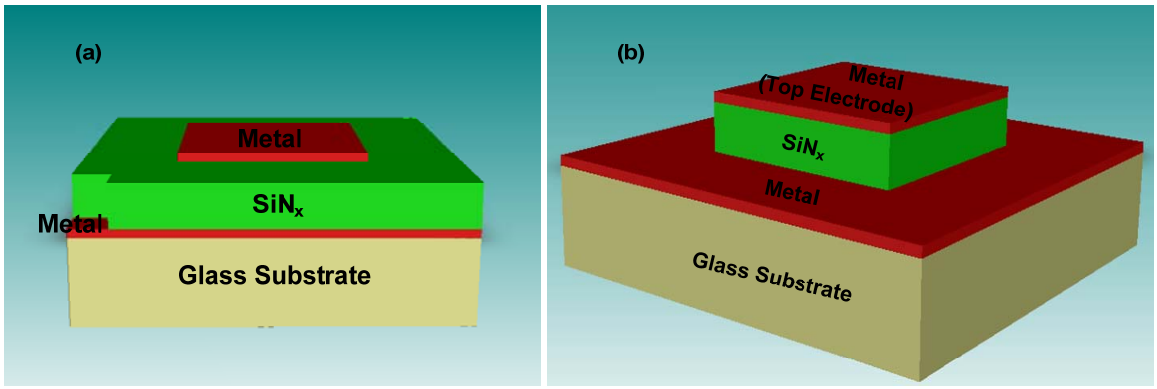

Figure 3.10: Schematic illustration of silicon nitride with (a) continues and (b) patterned structures.

The electrical characteristics are measured before and after patterning the silicon nitride as well as after the annealing the RIE-etched structure. The results for the 400μm × 400μm size capacitors are shown in Figure 3.11. It is observed that the leakage current increases 2 to 3 orders of magnitude after the formation of the islands by the RIE process.

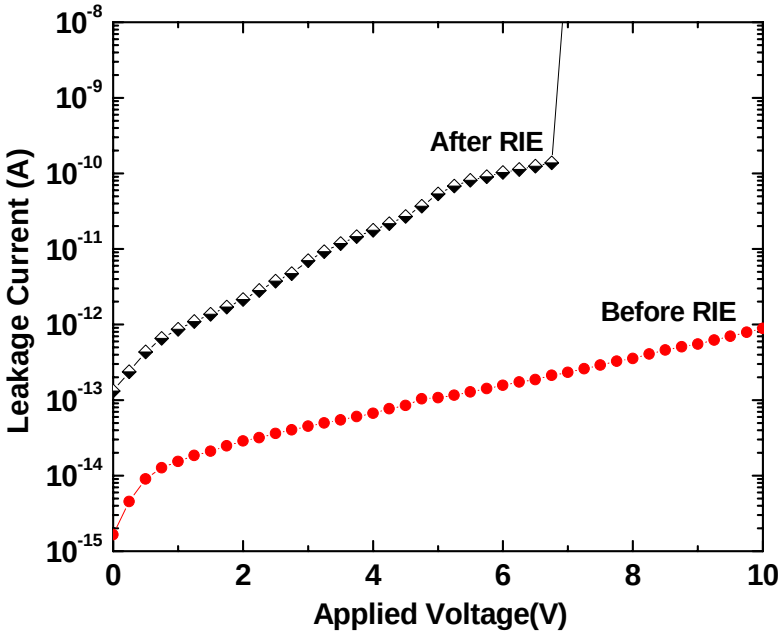

Figure 3.11: Current-voltage characteristics of the continuous and RIE-patterned SiN_x.

Samples exposed to the reactive ion etching always contain surface damage [15]. In our case, the surface damage of the RIE can be due to the deposited polymer on the sidewall or the roughening of the vertical surface. The formation of the polymer layers is inherent to the mechanism of the anisotropic etching of the SiN_x. However, this layer is removable in a high-pressure oxygen plasma, or an EKC-RIE-residue removal solution. It is deduced that the surface roughening, caused by ion bombardment increases the leakage current and lowers the average breakdown field of the material. Ion bombardment also creates

the dangling bonds on the sidewall of the patterned layer raising the charge trapping density after the RIE.

It is possible to reduce the density of dangling bonds or defect states, induced by the RIE etching in an annealing process similar to the method employed to cure the bias-stressed TFTs [16]. To examine this idea, the etched samples are subjected to 2 hours of 180°C annealing process. The result of this treatment, depicted in Figure 3.12, demonstrates that the annealing process substantially reduces the leakage current of the RIE etched insulator to values close to that of a continuous layer.

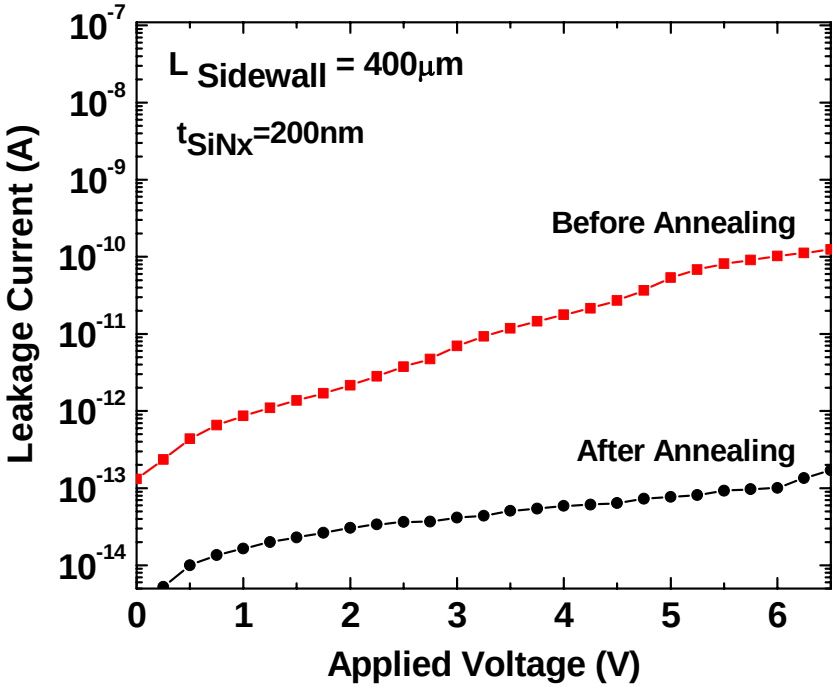

Figure 3.12: Annealing effect on the leakage current after RIE patterning.

3.5 Summary

The electrical and physical characteristics of the SiN_x films with different thicknesses are studied in this chapter. It is observed that the reduction in the dielectric thickness induces a high leakage current and early breakdown of the material. According to the experimental measurements, these electrical adversities are accompanied by an increase in the pinhole density and surface roughness of the dielectric layer.

Also, the current-voltage (I-V) characteristics measurements reveal that the leakage current of the SiN_x film deposited on a vertical surface, as an instance on the channel of the VTFT device, is at least 3 orders of magnitude higher than that of the same-thickness film deposited on a planar substrate. Furthermore, the breakdown voltage of the film is significantly lower for an insulator, deposited on a vertical sidewall. Two possible sources for the high leakage currents and low breakdown voltages of the thin nitride films; namely the high electric field at the corners and the poor step coverage, are examined. The experimental results show that the electric field singularity at the corners is not the cause of the high leakage current and poor device reliability. Rather, the cause is the poor step coverage of the PECVD-deposited dielectric on the vertical sidewall. Another important phenomenon is the detrimental consequence of the RIE etching on the leakage current of the patterned silicon nitride layer. Fortunately, a subsequent annealing process at temperatures around 200 °C can effectively alleviate this problem.

Based on the above discussion, the modification and optimization of the deposition conditions to produce thin SiN_x films with good dielectric characteristics is essential to

enhance the performance of the short channel TFTs, in general, and VTFTs, in particular. Chapter 5 reports the electrical and physical characteristics of the newly developed sub-50nm SiN_x layers suitable for application in short channel TFTs.

3.6 References

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Chapter 4

Thinning the SiN_x Gate Dielectric

The previous study from Chapter 3 demonstrates that the electrical and physical characteristics of the conventional SiN_x are strongly dependent on the film thickness. Therefore, to advance the performance of short channel TFTs in general and VTFTs in particular, the modification of the deposition conditions to achieve good dielectric characteristics of thin SiN_x films is indispensable.

This chapter focuses on the development of sub-50nm silicon nitride layers suitable for short channel TFTs. A systematic study on the relation between the material properties and the process conditions is conducted to develop a functional ultra-thin SiN_x. The results of the different method of characterizations employed to study the electrical, physical, and chemical properties of the new SiN_x are described in this chapter.

4.1 Deposition of Ultra-Thin SiN_x

To develop a new process for a functional sub-50nm silicon nitride, the conventional gas precursors (silane and ammonia) are diluted in nitrogen. The following sections provide comprehensive discussions of the dilution effect on the electrical, physical, and chemical characteristics of the developed insulator layers.

4.1.1 Electrical Characteristics

The current-voltage characteristics of the 50 nm silicon nitride films deposited using the conventional (silane and ammonia) and modified (silane and ammonia diluted in the nitrogen) processes, are depicted in Figure 4.1. It is clear that the SiN_x deposited by using the nitrogen dilution is a favorable gate insulator with a substantially lower leakage current and higher breakdown voltage. The ratio of the ammonia to the silane is kept at 20 in these depositions.

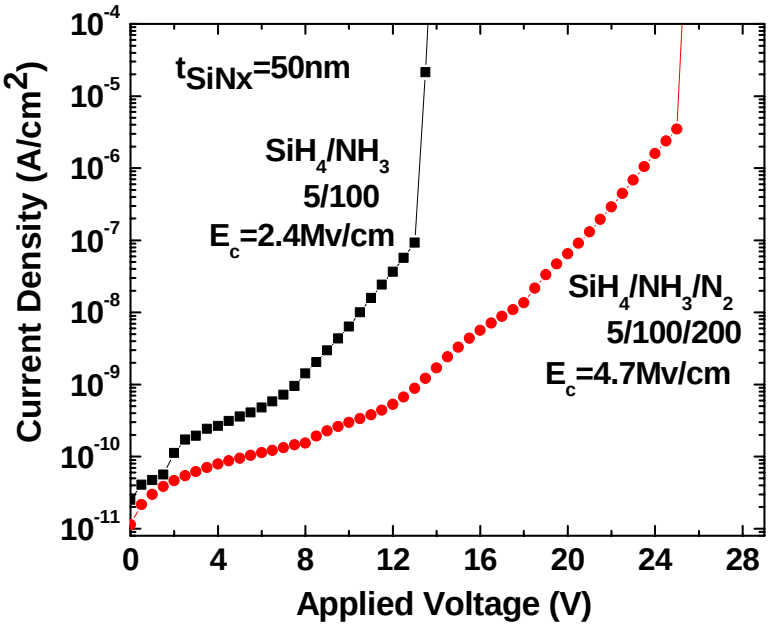

Figure 4.1: Current-voltage characteristics and the breakdown field of a 50nm SiN_x deposited with conventional (SiH_4/NH_3) and a modified ($SiH_4/NH_3/N_2$) processes.

The experimental results demonstrate that adding 200 sccm of N_2 flow to silane and ammonia, at pressure of 1 Torr and power of 15 W, increases the breakdown field (E_c) of the layer from 2.4 to 4.7 MV/cm and decreases the leakage current density by at least one order of magnitude at typical gate operating voltages.

In addition, a substantial reduction in the deposition rate is observed when the gas precursors are diluted in N_2, as shown Figure 4.2. In fact, for film thicknesses below 100 nm, the deposition rate becomes thickness dependent using $SiH_4/NH_3/N_2$ gas mixture. On the contrary, in the two-gas deposition process (SiH_4/NH_3), the deposition rate is constant even at thicknesses as low as 30nm.

The role of the N_2 dilution gas can be understood from the following discussion. The N-N (9.8ev) bond in N_2 is stronger than the N-H (4.7ev) bond in NH_3 and the Si-H (3.9ev) in

SiH_4 [1]. Therefore, the dissociation of the N_2 gas is more difficult than that of the other feeding gases. In the case of SiH_4, for example, in a typical glow discharge environment almost all of the molecules dissociate into SiH_n ($n<4$), even at extremely low power densities [2], [3]. The inactive N_2 molecules do not react with the SiH_n; instead act as inert diluents, which serve to reduce the gas-phase collisions between the SiH_n species. This, in turn, reduces the formation of the polymeric silane species in the gas phase [4]; therefore alleviating the incorporation of impurities and producing a high quality film structure.

On the other hand, the addition of N_2 to the deposition gasses increases the dissociation possibilities of SiH_4 and NH_3 raising the concentrations of SiH, NH, and H radicals in the plasma environment [4]. Therefore, the other role of N_2 is to serve as an energy booster, whereby its energy is transferred to the other gases, enhancing the dissociation potentials. A high hydrogen concentration, resulting from the dilution of the precursors in nitrogen, is beneficial to the SiN_x film by means of the hydrogen etching mechanism. Hydrogen terminates the dangling bonds, producing a film with less defect density [4], [5].

The deposition rate for different film thicknesses is extracted by a surface profilometer after patterning the islands in the films. The experimental results indicate a considerable reduction in the deposition rate when the gas precursors are diluted in N_2 gas. Under the same deposition conditions, adding 200sccm of nitrogen to silane and ammonia reduces the deposition rate to 1/3 of its original value. The reduction of the deposition rate assures the most possible role of the N_2 as the dilution gas.

Figure 4.2 indicates that the deposition rate using the modified gas mixture ($SiH_4/NH_3/N_2$) is slower in thinner films but rises up to a steady value for film thicknesses above 100 nm. The high rate of hydrogen etching due to the presence of more defect sites in the film at the early stages of the deposition is responsible for the reduced deposition rate. The high rate of hydrogen etching can be expected, when the concentration of hydrogen is high. Indeed, the inclusion of nitrogen in the plasma gasses increases the concentration of the hydrogen due to the role of nitrogen as an energy booster.

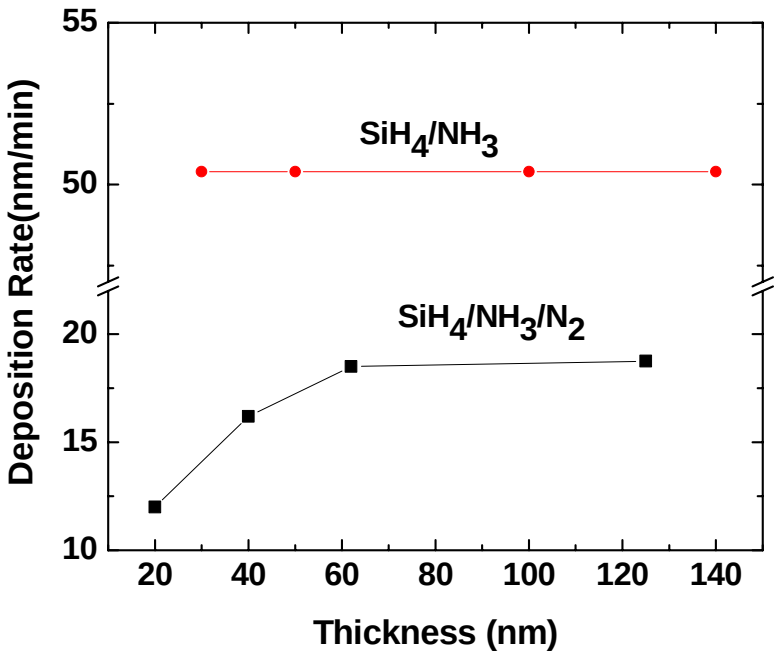

Figure 4.2: Deposition rate as a function of the thickness for the silicon nitride films deposited with the conventional (SiH_4/NH_3) and modified ($SiH_4/NH_3/N_2$) processes.

Figure 4.3 shows the breakdown electric field as a function of the film thickness for the SiN_x layers deposited with the conventional (SiH_4/NH_3) and modified ($SiH_4/NH_3/N_2$) processes. When the film thickness goes below 100 nm, only a small change (<1 MV/cm)

in the breakdown field of the nitrogen-diluted SiN_x is observed, while there is a 3 MV/cm drop for the conventional SiN_x. Intuitively, the drop in the deposition rate by virtue of enhanced hydrogen etching rate, specifies the constructive effect of the N_2 flow on the electrical characteristics of the SiN_x films such as the reduction of the leakage current and increase of the breakdown field.

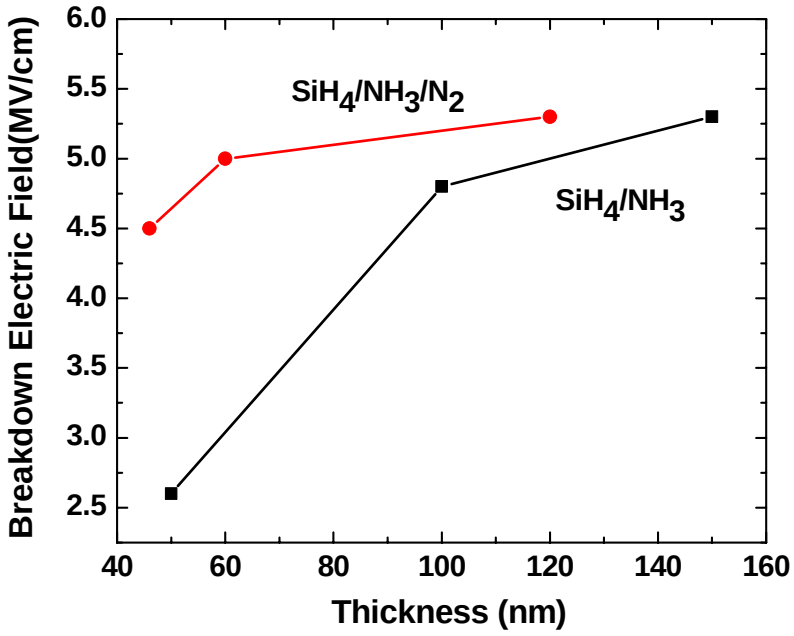

Figure 4.3: The breakdown field as a function of thickness for the silicon nitride films deposited with the conventional (SiH_4/NH_3) and modified ($SiH_4/NH_3/N_2$) processes.

In Chapter 3 we reported, conventional silicon nitride films with thickness less than 100 nm are observed to fail significantly at low operating voltages because of the high pinhole density. Similar experiments are now conducted to illustrate the high quality of the thin SiN_x layers, deposited using the modified gas mixture.

4.1.2 Physical Properties

To investigate the impact of N_2 on the physical properties of the SiN_x, the pinhole density, and the surface roughness of the film deposited with $SiH_4/NH_3/N_2$ as the feeding gas are measured and compared to the result collected from the film deposited with SiH_4/NH_3.

In order to measure the pinhole density, the selective etching method is employed. A silicon nitride layer with thickness of 50nm is deposited, by using $SiH_4/NH_3/N_2$ as the gas mixture onto a metallized substrate and then subjected to a chemical solution that enters the cracks or pinholes and etches the underlying metal. The etched metal spots provide a means to obtain a rough estimate of the defect pinhole density in the film. To increase the accuracy of the pinhole count, the observation field is magnified by a factor of 20. Figure 4.4 (a) and (b) show the 10x magnified images of the 50 nm silicon nitride films deposited with and without nitrogen dilution after the selective etching of the underneath metal layer. It is realized that while the pinhole density of the 50 nm silicon nitride deposited by SiH_4/NH_3 is $8.7\times10^3/cm^2$, this value drops to $2.5\times10^3/cm^2$ for films deposited by $SiH_4/NH_3/N_2$. Consequently, a 3.5 times decrease in the density of pinholes is achieved by introducing nitrogen gas to the deposition precursors.

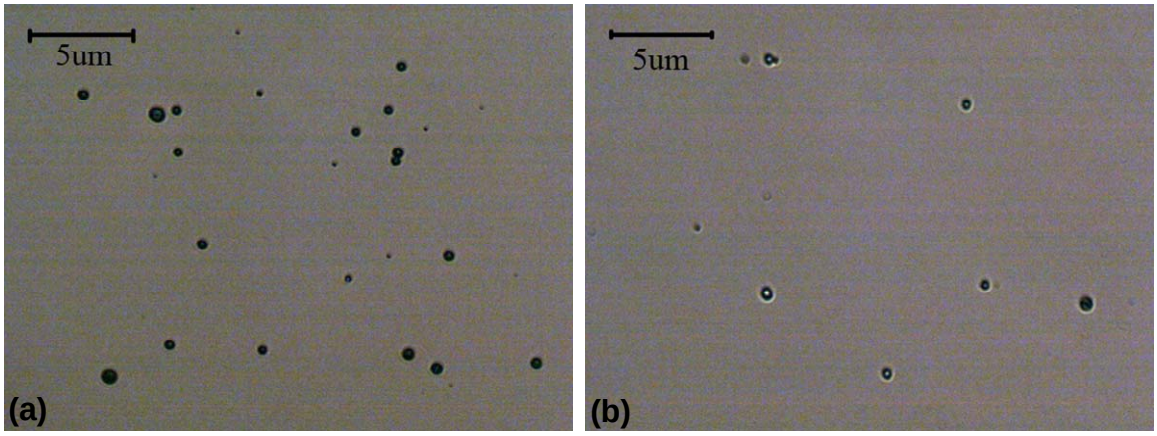

Figure 4.4: Optical images illustrating the aerial pinhole density of the SiN_x layers deposited by (a) SiH_4/NH_3 and (b) $SiH_4/NH_3/N_2$ precursor gasses, respectively.

A conducting tip atomic force microscope (AFM) system is employed to measure the effect of the nitrogen dilution on the surface morphology of the sub-50nm deposited silicon nitride layers. It is found out that the surface roughness of the SiN_x is reduced in the case of deposition with $SiH_4/NH_3/N_2$ precursor gasses. For instance, the AFM measurements indicates that, while a 50nm SiN_x film deposited with gas mixture of SiH_4/NH_3 has peak-to-valley roughness of 18.5 nm (Figure 4.5 (a)), this value drops to 12.3 nm for the film deposited with $SiH_4/NH_3/N_2$ gas mixture (Figure 4.5 (b)). The importance of this argument stems from the fact that, a rough surface leads to a wide tail state distribution and high defect density adversely affecting the performance of TFT [1].

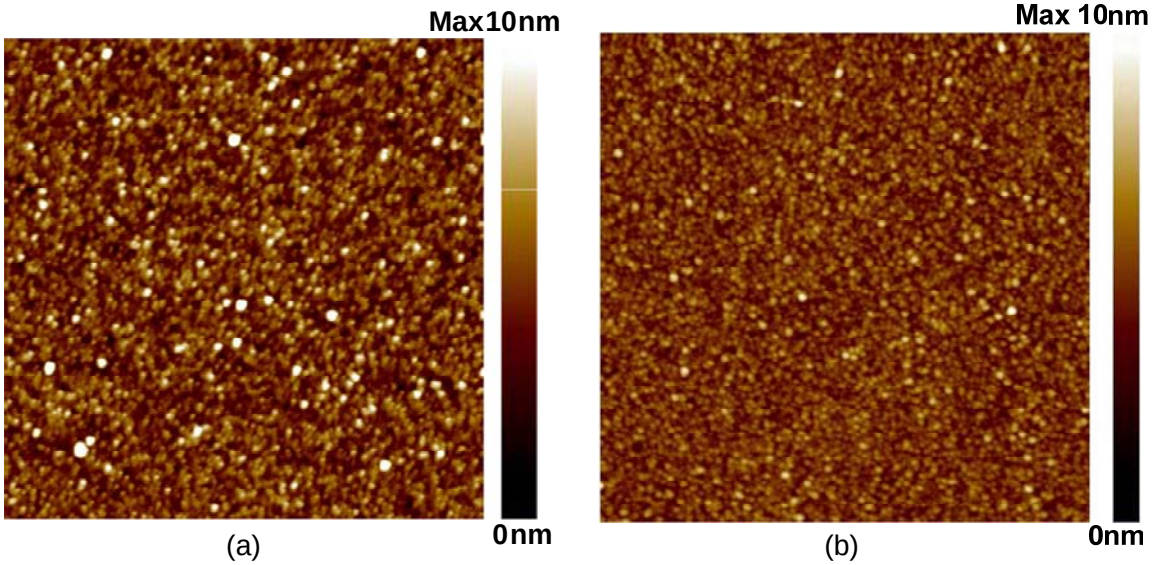

Figure 4.5: AFM images of the surface morphology for the SiN_x films deposited by (a) SiH_4/NH_3 and (b) $SiH_4/NH_3/N_2$ gas mixtures.

4.1.3 Chemical Composition

Silicon nitride can be characterized according to its chemical properties, such as silicon to nitrogen atomic ratio (Si/N), Si-H bond percentage, and N-H bond concentration. The composition of SiN_x can be varied from nearly stoichiometric Si_3N_4 to a-Si:H by changing the deposition conditions [6]. As a gate dielectric, a higher N/Si ratio is preferred over the Si-rich counterpart in terms of electrical stability [1]. It has been shown that the Si-rich SiN_x has a much higher density of Si dangling bonds [7] which act as charge trapping states leading to a high leakage current and device instability [8],[9]. In addition, it is believed that the N-rich SiN_x produces a smoother interface with the channel layer, resulting in higher mobility [10]. In particular, the TFTs with N-rich gate silicon nitride exhibit considerably less charge trapping in the dielectric or at the interface

of the active layer. This improves the stability of the device against the bias stress and enhances the field effect mobility.

To characterize the atomic ratio (Si/N) and the bond concentrations (Si-H, and N-H) of the newly developed SiN_x, ellipsomerty and the Fourier Transform IR (FTIR) measurements are conducted. The results of these measurements are also discussed in this section.

It has been reported that there is a proportional relation between the Si/N atomic ratio and the refractive index, *n*, of silicon nitride dielectric expressed as the following equation [11]:

$$n = 0.70\left(\frac{Si}{N}\right) + 1.39 \tag{4.1}$$

In this work, the refractive index is extracted from the spectroscopic ellipsometry results performed with 70-degree incidence angle over the visible range of spectrum (400-700 nm wavelengths). The measurements reveal that the SiN_x film deposited with and without nitrogen dilution have a refractive index of 1.84 and 1.78 at 550 nm wavelength, respectively. The results suggest that the addition of nitrogen gas to the deposition precursors increases the nitrogen content of the material.

To determine the Si-H, Si-N, N-H, and the total bonded hydrogen content, the FTIR spectroscopy is employed. The FTIR spectra measurements are performed using a Shimadzu FTIR- 8400S spectrometer in the wave number range of 600–3600 cm^{-1}. The spectrum of the film is obtained by subtracting the FTIR spectrum of the bare Si substrate

from the spectrum of the film on the substrate. Figure 4.6 shows the FTIR results of the silicon nitride deposited with SiH_4/NH_3 and $SiH_4/NH_3/N_2$.

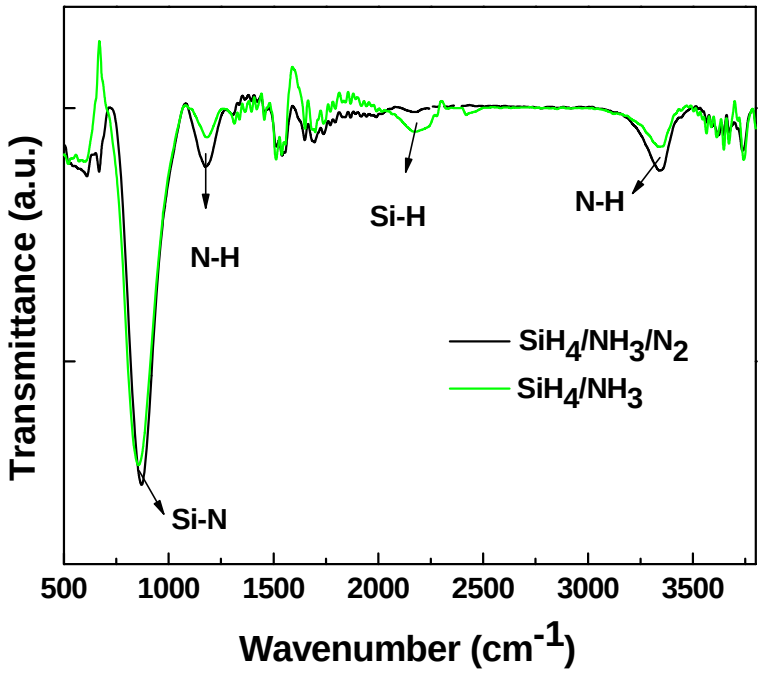

Figure 4.6: FTIR spectra of the silicon nitride deposited with and without nitrogen dilution of SiH_4 and NH_3 gasses.

The primary absorption peaks in the spectra are due to the Si-N bond stretching at 880-900 cm^{-1}, N-H bond bending at 1160 cm^{-1}, Si-H bond stretching at 2150-2180 cm^{-1}, and the N-H bond stretching at 3340 cm^{-1} [12]. Adding N_2 gas flow to the gas precursors appears to strengthen the N-H bond peaks and weaken the Si-H bond stretching, indicating an increase in nitrogen content in the film. As nitrogen content of the film increases, silicon atoms in the environment of Si-H bonds are replaced by nitrogen due to the higher electro-negativity of the nitrogen, compared to the silicon [13]. The replacement of atoms in the vicinity of the Si-H bond involves a charge transfer hence a

modification in the strength and length of the bonds [13]. Furthermore, the literature reports that the Si-H bonds contribute to the electrical conductivity of the deposited silicon nitride [3].

The following linear relationship between the Si/N and Si-H/N-H bond ratios has also been suggested by Claassen et al [11]:

$$Si/N = 0.084\left(Si-H/N-H\right)+0.70\,. \tag{4.2}$$

Based on this equation, it is concluded that the FTIR results as well as the ellipsometry measurements indicate an increase in the N content and N-H concentration of the films that are deposited with the $SiH_4/NH_3/N_2$ gas mixture.

4.1.4 Influence of Plasma Power Density

The plasma power density has a significant impact on the characteristics of PECVD-deposited dielectric layers. In this research, the applied RF power has been optimized to develop a suitable sub-50nm silicon nitride film for application as the gate dielectric of the short channel transistors. As illustrated in Figure 4.7, an enhancement in the deposition rate is observed when the RF power is increased. However, the deposition rate saturates at RF powers above 10W.

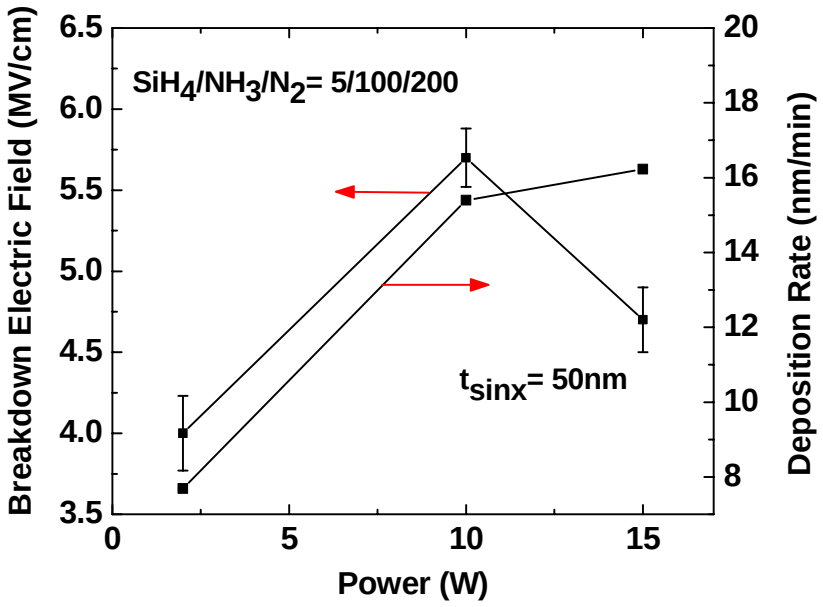

Figure 4.7: Breakdown field and the deposition rate of the 50nm-thick silicon nitride films as a function of the deposition power.

The variation in the film deposition rate as a function of the power can be explained by considering the kinetics of the plasma process. Any PECVD deposition process is composed of three major mechanisms; namely, the plasma phase reactions, particle transport, and surface process. Naturally, the slowest involving process determines the deposition rate.

The plasma phase reactions are initiated by the dissociation of the feeding gas molecules [14], [15]. The dissociation phenomenon is the result of the collisions between the feeding gas molecules and the energized particles such as electrons, radicals, or ions. Then, the reactants transport to the wafer surface by diffusion for the neutrals or by ion bombardments in the case of charged particles. The term surface process is attributed to the chemical decomposition, reaction, surface migration, or any other surface reaction [16].

Any typical plasma process includes both etching and deposition mechanisms. It has been reported that the etching mechanism is enhanced by the Ion bombardment [14]. In low power conditions, the plasma potential is low and the ion bombardment effect on the surface reactions is negligible [15]. Furthermore, the densities of the precursor reactants are low in the plasma. Therefore, the deposition rate and film structure is mainly controlled by the supply of precursors such as SiH_n and NH_n to the plasma phase. On the other hand, the deposition rate is amplified by the applied power since the dissociation efficiencies of the feeding molecules increase accordingly. At high powers, the surface reaction mostly controls the deposition process [15], which explains the saturation of the deposition rate.

From Figure 4.7, it is evident that there is a transition point for the breakdown field (E_c) depending on the power. Note that the highest breakdown voltage is achieved at the critical power. But, beyond this point, surface damage due to high ion bombardment energy at the high plasma power can explain the reduction of the E_c when the power goes beyond the critical value.

4.1.5 Impact of N_2 Flow Ratio

To study the effect of nitrogen flow on silicon nitride material properties, the electrical characteristics of the deposited layers using $SiH_4/NH_3/N_2$ gasses with ratios of 5/100/0, 5/100/100, and 5/100/200 are examined. It is observed that at 200 sccm nitrogen flow, the deposited film exhibits a critical electric filed of 4.7 MV/cm while this value drops to 3.6

and 2.5 for the SiN_x deposited with 5/100/100 and 5/100/0 gas mixtures, respectively (Figure 4.8).

Figure 4.8 shows the deposition rate of SiN_x films as a function of N_2 gas flow. The observed trend is the reduction in the deposition rate as the nitrogen content of the plasma increases. At high nitrogen dilution rates, the partial pressures of the reactive gases and consequently, the density of the reactants species are reduced, leading to a considerable drop in the deposition rate. On the other hand, the lower partial pressures help to decrease the possibility of gas phase reactions that produce larger molecules. The incorporation of large molecules in the depositing layer results in a high surface roughness and the poor quality of the insulator film.

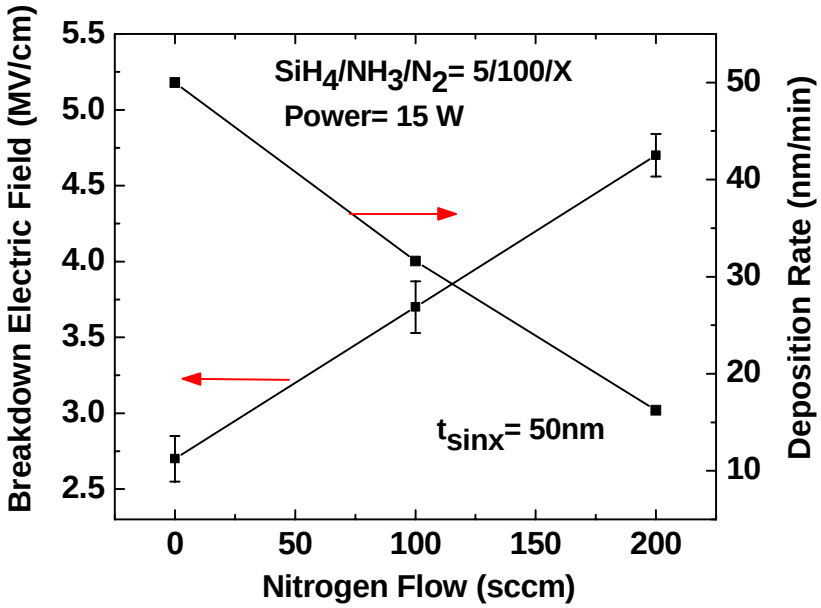

Figure 4.8: The breakdown field and the deposition rate of the 50nm-thick silicon nitride layer as a function of nitrogen flow.

4.2 Deposition with H_2-Diluted Precursor Gases

The performance of PECVD SiN_x can be also improved by dilution of the deposition gasses in H_2. The first observed consequence of the H_2 dilution is the reduction of the deposition rate to even below those associated with the films deposited by $SiH_4/NH_3/N_2$ gas mixture (see Figure 4.9). Intuitively predicted, the rate of the deposition is slower for the silicon nitride film deposited by $SiH_4/NH_3/H_2$ gasses due to the presence of higher atomic H concentrations in the plasma, resulting in a faster etching mechanism.

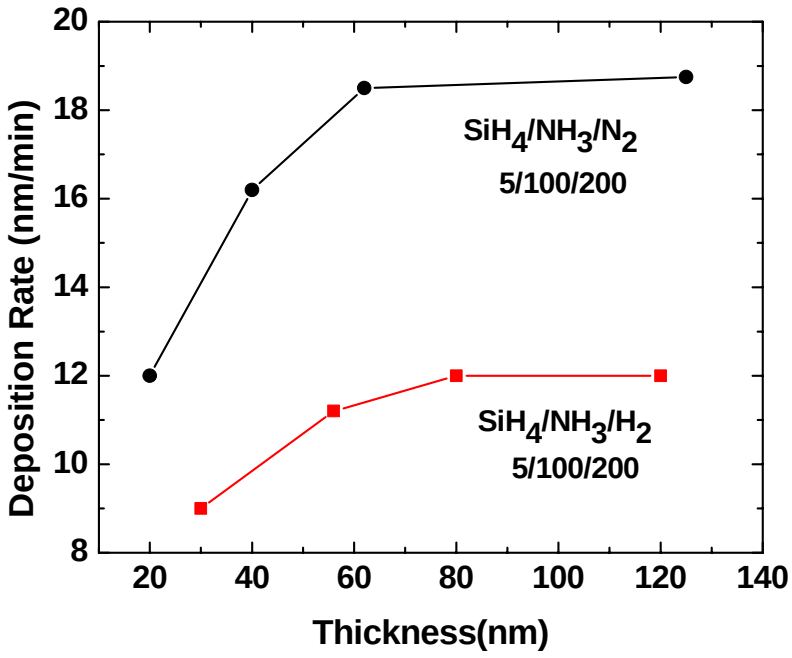

Figure 4.9: Deposition rate as a function of thickness for the silicon nitride films deposited with $SiH_4/NH_3/H_2$ and $SiH_4/NH_3/N_2$ gas mixtures.

As discussed earlier, during the growth of SiN_x films, two competing processes of the deposition and etching take place. The former process is the result of the chemical reaction between the silicon and nitrogen containing radicals and the top surface of the substrate or the deposited layer [1]. The etching mechanism is due to material sputtering by ion bombardment or the reaction of the deposited film with hydrogen radicals released from the silane, ammonia, and hydrogen molecules [1]. Therefore, the higher concentration of the hydrogen radicals in the plasma enhances the etching process during the deposition. This phenomenon explains the reduction of the deposition rate when hydrogen is introduced to the system.

Figure 4.9 demonstrates the dependence of the deposition rate to the film thickness. As mentioned in chapter 3, the thinner films are more defective due to nucleation and islanding at the initial stage of the PECVD deposition. Therefore, the etching process is more pronounced in the early stage of the deposition when the concentrations of the dangling and weak bonds are higher.

4.2.1 Electrical Characteristics

The current-voltage characteristics of the 50nm SiN_x films, deposited with gas mixtures of SiH_4/NH_3 (5/100), $SiH_4/NH_3/H_2$ (5/100/200), and $SiH_4/NH_3/N_2$ (5/100/200) at the pressure of 1 Torr and 10 W plasma power, are shown in Figure 4.10. The addition of H_2 and N_2 improves the electrical characteristics of the material by increasing the breakdown electric field (E_c) to 4.2MV/cm and 5.6 MV/cm, respectively. Moreover, more than one

order of magnitude decrease in the leakage current is achieved for the silicon nitride layers that are deposited by the diluted gasses.

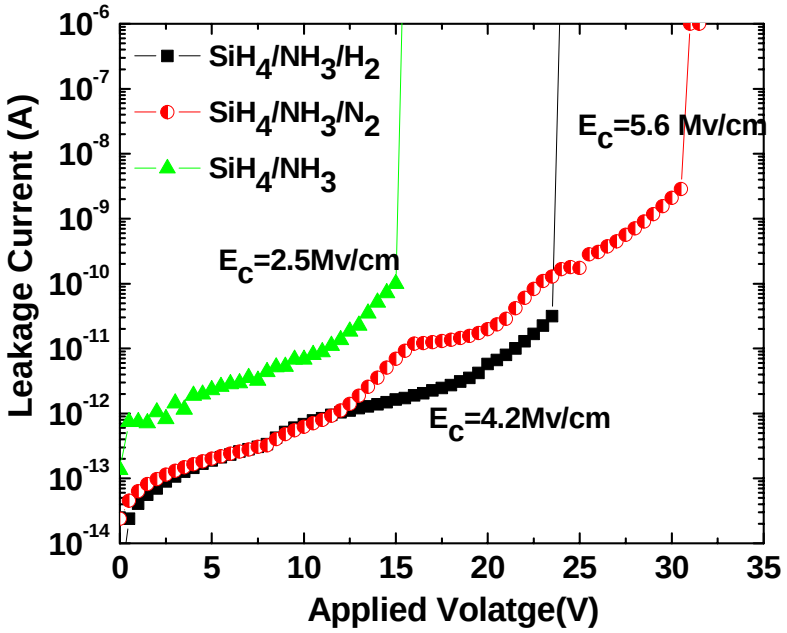

Figure 4.10: *I-V* characteristics of the 50nm silicon nitride deposited with different gas mixtures.

4.2.2 Physical Properties

The pinhole density of the 50nm SiN_x film, deposited with $SiH_4/NH_3/H_2$ as the PECVD feeding gas is measured by employing the selective etching method. From Figure 4.11 (a), a pinhole density of 5.8×10^3 cm^{-2} is obtained for a 50nm film deposited with H_2 diluted gasses. Earlier in this chapter, values of 8.7×10^3 cm^{-2} and 2.5×10^3 cm^{-2} are reported for the pinhole densities of same thickness SiN_x layers, produced with SiH_4/NH_3 and $SiH_4/NH_3/N_2$ gases, respectively. Therefore, compared to the film deposited with SiH_4/NH_3, the pinhole density is reduced by a factor of 1.5 and 3.5, respectively, for the

50nm-thick SiN_x layers, deposited by the H_2 and N_2 diluted gasses. In Figure 4.11, the 10x magnified optical images of the SiN_x films, deposited with diluted and undiluted gasses are presented to facilitate the comparison.

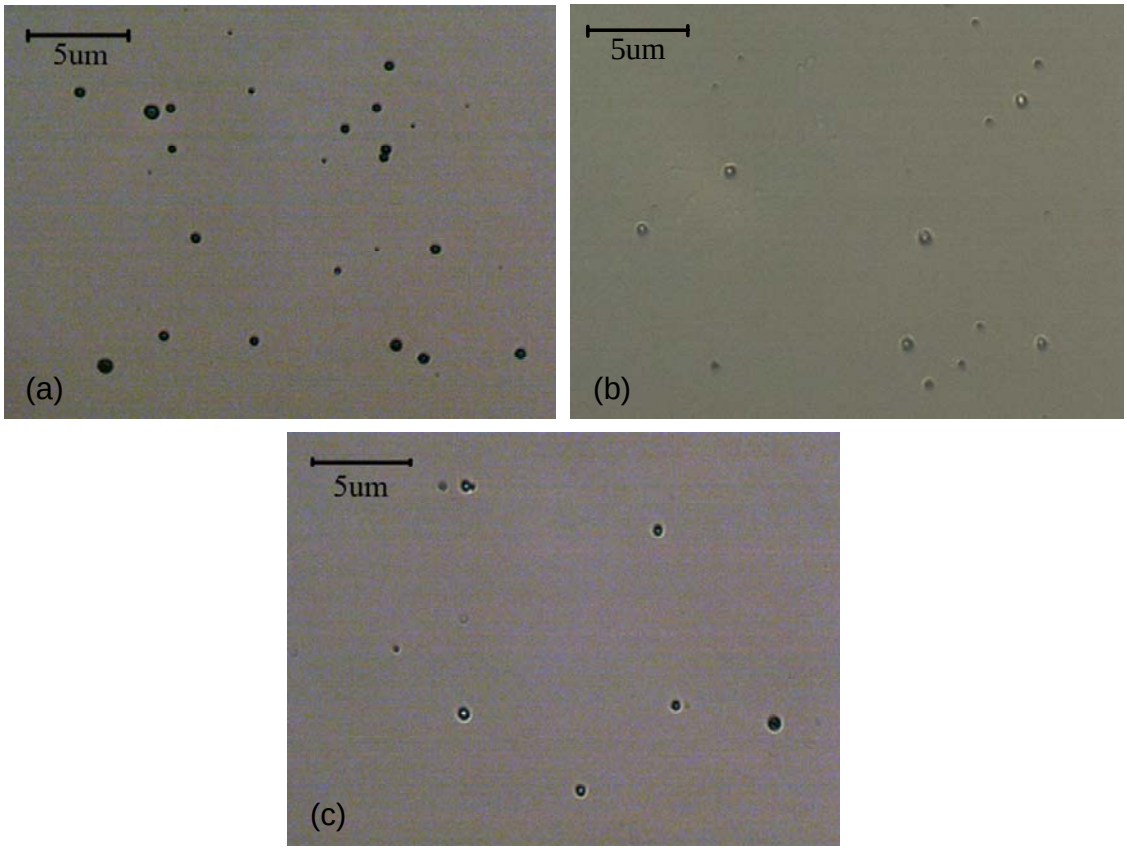

Figure 4.11: Optical images of the 50nm SiN_x layers deposited with (a) SiH_4/NH_3 (5/100), (b) $SiH_4/NH_3/H_2$ (5/100/200), and (c) $SiH_4/NH_3/N_2$ (5/100/200) gases, illustrating the populations of the pinholes in the film.

In the literature, it is found that the breakdown is usually initiated from a small defective area of the device [17]. As a direct consequence, the concentration of the pinhole influences the reliability of the deposited film. Therefore, based on the pinhole density measurement results, it is concluded that 50nm-thick films deposited with the gas mixture

of $SiH_4/NH_3/N_2$ are preferred over the ones with $SiH_4/NH_3/H_2$. That is, the thin SiN_x films produced by the N_2 diluted gasses are more reliable in terms of the smaller breakdown probability due to the lower pinhole density of the film compared to the materials deposited with $SiH_4/NH_3/H_2$.

4.2.3 Chemical Composition

SiN_x films of a 50 nm thickness are deposited on silicon substrates, and their refractive indexes, *n*, are measured by a spectroscopic ellipsometer. The refractive index of the material, deposited with SiH_4/NH_3 (5/100) gasses diluted in 200sccm of hydrogen, is 1.86, extracted at 550 nm wavelength. According to (4.2) indicating the proportional relation between *n* and the Si/N ratio, the ellipsometry measurement results demonstrate that the SiN_x films deposited with hydrogen diluted gasses, have higher Si contents compared to those produced by $SiH_4/NH_3/N_2$. Consequently, the SiN_x films deposited by the N_2 diluted gases are better candidates for the gate dielectric application which demand nitrogen rich materials.

To monitor the bond content of the SiN_x films deposited by the H_2 diluted gases, the FTIR measurements are carried out. Figure 4.12 represents the results of the IR spectroscopy of SiN_x layers, produced by gas mixtures of $SiH_4/NH_3/H_2$ and $SiH_4/NH_3/N_2$. It is clear that the addition of hydrogen to the plasma environment increases the density of the Si-H bonds.

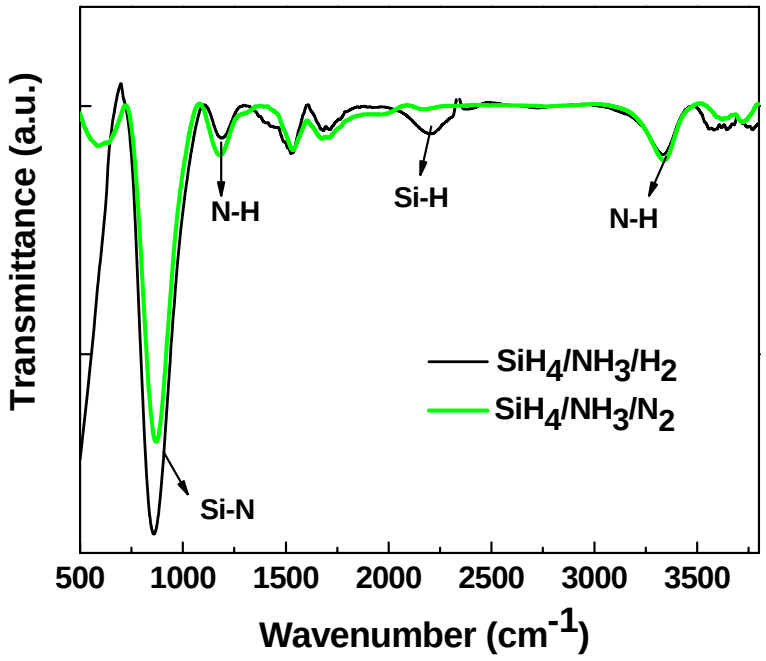

Figure 4.12: FTIR spectra of the silicon nitride films deposited by $SiH_4/NH_3/H_2$ and $SiH_4/NH_3/N_2$ gas mixtures.

A higher Si-H bonds concentration is expected when the gas mixture is diluted in H_2 instead of N_2. It is reported that when the N-content of the film increases, the Si-H bonds tend to disappear and are replaced with N-H bonds [18]. This speculation is also confirmed by the higher refractive index of SiN_x films deposited by $SiH_4/NH_3/H_2$ compared to the films produced by $SiH_4/NH_3/N_2$.

Another effect of the H_2 dilution during the deposition of the SiN_x films is to reduce the band gap of the dielectric [19]. By varying the Si/N ratio of the silicon nitride from N-rich to Si-rich material, the bandgap is continuously reduced from about 5 ev at nearly stoichiometric composition to less than 2 ev, the corresponding value for a-Si:H [20], [21]. The reduction in the band gap of the insulator has the adverse effect of the leakage

current enhancement; therefore, the SiN_x films deposited with N_2 diluted gasses are the preferred candidates for application as the gate dielectric of TFTs.

4.3 Summary

A systemic study on the relation between the deposition conditions and the material properties of the SiN_x films has leaded to development of an ultra-thin functional dielectric layer. The electrical properties of the 50nm SiN_x layers, deposited by silane and ammonia diluted in N_2 gas, reveal that the newly developed film can successfully serve as the gate dielectric of short channel TFTs and VTFTs with excellent performance characteristics of the leakage current density as low as $0.1nA/cm^2$ and breakdown electric field of 5.6MV/cm. In addition, the ellipsomerty and FTIR measurements ascertain the suitability of the ultra-thin dielectric film for the gate dielectric application.

Also, in this chapter, the impact of the H_2 dilution on the material properties of the sub-50nm SiN_x film is described. The electrical characteristics of the 50nm silicon nitride layer indicates that the inclusion of H_2 in the gas mixture (silane and ammonia) also reduces the leakage current by at least one order of magnitude along with increasing the breakdown voltage to 4.2MV/cm. However, the breakdown voltage of this material is lower than that of the deposited film with the $SiH_4/NH_3/N_2$ gases. Furthermore, a lower pinhole density is observed in the dielectric produced by the N_2 dilution.

The refractive index and bonding content of SiN_x deposited with different feeding gases are addressed. A N-rich SiN_x film characteristic, identified as the appropriate gate

dielectric material, is achieved with addition of the N_2 to the silane and ammonia during the deposition of the silicon nitride layer.

4.4 References

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Chapter 5

VTFTs with Ultra-Thin Gate Dielectric

This chapter provides the characteristics of the VTFTs, fabricated by employing the newly developed SiN_x as the gate dielectric. As discussed earlier, the previous attempts at fabricating VTFTs have yielded devices with high drain leakage current, low ON/OFF current ratio, and absence of saturation behaviour at high drain voltages, all induced by short channel effects. To overcome these adversities, which become dominant as the channel length approaches the nano-scale regime, the reduction of the gate dielectric thickness is mandatory. In Chapter 4, a systematic study on the development of functional ultra-thin SiN_x films for application as the gate dielectric of VTFT has been conducted.

In this chapter, initially the electrical characteristics of the 500nm channel length VTFTs with 100nm conventional silicon nitride gate dielectric layers are discussed. Then, to demonstrate the potential of the newly developed ultra-thin silicon nitride for application

in short channel TFTs, the fabrication results of the VTFT utilizing 50nm and 30nm new SiN_x gate dielectric, is presented. The transistors characteristics are analyzed based on the fabricated devices and the effect of the gate dielectric thickness on the VTFT performance is addressed. The final part of this chapter is devoted to the nc-Si:H VTFTs and their electrical characteristics. In addition, the impact of the gate dielectric on the performance of the nc-Si VTFTs is delineated.

5.1 Effect of Gate Dielectric Scaling on a-Si:H VTFT

The 0.5µm channel length vertical thin-film transistors are fabricated on glass substrates with 100nm, 50nm, and 30nm SiN_x as the gate dielectric. For the 100nm gate dielectric, the conventional silicon nitride recipe is used, and the newly developed material is employed for the 50nm and 30nm SiN_x gate insulators. The details of the fabrication process have been presented in chapter 2. Figure 5.1 shows the cross section schematic and the SEM image of the fabricated 0.5µm channel length VTFT, utilizing the 50nm new SiN_x as the gate dielectric.

Current–voltage characteristics of the VTFTs are measured at room temperature using a Keithley 4200 semiconductor characterization system. Prior to the measurements, the VTFTs are annealed at 170 °C for 2h to improve the contact properties [1].

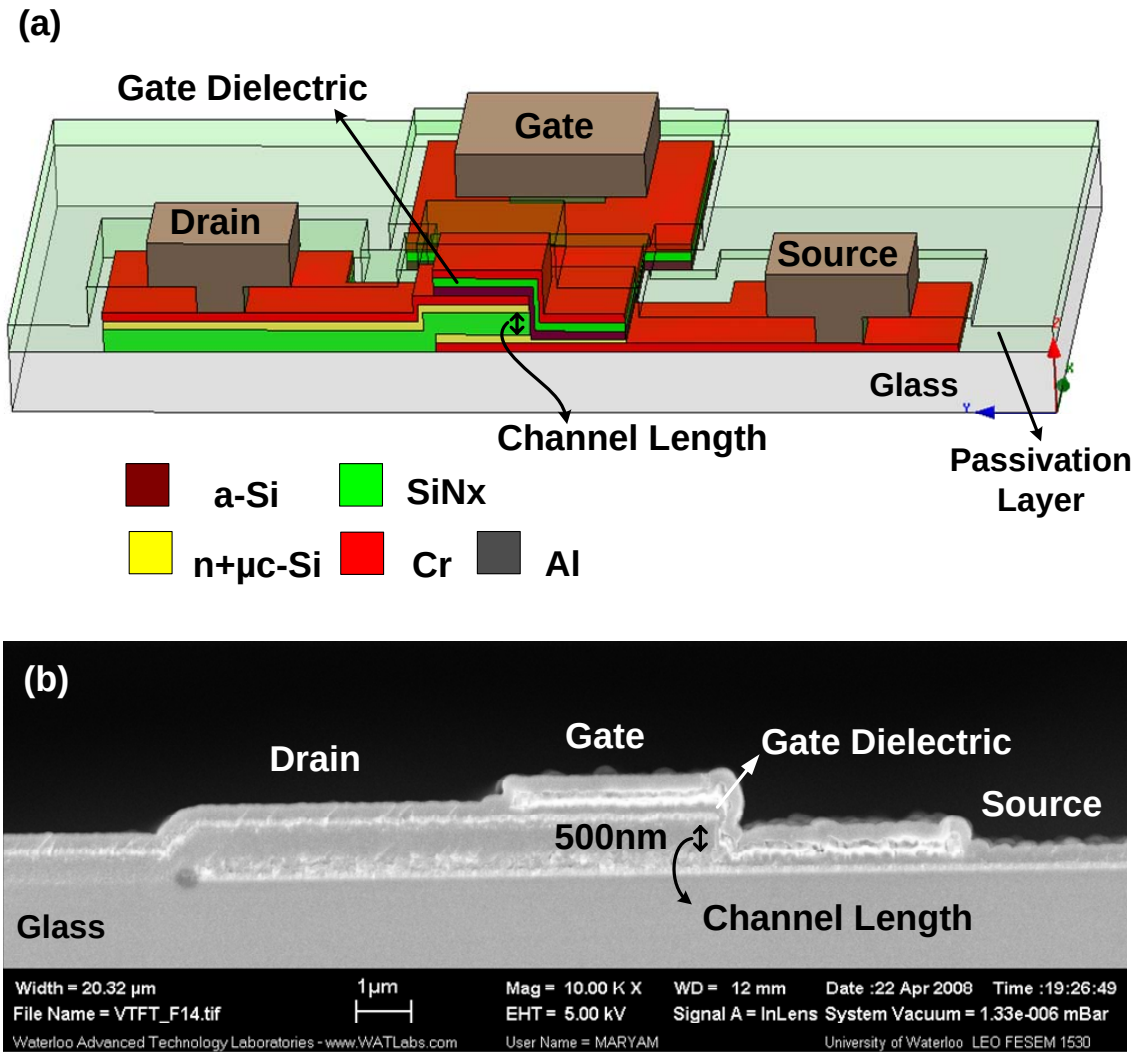

Figure 5.1: (a) Cross-section schematic and (b) SEM image of the vertical thin film transistor (VTFT).

The I_{DS} - V_{GS} characteristics of the a-Si:H VTFT with the channel length of 0.5 µm, channel width of 31 µm, and gate dielectric thickness of 100nm is portrayed in Figure 5.2. The fabricated VTFTs exhibit the ON/OFF current ratios of around 10^6 and leakage currents of ~2×10^{-12} A at V_{GS} = -3V. The subthreshold slope is approximately 0.98 V/dec, hence high gates voltage are required to turn ON the devices. The subthreshold slope defined by (5.1) is particularly important when the device is used as a low-voltage, low-

power switch. The subthreshold slope determines how fast a turned OFF or ON switch moves to the other state of the operation [2].

$$S = \left(\frac{dV_{GS}}{d(\log I_{DS})} \right) \tag{5.1}$$

The 10^6 ON/OFF current ratio obtained at V_{DS} =1.5 V drops when the drain voltage increases due to a rapid rise in the OFF current of the VTFT. This drawback is mainly caused by the back channel current of the VTFT discussed in Section 2.6. The ON and OFF currents are selected as the maximum and minimum drain currents, respectively, observed on the transfer characteristics for the same drain bias.

The extracted threshold voltage (V_{Th}) of the device is 2.7V obtained by fitting a straight line to the plot of the square root of I_{DS} versus V_{GS}, according to the following expression at the saturation region of operation:

$$I_{DS} = \frac{1}{2} \mu_{FE} C_{gate} \frac{W}{L} (V_{GS} - V_{Th})^2 \tag{5.2}$$

Here, μ_{FE}, C_{gate}, W, and L are the electron field effect mobility, gate capacitance, channel width, and channel length of the transistor, respectively. The extracted parameters of the VTFT are summarized in Table 5.1.

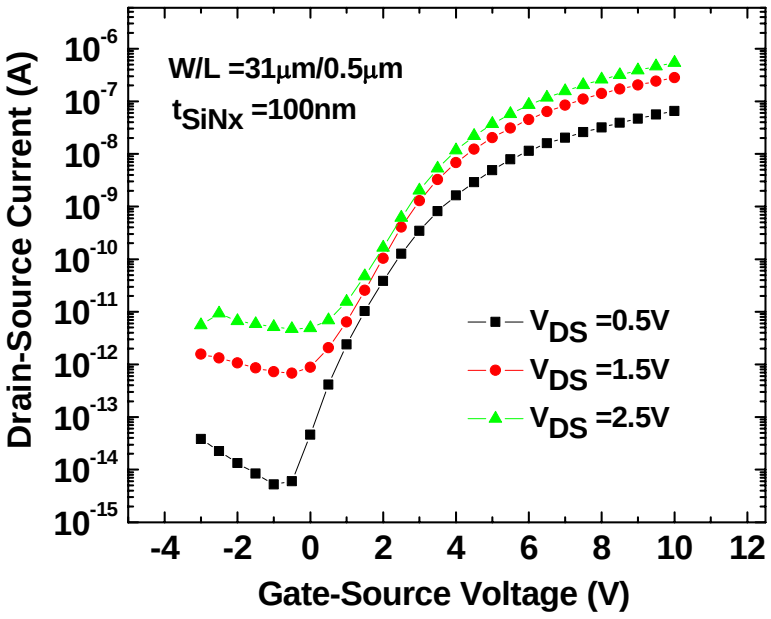

Figure 5.2: I_{DS} - V_{GS} characteristics of the 0.5μm channel length VTFT employing 100nm conventional gate silicon nitride.

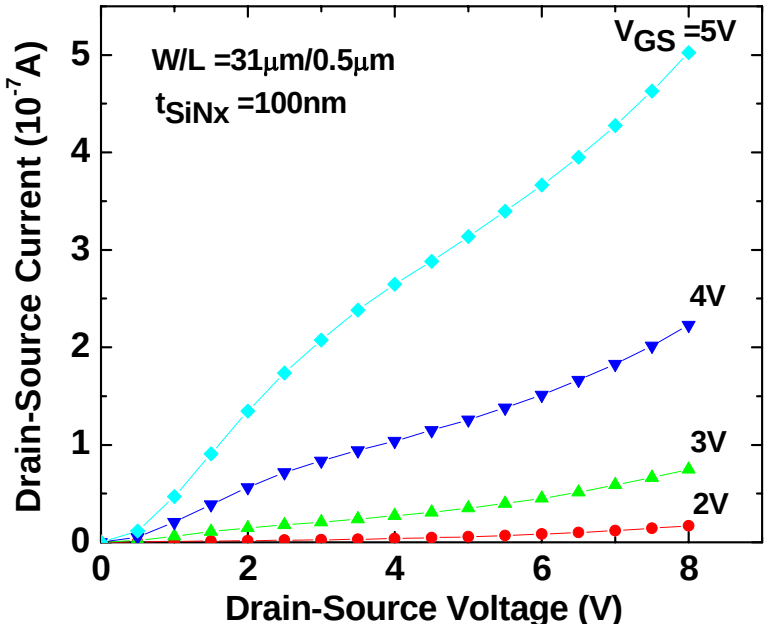

Figure 5.3: Output characteristics of the 0.5 μm channel length VTFT employing 100nm conventional gate silicon nitride.

Figure 5.3 demonstrates very low output currents at small drain voltages with a poor saturating behaviour as the drain bias increases.

The current-voltage characteristics of a 0.5 μm channel length and 31μm channel width VTFT with 50nm SiN_x as the gate dielectric is presented in Figure 5.4. For comparison, the gate leakage current as a function of the gate voltage at different drain biases is also shown in Figure 5.4 (a), along with the transfer characteristics of the device. It is evident that even at gate voltages as high as 15V, the drain current is more than five orders of magnitude higher than the gate leakage.

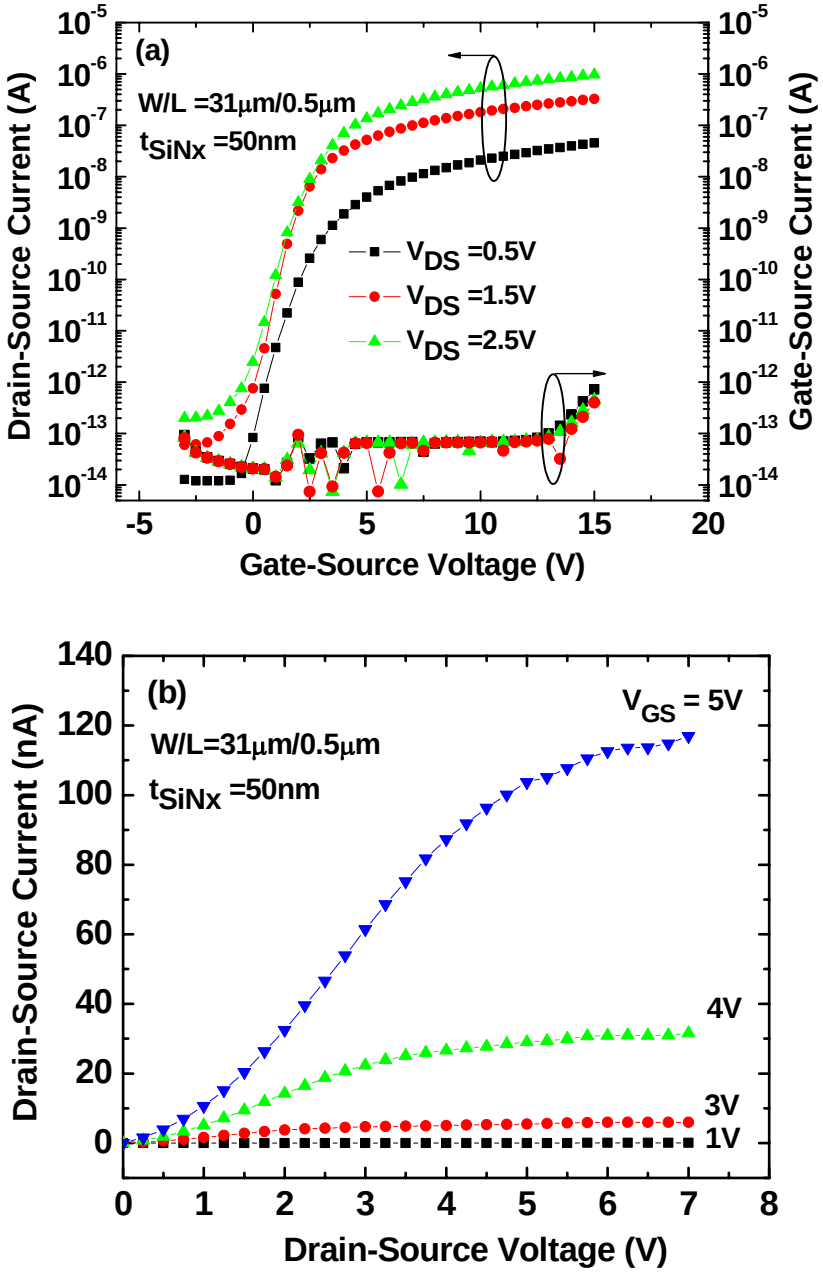

Figure 5.4: (a) Output current and the gate leakage as a function of the gate voltage at different drain biases and (b) the output characteristics for a 0.5μm channel length VTFT with 50nm silicon nitride as the gate dielectric.

The small gate leakage current of less than 0.1 pA within the bias window reveals that the new nitride is a promising candidate for short channel TFTs. The fabricated VTFTs demonstrate the ON/OFF current ratios of more than 10^7, threshold voltages (V_{Th}) of ~1.9

V, and subthreshold slopes of 0.48V/dec. The extracted parameters in addition to the reproducibility of the device characteristics demonstrate the great application potential of this device for large area electronics. The associated yield of the process is confirmed to be over 90% by measuring the electrical characteristics of more than 50 VTFTs.

The I_{DS} - V_{DS} characteristic of a 0.5 μm channel length VTFT exhibits saturation behavior at high drain voltages, implying the good control of the gate over the channel. The high contact resistance observed at low drain voltages is mainly due to the short channel characteristics, in which, the value of channel resistance approaches that of contact resistance. In our devices, n+ nc-Si buffer layers are used between the source and drain metals and the intrinsic a-Si:H active layer to ensure the ohmic behavior of the contacts [3]. However, even with low resistive ohmic contacts, the current crowding can occur in the TFTs with a staggered-electrode structure [4]. When VTFT is in the ON-state, electrons from the n+ contact should travel across the a-Si:H intrinsic layer to reach the conducting channel. This current is known as the space charge limited current (SCLC) [5]. The intrinsic layer is mostly un-accumulated, and the carriers face a high resistance before arriving at the channel. Consequently, this portion of the contact resistance becomes noticeable, especially when the channel length is scaled down to submicron dimensions.

The I_{DS} - V_{DS} characteristics at zero gate voltage are shown in Figure 5.5 for the VTFTs with a 50nm newly developed and a 100nm conventional SiN_x as the gate dielectric. Irrespective of the drain voltage, the transistor with 50nm new silicon nitride gate dielectric remains in the OFF state when the V_{GS} is set to zero. Therefore, an excellent control of the gate over the channel charge is observed for this device. On the contrary,

the transistor with the 100nm conventional nitride gate dielectric is turned ON by the drain bias even at V_{GS} below the threshold voltage of the VTFT.

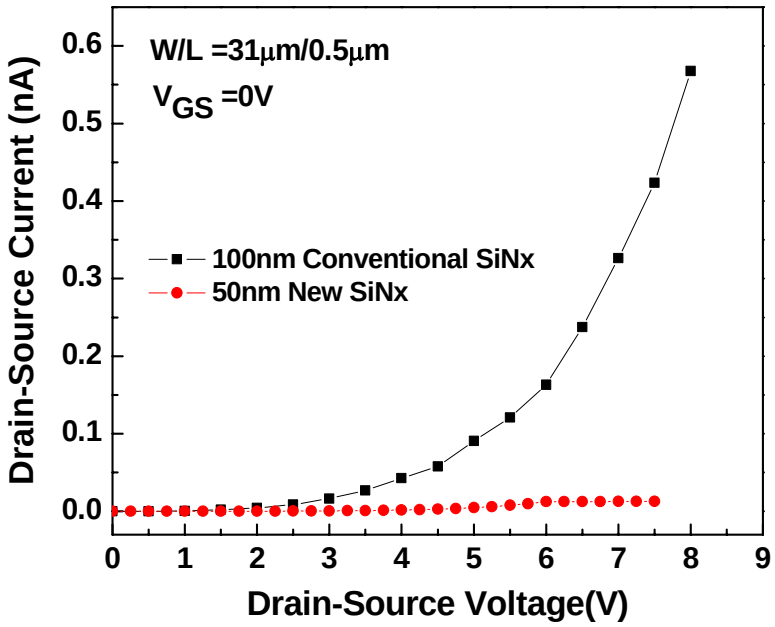

Figure 5.5: I_{DS} - V_{DS} characteristics at V_{GS} = 0V for the VTFT with 100nm conventional and 50nm new SiNx gate dielectrics.

It was argued that the major obstacle for scaling the gate dielectric thickness is the high leakage current and low breakdown voltage of the gate undermining the reliability and performance of the transistor. To demonstrate the superior electrical characteristics of the newly developed silicon nitride, the gate leakage current of the VTFTs with 100nm conventional SiN_x and 50nm new SiN_x is measured at the zero drain voltage. Figure 5.6 illustrates the three orders of magnitude lower gate leakage current of the new silicon nitride compared to the 100nm conventional gate dielectric. Moreover, significantly higher degree of reproducibility in the characteristics of the device with 50nm new gate dielectric is observed compared to that of the VTFT with 100nm conventional gate dielectric.

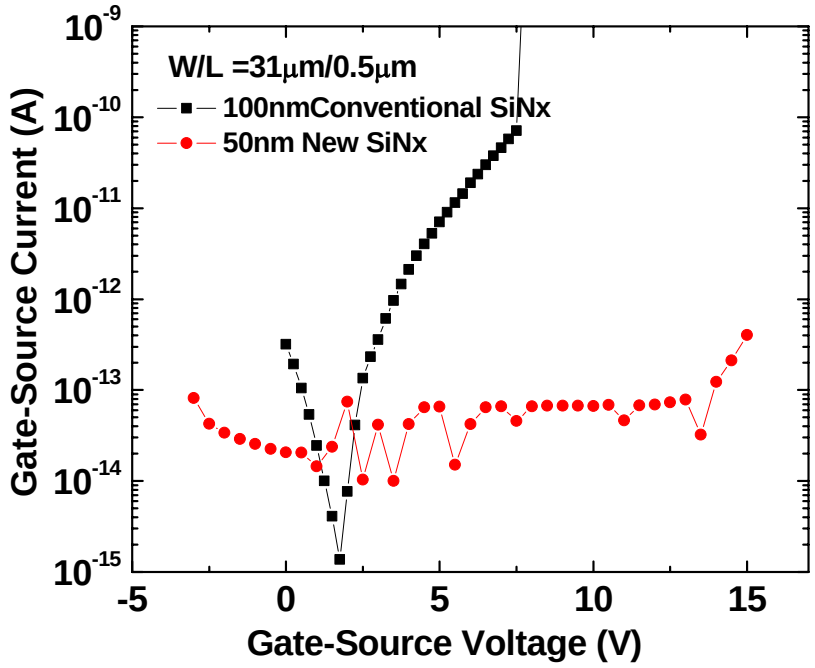

Figure 5.6: Gate leakage current as a function of the gate voltage for the VTFTs with 100nm conventional and 50nm new silicon nitride insulators.

To further study the influence of the gate dielectric thickness on the VTFT performance, a device with 30nm SiN_x gate dielectric is fabricated. The output and transfer characteristics of this device are presented in Figure 5.7.

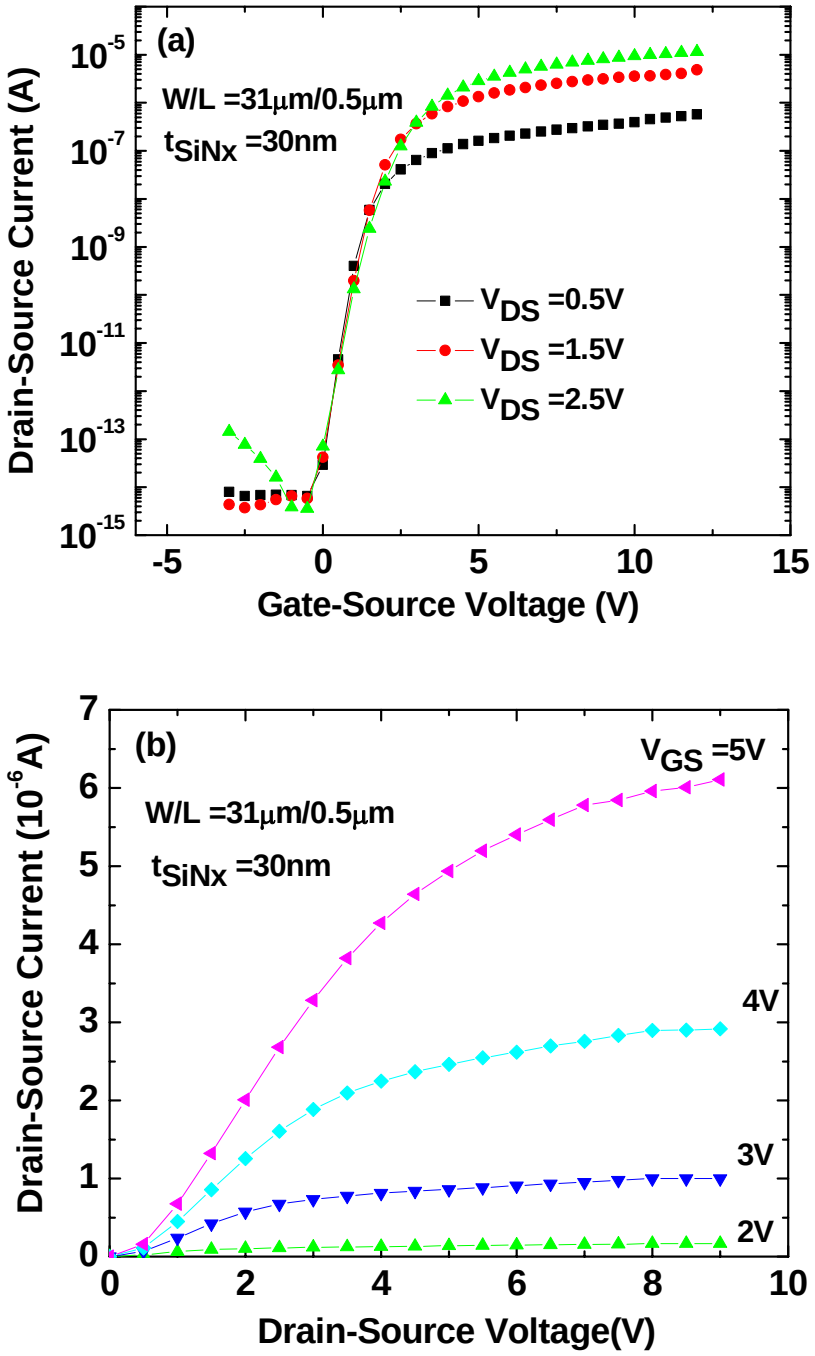

Figure 5.7 (a) Transfer and (b) output characteristics of the 0.5 μm channel length VTFT with 30 nm silicon nitride as the gate dielectric.

The current-voltage measurements illustrate that the VTFT with 30nm SiN_x gate dielectric exhibits outstanding characteristics such as an ON/OFF current ratio as high as 10^9, a subthreshold slope as sharp as 0.23 V/dec, and a drain leakage current as low as

1fA. Despite the excellent performance of the transistors, a lower degree of characteristic reproducibility is observed, compared to VTFTs that have the 50nm SiN_x as the gate dielectric.

Table 5.1 summarizes the extracted circuit parameters of the 0.5um channel length a-Si:H VTFT with 100nm, 50nm, and 30nm SiN_x gate dielectric.

Table 5.1: Summary of the 0.5 µm channel length a-Si:H VTFT performance parameters with different gate dielectric thicknesses.

VTFT Specifications / Parameter	Gate Dielectric 100nm	Gate Dielectric 50nm	Gate Dielectric 30nm
Threshold Voltage	2.7V	1.9V	1.1V
ON/OFF Current Ratio	$< 10^6$	$\geq 10^7$	**$\geq 10^9$**
Subthreshold Slope	0.98V/dec	0.48V/dec	**0.23V/dec**
Drain-Source Leakage Current	1.5×10^{-12} A	6×10^{-14}A	**2×10^{-15}A**

The evolution of the electrical characteristics of VTFTs with different gate dielectric thicknesses confirms the constructive effect of the gate dielectric scaling on the performance of the VTFT. The high OFF current, low ON/OFF current ratio, and large subthreshold slope of the short channel TFTs are improved by application of the sub-50nm new silicon nitride as the gate dielectric of the transistor.

The remainder of this chapter provides a detailed discussion on the physics behind the improvement of the VTFT performance due to the application of the new SiN_x films as the gate dielectric. In the next section, the transport mechanisms in a-Si:H VTFTs are reviewed with the emphasis on short channel devices.

5.2 Transport Mechanisms

There are believed to be three parallel mechanisms for current conduction between drain and source in VTFTs:

1- Channel current (I_{ch})

2- Bulk current (I_{bulk})

3- Back channel current (I_{back})

Therefore, the total current of the VTFT (I_d) can be written as

$$I_d = I_{ch} + I_{bulk} + I_{back} \tag{5.3}$$

The main component of the drain current is called the channel current where similar to the conventional TFT expressed in (5.2) in the saturation region of the operation. However, as discussed in Chapter 2, VTFT with sub-micrometer channel length, the drain electric field penetrates the channel region affecting the channel formation. This phenomenon can raise the drain current when the drain voltage is increased, and hence compromise the saturation behavior of the drain and the gate control over the channel charge.

The second component of the VTFT current is the bulk current. For a device with a 25nm-thick active layer, a significant portion of the a-Si:H film remains un-accumulated, since the conduction channel is within 10nm from the gate dielectric interface [6]. As the channel length shrinks in the VTFT, a high electric field is formed in the un-accumulated region of the channel. Consequently, the injected carriers from the source drift through the bulk of the a-Si:H until reach the drain contact. This current is known as the space charge limited current (SCLC) explained in Chapter 2 of this thesis.

The last component of the current in the VTFT is associated with the back interface

states. Basically, the drain electric field penetrates the dielectric between the drain and source and accumulates electrons along the back interface. Therefore, a weak channel is formed at the interface of the active layer with the intermediate dielectric particularly close to the drain end, where the electric field is stronger. The back channel current in the ON state of the operation is negligible compared to the other two current components. However, the I_{back} becomes crucial in the OFF state condition, when there is no charge accumulation in the front channel [7]. Figure 5.2 demonstrates that in the OFF-state operation, the drain leakage current is significantly increased at the high drain voltages.

5.3 OFF Current and Subthreshold Slope

The transfer characteristics of the VTFTs with different gate dielectric thicknesses are presented in Figure 5.8 for comparison. At V_{DS} = 1.5V, the VTFT with 100nm gate dielectric has an OFF current of 1.5×10^{-12} A, and this value drops to 6×10^{-14} and 2×10^{-15} A for the devices with 50nm and 30nm SiN_x gate dielectrics, respectively. Therefore, scaling the gate dielectric thickness has significantly improved the OFF-state performance of the VTFT.

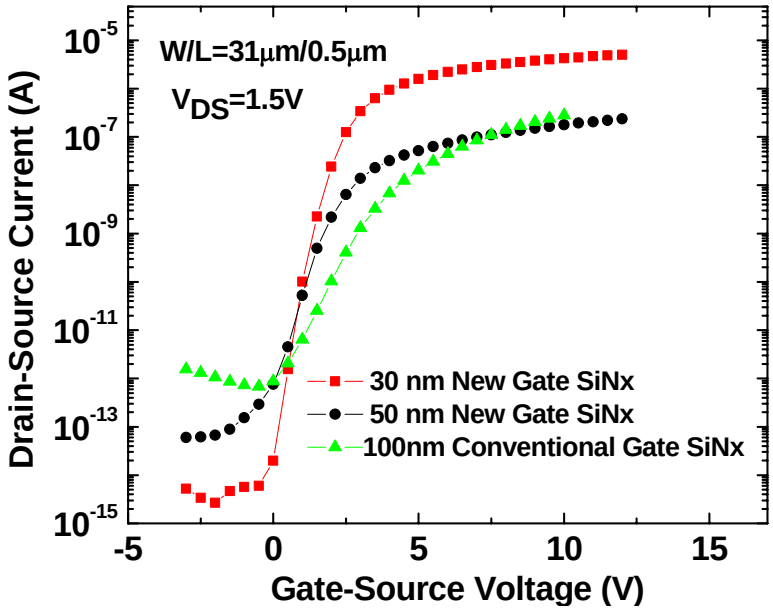

Figure 5.8: Transfer characteristics of the VTFTs with gate dielectric thicknesses of 100nm, 50nm, and 30nm.

It is proposed that the electron accumulation at the back interface induced by the drain electric field, is probably the main source of the drain leakage current in the VTFT structure. For a VTFT with 100nm SiN_x gate dielectric, over two orders of magnitude increase in the OFF current of the device is observed when the drain voltage rises from 0.5V to 1.5V, reflected in Figure 5.2. While, for the same change in the drain voltage, less than a one order of magnitude increase and almost no enhancement in the leakage current are measured for the VTFT with gate dielectric thicknesses of 50nm and 30nm, respectively (Figure 5.4 and Figure 5.7).

A possible explanation for the improvement of the OFF-state performance can be speculated by considering the capacitive circuit elements. When the gate dielectric thickness (t) is reduced, the gate capacitance per area (C_G) increases according to:

$$C_G = \frac{\varepsilon}{t}, \tag{5.4}$$

where ε is the permittivity of the gate dielectric.

Consequently, $C_{eq} = C_A \parallel C_G$, the equivalent capacitance between the gate metal and any point at the back interface (Figure 5.9) rises since the active layer capacitance (C_A) is constant. If the parasitic resistances between the gate, back channel, and drain are neglected, the voltage of any point in the back channel can be expressed by the following equation:

$$V_{BG} = \left(\frac{C_D}{C_D + C_{eq}}\right) V_{DG}, \tag{5.5}$$

where V_{BG}, V_{DG}, and C_D are the gate-back interface voltage, back drain-gate voltage, and drain capacitance, respectively. Therefore, according to (5.5), increasing the gate capacitance, reduces V_{BG} and the dependence of the back channel voltage on the drain bias. That is, decreasing the gate dielectric thickness enhances the gate control over the back channel of the VTFT

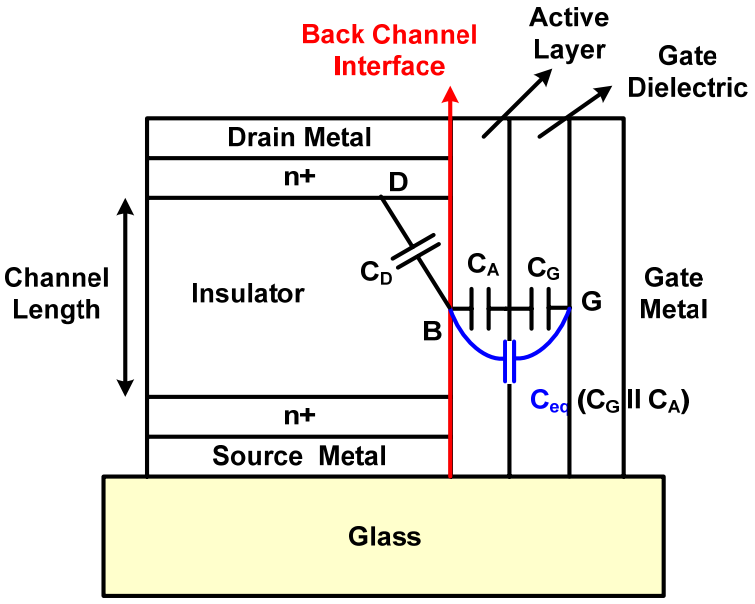

Figure 5.9 Schematic cross section of the VTFT structure illustrating the capacitive circuit elements.

The subthreshold slope, *S*, defined as the required gate voltage to induce a tenfold increase of the drain current in the subthershold region, is given by (5.1). It is evident from Figure 5.8 that the subthreshold slope decreases, when the gate dielectric thickness is scaled. The extracted value of *S* for the VTFT with 100nm conventional SiN_x gate dielectric is 0.98 V/dec while this value drops to 0.48V/dec and 0.23V/dec for the VTFT with 50nm and 30nm silicon nitride gate dielectric, respectively.

The most important factors determining the subthreshold slope are the trap densities in the bulk of the active layer (N_T) and at the interface (D_{it}) between the channel and the gate dielectric [8]. The following relation holds for the VTFTs,

$$S = \frac{qK_BT\left(N_T t_s + D_{it}\right)}{C_G \log_{10}^{e}} \tag{5.6}$$

where q, K_B, T, and t_s are the electron charge, Boltzmann's constant, the absolute temperature, and the active layer thickness, respectively [8]. Hence, increasing the gate capacitance (C_G) by decreasing the gate dielectric thickness enhances the transistor performance in the subthreshold region of operation. From Figure 5.8, it is clearly observed that the lowest *S* value is obtained from the VTFT with the thinnest SiN_x gate dielectric.

5.4 Nanocrystalline Silicon (nc-Si) VTFTs

Another approach to boost the performance of the VTFT is the application of nc-Si as the active layer of the transistor. The nc-Si:H consists of small crystallites (40-1000Å) embedded in an amorphous matrix. It is deposited at substrate temperatures of 150-300 ºC from the strongly H_2-diluted Silane (SiH_4) by various types of PECVD [9]-[11],

HWCVD [12], or the layer-by-layer (LBL) technique [13] which is the alternative deposition of several amorphous silicon layers and the exposure to H_2 plasma.

The properties of this material such as the crystalline fraction and carrier mobility depend mostly on the hydrogen dilution. The effect of the hydrogen atoms on the network structure of nc-Si has been studied [14], [15]. Three possible roles of H atoms during the deposition process have been proposed: (1) The hydrogen coverage of the growing surface enhances the diffusion of the adsorbed radicals such as SiH_3 and SiH_2 (2) hydrogen radicals act as the etchant of the Si surface (weak Si-Si bonds) and create a chemical equilibrium between the deposition and etching of the growing surface and (3) hydrogen atoms penetrate into several layers below the top surface and promote the network propagation reactions. The deposition temperature also affects the crystalline fraction and crystal grain size; that is, with increasing the temperature, these properties improve [16]. In this work, for the PECVD deposition of the nc-Si, the gas mixture of SiH_4/H_2 (2/100) and substrate temperature of 300 ºC have been employed.

The material properties such as the crystallinity, grain size and the microstructure of nc-Si (gain boundaries and amorphous phase) are also influenced by the film thickness. Previous studies have confirmed that the crystallinity of the material is higher for thicker nc-Si films [17]. At the initial stage of the deposition, the structure of the nc-Si is entirely amorphous or comprises of very small grains (few nano meter) with the dominant amorphous phase [17]. However, as the deposition proceeds, larger and larger crystallites prevail, and the average crystalline size and crystalline fraction increase, as depicted in Figure 5.10 [18].

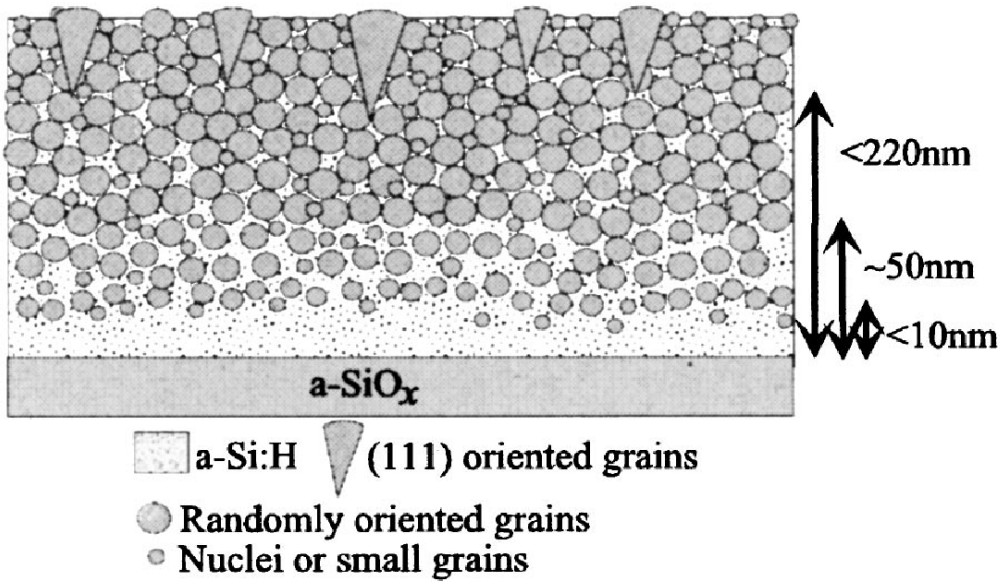

Figure 5.10: Schematic cross-section of nc-Si film illustrating the evolution of material microstructure when the film thickness grows (adapted from [17]).

This important characteristic of the nc-Si that the bottom and top surfaces of the film have different material properties must be considered in the design of TFTs. In the top gate TFTs, in which the gate dielectric and gate metal are placed on top of the active layer, the channel is formed in the highly crystalline segment of the nc-Si film. Therefore, the application of the nc-Si material as the active layer of the top gate TFT enhances the performance of the transistor. On the contrary, in the bottom gate TFTs, the performance of the nc-Si TFT is determined by the quality of the first few deposited layers of the nc-Si film, where the crystallinity is poor.

The VTFT is considered as a top gate device, since the gate insulator and metal are deposited after the nc-Si active layer (see Figure 5.11). Therefore, in a nc-Si VTFT where the channel is formed on the crystalline section of the active layer, the device is expected to exhibit higher ON currents than that of the a-Si:H VTFT. The experimental results indicate that a TFT with nc-Si as the active layer does have a larger ON current than that

of the a-Si:H counterpart [19]. However, high electron mobilities are demonstrated by the top gate TFTs with silicon dioxide (SiO_2) as the gate dielectric. The reported mobilities are in the range of 11-150 $cm^2/V.s$ [10], [20]-[23] and 0.5-2 $cm^2/V.s$ [24]-[26] for SiO_2 and SiN_x gate dielectric TFTs, respectively. The higher mobility of the TFTs with SiO_2 gate dielectric is attributed to the better interface quality of the dielectric with active layer than that in the devices with SiN_x gate insulator.

Despite the higher electron mobility and ON current of the SiO_2 dielectric nc-Si TFTs, the devices suffer from the poor insulating quality of the PECVD deposited SiO_2 at temperatures below 300 ºC [20], [27]. Besides the gate leakage current, the nc-Si:H TFTs have higher drain leakage currents than those of a-Si:H TFTs due to the higher mobility of the nc-Si.

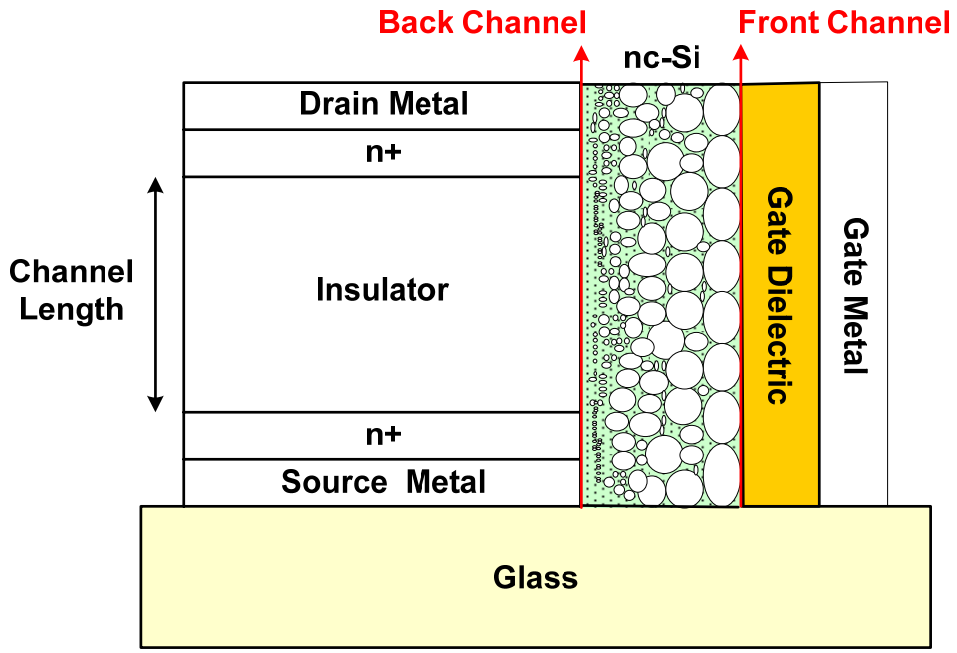

Figure 5.11: Cross section schematic of the VTFT structure with nc-Si as the transistor active layer.

The nc-Si material is fully compatible with the a-Si:H technology, and the fabrication of the nc-Si VTFT is the same as that of the a-Si:H VTFT; the only difference is the deposition of nc-Si:H instead of a-Si:H as the active layer of the device. In this study, the nc-Si film is deposited in PECVD at the pressure of 900mTorr and plasma power of 2W by using highly hydrogen diluted silane (SiH_4/H_2: 2/200). The deposited film on the lateral sidewall has the crystalline volume fraction of over 60% for the film thickness of 20nm, confirmed by Raman measurement [20]. However, the crystalline characteristic of the deposited film on the vertical sidewall has not been studied. Figure 5.12 illustrates the transfer and output characteristics of a 0.5um channel length nc-Si VTFT. The new 50nm thick silicon nitride has been employed as the gate dielectric of the VTFT.

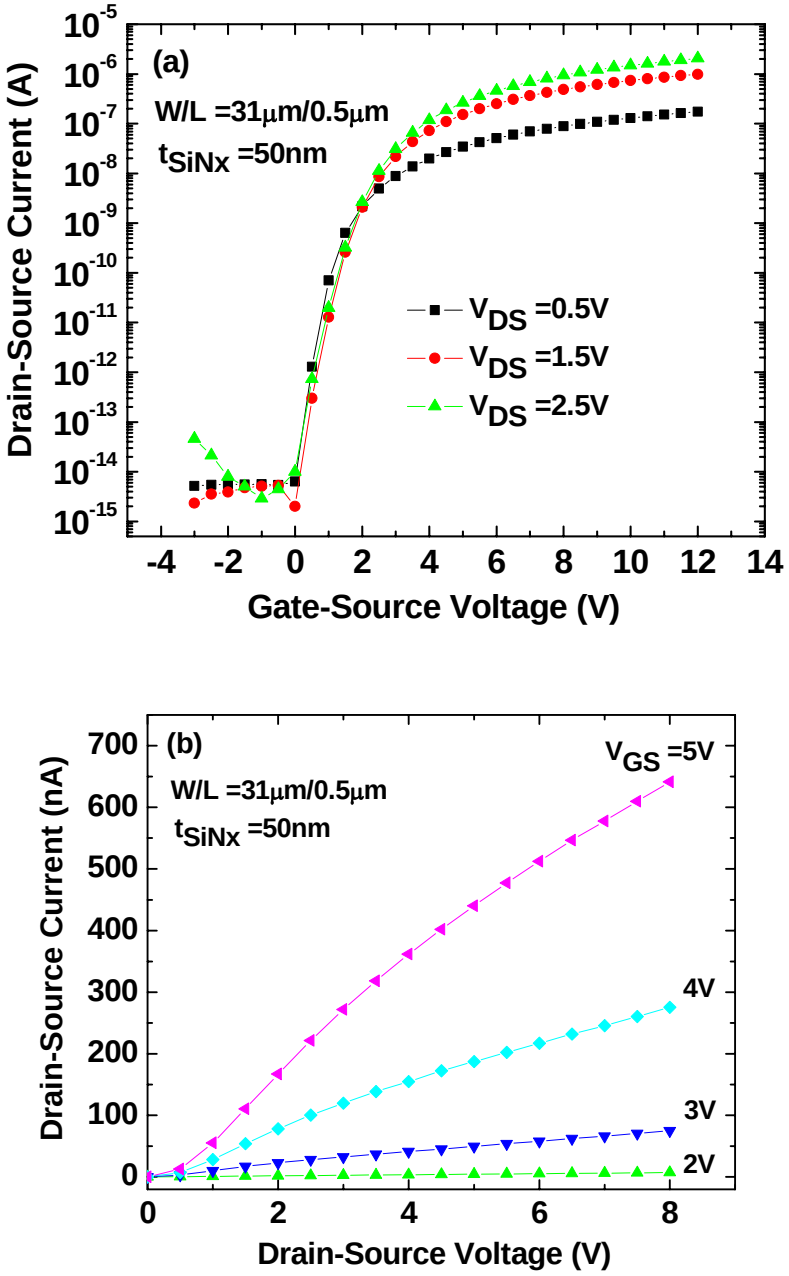

Figure 5.12: (a) Transfer and (b) output characteristics of the nc-Si VTFT with 50nm SiN_x gate dielectric.

The extracted parameters of the fabricated devices are shown in table 5.2. The nc-Si VTFT exhibits an ON/OFF current ratio of more than 10^8, the subthreshold slope (S) of 0.35 V/dec, and the drain-source leakage current of 10^{-14} A.

Table 5.2: Extracted performance parameters of the 0.5 µm channel length nc-Si VTFT with 50nm new SiN_x as the gate dielectric.

Parameter	Extracted Value
Threshold Voltage	1.9V
ON/OFF Current Ratio	$> 10^8$
Subthreshold Slope	0.35 V/dec
Drain-Source Leakage Current	10^{-14} A

As discussed earlier in this thesis, the back channel formation is most likely the responsible mechanism for the leakage current of VTFTs. In the nc-Si VTFT, the back channel component of the leakage current flows through the first few atomic layers called the incubation layer [28], consisting mainly of amorphous silicon. Consequently, as intuitively predicted, the drain leakage current in a nc-Si VTFT should be in the same range of the a-Si:H VTFTs. The measured current-voltage characteristics of the devices clearly confirm this theory.

For a quantitative comparison, the transfer characteristics of the a-Si:H and nc-Si VTFTs at the 0.5 V drain-source bias for the V_{GS} sweep range of -3 to 12 V are plotted in Figure 5.13. The experimental results indicate that although the leakage current roughly remains the same, the ON current of the nc-Si VTFT is almost one order of magnitude higher compared to the a-Si:H counterpart.

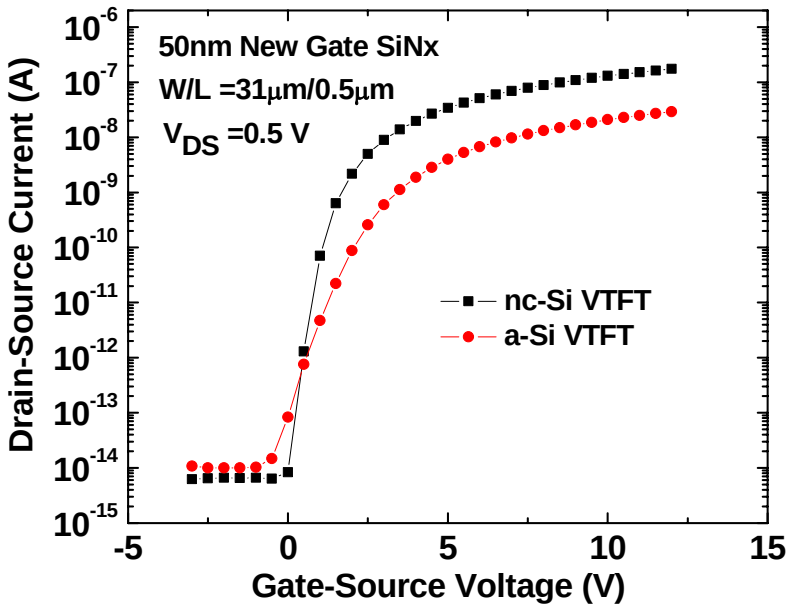

Figure 5.13: Transfer characteristics of the a-Si:H and nc-Si VTFTs with 50nm new SiN_x as the gate dielectric.

In Figure 5.14, the extracted electron field effect mobilities, μ_{FE}, for a-Si:H and nc-Si transistors are depicted. The μ_{FE} is calculated from the transconductance of the TFT operating in the linear region of operation at V_{DS} = 1 V according to:

$$\mu_{FE} = \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)\left(\frac{L}{C_G W V_{DS}}\right) \tag{6.7}$$

where $\partial I_{DS} / \partial V_{GS}$, C_G, V_{DS}, W, and L are the transconductance (g_m), gate dielectric capacitance per unit area, drain-source voltage, width, and length of the TFT, respectively. As it is expected, the extracted mobility of the nc-Si VTFT is six times higher than the mobility in the a-Si:H VTFT (Figure 5.14).

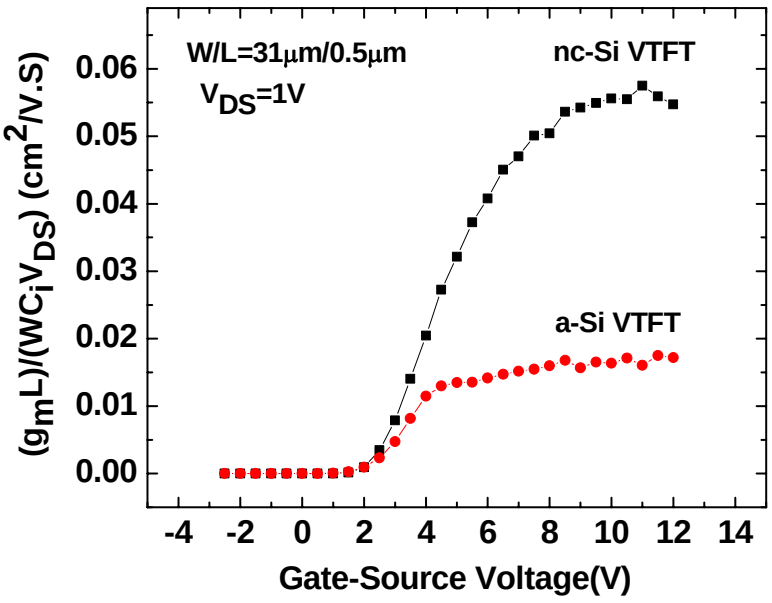

Figure 5.14: Extracted field effect mobilities of the fabricated a-Si:H and nc-Si VTFTs; the SiN_x gate dielectric thickness is 50nm for both devices.

The mobility enhancement is explained by the increase in the crystallinity and the grain size of the active channel, enabling the carrier percolation transport path through the crystalline grains and resulting in a higher mobility [17]. In other words, the higher mobility of the device is the result of the carrier transport through the crystalline grains. Thus, application of nc-Si:H as the active layer of the VTFTs increases the ON current of the transistor while it does not significantly affect the OFF-state drain leakage current. As a result, a higher ON/OFF current ratio is obtained for nc-Si:H VTFTs compared to the a-Si:H counterparts.

The extracted subthreshold slope of the nc-Si and a-Si:H VTFTs are 0.35 and 0.49V/dec, respectively, for the transistors with an aspect ratio of 31um/0.5um and gate dielectric thickness of 50nm. It is proposed that the subthreshold slope, *S*, is correlated with the bulk defect density and the interface state density at the channel/gate-dielectric interface (see (5.6)) [8], [29]. Therefore, the lower value of *S,* extracted from the nc-Si VTFT,

indicates a higher interface quality of the nc-si channel with the newly developed silicon nitride material. Given these facts, by employing the nanocrystalline silicon as the active layer of the VTFTs, the overall performance of these devices can be improved.

To study the interface quality of the newly developed SiN_x with the active layer, the electrical characteristics of a-Si:H and nc-Si VTFTs with the 100nm conventional SiN_x are compared to those of the devices employing 50nm newly developed SiN_x as the gate dielectric. Figure 5.15 represents the transfer characteristic of the a-Si:H and nc-Si VTFTs with 100nm conventional silicon nitride as the gate dielectric. It is evident that no increase in the ON current and no significant reduction in the subthreshold slope are observed for the transistor with nc-Si as the active layer. However, by replacing the conventional SiN_x dielectric with the novel film, both the mobility and the subthreshold slope of the device are improved. Given the fact that, the deposition conditions for the nc-Si material remain the same, the performance enhancement can be associated with the higher interface quality of the nc-Si with the new SiN_x dielectric. That is, the active layer has a lower interface defect density with the new SiN_x than with the conventional SiN_x dielectric.

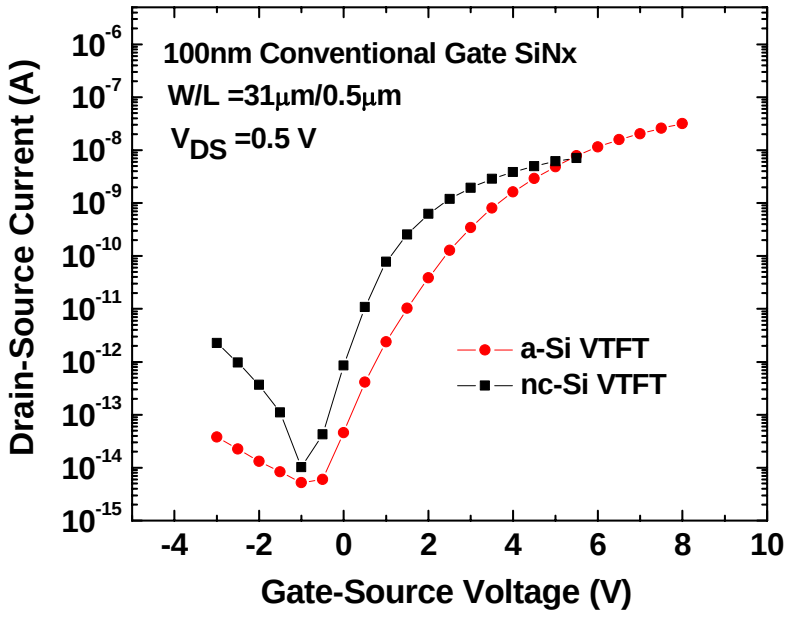

Figure 5.15: Transfer characteristics of a-Si:H and nc-Si VTFTs with 100nm conventional SiNx as the gate dielectric; no performance improvement is observed for the nc-Si VTFT.

5.5 Summary

In this chapter, the reduction of the gate dielectric thickness is demonstrated to be an effective solution to overcome the short channel effects as the channel length approaches the nano-scale regime. It is also pointed out that the newly developed ultra-thin SiN_x has a tremendous potential for application as the gate dielectric of VTFT.

The electrical characteristics of the a-Si:H VTFT with 100nm conventional SiN_x as the gate dielectric reveal the poor performance of the device in terms of low ON/OFF current ratio, high OFF current, and non-saturating behaviour at the high drain voltages induced by the short channel effects. On the contrary, the devices employing 50nm and 30nm-

thick gate dielectric layers exhibit a superior performance compared to that of the former devices. The extracted parameters from the VTFTs with 30nm newly developed SiN_x gate dielectric illustrate the excellent characteristics of the VTFT such as an ON/OFF current ratio over 10^9, a subthreshold slope of 0.23 V/dec, and a leakage current in fA range.

Finally, the fabrication and characterization results for the nc-Si VTFTs are reported. Due to a larger mobility and material structure, a higher ON current is observed for nc-Si VTFT than for the a-Si:H counterpart, while the leakage current remains the same for both types of devices. Also, a higher interface quality is obtained for the nc-Si/ new SiN_x in comparison with the interface of nc-Si with the conventional SiN_x.

5.6 References

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Chapter 6

VTFT AMOLED Displays

Organic light emitting diode (OLED) displays have gained significant attention due to their fast response time, wide viewing angle, high image contrast, and low power consumption [1]-[3]. The architecture of an OLED display consists of a matrix of pixels, each utilizing two or more TFTs for charge transfer to the pixel. Rationally, the physical and electrical characteristics of the employed TFTs determine the performance of the OLED displays.

At present, lateral hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) are widely used in flat panel active matrix displays and X-ray imaging arrays. The a-Si:H TFT-based technology enables device integration over large areas with a high uniformity by a relatively simple fabrication process that can be extended to temperatures as low as 150 $^{\circ}$C for compatibility with plastic substrates [4]. However, TFTs are routinely fabricated in lateral structure that consumes a sizeable portion of the pixel area

particularly when there are large currents needed to be sourced or sinked. The constraining geometrical sizing requirement is enforced to compensate for the relatively low mobility of a-Si:H. Moreover, the TFT size is becoming increasingly important for large area electronics. TFTs with small geometrical dimensions facilitate the high sensitivity operation due to the enhanced fill factor and the high-resolution applications by scaling down the pixel size. For conventional co-planar pixel architectures, where the TFT is placed alongside a sensing or display element, an important figure of merit is the fill factor or aperture ratio. As discussed throughout the thesis, one of the most promising solutions to increase the resolution of the displays of imagers is to employ the VTFT structure where the transistor size is small and channel length can hide between the source and drain.

In this chapter, we focus on the application of VTFTs in AMOLED displays and address the associated issues with the performance, fabrication and reliability of the system. A 2.2-inch AMOLED array is designed and fabricated with 2-VTFT in-pixel driver circuits. Furthermore, two different pixel architectures are utilized to illustrate the enhanced fill factor of the display.

6.1 Organic Light Emitting Diode (OLED)

An OLED is a light emitting diode consist of a series of organic luminescent thin films between two appropriate electrodes [5]. Electrons and holes are injected from the electrodes into the organic layer. The recombination of the injected electrons and holes into the organic material generates excitons, which decay radiatively and produce visible photons. Thus, the brightness level of the OLED depends on the current passing through

the device. Typically, a transistor in the backplane of the display is used to control the flow of current.

Compared to the current LCD display technology, OLEDs have the following advantages [6]:

- Wider viewing angles
- Higher contrast ratio
- Faster response time
- Lower power consumption
- Lighter weight

Despite such superiorities, AMOLED is one of the most demanding applications in terms of the TFT characteristics. To construct the in-pixel circuit driver of an AMOLED display, at least two transistors are required. Moreover, the drive transistor, which supplies the OLED current, must be capable of handling high currents. These constraints dictate the size of the transistors and limit the aspect ratio of the panel. In this chapter, to enhance the performance, the possible application of VTFTs as the circuit elements of AMOLEDs is considered.

6.2 2-TFT AMOLED Driver Circuits

The 2-TFT driver circuit is the simplest pixel architecture employed in AMOLED arrays. The circuit includes a switching TFT (S-TFT), a driver transistor (D-TFT), and a storage capacitor. There are two stages of operation namely the programming and the driving cycles. During the programming cycle, the S-TFT is turned ON, and the data voltage is written from the data line to the storage capacitor, connected to the gate of D-TFT.

Subsequently, the S-TFT is switched to the OFF-state ideally maintaining a constant voltage at the gate of the D-TFT. During the driving cycle, a constant current passes through the OLED that is determined by the data voltage and the characteristics of the D-TFT. Since in AMOLED arrays, the OLED light intensity is proportional to the amount of passing current, the electrical characteristics of the D-TFT specify the quality of operation. This study employs 2-TFT driver due to the simplicity of the circuit and to avoid the complications associated with the design of the more complex circuits.

6.3 VTFT for AMOLED

Among the proposed structure, the VTFT can be argued to have the most promising configuration for high-resolution large area electronics. For lateral structures, the consumed area by the TFT is a function of the channel length and width product (L×W), whereas in VTFTs, the channel length is perpendicular to the substrate and the source and drain contacts are stacked vertically. Therefore, the area occupied by the VTFT is effectively less than half of the lateral TFTs counterpart.

In Chapter 5 it is demonstrated that by thinning the gate dielectric thickness, a VTFT with aspect ratio of 31um/0.5um exhibits an ON/OFF current ratio of over 10^9, a subthereshold slope of 0.23 V/dec, an OFF current in the fA range, and the saturation characteristics in the drain current. Thus, the concerns of poor VTFT performance induced by the short channel effects have been resolved by aggressively reduction of the gate dielectric thickness. Furthermore, the VTFT is capable of flowing currents as high as 10μA at very low V_{DS} voltage of 1.5 V and V_{GS} of 10V. This is very attractive for an AMOLED application in which the luminescence is proportional to the drive current. It is

also reported that 0.5μm channel length VTFTs with newly developed SiN_x gate dielectric have higher fabrication yield compared to the VTFTs employing the conventional SiN_x.

In addition, there is a continuous demand for expanding the active matrix dimensions while maintaining the standard video frame rate. Hence, the address time and as a result the switching time of the TFT must be shortened to maintain the same frame rate. Since the VTFT is a short channel device, it is a promising candidate for high frame rate operation.

6.4 2.2-inch AMOLED Display with 2-VTFT Driver

To confirm the suitability of the VTFT for large area electronics applications, a 2.2-inch QVGA (quarter video graphics array, 240×320 pixels) AMOLED display utilizing 2-VTFT in-pixel circuit drivers is designed and fabricated. Each pixel in the array has an area of 90μm×140μm. In this section, the important factors that are considered in the design of AMOLED arrays are addressed.

6.4.1 Pixel Architecture

There are two architectures for AMOLED displays: 1) bottom emission and 2) top emission, as depicted in Figure 6.1. Typically, bottom emission OLED displays are fabricated on transparent glass or plastic to allow the light transmission through the

substrate. For both architectures, the TFT circuit is fabricated on the substrate and stacked with the OLED material.

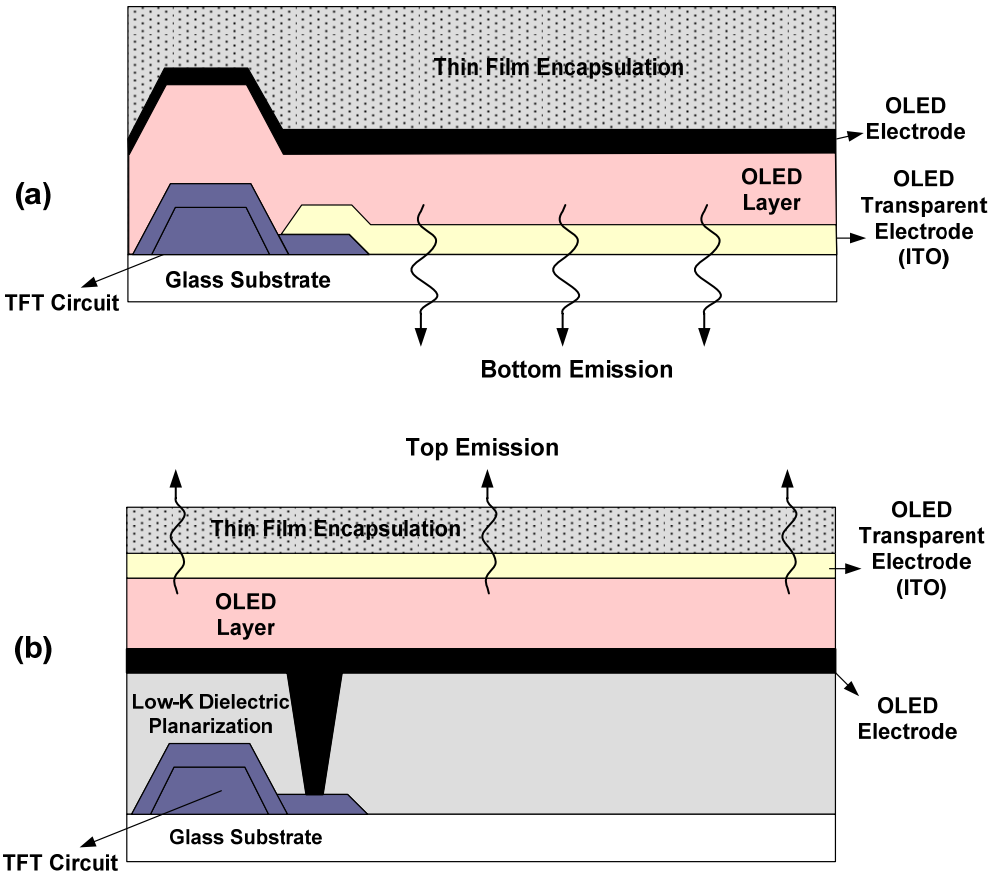

Figure 6.1 (a) Bottom emission and (b) top emission OLED pixel structures.

In the bottom emission structure, the top electrode is a metal and the bottom electrode is a transparent conductor typically from indium tin oxide (ITO) [7]. The major disadvantage of the bottom emission structures is the reduction in the overall aperture ratio due to the area consumed by the driver circuit. Moreover, increasing the size/complexity of the on-pixel circuitry or scaling down the pixel size reduces the aperture ratio.

The other structure is the top emission (Figure 6.1(b)) where the cathode metal is deposited first and subsequently covered by the organic electroluminescent layers and the ITO transparent electrode. Although the top emission architecture provides a higher

aperture ratio, the fabrication process is more challenging due to the larger number of process steps, compared to those of the bottom emission structures. Encapsulation is another hurdle, rendering the top emission structures less attractive. Therefore, the conventional AMOLED displays are based on the bottom emission architecture [8]. In this work, VTFTs are employed in the bottom emission AMOLED backplane to effectively increase the aperture ratio of the display.

6.4.2 Aperture Ratio

As discussed earlier, in AMOLEDs, a high aperture ratio is necessary to ensure a high image quality for the display. Application of VTFTs in the back plane of AMOLEDs is an effective solution to increase the aperture ratio due to the inherent miniature dimensions of the device.

In the circuitry design, a simple 2-TFT driver utilizing the VTFT with channel length of 0.5um and the gate dielectric thickness of 50nm is employed. To demonstrate the enhanced aperture ratio of the pixel, two different pixel architectures are designed, as shown in Figure 6.2. An aperture ratio of 51% is achieved by employing the driver circuit depicted in Figure 6.2 (a). However, it is possible to further boost the aperture ratio to 56% by placing the VTFT between the Data and V_{DD} lines (Figure 6.2 (b)). If the above values for the aperture ratio are compared to the value of 30.5% [9] for the pixels with the conventional lateral TFTs, the excellent potential of VTFT for application in large are electronics is revealed.

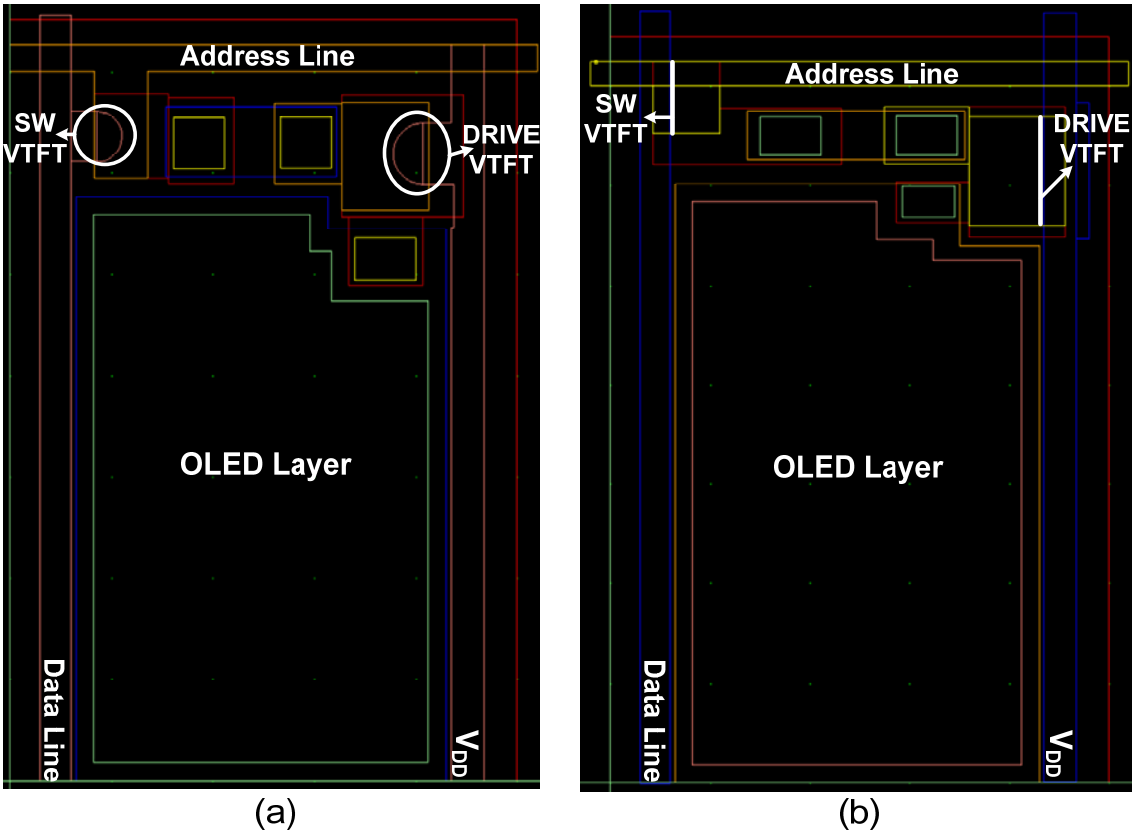

Figure 6.2 Two different driver circuitry employed in a 2.2-inch QVGA AMOLED array.

6.5 Display Fabrication

The fabrication of the AMOLED arrays is a 6-mask process. The VTFTs and metal interconnect layers are first deposited on the glass substrate and then OLED is integrated on top. The first three masks are associated with the formation of the source, drain, and gate of the VTFTs in a process similar to the fabrication of a single VTFT device elaborated in chapter 2. Upon the completion of the first three masks, the data, V_{DD}, and address lines are also defined. Then, for protecting the completed VTFT back-plane, a top-passivation SiN_x layer is deposited and the contact via holes are opened in the fourth

photolithography process. At the end of this step, the fabrication of the array circuitry is complete and the sample is ready for the ITO, OLED, and top electrode deposition. Figure 6.3 shows the optical images of the fabricated array before OLED deposition. The images of the two different fabricated pixel circuits are illustrated in Figure 6.4.

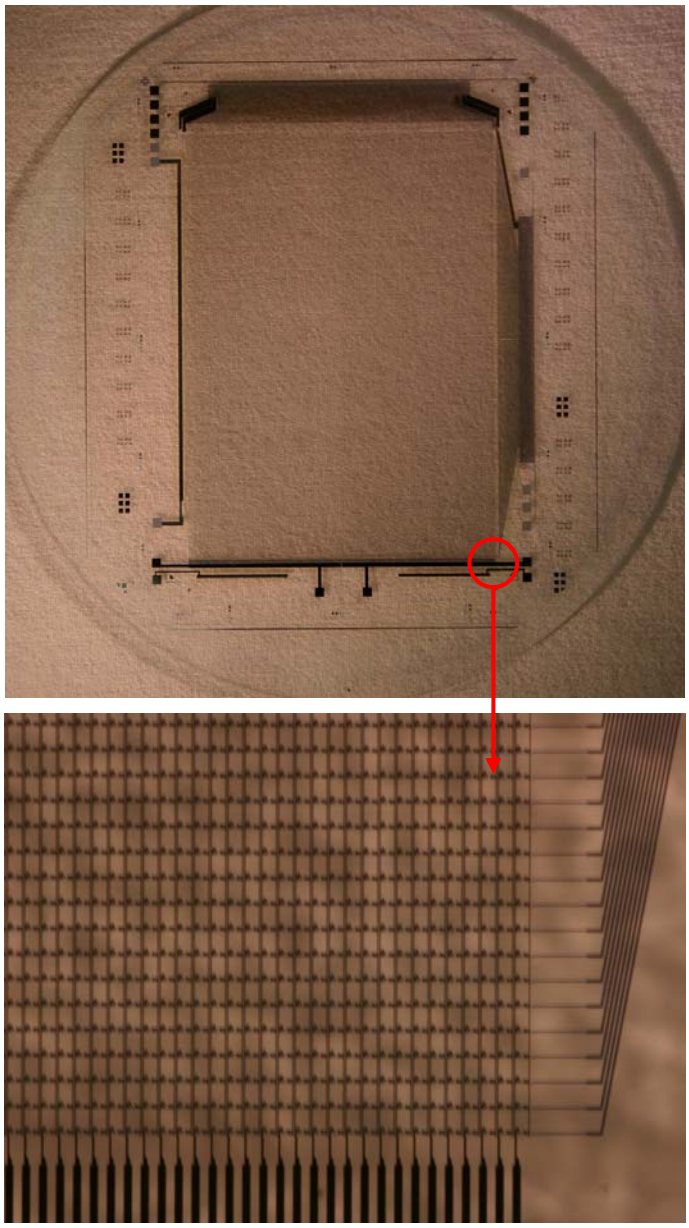

Figure 6.3: Top view images of a fabricated VTFT array before the deposition of OLED.

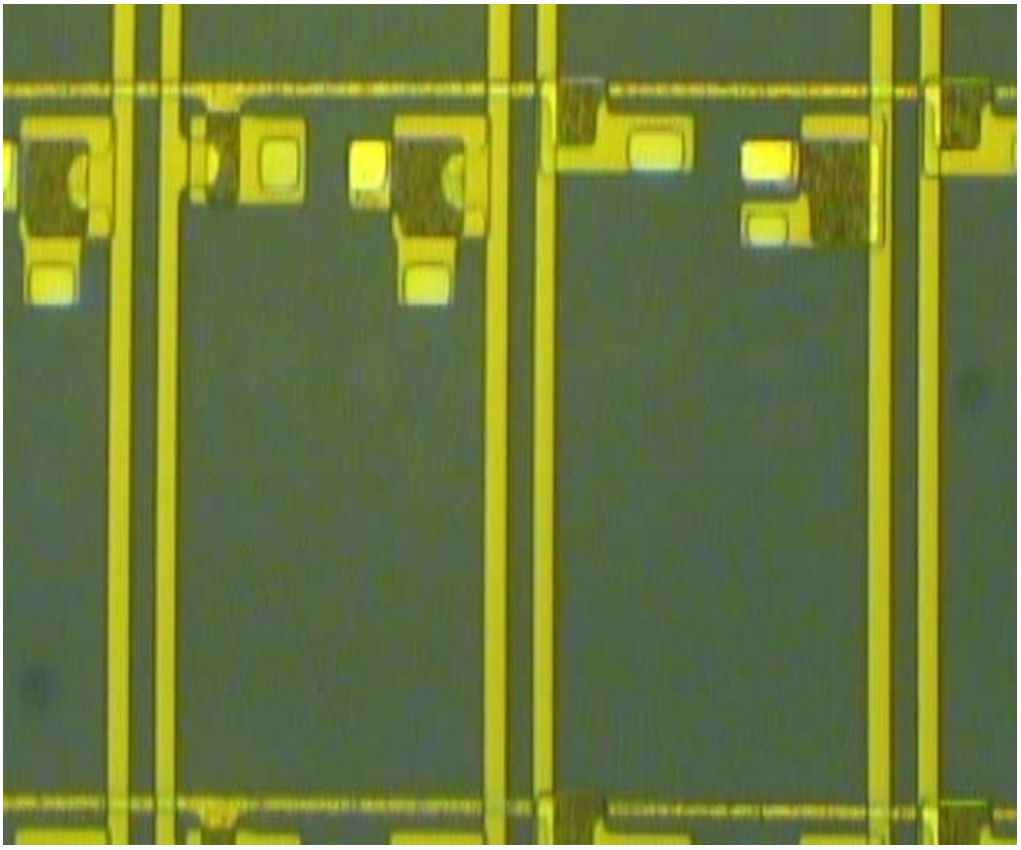

Figure 6.4: Optical image of the fabricated driver circuits.

The next steps are the deposition of the anode, OLED materials and the top conductor. Since the facilities needed for the OLED deposition are not available at the University of Waterloo, the OLED deposition process is conducted at Arizona State University. Masks 5 and 6 are designed based on the OLED process requirement.

The fabricated array is based on the bottom emission architecture; hence the bottom electrode is made of ITO to allow the emission of light through it. Mask 5 is used for patterning the ITO layer as the anode electrode. To define the OLED area, a SiN_x layer is deposited and mask 6 is employed to form the contact vias over each pixel on top of the ITO layer. The organic layer is then deposited over the entire pixel areas by using a shadow mask called the OLED bank. However, the OLED layers are making contact with

the ITO layer only through the defined vias holes. In the next step, the cathode layer is deposited over the area defined by the cathode shadow mask. Finally, the entire structure needs to be encapsulated to prevent moisture and oxygen from degrading the OLEDs.

To ensure the functionality of the addressing matrix, the preliminary electrical measurements are performed on the TFTs and pixel circuits, after the completion of the fourth mask. The experimental results are in good agreement with the data achieved from the VTFT presented in chapter 5. Figure 6.5 demonstrates the average output characteristics, normalized to the transistor width, along with the maximum deviation, obtained from several devices across the fabricated AMOLED panel. However, the OLED deposition and final testing are in progress.

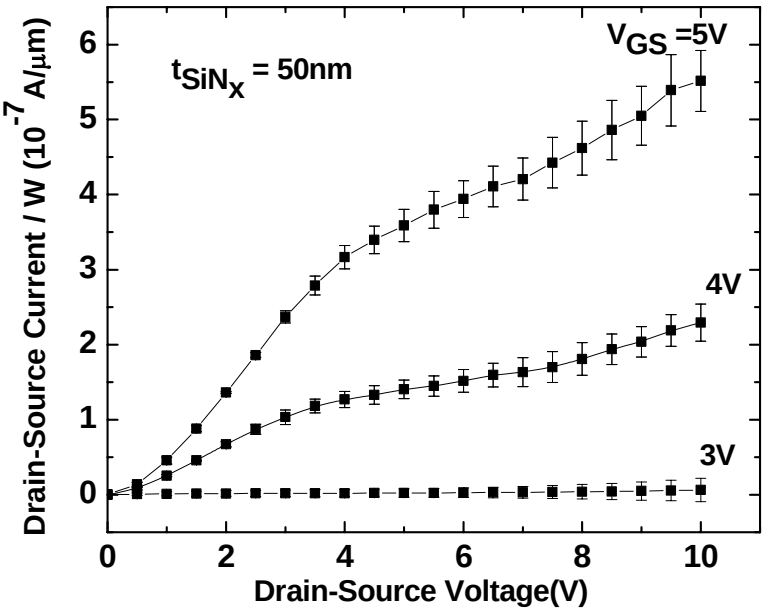

Figure 6.5: Average normalized output characteristics of several devices across the fabricated AMOLED panel at different V_{GS} biases. Error bars at each point illustrate the maximum deviation.

6.6 Summary

To ensure the application potential of the VTFT for large area electronics, a 2.2-inch QVGA AMOLED array with a simple 2-VTFT driver circuit has been designed and fabricated. In the design of the OLED display, two pixel layouts have been considered to demonstrate the capability of the VTFT to enhance the aperture ratio. An excellent aperture ratio of 56% is achieved through the application of VTFT, compared to the 30% value obtained for the conventional TFT. The fabrication results for the back-plane array have been presented to conclude this chapter.

6.7 References

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Chapter 7

Conclusions and Future Work

The aim of this thesis was to address the issues in deploying VTFTs as high performance devices in large area electronics, specifically for high-resolution displays or imagers, in view of its short channel length and small area. Previous fabrication attempts have produced transistors with electrical characteristics plagued by the short channel effects.

The main approach chosen to overcome short channel effects was the aggressive reduction of the SiN_x gate dielectric thickness. Although effective, the scaling of gate dielectric thickness can induce a high leakage current and early breakdown. In this work, the electrical and physical characteristics of the SiN_x films of different thicknesses were examined. Experimental results demonstrate a strong correlation in dielectric failure, its pinhole density, and surface roughness.

To eliminate the sources of high leakage current and early breakdown voltage of thin SiN_x films, a systematic study of the impact of deposition conditions on dielectric

properties was conducted. It is observed that the SiN_x layers produced by PECVD deposition in H_2- or N_2- diluted silane and ammonia precursor gases exhibit excellent dielectric qualities as a result of lower pinhole density and lower surface roughness. However, among the family of deposited materials, SiN_x films produced by a $SiH_4/NH_3/N_2$ gas mixture were preferred due to its higher nitrogen content and reduced pinhole density.

The ultra-thin SiNx was then employed as a gate dielectric so as to alleviate short channel effects on the electrical characteristics of the VTFT. Indeed, 500 nm channel length VTFTs with 50 nm and 30 nm SiN_x gate dielectric demonstrated excellent performance with high ON/OFF current ratio, sharp sub-threshold slope, low OFF-current, and saturating behaviour of the drain current. Moreover, the ON-current of the VTFT was further improved by replacing the a-Si:H active layer with nc-Si, while the OFF-current was not compromised because of the top gate structure. This enhanced performance is only observed for nc-Si VTFTs with the new gate dielectric, suggesting better interface integrity of the nc-Si with the new SiN_x than with the conventional SiNx.

To illustrate the application potential of VTFT for large area electronics, a 2.2-inch QVGA AMOLED array with a simple two-VTFT pixel circuit has been designed and fabricated. A significant improvement in aperture ratio was achieved.

Future Work

Although this thesis represents some effective contributions to improve the functionality of vertical thin-film transistors (VTFT), there still remain several unexplored concerns for further advancement of the device performance. Some of the unresolved issues include the following.

- High Contact Resistance: VTFTs are prone to a high contact resistance at low drain voltages, producing a noticeable current crowding phenomenon in the output characteristics of the transistor. To minimize this adverse effect, additional study is required.

- Low Carrier Mobility: The parameters that are extracted from the transfer characteristics indicate low field effect mobility for fabricated VTFTs. It is speculated that the surface roughness or defects at the vertical sidewall, caused by the dry etching process, significantly affect the quality of the deposited active layer and the gate dielectric. The result is a poor performance of the device in terms of the carrier mobility. Therefore, the optimization of the dry etching process for the formation of the vertical structure and the development of additional treatment processes to minimize the sidewall roughness are essential to improve the field effect mobility and enhance the ON current of VTFTs.