Low Temperature RF MEMS Inductors Using Porous Anodic Alumina

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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ABSTRACT

In today's communication devices, the need for high performance inductors is increasing as they are extensively used in RF integrated circuits (RFICs). This need is even more pronounced for variable inductors as they are widely required in tunable filters, voltage controlled amplifiers (VCO) and low noise amplifiers (LNA). For RFICs, the main tuning elements are solid state varactors that are used in conjunction with invariable inductors. However, they have limited linearity, high resistive losses, and low self resonant frequencies. This emphasizes the need for developing another tuning element that can be fabricated monolithically with ICs and can offer high range of tuning.

Due to the ease of CMOS integration and low cost silicon based IC fabrication, the inductors currently used are a major source of energy loss, therefore driving the overall quality factor and performance of the chip down. During the last decade there has been an increase in research in RF MicroelectroMechanical Systems (RF MEMS) to develop high quality on chip tunable RF components. MEMS capacitors were initially proposed to substitute the existing varactors, however they can not be easily integrated on top of CMOS circuits. RF MEMS variable inductors have recently attracted attention as a better alternative.

The research presented here explores using porous anodic alumina (PAA) in CMOS and MEMS fabrication. Due to its low cost and low temperature processing, PAA is an excellent candidate for silicon system integration.

At first, PAA is explored as an isolation layer between the inductor and the lossy silicon substrate. Simulations show that although the dielectric constant of the PAA is tunable, the stress produced by the required thicker layers is problematic.

Nevertheless, the use of PAA as a MEMS material shows much more promise. Tunable RF MEMS inductors based on bimorph sandwich layer of aluminum PAA and aluminum are fabricated and tested. A tuning range of 31% is achieved for an inductance variation of 5.8 nH to 7.6 nH at 3 GHz.

To further improve the Q, bimorph layers of gold and PAA are fabricated on Alumina substrates. A lower tuning range is produced; however the quality factor performance is greatly improved. A peak Q of over 30 with a demonstrated 3% tuning range is presented.

Depending on the need for either high performance or tunability, two types of tunable RF MEMS inductors are presented. Although PAA shows promise as a mechanical material for MEMS, the processing parameters (mainly stress and loss tangent) need to be improved if used as an isolation layer. To our knowledge, this is the first time this material has been proposed and successfully used as a structural material for MEMS devices and CMOS processes.

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DEDICATION

To my parents, Suresh and Bernadette Oogarah,

Thank you for making me who am I today. Your love and guidance are without a doubt a god send.

To my husband Eric,

Without you, there would be none of this. Thank you for your support, your patience, and your love.

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Chapter 1

1.1 INTRODUCTION AND MOTIVATION

For today's wireless communication devices, the need for high performance components is a constant engineering issue. The global demand for wireless phones and other handheld devices is increasing, as evidenced by the sale of more than 1.15 billion phones in 2007, a 16% increase from last year [1]. In Canada alone, 1.6 million new wireless customers were added to the now 20.1 million users [2]. While the functionality and performance of these devices has improved, manufacturers and foundries are still looking for ways to reduce costs.

An important parameter in realizing high performance RF circuits is the quality factor (Q) of integrated passive devices such as low-noise amplifiers (LNA), voltage controlled-oscillators (VCO) and RF filters. Inductors used in these GHz wireless circuits (< 10 GHz) must display a high quality factor Q (ideally greater than 10), have a high self resonance frequency (above 10 GHz) and must have an inductance of 1-5 nH [3]. And while inductors play a major role in these devices, a low loss device has yet to be successfully integrated with Silicon ICs. The standard low cost silicon CMOS technologies have produced inductors limited to around a quality factor of 10, with self resonating frequencies in the range of 5-20 GHz [3]

To approach this issue, there are several factors that must be addressed in inductor performance. The inductance (L), the quality factor (Q) and the self-resonant frequency (f_{res}). The following section will address these parameters.

By improving the quality of the inductor, the overall performance of many devices will follow suite. This is evidenced by enhanced phase noise performance and reduced power consumption in VCO. A better insertion loss allows for less power needed to compensate for loss in RF filters and a higher Q will improve the gain in LNA's.

While RF integrated circuits (RFICs) are produced by conventional si-CMOS processes [4], the performance of integral passive components is poor compared to those based on SiGe and GaAs [5]. However, the cost of silicon based CMOS processing is relatively lower and the main reason why they are still used today.

Recently, CMOS processing is becoming integrated with microelectromechanical systems (MEMS). Traditionally, the hybrid approach was used to integrate MEMS and CMOS chips on one substrate, connected by various wire bonds. However, this increases complexity in packaging and parasitic losses. A better approach is to build the MEMS device directly on the CMOS chip at the end or prior to the final processing steps. While this approach is beneficial, the thermal budget of additional fabrication steps must be restricted to prevent damage to the CMOS circuit [7].

The work done in this thesis will explore Porous Anodic Alumina as a novel low temperature, low cost material for RF MEMS inductors and show compatibility with standard CMOS processes. Porous Anodic Alumina will be integrated in the design and fabrication of a RF MEMS inductor. This will be shown by the following:

1. Fabrication and characterization of Porous Anodic Alumina as a low temperature MEMS material

2. Planar Inductors built on PAA isolation films on low resistive Silicon Substrates.

3. Bimorph RF MEMS Inductors integrating Porous Anodic Alumina will be fabricated. Porous Anodic Alumina compatibility with aluminum and gold will be demonstrated. The warped devices are tuned by applying a voltage across the terminal allowing the eventual flattening of the device. Thermomechanical and RF simulations show structural and electrical performance.

1.2 THESIS ORGANIZATION

The following chapter will provide a background on porous anodic alumina and its past and current applications. In addition, previous work on improving the performance of inductors will be presented.

This will be followed by the fabrication and characterization of the film. The next chapters will present porous anodic alumina as an isolation layer and structural layer. The modeling, fabrication and testing will be further discussed along with future improvements and conclusions.

Chapter 2

2.1 HISTORY OF POROUS ANODIC ALUMINA

The anodization of aluminum is a decades old electrochemical synthesis that has its roots in corrosion resistance for the automotive industry and has developed over the years as a tried and true method to protect many household items from architectural windows and framing to household cookware [8].

In recent years, this chemistry has attracted much attention to those who work in the nanotechnology field [10-11]. Some of the research includes sensing, optics, biomedical implantation, or as "nanotemplates" for innovative structures such as carbon nanotubes (CNTs) and quantum dots [10-12].

The term "Anodized Aluminum" can also be referred to as Anodic Aluminum Oxide or (AAO), Porous Alumina, Anodic Alumina, or Porous Anodic Alumina (PAA). Due to the confusing amount of acronyms, it will be called Porous Anodic Alumina (PAA) henceforth in this thesis.

Applications of Porous Anodic Alumina

2.1.1 Nanotechnology applications

Recently, the research on self organization in nanotechnology has gained momentum with the use of porous anodic alumina. 1D materials such as nanowires or carbon nanotubes have already shown great promise in applications for quantum devices [10]. By using PAA, researchers have been able to fabricate an inexpensive, high throughput and easily tunable template.

Anodized Porous Alumina has several advantages in the effort to produce Carbon Nanotubes (CNTs). Primarily, they offer consistently parallel pore channels, the ability to engineer varying pore diameters, are optically transparent in the visible spectrum and are resistant to most chemicals except for strong bases and acids [9].

CNTs in PAA have been explored by several groups [10, 11]. The potential applications in electrochemical devices, quantum wires and electrodes for rechargeable Li-batteries are just some of the numerous areas that have been explored.

Most importantly CNTs in PAA can withstand high temperatures, up to a 1000°C; this is more than sufficient to handle the high temperatures of Chemical Vapor Deposition (CVD), which is the most common method for synthesizing CNTs. As shown in Figure 1, CVD offers control over the length and diameter of the CNT. Once the deposition is completed, the PAA template is removed, releasing the tubes.

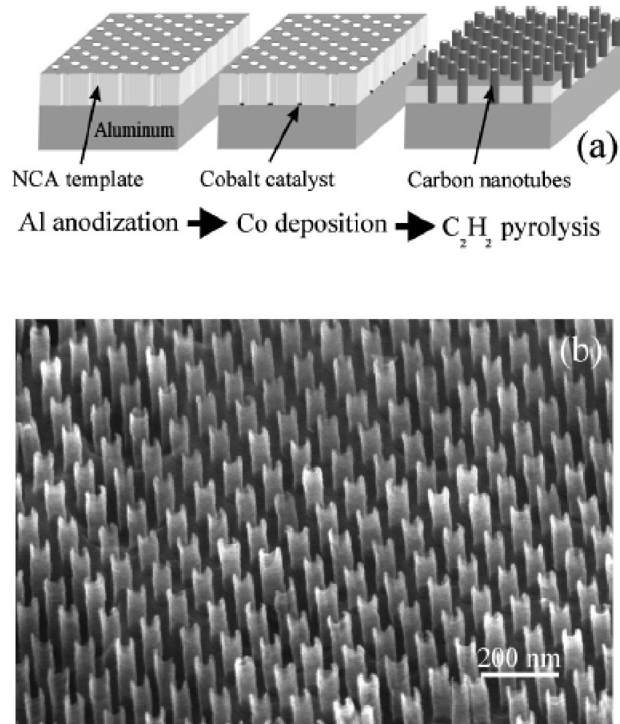


Figure 1: (a) Fabrication Process (b) SEM of CNT using PAA as a template [9]

In addition to CNTs, magnetic nanowires are attracting a growing interest for applications in magnetic storage. By using PAA, one can control the height and diameter of the magnetic wires [11]. The ability to create a dense array of magnetic wires will be a promising candidate for magnetic hard disks with a recording density of up to 1 terabit/in^2.

Several types of metals and alloys have been successfully deposited or electroplated into nanowire structures [12] as seen in Figure 2.

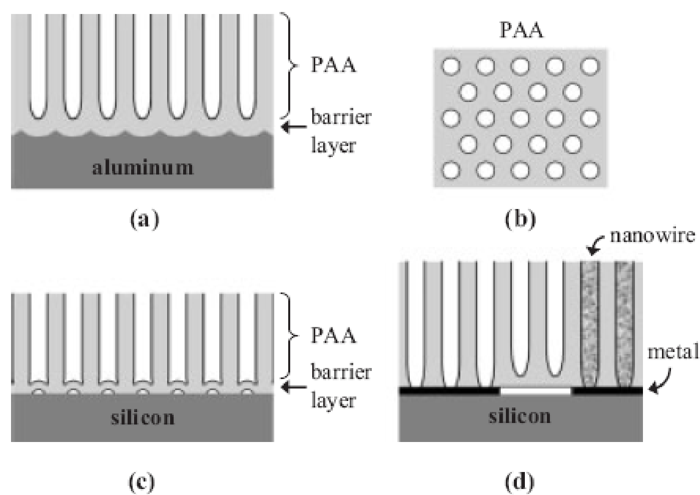


Figure 2: Schematic representation of the process to making nanowires [12]

The optical properties of PAA have been well documented and the material has been utilized in both polarizers and electroluminescent devices [11]. The photoluminescent (PL) properties of PAA are further enhanced when they are filled with semiconductor composites such as CdS or ZnO. These optical nanowires are being utilized in polymer light emitting diodes (PLEDs) and optical displays.

2.1.2 Humidity sensors and biosensors

Due to its hydrophilic properties, PAA is currently used in micro humidity sensors that show good response and are easily fabricated. These devices are based on interdigitated electrodes that take advantage of the sensitive capacitance-humidity relationship [11].

Another interesting characteristic of PAA is its biological properties, and for years, PAA has been used in dental and bone implants due to its biocompatibility and ease of integration with medical implants.

Furthermore, these PAA membranes are now employed as electrochemical biosensors. The membrane acts as a support for enzymes and other biological materials. The sensors shown in Figure 3 have been used to monitor blood glucose levels and for DNA detection [13].

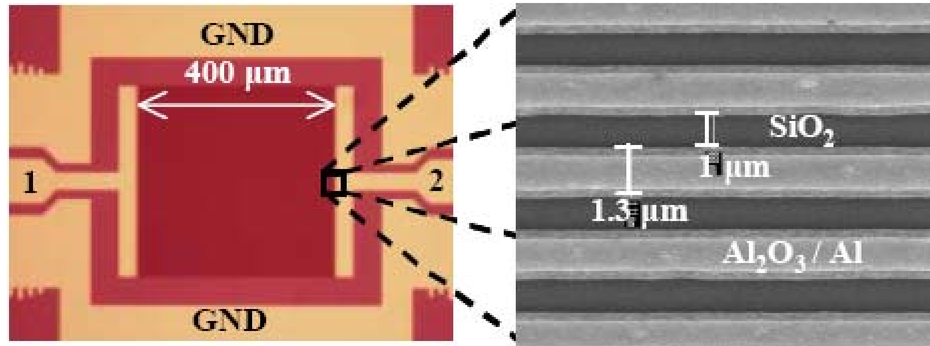


Figure 3: (left) interdigitated capacitor, (right) SEM picture of fingers [13]

2.1.3 RF applications

To date, for RF and microwave applications, PAA has been used mainly as an isolation layer in multilevel circuits. In [22] PAA was formed on a glass substrate to produce Multichip Module Deposited (MCM-D) substrates. In this process, they were able to fabricate several interconnecting layers of porous and barrier layers of PAA as shown in Figure 4. The measured resistance of the layer insulation dielectric layer was on the order of 10^9 Ω·cm much, higher than porous Si [23] at 10^6 Ω·cm.

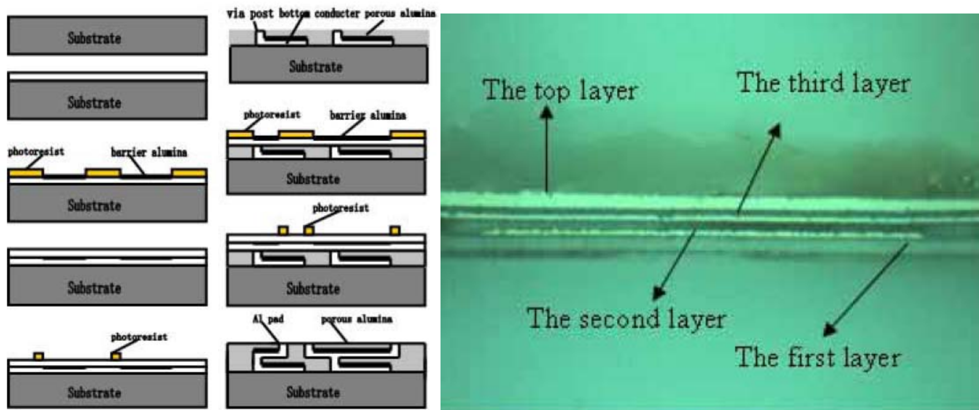


Figure 4: (left) Schematic of aluminum anodization substrate process (right) image of four layer substrate [22].

To improve interconnect delays; PAA was used as a low dielectric material for isolation [24]. Here they introduced a CMOS compatible process where a multilayer system of Niobium and aluminum was used. By selectively anodizing areas, an interlevel alumina insulator was fabricated as shown in Figure 5. A dielectric constant of 4.4 and a breakdown voltage of more than 400 V were reported.

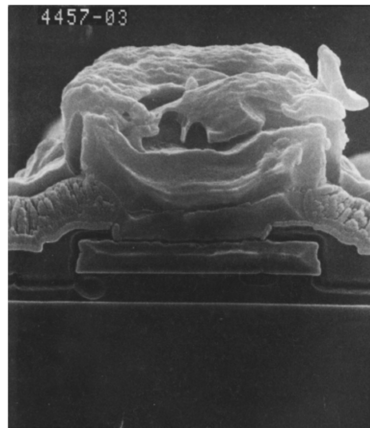


Figure 5: SEM cross-section micrograph of multilevel aluminum interconnections with the interlevel porous alumina insulator [24].

2.2 PREVIOUS WORK ON INDUCTORS AND SILICON

Before we can summarize the recent work on integrated inductors, it is important to understand the fundamental physics and issues when designing inductors.

2.2.1 Model

The most common lumped model is the Π model shown in Figure 6. While it is simple and can easily fit empirical data, it is useful for only a narrow frequency band [14].

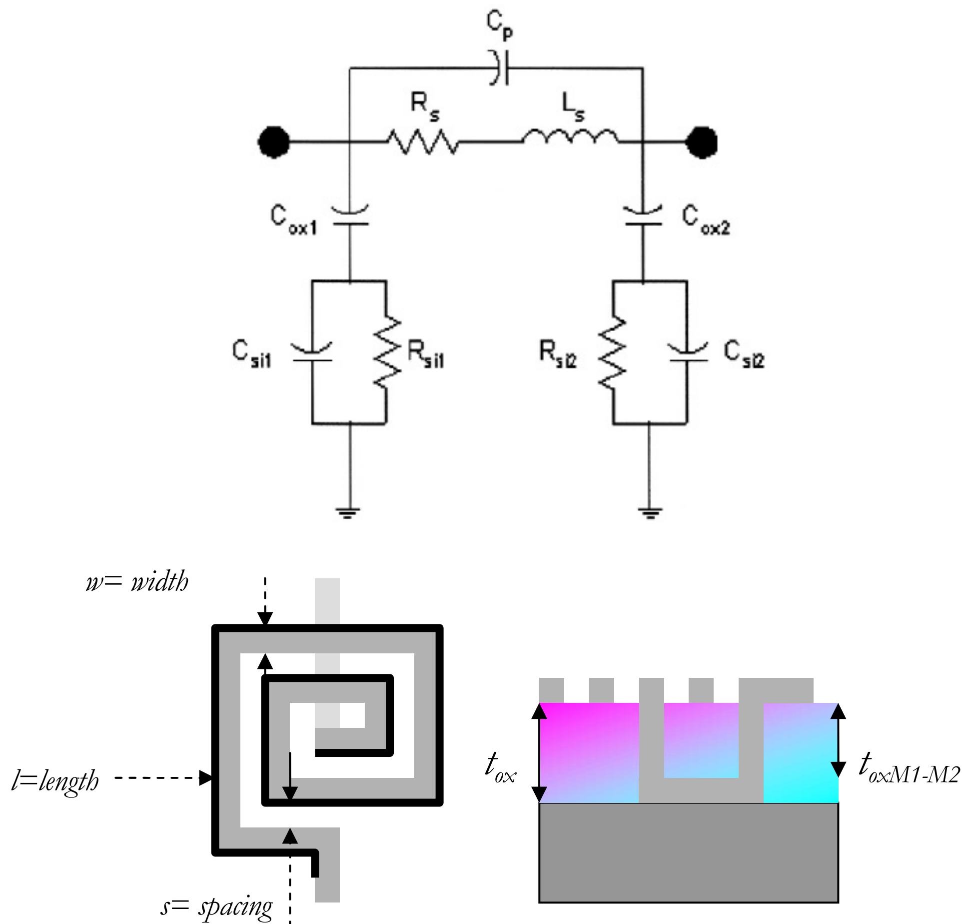


Figure 6: (top) Two Port Π model [14] (bottom) schematic of typical inductor

The model is made up of ideal resistors, inductors and capacitors. These elements are summarized in Table 1.

	Equation	Relation
C_p	$\frac{nw^2\varepsilon_{ox}}{t_{oxM_1-M_2}}$	Capacitance between the underpass and overpass metal strips. This value is normally negligible. n= number of crossing between the coil and central lower connection w = width ε_{ox} = oxide dielectric constant $t_{oxM1-M2}$ = oxide depth between the spiral tracks and its central interconnection
L_s	$n^2\mu\frac{wt}{l}$	Inductance of the coil n = number of turns μ = permeability of the metal w = width t = depth of metal strip l = length of spiral
R_s	$\frac{\rho l}{w\delta[1-e^{t/\delta}]}$	Inductor resistance. Accounting for ohmic losses due to the metal resistance, induced effects in the metallic conductor and magnetic induced currents in the substrate. w = width t = depth of metal strip l = length of spiral δ =skin depth ρ = resistivity
C_{ox}	$\frac{lw\varepsilon_{ox}}{2t_{ox}}$	Parasitic capacitance between metal of the coil and substrate w = width, l = length of spiral t_{ox} = depth of oxide, ε_{ox} = oxide dielectric constant
R_{si}	$\frac{2}{lwG_{sub}}$	Resistivity caused by the ohmic losses in the silicon substrate G_{sub} = substrate conductance per unit area
C_{si}	$\frac{lwC_{sub}}{2}$	Capacitance effect of the substrate due to the silicon substrate characteristics C_{sub} = substrate capacitance per unit area

Table 1: Summary of equations and parameter effects in the Π model (Aguilera)

2.2.1.1 Inductance

There are two components that makeup the inductance of an inductor: self (L_{self}) and mutual inductance (M).

The self inductance of a rectangular conductor as derived by Grover [15] is given by:

$$L_{self} = 2l\left\{\ln\frac{2l}{w+t} + 0.5 + \frac{w+t}{3l}\right\} \tag{2.1}$$

Where L_{self} is measured in nH, and l is the length, w is the width and t is the thickness of the conductor in cm.

The mutual inductance is defined as the ratio between the flux generated by one circuit crossing another circuit. Mutual inductance is positive when the current in two parallel lines is in the same direction and negative when they run in the opposite direction. The mutual inductance is zero when two lines run orthogonal to each other. This is represented by:

$$M = 2lQ \tag{2.2}$$

$$Q = \ln\left\{\left(\frac{l}{GMD}\right) + \left[1 + \frac{l^2}{GMD^2}\right]^{1/2}\right\} - \left\{1 + \frac{GMD^2}{l^2}\right\}^{1/2} + \left[\frac{GMD}{l}\right] \tag{2.3}$$

$$\ln GMD = \ln d - \frac{w^2}{12d^2} - \frac{w^4}{60d^4} - \frac{w^6}{168d^6} - \frac{w^8}{360d^8} - \ldots \tag{2.4}$$

The GMD is the geometric average of the distance between two areas of the two conductors, where w and *d* represent the width and distance, center to center between the two conductors.

As an example, if we look at the inductor in Figure 7, we can summarize the total inductance given by Greenhouse [16] as:

$$\begin{aligned} L_{total} &= \sum L_{self} + \sum M_{+} + \sum M_{-} \\ L_{total} &= L_1 + L_2 + L_3 + L_4 + L_5 + 2M_{1,5} - 2(M_{1,3} + M_{2,4} + M_{3,5}) \end{aligned} \tag{2.5}$$

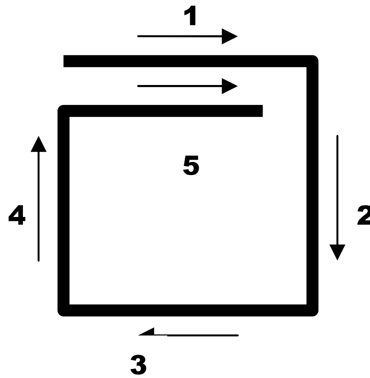


Figure 7: Schematic of coil to demonstrate self and mutual inductance

The Π model can give a better understanding of the inductor performance and pinpoint any integration challenges. From the equations in Table 1, it is obvious that the choice of substrate and metals can have a major influence on the performance. To improve upon the device, the path for any potential losses must be understood. These loss mechanisms are shown in Figure 8.

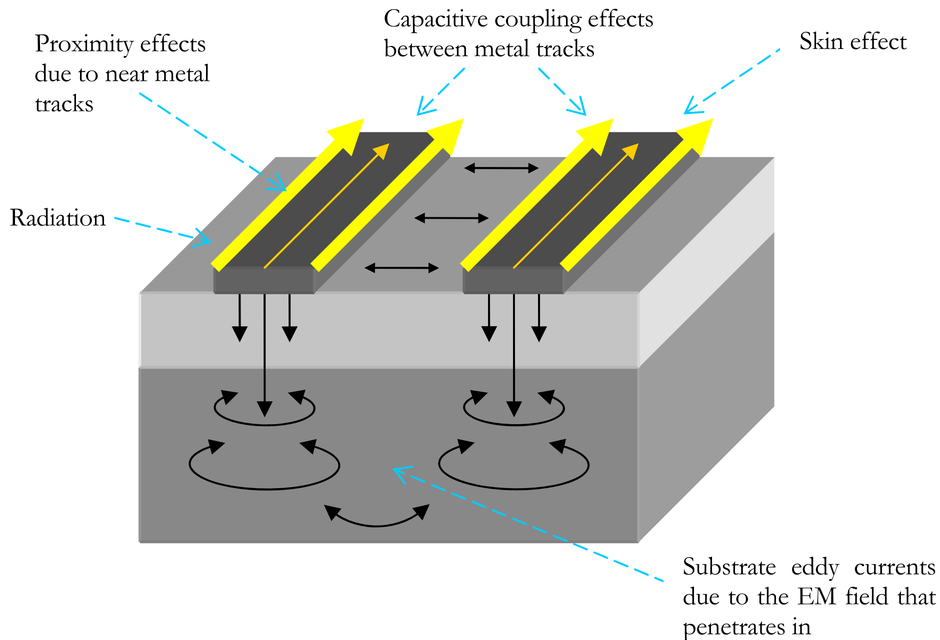


Figure 8: Loss mechanisms for Inductors

These losses and their physical origins will be explained below.

2.2.1.2 Metal losses

Passive elements in CMOS make use of the many metallization layers. For example, a typical inductor is made up of one metal layer parallel to lower tracks of concentric turns, eventually making a full coil. The quality is determined by the conductivity of the metal. At

high frequencies, the current is no longer uniform due to skin and proximity effects. As you increase the frequency, the effective area which the current circulates is decreased. This in turn, increases the current density, creating losses due to the Joule effect [14].

Due to the geometry of the inductor, the alternating magnetic fields penetrate the conductor and create opposing electric fields. This increases the resistivity in the inner section of the inductor, so that the current will likely travel in the outer layer of the conductor. When the time varying magnetic field induces eddy currents in the conductor, this is called *"the skin effect"*. When the time varying fields are produced by neighboring conductors and then influence the main conductor, this is called *"the proximity effect"*.

An important factor that influences these eddy currents is the skin depth (δ)

$$\delta = \sqrt{\frac{\rho}{\pi\mu f}} \tag{2.6}$$

Where ρ is the resistivity, μ is the permeability and f is the frequency. When the metal traces are thicker than the skin depth, the eddy current become negligible. For example, for aluminum with σ= 3.72 x 10^7 S/m, the skin depth is 1.84 µm at 2 GHz and 0.824µm at 10 GHz [17]. For gold, with σ= 4.55 x 10^7 S/m the skin depth is 1.51 µm at 2 GHz and 0.675µm at 10 GHz.

2.2.1.3 Capacitance Losses

As well as the resistance effects of the metal tracks, the capacitance between the metal tracks and the capacitance between the metal and the substrate must be examined.

The series capacitance C_s represents two types of capacitance at work: the first is among and between the metal tracks of the coil (Figure 9), and second is between the coil and the substrate below (Figure 10).

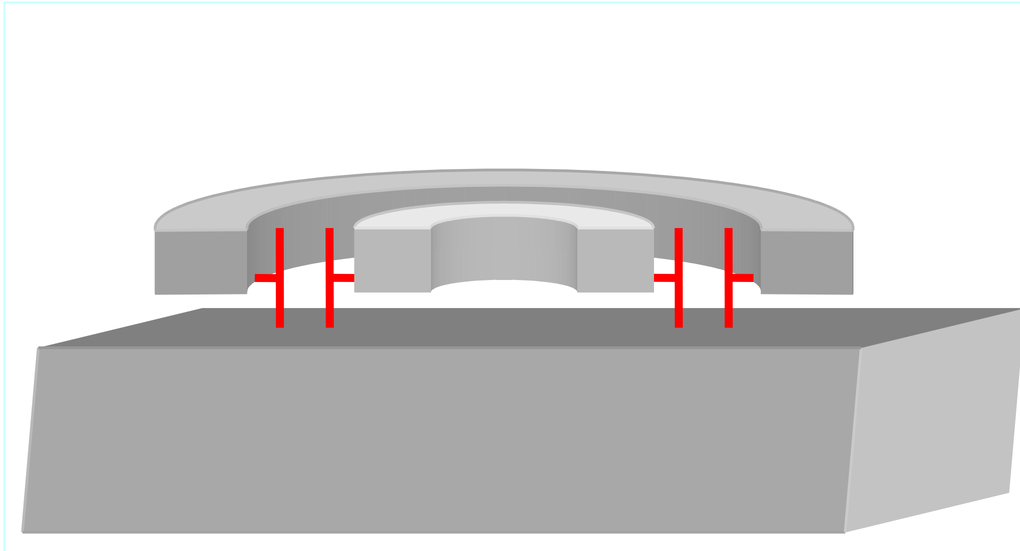


Figure 9: Schematic representation of the parasitic capacitance between metal turns

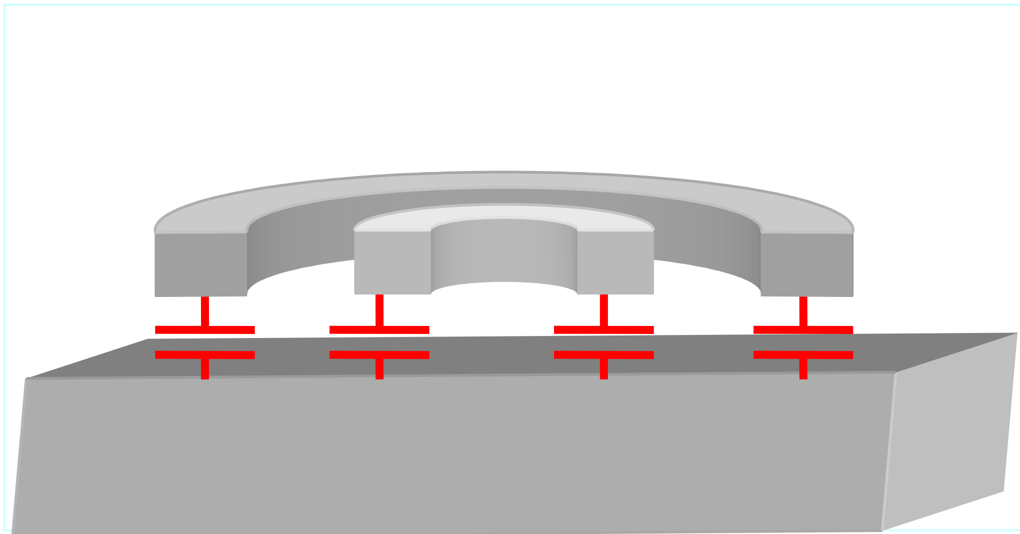


Figure 10: Schematic representation of parasitic capacitance between the metal and substrate.

The first parasitic capacitance loss between the metal turns arises from the metal/oxide/metal or in this thesis work, metal/air/metal structure. The crosstalk that occurs can be neglected [14]. The second loss is due to the metal inductor and the silicon

substrate, which acts as a large capacitor. Depending on the capacitance and frequency, some of this inductor energy will be stored in this structure therefore the inductor will begin to behave as a capacitor. This will occur at the resonant frequency (f_{res}) and this phenomenon can easily be seen on a Smith chart.

2.2.1.4 Substrate losses

The typical low cost silicon substrate is one the greatest sources of loss due to its high conductivity. The effects of this loss occur (i) between the metal layers and the conductive substrate (ii) by induced currents in the substrate due to the varying magnetic fields from the metal layers that penetrate the substrate.

The inductor generates a magnetic field that penetrates into the substrate. This induces a voltage difference, which then generates a current. The energy of the coil, and corresponding quality factor of the inductor decreases.

2.2.1.5 Parameter Extraction

In order to verify the performance of the inductor design, the inductance (L), quality factor (Q) and resonant frequency (f_{res}) must be calculated.

The quality factor is defined as the ratio between the maximum energy stored and the average power dissipated on a duty cycle, or:

$$Q = \frac{\omega W_{\max}}{P_{diss}} = 2\pi \frac{energy_stored}{energy_loss_in_one_oscillation_cycle} \qquad (2.7)$$

As stated earlier, the resonant frequency occurs when the inductor is in resonance with its parasitic capacitances. The device normally operates below this frequency. In this regime, by combining the terms from the one port Π model shown in Figure 11 [18] the quality factor becomes:

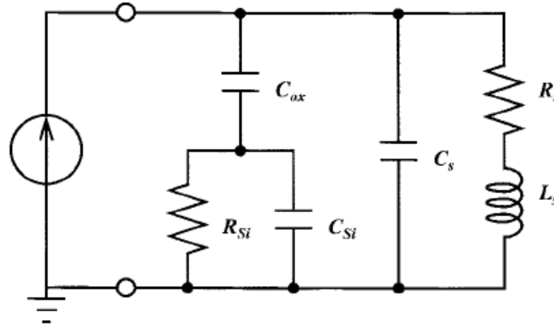


Figure 11: Lumped physical model of a spiral inductor on silicon [18]

$$Q = \left(\frac{\omega L_s}{R_s}\right) \cdot \left(\frac{R_p}{R_p + \left[\left(\frac{\omega L_s}{R_s}\right)^2 + 1\right] \cdot R_s}\right) \cdot \left(1 - \frac{R_s^2 C_o}{L_s} - \omega^2 L_s C_o\right) \tag{2.8}$$

The first term represents the stored magnetic energy and the ohmic losses in the conducting metal layer. The second term is the substrate loss factor representing the energy lost due to the silicon substrate. The last term is the self resonance factor describing the reduction in the quality factor due to the increase in the peak electric energy with frequency and the reduction of Q at the resonant frequency. Therefore by equating this last term to zero, one can calculate the self resonant frequency or:

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{2.9}$$

From Equation (2.9), we see that the spiral inductor has both an inductance and capacitive behaviors.

L_s, R_s, R_p and C_o ($C_o = C_p + C_s$) represent the total inductance, the conductor losses, the substrate losses and the total capacitance.

Both R_p and C_p which are frequency dependent represent the combined effects of $C_{ox,}$ C_{si} and R_{si} so that the general model is then simplified as shown in Figure 12. By making this substitution, the analysis of R_p's effect on the Q and the extraction of the shunt parasitics from the measured S parameters are simplified.

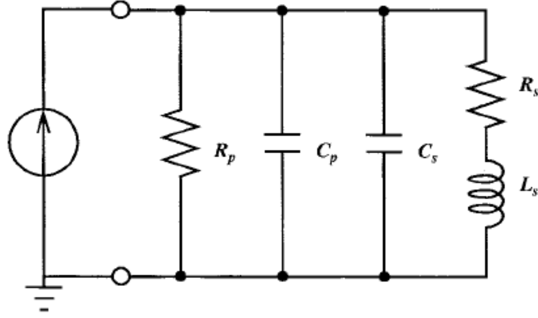


Figure 12: Equivalent model with combined impedance of C_{ox}, C_{si} and R_{si}

Then,

$$R_p = \frac{1}{\omega^2 C_{ox}^2 R_{si}} + \frac{R_{si}(C_{ox} + C_{si})^2}{C_{ox}^2} \tag{2.10}$$

and

$$C_p = C_{ox} \cdot \frac{1 + \omega^2 (C_{ox} + C_{si}) C_{si} R_{si}^2}{1 + \omega^2 (C_{ox} + C_{si})^2 R_{si}^2} \tag{2.11}$$

The L and Q calculations from the S parameters will be further discussed in chapter 4.

2.2.2 Previous Work

There have been several methods introduced in literature with a focus on improving the quality factor of Silicon CMOS based inductors. While silicon CMOS is an attractive high yield low cost production, the conductivity of the substrate remains a problem.

One fairly obvious solution would be to remove the silicon substrate entirely and switch to a more resistive substrate such as quartz, sapphire or high resistive silicon. Unfortunately, this method is not CMOS compatible and the required fabrication costs increase.

This section will summarize some of the most recent methods that have been proposed to improve inductor performance. The first approach is to tackle the substrate itself and explore ways to minimize the loss using standard CMOS planar processes. The second section will look at the MEMS approach using both bulk and micromachining methods.

2.2.2.1 Conventional RFIC Inductors

When an inductor is fabricated on silicon, the substrate is lossy enough to allow the magnetic field of the inductor to penetrate and create eddy currents which work against the inductor. The usual conventional RFIC methods can be categorized as either (i) substrate insulation techniques, or (ii) layout optimization.

Patterned Ground Plane

In the patterned ground approach, metal slots, oriented perpendicularly to the spiral inductor are etched in the ground plane [18]. As shown in Figure 13, these act as an open circuit which impedes the path the of the eddy currents that are generated from the inductor. By using this method, the Q improved from 5.08 to 6.76 (33%) at 2 GHz on a 7.5 nH inductor. While this method is compatible with standard CMOS processes, this

does reduce the resonant frequency of the inductor, thereby reducing its operational performance.

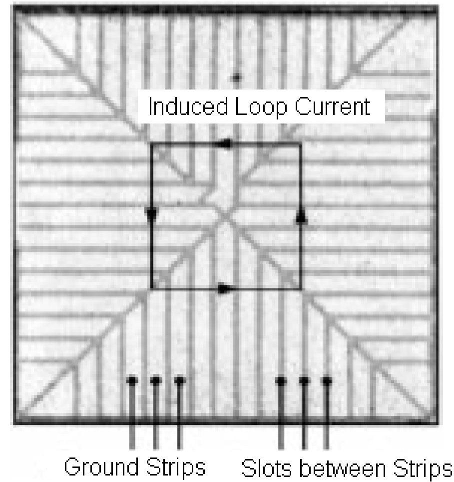


Figure 13: Patterned Ground Shield [18]

Substrate isolation

In conventional RFIC, an oxide is used a dielectric isolation layer to separate the metal inductor and the lossy silicon substrate. However, good quality oxides require high deposition temperatures, while oxides at lower temperatures exhibit poorer quality and structural issues (such as porosity) [19]. Theoretically, a thicker oxide (50 μm or more) would prove better isolation, yet these thicker films have introduced stress issues. This stress is due to the difference in thermal expansion coefficients (CTE) between the silicon substrate and the oxide [20].

One proposed isolation material is porous silicon formed by electrochemical means. Films of 54 μm to 200 μm were fabricated and then sealed with a thick PECVD oxide film. This was done in order to seal the open exposed pores and allow for a smoother metal topology. Figure 14 shows a 4.6 nH spiral inductor fabricated on such layers. They show a quality factor of 11.4 at around 13.4 GHz; a nearly 50% increase compared to the same

inductor fabricated on bulk silicon alone [21]. One of the drawbacks of this material is the need to cover the porous silicon with a capping layer to seal it from the ambient. Otherwise, any subsequent layers will not be completely electrically isolated from the substrate.

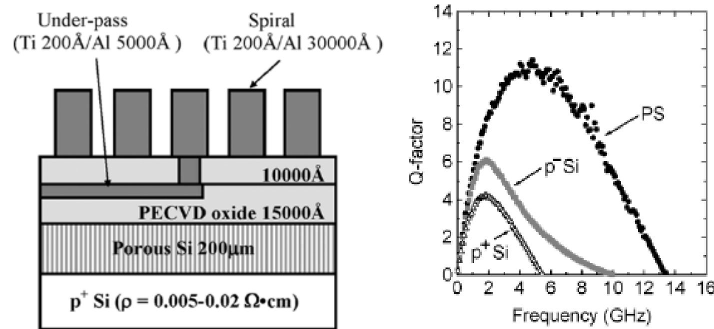


Figure 14: (left) Cross section of device and (right) extracted Q factor for the inductor [21]

Since anodized aluminum has shown promise in planar interconnection systems for IC, planar inductors and capacitors were fabricated on glass substrates using PAA as an isolation spacer and barrier alumina as a capping layer [25]. A peak quality factor of 60 was reported for a 4 turn 400 nH inductor as shown in Figure 15. However, these low frequency (1 kHz-300 MHz) inductors had an area in the millimeter range (high footprint) and were fabricated on glass substrates, making these incompatible with CMOS processes.

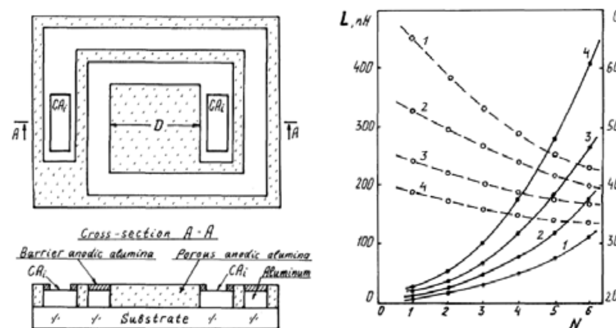


Figure 15: (left) Schematic diagram of the planar inductor (right) Inductance and Q performance as a function of the number of turns [25].

Layout Optimization

It was determined from [26] that the ohmic losses in a spiral inductor are predominant in the outer turns, while the magnetic losses predominate in the inner turns. An algorithm was used to vary the trace width of the metal from a small width in the inner turns, to larger widths at the outer turns. The layout optimized structure is shown in Figure 16. The Q of these inductors was greater than 40 for a 20 nH at 3.5 GHz, a 60% improvement with respect to the single width inductors operating at the same frequency.

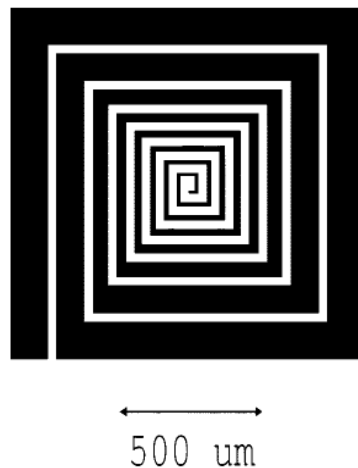


Figure 16: Metal loss-optimized inductor [26].

2.2.2.2 RF MEMS Inductors using Bulk or Surface Micromachining

MEMS technology allows the inductors to be either suspended or levitated in air away from the silicon substrate. This increase in distance reduces the eddy current effects. The use of bulk and surface micromachining methods is presented.

Bulk Micromachining

In bulk micromachining, the lossy silicon substrate is etched away from underneath the inductor using an anisotropic etchant such as KOH, TMAH or EDP. This allows the inductor to be suspended in mid air reducing the substrate losses and the capacitive coupling of the inductor/substrate. This membrane building technique is implemented in standard 2 μm CMOS processes by [27] and in 0.7 μm CMOS processes [28] as shown in Figure 17. While this technique improves the Q (22 at 270 MHz on a 115 nH inductor) and resonant frequency (100 MHz to 3 GHz) there is an issue of fragility, limitations to subsequent wafer processing and increased complexity in packaging.

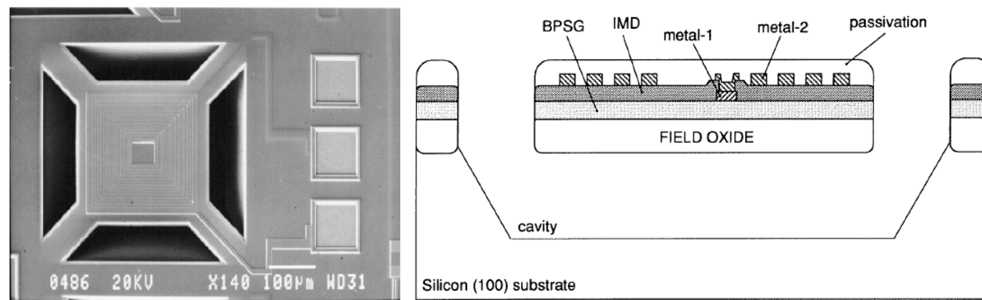


Figure 17: (left) Membrane suspended spiral inductor integrated with 0.7um CMOS process (right) Schematic cross section of device [28].

Surface Micromachining

Though the previous techniques do improve the inductor performance, the remaining parasitic capacitance between the conductive metal and substrate poses limitations [5]. Another approach is to use surface micromachining to build elevated structures away from the substrate. Using a 3D photoresist mould, the structure is electroplated and eventually released as shown in Figure 18. This method resulted in a Q of 16.7 at 2.4 GHz on a 2.67 nH inductor [29]

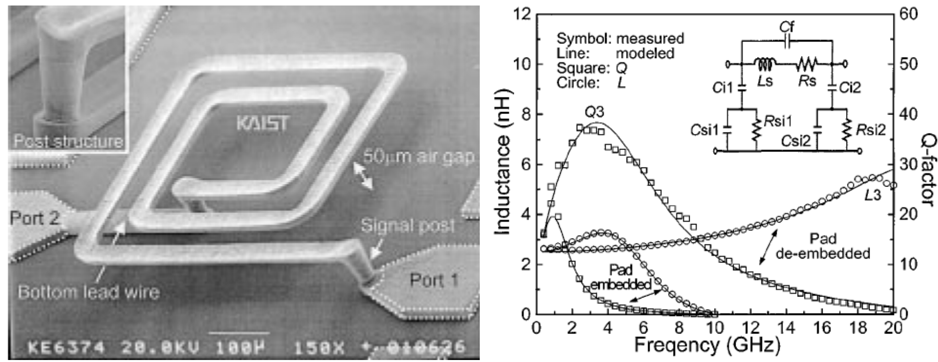


Figure 18: (left) SEM micrograph of elevated inductor (right) Measured and modeled performance of inductor [29].

Self Assembly

Another method of elevating the inductor from the substrate is to use self assembly techniques. These structures are fabricated using a planar batch process, but with an added meltable hinge pad placed at the substrate anchor and the released section of the device. Once the pads are melted, the surface tension force rotates the inductor out of the substrate plane. Figure 19 shows these out of plane inductors that are perpendicular to the substrate and have improved the Q from 4 at 0.5 GHz (released yet not self assembled), to a peak Q of 17 at 3.5 GHz for the same inductor when self assembled at a 90° angle [30].

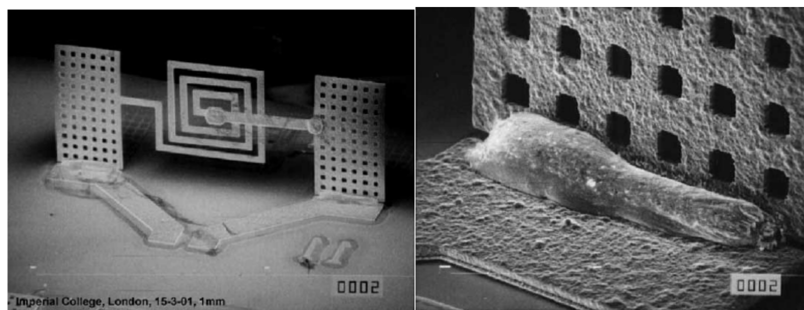


Figure 19: (left) Self assembled out of plane spiral inductor (right) view of solder hinge region after self assembly [30].

RF MEMS Tunable Inductor

Only recently has there been any substantial work done on developing tunable inductors. The benefit of such devices provides optimization and added functionality to many RF components.

The first such device was proposed by Lubecke [31] who used the PolyMUMPS process to fabricate bimorph structures. The inductor bends away from the substrate by means of an interlayer stress caused by using two materials. In this process, polysilicon and chromium-gold metal layers are used as shown in Figure 20. These devices reached a peak Q of 13 at 9 GHz with an L of 1.2 nH.

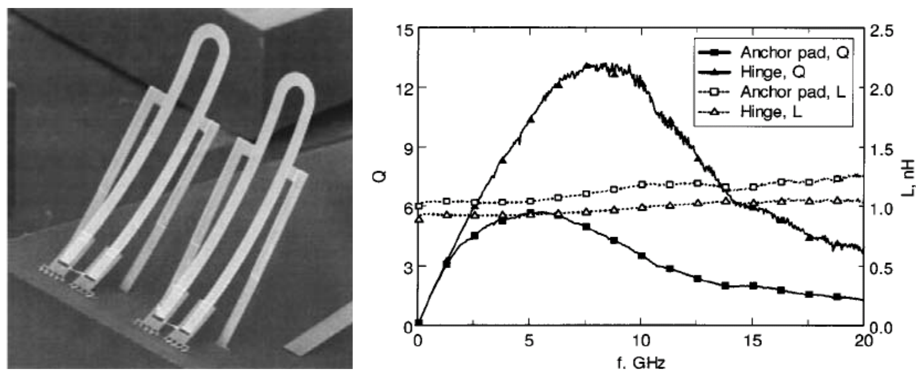


Figure 20: (left) SEM micrograph of hinged Self Assembling Inductor (right) Q and L performance [31].

Another tunable inductor presented in [32] is based on the mutual coupling between two coils. In one state, the actuators displace the external coil, reducing the mutual coupling, and in the other state (rest), the coil remains in the closest position to the other coil, creating a higher mutual coupling. By changing the pitch, the coupling can increase or decrease with tuning based on thermal bimorph structures as seen in Figure 21. Similar to bulk micromachining methods, the substrate was removed by XeF2 etch. This device presented a tuning range of 30% with peak quality factor of almost 25 at 7 GHz.

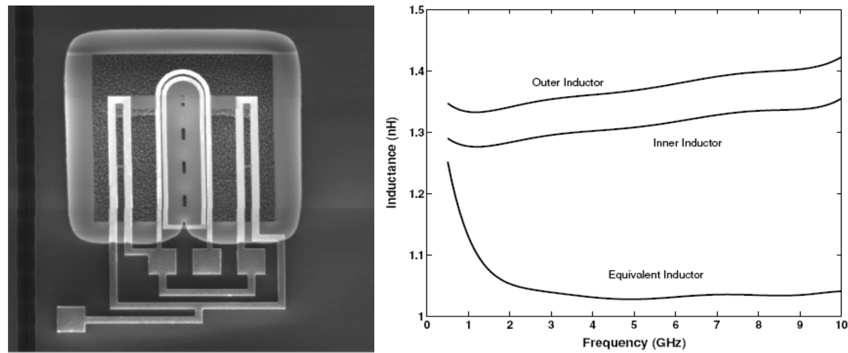


Figure 21: (left) SEM micrograph of tunable inductor (right) measured inductance of the inner and outer coil [32].

More recently a tunable RF MEMS inductor based on amorphous silicon was presented [33]. The bimorph structure of amorphous silicon and aluminum shown in Figure 22 achieved a 32% tuning range with a peak quality factor reaching 15.

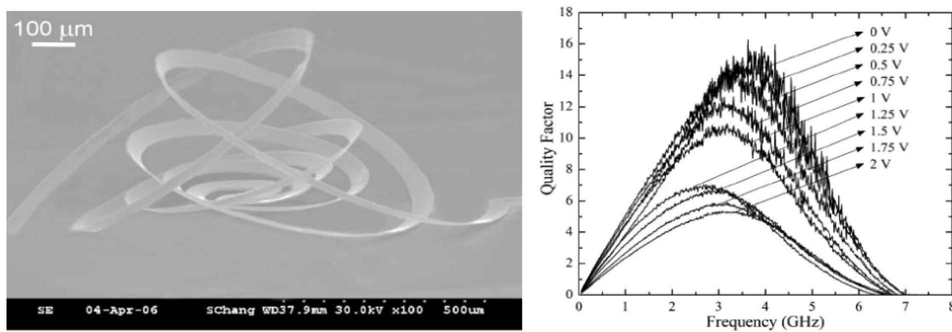


Figure 22: (left) SEM micrograph of warped inductor (right) Quality factor performance [33].

The design structure of the RF tunable inductors presented in this thesis is based on the work in [17]. In this work, we will show how PAA can be a lower cost and lower temperature alternative to many of the tunable inductors presented earlier.

3.1 POROUS ANODIC ALUMINA FORMATION

aluminum has the natural tendency to oxidize when exposed to the atmosphere. The thickness of this native oxide coating, Al_2O_3, can be in the submicron range and is generated to protect the metal surface from further reactions. The term "anodic oxidation" or anodization is defined by the electrolytic process or hydrolysis for producing thicker oxide coatings. The process of anodization further enhances the native oxide, creating a thicker, anti-corrosive layer.

In Figure 23, the two types of anodic films that can be produced are shown: barrier and porous. Barrier type films are formed in insoluble electrolytes ($5 < pH < 7$) such as a neutral boric acid, ammonium borate, tartrate and ammonium tetraborate in ethylene glycol. To create porous films, slightly soluble electrolytes such as sulfuric, phosphoric, chromic and oxalic acids are used [34].

Both types of film consist of a high purity alumina inner oxide and an outer oxide layer composed of alumina with incorporated anions [35]. The inner oxide is adjacent to the oxide-metal interface, while the outer oxide is adjacent to the electrolyte-oxide interface.

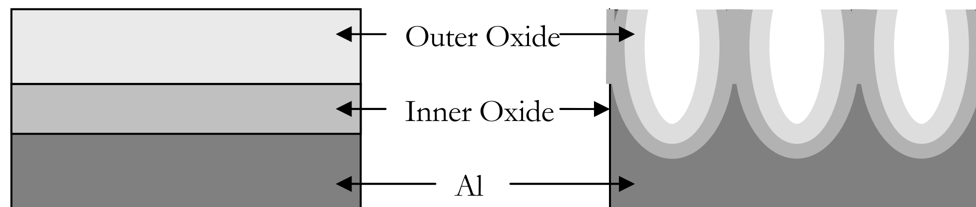


Figure 23: Schematic diagram of (left) barrier type alumina and (right) porous type alumina.

The general principle of electrolysis is as follows: In a bath containing a solution of either a dilute acid or a base (the electrolyte), a cathode of either platinum or any other metal that cannot be dissolved in the solution, is placed with an anode, in this case, aluminum. Figure 24 shows a common anodic cell setup. If one chooses the anode to be made of copper, it would dissolve in the solution and redeposit on the cathode (the basis of electroplating).

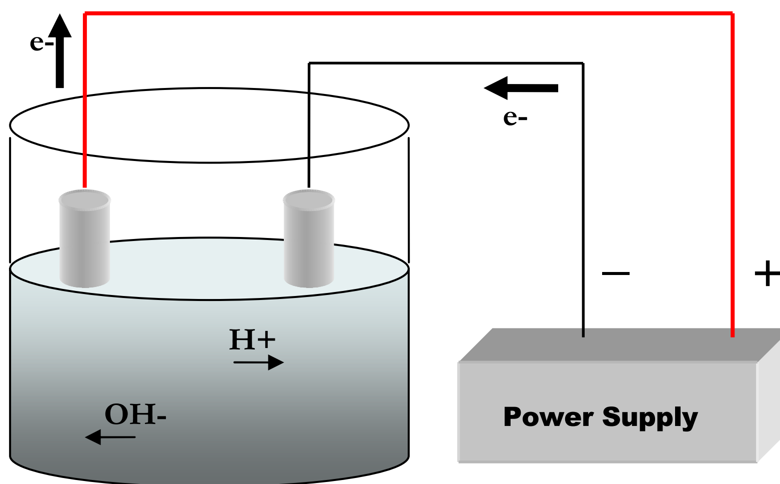
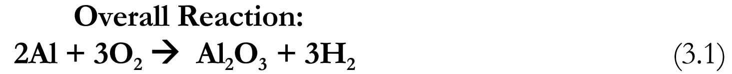


Figure 24: Anodic Cell

Once a voltage or current is applied and the circuit is closed, electrons are withdrawn from the positive terminal. The applied current sets up an electrostatic field in the native oxide. This allows the oxygen ions in the solution to be pulled through the film and react with the metal surface to form the aluminum oxide. At the cathode end, the electrons return to the solution where they react with the hydrogen ions. This causes the formation of hydrogen gas.

This reaction is defined by 3 equations.



Overall Reaction:

$$2Al + 3O_2 \rightarrow Al_2O_3 + 3H_2 \quad (3.1)$$

Reaction at Anode:

$$2Al + 3O_2 \rightarrow Al_2O_3 + 6e^- \quad (3.2)$$

Reaction at Cathode:

$$6H^+ + 6e^- \rightarrow 3H_2 \quad (3.3)$$

The first reaction contributes most of the anodic current, while the remaining equations relate to the growth of the aluminum oxide film with hydrogen gas generated as a by product.

In electrochemistry, the Nernst equation describes the equilibrium reduction potential of a half cell in an electrochemical cell. Assuming there are no complex anions, the Nernst half cell reduction potential equation is:

$$E_{red} = E^o - \frac{RT}{zF}\ln\left(\frac{^{a}\mathrm{Re}duction}{^{a}Oxidation}\right) \quad (3.4)$$

Where R is the universal gas constant, T is the absolute temperature in Kelvin, z is the charge number of the electrode reaction, and F is Faraday's constant.

Solving for equation (3.4), the potential E at the anode becomes:

$$E = -1.550 - 0.0591pH \quad (3.5)$$

Equation (3.5) shows that the reaction that occurs at the anode is thermodynamically dependent on the pH of the solution. By changing the pH, the pore size can vary.

Figure 25 shows the typical voltage time characteristic during a constant voltage anodization. During the first few seconds, a barrier layer is formed on top of the aluminum film. As time continues, the pores begin to develop on top of the barrier layer. The diameters of the pores increase until they are crowded against each other. Once this competition is complete, the pore depths increase and propagate downward and a steady state current is reached. As the aluminum is consumed, the current drops to nearly zero and the anodization is complete.

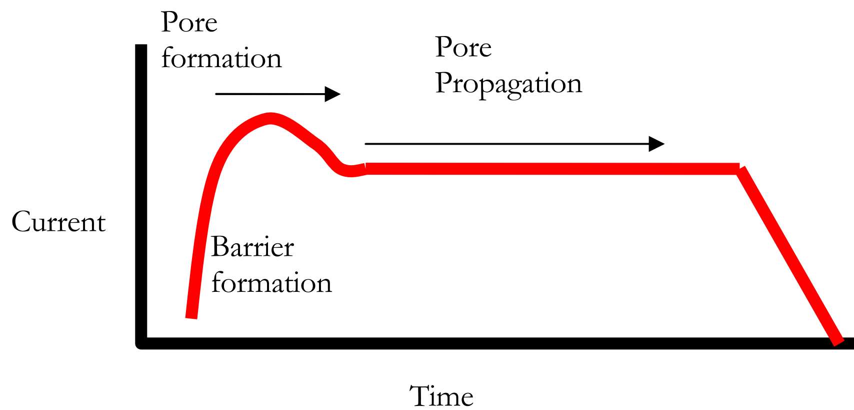


Figure 25: A typical experimental current time characteristic during a constant voltage anodization

The pore formation is shown in Figure 26. Initially, a barrier of protective oxide covers the entire aluminum surface. Once the voltage is applied, an electric field is locally focused on the surface. This is followed by field enhanced dissolution of the formed oxide. Subsequently, the pores continue to grow until they begin to compete with each others surrounding areas. The pore growth will continue to expand in the vertical direction. This will continue until all of the conductive aluminum is consumed.

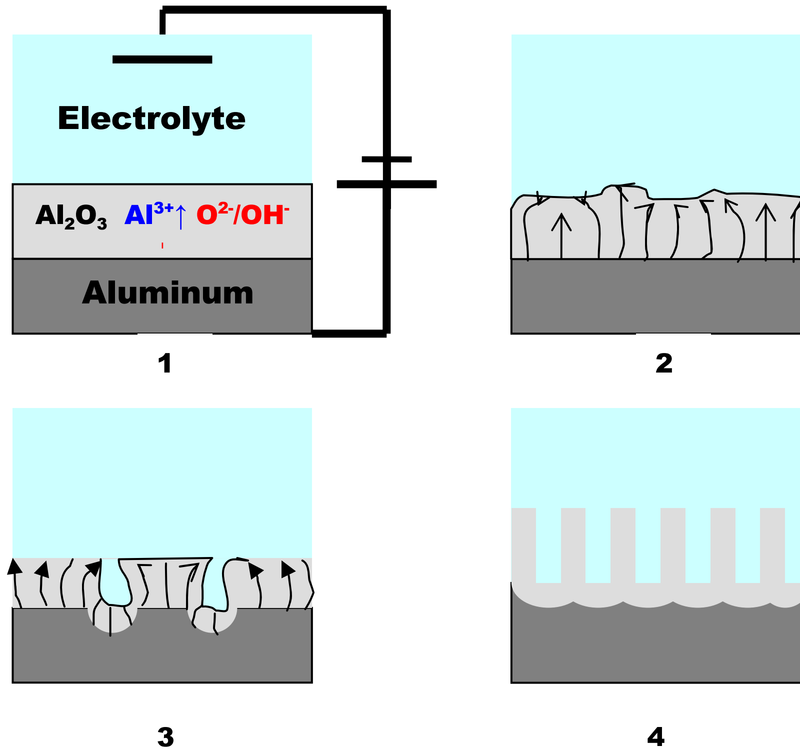


Figure 26: Schematic diagram of the pore formation. (1) formation of barrier oxide over entire surface, (2) local field distributions caused by surface fluctuations (3) initial stages of pore creation cause by dissolution (4) stable and steady pore growth

As aluminum is oxidized, the volume of the aluminum oxide also expands by roughly a factor of 1.4-1.6 of its original thickness. Since this process takes place over the entire metal/oxide interface, the newly created material can only expand in the vertical direction. The geometry of PAA can be described as a honeycomb structure with a high aspect ratio. The cells are shown in Figure 27 and are arranged in a hexagonal array of column-like pores. However, this array is non uniform and randomly spaced [36].

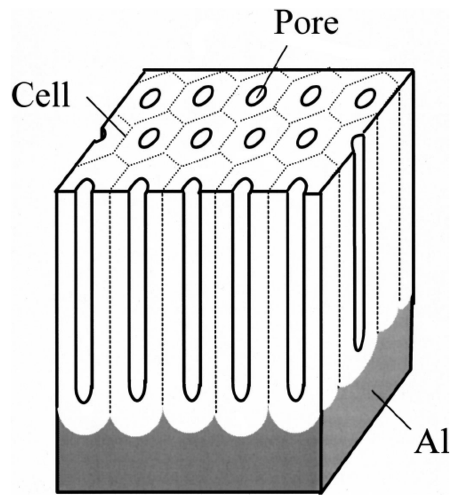


Figure 27: Schematic drawing of an idealized hexagonal PAA structure [36].

The pore and cell diameters are dependent on the choice of electrolyte and its pH value. Pore diameters ranging from 4 nm to over 400 nm as shown in Figure 28, have been fabricated [9, 37]. Some researchers have also been able to develop a more uniform and self organized packing system by using nano-imprinting or two step anodization.

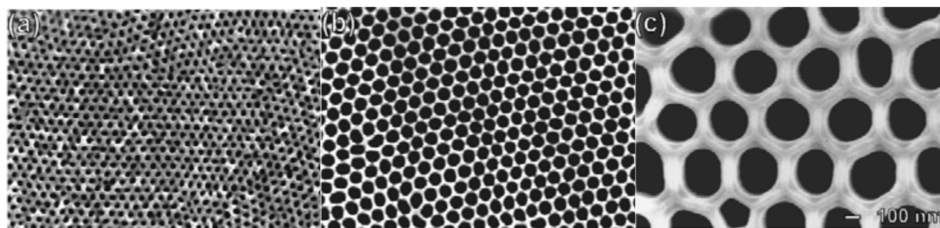


Figure 28: SEM micrographs of PAA. (a) 0.3M sulfuric acid at 25V (b) 0.3M oxalic acid at 40V (c) 10 wt% phosphoric acid at 160V. The pore diameters are 60, 95 and 420nm respectively [9].

Generally, there are several process conditions that can affect the material and electrical properties of the film:

Choice of Electrolyte: Typical electrolyte solutions are dilute sulfuric acid, oxalic acid and phosphoric acid. As the pH of the electrolyte increases, the applied voltage increases. a circulating cooling bath is often incorporated into the experimental setup as this increase in voltage will also increase the temperature of the solution.

Typically, electrolyte solutions containing sulfuric acid generate the smallest pore diameters; on the order of 50-70 nm with phosphoric acid give a pore diameter of 420 nm or higher.

By changing the pore size, the dielectric constant can be either as low as 1 (with a high porosity), or as high as 10 (with a low, more dense porosity).

Temperature: Changing the temperature of the electrolyte solution will affect the stress and surface roughness. During anodization, there is an excessive amount of heat that is generated. Without adequate cooling, this heat will cause stress in the film and cracks will develop, with the film eventually peeling and falling off of the underlying aluminum film.

Voltage: The applied voltage to the sample can change the desired pore diameter.

3.2 FILM CHARACTERIZATION

Once the anodization process was developed, the film characteristics, both physical and electrical were investigated and summarized. Some of these values are verified in this work, while others are referenced.

3.2.1 Surface Roughness of PAA Film

Films of 1 μm and 2 μm PAA were anodized on glass wafers. To measure the surface roughness of the film, a Veeco optical profiler was used to calculate the average roughness and is shown in Figure 29 and Figure 30.

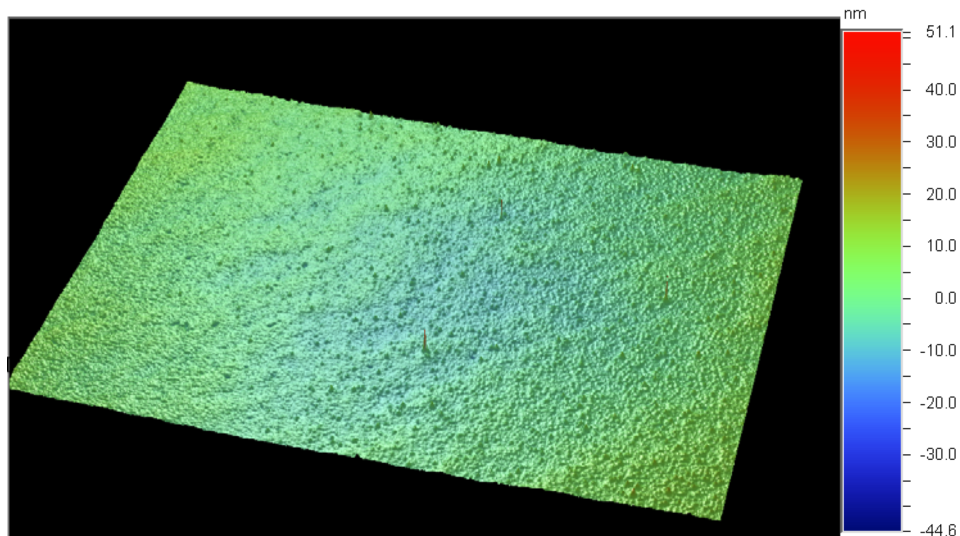


Figure 29: Surface Roughness of 1μm PAA (top) at 5x magnification

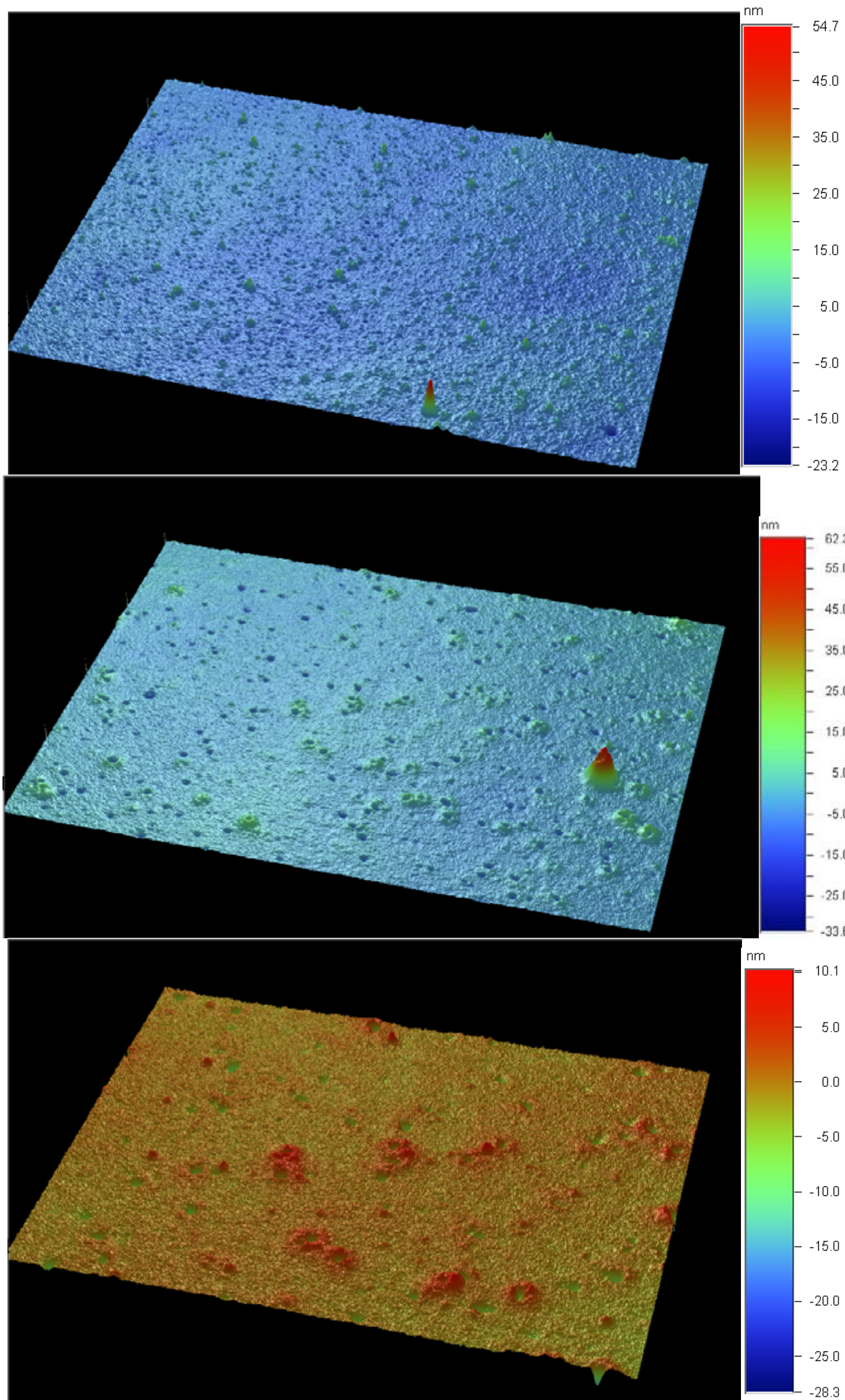


Figure 30: Surface Roughness of 1μm PAA (top) at 10X magnification, (middle) 50X magnification, (bottom) 100X magnification

The profiler can measure the average roughness of the PAA film over a certain area. For a 45 x 59 μm^2 area, the average roughness was 1.30 nm at 100X magnification. As seen in the middle and bottom of Figure 30, at these magnifications the pores of the PAA are clearly visible.

3.2.2 Maximum deflection

In order to verify PAA as a viable structural material for MEMS production, several test structures were fabricated. Bimorph cantilever beams of varying lengths were made and the deflection was measured.

For a bimorph cantilever beam as in Figure 31, the radius of curvature can be calculated as [38]:

$$\frac{1}{r} = \frac{6b_1b_2E_1E_2t_1t_2(t_1+t_2)(\alpha_1-\alpha_2)\Delta T}{(b_1E_1t_1^2)^2+(b_2E_2t_2^2)^2+2b_1b_2E_1E_2t_1t_2(2t_1^2+3t_1t_2+2t_2^2)} \tag{3.6}$$

Where b is the width, t is the thickness, α is the coefficient of thermal expansion, E is Young's modulus and ΔT is the temperature change. The subscript 1 and 2 refer to the top and bottom layers respectively.

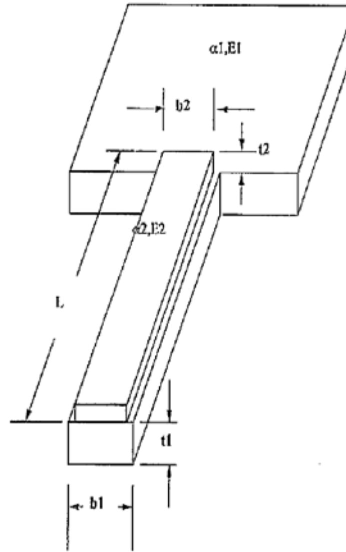


Figure 31: Schematic of a bimorph cantilever beam [38].

Since the materials used in this thesis have a Young's moduli on the same magnitude, we can simplify the above equation to:

$$\frac{1}{r} = \frac{3\Delta\alpha\Delta T}{8t} \tag{3.7}$$

Where Δα is the difference in the coefficient of thermal expansion and t is the total thickness of both layers in the beam.

The vertical tip deflection is

$$d = \frac{l^2}{2r} \tag{3.8}$$

Where *l* is the free deflection length. If *l* << r, then the equation for the deflection becomes:

$$d = \frac{3l^2 \Delta\alpha \Delta T}{16t} \tag{3.9}$$

From the above equation, we can see that in order to maximize the tip deflection, the Δα and the ΔT must be large. Using the structure in Figure 32, the tip deflection of various structures as a function of ΔT was calculated.

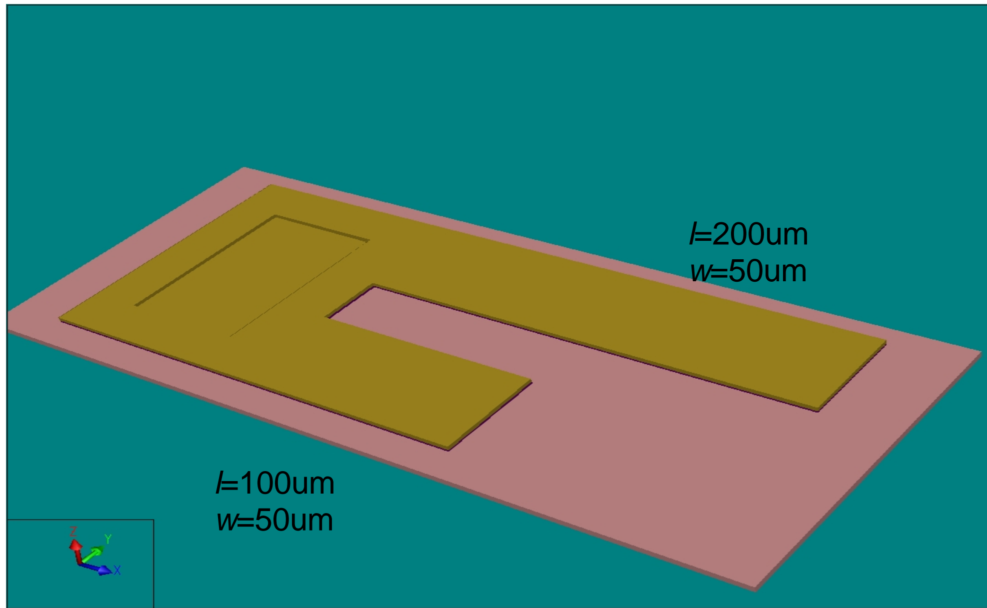


Figure 32: Schematic of the bimorph cantilever beams

From the values listed in Table 2, it is obvious that a bimorph structure of aluminum and PAA will give a higher deflection than gold and PAA. However, the excellent conductivity properties of gold are attractive to many RF applications.

Material	Coefficient of thermal Expansion (1/K)	Maximum Tip deflection
gold	14×10^{-6}	0.027 ΔT
PAA	6.8×10^{-6}	
aluminum	25×10^{-6}	0.068 ΔT
PAA	6.8×10^{-6}	

Table 2: Calculated tip deflection for bimorph cantilever beams

To verify these conditions, bimorph structures were fabricated in the process in Figure 33. After the p-type <100> 8-12 Ω·cm silicon wafer was cleaned using a standard RCA-1 recipe, it was then coated with a 2 μm photoresist sacrificial layer. The anchors were then patterned and after hard baking to prevent any further outgassing, 1μm of aluminum was sputtered. The maximum temperature inside the sputtering chamber reached almost 70°C. The aluminum film was then anodized in a 0.3M oxalic acid solution for 5 minutes or until the film became transparent. For the aluminum/PAA bimorph structures, another 2 μm of aluminum was sputtered. For the gold/PAA bimorph structures, a thin 100 nm layer of gold was sputtered, followed by another 2 μm of electroplated gold. The top layer for both substrates was patterned and etched, followed by the etching of the PAA. To remove the sacrificial layer, Reactive Ion Etching (RIE) was used to release the beams. Due to the residual stress in the layers, the beams are warped upwards after release.

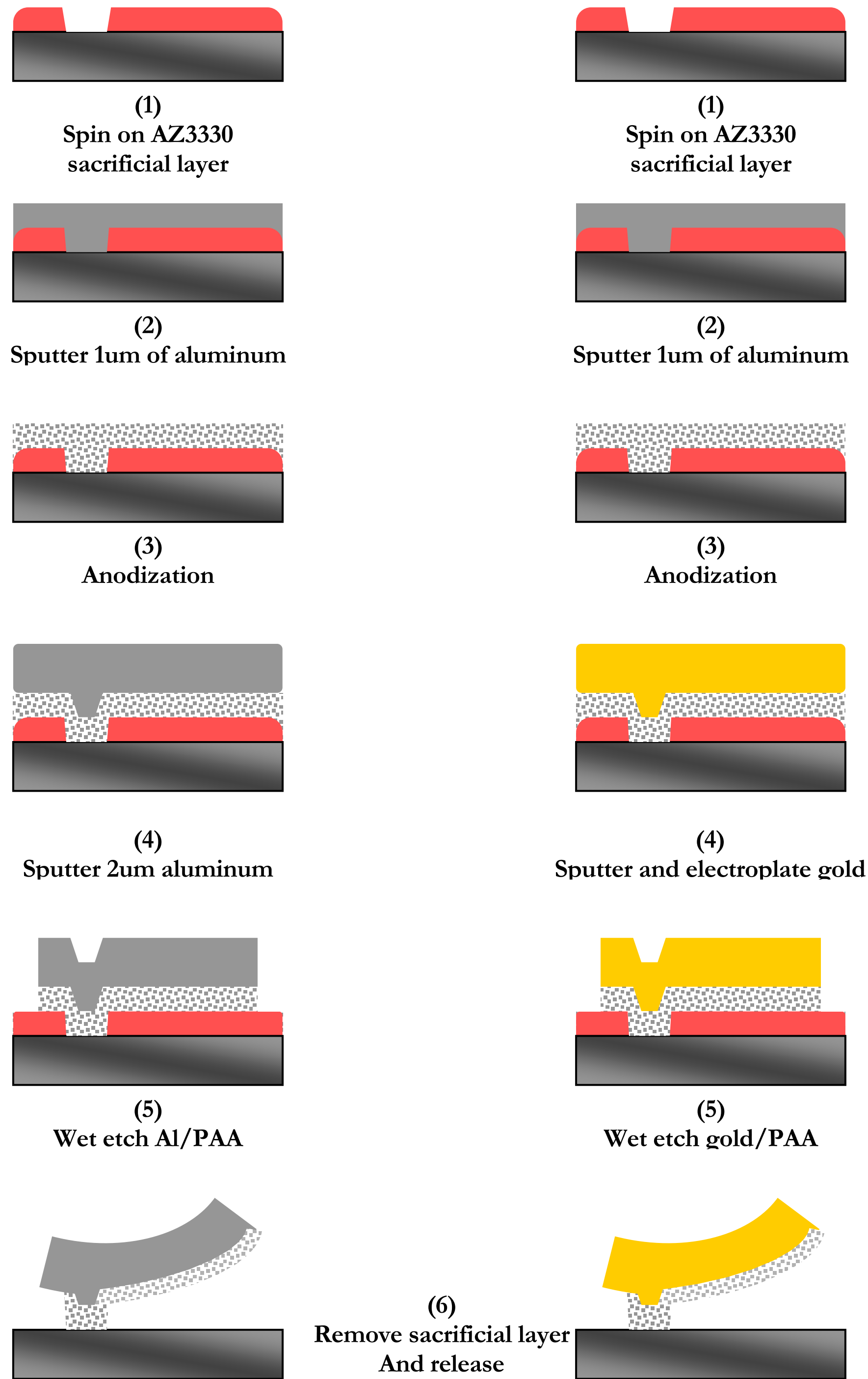


Figure 33: Fabrication steps for (left) aluminum/PAA and (right) gold/PAA bimorph cantilever beams

The tip deflection and curvature were measured using a Veeco optical profiler as shown in Figure 34. As was predicted earlier, the aluminum and PAA structures produced the highest deflection as shown in Table 3.

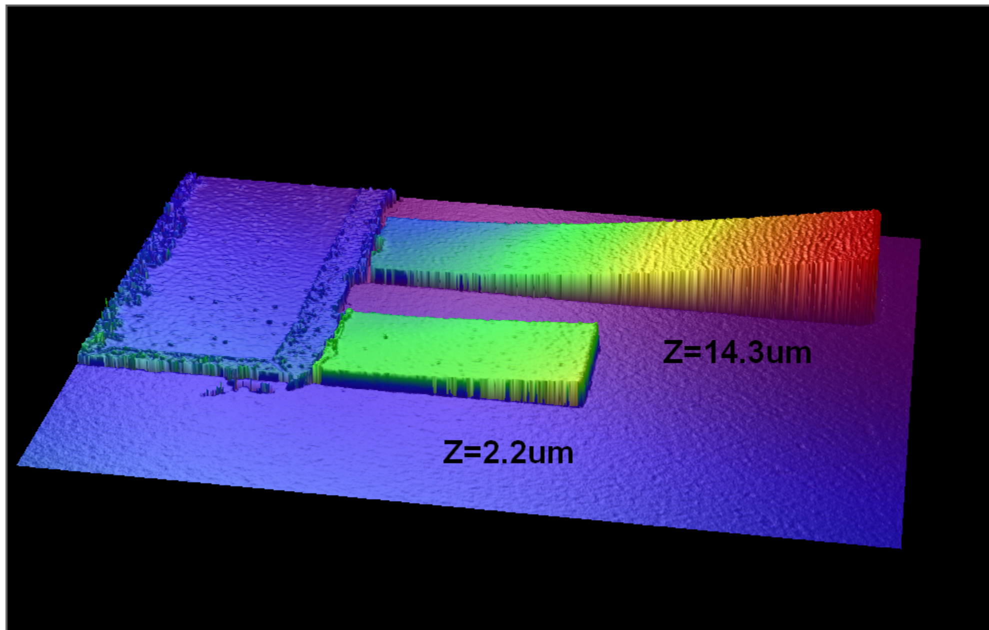


Figure 34: Micrograph of gold/PAA Bimorph Cantilever beams

Structure	Length (μm)	Maximum Tip Deflection (μm)	Radius of Curvature (mm)
gold/PAA	182.8	14.3	1.44
aluminum/PAA	186.1	19.1	1.69

Table 3: Optical Profiler measurements for fabricated bimorph cantilever beams

3.2.3 Dielectric Constant and Stress of PAA Films

Although the chemical makeup of PAA is similar to the more common aluminum oxide, the structure is more of a porous nature than a crystalline arrangement. PAA is constructed of pillars of alumina with air filled pores. Due to this porosity, the dielectric constant of this material can be estimated as a mixture of $\varepsilon_{Alumina}$= 9.9 and ε_{Air}= 1.0. By varying the diameter of the pore cell, the dielectric constant of PAA can vary between these two values.

While there are several methods of measuring the dielectric constant, it is still one of the most difficult properties to accurately deduce. A summary of published dielectric constants is shown in Table 4. It is evident that by simply varying the anodization conditions, the dielectric constant is tunable to any specific application. The two most popular methods of calculating the dielectric constant are summarized below.

Dielectric Constant	Electrolyte	Voltage or Current Density	Thickness	Pore Diameter (nm)	Pore Spacing (nm)	Porosity	Method of Measurement	Source
1.98-2.02	20% sulfuric acid	15, 20, 30 mA/cm^2	0.2 µm			77%	Capacitor-Voltage	[39]
7.2	0.3M oxalic acid	40V		50	100	23%	unknown	[41]
4.4	1 M sulfuric acid + 2 M phosphoric acid	10V	0.5 µm			75%	Ellipsometry	[24]
6.5	10 wt% sulfuric acid	20V	100 nm	16			Capacitor-Voltage	[48]
10.5	boric acid/ ammonium hydroxide	1 mA/cm^2					Capacitor-Voltage And Ellipsometry	[13]

Table 4: Summary of reported PAA

3.2.3.1 Capacitance-Voltage (CV) Characterization

In this method, metal-insulator-semiconductor (MIS) structures are fabricated to determine carrier density, threshold voltage and flatband voltage [39]. Since the capacitance C_0 is determined by the properties of the dielectric or insulating layer, this device can be used to measure the dielectric constant of PAA by:

$$\varepsilon = \frac{C_o t_{ox}}{\varepsilon_o A} \tag{3.10}$$

Where C_o is the oxide capacitance (F), t_{ox} is the oxide thickness (m), and A is the area of the top contact (m^2).

However, as Das et al. had shown, measured capacitance is combination of the capacitance of the air filled pores plus the capacitance of aluminum oxide, or

$$C_o = C_{air} + C_{alox} \tag{3.11}$$

They found that as the pore size increase (larger volume of air filled holes versus aluminum oxide) would see a decrease in the overall dielectric constant. However, by widening the pore diameter, this allowed the top metal contact to partially fill the pores as seen in Figure 35.

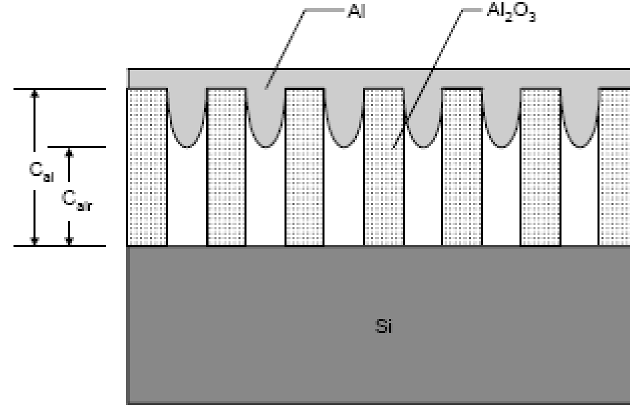


Figure 35: Schematic cross section of Al/Alumina/p-Si capacitors [39]

This method was initially used to calculate the dielectric constant of the PAA in this work; however the results were found to be inconclusive.

3.2.3.2 Ellipsometry

A non destructive method that can be used to measure the dielectric constant is to use optical means. Ellipsometry is used to study thin films on solid substrates. By measuring the reflected elliptically polarized light, the film thickness and index of refraction can be solved.

To date, the Maxwell-Garnett model is used to represent a good approximation of the complex structure of PAA [40]. If we assume that ε_{Alox}=9.9, then the effective dielectric constant is given by:

$$\varepsilon_{eff} = \frac{\varepsilon_{air} + 2\varepsilon_{Alox} + 2f(\varepsilon_{air} - \varepsilon_{Alox})}{\varepsilon_{air} + 2\varepsilon_{Alox} - f(\varepsilon_{air} - \varepsilon_{Alox})} \tag{3.12}$$

Where *f* is the filling fraction of air, in this case equal to the porosity *p*. The porosity *p* of the hexagonal cell structure is given by:

$$p = \frac{\pi}{2\sqrt{3}}\left(\frac{D}{D_{\text{int}}}\right)^2 \tag{3.13}$$

Table 5 shows the results of the above calculations and the measured results from the ellipsometer.

Interpore Distance D_{int} (nm)	Pore Diameter D(nm)	Porosity	ε_{eff} (Model)	ε_{eff} (Ellipsometry)
100	50	0.2267	7.27	3.72

Table 5: Results from Model and Ellipsometry Calculations

As shown, there is still a wide discrepancy from these measurements. However, since the PAA in this thesis has a low porosity, it is safe to assume that the effective dielectric constant that was calculated from the model is the most accurate. The dielectric constant measured from the model shows good agreement with the one reported by Delendrik [41] that used the same anodization conditions as in this work.

As with the dielectric constant, the value of the stress depends on the porosity of the PAA film. In [42], the mechanical properties and residual stress in PAA films are investigated using nano indentation tests. The relationship between the pore size and the porosity is shown in Table 6 and shows good agreement with the model previously presented. It was found that the Young's modulus and the hardness of the structure decreased as the size of the pores increased. This is expected since the composition of the material shifts from a solid to a more porous state. As seen in Figure 36, the residual stress decreases as the porosity increases. Based on the fabrication of the PAA film presented in this thesis, the

Young's modulus is 137-141 GPa [41, 42] and the residual stress is approximately 600 MPa.

Hole diameter of specimens (nm)	Porosity (nm)
30	8
40	15
50	23
60	33
70	44
80	58

Table 6: Hole diameter and porosity

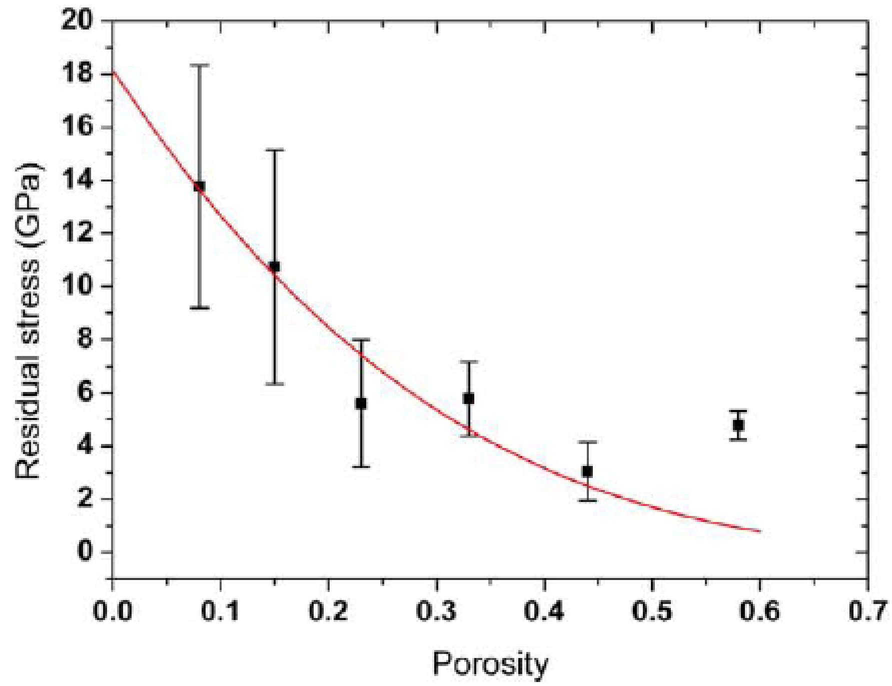


Figure 36: Residual stress as a function of porosity [42]

3.3 Film Fabrication and setup

The experimental setup and cell is shown in Figure 37. The anodization setup consisted of a 1L Pyrex beaker filled with 0.3M oxalic acid. A magnetic stir bar is placed inside to allow agitation. A power supply is provided that will allow a constant current source between the test device (anode) and the cathode. The test device is held by alligator clips and slowly submerged into the solution. A thin piece of Kapton tape is placed at the interface in order to reduce any early anodization that can eventually lead to breaking electrical contact with the rest of the film [43]. The backside of the silicon wafer is also protected to avoid any anodization of the substrate surface.

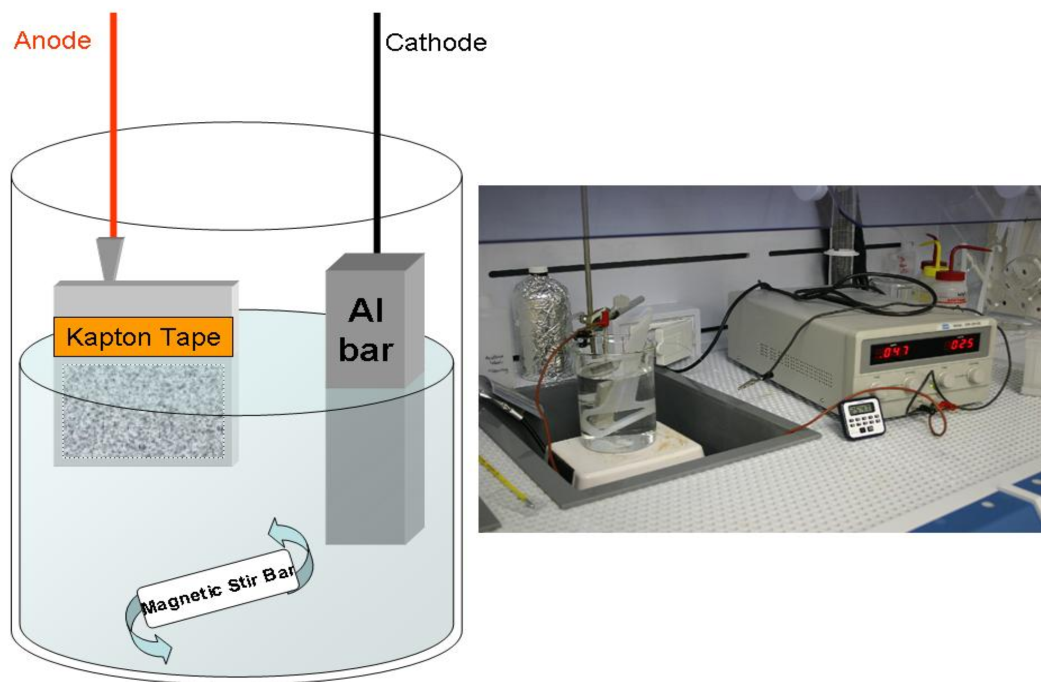


Figure 37: Anodization cell and laboratory wet bench setup

After an applied voltage was set, the current rose briefly until it reached a steady state. It was during this time that the aluminum was being consumed and PAA was formed in its

place. Eventually, as the aluminum was further consumed, the current began to drop until it reached zero. At this point, the aluminum metal was completely consumed and only a dielectric layer of PAA was left. It should also be pointed out that during this drop in current, the metal colour of the aluminum began to fade and become transparent. Once the film was completely transparent and the current has reached zero, the power was shut off and anodization was complete. An example of this transparent transformation can be seen in Figure 38. Due to the transparency of the PAA, the photoresist sacrificial layer and underlying first metal contacts can be seen. The dark corners on the edge of the wafers are where the Kapton film was placed. Once removed, it also removed any underlying aluminum.

If the thickness and area of the film are known, then an accurate anodization rate can be calculated. In this manner, films of any required thickness can be fabricated. For example, if it takes 5 minutes to fully anodize a 1 $inch^2$ area of 2 μm aluminum, then anodizing for 2 and half minutes will create a 1μm film of PAA.

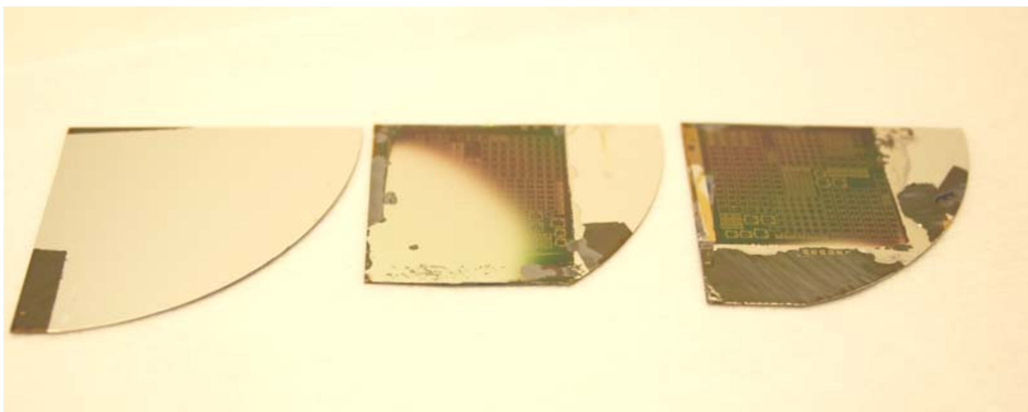


Figure 38: Anodization of aluminum film. Before anodization (left), half time anodization (middle) fully anodized (right)

One disadvantage of this method is that if any conductive metal is exposed, it will become anodized. For example, the exposed backside of silicon substrates must be protected using photoresist or Kapton tape. Metals such as chromium and titanium can also form porous

oxides and have been explored by various researchers [12]. However, in this case, they also showed poor adhesion to the substrate as shown in Figure 39 below. A chromium/gold coplanar waveguide (CPW) transmission was blanket coated with aluminum. The aluminum film was then anodized and it was observed that the chromium adhesion layer was first anodized and then began to dissolve.

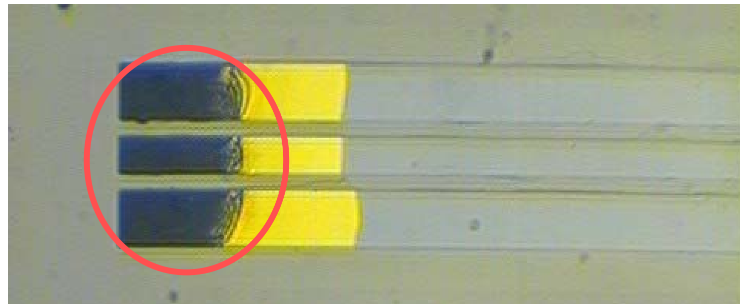


Figure 39: Micrograph backside image of chromium/gold CPW line with PAA film above. The chromium became an oxide and eventually dissolved.

When noble metals such as gold or platinum are exposed to the electrolyte, it is observed that the overall current density changes. This causes any formed PAA films to peel off the substrate as shown in Figure 40.

If the gold is protected with a thick photoresist layer for example, then the PAA film can be anodized without any peeling. This method is explored in the last section of this thesis.

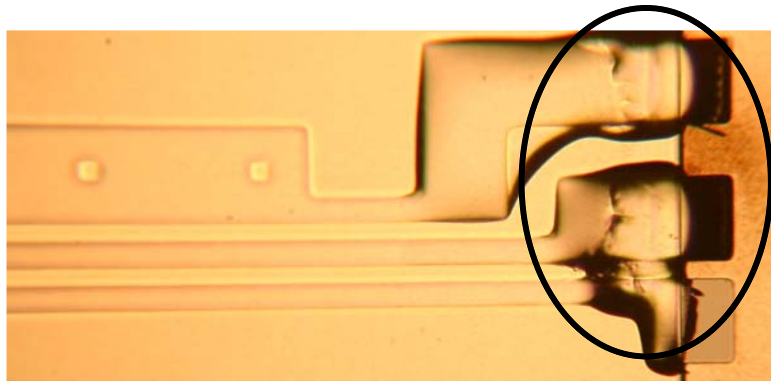


Figure 40: Micrograph image showing the PAA film peeling off the gold structure

Chapter 4

In this chapter, Porous Anodic Alumina is integrated with standard CMOS materials. An RF MEMS Tunable Inductor was fabricated and tested based on the bimorph effect of PAA and aluminum. To further improve the Q, PAA was integrated with gold on an alumina substrate. Since PAA can easily be used in silicon and alumina substrates at low temperatures, this clearly shows the versatility and functionality of this novel material.

Number of Turns

As the number of turns in a spiral inductor increase, the value of the inductance will also increase. This is because the area of the inner turns is smaller than those on the outer (if the area of spiral is constant). However, the resonant frequency will decrease due to the increase in capacitive coupling of the extra metal turns to the substrate. The Q will also decrease because of the added metal losses.

Separation between Windings

By increasing the separation between the windings, the inductance decreases due to the decreasing inner spiral diameter (if the area of the spiral is constant). Since there is less metal, the capacitive coupling between adjacent turns decreases, which will increase the resonant frequency. The Q will also increase.

Width of Windings

By increasing the width of the metal, the inductance decreases due to the decreasing inner spiral diameter (if the area of the spiral is constant). Due to the increased area of the metal of the windings, the capacitive coupling between the metal and the substrate increases. This causes the resonant frequency to decrease.

Thickness and choice of Metal

The thickness of the metal trace should be at least two times greater than the skin depth at the operating frequency. A thicker metal will increase the Q performance. In addition, metals with a higher conductivity (such as gold or copper) will reduce the resistive losses of the current, therefore increasing the Q.

Thickness of Isolation Layer

While adding an isolation layer between the metal inductor and the lossy silicon substrate will increase the Q and resonant frequency, the inductance will remain unchanged. In this work, the increased distance between the inductor and the substrate will be realized by the warped bimorph structures.

4.1 PLANAR INDUCTORS

To further study the electrical properties of PAA, a series of planar inductors and coplanar wave lines were fabricated. The insertion loss of the lines will indicate if PAA can be used as an isolation layer

4.1.1 Simulation

Simulations were performed to determine the correct composition of PAA to reduce the thermal noise due to parasitic loss of the silicon substrate. A 1000 μm aluminum coplanar waveguide (CPW) line as shown in Figure 41 was simulated using Sonnet software [44]. A 3.0 μm layer of PAA was used as an isolation layer between the metal lines and the silicon substrate.

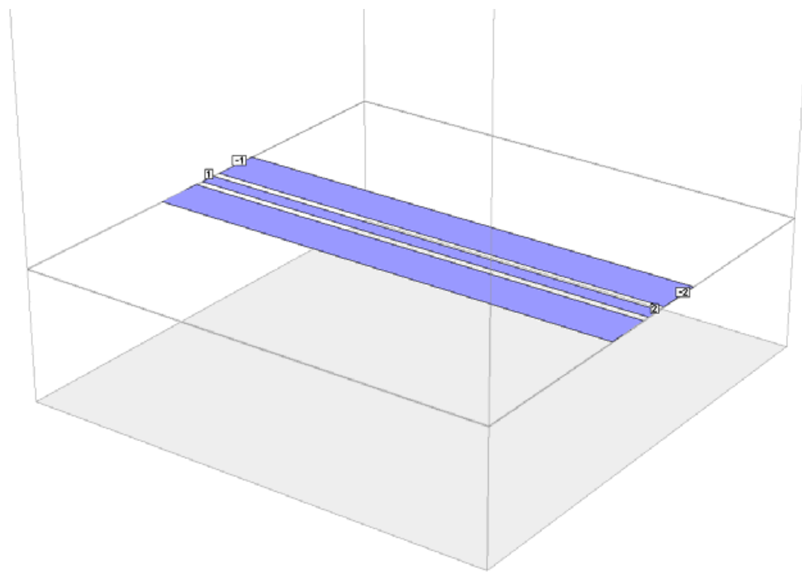


Figure 41: Sonnet Simulation layout for CPW lines

The dielectric constant of the PAA was varied from 3.0 to 9.0. As shown in Figure 42, the change in dielectric constant does not have a tremendous effect on the insertion loss.

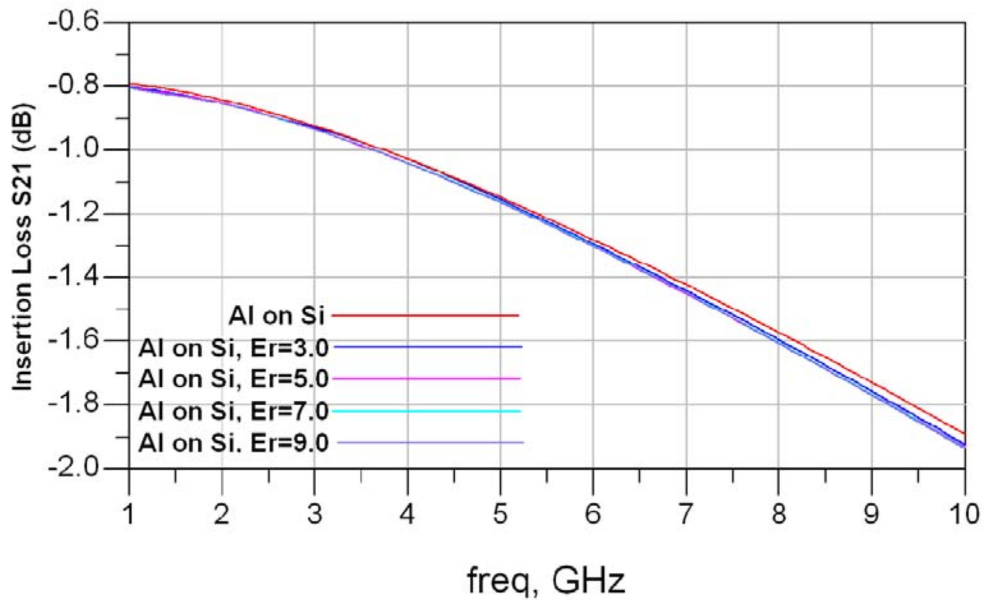


Figure 42: Simulated insertion loss of CPW transmission lines with the ε varying from 3.0 to 9.0

Since the dielectric constant of the PAA films in this thesis is around 7.0, another simulation was performed by varying the thickness. It is obvious that a thicker film will not reduce the parasitic loss as shown in Figure 43. One of the reasons for this behaviour is the loss tangent of the PAA film. The value of the loss tangent used in this simulation was 0.003 obtained from one of the only papers to have it reported [41].This value is 10 times higher than traditional Alumina and poorer than Silicon (0.005 at 1 GHz).

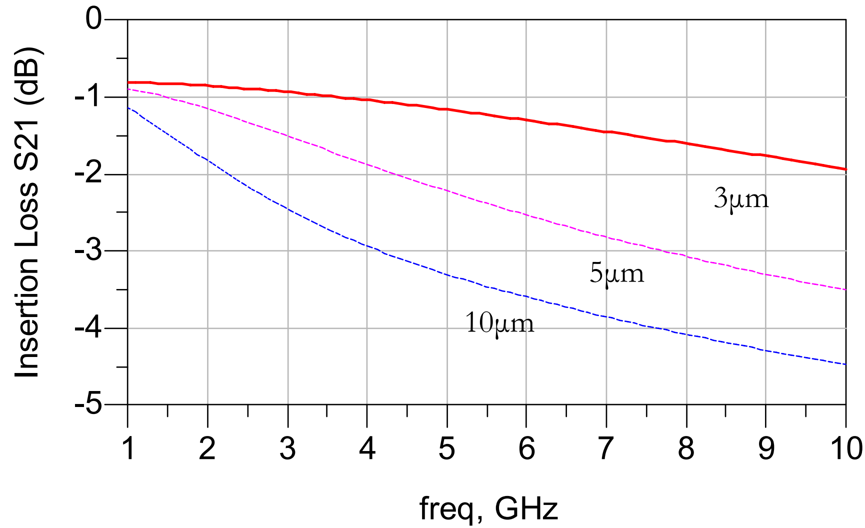


Figure 43: Simulated insertion loss of CPW transmission lines with varying the PAA thickness

4.1.2. Device Fabrication

To verify the simulations, coplanar waveguide (CPW) lines were fabricated with and without a PAA isolation layer. In this study, low resistivity p-type <100> 8-12 Ω·cm c-Si substrates were cleaned using a standard RCA-1 procedure. To form the isolation layer, 2 µm of aluminum was sputtered and then fully anodized to create a 3 µm film of PAA. Another 1 µm layer of aluminum was sputtered. Once the metal contact layer was deposited, the wafers were patterned and etched using standard photolithographic methods.

4.1.3 Results and Discussion

The S-parameters of the fabricated CPW lines were measured using Agilent 8510 network analyzer and Cascade Microtech GSG probes. The insertion loss (S_{21}) of aluminum on silicon and the aluminum on PAA/silicon is shown in Figure 44. At the lower frequencies, the loss is lower for the aluminum on PAA/Silicon CPW lines, however after 2 GHz, the losses dominate.

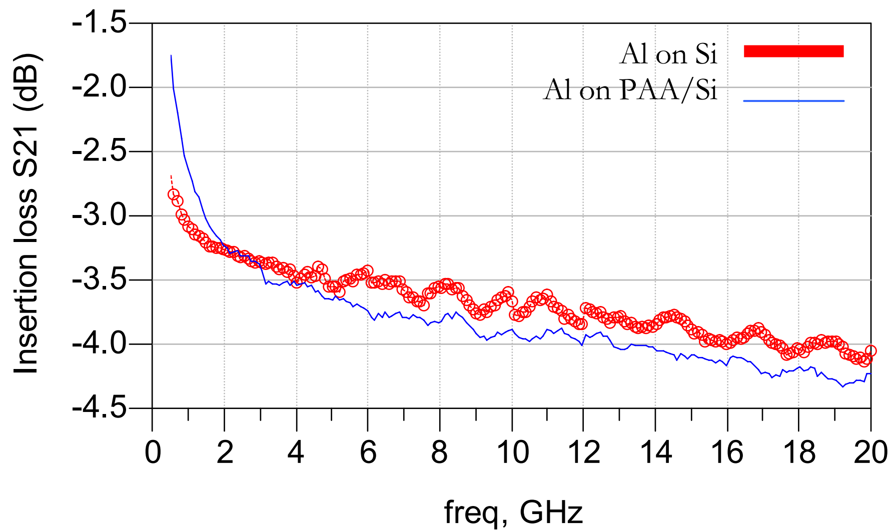


Figure 44: The measured insertion loss of the fabricated CPW lines with and without PAA isolation layer

For the planar inductor shown in Figure 45 it is clear that PAA would not be a suitable candidate as an isolation layer, as the Q had deteriorated by nearly 8%. Further work must be made in order to use PAA as an isolation layer. As the interest in nanomaterials grows [10], the argument for further material characterization can be made. It is believed that with a lower loss tangent, this material could definitely be integrated as a passivation layer.

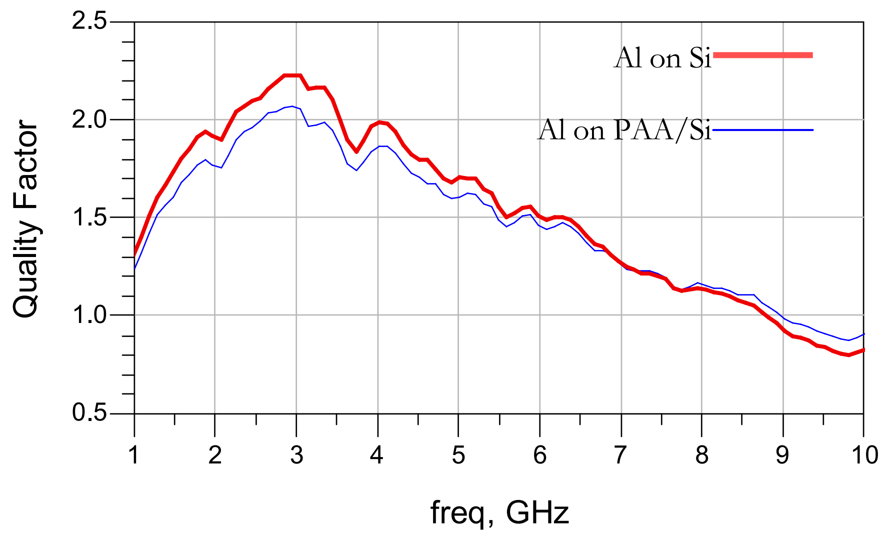


Figure 45: Quality factor of planar inductors with and without PAA as an isolation layer between Silicon

4.2 TUNABLE RF MEMS INDUCTORS USING AN ALUMINUM, PAA AND ALUMINUM SANDWICH ON SILICON WAFERS

4.2.1 Design

A tunable inductor based on the thermal actuation of an aluminum, Porous Anodic Alumina and aluminum sandwich structural layer is presented. When a voltage is applied to the device, the structure will warp due to the difference in the CTE of the two materials. Due to its low temperature processing and low fabricating costs, this process is ideal for CMOS RFIC applications.

4.2.2 Device Fabrication

Due to the large mismatch in CTE and stress of the aluminum and PAA, the vertical deflection should be large as well. Any fine tuning can be adjusted by changing the anodization conditions and therefore the porosity as shown earlier in Figure 36.

The fabrication process is shown in Figure 48. A p-type <100> 8-12 Ω·cm silicon wafer was cleaned using a standard RCA-1 recipe. Afterwards, the first aluminum metal layer was deposited by DC sputtering for a thickness of 1 μm. This layer was then patterned and etched to form the contact pad structure. The wafer was then coated with a 2 μm photoresist sacrificial layer and patterned to form the anchors. After hard baking to prevent any further outgassing, 2 μm of aluminum was sputtered. The aluminum film was then anodized in a 0.3M oxalic acid solution for 3 minutes, forming a 1 μm PAA layer. A third mask is used to pattern the PAA layer and the patterning resist is ashed away using the Reaction Ion Etching (RIE). To complete the aluminum/PAA sandwich structures, another 2 μm of aluminum was sputtered. The top layer aluminum layer was patterned

and etched. The photoresist sacrificial layer was removed and the structure was released using the RIE.

By applying a DC voltage across the inductor, the warped structure will begin to collapse. Increasing the voltage, therefore increasing the temperature running through the structure, will cause the warped inductor to eventually flatten. This thermomechanical process was simulated using CoventorWare [45] and is shown in Figure 46. The fabricated released structure shown in Figure 47, shows good agreement with the thermomechanical simulation.

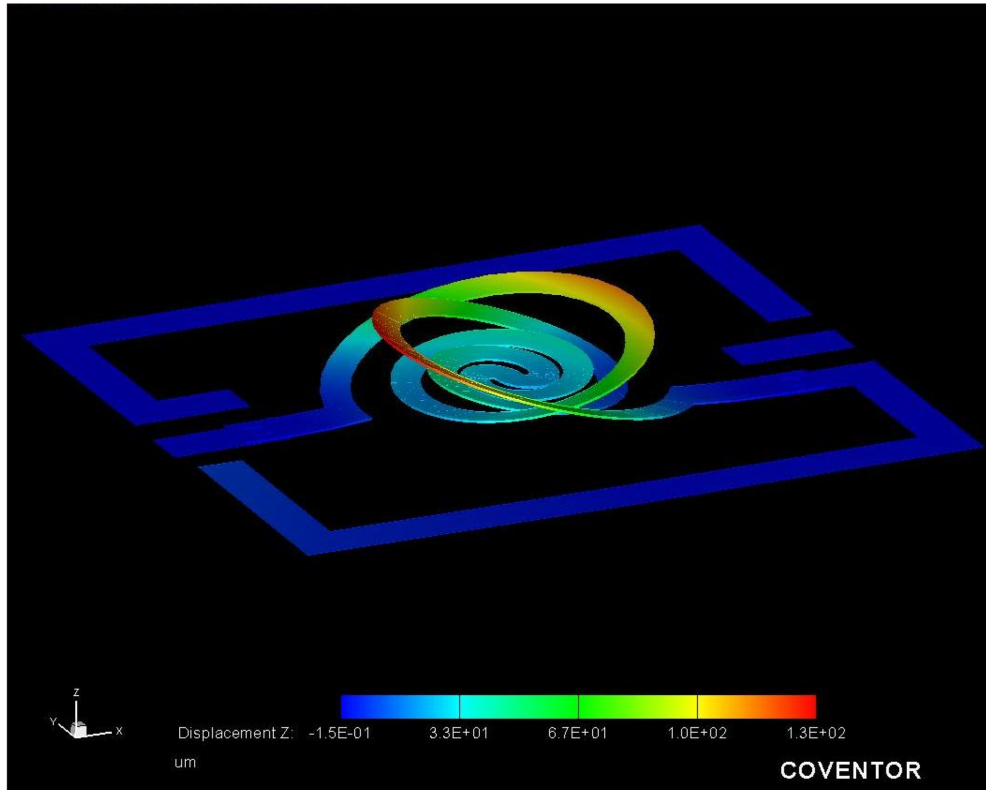


Figure 46: Thermomechanical simulation performed using Coventor of the fabricated tunable RF MEMS inductor based on an aluminum/PAA/aluminum sandwich layer

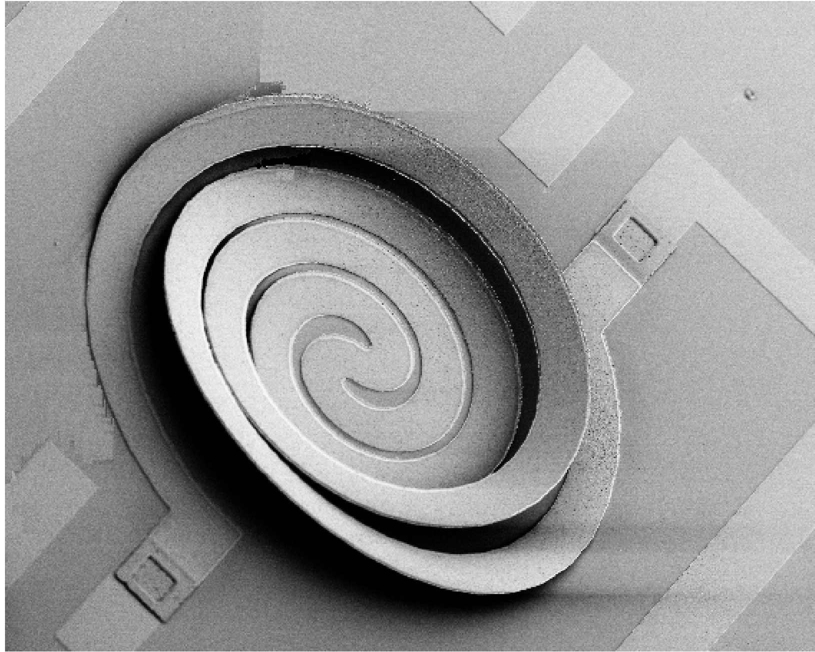


Figure 47: SEM Micrograph at 120X of an RF MEMS Tunable Inductor based on the aluminum/PAA/aluminum sandwich structure

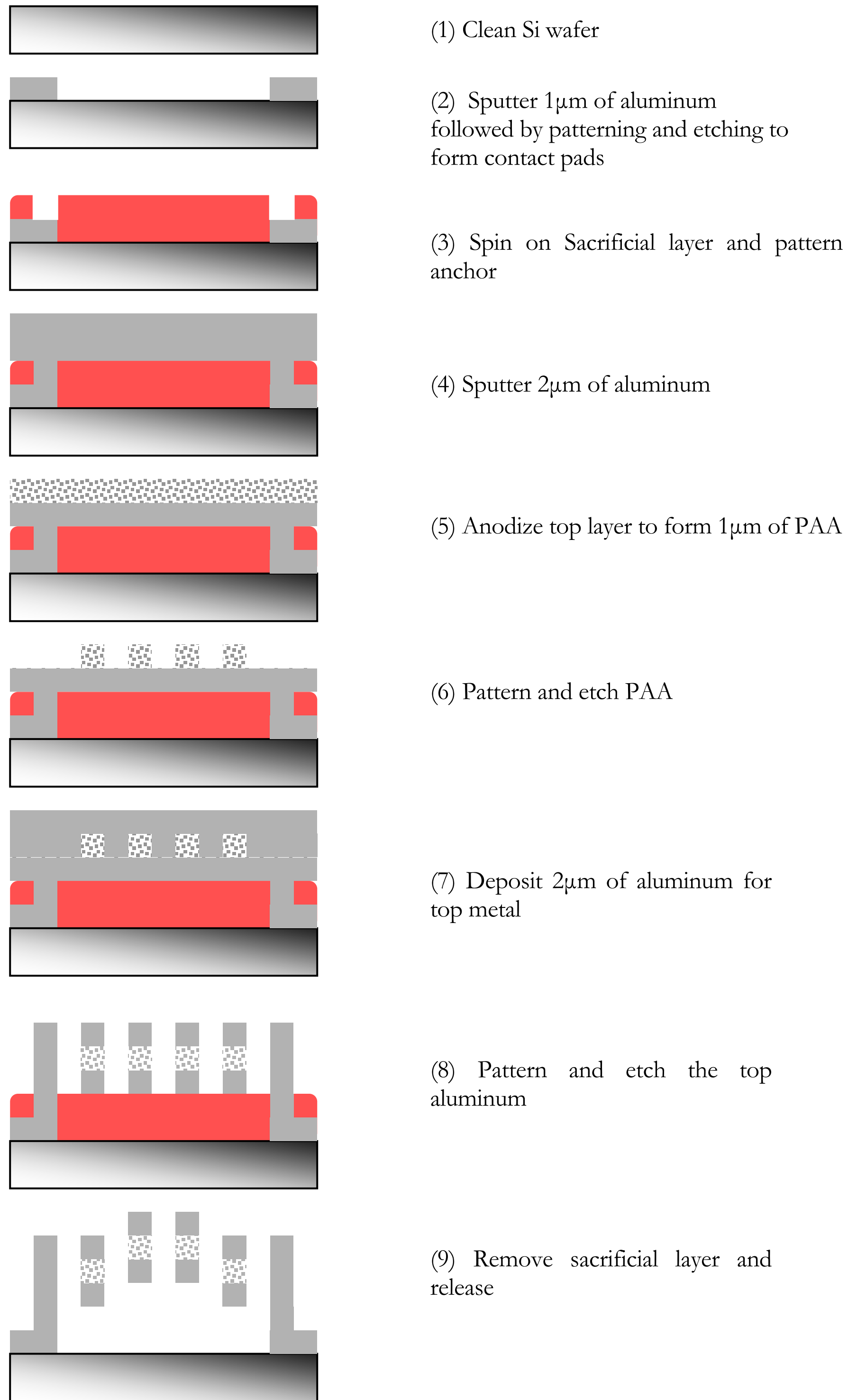


Figure 48: Fabrication of tunable RF MEMS inductor based on aluminum/PAA/aluminum sandwich

4.2.3 Results and Discussion

4.2.3.1 Parameter Extraction

The S-parameters of the fabricated inductors were measured from 50 MHz to 20 GHz. A series of 1 and 2 port structures were tested. For a two port structure, S_{11} and S_{22} represent the reflected signal from port 1 and port 2. The transmitted signal in the forward and reverse direction between port 1 and port 2 are represented by S_{12} and S_{21} and should theoretically be equal for a symmetric passive device.

De embedding measures the true performance of the device. After measuring the device and an open test structure the S parameters are transformed to Y parameters, by using:

$$[Y] = ([U]-[S])([U]+[S])^{-1} \tag{4.1}$$

After the S parameters are converted, the true device under test (DUT) is found by using:

$$Y_{de-embed} = Y_{DUT} = Y[S_{total}] - Y[S_{open}] \tag{4.2}$$

After de embedding, the impedance and the series inductance and resistance can be extracted from Y_{11}.

$$L_s = \frac{\text{Im}\left\{\frac{1}{Y_{11}}\right\}}{2\pi f} \tag{4.3}$$

$$\text{and } R_s = \text{Re}\left\{\frac{1}{Y_{11}}\right\} \tag{4.4}$$

The Q can be extracted from Y_{11} as:

$$Q = \frac{\text{Im}\left\{\frac{1}{Y_{11}}\right\}}{\text{Re}\left\{\frac{1}{Y_{11}}\right\}} \tag{4.5}$$

Another method of finding the desired parameters is to transform the 2 port to a 1 port by short circuiting the output terminal. In Figure 49, a two port network is terminated by a load Z_L. In this case, if we made Z_L a short circuit, then Γ=-1.

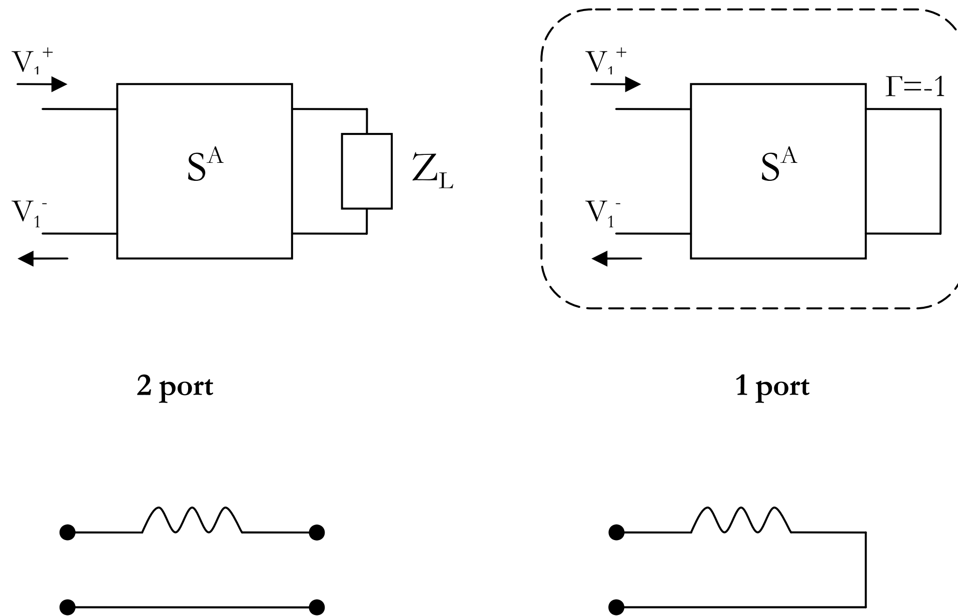


Figure 49: Transforming 2 port to 1 port

The S_{11} of the 2 port structure is:

$$V_1^- = S_{11}V_1^+ + \frac{S_{12}^A \Gamma S_{21}^A}{1 - \Gamma S_{22}^A} V_1^+ \tag{4.6}$$

And since we know Γ=-1, then S_{11} overall becomes:

$$\frac{V_1^-}{V_1^+} = S_{11_1port} = S_{11} - \frac{S_{12}S_{21}}{1 + S_{22}} \tag{4.7}$$

The associative Z parameter for the above equation is:

$$Z_{11_1port} = Z_o \cdot \frac{1 + S_{11_1port}}{1 - S_{11_1port}} \tag{4.8}$$

The quality factor and the inductance of the spiral inductor are:

$$Q = \frac{\mathrm{Im}(Z_{11_1port})}{\mathrm{Re}(Z_{11_1port})} \tag{4.9}$$

$$L = \frac{\mathrm{Im}(Z_{11_1_port})}{(2\pi f)} \tag{4.10}$$

Using this method will give the same result as obtained using Y parameters.

4.2.3.2 Measurement Results

The devices were measured using an Agilent 8510 network analyzer and Cascade Microtech GSG probes. Before any measurements were made, the system was calibrated using the short-open-load-through (SOLT) calibration.

When a DC voltage was applied across the inductor, the warped structure began to flatten as shown in Figure 50.

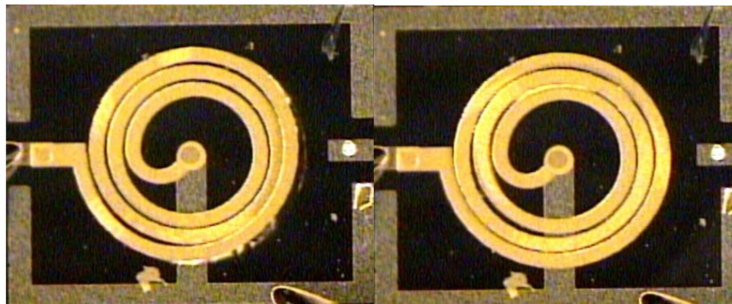


Figure 50: Top view micrograph of a 1 port RF MEMS tunable inductor (left) no actuation (right) with 1.18V applied across the device

The Q and the inductance were calculated using equations (4.9) and (4.10) and are presented below. The non de-embedded results for the 1 port design are shown in Figure 51. The inductance varied from 5.8 nH to 7.6 nH (31%) at 3 GHz by increasing the applied voltage up to 2 V. However, Figure 52 shows that the Q is low but expected since the parasitic effects of the silicon substrate are still in effect.

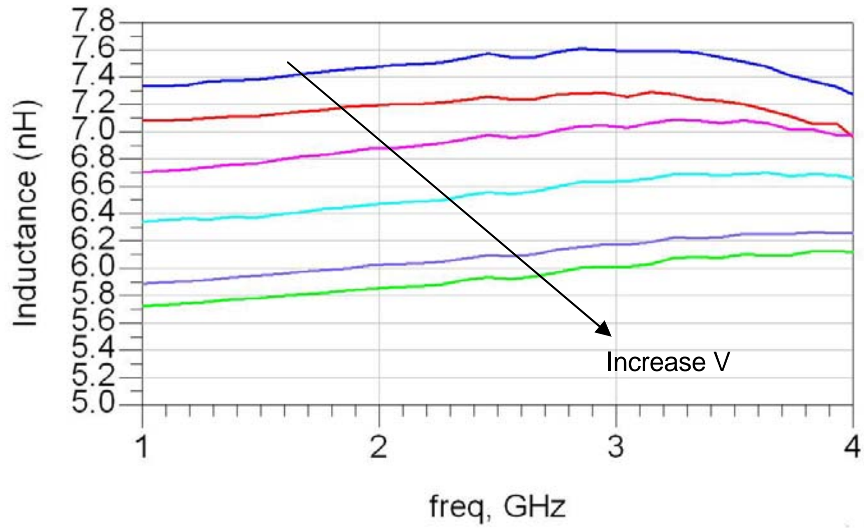


Figure 51: Measured inductance of a fabricated 1 port RF MEMS tunable inductor based on the aluminum/PAA/aluminum sandwich structure, with 0 to 2V applied across the device.

Figure 52: Measured Q of a fabricated RF MEMS tunable inductor based on an aluminum/PAA/aluminum sandwich structure at 0 V.

Another design based on a 2 port coil with no under pass through was also tested and is shown in Figure 53.

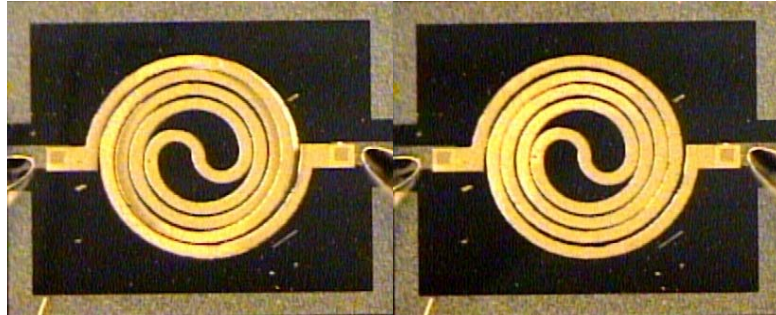


Figure 53: Top view micrograph of a 2 port RF MEMS tunable inductor (left) no actuation (right) with 1.38V applied across the device

The tuning range varied from 2.6 nH to 3.2 nH (23%) at 3 GHz by increasing the applied voltage up to 2 V as shown in Figure 54. Due to the increase of the separation between the windings, the inductance is lower than the previous design. The peak Q reaches 4.5 and then drops as the applied voltage increases. The lower Q of this design could be attributed to the increase in turns (3 to 4) which increase the metal losses as shown in Figure 55.

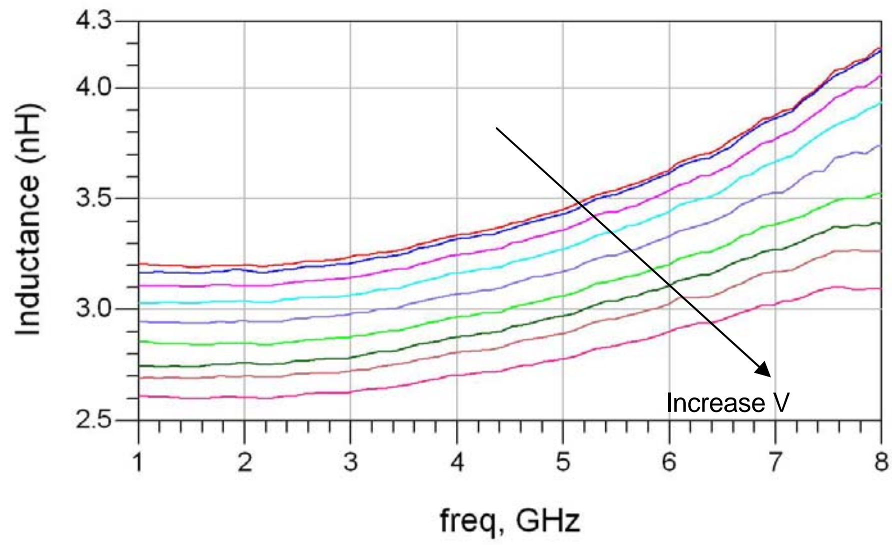


Figure 54: Measured inductance of a fabricated 2 port RF MEMS tunable inductor based on the aluminum/PAA/aluminum sandwich structure, with 0 to 2V applied across the device.

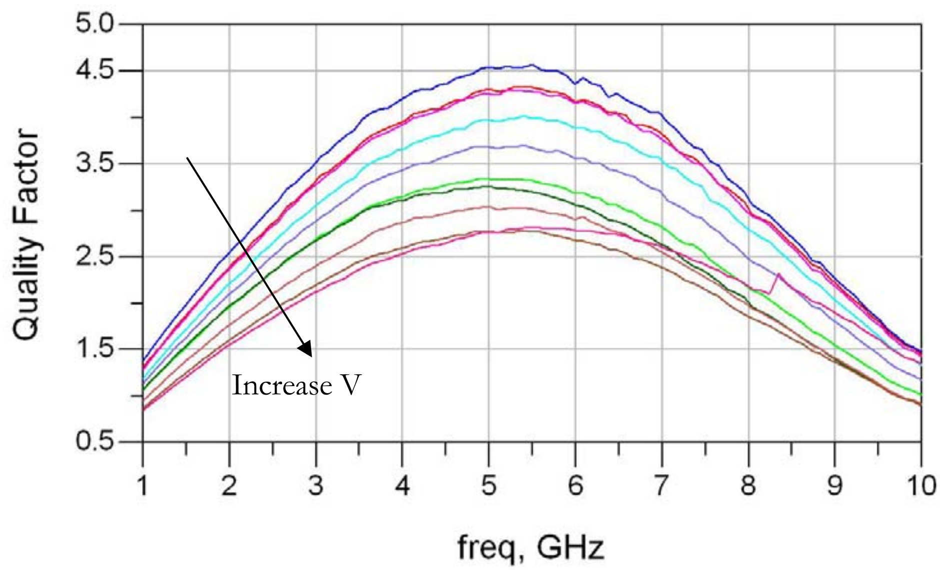


Figure 55: Measured Q of a fabricated 2 port RF MEMS tunable inductor based on an aluminum/PAA/aluminum sandwich structure.

One reason why the performance could be low is due to the deflection height of the coil. The peak deflection for the aluminum/PAA/aluminum structure is 133 µm. Due to the poor deflection, a simpler bilayer of aluminum and PAA is proposed. It is believed that this structure would have a greater tunability and Q than the sandwich structure.

Using CoventorWare [45], the thermomechanical deflection of the bilayer was simulated and shown is in Figure 56. As predicted, a deflection height of over 256 µm is achieved, almost double the sandwich structure.

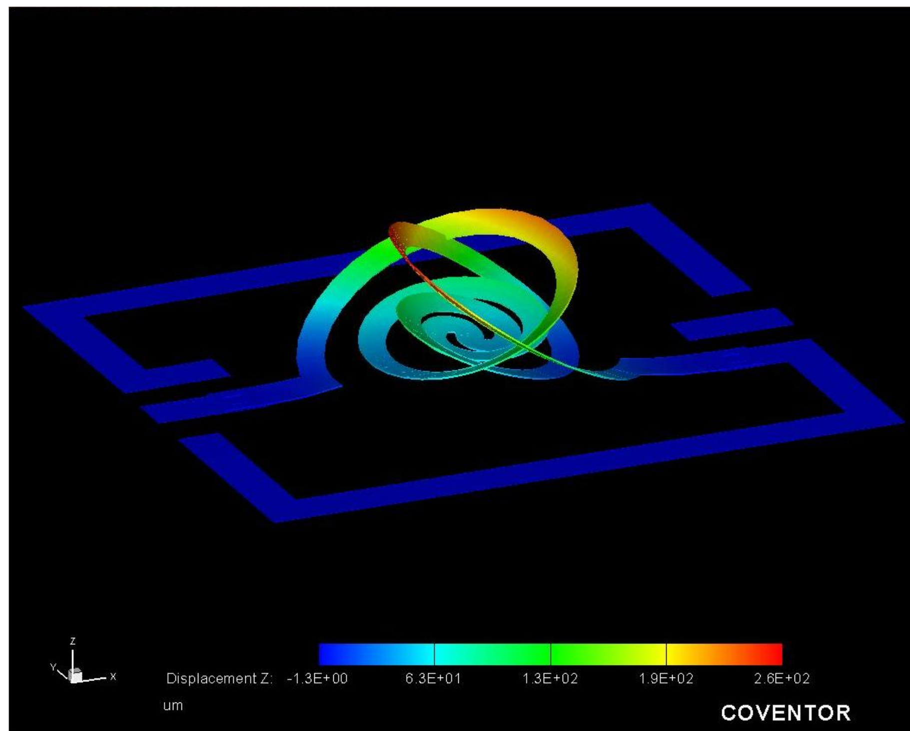


Figure 56: Thermomechanical simulation performed using Coventor of the fabricated tunable RF MEMS inductor based on an aluminum/PAA layer

Since the top metal layer and the bottom contact pads would be electrically connected if the anodization were continued, there is a chance that the anchors would be anodized. This would cause a discontinuity in the electrical path from the contact pads to the device as shown in Figure 57. It some cases, it was observed that the anodization continued

underneath the anchor and beyond the photoresist sacrificial layer. In order to ensure that the first layer is a complete dielectric, the fabrication process must be altered.

In the new process, the photoresist sacrificial layer will be deposited first, followed by the PAA layer. The anchors are then etched after the anodization, therefore ensuring that the first contact metal layer remains conductive. By changing this process, other noble metals such as gold can now be used.

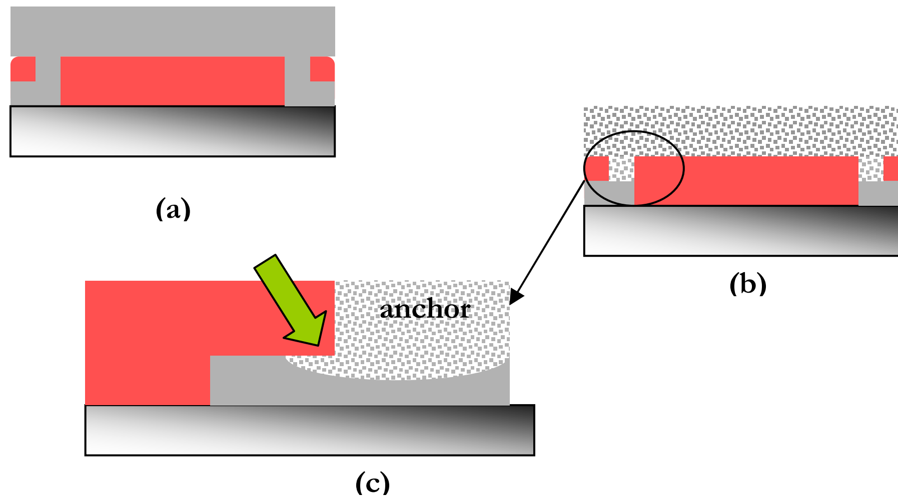


Figure 57: Schematic diagram showing (a) Top aluminum film connected to the first metal layer through the anchors (b) Film is completely anodized (c) enlarged area of the anchor and contact pad interface

The proposed fabrication process is shown in Figure 58. A p-type <100> 8-12 Ω·cm silicon wafer was cleaned using a standard RCA-1 recipe. Afterwards, the first 1 μm aluminum metal layer was deposited by DC sputtering. This layer was then patterned and etched to form the contact pad structure. The wafer was then coated with a 2 μm photoresist sacrificial layer. After hard baking to prevent any further outgassing, 1μm of aluminum was sputtered. The aluminum film was then anodized in a 0.3M oxalic acid solution for 5 minutes or until the film became transparent. Anchor holes were patterned and etched using the RIE, which also removed the patterning photoresist. To complete

the aluminum/PAA bimorph structures, another 2 μm of aluminum were sputtered. The top layer PAA and aluminum layer was patterned and etched, followed by the removal of the photoresist sacrificial layer by Reactive Ion Etching (RIE).

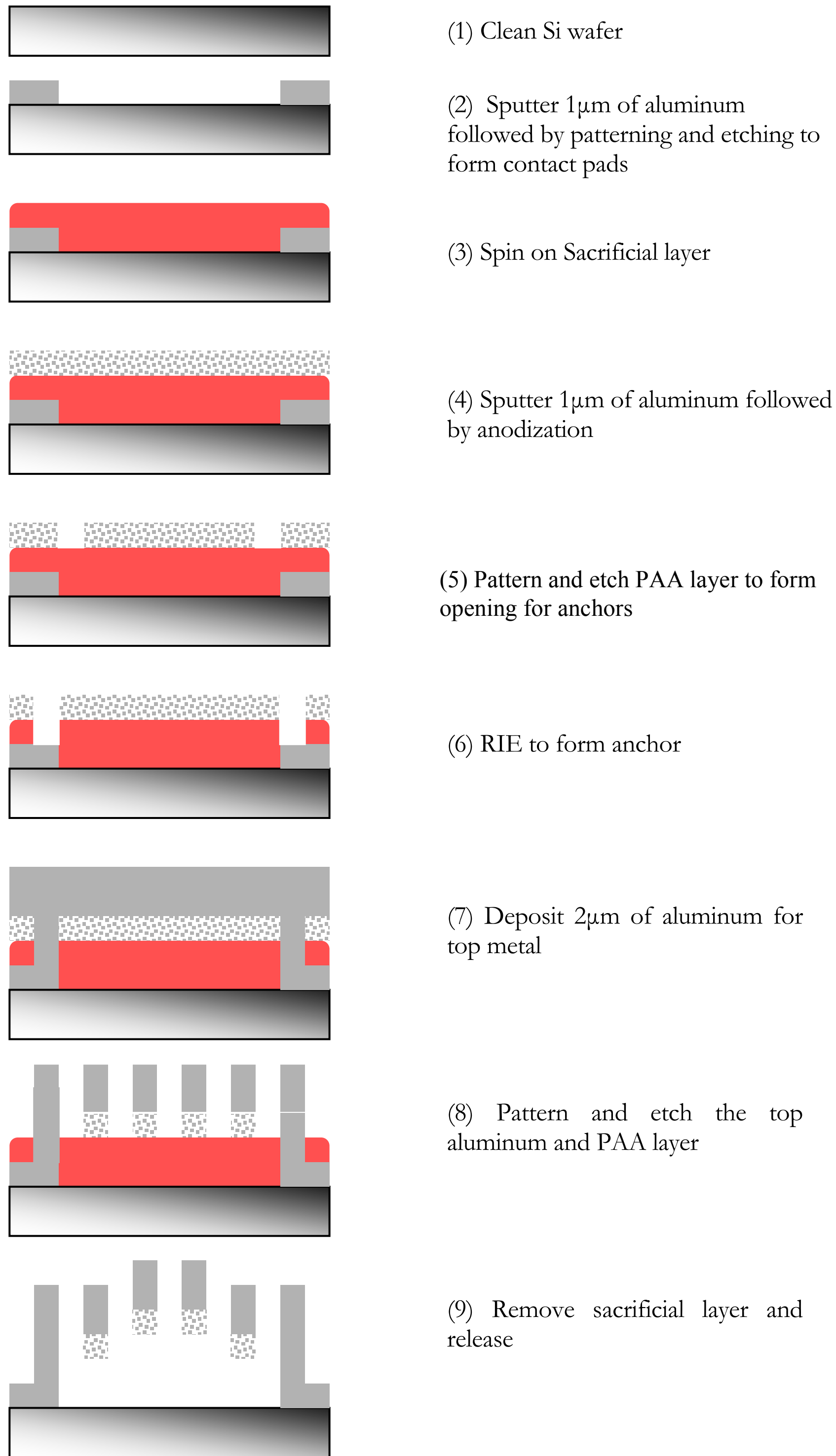


Figure 58: Fabrication of tunable RF MEMS inductor based on PAA/aluminum

Ansoft's High Frequency Structure Simulator (HFSS) [46], a commercial 3D EM solver is used to study the RF performance of the inductors. The software is based on the finite-element method and models the effects of substrate resistivity, conducting material and air gap thickness. The effect of the air gap on the Q factor was studied by varying the height, while keeping all the other variables constant. After the layout was imported, a 3D model of the spiral inductor is constructed as shown in Figure 59. Simulation boundaries and the port were defined. A frequency sweep from 0 to 10 GHz with a 0.1 GHz step size was entered. After the S parameters were converted into impedance parameters, the Q and the inductance were calculated. The Q factor as a function of frequency for a range of air gap values is shown in Figure 60.

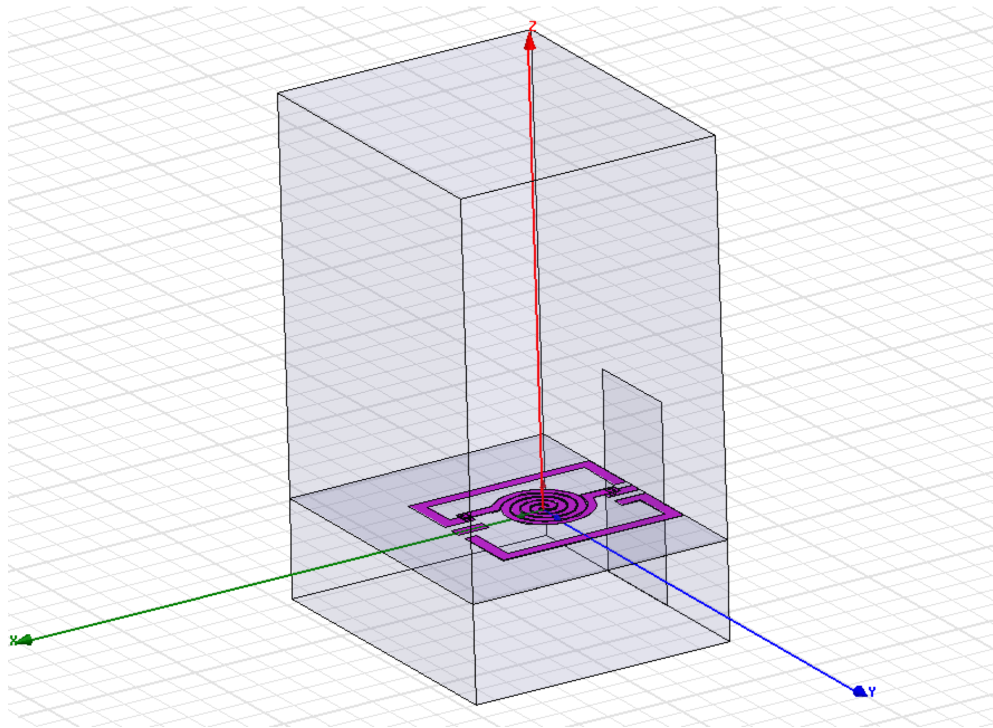


Figure 59: HFSS Model of 1 port RF MEMS tunable inductor used in this thesis

At lower frequencies, the Q is largely determined by the series resistance of the inductor, and therefore, the increase in air gap has little effect. At higher frequencies, the RF signal

begins to couple into the substrate. The thicker air gap increases the isolation of the inductor and the lossy substrate.

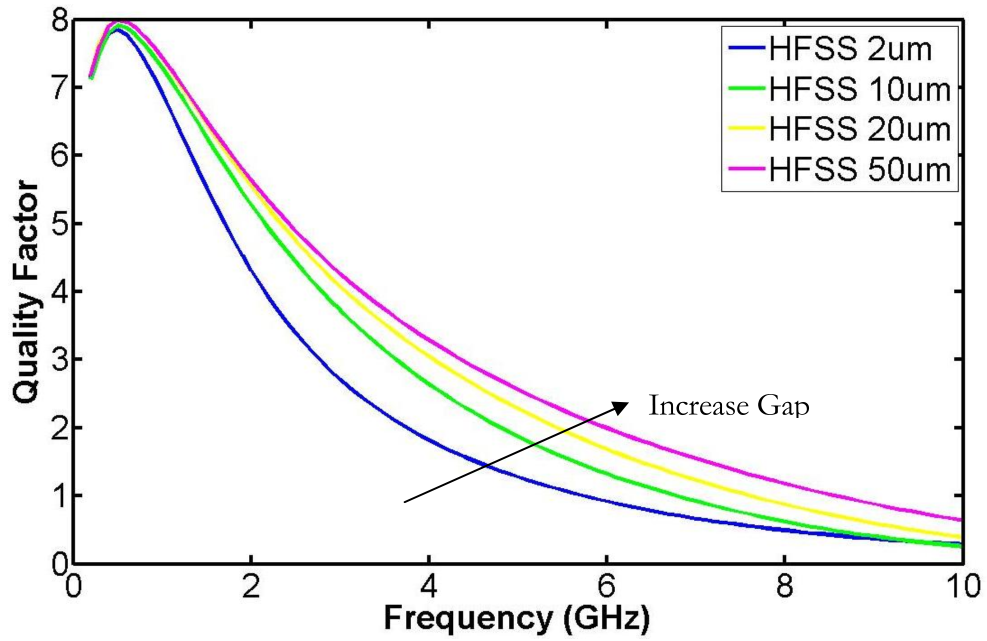


Figure 60: Simulated Q factor of inductor with different air gap thicknesses

4.3 HIGH Q TUNABLE RF MEMS INDUCTORS

4.3.1 Design

aluminum is one of the main conducting materials used in IC fabrication due to its good conductivity and compatibility with CMOS processes. Due to their excellent conductivity, copper and gold are introduced into IC compatible high-Q RFIC applications [47]. Since the effect of the substrate resistivity on the performance of inductors is well known, other materials such as glass and ceramics are used for RF and microwave applications.

Ansoft's HFSS [46] is once again used to study the RF performance of the inductors. Simulations show that by replacing the aluminum with gold, and the silicon substrate with alumina, the Q increases as shown in Figure 61. gold has a higher conductivity (σ_{gold}=4.6 x 10^7 S/m) than aluminum (σ_{Al}= 3.7 x10^7 S/m). A higher conductivity reduces the losses due to the skin effect. By changing the metal and the substrate, the Q peak widens and improves from a peak of 7 to 20. By using alumina; there is a reduction in the loss, which increases the Q.

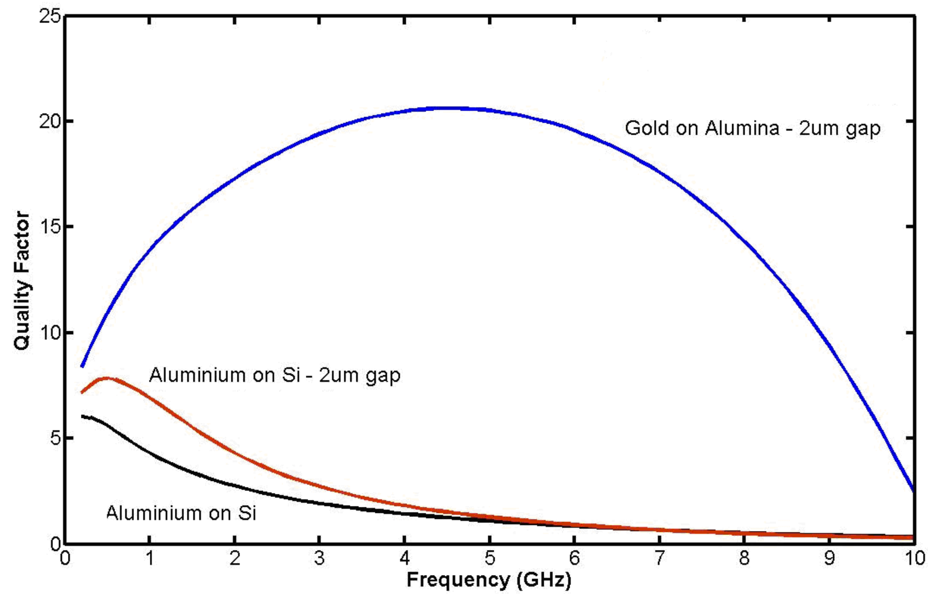


Figure 61: HFSS simulations comparing aluminum on Silicon RF MEMS inductors and gold on Alumina RF MEMS inductors. The Q improves from 7 to 20.

From these simulations, a tunable inductor based on thermal actuation of a PAA and gold bimorph structural layer is presented. When a voltage is applied to the device, the structure will warp due to the difference in the CTE of the two materials.

4.3.2 Device Fabrication

In this design, a tunable inductor was composed of PAA and gold. The fabrication process is shown in Figure 62. A 25 mil alumina wafer was cleaned using a standard RCA-1 recipe. Afterwards, the first metal layer was deposited, 400 Å of chromium for adhesion, followed by 1 μm of evaporated gold. This layer was then patterned and etched to form the contact pad structure. The wafer was then coated with a 2 μm photoresist sacrificial layer. After hard baking to prevent any further outgassing, 1 μm of aluminum was sputtered. The aluminum film was then anodized in a 0.3M oxalic acid solution for 5

minutes or until the film became transparent. Anchor holes were patterned and etched using the RIE, which also removed the patterning photoresist. A thin 2000 Å layer of sputtered gold is deposited, followed by another 2 μm of electroplated gold. The top layer was patterned, after which the gold and the PAA were etched. The sacrificial resist was then removed via dry release in the RIE. Due to the residual stress in the layers, the coil is warped after release.

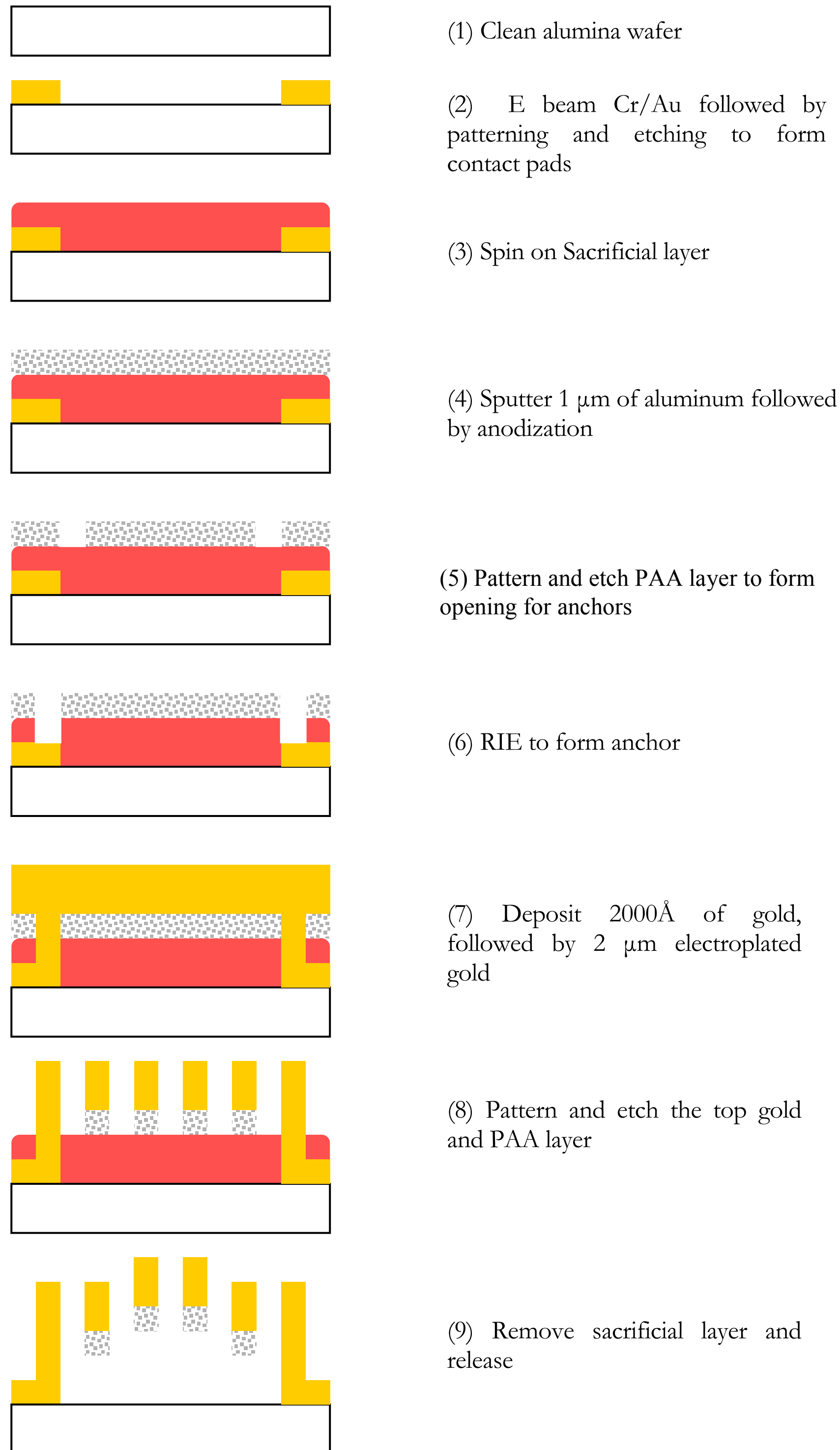


Figure 62: Fabrication of tunable RF MEMS Inductor based on gold/PAA layers

The gold/PAA structure warps in a similar manner as the aluminum/PAA structure. However, as shown in the Figure 63, the height displacement is less. The fabricated released structure seen in Figure 64 showed good agreement with the thermomechanical simulation.

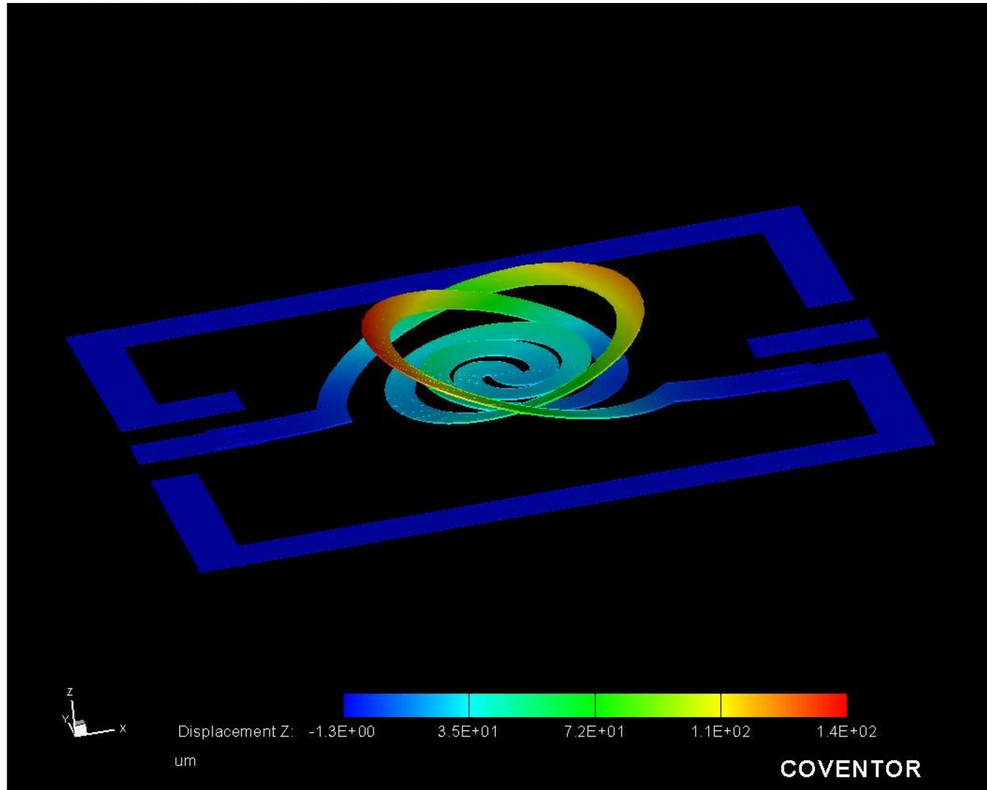


Figure 63: Thermomechanical simulation performed using CoventorWare of a fabricated tunable RF MEMS Inductor based on the gold/PAA bilayer structure.

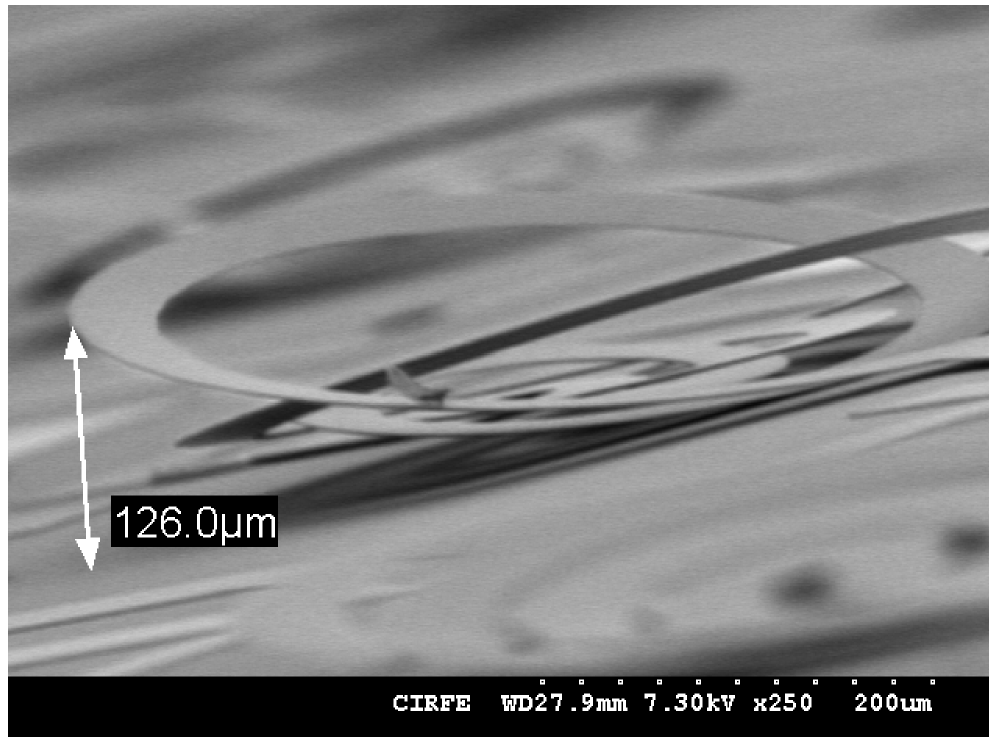


Figure 64: SEM of tunable RF MEMS inductor based on gold/PAA structure. The outer coil reached a height of nearly 130µm and shows good agreement with the simulated structure.

4.3.3 Measurement results and Simulations

The devices were measured using an Agilent 8510 network analyzer and Cascade Microtech GSG probes. Before any measurements were made, the system was calibrated using the short-open-load-through (SOLT) calibration. De-embedding was performed using open structures that were measured in order to remove the effects of the measurement pads and leads.

Figure 65 shows that when a DC voltage is applied across the device, the structure flattens.

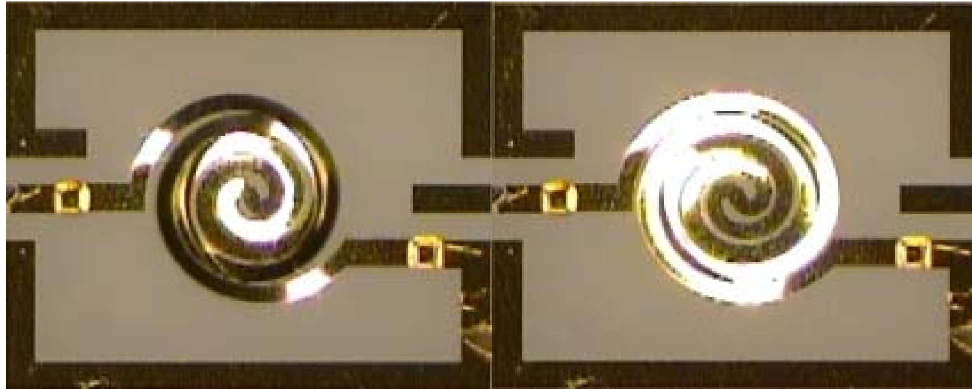


Figure 65: Top view micrograph of a 1 port RF MEMS tunable inductor (left) no actuation (right) with 1.4V applied across the device

As predicted, the Q of the gold/PAA devices as show in Figure 66 was much higher than the aluminum/PAA/aluminum sandwich devices, reaching a peak of over 30; however the tunability is greatly reduced. The reduced tunability is because the gold/PAA bilayer does not warp as much as the aluminum/PAA layer as seen in Figure 56 and Figure 63. The tunability is lower with a range of 7.45 nH to 7.7 nH or 3 % as shown in Figure 67.

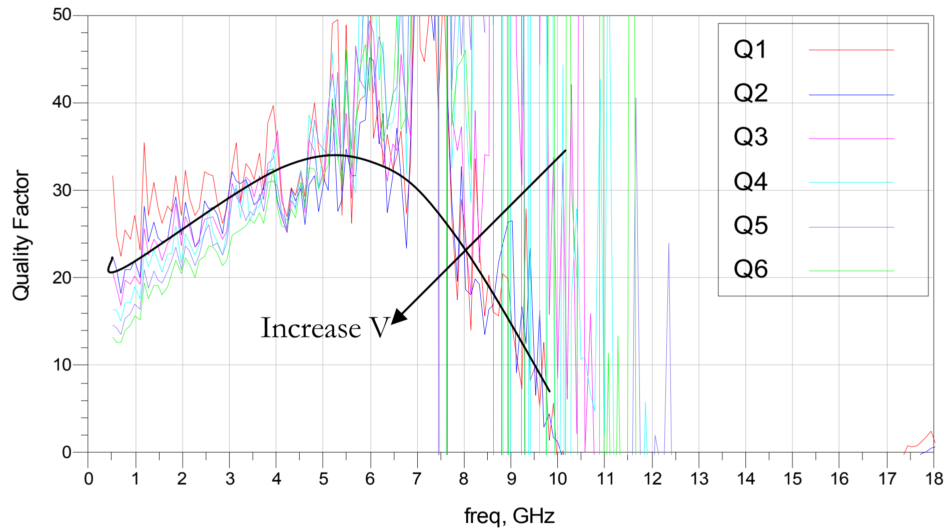


Figure 66: Measured Q of a fabricated RF MEMS tunable inductor based on the gold/PAA bilayer with 0 to 1.6 V applied across the device.

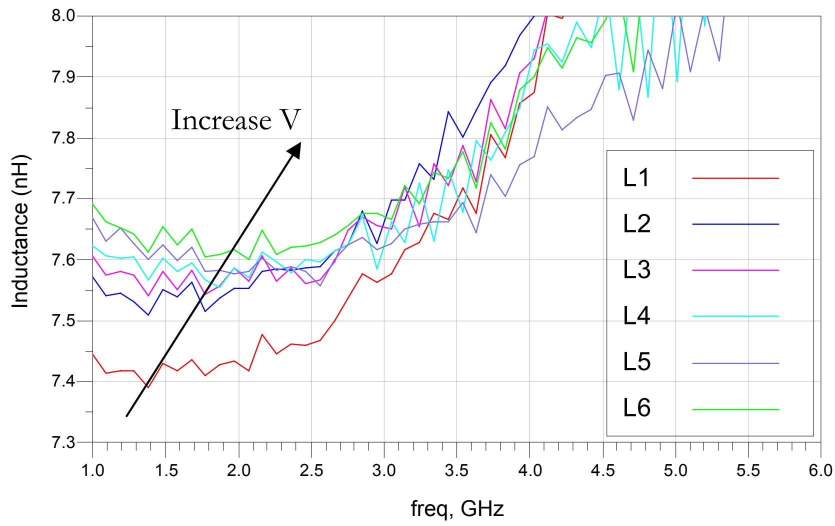


Figure 67: Measured inductance of a fabricated RF MEMS tunable inductor with 0 to 1.6V applied across the device.

The improved Q is promising and the gold/PAA bimorph process could be integrated with CMOS during post processing.

Chapter 5

5.1 Conclusions

The work in this thesis successfully introduced PAA as a low cost and low temperature material for use in CMOS RFICs and MEMS fabrication. The process development as well as material characterization was presented.

A simple and low cost anodic cell is used to form the PAA. Placed inside the electrolyte, a voltage is applied to the aluminum film. After a steady state is reached, the current begins to drop as the conductive material is consumed and PAA is formed.

Planar inductors and coplanar waveguide transmission lines were fabricated on silicon wafers with PAA as an isolation layer. Although PAA has a reasonable dielectric constant and high resistivity, the loss tangent is almost 10 times more than traditional Alumina ceramics. Although PAA is easily formed on silicon and Alumina substrates, the RF properties are still relatively unknown. However, due to the ability to tune the porosity, and therefore the stress and dielectric constant, there is a possibility for further material improvement.

Tunable RF MEMS inductors based on bimorph effect were fabricated and tested. After release, the coil warps away from the substrate due to the residual stress between the aluminum and PAA layer. By applying a DC voltage, the inductor begins to flatten in a controllable manner. The aluminum/PAA sandwich bilayer structure on silicon has a high tunability (31%) and a peak Q of 6. Simulations show that a simpler bilayer of aluminum and PAA would have a higher deflection height and therefore increase the Q and the tunability. Due to the low temperature fabrication, this process meets the thermal budget constraints of traditional CMOS processing.

To improve the Q, another bimorph structure based on a gold/PAA bilayer was fabricated on Alumina substrates. As predicted, the performance did improve; however

due to the lower deflection height of the bilayer coil, the tunability is greatly reduced. It is believed that with further tuning of the stress of the PAA film, the inductor performance could be improved.

Simulations were performed using HFSS to model the effects of the choice of conductive material and substrate. The measured results show good agreement with the simulated results.

5.2 Future Work

One of the main concerns regarding MEMS technology is packaging formats. A structure with such a large deflection height as the one presented in this thesis would require a clearance of over a few hundred microns. While on-wafer packaging is an attractive alternative to flip chip and wafer bonding, they are still in the developmental stages.

The initial inductor designs were based on aluminum and amorphous silicon bilayers. To optimize the inductors performance, the RF and material properties of PAA must be further understood. The inductor designs were only modeled on their planar structures. The warpage height depended greatly on the coiling and the position of the anchor and post. Future designs should focus on the thermomechanical simulations as a guide on the deflection height, and therefore the tuning of the quality factor and inductance.

Finally, the ability to use PAA with other materials is attractive and intriguing to the engineering designers' perspective. This author believes that PAA could be used in other bimorph structures such as RF switches and tunable capacitors. To our knowledge, this is the first time this material has been proposed and successfully used as a structural material for MEMS devices and CMOS processes.

GLOSSARY

AAO anodic aluminum oxide

CdS Cadmium Sulphide

CMOS complementary metal-oxide-semiconductor

CNT carbon nanotube

CPW coplanar waveguide

CTE coefficient of thermal expansion

CV capacitance-voltage measurement

CVD chemical vapour deposition

DC direct current

DNA Deoxyribunucleic acid

CNT carbon nanotube

EDP ethylenediamene pyrocatecol

f_{res} resonant frequency

GaAs gallium arsenide

GMD geometric mean distance

GSG ground signal ground

IC integrated circuit

KOH potassium hydroxide

L inductance

LNA low noise amplifier

M mole

MEMS microcrystalline silicon

PAA porous anodic alumina

PAN phosphoric-acetic-nitric acid

PLED polymer light emitting diode

pH potential of Hydrogen, or measure of acidity

RCA Radio Corporation of America

RF radio frequency

RFICs radio frequency integrated circuits

RIE reactive ion etching

S-parameters scattering parameters

$\mathbf{S_{11}}$ return loss

$\mathbf{S_{21}}$ insertion loss

SEM scanning electron microscope

SiGe silicon germanium

SOLT short open load through

TMAH tetramethyalmmonium hydroxide

VCO voltage controlled oscillators

$\mathbf{XeF_2}$ xenon difluoride

Y-parameters admittance parameters

Z-parameters impedance parameters

ZnO zinc oxide

Appendix A

FABRICATION PROCESS FOR RF MEMS TUNABLE INDUCTORS BASED ON THE ALUMINUM/PAA/ALUMINUM SANDWICH STRUCTURE

The following is a step by step process description of the 4 mask development for an aluminum/PAA/aluminum RF MEMS Tunable Inductor.

1. Clean Wafer

- Standard RCA-1 solution composed of DI water/ammonium hydroxide/hydrogen Peroxide (600ml/130ml/130ml)
- Heat to 70ºC and immerse samples
- Keep in solution for 15 minutes
- Rinse wafers in DI water, followed by N_2 dry

2. Aluminum 1 deposition using DC magnetron sputtering

- Argon flow = 50 sccm
- Power level = 500 W
- Deposition Rate = 180 Å
- Time= 55 minutes for 1μm thickness

3. Aluminum 1 Patterning using Mask 1

- Dispense AZ3312 photoresist onto wafer
- Spin at 3000 rpm for 30 s to give a thickness of 0.8μm
- Soft Bake at 90 ºC on vacuum hot plate for 60 s

- Expose for 12 s at 41 mW
- Post-Exposure Bake at 110°C on vacuum hot plate for 60 s
- Develop in AZ MIF 300 developer for 60 s with agitation
- Rinse with DI water and dry with N_2 gas

4. Etching of Aluminum 1 layer

- To etch aluminum, use PAN etchant. PAN etch is composed of H_3PO_4:H_2O:$C_2H_4O_2$:HNO_3 at 16:2:1:1.
- Heat up to 40°C and etch for 4 minutes
- Rinse with DI water and dry with N_2 gas

5. Remove Patterning Photoresist

- Heat AZ Kwik Strip to 70°C and immerse samples.
- Keep in solution for 15 minutes until all photoresist is removed
- Rinse with DI water and dry with N_2 gas

6. Sacrificial Layer and Anchor formation using Mask 2

- Dispense AZ3330 photoresist onto wafer
- Spin at 3000 rpm for 30 s to give a thickness of 2.2 μm
- Expose for 15 s at 41 mW
- Post-Exposure Bake at 110°C hot plate for 60 s
- Develop in AZ MIF 300 developer for 60 s with agitation
- Rinse with DI water and dry with N_2 gas
- Hard Bake at 120 °C on vacuum hot plate for 5 minutes

7. Aluminum 2 deposition

- Argon flow = 50 sccm
- Power level = 500 W
- Deposition Rate = 180 Å
- Time= 110 minutes for 2 μm thickness

8. Anodization

- To form 0.3M oxalic acid, measure 37.82g of anhydrous oxalic acid into 1L of DI water.
- Cover backside of silicon wafer with Kapton tape
- Tape a thin strip of Kapton tape on front side at interface of solution and air.
- Connect silicon wafer at anode and aluminum bar to cathode.
- Immerse silicon wafer and aluminum bar into the beaker with oxalic Acid. Make sure that the Kapton tape on the front side is at the interface.
- Place a magnetic stir bar inside beaker and apply spin for agitation
- Apply 40V. Current will begin to rise and plateau. Anodize for 3 minutes to form 1μm PAA film
- Remove silicon wafer
- Rinse with DI water and dry with N_2 gas

9. PAA Patterning using Mask 3

- Dispense AZ3312 photoresist onto wafer
- Spin at 3000rpm for 30 s to give a thickness of 0.8 μm
- Soft Bake at 90ºC on vacuum hot plate for 60 s
- Expose for 12 s at 41 mW

- Post-Exposure Bake at 110ºC (NO VACUUM) hot plate for 60s
- Develop in AZ MIF 300 developer for 60s with agitation
- Rinse with DI water and dry with N_2 gas

10. Etching of PAA layer

- To etch PAA, use PAN etchant and heat up to 40°C
- Etch 1µm PAA layer until the aluminum layer is reached. When the aluminum is exposed to PAN etch, hydrogen gas bubbles will form. Once this occurs, remove silicon sample from etchant.
- Rinse with DI water and dry with N_2 gas

11. Ashing of photoresist using Reactive Ion Etching

- Pressure= 500mTorr
- RF Power level =100 W
- Oxygen= 50 sccm
- Time= 300 s

12. Aluminum 3 deposition

- Argon flow = 50 sccm
- Power level = 500 W
- Deposition Rate = 180 Å
- Time= 110 minutes for 2µm thickness

13. Aluminum 3 Patterning using Mask 4

- Dispense AZ3312 photoresist onto wafer
- Spin at 3000 rpm for 30 s to give a thickness of 0.8 μm
- Soft Bake at 90 °C on vacuum hot plate for 60 s
- Expose for 12 s at 41 mW
- Post-Exposure Bake at 110 °C (NO VACUUM) hot plate for 60 s
- Develop in AZ MIF 300 developer for 60 s with agitation
- Rinse with DI water and dry with N_2 gas

14. Etching of Aluminum 3 and PAA layers

- To etch PAA, use PAN etchant.
- Heat up to 40 °C and etch for 6 minutes
- Rinse with DI water and dry with N_2 gas

15. Release

Begin with anisotropic etching

Step 1

- Pressure= 100 mTorr
- ICP Power level = 50 W
- Oxygen= 10 sccm
- Time= 300 s

For isotropic etching

Step 2

- Pressure= 100 mTorr
- ICP Power level = 100 W
- Oxygen= 10 sccm
- Time= 500 s

Step 3

- Pressure= 100 mTorr
- ICP Power level = 200 W
- Oxygen= 5 sccm
- Time= 1200 s

Step 4

- Pressure= 100 mTorr
- ICP Power level = 300 W
- Oxygen= 5 sccm
- Time= 1800 s

FABRICATION PROCESS FOR RF MEMS TUNABLE INDUCTORS USING GOLD AND PAA

The following is a step by step process description of the 3 mask development for an gold/PAA RF MEMS Tunable Inductor.

1. **Clean Alumina Wafer**

- Standard RCA-1 solution composed of DI water/ammonium hydroxide/hydrogen peroxide (600ml/130ml/130ml)
- Heat to 70ºC and immerse samples
- Keep in solution for 15 minutes
- Rinse wafers in DI water, followed by N_2 dry

2. **Chromium/gold deposition using E beam evaporator**

- Deposit 400 Å Cr adhesion layer, followed by 1 μm of gold

3. **Chromium/gold Patterning using Mask 1**

- Dispense AZ3312 photoresist onto wafer
- Spin at 3000 rpm for 30 s to give a thickness of 0.8 μm
- Soft Bake at 90 ºC on vacuum hot plate for 60 s
- Expose for 12 s at 41 mW
- Post-Exposure Bake at 110 ºC on vacuum hot plate for 60 s
- Develop in AZ MIF 300 developer for 60 s with agitation
- Rinse with DI water and dry with N_2 gas

4. Etching of chromium/gold layer

- Wet etch gold using Transene gold etchant for 3 minutes
- Rinse with DI water and dry with N_2 gas
- Wet etch chromium using Transene chromium 1020 etchant for 1 minute
- Rinse with DI water and dry with N_2 gas

5. Remove Patterning Photoresist

- Heat AZ Kwik Strip to 70ºC and immerse samples.
- Keep in solution for 15 minutes until all photoresist is removed
- Rinse with DI water and dry with N_2 gas

6. Sacrificial Layer

- Dispense AZ3330 photoresist onto wafer
- Spin at 3000 rpm for 30 s to give a thickness of 2.2 μm
- Hard Bake at 120 ºC on vacuum hot plate for 5 minutes

7. Aluminum 2 deposition

- Argon flow = 50 sccm
- Power level = 500 W
- Deposition Rate = 180 Å
- Time= 50 minutes for 1 μm thickness

8. Anodization

- To form 0.3M oxalic acid, measure 37.82 g of anhydrous oxalic acid into 1L of DI water.
- Tape a thin strip of Kapton tape on front side at interface of solution and air.
- Connect alumina wafer at anode and aluminum bar to cathode.
- Immerse alumina wafer and aluminum bar into the beaker with oxalic acid. Make sure that the Kapton tape on the front side is at the interface.
- Place a magnetic stir bar inside beaker and apply spin for agitation
- Apply 40V. Current will begin to rise and plateau. After a long steady state, the current will drop and the film will become transparent. When the current drops to nearly zero and the film is transparent, turn off power supply.
- Remove alumina wafer
- Rinse with DI water and dry with N_2 gas

9. PAA Patterning using Mask 2

- Dispense AZ3312 photoresist onto wafer
- Spin at 3000 rpm for 30 s to give a thickness of 0.8 μm
- Soft Bake at 90 °C on vacuum hot plate for 60 s
- Expose for 12 s at 41 mW
- Post-Exposure Bake at 110 °C (NO VACUUM) hot plate for 60 s
- Develop in AZ MIF 300 developer for 60 s with agitation
- Rinse with DI water and dry with N_2 gas

10. Etching of PAA layer

- To etch PAA, use PAN etchant.
- Heat up to 40 °C and etch for 4 minutes
- Rinse with DI water and dry with N_2 gas

11. Etching of Anchors using Reactive Ion Etching

For anisotropic etching of the photoresist sacrificial layer

- Pressure= 250 mTorr
- ICP Power level = 50 W
- RF Power level =100 W
- Oxygen= 30 sccm
- Time= 350 s

12. Gold seed sputtering deposition

- Argon flow = 10 sccm
- Power level = 300 W
- Deposition Rate = 300 Å
- Time= 6:40 minutes for 2000 Å thickness

13. Electroplate top gold layer

To electroplate 2μm of gold

- Current Density (ASF) =4
- Plating time (A-min) = 0.63

14. Top gold Patterning using Mask 3

- Dispense AZ3312 photoresist onto wafer
- Spin at 3000 rpm for 30 s to give a thickness of 0.8 μm
- Soft Bake at 90 °C on vacuum hot plate for 60 s
- Expose for 12 s at 41 mW
- Post-Exposure Bake at 110 °C (NO VACUUM) hot plate for 60 s
- Develop in AZ MIF 300 developer for 60 s with agitation
- Rinse with DI water and dry with N_2 gas

15. Etching of top gold

- Wet etch gold using Transene gold etchant for 8 minutes
- Rinse with DI water and dry with N_2 gas

16. Etching PAA layer

- To etch PAA, use PAN etchant.
- Heat up to 40°C and etch for 4 minutes
- Rinse with DI water and dry with N_2 gas

17. Release

Begin with anisotropic etching

Step 1

- Pressure= 100 mTorr
- ICP Power level = 50 W
- Oxygen= 10 sccm
- Time= 300 s

For isotropic etching

Step 2

- Pressure= 100 mTorr
- ICP Power level = 100 W
- Oxygen= 10 sccm
- Time= 500 s

Step 3

- Pressure= 100 mTorr
- ICP Power level = 200 W
- Oxygen= 5 sccm
- Time= 1200 s

Step 4

- Pressure= 100 mTorr
- ICP Power level = 300 W
- Oxygen= 5 sccm
- Time= 1800 s

Appendix B

DE EMBEDDING TECHNIQUES WITH Y MATRICES

In high frequency measurements, the parasitic components such as packaging, carriers or substrate choice will have a huge effect on the performance. In reality, inductors in IC are not encumbered by pads and are connected directly to other circuits via wire bonding or interconnect. For testing purposes, each inductor is connected to test pads so that on-wafer testing can be performed with the VNA. Once the values of the parasitic components are known, their effect can be eliminated by using matrix operations to get the true s-parameters of the device.

The device under test (DUT) is shown in Figure 1.

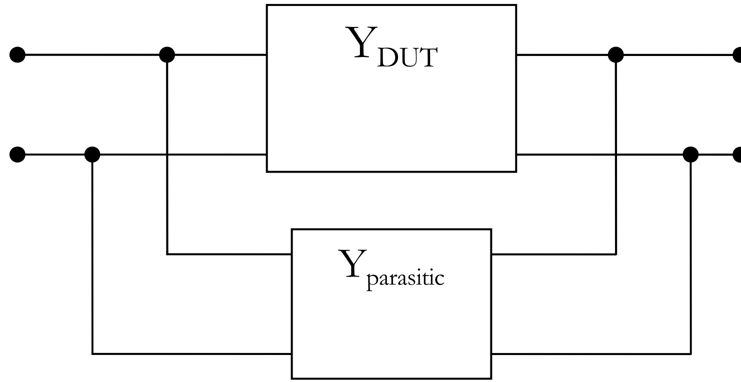


Figure 1: Schematic of test device and parasitics

Where to total Y parameter is:

$$Y_{TOTAL}=Y_{DUT}+Y_{PARAS}$$

For the inductors in this thesis, the main source of parasitic noise is from the metal contact pads. An open test structure is measured and the S-parameters are recorded, followed by the measurement of the inductor.

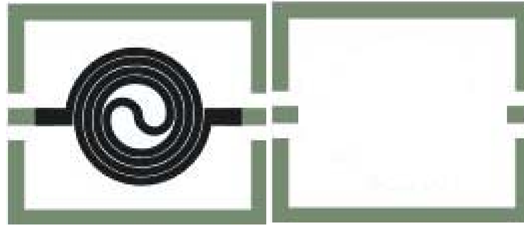


Figure 2: (left) inductor under test (right) open test structure

Once the S parameters are known, they can now be converted to Y parameters. The Y parameters of the true inductor is

$$Y_{DUT}=Y_{MEAS}+Y_{OPEN}$$

The true inductance and the quality factor of the inductor can now be calculated.

A p p e n d i x   C

SIMULATIONS FOR FINDING THE DIELECTRIC CONSTANT OF PAA USING A WAVEGUIDE RESONATOR LOADED WITH A KNOWN DIELECTRIC SLAB

Another method of finding the dielectric constant of an unknown substance is to place it inside a waveguide cavity. When a cavity is loaded with a dielectric material, a shift in the resonant frequency is observed. As the dielectric constant changes, so does the resonant frequency.

At first, an empty cavity is simulated using HFSS. Once the modes and resonant frequency is determined, a known dielectric slabs, in this case an alumina wafer $\varepsilon = 9.8$ is placed inside the cavity.

In order to determine the correct position of the dielectric, an empty cavity of 0.9" x 0.9" x 1.9" is simulated in HFSS and is shown in Figure 1 below.

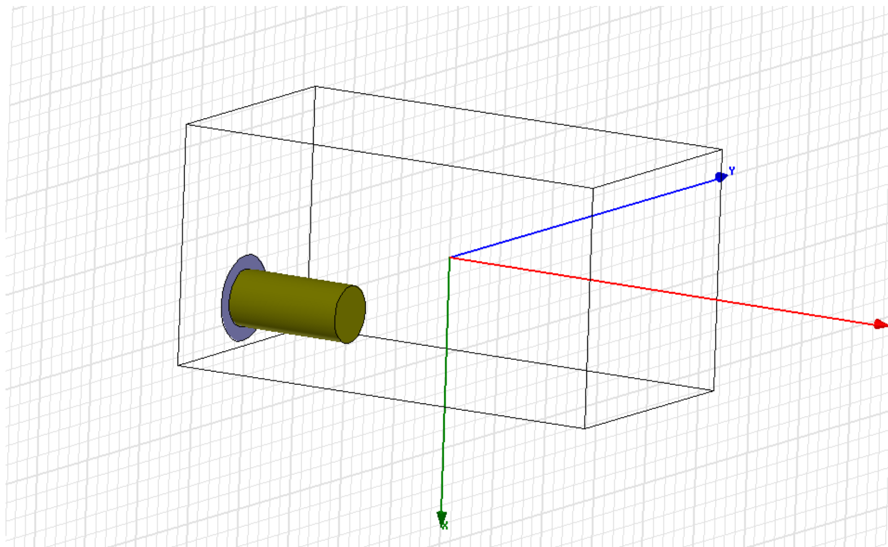


Figure 1: HFSS layout of cavity

A frequency sweep is conducted and the modes are examined. In Figure 2, a TE 113 mode at 12. 41 GHz is shown. The figure allows us to determine where to place the alumina sample as shown in Figure 3. The dimensions of the wafer are 0.5" x 1.0" x 25 mil.

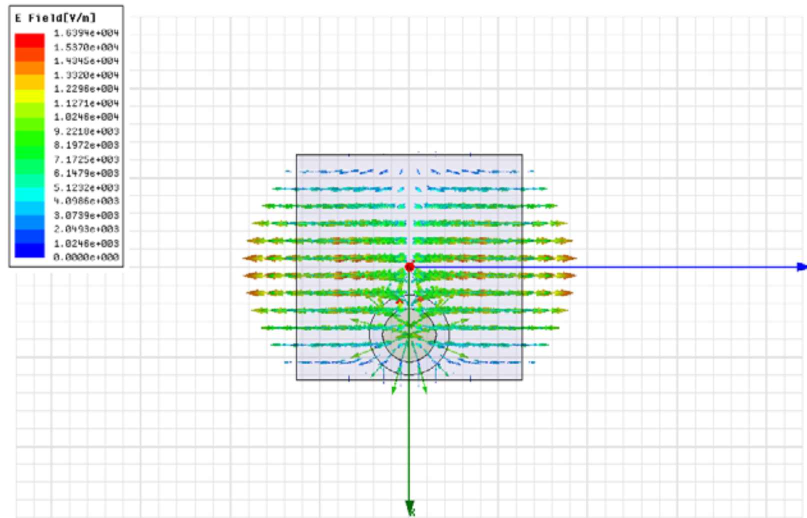


Figure 2: Electric field distribution of TE = 12. 41 GHz

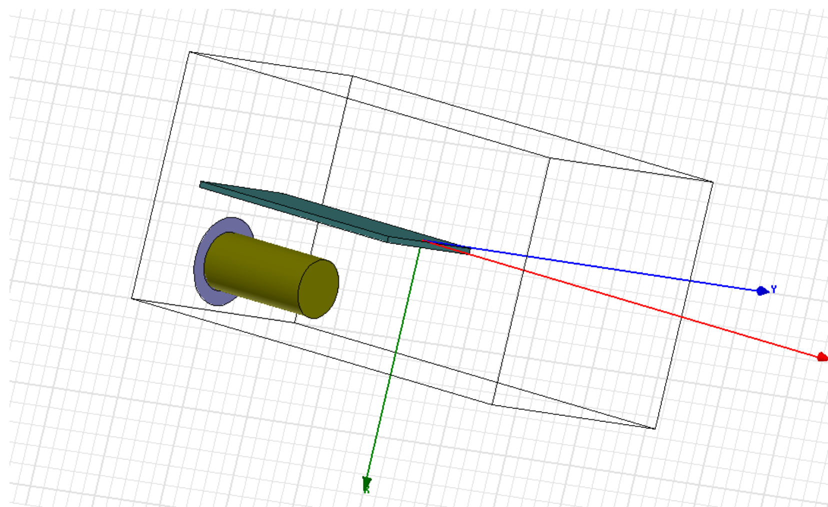


Figure 3: HFSS layout of cavity and alumina substrate

By looking at the S_{11} of both simulations, a different set of resonant frequencies is observed for the cavity with the dielectric slab. As shown in Figure 4. Figure 5 shows the electric fields of the cavity with the substrate inside.

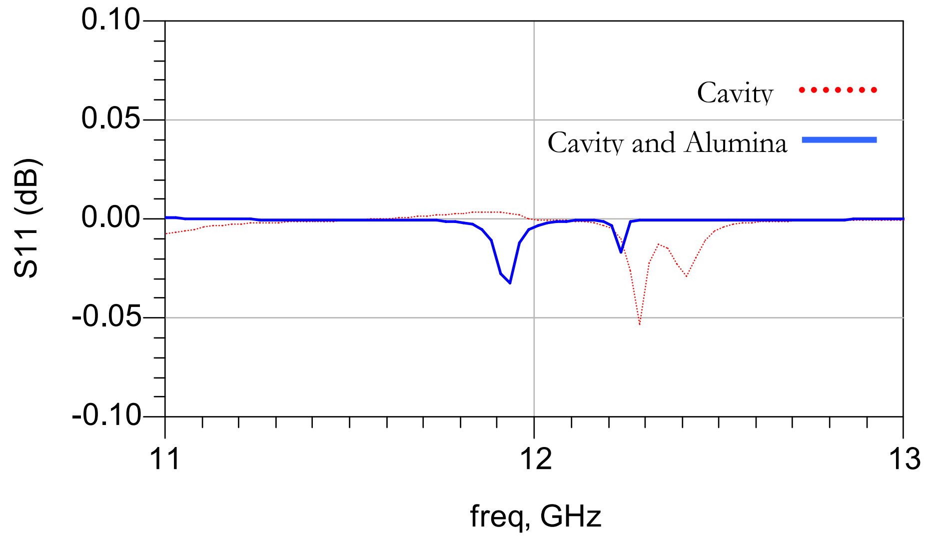
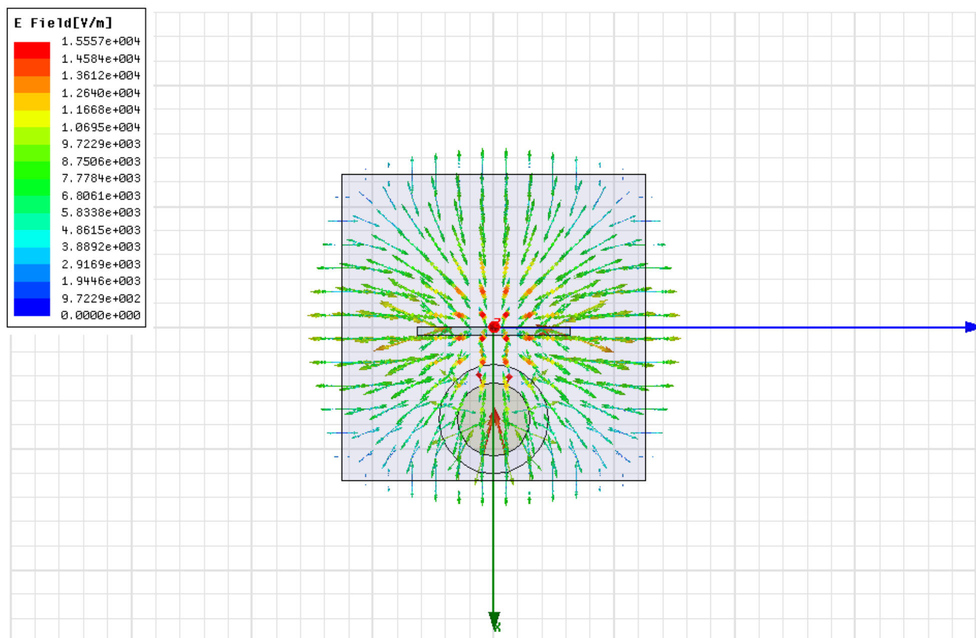


Figure 4: S_{11} of cavity and the cavity with the alumina substrate



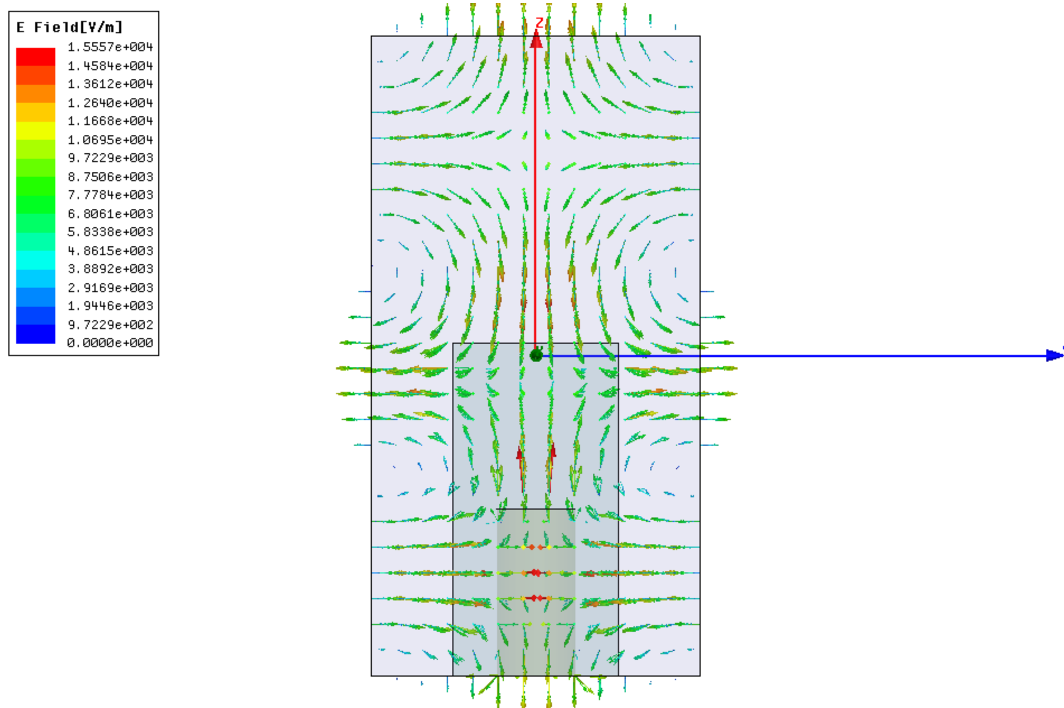


Figure 5: Electric field distribution of cavity with alumina substrate at 11.93 GHz

Another simulation is run by adding a 1um layer of PAA on the substrate as shown in Figure 6. This layer is given a $\varepsilon = 7.0$ (alumina is 9.8).

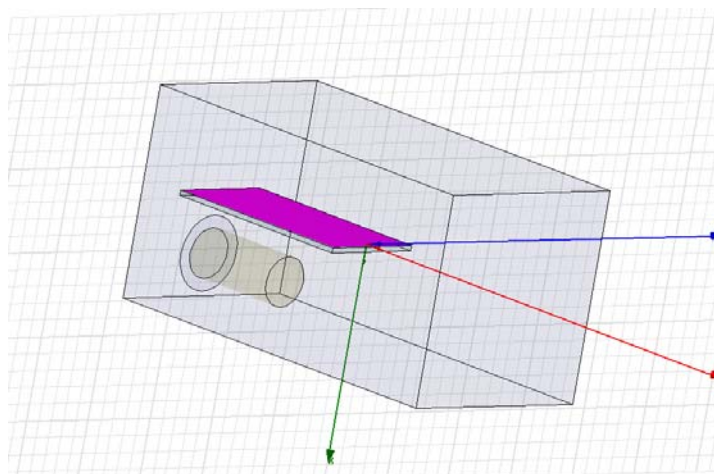


Figure 6: HFSS Layout of PAA layer on alumina inside cavity

As Figure 7 shows, the change in resonant frequency is very small after the PAA layer is added.

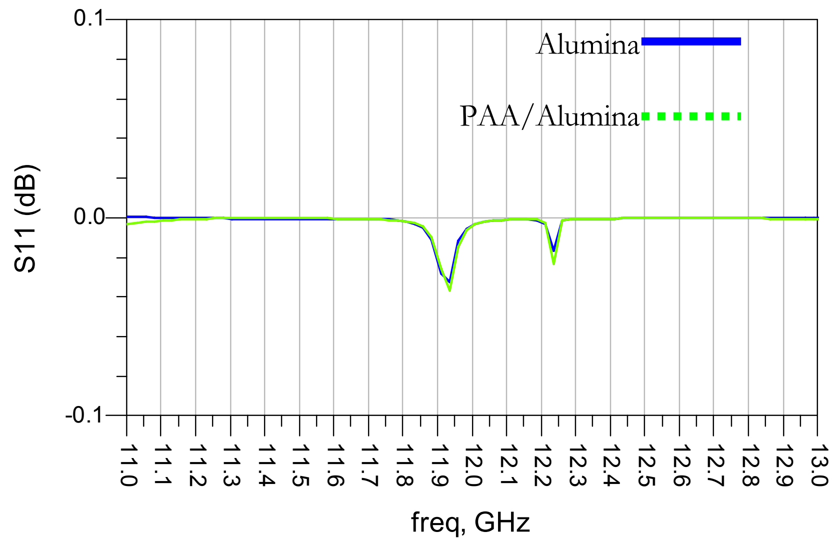


Figure 7: S_{11} of alumina substrate and alumina substrate with 1um layer of PAA

From these simulations, it is difficult to determine the dielectric constant of PAA. For a more accurate measurement, a dedicated setup is required. The alumina slab with and without PAA must be identical in size, which is difficult to do with dicing. A permanent Teflon post must be engineered inside the cavity so that the slab is corrected positioned.

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