Current Programmed Active Pixel Sensors for Large Area Diagnostic X-ray Imaging

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Rapid progress over the last decade on large area thin film transistor (TFT) arrays led to the emergence of high-performance, low-power, low-cost active matrix flat panel imagers. Despite the shortcomings associated with the instability and low mobility of TFTs, the amorphous silicon TFT technology still remains the primary solution for the backplane of flat panel imagers. The use of a-Si:H TFTs as the building block of the large area integrated circuit becomes challenging particularly when the role of the TFT is extended from traditional switching applications to on-pixel signal amplifier for large area digital imaging. This is the idea behind active pixel sensor (APS) architectures in which under each pixel an amplifier circuit consisting of one or two switching TFTs integrated with one amplifying TFT is fabricated. To take advantage of the full potential of these amplifiers, it is crucial to develop APS architectures to compensate for the limitations of the TFTs.

In this thesis several APS architectures are designed, simulated, fabricated, and tested addressing these challenges using the mask sets presented in Appendix A. The proposed APS architectures can compensate for inherent stabilities of the comprising TFTs. Therefore, the sensitivity of their output data to the transistor variations is significantly suppressed. This is achieved by using a well defined external current source instead of the traditional voltage source to reset the APS architectures during the reset cycle of their periodic operation. The performance of these circuits is analyzed in terms of their stability, settling time, noise, and temperature-dependence. For appropriate readout of the current mode APS architectures, high gain transresistance amplifiers with correlated double sampling capability is designed, simulated and fabricated in CMOS technology. Measurement and measurement based calculation results reveal that the proposed APS architectures can meet even the stringent requirements of low noise, real-time digital fluoroscopy.

Organization of the Thesis (6 Chapters)

In ***Chapter1,*** the general information on large area digital imaging and x-ray medical diagnostics imaging are introduced and presented. ***Chapter 2*** contains information on previously proposed active pixel sensor architectures as well as a new voltage mode APS capable of threshold voltage

shift compensation. For those readers unfamiliar with the operation and modeling of a-Si:H TFTs, an introduction is provided in Appendix B. In Appendix B, a-Si:H material shortcomings related to metastability, high temperature sensitivity and the challenges associated with designing analog circuits using a-Si:H TFTs as building blocks are also discussed. To address the problems of voltage mode APS architectures explained in chapter 2, a new generation of active pixel sensors called current programmed APS circuits is proposed. Several novel pixel architectures based on this idea are designed, simulated, fabricated, and tested. The results are presented in ***Chapter 3.*** The performance of these circuits is analyzed in terms of stability, settling time, temperature dependence and noise behaviour. For reset and readout of the current programmed APS designs presented in chapter 3, temperature independent current sources and high gain transresistance amplifiers are designed and implemented in conventional CMOS process. Measurement results revealed in ***Chapter 4*** show that the temperature invariant current source can provide stable current with less that 0.5% shift in spite of considerable variations in the characteristics of the TFTs involved in the circuit. The current amplifier is sensitive enough to be able to detect signals from the current mode APS circuits as low as 1nA, corresponding to lower signal range of fluoroscopic application. Detective quantum efficiency (DQE) measures the ability of the detector to transfer signal relative to noise from its input to its output. It is considered as the appropriate metric of system performance for an ideal detector. DQE(0) under various operating conditions is calculated and the significance of noise reduction is emphasized in ***Chapter 5***. Finally, the research work is summarized in ***Chapter 6*** with conclusion and contributions of the author to the field of large area digital imaging. Bibliographies are at the end of each chapter.

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List of Abbreviations

a-Se	Amorphous selenium
a-Si:H	Hydrogenated amorphous silicon
ADC	Analog to digital conversion
AMA	Active matrix array
AMFPI	Active matrix flat panel imager
APS	Active Pixel Sensor
DCAPS	Dual mode current-programmed, current-output active pixel sensor
CCII	Second Generation Current Conveyer
CDS	Correlated Double Sampling
CMOS	Complementary Metal Oxide Semiconductor
CT	Computed Tomography
DQE	Detective quantum efficiency
DR	Dynamic range
EHP	Electron-hole pair
keV	kilo electron volt
kVp	kilo volt peak
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTF	Modulation transfer function
NPS	Noise power spectrum
PECVD	Plasma Enhanced Chemical Vapour Deposition
SNR	Signal to noise ratio
TFT	Thin Film Transistor
V_T	Threshold Voltage

1 Introduction

1.1 Radiographic Imaging

Wilhelm Roentgen, a physicist at the University of Wurzburg discovered x-rays on November 8, 1895. This discovery was named “x rays” because “x” stands for an unknown quantity. For his work, Rontgen received the first Nobel Prize in Physics in 1901. This discovery led to the quick development of the field of medical imaging and Radiography. The images captured by radiography are very powerful diagnostic tools for physicians. When the ionizing radiation from the x-ray tube enters the body of the patient, it undergoes different attenuation depending on the tissue it passes through. This differential attenuation gives rise to the contrast in the final image required for high quality radiographic images.

In the conventional radiographic imaging system used to acquire the diagnostic x-ray images, a cassette of photographic film is positioned beneath a light emitting phosphor screen. X rays passing through the patient’s body impinge upon the screen and interact with the phosphor. The result of x-ray interaction with the phosphor is light photons that expose the radiographic film. The reaction between the light photons and the film gives rise to a latent image that is subsequently amplified by the chemical development process. This simple process makes the film based, analog technology for radiography. Recent advances in Liquid Crystal Display (LCD) and large area solid-state active matrix array technology have provided an alternative to the traditional film-based radiographic systems and made the transition to digital x-ray imaging systems possible. Digital x-ray imaging has significant advantages over its film-based analog counterpart: The captured x-ray images would become available immediately after the patient exposure for real-time imaging. They can be conveniently stored in the data base, transmitted to various medical centers over the communication networks, and retrieved by image processing software; and the inherent gain of the digital x-ray imaging systems allows improvement in different aspects of image quality including resolution and contrast as well as potential reduction in the required x-ray dose.

To replace the conventional film/screen cassette based analog x-ray imaging technology, it is proven that self scanned large area flat panel x-ray image detectors based on thin-film transistor (TFT) technology or switching diode active matrix array are very promising for diagnostic medical digital x-ray imaging applications such as chest radiography, fluoroscopy and mammography.

Extensive research in recent years has shown that the flat panel x-ray image detectors based on a large area thin-film transistor (TFT) or switching diode self- scanned active matrix array (AMA) is the most promising digital radiographic technique and suitable to replace the conventional x-ray film/screen cassettes for diagnostic medical digital x-ray imaging applications (e.g., mammography, chest radiography and fluoroscopy) [**1**] [**2**]. This technology allows the creation of imagers that contain two dimensional arrays based on thin-film electronics. Large area flat panel imagers employing active matrix arrays are often called active matrix flat panel imagers or AMFPI. There is very close similarity between the physical form of the AMFPI and the conventional film/screen based cassette. Therefore AMFPI can easily be used in the currently installed medical x-ray systems of the hospitals. Active matrix arrays of TFTs can be considered as large area integrated circuits. The technology has been developed and matured in the large area display industry. Therefore the extensive developed knowledge is ready to be used in for the digital x-ray imaging application. Immediately after the patient exposure to the diagnostic range x-ray, the image can be stored and displayed on the computer monitor. The readout of the x-ray image data from the AMFPIs can be achieved in less than 1/30 seconds. This image acquisition is fast enough for real-time imaging or fluoroscopy [**3**]. The use of AMFPIs enables imagers with dynamic ranges much higher than those currently achieved by the film/screen cassette based systems [**4**]. The captured images can be transmitted over the communication networks to remote locations for further diagnostic analysis. The technology has become widely available in a variety of projection and tomographic imaging applications including cardiovascular imaging, radiography, cone beam computed tomography (CT), portal imaging, mammography and fluoroscopy. Table 1.1 shows the various major imaging applications that use active matrix, flat panel imagers, the size of the imagers and the pixel pitch of the corresponding arrays.

Table 1.1. The table shows the extent to which active matrix, flat panel imagers have become available for a variety of different medical imaging applications [**5**].

Medical application	Array size of the AMFPI	Pixel Pitch
Fluoroscopy	13×13-43×43 cm^2	100-200µm
Cardiovascular Imaging	18×18-41×41 cm^2	154-200µm
Radiology	23×29-43×43cm^2	100-200µm
Mamography	17×24-24×31cm^2	70-100µm
Portal Imaging	30×40-41×41cm^2	392-800µm
Cone Beam CT	20×25-41×µ41cm^2	127-400µm

1.2 Flat-panel Detectors

Figure 1.1 shows the concept of AMFPIs. The radiation sensitive area of the imager is divided into millions of equally spaced segments called pixels. Each pixel can be considered as an isolated individual detector. The radiation sensitive part of the pixel converts the received radiation to a proportional amount of electric charge. The electric charge is first stored in each pixel and is ready to be read out by scanning the array row by row using the gate addressing electronics. The parallel data from different columns are multiplexed to a serial data and transmitted subsequently to a computer system for storage and display purposes. The x-rays first pass though the part of the body that is being imaged and are attenuated accordingly. The attenuated x-ray photons are incident on the large area AMFPI. To convert the x-ray photons to an electric charge signal under each pixel, two methods are used: In the first method called indirect approach, the x-ray photons are converted to visible light photons by a phosphor screen. The resulting visible light photons are detected by a pin photodiode at the pixel location; in the second method usually referred to as direct approach, an x-ray photoconductor converts the incident x rays to electric charge. For both methods of direct or indirect conversion, the latent x-ray image is in the form of charge density distribution across the area of the flat panel imager and stored on the storage capacitors of the various pixels constructing the entire array.

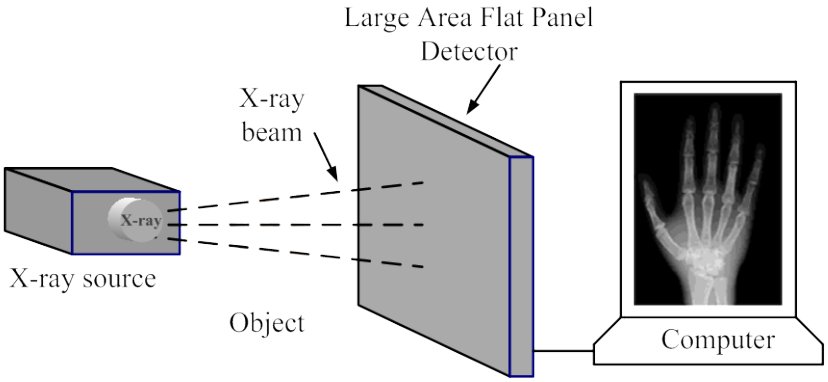


Figure 1.1 Schematic of a flat panel x-ray detector

AMFPIs using direct imaging scheme are believed to produce x-ray images with higher quality compared to those captured in the indirect imagers. Due to the simpler structure of the x-ray sensor in direct imagers, their manufacturing cost is also lower compared to that of indirect imagers [**6**] [**7**]. Figure 1.2 shows a photograph of a direct conversion AMFPI. In this thesis, direct conversion x-ray imagers are considered when calculating the detective quantum efficiency (DQE) of the detector. The fabrication process of the direct conversion imagers is simple and results in a compact and inherently digital structure [**8**].

Figure 1.2 Close-up picture of a corner of a Samsung (039-s) PPS based 45 cm X 45 cm indirect detection flat panel detector with 149μm pixel pitch [**9**].

1.3 Direct Conversion Detector

In direct conversion detectors, a photoconductor used to convert the incoming x-ray photons to charge carriers. The photoconductor used as the x-ray sensitive material has to have a wide bandgap (>2eV) so that it would have a small value for the dark current. It should also have a high atomic number to manifest large linear attenuation coefficient. One of the best candidates with these characteristics is the stabilized amorphous selenium, a-Se which can be deposited with the standard vacuum deposition techniques onto the active matrix array to act as the photoconductor layer. An electrode metal layer is deposited on top of the photoconductor layer to enable the application of a biasing voltage and consequently electric field F in the photoconductor layer. The electric field F causes the drift of the photo generated carriers to the top and bottom electrodes depending on the polarity of the applied voltage and the type of the carrier.

The x-rays are attenuated exponentially across the photoconductor thickness. They generate electron hole pairs (EHPs) with the concentration that decreases exponentially similar to the absorption profile of the x-rays as they traverse along the thickness of the photoconductor. The probability density of x-ray interaction with the photodetector for an incident x-ray photon at a distance x from the top electrode is given by

$$P_x(x) = \begin{cases} \alpha e^{-\alpha x}, & 0 \le x \le L \\ 0, & \text{elsewhere'} \end{cases} \quad (1.1)$$

Here α(E) is defined as the linear attenuation coefficient and E is the energy of the incident x-ray photon. The generated electron-hole pairs due to the absorption of x-ray photons drift along the field lines. Their movements cause charge induction of the storage capacitors of the pixels. Changing the polarity of the applied bias to the bias electrode, changes the movement direction of charge carries. Applying a positive voltage, causes the accumulation of holes on the pixel capacitor made out of the pixel electrode and the accumulation of electrons at the positive bias electrode. After going through the integration cycle, the amount of charge accumulated on each pixel capacitor is proportional to the amount of incident x-ray radiation incident over that pixel. Because of the thickness of the photoconductor layer, the capacitance from the photoconductor layer is much smaller than the pixel capacitance. Therefore, most of the applied voltage on the bias electrode drops across the photoconductor. The applied bias voltage value varies from few

hundred to several thousand volts depending on the thickness of the semiconductor layer. In order to be able to absorb all of the incoming x-rays, the thickness of the amorphous selenium layer should be about 500 μm. Also a high electric field (~10 V/μm) is required to successfully separate the EHPs generated by absorbed x-ray photons. Therefore the required bias voltage across the detector is around 5-10KV.

1.4 General Requirements of the Systems Used in Different X-ray Imaging Modalities

The digital x-ray imaging systems introduced as alternative solutions must meet the required performance criteria for the specific x-ray imaging modality. For instance, they should meet the appropriate resolution, dynamic range (DR) and timing requirements as well as the requirements on x-ray spectrum and mean exposure to the detector for the particular imaging modality, e.g., mammography, chest radiography, and fluoroscopy. Table1.2 summarizes the specifications and constraints on pixel size, detector area as well as the dynamic range for chest radiology, mammography and fluoroscopy.

Table 1.2 Parameters for digital x-ray imaging systems. kVp is the maximum kV value applied across the x-ray tube during the exposure, and the maximum energy of emitted x-ray photons is equal to the kVp value [**2**].

	Radiography	Mammography	Fluoroscopy
Imager size(cm)	23×29-43×43	17 × 24-24×31	13×13-43×43
Pixel size (μm)	100-200	70-100	127-200
Pixel Count	1750 x2150	3600 x4800	1000 x1000
Readout Time(S)	<5	<5	0.033/frame
X-ray Energy(KVp)	80-130	25-50	80
Exposure(mR)	0.03-3	0.6-240	0.0001-0.01
Patient thickness(cm)	20	5	20
Object Size	0.5mm(bone detail)	50-100μm	2mm

From the data in Table 1.2, it is seen that the readout in fluoroscopy should be achieved much faster than the other two modalities. Also, the patient dose is much smaller in fluoroscopy which imposes a challenge on the design and implementation of the associated detectors. Converting the dose to number of electrons, it is concluded that the minimum x-ray input signal yields merely 1000 signal electrons for both direct and indirect x-ray detection schemes. This makes the input signal vulnerable to noise added by the external readout electronics as well as the noise from the data and gate lines. The pixel size in mammography is the smallest among the three different modalities imposing challenge on the number of TFTs included in the circuit design for each pixel. Considering the timing requirements, the pixel size and the relative size of the input signal among different modalities presented in table 1.2, fluoroscopy has the most stringent requirements in terms of timing and noise behaviour while mammography needs the smallest pixel size for high-resolution imaging.

1.5 Different Photoconductors for Direct X-ray Medical Imaging

The choice of the photoconductor has a critical role on the performance of direct conversion x-ray detectors. The photoconductive layer should have the following properties to be considered an ideal choice for the x-ray sensitive layer of the detector:

(a) The photoconductor material should be able to generate as many electron-hole pairs as possible per incident radiation unit. In other words, the amount of radiation energy required to generate a single electron-hole pair should be as low as possible. This value is usually referred to as $W_{\pm}$ in the literature and typically increases with an increase in the bandgap of the photoconductor [**10**].

(b) For the diagnostic energy range of interest, most of the impinging photons on the x-ray detector should be absorbed within a reasonable distance from the radiation receiving surface of the photoconductor. In other words, the absorption depth δ of the x-rays must be substantially less than the photoconductor layer thickness deposited on top of the TFT circuit array.

(c) After the electron-hole pairs are generated as a result of x-ray exposure, they drift towards opposite electrodes in the array. As they drift towards the pixel and bias electrodes, the amount of bulk recombination should be minimized.

(d) Deep trapping of the EHPs should be negligible since the trapped carriers cause charge induction on the neighbouring pixels and therefore reduce the resolution of the imager.

(e) Overtime, the properties of the photoconductor layer should not deteriorate or change i.e. x-ray fatigue and x-ray damage should be negligible.

(f) The characteristics of the photoconductor over the area of the entire array should be as uniform as possible.

(g) The temporal artifacts such as image lag and ghosting should be as small as possible.

(h) The fabrication process of the photoconductor should be low cost and easy.

The ubiquity of AMFPIs using a-Si:H technology in various display applications like LCDs and AMOLEDs have made them a strong candidate for implementation of active matrix imagers. However they suffer from a number of performance limitations. The pixel gain of the a-Si:H imagers is modest compared to the electronic noise introduced by the data line and external charge amplifiers. This characteristic results in image quality degradation especially in the conditions of low exposure or high spatial frequency. This condition is valid in the case of fluoroscopy where the exposure rate for the minimum signal is below 1μR per frame or for imagers with very high degree of resolution requiring pixel pitch below 1μm. The frame rates of large area AMFPIs is usually smaller than x-ray image intensifiers and CCDs (charge coupled devices) or complementary metal oxide semiconductor (CMOS) sensors [**11**]. Image intensifiers are not shift invariant imagers and suffer from image distortion particularly in the edges of the image sensor [**2**]. CMOS sensors cannot be implemented in large area dimensions. Therefore the image has to be focused to a small area resulting in loss of resolution and quality of the image. To overcome these problems and be able to use large area imagers, one solution is the use of polycrystalline silicon (poly-Si) thin film transistors. The mobility of n and p channel poly-Si TFTs are two orders of magnitude higher that there a-Si:H TFT counterparts [**11**]. Therefore fast pixel circuits and rather complex CMOS type circuits can be implemented by this technology. The main drawback of poly-Si TFTs is their fabrication cost, their relatively high leakage current as well as their susceptibility to radiation damage. In this thesis an alternative approach is presented where amplifier pixels implemented with a-Si:H TFTs are fabricated in each pixel to

provide additional gain to the charge signal from the overlaying x-ray sensor. This additional gain suppresses the extra noise originated from the data line and off-panel electronics and makes the quantum noise limited imagers feasible. Sophisticated circuit techniques are used to overcome the problem of inherent low speed associated with a-Si:H TFTs. These circuit techniques can also address the problem of circuit design with a-Si:H TFTs risen from their inherent instability caused by voltage or temperature stress.

2 Passive Pixel Sensor and Voltage Programmed Active Pixel Sensors

In this chapter several voltage and current mode active pixel sensor (APS) designs are presented and described for use in different modalities of medical imaging. The basic operation of the architectures is presented with a focus on gain, metastability, linearity and readout speed. First, the currently popular and ubiquitous a-Si:H TFT switch based passive pixel sensor (PPS) architecture is introduced and the advantages and drawbacks are highlighted. Then, several a-Si:H TFT based active pixel sensors (APS) that attempt to address the shortcomings of the PPS are introduced. Unlike MOSFET, a-Si: TFTs are not well-known and widely used by circuit designers. Therefore, the operation and modeling of a-Si TFTs are discussed. Specific issues regarding the design of active pixel sensor circuits and using a-Si:H TFTs as analog amplifier component in the circuits are discussed. Based on measurements of in-house fabricated a-Si:H TFTs, it is shown that a-Si:H TFTs suffer from major limitations including instability, temperature dependence characteristic change, noise and power consumption. These limitations affect the performance of analog circuits with a-Si:H TFTs as their building blocks.

2.1 Passive Pixel Sensor (PPS)

Passive pixel sensor (PPS) architecture was first introduced by Gene Weckler [**12**]. Currently it is used as the pixel architecture of choice in many digital AMFPIs. Figure 2.1 shows the simple schematic of the PPS structure. It consists of a TFT acting as a switch along with a sensing element that can be a-Se photoconductor in the case of direct imaging or a photodiode in the case of indirect imaging [**13**]. All the pixels in one column share a common data line. The data line is connected to the input of the charge amplifier and transfers the charge accumulated on the storage capacitor to the feedback capacitor across the charge amplifier. This capacitor establishes a feedback with the opamp in the charge amplifier and converts the accumulated charge during integration into a stable voltage at the output of the charge amplifier (Figure 2.2) for further

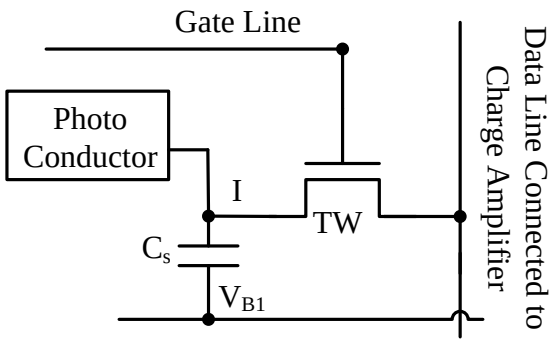


Figure 2.1 Passive Pixel Sensor (PPS) architecture connected to the x-ray sensor

processing with peripheral electronics as well as the correction software. All the gates of the switching TFTs in one row are connected together making a common row gate signal line. A clock generator scans the entire array and selects the pixels, one row at a time. In this architecture, reset and readout are performed simultaneously. During the readout, all the signal charge from various pixels located in the selected row is transferred through data lines to the input of the column charge amplifiers. The converted signals at the output of charge amplifiers are in the form of voltage. They are digitized with an A/D, multiplexed to the serial line and sent out for further image processing and display on the computer monitor [**14**].

2.1.1 PPS Operation Cycles

PPS pixel circuit has two modes of operation. In this architecture, readout and reset modes are achieved simultaneously.

• Integration Mode: Electric charge signal accumulates on C_S (Figure 2.1) which is equal to the total capacitance at the integration node (I) and is the summation of the storage capacitance and the parasitic capacitance of the gate-drain overlap. The amount of deposited charge is proportional to the amount of x-ray radiation.

• Readout/Reset Mode: After the integration, the accumulated signal charge on the storage capacitance is transferred from C_S to the column charge amplifier causing pixel readout and reset to occur simultaneously. The two inverting and non-inverting terminals of the charge amplifier are virtually grounded and the pixel capacitance, C_S, is reset to the voltage value equal to the bias voltage applied to the positive input of the charge amplifier at the end of readout/reset mode.

During simultaneous readout and reset, the switch TFT is biased in the linear mode of operation to provide a low ON resistance path for the quick transfer of charge to the external electronics. During the Integration, the TFT is biased in the OFF state acting like a switch in the non-conducting mode. The small leakage current flowing through the channel of the OFF TFT changes the voltage across C_S and corrupts the signal. Fortunately, in the a-Si:H TFT technology the leakage current is small (on the order of fA) and therefore the noise associated with the leakage current is manageable. The gate voltage applied to the switch TFT has a considerable effect on the value of the leakage current and choosing an optimal OFF voltage results in significant reduction of the drain-source leakage current. During the readout, the charge accumulated on C_S is transferred through the TFT ON resistance and subsequently converted to a voltage via the column charge amplifier.

Figure 2.2 shows the PPS structure used in direct imaging technology. The photodetector is represented by the large value resistor in the figure. The bias line is a continuous layer of metal coated on top of the selenium layer and it is shared among all the pixels in the array. The extra storage capacitor, C_S is fabricated in each pixel via the gate-drain metals [**14**]. This capacitor is required in case the parasitic capacitance made out of the gate-drain overlap capacitance and the data-line, gate-line overlap capacitance is not enough to hold the x-ray generated accumulated charge. The capacitance contributed by the a-Se sensor is usually very small. Since the thickness of the a-Se layer should be very large (200μm to 1mm) to be able to absorb a large segment of the incident x-rays, the value of its capacitance is very small and negligible compared to the magnitude of the storage capacitance [**15**].

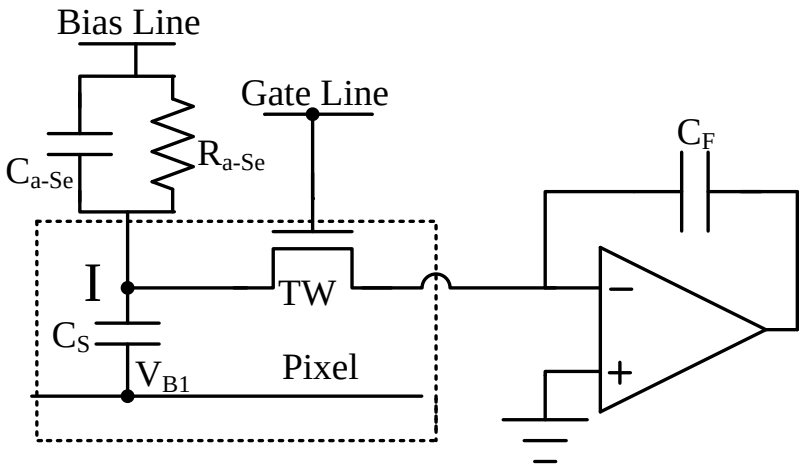


Figure 2.2 Schematic of the PPS structure connected to the column charge amplifier

Because of the large thickness required for the a-Se sensor, a large detector bias is necessary to generate a sufficiently large electric field across the photoconductor layer. The electric field should be large enough to be able to separate the generated electron-hole pairs and reduce the trapping probability of the generated carriers. The large sensor thickness also reduces the amount of sensor capacitance contribution to the integration node [**16**].

A problem that usually arises from application of a high value detector bias is large voltage build up at the integration node (I in Figure 2.2). The capacitance from the a-Se detector ($C_{a\text{-}Se}$) and the storage capacitor (C_s) form a capacitive divider. For typical thickness of the a-Se layer, its capacitance is in the range of several femtofarads. As the impinging x-ray photons generate carriers in the photoconductor layer represented by $C_{a\text{-}Se}$ and $R_{a\text{-}Se}$ in Figure 2.2, and they drift toward the storage capacitor (C_S), the problem becomes worse. The voltage at the integration node (I) can rise to very large values causing increase in the TFT leakage and eventual breakdown of the switching TFT, TW. To avoid this problem, the additional storage capacitor, C_S, is fabricated in series with TW. The typical value of the storage capacitor is about 1pF. It prevents the voltage at the integration node to become so large to cause TFT breakdown. Compared to the other parasitic capacitors, the value of C_S, is much larger and therefore it is the main contributor to the pixel capacitor.

2.1.2 Readout/Reset Rate of the PPS

Here we investigate the speed of reset and readout of the PPS structure and show by calculations that the readout and reset operation of the PPS structure is fast enough to be employed in real-time imaging applications. During reset/readout of the image array, the integration node is connected to virtual ground through the ON resistance of the switching TFT, R_{ON}. The storage capacitor is connecter in series to R_{ON} and they make a simple RC circuit. Therefore charge accumulated on the storage capacitance is discharged exponentially with the time constant τ_{ON} equal to:

$$\tau_{ON}=R_{ON}\times C_{PIX} \tag{2.1}$$

Here R_{ON} is the ON resistance of the switching TFT and C_{PIX} is the value of the pixel capacitance. Since the switching TFT is biased in the linear mode, approximating its operation with first order CMOS transistor equations, R_{ON} can be approximated as:

$$R_{ON} = \left[\frac{\mathrm{W}}{\mathrm{L}}\mu_{EFF}C_G(V_{GS}-V_T)\right]^{-1} \tag{2.2}$$

Here it is assumed that the TFT is biased in deep triode region, i.e: $V_{DS} << V_{GS} - V_T$. In this equation, V_{GS} is the gate-source voltage of the switching TFT, μ_{EFF} is the effective carrier mobility, C_G is the gate capacitance per unit area and V_T is the threshold voltage of the TFT. The conventional capacitance formula can be used to find the value for the intrinsic photoconductor capacitance:

$$C_{a-Se} = \frac{\epsilon_0 \times \epsilon_{a-Se} \times A_{PC}}{t_{a-Se}}, \tag{2.3}$$

Here, A_{PC}, is the pixel area and $t_{a\text{-}Se}$ is the thickness of the photoconductor. For the typical values of ε_0=8.85×10^{-12}F/m, $\varepsilon_{a\text{-}Se}$=6.5, A_{PC}=250×250μm^2, $t_{a\text{-}Se}$=1mm, $C_{a\text{-}Se}$ is about 3fF. The value of the storage capacitor is about 1pF. Therefore, C_{PIX} is approximately equal to 1pF. The typical values of V_{GS}, V_T, C_G, μ_{EFF} and W/L for the switching TFT are 15V, 2V, 25nF/cm^2 and 1cm^2/V.s, respectively. These values give the value for the ON resistance of the switching TFT to be around 1MΩ, i.e.: R_{ON} ~ 1 MΩ. For the typical design parameters, τ_{ON} can then be calculated to be around 1 μs. For efficient charge transfer in the typical RC circuit, about five times the RC time constant needs to be passed. Therefore the readout time is about 5 μs and therefore the

scheme is fast enough for real-time imaging or fluoroscopy. While the design of the PPS structure is quite compact and useful for high resolution imaging applications, the signal accumulated across the storage capacitor is directly exposed to the noise of the data line and off-panel charge amplifier. Providing on-pixel amplification suppresses the noise effect on the data line and the external off panel charge amplifier.

2.2 Voltage Mode Active Pixel Sensor

Figure 2.3 illustrates the schematic of the voltage mode APS architecture. Each pixel incorporates a single-stage amplifier in the form of a source-follower circuit. Thus, in addition to the usual photoconductor and addressing TFT, TR, the circuit elements that determine the operation of the pixel are a reset TFT, T_S, a source-follower TFT, TA, and the capacitance formed by parasitic effects between the associated data line and other elements of the design, C_S. The circuit is configured so that, when radiation is detected in the vicinity of the pixel: (a) the photoconductor capacitance is discharged; and (b) the potential of the gate electrode of the source-follower TFT is reduced in proportion to the amount of imaging signal generated by the x-ray radiation. In this way, the image is recorded in the pixels across the storage capacitors. The imaging signal stored in the pixel is then sampled and amplified by turning on the addressing TFT, TR. This results in the creation of a current flow that charges the data line capacitance (C_d). If the addressing TFT is left in the conducting state sufficiently long, current flow will continue until the potential of the data line approaches that of the gate of TA minus the threshold voltage of TA. In this way, the pixel imaging charge signal is amplified by an amount equal to the ratio of the capacitance of the data line to that of the photoconductor, i.e.:

$$\textit{Charge gain}=C_d/C_S \tag{2.4}$$

The change in the potential across the data line capacitance as a result of this sampling is approximately equal to the change in the potential of the gate contact as a result of the radiation. Next, the imaging signal stored in the data line capacitance is read out by an external charge preamplifier. After integration, the preamplifier is initialized and the pixel reset TFT,T_S, is used

to return the pixel to its initial state, leaving the potential across the x-ray sensor at V_{DD} and the pixel storage capacitor re-charged.

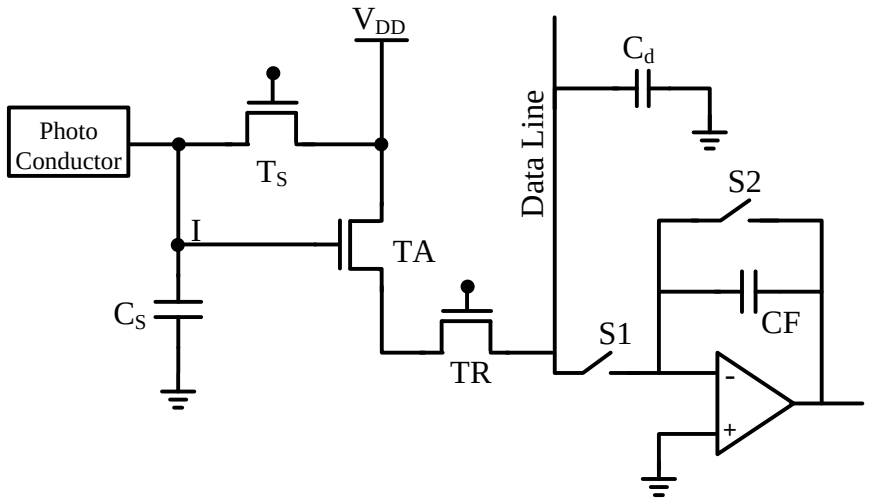


Figure 2.3 Three TFT Voltage Mode Active Pixel Sensor [**15**].

The voltage mode APS in Figure 2.3 provides a considerable amount of charge gain since the data line capacitance which consists of many parasitic and overlap capacitors is usually in the order of several tens of picofarads where as the storage capacitor is usually less than 1pF. The problem with the above scheme is that the signal readout is not fast enough to meet the timing requirements of fast imaging modalities such as fluoroscopy, particularly if a-Si:H technology is used for the fabrication of the AMFPI array. Some of the imaging modalities such as mammography require large imaging arrays with 3600 x 4800 pixels and a fast readout scheme [**13**]. Large area arrays have large column capacitances. The column capacitance comprises primarily of the gate to source capacitances as well as the overlap capacitances of the TFTs and data and gate lines. This capacitance is usually in the range of 10 pF to 100 pF depending on the size of the array. On the other hand, in the a-Si:H TFT technology, the current amplitudes are small because of relatively small mobility of the majority carriers in the channel. For instance if the output current of the APS is about 1μA, and the line capacitance is 100pF, it takes about 1.5ms for the APS to fully charge the line capacitance. Therefore the voltage mode APS is not suitable for real time imaging applications. To further investigate the operation of the voltage mode APS, a test pixel was fabricated in-house and is shown in Figure 2.4. The measurement

results in Figure 2.5 show high degree of linearity for large signal operation. For accurate voltage measurement, Keithley Model 236 SMUs are used to supply and measure the input and output voltages, respectively.

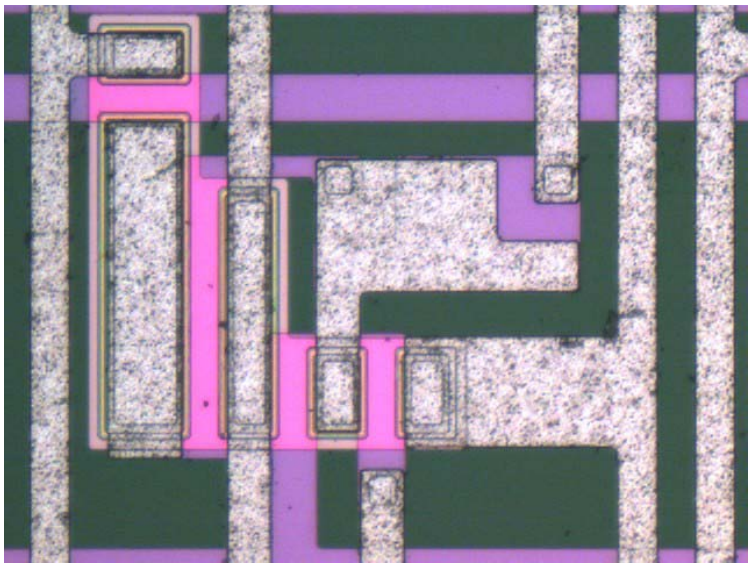


Figure 2.4 The micrograph of the voltage mode APS fabricated with a-Si:H technology at university of waterloo.

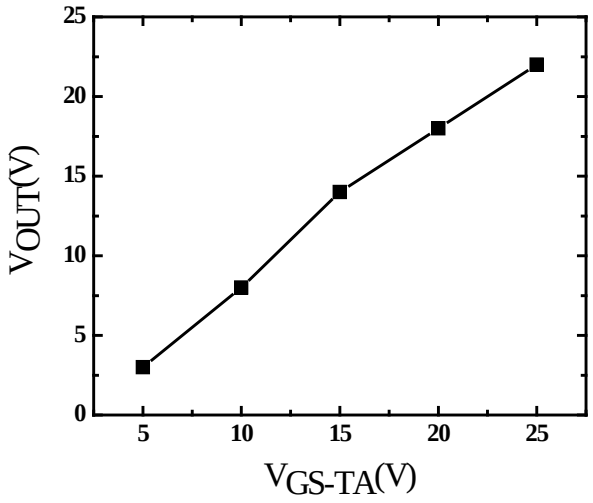


Figure 2.5 Linearity of the transfer characteristics of the voltage programmed APS in Figure 2.4.

2.3 Voltage Programmed APS circuit with threshold voltage shift compensation

In the voltage programmed scheme of Figure 2.3, a constant voltage is used to reset the APS pixel circuit. Therefore there is no feedback mechanism to compensate for the on pixel variations of the threshold voltage shift [**17**], [**18**]. To mitigate this problem, one solution is to have a pixel architecture in which the V_T shift compensation is achieved by on-pixel calculation of the absolute value of the threshold voltage. This value can then be added to a fixed voltage value that is used to bias the amplifying TFT during readout. Figure 2.6 illustrates the operation and the general concept of this driving scheme. The programming cycle starts by precharging a capacitor (C_C) to a voltage larger than V_T of the drive TFT (T_1). During the compensating phase, C_C is connected to the gate of T_1 while T_1 is diode connected. As a result, the capacitor discharges through the channel of T_1, and the capacitor voltage (V_C) degrades until it gets close to V_T. Then a predefined voltage value, (V_{Bias}) is added to the voltage of the capacitor, thus, a gate-source voltage close to V_T+V_{Bias} is applied to T_1. If T_1 is in the saturation region, the current through T_1 is independent of V_T and is given by

$$I_{out} = \frac{1}{2} \times k_{TA}(V_{bias} + V_T - V_T)^2 \tag{2.5}$$

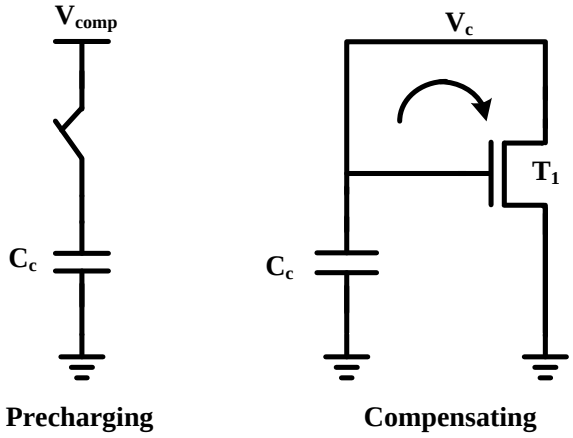


Figure 2.6 Mechanism for threshold voltage compensation using voltage mode programming

In the next section, an APS realizing this method of compensation for threshold voltage shift is presented.

2.4 Realization of Voltage Programmed, Threshold Voltage Shift Compensated APS

The voltage programmed active pixel sensor (APS) circuit in Figure 2.7 features five TFTs to compensate for the threshold voltage shift of the amplifying TFT (AMP) [**19**]. Central to the circuit is a degenerate common source circuit comprising AMP and LOAD TFTs, which produces a current output to drive an external charge amplifier. The active matrix array architecture is assumed to be column-parallel, i.e. one charge amplifier per column so that an entire row can be read out simultaneously. The APS circuit operates in three modes:

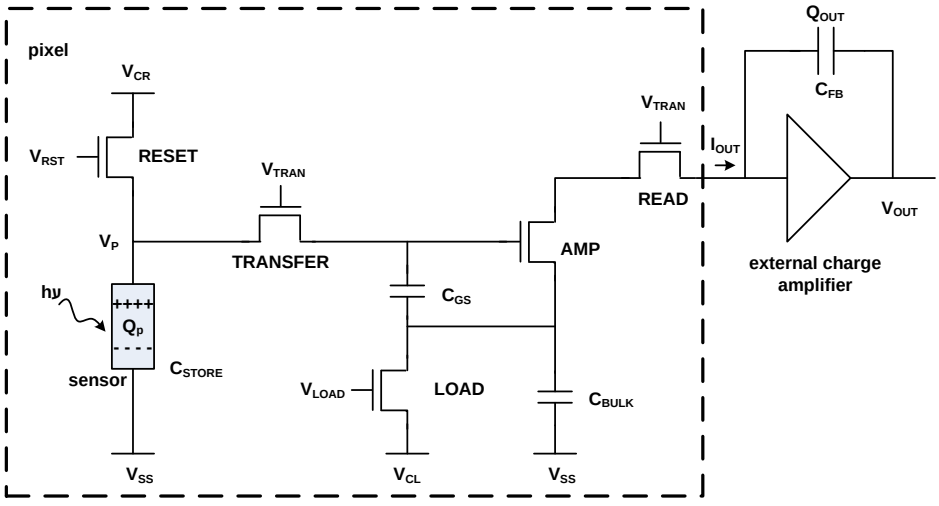


Figure 2.7 Schematic diagram of voltage programmed, current output APS with V_T shift compensation capability

(i) Initialisation: This mode itself is divided into two sub-steps to precharge the capacitor C_{GS} to V_T of the AMP TFT:

a. Current flow: Here the RESET, TRANSFER and LOAD TFTs are pulsed ON. V_{CR} and V_{CL} are set to 0 and -20 V, respectively. The gate voltage of the AMP TFT becomes 0 V and the AMP TFT operates in the saturation region.

b. Threshold voltage (V_T) extraction: The LOAD TFT switch is turned OFF. As a result, the current through the AMP TFT causes its source voltage to increase. This increase will continue until the gate-source voltage of the AMP TFT reaches its threshold voltage value, V_T. As a consequence, the AMP TFT is turned OFF and its gate and source nodal voltages are 0 and V_T, respectively.

(ii) Integration: TRANSFER is pulsed OFF while RESET is turned ON, and VCR is programmed to V_{DD}. Consequently C_{STORE} charges up to Q_P through the RESET TFT's ON-resistance. Afterwards, the RESET TFT is switched OFF and integration starts. During this integration period T_{INT}, the input signal generates carriers that discharge C_{STORE} by ΔQ_P and decreases its potential by a small-signal voltage of ΔV_P.

(iii) Readout mode: After integration, the TRANSFER TFT is turned ON. A step voltage with an amplitude V_{DD}-ΔV_P will be applied to the gate of the AMP TFT. This step voltage causes an increase in the source voltage of the AMP TFT equal to:

$$(V_{DD} - \Delta V_P) \times \frac{C_{GS}}{C_{GS} + C_{BULK}} \tag{2.6}$$

If C_{GS} is designed to be much smaller than C_{BULK}, this increase will become negligible and the source terminal will retain its initial value of V_T. So the applied voltage across the gate-source of the AMP TFT will be:

$$V_{DD} - \Delta V_P + V_T \tag{2.7}$$

On the other hand, to the first order of approximation, the drain-source current expressions of the TFT are:

$$I_{DS} = \frac{W}{L}\mu C_I \left[(V_{GS} - V_{T0})^{\frac{2}{K_l}} - (V_{GS} - V_{T0} - V_{DS})^{\frac{2}{K_l}}\right] x_S \quad \text{for } V_D \leq V_{GS} - V_T$$
$$I_D = \frac{W}{L}\mu C_I (V_{GS} - V_{T0})^{\frac{2}{K_l}} x_S \quad \text{for } V_D \geq V_{GS} - V_T \tag{2.8}$$

It is apparent, from substituting the gate-source voltage (3.18) into (3.19), that the output current of the AMP TFT has become independent of its threshold voltage. Finally the TRANSFER TFT is turned OFF and the LOAD TFT is switched ON to provide a current sinking path. The current through the AMP TFT will flow to the charge amplifier and develop a voltage across its capacitance which is proportional to:

$$V_{data} = V_{DD} - \Delta V_P \tag{2.9}$$

Evaluation of the stability and linearity of the proposed pixel circuit is examined with an in-house developed amorphous silicon device model and Cadence SPECTRE simulator (Cadence Design Systems Inc.). Here, C_{STORE}, C_{GS} and C_{BULK} are chosen to be 2, 0.2 and 4 pF, respectively. Also the TFT sizes are:

$$\begin{gathered}(W/L)_{AMP} = 150\mu m/23\mu m \\ (W/L)_{TRANSFER} = (W/L)_{LOAD} = (W/L)_{READ} = 50\mu m/23\mu m\end{gathered} \tag{2.10}$$

Figure 2.8 illustrates the readout current (I_{OUT}) of the AMP TFT against its threshold voltage for a nominal current of 1 μA. It can be seen that the relative error in the output current is less than 1% due to variation in the threshold voltage. On the same graph, the output current of a 3-TFT APS circuit is plotted and shows almost a 20% fluctuation on 1 V change in threshold voltage. According to these simulated data, the proposed pixel circuit provides at least a tenfold improvement in output current stability, which is essential in ensuring reliable long-term APS performance. Figure 2.9 shows a linear pixel current gain of 4 on the input charge signal accumulated at C_{STORE} during integration. Combining with off-pixel amplification, the circuit will meet the requirements of the low dose X-ray imaging modalities.

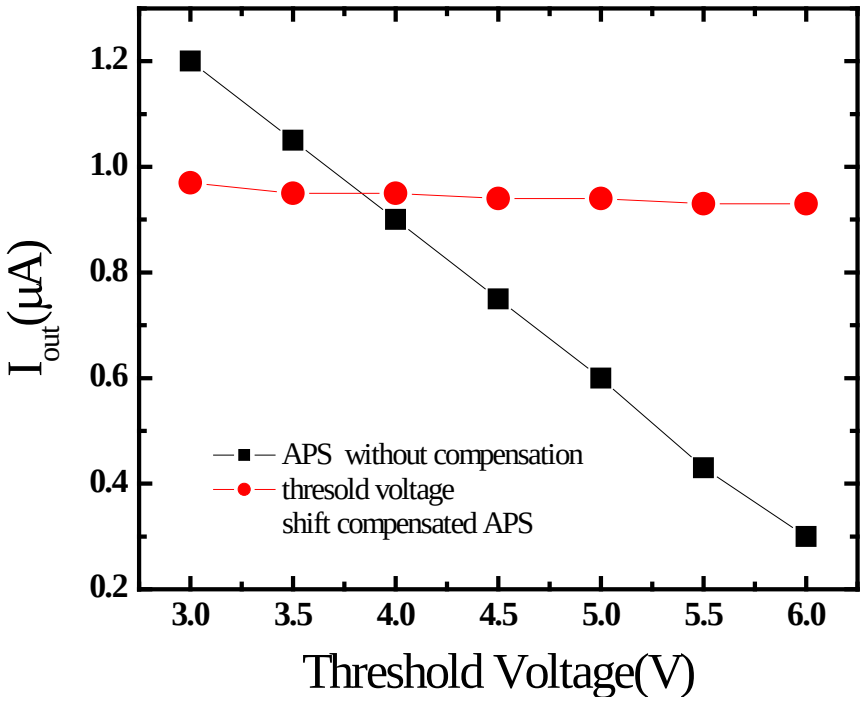


Figure 2.8 Output Current versus Threshold Voltage Shift

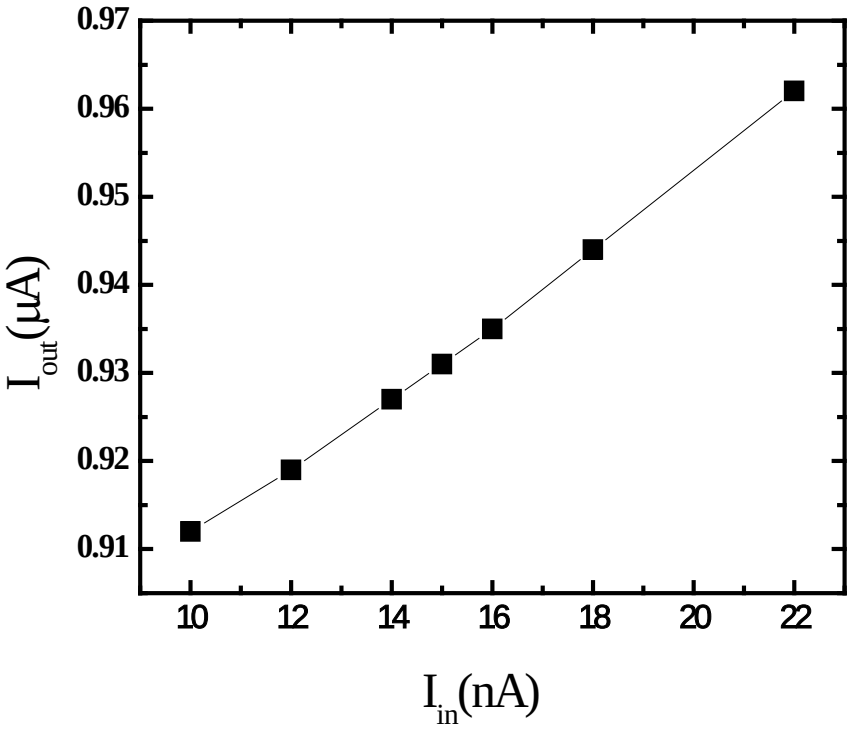


Figure 2.9 Input-Output Transfer Characteristic demonstrating the current gain of the APS

2.5 Current Mediated Active Pixel Sensor

Voltage mode APS has the advantage of non-destructive readout in the sense that regardless of the number of signal readouts of the APS, the initial voltage established across the storage capacitor in unaffected. By several readouts of the original signal and taking the average of the set, the output signal is effectively low pass filtered causing noise reduction of the signal. Also, it is possible to subtract the reset signal from the x-ray signal without any reset in between. This way, the thermal noise accumulated across the capacitor or the KTC noise as well as the low frequency 1/f noise can be effectively cancelled or reduced. However, its implementation in a-Si technology is unsuitable for real time performance posing a challenge to some medical imaging applications such as fluoroscopy [**13**]. Hence, it is necessary to modify the APS in such a way to provide high speed readout as well as gain to reduce the noise effect. The circuit in Figure 2.10 has been proposed to provide a high speed solution for the real-time imaging application [**20**]. The difference between this circuit and the one shown in Figure 2.3 is that the source of the READ TFT which defines the output of the APS is constantly connected to the low impedance input terminal of the charge amplifier. The low input impedance effectively suppresses the large capacitance associated with the data line and decreases the readout time to values acceptable for fluoroscopic applications.

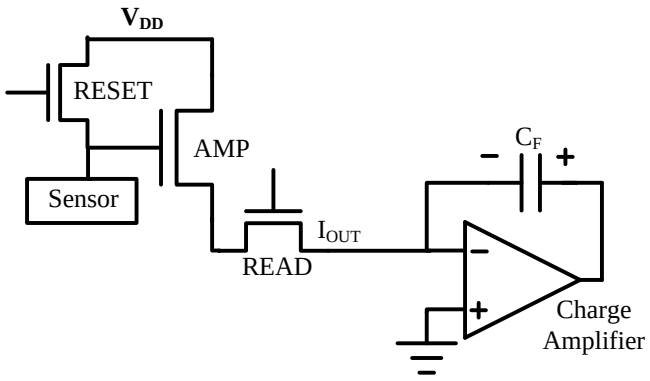


Figure 2.10 Schematic of the Current Mediated a-Si:H pixel circuit [**20**].

During the readout, the APS reduces to a source follower topology consisting of AMP as the amplifying TFT and READ as the switch TFT acting as a resistor. The total gain of the APS is proportional to the transconductance of this circuit given by,

$$G_{m-tot} = \frac{g_{m-AMP}}{1 + g_{m-AMP} \times R_{on-READ}} \tag{2.5}$$

Where, $G_{m\text{-}tot}$ is the total transconductance of the APS circuit, $g_{m\text{-}AMP}$ is the transconductance of the AMP TFT and $R_{on\text{-}READ}$ is the ON resistance of the READ TFT. If the pixel circuit is changed in a way that during readout, the circuit resembles a common source instead of a source follower configuration, we can expect the gain to increase by a factor of $1+ R_{on\text{-}READ}\times g_{m\text{-}AMP}$. Another drawback in the pixel in Figure 2.10 is that the transfer function of the a-Si:H TFTs has strong dependence to temperature as explained in the following sections. Therefore, if there is temperature variation across the array, it easily translates itself into fixed pattern noise or structure noise in the output image of the flat panel imager. In what follows, the details and challenges of designing the active pixel sensor circuits with the a-Si:H technology are investigated. Most of these challenges originate from instability of the a-Si:H TFTs caused by temperature or voltage stress. Unlike MOSFETs, a-Si:H TFTs are not widely used by analog circuit designers. Therefore a detailed study and investigation of the operation and characteristics of a-Si:H TFTs is crucial to the successful design of analog circuits using these type of transistors. A-Si:H TFTs are the building blocks of the APS circuits presented in this thesis. They are used both as switches and analog amplifiers in the presented APS circuits. However, since the a-Si TFT is not a well-known device for circuit designers, particularly as an analog device, an understanding of the device operation and its specific characteristics is essential. In what follows, a brief introduction to the operation and fabrication process of the a-Si:H TFT is provided and instabilities in the behaviour of a-Si:H TFT associated with temperature and voltage stress are discussed.

2.6 Conclusion

A-Si:H TFTs have many advantages for use as building blocks of backplane integrated circuit of large area active matrix flat panel imagers. These advantages include low fabrication cost, and well-established infrastructure. At the same time, they suffer from low effective mobility resulting in low transconductance gain, instability and high temperature sensitivity causing drift of the transconductance gain over time and with change in temperature (Appendix B). This makes their usage as an analog element in analog circuit design challenging and complicated. Therefore, to use a-Si:H TFTs in APS circuit design, which is analog in nature, driving schemes are required to compensate for device shortcomings in circuit level. In particular, for these driving schemes to be successful, they should be able to compensate for the variations in the threshold voltage and mobility over time and in a temperature varying environment. In this section, several previously proposed APS schemes and their shortcomings were discussed. Several instability measurements conducted on the in-house fabricated TFTs were presented confirming the instability mechanisms previously discussed by other scientists. A new voltage programmed APS capable of compensating for threshold voltage shift was presented. Eventhough the operation of this voltage mode APS is immune to instability induced variations in the characteristics of TFTs, the pixel circuit and its driving scheme is complex.

3 Current Programmed Active Pixel Sensors

As discussed in previous chapters, the output data current of the voltage programmed conventional 3-TFT APS pixel circuit is sensitive to the variations in the characteristics of the comprising TFTs including threshold voltage shift and mobility change [**12**]. The voltage or temperature stress induced shift in the TFT characteristics is an inherent property of a-Si:H TFTs, leading to fixed pattern noise and image quality degradation over the operational time of the imager. In order to reduce the sensitivity of the APS output data to the change in TFT characteristics, various programming schemes have been introduced. In this chapter, we discuss the details of several important APS programming schemes including current and voltage programming. The performance of the current programmed APS pixel circuits in terms of settling time and noise is investigated.

3.1 The Concept of Current Programming

In the APS current programming scheme, a predetermined off-panel generated current source is used to set the gate voltage of the amplifying TFT, TA, during each frame (Figure 3.1). Should the V_T of the amplifying TFT shift, the programming current adjusts the overdrive voltage of TA, (V_{GS}-V_T), to force the same current in TA each time thus making the pixel transconductance gain, G_m insensitive to variations in V_T over time. The same principle applies to process or temperature variations across the array. During the integration cycle, the sensor signal is integrated on the pixel sense node capacitance (C_S) and a voltage develops which changes the output current (I_{OUT}) during readout. Such a driving scheme compensates for the V_T shift in the TFTs since the APS current does not directly depend on the characteristics of the comprising TFTs. Figure 3.1 demonstrates the basic circuit diagram of a typical current programmed APS. Here the main components of the APS are the sensor, a storage capacitor (C_S), an amplifying TFT (TA), and some other TFTs acting as switches (S1 to S3). During the reset or programming cycle, S1 and S2 are turned on and S3 is turned OFF.

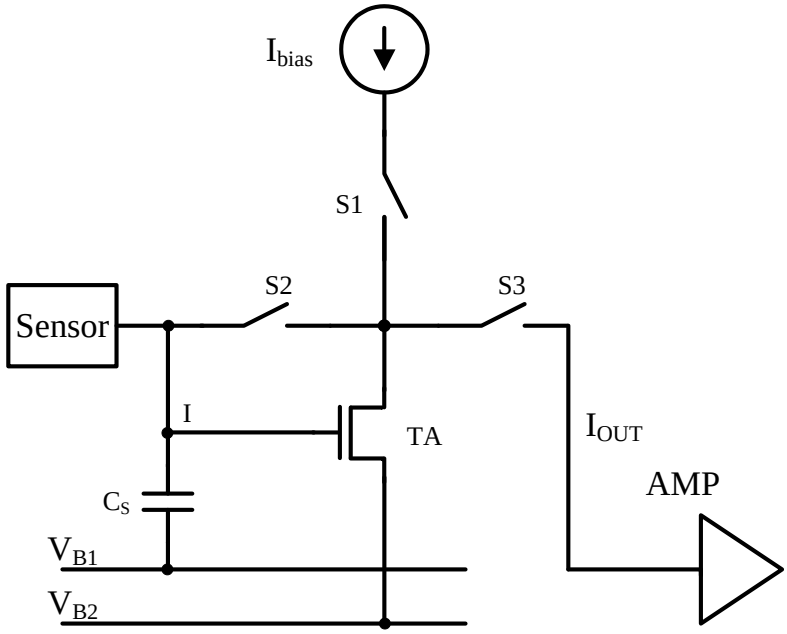


Figure 3.1 The basic circuit diagram of a typical current programmed APS.

The programming current flows into the amplifying TFT through S1 and S2 and the gate-source voltage of TA is stored in C_S. After the reset cycle, the switch TFTs are turned off and the storage capacitor is isolated from the data line. The electric charge due to incident X-ray signal changes the voltage across the storage capacitor during the integration cycle. In the readout cycle, switch S3 is turned ON and a copy of the programming current modulated by the amount of charge deposited on the storage capacitor flows to the off-panel charge or current amplifier. In the following sections, we elaborate on the settling time, stability and uniformity of the current programmed, current output APS pixel circuits.

3.2 Settling Time in Current Programmed APS

Even though it has been proved that programming the TFT circuits with a constant value off-panel CMOS current source can achieve high degree of stability [**21**], the usage of this method in real time imagers can be hindered due to the long settling caused by low mobility of the TFTs and the large parasitic capacitance of the reset line. In particular, for small sub μA programming currents, the settling time can be in the range of milliseconds which is far longer than the programming times required for high-resolution imagers. Therefore it is absolutely critical to

conduct a detail study of the settling time during the programming mode and find methods to reduce this time to the amounts acceptable for real-time imaging modalities (i.e. fluoroscopy). In the following a detailed model for tackling the problem is used to optimize the settling time and the model is simplified to derive analytical formulas proving insight to the relation between the settling time and various elements of the pixel circuit.

3.3 Analytical Model of the Current Programmed APS

The time devoted to programming and readout of each pixel is constrained by the size of the flat-panel imager as well as the mode in which the imager is supposed to work. For example, assuming column parallel readout, a typical array comprising of 1000×1000 pixels operating in real-time at 30 frames per second allows about 33 μsec for each pixel [**13**]. During the programming mode, the 3-TFT hybrid APS is modeled as a diode-connected TFT and a storage capacitor (C_S) in series with a TFT (TW) as indicated in Figure 3.2. All of the pixels in the same column add a parasitic capacitor (C_L/N) to the data line. This capacitor is associated with the gate-drain overlap capacitor of the switching TFT (TR) in each pixel and the overlap between column and row lines. The on-resistance of TR is in the range of MΩ while the data line resistance is usually about several tens of kΩ and consequently the line resistance can be neglected. All the pixels connected to the same column line introduce a parasitic capacitance to the data line. To achieve an analytical solution, the model in Figure 3.2 is simplified to a circuit consisting of a diode-connected TFT (TA), an equivalent parasitic capacitance (C_S+C_L), and a current source, as shown in Figure 3.3.

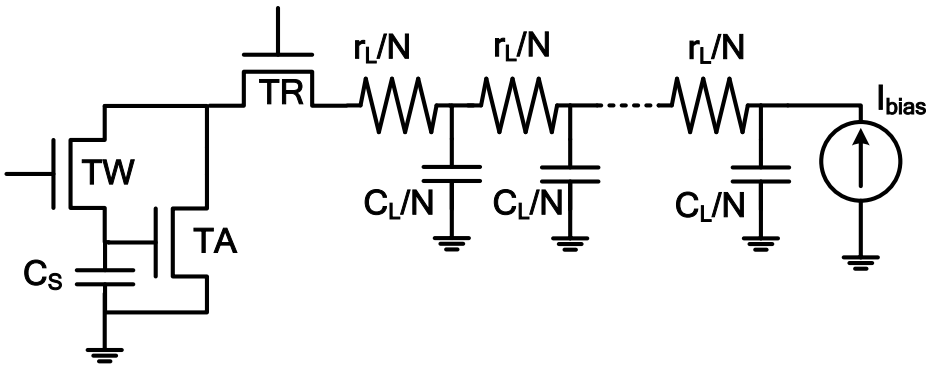


Figure 3.2 Circuit diagram for analyzing the time required to program the 3-TFT pixel circuit

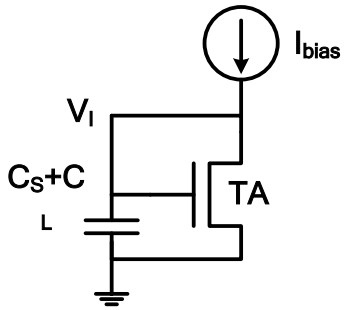


Figure 3.3 Simplified Circuit diagram for driving an analytical formula for the programming time

The relation between the current source column driver, the displacement current of the parasitic capacitor and the current of the pixel is described by the following equations:

$$I_{bias} = i_{para}(t) + i_{pix}(t) \tag{3.1}$$

where

$$i_{para}(t) = (C_S + C_L)\frac{dV_I}{dt} \tag{3.2}$$

and

$$i_{pix}(t) = \frac{1}{2}K_{TA}(V_I - V_{T_{TA}})^2 \tag{3.3}$$

Substituting (3.2) and (3.3) into (3.1) and applying boundary conditions, we obtain

$$\frac{\sqrt{2K_{TA}I_{bias}}}{(C_L+C_S)}t=\ln\frac{(\sqrt{P(t)}+1)\sqrt{P(0)}-1)}{(\sqrt{P(t)}-1)\sqrt{P(0)}+1)} \tag{3.4}$$

where *P(t)* is given by [**22**]

$$P(t)=\frac{i_{pix}(t)}{I_{bias}} \tag{3.5}$$

The parameter *P(t)* indicates how close $i_{pix}(t)$ is to I_{bias} at the time *t* during programming mode. Ideally, $P\rightarrow 1$ for successful current programming. Eq. (3.4) shows that for increasing the programming speed, K_{TA} and I_{bias} should be large while (C_L+C_S) should be made as small as possible. By assuming that at the beginning of the programming cycle, the reset line is precharged to the threshold voltage of TA, the current of TA as a function of time can be expressed as

$$I_{pix}(t)=I_{bias}\left(\frac{1-exp\left(-\frac{t}{\tau}\right)}{1+exp\left(-\frac{t}{\tau}\right)}\right)^2 \tag{3.6}$$

Where τ can be regarded as the programming time constant and can be written as

$$\tau=\frac{C_L+C_S}{\sqrt{2\mu_{TA}\frac{c_iW_{TA}}{L_{TA}}I_{bias}}} \tag{3.7}$$

Here, c_i is the gate capacitance, W_{TA} and L_{TA} are the width and length of TA and μ_{TA} is the mobility of TA. From this formula, it is concluded that the time constant with which the current of the APS rises to the programming current is proportional to C_L+C_S and inversely proportional to the square root of the mobility of the TFTs as well as the constant off panel programming current. Therefore, to avoid long programming time, a relatively large programming current should be selected. Figure 3.4 shows the settling time versus the value of the off-panel bias current. It is shown that higher bias current magnitude results in considerable reduction in the amount of the settling time [**23**]. The dependence of the settling time on the transconductance of the amplifying TFT, TA is shown in Figure 3.5.

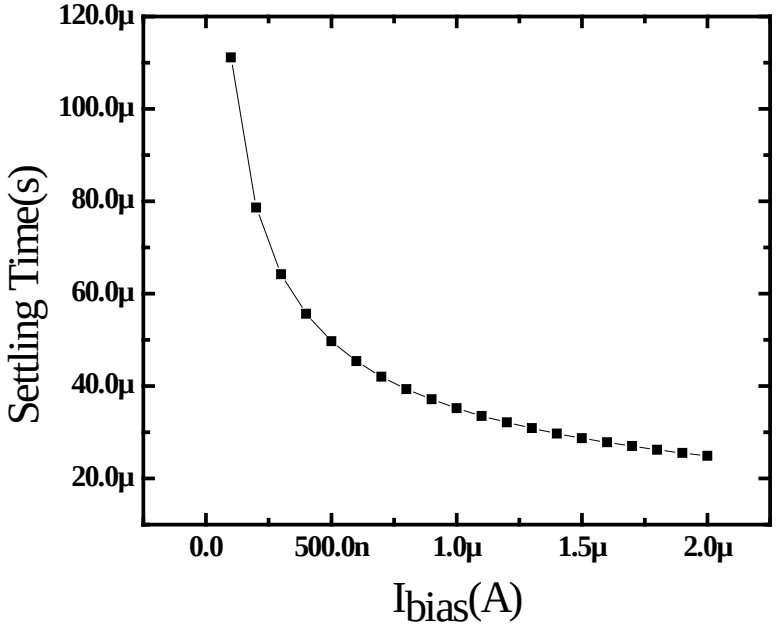


Figure 3.4 Settling time for various bias current, I_{bias}.

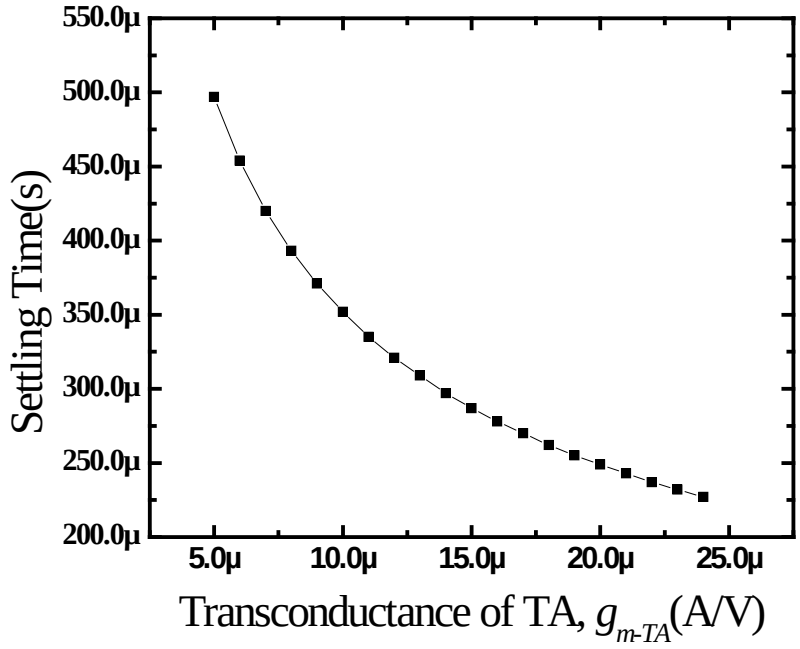


Figure 3.5 Settling time for various transconductance gain.

As a feasibility study and in order to investigate the effect of other circuit parameters on the settling time of the current programmed APS including the resistance value introduced by the

ON resistance of TR and TW in different imager modalities, the detailed model in Figure 3.2 is simplified and replaced by the circuit in Figure 3.6. The operating condition of the circuit in Figure 3.6 is derived numerically using MATLAB.

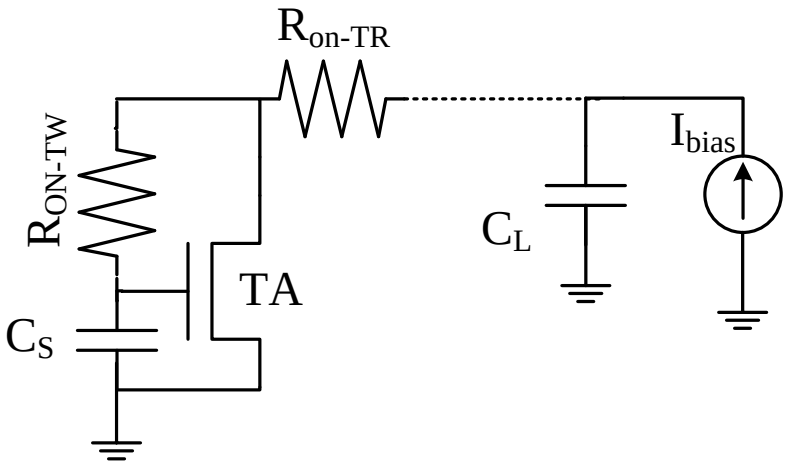


Figure 3.6 A detailed representation of the circuit in Figure 3.2 used to estimate the programming speed of the current programmed APS.

In Figure 3.6, TA is the amplifying TFT, I_{bias} is the fixed current source outside the AMFPI used to program the APS, C_S is the storage capacitor of the APS and C_L is the large capacitor associated with the data line. C_L is calculated by

$$C_L = N.C_i\,(W_{TR}L_{OV} + A_{OV}) \tag{3.8}$$

Here N is the number of rows in the active matrix flat panel imager (AMFPI) and A_{OV} is the total overlap area between the data line and gate line under each pixel. W_{TR} is the width of the switch TFT, TR, that isolates the pixel from the data line when the pixel is in the integration mode and L_{OV} is the length of the gate-drain overlap of TR. Table 3.1 shows some of the circuit and device parameters used in the simulation. The TFT parameters are chosen to be close to the typical measured values of the in-house a-Si:H TFT process. A simplified model for calculating the settling of the current in TA is given by solving the following set of differential equations:

$$I_{bias} = C_{line}\frac{dV_{line}}{d_t} + \frac{V_{line} - V_2}{R_{ON-TR}} \tag{3.10}$$

$$\frac{V_{line} - V_2}{R_{ON-TR}} - \frac{V_2 - V_1}{R_{ON-TW}} = \frac{1}{2} K_{TA}(V_1 - V_T)^2 \quad (3.11)$$

$$\frac{V_2 - V_1}{R_{ON-TW}} = C_S \frac{dV_1}{dt} \quad (3.12)$$

Table 3.1 Device and Circuit parameters used to simulate the APS transient settling in the programming mode.

Circuit parameter	Description	Common Value in the literature
μ	Field Effect Mobility	$1cm^2/Vs$
L	a-Si:H TFT channel length	5 μm
L_{OV}	Overlap capacitance between gate and drain in each switch TFT	3 μm
I_{bias}	Bias current source to program the APS circuit	1 μA-5 μA
C_S	Storage capacitor	250fF
V_{Ti}	Initial threshold voltage of the amplifying TFT	2V
V_{linei}	Initial voltage across the data line	2V

Here, TR and TW are biased in the triode mode and can be represented by R_{ON-TR} and R_{ON-TW}.

$$R_{ON-TR} = \frac{1}{K_{TR}(V_{GS-TR} - VT_{TR})} \quad (3.13)$$

$$R_{ON-TW} = \frac{1}{K_{TW}(V_{GS-TW} - \mathrm{V}T_{TW})} \quad (3.14)$$

$V_{T_{TR}}$, $V_{T_{TW}}$ and V_T are the threshold voltages of TR, TW and TA, respectively and K_{TR}, K_{TW} and K_{TA} represent the transconductance coefficients of TR, TW and TA, respectively. C_{line} is the total capacitance associated with the data line and C_S is the sum of the storage capacitance and the gate capacitance of the amplifying TFT. Here, we investigate the effect of the size of TW and TR on the programming speed. The programming speed versus $R_{ON\text{-}TR}$ and $R_{ON\text{-}TW}$ is demonstrated in Figure 3.7. The bias current value is set to be 2μA. From the result in Figure 3.7, it is obvious that the effect of changing $R_{ON\text{-}TR}$ is far more significant than that of $R_{ON\text{-}TW}$.

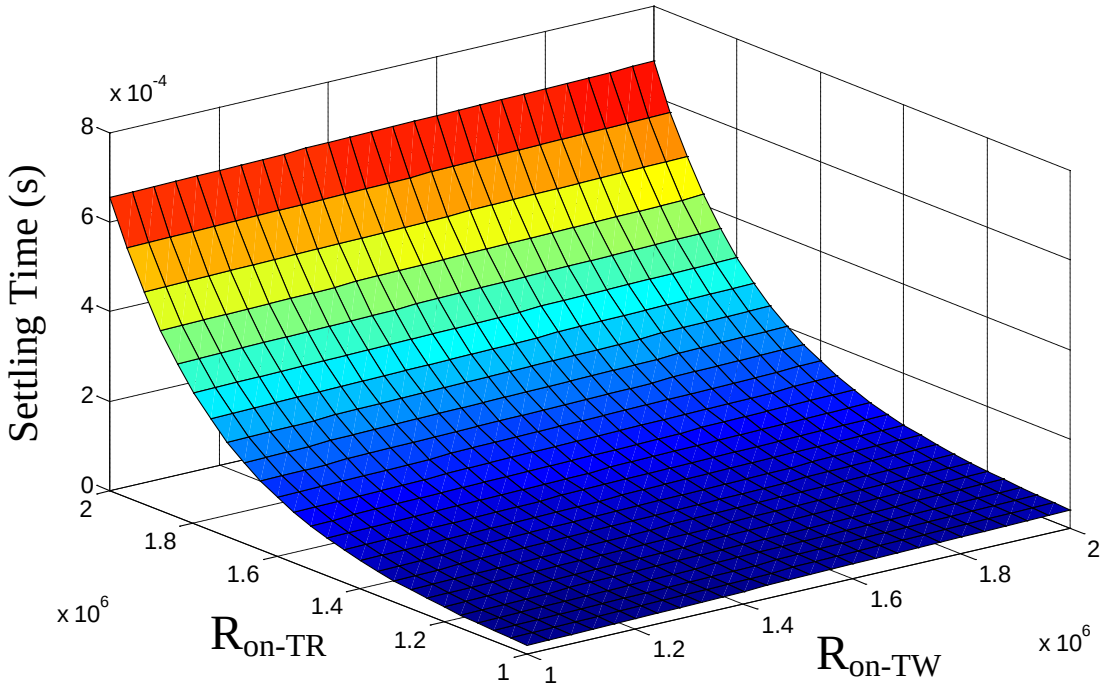


Figure 3.7 Programming speed for different values in the resistance of $R_{on\text{-}TR}$ and $R_{on\text{-}TW}$.

Figure 3.8 shows the effect of changing the ON resistance value of TR and the transconductance of TA of the programming speed. As seen previously, the programming speed is higher for lower value of $R_{ON\text{-}TR}$. On the other hand, the programming gets faster for higher transconductance of TA, $g_{m\text{-}TA}$. However, the size of TA is limited by the area of the pixel.

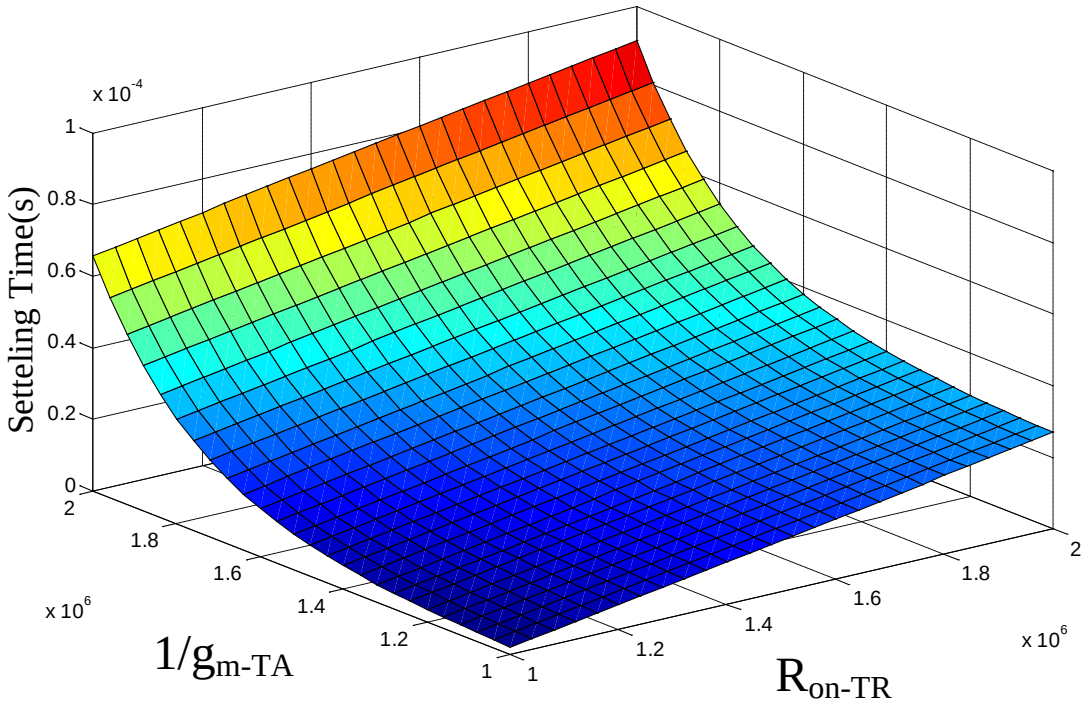


Figure 3.8 Programming speed for different values in the resistance of $R_{on\text{-}TR}$ and $g_{m\text{-}TA}$.

3.4 Increasing the Settling Time of the Current Programmed APS

High resolution real time imaging applications such as fluoroscopy require fast reset and readout of each row. In real time video applications, the entire frame has to be read out and refreshed with the frequency of 30 Hz. Assuming the array has 1000 rows, the time devoted to each row is about 33 µs. Results presented here show that the conventional current programmed scheme fails to satisfy this timing constraint. Therefore, despite the fact that current programmed APS shows immunity to threshold voltage shift caused by voltage or temperature stress, it cannot be used in medical imaging modalities that require fast operation of the pixel sensor. This problem is less severe in polysilicon technology due to high mobility of polysilicon TFTs. To mitigate this problem, various solutions are proposed. These schemes are categorized as current scaling, current offset, and precharging.

3.4.1 Scaling the Current during Readout versus the Current during Reset

As shown by Eq (3.7) and demonstrated in Figure 3.5, the greater the magnitude of the current bias, I_{bias}, is, the smaller the value of the settling time. On the other hand, unlimited increase in the magnitude of I_{bias} results is direct increase in power consumption and rise in the array temperature. Also, raising the value of the bias current source increases the voltage drop across the switch TFT resistors and therefore the voltage of the data line. This voltage cannot exceed the maximum tolerable value of the external bias current source. One solution to reduce the total power consumption of the array is to use a large current value during programming and then scale this value down during readout. With this scheme, it should be possible to increase the current during reset to reduce the settling time. One method of scaling is to use a current mirror under each pixel. In this method the scaling parameter is the ratio of the bias current to the readout current and it is almost equal to the ratio of the two transistors in the current mirror circuit. Current scaling can also be implemented in the nonmirrored scheme in which the amplifying TFT is biased in saturation during reset and the bias is shifted to the linear region during readout. The detail of the implementation of a circuit with this characteristic is given in the following sections. Figure 3.9 demonstrates the reduction in the settling time versus scaling parameter. It should be noted that increasing the scaling parameter results in increasing the voltage of the data line and this value should not exceed the operating range of the off-panel current source.

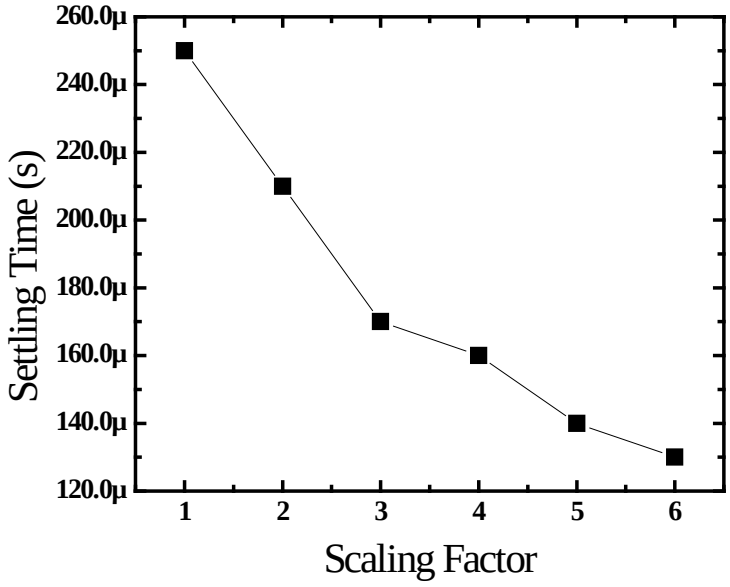


Figure 3.9 Settling Time as a function of the scaling factor

3.4.2 Offsetting the Current during Readout versus the Current during Reset

As discussed previously, for improving the settling and reducing the power consumption, it is required to have a large reset current and a small readout current. Another method to achieve this is to subtract a constant value from the programming current inside the APS pixel. The pixel circuit in Figure 3.10 is capable of the subtraction process. An extra metal line gives access to the bottom electrode of the storage capacitor. The reduction in the settling time versus offset current is shown in Figure 3.11. It is evident that with this method, we can achieve settling time values less than 40 µs. A drawback of this scheme is that the readout current is dependent on the absolute values of the amplifying TFT parameters making the method vulnerable to fixed pattern noise.

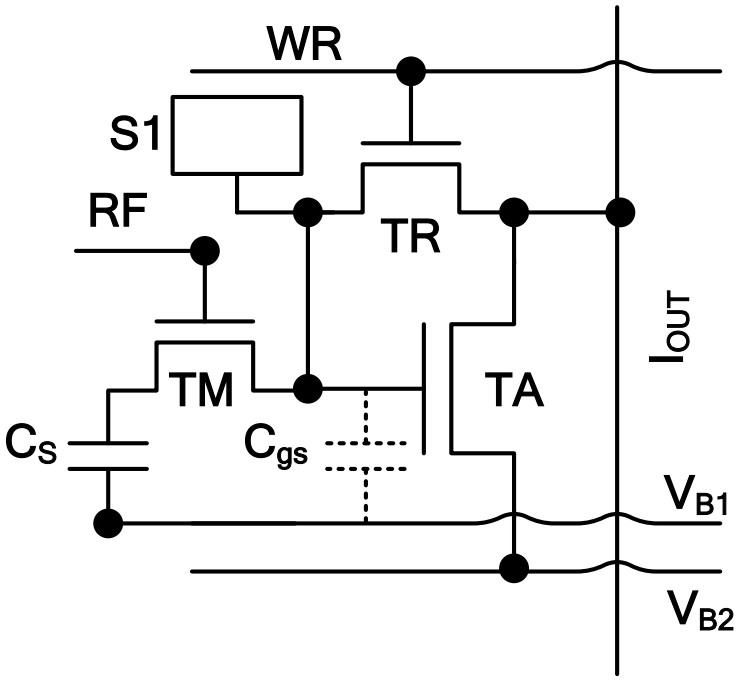


Figure 3.10 The APS pixel circuit with current subtraction capability

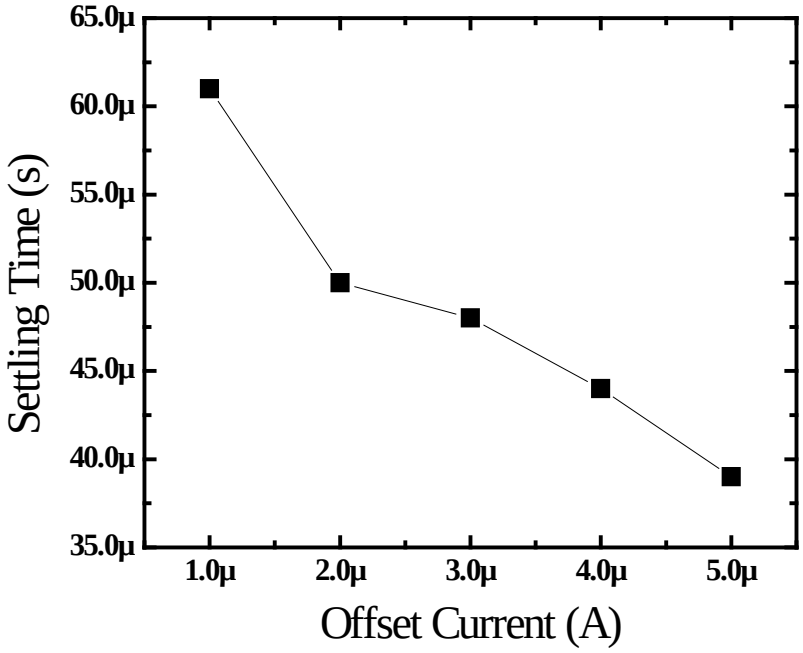


Figure 3.11 Settling Time as a function of offset current

3.4.3 Precharging the Reset line

Another method of increasing the settling time is Precharging the data line to the appropriate voltage value. Assuming the initial voltage across the data line is zero, for every value of the bias current, the voltage of the data line approaches the final steady state value of

$$V_{line} = I_{bias} \times R_{ON-TR} + V_{GS-TA} \tag{3.15}$$

Where

$$V_{GS-TA} = V_{T_{TA}} + \sqrt{\frac{2 \times I_{bias}}{K_{TA}}} \tag{3.16}$$

Here we have assumed square law relation for the transfer function of the TFT. In the Precharging method, before the Reset cycle, a voltage close to the final value associated with the bias current is applied across the data line. Figures 3.12 and 3.13 show the settling time versus the precharge voltage for several different bias currents. It is seen that by properly choosing the precharge voltage according to the specific bias current, settling time values less than 10μs can be achieved making the method acceptable for high resolution, real-time imaging. In the Precharging method, no modification is needed in the design of the APS circuit. Therefore, the method can be used in all of the current programmed APS circuits. The column bias current source needs to have the precharging capability. However, since for all the pixel circuits in the array, a fixed value for the bias current is used, there is no need for the value of the precharge voltage to be changed for each column making the implementation of the scheme easier. Due to the voltage stress across the gate-source of each amplifying TFT, the threshold voltage increases over time. Therefore, in order to have a successful precharging method, the amount of the precharge voltage has to be increased accordingly. To mitigate this problem, the voltage of the data line can be measured dynamically during the operation of the array. The measuring process can be done every couple of hours and the measured value can be used to update the precharging voltage amount during that time span [**23**].

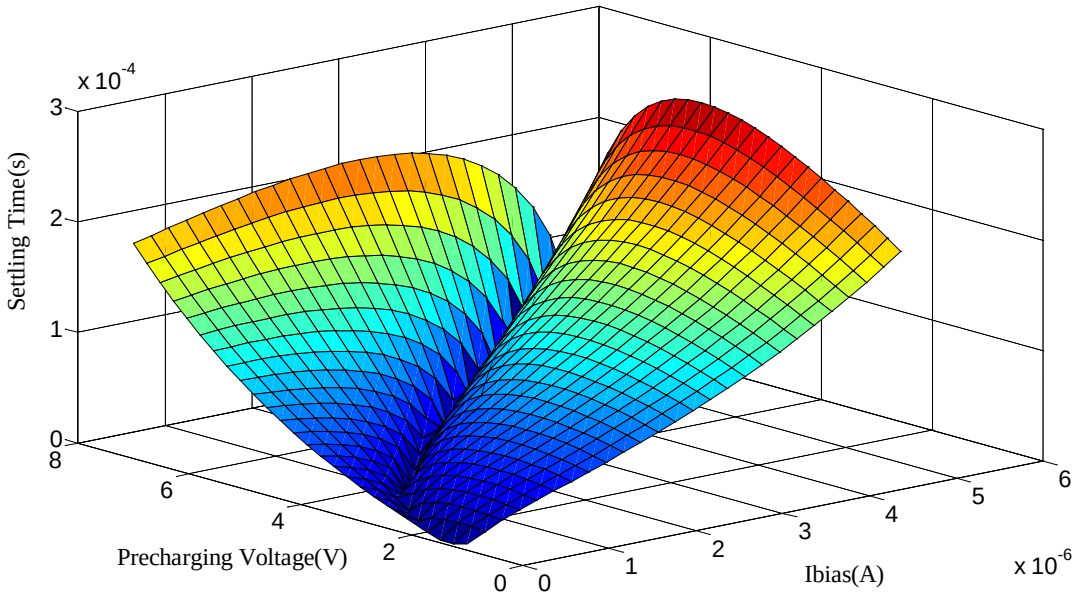


Figure 3.12 Reduction in the settling time as a function of Precharge Voltage and the bias current, Ibias.

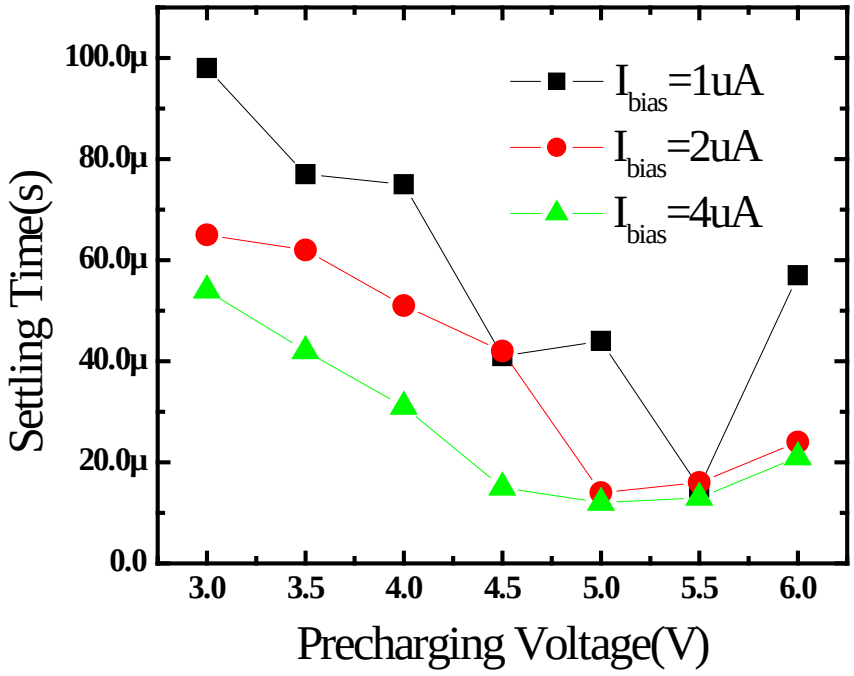


Figure 3.13 Reduction in the settling time as a function of Precharge Voltage

In the following sections of this chapter, several realizations of the current programmed, current output APS along with measurement and simulation data associated with their operation are presented.

3.5 3-TFT Current Programmed Hybrid Active-Passive Pixel for Medical X-ray Imaging

In this section, a hybrid 3-TFT current programmed, current output active pixel sensor suitable for real-time x-ray imaging is presented. The pixel circuit extends the application of a-Si:H TFT from conventional switching element to ON-pixel amplifier for enhanced signal-to-noise ratio and higher imager dynamic range. The capability of operation in both passive and active modes as well as being able to compensate for inherent instabilities of the TFTs makes the architecture a good candidate for x-ray imaging modalities with a wide range of incoming x-ray intensities.

3.5.1 Operation of the 3-TFT Current Programmed Hybrid APS

The pixel circuit presented in Figure 3.14(a) contains three TFTs (TA, TR and TW) coupled to the x-ray sensor [**24**]. Using the pixel circuit in the active mode, TA is the amplifying TFT while TR and TW act as switches. Following the timing diagram displayed in Figure 3.14(b), the pixel circuit operation can be described as follows. During the programming mode (P), S1 is connected and the SELECT and READ control line signals turn ON the switching TFTs TR and TW. Consequently the pixel is selected and when the steady state is reached in this mode, the entire constant bias current I_{bias} passes through the TFTs, TR and TA. The current flowing through TW approaches zero and the diode-connected TFT, TA, will be biased in the saturation region

$$I_{bias} = \frac{K_{TA}}{2}\left(V_I - V_{B2} - V_{T_{TA}}\right)^2 \tag{3.17}$$

Here, K_{TA}, V_I and $V_{T_{TA}}$ are the gain parameter, gate voltage and the threshold voltage of TA, respectively. After programming, both TR and TW are turned off. The storage capacitor C_S holds

the previously established voltage value on the integration node (I). During the integration mode, the photo-carriers caused by incident x-ray photons change the voltage at node I by ΔV_I

$$\Delta V_I = \frac{qN_h}{C_S} \tag{3.18}$$

where N_h is the total number of holes accumulated on C_S. In the readout mode, S2 connects the output of the pixel (I_{OUT}) to the off panel CMOS amplifier (AMP). The output current change of the common-source structure incorporating TA and TR as a result of charge integration across Cs is approximately equal to

$$\Delta I_{out} = g_{m-TA} \times \Delta V_I, \; g_{m-TA} = 2\sqrt{K_{TA} I_{bias}} \tag{3.19}$$

Here, $g_{m\text{-}TA}$ is the transconductance of TA. For exposure ranges in fluoroscopy, the corresponding small signal voltage, ΔV_I, is much smaller than $2(V_I\text{-}V_{T_{TA}})$ and therefore usage of small signal model is justified.

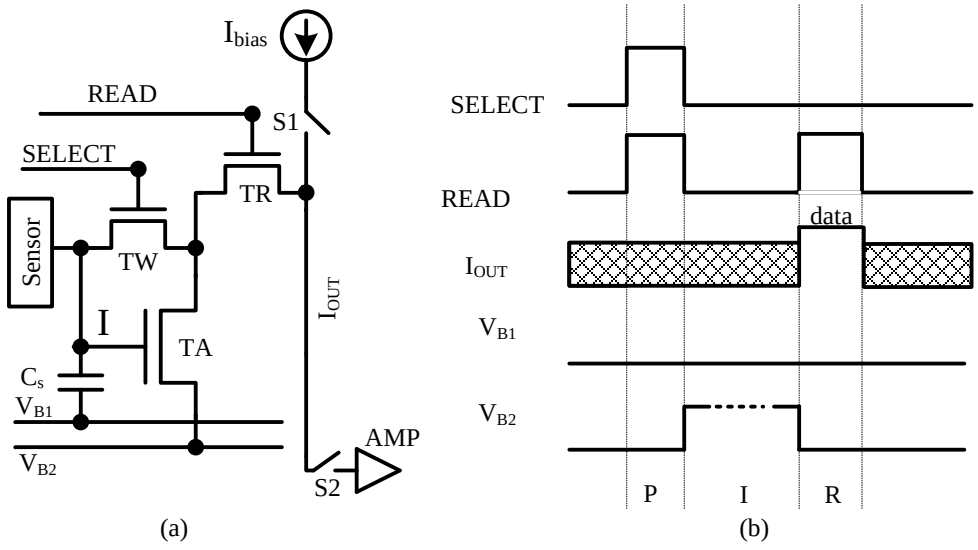


Figure 3.14 (a) Schematic diagram of the current programmed pixel circuit in the active mode and (b) the corresponding programming waveforms.

Figure 3.15(a) demonstrates the configuration of the pixel circuit in passive mode. By disabling TA, the circuit resembles that of a PPS structure to be used in high intensity modalities such as digital radiography [**13**]. In this mode, voltage levels that turn off TA are applied through V_{B1}

and V_{B2} (Figure 3.15(b)). If the readout operation is carried out through a low input impedance amplifier, the readout charge of the storage capacitor developed during integration and the reset of this capacitor are achieved simultaneously.

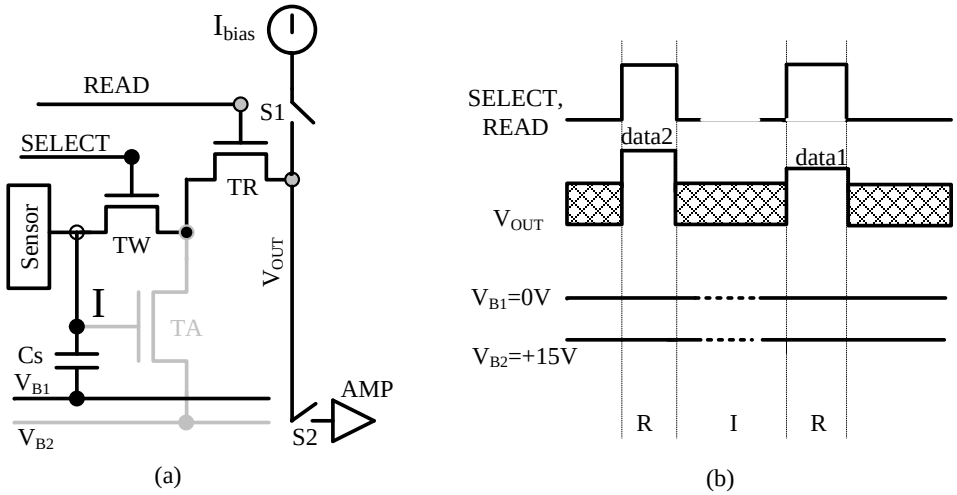


Figure 3.15 (a) Schematic diagram of the pixel circuit in the passive mode and (b) the corresponding programming waveforms.

3.5.2 3-TFT APS Pixel Fabrication

Prototypes of the pixel circuit were fabricated at the University of Waterloo using an in-house fully wet-etched 260^{o}C inverted-staggered amorphous silicon TFT process [**25**]. Plasma enhanced chemical vapor deposition (PECVD) is used for deposition of a-SiN (300nm thick), a-Si:H (70 nm thick), and passivation layers at a temperature of 300 $^{\circ}$C. Figure 3.16 shows a photomicrograph of a fabricated pixel circuit. The TFT pixel circuit, the transresistance amplifier and auxiliary circuitry was assembled on a printed circuit board. Discrete capacitors were used to emulate the effect of parasitic capacitance of the lines to obtain the transient response of the pixel circuit. The (W/L) of TA, TR and TW are 1000 µm/23 µm, 200 µm/23 µm and 50 µm/23 µm, respectively. The size of the storage capacitor is 2 pF.

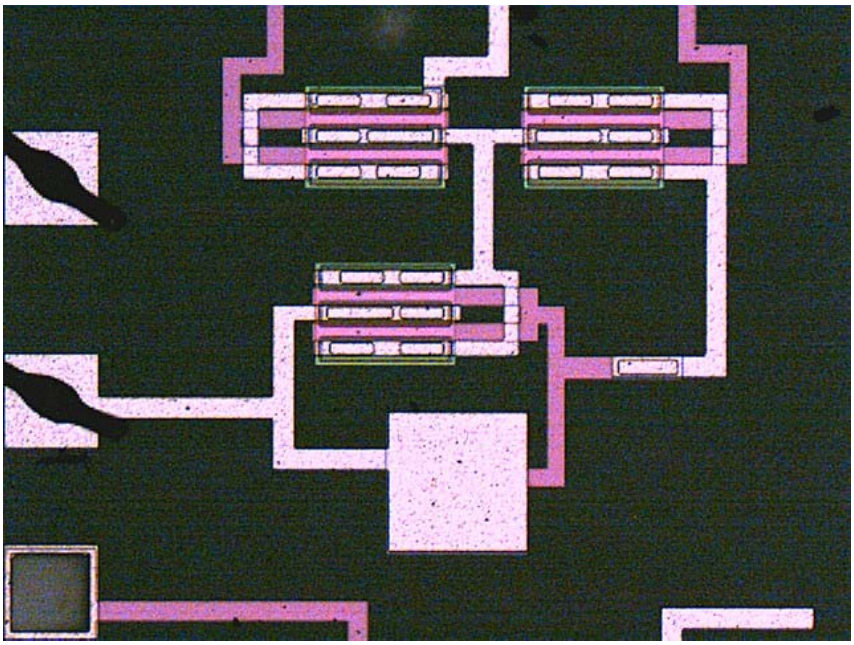


Figure 3.16 Micrograph of a fabricated APS pixel circuit with a-Si:H TFTs

3.5.3 3-TFTAPS Pixel lifetime

To investigate the stability of the proposed pixel circuit and the influence of the threshold voltage shift of TFTs on the output current, we conducted a lifetime test for more than 180 hours at room temperature. The same experiment was conducted on the previously reported 3-TFT APS pixel circuit [**26**]. The hybrid pixel circuit was driven by a 1.5 µA current pulse with timing characteristics similar to that expected in real-time fluoroscopic imaging (i.e 33 µs readout time, 33 ms integration time). Figure 3.17 shows the measured current samples of TA during readout mode as a function of stress time. The measurement result shows higher degree of stability in the output current of the 3-TFT hybrid APS compared to that of the previously reported 3-TFT APS pixel circuit [**27**]. To emulate the x-ray sensor, a voltage source with amplitude varying from 10 mV to 1 V is connected to the integration node (I) through capacitive coupling. Figure 3.18 demonstrates successful compensation for threshold voltage shift of TA for a programming current of 8.5 µA. The voltage gain is shown in the inset of Figure 3.18, confirming that the pixel circuit maintains a constant gain across a wide dynamic range of input signals.

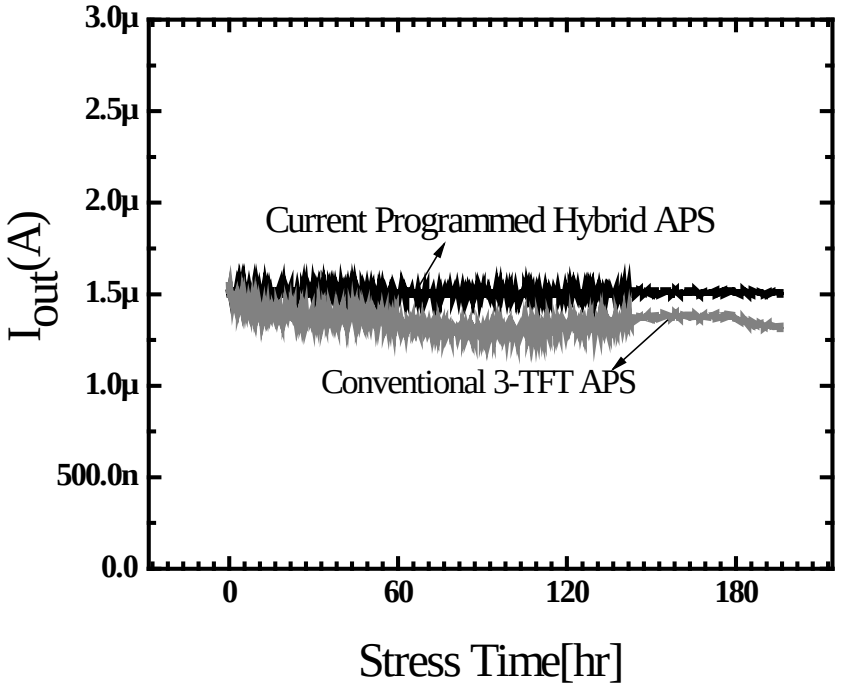


Figure 3.17 Output Current of the 3-TFT Current Programmed Hybrid APS and the standard APS architecture output current as a function of stress time at room temperature.

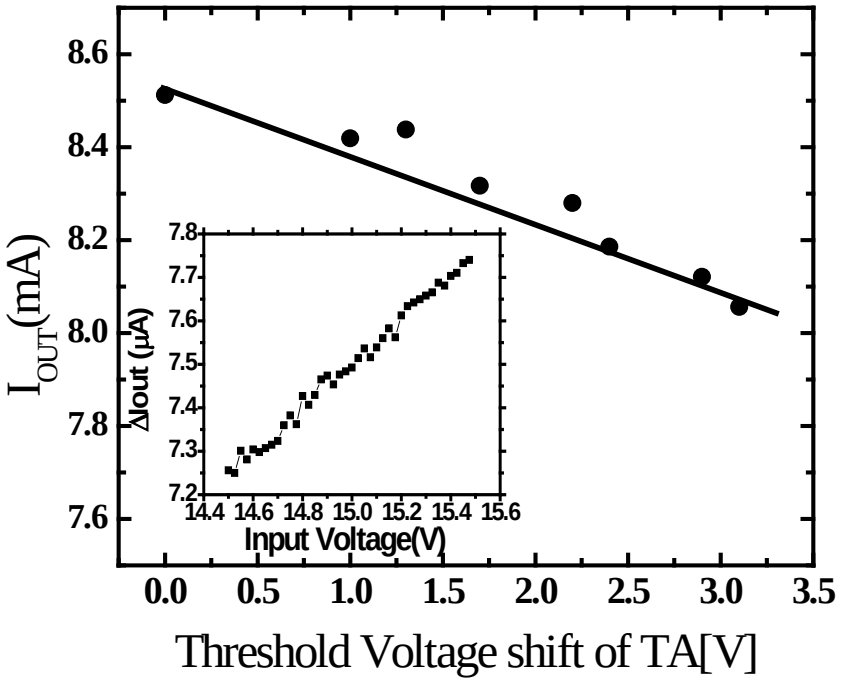


Figure 3.18 Measured output current as a function of TA threshold voltage shift; the dynamic range is shown in the insert.

3.5.4 Charge Injection and Clock feed-through Induced Errors

Since the current programming scheme is used, ideally the value of the output current during readout is independent of the parameters of the TFT TA and of linearity and hysteresis of the storage capacitance C_S. In principle, the current is modulated only by the integration node voltage change induced by the impinging x-ray radiation during integration. However, dynamic effects such as charge injection, clock feed-through, and variation of the drain-source voltage of TA in different modes of operation cause an error in the final value of the readout current. These effects are not only responsible for gain and offset errors in the pixel circuits, but also lead to dependence of the pixel characteristics on the threshold voltage shift. The latter is more critical because it is time dependent and cannot be completely compensated by external calibration. The error in the current of TA from programming to readout mode is caused by the change in the V_{GS} of TA, induced by charge injection and charge feed-through of different TFTs, and a change in the V_{DS} of TA caused by channel-length modulation. The values of induced errors in the voltages are small compared to the absolute values and, consequently using small-signal models is justified. The error in the output current can be expressed as [**28**]

$$I_{error} = g_m \Delta V_{GS} + g_{ds} \Delta V_{DS} \tag{3.20}$$

Here I_{error} is the output current error by virtue of variations in the V_{GS} and V_{DS} (ΔV_{GS} and ΔV_{DS}), g_m and g_{ds} are $\partial I_{DS}/\partial V_{GS}$ and $\partial I_{DS}/\partial V_{DS}$, respectively. The threshold voltage of TR and TW can be assumed to be relatively unchanged since they are turned off during most of the operation time. The dependence of I_{error} on the threshold voltage shift of TA, ΔV_{T_A}, can be estimated with [**28**]

$$\Delta I_{error} = \frac{\partial I_{error}}{\partial V_{T_A}} \Delta V_{T_A} = g_m \frac{\partial \Delta V_{GS}}{\partial V_{T_A}} \Delta V_{T_A} + g_{ds} \frac{\partial \Delta V_{DS}}{\partial V_{T_A}} \Delta V_{T_A} \tag{3.21}$$

Three major effects contribute to ΔV_{GS}:

1. Charge injection of TW: In the programming mode, the accumulated charge under the channel of TW is

$$Q_{ch} = C_{GSW}(V_{SELH} - V_I - V_{T_W}) \tag{3.22}$$

where V_{SELH} is the high voltage of the SELECT control signal, V_I is defined in (2), V_{T_W} is the threshold voltage of TW, and C_{GSW} is the channel capacitance of TW. Entering from programming mode to integration mode, half of this charge will be injected to the total capacitance in the integration node $C_{ST}=C_S+C_{GSA}$, provided that the falling rate is relatively high [**29**]. Therefore, the voltage error contributed by this factor is

$$\Delta V_{GS1} = -\frac{C_{GSW}(V_{SELH} - V_I - V_{T_W})}{2 \times C_{ST}} \tag{3.23}$$

2. Charge feed-through of TW: The gate-source overlap capacitor of TW (C_{OVW}) along with the total gate capacitor of TA (C_{ST}) constitutes a capacitive voltage divider. When TW is turned off at the end of programming mode, it will induce a voltage error in the amount of

$$\Delta V_{GS2} = -\frac{C_{OVW}}{C_{ST}}(V_{SELH} - V_{SELL}) \tag{3.24}$$

in which V_{SELL} is the value of the SELECT control signal during integration mode. Here we have assumed that $C_{OVW} << C_{ST}$.

3. Charge feed-through of TA: During the programming mode, the gate and drain of TA are connected through the ON resistance of TW. At the end of this mode the current flowing through TW is negligible and the drain voltage of TA (V_{DSA}) is equal to V_I. In the readout mode, the drain voltage of TA changes to

$$V_{DSA}(t_R) = V_{DD} - I_{out}(t_R) \times r_{oR} \tag{3.25}$$

The resulting change in the gate-source of TA can be approximated as

$$\Delta V_{GS3} = \frac{C_{OVAMP}}{C_{ST}}(V_{DD} - I_{out}(t_R) \times r_{oR} - V_I) \tag{3.26}$$

where r_{oR} is the ON resistance of TR and $I_{OUT}(t_R)$ is the pixel current during readout. The total error in the V_{GS} of TA is the superposition of the aforementioned factors

$$\Delta V_{GS} = \Delta V_{GS1} + \Delta V_{GS2} + \Delta V_{GS3} \tag{3.27}$$

Because of channel length modulation and high drain and source contact resistances of TA, the change in V_{DS} appears as another source of error in the output pixel current. The variation in V_{DS} of TA from integration mode to readout mode is

$$\Delta V_{DS} = V_{DD} - I_{out}(t_R) \times r_{oR} - V_I \tag{3.28}$$

Substituting equation (3.27) in (3.21) and assuming that $I_{out}(t_R)$ is independent of V_{T_A}, ΔI_{error} can be written as

$$\Delta I_{error} = (g_{mA} \frac{C_{GSW} - C_{OVA}}{C_{ST}} - g_{oA}) \times \Delta V_{T_A} \tag{3.29}$$

The above equation shows the dependence of the output current error induced by charge injection, charge feed-through and channel length modulation on the threshold voltage shift of TA. Here, TA causes a time-dependent error as its threshold voltage shifts over time. Usually the size of the amplifying TFT, TA, is chosen to be larger than the size of the switch TFT, TW. Figure 3.19 shows the effect of ΔV_{T_A} for two different sizes of TA, W_{TA}=100,150μm. It is evident that the rate of increase in the time dependent error can be minimized by carefully choosing the overlap, channel and storage capacitances as well as the transconductance and output resistance of TA and TW.

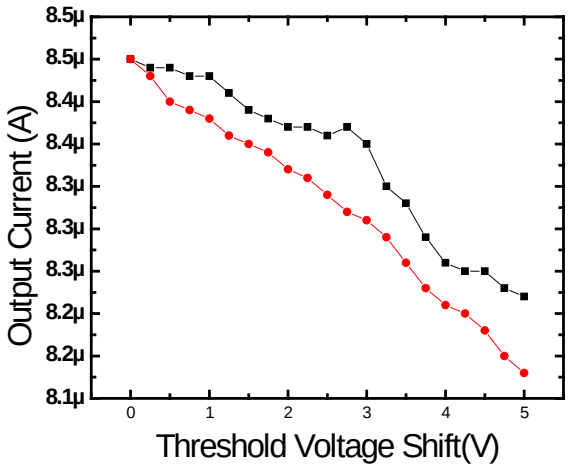


Figure 3.19 Error in the output of the APS for two different sizes of W_{TA}

3.5.5 Settling Time of the 3-TFT APS

Figure 3.20 shows the measured settling time as a function of the precharge voltage. It is readily seen that if the line is precharged properly, the settling time is substantially reduced. However, the external bias current column driver circuit should have precharging capability making its design more complicated. As the V_T of TA shifts, the required precharge voltage increases. As a result, the performance of the precharging degrades over time, if the lines are precharged with constant voltages.

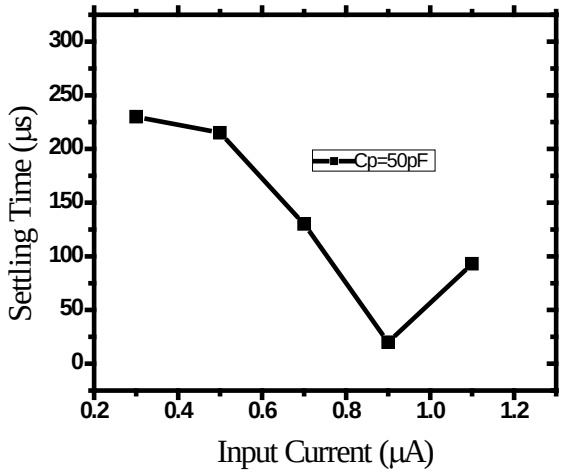


Figure 3.20 Measured settling time for current programmed pixel circuit for 8-V initial voltage

During the readout mode, the low impedance input terminal of the current amplifier minimizes the effect of the large line capacitance, thus making fast signal readout feasible. Figure 3.21 shows the measured output voltage transient response to a current pulse input with an amplitude of 1 μA for the hybrid APS. As evident, the output voltage of the transresistance amplifier settles to its final value in less than 12 μs.

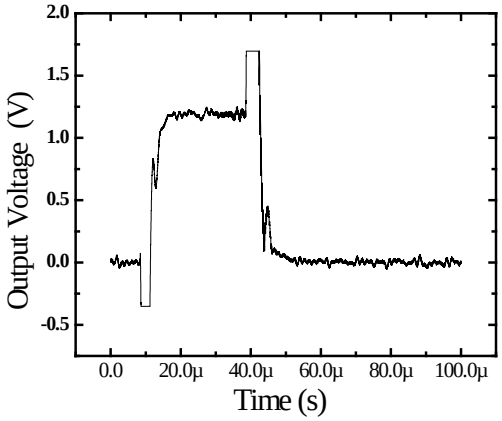


Figure 3.21 Measured Transient output response of the transresistance amplifier to a 1μA input current pulse.

3.5.6 Noise Performance of the 3-TFT APS

Analyzing the noise performance of flat panel imagers is crucial in understanding performance limitations of the system. A variety of factors determine the noise performance of an imaging system including quantum noise, i.e. the fluctuations in the number of x-ray quanta, and additive electronic noise, which is defined as the system noise in the absence of radiation. The total additive noise consists of several uncorrelated noise components such as photoconductor shot noise, transistor leakage noise, circuit thermal noise, circuit flicker noise, data line noise, off-panel amplifier noise and ADC digitization noise. Here, we limit our analysis only to those noise sources associated with the photoconductor and TFTs comprising the pixel amplifier, namely the reset noise, and the TA and TR flicker and thermal noise components. The input referred noise from external noise sources, including the data line thermal noise and the charge amplifier noise are assumed to be sufficiently attenuated by the gain of the hybrid APS such that they can be neglected. The flicker and thermal noise sources induce error on the operation of the pixel circuit during programming and readout modes. We can categorize the noise sources into two different

kinds: (i) direct noise, which occurs when there is a current in the output line. This noise is generated by the TFT noise sources of the pixel circuit and is present in the readout mode and (ii) sampled noise, which is due to the storage of the instantaneous value of the noise voltage on the storage capacitor, C_S and occurs at the end of the programming mode. In the following, we adopt a simplified analysis to derive the total noise as a function of pixel circuit parameters.

3.5.6.1 Noise during Readout

During readout, the hybrid 3-TFT pixel circuit of Figure 3.14(a) reduces to a common source amplifier stage. Including the uncorrelated noise sources of the TFTs, Figure 3.22 illustrates the small-signal model used to determine the noise of the pixel circuit. Here, C_S is the sum of capacitances between the detector node and ground. After reaching steady state, the amplifying

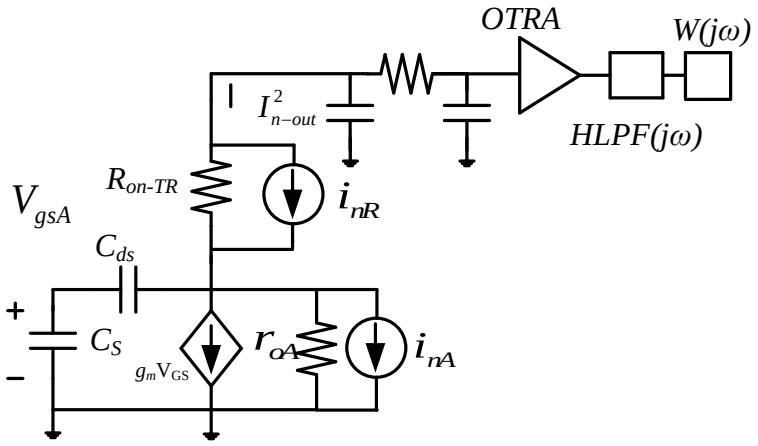


Figure 3.22 Small signal equivalent circuit for noise measurement during readout

TFT, TA, operates in saturation while TR operates in the linear mode. Therefore, we can represent TR by its ON resistance $r_{oR} = (1/g_{oR})$ which can be approximated as $r_{oR} = dI_{DS(lin)}/dV_{DS} \sim [K_R(V_{GSR}-V_{T_R})]^{-1}$. In Figure 3.22, i_{nA} represents the noise current from TA while i_{nR} represents the noise current from TR.

Conducting a nodal analysis in the frequency domain ($s = j\omega$) of the equivalent circuit of Figure 3.22, the output noise current becomes

$$I_{n-out}(s) = \frac{\mathrm{i}_{\mathrm{nA}} + \mathrm{i}_{\mathrm{nR}}}{1 + \frac{\mathrm{r}_{\mathrm{O_R}}}{r_{O_A}} + \frac{r_{O_R} g_{m_A} C_{gd_A}}{C_{gd_A} + C_{gs_A}} + s\frac{r_{O_R} C_{gd_A} C_{gs_A}}{C_{gd_A} + C_{gs_A}}}. \tag{3.30}$$

Since $\mathrm{r_{oA}}$ ($=1/\lambda \mathrm{I_{ds}}$, $\lambda=0.04$ typically for a-Si TFTs [**25**]) >> r_{O_R} we can simplify the above expression to yield,

$$I_{n-out}(j\omega) = \frac{(\mathrm{i}_{\mathrm{nA}} + \mathrm{i}_{\mathrm{nR}})/(1 + \frac{\mathrm{r}_{\mathrm{O_R}}}{r_{O_A}} + \frac{r_{oR} g_{mA} C_{gd_A}}{C_{gd_A} + C_{gs_A}})}{1 + j(\omega/\varpi_{eq})}$$

$$\varpi_{eq} = \left[\frac{C_{gd_A} + C_S + r_{O_R} g_{m_A} C_{gd_A}}{r_{o_R} C g_{d_A} C_S}\right] \tag{3.31}$$

The spectral density of the current noise, S_{Inout}, at the output may be expressed as,

$$S_{Inout} = \frac{(\mathrm{S}_{\mathrm{i}_{\mathrm{nA}}} + S_{\mathrm{i}_{\mathrm{nR}}})/(1 + \frac{\mathrm{r}_{\mathrm{O_R}}}{r_{o_A}} + \frac{r_{O_R} g_{m_A} C_{gd_A}}{C_{gd_A} + C_{gs_A}})^2}{1 + (\omega/\omega_{eq})^2} \tag{3.32}$$

Here $\omega_{eq}=2\pi f_{eq}$ represents the bandwidth of the APS circuit. The current noise power can be written as,

$$\overline{I_{nout}^2} = \int_0^\infty \frac{(\mathrm{S}_{\mathrm{i}_{\mathrm{nA}}} + S_{\mathrm{i}_{\mathrm{nR}}})/(1 + \frac{\mathrm{r}_{\mathrm{O_R}}}{r_{OA}} + \frac{r_{o_R} g_{m_A} C_{gd_A}}{C_{gd_A} + C_{gs_A}})^2}{1 + (\omega/\omega_{eq})^2} d\omega \tag{3.33}$$

In order to determine the thermal noise and flicker noise of TA and TR TFTs, we simply need to insert the appropriate noise densities and solve using numerical integration methods. The thermal noise current spectral densities for a-Si TFTs in the saturation and linear regimes are modeled respectively as

$$\overline{I_{n_A}^2} = \frac{8}{3} KT g_{mA}, \quad \overline{I_{n_A}^2} = \frac{4KT}{r_{O_R}} \tag{3.34}$$

Yielding the thermal noise current power as

$$\overline{I_{nout}^2(th)} = \frac{(feq)(\pi/2).\left(\frac{8}{3}KTg_{m_A} + \frac{4KT}{r_{O_R}}\right)}{(1+\frac{r_{O_R}}{r_{O_A}} + \frac{r_{O_R} g_{m_A} C_{gd_A}}{C_{gd_A} + C_{gs_A}})^2} \tag{3.35}$$

Here, f_{eq} is the circuit bandwidth and $(\pi/2)(f_{eq})$ is the classic noise bandwidth of a first order low pass filtering circuit. The flicker noise current spectral densities for a-Si TFTs in the saturation and linear regimes are modeled respectively using the mobility fluctuation model as [**30**], [**31**]

$$\overline{I_{nA}^2(f)} = \frac{\alpha_{sat} q \mu_{eff}^2 C_{ox} W (V_{gs} - V_T)^3}{2fL^3}$$
$$\overline{I_{nR}^2(f)} = \frac{\alpha_{triode} q \mu_{eff}^2 C_{ox} W (V_{gs} - V_T) V_{ds}^2}{fL^3} \tag{3.36}$$

Here, q is the charge of electron, f is the frequency, and α_{triode} and α_{sat} are the fitting constants, and depend on the fabrication characteristics of the TFTs. For the in-house fabricated TFTs (inverted staggered bottom gate structure), the approximated values of α_{triode} and α_{sat} are 0.02 and 0.008, respectively. The flicker noise current power is

$$\overline{I_{nout}^2(f)} = \frac{(a_{fl1} + a_{fl2})}{(1+\frac{r_{O_R}}{r_{O_A}} + \frac{r_{O_R} g_{m_A} C_{gd_A}}{C_{gd_A} + C_{gs_A}})^2} \int_{f_{OBS}=1/T_{OBS}}^{\infty} \frac{1}{f\left(1 + f^2 / f_{eq}^2\right)} df =$$
$$\frac{(a_{fl1} + a_{fl2})}{(1+\frac{r_{O_R}}{r_{O_A}} + \frac{r_{O_R} g_{m_A} C_{gd_A}}{C_{gd_A} + C_{gs_A}})^2} (1/2) \ln\left(1 + \frac{f_{eq}^2}{f_{OBS}^2}\right). \tag{3.37}$$

where T_{OBS} is the time of observation of the flicker noise and a_{fl1} and a_{fl2} are given in [**30**], [**32**]:

$$a_{fl1} = \frac{\alpha_{sat}.q.\mu_{EFF}^2.C_G.(W/L)^2}{2(W.L)}.(V_G - V_T)^3,$$
$$a_{fl2} = \frac{\alpha_{lin}.q.\mu_{EFF}^2.C_G.(W/L)^2}{(W.L)}.(V_G - V_T).V_{DS}^2. \tag{3.38}$$

The $H_{LPF}(\omega)$ and $W(\omega)$ blocks represent a low-pass filter and a double-sampling (DS) operation, respectively. The low-pass filter single pole power spectral transfer function is given by:

$$H_{LPF}^{2}(\omega) = \frac{1}{1+\omega^{2}\tau^{2}} \tag{3.39}$$

where τ is the low-pass filter time constant. The effect of the low-pass filter is to limit the bandwidth in order to reduce the thermal noise of the system, and is located after the current amplifier. The power spectral density transfer function for double sampling is given by [**33**], [**34**]

$$W^{2}(\omega) = 2\{1-\cos(\omega T_{S})\} \tag{3.40}$$

where T_s is the double sampling time (the time between the signal and reset samples). For an a-Se photoconductor, the associated dark current shot noise is given by

$$\sigma_{a-Se} = \sqrt{\frac{A_{ph} J_{a-Se,dark} T_{F}}{q}} \tag{3.41}$$

where T_F is the frame time (33 ms) and A_{ph} is the effective photoconductor area per pixel. The dark current noise density, $J_{a\text{-}se,dark}$, has been given as 1 pA/mm^2 at an electric field of 10V/μm [**35**], [**36**], though values as low as 7 fA/mm^2 have been reported for thick a-Se photoconductor layers at an electric field of 14 V/μm [**33**].

Embedding the TFTs underneath the sensor in a fully overlapped pixel architecture allows the pixel to achieve a near 100% fill factor. A small C_S in addition to a high fill factor can be achieved by using a thick, continuous layer sensor such as an a-Se photoconductor for detecting X-rays. In digital fluoroscopy (250×250μm^2 pixels), the a-Se photoconductor thickness ranges from 0.5 to 1 mm which gives C_{sensor}<10fF. Here, C_{sensor}, is the capacitance associated with the a-Se layer. The transistor current leakage noise at the detection node is due to the TW TFT, and is given by

$$\sigma_{TW,L} = \sqrt{\frac{I_{TW,L} T_{F}}{q}} \tag{3.42}$$

where $I_{TW,L}$ is the transistor leakage current of TW. Measuring the transfer function of TW, the leakage current is about 100 fA.

3.5.6.2 Noise during Programming

During programming, TW and TR operate in linear mode while TA operates in saturation. As a result, TW and TR are replaced by their ON-resistances in the small signal circuit model. Here, the circuit of Figure 3.14(a) is replaced by a small signal equivalent, shown in Figure 3.23. The noise sources are included as independent current and voltage sources in the circuit. During the programming mode, noise from both TW and TA modulate the voltage across C_S. At the end of programming mode, noise from TA, TW and TR is sampled on C_S and alters the ideal stored across C_S. Assuming that $r_{o_W} << 1/g_{m_A}$ where $r_{o_W} = dI_{DS(lin)}/dV_{DS} \sim [K_W(V_{GS_W} - V_{T_W})]^{-1}$ is the ON resistance of TW, the loop bandwidth of this equivalent circuit during programming is,

$$f_0 = g_{m_A} / 2\pi C_S \tag{3.43}$$

The voltage across C_S is related to the noise voltage of TW (V_{nW}) by

$$\frac{V_{C_S}}{V_{n_W}} = \frac{g_{o_A}/(g_{m_A} + g_{o_A})}{1 + j2\pi f \times C_S(1 + g_{o_A} r_{o_W})/(g_{m_A} + g_{o_A})} \approx \frac{g_{o_A}/g_{m_A}}{1 + jf/f_0} \tag{3.44}$$

where g_{oA} is the output conductance of TA. Therefore the power spectral density of the noise from r_{oW} contributed to the voltage of C_S is,

$$\overline{V^2_{C_S-TW}(f)} = \left|\frac{V_{C_S}}{V_{nW}}\right|^2 \overline{V^2_{nW}(f)} \approx \left[\frac{(g_o/g_m)^2}{1 + (f/f_0)^2}\right] \overline{V^2_{nW}(f)} \tag{3.45}$$

In this equation, since $g_{oA}/g_{mA} << 1$, the effect of TW noise on the voltage of storage capacitor will be highly attenuated. Similarly, the voltage across C_S is related to TA noise voltage by

$$\frac{V_{C_S}}{V_{nA}} = \frac{g_{m_A}/(g_{m_A} + g_{o_A})}{1 + j2\pi f C_S(1 + g_{o_A} r_{o_W})/(g_{m_A} + g_{o_A})} \approx \frac{1}{1 + jf/f_0} \tag{3.46}$$

Here, V_{nA} is the equivalent noise voltage of TA transferred from the drain-source current to the gate voltage. The power spectral density of noise on C_S due to TA is

$$\overline{V^2_{C_S-TA}(f)} = \left|\frac{V_{C_S}}{V_{nA}}\right|^2 \overline{V^2_{nA}(f)} \approx \left[\frac{1}{1 + (f/f_0)^2}\right] \overline{V^2_{C_S-TA}(f)} \tag{3.47}$$

Compared to the noise of TW, equations (3.44) and (3.46) indicate that the noise of TA is the dominant noise component sampled on C_S. Note that component of noise contributed by these two (TW

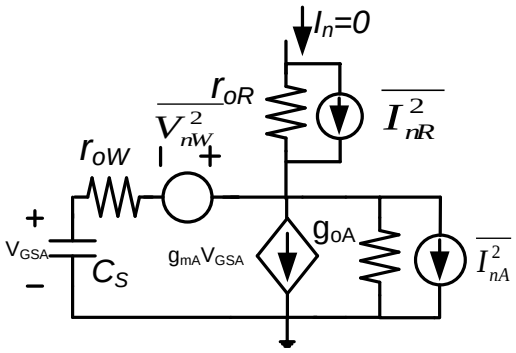
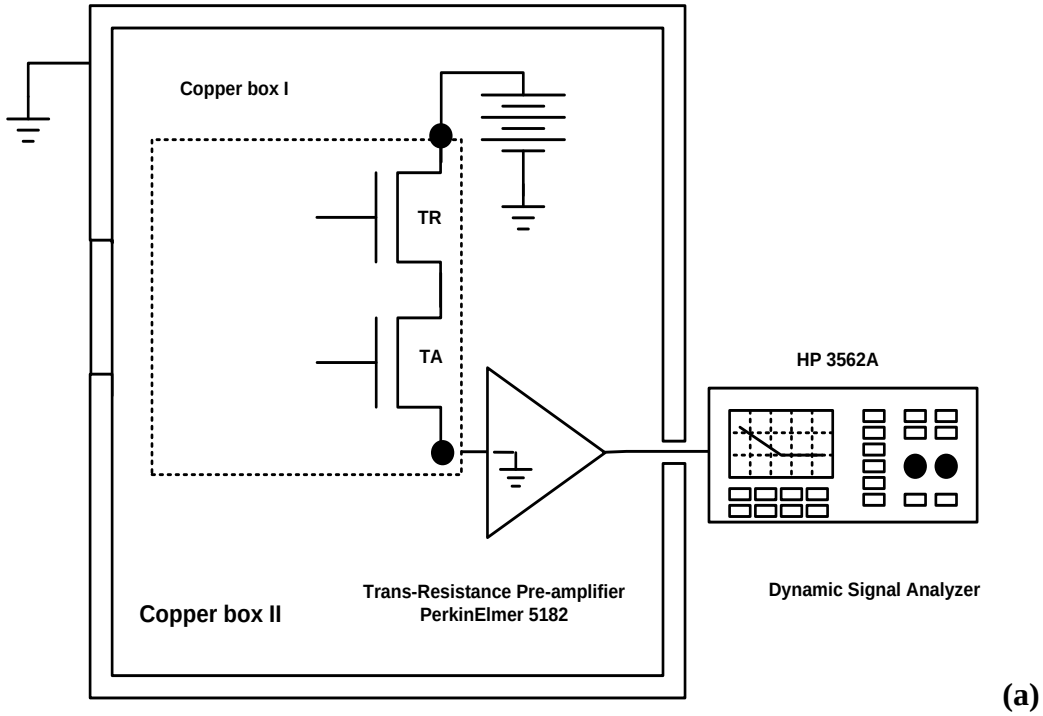


Figure 3.23 Small signal equivalent circuit for noise measurement during programming

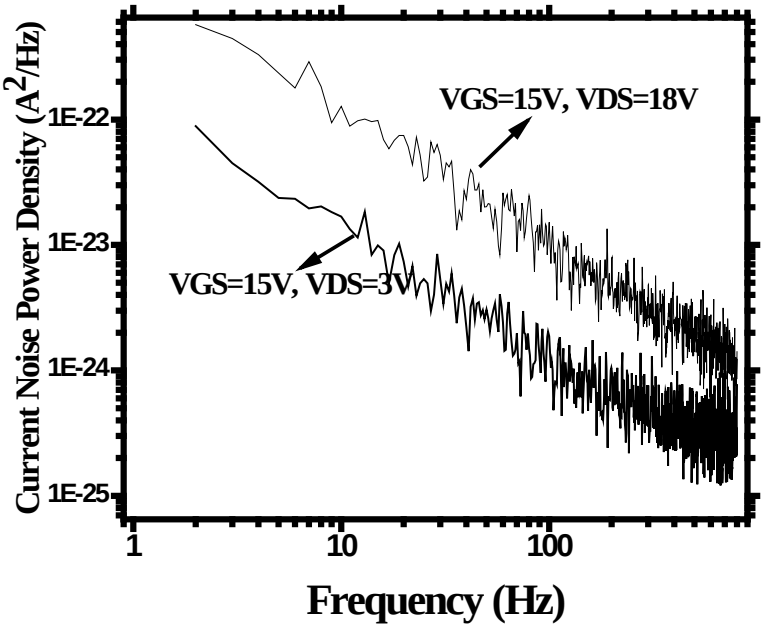
and TA) noise sources to the noise voltage on C_S are uncorrelated. Thus the two PSDs can be added to form the sampled noise PSD

$$\overline{V_{C_S}^2(f)} = \overline{V_{C_S-TW}^2(f)} + \overline{V_{C_S-TA}^2(f)} \tag{3.48}$$

Assuming that the current noise of the biasing current sources (being CMOS devices) is negligible compared to the a-Si TFT current noise value, and thus, the effect of $\overline{I_{nR}^2}$ on the noise voltage developed on C_S can be neglected. The 3-TFT APS noise measurements were carried out for the fabricated test pixel shown in Figure 3.14(a). V_{B1} and V_{B2} are provided by high amp hour DC batteries. The entire setup is put in a double-shielded copper box to reduce external noise coupling (Figure 3.24(a)). An ac-coupled Perkin-Elmer 5182 transresistance amplifier was used to amplify the noise signal. The output signal was fed to a HP 3562A spectrum analyzer to extract the power spectral density of the amplified noise signal. The SELECT line voltage was set to zero volts during this measurement. The system noise was at least one order of magnitude lower (at high frequencies) than the pixel circuit output noise and was subtracted from each measured power spectrum. For each measurement, acquisition began an hour after application of the bias voltages to allow the APS bias current and the noise to stabilize. Figure 3.24(b) shows the measured noise spectrum of the hybrid 3-TFT pixel circuit in the readout mode for a few biasing arrangements. Integrating the area under the noise curves retrieves the total RMS noise of the APS output current including the effect of TA, TR and TW.



(a)



(b)

Figure 3.24 (a) Hybrid 3-TFT Noise measurement setup and (b) Current noise PSD in A2/Hz for selected bias voltages.

The RMS output noise for different bias currents of the 3-TFT hybrid APS is shown in Figure 3.25. The lower limit of the integrations is usually determined from the frame rate of the imager. From the noise spectrum in Figure 3.24(b), it is evident that the noise of the 3-TFT APS is dominated by flicker noise of TA and TR TFTs.

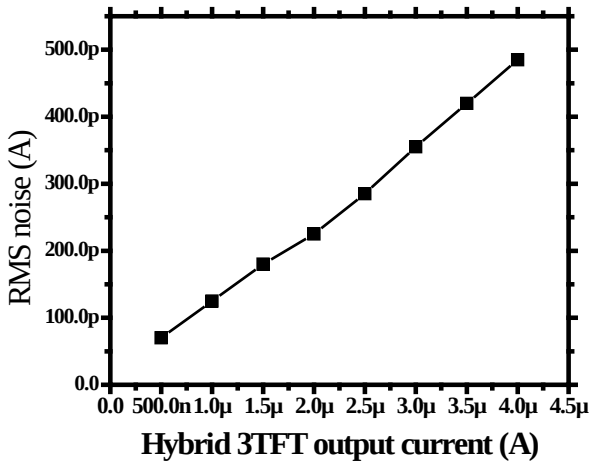


Figure 3.25 RMS noise of the 3-TFT Hybrid pixel circuit as a function of the bias current.

When the 3-TFT APS circuit is used in digital imaging, double sampling used to perform offset and gain corrections for proper operation of the 3-TFT APS, mitigates the effect of non-uniformities as well as any dc components including low-frequency flicker noise. Using the theory presented previously in this section, the results of the 3-TFT hybrid APS noise analysis with double sampling are presented in Table 3.2. It appears promising for diagnostic medical imaging (particularly for real time fluoroscopy where the minimum signal is only 1000 electrons [**12**]).

Table 3.2 Predicted Total 3-TFT hybrid APS noise (in electrons) from various noise sources. The noise results are extracted for the fabricated 3TFT APS pixel circuit using the theory presented in the paper with the measured gain and noise values.

Input referred noise (electrons)	a-Si:H TFT circuit
TA thermal noise	51
TA flicker noise	730
TR thermal noise	42
TR flicker noise	370
Data line thermal noise	20
Current Amplifier thermal noise	63
Current Amplifier flicker noise	40
a-Se dark current shot noise	67
TW leakage current shot noise	24
TW KTC noise	301
Total noise	887

3.6 Linearity of the Current Programmed APS Circuit

The linearity of the current programmed, current output APS can be defined as the variation in the output current versus the change in the input illumination

$$\gamma = \frac{dI_{OUT}}{dhv} = \frac{dQ_P}{dhv}\frac{dV_G}{dQ_P}\frac{dI_{OUT}}{dV_G} \tag{3.49}$$

where, γ defines the linearity of the APS pixel circuit integrated to the x-ray sensitive sensor. The first term defines the linearity degree of the sensor whereas the second term represents the change across the storage capacitor versus the change in the generated charge.

$$\Delta Q_P = \Delta V_G . C_{PIX} \tag{3.50}$$

This linear relation between the charge accumulated across the capacitor and its voltage is correct as long as the capacitor is not saturated and the bias dependent parasitic capacitors of the

amplifying TFT are negligible compared to the fixed storage capacitor. The last term represents the transconductance of the amplifying TFT and demonstrates the change in the output current of the TFT versus its gate voltage change. Approximating the operation of the TFT with the CMOS level 1 model, the I–V relationship can be written as,

$$I_{OUT} + \Delta I_{OUT} = K/2(V_G + \Delta V_G - V_T)^2 \tag{3.51}$$

Cancelling the bias value,

$$\Delta I_{OUT} = K(V_G - V_T)\Delta V_{G+}K/2(\Delta V_G)^2 \tag{3.52}$$

In order to get linear operation, the second term causing the first degree of nonlinearity must be minimized compared to the other one:

$$\Delta V_G \ll 2(V_G - V_T) \tag{3.53}$$

This equation defines the range of input voltages acceptable for linear operation of the APS pixel circuit. V_G is the DC bias value of the gate voltage and V_T is its threshold voltage. Thus, for linear operation, the change in voltage at the integration node due to the x-ray input (ΔV_G) must be kept small. The above equations show that the output current from the APS consists of a DC component added to an AC component that shows the x-ray induced signal. The bias current component (I_{OUT}) comes from the steady state value of the gate voltage while the signal current (ΔI_{OUT}) comes from the small signal change at the AMP TFT gate (ΔV_G).

3.7 Current Programmed APS for Dual Mode Diagnostic Digital X-ray Imaging

Dual mode current-programmed, current-output active pixel sensor (DCAPS) in amorphous silicon (a-Si:H) technology is useful in particular, for hybrid fluoroscopic and radiographic imagers. In DCAPS, each pixel includes an extra capacitor that selectively is coupled to the pixel capacitance to realize the dual mode behaviour. Previous APS circuits provide a linear response only to small-signal X-ray inputs limiting their use in multi-mode X-ray imaging modalities. For example, using an APS for real-time fluoroscopy where the exposure level is small gives a linear output. However, the voltage change at the APS input is much higher in chest radiography or

mammography due to the larger X-ray exposure levels. The larger input voltage causes the APS output to be non-linear thus requiring additional off-panel signal processing. To address this concern, dual mode pixels based on a combination of PPS and APS circuits were reported [**18**], [**17**]. However, these circuits do not provide an SNR improvement when the PPS mode is used for larger X-ray signals thus limiting potential X-ray dose reduction benefits. Here, a novel dual mode current-programmed, current-output active pixel sensor (DCAPS) circuit that provides SNR improvements across the entire range of input x-ray signal. The DCAPS is immune to V_T shift both from temperature and process variation perspectives. Measured results of stability (thermal and voltage stress) and transient response underscore the immunity of the DCAPS pixel to V_T, temperature and process variations. The transient and noise analysis of the pixel circuit show that the proposed circuit can meet the requirements of real-time X-ray imaging (fluoroscopy).

3.7.1 DCAPS Pixel Operation

Figure 3.26 shows the DCAPS schematic and the operating signals. The pixel circuit presented in Figure 3.26(a) contains three TFTs (TA, TR and TM) coupled to the x-ray sensor. TA is the amplifying TFT operating in saturation mode while TR and TM act as switches. TM is a mode varying transistor controlled by a globally controlled enable signal. For large X-ray input signals (e.g. in chest radiography), the global signal RF turns on the mode changing transistor, TM, of the pixel array, increasing the effective storage capacitance of each pixel. For small X-ray input signals (e.g. in real-time fluoroscopy), RF is switched to a negative voltage value thereby turning off TM for all the array pixels and lowering the effective pixel storage capacitance. During the integration cycle, the sensor signal is integrated on the pixel sense node capacitance (C_S) and a voltage develops which modulates the output current (I_{OUT}) during readout. Turning on transistor switch TM causes an increase in the value of C_S. For example, a typical TA channel gate capacitance is C_g = 200 fF while an additional storage capacitor (C_S) of 1.8 pF can increase the total capacitance to 2 pF, yielding a tenfold increase in the pixel dynamic range for dual mode imaging applications. Alternately, larger or smaller capacitance values can be used as dictated by the application. Following the timing diagram displayed in Figure 3.26(b), the pixel circuit operation is as follows. During the programming mode (P), the WR control line signal turns on

the switching TFT TR. Consequently the pixel is selected and when the steady state is reached in this mode, the entire constant bias current I_{bias} passes through TA. The current flowing through TR approaches zero and the diode-connected TFT, TA, is biased in the saturation region:

$$I_{bias} = \frac{K_{TA}}{2}\left(V_I - V_{B2} - V_{T_{TA}}\right)^2 \tag{3.54}$$

Here, K_{TA}, V_I and $V_{T_{TA}}$ are the gain parameter, gate voltage and the V_T of TA, respectively. After programming, both TA and TR are turned off. The storage capacitor C_S holds the previously established voltage value on the integration node, I. During X-ray signal integration, the photo-carriers generated by absorbed x-ray photons change the voltage at node I by ΔV_I

$$\Delta V_I = \frac{qN_h}{C_S} \tag{3.55}$$

where N_h is the total number of charge carriers accumulated on C_S. In the readout mode, the output of the pixel (I_{OUT}) is connected to the off panel CMOS current amplifier. The output current change (ΔI_{OUT}) of the common-source structure incorporating TA and TR is approximately equal to

$$\Delta I_{out} = g_{m-TA} \times \Delta V_I \text{ , } g_{m-TA} = 2\sqrt{K_{TA} I_{bias}} \tag{3.56}$$

where $g_{m\text{-}TA}$ is the transconductance of TA. For exposure ranges in fluoroscopy, the corresponding small signal voltage, ΔV_I, is much smaller than $2(V_I - V_{T_{TA}})$ and therefore using the small signal model is justified.

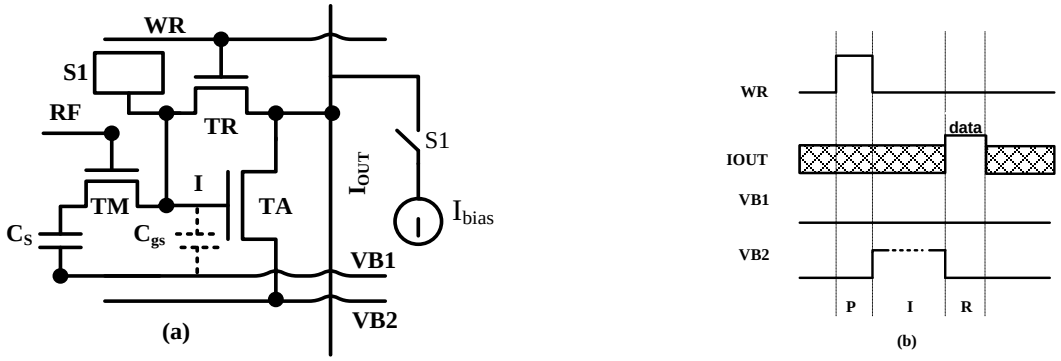


Figure 3.26 (a) DCAPS pixel circuit schematic, (b) Controlling Signals during three modes of operation.

3.7.2 Stability versus Voltage and Temperature Stress

Since a predetermined off-panel current source is used to set the gate voltage of TA during each frame, should the V_T shift, the programming current adjusts ($V_{GS} - V_T$) to force the same current in TA each time thus making the pixel transconductance gain, $g_{m\text{-}TA}$ insensitive to variations in V_T over time. The same principle applies to process or temperature variations across the array. It should be noted that I_{bias} is programmable which allows for a programmable gain to enable potentially lower X-ray doses. In addition, unlike the previously reported circuits, the DCAPS offers non-destructive readout for both low and high level input signals. Figure 3.27 shows the measured output current of the DCAPS circuit over 12 hours of operation at room temperature. The programming and output currents respectively are 9.6 μA with a timing characteristic compatible with fluoroscopy [**13**]. It is seen that ΔI_{OUT} of the DCAPS circuit is about 0.2%.

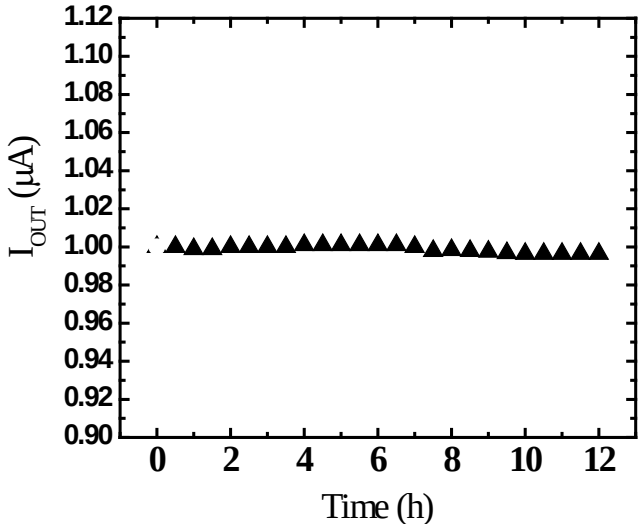


Figure 3.27 Stability of the DCAPS versus time for a pulsed DC bias stress experiment. TA is biased with -5 V and +15 V during the OFF (33 ms long) and ON (33μs long) cycles respectively.

The electrical characteristics of a-Si:H TFTs are very sensitive to the change in temperature (Figure 3.28). This sensitivity causes problems particularly when the array is used in fluoroscopy. During fluoroscopy, the array is continuously exposed to the incoming X-ray radiation. Also, the continuous switching of the TFTs, which is necessary to perform the read, integration and reset cycles, causes a large amount of dynamic power dissipation. This is in addition to the static power dissipation caused by the leakage currents in the TFTs and the X-ray

sensitive photoconductor. This power consumption, results in noticeable increase in the temperature of the active matrix flat panel imager in the fluoroscopic mode of operation. If the temperature passes a certain limit, it causes the crystallization of the a-Se sensor and consequently a considerable increase in the leakage current and reduction of the signal to noise ratio.

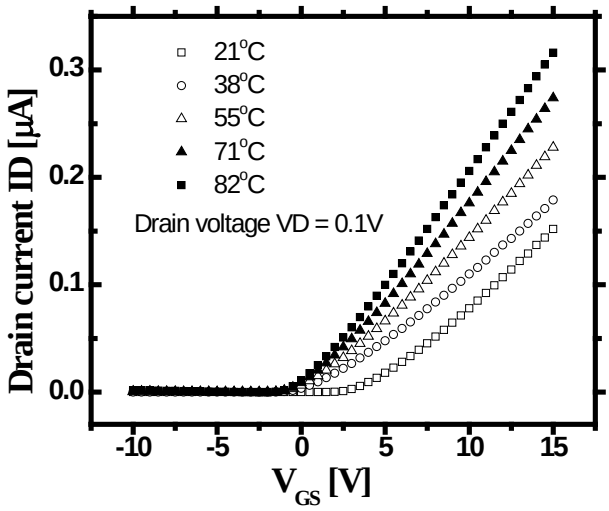


Figure 3.28 The change in the characteristics of a TFT biased in linear mode for four different temperatures.

To prevent this phenomenon from happening, cooling fans are usually used. The operation of the cooling fans causes temperature gradient across the surface of the active matrix flat panel imager. On the other hand as mentioned before, since the characteristics of the TFTs are very temperature sensitive, the output of the active pixel circuits in different locations of the array with different temperature would not be the same even if the bias voltages and the input x-ray generated charge to these pixel circuits are exactly the same. This problem demonstrates itself in the form of fixed pattern noise in the final image of the array. In Figure 3.29 the output current of a discrete TFT as a function of temperature compared to the stable output current of DCAPS is demonstrated. As can be seen, the change in temperature from 20°C to 80 °C causes a 6-fold increase in the output current of the discrete TFT while DCAPS gives a stable current with changes in temperature. Although the DCAPS suffers from array level fixed pattern noise due to feedthrough at C_S at the end of the reset cycle, difference mode sampling [**37**] can alleviate this problem.

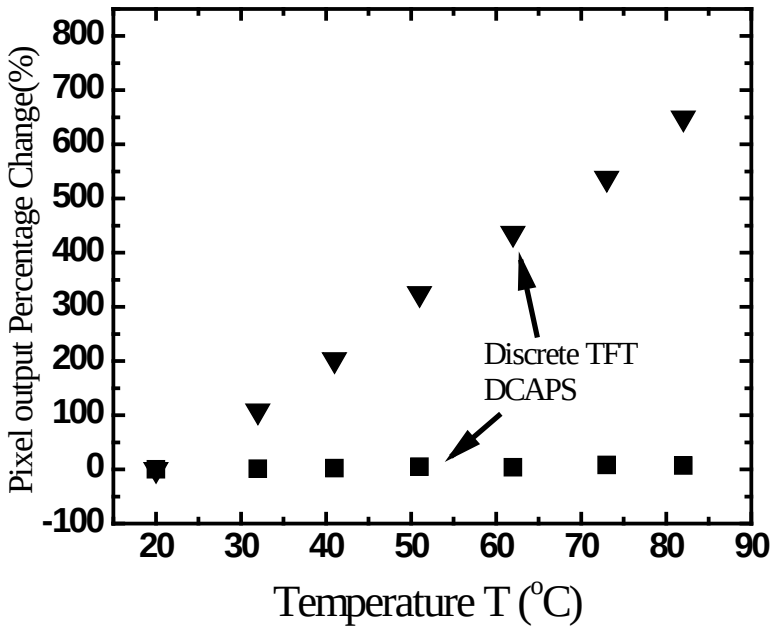


Figure 3.29 Temperature sensitivity of a Discrete TFT and the DCAPS.

3.7.3 Noise Analysis of the Multimode APS pixel circuit

Analyzing the noise performance of the DCAPS pixel is crucial in understanding performance limitations of the imager array. Here, we consider the following noise sources associated with the photoconductor, TFTs comprising the DCAPS circuit, data line and off-panel CMOS current amplifier for a direct conversion imaging system: photodetector shot noise, transistor leakage noise, reset (kTC) noise, circuit thermal noise, circuit flicker noise, data line noise, current amplifier and the current bias source noise. Figure 3.30 and 3.31 show the equivalent small signal of the APS during programming and readout modes of operation, respectively with the noise sources from the programming current source and the transresistance current amplifier readout present. The transfer functions of the various noise sources referred to the integration node across the pixel capacitor, C_{pix}, are:

$$\frac{VI}{I_{n2}} = \left(\frac{1 + sRon(CP1X + Cgd}{1 + SRonCgd}\right)\left(\frac{ro + Ron + SRonro(Cgd + Cline)}{Ronro}\right) + \left(\frac{gmRo - 1 - SRonCgd}{Ron}\right) \tag{3.57}$$

$$\frac{VI}{V_{n2}}$$

$$= \left(\frac{SCgd\left[\left(\frac{1}{Ron} + SCgd\right) + \left(\frac{1}{Ron} + \frac{1}{ro} + S(Cgd + Cline)\right)\right]}{\left(\frac{1}{Ron} + S(Cgd + Cpix)\right)\left(\frac{1}{Ron} + \frac{1}{ro} + S(Cline + Cgd)\right) + \left(\frac{1}{Ron} + SCgd\right)(gm - \frac{1}{Ron} - SCgd} \right) \quad (3.58)$$

$$\frac{VI}{I_{n1}}$$

$$= \left(\frac{\left[\left(\frac{1}{Ron} + \frac{1}{ro} + S(Cgd + Cline\right) - (\frac{1}{Ron} + SCgd)\right]}{\left(\frac{1}{Ron} + S(Cgd + Cpix)\right)\left(\frac{1}{Ron} + \frac{1}{ro} + S(Cline + Cgd)\right) + \left(\frac{1}{Ron} + SCgd\right)(gm - \frac{1}{Ron} - SCgd} \right) \quad (3.59)$$

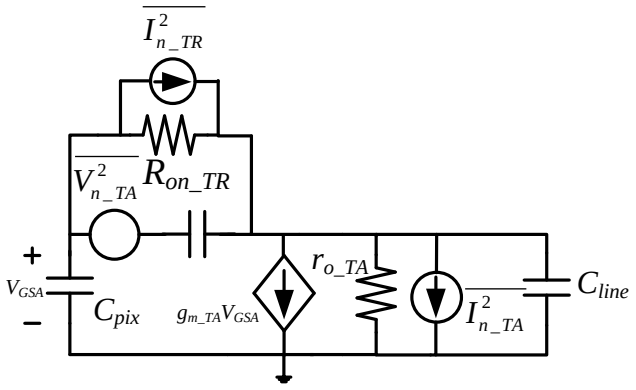


Figure 3.30 Equivalent small signal of the APS during programming.

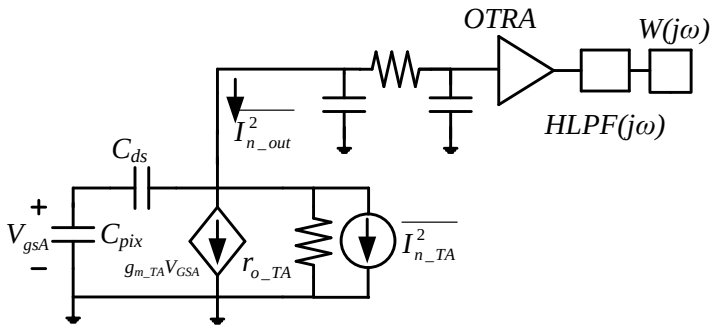


Figure 3.31 Equivalent small signal of the APS during Readout.

Here, I_{n2} is the thermal noise of the amplifying TFT, TA. V_{n2} is the flicker noise of the amplifying TFT, TA and I_{n1} is the thermal noise of the reset TFT, TR. Since in the steady state during programming, the current flowing through TR approaches zero, there is no flicker noise associated with TR. Using the technique described in [**38**], the power spectral density of the total noise is calculated as

$$S_{AZ}(f) = |H_0(f)|^2 S_N(f) + S_{fold}(f) \tag{3.60}$$

$$S_{fold}(f) = \sum_{n=-\infty, n\neq 0}^{n=+\infty} |H_n(f)|^2 S_N\left(f - \frac{n}{T_s}\right) \tag{3.61}$$

Where, the first term represents the baseband noise and the second term shows the fold-over component due to aliasing. All the noise sources contributing to the total input referred noise are considered and their corresponding transfer functions are used instead of $S_N(f)$.The dominant term in the expression for the total input referred noise is the transconductance, $g_{m\text{-}TA}$, of the amplifying TFT, TA. Total input referred noise in terms of number of electrons is shown in Figure 3.32. It is shown that for values of $g_{m\text{-}TA}$ larger than 1μA/V, the input referred noise becomes less than 1000 electrons which is the required value for fluoroscopic applications.

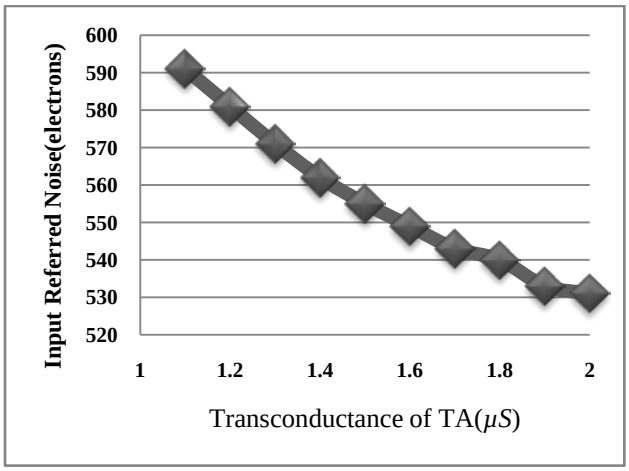


Figure 3.32 The total input referred noise in electrons versus the transconductance of TA

Using the theory presented earlier, the contribution from various noise sources is presented in Table 3.3. In order to produce low-noise images for x-ray modalities like fluoroscopy throughout the dosage range, the total electronic noise should be less than the quantum noise, which is approximately 1000 electrons for a-Se photoconductors at electric fields of 10 V/μm at fluoroscopy energy levels [**12**]. We have calculated the total input referred noise based on the theoretical analysis presented in [**38**]. It is found that the thermal noise coming from TA during readout and the thermal noise of TW during programming have the most significant noise contribution among all the different noise sources present in the circuit due to the foldover effect caused by aliasing. These calculations are based on the power spectral density measurements of the thin film transistors fabricated in University of Waterloo. Table 3.3 shows the various noise contributions confirming that the total input referred noise is below the quantum noise limit of the x-ray imager.

Table 3.3 Total input referred noise of DCAPS (in electrons) from various noise sources. The noise results are extracted from the fabricated 3TFT DCAPS pixel circuit using the theory presented in the paper with the measured gain and noise values.

Input referred noise (electrons)	a-Si:H TFT circuit
TA thermal noise(prog)	10
TW thermal (prog)	141
TA flicker (prog)	100
TA flicker(readout)	450
Data line thermal noise	20
Current Amplifier thermal noise	63
Current Amplifier flicker noise	40
a-Se dark current shot noise	67
TW leakage current shot noise	24
TA thermal(readout)	198
Total noise	530

3.8 Current scaling active pixel sensor

The pixel circuit presented in Figure 3.33 contains four TFTs (T1, T2, TD and TAMP) coupled to the X-ray sensor. TAMP is the amplifying TFT while T1 and T2 act as switches and TD imposes the operation mode of TAMP. Following the timing diagram displayed in Figure 3.33, the pixel circuit operation can be described as follows. During the programming cycle, S1 is connected and the SELECT and READ control line signals turn on the switching TFTs T1 and T2. Consequently the pixel is selected and in the steady state, the whole of constant bias current I_{bias} passes through T2, TD and TAMP. In this cycle, when the steady state is reached, the current flowing through T1 approaches zero and consequently TAMP and TD have the same gate voltage. The diode-connected TFT, TD, always operates in the saturation region (3.69) while TAMP operates in the triode region (3.70) since its drain voltage is lower than the pinch-off voltage.

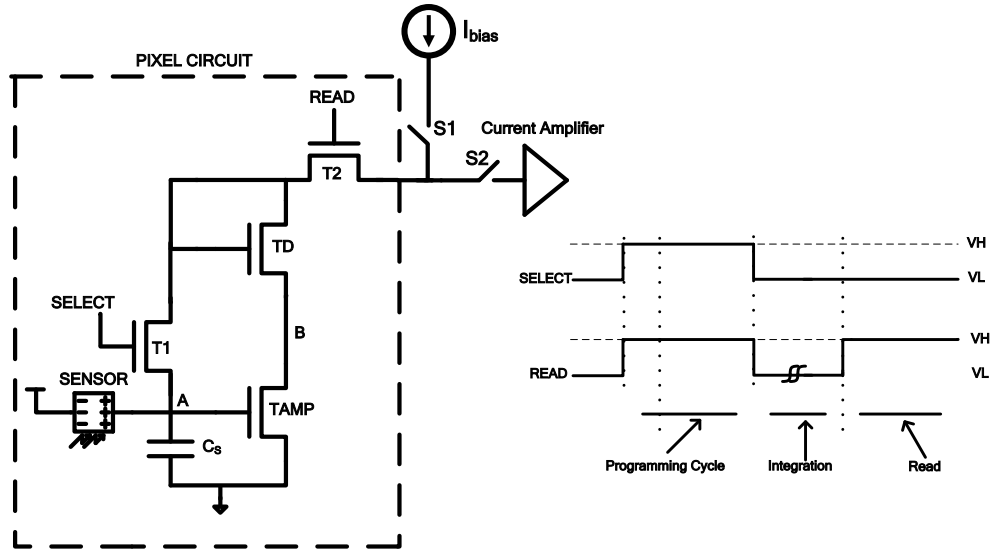


Figure 3.33 Schematic diagram of the current scaling pixel circuit and the programming waveforms

$$I_{bias} = \frac{K_{TD}}{2}\left(V_A - V_B - V_T\right)^2 \tag{3.62}$$

$$I_{bias} = K_{TAMP}\left(\left(V_A - V_T\right)V_B - \frac{1}{2}V_B{}^2\right) \tag{3.63}$$

After programming, both T1 and T2 are turned off. The storage capacitor C_S holds the previously established voltage value on the integration node (A). During the integration cycle, the photo-carriers caused by incident x-ray photons change the voltage at node A by ΔV_A

$$\Delta V_A = \frac{qN_h}{C_S} \tag{3.64}$$

where N_h is the total number of holes accumulated on C_S. In the readout cycle, S2 is connected. The current signal is read out non-destructively through the ON-resistance of T2. Here, both TAMP and TD operate in saturation. Consequently, the current-voltage characteristic of TAMP can be written as

$$I_{out} = \frac{K_{TAMP}}{2}\left(V_A + \Delta V_A - V_T\right)^2 \tag{3.65}$$

Combining the previous equations to obtain an explicit analytic formula which can be used for pixel design, the result can be simplified to read

$$\begin{aligned} I_{out} &= \left(I_{bias} + g_{m-TAMP} \times \Delta V_A\right)\left(1 + \frac{K_{TAMP}}{2 \times K_{TD}}\right) \\ &= \left(I_{bias} + g_{m-TAMP} \times \Delta V_A\right)\left(1 + \frac{\left(W/L\right)_{TAMP}}{\left(W/L\right)_{TD}}\right) \end{aligned} \tag{3.66}$$

It is seen that I_{out} is a linear function of the transistors' dimensions and is independent of the nonuniformity of the a-Si:H TFTs between pixels. The total transconductance gain provided by this pixel is $g_{m-TAMP\times}\left(1 + \frac{\left(W/L\right)_{TAMP}}{\left(W/L\right)_{TD}}\right)$. Therefore, the total gain provided by this pixel circuit is scaled up compared with g_{m-TAMP} of the 3-TFT APS presented earlier by a factor controlled by

TFT dimensions comprising the pixel circuit. To verify the effectiveness of the proposed pixel circuit, several measurement based simulations were conducted using an inverted staggered a-Si:H TFT structure. Plasma enhanced chemical vapor deposition (PECVD) is used for deposition of a-SiN (300 nm thick), a-Si:H, and passivation layers at a temperature of 300°C. Cadence SpectreS simulation tool with a measurement based a-Si:H TFT model [**39**] previously developed was used to further investigate the operation of the circuit. The concept is that if the threshold voltage of TAMP changes due to inherent instability of TFTs, the TAMP gate voltage will be adjusted accordingly to pass the constant I_{bias} during programming. Figure 3.34 demonstrates successful compensation for threshold voltage shift of both TAMP and TD. Since TAMP and TD are located close to each other, it can be assumed that their threshold voltages change similarly. The relative error of the output current is less than 6% for over 4 V shift in the threshold voltage of TAMP. The device parameters used for circuit simulations are as follows. $W/L_{(TAMP)}$ = 1000μm/23μm, $W/L_{(TD)}$ = 500μm/23μm, $W/L_{(T1)}$ = 50μm/23μm and $W/L_{(T2)}$ = 50μm/23μm. C_S = 2pF and K_{TAMP} = 0.02 μF/Vs. [assuming W/L(TAMP)=1]. Initially, it is assumed that the threshold voltage is 2 V for all the TFTs.

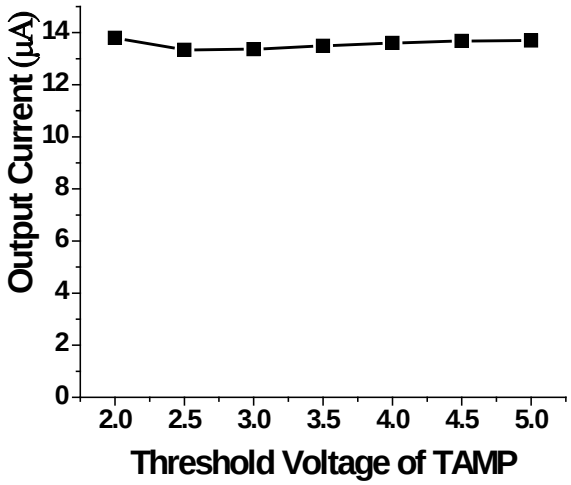


Figure 3.34 Output current versus threshold voltage shift

Figure 3.35 shows a linear relationship between the input current during programming and output current during readout for a relatively wide range of input current. Here the change in the

gate-source voltage during integration mode has been emulated by the change in the input programming current.

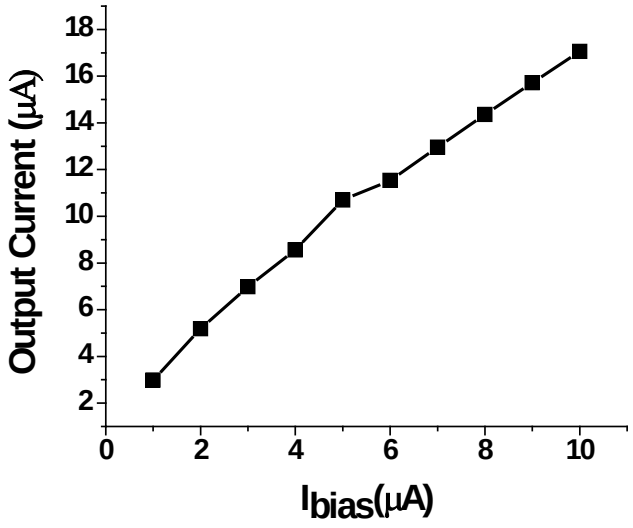


Figure 3.35 Output-Input current characteristics of the current scaling pixel circuit.

3.9 Summary

The immunity of the current programmed APS circuits presented in this chapter to V_T, temperature and process variations makes them attractive for large area digital X-ray imaging applications. Coupled with a strong SNR over a large dynamic range, the a-Si:H APS pixels, interfaced to a commercially available a-Se X-ray detector can usher in a new generation of high performance dual mode medical imagers. The transient response, noise analysis and stability measurements presented here show that the proposed schemes meet the stringent requirements of real time imaging.

4 Implementation of the Bias Current Source and the Current Amplifier

All the APS pixels present in each column in the array share a common current source located at the peripheral of the active matrix flat panel imager (AMFPI). These current sources have fixed values and the magnitude of their currents does not change during the operation of the imager. Therefore, one method to realize these current sources is to have a fixed, temperature invariant current source and copy the value of its current to all the columns of the array. The resistors seen in the APS pixels made of a-Si:H TFTs are in the range of mega ohms and the current mirrors should have output resistances much larger than theses values to act as ideal current sources. To suppress fixed pattern noise arising from high sensitivity of a-S:H TFTs to temperature gradient across the array, temperature independent current sources are proposed, designed and implemented. For the successful readout of current signal provided by individual active pixel sensors in the flat panel array, high gain transresistance amplifiers are designed and implemented in conventional CMOS process. Measurement results revealed in this chapter show that the temperature invariant current source can provide stable current with less that 0.5% shift in spite of considerable variations in the characteristics of the TFTs involved in the circuit. The current amplifier is sensitive enough to be able to detect signals from the current mode APS circuits as low as 1nA, corresponding to lower signal range of fluoroscopic application.

4.1 Cascode CMOS Current Source

The cascode current mirror is a reasonable candidate for the implementation of the current mirror. The current flowing to the gate of each CMOS transistor is zero. Therefore the current mirroring operation does not suffer from finite gate current effects. Figure 4.1 shows the simplest

form of cascode current source realization. Substituting the transistors with their small signal models, the small signal output resistance is

$$R_o=r_{o2}[1+(g_{m2}+g_{mb2})r_{o1}]+r_{o1} \tag{4.1}$$

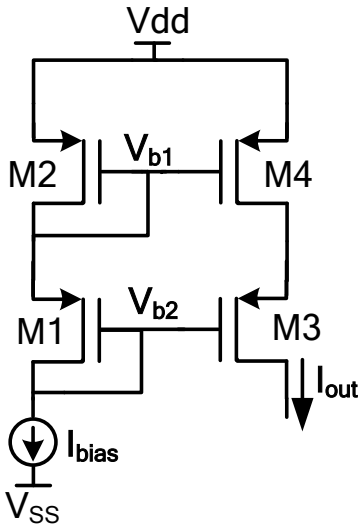


Figure 4.1 Simple Implementation of the current source for each column of the AMFPI

Here, it is worth mentioning that the operation of the MOS cascode current mirror is superior to that of the bipolar cascode current mirror in the sense that the bipolar cascode current mirror cannot realize an output resistance which is larger in value that half of the product of β and output resistance of each transistor [**40**]. In contrast, using CMOS transistors as the building blocks of the cascode current source enables the designer to have arbitrarily high output resistance by increasing the number of stages stacked on top of each other. Using KVL in the simple cascode structure in Figure 4.1,

$$V_{dd}-V_{SD4}=V_{SG2}+V_{SG1}-V_{SG3} \tag{4.2}$$

Since M1 and M2 are diode connected, in the case of $V_{SG1}=V_{SG3}$, M2 and M4 have identical drain-source voltages, i.e. $V_{SD2}=V_{SD4}$. Under this condition, M2 and M4 are identically biased and there is no systematic gain error in the operation of the cascode current mirror. In practice, the output voltage of the current mirror is not equal to the drain voltage of M1. Therefore, due to the errors originated by channel length modulation, as well as mismatch related errors caused by

non-ideal lithographic processes; V_{SG1} is not exactly equal to V_{SG3} giving rise to non-zero systematic gain error. Here we discover the limitations required for input and output voltage headroom. These limitations come from the fact that the proper operation of the current source is achieved only when all the transistors involved are biased properly in the deep saturation region. The input voltage of the MOS cascode current mirror is given by

$$V_{IN}=V_{dd}-V_{SG1}-V_{SG2}= V_{dd}-(V_{T1}+V_{ov1}+V_{T2}+V_{ov2}) \tag{4.3}$$

Here, V_{T1} and V_{T2} are the threshold voltages of M1 and M2, respectively and V_{ov1} and V_{ov2} are the overdrive voltages of the associated transistors. It is seen that the input voltage includes two gate-source voltages which include two threshold voltages as well as two overdrive voltages. For the sake of comparison with the wide swing current source, we ignore the threshold voltage change caused by the body effect and assume equal overdrive voltages for all the transistors involved. Therefore, the value for the input voltage is:

$$V_{IN}=V_{dd}-(2V_{ov}+2V_T) \tag{4.4}$$

It is required that all the transistors including M3 and M4 operate in the saturation region. Under this circumstance,

$$V_{SG2}=V_{SD2}\approx V_{SD4} \tag{4.5}$$

Also, for M2 to be able to operate in the saturation region, it is required that its drain-source voltage be higher than its over drive voltage. Consequently the minimum output voltage for which both transistors in the output branch, M1 and M2 are in the saturation region of their operation is

$$V_{OUT(min)}=V_{DS1}+V_{ov2}=V_{GS3}+V_{ov2}=V_T+V_{ov3}+V_{ov2} \tag{4.6}$$

Assuming that all the transistors have equal threshold and overdrive voltages, the equation is simplified to

$$V_{OUT(min)}\approx V_T+2\times V_{ov} \tag{4.7}$$

If the output voltage is reduced bellow this minimum value, initially M2 goes into triode region for the voltage range of

$$V_{ov1}<V_{OUT}<V_{OUT(min)} \tag{4.8}$$

And if $V_{OUT}<V_{ov1}$, both M1 and M2 are biased in the triode region of their operation. The current source in the actual operation of the array is connected in series to the APS circuit. In order to reduce the power consumption and have higher voltage swing at the output of the current source, the dynamic range of the output voltage of the current source should be maximized. The overdrive voltage can be reduced by increasing the width of M2 at the cost of larger area consumption. The threshold voltage term in (4.7) stems from the fact that M1 is biased at

$$V_{DS1}=V_{IN}-V_{GS2} \tag{4.9}$$

which is equal to V_T+V_{ov} assuming that all the transistors are biased in the saturation region and they have equal threshold and overdrive voltages. However, for M1 to operate in the saturation region, its drain-source voltage should be equal to V_{ov}. Therefore, the drain-source voltage is one threshold voltage larger than the required amplitude. To address the problem, the high swing current mirror shown in Figure 4.2 can be used [**41**]. Here the source follower transistor, M3 is used as a level shifter to transfer the voltage at the gate of M1 to the gate of M5 and level shift the drain voltage of M6 one threshold voltage higher. Here, M3 acts in the source follower configuration and it is biased by the simple current mirror made by M2 and M4. If all transistors have equal threshold and overdrive voltages, the drain-source voltage of M6 would be zero.

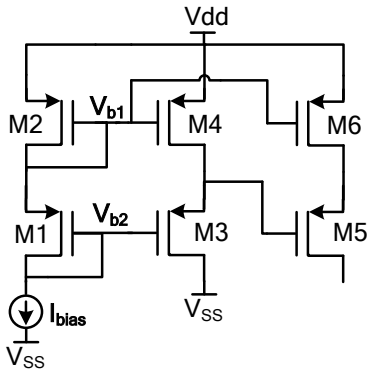


Figure 4.2 High Swing Current Source

However, for M6 to be biased at the boundary between the triode and active region, its drain-source voltage should be equal to the overdrive voltage. Assuming square law operation of the transistors, this can be achieved by doubling the overdrive voltage of M1 by reducing its aspect ratio by a factor of four. By this reduction, the threshold voltage term at the drain bias of M6 is deleted and

$$V_{OUT(max)}=V_{dd}-2V_{ov} \tag{4.10}$$

The maximum output voltage at the output terminal of the high swing current mirror does not have a threshold voltage term allowing enough voltage swing at the input terminal of the APS pixel circuits. Both transistors M5 and M6 are biased in the saturation region and therefore the output resistance of the high swing cascode current source can be expressed as (4.1). The input voltage of the current mirror is given by

$$V_{IN}=V_{dd}-V_{SG2}-V_{SG1}=V_{dd}-V_{T2}-V_{ov2}-V_{T1}-V_{ov1} \tag{4.11}$$

The drop in the voltage across M1 and M2 is increased compared to that of the simple cascode current mirror due to the fact that the overdrive voltage of M1 is increased by a factor of two because of four times reduction in its aspect ratio. Therefore,

$$V_{IN}=V_{dd}-2V_{T}-3V_{ov} \tag{4.12}$$

M2 and M6 form a simple current mirror. The drain-source voltage of M2 is $V_{ov}+V_T$, whereas the voltage across the drain-source terminal of M6 is V_{ov} thanks to efforts made to maximize the output voltage swing of the current source. This causes a systematic error in the operation of this current source equal to

$$\epsilon = \frac{V_{DS6}-V_{DS2}}{V_A} = \frac{V_{ov6}-(V_{ov2}+V_T)}{V_A} = \frac{-V_T}{V_A} \tag{4.13}$$

The aspect ratio of the transistors are given in Table 4.1 and are chosen such that all the transistors operate in the saturation mode while delivering the small current value of 1µA to the APS circuit. Figure 4.3 shows the output current of the current source versus its terminal voltage. From this graph, it is apparent that the current source can provide output resistance in the excess of 2GΩ which is much larger compared to the mega ohm resistances seen in the APS circuit. In

Figure 4.4 the current noise power spectral density at the output of the current source is shown. This data is used to calculate the total electron noise referred to the integration node of the APS circuit.

Table 4.1 Aspect ratio of the transistors comprising the Current Source

Name	Aspect Ratio
M1	438n/180n
M2	8.75µ/900n
M3	8.75µ/180n
M4	8.75µ/900n
M5	9.5µ/1µ
M6	9.5µ/1µ

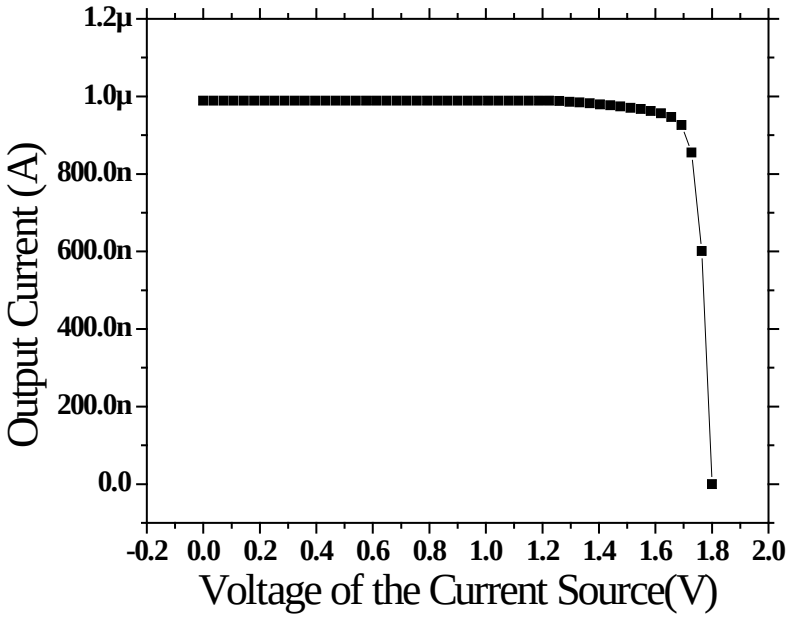


Figure 4.3 Output current of the current source versus its terminal voltage

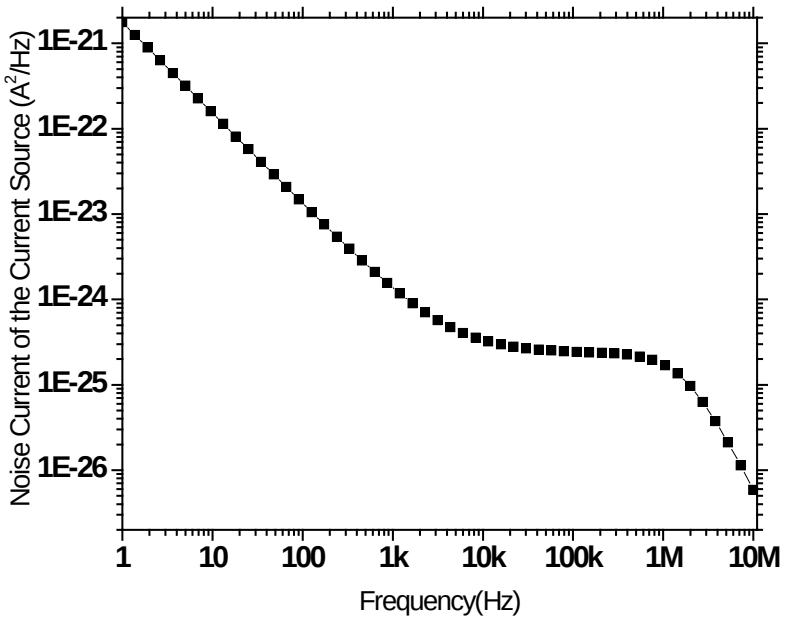


Figure 4.4 Current noise power spectral density at the output of the current source

4.2 Feedback Controlled Current Source

An alternative solution for realizing the off-panel current source is shown in Figure 4.5. In this configuration, negative feedback has been employed to take advantage of performance improvements such reduced sensitivity of gain to device parameter changes. The transistor TC can be both a TFT located at the peripheral of the imager or a CMOS transistor. The current source consists of a current driving TFT (TC) and a feedback resistor (R_C). The opamp used in the feedback configuration in a rudimentary form is a differential input, single output amplifier. When the feedback is established, the current flowing through the drain-source terminal of TC is converted to a voltage by making a voltage drop across the feedback resistor, R_C. The feedback line conveys this feedback voltage to the non-inverting terminal of the differential amplifier. Because of the negative feedback in the system, the output of the differential amplifier adjusts the voltage at the gate terminal of TC and therefore modulates the drain-source current terminal of TC to minimize the voltage difference at the inverting and non-inverting terminals of the

opamp. Assuming that the opamp is ideal, it exhibits a very high voltage gain, creating a virtual ground between its inverting and non-inverting terminals. The bias current flowing through the channel of TC and used to reset the current programmed APS pixel circuits is in the range of microamps which is much larger than the leakage current flowing into the input terminals of the opamp. Therefore, the steady state current value of TC is

$$I_{bias} = \frac{V_{bias}}{R_C} \tag{4.14}$$

It is seen that the bias current is directly determined by V_{bias} and R_C. It is independent of the parameters and the characteristics of TC. This characteristic is important particularly when a TFT is used for TC. V_{bias} and R_C can be provided with high degree of stability. Therefore this circuit can provide a constant and stable bias current for the APS circuits. The current bias pixel circuit compensates for the V_T shift in TC, as long as the voltage at the gate of TC does not exceed the maximum output range of the differential amplifier. The drain bias voltage supplied by V_{CC} should be high enough to keep TC in the saturation region.

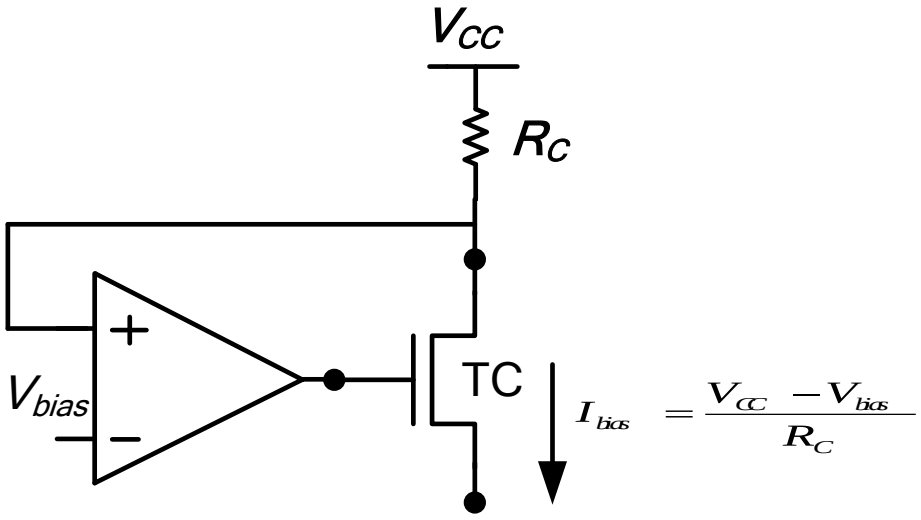


Figure 4.5 Realization of the feedback Controlled Current Source

4.2.1 Stability Analysis of the Feedback Controlled Current Source

Due to the inherent negative feedback in the current source, ideally, there is no error in the output current, I_{bias} due to variations in the static characteristics of TC, in particular, those

associated with the threshold voltage shift. However, static effects such as the limited gain of the external differential amplifier cause error in the final value of the output bias current, I_{bias} which will be further discussed in the following. These errors cause variation in the bias established across the storage capacitors of the APS circuits resulting in fixed pattern noise of the final image.

4.2.2 Stability of Feedback Resistor

According to (4.14), the output current of the current bias is inversely proportional to R_C; thus, instability in R_C instigates instability in the value of I_{bias} .Therefore, it is crucial to investigate the stability of R_C at the first step of the design of the current source. High precision temperature stable resistor array with precision of 0.01% in the temperature range of -25^{o}C to+125^{o}C are commercially available. These resistors can be used to provide the array of current sources with low temperature sensitivity and high degree of matching between the values of the output currents. These resistors can be used in the feedback to provide a highly stable, temperature insensitive bias current if an a-Si:H TFT is used as TC. The output current of the current source is determined by the value of the feedback resistor. Therefore the uniformity of the pixel current depends on the matching properties of the feedback resistors across the entire column of the imager.

4.2.3 Temperature Induced Instability

As discussed in previous chapters, temperature variation has a profound effect on the threshold voltage and mobility of a-Si TFTs. Due to the inherent characteristics of the negative feedback, the proposed topology for the off-panel bias current source significantly reduces the sensitivity of the column current to the variations in TFT parameters, and thus, temperature variations. However, there are still some temperature dependent mechanisms that affect the output current namely temperature-dependence of R_C [**23**].

4.2.4 Temperature Induced Variations of R_F

In the proposed current source scheme in Figure 4.5, I_{bias} directly depends on the value of R_C. Therefore any change in R_C by temperature, changes I_{bias}. Although the estimated change is

much smaller than that in a conventional 3-TFT APS [**27**] or the voltage programmed APS [**19**]. To improve the sensitivity of the bias current source, I_{bias}, to temperature, two resistors in each column current source can be used as shown in Figure 4.6. Here, the voltage at the non-inverting terminal of the opamp is generated by passing the bias current, I_{bias} through a reference resistor, R_2. Therefore, the programming current of the APS is set as

$$I_{bias} = I_{in} \frac{R_1}{R_2} \tag{4.16}$$

Since R_1 and R_2 have identical temperature coefficients, sensitivity of the bias current to the temperature is significantly reduced.

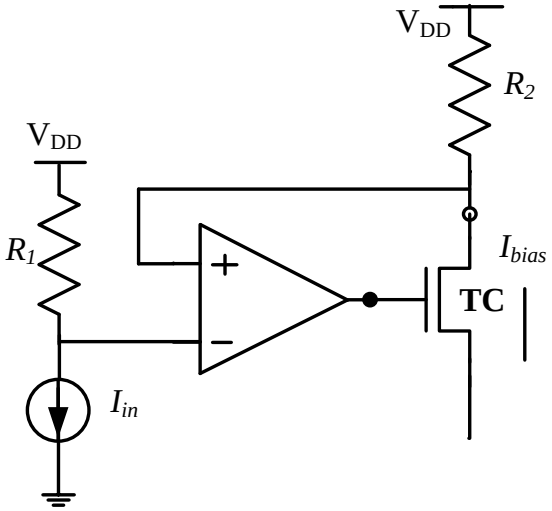


Figure 4.6 Temperature independent Current Source

4.2.5 Effect of the Reverse Current of TFTs

When an APS pixel is selected for resetting by the fixed off-panel current source, the other APS pixels in the same column are deselected and their switch TFTs are OFF. However, each OFF TFT has a small reverse current, as shown in Figure 4.7. Due to the large number of switch TFTs connected to the data line, the total parasitic current can be considerable. The leakage current of the switching TFTs is directly added to the bias current source, I_{bias}. If the reverse current of a TFT switch is I_{OFF}, then the programming current of the selected pixel is approximated by

$$I_{bias} = \frac{V_{bias}}{R_C} + (N-1) \times I_{OFF} \tag{4.17}$$

For simplicity, it is assumed that the gain and the input resistance of the external differential amplifier are infinite. The second term in (4.17) is the error associated with the reverse current and should be smaller than the minimum pixel current. The value of I_{OFF} principally depends on the fabrication process, TFT size, and the biasing voltage of the switch TFTs, and can be in the range of 0.1 pA to 10 pA [**42**]. Assuming that the array has 1000×1000 pixels and I_{OFF}=1pA the estimated error in I_{bias} is close to 1 nA witch is quite tolerable. To minimize the error, it is crucial to minimize I_{OFF} by properly biasing the TFT switches in the reverse mode.

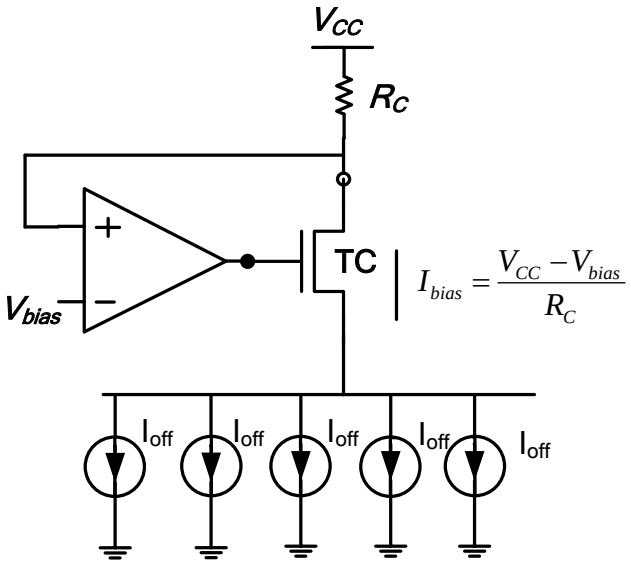


Figure 4.7 Circuit model to illustrate the Effect of the reverse current of the TFTs on the same column of the bias current

4.2.6 Static Stability of the Feedback Current Source

The implementation of the current source with the negative feedback as shown in Figure 4.5 has the advantage of reducing the sensitivity of the output current, I_{bias}, to the inevitable shift in threshold voltage of TC. Although the sensitivity is not entirely eliminated due to the finite gain of the opamp present in the feedback loop, it is significantly reduced. To investigate the effect of finite opamp gain on the sensitivity of the output current of the bias source to the variation in the threshold voltage, the following sets of equations are solved:

$$I_{bias} = \frac{1}{2} K_{TC} (V_{GS-TC} - V_{T-TC})^2 \tag{4.18}$$

$$V_{GS-TC} = A_v(V_{bias} - I_{bias} \times R_C)^2 \quad (4.19)$$

where it is assumed that the gain of the opamp is equal to A_v. We define the relative error in the output current of the current source, I_{bias}, as ΔI_{bias} /I_{bias}. Here, I_{bias} is the nominal value and ΔI_{bias} is caused by shift in the threshold voltage of TC due to prolonged voltage stress. To investigate this error, the current source circuit in Figure 4.5 with the circuit parameters in Table 4.2 is simulated. Figure 4.8 shows the relative error in the amount of output current of the current source for different gains in the opamp. It is seen that the higher the voltage gain of the opamp, the lower is the relative error caused by the shift in the threshold voltage of TC.

Table 4.2 Circuit parameters used for simulation of the circuit in Figure 4.5

Design Parameter	Value
C_S	1pF
I_{bias}	1µA
W_c/L_c	250µm/23µm
A_v	10^3,10^4,10^5

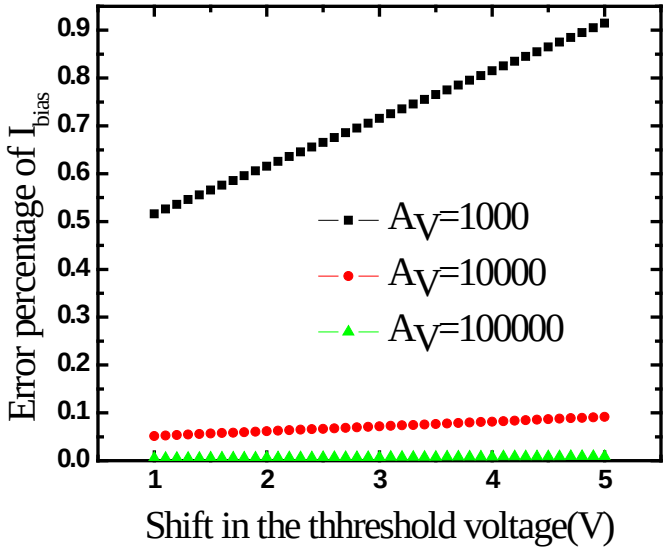


Figure 4.8 Relative error in the amount of output current of the current source for different opamp gains

4.2.7 Discussion and Results of the feedback controlled current source

To measure different characteristics of the feedback current source including DC response, transient response, noise and stability, a discrete TFT fabricated with tri-layer in-house process [**42**] is used. The contact layer for the TFT is n+ microcrystalline. To realize the capacitor, the top plate is the same as the contact layer of the TFT used for connecting the source/drain terminals to other parts of the circuit and the bottom plate is the same as the gate metal layer. The threshold voltage, effective mobility and the ON/OFF current ratio are approximately equal to 2-4, 0.8-1 cm^2/Vs and 10^8-10^9, respectively. The pixel circuits are diced and packaged in 24-pin DIP ceramic packages. A general purpose bread board is used to connect the pins of the ceramic package to the proper pins of the opamp and the voltage sources. A Keithley SMU was used to apply the bias voltages and read the output current. For transient and settling time tests, discrete capacitors are used to emulate the effect of the large capacitance associated with the data line. A commercial monolithic Op-Amp (AN604) is used as the amplifier of the feedback due to its high gain and low input bias current. In the transient measurements, a resistor in connected to the output of the current source to convert the output current to voltage. This voltage is captured and saved by a digital oscilloscope with 8-bit resolution.

4.2.8 Measurement of the DC operation of the Feedback Current Source

The current source is supposed to provide the entire APS pixels in each column with a DC constant value current. The output of the current source should be directly proportional to the applied bias to the opamp terminal and proportional to the reverse of the feedback resistor. Figure 4.9 shows the measured output current versus the bias voltage. The output current measurement is achieved by a Kiethley 236 source-meter unit (SMU). Here the feedback resistance is 1MΩ and the bias voltage is varied from 0 to ten volts. As predicted by (4.1), there is a linear relation between I_{bias} and V_{bias}. During the operation of the array, there might be times where the bias current has to change instantly for higher noise performance or lower power dissipation. This can be simply achievable by varying the bias voltage making the current source, variable.

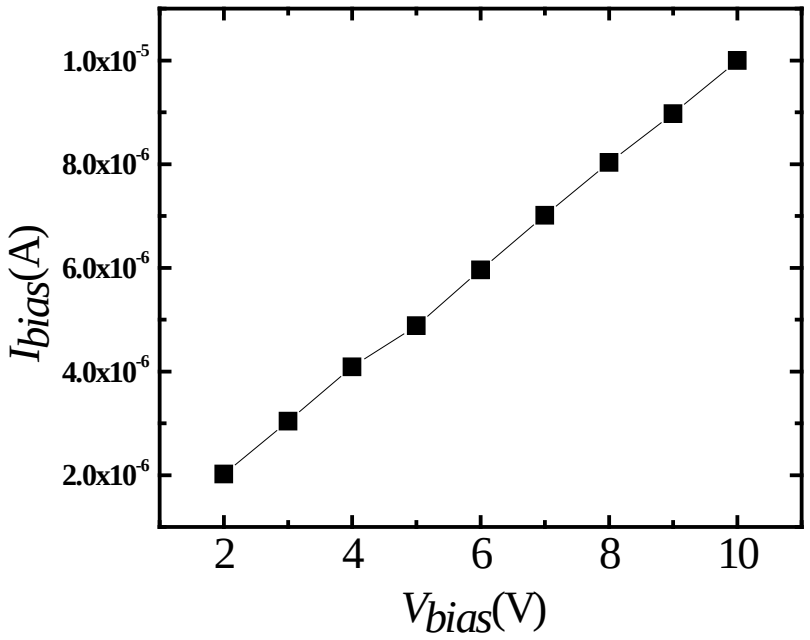


Figure 4.9 Measured output current versus the bias voltage.

4.2.9 Simulation results on the temperature independent Current Source

As mentioned in the previous chapters, the parameters of the a-Si:H TFT including its threshold voltage and mobility have a large correlation with temperature. The simulations in this part show the effectiveness of the feedback controlled current source to address this problem. First the temperature sensitivity of the circuit is Figure 4.5 is simulated. Figure 4.10 shows the output current of the current source versus temperature when the initial current is 1μA. In this circuit, the output current is inversely proportional to the feedback resistor, R_F. Therefore by using an off-chip temperature invariant resistor, the sensitivity of the output current versus temperature is expected to drop. However this leads to higher cost. As discussed before, an alternative solution is to use two identical resistors at both the inverting and non-inverting terminals of the opamp. In this case, ordinary resistors with higher temperature coefficients can be used. Also as suggested in Figure 4.11, the two resistors can be realised by two identically biased transistors in the saturation region. It is worth mentioning that the transistors are biased in the saturation region in order to be able to provide output resistance in the range of hundreds of kΩ. Simulations results on the temperature independent circuit of Figure 4.11 are shown in Figure 4.12. Here the variation in the output current is less than the 0.03% over 60^{o}C change in temperature.

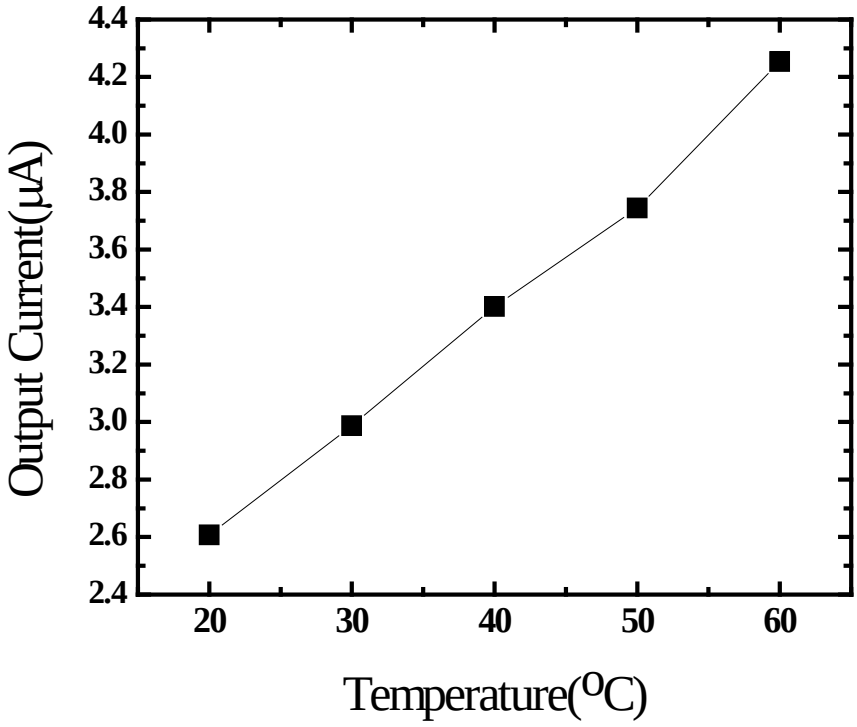


Figure 4.10 change in the output current versus temperature is around 60%

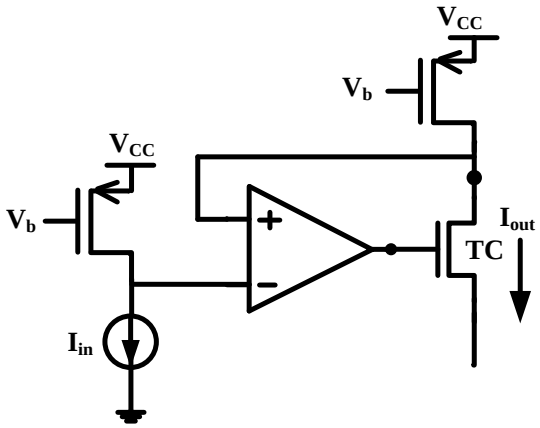


Figure 4.11 Replacing the resistors with PMOS transistors biased in saturation

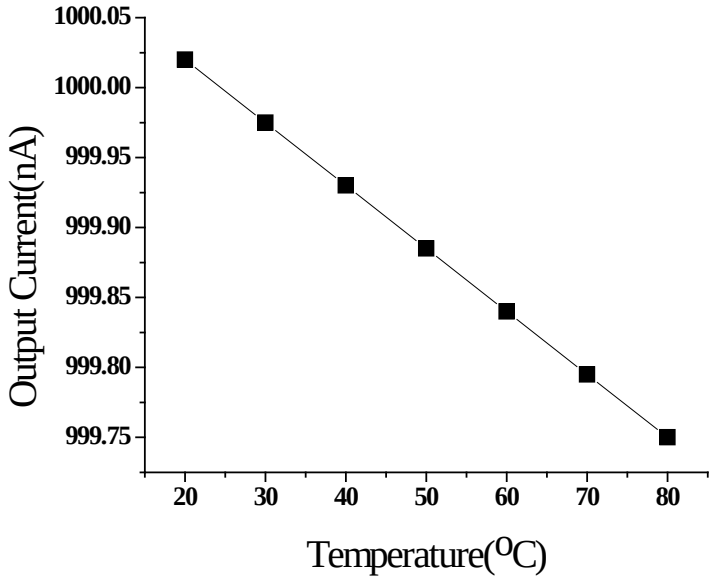


Figure 4.12 Change in the output current versus temperature is less that 0.03%

4.3 Implementation of CMOS Readout Current Amplifier

Here, we discuss the circuit techniques and implementation of high-performance current amplifiers. Offset compensation strategies are reviewed and different ways of implementing them are discussed. According to the proposed and suggested design strategies a novel transresistance amplifier as off-panel signal readout circuit is presented. The proposed CMOS amplifier achieved a high speed operation, demonstrated a low input resistance in the frequency range of operation and a well defined input bias voltage that can be used to bias the on-pixel amplifier TFT APS circuit.

4.3.1 Offset Compensation Schemes

One of the fist current amplifiers with offset compensation was proposed in [**43**]. The problem with this approach is its complexity and the fact that it cannot easily be extended to different circuit architectures. There are two offset-compensation techniques that can easily be applied to different comparator circuits. In these techniques, the circuit can be divided to two distinct parts: one part is the uncompensated current amplifier and the other part has a compensating role for

the former segment of the circuit. The latter can be connected in parallel or series form to the uncompensated current amplifier. In what follows, the two different compensation techniques together with the circuit implementation are discussed. We will also discuss the error originated from charge injection and clock feed-through of the switch transistors and the topology to reduce that error.

4.3.2 Connecting the Compensation Circuit in Parallel Form to the Transresistance Amplifier

The solution for offset compensation of the transresistance amplifier is schematically demonstrated in Figure 4.13 [**44**]. Here, the schematic consisting of g_m and r_{o2} represents a transconductance amplifier. In this scheme, the compensation circuit consists of the storage capacitor, C_S, the switch SC and the transconductance circuit which is connected in parallel to the output node. The uncompensated current amplifier is modeled by the current controlled current source with r_{O1} as its output resistance and I_{OSA} representing its input current offset. The compensation circuit is represented by the voltage controlled current source, g_m, and it output resistance, r_{O2}. V_{OS} shows the input offset voltage of the transconductance circuit. Assuming that switch SC is initially open and capacitor C_S is discharged, the total offset transferred to the output of the circuit is

$$V_{OSO}=r_O I_{OSA}+g_m r_O V_{OS} \tag{4.20}$$

Here r_O is the total resistance at the output of the circuit

$$r_O=r_{O1}||r_{O2} \tag{4.21}$$

Referring the offset to the input of the main current amplifier, we have

$$I_{OS}=I_{OSA}+V_{OSO}/r_O \tag{4.22}$$

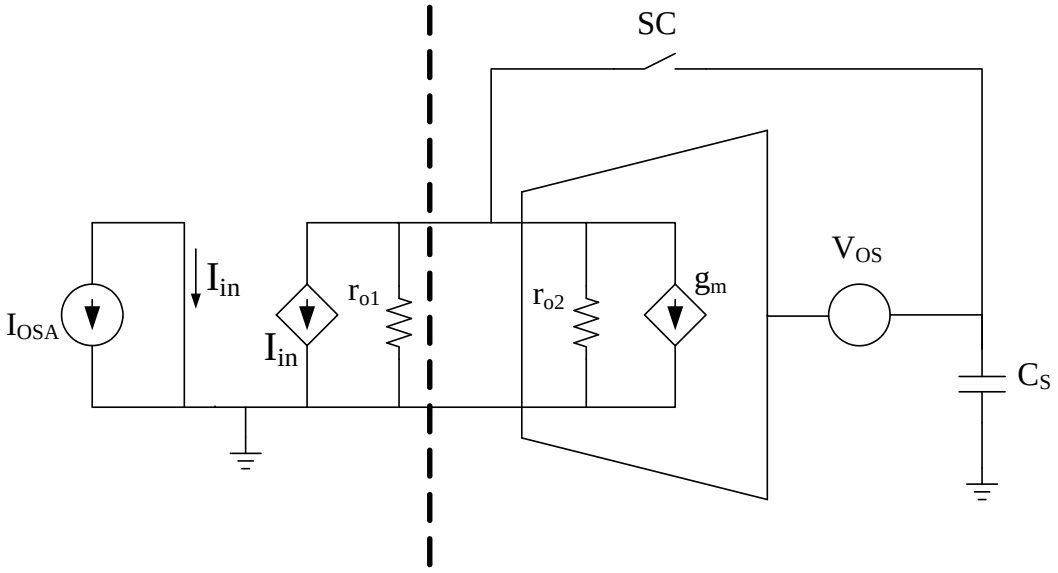


Figure 4.13 The schematic of the offset compensation scheme [**44**].

During the offset cancellation phase, switch SC is closed and the offset cancelling part of the circuit, i.e. the transconductance circuit is in a unity gain configuration feedback. In this mode, the offset voltage at the output node of the circuit becomes

$$V_{OSC} = \frac{I_{OSA} r_O + g_m r_O V_{OS}}{1 + g_m r_O} \cong \frac{I_{OSA}}{g_m} + V_{OS} \tag{4.23}$$

Here, V_{OSC} represents the voltage offset of the output node while switch SC is closed. Upon changing the circuit state from compensation to current amplification mode, switch SC is turned off. The voltage developed across the output during the compensation mode, is stored across the storage capacitor, C_S. The input referred equivalent offset current at the input of the current amplifier becomes

$$I_{OSC} = \frac{V_{OSC}}{r_O} \cong \frac{I_{OS}}{g_m r_O} \tag{4.24}$$

Although the addition of extra offset compensation circuit contributes an extra term to the overall offset current of the circuit, eventually a very low input referred offset current is achieved. The total offset current is reduced by the voltage gain of the transconductance offset cancelation circuit. The actual input signal has to be applied to the input of the current amplifier after the opening of the switch, SC [**44**]. For realisation of the transconductance stage, fully differential,

single ended operational transconductance amplifier (OTA) structures with cascade current mirrors providing high output impedance can be used [**40**].

4.3.3 Compensating for the Error Caused by Charge Injection and Clock Feed-through of the Switches

The accuracy of the circuit structure shown in Figure 4.13 is affected by the charge injection and clock feed-through of the SC switch. When the switch transistor is turned on, it would be biased in the triode mode. When it is turned off at the end of the compensation mode, a portion of its channel charge is directed towards the storage capacitor, C_S, causing an uncompensated term in the circuit offset. If ΔQ is the channel charge of SC, the charge injection modifies the input referred offset current of the current amplifier into

$$I_{OSC} = \frac{I_{OS}}{g_m r_O} + g_m \Delta \mathrm{VQ} \tag{4.25}$$

Here ΔVQ is the change of the storage capacitor voltage at the input of the transconductance stage caused by the charge injection, ΔQ.

$$\Delta \mathrm{VQ} = \Delta Q / C_S \tag{4.26}$$

The portion of the charge released from SC into the storage capacitor, C_S, depends on the falling rate of the control voltage of the switch, the total amount of the channel charge of the switch as well as the ratio between the capacitances at its drain and source terminals [**45**], [**46**]. To address this problem and reduce the value of ΔVQ, common solutions are to use a larger C_S and/or dummy CMOS switches. Another more useful and efficient method is to make the input of the current compensating transconductance amplifier fully differential by using another replica in the second input terminal (Figure 4.14). Here the switches S_{A1} and S_{A2} have equal aspect ratio as well as equal voltages at their terminals. Assuming that the clock turning off the switches has a sharp edge, the voltage change across the capacitors CH1 and CH2 is equal. Consequently, the injected charge from the switches gives rise to the common mode input signal which will be rejected due to the differential nature of the transconductance amplifier [**44**].

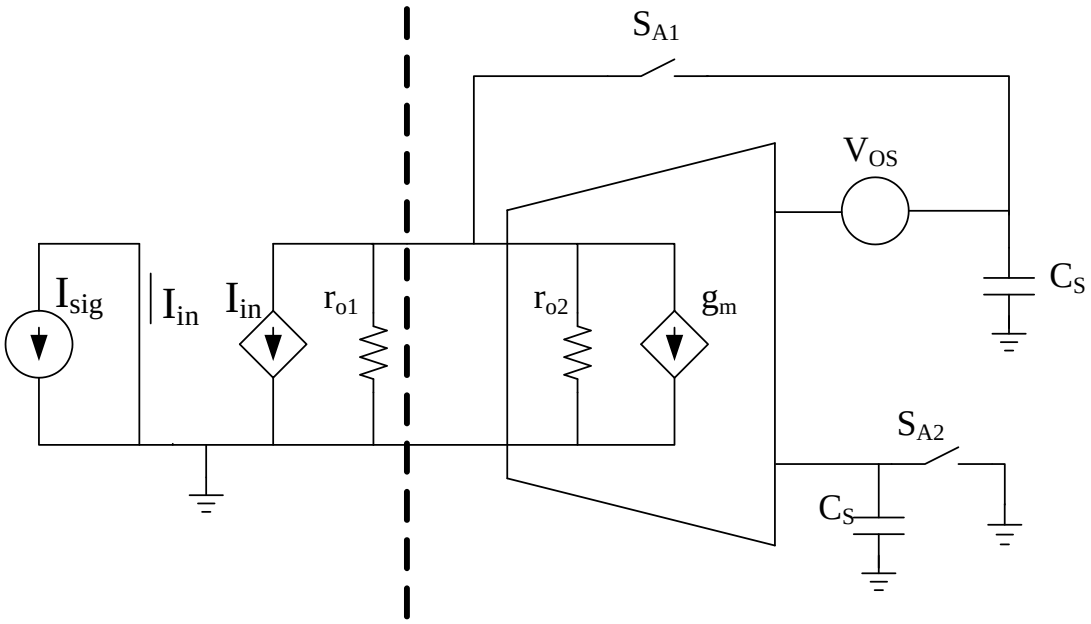


Figure 4.14 Cancelling the effect of charge Injection [**44**]

4.3.4 Connecting the Compensation Circuit in Series Form to the Transresistance Amplifier

In the former approach, the compensation circuit is connected to the output of the current amplifier in parallel form. The advantage of this scheme is that, provided that the compensation circuit and the current amplifiers are stable, no further limitation on the frequency response of the current amplifier would be imposed. However, the drawback of this method is that due to the parallel connection of the compensation circuit and the current amplifier, the output impedance and hence the overall gain will be lowered, causing reduction in the sensitivity of the current amplifier. One way to address this problem is to use compensation circuit topologies with very high output impedance levels. However, it is rather difficult to implement such topologies due to the limited voltage headroom and the need for cascade stacking of the CMOS transistors. Figure 4.15 shows an alternative solution which does not affect the low frequency gain of the current amplifier [**44**]. This method uses a feedback loop to generate the offset cancelling current signal and subtract it from the input current. The feedback loop includes a switch SC, a voltage gain block, A, and a transconductance block which can be simply realised by the transistor M1.

Contrary to the parallel connected scheme, the transconductance part which is represented by M1 is in series with the output of the current amplifier. Therefore the output impedance is not

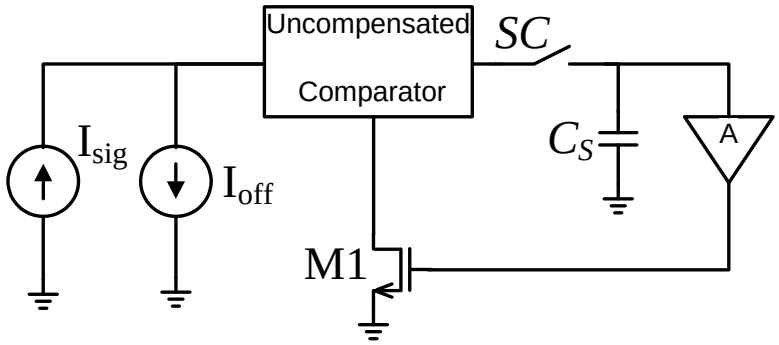


Figure 4.15 Current Amplifier using the series-connected offset compensation [**44**]

reduced and affected. The analysis of the parallel connected scheme can easily be extended to this method. It is worth mentioning that g_m should be replaced by $A.g_{M1}$ where A is the DC gain of the voltage gain stage and g_{M1} is the transconductance of M1 [**44**]. The total offset current referred to the input of the current amplifier before cancelation is

$$I_{OS}=I_{OS1}+Ag_{M1}V_{OS2} \tag{4.27}$$

After offset compensation, the input referred offset will reduce to

$$I_{OSC} = \frac{I_{OS}}{g_{m1}\mathrm{A}r_O} \tag{4.28}$$

Here V_{OS2} is the input referred offset voltage of the voltage gain A block and r_O is the total output resistance of the uncompensated current amplifier. When switch SC is closed the stability of the loop should be investigated. Similar to what was proposed in the parallel connected scheme, Figure 4.16 shows the circuit to reduce the error caused by charge injection and clock feed through of the operating switches. Here the voltage gain block A is replaced by a differential input stage. Fabricated transistors suffer from threshold-, mobility-, and geometry-induced mismatch effects as well as the low frequency $1/f$ noise resulting in dc offset and limiting the

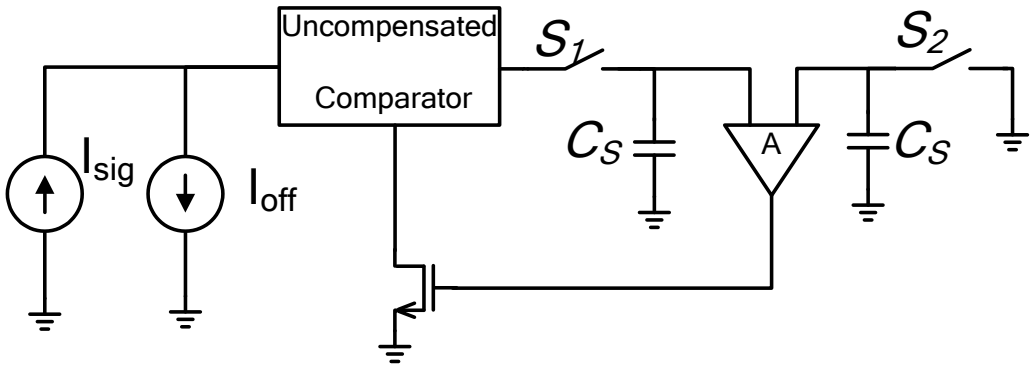


Figure 4.16 Cancelling the effect of charge injection of the switches [**44**]

minimum detectable signal level . To alleviate these problems, devices with large active areas are chosen for input stages because threshold voltage and mobility mismatches and 1/f noise are inversely proportional to the size of the device. However, to achieve input-referred offset currents in the range of few nano amps without sacrificing a large die area, dynamic offset-cancellation circuit techniques such as correlated double sampling CDS are usually employed. The CDS principle can be used to reduce the offset and low-frequency noise of the on-pixel amplifiers and off-panel readout CMOS circuits [**47**].

4.4 Design of the Readout Transresistance Amplifier

In the ideal case, a transresistance amplifier has zero input impedance and an infinite transresistance gain converting the input current data from the APS pixel circuit to the output voltage form. One method for implementation of the transresistance amplifier is using a two stage amplifier in which the first stage is a second generation current conveyer (CCII) and the second stage is the voltage gain stage. A simplified schematic of this design is shown in Figure 4.17 [**48**].

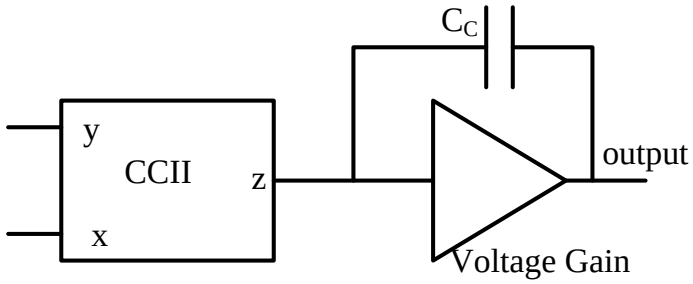


Figure 4.17 The general schematic for the implementation of the transresistance amplifier

In a second generation current conveyer port [**49**], the x terminal has low input impedance while the y terminal has high input impedance. Therefore the x terminal is used as the input terminal of the current data from the APS pixel circuit. The voltage at the x terminal follows the voltage applied to the y terminal. Therefore in the operation of the transresistance amplifier we have the degree of freedom to change the voltage applied to the y terminal and therefore change the bias of the APS circuit. The input current to the x terminal is conveyed to the z terminal and because of the high impedance of the z terminal; it is converted to voltage with high gain. In order to achieve very high transresistance gain, another voltage gain stage is cascaded to the CCII stage. C_C is the compensating feedback capacitor for generating dominant pole at the z terminal of the CCII due to the Miller effect.

4.5 Transresistance Amplifier as the Off-panel External Circuit

To realize the current amplifier, the circuit in Figure 4.18 was first suggested and implemented [**50**]. The pixel readout circuitry utilizes second generation current conveyor as its basic building block.

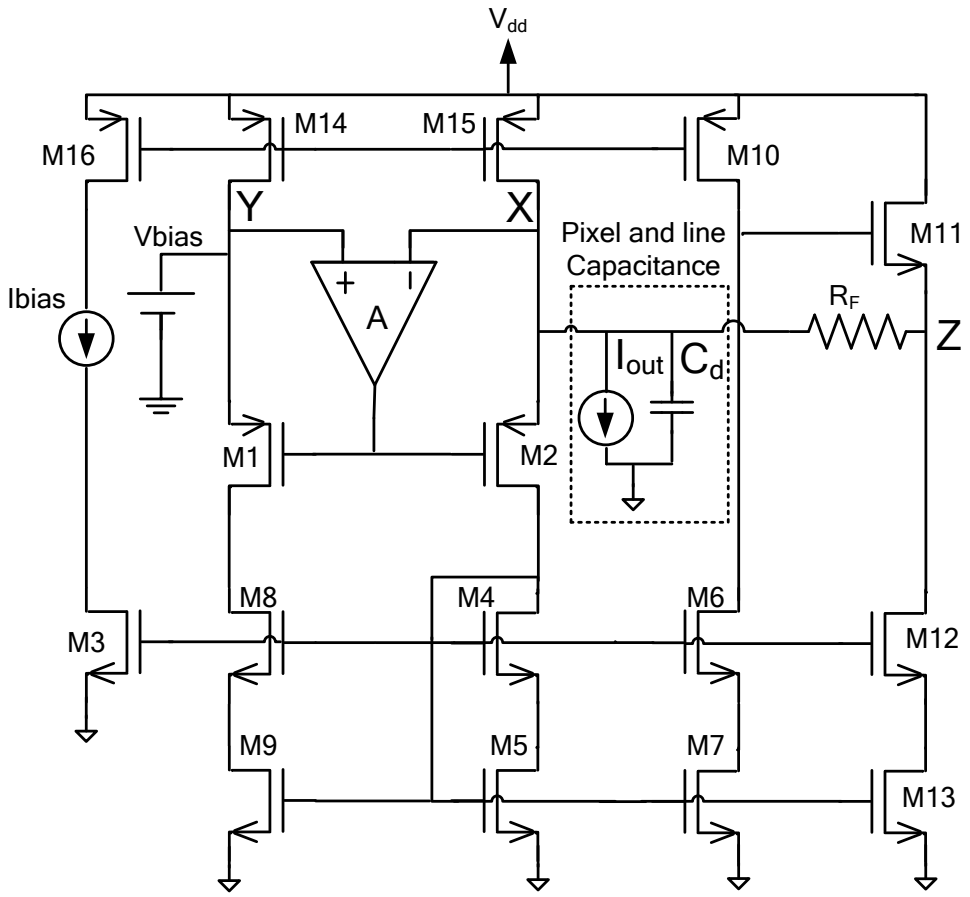


Figure 4.18 CMOS transresistance feedback amplifier.

The low input impedance is intended to reduce the readout time by decreasing the effect of relatively large parasitic capacitor of the data line C_d. The transresistance feedback amplifier in Figure 4.18 can be used for the column readout circuitry. I_{OUT} and C_d=20pF represent a first-order simple model of the pixel circuit during readout and the large line capacitance, respectively. V_{bias} is connected to the high-impedance Y terminal and is followed by the low impedance virtually grounded X terminal. M3-M9 make a wide swing cascade current mirror [**49**] which conveys the input current to the internal high impedance gate node of M11. M11-M13 form the source follower. The feedback network consists of R_F=80K which samples the output voltage at the Z terminal and feeds back the proportional current to the input X terminal. Amplifier A is used to increase the transconductance of M2 and consequently decrease the input impedance of X. M3 and M16 form the bias circuit and M10, M14 and M15 are used as current sources.

4.5.1 Simulation Results of the Pixel and Transresistance Readout Circuits

To implement the transresistance column amplifier, 0.35μm CMOS process and CADENCE SPECTRE simulator are used. Figure 4.19 depicts the transient output voltage at the Z terminal when a current pulse of 10μA is applied to the input. It can be seen that the output settling is achieved rather fast which makes the reading scheme suitable for correlated double sampling (CDS) in the timing constraint of real-time fluoroscopy.

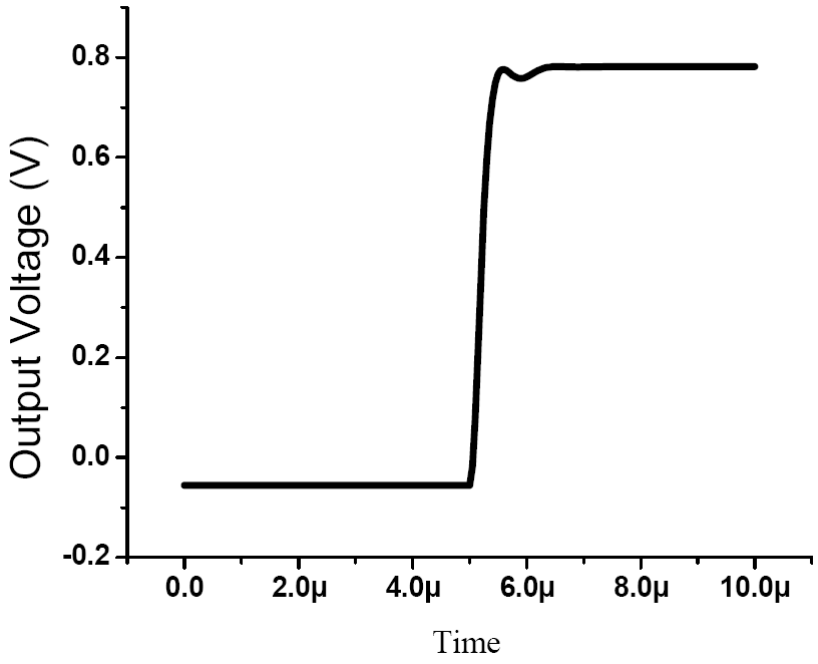


Figure 4.19 Transient output voltage response to input pulse current

Figure 4.20 illustrates the gain magnitude of the transresistance amplifier versus frequency. The low-frequency high-gain is required to cope with the problem of low x-ray dosage in some diagnostic schemes such as fluoroscopy. Figure 4.21 demonstrates the low input impedance versus frequency. The input low impedance bypasses the large capacitor of the column line and therefore improves the readout time of the pixel circuit. In the same graph, the input impedance without amplifier is shown. As can be seen, the amplifier has a considerable effect in lowering the input impedance [**51**].

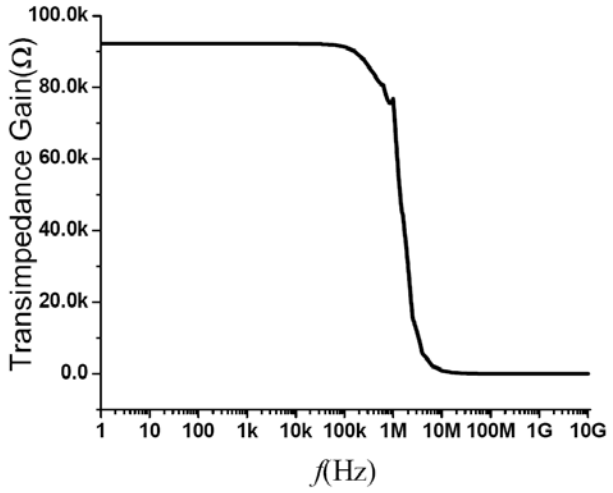


Figure 4.20 Closed loop gain of the amplifier versus frequency

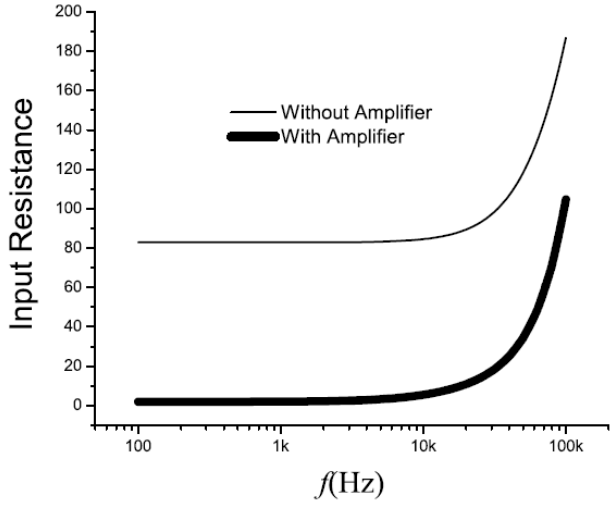


Figure 4.21 The input impedances of the transresistance circuit with and without the opamp, A, at the input versus frequency

Even though the circuit in Figure 4.18 provides very low input impedance necessary for fast readout of the APS pixels, It cannot perform correlated double sampling which is necessary for noise and offset reduction [**52**]. In the following, three transresistance amplifiers with the ability of operation correlated double sampling on the output signal from the APS circuits are proposed and implemented.

4.6 Transresistance Amplifier with Double Sampling as the Off-panel External Circuit

The correlated double sampling (CDS) principle can be used to reduce the offset and low-frequency noise of the on-pixel amplifiers and off-panel readout circuits. A simplified schematic of the approach is shown in Figure 4.22 [**53**]. It is shown that this approach can be optimized for both offset and charge injection compensation [**44**]. The method is based on a feedback loop. A transresistance amplifier constitutes the basic amplifier of the feedback loop while the feedback network consists of a switch, a storage capacitor (C_S) and a voltage to current converter. If we assume that initially C_S is discharged, the total input offset current of the amplifier is

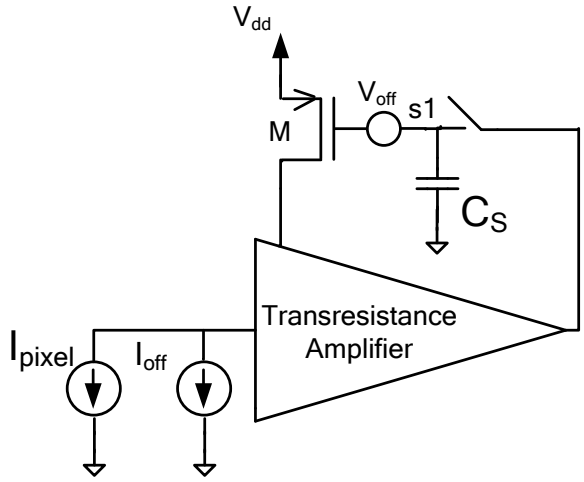


Figure 4.22 Block diagram of the Transresistance Amplifier with offset compensation

$$I_{off-TOT} = I_{off} + g_m V_{off} \tag{4.29}$$

Here, I_{off} is the input offset current of the transresistance amplifier, V_{off} is the input offset voltage of the feedback network and g_m represents the feedback gain. When the S1 switch is closed, the compensated input offset current reduces to [**44**]

$$I_{off-comp} \approx \frac{I_{off-TOT}}{1+g_m R} \tag{4.30}$$

where R accounts for the forward gain of the transresistance amplifier. Therefore, this method effectively reduces the offset currents and voltages at the inputs of the basic amplifier and the feedback network. The schematic of the proposed readout circuit utilizing CDS is shown in Figure 4.23. The readout circuit operation consists of two phases: a sampling phase (Φ_S) during which the current data, offset and the current noise of readout circuit and the pixel are sampled and stored and an amplifying phase (Φ_A) during which the offset and noise free transresistance amplifier is available for signal readout. During the sampling phase, the switches S1 are closed. As a result, the total circuit implements a shunt-shunt feedback configuration. The basic transresistance amplifier in this feedback configuration is composed of transistors M1- M20 and includes cascode current sources and cascode current mirrors. The feedback network consists of transistors M21 and M22 making a differential pair. It shunts both the output and the input of the

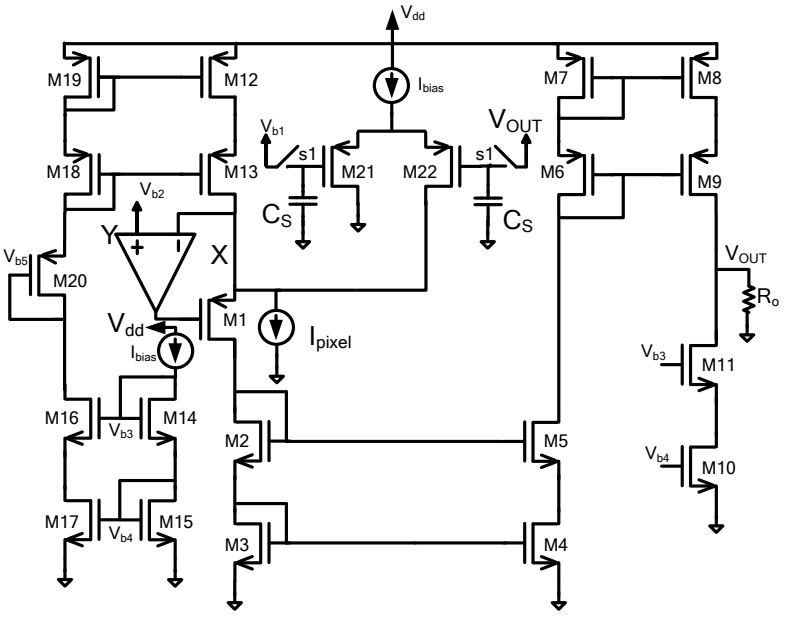


Figure 4.23 Schematic of the proposed Transresistance Amplifier with Double Sampling Capability.

basic amplifier and feeds back a current proportional to the output voltage V_{OUT}. The DC

transresistance gain of the basic amplifier is given by

$$A_r(0) \approx \left[(g_{m9} r_{o9} r_{08}) \| (g_{m11} r_{o10} r_{011}) \| R_O \right] \times \frac{W_4}{W_3} \times \frac{W_8}{W_7} \tag{4.31}$$

while the DC transconductance feedback factor is determined by

$$f(0) \approx g_{m22} \tag{4.32}$$

Thanks to the high value of the loop gain, the error current approaches zero and therefore the drain current of M22 becomes almost equal to $I_{pixel}(\Phi_S)$ in this phase. $I_{pixel}(\Phi_S)$ consists of various factors during the sampling mode.

$$I_{pixel}(\phi_s) = I_{bias} + I_{data} + I_{os} + I_N(\phi_S) \tag{4.33}$$

Here I_{os} and $I_N(\Phi_S)$ represent the offset current of the transresistance amplifier and the noise of both the off-panel amplifier and the pixel circuit at the end of sampling phase, respectively. The gate-source voltage corresponding to $I_{pixel}(\Phi_S)$ is sampled and stored across the storage capacitor C_S. In the amplifying phase, the S1 switches are turned off and the feedback network is disconnected from the signal path. The pixel circuit is also reset and read out. Therefore $I_{pixel}(\Phi_A)$ changes to

$$I_{pixel}(\phi_A) = I_{bias} + I_{OS} + I_N(\phi_A) \tag{4.34}$$

Here, $I_N(\Phi_A)$ is the total noise of the amplifier and the pixel circuit during the amplifying phase. At this phase, $I_{pixel}(\Phi_S)$ and $I_{pixel}(\Phi_A)$ are effectively deducted from each other and the resulting current is amplifies by the feed-back free, transresistance amplifier. This method can be used not only to cancel the off-panel current amplifier offset but also to reduce the low frequency noise of both the on-pixel amplifier and the off-panel transresistance amplifier. The opamp at the input terminal, X, is used to reduce the input resistance of the amplifier to

$$R_{input} = \frac{1}{g_{m1} \times A_V} \tag{4.35}$$

where A_V is the opamp gain and g_{m1} is the transconductance of M1. To have a large gain, the opamp is implemented using cascode topology shown in Figure 4.24. To implement the transresistance amplifier, standard 0.35µm CMOS process models are used. The circuit parameters are listed in Table 4.3. The feedback switches S1 are turned off at 12.5µs. Before the feedback loop is inactive (S1 switches are closed), the amplifier output voltage (V_{OUT}) is equal to V_{b1} which is set to 0V for this design. When the S1 switches are turned off, the feedback loop becomes inactive and the basic transresistance circuit amplifies the input current with high gain and sensitivity. Figure 4.25(b) shows the transient response of the readout circuit to the input current waveform of Figure 4.25(a).

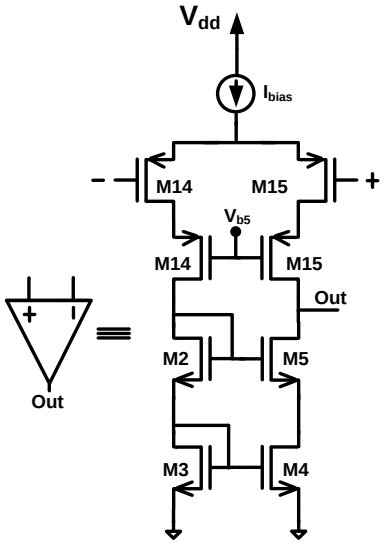
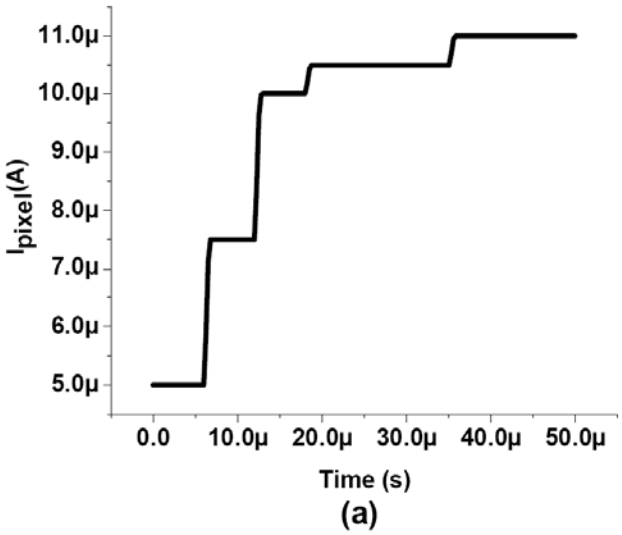


Figure 4.24 Topology of the opamp used in the Transresistance Amplifier of Figure 4.27.

Table 4.3 Circuit Parameters of the Transresistance Amplifier

Name	Value	Name	Value
M14, M15	2µm/0.35 µm	M12, M13	1µm/0.35 µm
M2, M3	2µm/0.35 µm	M4, M5	4µm/0.35 µm
M4, M5	2µm/0.35 µm	M10, M11	8µm/0.35 µm
M18, M19, M20	2µm/0.35 µm	M16, M17	2µm/0.35 µm
M6, M7	4µm/0.35 µm	M8, M9	8µm/0.35 µm



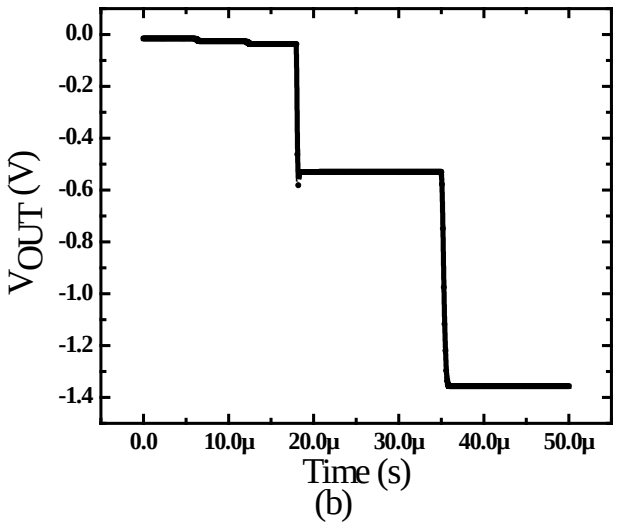


Figure 4.25 (a) Input current, (b) Transient response of the column amplifier.

Even though the transresistance circuit in Figure 4.23 can perform double sampling necessary for noise reduction, the gain of the circuit is not high enough for exposure modalities such as fluoroscopy. The other drawback with this circuit is that the transconductance stage is not fully differential. As a result, the charge injection and clock feed through associated with the switch

causes error in the output voltage. To mitigate these problems, another current amplifier with charge injection cancellation is proposed and implemented in the following section.

4.7 Transresistance Amplifier with Double Sampling Capability and Fully Differential Feedback Network

Fabricated transistors suffer from threshold-, mobility-, and geometry-induced mismatch effects as well as the low frequency 1/f noise resulting in dc offset and limiting the minimum detectable signal level [**54**]. To alleviate these problems, devices with large active areas are chosen for input stages because threshold voltage and mobility mismatches and 1/f noise are inversely proportional to the size of the device. However, to achieve input-referred offset currents in the range of few nano amps without sacrificing a large die area, dynamic offset-cancellation circuit techniques such as correlated double sampling CDS are usually employed. The CDS principle can be used to reduce the offset and low-frequency noise of the on-pixel amplifiers and off-panel readout circuits [**38**]. A simplified schematic of the proposed low offset approach is shown in Figure 4.26. The method is based on a feedback loop. A second generation current conveyor topology (CCII) constitutes the forward amplifier of the feedback loop while the feedback network is comprised of a transconductance amplifier (i.e., g_m), two offset cancelling capacitors (i.e., C_{h1} and C_{h2}) and the clock signal φ. The input voltages V_{ref1} and V_{ref2} are used as virtual ac grounds. V_{ref1} determines the voltage across the low input resistance terminal of the transresistance amplifier and V_{ref2} is used as the reference for the amplifier's output voltage, V_{out}.

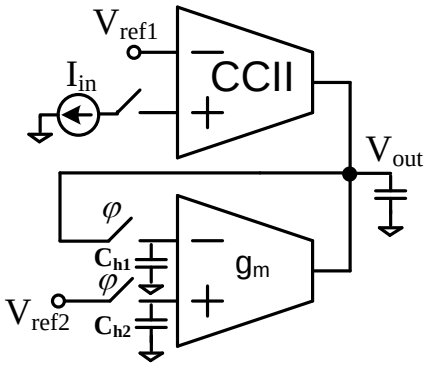


Figure 4.26 Block diagram of the Transresistance Amplifier with offset compensation.

4.7.1 Offset Cancellation of the Transresistance Amplifier

Assuming that the capacitors C_{h1} and C_{h2} are initially discharged, the total input referred offset current of the amplifier originates mainly from the input offset current of the CCII and the input offset voltage of the g_m amplifier

$$I_{off-TOT} = I_{os} + g_m V_{os} \tag{4.36}$$

Here, I_{os} is the input offset current of the CCII, V_{os} is the input offset voltage of the transconductance amplifier and g_m represents the gain of the transconductance amplifier. During the offset cancellation phase [Figure 4.27(a)], the low resistance terminal of the CCII is disconnected from the signal path and the transconductance amplifier connected in unity-gain configuration. The voltage stored in the capacitor C_{h1} becomes

$$V(C_{h1}) = \frac{I_{os} \times R_{out} + (V_{ref\,2} + V_{os}) \times g_m R_{out}}{1 + g_m R_{out}} \approx \frac{I_{os}}{g_m} + (V_{ref\,2} + V_{os}) \tag{4.37}$$

where R_{out} accounts for the total resistance at the amplifier's output node and $g_m R_{out}$ is the loop gain which is designed to be much larger than one. In the amplification phase, the input current data is connected to the CCII and the two switches connected to the storage capacitors are turned off, breaking the unity gain feedback loop. The previously stored voltage values remain across the storage capacitors except a small change, V_{inj}, due to charge injection and clock feed through errors of S1 and S2.

$$V(out) = \left[I_{in} + I_{os} + V_{ref2} + (V_{os} + V_{inj} - V(Ch1)) \times g_m\right] R_{out} = \begin{bmatrix} I_{in} + I_{os} + V_{ref2} + (V_{os} + V_{inj}) \times g_m \\ -(\frac{I_{os}}{g_m} + (V_{ref2} + V_{os})) \times g_m \end{bmatrix} R_{out} \quad (4.38)$$
$$\approx \left[I_{in} + V_{inj} \times g_m\right] R_{out}$$

In the above formulae it is postulated that the CCII, conveys the current to its output terminal with unity gain. Therefore, this method effectively reduces the offset currents and voltages at the inputs of the basic amplifier and the feedback network. Therefore, the input referred offset after the cancellation phase is limited by V_{inj} and can be alleviated by increasing the size of storage capacitors, C_{h1} and C_{h2}, at the differential input of the g_m amplifier. This method not only reduces offset of the off-panel amplifier, but also suppresses the low frequency noise of both the on-pixel amplifier and the off-panel CMOS readout circuit.

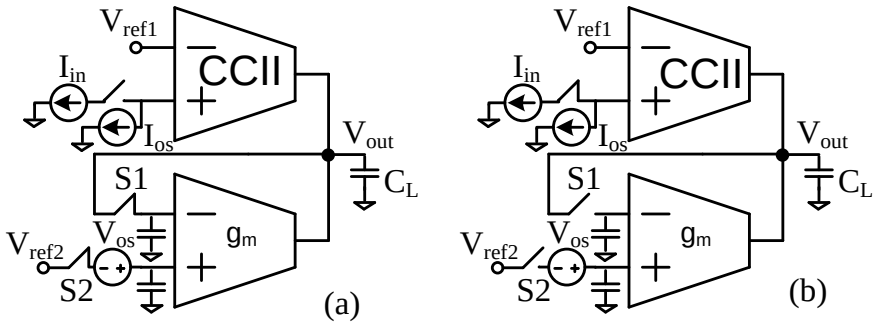
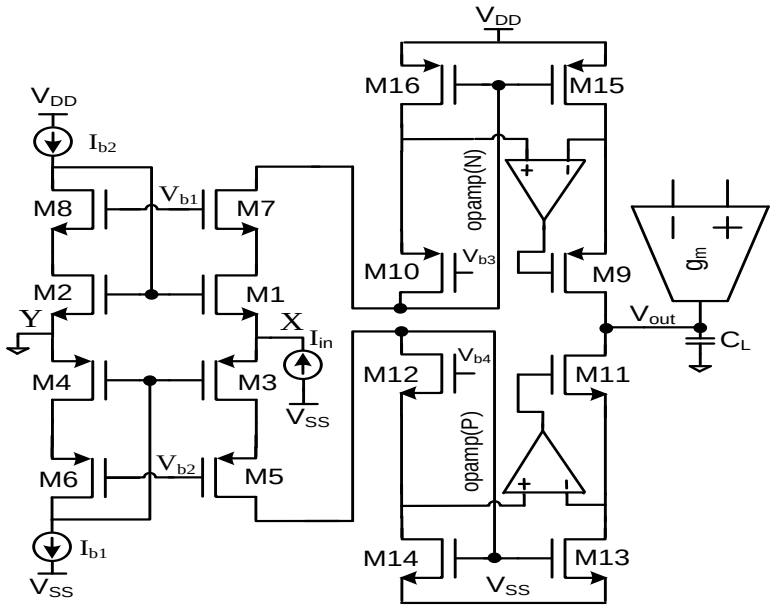


Figure 4.27 (a) Phase 1: Offset Cancellation, (b) Phase 2: Input Current Amplification.

4.7.2 Circuit Realization of the Fully Differential Transresistance Amplifier

To realize the current amplifier scheme utilizing CDS, the circuit in Figure 4.28(a) is proposed [**47**]. The class AB current conveyor (CCII) exhibits a current following action between the input node (X) and the output node (V_{OUT}) and a voltage following action between Y and X. It is comprised of transistors M1-M16, current sources I_{b1} and I_{b2} and two opamps (opamp(N) and opamp(P)) with nMOS and pMOS input differential pairs, respectively. The current source I_{in} represents the current data coming out of the pixel circuit in different modes of operation. The amplifiers opamp(N) and opamp(P) are standard two-stage, Miller-compensated opamps. The input terminals of opamp(N) are virtually short-circuited. Therefore it equates the drain voltages

of M15 and M16 causing significant reduction in channel-length modulation related errors. Its other role is to provide bias for the cascading pMOS, M9. The same argument applies to opamp(P) and the devices M13, M14 and M11. The cascading devices M9 and M11 are added to the upper and lower branches to boost their respective output impedances resulting in overall increase in the output impedance of the current conveyor and equivalently the overall gain of the transresistance amplifier. The transconductance stage (g_m) used in the offset cancellation process is realized by the single-ended differential cascode topology to achieve high output impedance as shown in Figure 4.28(b).



(a)

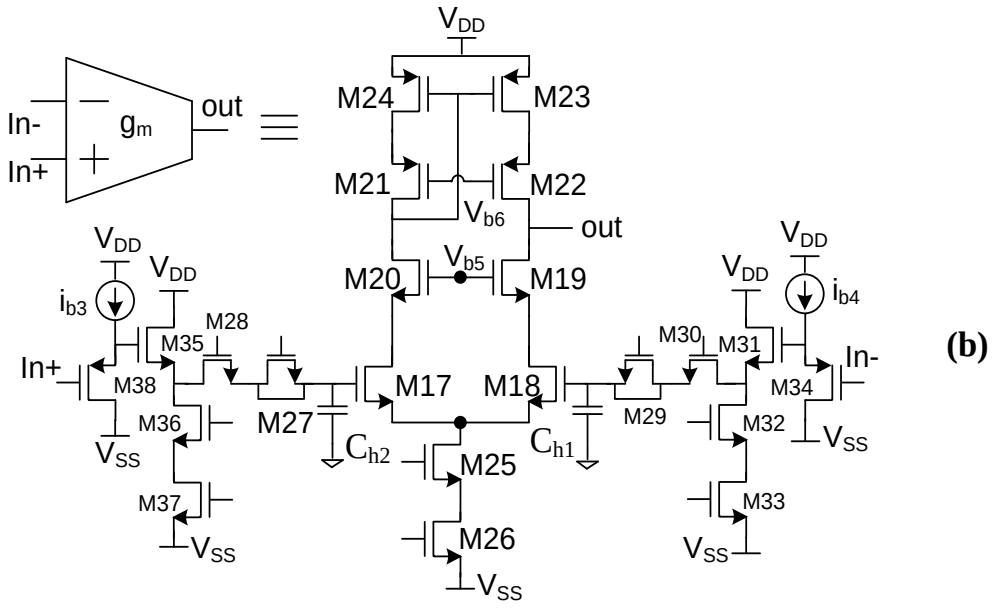


Figure 4.28 (a) Proposed CCII transresistance amplifier and its offset cancellation transconductance stage, (b) Implementation of the transconductance (gm) stage.

4.7.3 Experimental Results of the Fully Differential Transresistance Amplifier

Prototypes of the pixel circuit were fabricated with in-house tri-layer inverted-staggered amorphous silicon TFT process. Plasma enhanced chemical vapor deposition (PECVD) is used for deposition of a-SiN (300 nm thick), a-Si:H, and passivation layers at a temperature of 300 ˚C. Figure 4.29 shows a photomicrograph of a fabricated pixel circuit. The circuits were then diced and packaged. The transresistance amplifier was fabricated in a 0.35 µm CMOS technology. Figure 4.30 shows a die photomicrograph of the transresistance amplifier. The TFT pixel circuit, the transresistance amplifier and auxiliary circuitry were assembled on a printed circuit board. Discrete capacitors were used to emulate the effect of parasitic capacitance of the lines on the transient response of the pixel circuit. Figure 4.31 demonstrates successful compensation for threshold voltage shift of TA for a programming current of 8.5 µA. The (W/L) of TA, TR and TW are 1000µm/23 µm, 200 µm/23 µm and 50 µm/23 µm, respectively. The size of the storage capacitor is 2pF. For 3V V_T shift in TA, the relative change in the output current is less than 5%. To emulate the x-ray sensor a voltage source with amplitude varying from 10mV to 1V is connected to the integration node (I) through capacitive coupling. The voltage gain is shown in

the inset of Figure 4.31, confirming that the pixel circuit maintains a relatively constant gain across a wide dynamic range of input signals.

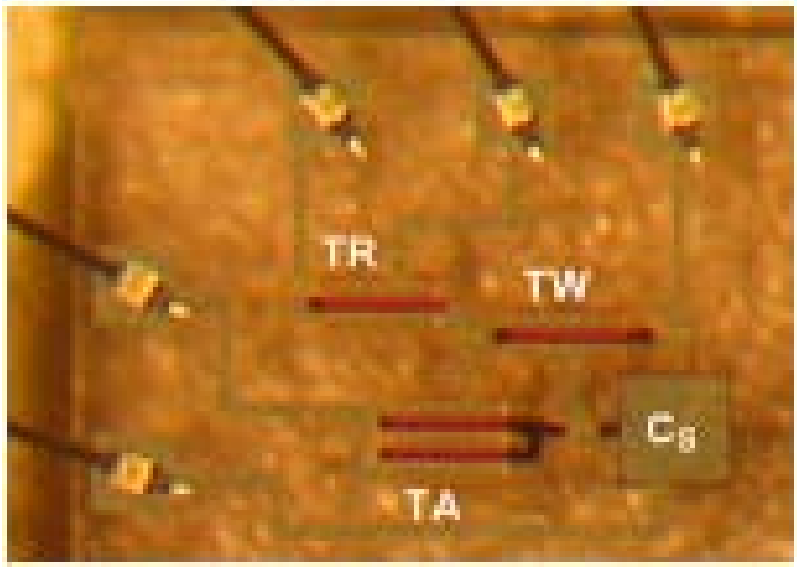


Figure 4.29 Micrograph of a fabricated APS pixel circuit with a-Si:H TFTs

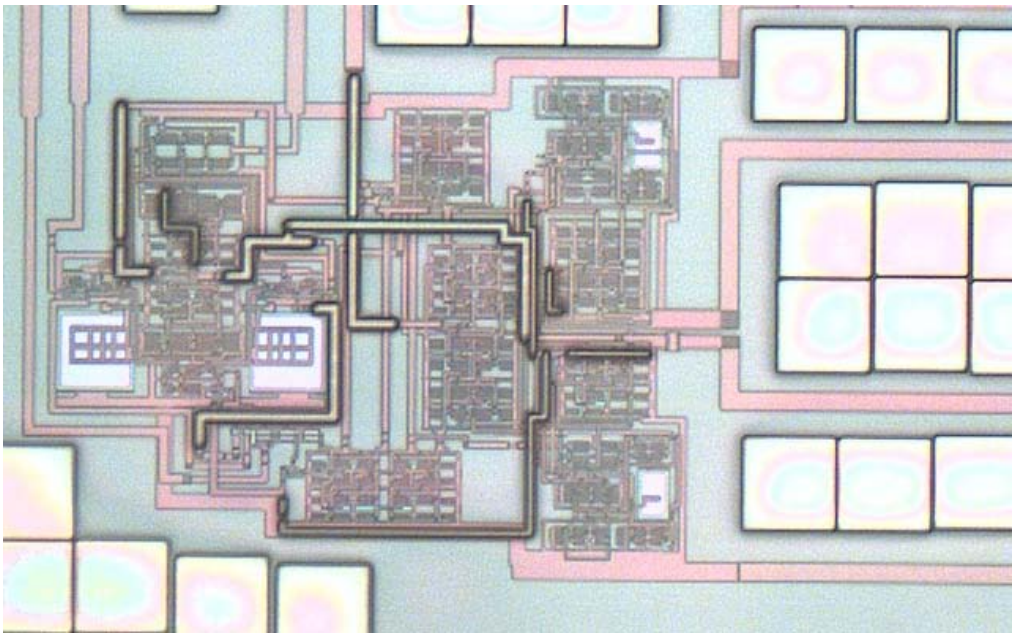


Figure 4.30 Die photomicrograph of the CMOS current amplifier

In the current amplifier, the offset error originates primarily from mismatch of the transistors used to create current mirrors and the input stage. Figure 4.32 shows the effectiveness of the offset cancellation scheme. Assuming that the bias current of 50µA flows in the input stage, the circuit is subjected to ±10% of this value as the input referred current offset. The first 25µs shows the output of the circuit during the offset cancellation phase and the second one demonstrates the timing response of the offset free circuit to the input signal. It is seen that the offset varying from -10mV to 14mV in the first phase is reduced to within 1.6mV or equivalently an input referred offset current of 0.87nA for the transresistance gain of 1.84MΩ. Figure 4.33 is the transient output voltage response of the transresistance amplifier to the desired input current signal with the amplitude and frequency of 10nA and 300kHz, respectively superimposed on offset currents of ±5µA, showing the effective offset cancellation and amplification at the first and second phases of operation. Figure 4.34 shows the measured output voltage transient response to a current pulse input with the amplitude of 1 µA. As can be seen, the output voltage of the transresistance amplifier settles to its final value in less than 12µsec.

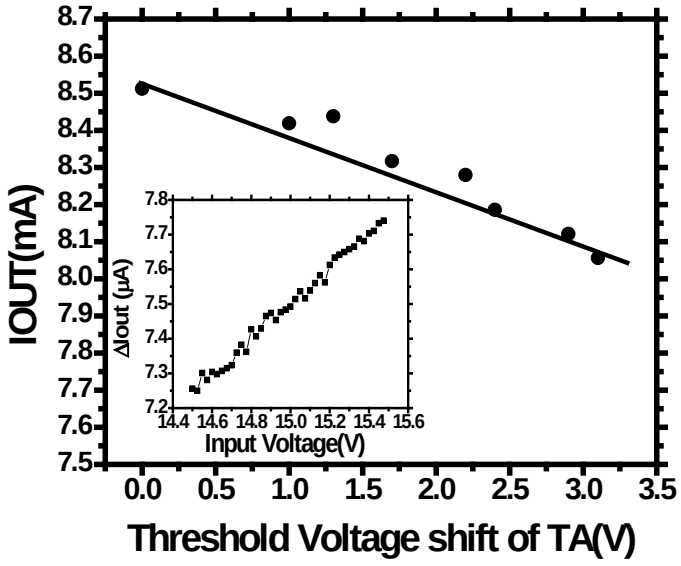


Figure 4.31 Measured output current as a function of TA threshold voltage shift; the dynamic range is shown in the insert.

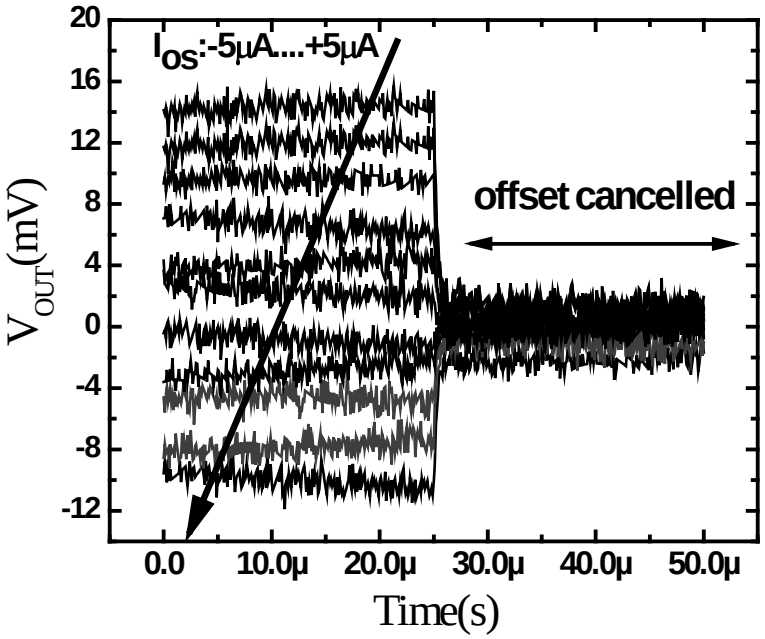


Figure 4.32 Measurement showing Offset-cancellation functionality for the input offset current ranging from -5μA to +5μA.

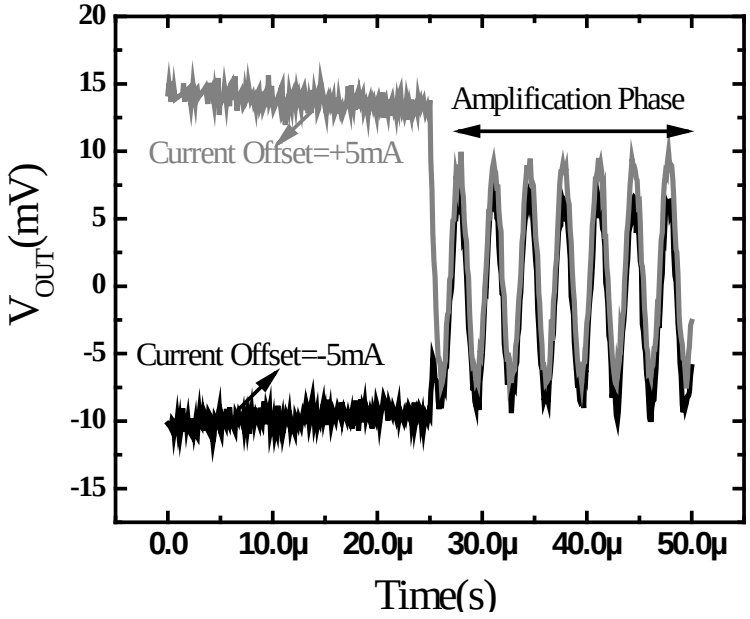


Figure 4.33 Output Voltage Measurement showing successful offset cancellation followed by amplification of the signal Iin=10nAsin(2π×300KHz×t).

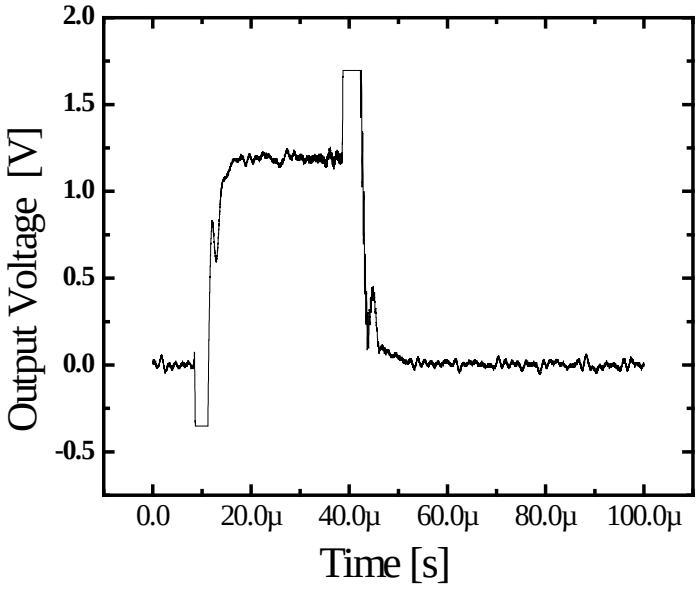


Figure 4.34 Measured Transient output response of the transresistance amplifier to a 1µA input current pulse.

4.8 High Gain Transresistance Amplifier with Double Sampling Capability

The drawback of the transresistance amplifier presented in the previous section is that the output of the transconductance stage is directly connected to the output node of the amplifier. This results in loading of the output and therefore potential decrease in the gain of the amplifier. To address this problem, the architecture is modified to that of Figure 4.35.

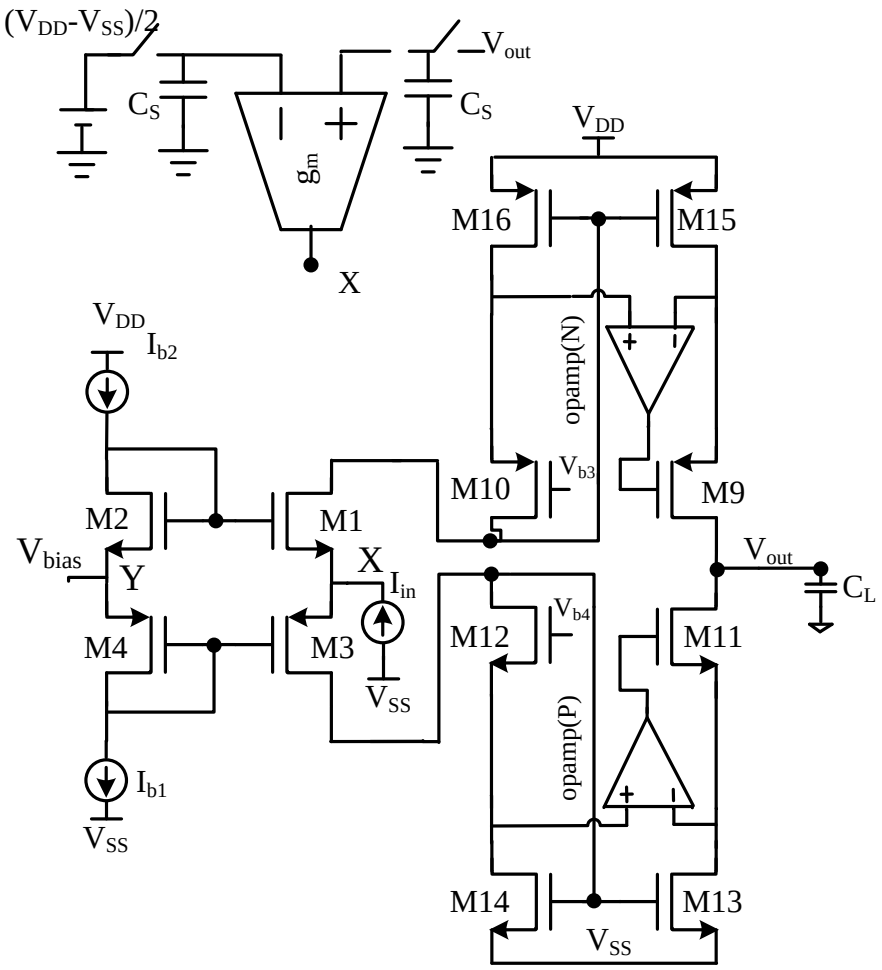


Figure 4.35 Modified transresistance amplifier with higher gain.

In this configuration the output of the transconductance stage, g_m, is connected to the input node, avoiding additional loading of the output node, V_{out} at lower frequencies. To verify the effectiveness of the proposed scheme, 0.18 μm CMOS process and CADENCE SPECTRE simulator are used. Figure 4.36 depicts the input impedance of the low impedance terminal versus frequency.

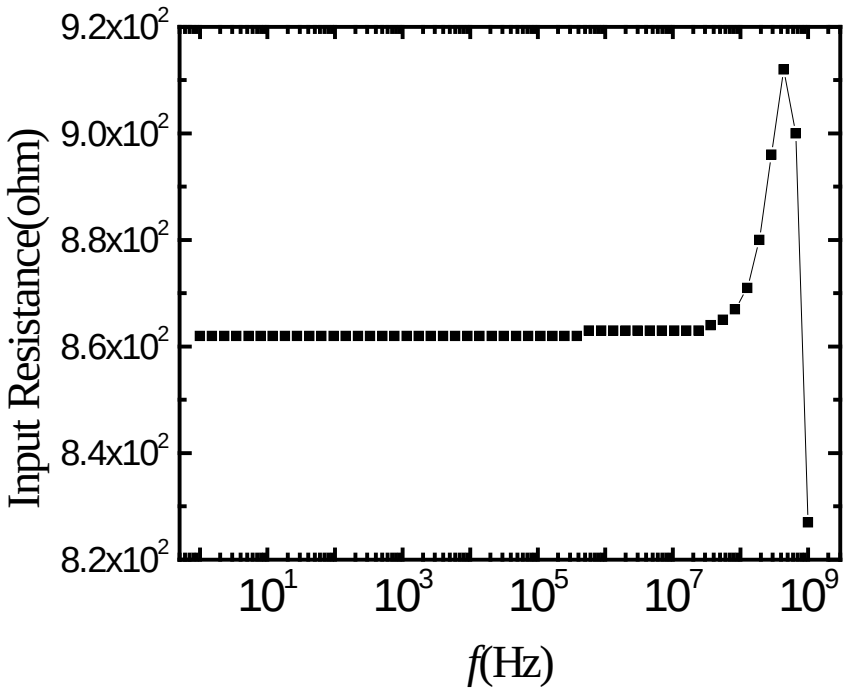


Figure 4.36 Input resistance of the transresistance amplifier versus frequency.

The input resistance is low enough to bypass the large capacitance associated with the long data line, making fast signal readout for real-time operations feasible. Two opamps in the design, opamp(N) and opamp(P) are used for boosting the output resistance and the gain of the amplifier [**41**]. The effect of varying the gain of these opamps on the transient behaviour of the output voltage is shown in Figure 4.37. The simulation result in Figure 4.37 shows the transient response in the output node to a 1nA current step in the input. The input step current occurs at 60µs point. The output resistance of the amplifier is directly proportional to the opamp gain. The only high impedance node of the transresistance circuit is the output node. Therefore, this node contributes the dominant pole of the circuit. For higher values of the opamp gain, the RC time constant associated with the output node increases linearly, resulting in longer transient response in the output. The feedback switch is turned off at 30µs. As can be seen in the figure, the effect of charge injection is negligible compared to the change caused by the input current data. The small change in the voltage of the output node, V_{OUT} is attributed to the fully differential architecture of the transresistance stage, g_m, which is expected to have good common mode rejection ration (CMRR) behaviour.

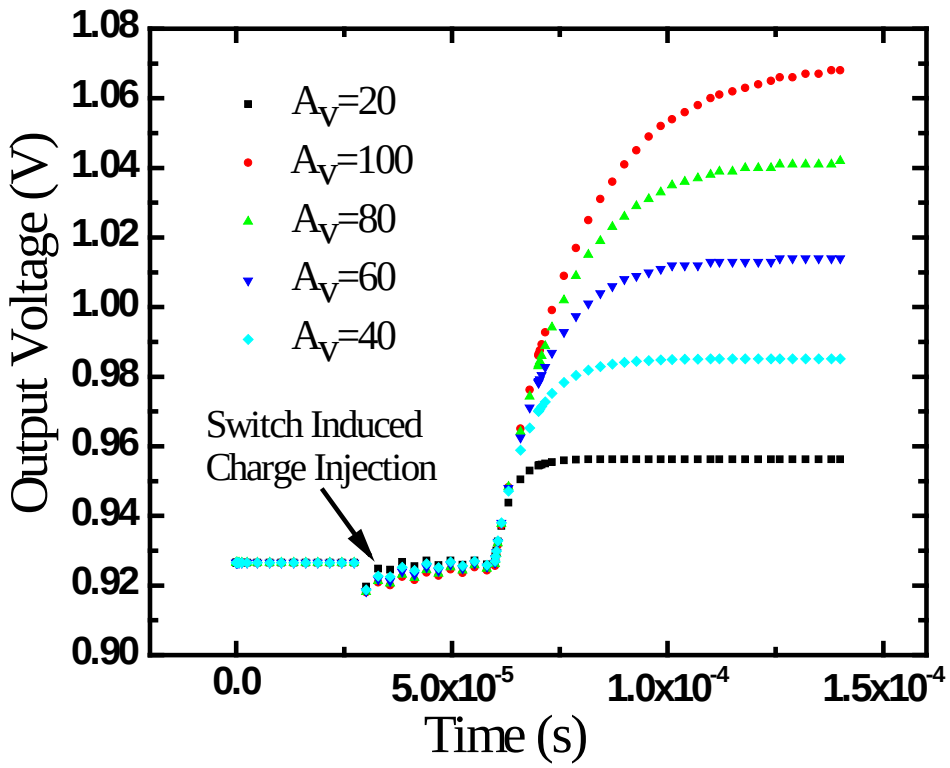


Figure 4.37 Transient response at the output of the current amplifier to the input current step at 60µs for different values of gain boosting opamp gain. The step amplitude of the input current pulse is 1nA representing the lower range of signal in fluoroscopy.

Figure 4.38 shows the transient response of the circuit to various input current pulses with different magnitudes. The input current pulse occurs at 60µs. The magnitude of the input current pulse represents the input x-ray signal. Here, it is assumed that for 0.1µR, 1µR and 10µR, the current step size is 1nA, 10nA and 100nA, respectively. The power spectral density of the input referred noise of the current amplifier circuit is shown in Figure 4.39. This data is later used for calculation of input refereed noise of the APS circuit. Figure 4.40 demonstrates the AC response of the current amplifier circuit to an AC input current source with the amplitude of 10nA.

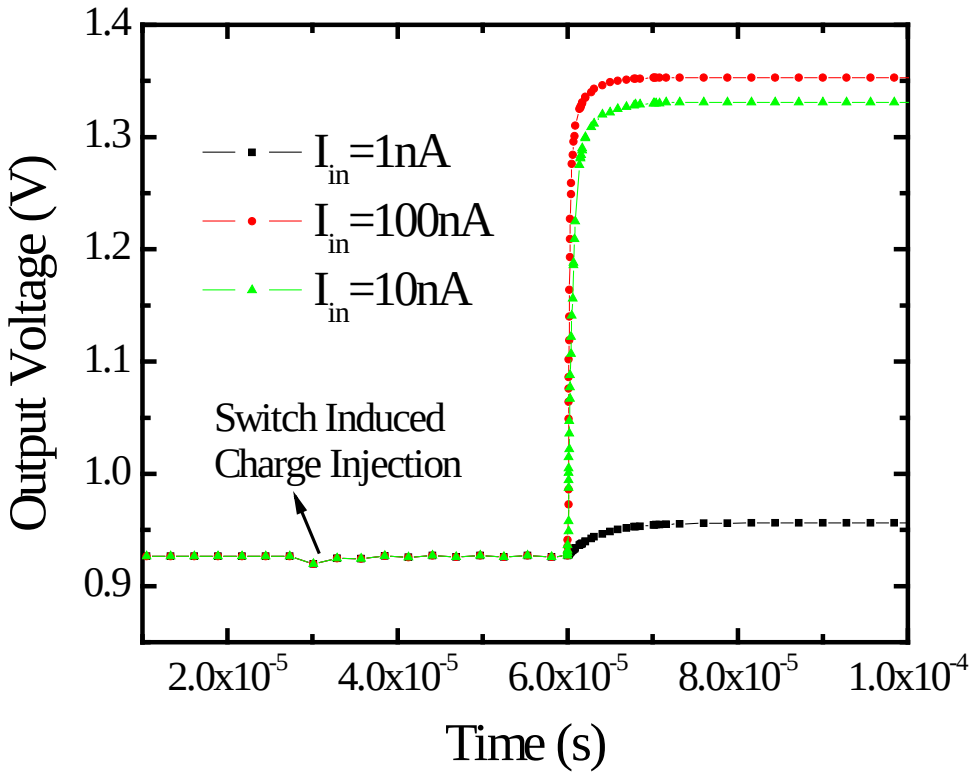


Figure 4.38 Transient response at the output of the current amplifier to the input current step occurring at 60µs for different values of input current step of 1nA, 10nA and 100nA representing 0.1µR, 1µR and 10µR, respectively, in fluoroscopy.

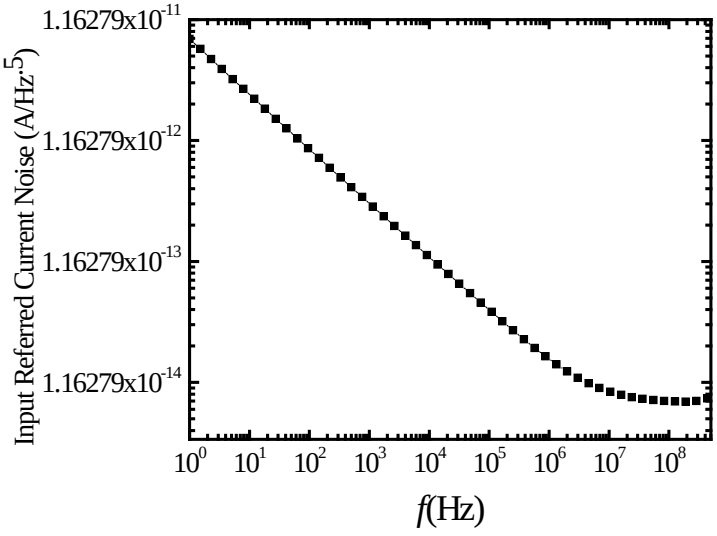


Figure 4.39 Input referred current noise density versus frequency of the current amplifier.

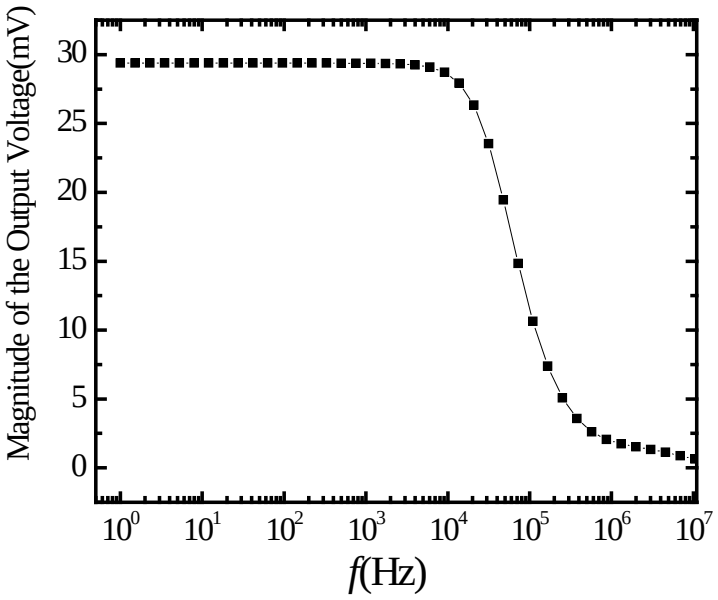


Figure 4.40 The output ac magnitude response of the current amplifier to an input ac current with the magnitude of 1nA. This graph shows that at low frequencies, the gain of the transresistance amplifier is about 30MΩ. This high gain enables the current amplifier to detect very small current signals of the APS caused by the minimum signal of the fluoroscopy.

4.9 Summary

In this chapter the off panel CMOS circuits required for proper operation of the APS pixel circuits in the flat panel imagers are proposed and implemented. The feedback based offset cancellation scheme employed in the transresistance amplifier decreases the input referred offset and noise to the levels acceptable for precise detection of the signals generated by on-pixel TFT amplifiers. The implemented CMOS transresistance amplifiers can successfully detect input current signals in the order of nano amps which correspond to lower range of fluoroscopic application. The signal readout can be achieved in less than 12μs making the scheme amenable towards real time medical imaging.

5 Detective Quantum Efficiency of Active Matrix Flat Panel Imagers

The detective quantum efficiency (DQE) is considered as the appropriate metric of imaging performance. This metric is used for evaluating the image quality in both direct and indirect active matrix flat panel imagers. Among various medical applications, fluoroscopy (real-time x-ray imaging) has the minimum input dosage range of operation and therefore, is the most challenging technology. The exposure rate in fluoroscopy is very low compared to other modalities such as chest radiography or mammography. Therefore the quality of the captured images is highly dependent and sensitive to the added noise in the imaging chain. To overcome this problem, one way is to increase the sensitivity of the x-ray photoconductor. Some of the potential photoconductors that can be used in direct conversion image detectors are a-Se, poly-HgI_2, and poly-CdZnTe) [**55**], [**56**], [**57**]. The incoming x-ray photons interact with the photoconductor or the phosphor layer. A fraction of the fluorescent or scattered x-rays escape the photoconductor volume resulting in reduction in absorbed energy per attenuated x-ray photon. This effect reduces the number of generated electron-hole pairs known as the conversion gain and therefore reduces the DQE. Those scattered x-ray photons that are reabsorb in the photoconductor volume, contribute to the signal and the blurring effect of the image. Most of the K-fluorescent photons are reabsorbed inside the photoconductor volume [**58**]. Since the reabsorption probability of the K-fluorescent photon depends on the location of k- fluorescent photon creation, this phenomenon causes variation of the conversion gain across the photoconductor area. The conversion gain and charge collection are dependent on the depth of the x-ray interaction. The zero spatial frequency detective quantum efficiency, i.e. DQE(0) = DQE(f) at f = 0, of a-Se as the photoconductive detector and the APS as the pixel amplifier for a fluoroscopic application is analysed in detail as a function of varying amounts of input signal exposure and added electronic noise. It is found that to maximize the value of DQE(0) for a specific value of electronic noise and input exposure, there is an optimum value for the photoconductor thickness. The actual broad x-ray spectrum emitted from a typical x-ray tube is approximated by a monoenergetic x-ray beam having the same average photon energy. This monoenergetix x-ray beam is used to calculate the DQE of an a-Se coated large area imager. The

cascaded linear system model of DQE(0) is applied to a-Se based detectors for fluoroscopic applications with PPS and APS as the pixel level circuits to study and compare their DQE(0) performances.

5.1 DQE(0) Model

In order to calculate the DQE(0) of a flat panel imager, the model in Figure 5.1 is used in which the photoconductor material has been sandwiched between two large area parallel plate electrodes. A bias voltage has been applied across the two terminals to establish an electric field *F* between the two electrodes. This electric field separates the electrons and holes generated by x-ray interaction and causes them to drift towards top and bottom terminals depending on the polarity of the applied bias.

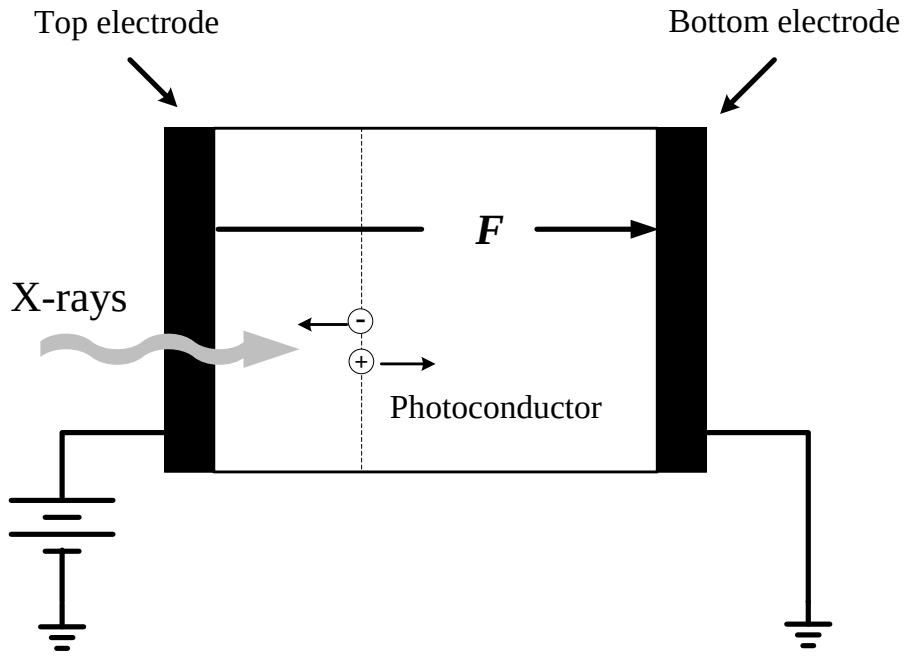


Figure 5.1 The photoconductor is sandwiched between two large area parallel plate electrodes. As a result of x-ray interaction, an electron and a hole are generated at the location x′ from the left large area electrode. Due to the established electric field, the charge carriers of opposite polarities are drifting towards opposite electrodes.

For a practical x-ray imaging detector, the value of DQE is degraded as the signal and noise propagate through different stages of the detector. Detective quantum efficiency of an imaging

detector is defined as the ratio of the square of the signal-to-noise ratio at the output of the imager over the square of the signal to noise ratio at the input of the imager.

$$DQE(f) = \frac{SNR_{out}}{SNR_{in}} \tag{5.1}$$

DQE is generally a function of spatial frequency and provides information on the overall signal and noise performance of the imaging detector [**59**]. The spatial frequency dependent DQE, DQE(f), is a generally accepted and powerful criteria to compare the performance of various detectors with different structure parameters. In the indirect case, CsI scintillators as the x-ray converter and a-Si TFT/photodiode arrays are used [**60**]. The interacting x-rays undergo an exponential attenuation across the thickness of the photoconductor. The probability density of interaction of an attenuated photon at a distance x′ from the radiation receiving electrode is given by,

$$p_{\acute{x}}(E, \acute{x}) = \begin{cases} \dfrac{\alpha e^{-\alpha \acute{x}}}{\eta}, & 0 \le \acute{x} \le L \\ 0, & \text{elsewhere} \end{cases} \tag{5.2}$$

Here, E is the energy of the incident x-ray photon, α(E) is the energy dependent linear attenuation coefficient and L is the thickness of the photoconductor layer. The quantum efficiency, $\eta(E)$, is a function of the incident x-ray photon and is defined as,

$$\eta(E) = 1 - e^{-\alpha(E) d_{Se}} \tag{5.3}$$

5.1.1 Cascaded Linear System Model

Many researchers have used the cascaded linear system model to characterize and quantify the imaging performance and image quality of various imager systems. The signal and noise transfer through an x-ray image detector is a complex process. In this model the entire imager is represented by a chain of individual simple and independent stages. The input and output to each stage is usually a spatial distribution of quanta. Depending on the specific elementary stage, the quanta can be x-ray distribution, light photons or charge carriers including electrons and holes. Figure 5.2 shows the linear cascaded system model used for the calculation of DQE(0) of a direct imager with photoconductive detector as the x-ray sensor. The cascaded system includes four

stages: (1) X-ray attenuation, (2) the generation of charge carriers (conversion gain), (3) charge collection, (4) the addition of electronic noise.

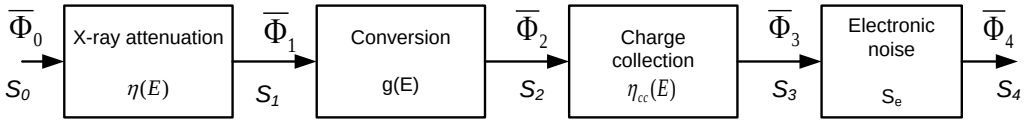


Figure 5.2 The flow chart of the linear cascaded system model showing the propagation of signal and noise through the main four stages of the x-ray image detector.

In this model, the spatial dependence of signals and noise are not considered. Therefore, this model can only be used in the calculation of zero spatial frequency detective quantum efficiency DQE (f = 0). DQE(0) represents signal quality degradation due to the signal and noise transfer characteristics of the system without considering the effect of signal spreading.

Each stage of an imaging detector may have one of these three types of processes:

1- An amplification process.
2- A stochastic blurring process
3- A deterministic blurring process.

If stage i represents amplification in the signal with the gain g_i and gain variance, σ_{gi}, the output mean number of quanta per unit area and NPS For stage i with amplification only, can be written as

$$\begin{aligned} \overline{\Phi}_i(E,x) &= \bar{g}_i(E,x)\overline{\Phi}_{i-1}(E,x) \\ S_{N_i}(E,x) &= \bar{g}_i^2(E,x)S_{N_{i-1}}(E,x) + \sigma_{g_i}^2(E,x)\overline{\Phi}_{i-1}(E,x) \end{aligned} \tag{5.4}$$

Here, E is the energy of the incident x-ray photon, $\overline{\Phi}_{i-1}(E,x)$ and $S_{N_{i-1}}(E,x)$ are the mean number of quanta and the NPS incident on stage i, respectively, and $\bar{g}_i(E,x)$ and $\sigma_{g_i}^2(E,x)$ are the mean gain and variance of the gain of the i_{th} stage. The amplification stage is stochastic in the sense that there is noise associated with the value of the gain and the gain value is not quite deterministic. The stochastic nature of the gain stage causes the noise of the quanta to increase in two different ways. First, the input power spectrum of the noise is amplified by the gain of the gain stage, and second, the variation in the gain of the gain stage introduces another source of noise in the noise power spectrum of the output. In the following, based on the physical nature of

each stage, the mean gain and the variance of gain of individual stages are discussed and quantified.

1-X-ray attenuation

The interaction of an incident x-ray photon with the photoconductor detector is a binary process in the sense that it interacts with the detector with probability g_1, or does not interact with probability 1-g_1. Here g_1 is equal to the quantum efficiency η of the detector [**61**]. The variance of a binomial process is given by,

$$\sigma_{g1}^2 = \bar{g}_1(1 - \bar{g}_1) = \eta(1 - \eta) \tag{5.5}$$

2- Conversion gain

The second stage represents the conversion from x-ray quanta to charge carriers. The mean conversion gain equals the mean number of free electron-hole pairs (EHPs) generated as a result of x-ray of energy *E* interacting at the distance x from the radiation receiving electrode,

$$\bar{g}_2(E, x) = \frac{E_{ab}(E, x)}{W_{\pm}} \tag{5.6}$$

Here, $W_{\pm}$ is the energy required to generate an electron-hole pair inside the photoconductor and $E_{ab}(E, x)$ is the average absorbed energy per x-ray photon of energy *E*, interacting at distance x from the radiation receiving electrode.

There is variation associated with the conversion gain rising from the statistical nature of the number of generated electron-hole pairs per interacting x-ray photon. Assuming that the mean number of free charge carriers generated per x-ray photon at location x obeys the Poisson distribution and the K-fluorescence is negligible, the variance of the depth dependent conversion gain, $\sigma_{g2}^2(\mathrm{E}, \mathrm{x}) = \bar{\mathrm{g}}_2(\mathrm{E}, \mathrm{x})$. The K-fluorescence reabsorption is another source of conversion gain fluctuation. The effect of fluctuation in the conversion gain due to K-fluorescence reabsorption is quite noticeable and maximized just above the K-edge (12.7 keV in the case of a-Se) of the photoconductor. However, as the energy of the incident x-ray photon becomes larger compared to the K-edge energy, this source of gain fluctuation becomes negligible [**62**]. For fluoroscopic

and chest radiographic applications, the x-ray spectrum is 70 kVp and 120 kVp, respectively. Therefore, the mean energy of the x-ray beam is much higher compared to the K-edge of a-Se and the effect of K-fluorescence on gain fluctuations can be neglected, i.e.:

$$\sigma_{g2}^2(E,x) = \bar{g}_2(E,x) \tag{5.7}$$

3-Charge collection

If an EHP is generated at the location x from the radiation receiving electrode, under the influence of the applied electric field, the carriers will drift toward opposite electrodes. Neglecting carrier diffusion and bulk recombination, the average charge collection efficiency, $\bar{g}_3(x)$, at the electrodes can be described by the Hecht charge collection efficiency formula given by,

$$\bar{g}_3(x) = \tau_t\left(1 - e^{-\frac{x}{\tau_t}}\right) + \tau_b\left(1 - e^{-\frac{1-x}{\tau_b}}\right) \tag{5.8}$$

Here it is assumed the EHP is initially generated at location x from the radiation receiving electrode. In the above formula, $\tau_t = \mu_t T_t F/L$, $\tau_b = \mu_b T_b F/L$ and μ is the drift mobility of the carriers and τ' is the lifetime (the time that a carrier can move on average before getting trapped in the deep trapping centers of the photoconductor) of the charge carriers. The schubweg parameter ($\mu\tau' F$) is the average distance a carrier drifts before becoming trapped in the deep trapping centers. The subscript t and b refer to the carriers drifting to the top or bottom electrodes, respectively. In the case of applying a positive bias to the radiation receiving electrode, the subscript t represents electrons (e) and b represents holes (h). It is shown that if random trapping of the drifting charge carriers is considered in the charge collection efficiency stage, the variance in the gain is given by [**63**],

$$\sigma_{g3}^2(x) = \tau_t^2 + \tau_b^2 - \tau_t^2 e^{-\frac{2x}{\tau_t}} - \tau_b^2 e^{-\frac{2(1-x)}{\tau_b}} - 2\tau_t x e^{-\frac{x}{\tau_t}} - 2\tau_b(1-x)e^{-\frac{(1-x)}{\tau_b}} \tag{5.9}$$

4-Addition of electronic noise

During the readout mode of operation, the electronic noise power originated from the photoconductor sensor, the TFT readout circuit under each pixel, the data and gate line as well as the external CMOS readout and gate driver circuits will be added to the total noise power. Different sources of noise are independent [**64**] and consequently, the total noise power can be calculated as the sum of the noise powers of the different noise sources. Here, the DQE(0) for the case of PPS is calculated and the results are compared with that of the APS structure.

5.2 Results and Discussions

Here, DQE(0) is calculated for a direct detector with a-Se as the photoconductor. The incoming x-ray beam is assumed to be monoenergetic with the energy equal to the average of a typical fluoroscopic beam. The expected signal $\overline{\Phi}_3$ and quantum noise S_3 are calculated at the output of the third stage. The noise value of the PPS and APS designs calculated in the noise section of the thesis are included to demonstrate the significance of the APS design in improving DQE(0) particularly in the fluoroscopic input signal range. The x-ray beam spectrum used for fluoroscopic applications is usually 70 kVp. The pixel area is A = 150 μm × 150 μm in state of the art fluoroscopic panels. Under each 150 μm × 150 μm pixel there is a storage cap acitor and a TFT pixel circuit that can be a single TFT acting as a switch in the case of PPS design or a number of TFTs with one of them usually acting as an amplifier and the rest of them acting as switches in the case of APS design. The geometrical fill factor is usually about 65-80 %. Because of the bending of the electric fields close to the pixel electrodes, it has been shown that the effective fill factor increases to 100% in the case of selenium based detectors [**65**]. Consequently, the entire pixel area can be used for radiation detection. The mobilities and lifetimes of carriers are taken from the literature and assume to be $\mu_h \approx 0.12$ cm^2/Vs, $\mu_e \approx 0.003$ cm^2/Vs, $\tau'_h \approx 50$ μs and $\tau'_e \approx 200$ μs for drifting holes and electrodes, respectively. It is shown that for the x-ray spectrum of a 70 kVp tungsten anode naked x-ray tube with 23.5 mm Al acting as a filter (RQA5 beam quality of the IEC1267 standard), the average photon energy E_{av} is 52.1 keV. In the

fluoroscopic application, the incident x-ray exposure changes from 0.1 μR to 10 μR, where 1 μR is the mean value for the exposure range [**2**]. The value for additive electronic noise, for direct conversion flat-panel imaging sensors is typically in the range of 1000 to 3000 electrons per pixel in the case of PPS and 250 to 500 electrons in the case of APS pixel circuits. The energy required for creation of a single electron-hole-pair, $W_{\pm}$ in a-Se, is a strong function of the electric field [**66**]. It is shown that $W_{\pm}$ also has a weak dependence on the incoming x-ray energy [**67**]. The value of $W_{\pm}$ decreases with increasing electric field and higher photon energies. For an x-ray beam with the average energy of 52.1 keV , $W_{\pm} \approx 44$ eV at the electric field of F = 10 V/μm [**66**]. Figure 5.3 demonstrates the quantum efficiency versus the detector thickness. It is assumed that the amount of electric field is kept constant at F = 10 V/μm. Therefore, as the thickness is increased, the biased voltage across the detectors is also linearly increased correspondingly. The x-ray absorption is not uniform and the intensity is reduced exponentially across the detector. Although both types of charge carriers (electrons and holes) contribute to the final charge collection efficiency, the dominant contribution comes from the charges that have the same polarity as the bias applied to the radiation receiving electrode, i.e. electrons and holes for negative and positive bias, respectively. Since the mobility-lifetime for holes is much better in a-Se compared to that of electrons, the charge collection efficiency is expected to be much higher when positive bias is applied to the top electrode. Figure 5.4 shows the charge collection efficiency as a function of the thickness in a-Se photoconductor detector. It is assumed that the amount of electric field is kept constant at F = 10 V/μm.

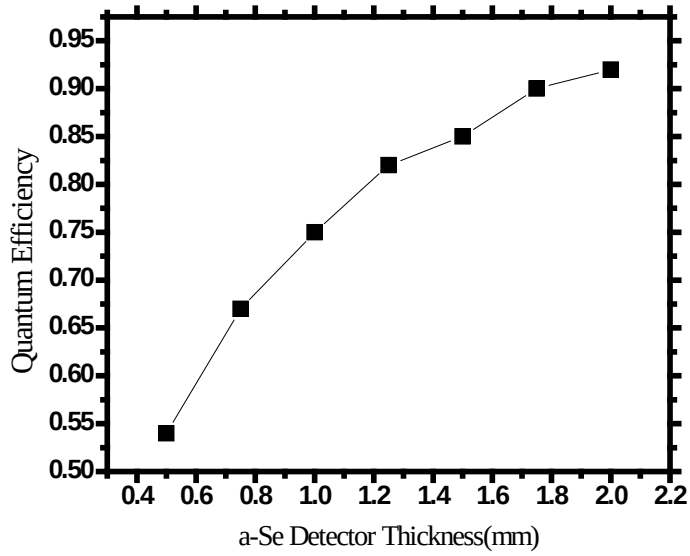


Figure 5.3 Quantum efficiency versus a-Se detector thickness with the electric field of 10V/μm

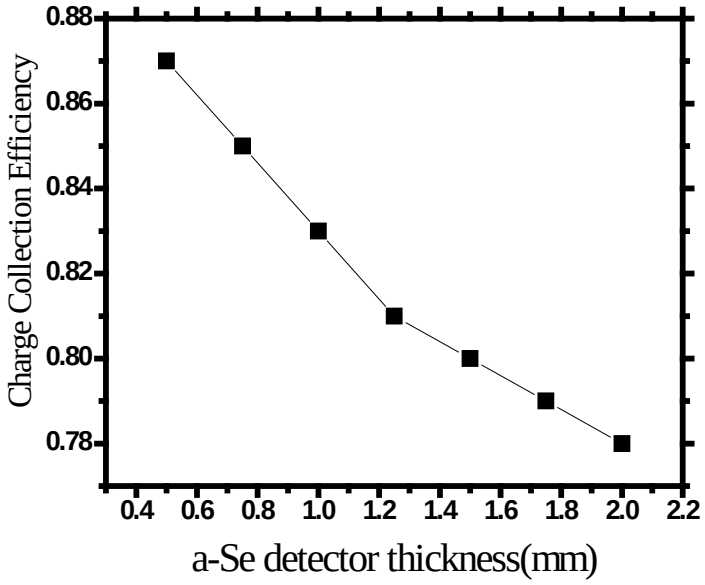


Figure 5.4 Quantum efficiency versus a-Se detector thickness with the electric field of 10V/μm

DQE(0) for the APS circuit was computed to be 0.4 at 0.1 μR for digital fluoroscopy. The best achieved input referred noise was around 380 for the a-Si APS circuit. Using an overlying a-Se direct detector, the APS pixels improve the DQE by 18% at 0.1 μR compared to state-of-the-art PPS pixels. As such, they can enable a variety of electronic noise limited digital x-ray imaging modalities without resorting to newer detectors (e.g. PbO) or backplane readout electronics (e.g.

CMOS). Figure 5.5 shows the calculated DQE(0) versus the input exposure range for the APS architecture with input referred noise of 380 electrons. The effect of input referred noise on the calculated DQE is shown in Figure 5.6.

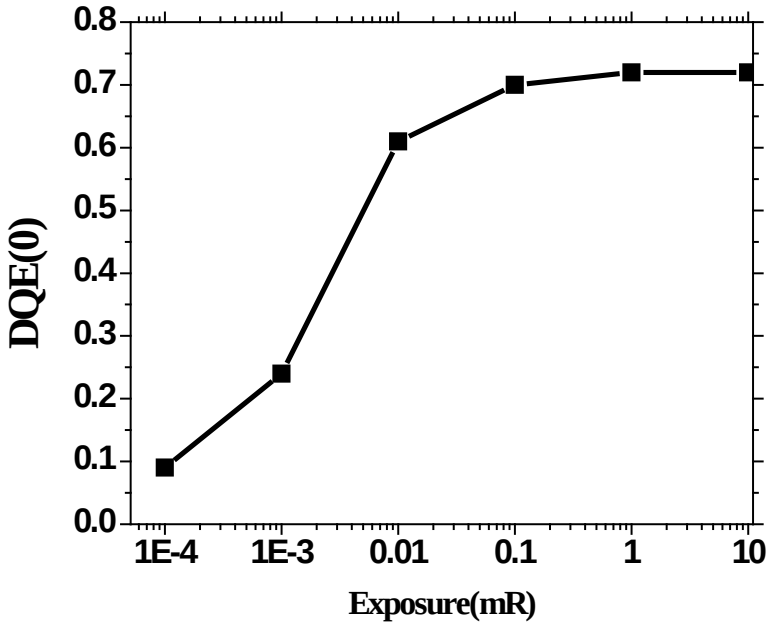


Figure 5.5 DQE(0) versus the input exposure range for the APS architecture with input referred noise of 380 electrons.

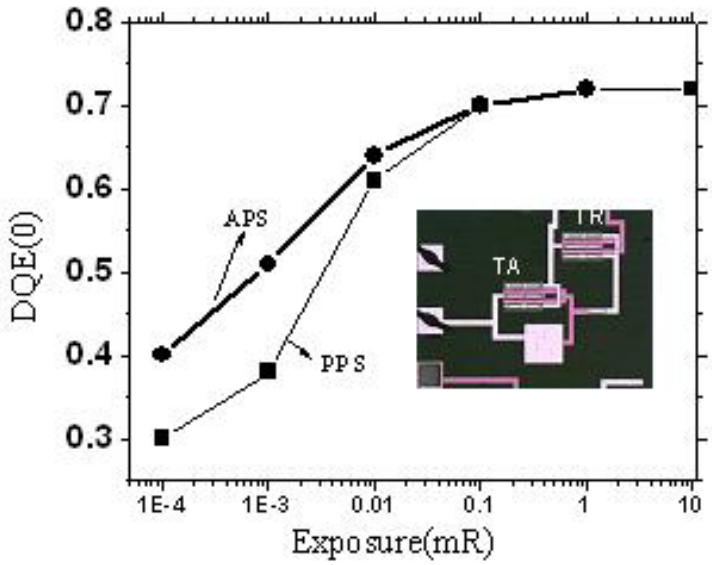


Figure 5.6 DQE(0) versus exposure, for the case of PPS and APS structures

Figure 5.7 shows the DQE as a function of detector thickness under the operating condition of constant electric field at F=10 V/μm. Here positive bias voltage is applied to the top electrode. The input x-ray signal with 1 μR exposure is applied to the detector. Here the x-ray beam is assumed to be monoenergetic with the x-ray photon energy equal to 52.1 keV which is appropriate for fluoroscopy. It is seen that electronic noise has a considerable effect on the amount of detective quantum efficiency, particularly at lower exposure levels. For the typical values of mobility and lifetime in a-Se for both types of carriers, the mobility-lifetime product (carrier range) of holes is longer than that of electrons. On the other hand, x-ray is absorbed exponentially inside the detector and its absorption is not uniform across the detector. Therefore, the type of carrier that has the same polarity as the bias applied on the radiation receiving electrode has the most contribution to the charge collection efficiency [**63**], [**68**]. Since the carrier range ($\mu\tau'$) for holes in a-Se is higher compared to that of electrons, the charge collection efficiency for positive bias is higher than for negative bias. Positive bias also results in smaller effective noise originated from stochastic charge collection mechanism [**69**], [**70**]. Therefore, applying positive bias improves the DQE because of higher charge collection efficiency and lower noise associated with charge trapping.

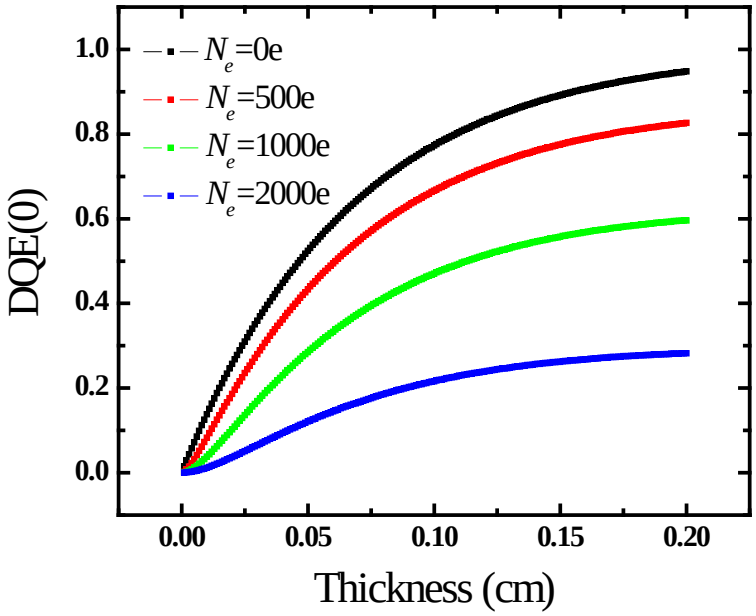


Figure 5.7 DQE(0) versus detector thickness at a constant electric field of 10 V/μm for positive bias. The a-Se detector is exposed to 1 μR exposure at an x-ray photon energy of 52.1 keV (monoenergetic beam).

Increasing the electronic noise has a drastic effect on the value of DQE as shown in Figure 5.7. Using the linear cascaded model, the calculated value of DQE(0) for N_e = 0, L = 1 mm and X = 0.1 μR, is DQE≈ 0.773, whereas for N_e = 2000e the DQE≈ 0.216 (reduces by 72.9%). Figure 5.8 shows the quantum efficiency using the average energy (52.1 keV) of the x-ray spectrum (70 kVp) when positive bias is applied to the radiation receiving electrode. The average photon energy E_{av} is 52.12 keV for 70 kVp x-ray spectrum with 23.5 mm added Al filtration. There is no significant difference in the quantum efficiency [**71**].

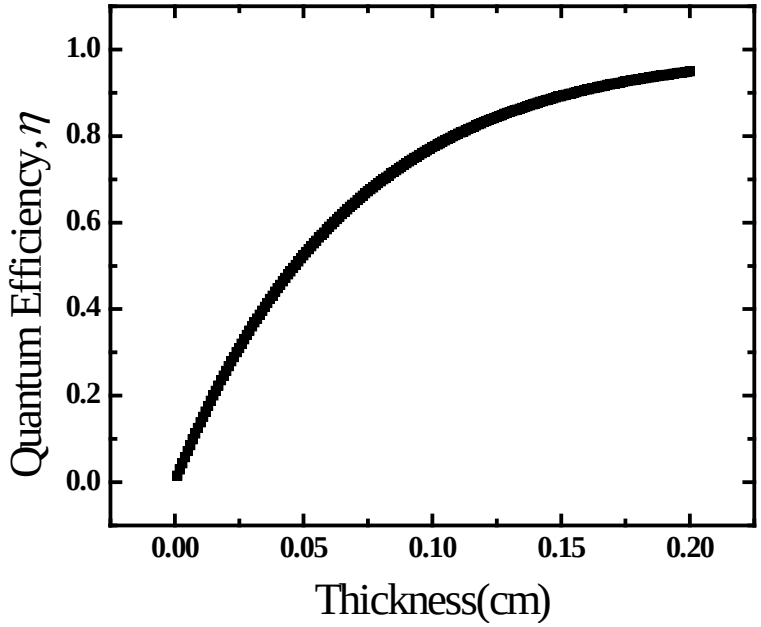


Figure 5.8 Calculation of quantum efficiency using the average energy (52.1 keV) for positive bias.

Figure 5.9 shows the effect of electronic noise and charge collection on the DQE as a function of detector thickness when a constant bias voltage of 10 kV is applied to the top electrode across the a-Se detector and the detector is exposed to a monoenergetic x-ray beam with photon energy equal to 52.1 keV. Here, the x-ray exposure is set to be the minimum value of the fluoroscopic range or 0.1 μR. At L = 1 mm and Ne = 0, the DQE≈ 0.773 for positive bias, whereas for Ne = 2000 e, the DQE ≈ 0.237 for positive bias. Contrary to the previous case, here the electric field is not assumed to be constant. Instead a constant voltage equal to 10 kV is applied to the radiation receiving electrode. Since the electric field is inversely proportional to the thickness, it decreases with increasing the detector thickness. This reduction in the electric field modifies the conversion

gain and charge collection in the detector. The value of W± increases with decreasing electric field. The conversion gain is inversely proportional to W±. There is a compromise between higher quantum efficiency (achieved with larger detector thickness), higher charge collection efficiency (achieved with smaller detector thickness), and higher conversion gain (achieved with smaller detector thickness). Therefore, in the case of constant bias, for each specific value for the electronic noise and incoming x-ray exposure, there is an optimum value for the chosen detector thickness. The need for the optimum detector thickness is more significant especially for higher electronic noise as evident in Figure 5.9.

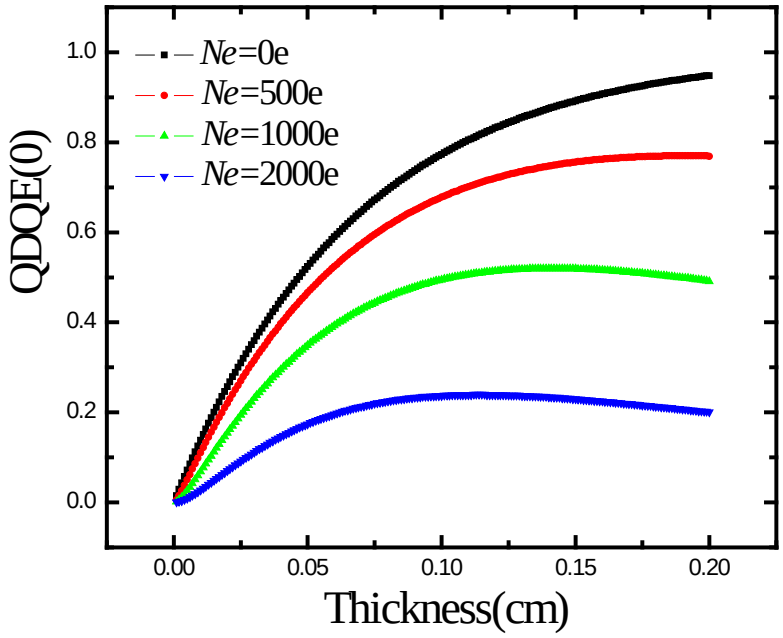


Figure 5.9 DQE(0) versus detector thickness with the constant bias value of 10 kV applied to the radiation receiving electrode and a monoenergetic x-ray beam of photon energy E = 52.1 keV.

Figure 5.10 exhibits DQE(0) versus detector thickness for various levels of x-ray exposure (*X*) in the fluoroscopic range of operation for a monoenergetic x-ray beam of photon energy *E* = 52.1keV. As the x-ray exposure increases, the DQE improves. The reason is each pixel in the array receives more photons and the relative significance of electronic noise is reduced.

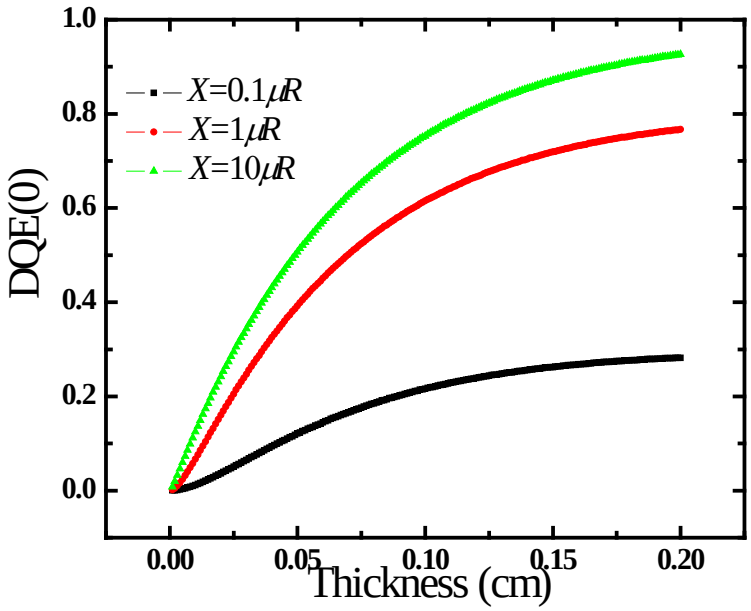


Figure 5.10 DQE(0) versus detector thickness for various levels of x-ray exposure (X) in the fluoroscopic range of operation for a monoenergetic x-ray beam of photon energy E = 52.1 keV.

Figure 5.11 demonstrates a 3-D plot of the DQE versus L and N_e at a constant electric field of 10 V/μm for positive bias. The *a*-Se detector is exposed to 1 μR exposure at an x-ray photon energy of 52.1 keV (monoenergetic beam). For every level of electronic noise, there exists a DQE peak and the DQE peak shifts towards higher L, as N_e gets lower.

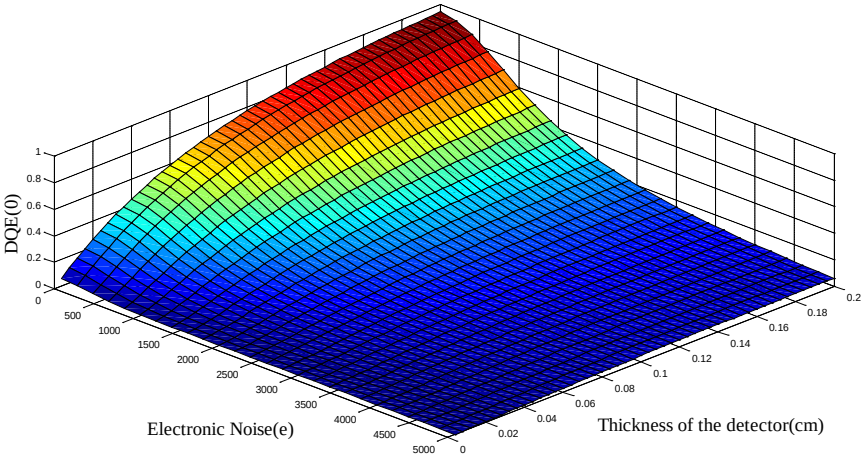


Figure 5.11 DQE(0) versus detector thickness (L) and electronic noise (Ne) at a constant electric field of 10 V/μm for positive bias. The a-Se detector is exposed to 1 μR exposure at an x-ray photon energy of 52.1 keV (monoenergetic beam).

5.3 Summary

A cascaded linear system model has been considered for the calculation of the DQE(0) of a direct conversion x-ray image detector having a-Se as the photoconductor and operating in fluoroscopic application. In the calculation of DQE(0), incomplete charge collection and x-ray interaction depth dependent conversion gain and charge collection are considered. Using this model, the DQE(0) of *a*-Se detectors for fluoroscopic applications has been examined in detail as a function of electronic noise, x-ray exposure and detector thickness. Calculations reveal that the amount of the electronic noise has a considerable effect on the total value of DQE(0). As a result, by employing APS architectures as presented in chapter 3, higher DQE(0) and equivalently higher image quality of the detector can be achieved.

6 Conclusion and Contributions

Active matrix flat panel technology based on a-Si:H TFTs has been extensively applied to digital x-ray diagnostic medical imaging. The technology has several desirable attributes such as uniformity, low temperature fabrication and low capital infrastructure costs. Despite major shortcomings in the characteristics of the TFT, in particular, its instability caused by voltage or thermal stress and low mobility, amorphous silicon TFT technology remains the primary low-cost solution for use in large area medical imagers. Various circuit techniques can be used to overcome the instability related problems and make this technology advantageous for large area medical imagers. The solutions must be compatible with the range of voltages and currents met in the a-Si:H, a-Se as well as CMOS technologies, simple to implement in large area imager arrays and capable of compensating for instabilities associated with a-Si:H technology.

In this thesis we have introduced a new generation of current programmed active pixel sensor readout circuits, particularly for use in low noise and real time as well as dual mode imaging applications. In these designs, the sensitivity of the APS gain from different pixels across the array to spatial and temporal variations in TFT parameters is suppressed significantly by using fixed current sources outside the flat panel imager to program the APS circuits under each pixel.

We have also introduced novel dual mode APS circuits in which the array can be used for both low dose fluoroscopic and high dose, radiographic applications. To reduce the number of TFT transistors per pixel and eliminate the need for a separate switched addressing transistor, the amplifier/driver TFT is itself switched ON and OFF.

In the APS circuits presented in this thesis, during readout, the amplifying TFTs are biased in the common-source configuration as opposed to the usual source follower configuration. Using this biasing scheme, the signal-to-noise ratio (SNR) of the detector array can be improved by virtue of both, an increase in the pixel amplification gain and a reduction in the input referred noise.

An alternate design for the APS was investigated in which the current during the readout phase is scaled up and increased compared to the current flowing into the APS during the programming phase. This design can be used to reduce the power consumption of the array and avoid heating the x-ray sensor. It is shown that the gain of the current scaling APS is scaled up with a factor that is purely a function of the APS physical parameters and therefore the gain is stable in the presence of variations in the electrical characteristics of the comprising TFTs including threshold voltage shift.

To compensate for the variations in the electrical properties of the TFTs, an alternative way is to use voltage programmed APS in which the compensation for shift in the threshold voltage is achieved by on-pixel measuring of the V_T, and adding the measured value to a fix, reset. This idea was investigated and implemented in one of the APS designs proposed in this thesis. This design has a key advantage over the current programmed APS designs because it can be operated by regular gate drivers used in the conventional PPS arrays in contrast to the other current programmed architectures that require off-panel current sources as their biasing drivers. The voltage programmed design can be incorporated more easily into the existing technology of flat panel detectors.

Different active pixel sensor designs presented in this thesis were successfully implemented in the form of test arrays or individual pixel circuits using the in-house a-Si:H technology in university of waterloo. Various tests and measurements including, gain, transient, life-time and noise measurements were conducted on the fabricated test pixels. The measurements and measurement based calculations show that the active pixel sensors, coupled with a low capacitance can meet even the stringent requirements of low noise, digital fluoroscopy (less than 1000 input referred noise electrons). The presented results provide the impetus to expedite the development of large area a-Si:H based detectors with APS as the amplifying element in each pixel.

High degree of accuracy and matching among the output current of different current sources can be achieved using CMOS technology. Depending on the nature of the output signal from the APS circuits (i.e. current and voltage in the case of current mode or voltage mode APS,

respectively) different external readout circuits can be implemented and used. In the case of current mode APS, the output signal from each APS is in the form of current flowing from that particular pixel to the output of the flat panel array. Using charge amplifier or transresistance amplifier enables us to have fast readout by mitigating the effect of large capacitance associated with the data line through the small impedance of their low resistance input terminal. In the case of charge amplifier, the gain provide by the amplifier circuit is directly proportional to the integration time whereas, the gain of the current amplifier is independent of the integration time. Therefore, using the current amplifier results in faster signal readout which can lead to larger imagers with higher frame rate readout operation. In this thesis, several current amplifiers are designed and implemented using CMOS technology. The typical bias current of the APS pixels is in the order of several micro amps whereas the signal current caused by x-ray irradiation in low dose applications such as fluoroscopy can be as low as several nano amps. Therefore, directly feeding the output current of the APS into a charge amplifier or high gain current amplifier results in saturation of the output of these readout circuits. The implemented current amplifiers have the capability of saving the bias current and subtracting the captured value from the total current. It is demonstrated that with this scheme, small current values in the range of nano amp can be successfully amplified and detected in the output of the imager panel.

The original contributions of the research presented in this thesis to the field of large area digital imaging are listed below:

Design and Implementation of Current Programmed Active Pixel Sensor Architectures:

- Different current programmed, current output APS architectures to meet various imager requirements including uniformity, low noise, high speed, dual mode (fluoroscopy and radiography) and low power applications.

Design and Implementation of Voltage Programmed Active Pixel Sensor Architecture:

- This pixel circuit compensates for variations in the electrical characteristics of the TFTs across the array and versus time. At the same time can be incorporated into the standard driving methods used for ubiquitous PPS design.

Design and Implementation of CMOS off-panel current sources and off-panel current amplifiers for fast programming and readout of each APS in the array:

- The current mode amplifiers are capable of operation the correlated double sampling operation to reduce the low frequency noise of the TFTs, the data lime as well as the noise of the amplifier. They are high gain to be able to detect current signals in the order of few nano-amps corresponding to the lower range of fluoroscopy.

Appendix A

Mask Layouts

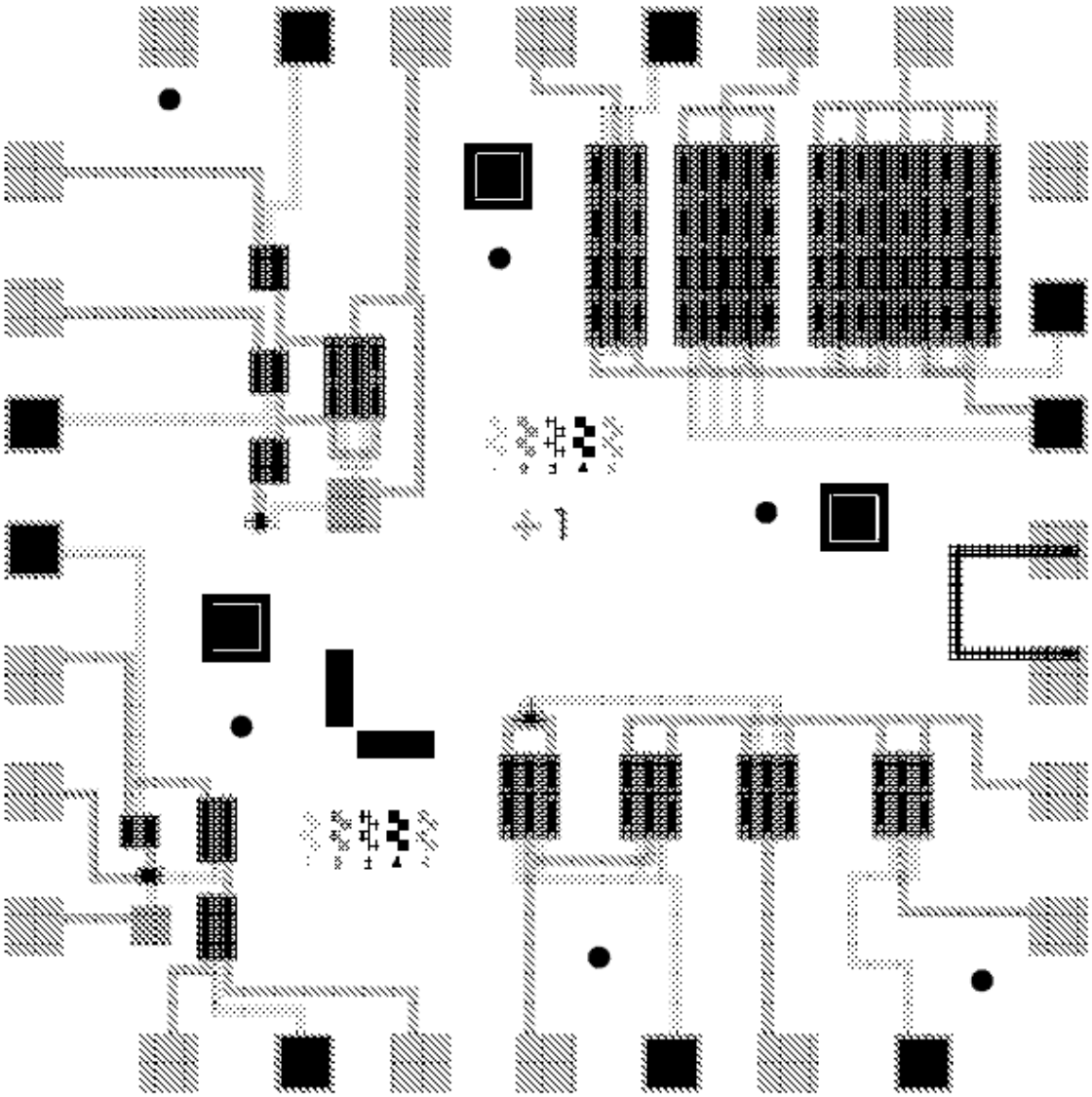


Figure A. 1 Voltage compensated APS, 3-TFT current mediated APS and two current programmed APS

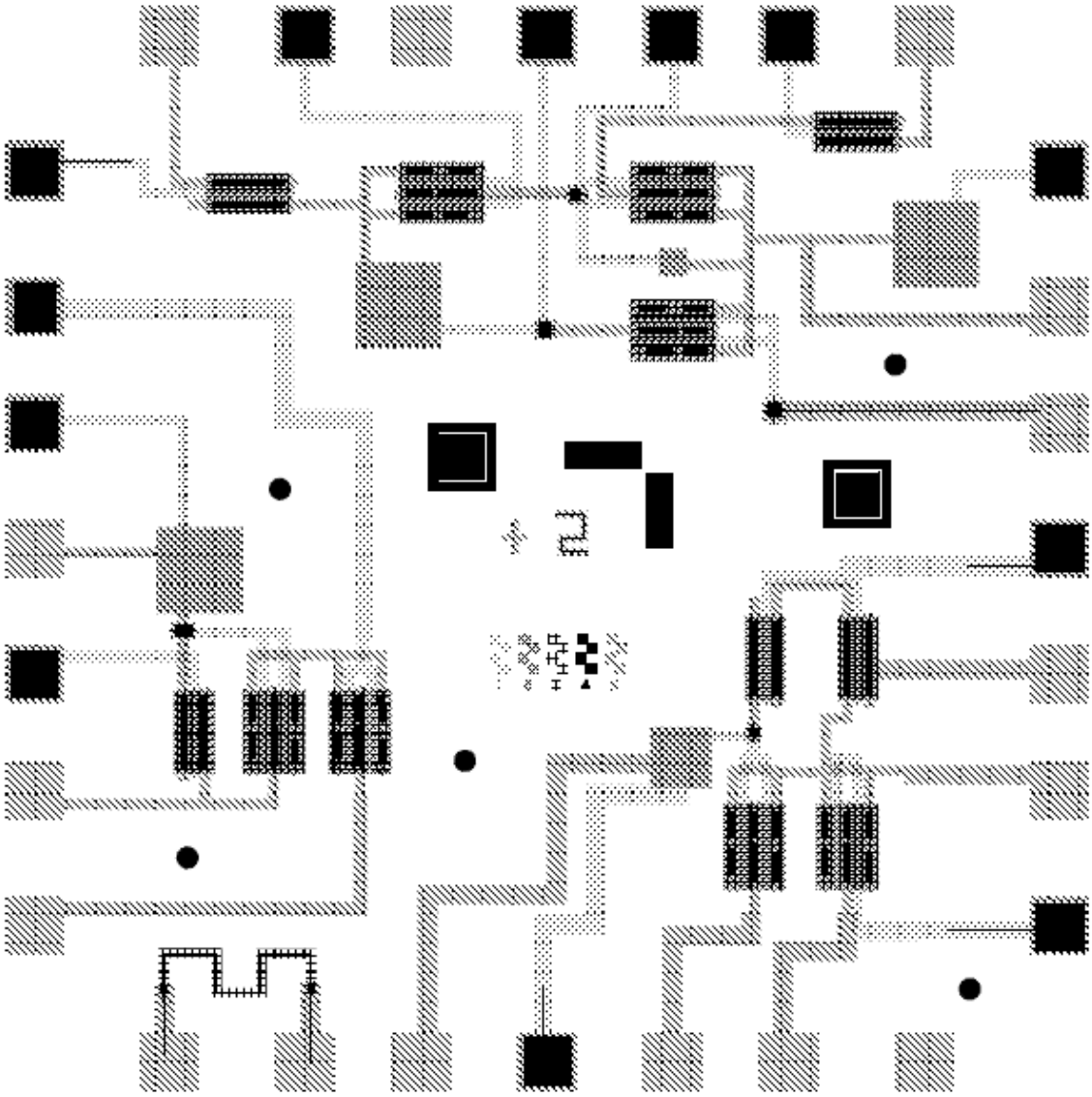


Figure A. 2 Voltage compensated APS, 4TFT current mode APS and 3-TFT APS

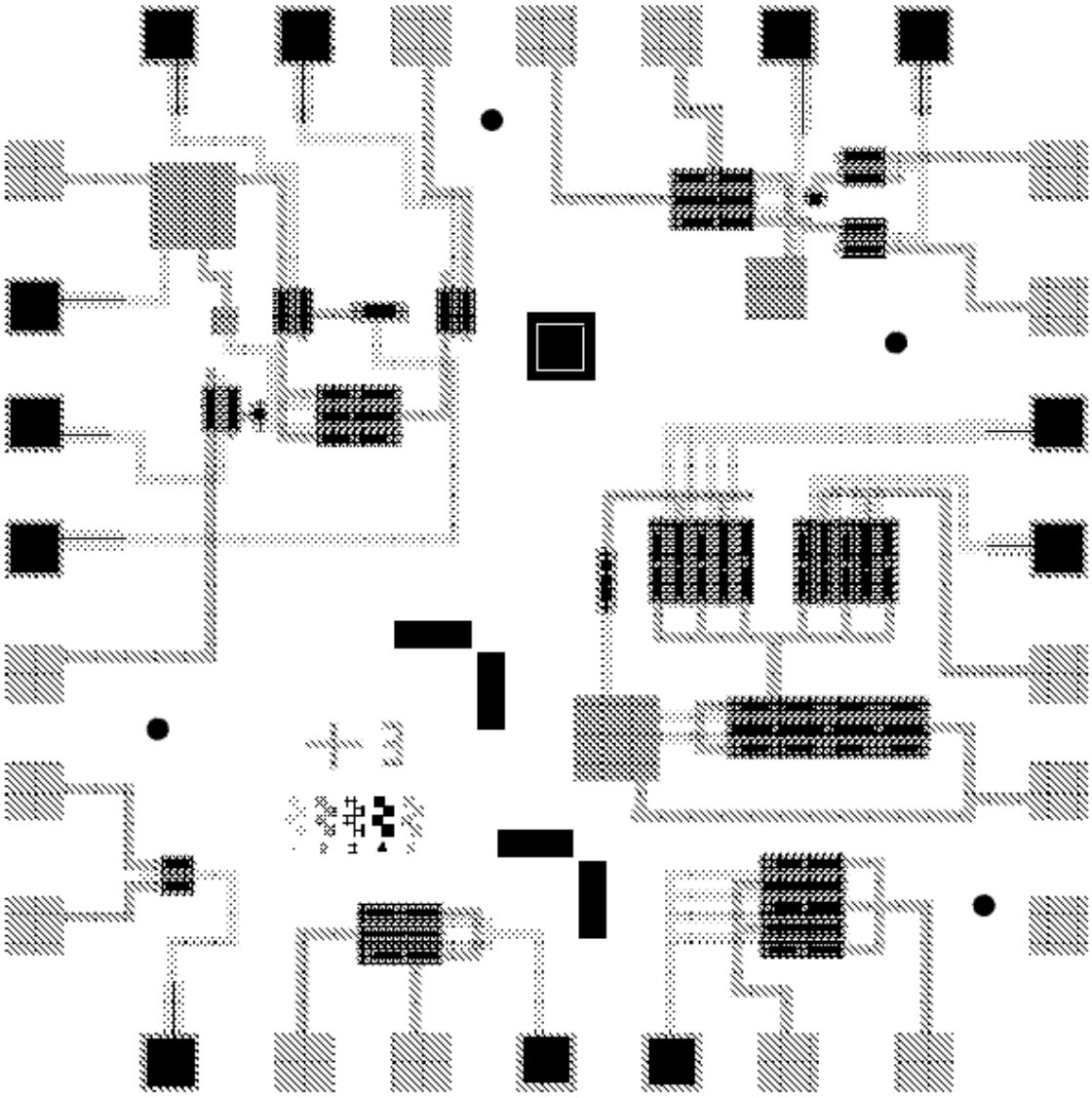


Figure A. 3 Several discrete TFTs and 3-TFT and 4TFT current programmed APS

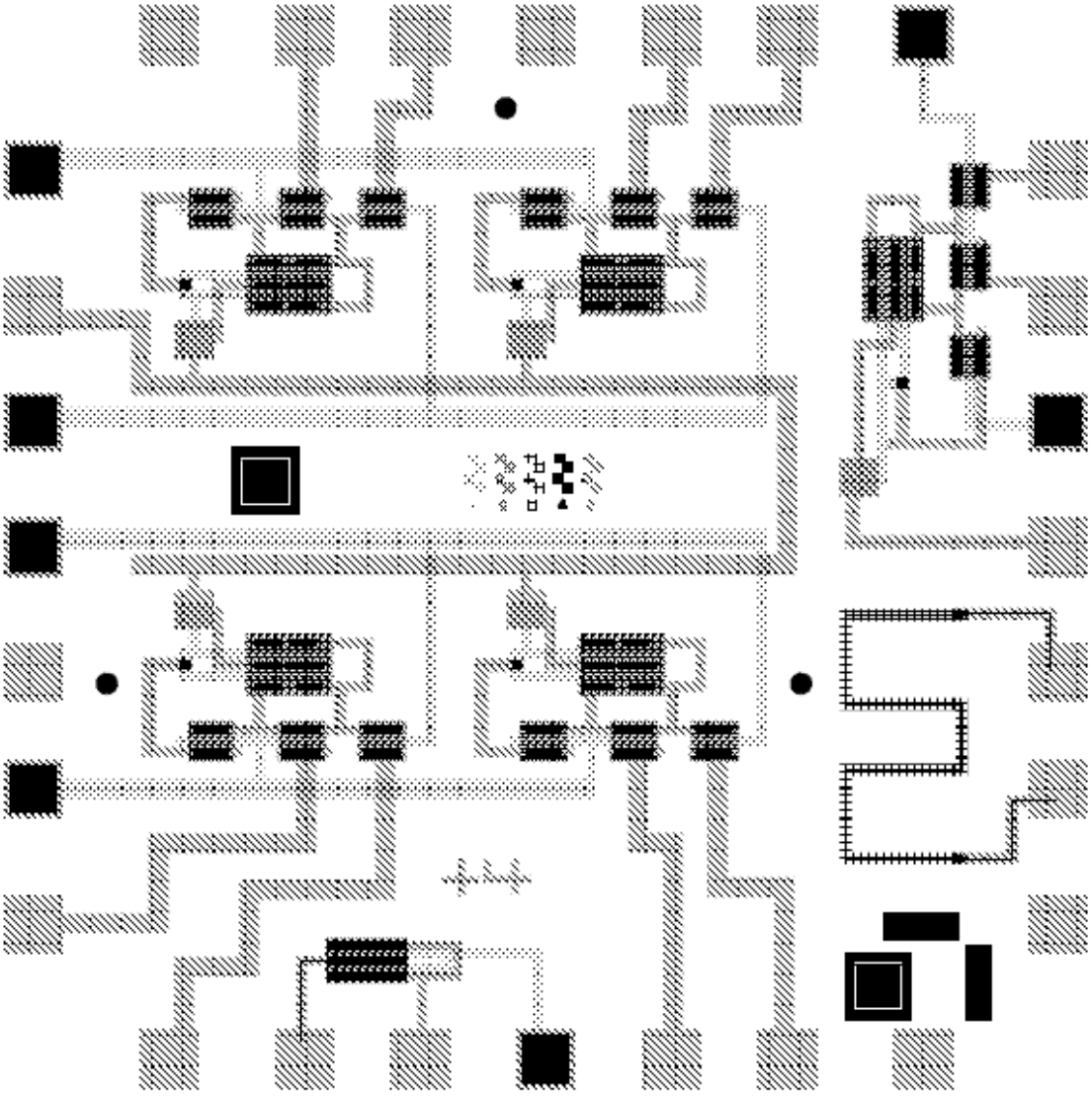


Figure A. 4 2×2 current programmed APS array, 3-TFT APS pixel, discrete TFT

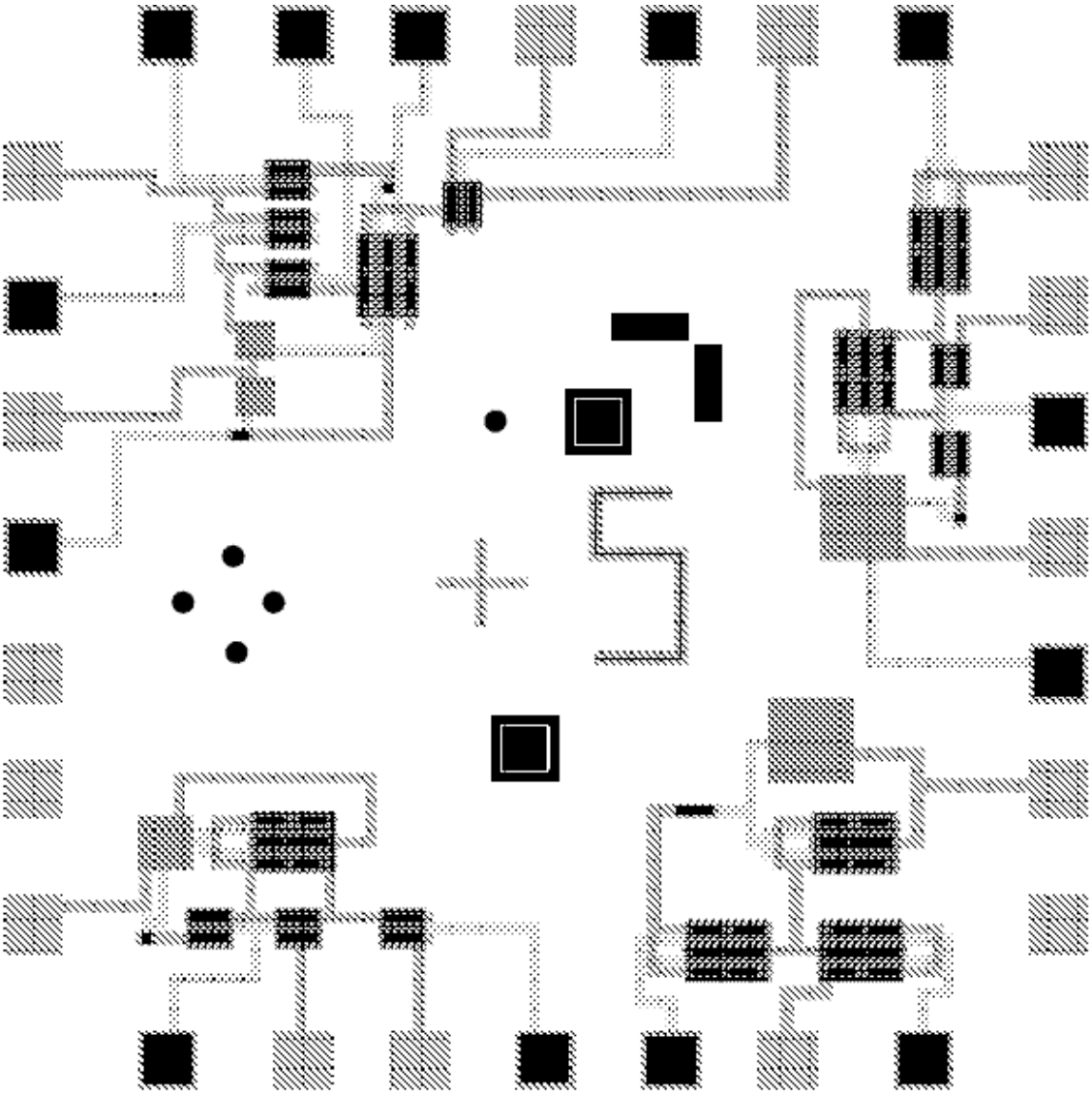


Figure A. 5 Voltage compensated APS, two versions of 4-TFT APS, 3-TFT APS

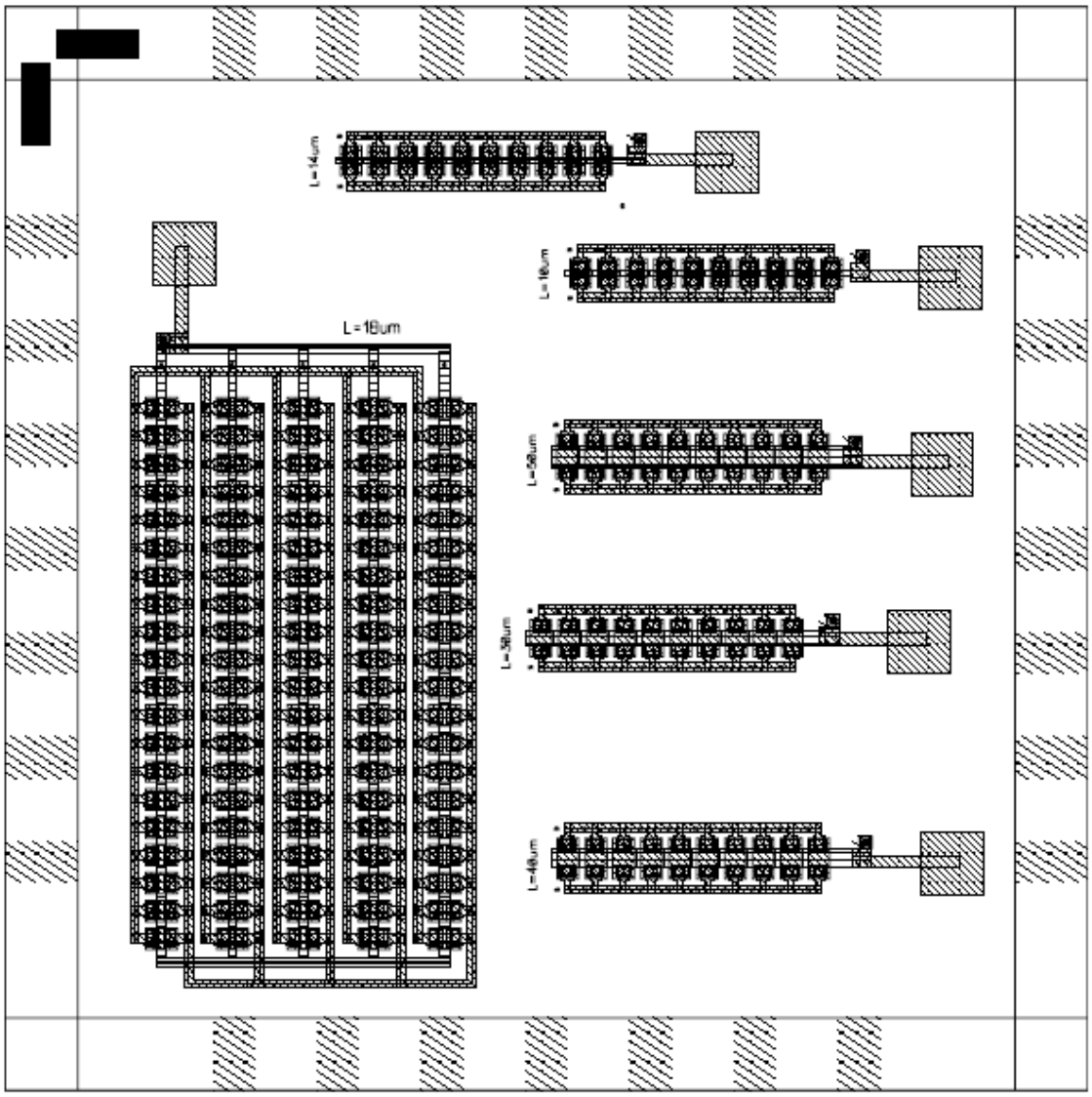


Figure A. 6 Array of single TFTs connected in parallel to measure the leakage current

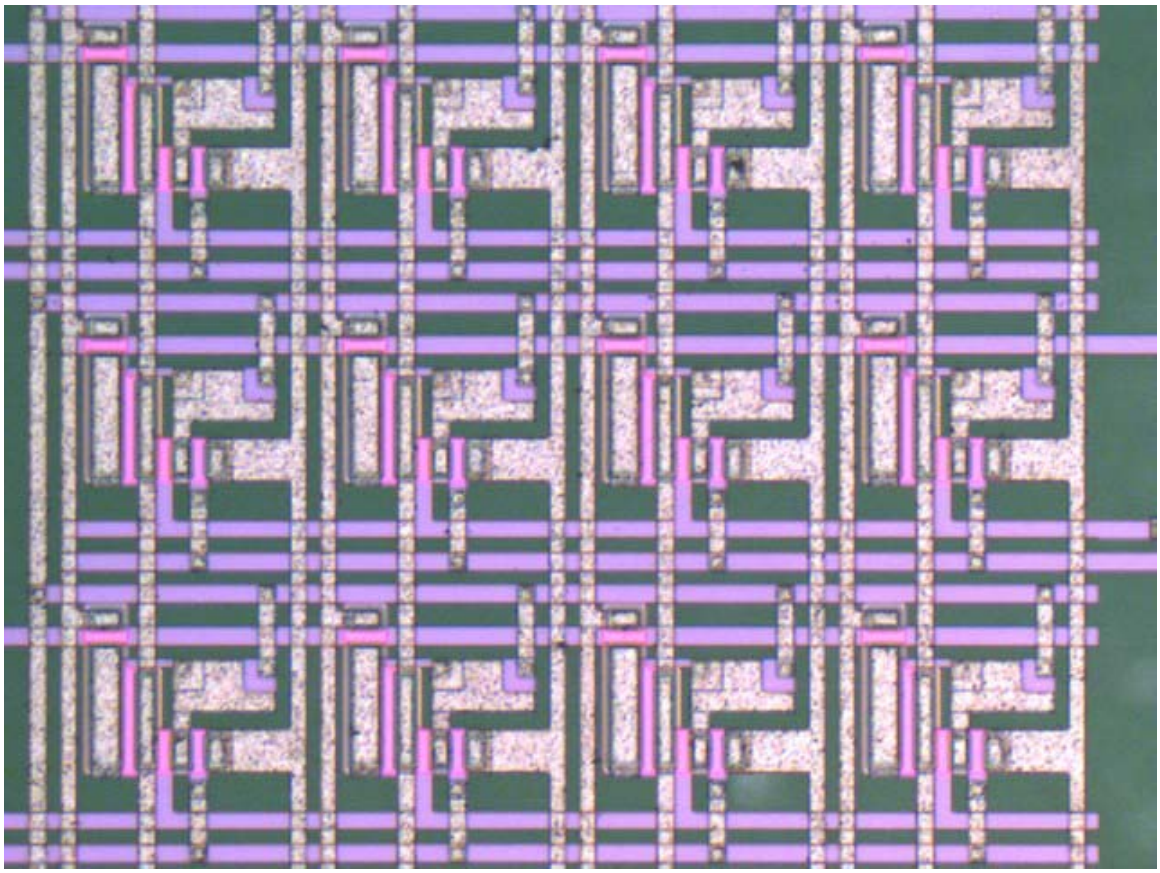


Figure A. 7 3×4 3-TFT pixel array fabricated at University of Waterloo

Appendix B

B.1 Hydrogenated Amorphous Silicon TFTs

Fabrication of a-Si:H TFTs is usually done using Plasma Enhanced Chemical Vapor Deposition (PECVD). Depending on the number of the layers used and the order of their deposition, a-Si:H TFTs can be categorized to four different types [**72**]. Figure B.1 shows the schematic of these four TFT configurations. Figure B.1 (a) and B.1 (b) show the inverted staggered configurations where the gate terminal is deposited on the opposite sides of the drain and source terminals. On the contrary, Figure B.1 (c) and B.1 (d) show the coplanar configurations in which the gate, source, and drain terminals are deposited simultaneously in one layer and are located on the same side. The structures in Figure B.1 (a) and B.1 (b) are usually referred to as top gate and bottom gate TFTs, respectively. In the top gate configuration, the gate is deposited on the top of the a-Si:H layer which acts as the intrinsic layer whereas in the bottom gate structure, the gate terminal is the first deposited layer followed by the gate dielectric and the intrinsic layer. Most of the APS pixel circuits fabricated and tested in this thesis use the tri-layer bottom gate inverted staggered structure [**73**].

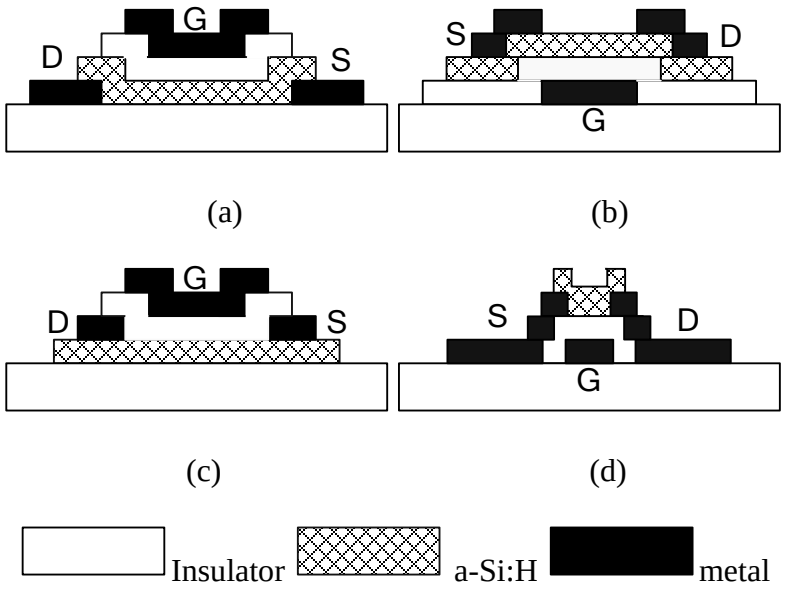


Figure B. 1 Different structures for the implementation of a-Si:H TFTs: (a) staggered, (b) inverted staggered, (c) coplanar, (d) inverted coplanar.

A simplified schematic of the tri layer a-Si:H TFT is shown in Figure B.2. The tri-layer a-Si:H TFT has three layers of silicon nitride. The top layer is used to passivate the intrinsic a-Si:H layer. The middle layer is used to define the source-drain contacts and the lower layer is used as the gate dielectric layer. For the complete fabrication, the tri-layer a-Si:H needs 5 masks [**73**].

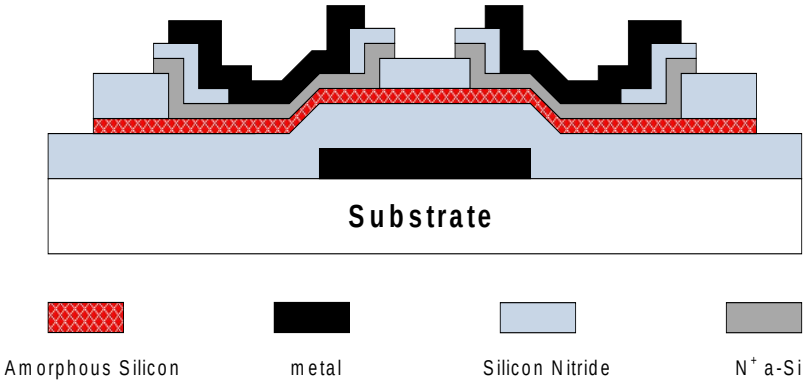


Figure B. 2 Tri-layer Inverted-Staggered TFT structure

An alternative structure to the inverted staggered bottom gate TFT is the Back Channel Etched (BCE) TFT shown in Figure B.3. Here the top surface of the intrinsic a-Si:H layer is not passivated with a layer of silicon nitride and therefore the number of masks can be reduced to four.

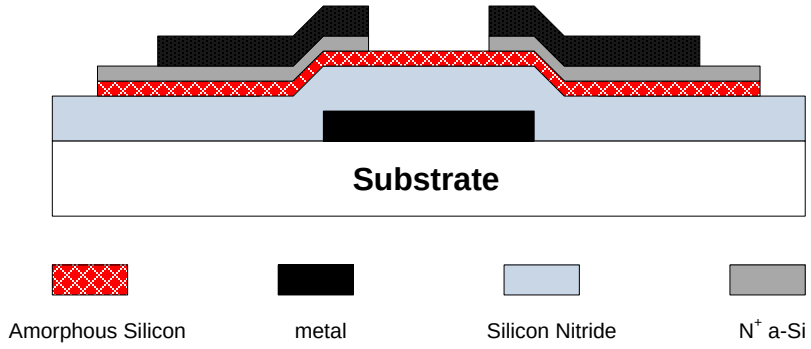


Figure B. 3 Inverted-Staggered back-channel etched (BCE) TFT structure

Due to the formation of the back channel because of the lack of passivation of the top intrinsic layer, the BCE inverted staggered a-Si:H TFT has a higher reverse current value and therefore a lower ON/OFF ratio [**74**] [**75**]. On the contrary, a tri-layer TFT with top layer passivation has a lower reverse current and a better ON/OFF ratio. Lower degree of complexity as well as fewer fabrication steps has made the BCE a-Si:H TFTs the most popular choice in the LCD industry. In the fabrication process of the a-Si:H TFTs, PECVD is used for the deposition of intrinsic a-Si:H, nitride, and n+ microcrystalline layers while sputtering is used for Chromium (Cr) or Molybdenum (Mo) as the gate and drain-source metals. Table 2.1 shows the thickness of various layers used in the fabrication process [**73**].

Table B. 1 The thickness of various layers constructing the Inverted-Staggered a-Si:H TFT

Layer in a-Si:H TFT	Thickness(nm)
Intrinsic a-Si:H	50
Gate Metal	120
a-SiN_X gate Insulator	250
n+ microcrystalline contact layer	30
Drain –Source contact layer	400

B.2 Operation of the a-Si:H TFT

Crystalline silicon has both short range and long range order in the placement of the atoms resulting in a well-defined bandgap in the material. Even though a-Si:H is a disordered material, it has short-range order similar to crystalline silicon and thus, bandgap can be defined for the material [**76**]. However, due to the lack of a long-range order, the conduction and valence bands in a-Si:H do not have well defined abrupt band edges, but broadened tail states that continue into the forbidden bandgap. A-Si TFT is an accumulation-mode field-effect transistor meaning that there is no surface inversion during the conduction of the transistor. The conductivity of the electrons and holes in an a-Si:H TFT is affected by the density of states near the conduction and valence bands. Figure B.4 shows a qualitative sketch of the density of states in intrinsic a-Si:H. It is seen that the tail of the valence band is broader resulting in significant reduction in the hole mobility. The tail states close to the conduction band are called acceptor like states because if they trap an electron, they become negatively charged whereas the tail states close to the valence band are called as donor-like states meaning that they are neutral as long as they do not lose an electron and when they trap a hole, they become positively charged. In addition to the tail states, in the a-Si:H bandgap we have localized deep states. The density of these deep states depends on the deposition conditions and the concentration of hydrogen, and is on the order of 10^{15} to 10^{17} in electronic-grade a-Si:H [**76**]. These states are associated with dangling bonds and they are placed between 0.6eV to 1.4eV above the valence band.

The large number of tail states near the conduction band and the valence band is the primary reason for the low mobility of the electrons and holes in a-Si:H because of the frequent trapping of the charge carriers. In a-Si:H, the number of trapped electrons in the tail states is much larger than the number of free electrons.

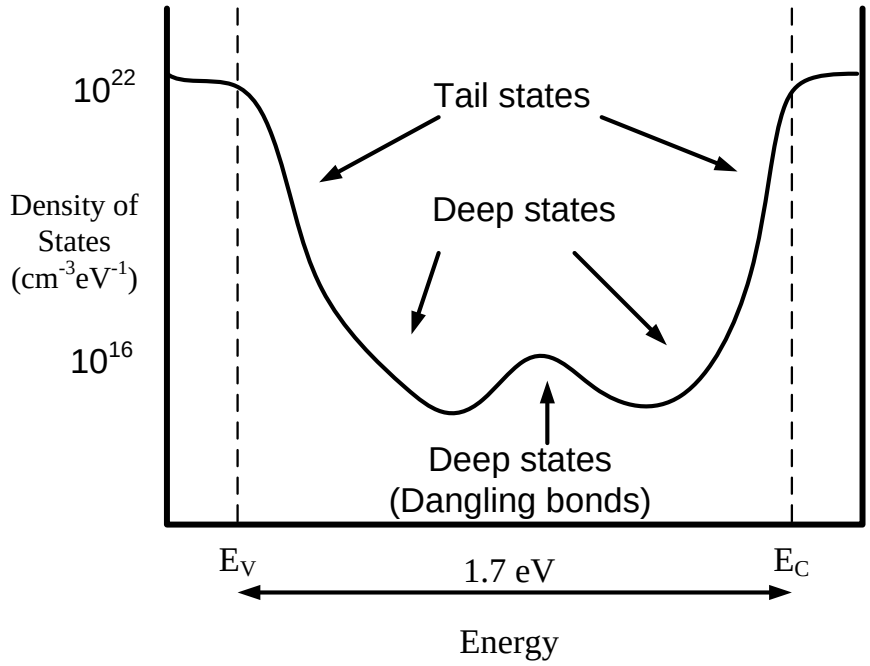


Figure B. 4 Typical Density of states in hydrogenated amorphous silicon.

The large number of tail states that are located near the conduction band edge and the valence band edge cause frequent trapping and detrapping of the free electron and hole charge carriers in the conduction band and valence band, respectively. Therefore these traps are the main reasons for significant reduction of the electron and hole mobility As a result of trapping of electrons, the effective mobility reduces to

$$\mu_{FET=}\mu_n \frac{n_{free}}{n_{trap} + n_{free}} \tag{B.1}$$

Here, μ_n is the mobility of the free electrons in the conduction band, n_{free} is the number of free electrons with energies above the conduction band energy and n_{trap} is the number of trapped electrons in the band tail states [**77**]. Figure B.5 is the transverse characteristic of the TFT

showing the drain-source current of an a-Si:H TFT, I_{DS} as a function of its gate-source voltage (V_{GS}). The operation of the TFT can be categorized to three distinct regions depending on the value of V_{GS}:

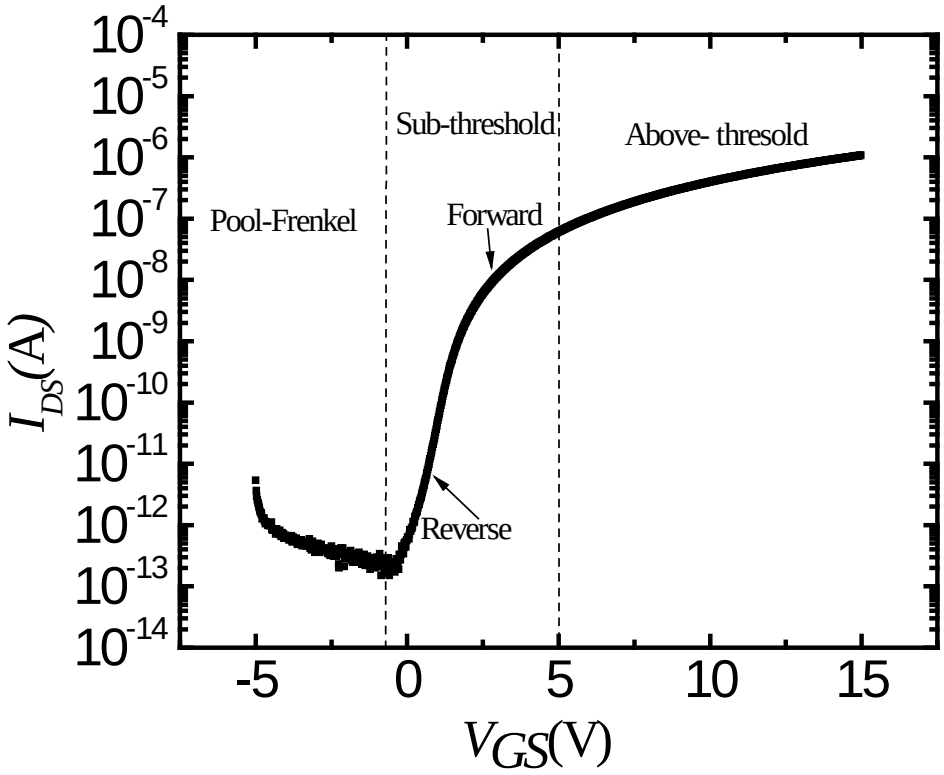


Figure B. 5 Typical I-V characteristic of an a-Si:H TFT fabricated at University of Waterloo. Here the applied drain-source voltage, V_{DS}, is 15 volts.

above threshold, sub-threshold, and Pool-Frenkel emission [**78**]. When the gate-source voltage is zero, the Fermi level is located in the middle of the bandgap among the deep states. Upon small increase in the value of gate-source voltage, the Fermi level increases towards the conduction edge creating the forward sub-threshold region. The current value in this region is in the range of 10^{-9} to 10^{-12} A. In this region, the drain-source current value has an exponential dependence on the value of gate-source voltage. The threshold voltage here is defined as the gate-source voltage that causes the number of electrons in the band tail states to exceed the number of electrons in the deep defect states. For gate-source voltages above the threshold voltage, the Fermi level enters the band tail states. Since the density of states in the conduction band tail is several orders

of magnitude more than the density of states in the deep defect region, the Fermi level is pinned once it enters the band tail states. Therefore, for gate voltages above the threshold voltage, the drain-source current versus the gate-source voltage curve follows approximately a square law relationship. For above threshold region, the drain-source current level is in the range of micro amps. When a negative gate source voltage is applied the TFT enters the reverse sub-threshold region in which the Fermi level goes to lower energies in the deep defect states. Here, the small negative voltage depletes the electrons in the tail states and the channel charge under the forward channel gate insulator becomes negligible. On the other hand, a back channel at the interface of the intrinsic a-Si:H and the passivation layer is formed causing a small conduction in this region. The drain-source current increases exponentially for higher magnitude negative gate-source voltages (Pool-Frenkel emission). Here the conduction is created by the accumulation of holes near the interface between the intrinsic a-Si:H layer and the gate dielectric. These holes are generated by the Pool-Frenkel thermoionic emission at the drain-gate overlap region [**78**].

B.3 Instability of a-Si:H TFTs

In contrast to crystalline silicon MOSFETs, different kind of stress including prolonged gate voltage bias stress or temperature stress causes instability in a-Si:H TFTs. This instability is sensed in the form of variation in the threshold voltage or change in the mobility of the transistors. Figure B.6 demonstrates the measured V_T shift of an a-Si:H TFT under stress of various gate-source voltages for a period of 1000 minutes.

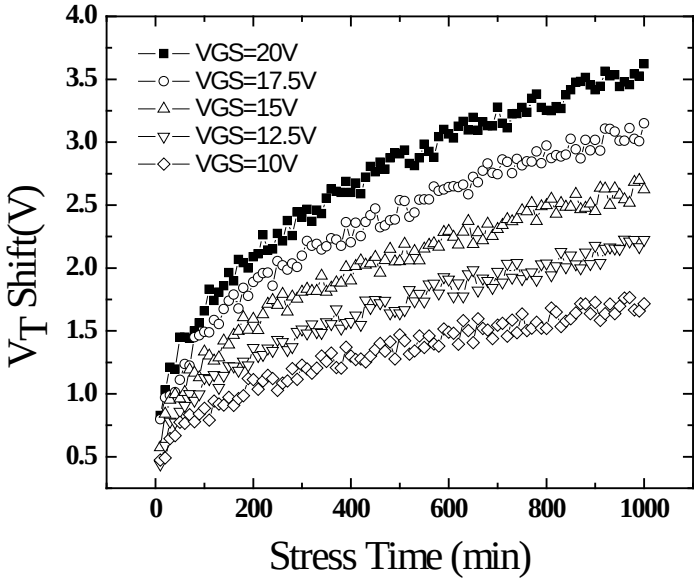


Figure B. 6 Measured V_T-Shift of in-house fabricated a-Si:H TFTs versus time caused by voltage stress.

It is seen that the voltage stress causes an initially fast increase in the value of the threshold voltage followed by a reduction in the rate of threshold voltage increase. The data shows that a 20V stress on the a-Si:H TFT causes its threshold voltage to increase about 3 V in less than 10 hours which is very large compared to the range of data seen in fluoroscopy or radiography. There has been an extensive study on the mechanisms involved in the phenomena of threshold voltage shift variations due to voltage stress [**79**], [**80**], [**81**], [**82**], [**77**], [**83**], [**84**], [**85**]. Unfortunately the suggested qualitative models are unable to predict the exact value for the V_T shift with high degree of accuracy. It is suggested that two distinct main mechanisms are responsible for the V_T shift of a-Si:H TFTs: defect state creation in the bulk of intrinsic a-Si:H and charge trapping in the a-SiN gate dielectric as well as the interface between the intrinsic channel and the gate dielectric. Powel has used an ambipolar TFT to differentiate between the two mechanisms and shine light on the physical origin of the phenomena [**79**]. The experimental results show that at low gate-source bias voltages, the defect state creation in the bulk of the intrinsic layer is the dominant mechanism responsible for the V_T shift. As a result of bias stress, the weak Si-Si bonds break causing acceptor-like tail states in the bulk of a-Si:H. The resulting

broken weak bonds form dangling bonds. The dangling bonds are passivated by the diffusion of hydrogen atoms in the a-Si:H [**84**]. The generated defect states are below the Fermi level, causing a positive shift in the threshold voltage. At higher temperatures the creation rate of defect states increases causing faster increase in the threshold voltage as a result of positive bias stress. At large value of voltage stress, charge trapping is the main origin of shift in the threshold voltage. The density of defects acting as trap centers for charge carries are high in both gate dielectric and the interface of the gate dielectric and the intrinsic silicon because of the disordered nature of a-Si:H and a-SiN. As a result, the free electrons in the channel of the a-Si:H TFT can get trapped in both the interface states and the deep bulk states of the silicon nitride gate dielectric. These two types of trap states can be differentiated by the large difference in their time constants. The time constant related to the interface trap states are in the range of few to hundreds of milliseconds. When the bias stress is removed from the gate, the trapped electrons can be released with this time constant and the value of V_T returns back to its initial value [**85**]. On the contrary, the deep defect states in the bulk of silicon nitride gate dielectric have much longer time constants in the range of hundreds of hours. Therefore the trapped electrons in these states cause nearly permanent shift in the threshold voltage of the a-Si:H TFT. For the electrons to have enough energy to get trapped in the defects located in the bulk of the silicon nitride, the gate voltage should be in excess of 50 volts [**79**]. To reduce the density of traps in the bulk of gate dielectric, the silicon nitride should be as nitride rich as possible meaning that the nitride percentage should be increased [**86**]. As mentioned earlier, the mechanisms associated with threshold voltage shift are reversible and they are highly temperature dependent. Increasing the temperature to elevated values result in fast recovery of the initial state in the threshold voltage. The process of heating the a-Si:H TFT in order to restore its threshold voltage is called Annealing. In the Annealing process, the TFT is heated at the temperature range of around 170^oC for nearly two hours. Then the heater is turned OFF and the TFT is allowed to slowly cool down to room temperature in about 3 hour time span. It is important to avoid sudden decrease in the ambient temperature of the TFT after Annealing because this will cause a temperature shock and permanent damage to the characteristic of the TFT. Annealing removes all the defect states and repels the trapped electrons and therefore restores the initial value of the threshold voltage. Another way to bring the shifted threshold voltage back to its initial value is to apply a negative gate-source voltage to the gate of the TFT [**79**], [**83**]. The applied negative voltage repels the

trapped electrons in the interface states and the silicon nitride deep defect states causing faster recovery of the threshold voltage. It also generates deep defect states that are located in energies above the Fermi level and therefore they cause reduction of the threshold voltage. Even though the application of negative voltage counters the positive shift in the threshold voltage caused by the positive voltage stress, this compensation is not perfect and the absolute value of the positive and negative voltages that completely compensate the threshold voltage depend highly on the fabrication conditions as well as the operating temperature. For instance, measurement data has shown that if the positive and negative gate voltages have the same absolute amplitude, the rate of increase in the threshold voltage caused by the positive voltage stress is higher than the rate of decrease in the threshold voltage caused by the negative voltage stress [**83**].

B.4 Effect of Temperature on the transfer Characteristics of a-Si:H TFTs

The electrical characteristics of a-Si:H TFTs are very sensitive to the change in temperature. This sensitivity causes problem particularly when the array is used in fluoroscopy. During fluoroscopy, the array is continuously exposed to the incoming x-ray radiation. Also, the continuous switching of the TFTs, which is necessary to perform the read, integration and reset cycles, causes a considerable amount of dynamic power dissipation. This is in addition to the static power dissipation caused by the leakage currents in the TFTs and the x-ray sensitive photoconductor. This power consumption, results in noticeable increase in the temperature of the active matrix flat panel imager in the fluoroscopic mode of operation. If the temperature passes a certain limit, it causes the crystallization of the a-Se sensor and consequently a considerable increase in the leakage current and reduction of the signal to noise ratio. To prevent this phenomenon from happening, cooling fans are usually used. The operation of the cooling fans causes a temperature gradient across the surface of the active matrix flat panel imager. On the other hand as mentioned before, since the characteristics of a-Si:H TFTs are very temperature

sensitive, the output of the active pixel circuits in different locations of the array with different temperature would not be the same even if the bias voltages and the input x-ray generated charge to these pixel circuits are exactly the same. This problem demonstrates itself in the form of fixed pattern noise in the final image of the array. In Figure B.7, the change in the measured output current of a discrete TFT fabricated in University of Waterloo as a function of temperature is demonstrated. As can be seen, the change in temperature from 20^{o}C to 80 ^{o}C causes a 6-fold increase in the output current.

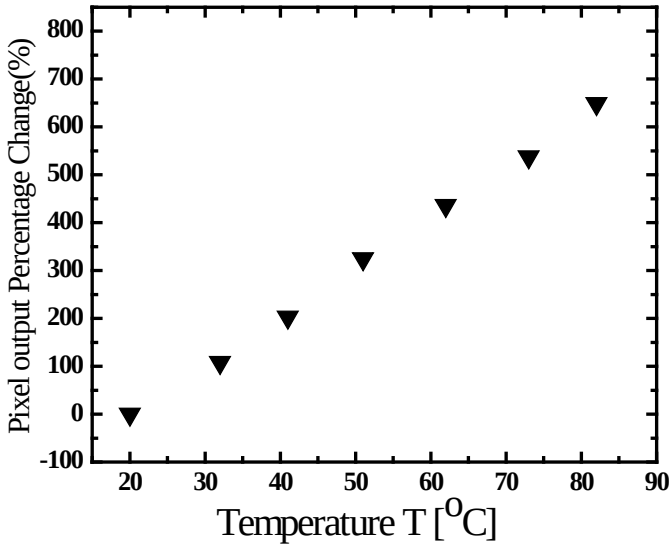


Figure B. 7 Percentage change in the output current of a discrete TFT versus ambient temperature

Figure B.8 shows the measured drain-source current versus gate voltage characteristics for a discrete TFT fabricated at University of Waterloo and biased in the triode region. As can be seen, the drain-source current increases with the increase in temperature [**87**]. Figure B.9 shows the measured transconductance of a TFT biased in saturation as a function of temperature. This increase can be attributed to higher effective mobility and higher number of free charge carriers in the channel at elevated temperatures. The power factor of the TFT, α, slightly decreases with the temperature, as shown in Figure B.10. The threshold voltage of a TFT decreases as the temperature increases as shown in Figure B.11. For an a-Si TFT in the saturation region, an empirical temperature model has been reported in [**88**].

The TFT I-V characteristic is expressed by

$$I = K(T)(V_{DATA} - V_T(T))^{\alpha(T)} \tag{B.2}$$

Where, *K(T)*, $V_T(T)$, and $\alpha(T)$ are determined by the following equations:

$$V_T(T) = V_T(T_0) - \eta 1(T - T_0) \tag{B.3}$$

$$\alpha(T) = \frac{0.95q}{KT\beta} + \alpha_0 \tag{B.4}$$

$$K(T) = K_{To} exp\left[\eta 2\left(\frac{1}{T_0} - \frac{1}{T}\right)\right] \tag{B.5}$$

Here, η_1, η_2, and β are process-dependent parameters and are obtained from measurement.

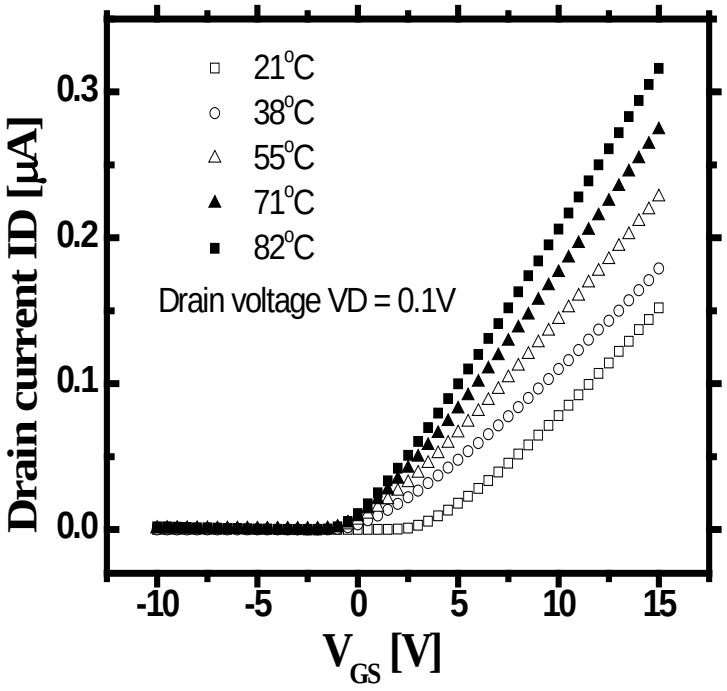


Figure B. 8 IDS versus VGS of an in-house fabricated a-Si:H TFT for several operating temperature. The TFT is biased in Linear Mode of operation.

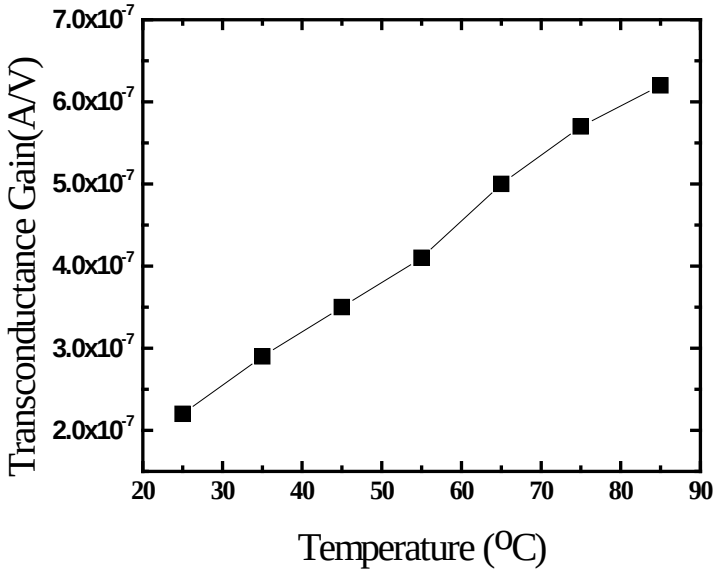


Figure B. 9 Increase in the transconductance gain of an a-Si:H TFT biased in saturation versus temperature.

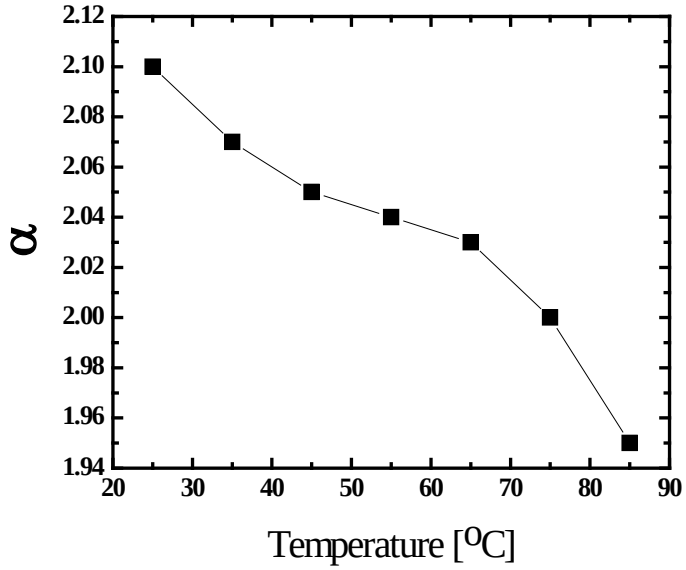


Figure B. 10 Decrease in the power factor of the transfer function of the TFTas the ambient temperature is increased from 20 to 80oC

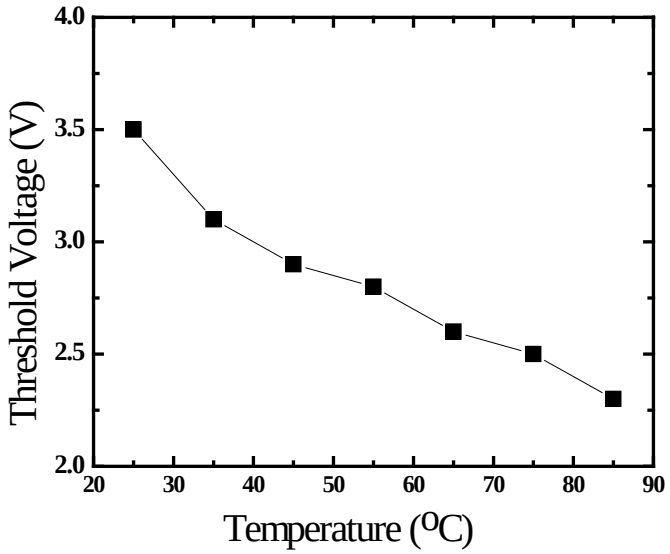


Figure B. 11 Decrease in Threshold voltage of a TFT as the ambient temperature is increased from 20 to 80°C

B.5 Lack of p-channel Device

In a-Si:H TFTs, the mobility of holes is considerably lower than electrons [**73**]. Therefore the size of p-channel TFTs has to be very large making it impossible for their use in high resolution imaging flat panel arrays. Consequently, in the design of active pixel sensor circuits, we are limited only to the use of n-channel TFTs. This limits the number of design options.

B.6 Leakage Current of a-Si:H contributing to image quality degradation

During the Integration mode, the leakage current of the switch TFT discharges the storage capacitor, C_S, causing the voltage developed across it in the reset mode to decrease over time. This is one of the sources of noise and will be considered in details in the noise calculations.

Assuming that the sequence for the operation of each pixel in the array is Reset, Integration and Readout, respectively, on average the output current of the APS during Readout is less than the output current at the end of Reset by [**23**]

$$\Delta I_H \approx \frac{1}{2}\frac{t_{int}}{C_S} I_{OFF} g_m \tag{B.6}$$

where t_{int} is the integration time, I_{OFF} is the leakage current of the switching TFT, and g_m is the transconductance of the amplifying TFT for the nominal reset current. The leakage current of the switching TFTs is about 1pA. For instance, for a flat panel imager with a readout rate of 30 Hz, the storage capacitor of the pixel circuit equal to 1pF and the transconductance of the amplifying TFT g_m=1 μA/V the change in the output current is about 30nA.

B.7 Number of TFTs per Pixel

High resolution flat panel imagers require a certain area per pixel. For instance, in case of fluoroscopy, the pixel area cannot exceed 250μm×250 μm or if a flat panel imager is supposed to be used in dual mode fluoroscopic and radiographic applications, the pixel pitch has to be between 100 and 200 μm. Due to relatively small effective mobility of the a-Si:H TFTs, the aspect ratio of the circuit transistors, especially the amplifying TFT, should be large. This also limits the number of transistors allowed to be used under each pixel. Also, to get a high quality image out of the flat panel imager, a very high percentage of the pixels in the array should work properly. This requisite translates to the required high yield and put a further restriction on the number of TFTs in each APS. This limitation in the number of TFTs in each APS prevents the designer from having complex circuits and implementing the necessary compensation of the TFT characteristic changes within the APS circuit. On the other hand, the off-panel external current or voltage drivers are fabricated in the CMOS technology which allows the realization of very complex circuits. Therefore a successful driving scheme which can compensate for the instabilities of the TFTs uses a combination of simple on-pixel TFT circuits and more complex off-panel CMOS driver/readout circuits.

B.8 Charge Injection

An error will be induced on the charge held by the storage capacitor when the TFTs acting as switches in the APS circuit are turned off. This is due to the charge injection and clock feed though originated from the channel charge and the overlap capacitor of the switch TFTs, respectively. To minimize this effect, the size of the switch TFT, amplifying TFT as well as the storage capacitor should be chosen appropriately. For larger value of the storage capacitor, the induced error is smaller. But at the same time, larger storage capacitor results in lower input voltage signal for the same amount of radiation. Also, the size of the switching TFTs has a considerable effect on the amount of charge injection. It is useful to minimize the size of the switching TFTs to reduce the charge injection error. On the other hand, small switch sizes show large on resistance causing long programming time. Therefore, there is a compromise in the design of switching TFTs between the programming time and the charge injection error. In addition, the amount of charge injection is dependent on the threshold voltage of the amplifying TFT causing a time variant charge injection error on the storage capacitance. This problem will be further investigated in Chapter 3.

B.9 Models for Hydrogenated Amorphous silicon TFTs

In order to have a better insight of the function of the a-Si:H TFTs and understand their behaviour in different modes of operation, several physical models have been proposed [**75**], [**89**], [**73**], [**76**], [**78**]. These models focus on the above threshold and forward subthreshold region of operation of the TFTs. Some other models investigate the reverse current-voltage characteristics of inverted staggered a-Si:H TFTs [**78**]. In most of the models, gradual channel approximation is used to drive the I-V characteristics of the TFT. Also they assume that the density of states in the intrinsic a-Si:H channel consists of two separate exponential distributions for conduction and valence band tail states. The gradual channel approximation results in the following equations for the drain-source current versus the characteristics of the TFT:

$$I_D = -q\mu_{FET} n_{ind} W \frac{dV(x)}{dx} \tag{B.7}$$

$$n_{ind} = \frac{c_i}{q}\left(V_{gs} - V_{FB} - V(x)\right) \tag{B.8}$$

Here, n_{ind} is the total number of electrons in the channel that are either free in the conduction band or are trapped in the shallow band tail states, $V(x)$ is the channel potential, V_{FB} is the flat band voltage and W is the channel width. In the crystalline MOSFET, μ_{FET} is equal to μ_n, the electron band mobility, and n_{ind} is equal to the free electrons, n_{free}. In a-Si TFT, on the contrary, the number of free carriers is a small percentage of the total number of channel charge and μ_{FET} is much smaller than μ_n. The effective mobility μ_{FET} versus μ_n can be written as

$$\mu_{FET} = \mu_n \frac{n_{free}}{n_{ind}} \tag{B.9}$$

Experimental results show that the distribution of donor like and acceptor like density of states can be presented as:

$$g_D(E) = g_{tv}\, exp\left(\frac{E_V - E}{E_{tv}}\right) + g_{dv}\, exp\left(\frac{E_V - E}{E_{dv}}\right) \tag{B.10}$$

$$g_A(E) = g_{tc}\, exp\left(\frac{E - E_C}{E_{tc}}\right) + g_{dc}\, exp\left(\frac{E - E_C}{E_{dc}}\right) \tag{B.11}$$

These results can be used to derive the effective mobility, μ_{EFT}, of the a-Si:H TFT. Figure B.12 shows the density of states for donor-like and acceptor like defects [**90**]. In different a-Si:H TFT models, various methods are used to derive the effective mobility, μ_{FET} from the density of states. Shur et al. have assumed that there is a strong relation between μ_{FET} and the amount of charge induced in the channel which is a function of the voltage applied across the gate-source terminal [**90**]. In [**91**], an analytical model based on solving the Poisson's equation has been reported. Another empirical model, assuming that the effective mobility is a function of the applied voltage has been presented and implemented in AIM-SPICE [**92**].

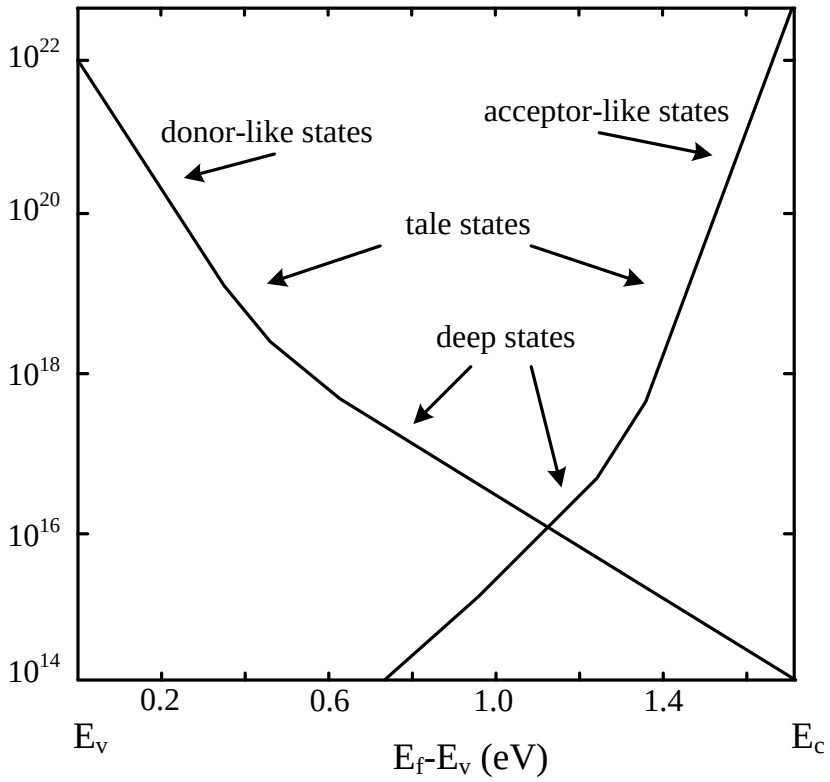


Figure B. 12 Exponential model of the density of states in a-Si:H.

B.10 Models for threshold voltage shift

Threshold voltage shift (ΔV_T) is one of the most apparent instability mechanisms seen in a-Si:H TFTs. It is induced as a result of different stress mechanisms such as voltage, thermal, mechanical and light stress. In the case of voltage stress, the voltage can be either prolonged DC voltage with positive or negative polarity or time varying pulsed voltage. To explain the threshold voltage shift phenomenon, usually two instability mechanisms have been reported to be involved [**84**]. One of the mechanisms is charge trapping in the a-Si:H gate dielectric (a-SiN_x:H) of the TFT which is believed to dominate at large positive or negative bias and the second one is the creation of metastable states in the a-Si:H layer or at the a-Si:H/a-SiN_x:H interface. Charge trapping in the gate dielectric under positive bias has a strong dependence on the applied field and the dominant mechanism contributing to the threshold voltage shift changes

from state creation in the bulk intrinsic layer to charge trapping in the nitride as we increase the applied stress voltage. For lower bias voltages (e.g., <25 V) defect creation dominates whereas the dominant mechanism at higher gate voltages becomes charge trapping [**73**], [**76**], [**72**]. Bias stress measurements on ambipolar a-Si:H TFTs has been conducted to distinguish between trapping in slow states in the gate dielectric and creation of extra fast states in the bulk a-Si:H. Metastable defect state creation is consistent with the model of Si dangling bond formation in the bulk of a-Si:H channel. The dangling bond creation is due to weak Si-Si bond being broken by the presence of electrons in the channel. These dangling bonds are later stabilized by diffusion of hydrogen atoms. Therefore this mechanism has strong dependence on the quality of a-Si:H films. Charge trapping, on the other hand, is largely influenced by the quality of the gate nitride. It is seen that under the same defect density of the intrinsic a-Si:H layer, the TFTs with N-rich gate nitride show lower amount of charge trapping compared to TFTs with Si-rich gate nitride and the number of trap sites inside the gate nitride and near the a-Si:H/a-SiN_x interface depends on the quality of the gate nitride [**78**]. Plasma-enhanced chemical vapour deposition (PECVD) is usually used to deposit the a-SiN_x:H gate insulator of the TFTs. When the TFT is turned on, the electron charges accumulated under the channel and near the interface between a-Si:H and a-SiN_x:H get trapped in the high density of defects inside the insulator [**79**]. For the process of charge trapping, they are first trapped within the localized interfacial states at boundary of the a-Si:H/a-SiN_x:H, and then, due to the thermal energy the deeper traps are occupied by the electrons either by hopping or through a multiple-trapping and emission process [**85**]. Logarithmic time dependence is usually seen for charge injection into an insulator, where the injection current depends exponentially on the density of previously injected charge. Charge trapping process is virtually shown to be temperature independent [**84**].

$$\Delta V_T \sim r_d \log(1 + \frac{t}{t_0}) \tag{B.12}$$

Here t_o is temperature dependent parameter, r_d is a temperature independent constant which depends on the density of traps and t is the bias stress time duration. For state creation, it is reported that this phenomenon is related to the breaking of weak Si-Si bonds and the dispersive diffusion of hydrogen [**83**]. The breaking of weak Si-Si bonds usually dominates at low positive gate voltages (<25 V).When a low value positive voltage is applied to the gate of the TFT,

electrons accumulate and form a channel near the interface between a-Si:N_x and a-Si:H. The majority of these electrons reside in conduction band tail states. The bond breaking reaction proceeds by a single electron being captured at the weak bonds which are a subset of the conduction band tail states. The broken band tail bonds form silicon dangling bonds which are regarded as deep defect states [**77**]. The defect pool concept has been incorporated into the instability mechanism for low stress voltages. In this model, it is assumed that the rate of defect creation is a function of the density of the week bonds in the band tail states, the barrier to defect formation, and the number of electrons in the channel. Deep-state defect creation has power law dependence on the stress time and is a strong function of temperature [**81**]. If a TFT is stressed with low value voltages, the dominant mechanism for the induced threshold voltage shift is defect creation and based on the above explanations, the threshold voltage shift, ΔV_T can be expressed as [**79**]:

$$\Delta V_T(t) = A(V_{GS} - V_{Ti})^{\alpha}(t)^{\beta} \tag{B.13}$$

Here A, α, β are temperature-dependent parameters, V_{GS} is the stress voltage across the gate-source terminal of the TFT, V_{Ti} is the initial voltage of the TFT before the bias stress is applied and t is the duration of the bias stress.

B.11 Metastability measurement of discrete TFTs at positive and negative DC bias voltages

The change in the threshold voltage of discrete TFTs after applying positive and negative DC stress voltages continuously for more than 1000 minutes is shown in Figure B.13 and Figure B.14, respectively. It is seen that positive DC bias stress causes increase in the threshold voltage of the TFT whereas negative bias stress decreases the value of the threshold voltage of the a-Si:H TFT.

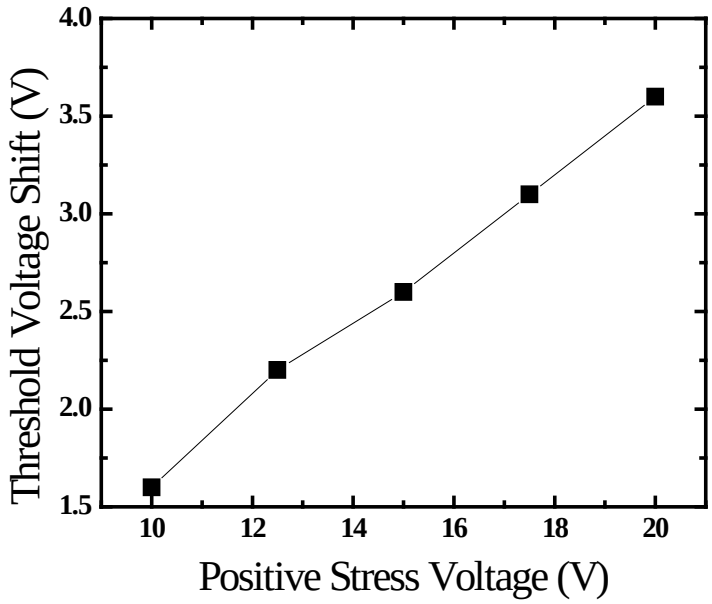


Figure B. 13 Change in the threshold voltage as a result of positive bias stress

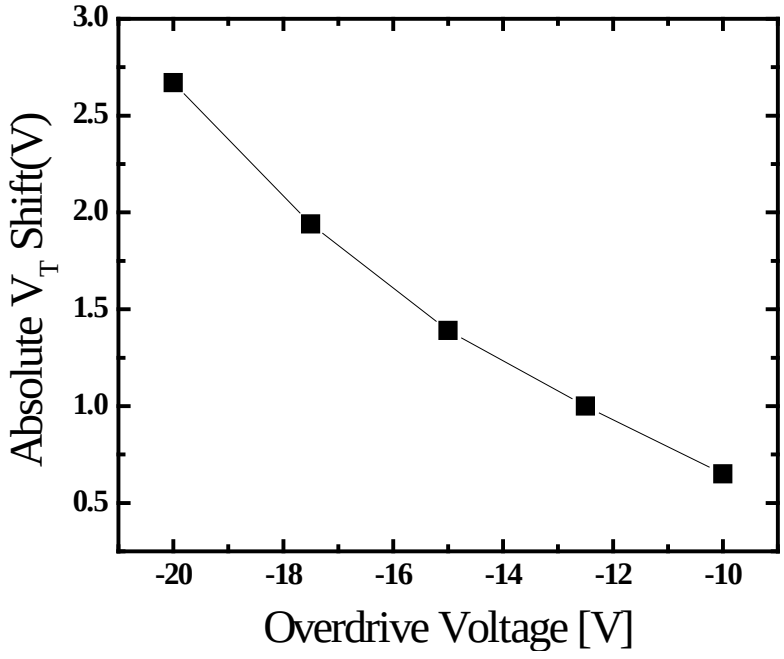


Figure B. 14 Change in the threshold voltage as a result of negative bias stress

Form the measurements, it is seen that for a specific stress duration, positive voltage results in higher amplitude of the threshold voltage shift compared to the negative voltage with the same absolute value. Some research results show that charge trapping in the gate nitride is the main

reason of threshold voltage shift due to positive gate stress whereas the outcome of other researches demonstrate that both charge trapping and defect state creation contribute to the increase in the threshold voltage. For the negative voltage, it is suggested that the simultaneous creation and reduction of defect states in the bulk as well as the interface between the gate nitride and the a-Si:H channel are the mechanisms involved in the change in threshold voltage [**93**].

B.12 Experimental Setup for Threshold Voltage Shift in a-Si:H TFTs

The a-Si:H TFTs used for metastability stress are of various sizes and are bottom gate, inverted staggered type. Before stressing the individual a-Si:H TFTs for threshold voltage shift measurements, they are annealed at 170^{o}C for 2 hours proceeded by cooling down to room temperature for 5 hours. This sequence causes the TFTs to approximately restore their initial transfer characteristics. The time devoted for high temperature annealing and cooling was the same in all different experiments on various samples. Keithley SMU parameter analyzers were used to supply exact, temperature invariant bias voltages to the terminals of the TFTs under bias stress. The same SMUs were used to measure the transfer curve, I_D-V_{GS}, of the TFT under stress every 30 minutes. After the test is completed, the TFT is annealed and the transfer characteristic is measured one more to confirm that the original TFT characteristic is restored to a value within 5% of the original parameters. After that the test is repeated two more times and the associated data is averaged to increase the reliability of the measured data.

In the sweeping process used for measuring the TFT transfer characteristic (I_D-V_{GS}), the drain voltage is set to a small value (0.1V). This small drain voltage value is chosen for the drain voltage to bias the TFT in the linear mode of operation. It is reported that changing the drain voltage of the TFT has a profound effect on the threshold voltage shift profile [**15**]. The gate-source voltage was swept from -5V to +20V during the transfer extraction process. The resolution was chosen to be 0.5V/step and the fast setting of the Keithley SMU was chosen. The transfer extraction period should be very small compared to the stress time period to make sure that it would not have an interfering effect with the threshold voltage shift measurements caused

by the DC bias stress. This problem is more significant in the case of negative threshold voltage measurements. Therefore it is suggested that for negative bias stress, the time span between each transfer characteristics extraction should be increased [**15**].

B.13 Effect of Positive DC Voltage stress

It is believed that for low voltage value DC bias stress, defect state creation is the main mechanism responsible for the shift in the threshold voltage. In this scheme, $\Delta V_T(t)$ has a power law dependence on the duration of the stress and it is directly proportional to overdrive voltage applied across the gate-source terminal of the a-Si:H TFT [**86**].

$$\Delta V_T(t) = A(V_{GS} - V_{Ti})^{\alpha} t^{\beta} \tag{B.14}$$

Here, V_{GS} is the stress voltage during the experiment. V_{Ti} is the initial threshold voltage of the TFT and α and β are the fabrication related constants. To verify that the in-house, bottom gate, inverted staggered TFTs have defect state creation as their dominant method of metastability, two sets of extended stress tests were performed. In the first test, the stress time duration is kept constant for 24 hours and the overdrive voltage is changed. Figure B.15 shows the measurement results. The slope of the measured experiments gives α value to be approximately equal to unity. In the second set of tests, the applied gate bias voltage is kept constant and the threshold voltage is continuously measured over time. From this experiment, according to equation B.14 and the results in figure B.16, the change in the threshold voltage versus time and therefore the parameter β can be extracted. By fitting the equation $\Delta V_T(t) = A(V_{GS} - V_{Ti})^{\alpha} t^{\beta}$ to the measured data, the parameters, A, α and β are extracted to be 0.0123, 1.1 and .34, respectively.

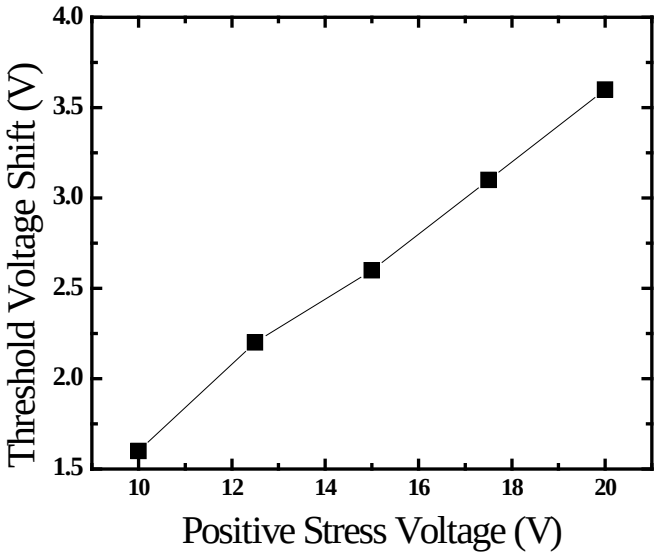


Figure B. 15 Threshold voltage shift versus overdrive voltage for positive bias stress.

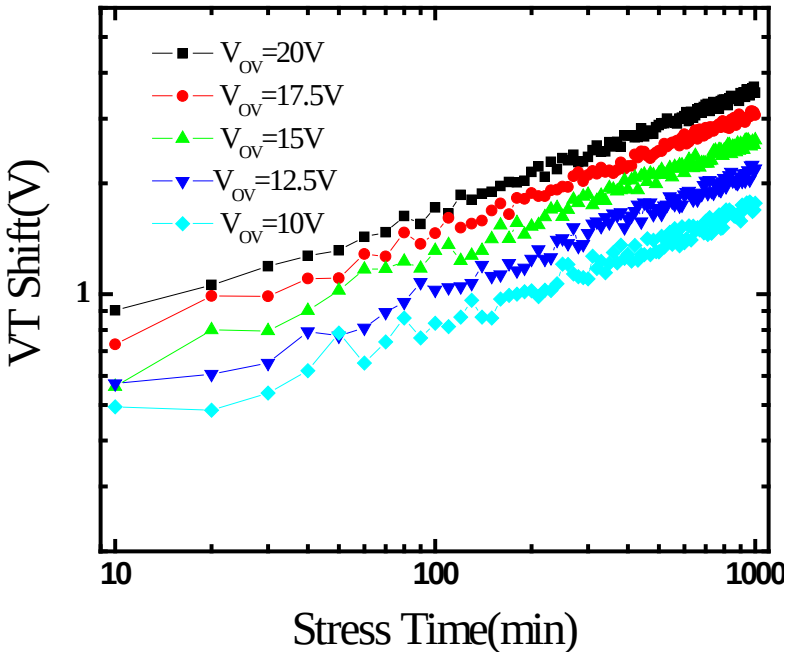


Figure B. 16 Threshold voltage shift versus time for positive bias stress

B.14 Effect of Negative DC Voltage stress

The switching TFTs undergo negative bias stress during most of the operation cycle in the flat panel imager. To quantify the effect of continuous negative gate stress on the threshold voltage shift of discrete TFTs, two sets of tests have been conducted. Figure B.17 shows the threshold voltage shift data plotted versus negative gate overdrive stress. Assuming that similar to the DC positive voltage stress, threshold voltage shift has a power law dependence on the overdrive voltage stress and the stress time duration,

$$\Delta V_T = -A|V_{GS} - V_T|^{\alpha} t^{\beta} \tag{B.15}$$

We conclude the value of α is around 2.2 and A is around 0.0006 by fitting the above equation into the measured data. Figure B.18 on the other hand shows the change in the threshold voltage versus time as a result of negative gate stress. From this data, a value of around 0.25 is extracted for β.

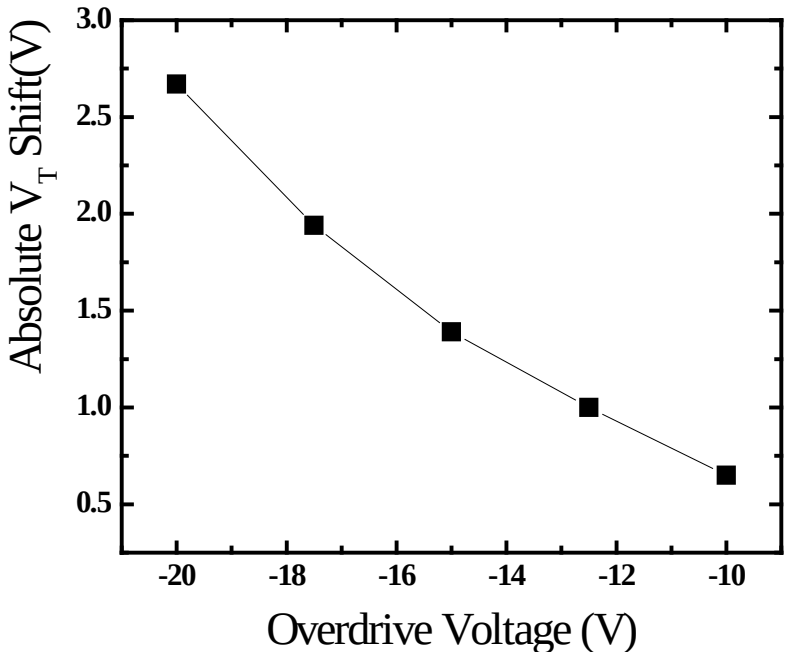


Figure B. 17 Threshold voltage shift data plotted versus negative gate stress overdrive voltage (V_{GS}-V_T)

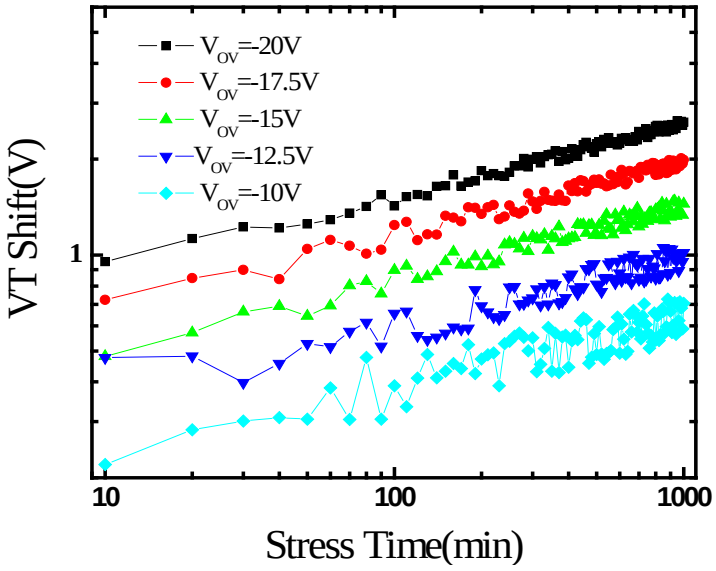


Figure B. 18 The threshold voltage versus time as a result of negative gate stress

Unlike the case of positive voltage stress, the theory for negative voltage stress is not yet well developed and the models used are mostly empirical. The extracted values for α and β are given in Table 2.2 and compared with the values reported by other researchers. The values are highly dependent on the processing conditions and they are in agreement with the previously published data.

Table B. 2 α and β values extracted by various researchers for a-Si TFT ΔV_T.

Positive Voltage Stress	α	β
In-house	1.1	0.34
Karim [**15**]	1	0.3
Powell [**86**]	1	0.45
Libsch [**82**]	1	0.25
Kanicki [**81**]	1.9	0.5
Negative Voltage Stress	α	β
In-house	2.2	0.25
Karim [**15**]	2.5	0.28
Kanicki [**81**]	2.4	0.32
Tsukada [**94**]	3.8	0.25

Bibliography

[1] M. J. Yaffe and J. A. Rowlands, “X-ray detectors for digital radiology,” Phys. Med. Biol., 42, pp. 1-39, (1997).

[2] J. A. Rowlands and J. Yorkston, “Flat panel detectors for digital radiography” in Handbook of Medical Imaging Vol. 1, edited by J. Beutel, H. L. Kundel and R. L. Van Metter (SPIE Press, Washington, 2000), Ch. 4 and references therein.

[3] D. C. Hunt, O. Tousignant, and J. A. Rowlands, “Evaluation of the imaging properties of an amorphous selenium-based flat panel detector for digital fluoroscopy,” Med. Phys., 31, pp. 1166-1175, (2004).

[4] V. N. Cooper III, T. Oshiro, C. H. Cagnon, L. W. Bassett, T. M. McLeod-Stockmann, N. V. Bezrukiy, “Evaluation of detector dynamic range in the x-ray exposure domain in mammography: A comparison between film-screen and flat panel detector systems,” Med. Ph.

[5] Larry E. Antonuk, Martin Koniczek, Youcef El-Mohri, and Qihua Zhao , “Active pixel and photon counting imagers based on poly-Si TFTs: rewriting the rule book on large area flat panel x-ray devices”, Proc. SPIE, 7258, (2009).

[6] E. Samei, and M. J. Flynn, “An experimental comparison of detector performance for direct and indirect digital radiography systems,” Med. Phys., 30, pp. 608-622, (2003).

[7] R. S. Saunders Jr., E. Samei, and C. Hoeschen, “Impact of resolution and noise characteristics of digital radiographic detectors on the detectability of Lung nodules,” Med. Phys., 31, pp. 1603-1613, (2004). 198.

[8] B. Polischuk, Z. Shukri, A. Legros, and H. Rougeot, “Selenium direct converter structure for static and dynamic x-ray detection in medical imaging,” Proc. SPIE, 3336, pp. 494-504, (1998).

[9] http://www.gizmag.com/samsung-digital-x-ray-detector/8396, accessed on: April 22, 2009.

[10] S. O. Kasap and J. A. Rowlands, “X-ray photoconductors and stabilized a-Se for direct conversion digital flat panel x-ray image detectors,” in Optoelectronics & Photonics: Principles and Practices, S.O. Kasap, (Prentice-Hall, Upper Saddle River, New Jersey.

[11] Farhad Taghibakhsh, Active Pixel Sensor Architectures for High Resolution Large Area Digital Imaging, PhD Thesis, University Of Waterloo, 2008.

[12] K.S. Karim, Pixel Architectures for Digital Imaging Using Amorphous Silicon Technology, PhD Thesis, University Of Waterloo, 2002.

[13] Handbook of Medical Imaging, 1, Physics and Psychophysics, Eds. J. Beutel, H.L. Kundel, R.L. Van Metter, SPIE, 2000, www.spie.org/bookstore/.

[14] W. Zhao and J. A. Rowlands, “Digital radiology using active matrix readout of amorphous selenium: Theoretical analysis of detective quantum efficiency,” Medical Physics, 24(12), pp. 1819-1833, 1997.

[15] K. S. Karim, Pixel Architectures for Digital Imaging Using Amorphous Silicon Technology, PhD Thesis, University Of Waterloo, 2002.

[16] M. Z. Kabir, Modeling of x-ray photoconductors for x-ray image detectors, PhD Thesis, University of Saskatchewan , 2005.

[17] M.H. Izadi, K.S. Karim, "High dynamic range pixel architecture for advanced diagnostic medical X-ray imaging applications," Journal of Vacuum Science and Technology A, 24(3), pp 846-849, May 2006.

[18] F. Taghibakhsh, K.S. Karim, "Two-Transistor Active Pixel Sensor Readout Circuits in Amorphous Silicon Technology for High Resolution Digital Imaging Applications," IEEE Transactions on Electron Devices, 55(8), pp. 2121-2128, August 2008.

[19] N. Safavian, J. Lai, A. Nathan, “Threshold voltage shift compensated active pixel sensor array for digital X-ray imaging in a-Si technology”, Electronics Letters, 41, pp.411-412, 2005.

[20] K.S. Karim, A. Nathan, “Readout circuit in active pixel sensors in amorphous silicon technology,” IEEE Electron Device Letters, 22(10), pp. 469-471, 2001.

[21] G. R. Chaji, N. Safavian, A. Nathan,”Dynamic-effect compensating technique for stable a-Si:H AMOLED displays”, 48th Midwest Symposium on Circuits and Systems, pp. 786-789, Aug. 2005.

[22] N. Safavian, D. Wu, K. Karim, A. Nathan, “Transient response of a 3-TFT hybrid active-passive pixel with correlated double sampling CMOS readout circuit for real-time medical X-ray imaging”, Microsystems and Nanoelectronics Research Conference, pp. 85.

[23] Shahin Jafarabadiashtiani, Pixel Circuits and Driving Schemes for Active-Matrix Organic Light-Emitting Diode Displays, PhD thesis, University Of Waterloo, 2007.

[24] N. Safavian, G. R. Chaji, A. Nathan, J. A. Rowlands,”Three-TFT image sensor for real-time digital X-ray imaging”,Electronics Letters, 42, pp. 150-151, 2006.

[25] A. Nathan, A. Kumar, K. Sakariya, P. Servati, S. Sambandan, and D. Striakhilev, “Amorphous silicon thin film transistor circuit integration for organic LED displays on glass and plastic,” IEEE J. Solid-State Circuits, vol. 39, no. 9, pp. 1477–1486, Sep. 2002.

[26] K. S. Karim, A. Nathan, and J. A. Rowlands, “Alternate pixel architectures for large area medical

imaging," in Proc. SPIE's International Symposium on Medical Imaging, San Diego, CA, Feb. 17–23, 2001.

[27] K. S. Karim, A. Nathan, J. A. Rowlands, "Amorphous Silicon Active Pixel Sensor Readout Circuit for Digital Imaging", IEEE Transactions on Electron Devices, 50(1), pp. 200- 208, 2003.

[28] S. J. Ashtiani, P. Servati, D. Striakhilev, and A. Nathan, "A 3-TFT current-programmed pixel circuit for active-matrix organic light-emitting diode displays," IEEE Trans. Electron Devices, vol. 52, no. 7, pp.1514–1518, Jul. 2005.

[29] C. Toumazou, F. J. Lidgey, and D. G. Haigh, Eds., "Analogue IC Design: The Current-Mode Approach" Stevenage, U.K.: Peregrinus, 1990.

[30] J. Rhayem, D. Rigaud, M. Valenza, N. Szydlo, H. Lebrun, "1/f noise investigations in long channel length amorphous silicon thin-film transistors," Journal of Applied Physics, 87(4), pp. 1983-1989, 2000.

[31] M. Rahal, M. Lee, and A. P. Burdett, "Flicker noise in Gate Overlapped Polycrystalline Silicon Thin-Film Transistors", IEEE Transactions on Electron Devices, 49(2), pp. 319-323, 2002.

[32] J.M. Boudry and L.E. Antonuk, "Current-noise-power spectra of amorphous silicon thin-film transistors," Journal of Applied Physics, 76, pp. 2529-2534,1994.

[33] S. Adachi, S. Hirasawa, M. Takahashi, H. Okada, Y. Yamane, and S. Yamada, "Noise Properties of a Se-based Flat-Panel X-ray Detector with CMOS Readout Integrated Circuits", Proc. SPIE, vol. 4682, pp.580-591, 2002.

[34] M.H. Izadi, K.S. Karim, "Noise optimisation analysis of an active pixel sensor for low-noise real-time X-ray fluoroscopy", IET Circuits, Devices & Systems, vol. 1, no. 3, pp. 251-256, June 2007.

[35] N. Matsuura, W. Zhao, Z. Huang, J.A. Rowlands, "Digital radiology using active matrix readout: Amplified pixel detector array for fluoroscopy", Medical Physics, 26(5), pp. 672-681, 1999.

[36] D.M. Hunter et al., "High-resolution (20 cycles/mm) digital X-ray mammography using amorphous selenium directly coupled to CCD readout devices", Proc. SPIE, vol. 5368, pp.466-477, 2004.

[37] L. McIlrath, V. Clark, P. Duane, D. McGrath, W. Waskurak, "Design and analysis of a 512×768 current-mediated active pixel array image sensor," IEEE Transactions on Electron Devices, 44(10), pp. 1706-1715, 1997.

[38] C. Enz and G. Temes, "Circuit technique for reducing the effects of circuit imperfections," Proc. IEEE, vol. 84, no. 11, pp. 1586–1614, Nov. 1996.

[39] P. Servati, S. Striakhilev, and A. Nathan, "Above-threshold parameter extraction and modeling for amorphous silicon thin film transistors," IEEE Trans. Electron Devices, 2003, 50, pp. 2227-2235.

[40] Johns, D and Martin, K.W., “Analog Integrated Circuit Design”, John Wiley & Sons, 1997.

[41] D. A. Johns, K. Martin., “Analog integrated circuit design”, Canada, John Wiley & Sons, 1996.

[42] A. Nathan, A. Kumar, K. Sakariya, P. Servati, S. Sambandan, and D. Striakhilev, “Amorphous silicon thin film transistor circuit integration for organic LED displays on glass and plastic,” IEEE J. Solid-State Circuits, vol. 39, no. 9, pp. 215-222, 2003.

[43] C Wu, C Chen, M Tsa, and C Cho, “A 0 5 mA offset-free current comparator for high precision current-mode signal processing,” in Proc ISCAS’91, 1991.

[44] Palmisano, G.; Palumbo, G.,”High performance CMOS current comparator design”, IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 43, pp. 785- 790, 1996.

[45] J Shieh, M Patil and R Shen “Measurement and analysis of charge injection in MOS analog switches,” IEEE J Solid-State Circuits, vol SC 22, pp 277-281, Apr 1987.

[46] G Wegmann, E Vittoz, and F Rahali, ‘Charge injection in analog MOS switches,” IEEE J Solid-State Circuits, vol SC-22, pp 1091-1 1097,Dec 1987.

[47] N. Safavian, K.S. Karim,A. Nathan, J. A. Rowlands,” A 3-TFT hybrid active-passive pixel with correlated double sampling CMOS readout circuit for real-time medical x-ray imaging”, 34th European Solid-State Circuits Conference, 15-19 Sept. 2008 pp. 122 – 125, 15-19 sept, 2008.

[48] H. Elwan, A. M. Soliman, and M. Ismail, “A CMOS norton amplifier-based digitally controlled VGA for low-power wireless applications,” IEEE J. Solid-State Circuits, vol. 48, no. 3, pp. 245-254, Sept. 2004.

[49] A.S. Sedra, G.W. Roberts, and F. Gohh, “The current conveyor: history, progress and new results,” IEE Proc. G., Electron. Circuits Syst., vol. 137, (2), pp. 78-87, 1990.

[50] N. Safavian, G.R. Chaji, S. J Ashtiani, A. Nathan, J.A. Rowlands, ”Self-compensated a-Si:H detector with current-mode readout circuit for digital X-ray fluoroscopy Source”, IEEE International 48th Midwest Symposium on Circuits and Systems, pp. 774-777, 2005.

[51] N. Safavian, G.R. Chaji, S. J Ashtiani, A. Nathan, J.A. Rowlands, , “TFT active image sensor with current-mode readout circuit for digital x-ray fluoroscopy”, SPIE photonics North, pp. 29-38, 2005.

[52] S.K. Mendis, S.E. Kemeny, and E.R. Fossum, “CMOS active pixel image sensor,” IEEE Transactions on Electron Devices, 41(3), pp. 452-453, 1994.

[53] N. Safavian, G.R. Chaji, S. J Ashtiani, A. Nathan, J.A. Rowlands, “A novel current scaling active pixel sensor with correlated double sampling readout circuit for real time medical X-ray imaging, IEEE International Symposium on Circuits and Systems, pp. 93-96, 27-30 May, 2007.

[54] H. P. Forghani-Zadeh, G. A. Rincon Mora, “A Programmable 210µV Offset Rail-to-Rail Gm–C Filter” , IEEE Transactions on Circuits and Systems-I, Vol. 54, No. 8, August 2007.

[55] M. Choquette, Y. Demers, Z. Shukri, O. Tousignant, K. Aoki, M. Honda, A. Takahashi, and A. Tsukamoto, “Performance of a real time selenium based x-ray detector for fluoroscopy,” Proc. SPIE, 4320, pp. 501-508, (2001).

[56] R. A. Street, Hydrogenated Amorphous Silicon, London, Cambridge University Press, 1991.

[57] S. Tokuda, S. Adachi, T. Sato, T. Yoshimuta, H. Nagata, K. Uehara, Y. Izumi, O. Teranuma, and S. Yamada, “Experimental evaluation of a novel CdZnTe flat-panel x-ray detector for digital radiography and fluoroscopy,” Proc. SPIE 4320, pp. 140-147, (2001).

[58] H. P. Chan and K. Doi, “Energy and angular dependence of x-ray absorption and its effect on radiographic response in screen-film systems,” Phys. Med. Biol. 28, pp. 565-579, (1983).

[59] J. M. Sandrik and R. F. Wagner, ‘‘Absolute measures of physical image quality: Measurement and application to radiographic magnification,’’ Med. Phys. 9, 540–549, 1982.

[60] J. H. Siewerdsen, L. E. Antonuk, and J. Yorkston, ‘‘Theoretical performance of amorphous silicon imagers in diagnostic radiology,’’ Proc.SPIE 2708, 484–493 , 1996.

[61] Zuck, M. Schieber, O. Khakhan, and Z. Burshtein, “Near single-crystal electrical properties of polycrystalline HgI2 produced by physical vapor deposition,” IEEE Trans. Nucl. Sci., 50, pp. 991-997, (2003).

[62] I. M. Blevis, D. C. Hunt, and J. A. Rowlands, “X-ray imaging using amorphous selenium: Determination of Swank factor by pulse height spectroscopy,” Med. Phys. 25, pp. 638-641, (1998).

[63] J. G. Mainprize, D. C. Hunt, and M. J. Yaffe, “Direct conversion detectors: the effect of incomplete charge collection on detective quantum efficiency,” Med. Phys., 29, pp. 976-990, (2002).

[64] W. Zhao and J. A. Rowlands, “X-ray imaging using amorphous selenium: Feasibility of a flat panel self-scanned detector for digital radiology,”Med. Phys., vol. 22, no. 10, pp. 1595–1604, 1995.

[65] G. Pang, W. Zhao and J.A. Rowlands, “Digital radiology using active matrix readout of amorphous selenium: geometric and effective fill factors,” Med. Phys. 25, pp. 1636-1646, (1998).

[66] I. M. Blevis, D. C. Hunt, and J. A. Rowlands, “Measurement of X-ray photogeneration in amorphous selenium,” J. Appl. Phys., 85, pp. 7958-7963, (1999).

[67] M. F. Stone, W. Zhao, B. V. Jacak, P. O'Conner, B. Yu, and P. Rehak, "The x-ray sensitivity of amorphous selenium for mammography," Med. Phys., 29, pp. 319-324, (2002).

[68] A. Ruzin and Y. Nemirovsky, "Statistical models for charge collection efficiency and variance in semiconductor spectrometers," J. Appl. Phys. 82, pp. 2754-2758, (1997).

[69] M. Zahangir Kabir and S. O. Kasap, "Charge collection and absorption-limited sensitivity of x-ray photoconductors: Applications to a-Se and HgI2," Appl. Phys. Lett., 80, pp. 1664-1666, (2002).

[70] M. Zahangir Kabir and S. O. Kasap, "Sensitivity of x-ray photoconductors: Charge trapping and absorption-limited universal sensitivity curves," J. Vac. Sci. Tech. A, 20, pp. 1082-1086, (2002).

[71] M. Zahangir Kabir and S. O. Kasap, "Dependence of the DQE of photoconductive X-ray detectors on charge transport and trapping," Proc. SPIE – Int. Soc. Opt. Eng., 4682, pp. 42-52, (2002).

[72] M. J. Powell, "The Physics of Amorphous-Silicon Thin-Film Transistors," IEEE Trans. Electron Devices, vol. 36, no. 12, pp. 2753-2763, Dec. 1989.

[73] A. Nathan, P. Servati, A. Sazonov, D. Stryahilev, and K.S. Karim, a-Si:H TFTs on glass and plastic in a-Si:H Thin Film Transistors, Ed: Y. Kuo, Kluwer Academic Publishers (2003) 79- 181.

[74] S. M. GadelRab and S. G. Chamberlain, "Thick-layered etched-contact amorphous silicon transistors," IEEE Trans. Electron Devices, vol. 45, pp. 465-471, 1998. 157.

[75] S. GadelRab, A. Miri and S. Chamberlain, "A comparison of the performance and reliability of wet-etched and dry-etched a-Si: H TFTs," Electron Devices, IEEE Transactions on, vol. 45, pp. 560-563, 1998.

[76] R. A. Street, Hydrogenated Amorphous Silicon, London, Cambridge University Press, 1991.

[77] M. J. Powell, C. van Berkel, and J. R. Hughes, "Time and temperature dependence of instability mechanisms in amorphous silicon thin-film transistors," App. Phys. Lett., vol. 54, no. 14, pp. 1323-1325, April 1989. 159.

[78] P. Servati and A. Nathan, "Modeling of the reverse characteristics of a-Si:H TFTs," IEEE Trans. Electron Devices, vol. 49, no. 5, pp. 812-819, 2002.

[79] C. van Berkel, and M. J. Powell, "Resolution of amorphous silicon thin-film transistor instability mechanisms using ambipolar transistors," App. Phys. Lett., vol. 51, no. 14, pp. 1094-1096, 1987.

[80] S. Sambandan and A. Nathan, "Equivalent circuit description of threshold voltage shift in a-Si:H TFTs from a probabilistic analysis of carrier population dynamics," IEEE Trans. Electron Devices, vol. 53, pp. 2306-11, 2006.

[81] C.-S. Chiang, J. Kanicki, and K. Takechi, "Electrical instability of hydrogenated amorphous silicon

thin-film transistors for active-matrix liquid-crystal displays," Jpn. J.Appl. Phys., Part 1, vol. 37, no.11, pp. 4704-4710, 1998.

[82] F. R. Libsch and J. Kanicki, "Bias-stress-induced stretch-exponential time dependence of charge injection and trapping in amorphous silicon thin-flm transistors," Appl. Phys. Lett., vol. 62, no. 11, pp. 1286-1288, 1993.

[83] Ya-Hsiang Tai, Jun-Wei Tsai, Huang-Chung Cheng and Feng-Cheng Su, "Instability mechanisms for the hydrogenated amorphous silicon thin-film transistors with negative and positive bias stresses on the gate electrodes," Appl. Phys. Lett., vol. 67, pp. 76-78.

[84] W. B. Jackson, M. Marshall, and M. D. Moyer, "Role of hydrogen in the formation of metastable defects in hydrogenated amorphous silicon," Phys. Rev. B, vol. 39, no. 2, pp. 1164-1179, 1989.

[85] A. Akavan Fooman, Threshold Voltage Instability and Relaxation in Hydrogenated Amorphous Silicon Thin Film Transistors, Master thesis, University of Waterloo, 2005.

[86] M. J. Powell, C. van Berkel, I. D. French and D. H. Nicholls, "Bias dependence of instability mechanisms in amorphous silicon thin-film transistors," Appl. Phys. Lett., vol. 51, pp. 1242- 4, 10/19. 1987.

[87] N. Safavian, M. Yazdandoost, D. Wu, A,Sultana, M. H. Izadi, K.S. Karim,A. Nathan, J. A. Rowlands, Characterization of current programmed amorphous silicon active pixel sensor readout circuit for dual mode diagnostic digital x-ray imaging , in *Medical Imaging 2009: Physics of Medical Imaging*, SPIE 7258, Feb 2009.

[88] W. Lee, G. W. Neudeck, J. Choi, and S. Luan, " A model for the temperature-dependent saturated ID-VD characteristics of an a-Si:H thin-film transistor," IEEE Trans. Electron Devices, vol. 38, no. 9, pp. 2070-2074, 1991.

[89] A. M. Miri and S. G. Chamberlain, "A totally wet etch fabrication technology for amorphous silicon thin film transistors," in Amorphous Silicon Technology - 1995. Symposium, pp. 737- 742, 1995.

[90] M. Hack, M. S. Shur, and J. G. Shaw, "Physical models for amorphous silicon thin-film transistors and their implementation in a circuit simulation program," IEEE Trans. Electron Devices, vol. 36, no. 12, pp. 2764-2769, 1989.

[91] M. Shur, M. Hack, and J. G. Shaw, "A new analytical model for amorphous silicon thin-film transistors," J. Appl. Phys., vol. 66, no.7, pp. 3371-3380, 1989.

[92] M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owusu, and T. Ytterdal, "SPICE models for amorphous silicon and polysilicon thin film transistors," J. Electrochem.Soc., vol. 144, no. 8, pp. 2833-2839, 1997.

[93] M.J. Powell, S.C. Deane, W.I. Milne, “Bias-stress-induced creation and removal of dangling-bond states in amorphous silicon thin-film transistors,” Applied Physics Letters,60 (2), p. 207, 1991.

[94] R. Oritsuki, T. Horii, A. Sasano, K. Tsutsui, T. Koizumi, Y. Kaneko, and T. Tsukada, Threshold Voltage Shift of Amorphous Silicon Thin-Film Transistors During Pulse Operation,” Jpn. J. Appl. Phys., 30, Part 1, No. 12B, pp. 3719-3723, 1991.

[95] A. Sultana, N. Safavian, M. H. Izadi, K. S. Karim, J. A. Rowlands,”Characterization of bias induced metastability of amorphous silicon thin film transistor based passive pixel sensor switch and its impact on biomedical x-ray imaging application “,in Medical Imaging 2009: Physics of Medical Imaging, SPIE 7258, Feb 2009.