Monolithic RF Frequency Synthesis for Wireless Communications

by

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Abstract

The increasing demand for a small sized, low cost wireless transceivers with a long battery life calls for a move towards higher levels of integration. However, the design of the frequency synthesizer hinders the development of a fully integrated wireless radio, because of the stringent phase noise requirements for both the transmit and receive synthesizers. Moreover, the synthesizers require fast switching speeds, low spur levels, and reduced sensitivity to interference caused by other components sharing the same power supply and/or substrate. Unlike other radio components, the synthesizer is active most of the time. Therefore, minimizing its power consumption is critical for a longer battery life.

Traditionally, the VCO has dominated the phase noise in the design of the frequency synthesizer. The key has been the use of an off-chip VCO module with high Q discrete resonators to realize the low phase noise requirement. The lack of high Q integrated resonators constitutes a major challenge towards integrating the VCO. Also, applications of integrated VCO's are limited, due to the large fabrication tolerances in the integrated varactor values. Consequently, a wide VCO tuning range is needed to cover the process variations, using only a limited control voltage range. However, this high tuning sensitivity exposes the VCO to more noise pick up.

The objective of this thesis is to provide both circuit and system level solutions to enhance the performance of integrated frequency synthesizers. On the circuit level, two VCO architectures are presented, to reduce the VCO phase noise, as well as its sensitivity to noise pick up. A fully differential PLL (including the VCO) is integrated on a single chip in a 0.5 micron CMOS process. The differential architecture reduces the circuit sensitivity to both supply and substrate noise. A novel technique is used to differentially control the LC VCO without sacrificing the tuning range. The measured VCO phase noise is -119 dBc at 1 MHz offset, and its tuning range is 26% around its 1.25 GHz center frequency. The PLL in-band phase noise is -96 dBc with a total power consumption of 13.6 mA from a 3 V supply.

In order to reduce the VCO phase noise, we propose a VCO architecture based on coupled tank resonators. The coupled tanks provide a higher frequency selectivity, that reduces the phase noise. The phase noise is further reduced by cascading four of these resonators in a ring VCO structure, that provides accurate quadrature outputs. The proposed VCO is designed in a 0.35 micron CMOS technology, and achieves a phase noise as low as -122 dBc at 600 kHz offset from a 1.93 GHz oscillator center frequency with a current consumption of 9.2 mA. This phase noise is significantly better than other I-Q VCO implementations reported in the literature with similar power consumption.

On the synthesizer system architecture level, many researchers have proposed the use of wide band PLLs to relax the VCO phase noise requirements. Not only does this ease the VCO design, but also increases the synthesizer switching speed. Fractional-N frequency division is a very popular way to increase the PLL loop

band width without changing the channel spacing. Following this trend, we pursue a detailed circuit level implementation of a fractional-N synthesizer with an on chip spur compensation. This compensation technique relies on a digitally controlled delay to shift the fractional divider output so that no phase error is produced. Even though this technique has, theoretically, no systematic error, circuit level simulations do show high levels of fractional spurs. It seems that a more drastic system architecture change is required.

Therefore, we present a phase domain fractional-N frequency synthesizer architecture that achieves high switching speeds and a very narrow channel spacing. In this architecture, a numerical phase comparator is used as a linear *Weighted Phase Frequency Detector*. The output spur level is limited by the delay of the numerical phase comparator, and the accuracy of the DAC used to convert the phase error to the analog domain. A novel timing error cancelation scheme that is capable of eliminating the effect of the phase comparator delays, is proposed. With this technique and a 10-bit accuracy DAC, the simulated spur level is as low as -65 dBc. The settling time is less than 7 μs, and is independent of the channel spacing. The advantages of the synthesizer architecture, design considerations, and system level simulations are discussed.

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Chapter 1

Introduction

Currently, the wireless communications market is rapidly expanding. Not only is this due to the increasing number of cellular phone users, but also new services such as wireless LAN, two-way pagers, and hand held web browsers.

Unlike that of wire-line communication systems, the capacity of the wireless media is limited by the available frequency spectrum. Consequently, new standards with very sophisticated protocols and modulation schemes are being introduced to efficiently utilize the limited spectrum. This sets very stringent performance requirements for radio design. As a consumer product, hand held terminals should also have a small size, low cost, and long battery life. In addition to meeting the system specification, a large number of companies competing in the wireless market are focusing on these three factors. A move towards higher levels of integration may determine who the winners will be in this competition. Higher integration not only reduces the size and the cost of the radio, but also decrease its power consumption. This reduction in power consumption is attributed to the elimination of the many

buffering stages needed for inter-chip communication.

In silicon technologies, the development of submicron and deep submicron lithographies, has greatly improved the speed, size, and power consumption for digital circuits. For analog circuits, submicron technologies have made it possible, for the first time, to integrate some of the RF front end components that run in the low gigahertz frequency range. These RF components include power amplifiers, low noise amplifiers, mixers, and frequency synthesizers. For many years, Bipolar technologies have been exclusively used for RF analog design, and CMOS is exclusively used for digital design. Now, though, the increased speed of CMOS devices is also attracting more analog RF designers, because of their low cost and potential for higher integration. In this work we follow that trend and use only CMOS technology for all our designs.

We already realize that all RF components are very sensitive, and therefore, challenging to integrate, but it is the frequency synthesizer that hinders a fully integrated transceiver, because of the very high signal purity requirements set by the limited spectrum. A typical frequency synthesizer should have an RF output frequency in the (1~3 GHz) range, a very narrow channel spacing, a high switching speed, and extremely low phase noise and spur levels.

In order to meet this tough phase noise requirement, an external voltage controlled oscillator (VCO) module is usually required. This VCO utilizes discrete, high quality, and expensive resonators to lower the phase noise. However, the absence of high quality passive inductors and varactors on silicon chips has challenged the VCO integration. The second obstacle to the integration of the frequency syn-

thesizer is the limited substrate isolation, which complicates the integration of this sensitive component with the other noisy components on the same chip.

Our purpose in this thesis is to provide solutions both at the circuit level and the system level to enhance the performance of integrated frequency synthesizers. The technology improvements, by increasing the quality factor of integrated passive components, have a significant impact on the achievable performance. No less important are the innovations on the circuit and architecture levels. With the current state of the art integrated inductor quality factor around 10, it is very difficult to meet the phase noise requirements using conventional VCO and synthesizer designs. Therefore, several architectural variations both on the circuit and the system level are presented to improve the performance of the integrated synthesizers. Although circuit design directly influences the VCO phase noise, different synthesizer architecture variations are also important in order to relax the requirements on the VCO without sacrificing the overall spectral purity. In addition we focus on the circuits' sensitivity to interference caused by other components sharing the same power supply and/or substrate.

In this work, we concentrate on three main tasks to facilitate the integration of the frequency synthesizer. The first is to transform the frequency synthesizer architecture into a differential one to reduce the sensitivity to both supply and substrate noise. This step is critical if we want to use an integrated VCO. Usually, an integrated VCO has a wide tolerance in its center frequency that mandates a wide tuning range. Because of the limited VCO control voltage range, a high VCO gain is needed in order to cover this large tuning range. However, this high VCO

gain makes it more vulnerable to noise pick up. The second task is to design an integrated VCO that has a lower phase noise, and is capable of providing quadrature outputs. Such outputs are important for many transceiver architectures, and are not available in discrete VCO's. Finally, we investigate the use of fractional-N frequency synthesis techniques, as well as other architectural variations to open up the PLL loop bandwidth and relax the VCO phase noise requirements.

The integration of the above three aspects on a single chip is an ultimate goal for this work. However, due to time constraints and potential risks, we approach one problem at a time. This also reduces the complexity to gain more insight.

After this introduction, the thesis begins in chapter 2 with a brief overview of basic wireless transceiver architectures, and their impact on frequency synthesis requirements. We also review the different frequency synthesis techniques. Chapter 3 is devoted to the VCO basics, where we discuss various VCO architectures, noise performance and analysis techniques.

In chapter 4 we introduce a fully differential PLL implementation. The PLL architecture is based on a novel monolithic LC tuned VCO architecture that has differential control. A new and simple common mode control scheme is used for the control voltages without introducing more noise. Unlike previous architectures, this common mode control technique doesn't require a clean reference. When implemented in a 0.5 μm CMOS technology, the VCO control scheme provides more than 46 dB common mode rejection at low frequencies with less than 1 dB degradation in the phase noise. The measured VCO tuning range is around 26%, the highest reported in literature for an LC tuned integrated VCO. The PLL which consumes

13.6 mA from a 3 V supply achieves a -96 dBc in-band noise level at 30 KHz offset from the carrier.

Chapter 5 concentrates on lowering the phase noise of the VCO. Coupled tank resonators provide higher frequency selectivity to lessen the phase noise. Four resonators are cascaded in a new ring LC VCO architecture that not only provides I-Q outputs, but also improves the phase noise performance. Like other I-Q VCO architectures, this design doubles both the chip area and power consumption in order to produce the quadrature outputs. However, it provides a significant improvement in the phase noise, at no extra cost. A 1.93 GHz VCO prototype is designed in a 0.35 μm technology and provides accurate I-Q outputs. The measured phase noise is -122 dBc at 600KHz offset, and a total power consumption of 9.2 mA from a 3 V supply.

Chapter 6 deals with the practical implementation of a fractional-N synthesizer that has an on chip phase error compensation circuitry. The fractional spurs are compensated for, by using a digitally controlled delay to shift the rising edges of the fractional divider output so that no phase error is detected. Theoretically, this compensation technique has no systematic error and appears to be limited only by the device matching on the chip. However, a detailed circuit level analysis and simulations are used to illustrate that relatively high fractional spurs exist even with perfect matching.

Finally, in chapter 7 we take the fractional-N frequency synthesis one step further by proposing a synthesizer architecture that performs the fractional division in the phase domain. A numerical phase comparator is used as a *Weighted Phase*

Frequency Detector. The resulting synthesizer achieves high switching speeds while permitting very narrow channel spacing. The output spur level is limited by both the delay of the numerical phase comparator, as well as the accuracy of the DAC used to convert its phase error output to the analog domain. A novel timing error cancelation scheme that is capable of eliminating the effect of the phase comparator delays is presented. With the use of this technique and a 10-bit accuracy DAC, the simulated spur level is as low as -65 dBc. A thorough analysis and system level simulations of the proposed architecture are detailed. We also identify implementation challenges, and propose solutions. In the conclusion of the thesis, we discuss our research and suggest future work.

Chapter 2

Frequency Synthesis Overview

2.1 Wireless Transceiver & Synthesizer Requirements

In a wireless transceiver, the frequency synthesizer is used to precisely generate a digitally selected local oscillator (LO) output frequency that corresponds to one of several closely spaced channels. The specifications of the frequency synthesizer include the output frequency range, channel spacing, the number of channels, spectral purity, switching speed, and the center frequency accuracy. Communication standards usually define the synthesizer requirements. Table 2.1 summarizes the most popular wireless communication standards including those of cellular phones, cordless phones, and wireless LAN's. The most important requirement for a frequency synthesizer is the spectral purity of the output frequency. The spectral purity has two parameters: the phase noise and the spurious sidebands. As will be

detailed in section 2.2.3, the phase noise defines the short term center frequency jitter and appears in the frequency domain as skirts around the carrier, whereas spurious sidebands are fixed frequency tones on both sides of the carrier (Fig. 2.1).

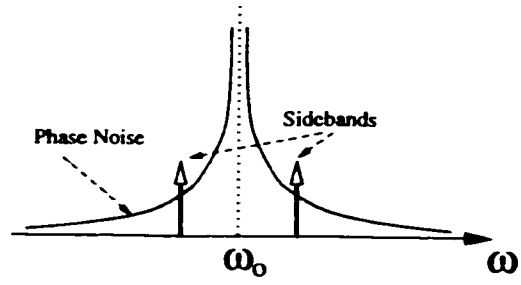


Figure 2.1: Typical frequency synthesizer output in the frequency domain

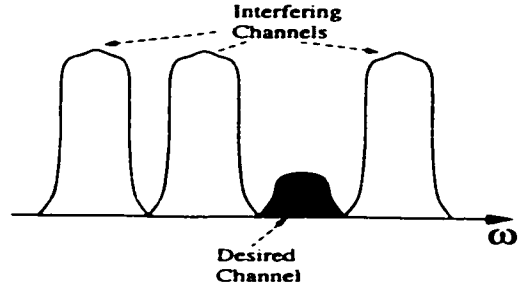


Figure 2.2: A weak desired channel surrounded by strong interferer(s)

Even though the frequency synthesizers for both the receiver and transmitter have different spectral purity specifications, they arise from the same concept. As shown in Fig. 2.2, a very weak desired channel signal may be surrounded by strong unwanted channels. To further explain this we depict the typical heterodyne transceiver in Fig. 2.3. For the transmitter, an upconverter is used to mix the baseband DAC outputs with the transmitter synthesizer signal to generate an RF signal. The center frequency of this RF signal is defined by the synthesizer. Its

Parameter	AMPS	IS54	GSM	JCP	DECT	CT2	PHP	802.11FH
Origin	EIA/TIA	EIA/TIA	ETSI		ETSI	UK	Japan	IEEE
Access	FDD	FDM/FDD/TDM	FDM/FDD/TDM		FDM/TDM/TDM	FDM/TDD	TDM/TDD	FH/FDM
Modulation	FM	pi/4QPSK	GMSK, diff	pi/4DQPSK	GPSK	GPSK	pi/4DQPSK	(G)FSK
RF channel frequencies (MHz)	824.04-848.97(X), 869.04-893.97(R)	824.04-848.97(X), 869.04-893.97(R)	890-915(X), 935-960(R)		1897.3-1881.8	864.15-868.05	1895-1911	2400-2500
No. of RF channels	833	833	124	1600	10	40	52	75
Channel spacing	30KHz	30KHz	200KHz		1.728MHz	10KHz	300KHz	1MHz
Synthesizer switching speed	slow	slow			30μs(BS) 450μs(HS)	1ms(ch-ch) 2ms	30μs(BS) 1.5ms(HS)	several μs
Frequency accuracy	2.5ppm	200Hz			50KHz	10KHz	3ppm	
Peak power	3W(6max)	3W(6max)	3W(20max)		250mW	10mW	100mW	1W

Table 2.1: Summary of cellular phone, cordless phone and wireless LAN standards [1]

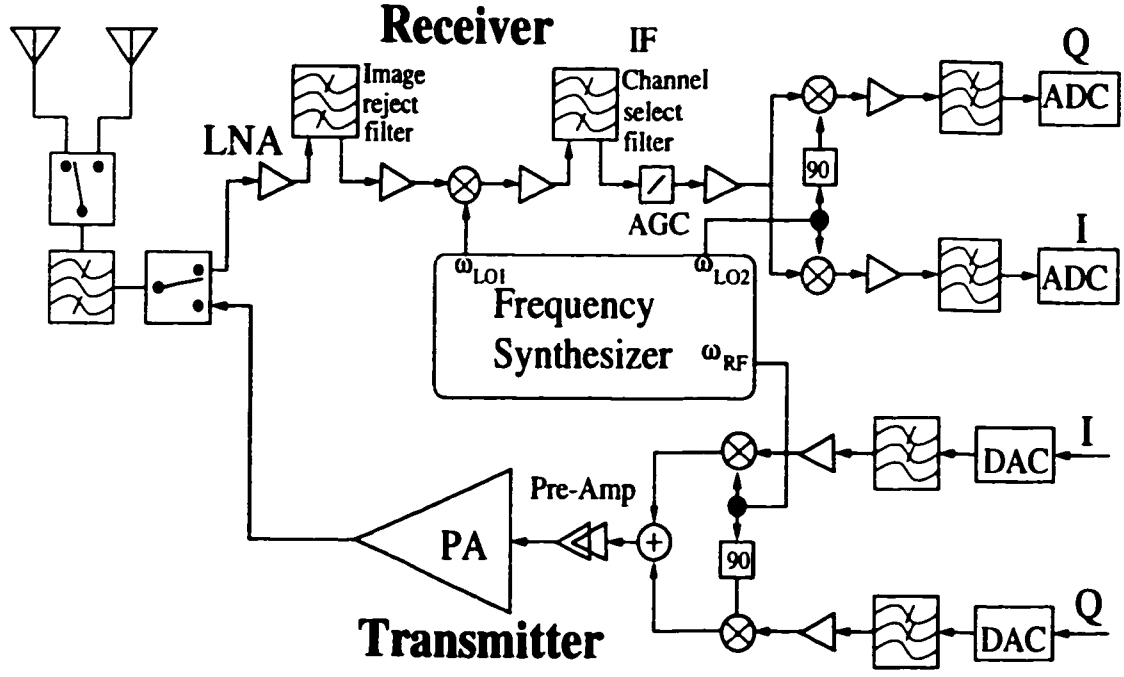


Figure 2.3: Block diagram of a typical heterodyne transceiver

bandwidth (BW) is equal to the BW of the baseband DAC output. This RF signal is then amplified by a power amplifier and fed to the antenna. The synthesizer phase noise skirts and its spurious sidebands directly add to the transmitted RF signal and are not filtered by the RF filter. Their out-of-band components act as interferers to adjacent channels. The spurious tone and phase noise levels of the transmitter are then specified so as to contain the signal to noise ratio (SNR) degradation of a weak channel, due to the interference of strong adjacent channels.

The situation is different for the receiver. After traveling through a low noise amplifier (LNA) and then an image reject filter, the received RF signal is down-converted to a fixed IF frequency. Channel selection is achieved through mixing with a synthesized frequency equal to the desired channel frequency minus the IF frequency. A sharp IF filter is then used to reject the unwanted channels. The image reject filter is important to filter out any signal or noise at frequencies 2*IF away from the desired signal, which would be converted to exactly the IF frequency and corrupt the desired signal. The IF frequency should be kept high enough to relax the requirements of this filter. Further corruption evolves as the strong in-band interfering channels mix with the LO phase noise skirts and/or spurious side bands to the IF frequency. This effect cannot be filtered out. Thus, a stringent requirements are set on the LO spectral purity.

Consequently, we can conclude that the phase noise and the spurious sidebands of the receiver synthesizer are more serious than those of the transmitter; the noise and sidebands directly add interfering information from the adjacent channels to the desired channel information. In the transmitter, they effectively increase the

overall system noise floor.

Even though the spectral purity requirement is not listed in Table 2.1, we can still predict how stringent they are for the different standards by noting the effect of the other parameters in the table. Cellular systems transmit higher power than the cordless ones to cover the wider cells. The result is a higher dynamic range (typically 100 dB) for the different channel signals. To achieve the same receiver sensitivity (the minimum signal level that can be satisfactorily detected), an LO with higher spectral purity is required to minimize the effect of the strong blocking channels. The channel spacing is also important; smaller channel spacing means tougher phase noise specifications. As will be discussed in section 2.2.3, this narrow channel spacing makes the spurious sidebands more profound. The modulation technique also affects the spectral purity requirement for a specific error rate (BER) for digital systems, or signal to noise ratio (SNR) for analog systems [2]. GSM, which requires an LO with phase noise less than -121dBc/Hz@600KHzoffset from the carrier, is an example of tough spectral purity specification. On the other hand, cordless phones have more relaxed values of -131dBc/Hz@4.7MHz for DECT, and -96dBc/Hz@100KHz for PHS. The frequency at which the phase noise specification is defined does not have to be equal to a single channel spacing and depends on the frequency allocation among the different cells in each standard. For example, in a GSM system the cells are arranged such that the first critical blocking channel is 600 KHz (or three channels) away from the channel of interest. We should also note that the phase noise increases with the square of the center frequency. So, it is more difficult to achieve the phase noise requirement for systems with carriers in

the range of 2.0 GHz than those in the range of 1.0 GHz.

Most current radio systems use frequency and phase modulation schemes where the RF signal is mixed with both the LO signal and its quadrature to provide phase information. In the conventional architecture shown in Fig. 2.3, this quadrature mixing is usually done at the second IF. In some architectures, these quadrature LO outputs may be required at the RF frequency. Two examples are direct conversion [3, 4] and low IF [5] receivers. The aim of these architectures is to eliminate the RF image reject filter, as well as the IF channel select filter to make them good candidates for a fully integrated transceiver. In a direct conversion receiver, a zero IF is used to place the image on the desired signal. The main problem with this architecture is the unavoidable time varying DC offset which corrupts the low frequency information of the signal. Several sources contribute to this offset including the LO leakage to the RF path mixing with itself, and the flicker noise of the front end electronics.

Many research groups are currently active addressing this DC offset problem [6]. One approach is to use a low IF instead of a zero IF, but this leads us back to the image reject problem. The trigonometric properties of the LO signal and its quadrature could be utilized to reject the image by using two mixers (see Fig. 2.4). The maximum achievable image rejection is limited by the accuracy of the 90° phase shift between the quadrature LO signals. An $RC - CR$ phase shift circuit could be used to generate these quadrature signals, but with a limited accuracy due the generally poor resistor and capacitor matching. The other limitation of this $RC - CR$ technique is the amplitude variation with frequency, which is con-

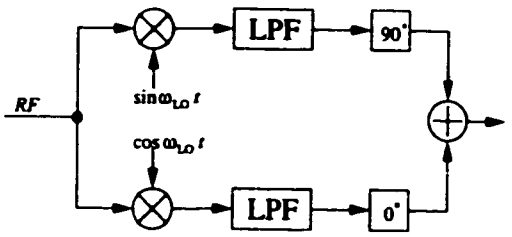


Figure 2.4: Image reject mixer

verted to frequency modulation due to the mixer nonlinearity. A commonly used technique is to generate double the required frequency and use an edge triggered Flip Flop divide-by-two to get the signal and its quadrature output. This technique is clearly an expensive one, as we push the circuit electronics to operate at twice the RF frequency. The accuracy of this method is limited by the deviation of the synthesizer signal from the 50% duty cycle. This imposes another requirement on the synthesizer output; that is, to have a minimum even harmonic content. Even though recent research [7] has promising results to accurately generate I and Q using integrated RC networks, it is highly desirable to have a synthesizer that inherently generates the signal and its quadrature such as those which use ring oscillators or other architectures [8].

Also, it should be mentioned that some radio architecture variations on the system level can simplify the implementation of the frequency synthesizer requirements. For example, Dr. Gray *et al* [9, 10] proposed a receiver architecture (Fig. 2.5) in which the high frequency channel select LO was replaced by a fixed high frequency LO followed by a channel select low frequency one. This relaxes the implementation of the phase noise and spurious sideband requirements for both LO's. For the fixed frequency LO, we can use a wideband PLL to relax the VCO phase

noise requirements. For the low frequency channel select LO the phase noise is much lower because of the low center frequency. Moreover, this architecture uses single sideband mixers to avoid the image reject filter. The DC offset due to direct conversion is corrected by using "DC offset current DAC". On the transmitter side, direct modulation of the synthesized frequency can help avoid LO frequency pulling by the power amplifier output (see Fig. 2.6) [11].

2.2 Frequency Synthesis Techniques

The challenge of frequency synthesizer design is as old as the radio industry itself. Several techniques have been used to implement this function. These techniques fall into four main categories: incoherent synthesis, coherent direct synthesis, direct digital synthesis, and indirect (or phase locked loop) synthesis. An incoherent synthesizer uses several sources, and switches their outputs to mixer inputs to get the desired output frequency through a tunable filter. The coherent direct synthesizer avoids the use of a large number of oscillators. It uses several mixers and frequency multipliers to generate all the required frequencies from a single reference frequency. The use of several filters, oscillators, and/or mixers in these two techniques makes them bulky, expensive, power consuming, and hence, unsuitable for integration in a wireless handset. The two other techniques are good candidates for fully integrated solutions, and will be detailed next.

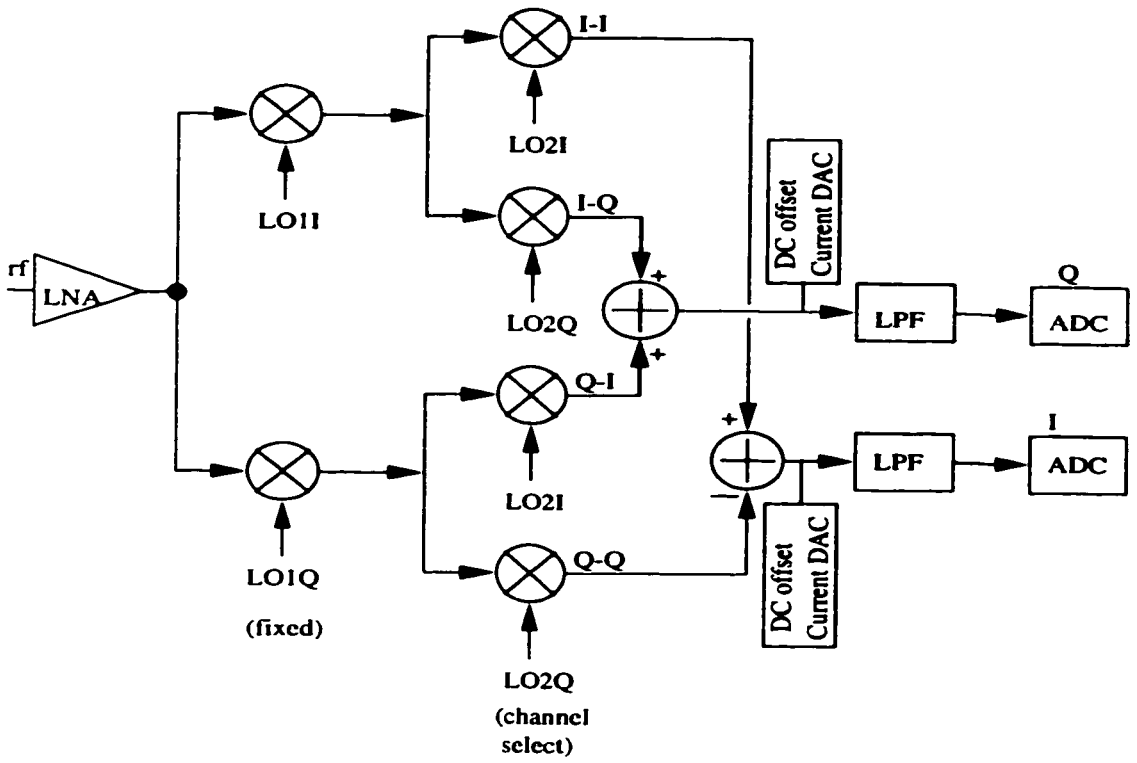


Figure 2.5: Receiver architecture with split frequency synthesis requirements

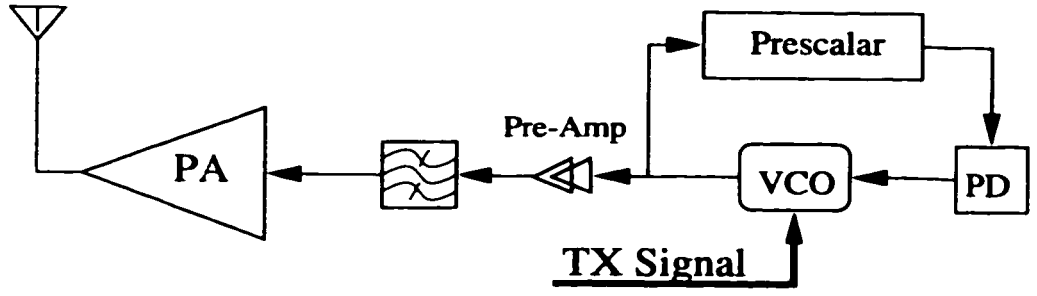


Figure 2.6: Direct modulation transmitter

2.2.1 Direct Digital Frequency Synthesizer (DDFS)

Recently, this technique has gained more attention as a result of the great development in digital integrated circuit technologies. The main idea here, as shown in Fig. 2.7, is to store several equally spaced samples of the trigonometric sine or cosine wave in a ROM lookup table. An input reference clock is used with an accumulator to increment the memory output address. A precise DAC, followed by an antialiasing filter, is used to convert this digital output to the desired frequency

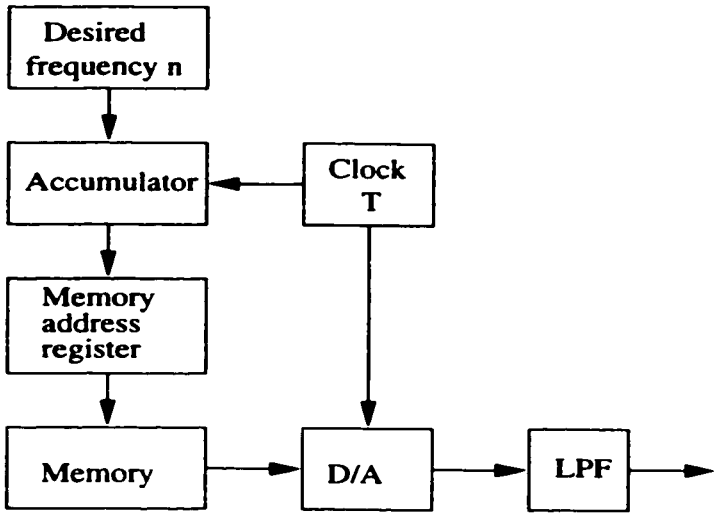


Figure 2.7: Block diagram of a direct digital frequency synthesizer

signal. Higher frequencies are obtained by controlling the accumulator increments so that the sine wave is scanned in a smaller number of clock cycles with a fewer samples. The number of the memory words determines the minimum achievable frequency, which is equal to the clock frequency divided by this number. This minimum frequency defines the synthesizer resolution. The theoretical maximum frequency determined by the Nyquist sampling theorem is equal to the input clock

frequency divided by a factor of two. In practice, a slightly larger factor is used to relax the requirements of the antialiasing filter. The output signal is as stable as the input reference frequency (or even better because of the frequency division effect). This nets an excellent phase noise performance. The signal, however, exhibits spurious sidebands caused by the quantization error due to the limited memory word length. These spurious signals tend to form clusters at fractional values of the output frequency. They are very close to the output signal and cannot be filtered out. The memory word length is limited by the output DAC resolution, which turns out to be the stumbling block in designing a high frequency and high spectral purity DDFS. This DAC should have a conversion speed equal to the input reference clock frequency, as well as a very high resolution. For example, a 14 bit DAC is needed, to achieve a spurious power level less than -80 dBc, a real challenge for clock rates in the range of few hundred MHz. This puts an upper limit on the frequencies where this technique is applied. Another important limitation is the high power consumption of the digital blocks at such high clock speeds.

Theoretically, the DDFS has instantaneous output frequency switching. Thus, it is very attractive for spread spectrum techniques, which require fast frequency hopping to spread the signal over the whole spectrum. We should note that the resolution of the DDFS is also, theoretically, unlimited as the number of memory words can be arbitrarily increased to achieve the desired resolution. In reality, this is not a large number of words, because the number is limited by the maximum number of unique values that can be represented by the available bits per word. Consequently, only the accumulator size need to be increased to achieve higher

resolution, and the memory is addressed only by the most significant bits. Another very attractive property of the DDFS is its ability to generate quadrature outputs with a high accuracy.

The maximum frequency limitation of the DDFS makes it unsuitable to directly synthesize RF frequencies. However, it can be upconverted using another fixed frequency signal source to generate the RF synthesized output.

2.2.2 Phase Locked Loop (PLL) Synthesizer

The phase locked loop is a basic block in almost every practical frequency synthesizer. Fig. 2.8 represents a basic PLL synthesizer which we examine. Section 2.3 highlights its use for practical RF synthesis. The PLL is a feedback control system, in which the phase detector is used to generate an error signal equivalent to the phase difference between the VCO output signal and an external input reference. This error signal is used to correct the VCO frequency until both phases are locked together with the result of transferring the properties of (usually) an extremely stable reference source to the VCO. The optional divide-by-N frequency divider has the effect of locking the VCO to the Nth multiple of the reference frequency. This division ratio is usually controlled by a digital input to synthesize the desired output frequency. Ideally, if the phase of the VCO output is ϕ_o and that of the reference ϕ_i, then the phase detector output (assuming linear characteristics) is equal to $k_d(\phi_i - \frac{\phi_o}{N})$ where k_d is the phase detector gain. This phase detector output is then filtered by the loop filter $H(s)$ and used to control the VCO frequency. If the VCO gain is K_v, its transfer function is K_v/s. The closed loop phase transfer

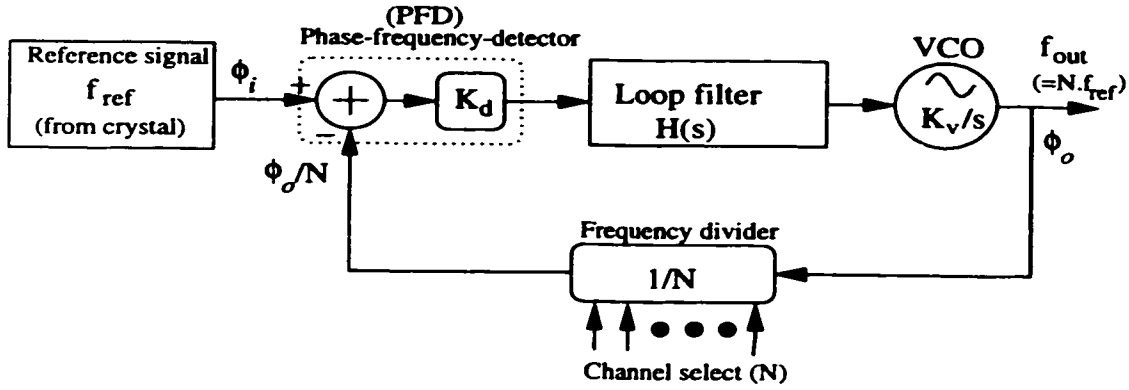


Figure 2.8: Block diagram of a basic PLL frequency synthesizer

function could then be written as

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{K_d K_v H(s)/s}{1 + K_d K_v H(s)/sN}. \tag{2.1}$$

In steady state when s tends to zero, the output phase (or frequency) is the Nth multiple of the the input phase (or frequency). The transient response of the loop, its switching times, as well as the steady state error are determined by the design parameters K_d, K_v, and $H(s)$. A comprehensive treatment of the different loop design parameters is available in several textbooks [12, 13, 14], and we will highlight a few points of the PLL design.

- It is desirable to have a higher order loop filter to allow more degrees of freedom in the design process. This, however, may degrade the loop stability due to the reduced phase margin. In fact, the loop filter should not add more than a 45° phase in order to maintain a 45° phase margin. This is due to the 90° added by the VCO in addition to another 180° added by the subtraction effect of the PFD. This leaves only a 90° margin before $+ve$ feedback is

achieved. This means that the loop filter should be predominantly first order, which requires the other poles to be far away enough from the first one.

- A large closed loop bandwidth provides fast frequency switching and settling times. This large bandwidth, however, reduces the averaging effect needed at the phase detector output to remove its nonidealities. Usually, this bandwidth needs to be an order of magnitude smaller than the input reference frequency, in order to have a clean signal at the VCO control input.

- To reduce the steady state error at the VCO input to zero, and to achieve a theoretically infinite frequency lock range, the loop filter should have an infinite DC gain (or equivalently a pure $1/s$ integration term). This could be obtained by using an active loop filter, but the noise added by the OpAmp involved directly modulates the VCO and degrades it spectral purity. A good way to achieve the $1/s$ integrating effect and avoid the OpAmp noise is the use of a charge pump in conjunction with a tri-state phase detector [15], as shown in Fig. 2.9. The $R_1 - C_1$ branch adds a pole and a zero, for stability and design flexibility.

- This last point is related to the loop effect on the different noise sources in the system, and will be discussed in a separate section because of its importance in our application.

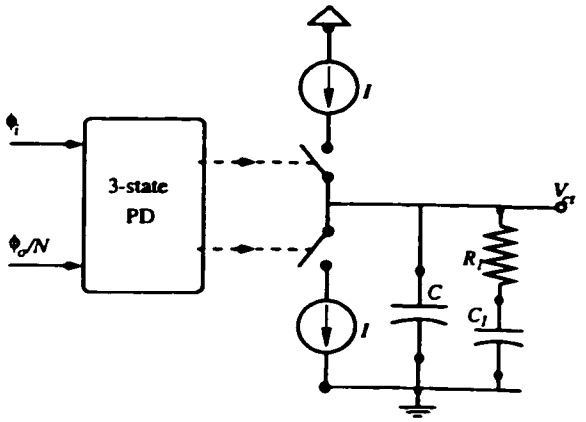


Figure 2.9: Charge pump loop filter combination

2.2.3 PLL Noise & Spurious Sidebands

As shown in Fig. 2.10, several sources contribute to a PLL based frequency synthesizer output phase noise. Because the noise levels are small, a linear model for the PLL is used, where summing nodes are used to add the noise from the different sources. These noise sources include the reference oscillator, VCO, divider, PFD, and the loop filter. Each of these noise sources is shaped to the PLL output by a different transfer function (T.F.). Working around the loop we write the following

T.F.:

$$TF_{ref}(s) = \frac{\phi_o}{\phi_i} = \frac{K_d K_v H(s)/s}{1 + K_d K_v H(s)/Ns} \tag{2.2}$$

$$TF_{pfd}(s) = \frac{\phi_o}{v_{pfd}} = \frac{K_v H(s)/s}{1 + K_d K_v H(s)/Ns} \tag{2.3}$$

$$TF_f(s) = \frac{\phi_o}{v_f} = \frac{K_v/s}{1 + K_d K_v H(s)/Ns} \tag{2.4}$$

$$TF_{div}(s) = \frac{\phi_o}{\phi_i} = \frac{K_d K_v H(s)/s}{1 + K_d K_v H(s)/Ns} \tag{2.5}$$

$$TF_{vco}(s) = \frac{\phi_o}{\phi_i} = \frac{1}{1 + K_d K_v H(s)/Ns} \tag{2.6}$$

Careful inspection of the above T.F's indicates that all the noise sources, other than the VCO noise, are shaped by a low pass T.F. due to the VCO integrating effect. The VCO noise, on the other hand, is shaped by a high pass T.F. This means that there is, "theoretically speaking", an optimum loop bandwidth (BW) to minimize the overall output noise. This BW is approximately at the intersection of the effective reference noise at the VCO output and the VCO noise curves, as shown in Fig. 2.11, curve (a). The effective reference noise includes noise from all the sources, other than the VCO, being referred to the VCO output frequency. For example, the reference or the divider noise when referred to the VCO frequency goes up by $20log(N)$.

In practice, the choice of the PLL BW is limited by the spurious sidebands. These sidebands are a direct consequence of any periodic signal on the PFD output. Usually, the output of a digital PFD has a frequency component at the comparison frequency, which can be avoided by the use of a charge pump and a tri-state detector

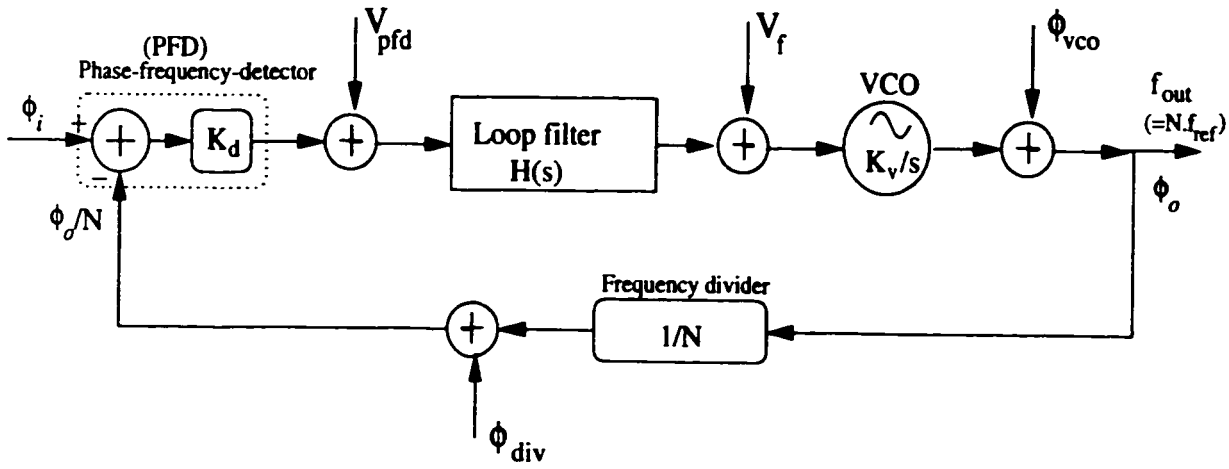


Figure 2.10: Phase noise contribution of different PLL components

as described in Fig. 2.9. Unfortunately, the mismatch between the two current sources constituting the charge pump prevents the complete removal of this tone. To achieve enough suppression for the resulting side bands the PLL BW is limited to approximately one tenth of the reference frequency. Consequently, the overall PLL output noise is dominated by the VCO noise, and is much higher as shown in Fig. 2.11, curve (b). To alleviate this problem, a high reference frequency is desirable. In the conventional PLL FS discussed so far the reference frequency is equal to the channel spacing, which is usually very small. In the next section we will discuss some design variations to help increase the reference frequency while maintaining the same channel spacing.

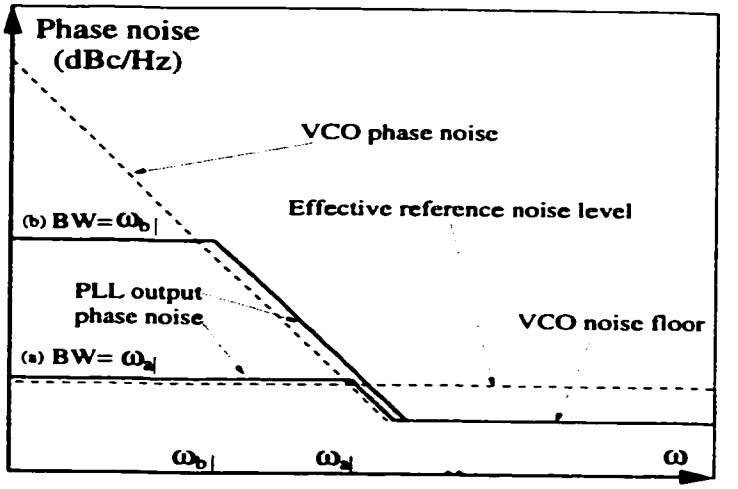


Figure 2.11: Effect of loop bandwidth (BW) on PLL phase noise output

2.3 High Resolution RF Synthesizers

As discussed in the last section, conventional PLL synthesizer architecture mandates that the reference frequency be equal to the required channel spacing. Therefore, for systems such as AMPS where the channel BW is 30 KHz, loop BW of approximately 3 KHz should be used to suppress the reference spurs. This very narrow loop BW does not inhibit the VCO phase noise, and the noise of the VCO dominates the system phase noise. The other drawback of this limited BW is the extremely slow response of the loop which makes it unsuitable for many applications. For an output frequency around 900MHz, a division ratio N=30,000 is required. This large division ratio has two effects: the first is the open loop gain reduction which again means a narrow BW and slow switching times. The other effect is a $20log(N)$ increase in the reference phase noise contribution to the synthesized output. In this section we describe some of the architectural variations [16, 17] that

has been used to reduce the division ratio, and/or increase the reference frequency for the same synthesizer requirements.

2.3.1 Offset Frequency

An offset frequency PLL synthesizer is achieved by introducing a frequency shift (or offset) to the output signal before going through the frequency divider by using a mixing stage (see Fig. 2.12). Two alternative architectures can be used in this context. The first is to use a fixed RF offset frequency to shift the PLL output close to the baseband. This results in a small value for N which is used for channel selection. This small N improves the open loop gain, and reduces the reference noise, but still have the low reference frequency problem.

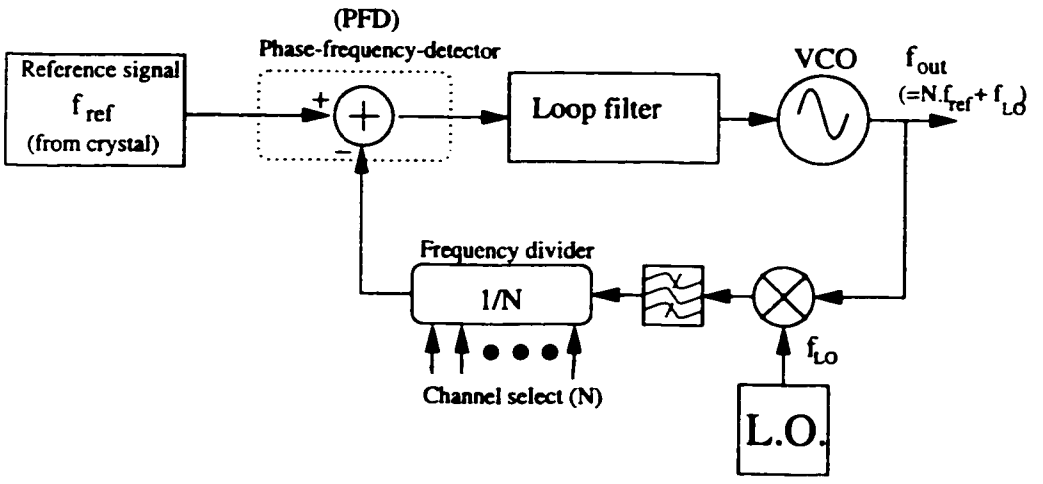


Figure 2.12: Using offset frequency to reduce N for the same channel spacing

The second alternative is to use a fixed value for N and a higher reference frequency. The tuning in this case is achieved through the use of a tunable low frequency source as an offset frequency. This tunable source is ideally a DDFS. In

this case, we could arbitrarily increase the reference frequency as well as the loop bandwidth, in order to inhibit the VCO output noise. The main difficulty with this architecture is the need for a single sideband mixer, because it is very difficult to filter the other mixer sideband output when the RF signal is mixed with the low frequency offset signal. Although this latter architecture might be expensive in its circuit requirements and power consumption, it is still a good candidate for an integrated synthesizer because it relaxes the requirements on the VCO design.

2.3.2 Multi-Loop Synthesizers

The dual loop architecture is also another solution extensively used in precise signal generators. It has, however, many components and could be an expensive solution for wireless handsets. As shown in Fig. 2.13, the idea is to use two closely spaced references which are generated from the same crystal oscillator output. The channel spacing is now limited by the difference between the two reference frequencies, not their absolute values. To switch the output one channel up, for example, N_2 is increased by one while N_1 is reduced by one at the same time so the output frequency is increased by $(\frac{f_{xo}}{M_2} - \frac{f_{xo}}{M_1})$. Multi-loop solutions has also been used to achieve wider tuning ranges and finer selectivity, but their excessive hardware requirement limits their use in wireless applications.

2.3.3 Fractional-N Division & Spur Reduction

Fractional-N PLL architecture has emerged as a less expensive alternative to other FS architectures that use mixers for frequency addition or subtraction. The simplest

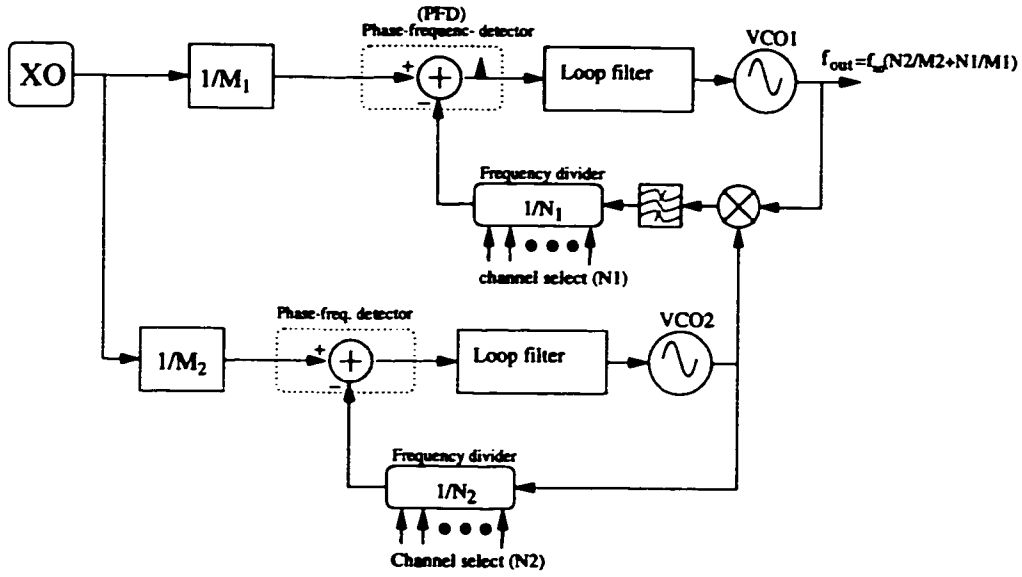


Figure 2.13: Dual loop frequency synthesizer

form of a fractional-N synthesizer is shown in Fig. 2.14. A dual modulus frequency prescalar/divider is used to switch the division ratio between N and N+1 over the time. The average division ratio could be any fractional value between N and N+1, depending on the ratio of the time durations. As shown in the figure, the switching between N and N+1 can be controlled by an accumulator overflow signal, where the accumulator input represents the required fraction. The accumulator is clocked at the reference frequency. The main problem with this architecture is that the divider output frequency is periodically changing, according to the different division ratios. This leads to a phase difference accumulation in one direction during N division, and in the other direction during the N+1 division. The resulting PFD output is modulated by this low frequency signal which cannot be filtered by the loop filter. The result is significant sideband spurs very close to the carrier frequency. Being otherwise an attractive architecture, the fractional-N has gained increasing

attention in the investigation of different ways to reduce this high spur level. Here, we summarize some of the current ideas and their advantages, as well as drawbacks. These techniques will be considered in more detail in chapters 6 & 7.

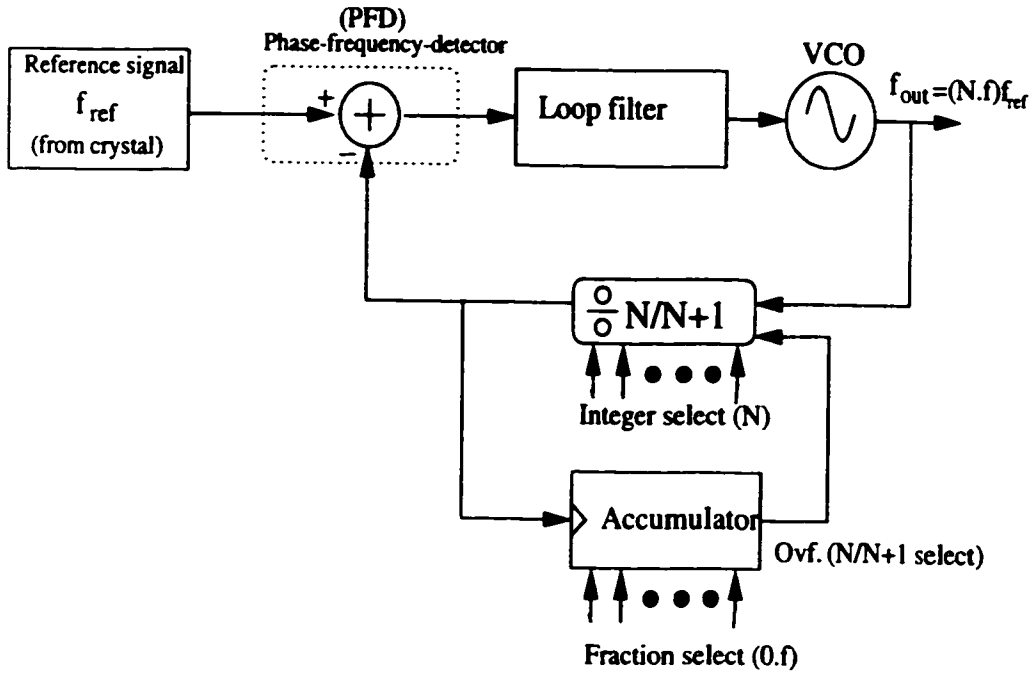


Figure 2.14: Basic fractional-N PLL frequency synthesizer

- *Phase estimation using DAC*: In this configuration, a DAC is used to convert the accumulator value to an analog signal corresponding to the phase of the divider output signal. This DAC output is then inverted and added to the the charge pump output to cancel out its AC component, and leave only the DC value. The main problem with this solution is the unavoidable mismatch between the DAC and the charge pump current outputs.

- *Randomized division*: Randomizing the divider control signal while keeping the statistical average at the required division ration can move the phase modulation to higher frequencies, but it may add extra frequency jitter.

- *Sigma-delta modulation*: Sigma-delta modulators have been very successful in shaping the quantization noise to higher frequencies in oversampled ADC's. A sigma-delta modulator could be used to convert the required fraction value into a single oversampled bit stream. The resulting phase modulation is then shaped to high frequencies. In order to have better shaping of the modulating signal, higher order sigma-delta are needed, which means faster rise of the quantization noise at higher frequencies. Consequently, the loop BW is limited to filter this noise.

- *Phase interpolation*: This architecture uses multiple phase shifters of the RF signal before feeding it to the frequency divider. The output of the dividers has different effective division ratios between N and N+1. Any division ratio can be interpolated by switching among the different phases.

Chapter 3

Voltage Controlled Oscillator (VCO)

The VCO is the heart of any PLL based frequency synthesizer. In most cases, the phase noise performance of the VCO determines the overall output signal purity of the synthesizer. The different VCO architectures fall into two main categories: narrow band oscillators and wide band ones. In this chapter, we briefly review these two categories and their phase noise performances. However, more concentration is given to the narrow band class because of its superior phase noise performance. This makes them the appropriate choice for most of wireless systems synthesizers.

3.1 Narrow Band Harmonic Oscillators

The term *narrow band* means the use of a frequency selective element (or a resonator) to set up the oscillation frequency. This resonator can be an LC tank,

surface acoustic wave filter (SAW), transmission line (TL), or crystal. The use of any of these depends on the operating frequency range and the required spectral purity.

Crystal oscillators offer the best phase noise, as a result of their extremely high effective quality factor Q (~500,000). They can be used for frequencies up to 100MHz; at higher frequencies they become mechanically unstable and other techniques have to be used. As a result of their superior phase noise performance, crystal oscillators are almost invariantly used to generate the reference frequency for different kinds of frequency synthesizers.

For VCO's operating at the RF frequency, all other kinds of resonators are usable, but in the (1~3 GHz) range, only the LC tank can be used in an integrated environment. The quality factor Q of an integrated inductor is, however, very low (<10) and challenges the design of a fully integrated VCO with low phase noise. The effect of this low Q on the noise performance is discussed in this chapter.

The other challenge in a fully monolithic environment is the large tolerance in the varactor value which implies a wide tuning range to cover the process tolerances, in addition to the required operating range. This wide tuning range sets stringent requirements on the maximum acceptable parasitic capacitance from other circuit components, and the maximum usable inductance values. For low voltage applications (the case for most wireless systems), this wide tuning range also requires a very high VCO tuning sensitivity, but this makes very vulnerable to noise pick up on the control lines. This effect will be detailed in chapter 4.

The main principle in a resonator based harmonic oscillator stems from the

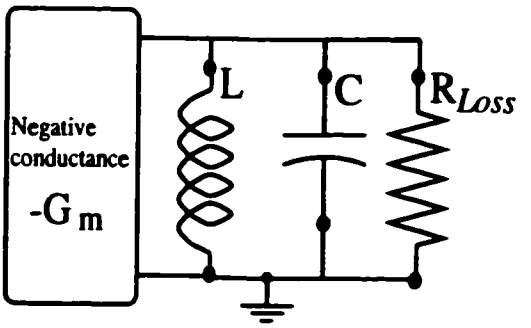


Figure 3.1: Basic model for negative resistance oscillator

nature of the resonator. An ideal resonator would be lossless, and if excited by an external signal it would oscillate at its natural frequency. Of course, such a resonator does not exist, and an active element (amplifier or a negative impedance) is used to compensate for the resonator loss, and sustain the oscillation. Two main approaches are used to analyze such oscillators; namely, positive feedback and negative resistance techniques. Both techniques are equivalent, but depending on the circuit configuration, one might be easier than the other.

As shown in Fig. 3.1 the active element in a negative resistance oscillator, generates an effective negative conductance that is greater than the resonator loss represented by its parallel resistance. The oscillation builds up as long as the negative conductance effect is greater than the loss. Eventually, the active circuit nonlinearity decreases the negative conductance effect with an increased oscillation amplitude. The final oscillation amplitude is the one at which the negative conductance is equivalent to the loss in the resonator.

In a positive feedback analysis, the oscillator loop is cut open at one point and treated as a feedback system. Two conditions for oscillation have to be satisfied.

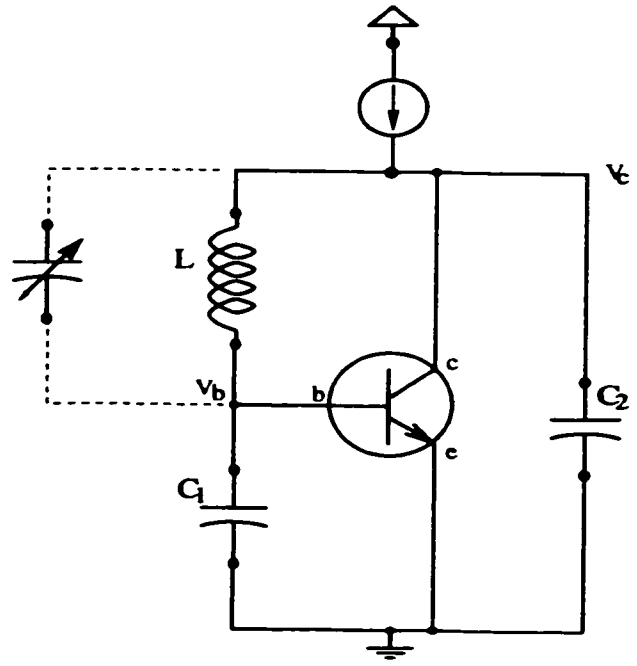


Figure 3.2: Simplified AC equivalent circuit of Pierce oscillator

The first is the phase condition which defines the frequency of oscillation. At this frequency, the total phase shift around the loop should be 360°. The second condition for oscillation (or the amplitude condition) is that the small signal open loop gain at the oscillation frequency is greater than unity. When the oscillation begins to build up, the amplitude grows and the system nonlinearity kicks in to reduce the effective gain. The steady state oscillation amplitude is the one that brings the gain around the loop down to unity.

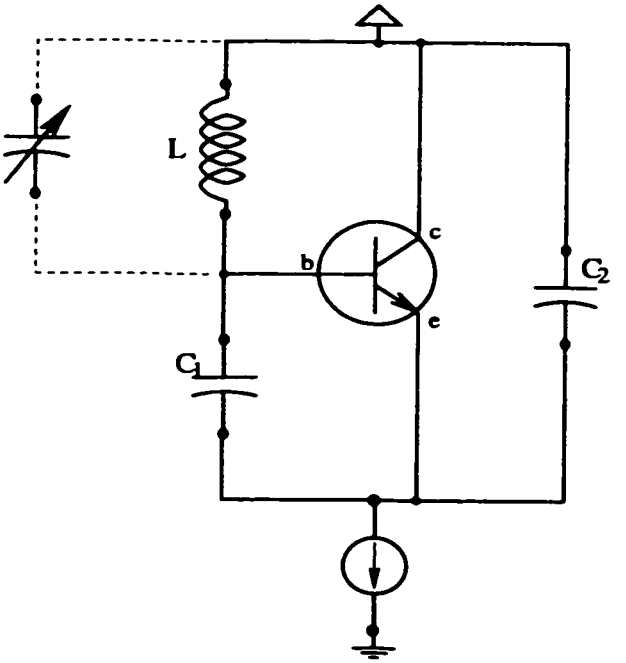


Figure 3.3: Simplified AC equivalent circuit of Colpits oscillator

3.1.1 Overview of Common LC Oscillator Architectures

Pierce and Colpits Oscillators

Both the Pierce and the Colpits oscillators are members of a large family of oscillators which have essentially the same resonator feedback model. They only differ in the method of feeding the DC power and biasing the transistor. In the Pierce oscillator (see Fig. 3.2) the transistor is biased in a common emitter configuration. The resonator feedback network has to provide 180° phase shift transimpedance to cancel out the transistor transconductance (G_M phase shift) and satisfy the phase condition for oscillation. This feedback network transfer function can be expressed

as

$$\frac{V_b}{I_c} = \frac{X_{C1}.X_{C2}}{X_{C1} + X_{C2} + X_L} \tag{3.1}$$

Normally, the tank losses are dominated by that of the inductor, and the capacitor losses could be neglected to simplify the analysis. Using this assumption the above transfer function reduces to

$$\frac{V_b}{I_c} = \frac{\frac{1}{sC_1}.\frac{1}{sC_2}}{\frac{1}{sC_1} + \frac{1}{sC_2} + (r_L + sL)} \tag{3.2}$$

The phase condition for oscillation is satisfied when the imaginary part of the denominator is zero and is written as

$$\omega^2 = \frac{1}{L}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) \tag{3.3}$$

The gain condition is expressed as

$$G_M > r_L\omega^2 C_1 C_2 \tag{3.4}$$

Similar expressions could be derived for the Colpits oscillator of Fig. 3.3. The Pierce configuration is preferred for crystal oscillators because it provides higher loaded Q [18]. For VCO design, the frequency is controlled by controlling a variable capacitance in parallel with the inductor to change the effective inductance value, as shown by the dotted lines in both Fig. 3.2 and Fig. 3.3. The Colpits configuration is more practical in this case because it allows one of the varactor terminals to be

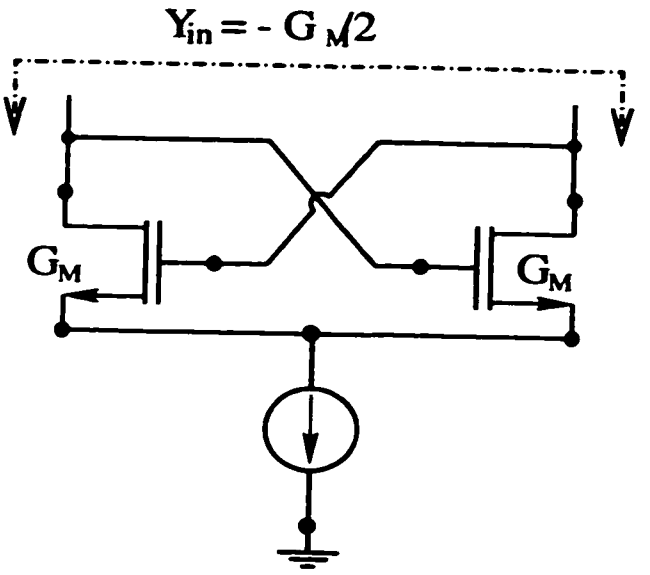


Figure 3.4: Implementation of negative impedance using differential cross coupled NMOS pair

connected to the ground.

Differential Cross Coupled Pair Oscillator

Colpits and Pierce oscillators are very popular for discrete designs. However, this is not the case in integrated VCO's, because these types of oscillators don't lend themselves to differential implementations. Differential outputs are important for integrated VCO's to reduce their sensitivity to interference from other components on the same chip. The simplest way to implement a differential VCO is the use a cross coupled differential pair (see Fig. 3.4) as a negative impedance element. The VCO is completed by connecting a tank circuit across the negative impedance similar to Fig. 3.1. This architecture is also attractive because two varactors could be connected back-to-back to tune the frequency with no need for decoupling

capacitors. This type of VCO's will be detailed in the next chapter.

3.1.2 Phase Noise Analysis

VCO phase noise output is caused by both internal and external sources. The internal noise is the main source, and results from the large amplification due to the positive feedback of the noise generated by the oscillator active elements, and the thermal noise of the resistive components representing the resonator loss. Another cause for the VCO internal noise is the upconversion of the baseband noise to the oscillation band. The external VCO noise (also called varactor modulation noise) is the phase noise generated as a result of modulating the VCO output by noise picked up on the frequency control line(s) from sources external to the circuit itself. The main sources of this noise are: substrate coupling of unwanted signals from other circuits sharing the same substrate with the VCO, and power supply fluctuations due to the switching activity of digital and/or analog circuits sharing the same supply. Another source of varactor modulation noise is the thermal noise of the resistive varactor loss itself. A full discussion of the different noise sources may be found in several textbooks [2, 19]. In this section of the thesis, the main theories governing the VCO phase noise are briefly reviewed. The main objective is to understand the different parameters affecting the VCO phase noise performance, rather than detailing the analysis.

Linear Time Invariant (LTI) Model and Leeson's Formula

LTI analysis is based on the linear small signal transfer function approximation of the oscillator loop. This approximation is valid if some sort of AGC is used such that in the steady state the oscillation amplitude remains small, and is not limited by the system nonlinearity. However, this is not the case for most practical oscillators, which are self limiting. In this case, the phase noise is predicted using the LTI model; then the several nonlinear effects are added to the final noise expression, empirically. The following popular Leeson's formula [20] is based on that model:

$$S_n(\Delta\omega) = \frac{1}{2}\frac{FKT}{C}\left[\frac{1}{4Q^2}\left(\frac{\omega_o}{\Delta\omega}\right)^2 + 1\right]\left[\frac{\omega_c}{\Delta\omega} + 1\right] \tag{3.5}$$

where F is an empirical factor that accounts for the amplifier noise figure and noise folding due to nonlinearity, C is the oscillator output power, Q is the resonator loaded quality factor, ω_o is the oscillation frequency, $\Delta\omega$ is the offset frequency at which the noise is to be calculated, and ω_c is the $1/f$ noise corner frequency of the amplifier.

The factor $\frac{FKT}{C}$ represents the thermal noise to signal power ratio of the VCO amplifier. The quantity in the first brace represent the noise shaping due to the selective feedback circuitry, where the 1.0 accounts for the thermal noise floor away from the center frequency. The second brace is empirically added to the expression, and accounts for the amplifier (and the bias circuit) $1/f$ flicker noise. Some recent studies [21, 22] show that the corner frequency (ω_c) of this term does not have to be the same as the $1/f$ corner frequency. Also, it is important to note that the "$\frac{1}{2}$" factor at the beginning of Leeson's noise expression is based on the assumption

that only 50% of the shaped noise power is converted to phase modulation (PM), whereas the rest of noise power represents amplitude modulation (AM) [2]. The contribution of different thermal noise sources to this relation in a typical oscillator has been described in the literature [23].

Varactor Modulation Noise

Varactor modulation noise can be described using the small phase deviation index approximation of the phase modulation theory, which relates the single sideband noise modulation power normalized to 1 Hz to the carrier power as [24]

$$\begin{aligned} S_{n\_varactor}(\Delta\omega) &= \frac{1}{2}\Delta\phi_{rms}^2 \\ \Delta\phi_{rms} &= \frac{\Delta\omega_{rms}}{\Delta\omega} \\ \Delta\omega_{rms} &= 2\pi V_{n\_var\_in\_rms} K_v co \end{aligned}$$

or

$$S_{n\_varactor}(\Delta\omega) = \frac{1}{2}\left(\frac{2\pi V_{n\_var\_in\_rms} K_{vco}}{\Delta\omega}\right)^2. \tag{3.6}$$

The factor "$\frac{1}{2}$" is the asymptotic value of the first order Bessel function, representing the frequency components of a phase modulated (PM) signal for small phase deviations. K_{vco} is the VCO gain defined as the output frequency change per one volt change in its control input. It should be noted that the above equation is valid only for small values of phase deviation ($\Delta\phi_{pk} \ll 1$ rad.), which is the case for the type of applications we are aiming at. The control circuit should be designed very

carefully to minimize the effect of this varactor modulation noise. In a good design, this noise should not degrade the overall VCO noise by more than 1 dB. Differential control circuits are also very desirable to minimize the effect of any noise pick up.

Hajimiri and Lee Model

The main limitation of the LTI noise analysis model is its inability to predict the upconversion of the baseband noise to the VCO oscillation band. It also fails to predict the effect of noise folding, and the cyclostationary nature of the active device noise. In 1998, A. Hajimiri and T. Lee [21] introduced a more general phase noise model that is capable of predicting such effects. The model is based on what is called the "Impulse Sensitivity Function" (ISF). If an impulse charge is introduced into the capacitance of the output node of an oscillator in its steady state, it will cause both amplitude and phase errors. Usually, the amplitude error dies out after a few cycles because of the amplitude limiting [25]. The phase error, however, is not attenuated, and is a function of the time τ when the charge is injected. The unit impulse response for the excess phase can be expressed as

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_o\tau)}{q_{max}}u(t-\tau), \tag{3.7}$$

where q_{max} is the maximum charge displacement across the capacitor, which represents the oscillation amplitude, and $u(t)$ is the unit step. $\Gamma(\omega_o\tau)$ is called the impulse sensitivity function (ISF). It is a periodic, dimensionless function that is independent of both frequency and amplitude. The ISF gives the dependence of the phase disturbance on the time at which the disturbance charge is injected. It

is a function of the oscillator waveform, which reflects the different system nonlinearities. The noise output, due to a noise source connected to the node where the charge pulse was injected, is the convolution in the time domain of the noise source and the impulse response $h_\phi(t,\tau)$, and is given by [21]

$$S_n(\Delta\omega) = \frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{i_n^2/\Delta f}{4.\Delta\omega^2} \tag{3.8}$$

where Γ_{rms} is the root mean square value of the ISF and $i_n^2/\Delta f$ is the the input noise source power spectral density. The ISF has to be derived for each node that has a noise source connected to it. Then, superposition is used to estimate the total output phase noise of the oscillator.

The cyclostationary nature of the noise can also be taken into account in the above expression. If a cyclostationary noise source $i_n(t)$ is represented as

$$i_n(t) = i_{no}(t).\alpha(\omega_o t) \tag{3.9}$$

where $i_{no}(t)$ represents a white stationary noise source. The effective ISF is then the multiplication of $\Gamma(\omega_o\tau)$ and $\alpha(\omega_o\tau)$. The root mean square of this effective ISF should be used in $S_n(\Delta\omega)$ (Eq. 3.8). According to this result, the phase noise can be significantly reduced by minimizing the overlap between $\Gamma(\omega_o\tau)$ and $\alpha(\omega_o\tau)$. Another important result that this work demonstrated is that the upconversion of the baseband noise to the oscillator frequency band is mainly affected by the DC, and the even harmonics of the ISF. For example, reducing those components by making the oscillation waveform very symmetric could drastically reduce, or even

eliminate the upconversion of the $1/f$ noise.

3.1.3 Monolithic Resonators

The move to the sub-micron and deep sub-micron silicon technologies has allowed the use of silicon for wireless front ends at frequencies in the gigahertz range. Once in this frequency range, the inductor values needed for different designs become smaller. This means that on chip spiral inductors which are commonly used in GaAs MMIC's can have reasonable sizes for integration on silicon chips. The conventional silicon processes, however, have two main disadvantages if compared to the GaAs ones. The large substrate losses due to the semi-conducting nature of the silicon substrate as opposed to the semi-insulating GaAs substrate, and the finite conductivity metalization used in conventional silicon technologies, as compared to high conductivity metals, like gold, that are commonly used in GaAs processes. These two loss mechanisms, in addition to the skin effect, limit the maximum obtainable Q-factor.

Depending on the frequency range, the inductor loss is usually dominated by one (or more) of these three effects. At low frequencies up to ($\sim$ 1GHz), the main loss is caused by the series inductor resistance due to the limited metal conductivity. Thus, the Q-factor ($\omega L/R$) is proportional to the frequency. Increasing the metal thickness or using several metal layers in this frequency range may improve Q. At higher frequencies (1$\sim$3 GHz), the skin effect becomes significant. As a result, the series resistance increases with the frequency, and Q-factor no longer increases linearly with the frequency. At these frequencies, the substrate loss comes into play.

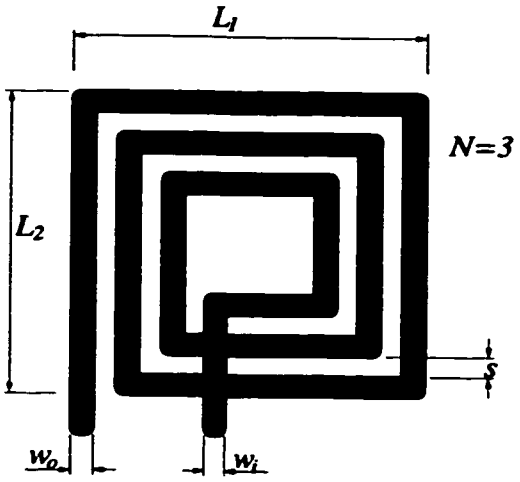


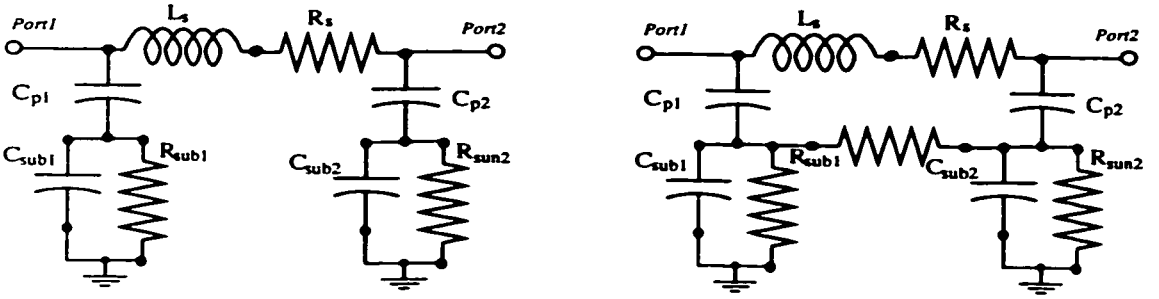
Figure 3.5: Spiral inductor layout and design parameter

Q eventually reaches a maximum value and decreases rapidly with frequency.

It is important to note that the above frequency values are only typical, and are strongly affected by the spiral design itself. For example, the substrate loss dominates at much lower frequencies for large inductors. Some work has been reported to reduce this effect for large inductors by using suspended inductors with an air gap to separate them from the substrate [26]. This technique greatly reduces the substrate loss, but is expensive and needs sophisticated processing, which limits its use to academic research only. Another way to reduce the substrate loss at the expense of lowering the self resonance frequency is to use patterned ground shields [27].

The optimization of the inductor layout for maximum Q is a key point in an integrated low phase noise VCO design. For the spiral inductor shown in Fig. 3.5, several design parameters need to be optimized including the number of turns (N), spiral side length (L), strip width (w), and the spacing between strips (s). An

accurate electro-magnetic simulation of the inductor using techniques like finite element methods, can lead to a well optimized design [28]. The electro-magnetic methods are, however, expensive and time consuming. Hence, they are not suitable for circuit optimization. The need for simple circuit models for spiral inductors has motivated lots of researchers to derive empirical models relating the different physical dimensions of the inductor to its circuit model [29, 30, 31]. Fig. 3.1.3(a) represents the simplest model for the spiral inductor while Fig. 3.1.3(b) is a modified model [32], which accounts for the effective inductance reduction measured at high frequencies. Distributed inductor models have also been used [33], which use the same model mentioned above for each segment of the inductor, and then combine the segments together.



(a) Commonly used model

(b) Resistance added to account for L_{eff} reduction [32]

Figure 3.6: Circuit models for spiral inductors

Understanding the tradeoff in the spiral inductor design help getting close to an optimum design using limited number of iterations. For example, an increased strip width w not only reduces the DC series resistance, but also reduces the inductance

so that a larger area is needed to implement the same inductance value. Also, the internal turns contribute little to the inductance, but add much to the series resistance. It appears that increasing the inductor area increases the Q-factor, but this is not valid for large areas because the capacitance to substrate increases resulting in two unwanted effects. First, it reduces the self resonance frequency and limits the tuning range of the VCO. Secondly, it reduces the Q-factor itself, as a result of increasing the substrate losses. Then, there is an optimal area for maximum Q (at a specific frequency) and a minimum self resonance frequency for the spiral inductor. The strip spacing (s) should be the minimum allowed by the process. Other considerations that may improve the Q include, some tapering in the stripe width from the outer stripe (w_o) to the inner one (w_i), where ($w_o > w_i$). Another helpful way is to use circular or close to circular layout to minimize the area and hence the capacitance to substrate. Using *ASITIC* (an inductor optimization tool available from UCB) good compromise between the different spiral parameters can be obtained. This tool [34] uses both the analytical models and electro-magnetic methods to perform the inductor optimization depending on the required accuracy.

Using an active negative resistance to enhance the inductor Q has also been studied and proven to be very noisy [23]. Another way of obtaining high Q inductors is to use the bond wire inductance for the VCO design [35] for a Q factor as high as $\sim$20, but the large fabrication tolerance associated with such inductors complicates the VCO design.

3.2 Wide Band Oscillators

Unlike narrow band oscillators, wide band oscillators don't use frequency selective filters. Therefore, they are more compatible with an integrated environment because no bulky inductors are needed. They mainly depend on R-C delay(s) to determine the oscillation frequency. In this case, the phase noise is higher as a result of lacking the noise filtering effect of the tank circuit. So, we might expect the phase noise to be Q^2 times higher than that of an LC based oscillator. This kind of oscillators can be classified into two main categories: multi-vibrators, and ring oscillators. Multivibrators (also called relaxation oscillators) have a higher phase noise because of the hard switching action [36], and are usually unsuitable for wireless applications. The ring oscillator is briefly discussed next.

3.2.1 Ring Oscillator

Ring oscillator are commonly used for clock generation PLL's because of their simplicity and ability to oscillate at very high frequencies, as well as their wide range tunability. A ring oscillator is composed of chain of inverters that act as delay stages. The minimum number of delay stages for a stable oscillation is three. The total delay of all the stages is equivalent to a 180° phase shift. The other 180° shift is added by the inverting effect of the whole chain. For single ended inverters, only odd number of stages can be used to achieve this inversion effect. If differential stages are utilized, an even number of stages can be also used provided that they are connected with the correct polarity. Fig. 3.7 is an example of a 4-stage oscillator used to generate quadrature outputs.

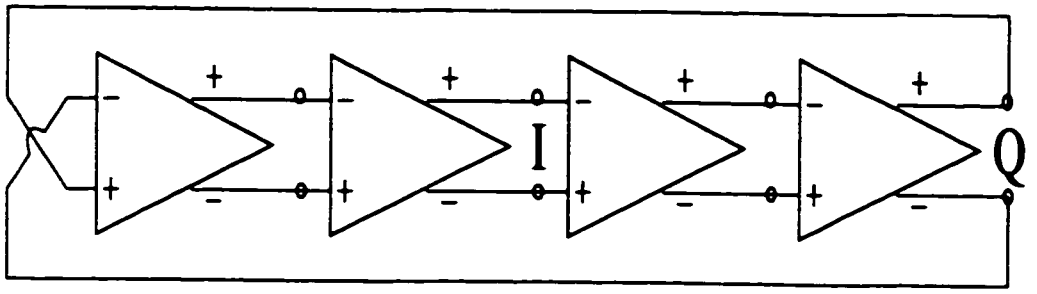


Figure 3.7: Four stage differential ring oscillator

Different approaches have been used in literature to analyze the phase noise. One approach is based on a time domain analysis [37, 38, 39], where the effect of the thermal noise on the timing jitter of each delay cell is considered. The second approach is a frequency domain one [40, 41], which assumes a linear system, and uses a noise shaping function similar to the technique used with harmonic oscillators. Both time domain and frequency domain analysis lead to phase noise relations similar to Lesson's formula (Eq. 3.5) with an equivalent quality factor Q=1, and a differently defined equivalent noise figure F. The ISF method has also been successfully used to estimate the noise of ring oscillators [42].

3.3 State of the Art Monolithic VCOs

Table 3.1 lists the phase noise and power consumption of some recently published integrated VCOs. The table data indicates that LC oscillators have a superior phase noise performance due to the filtering effect of the LC tank. However, none of these LC oscillators has a differential control, which renders them susceptible to substrate noise. They also use a very large chip area as compared to ring oscillators. Only

Type	Technology	Frequency GHz	Phase Noise dBc/Hz	Tuning Range	Power	Remarks	Source/Yr. [Ref.]
LC	RFIC ISOSAT Bipolar	1.10 1.55 2.20	-105@100KHz -102@100KHz -99@100KHz	13.6% 12.9% 11.4%	15mA@2.7V 16mA@2.7V 16mA@2.7V		HP/97[43]
LC-Colpit	0.8μBiCMOS	1.5	-105@100KHz	10%	40mW@3.6V		Carl.U/97[44]
Ring	0.8μCMOS	1.69			78mW@5V		Korea/97[45]
LC	0.6μCMOS	1.8	-100@500KHz	6.7%	2.3mA@3.3V	Linear cont.	UCLA/97[46]
LC		1	-95@100KHz	0	16mW@1.5V	Etched sub.	ESSCC/94 [47]
LC	0.5μBiCMOS	2.4	-92@100KHz	9%			IBM/96[48]
LC	0.7μCMOS	1.8	-115@200KHz	5%	8mA@3V	Bond Q=10	KU/94[49]
LC	0.5μBiCMOS	4.1	-106@1MHz	8%		M.Metal Q=7	IBM 96[50]
LC	1μCMOS	0.82	-85@100KHz	9%		Etched, Quad.	UCLA/96[8]
LC	0.7μCMOS	1.8	-116@600KHz	14%	4mA@1.5V		KU/96[28]
LC	25G Bipolar	0.9	-101@100KHz	20%	4mA@3V		Rockwell/96[51]
Ring Osc PLL	0.6μCMOS	1.8	-118@3.4MHz		60mW	Fully diff.	UCB/96
Ring Osc	CMOS	1	-85@100KHz			Fully diff.	UCB/94[38]
LC	40G Bipolar	1.9	-123@600KHz	6.3%	16mA@2.7V	Quad.	NTT/98[52]
LC	0.35μCMOS	2.6/5.2	-110@5MHz	6.1%	26mW@2.5V	Quad.	UCLA/99[53]
LC	0.35μCMOS	6.5	-98.4@1MHz	16.8%	18mW@1.5V	Quad.	Lucent/99[54]
LC	.8μCMOS	1.1	126@600KHz	7.6%	4.7mA@2.7V	bond Q=17	UF/00[55]

Table 3.1: Fully integrated VCOs state-of-the-art

a few of the LC VCOs have quadrature outputs. For these designs, the area and power are doubled in order to achieve such quadrature outputs.

On the other hand, ring oscillators have a differential control, and quadrature outputs are simple to generate. The main disadvantage of ring oscillators is that their poor phase noise performance limits their wireless applications to situations where a wide band PLL could be used to inhibit the VCO phase noise.

Chapter 4

CMOS Differential PLL for Wireless Applications with a Differentially Controlled LC VCO

Differentially controlled monolithic LC-VCO along with a differential charge pump is used to implement a differential PLL for substrate noise immunity. The differential VCO control is achieved with a minimal increase in power consumption without sacrificing the tuning range. In a 0.5μm CMOS technology, the measured VCO phase noise is -119dBc @1.0MHz, and the tuning range is 26% of the 1.25GHz center frequency at a total power consumption of 4.0mA from 3.0 V supply. The common mode rejection of the VCO control lines is more than 46 dB at low frequencies. The new differential charge pump architecture provides common mode correction without the need for a clean reference. The complete PLL, including the the VCO, draws 13.6 mA from a 3.0 V power supply. The measured in-band phase

noise is -96 dBc at 30 KHz offset.

4.1 Introduction

The VCO, the heart of any PLL based frequency synthesizer, consumes a major portion of the synthesizer power. Its performance determines to a large extent that of the whole synthesizer. Therefore, integrating the VCO can reduce the total power consumption of the synthesizer. This is mainly because the RF preamplifier that buffers the VCO input to the prescalar could be eliminated. In a fully integrated VCO, the tuning range must be large enough to cover for the frequency variations over temperature, supply, and process corners. For a typical control voltage from 0 to 3.0 V, this mandates a very large VCO gain that increases the PLL sensitivity to supply, ground and substrate noise, and makes it very difficult to integrate with other components on the same chip. A differentially controlled VCO can significantly reduce this sensitivity, and facilitate the VCO integration with other components on the same chip.

In LC VCOs, the differential frequency control is not a straightforward task, and is usually achieved at the expense of reducing the varactor tuning range. This reduction in the varactor tunability increases the required VCO power consumption in order to restore the same frequency tuning range without degrading the phase noise performance. This extra power requirement could be understood by noting that a larger varactor is needed to increase the ratio of the variable capacitance to the fixed tank and circuit parasitics. For the same oscillation frequency, this increase in capacitance commands a smaller inductor value. To maintain the same

phase noise, the current must be increased to produce the same output power on the tank.

The objective of this work is to design a differentially controlled CMOS LC VCO without sacrificing the tuning range, and without consuming extra power. To integrate this VCO in a PLL, we use a differential charge pump with a very simple common mode correction circuit which does not need a clean reference. Although, CMOS technology is cheaper and has more potential for integration. In addition, the CMOS has unique advantages for achieving our goals; namely, the availability of fast PMOS devices as opposed to very slow lateral PNP's in many commercial bipolar technologies, and a much simpler biasing circuitry.

The next section is an overview of the varactor control schemes in a standard CMOS technology. In section 4.3, we outline the proposed differentially controlled VCO architecture, and the practical considerations of the circuit design. The effect of the VCO architecture on the phase noise is addressed. Section 4.4 is devoted to the differential charge pump architecture. The remaining sections discuss the PLL design, measurement results, and conclusions.

4.2 Overview of Existing Varactor Control Schemes

In order to reduce the VCO sensitivity to the noise generated by other circuits sharing the same substrate and/or supply, it is desirable to have a differential VCO. "*Differential*" refers to not only differential outputs, which help in rejecting common mode additive noise, but also to differential control inputs. The importance of differential control increases as we move towards higher levels of integration. This

principle of differential control is commonly used in both ring and relaxation type oscillators [41]. In these oscillators, the frequency is usually controlled by changing the bias current, which can be differentially accomplished in an integrated environment, without sacrificing the tuning range. The situation is different for LC based VCOs, where a single ended control is commonly used as a DC reverse bias for the PN diode used as a varactor. Fig. 4.1 shows a common architecture for integrated LC VCOs. The cross coupled differential pair Q1-Q2 represents a negative resistance for both tank circuits. The varactors C1 and C2 are connected, back-to-back, with their cathodes biased at V_{dd}. The control voltage V_{ct} is applied at the virtual ground point, and pulls the anodes below V_{dd} to keep the junction reverse biased at all times. Changing V_{ct} modulates the diode depletion capacitance, and hence, the oscillation frequency. The back-to-back connection eliminates the need for decoupling capacitors, and thus improves tunability.

Such architecture has been successfully used for bipolar technologies [51], where the base-emitter junction of an NPN is used as a varactor diode, and the unused base-collector junction is connected to the virtual ground. However, the nature of the varactor diodes available in CMOS processes is a major drawback in this architecture. As shown in Fig. 4.2, the varactor in a typical CMOS technology is built by diffusing a P^+ region over an N-well, which is the parasitic vertical PNP transistor available in such a process. The problem with this varactor structure arises from the N-well to P-substrate junction diode hanging on the sensitive tank circuit point as shown in Fig.4.1. This junction adds a large parasitic capacitance, which is in the same order of magnitude as the useful P^+ N-well junction capacitance.

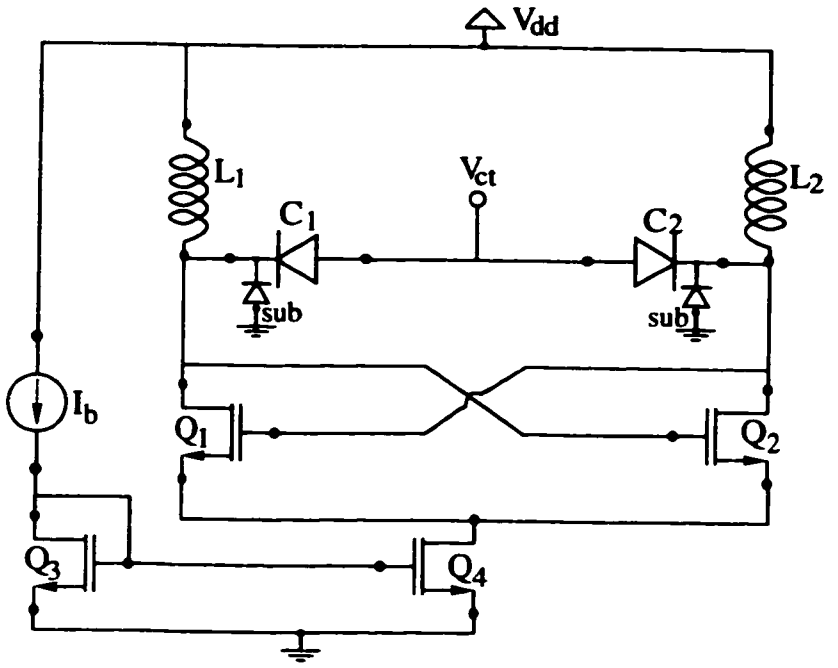


Figure 4.1: Classical NMOS LC based VCO

However, this capacitance is untunable, and severely reduces the tuning range of the VCO. The other drawback is that this capacitance is biased from V_{dd} to the substrate with the result of an increased oscillation frequency sensitivity to supply fluctuations. It is also clear that this architecture has a single ended frequency control.

A straight forward modification of this architecture to alleviate the parasitic junction diode problem and facilitate a differential control for the VCO is illustrated in Fig. 4.3. The capacitors C_{d1} and C_{d2} decouples the varactors from the circuit's DC. The varactors are then biased by the differential control inputs V_{ct1} and V_{ct2}. The AC decoupling resistors R_{ct1} and R_{ct2} are necessary to isolate the two differential RF output nodes. These resistors need to be large enough to minimize

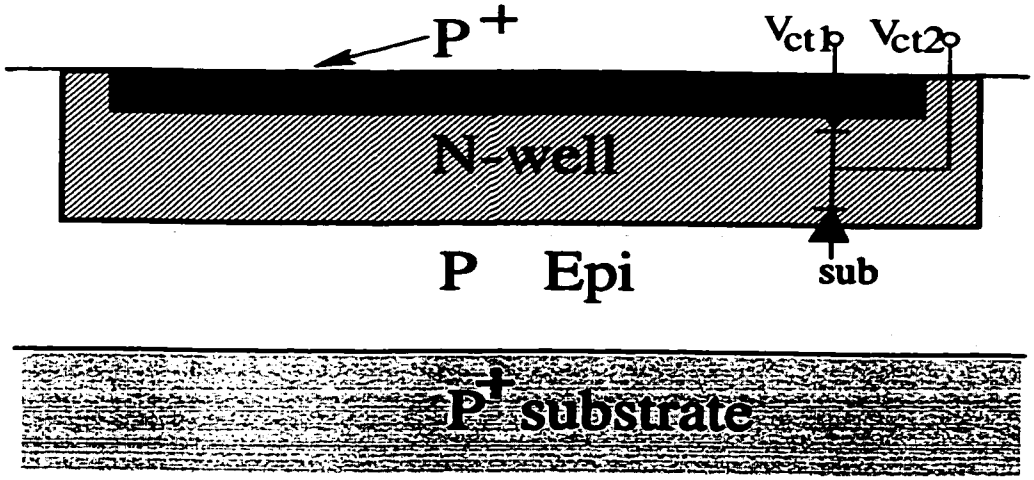


Figure 4.2: Varactor structure in a typical CMOS process

their loading effect on the VCO RF outputs. Even though the total noise voltage added by the resistor in an RC network reduces to KT/C and is independent of the resistance value, large resistance values may increase the noise power spectral density at low frequencies and its contribution to the varactor modulation. In addition to the differential control that can be achieved by using this architecture, the polarity of the varactor diodes could be chosen, as shown in the figure, to avoid the parasitic diodes effect by connecting them to the virtual ground at V_{ct1}. The decoupling capacitors must be large enough to limit the reduction in the effective varactor capacitance seen by the tank. The main problem with this architecture is the addition of parasitic capacitance to the tank due to the bottom plate capacitance of the large decoupling capacitors. In a typical CMOS process this capacitance is a considerable fraction of the main capacitor, and hangs in parallel with the main tank circuit reducing its tuning range. Consequently, this architecture becomes unusable for a typical process, where the achievable tuning range with a control voltage from

0 to 3.0 V is less than the frequency variations due to process tolerances.

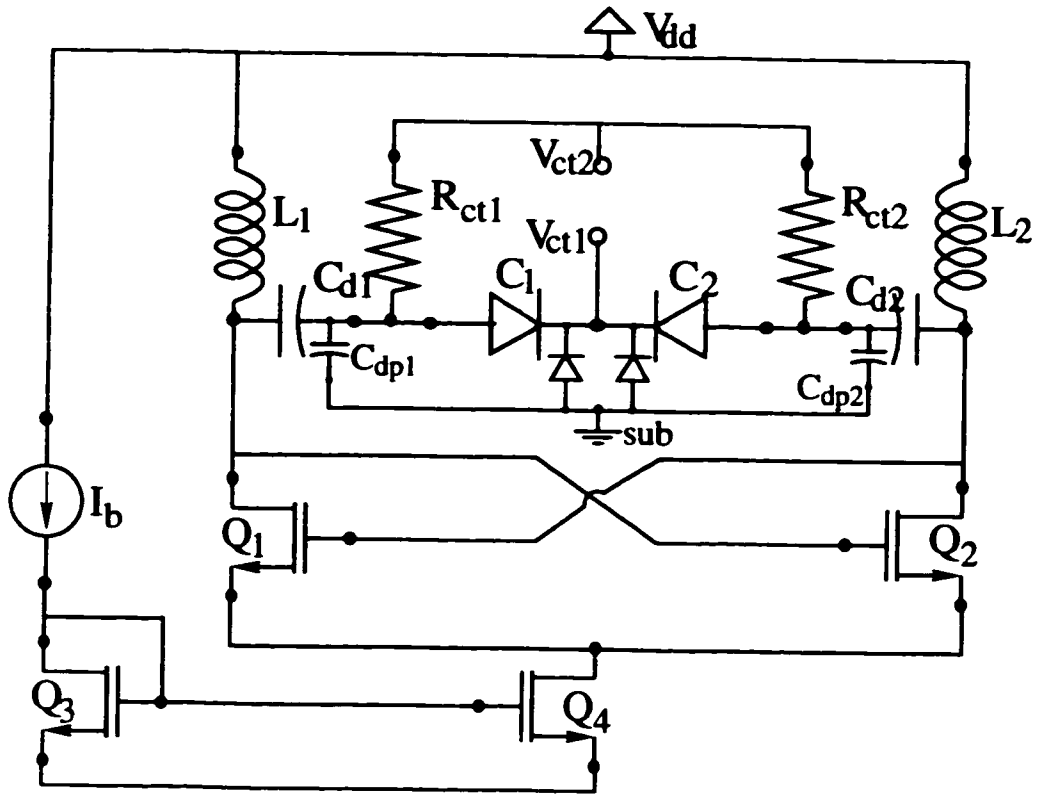


Figure 4.3: The use of decoupling capacitors for differential VCO varactor control

Rofougaran *et al* [8], proposed another technique to overcome the varactor parasitic diode effect (see Fig. 4.4). In this design, the anode of both varactors is connected to the real ground, and the cathode voltages are controlled by changing the voltage across the drop element (Q_3) to the inductors' common node. The Nwell to substrate diodes, which represented parasitic capacitances in other architectures, are a part of the tank varactor in this design. The main disadvantage of this architecture is the large variation in the VCO current over the tuning range. Another problem is the nonlinear relation between the control voltage and the voltage across

the varactor. A more recent technique [46] tries to reduce these two effects by using a more sophisticated voltage drop element. Clearly this architecture still does not provide differential control.

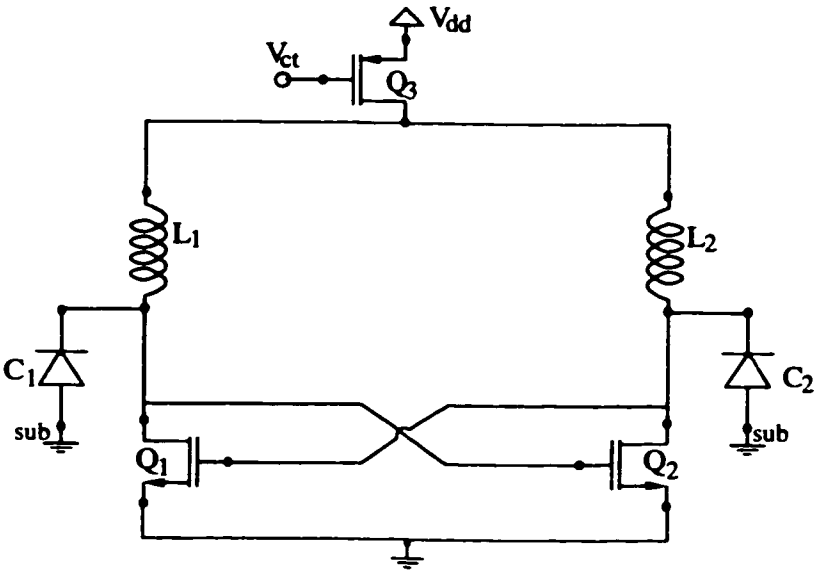


Figure 4.4: Varactor control using voltage drop element

4.3 Differentially Controlled CMOS LC VCO Using OpAmp Buffer

4.3.1 Architecture

The circuit proposed in this section [56] combines two methods of controlling the varactor, known in literature, to achieve what we call a "*semidifferential*" control of the varactor. The first method is the most commonly used varactor control scheme [28], illustrated in Fig. 4.1, and the second scheme is that of Fig. 4.4.

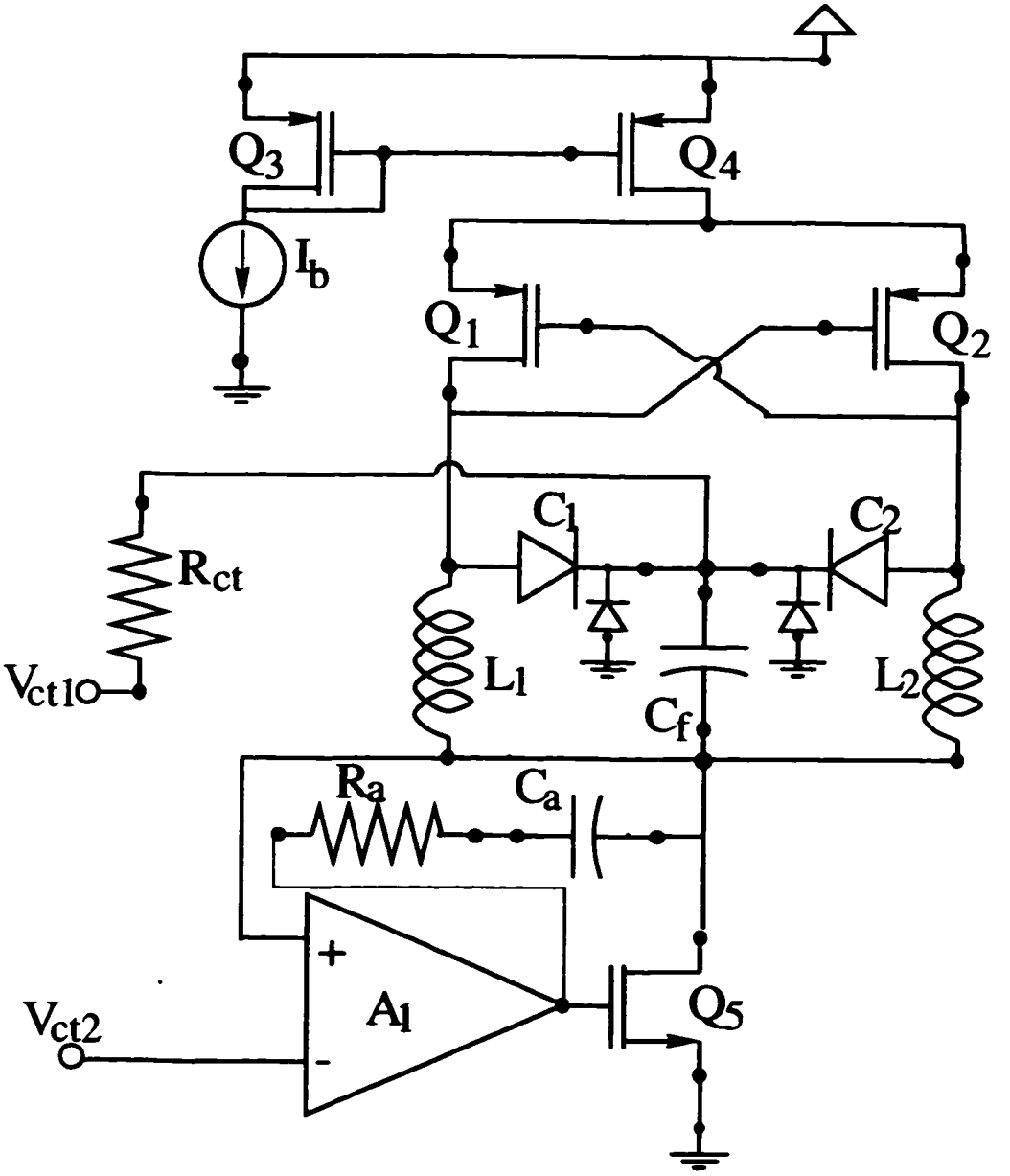


Figure 4.5: Proposed differential control architecture for an LC VCO

The new circuit proposed in Fig. 4.5 allows the control of both terminals of the varactor. The input V_{ct1} directly controls the varactor cathode terminal, whereas the input V_{ct2} controls the varactor anode through an OpAmp buffering stage (A1 and Q5). If the OpAmp open loop gain is high enough the control signal V_{ct2} can be almost exactly transfered to the varactor terminal within the buffer loop band width. The whole VCO with its main current source Q4 acts as a high impedance load (dominated by Q4 output impedance) for the second OpAmp stage Q5. Any interfering signal on V_{ct1} and V_{ct2} is transfered to the varactor terminals as common mode, and does not change the VCO frequency.

Why PMOS VCO Core?

Unlike the decoupling capacitor architecture of figure 4.3, this new proposed architecture does not solve the problem of the parasitic diodes between the varactor N-well to the substrate. To solve this problem we propose the use of PMOS transistors for the VCO core as shown in Fig. 4.5. There are several advantages in using this PMOS core:

- Most importantly, the polarity of the varactors change so that the parasitic diodes are at the virtual ground point but still maintain the entire supply range for tuning.
- Eliminate the parasitic diode problem and maintain a full swing control.
- Allow connecting the Nwell bulk of the PMOS transistors Q1 and Q2 to their source such that the drain to bulk diodes have a constant bias, and hence a constant capacitance, as long as the drain current is constant, regardless of

the control voltages. This could significantly reduce the oscillation frequency sensitivity to both ground and supply variations.

- The PMOS, being inside an Nwell is less susceptible to substrate noise pick up than NMOS.
- PMOS flicker (1/f) noise is an order of magnitude better than that of NMOS.

The main disadvantage of using a PMOS core is that larger device sizes are required to achieve the same G_M without increasing the bias current. This increase in the device size slightly reduces the tuning range. On the other hand, the $1/f$ noise is further reduced due to the larger device area [57].

4.3.2 VCO Design

The VCO of Fig. 4.5 is designed in a 0.5 μm CMOS technology for a center output frequency of 1.25 GHz. Two on chip square spiral inductors are used to build the differential tank circuit. Because of the thick top metal available in this process the 4.3 nH inductors have an estimated Q factor around 6 at 1.25 GHz. Each inductor has 2.75 turns and occupies a 300x300 μm^2. This large inductor area improves the Q factor, as long as it is limited by the metal series resistance. At higher frequencies (around 2.0 GHz) the substrate loss begins to dominate, and increasing the size degrades the Q.

PMOS transistors with a 400 μm width are used for the VCO core to provide enough open loop gain (around 3.0). The varactors are designed prescalar by using a number of parallel P^+-Nwell diodes. Each diode is designed as a narrow strip

of P^+ with Nwell contacts on both sides to reduce the series resistance, and to improve the Q factor. The estimated varactor Q is 13 with a resulting tank Q of ≈ 4.5. According to Hspice simulations, the tuning range is about 250MHz for the differential control voltages between 0 and 3.0 volts. This tuning range is enough to achieve the desired 25 MHz tuning around the 1.25 GHz center frequency at all the process corners, temperature, and supply variations from $0 - 70°C$ and 2.7-3.6 volts, respectively. The VCO core draws 4.0 mA from a 3.0 V supply. The simulated third harmonic level is -40dBc, whereas the second harmonic for a single ended output is -24dBc.

The VCO output is capacitively coupled to a 4.1 mA simple open drain NMOS differential stage that drives an on board 50 Ω load for testing. It is important to note that the capacitive coupling of the output is necessary, because the DC level of the VCO output varies with the control signal. Parallel to this buffering stage is another source follower stage (Fig. 4.6) that drives the capacitive prescalar inputs. This stage consumes 1.0 mA. The cross coupled pair Q3 and Q4 provide positive feedback to slightly boost the buffer output voltage for the same bias current [58]. Again, the output of this buffer is capacitively coupled to the prescalar CML inputs to restore its DC using resistor bias.

4.3.3 OpAmp Design

If an ideal operational amplifier existed, the architecture outlined is a great solution. Therefore, we must consider the different OpAmp non-idealities and their effect on the circuit performance. The noise introduced by the differential amplifier on one

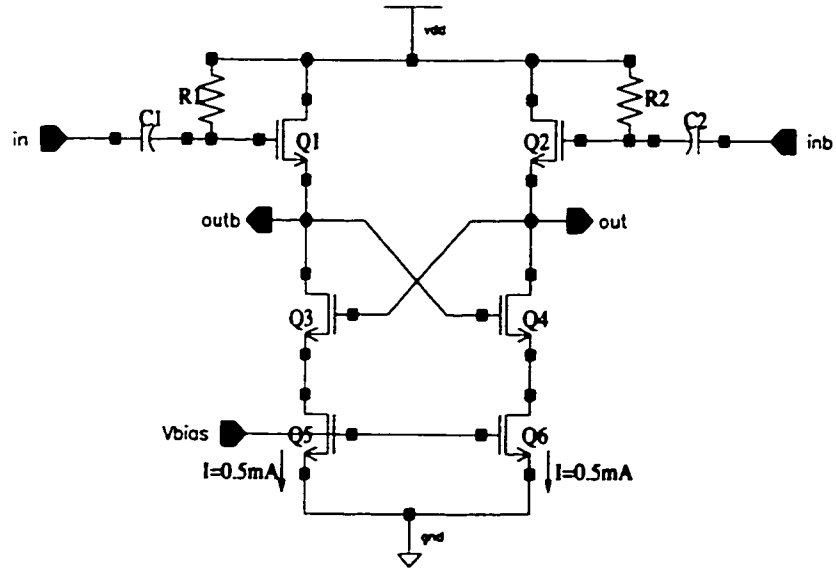


Figure 4.6: Differential VCO output buffer to drive the divider input

of the control lines is the most obvious problem. This noise is not in common mode for the differential control inputs, and directly modulates the varactors. In order to reduce this effect, the operational amplifier should be designed so that its noise contribution to the varactor modulation is much less than the expected common mode noise picked up on the control lines. Reducing the BW of the buffer helps to minimize this noise contribution. The problem, though, is that beyond this BW, the varactor terminal no longer follows the control voltage and we end up with an almost single ended control. Consequently, any common mode noise with frequencies much greater than the buffer BW is not rejected. Fortunately, the noise we are worried about is the low frequency one. The high frequency noise is filtered, to a large extent, by the PLL loop filter, secondly, the nature of the varactor modulation noise is inversely proportional to the frequency of the modulating signal. The filtering capacitor C_f attenuates any RF frequency noise, but if it is made too

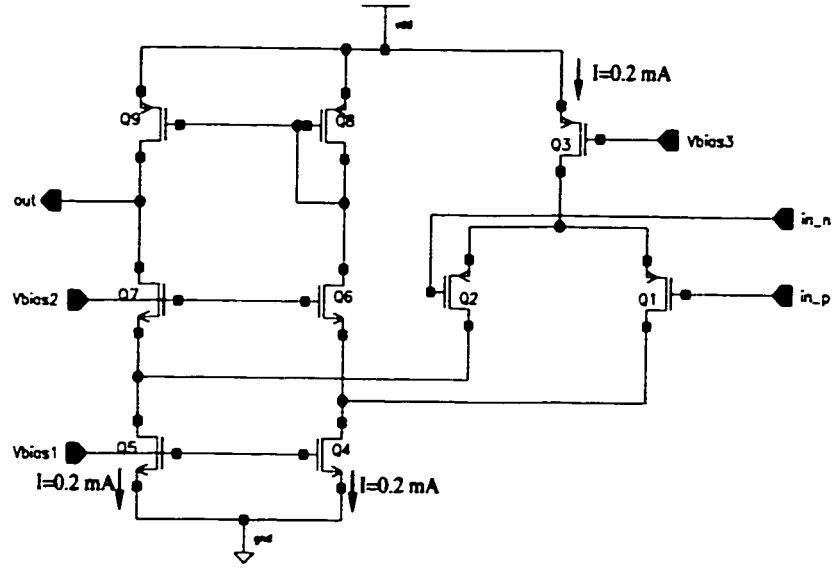


Figure 4.7: Folded cascode OpAmp used for VCO control buffering stage

large, instability develops in the buffer loop. Therefore, for noise with frequencies greater than the BW but too low to be attenuated by C_f, the situation may be worse than the one with single ended control. In this case, the varactor terminal is a high impedance node and more susceptible to noise. This noise can be filtered by the PLL loop filter in the single ended control situation. One way to solve this problem is to make the OpAmp BW as large as possible so that its dominant pole is due to C_f at the output. Further research is needed to investigate this circuit.

In addition, the OpAmp buffer is required to handle input voltage levels ranging from 0.0 V up to $V_{dd}/2$ or higher. In order to fulfill this requirement a folded cascode OpAmp with a PMOS input stage is used (see Fig. 4.7). Also, the PMOS input stage (Q1 and Q2) has the advantage of lower $(1/f)$ than NMOS. To further reduce the flicker noise, we increase the size of the PMOS input transistors. The NMOS current sources (Q4 and Q5) are designed with a large channel length to

increase their output impedance, and hence, the stage gain, and to reduce their input referred $1/f$ noise contribution [57]. The g_m of Q4 and Q5 is much smaller than that of the input pair Q1 and Q2, which minimizes their thermal noise contribution. Increasing the bias current reduces the overall input referred thermal noise by increasing the G_M of the input devices. However, this current cannot be too large, because the stage gain is inversely proportional to the square root of the bias current. This differential stage gain is 60 dB, which is large enough to minimize the noise contribution of the second NMOS stage (Q5 in Fig. 4.5). Therefore, the closed loop output noise is approximately equal to the input referred noise of the first stage. In order to guarantee a stable operation, a lead-lag miller compensation branch (C_a and R_a in Fig. 4.5) is used to produce a dominant pole at the output node of the first stage. The amplitude and the phase response of the open loop OpAmp in figure 4.8, show a 68° phase margin. Fig. 4.9(a) illustrates the resulting closed loop buffer gain, Fig. 4.9(b) shows its output noise at the varactor control node.

The buffer closed loop BW, determined by the compensation branch (C_a and R_a) is 8 MHz within which the differential control common mode rejection is above 46 dB. This BW is well beyond the PLL loop BW and the architecture should reject any common mode noise within the loop BW. This is also important to avoid degrading the PLL stability due to the extra pole. The settling time of the VCO output due to the buffer loop transients is approximately 100 ns, which is much faster than the PLL loop transients. The resistance R_{ct} and the capacitor C_f act as a low pass filter for the direct control signal V_{ct1} with a BW equal to that of the

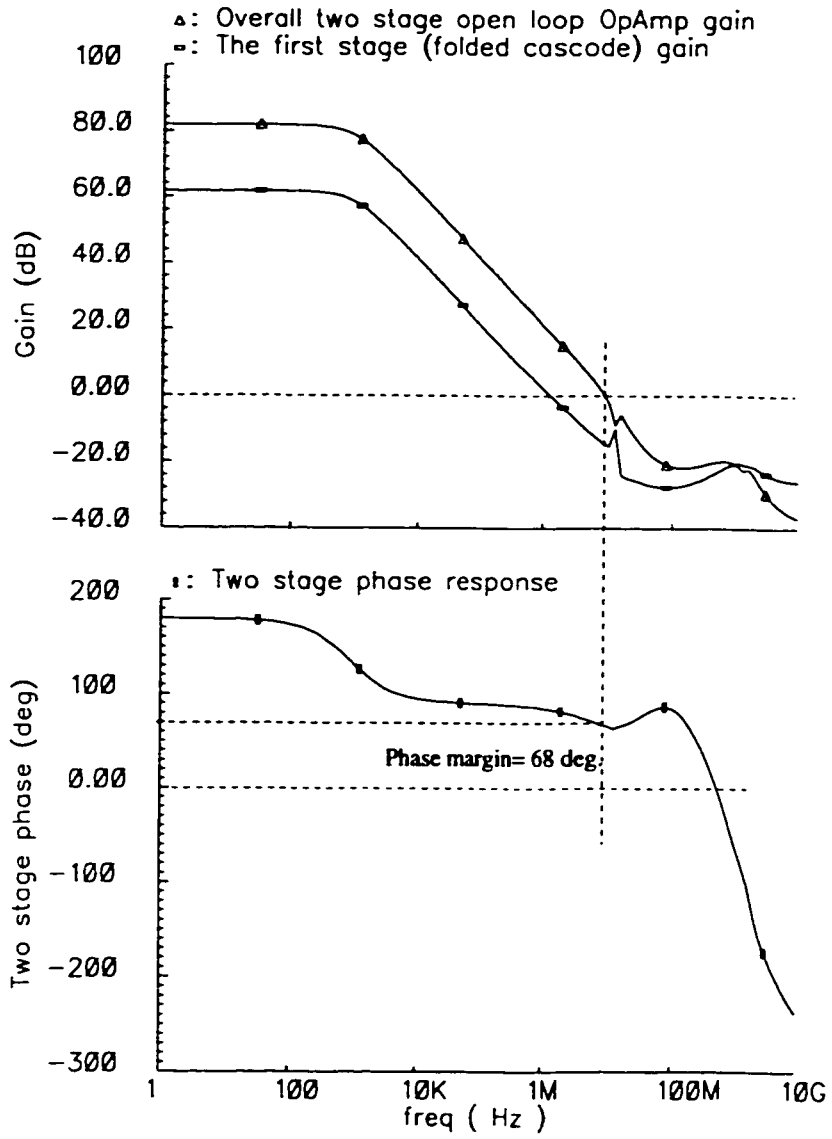
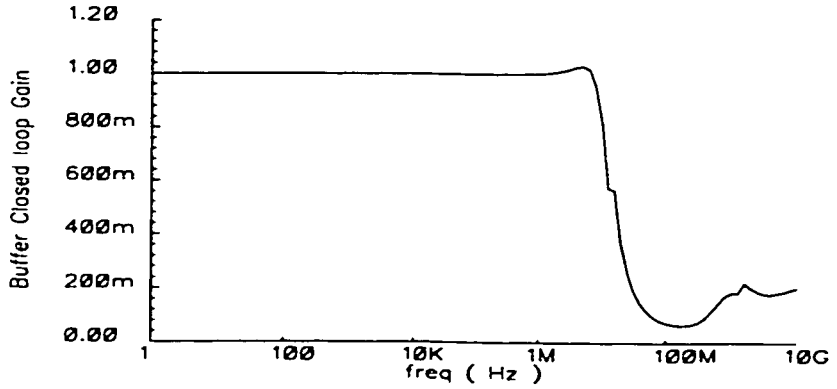
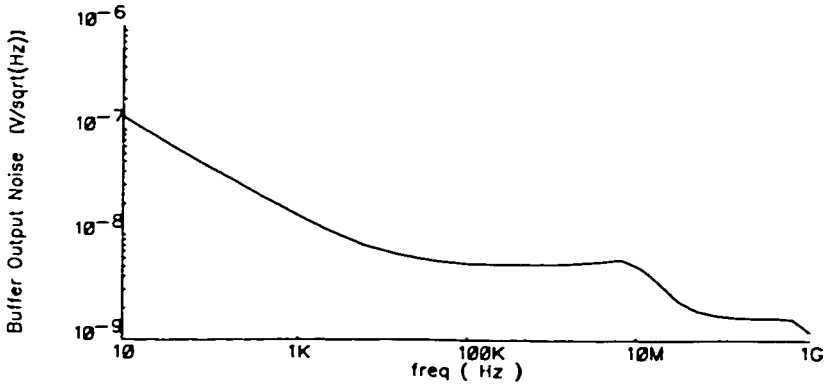


Figure 4.8: Open loop response of the OpAmp buffer



(a) Two stage OpAmp buffer closed loop gain



(b) OpAmp buffer output noise at the varactor control input

Figure 4.9: Closed loop OpAmp buffer gain and noise

OpAmp buffer, in order to slow down the common mode rejection degradation at higher frequencies.

4.3.4 Effect on Phase Noise

As detailed in chapter 3, the VCO phase noise output has both internal and external components. The internal phase noise is commonly estimated using Leeson's formula, whereas the external noise or the varactor modulation noise may be described using Eq. 3.6 which is repeated here for completeness.

$$S_{n\_varactor}(\Delta\omega) = \frac{1}{2}\left(\frac{2\pi V_{n\_var\_in\_rms} K_{vco}}{\Delta\omega}\right)^2. \tag{4.1}$$

The control circuit is carefully designed to minimize the effect of the varactor modulation noise. In order to estimate the output phase noise, the VCO core is simulated in an open loop condition using linear Hspice AC analysis to obtain the equivalent output noise voltage, which is used to calculate the value of the factor F in Leeson's formula as

$$F = \frac{V_{noise}^2}{4KTR_p} \tag{4.2}$$

where R_p is the equivalent parallel tank resistance at the oscillation frequency and is estimated to be 200 Ω. The resulting internal phase noise is around -100dBc@100KHz offset frequency from the center frequency of 1.25 GHz.

To estimate the amount of noise added by the control circuitry, we use AC analysis of the control buffer. The simulated thermal noise level at the varactor input

as shown in Fig. 4.9(b) is approximately 5.3 nV/$\sqrt{Hz}$ with a (1/f) noise corner frequency of 11 KHz. For a VCO gain of 85 MHz/volt the varactor modulation noise is estimated to be -109dBc@100KHz. The result is only 0.5 dB degradation in the overall VCO phase noise.

4.4 Differential Charge Pump with Common Mode Control

In this section, we present a new charge pump common mode control architecture, suitable for use with the differential VCO proposed in section 4.3. Before describing the new architecture, we briefly explain the need for a common mode control in a differential charge pump driving a differential VCO. Because of the unavoidable mismatches between the NMOS and PMOS current sources forming the charge pump, there is a net current going to the loop filter even when the PLL is in lock. This current causes the two differential control voltages to drift independently. The loop will correct for only a differential drift not a common mode drift. The common mode can then drift freely, and saturate the charge pump. Another effect of the common mode drift that is specific for our differential VCO architecture, is a common mode voltage above 1.5 volts may saturate the VCO, causing the oscillation to die out.

A common problem with different common mode control schemes is the lack of a clean reference for the common mode signal to locked. The noise on this reference line is directly coupled to the charge pump output. It is also desirable

not to have this common mode control circuit on all the time so that we don't lose the important advantage of the charge pump which, should ideally turn off when the PLL is in lock.

4.4.1 Architecture

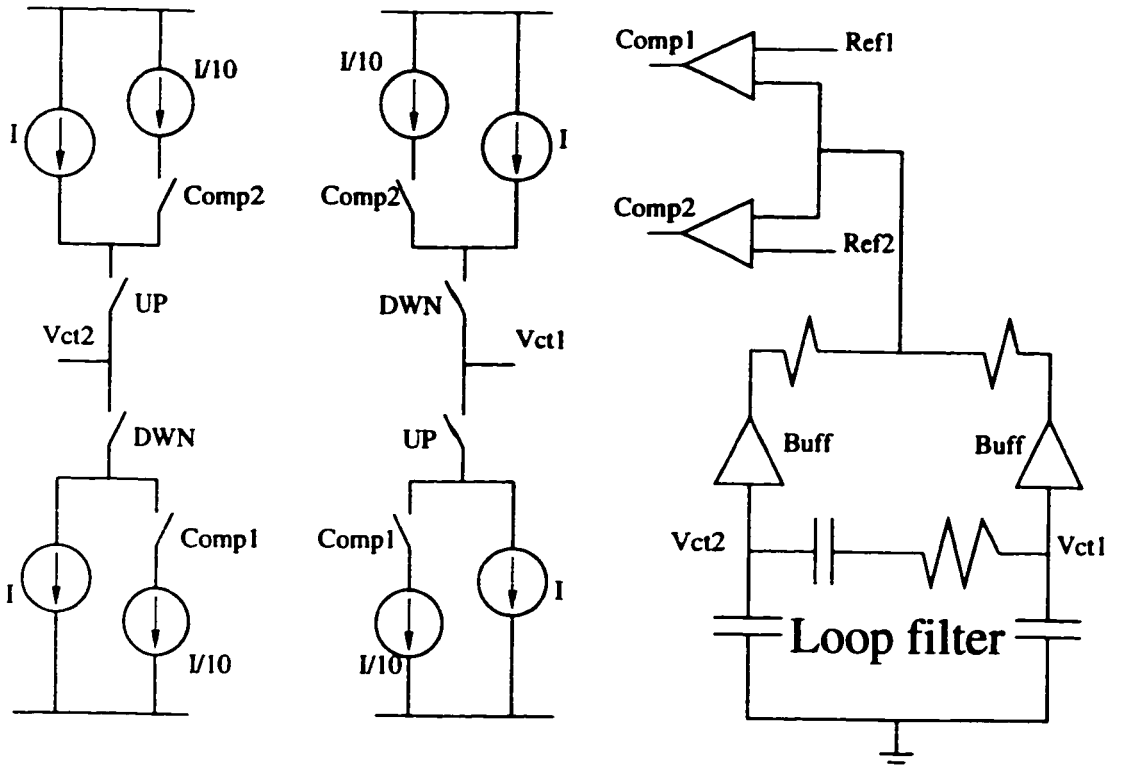


Figure 4.10: Proposed differential charge pump architecture

The architecture proposed in Fig. 4.10 doesn't actually attempt to tie the common mode of the control signals to a fixed reference, Instead, it forces the common mode level between two closely spaced references. This guarantees that neither the charge pump nor the VCO gets saturated. The noise of these two

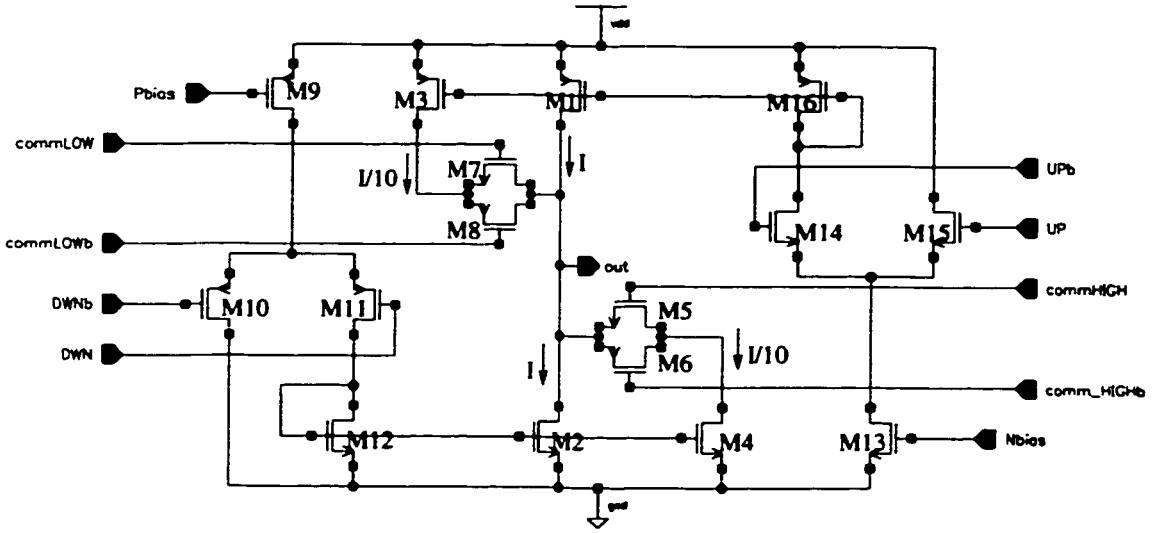


Figure 4.11: One half of the differential charge pump with the offset currents for common mode control

references is not critical, as the control circuit works in an open loop mode, and is off most of the time. This occurs because the common mode drift is a relatively slow process.

The full operation can be explained as follows: two simple source follower buffers are used with two summing resistors to detect the common mode value of the two control signals. Then, this signal is fed to a tristate comparison stage which uses two simple parallel comparators together with the two voltage references (Ref1 & Ref2) to generate two output signals. Both signals are zero as long as the common mode is between the two references. Once the common mode drifts beyond this range, one of the comparators outputs a one signal, which is used to add an intentional offset to either the positive or the negative current sources, depending on whether the common mode is to be pushed up or down. The offset (common mode control) current is switched on only when the charge pump is active. The value of the

offset current is designed such that it provides enough current to push the common mode to midway between the two references in one PLL reference frequency cycle. However, care should be taken that it doesn't push the common mode beyond the two references, which may cause the common mode control loop to oscillate around the two references and never actually settle between them.

4.4.2 Circuit Design

Fig. 4.11 is the detailed circuit implementation of one half of the differential charge pump with offset current controls for the common mode correction. In order to describe the operation, we consider only the UP current source (I) flowing through M1. The offset current source (I/10) through M3 is connected in parallel with the main current source M1 using the pass gate switch M7 and M8. This switch turns on when the common mode drifts down. Both current sources are biased by the diode connected transistor M16, which is controlled by the differential input pair M14 and M15. The current of this bias branch should be high enough to turn on the main current source with reasonable speed. In our design we chose I=300 μA with a bias branch current of 100 μA. Two identical charge pumps with opposite control inputs achieves the differential charge pump operation.

4.5 The Complete PLL

To complete the PLL design, the VCO output is fed to a fixed divide-by-16 CML prescalar. The prescalar output is converted to CMOS and fed to a programmable CMOS divider. A dead-zone free CMOS PFD is used to compare the divider output

to an external reference source. The PFD outputs control the differential charge pump, which drives an off-chip loop filter as shown in Fig. 4.10. The filtered signal is then applied to the VCO control inputs to close the PLL loop.

4.6 Experimental Results

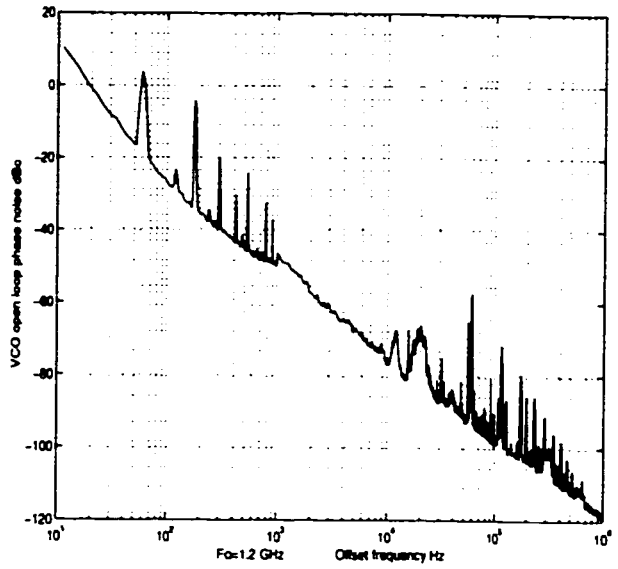


Figure 4.12: Measured open loop VCO phase noise at a carrier frequency of 1.2 GHz

The differential PLL components are integrated into a test chip using a 0.5 μm CMOS process, and packaged in a low profile TSSOP20 package. Fig. 4.12 plots the measured VCO phase noise. The values of -99dBc@100KHz and -119dBc@1.0MHz are close to the simulated ones. This confirms that the contribution of the control circuit is very small. The multiple spurs in the phase noise plot are due to the fact during this measurement both controls were connected to ground, which is outside

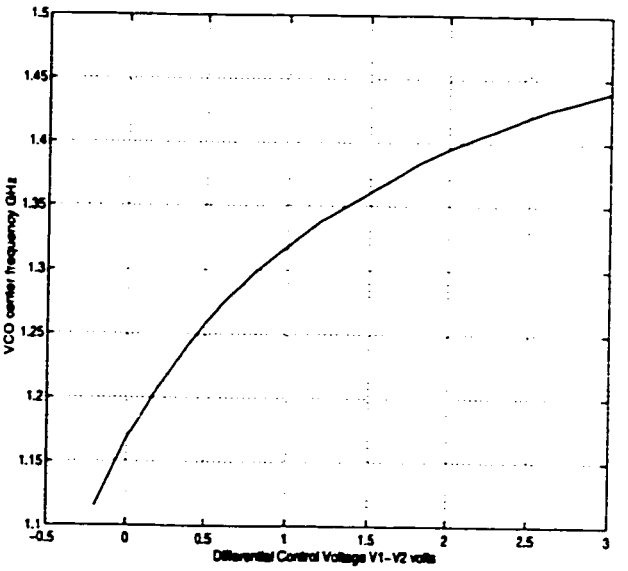


Figure 4.13: Measured VCO output frequency over the entire differential ($V_1 - V_2$) range

the linear range of the OpAmp buffer input. Thus, the corresponding varactor terminal suffered from several frequency components pickup. Fig. 4.13 shows the differential VCO tuning range from 1.115 GHz at -0.2 V where the varactors are slightly forward, to 1.440GHz at 3.0 V. Changing the common mode of the control voltage from .3 V to 1.5 V has changed the 1.2 GHz output frequency by only 638 KHz. This indicates an excellent common mode rejection of more than 46 dB at DC. A good supply rejection is also measured. Changing the supply from 2.5 to 3.5 V results in only a 1.275 MHz change to the 1.2 GHz VCO frequency. In order to measure the common mode rejection of the VCO at higher frequencies, both the VCO control terminals are shorted together and connected to a 1.0 V common mode voltage. A 200 mV (p-p) signal is applied at the common control node, and the output spur level is measured and plotted in Fig. 4.14. The spur levels are

levels are below -27 dBc for all the frequencies. Within the buffer loop BW, lower spur levels are observed and the level decreases with the frequency as expected. Once the frequency exceeds the loop BW, the common mode rejection becomes weak and the spurs rise again. It is noteworthy that the transition between the two regions of the common mode rejection curve in Fig. 4.14 is a smooth one. The sharp minimum in the figure is only due to the small number of the measurement points.

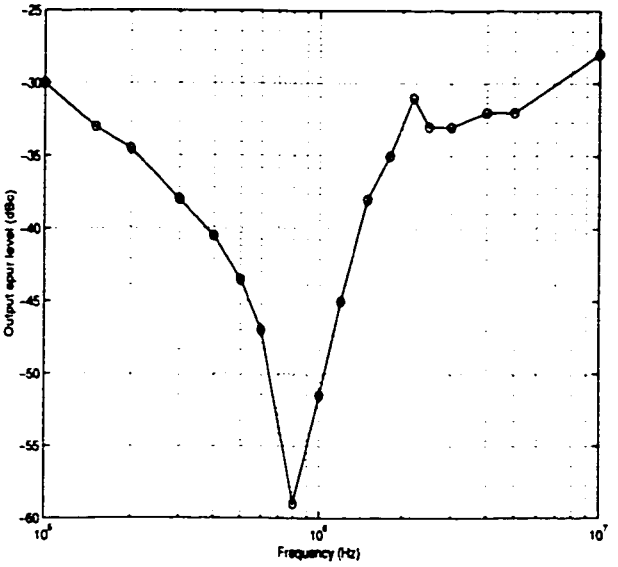


Figure 4.14: Measured VCO output spurs for a 200 mV (p-p) signal applied at a differential control voltage. The differential control is set to 0 V and VCO frequency is 1.164 GHz

To test the charge pump and the common mode control architecture, the loop is closed with a fixed division ratio of 48. The input reference is swept from 22.35 MHz to 29.72 MHZ to cover the full VCO range. The loop does lock correctly over the whole range. This means the common mode control architecture is functioning

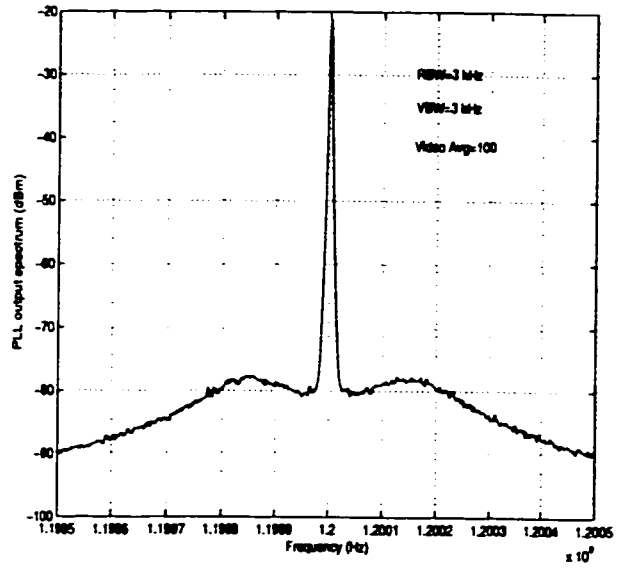


Figure 4.15: Measured VCO output frequency over the entire differential ($V_1 - V_2$) range

In order to measure the in-band PLL phase noise, the loop is locked to a 25 MHz low noise source with the same division ratio. The loop BW is 200 KHz, and the output spectrum is plotted in Fig. 4.15. The in-band noise is -96 dBc at 30 KHz offset from the 1.2 GHz center frequency. This noise level may be further reduced by increasing the charge pump current. In this case, the loop filter capacitance must be increased to maintain the same BW. The supply rejection of the whole PLL is also measured by applying a 200 mV (p-p) signal and measuring the output spurs. Fig. 4.16 is a plot of the resulting spur levels at different offset frequencies which are below -30 dBc.

The total PLL current consumption is 13.6 mA, plus 4.1 mA for the output buffers from a 3 V supply. The chip die photograph is shown in Fig. 4.17.

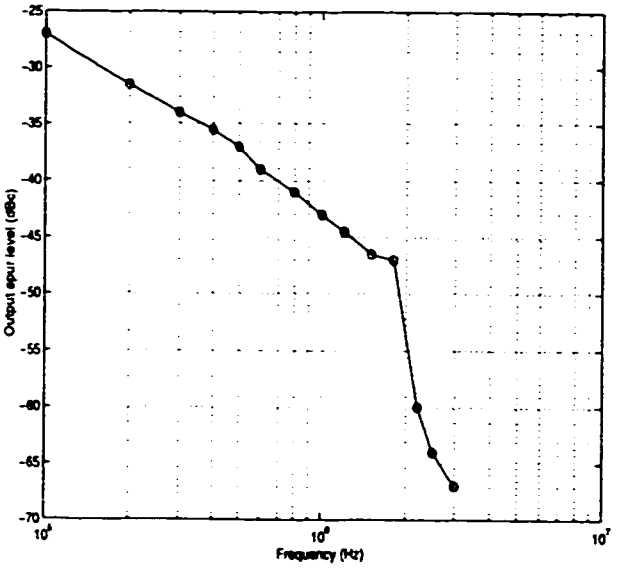


Figure 4.16: Measured PLL spurs for a 200 mV (p-p) signal applied at the supply. (The reference frequency is 26 MHz and the VCO frequency is 1.248 GHz)

4.7 Conclusion

An OpAmp buffer is successfully used to differentially control a CMOS LC-VCO with very small degradation in the phase noise, and no reduction in the tuning range. The increase of the power consumption of the differential VCO over that of a single ended one is less than 10%. A simple open loop common mode control is used with a differential charge pump in a fully integrated PLL. The open loop nature of the common mode control circuit eliminates the need for a clean voltage reference and uses two crude references instead. The differential control reduces sensitivity to supply, ground, and substrate noise.

In a 0.5 μm CMOS technology, the differential PLL achieves an in-band noise of -96 dBc at 30 KHz offset from 1.2 GHz. This noise is achieved with a 25 MHz

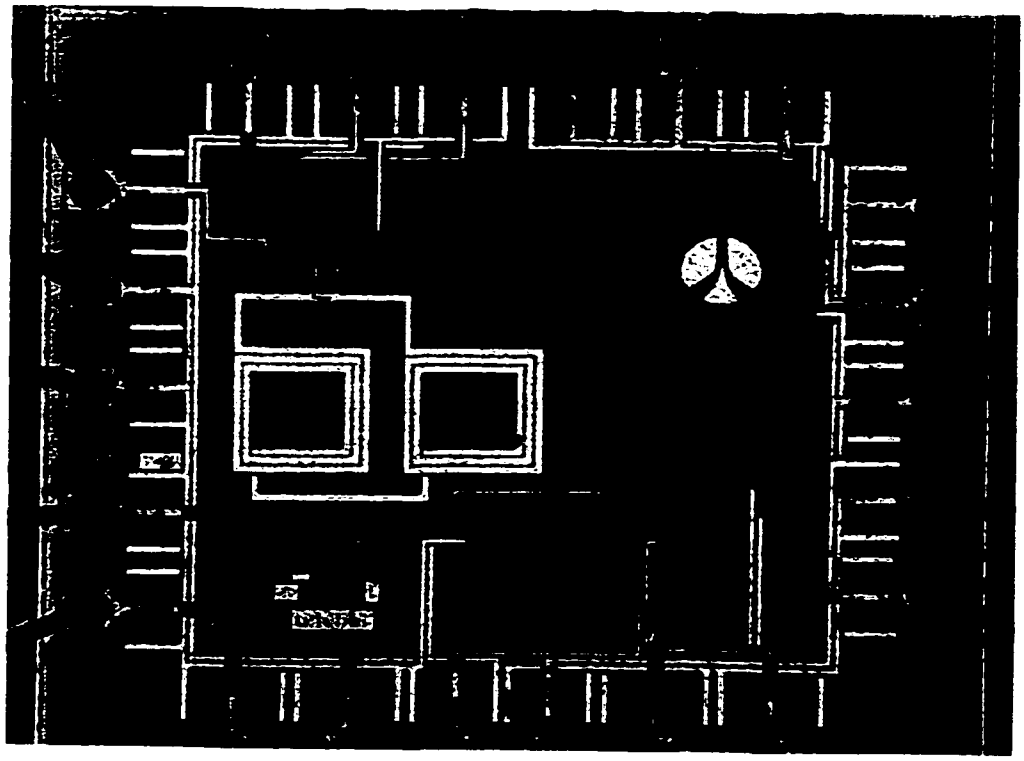


Figure 4.17: Differential PLL chip die photograph

reference frequency, and 13.6 mA current consumption from a 3 V supply. The VCO phase noise is -119 dBc at 1 MHz offset, and its tuning range is 26%. The differential VCO control provides a 46 dB common mode rejection. When the supply is changed from 2.5 to 3.5 V, the VCO output frequency changes by only 1.27 MHz. This supply sensitivity is much lower than other single ended VCOs.

Chapter 5

Low Phase Noise LC Quadrature VCO Using Coupled Tank Resonators in a Ring Structure

The concept of coupled resonators is employed in a ring VCO architecture to reduce the phase noise. This architecture allows the design of low phase noise VCOs using integrated low Q inductors. Quadrature differential outputs are also realized with this architecture. Two monolithic LC tanks are coupled together to implement a transimpedance resonator with an effective Q close to twice that of the single tank. In addition, the coupled tank transimpedance resonators provide 90° phase shift between the input current and the output voltage. The transimpedance resonator is driven by a transconductance gain stage. Four such stages are cascaded in a ring structure to provide I-Q differential outputs, and to further reduce the phase noise. The increase in the output noise power due to extra circuit components

is proportional to the number of stages, whereas the phase noise reduction due to the increased frequency selectivity is proportional to number of stages squared. Consequently, a net phase noise reduction is obtained. Phase noise analysis of the VCO architecture shows approximately 4 dB possible improvement over conventional cross coupled pair I-Q VCOs. A prototype of the VCO is built in a 0.35 μm CMOS technology. The measured phase noise is -122 dBc at 600 KHz offset from 1.93 GHz. The VCO draws 9.2 mA from a 3 V supply, and occupies a chip area of 1.1x1.1 mm^2.

5.1 Introduction

Many modern wireless transceiver architectures require the LO to have both *In-Phase* (I) and *Quadrature* (Q) outputs. Usually, these I-Q outputs are required to have carefully matched amplitudes, and a phase error within a fraction of a degree in their 90° phase shift. Three different ways are commonly used to generate these I-Q signals. An *RC-CR* 90° phase shift network produces a relatively large amplitude and phase mismatches, due to their dependence on process variations of in the absolute values of both the resistor and the capacitor. In order to reduce these errors bulky and power consuming phase correction circuits are needed [59]. Another approach is to run the LO at twice the required frequency (or use a frequency doubler); then use a master slave Flip Flop to divide the frequency by two. The master and slave outputs of the Flip Flop are in quadrature, and can be used to drive the mixer. Any second harmonic content in the VCO output degrades the accuracy of this technique. In addition, the VCO is required to run at double the LO

frequency, which not only increases the power consumption, but also complicates the design as the technology limits are approached.

The problems associated with the two I-Q generation techniques has motivated researcher to investigate VCO architectures that can inherently produce these quadrature components. A 4-stage, inverter based, ring oscillator is a common example of quadrature oscillators. However, the poor phase noise performance of these ring oscillators limits their applications in wireless systems.

The majority of LO's for wireless applications use LC tank based VCOs to improve the phase noise. These oscillators don't normally produce quadrature outputs and new architectures are needed to generate the I-Q outputs. Some recent designs [8, 54], relies on coupling two differential VCOs in order to produce quadrature outputs with accuracy that is only limited by the device matching on the chip. However, this technique doubles both the area and the power consumption of the VCO in order to achieve the quadrature signal, and provides no significant gain in terms of phase noise.

For a low phase noise VCO design we need passive components (inductor and varactor) with high quality factors. The lack of such components in an integrated environment has motivated this work, where we can utilize the extra area and power needed for the quadrature output generation to improve the phase noise as well. Only integrated spiral inductors and varactors are used in a low phase noise VCO design.

The goal is to use these low Q integrated components to build a highly selective coupled tank resonator. In principle, a second order bandpass filter which is com-

posed of two weakly coupled tanks may have a Q factor twice as high as that of a single tank. This doubling has a significant impact on the VCO phase noise. However, the transimpedance of such a high order filter normally has a 90° phase and cannot directly replace the single tank circuit in conventional VCO architectures. The VCO architecture presented in this work utilizes four coupled tank resonators in a ring structure that inherently generate quadrature outputs and significantly reduces the phase noise.

In the next section we examine some of the existing quadrature VCO architectures and their effect on the phase noise. In section 5.3, we present the principle of coupled tanks resonator and define the equivalent Q factor. Then, the proposed VCO architecture and its effect on phase noise is depicted. In section 5.5 we discuss the implementation issues in a CMOS technology, and present our prototype circuit design. The last three sections cover both the simulation and measurement results, and a conclusion.

5.2 Overview of Existing I-Q Oscillator Architectures

Two VCO architectures are commonly used for I-Q generation. The most straightforward way is to use a four stage ring oscillator. However, these ring oscillators are not suitable for wireless application, due to their poor phase noise. Other I-Q VCO architectures are based on coupling two LC differential VCOs in order to produce the quadrature outputs. The block diagram of this architecture is illustrated in Fig.

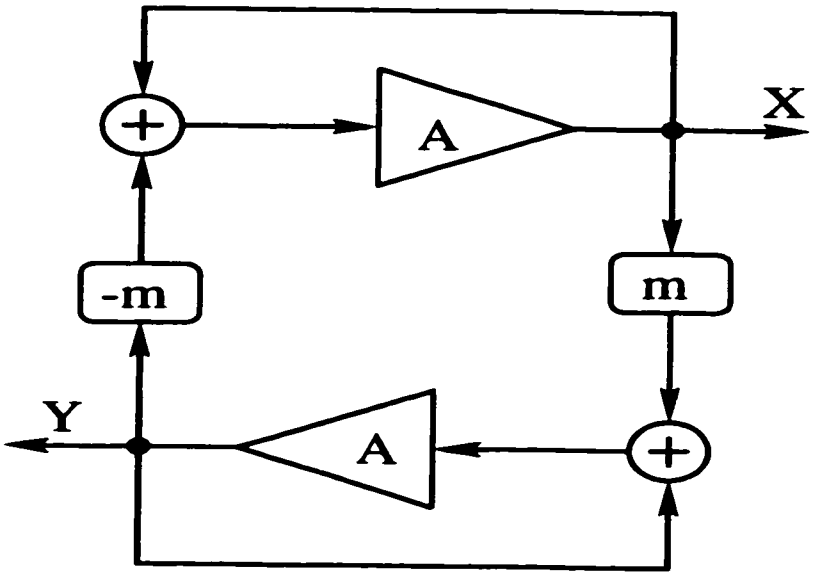


Figure 5.1: The use of coupled VCOs to produce I-Q outputs

5.1. The power consumption of the VCO in this case is twice that of a single phase one. In addition, a large coupling factor (m) is needed between the two VCOs to prevent multiple oscillations [54]. This large coupling coefficient shifts the oscillation frequency away form the LC tank resonance frequency. Consequently, the effective Q factor is lower and the phase noise is higher. This loss in the effective Q factor cancels out the phase noise reduction suggested by the coupled oscillator theory [60], as will be discussed in section 5.5.3.

5.3 Principle of Coupled Resonators

The order of a bandpass filter can in general be increased to improve its selectivity. A second order bandpass filter consists of two similar resonators with a coupling network in between. Reactive coupling networks are often preferred over resistive

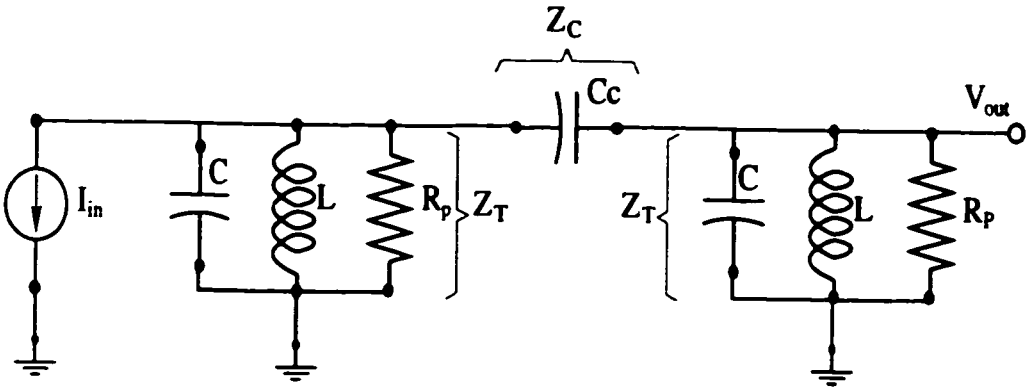


Figure 5.2: Second order transimpedance filter with series capacitive coupling

ones to preserve the Q factor of the individual tanks. This network may be either inductive or capacitive. It may also be a series or a parallel network. Fig. 5.2 illustrates a transimpedance filter with a series capacitive coupling. This transimpedance configuration is desirable for our application, because it is similar to that of a single tank resonator. The choice of the coupling configuration, as well as the coupling factor k are critical to achieve the required performance. Without loss of generality, the coupling factor k is defined in the series capacitive coupling case, as the ratio of the coupling capacitor C_c to the tank circuit capacitor C. The transimpedance transfer function defined as the ratio of output voltage to the input current is written as

$$Z_{eff} = \frac{V_{out}}{I_{in}} = \frac{Z_t^2}{Z_c + 2Z_t} \tag{5.1}$$

where Z_t and Z_c (see Fig. 5.2) are the single resonator impedance and the coupling element impedance, respectively. Ideally, if Z_c is much greater than Z_t and the Q factor of Z_t is high enough, the denominator may be considered as constant over all

frequencies within the bandwidth (BW) of Z_t. thus, Z_{eff} is directly proportional to Z_t^2 and has a BW equal to one half that of the original resonator. The effective quality factor Q_{eff} is then doubled. In practice, these very weakly coupled resonators cannot be used in a VCO design because of the large attenuation due to the large value of Z_c.

Therefore, we need to compromise between doubling the Q and allowing a reasonable attenuation. It is noteworthy that at resonance, Z_{eff} has a phase shift close to 90°. Thus, a different VCO configuration is needed to make use of that shift. In the following sections, this phase shifting property is used to design an oscillator with quadrature outputs.

In order to quantify both the Q enhancement and the transimpedance gain reduction, we consider the circuit of Fig. 5.2. The real and the imaginary parts of $1/Z_{eff}$ can be written in terms of the circuit elements as

$$Re(1/Z_{eff}) = \frac{2}{R_p}[1 + \frac{1}{\omega Ck}(\omega C - \frac{1}{\omega L})] \tag{5.2}$$

$$Im(1/Z_{eff}) = 2(\omega C - \frac{1}{\omega L}) + \frac{1}{\omega Ck(\omega C - \frac{1}{\omega L})^2} - \frac{1}{R_p^2 \omega Ck} \tag{5.3}$$

where we substitute $C_c = kC$. Now we define the resonance frequency (ω_o) to be the frequency at which the real part is equal to zero. This gives the 90° phase shift that we'll be using in our VCO design. Equating the real part to zero we obtain

$$\omega_o = \frac{1}{\sqrt{LC(1+k)}}. \tag{5.4}$$

Substituting this in Eq. 5.3 we get

$$Z_{eff}(\omega_o) = jR_p\frac{Qk}{1+Q^2k^2} \tag{5.5}$$

where the fraction represents the gain reduction due to the voltage drop across the coupling element. Then calculating Q_{eff} from the definition $Q = \frac{\omega}{2}\frac{d\phi}{d\omega}$ [41], where ϕ is the phase of Z_{eff}, we get

$$Q_{eff}(\omega_o) = 2Q\frac{1+k}{1+Q^2k^2} \tag{5.6}$$

where the fraction corresponds to the effective Q reduction due to the finite value of the coupling element impedance. Another useful value is the resonator input impedance (Z_{in}), which determines the output voltage swing of the oscillator. Ideally for a very small coupling coefficient k this impedance is equal to that of the single tank; i.e., R_p at resonance. It can be easily shown that in the case of finite coupling, Z_{in} at the 90° phase shift resonance frequency can be expressed as

$$Z_{in}(\omega_o) = R_p\frac{1}{1+Q^2k^2}. \tag{5.7}$$

Equations (5.5-5.7) suggest that the value of Qk should be chosen such that a good compromise between increasing Q_{eff} and the gain requirement is attained. This value of Qk, known as the normalized coupling coefficient, should be less than one to avoid multi peaking in the frequency response [61]. Fig. 5.3 illustrates both the phase and the amplitude frequency response of the circuit of Fig. 5.2, for different values of the coupling coefficient k assuming a typical value of $Q = 5$. The

response of a single tank resonator is plotted on the same graph for comparison. A reasonable choice for Qk value is 0.5, which gives $Q_{eff} = 8.8$ and an attenuation factor $Z_{eff}/R_p = 0.4$.

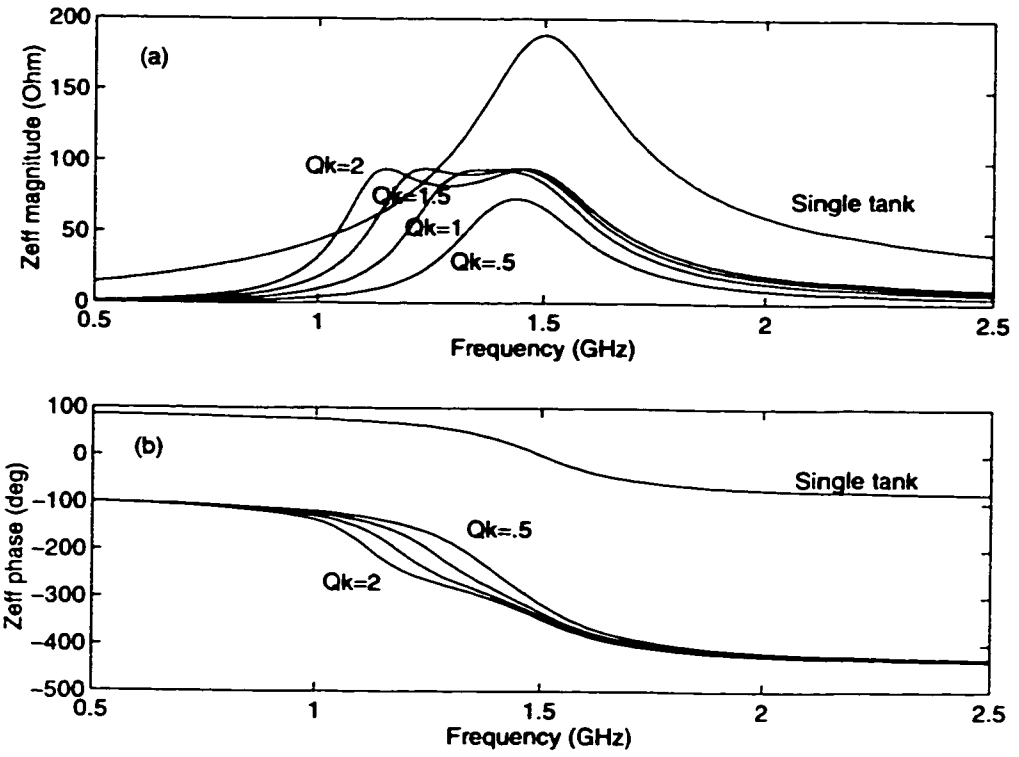


Figure 5.3: The effect of the coupling factor on Z_{eff} amplitude (a), and phase (b)

5.4 Proposed VCO Architecture

5.4.1 Architecture

The dual tank resonator outlined in the previous section cannot be directly used in the classical cross coupled VCO configuration of Fig. 5.6(a). That is because of

phase shift between the input current and the output voltage, that may offset the VCO oscillation frequency from the resonator resonance frequency. This frequency offset causes a degradation in both the loop gain and the effective Q factor. A better way to deal with this phase shift, which is close to 90°, is to push it to be exactly 90° with much less degradation in the gain and Q_{eff}. A VCO architecture that achieves this, and utilizes the phase shift to generate quadrature (I-Q) outputs is proposed in Fig. 5.4. The architecture is comprised of a 4-stage positive feedback loop. Each stage provides a 90° phase shift with a total of 360° around the loop. This phase condition determines the potential oscillation frequency. The second condition for oscillation requires the open loop gain be greater than unity at that frequency. This requires an active element transconductance gain G_m greater than $1/Z_{eff}(\omega_o)$, at each stage.

5.4.2 Phase Noise Analysis

Although, a more accurate estimation of the output phase noise can be achieved using LTV [21] analysis based on the Impulse Sensitivity Function (ISF), such complex analysis hides the basic effects that we are trying to track. Instead, the analysis presented in this section uses the Linear Time Invariant (LTI) system approximation [41], [23] to gain more insight into the role of the new architecture, and how it improves the phase noise performance over other single tank single stage architectures. The simplified model for this analysis is shown in Fig. 5.4. It is equivalent to a general 4-stage ring oscillator with a load circuitry that is capable of providing a full and stable 90° phase shift. The noise sources from the different

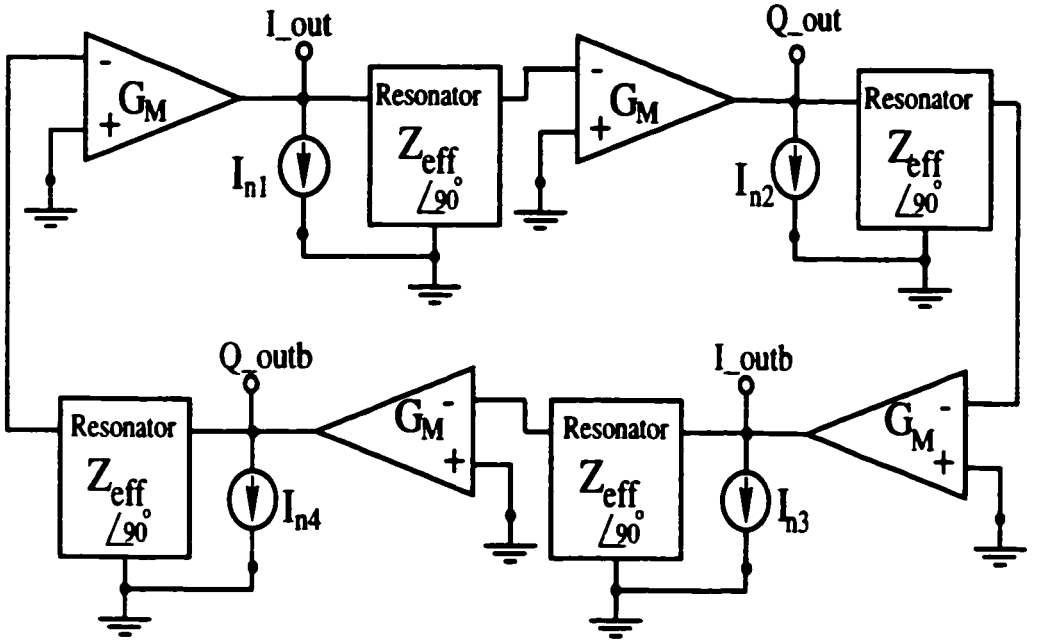


Figure 5.4: Low phase noise VCO architecture

components in each stage and its load are lumped into one noise current source (I_{n1},..., or I_{n2}) at the output of the stage. $I_{n1}, ..., I_{n4}$ are the RMS current values of these noise sources, and are calculated later. The total output noise power is equal to the sum of the noise powers at the output due to each of the noise sources. Using the linear closed loop transfer function for each noise source and applying superposition we get the RMS output noise voltage V_{o_noise1} at node "Q_outb" due to I_{n1}, as

$$V^2_{o\_noise1} = I^2_{n1} \left| \frac{Z_{in}(G_M Z_{eff})^3}{1-(G_M Z_{eff})^4} \right|^2 \tag{5.8}$$

and V_{o_noise2} due to I_{n2}, as

$$V_{o\_noise2}^2 = I_{n2}^2 |\frac{Z_{in}(G_M Z_{eff})^2}{1-(G_M Z_{eff})^4}|^2. \tag{5.9}$$

Assuming $I_{n1}^2 = ... = I_{n4}^2 = I_n^2$, the total output noise voltage V_{o_noise} becomes

$$V_{o\_noise}^2 = I_n^2 |Z_{in}|^2 \frac{1+G_M^2|Z_{eff}|^2+G_M^4|Z_{eff}|^4+G_M^6|Z_{eff}|^6}{|1-G_M^4 Z_{eff}^4|^2} \tag{5.10}$$

The oscillation frequency ω_o, as well as the minimum gain G_{Mo} required for oscillation, are calculated by equating the denominator to zero which leads to

$$G_M^4 Z_{eff}^4(\omega_o) = 1, \tag{5.11}$$

and hence,

$$\angle Z_{eff}(\omega_o) = n\pi/2 \tag{5.12}$$

where n is an arbitrary integer. The peak of $Z_{eff}(\omega)$ is close to an equivalent phase shift of 90° (Fig. 5.3) which corresponds to n=1. Thus, the oscillation frequency of Eq. 5.4 results. G_{Mo} is calculated using Eq. 5.5 as

$$G_{Mo} = 1/|Z_{eff}(\omega_o)| = \frac{1}{R_p}(\frac{1+Q^2k^2}{Qk}). \tag{5.13}$$

Secondary oscillations are prevented by choosing the coupling factor k such that kQ is always less than one. Therefore, the steady state loop gain is unity only when

the integer factor n is equal to one, and is smaller than unity for all other values of n.

In order to estimate the output phase noise, we define the closed loop noise shaping function T^2_{noise} as (V_{o_noise}/I_n). The inverse of this function H_{noise} is defined as

$$\begin{aligned} H_{noise}(\omega_o + \Delta\omega) &= \frac{I_n}{V_{o\_noise}(\omega_o+\Delta\omega)} \\ &= \frac{|1-G_M^4 Z_{eff}^4|}{|Z_{in}|\sqrt{1+G_M^2|Z_{eff}|^2+G_M^4|Z_{eff}|^4+G_M^6|Z_{eff}|^6}}. \end{aligned} \tag{5.14}$$

Then using Taylor's series we can write

$$H_{noise}(\omega_o + \Delta\omega) \approx \underbrace{H_{noise}(\omega_o)}_{=0} + \frac{dH_{noise}(\omega_o)}{d\omega}\Delta\omega, \tag{5.15}$$

and then differentiating and using Eq. 5.11

$$\frac{dH_{noise}(\omega_o)}{d\omega} = -\frac{2}{Z_{in}(\omega_o)}\left|\frac{1}{Z_{eff}(\omega)}\frac{dZ_{eff}(\omega)}{d\omega}\right|_{\omega_o}. \tag{5.16}$$

If we make use of the fact that the amplitude variation around the resonance frequency is much slower than that of the phase, the above relation can be approximated to

$$\frac{dH_{noise}(\omega_o)}{d\omega} \approx -\frac{2}{Z_{in}(\omega_o)}\frac{d\phi}{d\omega} = \frac{4Q_{eff}(\omega_o)}{\omega_o Z_{in}(\omega_o)} \tag{5.17}$$

where ϕ in this equation represents the phase of Z_{eff}. The inverse of the noise

transfer function $H_{noise}(\omega_o + \Delta\omega)$ may now be written as

$$H_{noise}(\omega_o + \Delta\omega) \approx -\frac{4}{Z_{in}(\omega_o)} Q_{eff}(\omega_o)\left(\frac{\Delta\omega}{\omega_o}\right). \tag{5.18}$$

Using Eq. 5.6 and Eq. 5.7, this transfer function can be written in terms of the single tank parameters as

$$H_{noise}(\omega_o + \Delta\omega) = -\frac{8(1+k)Q}{R_p}\left(\frac{\Delta\omega}{\omega_o}\right). \tag{5.19}$$

Assuming that the phase noise power is half of the total noise power at the output according to the narrow band phase modulation (PM) theory, he ratio of the phase noise power spectral density to the signal power at the VCO output is written as

$$\begin{aligned} S(\Delta\omega) &= \frac{1}{2}\left(\frac{V_{noise\_o}}{I_{o\_rms} Z_{in}(\omega_o)}\right)^2 \\ &= \frac{1}{2}\left[\frac{(1+Q^2k^2)I_n}{8Q(1+k)I_{o\_rms}}\left(\frac{\omega_o}{\Delta\omega}\right)\right]^2. \end{aligned} \tag{5.20}$$

The above expression relates the VCO phase noise to the lumped equivalent noise source of a single-stage I_n. In order to compare this result with the phase noise of other VCO architectures we calculate the single stage equivalent noise current source I_n in terms of the noise of a simple parallel tank. Fig 5.5 depicts the various noise sources in a single stage of our 4-stage oscillator. Both the G_M element noise $i_{n\_G_M}$ and the first tank noise $i_{n\_R_{p1}}$ are directly connected to the output node "A", and are not scaled. However, the second tank noise $i_{n\_R_{p2}}$ is scaled at node "A", by the inverse of the voltage gain from node "A" to the stage output "B". This gain

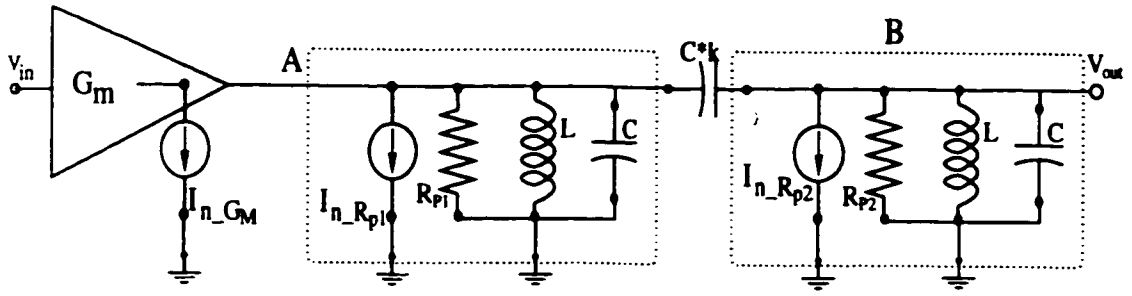


Figure 5.5: Noise sources in a single stage of the four stage dual tank VCO

is equal to the ratio between $Z_{eff}(\omega_o)$ and $Z_{in}(\omega_o)$. Using Eq. 5.5 and Eq. 5.7, the scaling factor for $i_{n\_R_{p2}}$ reduces to $1/kQ$, and I_n^2 can be written as

$$I_n^2 = i_{n\_G_M}^2 + i_{n\_R_{p1}}^2 + i_{n\_R_{p2}}^2/k^2Q^2. \tag{5.21}$$

Assuming both tanks are identical with an equivalent parallel resistance of R_p and assuming the excess noise factor of the active device to be $\mathcal{A}$ we use Eq. 5.13 to get

$$I_n^2 = \frac{4KT}{R_p}\left[1 + \frac{1}{k^2Q^2} + \mathcal{A}\frac{1+k^2Q^2}{kQ}\right] \tag{5.22}$$

where we have used the proportionality of $i_{n\_G_M}^2$ to G_M. Substituting this result into Eq. 5.20 we write the output phase noise of the VCO architecture as

$$S_{new\ arch}(\Delta\omega) = \frac{KT}{2R_pI_{o\_rms}^2}\left(\frac{\omega_o}{\Delta\omega}\right)^2\left(\frac{1+k^2Q^2}{4Q(1+k)}\right)^2\left[1 + \frac{1}{k^2Q^2} + \mathcal{A}\frac{1+k^2Q^2}{kQ}\right] \tag{5.23}$$

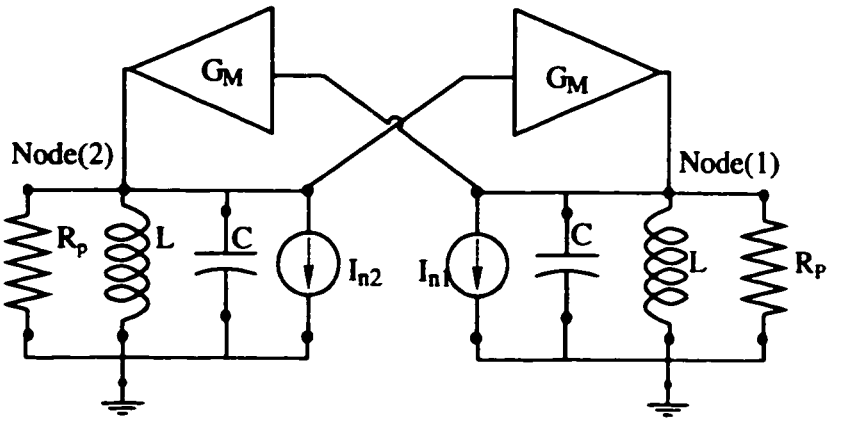
From the above expression, we see that overall phase noise reduction due to the Q enhancement improves for a smaller coupling coefficient k. On the other hand,

reducing k increases the stage noise current. In the next section, we attempt to find an optimum value for k that achieves the lowest phase noise in comparison to a conventional cross coupled pair VCO.

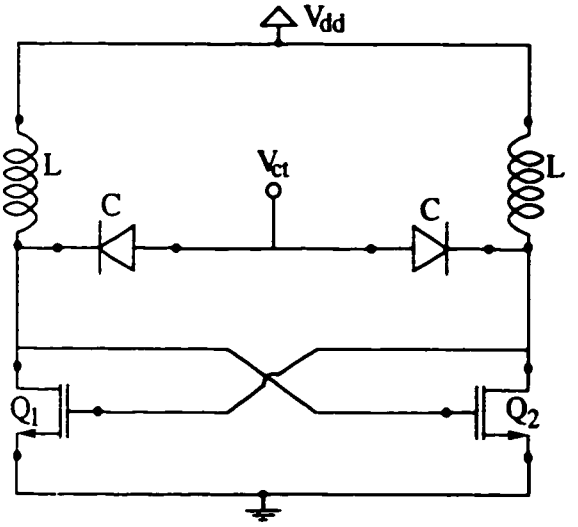
5.4.3 Comparison to Cross Coupled Pair VCOs

In order to have a fair comparison between our proposed LC ring VCO, and the conventional cross coupled pair VCO, we consider the VCO of Fig. 5.6(a). In this configuration we assume there is no coupling between the gain elements. In other words, if the active elements are NMOS's, for example, then their source nodes are connected to the ground, as shown in Fig. 5.6(b), instead of the current source shown in Fig. 5.6(c). In this case, the system is treated as a 2-stage positive feedback system and the analysis is much simpler than the differential stage of Fig. 5.6(c). The phase noise comparison is however valid for both cases. This occurs because of the following: if we compare the four stage VCO architecture of Fig. 5.4 with the differential cross coupled pair of Fig. 5.6(c) we would use a single current source for stages one and three and another for stages two and four to make the output signals fully differential as detailed in the circuit implementation. The effect of moving from a single ended to a differential architecture is the same for both designs, and the phase noise comparison does not change.

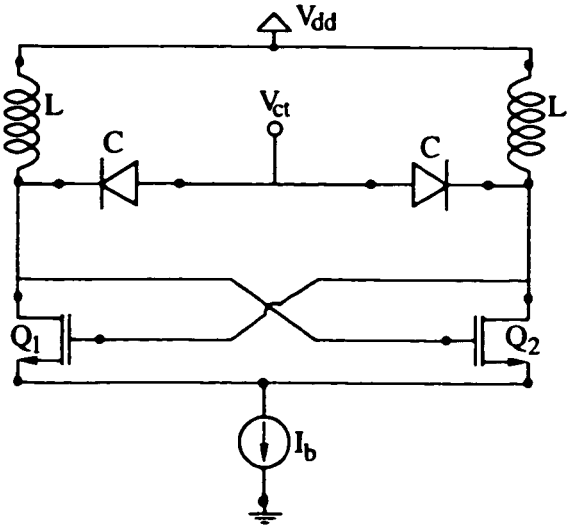
Multiplying each of the two noise sources I_{n1}^2 and I_{n2}^2 by its corresponding closed loop shaping transfer function and using superposition, we can write the total



(a) Equivalent circuit and noise sources



(b) Circuit implementation as 2-stage (no common current source)



(c) Differential implementation (common current source)

Figure 5.6: Conventional cross coupled pair VCO architecture and circuit implementation

output noise voltage at node "1" of Fig. 5.6(a) as

$$V_{o\_noise}^2 = \frac{Z_t^2 I_{n1}^2 + G_M^2 Z_t^4 I_{n2}^2}{(G_M^2 Z_t^2 - 1)^2} \tag{5.24}$$

where Z_t is the tank impedance, and (I_{n1}, I_{n2}) are the lumped equivalent noise current source for the corresponding stage. If the two stages are identical, then we can assume both current sources to be equal to I_n.

Calculating the inverse of the noise transfer function as we did in the previous section we may write

$$H_{noise}(\omega_o + \Delta\omega) = \frac{|G_M^2 Z_t^2 - 1|}{\sqrt{Z_t^2 + G_M^2 Z_t^4}}. \tag{5.25}$$

Using the Taylor expansion approximation around ω_o, H_{noise} becomes

$$H_{noise}(\omega_o + \Delta\omega) \approx \frac{dH_{noise}\omega_o}{d\omega}\Delta\omega. \tag{5.26}$$

In this case

$$\frac{dH_{noise}(\omega_o)}{d\omega}\Delta\omega = \frac{2G_M^2 Z_t^2}{Z_T\sqrt{1 + G_M^2 Z_t^2}}\frac{1}{Z_t}\frac{dZ_t}{d\omega}\Big|_{\omega_o} = 2\sqrt{2}\frac{Q}{R_p}\left(\frac{\Delta\omega}{\omega_o}\right). \tag{5.27}$$

Using this result, the output phase noise is calculated as

$$S(\Delta\omega)_{conv} = \frac{1}{2}\left[\frac{I_n}{2\sqrt{2}QI_{o\_rms}}\left(\frac{\omega_o}{\Delta\omega}\right)\right]^2. \tag{5.28}$$

Noting that I_n is the sum of the noise current due to the G_M element and the noise

current due to the tanks effective parallel resistance R_p at resonance, we write

$$I_n^2 = \frac{4KT}{R_p}(1 + \mathcal{A}) \tag{5.29}$$

and the final expression for phase noise is

$$S(\Delta\omega)_{conv} = \frac{KT}{2R_p I_{o\_rms}^2}(\frac{\omega_o}{\Delta\omega})^2(\frac{1+\mathcal{A}}{2Q^2}). \tag{5.30}$$

Comparing this result with that of Eq. 5.23, the overall noise enhancement for the new architecture is written as

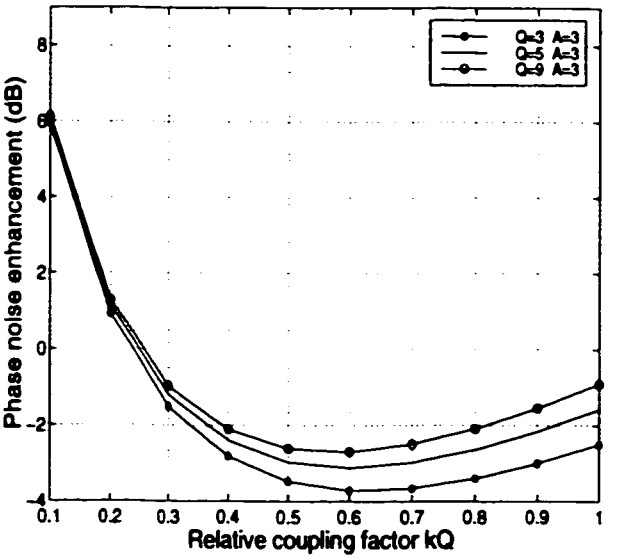
$$\frac{S_{new\ arch}}{S_{conv}} = \frac{1}{8(1+\mathcal{A})}\Big(1 + \frac{1}{k^2Q^2} + \mathcal{A}\frac{1+k^2Q^2}{kQ}\Big)(\frac{1+k^2Q^2}{1+k})^2 \tag{5.31}$$

where we assume both architectures have the same I_{o_rms}. Therefore, the total power consumption of the four stage VCO is twice that of the cross coupled pair one. Also, the excess noise factor per stage $\mathcal{A}$ is assumed to be the same for both architectures. The first term in Eq. 5.31 represents the total phase noise reduction due to the coupled tanks and the cascading of the four stages. The second term represents the excess noise penalty per stage due to the second tank and the extra gain per stage. The last term depicts the effect of the finite coupling on the effective Q-factor. The resulting phase noise enhancement ratio is plotted as a function of kQ for different values of Q and $\mathcal{A}$ in Fig. 5.7. We can see that the phase noise reduction due to the new VCO architecture ranges from two to four dB's. The reduction is more effective if the available circuit components have a limited noise performance; namely, for the lower values of Q (Fig. 5.7(a)) and the higher values

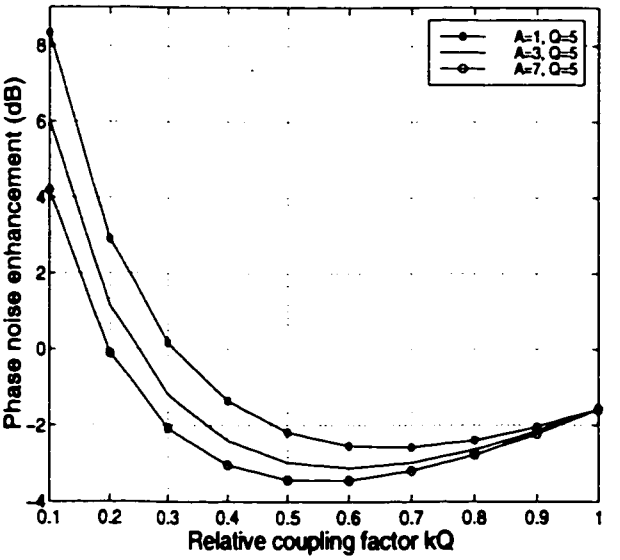
of $\mathcal{A}$ (Fig. 5.7(b)). For typical values of $Q = 5$ and $\mathcal{A} = 3$ (the solid curve on both figures), the optimum value of kQ is around 0.6 with a corresponding noise reduction of 3.1 dB. This is of course, with the added advantage of quadrature outputs inherently available in our proposed architecture.

5.5 CMOS Circuit Implementation

In this section, we closely look at the several tradeoffs involved in the implementation of the LC ring VCO using dual tank resonators proposed in the previous section. One tradeoff is the choice of fabrication technology. Usually, bipolar transistors are capable of providing a higher gain than CMOS ones are for the same bias current. Also, they are attractive for their low $1/f$ noise. In contrast, MOS transistors require a much simpler biasing circuitry, which proves to be critical in this design. Because an MOS transistor is guaranteed to operate in saturation when both the gate and drain are at the same DC level, it is easier to build identical tank circuits at both terminals, and tune them with a single control input without needing any level shifting. This property, joined by the fact that the effect of the $1/f$ noise can be significantly reduced by careful design [21], has driven our choice of the CMOS technology. Another important step in this design is the choice of a coupling element for the dual tank resonator. The type of coupling has a significant impact on the amplitude of the open loop gain, and its variation over the tuning range. Therefore, in section 5.5.1, we explain in detail the different coupling techniques to pick the most suitable one for our design goals.



(a) Constant $\mathcal{A} = 3$



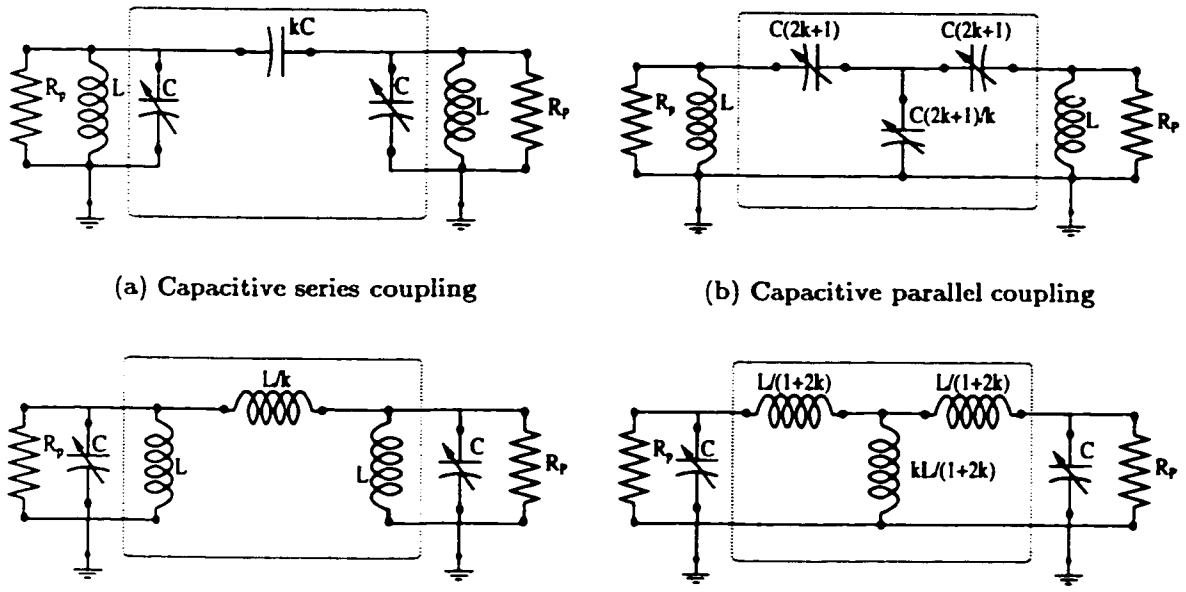
(b) Constant Q=5

Figure 5.7: VCO phase noise enhancement versus the relative coupling coefficient kQ (negative values on the noise enhancement curve means lower phase noise)

5.5.1 Coupling Techniques and Gain Control

In a 4-stage ring structure, the overall open loop gain is that of a single stage to the power of four. This means that the gain dependence on the oscillation frequency is much higher than that of a single stage oscillator. Knowing this, and assuming that the quality factor of the tanks is dominated be the inductor and the varactor series resistances, we realize that the gain is much smaller at lower frequencies. This is mainly due to the proportionality of Q (the tank quality factor) to the frequency, which leads to a smaller equivalent impedance (R_p) at lower frequencies. The bias current can be increased at the lower edge of the tuning range to compensate for this gain reduction. A careful choice of the coupling element reduces this effect. To further explain this, we consider the four possible reactive coupling structures shown in Fig. 5.8. The resistive coupling is not considered here, because it adds extra noise and it causes more signal attenuation for the same coupling coefficient than the reactive elements. We should also remember that the resistive coupling dose not provide the 90° phase shift required for the ring VCO architecture.

The series capacitive coupling configuration of Fig. 5.8(a) is the simplest. It requires only a small capacitor kC. It is not, however, the best choice because it does not provide a constant coupling factor k over the tuning range. The coupling factor k goes down for higher varactor values, and reduces the open loop gain at lower frequencies. This contradicts what we are trying to achieve from this coupling circuit. The series inductive coupling of Fig. 5.8(c) increases k, and hence the loop gain, at lower frequencies. However, this configuration is not practical in an integrated environment, because it requires a large value of inductance (L/k). The



(a) Capacitive series coupling

(b) Capacitive parallel coupling

(c) Inductive series coupling

(d) Inductive parallel coupling

Figure 5.8: Reactive coupling configurations for coupled tank resonators

parallel inductive coupling, and its equivalent magnetic (transformer) coupling can provide a constant k over the tuning range. This parallel coupling can be achieved by replacing the π network composed of the coupling inductor, and the two tank inductors by their equivalent T network (Fig. 5.8(d)). This technique requires an extra inductor in the design, and doesn't help the gain at low frequencies. The last choice is parallel capacitive coupling which can provide a constant k, if a varactor is used as the coupling element (Fig. 5.8(b)), or even increase k at lower frequencies, if a constant coupling capacitor is used. This design configuration is chosen to reduce the need for gain adjustment at low frequencies.

It is important to notice that for RF applications, the operating tuning range is very small. The wide tuning range of the VCO is only required to cover the process variations in the varactor values. This drastically reduces the impact of the open loop gain variation, because the VCO is optimized for this center frequency regardless of what the value of the control voltage is.

5.5.2 Circuit Design

Now we move on to the design of the whole stage of the ring oscillator. When a VCO is to be integrated with the whole synthesizer, a fully differential architecture is desirable to reduce the coupling of any common mode noise to the VCO outputs. In order to design a fully differential version of the proposed 4-stage ring VCO architecture of Fig. 5.4, we combine each two non-consecutive stages (stages one-three, and stages two-four) into one differential stage with a common tail current source. The resulting VCO comprises two such differential stages, each providing a 90° phase shift; proper connection of the differential stage terminals provides the remaining 180°. The resulting configuration is equivalent to that of Fig. 5.4. The phase noise relation to the differential cross coupled pair derived in the last section is the same.

The circuit implementation of the differential stage is shown in Fig. 5.9. Two CMOS (M1-M4, M2-M3) inverters are used as gain stages. The size ratio between the PMOS and the NMOS devices is optimized to achieve good symmetry for both the rising and the falling edges of the single ended voltage across the tank circuit. This reduces (or completely eliminates) the upconversion of the $1/f$ noise to the

oscillation band [21]. Two center-tapped inductors (L1-L2, L3-L4) are used for the differential tank circuits at both the drain and the gate terminals of the gain stages. Two T-networks are composed of the tank varactors (C1-C3, C2-C4) and the parallel coupling varactors (C5, C6) to tune the VCO. The cathodes of each three varactors are connected to a common node (see Fig. Fig.5.9), so that all the parasitic diode capacitances are adding to the coupling varactor, and do not limit the tuning range. This common node is connected to the control terminal via an RF blocking resistance (R4 or R5). The value of this resistance is kept small to reduce its noise contribution. It cannot, however, be too small or it may reduce the tank Q. Other small resistors (R1, R2, R3 $\approx$ 100 Ohms) are used to DC connect the virtual ground nodes of the varactors and the inductor taps, thus providing proper DC bias to the gates of the CMOS devices to guarantee their operation in the saturation region. Another benefit of such resistors is to prevent any common mode oscillations. A PMOS current source (I_{tail}) is used to provide a DC bias for the stage, because it has lower $1/f$ noise.

The tank circuits are fully integrated. Two series inductors are used to implement the center tapped inductor. Each of these inductors is a 5.3 nH spiral with 6 turns, and a total area of 200x200 μm^2. The varactors are designed as P^+-Nwell diodes. These diodes are laid out as thin parallel strips to reduce the Nwell series resistance. The tank estimated Q factor is approximately 6.0 at 2GHz.

Large size transistors are needed in this design to provide the required transconductance (G_M) per stage. This G_M is higher than that required in conventional cross coupled pair architectures. This large devices may reduce the tuning range of

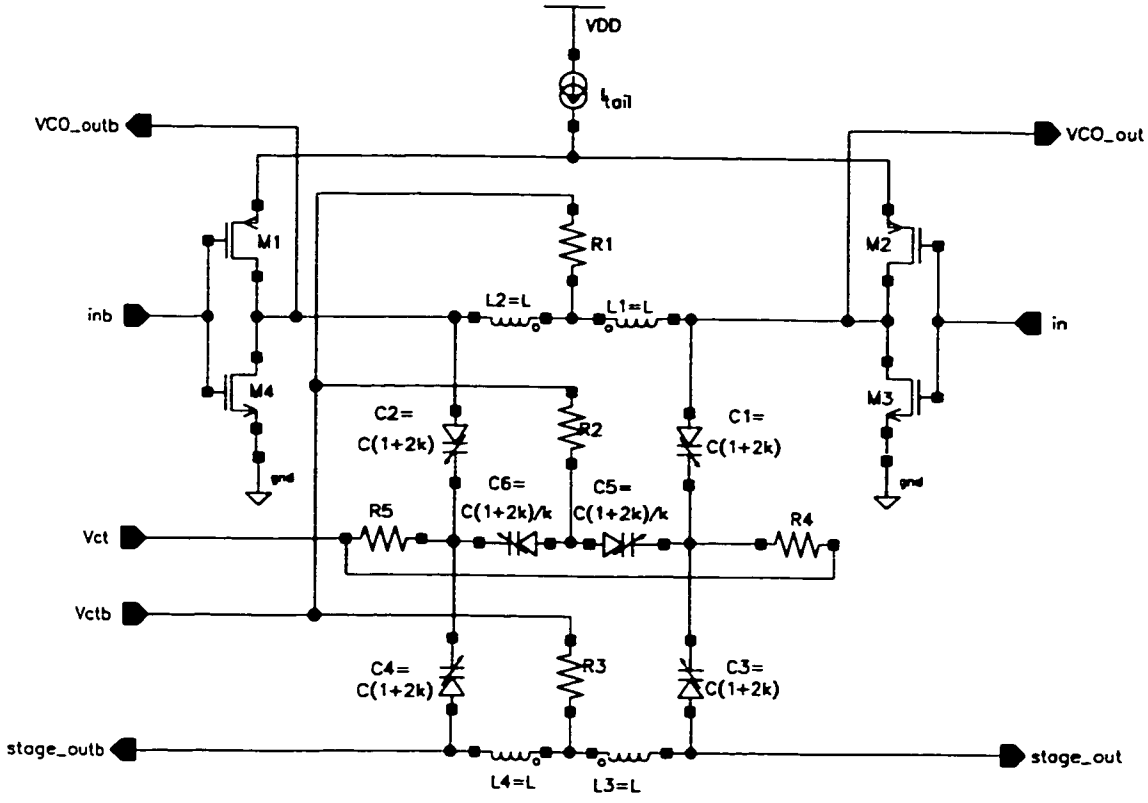


Figure 5.9: Single differential stage of the proposed VCO incorporating two non-consecutive stages of the 4-stage architecture biased with a single current source

the VCO. However, unlike the conventional cross coupled pair VCO case, the tank circuit is not loaded by the sum of both the gate and drain capacitances. Each tank is loaded by only the gate or the drain capacitance of the transistor. This reduces the tuning range degradation caused by the large size transistors. Normally, the drain capacitance is lower than that of the gate, which allows the drain to drive to VCO output buffers. The buffers input capacitance is designed to be equivalent to the difference between the drain and the gate capacitances. Thus, the center frequencies of the two coupled tanks become equal.

The output buffers are designed as open drain differential PMOS pairs that drive an off chip load of 50 Ω. One differential buffer is used for the in-phase I signals, and another for the quadrature Q signals. The VCO output signal is at a DC level equal to an NMOS V_{gs}, which easily drives the PMOS inputs of the output buffers. No decoupling capacitors are needed.

5.5.3 Cross Coupled Pair I-Q VCO

In this section we try to optimize a cross coupled pair based I-Q VCO for minimum phase noise using the same CMOS technology we used for our proposed architecture. In order to have a meaningful comparison, both circuits are designed to have an equal center frequency and power consumption, while using similar tank circuit components. Fig. 5.10 illustrates one of the two identical cross coupled pair VCOs used to build the I-Q VCO. We also use CMOS inverters (M1-M3, M2-M4) in this design as gain elements; their size ratio is chosen to minimize the upconversion of the $1/f$ noise. Less gain per stage is needed for oscillation, and too much gain may degrade the phase noise performance. In order to reduce the gain without reducing the output swing, smaller W/L ratios are used for both the NMOS and PMOS. One half of the tail current is used for the input stage, which uses only PMOS devices (M5, and M6) to avoid the high $1/f$ noise that an NMOS device may cause at this node. The resulting coupling value is enough to avoid multiple oscillations that could occur for smaller values of coupling coefficients [54], due to fabrication mismatches between the two VCOs. The differential outputs of each VCO are connected to the differential PMOS input pair of the other VCO. One

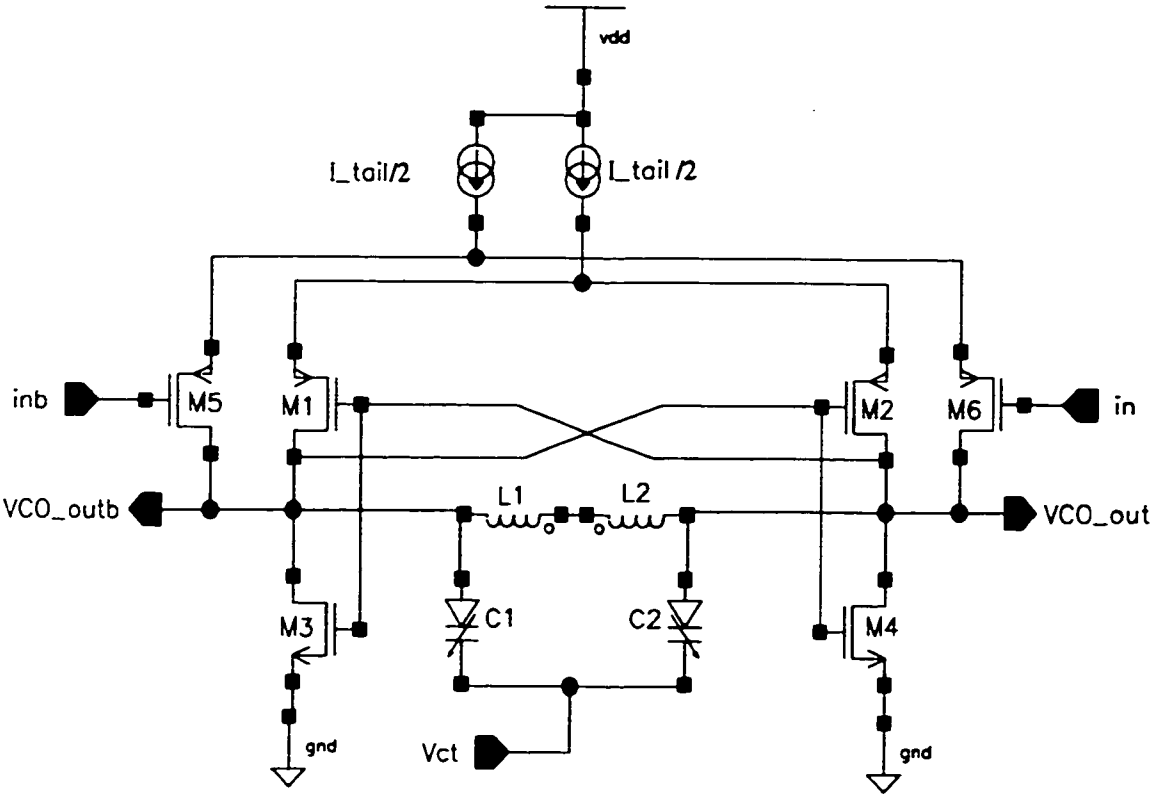


Figure 5.10: One of the two differential cross coupled pair VCOs used for generating I-Q outputs

connection is to the inverting inputs, and the other, to the non-inverting ones. This provides the opposite signs for the coupling coefficients required in Fig. 5.1.

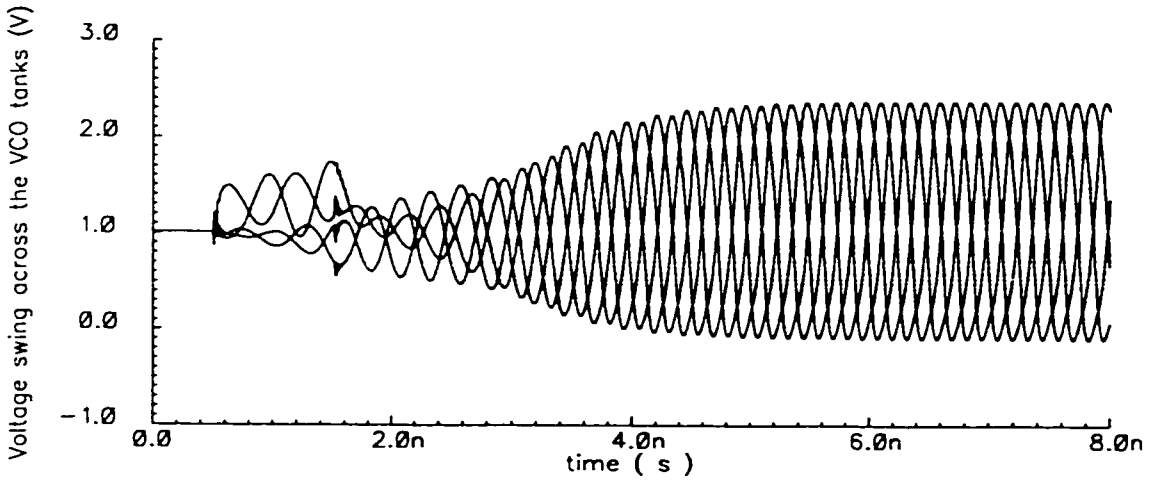
The fraction of the bias current that is used for the input stage does contribute to the current swing in the inductor. This means that the same VCO output power is maintained. However, we must keep this fraction small because it moves the oscillation frequency away from the tank circuit resonance frequency that, in turn, reduces its quality factor. The phase noise is degraded not only because of this Q reduction, but also because of the extra noise added by the input differential stages.

Although a complete phase noise analysis of this structure is beyond the scope of this work, the simulation results in the next section indicate that the phase noise degradation, due to these two effects, cancels out the 3.0 dB improvement suggested by the coupled oscillators theory [60]. The resulting phase noise is similar to that of a single cross coupled pair VCO.

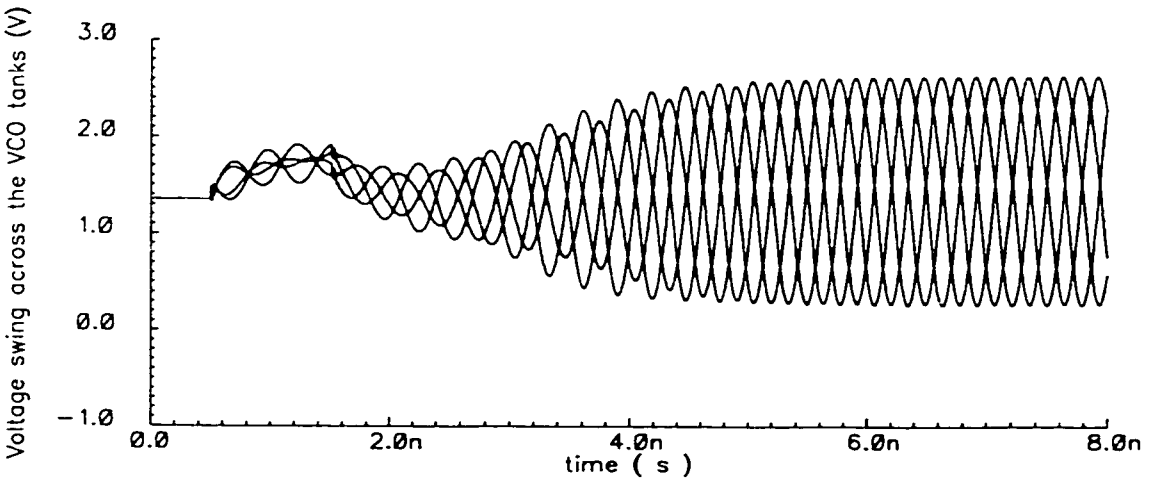
5.6 Simulation Results

Both VCOs designed in the previous section are simulated using "Spectre" transient simulation to prove their functionality. Fig. 5.11 displays the quadrature outputs of both VCOs. It is clear that the simulation start up times are similar, indicating enough open loop gain in both cases. Also, both architectures provide similar voltage swings across the tanks.

Figure 5.12 shows the simulated phase noise for both architectures. The simulated phase noise reduction due to the new architecture is around 3.5 dB at 600 KHz offset. This reduction increases for smaller offsets which means the new architecture has a better rejection of the $1/f$ noise. This is attributed to the higher effective open loop Q factor, which assures more symmetric signals. The symmetry of the voltage across the tank circuit has been proven to have a strong effect on the upconversion of low frequency noises [62]. The simulated ring VCO output frequency can be tuned from 1.642 to 1.919 GHz without much degradation in the phase noise when the control voltage is varied from 3 to 1.5 volts. Lower control voltages can further reduce the output frequency but it causes a severe increase in the phase noise due to the diodes being forward biased for part of the period. In



(a) Four stage coupled tanks ring VCO



(b) Two coupled cross coupled pair VCOs

Figure 5.11: Simulated VCO quadrature outputs monitored at the output buffer inputs for both VCO architectures

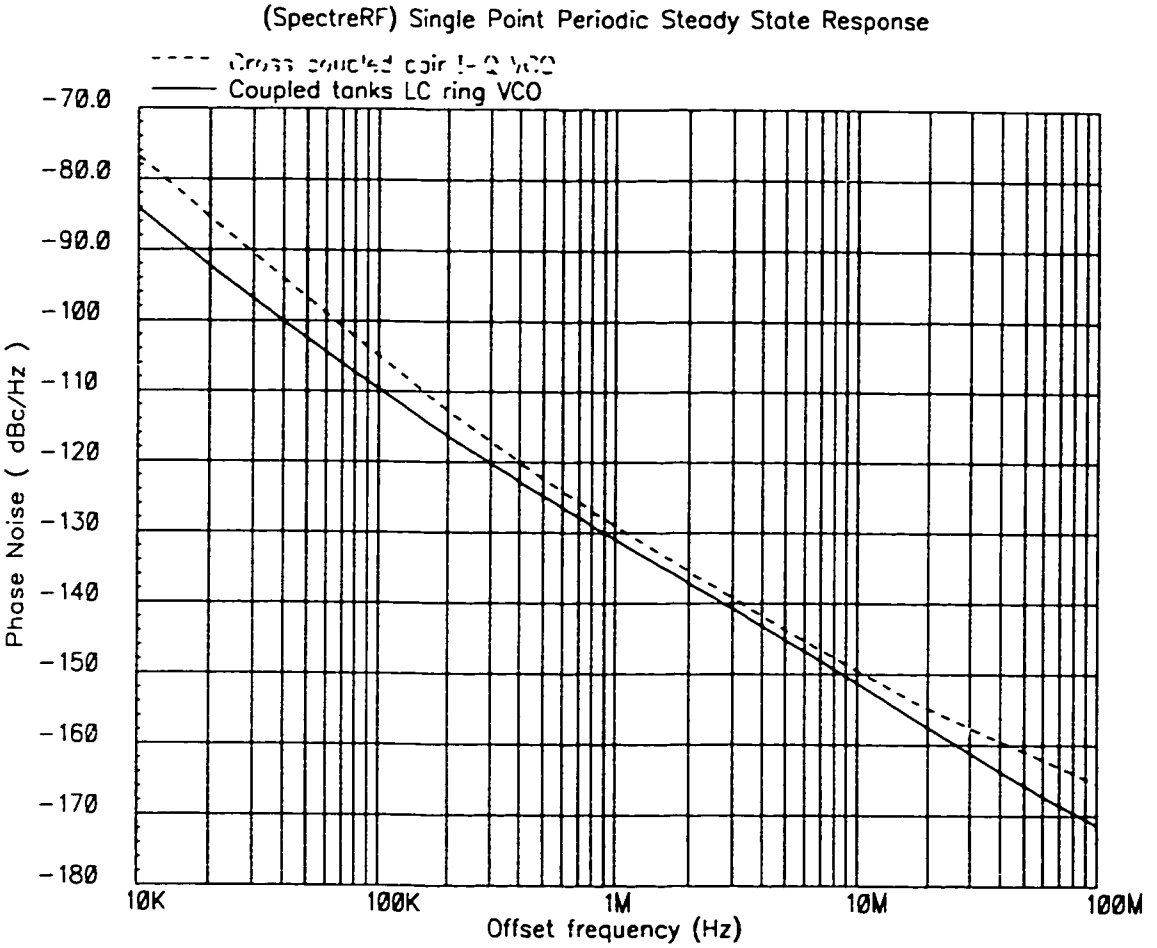


Figure 5.12: Simulated phase noise for both I-Q VCO architectures

the case of the cross coupled pair VCO, the minimum control voltage is kept higher because the NMOS devices are biased at higher $(V_{gs} - V_t)$ to reduce their gain for the same current. The anodes of the varactors are biased at the gate voltage of the NMOS and hence, the minimum cathode voltage is higher. The output frequency ranges from 1.550 to 1.734 GHz for control voltage between 3 and 1.8 volts. This suggests that the ring VCO has another advantage in the tuning range. The shift of the oscillation frequency from the tank resonance frequency, due to the coupling as discussed earlier, causes the slightly lower oscillation frequency for the coupled oscillators. Both VCOs consume 8.0 mA in the VCO core from a 3.0 V supply.

5.7 Measurement Results

A prototype of the ring VCO architecture using coupled tanks is built in a 0.35 μm CMOS technology. The measured phase noise is plotted in Fig. 5.13. The VCO meets the GSM system requirements, and achieves a phase noise of -122 dBc at 600 KHz offset from 1.93 GHz. This phase noise is almost 4 dB higher than the simulated one. This can be attributed to over estimating the inductor quality factor. Table 5.1 compares the VCO phase noise to other I-Q VCO implementations in the literature. To facilitate the comparison, the column "Normalized Phase Noise" is added, where the equivalent noise of a 1 GHz oscillator at 600 KHz offset is estimated by assuming 20 dB/decade frequency dependence. The table demonstrates that the VCO presented in this work provides a lower phase noise than most implementations. Only one design provides a 1 dB better phase noise [52], but consumes almost twice as much current. The comparison is based on

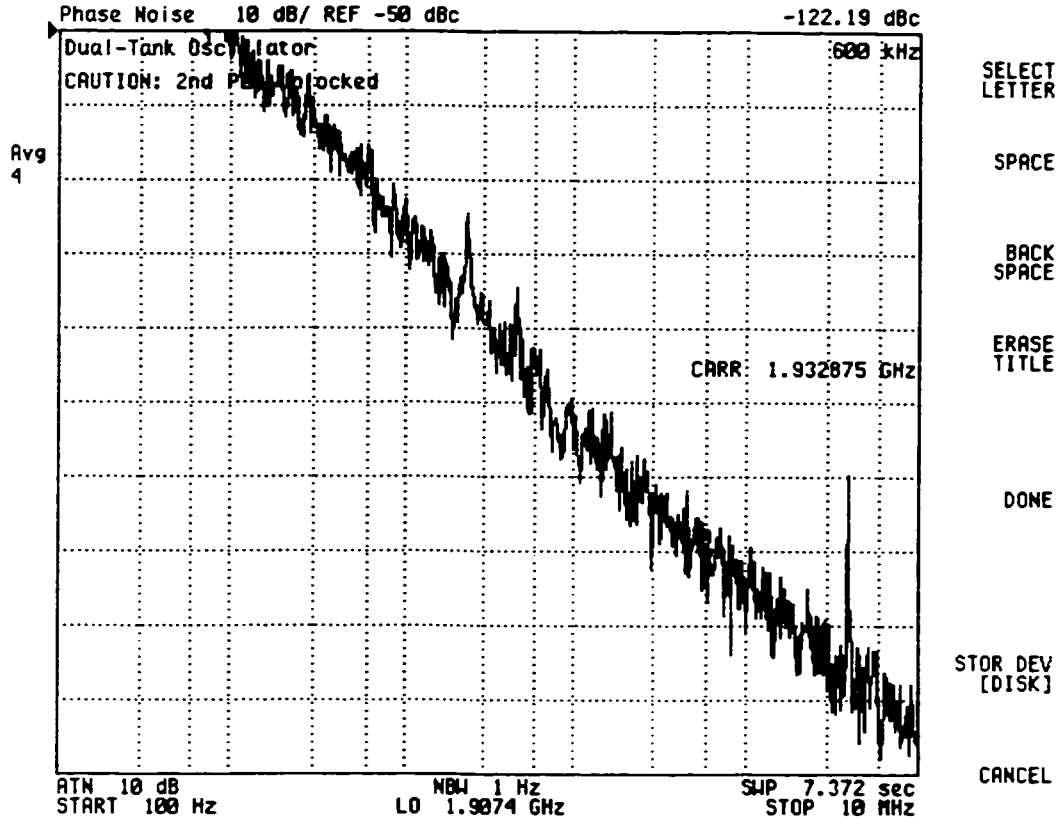


Figure 5.13: Measured phase noise of the coupled tank based ring I-Q VCO

Ref., Year	f_o (Hz)	Δf (Hz)	Phase Noise (dBc/Hz)	Normalized Phase-Noise (dBc/Hz) f_o=1GHz Δf=600KHz	Current (mA)	Supply (V)
[63], 95	1G	100k	-87	-101	~16.5mA	5 V
[8], 96	900M	100k	-85	-70.3	10mA	3 V
[46], 97	1.8G	500k	-100	-103.5	4.6 mA	3.3 V
[52], 98	1.9G	600k	-123	-128.6	16mA	2.7 V
[54], 99	6.53G	1M	-98.4	-110.3	12mA	1.5 V
[53], 99	2.6G	5M	-110	-99.9	10.4mA	2.5 V
This work	1.93G	600k	-122.2	-127.9	9.2mA	3 V

Table 5.1: Comparison of the coupled tank based LC Ring VCO with state-of-the-art I-Q oscillators

the current consumption rather than the power because the current value directly impact the VCO output swing and the overall phase noise. The supply voltage, on the other hand, does not have significant effect on the phase noise.

Because of the strong dependence of the VCO open loop gain on the inductor Q in this architecture, the reduction in the implemented inductor Q is compensated by extra drive current to increase the gain. The VCO prototype draws 9.2 mA from a 3 V supply, and occupies a chip area of 1.1x1.1 mm^2. The die photograph is shown in Fig. 5.14. The VCO tuning range was also limited because the oscillation died out, due to insufficient gain, for control voltages below 2.5 V. When the control voltage is changed from 2.5 to 3.5 V, the tuning range is 107 MHz.

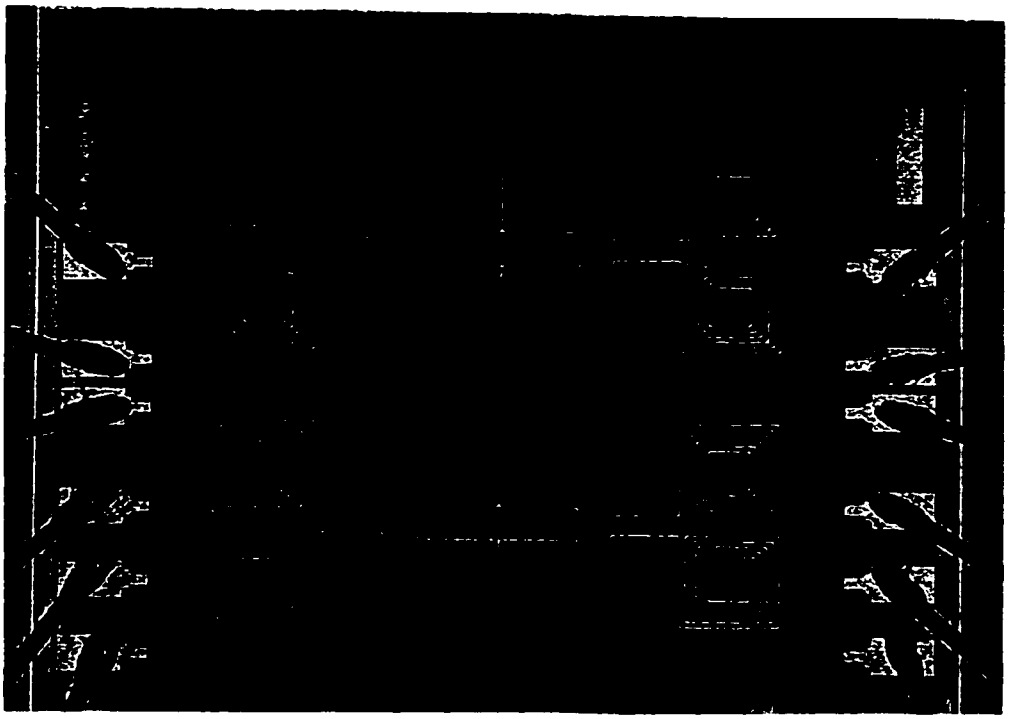


Figure 5.14: CMOS LC ring VCO die photograph

5.8 Conclusion

A novel VCO architecture is presented to improve the phase noise of integrated VCOs. This design utilizes two coupled tanks to implement a transimpedance resonator. Its effective Q factor is close to twice that of a single low Q integrated resonator. This increase in the frequency selectivity leads to a significant reduction in the VCO phase noise. Another attractive feature of this transimpedance resonator is that it has a 90° phase shift between its input current and output voltage. Such a feature is used to further reduce the phase noise by cascading four resonators in a ring VCO structure. This ring VCO architecture inherently provides

accurate quadrature outputs, which are conventionally generated by cross coupling two identical oscillators. In essence, this VCO utilizes the extra power and area that are normally needed for quadrature output generation to significantly reduce the phase noise.

Full phase noise analysis of the VCO is presented and compared to that of the conventional cross coupled pair VCOs. The VCO power consumption is similar to that of other I-Q VCO implementations in literature, with an estimated phase noise reduction of 4 dB. A prototype of the VCO was built in a 0.35 μm CMOS technology. The measured phase noise is -122 dBc at 600 KHz offset from 1.93 GHz. This phase noise is significantly lower than other I-Q VCO implementations in the literature, and is comparable to those with a single phase output. The VCO prototype draws 9.2 mA from a 3 V supply, and occupies a chip area of 1.1x1.1 mm^2. This VCO prototype is designed with a single ended control to reduce complexity, but it can be easily configured into the differential architecture outlined in chapter 4.

Chapter 6

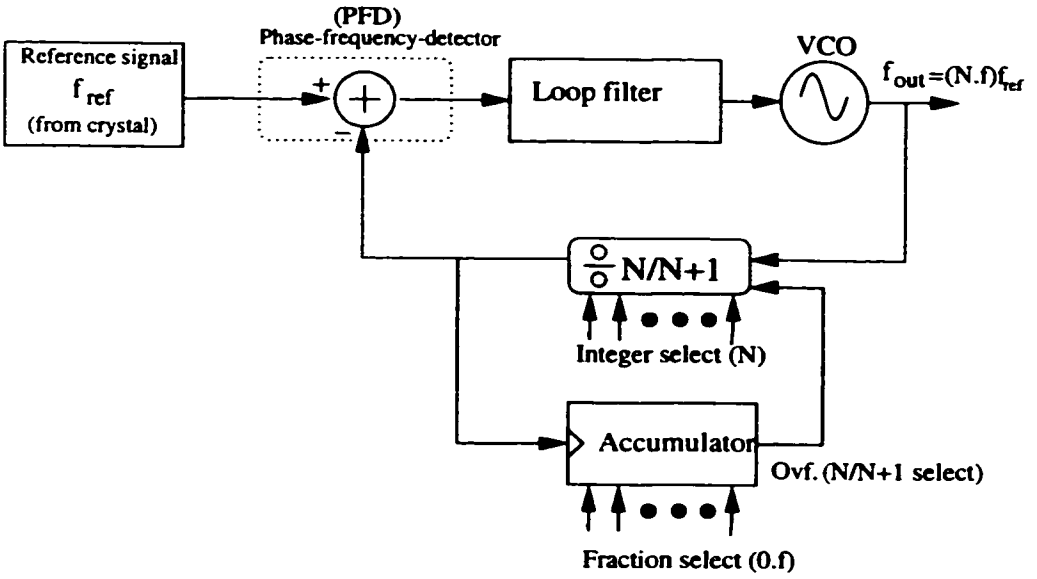
Spur Compensated Fractional-N Frequency Synthesizer

6.1 Introduction

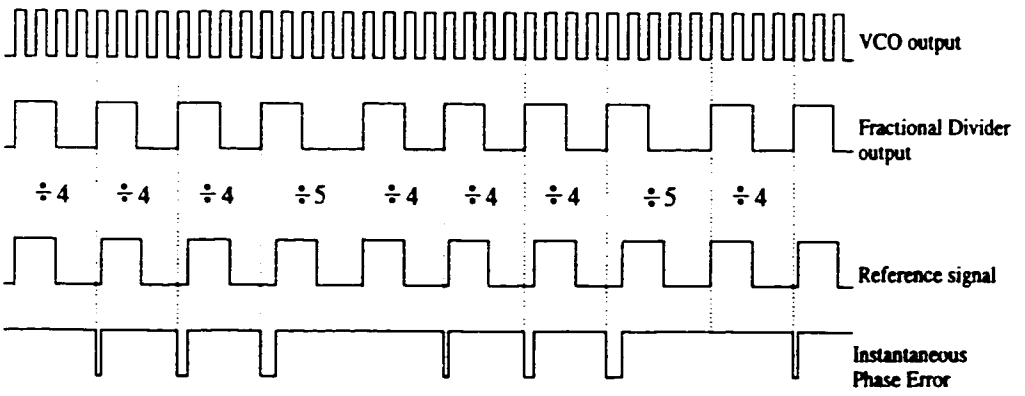
The increasing demand for faster switching synthesizers for wireless applications, along with their high spectral purity requirement, pushes the performance limits for the integer division PLL's, which have dominated the frequency synthesis market so far. In an integer-N PLL, the input reference frequency is divided down, before it is fed to phase detector, such that the phase comparison frequency is equal to the required channel spacing of the output frequency. When this channel spacing is much smaller than the output frequency, a large PLL division ratio N is required, which limits the attainable switching speed as well as the spectral purity of the output. Usually, the loop speed is limited by the maximum allowable spur level at the output. The spurs are produced at the Phase Frequency Detector (PFD)

comparison frequency, as a result of the mismatch between the UP and DOWN currents in the charge pump based PLL. Another important cause of the reference spurs is the leakage current of the VCO control input. The leakage current causes the control voltage to constantly drift from its steady state value, and gets corrected by the loop every cycle. As a result, the control voltage has a periodic component at the reference frequency causing a spur at the output. In order to reduce those reference spurs, the loop bandwidth (BW) is kept at a much lower value than the reference frequency (at least an order of magnitude). The narrow loop BW sets an upper limit for the switching speed of the frequency synthesizer (FS). The large value of N has also a detrimental effect on the spectral purity of the output. Within the loop BW of the PLL, the effect of the reference jitter, as well as that of the PFD and the charge pump, are multiplied up by a factor of N^2 when referred to the VCO output.

In summary, fractional dividers are desirable for two reasons. The first is to reduce the value of the required division ratio N, thus reducing the in-band noise of the synthesizer. The second reason, which is also a consequence of the first one, is to increase the input reference frequency beyond the required channel spacing. In most cases, the fractional division is achieved using a dual/multi modulus integer divider which switches the division ratio between N and N+1 (in the case of a dual modulus divider) with an effective fractional division ratio N+f. The value of the fraction f is determined by the ratio of the number of times we divide by N to those we divide by N+1. Fig. 6.1(a) describes this architecture. An accumulator is used to produce the fractional control signal. The fraction value f is equal to the ratio



(a) Architecture



(b) Waveforms for N=4 and f=1/4

Figure 6.1: Conventional fractional-N Frequency Synthesizer using a simple accumulator based fraction control

of the accumulator input to 2^n, where n is the number of bits of the accumulator register. The divider is controlled by the carry overflow of the accumulator which selects the N+1 division ratio. Otherwise, the divider divides by N. Fig. 6.1(b) is an example of the fractional synthesizer waveforms for the simple case of N=4 and f=1/4. By looking at the reference signal, we see that the effective division ratio is (4+1/4). It is also clear that, even though the loop is locked, there is a phase error signal at the output of the phase detector. In addition to having higher energy at the reference frequency, this signal has a frequency component at a lower frequency, which causes what we call a "*fractional spur*" at the output. The fractional spur is located at an offset from the carrier equivalent to the channel spacing. Because the reference frequency is now much higher than the channel spacing, it is relatively easy to suppress its spurs by the loop filter of the PLL. However, this is not the case for the fractional spurs at the channel spacing frequency. To take full advantage of the fractional-N synthesis, some way is required to compensate (or suppress) these spurs without reducing the loop BW.

In the next section, we review the existing fractional spur compensation techniques, and discuss the practical issues in their implementation. Then, we present the proposed spur compensation architecture. This technique uses digitally controlled delays to shift the divider output such that no phase error occurs at the PFD output. The rest of the chapter describes the full circuit implementation of this technique. Both system level and circuit level simulations are then presented.

6.2 Overview of Fractional Spur Compensation Techniques

6.2.1 Charge Injection Analog Compensation

Traditionally, the fractional spur compensation techniques have made use of the phase information in the accumulator, which is converted to a analog signal and subtracted from the phase error output of the PFD. In a charge pump based system, a charge equivalent and opposite to the phase error, is injected into the loop filter parallel to the main charge pump output. Many commercial fractional-N synthesizers employ this technique [64, 65, 66, 67]. It is sometimes called "*analog compensation*".

When no compensation is used, the charge pump output is a pulse width modulated signal, similar to the phase error plot of Fig. 6.1(b). The compensation pulses require the same charge (area) as that of the unwanted charge pump pulses with the opposite polarity. The injected charge pulses have a fixed width, and their height is varied such that the net charge injected to the loop in each cycle is zero. Fig. 6.2 demonstrates an example of both the charge pump current and its required compensation current. Usually, the charge pump error pulses are very short in time (few tens of picoseconds). This makes it hard to generate compensation pulses with a high accuracy and a comparable duration. In order to maintain the high timing accuracy of the compensation pulses, they are often derived from the undivided reference input of the PLL [66], which has a period around 50 ns. This large difference in pulse durations requires the compensation current to be very small compared to

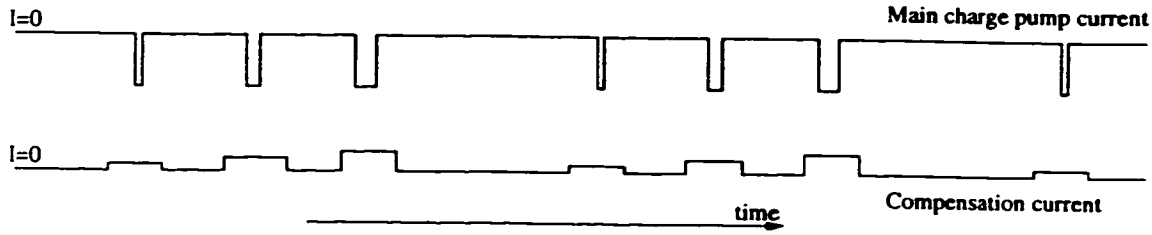


Figure 6.2: Charge injection analog compensation of fractional spurs

the main charge pump current. For example, a few μA current is required to be added to a 1.0 mA charge pump. The fractional spur compensation, in this case, is limited by the analog matching accuracy of the compensation currents. Another limitation of this technique is that it doesn't completely cancel the spurs even with perfect current matching. That is because, the error pulse width depends on the output frequency, whereas the compensation pulse width is constant. This limits the full cancelation to only one channel frequency. At other channel frequencies, a systematic error exists and the spur cancelation is limited. The other disadvantage of the charge (or area) cancelation technique is related to the pulse positions. In order to achieve full cancelation, the error pulse should be exactly at the center of the compensation pulse, which is not easy to achieve practically.

6.2.2 $\Sigma - \Delta$ Fractional Synthesis

$\Sigma - \Delta$ modulators can be used to randomize the fractional switching and convert the fractional spurs into a high frequency quantization noise that could be easily filtered by the loop filter. The main advantage over the analog compensation technique is that no analog circuits are involved. Being an all digital solution, the $\Sigma - \Delta$ delta technique allows very fine channel resolutions. For a 1.1 GHz synthesizer, a

resolution of 1 Hz has been reported [68].

The main limitation for $\Sigma - \Delta$ fractional synthesizers is that higher order modulators are needed to properly suppress the spurs, and convert them to a high frequency noise. Although such high order modulators provide very low quantization noise at low frequencies, their noise rises much faster at higher frequencies. A relatively small loop BW is required to attenuate this noise. Another difficulty with moving to higher order multi-bit $\Sigma - \Delta$ modulators is that a multi-modulus prescalar is used [69]. This results in larger excursions of the instantaneous division value N with the result of a higher quantization noise.

6.3 Digitally Controlled Delay Spur Compensation

In this chapter we investigate a less popular analog compensation technique that may be used in conjunction with a multi-bit $\Sigma - \Delta$ modulator to reduce the division ratio excursions. This can be accomplished by using the $\Sigma - \Delta$ modulator outputs, as the fraction inputs to an analog compensated fractional-N synthesizer, in order to perform what is called "*sub-fractional*" division [70]. In addition, the analog compensated synthesizer can be used as a stand alone if a fine channel spacing is not required. In the analog fractional compensation technique presented here, the phase error is compensated for by introducing a digitally controlled delay after the output of the divider to shift its rising and/or falling edges to coincide with those of the reference, and to avoid the occurrence of the phase error pulses at

the PFD output. This technique has been recently proposed [71], but no circuit implementation has been demonstrated. In this chapter we study the feasibility of the circuit implementation of this technique, and its advantage/disadvantage over the traditional charge injection analog technique.

6.3.1 Synthesizer Architecture

In order to understand the idea of the controlled delay spur compensation technique [72, 71] we consider the uncompensated fractional-N synthesizer phase error waveform of Fig. 6.1(b). The timing error between the divider output and the reference signal assumes the values $T_{vco}/4$, $2T_{vco}/4$, $3T_{vco}/4$ and then returns back to zero when the division ratio is switched to N+1. This result can be generalized for any fractional input (f) as

$$\Delta t = ACC[\frac{T_{vco}}{2^n}] \tag{6.1}$$

where ACC is the accumulator content during the cycle, and 2^n is the modulo of the fractional divider with n representing the size of the accumulator. In order to compensate for this timing error, we insert a controlled delay equal to the timing error after the divider; then we compare the delayed divider output with the reference signal in the PFD, instead of comparing it to the divider output itself. Consequently, the PFD won't sense the timing error, and the fractional spurs could be, theoretically, completely removed. In practice, the spur reduction is limited by the accuracy of the delay elements. In order to appreciate the challenge in implementing these delays, we should note that $2^n - 1$ delays are needed with an

absolute delay equal to $T_{VCO}/2^n$. For a typical VCO frequency of 2 GHz and n=3, the required delay value is 62.5 ps, which pushes the limits of today's technology.

We should also note that the required delay value is a function of the FS output frequency, which can be achieved using a Delay Locked Loop (DLL). The FS architecture including the DLL based phase compensation circuit is shown in Fig. 6.3. The VCO output drives a triple modulus prescalar. The prescalar has two modulus control inputs. If both controls are zero, it divides by Nps (32 in the figure). If only one of the control signals is active, the division ratio becomes Nps+1. When both lines are active, the division ration is Nps+2. This architecture of the prescalar is important to allow both the integer division ratio (using N and A counters[68]), and the fractional division ratio (using the carry overflow of the accumulator) to be controlled independently according to the N and f inputs of the synthesizer, respectively. The prescalar output is fed to the rest of the integer divider whose output is then passed through a cascade of eight delay cells. The outputs from these delays are multiplexed according to the fractional accumulator contents as shown in the figure, to select the input to the main PLL PFD. The accumulator is clocked by a delayed version of that PFD input. This delay is important to avoid switching the delays around the rising edge of the signal where the phase comparison occurs. The other input to the PFD is the reference signal. Its frequency is selected to be 1.6 MHz. This allows a channel spacing equal to 200 KHZ for the modulo eight fractionality used here. The PFD output drives the main charge pump whose output is filtered by H(s), and fed to the VCO control to close the loop for the main synthesizer PLL.

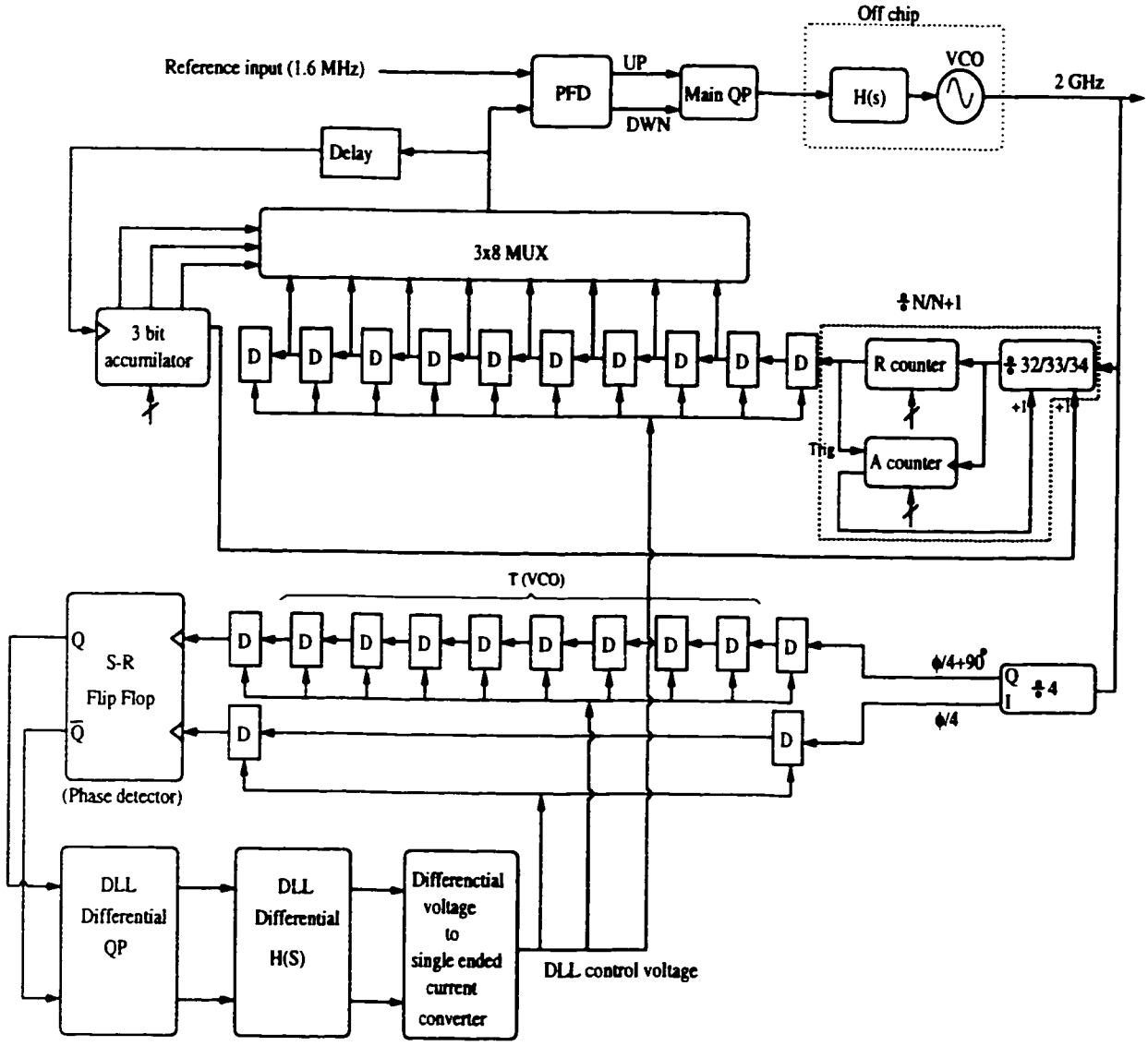


Figure 6.3: Complete architecture of the fractional-N frequency synthesizer with a DLL based fractional spur compensation

In order to guarantee that the compensation delays are precisely one eighth of the VCO period, voltage controlled delays are used instead of fixed ones. The control voltage of these delays is shared with identical ones, which are locked to the required $T_{VCO}/8$ value using a DLL. When designing the DLL, we don't require a phase frequency detector (PFD), because the two input signal have the same frequency. Phase-only detectors (PD's) such as XOR, S-R Flip Flop, or J-K Flip Flop are sufficient. These are simpler to implement at higher comparison frequencies. One way to generate the required delay value is to compare the phase of the VCO output to its version that is delayed through a cascade of controlled delays. If the number of delays is eight and the phase difference between the two signals in the comparison is zero then each delay becomes $T_{VCO}/8$.

The number of delays could be reduced if a different type of PD is used. In the case of XOR PD, the zero phase error output corresponds to a phase difference of 90° between the input signals. Therefore, only two delay elements are required in the DLL. The same kind of reduction could be achieved if quadrature VCO outputs are used. Other types of phase detectors such as S-R and J-K Flip Flops, which has a zero phase error at 180° phase shift between the inputs, can be used with the VCO quadrature outputs to provide the same reduction in the number of stages.

Because of the very high frequency of the VCO output, the implementation of the DLL PD and charge pump is challenging. Therefore, the VCO signal is divided by four first, and the I & Q outputs of the divider are used drive the DLL at one fourth the VCO frequency at the expense of increasing the number of required delay cells. If an S-R Flip Flop PD is used, eight delay cells are needed to delay the Q

output of the divide-by-4 output, by 90°. This corresponds to one VCO period when the phase shift between the PD inputs is 180°.

6.4 Synthesizer Circuit Design

In this section, the full circuit implementation of the synthesizer architecture of Fig. 6.3 is presented. The design specifications are based on the frequency bands indicated in the figure. The whole synthesizer, except for the VCO and the main PLL filter, is integrated on a single chip. The VCO center frequency is 2.0 GHz, and the divided reference frequency is 1.6 MHz. With modulo eight fractionality, the channel spacing is 200 KHZ. The VCO output is divided by four so that the DLL runs at 500 MHz comparison frequency. One advantage of the delay based compensation architecture used here is that the compensated divider output is very similar to that of an integer-N divider. This means that the main loop components are the same as those of conventional PLL's. Only the delay compensation circuit need to be designed, to convert an integer-N design to a fractional-N one. Other than a minor change in the prescalar design to add an extra modulus control, the whole PLL design remains the same. The design of an integer-N PLL has been covered in detail in chapter 4, and now we wish to concentrate on the compensation DLL design.

6.4.1 Voltage Controlled Delay Cell

At the heart of the digital controlled delay spur compensation architecture is the delay cell itself. It is designed to provide the required mean delay value of 62.5 ps

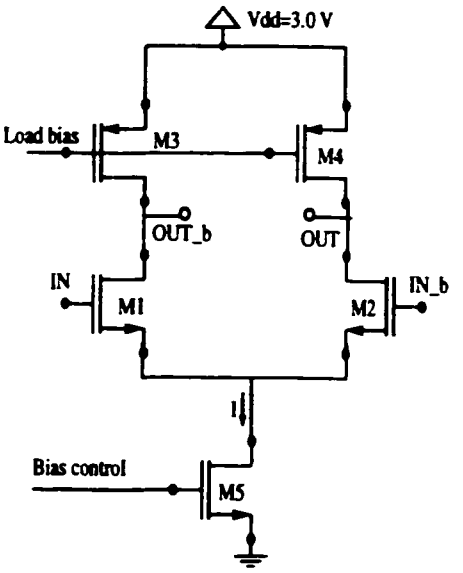


Figure 6.4: Basic CML delay cell of the DLL

with a tuning range that sufficiently covers both process and temperature variations, and the tuning range of the output frequency.

The delay cell is implemented as a differential CML stage (see Fig. 6.4). The switching transistors M1, M2 have minimum length to reduce the delay. Their width is chosen to guarantee full switching with 0.5 V swing at the inputs. Large bias current of 100 μA is used to minimize the charging time at the output and allow shorter delay. The bias current source is designed with a large area to improve the bias current matching among the different delay cells, and hence, the delay matching. Active loads with controlled replica bias are used to maintain the output swing at 0.5 V for different values of the bias current.

6.4.2 Differential Phase Detector at 500 MHz Comparison Frequency

One of the critical blocks in the design of a 500 MHz DLL is the design of the phase detector. At such high comparison frequency, conventional CMOS phase frequency detectors are not suitable. A better suited logic style would be CML. In addition to its high speed capability, CML is useful here to maintain the fully differential signal path for the DLL. Because the two signals to be compared are driven from the same source, their frequencies are the same at all times. Thus, a simple phase detector (with no frequency discrimination capability) is used.

Although, the XOR gate is the simplest phase detector, it is not desirable here because of the output dependence on the input signal duty cycle. Another difficulty with the XOR is that its output runs at twice the comparison frequency, which increases the power consumption. The edge triggered J-K Flip Flop is insensitive to the duty cycle, and its output is at the same frequency as the input signal. However, the design of this type of Flip Flop is not easy in high frequency CML. Therefore, the S-R Flip Flop is chosen for the phase detector design.

The S-R Flip Flop has similar characteristics to the J-K Flip Flop, with a simpler implementation in CML. The only limitation of this type of phase detector is its undefined state when both inputs are one. This is not a problem here because we know that when the loop is in lock, the two inputs are out of phase. Moreover the two inputs have a duty cycle close to 50%. This means that if the propagation delay is large enough, the one-one condition will not occur. Then the detector will properly detect a zero phase error, when the positive edges of the inputs are at a

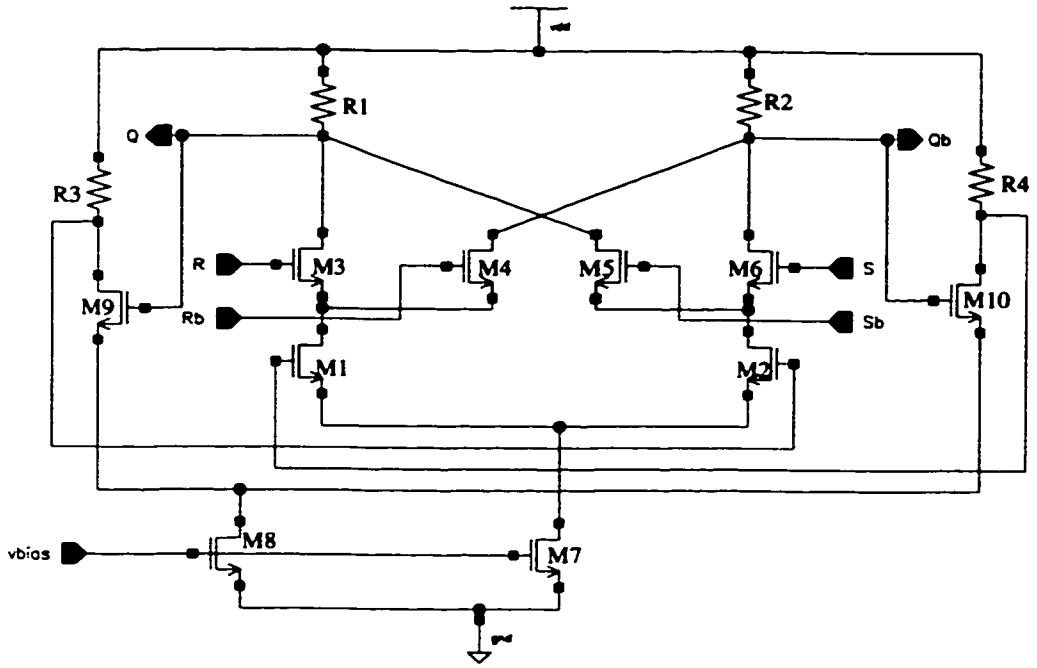


Figure 6.5: CML S-R Flip Flop used as a differential phase detector at 500 MHz comparison frequency

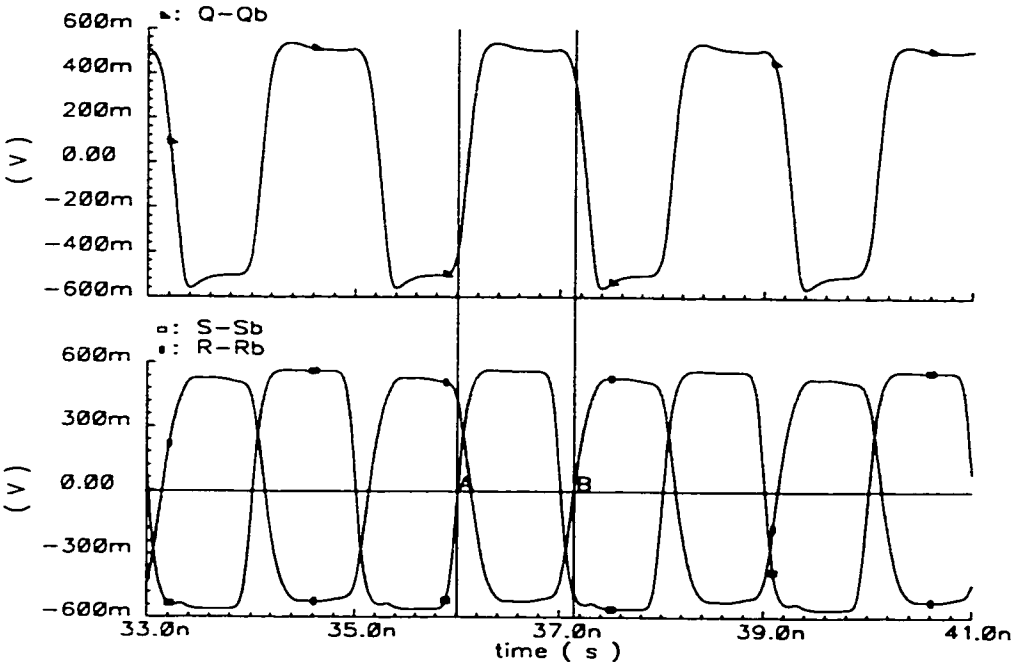


Figure 6.6: CML S-R Flip Flop differential output when phase shift between inputs is not 180°

180° phase shift. Because of the differential nature of the CML, it is possible to determine a zero differential output corresponding to the zero phase error without any need for a dual supply or an intermediate voltage reference.

The CML circuit for the S-R flip flop is shown in Fig. 6.5. The differential pair M1-M2 allows S-Sb to control the outputs Q-Qb when Q is low. When Q is high, the outputs are controlled by R-Rb. The outputs Q-Qb are delayed through the CML inverter M9-M10 before they are fed back to M1-M2. This delay is necessary to avoid the one-one overlap of S and R. Fig 6.6 shows the transit simulation of the differential S-R flip flop output (Q-Qb), when the inputs S and R are not at the 180° phase shift. The markers A and B in the figure indicate the points in time

when the positive edges of the differential inputs S and R cross zero. The output (Q-Qb) begins to change slightly before this crossing. The phase detector consumes 320 μA, out of which 80 μA is used for the delay inverter. This large current is needed to sufficiently drive the differential charge pump inputs.

6.4.3 DLL Differential Charge Pump

Even though the phase detector output is not tri-stated, a charge pump is used to facilitate the implementation of a pure integrator in the loop filter. Fig. 6.7 illustrates the differential charge pump design. The source follower buffers M1 and M2 are used as DC level shifters to shift the CML inputs to the middle of the supply. The shifted input is capable of driving both the up and down differential pair switches M5-8 and M9-12. Usually, when such differential switches are used for fast switching, the current is either selected to drive the loop filter, or it is dumped to either ground or Vdd, depending on its direction. In our case, instead of dumping the current, we use it with a simple filter R1-R2 and C1-C2 to detect the output common mode. This common mode is compared to a reference voltage using an OpAmp whose output controls the current sources M3 and M4. Because of the complementary nature of the phase detector outputs, the input switches are connected together so that only one signal A (and its complement Ab) is used to turn the UP or DWN current to the loop filter. The third state when both are off is not allowed here because of the PD nature. A large charge pump current of 200 μA is used to lower its noise contribution. The total current consumption is 650 μA: 200 μA for each current branch, 100 μA for each of the input buffers and 50

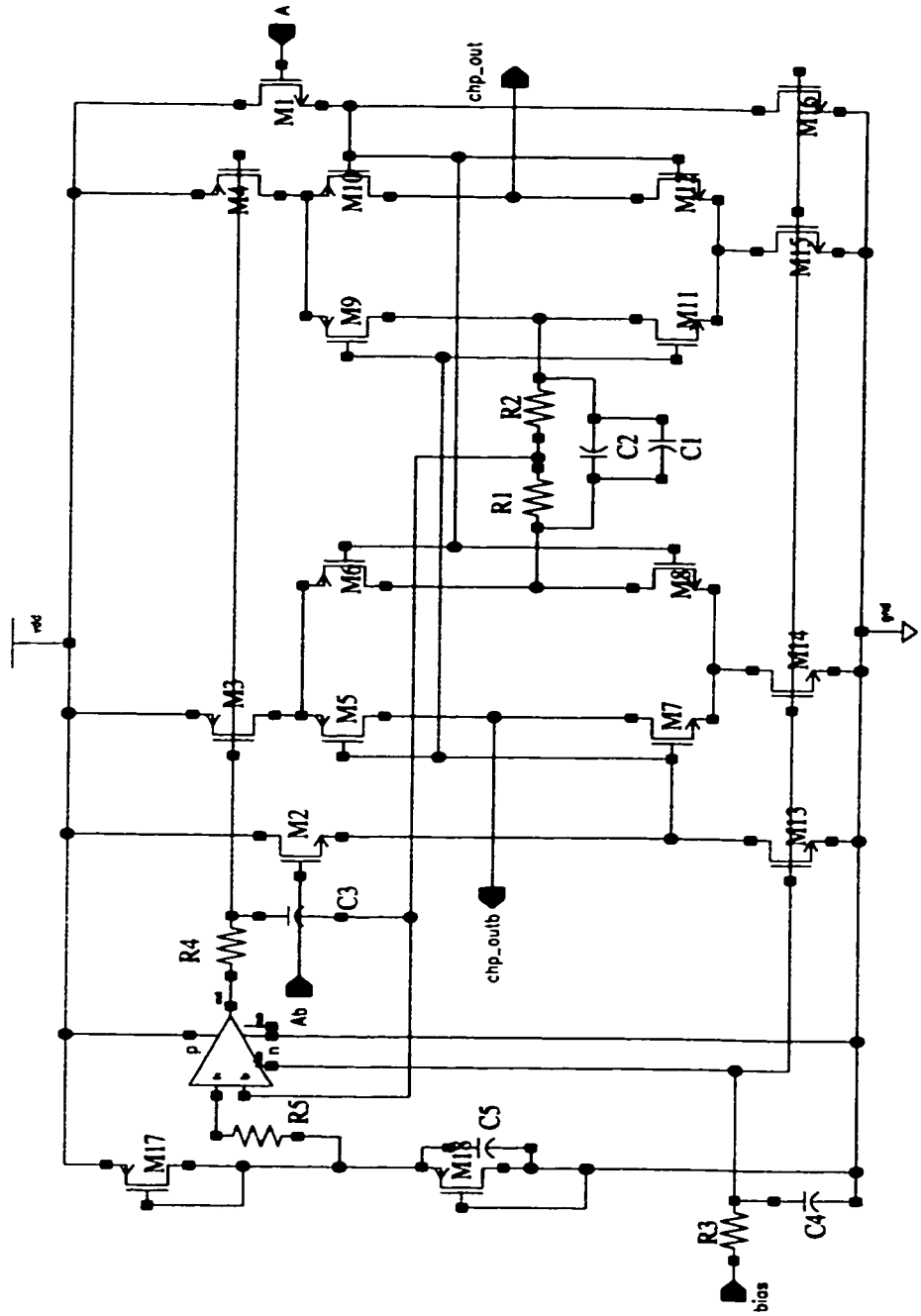


Figure 6.7: 500 MHz CML-input differential charge pump with common mode control

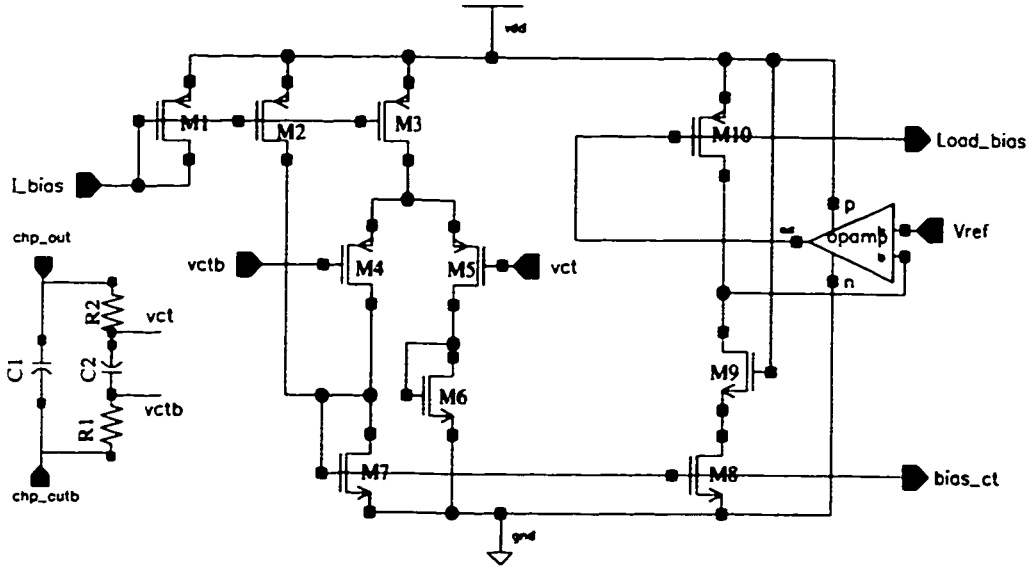


Figure 6.8: Differential to single ended control voltage converter with replica bias cell to drive the DLL delay cells

μA for the common mode compensation.

6.4.4 DLL Loop Filter and Delay Cell Control

Because the DLL doesn't have the integrating effect of the VCO, a pure integrator can be used in the loop filter with no need for the lead-lag compensation normally needed for PLL's. A single on-chip shunt capacitor (C1) is used to integrate the charge pump current. Another R-C smoothing stage (R1, C2, R2) is added before feeding the output to voltage-to-current converter that controls the delay cells, as shown in Fig. 6.8. The current in the diode connected transistor M7 is mirrored to the replica bias current source M8, as well as all the delay cell current sources. The total current flowing in M7 is the sum of the the current of M2, and the portion of M3 current that is directed to M7 through the differential pair M4-M5. The ratio

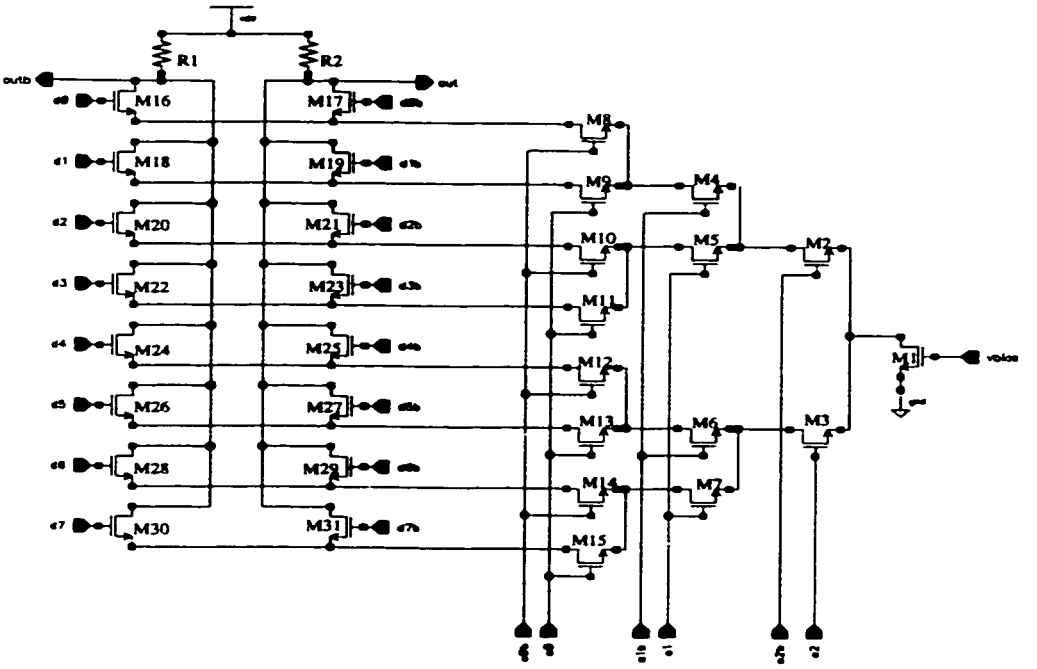


Figure 6.9: Time delay multiplexer circuit

between M2 and M3 sizes is used to control the gain of this stage. The replica bias stage M8-M10 and the OpAmp are important to control the delay cells active load bias so that a constant voltage swing is maintained for all the bias currents. M8 is identical to the delay cell current source, M9 is identical to one of its differential pair and M10 is identical to its load. The voltage reference Vref is used to set the Logic zero of the CML output to 2.5 volts, while the logic one is at Vdd (=3 volts).

6.4.5 Phase Multiplexer

Another important block in the compensation circuit design is the phase multiplexer. After, the divider output is converted to CML and passed through the delay chain, the multiplexer uses the accumulator contents (CMOS logic) to select

which delay output in the chain is to be converted to CMOS, and fed to the main loop PFD. Because the multiplexer control signals are at the CMOS levels, pass gate logic can be used for its implementation. The problem with this logic style is that the loading of the delay cells is dependent on the selected output. This causes undesirable systematic mismatches between the delays. To avoid this problem, the multiplexer circuit of Fig. 6.9 is proposed. It is similar to a CML MUX, but its control inputs are not converted to the CML level. They are kept at CMOS, and their complements are generated using CMOS inverters. This is possible because these control signals vary slowly. The DC current of the main current source M1 is steered, by the control inputs, through the pass gates M2-M15 to one of the eight CML stages M16-M31. Each of the inputs of these eight CML stages is driven by one of the delay cell outputs in the delay cell chain. Thus, all the delay cells have the same loading, regardless of the control inputs. Another dummy MUX is added to the delay cell chain in the DLL to match the loading of its delay cells to those of the main loop. It should be mentioned here that even though the control inputs are slow, their timing is carefully designed to be away from the rising or the falling edges of the divider output. The delay block in Fig. 6.3 is required for that reason.

6.5 Simulation Results

In order to examine the effectiveness of the DLL based spur compensation technique, the complete fractional-N PLL synthesizer is built on a single 0.35 μm CMOS prototype. The chip integrates all the synthesizer and its associated DLL functions. The only external components are the VCO and the main PLL loop filter. This

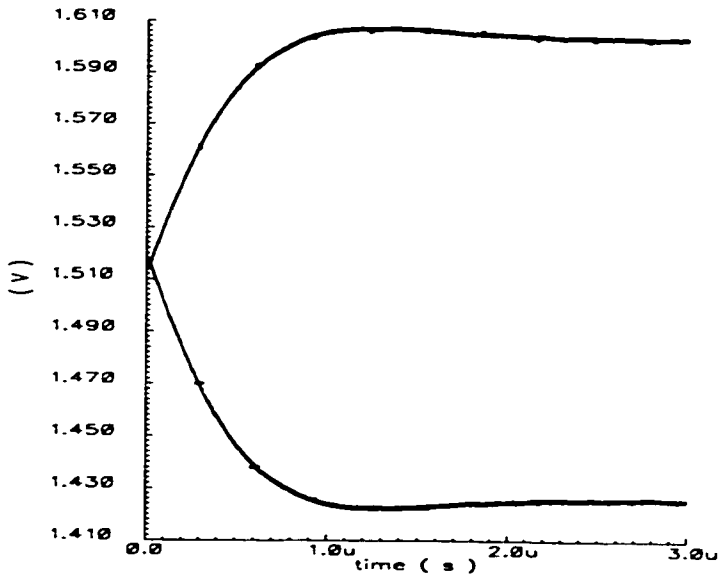


Figure 6.10: The differential DLL loop filter output

design is currently in fabrication and no measurement results are available yet. Therefore, simulation results are presented to test the circuit functionality, and to estimate the fractional spur level.

The full circuit level simulation of the fractional PLL may take several days (or weeks) to get a single results. Consequently, we modify the divider ratio in the original circuit to increase the comparison frequency from 1.6 MHz in the actual design to 62.2568 MHz in the simulated one, without touching the compensation circuits components.

This reference frequency is chosen so that the PLL output frequency is 2.0 GHz when the division ratio is 32.125. The PFD comparison frequency is increased by bypassing the integer CMOS divider (N and A counter in Fig. 6.3), and feeding the prescalar output directly to the compensation delay cells chain. In addition, the PLL BW is increased to reduce the simulation time needed for the loop to lock.

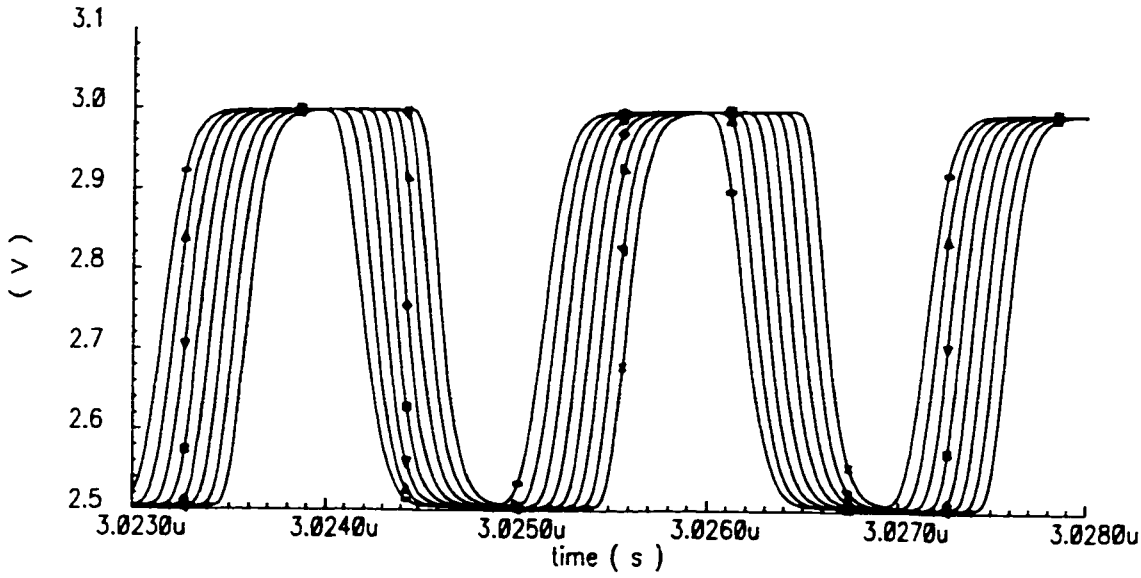


Figure 6.11: The DLL delay cells outputs

The simulated spurs in this case should give a direct indication of the spur levels in the actual circuit using 1.6 MHz reference.

Before trying the complete PLL simulation, the compensation DLL is simulated with an ideal input frequency of 2.0 GHz. After passing through the divide-by-4 counter this input runs the DLL at 500 MHz. Fig. 6.10 demonstrates the transient response of the differential DLL loop filter outputs. The settling time is slightly more than 1.0 μs, which is much faster than that of the original PLL with 1.6 MHz reference. The delay chain outputs are plotted in Fig. 6.11. Eight signals are shown with delay intervals of 62.5 ps. Even though a perfect device matching is assumed, the simulated delays exhibit ± 0.5 ps error. Those error may be attributed to the strong delay dependence on the rise and fall times of the inputs of each delay cell.

The full PLL simulation is performed twice, with and without fractional spur compensation. The transient PLL control voltage is shown in Fig. 6.12 with the

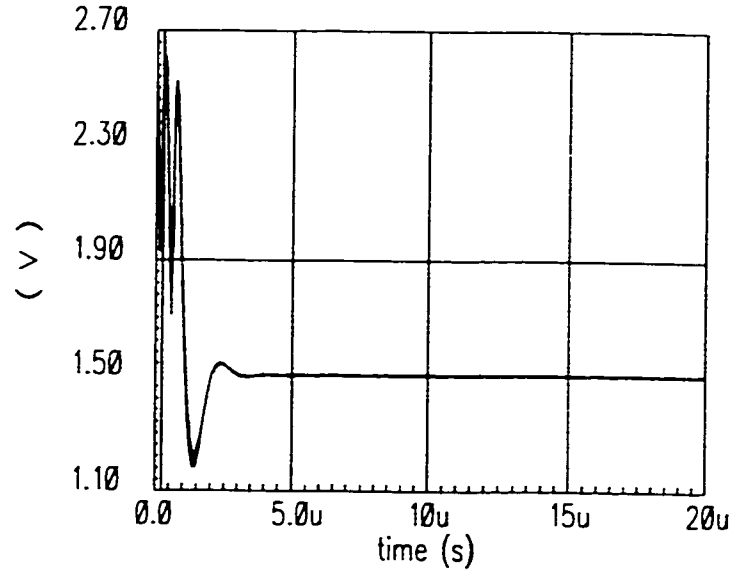


Figure 6.12: **Transient VCO control voltage of the PLL with the DLL fractional spur compensation**

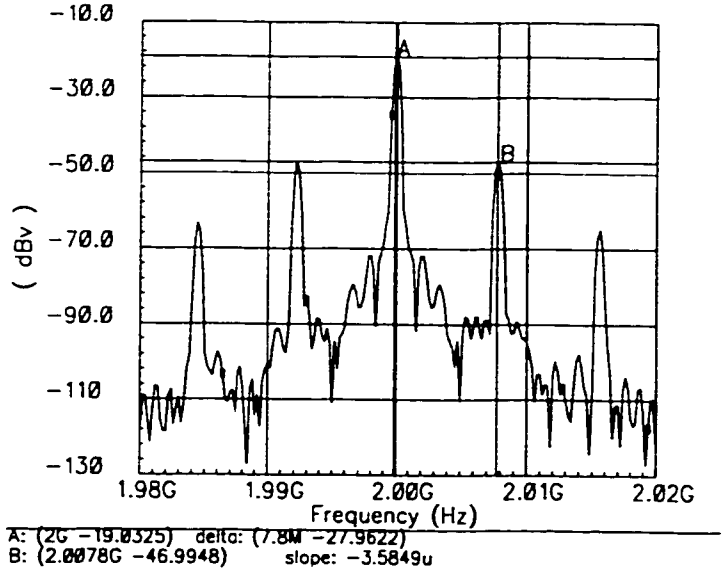


Figure 6.13: **Fractional PLL output spectrum without fractional spur compensation**

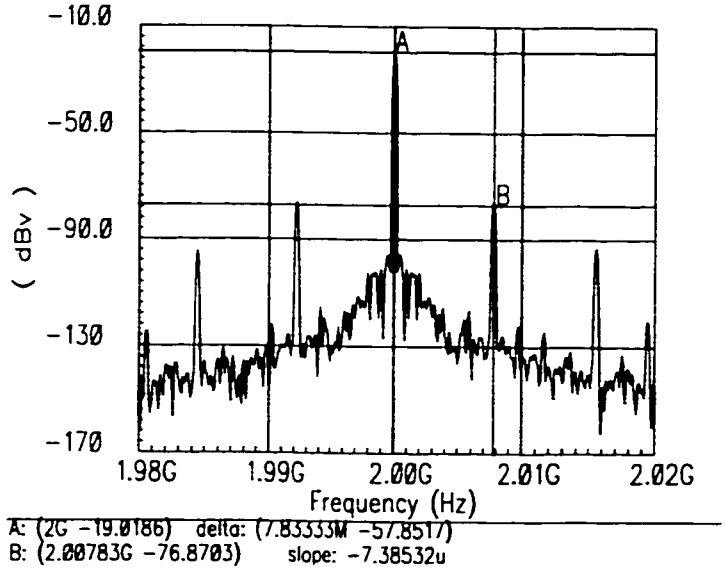


Figure 6.14: Fraction PLL output spectrum using DLL fractional spur compensation

compensation circuit engaged. The loop natural frequency is 600 KHZ and the settling time is 4.0 μs for a 100 MHz frequency step. The cycle slipping at the beginning is due to the long delays of the dead-zone free PFD and charge pump, which are designed to run at much lower frequencies. No significant change is noticed in the control voltage transients when the compensation circuit is disconnected. The output spectrum in the two cases is shown in Fig. 6.13 when no spur compensation is used, and in Fig 6.14 when the spur compensation is employed. In both cases, the fractional spurs occur at Δf = 7.81 MHz, which is one eighth the reference frequency. The spur level is -27.9 dBc in the first case. When the compensation circuit is used the spur level decreases to -57.8 dBc. Thus, the compensation techniques provides a 30 dB fractional spur suppression. Although a 30 dB fractional spur reduction is acceptable for some systems, it is not enough for most wireless

applications, which require the spur level to be below -65 dBc. This number is also much smaller than the suppression estimated by the system level simulations [71]. The limited spur suppression is caused by two reasons. First, there is a delay mismatch due to high sensitivity of the delay values to the rise and fall times of the delay cell inputs, which enhance the second order loading effects. The second reason is the strong coupling between the main PLL and the compensation DLL. Even though each loop dynamics is, to first order, independent of the other, their spurs are. Any spur in one of the loops results in a corresponding spur in the other loop, which in turn causes another spur in the first loop, and renders the full spur cancelation impossible. The whole fractional-N synthesizer, excluding the VCO, consumes 12 mA from a 3.0 V supply.

6.6 Conclusion

Full circuit implementation of the DLL based fractional spur compensation technique is presented. Several design challenges on the circuit levels are addressed. The final PLL consumes 36 mW and exhibits a simulated -57.8 dBc fractional spurs at 7.81 MHz offset from 2 GHz center frequency. This spur level corresponds to a 30 dB reduction due to the DLL based spur cancelation architecture. Contrary to system level simulation results presented in literature, the spur reduction is not enough for most wireless systems. The limited effectiveness of the architecture is attributed to the strong coupling between the main PLL and the compensation DLL.

Chapter 7

Phase Domain Fractional-N Frequency Synthesizers

7.1 Introduction

One of the important objectives of using fractional-N synthesizers is to obliterate the tradeoff between the switching speed and the channel spacing. As discussed chapter 6, fractional-N synthesizers that use analog or delay based compensation provide a limited fractionality between modulo-8 and modulo-16, in most cases. Often though, this is not enough to open up the loop bandwidth to achieve fast switching. Sigma-Delta fractional synthesizers [73, 74, 68] provide an unlimited resolution (depending only on the modulator number of bits), which allow high reference frequencies and a wider bandwidth. Unfortunately, the bandwidth increase is limited by the fast rise of the quantization noise at higher frequencies. All digital (DDFS) solutions can provide much faster switching, and high resolutions but they

do have a limited output frequency.

In this chapter, we investigate a fractional-N frequency synthesis technique that is based on using a numerical phase comparator to predict the phase error of the PLL. Some researchers have used such phase comparators in the past for several applications, and achieved promising results [75, 76, 77, 78]. In this chapter an attempt is made to adapt the use of such phase comparators for wireless applications.

In the next section, the concept of weighted phase error is presented, where a numerical phase comparator is necessary to achieve the channel selection. Then, a full frequency synthesizer architecture based on this concept is presented. Both the analog and digital implementation alternatives for this architecture are evaluated, and compared. The analog solution is simpler, but causes some uncertainty in the output channel frequency. This channel frequency error is not acceptable in many wireless systems; hence, the digital solution is favored. A novel timing error correction scheme that renders the digital implementation more practical is then presented. Some other circuit design issues are also discussed. System level simulations are used to prove the functionality of the proposed architecture. Switching times as low as 5 μs are feasible with theoretically unlimited channel resolutions. In this digital system, a DAC is needed to eventually produce the VCO analog control signal. The output spur levels and frequencies are shown to depend on the DAC accuracy. Spur levels as low as -65 dBc are achievable while requiring only a 10-bit DAC accuracy. The DAC need to be fast enough to resolve signals at frequencies up to 300 MHz at its input.

7.2 The Concept of Weighted Phase Error and Channel Selection

Usually fractional-N frequency synthesis, depends on a dual modulus divider in the feedback path of the PLL. Typically, for RF frequency synthesizers, this dual modulus divider utilizes a pulse swallow circuit to switch the division ratio between N and N+1 depending on an input control signal. This control signal is alternated between zero and one in a controlled pattern so that the the effective division ratio is N plus a controllable fraction f, which is determined by the switching pattern of the control signal. In this chapter, this type of fractional N synthesis is referred to as "*Time Domain Fractional Synthesis*" or (TDFS). This includes all popular types of fractional dividers. In essence, they change the division ratio in the time domain between multiple integer values in order to achieve an average fractional division, regardless of the spur compensation technique used.

In this work, a technique for achieving fractional-N synthesis that has received very little attention in the literature is evaluated. This technique will be referred to as "*Phase Domain Fractional Synthesis*" or (PDFS). As will be detailed, the signal is instantaneously divided by multiple integers. The phase of each divider output is compared to the reference to produce a certain phase error. The total phase error can then be generated as a weighted linear combination of these individual phase errors to produce an effective phase error, corresponding to a fractional divider. The fraction of the division ratio is determined by the ratio of the weighting factors used in the linear combination. Another way to understand this, as shown in Fig.

7.1, is to assume that two dividers are available. The first one continuously divides by N, while the other divides by N+1. If we are able, "somehow", to linearly combine the phases of the output signals from both dividers using the weighting factors α and β, then the output phase corresponds to a fractional division ratio (N+f) between N and N+1. This fractional division ratio can be expressed as

$$N + f = \left(\frac{\beta}{N} + \frac{\alpha}{N+1}\right)^{-1}. \tag{7.1}$$

From this expression we see that in order for the fraction (f) to have a value between

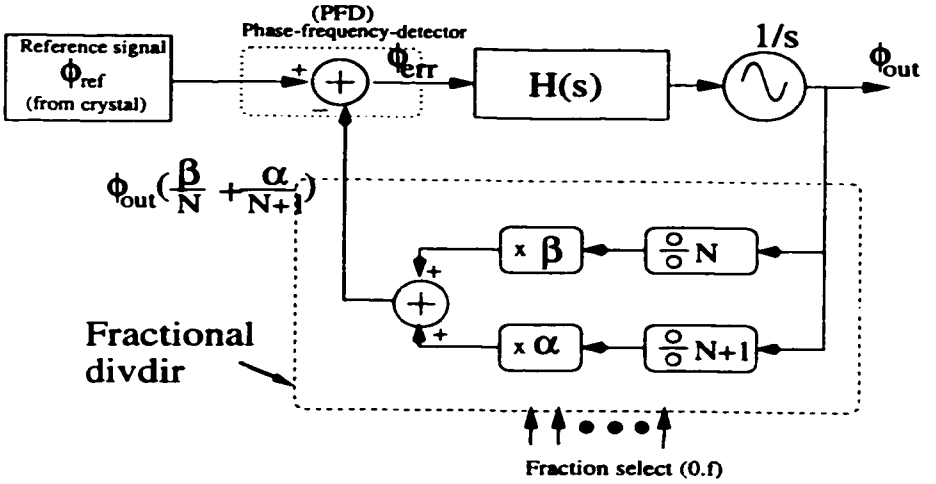


Figure 7.1: Basic idea of Phase Domain Frequency Synthesis (PDFS)

0 and 1, the sum of α and β must be equal to 1. However, it is impossible to have equally spaced fractions (f) with limited number of bits representations for both α and β. To overcome this restriction the architecture of Fig. 7.1 can be reduced to that of figure 7.2, where we add one more degree of freedom by multiplying the phase of the reference source by γ. In this case α and β no longer have to sum

to one. Instead, the summation of $\alpha/\gamma + \beta/\gamma$ has to be one to maintain effective division ratio between N and N+1. The total phase error output of the linear phase combiner can now be written as

$$\phi_{err} = \gamma\phi_{ref} - \phi_{out}(\frac{\beta}{N} + \frac{\alpha}{N+1}). \tag{7.2}$$

Usually, in a type two PLL [12], the loop filter would have a pure integrator; the phase error becomes zero when the loop is locked. Setting the above phase error to zero and choosing γ to be equal to $\alpha + \beta$, we can write the relation between the reference phase and the output phase as

$$\frac{\phi_{ref}}{\phi_{out}} = \frac{1}{N+f} = \frac{\alpha/(\alpha+\beta)}{N} + \frac{\beta/(\alpha+\beta)}{N+1} \tag{7.3}$$

In order for α and β to have a limited number of bits, we choose

$$\alpha + \beta = N + f \tag{7.4}$$

which results in

$$\alpha = f(N+1) \tag{7.4a}$$

$$\beta = N(1-f) \tag{7.4b}$$

The result of Eq. 7.4 suggests that the number of bits needed to represent α, β and γ is equal to the sum of the number of bits representing both the integer divisor (N) and its fraction (f). In other words, the required number of bits is determined

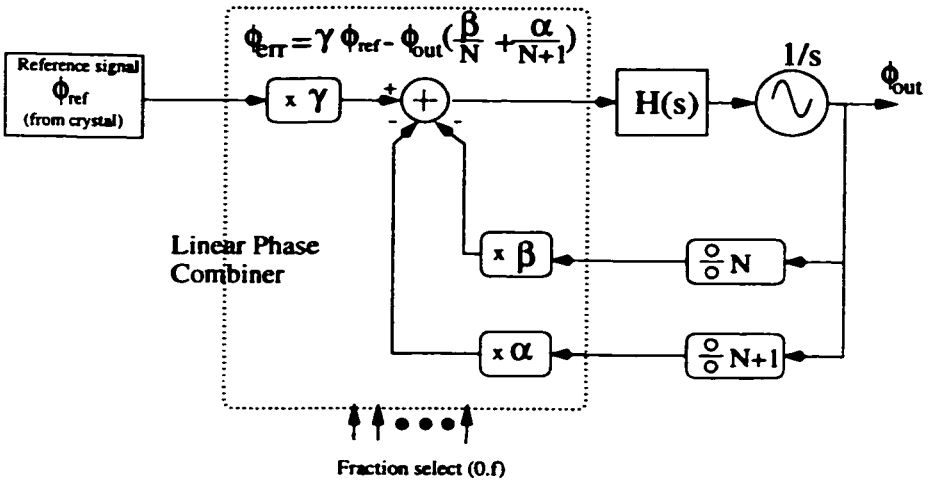


Figure 7.2: The use of linear phase combiner for (PDFS)

by the frequency resolution, or the ratio of the synthesizer output frequency to the minimum channel spacing. For example, in a GSM system this ratio is 900 MHz/200 KHz which is equivalent to 13 bits.

It is important to mention here that the linearity of the "Linear Phase Combiner" in Fig 7.2 is critical to prevent any fractional spurs at the VCO control. For a linear combiner, the only frequency components at the output are those fed at the input. Because this is a fractional division, the reference frequency can be chosen to be arbitrarily high; the result is an easy filtering of the reference frequency components at the VCO control input. It is this fact that makes this architecture capable of very fast switching. Switching times as low as 5 μs are possible, as will be shown later.

7.3 The Proposed Fractional-N PLL Architecture

A further look at both the PLL architectures of Fig. 7.1 and Fig. 7.2, indicates that both require two high speed frequency dividers, as opposed to only one in conventional PLL architectures. This necessitates more power consumption as well as a more complicated phase combiner design, which has to combine the phase of three signals instead of two. In order to reduce this extra hardware, we notice that the fractional divider of Fig. 7.1 has enough degrees of freedom to get the fractional division, and the extra degree of freedom introduced by adding γ in Fig. 7.2 is only needed to limit the required number of bits for α and β. This means that we can remove one degree of freedom from figure 7.2 and still obtain the required fractional division. Consequently, we chose to remove the (N+1) branch and attempt to obtain the fractional division with a finite bit representation for the two remaining coefficients γ and β. In order to prevent confusion, the integer divider value will be referred to as N_1, and the value N is reserved for the integer part of the required frequency multiplier N+f. It is easy to find a good mapping from (N_1, N and f) to (γ and β) that satisfies this requirement as follows:

$$\beta = N_1 \quad \text{and} \quad \gamma = N + f. \tag{7.5}$$

Substituting these values into Eq. 7.3 and setting $\alpha = 0$, the effective division ratio is found to be equal to N+f. The resulting fractional-N synthesizer architecture is shown in Fig. 7.3. It is noteworthy that the choice of N_1 is arbitrary; it does not have to be the same as N. The proper choice of N_1 may reduce the hardware and/or

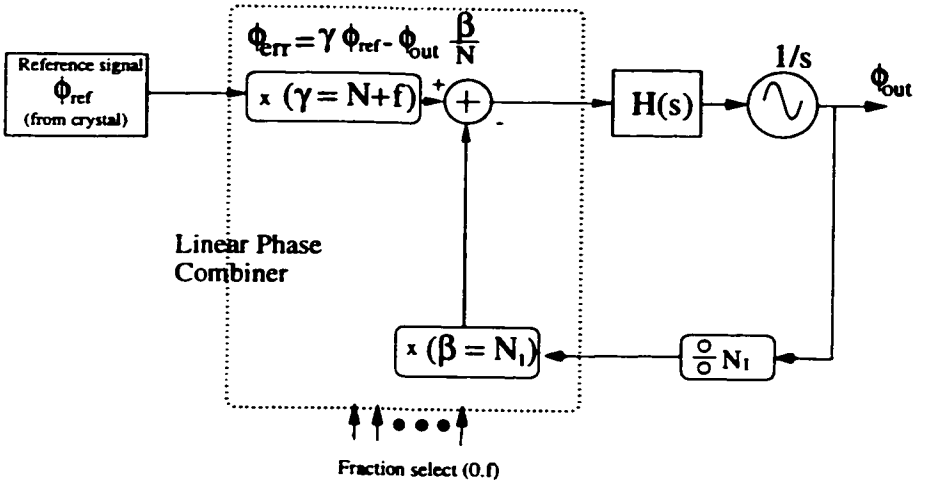


Figure 7.3: Reduced complexity phase domain frequency synthesizer using one frequency divider

the output spurs as will be discussed later.

In this architecture, not only is one divider branch and its associated hardware eliminated, but also the weighting factors are simplified to a direct mapping of N_1 and N+f. Again, the key element in this architecture is the linear phase combiner. Apparently we cannot use a conventional phase frequency detector (PFD), because it has a limited range for linear operation that requires the two input frequencies to be equal when the loop is locked, This is not the case here. A linear phase detector that takes the frequency into account can be implemented as a counter (or an accumulator) that is incremented at each positive (or negative) edge of its input. Instead of two accumulators (one for each input signal) and a subtracter to detect the phase difference, one accumulator can be used to add γ at the reference edge, and to subtract β at the divider output edge. The accumulator content at any time becomes the weighted phase error we require. If the loop filter is type

two, meaning that it has a pure integrator pole, the average phase error is zero when the loop is in lock. Thus, the accumulator does not overflow as long as it has enough bits to represent its value variation around zero (two bits more than N+f should be enough).

The output from the linear phase combiner should be in analog form to control the VCO input. This gives us two choices: convert γ and β to analog and implement the phase accumulator in the analog domain, or build the accumulator in the digital domain and then convert its output to analog to drive the loop filter. Both techniques have their advantages and disadvantages and will be discussed in detail in the following subsections.

7.3.1 Analog Phase Frequency Detector Implementation

The charge pump that is used in most PLL designs can be utilized to implement an analog accumulator. Fig. 7.4 describes the architecture of such a charge pump based analog accumulator. The digital data words γ and β are used to program two digitally controlled charge pumps: one for the up current, and one for the down current. A digitally controlled charge pump, which we call a "*digital-to-current*" converter, is in fact a digital to analog converter (DAC), whose output current does not need to be converted to a voltage, contrary to most other DAC's. Instead, the output current is integrated into an output capacitor to produce the phase error. The UP DAC requires a number of bits equal to that of N+f, whereas the DWN DAC needs only a number of bits equal to that of N_1. The integral nonlinearity (INL) requirements of those DAC's, as well as the matching of their

reference currents, are very strict. To explain this, the full operation of the linear phase combiner of figure 7.4 is described.

The positive edge pulse generator produces a pulse of a fixed width at each positive edge of its input signal. The width of the pulses generated by both the reference signal and the divided VCO output should be well matched. At the positive edge of the reference, a charge equal to $(\tau.\gamma)$ is pumped to the output capacitor. At the divided VCO output positive edge, a charge equal to $(\tau.\beta)$ is drawn from the capacitor. The net capacitor charge is then proportional to the accumulated phase of the reference (modified by its own DAC and pulse width error factor) minus that of the divided VCO output. An active loop filter is necessary to integrate the charge pump output which represents the phase error, not its integration. In the steady state, when the PLL is locked, the charge pump capacitor voltage should be zero corresponding to a zero phase error. Thus, a differential charge pump is necessary to avoid saturating the DWN current source. Because of the fact that each phase is modified by its own error factor before the subtraction, a false zero phase error can be detected, leading to an error in the resulting synthesizer output frequency. Although this error may be acceptable in some applications like cordless phones and wireless LAN systems, it is not acceptable in cellular systems. For example, the required channel frequency accuracy for GSM systems is ± 50 Hz of the output frequency which is around 900 MHz. This translates to a 24 bit INL accuracy for the current DAC. Also, the same level of accuracy is needed for the ratio between the two DAC outputs. These numbers are impractical and limit this architecture to those applications with a reasonable tolerance on the frequency

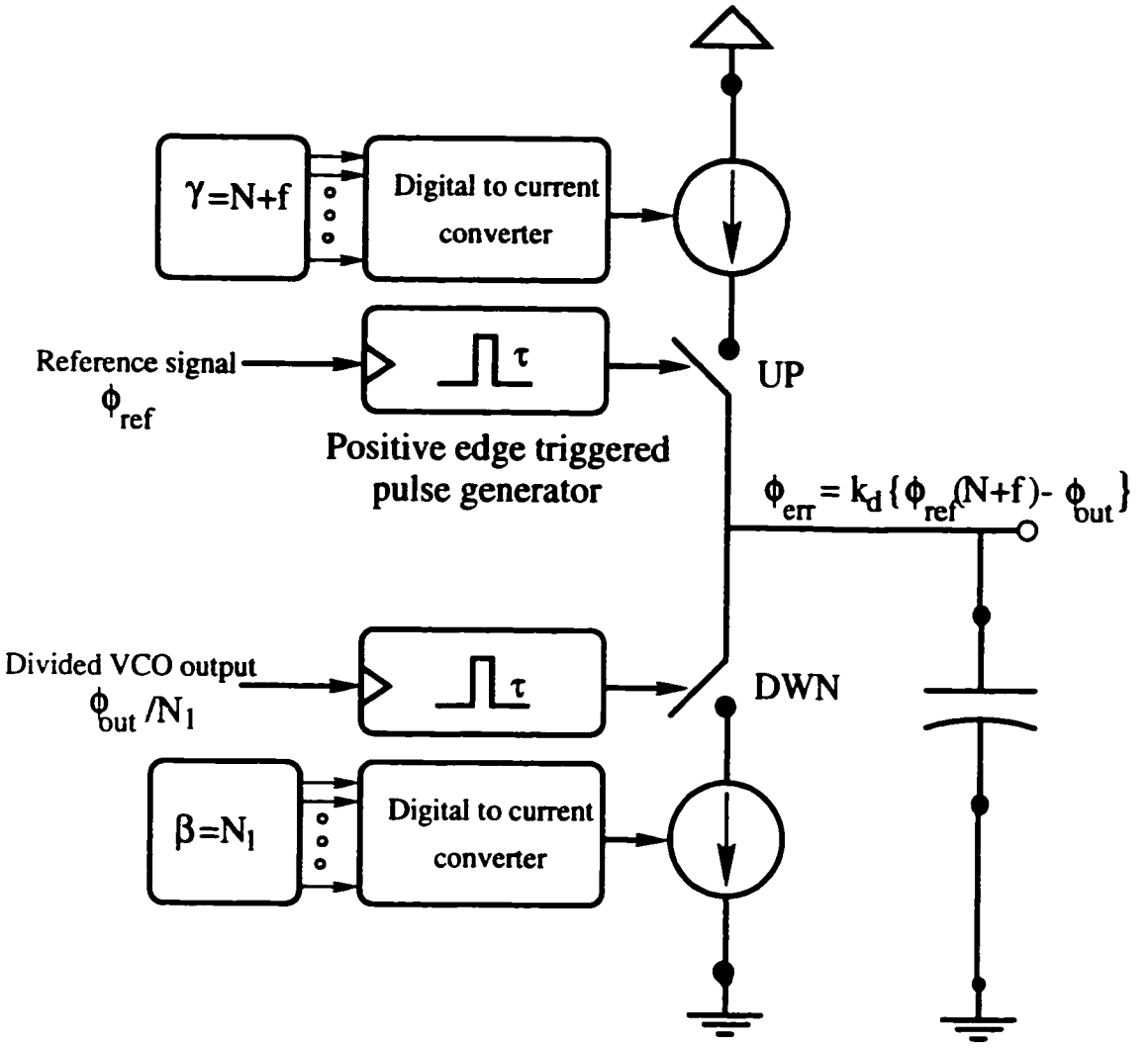


Figure 7.4: Charge pump based analog linear Weighted Phase Frequency Detector (WPFD)

accuracy.

Before we proceed to the digital alternative to avoid this frequency error, it is instructive to mention some of the advantages of this implementation. First, the current sources are independently controlled. This means no restrictions on the time spacing between the edges of the input signals. Both signals could arrive at exactly the same time with no problem. The second advantage is that the DAC speed is not important. It is only limited by the required channel switching speed, which is in the microsecond or even the millisecond range. This allows the use of sophisticated techniques to implement those DAC's such as digital Sigma-Delta modulators.

7.3.2 Digital Phase Frequency Detector Implementation

In order to avoid the frequency error inherent in an analog accumulator phase detector, a digital accumulator implementation is considered. Fig. 7.5 displays a full synthesizer built using a digital *Weighted Phase Frequency Detector* (WPFD). The accumulator register holds the current phase error value. A digital word γ is added at the positive edge of the reference signal. Another digital word β is subtracted at the positive edge of the divided VCO output. When the loop is in lock, the average accumulator contents, which represent the absolute phase of the reference multiplied by γ minus the absolute phase of the divided VCO output multiplied by β, is zero. After the signals are subtracted digitally, a DAC is used to convert the output to the analog domain before applying it to the loop filter. The DAC nonlinearity introduces similar errors to the analog WPFD case. The main

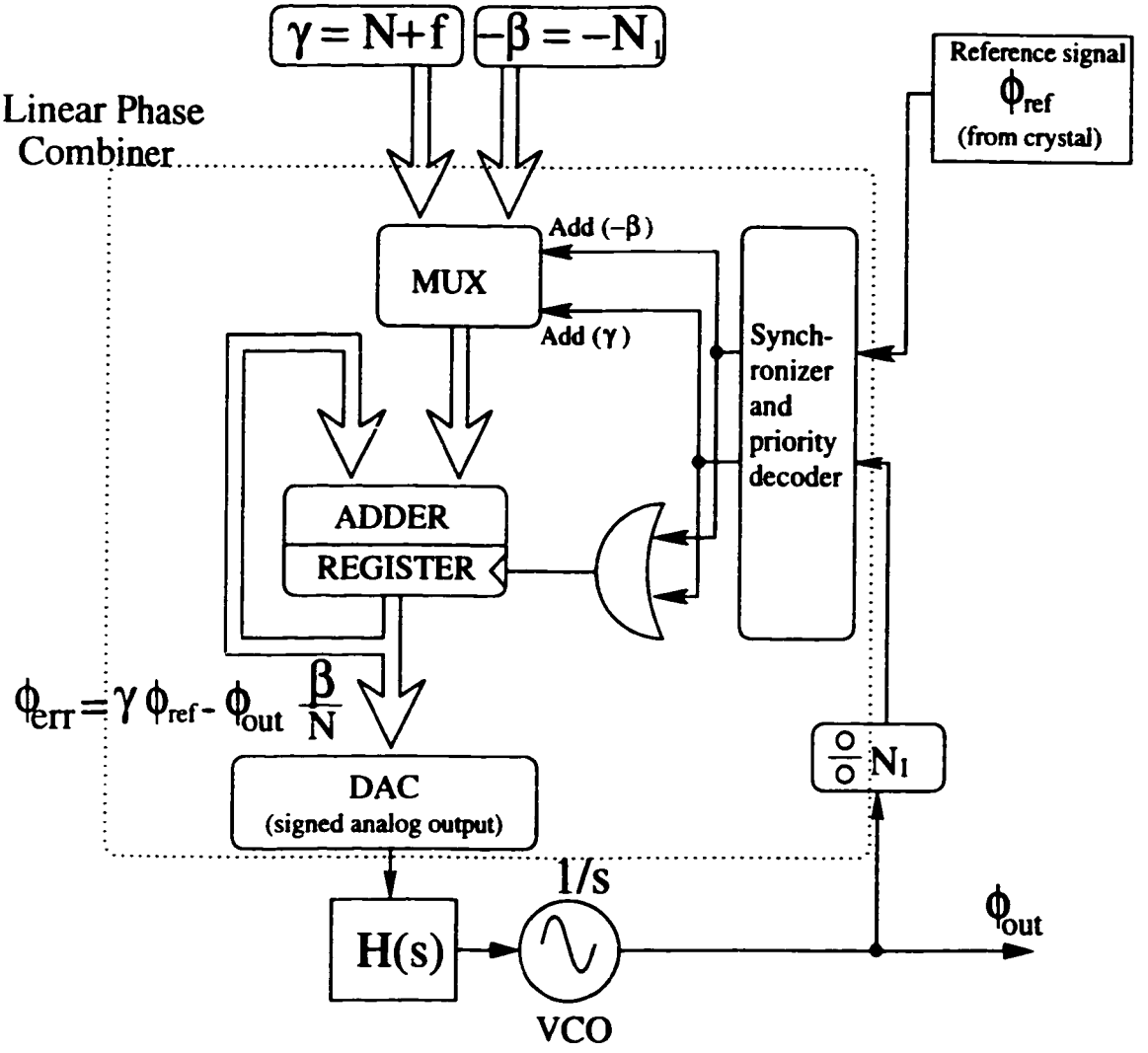


Figure 7.5: Full PLL frequency synthesizer using digital accumulator as a Weighted Phase Frequency Detector (WPFD)

difference is that the digital contents of the accumulator are always correct. The errors are introduced after the weighted phases are subtracted. As a result, the phase error does not accumulate, and the error in determining the center frequency is zero. Once the frequency is locked correctly, any inaccuracy in sensing the phase error due to the DAC, is transformed into spurs and does not affect the frequency accuracy.

Therefore, the digital WPFD implementation eliminates the output frequency inaccuracy at the expense of causing spurs at the output. The spurs are not only caused by the DAC nonlinearity, but also by the timing delay of the accumulator. The waveform (c) in Fig. 7.6, shows a sample of the accumulator contents in response to an input reference in trace (a), and a divided VCO output in trace (b). In ideal conditions when the loop is in lock, the average area under trace (c), which corresponds to the integrated phase error, should be equal to zero. An error in either the amplitude (due to the DAC) or the timing (due to finite adder delay) causes the loop to detect a false shift from the zero average, and attempts to compensate for it. Because the error does not accumulate, the loop soon detects the erroneous phase shift it has caused, and corrects for it again. The same scenario is repeated in a periodic manner, causing the output spurs. Several factors determine the period of such spurs, and they are best predicted by simulations. Among the factors are the DAC number of bits, the DAC accuracy, the desired output frequency, and the factors γ and β. Proper frequency planning through a good choice of γ and β help move the spurs away from the critical blocking channel frequencies. The level of the spurs is directly proportional to the errors introduced and are managed by only

controlling those errors, in the timing and amplitude.

Timing Error

Usually, the timing error is more serious than the amplitude one. In order to clarify this, the error caused due to the adder delay is depicted in Fig. 7.6. Both the reference signal and the divided VCO outputs run at different frequencies, and are not synchronized. Consequently, the positive edges of both signals could occur within a very short (or even zero) time interval. Because the accumulator cannot change its state instantaneously, it either ignores the second incoming pulse causing a huge unrecoverable phase an frequency error, or it responds to it after a certain delay. In this second case, no frequency error occurs and only a spur is caused at the output, as explained before. Traces (c) and (d) in Fig. 7.6 compare the ideal case to this second case. The shaded area in trace (d) represents the error introduced by the delayed accumulator response to one of its two inputs. The resulting integrated outputs are shown in traces (c') and (d'). Because the delay error represents a relatively large fraction of the input signal periods, the error it introduces is equivalent to the use of a very limited number of bits of the DAC. For example, assume the reference frequency is 50 MHz (20 ns period), and the accumulator-DAC delay is 3 ns. The error introduced by this delay corresponds to the use of a 3 bit DAC.

In order to reduce the effect of this delay error, an attempt is made to modify the accumulator operation such that it is capable of self correcting the delay error. Trace (e) of Fig. 7.6 shows a proposed solution; the resulting integrated output is shown in trace (e'). When signal (b) arrives while the accumulator is busy

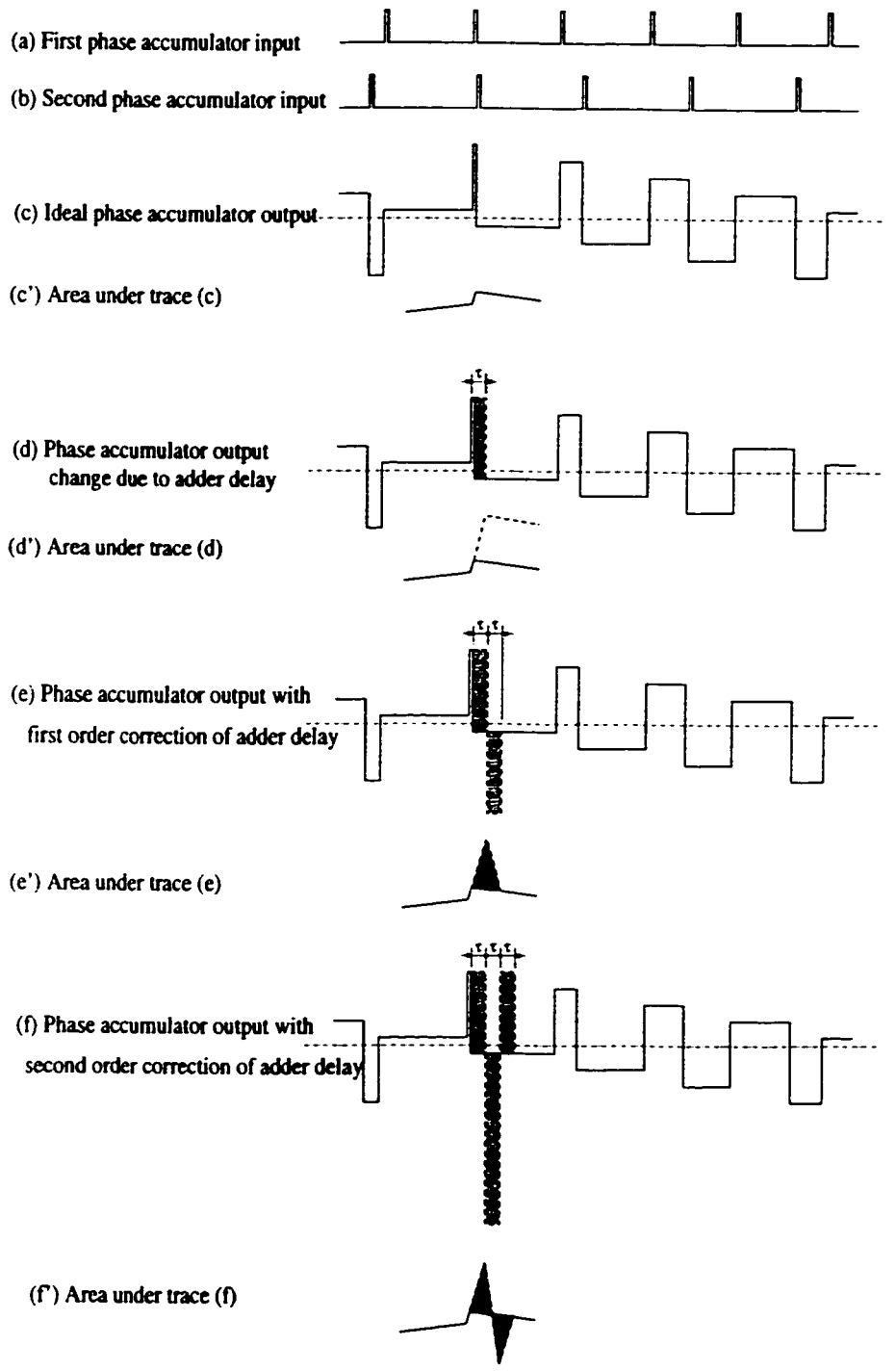


Figure 7.6: Adder delay

processing signal (a), signal (b) is passed twice through a fixed delay block. This delay is longer than the accumulator processing time. After the first round in the delay block, a value of 2β is subtracted from the accumulator contents. After the second round in the delay block, the value of β is added. The resulting integrator output at the end of these two delays as shown in trace (e') is the same as that of the ideal case of trace (c'). After implementing this correction, the system simulation shows a good reduction in the spurs, but there is still a considerable spur due to the delay error. We refer to this timing scheme as "*first order correction*".

If we investigate the loop dynamics further, it is clear that the subsequent filtering stages, after the integrator stage, perform another averaging of the integrator output. This averaging is equivalent to a second integration. This means that in order to completely cancel the delay error effect, the area under trace (e') should be the same as that under trace (c') which is not the case here. Therefore, a "*second order correction*" scheme is used. As explained in trace (f), signal (b) is passed through the delay block three times. The first time the value 3β is subtracted from the accumulator. After the second round, the value 3β is added. Finally, a value β is subtracted after the third delay. The resulting integrator output is shown in trace (f'), which has the same area under it as that of trace (c'). Simulations demonstrates a full cancelation of the delay error with this second order correction.

DAC Accuracy

Having the second order delay compensation in place, we are now left only with the spurs due to the limited DAC linearity. There is no straight forward relation between the DAC number of bits, and the synthesizer output spurs. This is because

the process is involved and both the level and the frequency of the spur depend an the number of bits, as well as the loop filter and divider parameters. Simulations show that an 8-bit to 10-bit DAC suffices for most applications. The "beauty of this system" is that the spur does not increase by increasing the accumulator size without any increase in the DAC bits. As a result, the frequency resolution is determined only at the hardware cost of adding extra bits to the adder and the register. Some error is introduced due to the rise and fall time mismatches and switching glitches of the DAC. In order to minimize this effect the output is allowed to settle for a relatively long time (~3.0ns) in each state before the next input pulse.

7.4 Circuit Design Issues

Although a full circuit implementation of the phase domain frequency synthesizer architecture is beyond the scope of this work, the objective of this section is to highlight some of the practical issues involved in such a design.

7.4.1 Digital Delay and Power Consumption

The design of the digital WPFD, its relevant controls, and the digital decoder for the DAC, necessitates a fast, yet power efficient logic style. The accumulator which uses about 16-bit adder requires a delay in the range of 1 to 2 ns. While it is not easy to achieve such high speeds using conventional CMOS implementations, current mode logic or CML consumes too much power. Most of the CML power consumption results from static current, which is justified only if the logic runs

at very high clock rates. Even though it needs high processing speed, the WPFD runs at rates around the reference frequency ($\leq$50 MHz), which makes the CML very inefficient. An alternative logic style that has delays comparable to CML but only uses DC current when an evaluations is needed may be DyCML [79] or SC^{2}L [80]. These logic styles meet our delay requirement, and their power consumption corresponds to the actual data rate which is not so high in this design.

7.4.2 Delay Correction Accuracy

Another important issue that arises when designing the delay compensation circuitry is how to match the different delays needed to achieve full spur cancelation. In order to avoid the mismatches among the various delay components, we propose using a single delay cell with a simple finite state machine to replace the three identical delays needed for the second order timing error cancelation. In addition to eliminating the mismatch between the delays, this architecture reduces the hardware required to implement those delays.

Also, the error cancelation accuracy is affected by the rise and fall times of the DAC outputs, which directly relates to those of the digital WPFD. This effect could be significantly reduced by matching the rise and the fall times. This could be best achieved using differential architectures both for the digital WPFD and the DAC. Another helpful technique is to increase the allowed delay value so that the rise and fall times represent a small fraction of this period. This delay value is limited by the faster of the reference signal or the divided VCO output. In order to find the maximum delay τ, we assume that the period of the faster of these two signal is

T. In the worst case when the second signal arrives at the end of the busy interval τ, due to a previous signal, another 3τ delay is required for error cancelation plus one more τ to clear the accumulator for the next incoming signal. Therefore, when choosing τ we have to be certain that

$$\tau \leq T/5 \tag{7.6}$$

In the example used for our simulations, T is approximately 17 ns, leading to a 3 ns reasonable value for τ.

7.4.3 DAC Speed and Linearity

The most challenging circuit design in the digital WPFD architecture is the DAC. The second order timing error compensation greatly reduces the speed requirements of the DAC and brings it into a feasible range. For the above example, the DAC is required to resolve samples with a minimum interval of 3 ns. The required DAC accuracy is in the range of 8-10 bits depending on the required spur level. Many DAC designs that meet such requirements [81, 82, 83] have been reported. Most of those designs are current mode designs that feed all the currents directly to the output. This is exactly what is needed for the WPFD DAC. The only problem with these designs is their relatively high power consumption for both the fast digital decoding of the inputs, and to achieve a high dynamic range at the output. The digital power consumption for the digital parts can be much lower in our case, due to the low average clock speed. In the WPFD DAC, the output current is being integrated into the output capacitor, rather than converted to a voltage through a

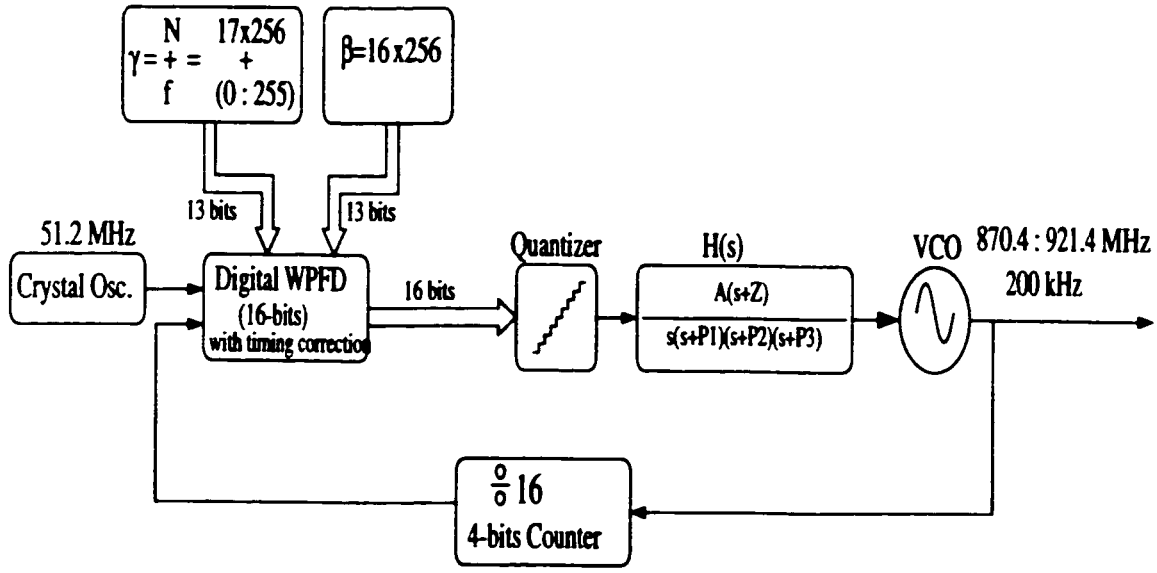


Figure 7.7: Block diagram for WPFD simulations

resistor. Consequently, no voltage dynamic range problem exist, and small currents can be used.

In order to achieve the required accuracy with reasonable device matching, the design should be segmented into thermometer coded, and binary weighted parts [84]. The full binary weighted design is much simpler because no decoding is involved. However, it suffers from severe matching requirements and large transition glitches. A full thermometer coded design avoids these problems, but requires full decoding, and a large number of current cells. Because of area issues segmentation is a good compromise, and is recommended for the WPFD DAC design.

7.5 System Simulations

In order to test the functionality of the WPFD based synthesizer architecture, a Matlab Simulink system based on the block diagram of Fig. 7.5 is used. A simplified block diagram of the simulated system is shown in Fig. 7.7; e.g., the frequency bands shown correspond to a GSM receiver. The high input reference frequency of 51.2 MHz allows a wide loop band width, and fast switching times. A 13-bit register is used for γ, out of which 8-bits are use for the fraction leading to a channel resolution of 51.2 MHz/256 or 200 KHz. The GSM band is covered by changing the fraction value only; the integer multiplier is kept at 17 all the time. A 4-bit counter provides a fixed divide-by-16, with a corresponding β value of 16. The VCO gain is 50 MHz/V, the PLL natural frequency is 190 KHz, and the damping factor is 0.707. Two secondary poles at 1.6 MHz and 5.4 MHz help reduce the reference spurs. The VCO control as well as the WPFD accumulator value (or the phase error) are shown in Fig. 7.8, for a 100 MHz output frequency step. The settling time is approximately 7 μs. The thin phase error excursions in the figure are a result of the second order timing correction.

The VCO output spectrum is shown in Fig. 7.9. For this plot, a 10-bit DAC is used with a second order timing correction and a τ value of 3 ns. The integer part of γ is 17, and fraction is 137/256. The resulting output frequency is 898.2 MHz. The simulation step is 13.13 ps, and four Mega samples are used for the FFT. The reference and the divided VCO spurs are at -92 and -96 dBc below the carrier, respectively. The close-in spurs due to the DAC quantization error are below -65 dBc.

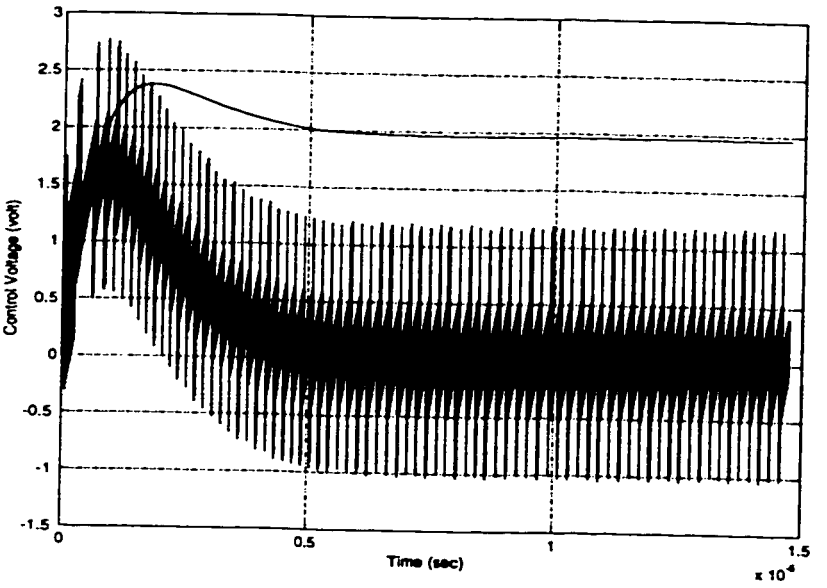


Figure 7.8: The transient response of WPFD PLL

In addition, the effects of both the first order and the second order delay correction schemes are examined. For this experiment, an ideal DAC is assumed for all cases. The WPFD DAC delay τ is set to 3 ns. Fig. 7.10 illustrates the output spectrum when no delay correction is used. The close-in spurs are as high as -20 dBc. The use of the first order delay correction drastically reduces the spurs as portrayed in Fig. 7.11. The spurs are at -51 dBc, which is too high for many applications. Further reduction in the spur levels is achieved when a second order correction is employed. The resulting spectrum is shown in Fig. 7.12, where the spurs are below -77 dBc. This spur level is equal to that resulting when an ideal accumulator (with no delays) is used (Fig. 7.13). Therefore, the second order correction does provide almost a complete timing error cancelation.

In order to determine the required DAC accuracy, we vary the quantizer number of bits to see its effect on the close-in spurs. The output spectrum using eight,

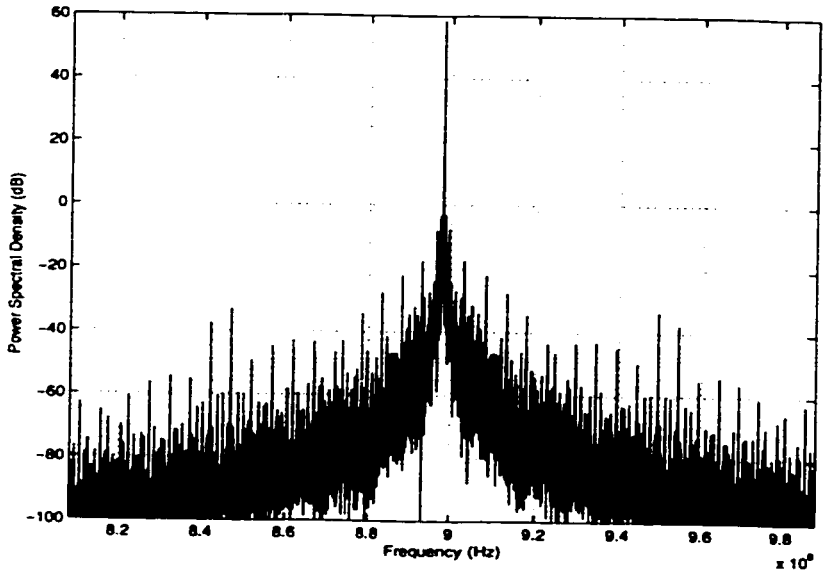


Figure 7.9: PLL output spectrum for a 10-bit DAC, and second order timing error correction

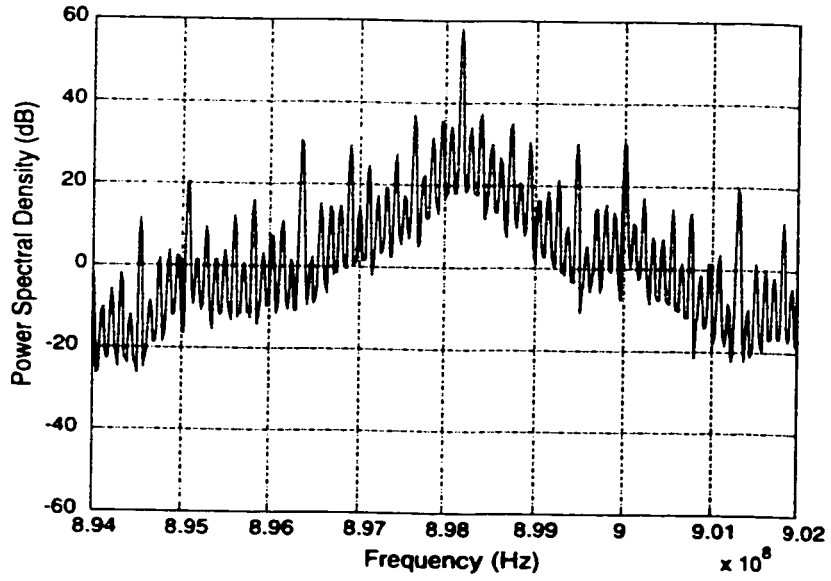


Figure 7.10: PLL output spectrum for an ideal DAC, and no timing error correction

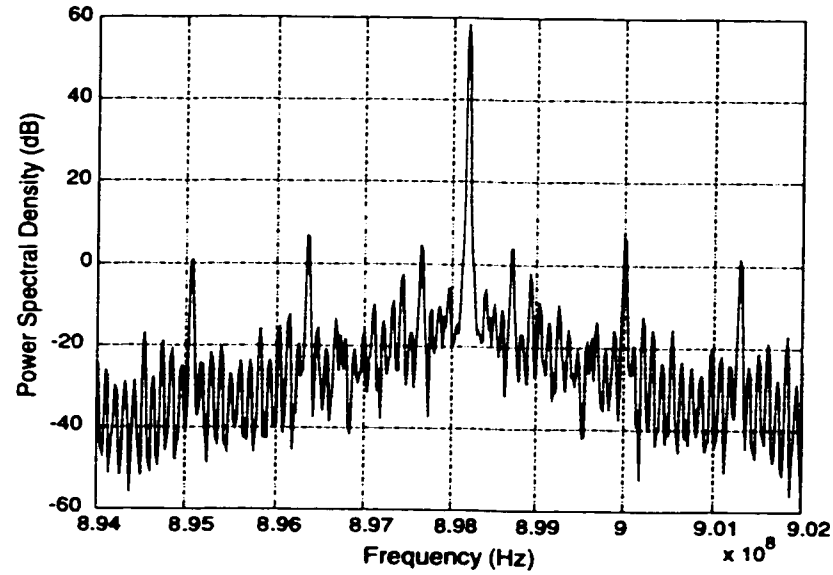


Figure 7.11: PLL output spectrum for an ideal DAC, and a first order timing error correction

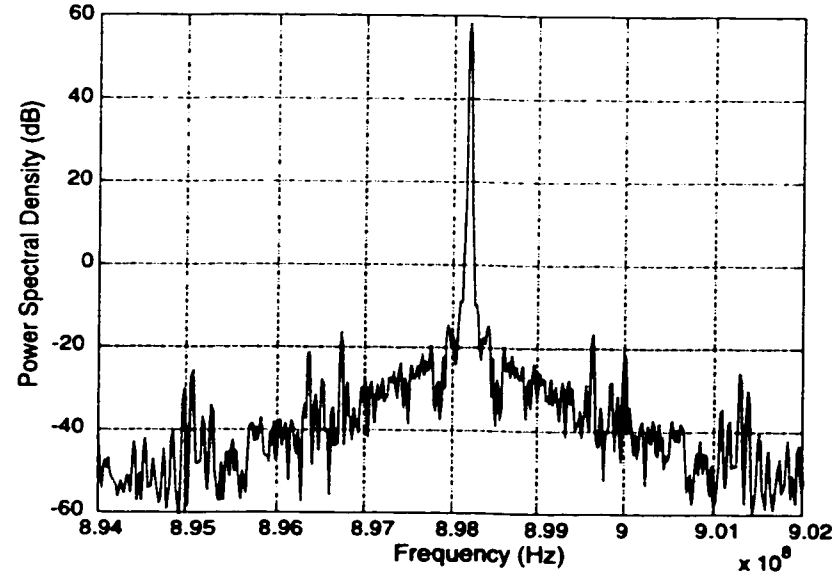


Figure 7.12: PLL output spectrum for an ideal DAC, and a second order timing error correction

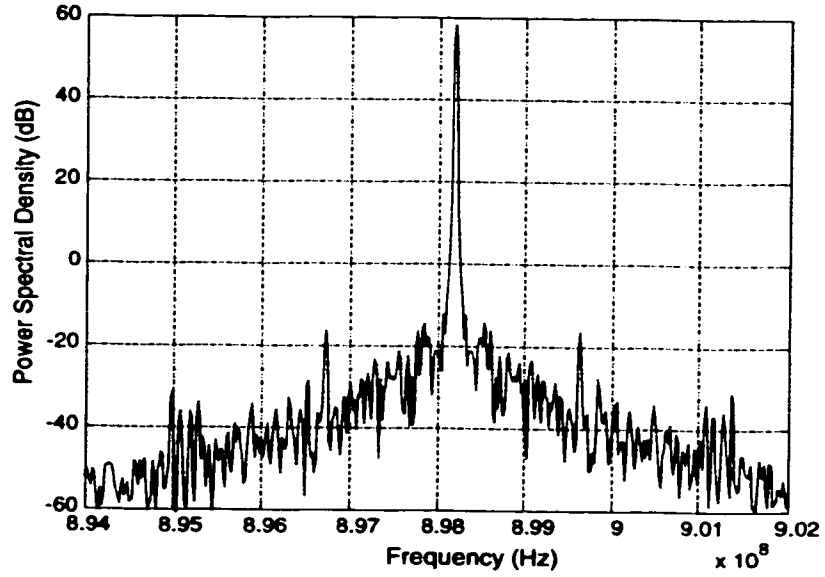


Figure 7.13: PLL output spectrum for for ideal DAC, and a delay free accumulator

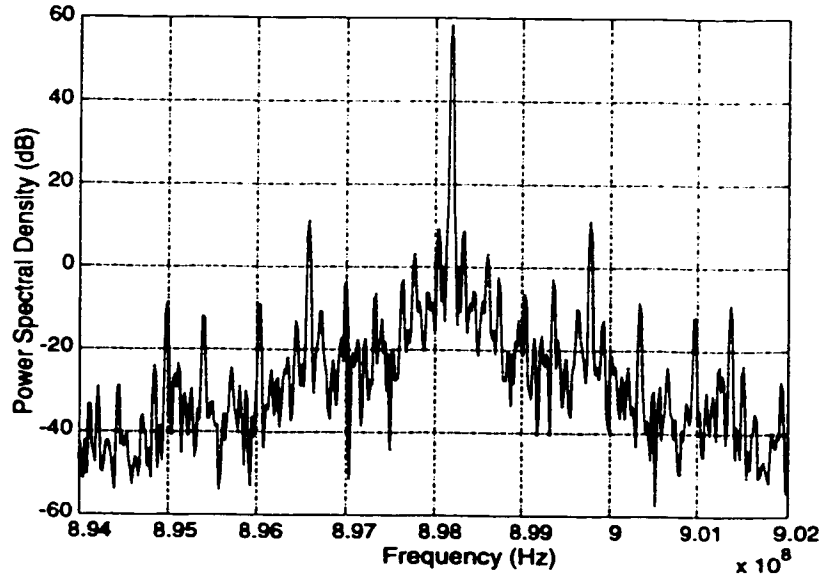


Figure 7.14: PLL output spectrum for an 8-bit DAC, and a second order timing error correction

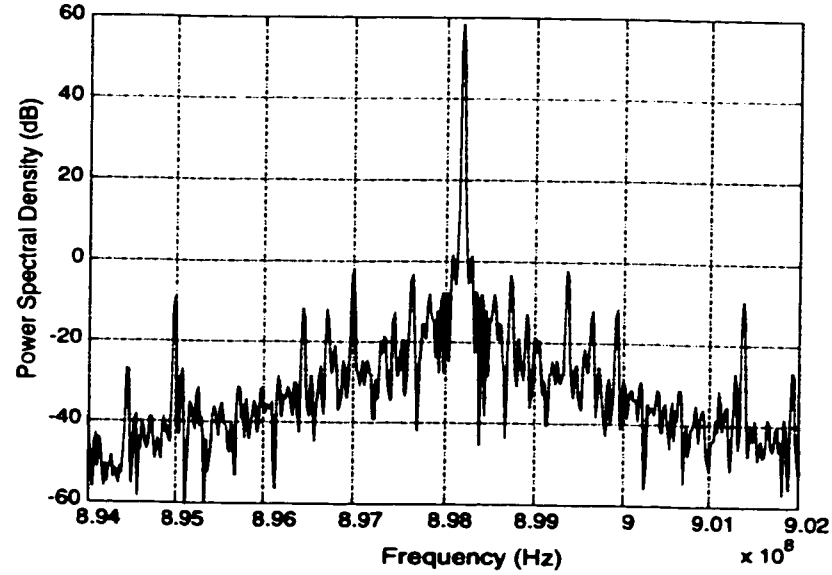


Figure 7.15: PLL output spectrum for a 9-bit DAC, and a second order timing error correction

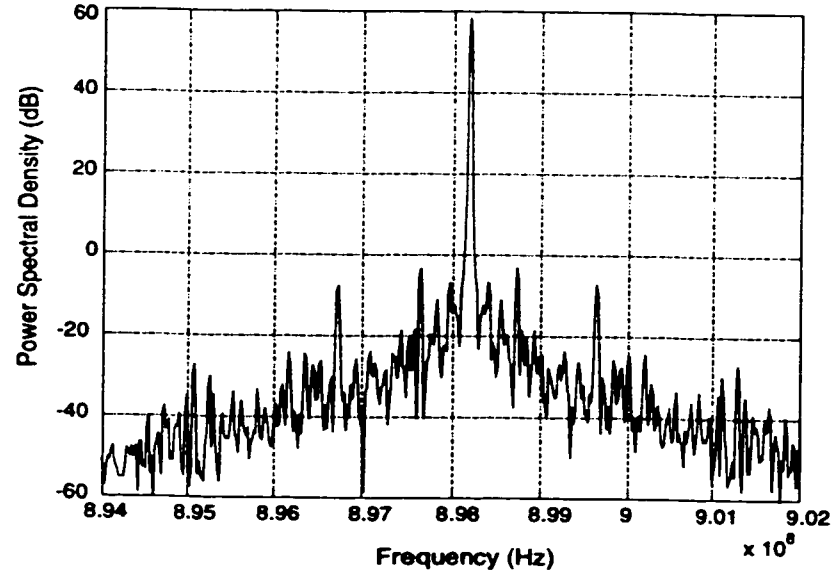


Figure 7.16: PLL output spectrum for a 10-bit DAC, and a second order timing error correction

nine, and ten-bits quantizers are illustrated in Fig. 7.14, Fig. 7.15, and Fig. 7.16, respectively. The spur level decreases from -50 dBc when an 8-bit DAC is used, to below -65 dBc when a 10-bit DAC is used. This number is sufficient for most cellular applications. Consequently, a 10-bit DAC seams to be enough for most complicated systems. Moreover, a smaller number of bits can be used for less demanding systems.

7.6 Conclusion

A numerical phase comparator is used to construct a fractional-N PLL frequency synthesizer, based on the weighted phase error concept. This architecture provides very fine channel spacing for a reasonably high reference frequency. The high reference frequency greatly reduces the effective division ratio thus, attenuating the in-band phase noise. Because of the high reference frequency the loop bandwidth could also be increased to increase the switching speed.

A novel timing error cancelation technique is used to remove the output spurs due to the delays in the digital phase comparator and its subsequent DAC. The output spur level is only limited by the DAC accuracy and its frequency is not related to the channel spacing. The frequency of the spur could be changed by changing the frequency divider ratio N_1, such that it does not fall on the blocking channel. Spur levels as low as -65 dBc could be achieved if a 10-bit DAC is used. Unlike the $\Sigma - \Delta$ technique the quantization noise does not increase at high frequencies. As a result a much larger loop BW is possible. The simulated switching time for a 900 MHz synthesizer with a 100 MHz frequency step is less than 7 μs.

Chapter 8

Conclusion and Future Work

Despite the great advent in the silicon fabrication technologies, the integration of the VCO remains a challenge for RF circuit designers. The reduction of the lithography sizes to the deep sub-micron range has provided designers with fast, high gain, active devices. However, the enhancement of integrated passive components; namely inductors and varactors, have been much slower. Partially, this is because the RF design is relatively new to the silicon technology. Another reason is that the task of improving these passive components is different in nature than improving the active ones. Due to the strong demand, many major technology providers are currently investigating various techniques for improving both the inductor and the varactor quality factor.

However, before an integrated VCO meets the stringent phase noise requirements with enough tuning range over all the temperature, supply and process variations is possible, two main process parameters has to be further improved. First, the quality factor of both the integrated inductor, as well as the varactor, has to

increase significantly. In addition, better control of the fabrication tolerance in the varactor values is very critical. Although, the effect of the Q factor on the phase noise is obvious, the effect of fabrication variance in the varactor value requires some explanation. The uncertainty in the varactor values mandates an extremely high VCO gain to cover for the resulting center frequency tolerances. The high VCO gain renders it very sensitive to supply, ground, and substrate noise. Until these two technology challenges are met, architectural variations both on the VCO design level, as well as that of the whole PLL system, remain the only way to achieve a fully monolithic frequency synthesizer. In this work, we have presented two techniques to improve the VCO noise using only the low Q wide tolerance integrated resonators. On the PLL system level, we have proposed a wide-band PLL architecture based on numerical phase comparison to relax the VCO phase noise requirements, and to enhance the frequency synthesizer performance.

The first technique reduces the high VCO sensitivity due to the varactor value inaccuracy by transforming the entire PLL into a fully differential design. A low noise OpAmp buffer is used to achieve the differential control for the LC VCO. This technique is not limited to a specific architecture, and can be used with any differential VCO structure. The OpAmp buffer is used to transfer one of the VCO differential control inputs to the common node between the differential inductors, without altering the VCO bias current. Thus, this control voltage is applied to the corresponding varactor terminals through the low DC impedance of the inductors. The common varactor terminal is directly connected to the second control input. Unlike other techniques, this architecture does not sacrifice the VCO tuning range.

It has been shown that through careful design of the OpAmp buffer, its noise contribution to the VCO phase noise can be less than half a dB.

We have also suggested [56] that the VCO sensitivity to both supply and substrate, can be further reduced in CMOS technologies by using PMOS transistors in the VCO core instead of NMOS transistors. The use of PMOS VCO core has been later adopted by many researchers.

The differentially controlled VCO architecture is configured in a fully differential PLL with a novel charge pump common mode correction architecture. The common mode correction is performed in an open loop manner using two crude voltage references, instead of the single clean one used in conventional architecture. This technique simplifies the reference design, and prevents the transfer of its noise to the charge pump output.

In a 0.5 μm CMOS technology, the differential PLL achieves an in-band noise of -96 dBc at 30 kHz offset from 1.2 GHz. This noise is achieved with a 25 MHz reference frequency, and a 13.6 mA current consumption from a 3 V supply. The VCO phase noise is -119 dBc at 1 MHz offset, and its tuning range is 26%. The differential VCO control provides 46 dB common mode rejection. The VCO output frequency changes by only 1.27 MHz, when the supply is changed from 2.5 to 3.5 V. This supply sensitivity is much lower than other single ended VCO's.

The second architecture presented in this work targets the reduction of the VCO phase noise. This design utilizes two coupled tanks to implement a transimpedance resonator with an effective Q factor close to twice that of a single low Q integrated resonator. This increase in the frequency selectivity may lead to significant reduc-

tion in the VCO phase noise. Another attractive feature for this transimpedance resonator is that it has a 90° phase shift between its input current and output voltage. This feature is used to further reduce the phase noise by cascading four such resonators in a ring VCO structure. This ring VCO architecture inherently provides accurate quadrature outputs, which are conventionally generated by cross coupling two identical oscillators. In essence, this VCO utilizes the extra power and area that are normally needed for quadrature output generation to significantly reduce the phase noise.

Full phase noise analysis of the VCO is presented and compared to that of the conventional cross coupled pair VCO's. For the same power consumption, a phase noise reduction of close to 4 dB is estimated. A prototype of the VCO has also been built in 0.35 μm CMOS technology. The measured phase noise is -122 dBc at 600 kHz offset from 1.93 GHz. This phase noise is significantly lower than other I-Q VCO implementations in the literature, and is comparable to those with single phase output. The VCO prototype draws 9.2 mA from a 3 V supply, and occupies a chip area of 1.1x1.1 mm^2. In this prototype the VCO has been designed with a single ended control to reduce complexity, but it can be easily transferred to the differential architecture outlined above.

Although, significant improvements in the noise performance of integrated VCO's are achievable using the above techniques, they remain insufficient to meet the stringent requirements of most wireless systems. The remaining part of the thesis concentrates on possible synthesizer architectural variations to relax the VCO noise requirements, by using wider band PLL's.

Currently, fractional-N division is the most popular way to achieve a wide band PLL. However, fractional spurs limit the achievable BW. Analog compensation techniques provide limited spur reduction, and allows only a few bits (2-4) of fractional resolution. $\Sigma - \Delta$ techniques transfer the fractional spurs to high frequency quantization noise, permitting a wider BW and an unlimited fractional resolution. Because of the quick rise in the quantization noise of the high-order multi-bit $\Sigma - \Delta$ modulators used, the PLL BW is limited to 30 or 40 kHz to suppress this noise. In order to further increase the loop BW, the multi-bit output of the $\Sigma - \Delta$ modulator can be used to drive the fraction inputs of an analog compensated fractional-N PLL to perform a sub-fractional division. The power of the resulting quantization noise in this case is much lower, due to the reduced excursions of the instantaneous division ratio. Because of the systematic error associated with charge injection analog compensation techniques, the circuit implementation of a digitally controlled delay analog compensation technique is attempted. This techniques has been recently proposed and is claimed to eliminate the systematic errors in the spur compensation. However, no circuit level implementation has been reported.

The digitally controlled delay analog compensation techniques is based on introducing a delay after the fractional divider that is equivalent to the instantaneous phase error introduced by the divider. Several current controlled delay cells are cascaded, and the number of those which are added to the loop is digitally controlled by the contents of the fractional division accumulator. To provide the correct value for the single delay cell, a DLL is used to lock those delays to the VCO output. The detailed circuit level implementation of this technique is pursued. From the

circuit simulations, fractional spur levels as high as -57.8 dBc are observed. These spurs are attributed to the strong coupling between the main PLL and the spur cancelation DLL. Any spur in one of the loops results in a corresponding spur in the other loop, which in turn causes another spur in the first loop, and renders the full spur cancelation impossible. Despite its negative indication, we believe that this result is important for many researches in the field of fractional-N PLL's.

Finally, the fractional-N frequency synthesis is taken one step further by proposing a synthesizer architecture that performs the fractional division in the phase domain. A numerical phase comparator is used as a *Weighted Phase Frequency Detector* . The resulting synthesizer can achieve high switching speeds, and a narrow channel spacing. The output spur level is limited by both the delay of the numerical phase comparator, as well as the accuracy of the DAC used to convert its phase error output to the analog domain.

A novel timing error cancelation scheme that is capable of eliminating the effect of the phase comparator delays is presented. Using this technique and a 10-bit accuracy DAC, the simulated spur level is as low as -65 dBc. Unlike direct digital frequency synthesis (DDFS) techniques, the output frequency is not limited by the DAC speed. Another important feature that simplifies the DAC design is that its desired analog output is a current rather than a voltage as in the DDFS case. In addition, this architecture has also a major advantage over the $\Sigma - \Delta$ techniques; no high frequency quantization noise is produced, and the loop BW is limited by only the required input reference spur suppression.

There are several areas of extension for this work. An obvious and a very

challenging task is to take the weighted phase synthesizer architecture one step further to the circuit implementation. With the many issues outlined, and solutions proposed, this is the natural next step. Careful frequency planing through further system level simulations and analysis is also critical for a successful circuit implementation.

Another area of improvement is the redesign of the differential PLL such that dominant pole of the OpAmp buffer is at its output. Although this is not easy to achieve without much degradation in the buffer BW, it could be a significant addition to the differential VCO control. The substrate and supply noise at frequencies higher than the buffer BW is suppressed by the low pass response of the buffer. Furthermore, the loop filter can be connected at the buffer output, instead of its input, to further reduce the effect of the buffer noise.

We believe that there is a room for improvement in the coupled tank VCO phase noise through further optimizations using phase noise simulation tools (for example, SpectreRF) that were not available at the time of the circuit design. The use of magnetic coupling instead of the capacitive and the implementation in Bipolar technologies are other possible research areas.

Finally, the combination of the two VCO architectures into a single low phase noise differentially controlled VCO may be attempted. This VCO can eventually be configured in the wide-band weighted phase fractional-N PLL, a reasonable solution to the synthesizer integration problem.

In conclusion, this research has advanced the state-of-the-art in the area of monolithic frequency synthesizers through the following contributions:

- Developing a novel I-Q VCO architecture that utilizes the extra power and area needed for the quadrature output generation to reduce the phase noise using coupled tank resonators [85].

- Presenting a new, power efficient technique to reduce the sensitivity of the high gain integrated VCO to both supply and substrate noise through differential control. This technique does not sacrifice neither the phase noise nor the tuning range of the VCO [56, 86, 87].

- Proposing the use of a numerical phase comparator in a weighted phase error fractional-N PLL that breaks the tradeoff between the PLL speed and spur levels through the use of a novel timing error correction scheme [88].

- Providing a detailed understanding, through a full circuit design and analysis of the limitations of digitally controlled delay spur compensation techniques in fractional-N frequency synthesis.

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Publications Resulting From This Research

1. Ayman Elsayed and Akbar Ali, "An LC-VCO, Charge-pump and Loop-filter Architecture for improved noise-immunity in integrated Phase-locked Loops," US patent pending, Dec. 1996.

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