High Efficiency CMOS Power Amplifiers for Drain Modulation Based RF Transmitters

by

Mohammad Reza Ghajar

A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Master of Applied Science
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2009

©Mohammad Reza Ghajar 2009

AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Mohammad Reza Ghajar

Abstract

The rapid evolution of wireless communication technologies increased the need for handheld devices that can support dissimilar standards or better user mobility and more battery life. Traditional radio architectures fail to satisfy these challenging features. Software Defined Radio (SDR) is recently introduced to implement a new generation of wireless radios capable of coping with these stringent requirements through software reprogramming. Although the term SDR is widely used, it is still an idealized method and is not implementable using available technologies. Hence, the term "SDR", has been so far, referring to only partially upgradeable radios. Two current practical solutions substituting SDR are broadband and multiband transceivers.

Radio Frequency (RF) front ends and especially the power amplifier is the main challenge in implementation of software defined radios. Power Amplifiers (PA) dominate the sources of distortions and power consumption in the RF-front end. They are typically operated in linear classes in order to minimize the linearity degradation. However, they lead to poor average power efficiency especially when fed with signals with high Peak to average power ratio (PAPR) such as Wideband Code Division Multiple Access (W-CDMA) and Long Term Evolution (LTE) signals. This is the main cause of short battery life in transceivers. To remedy this issue, some advanced methods like Doherty amplifier and drain modulation based architectures are introduced.

This thesis expounds on the implementation of high efficiency radio transmitters, capable of multi standard operation. The RF amplifier is still one of the main challenges in the realization of these transmitters. In this work, two RF PAs, having multiband and broad band characteristics, were implemented using 0.13µm CMOS technology. The first PA operates at two frequency bands, 2.4GHz and 3.5GHz. The other PA has center frequency equal to 2.4GHz and 600MHz bandwidth, respectively. These PAs are expected to lay the foundation for the realization of high efficiency drain modulation based multiband and broadband transmitters.

Acknowledgements

I would like to start by giving thanks to my father, mother and sisters for their unconditional support while I was away from home for the first time.

I would like to give my thanks to Dr. Boumaiza for his astonishing help during my studies at the University of Waterloo. I could not forget mentioning his efforts in making friendly and collaborative environment in his laboratory. I had the opportunity of working with Hassan Sarbishei and Daniel Febrowski who are extraordinary in teamwork. I also enjoyed having the company of Farouk Mokaddem, David Wu, Aynaz Vatankhah and Dylan Bespalko.

Certainly, I could not finish this marathon without having support of my friends, especially Afsaneh, Khorzoo and Ehsan.

Table of Contents

Author's Declaration ii
Abstract iii
Acknowledgements iv
Table of Contents v
List of Figures vii
List of Tables x
List of Abbriviations xi
Chapter 1 Introduction 1
1.1 Power Amplifier Figure of Merits 4
1.2 High Efficiency Power Amplifiers 7
1.2.a Linear classes of Power Amplifiers 7
1.2.b Switching Mode Power Amplifiers 10
1.2.b.1 Class D Operation 11
1.2.b.2 Class E Operation 13
1.2.b.3 Drain Modulation Based RF Transmitters 16
1.3 Transistor Device Choices 18
1.3.a CMOS Technology 19
1.3.b GaN High Electron Mobility Transistor 22
1.4 Discussion 25
Chapter 2 High Efficiency Class E Power Amplifier using Packaged GaN device 27
2.1 Choosing Class of Operation 27
2.2 Class E Amplifier Design Procedure 28
2.3 Measurement Results 32
2.4 Discussion 35
Chapter 3 Concurrent Dual Band RF Power Amplifier in 0.13µm CMOS Technology 36
3.1 Power Amplifier Design for in CMOS Technology 36
3.2 Proposed Dual Band PA architecture 37
3.3 Simulation Results 40
3.4 Discussion 43
Chapter 4 High Efficiency Broadband Integrated Power Amplifier 44

4.1 Design Procedure 44
4.1.a DC Characterization 44
4.1.b Load/Source Pull Simulation 45
4.1.c Matching Network Design 48
4.1.d Parameter Sweep 49
4.1.e Passive Components 51
4.2 Simulation Results 52
Conclusion and Future Work 57
References 59

List of Figures

Figure 1.1: Multiband Reconfigurable Transceiver 2
Figure 1.2: Power Amplifier block diagram 4
Figure 1.3: Power Gain versus Output power 5
Figure 1.4: An example of measured power amplifier output spectrum 6
Figure 1.5: Output spectrum of Intermodulation products 6
Figure 1.6: Class A amplifier 7
Figure 1.7: The quiescent bias point on the transistor transfer characteristic 8
Figure 1.8: PA efficiency vs class of operation 9
Figure 1.9: Inverse Class F Amplifier 9
Figure 1.10: Class F drain waveforms 10
Figure 1.11: Class D amplifier 11
Figure 1.12: Class D amplifier voltage and current waveforms 12
Figure 1.13: Class E amplifier with lumped elements matching network 13
Figure 1.14: Simplified class E amplifier 14
Figure 1.15: Class E efficiency vs load resistance 15
Figure 1.16: Power Added Efficiency vs Output power 16
Figure 1.17: Polar transmitter 17
Figure 1.18: Device availability for different frequencies and power levels 19
Figure 1.19: NMOS cross sectional 20
Figure 1.20: NMOS parasitic, cross sectional view 21
Figure 1.21: NMOS small signal model 21
Figure 1.22: GaN HEMT cross-section 23
Figure 1.23: GaN and AlGaN bandgap differences 23
Figure 1.24: Multi/Borad-Band Polar Transmitter 25
Figure 2.1: GaN transistor DC characteristics 28
Figure 2.2: Loci of lumped elements matching network's impedances on the Smith chart ... 29
Figure 2.3: Loci of load and source impedances versus frequency 30
Figure 2.4: Layout view of the Designed Matching Network 31

Figure 2.5: Drain voltage and current of Class E PA 31
Figure 2.6: Photograph of implemented Class E 32
Figure 2.7: Measured Drain Efficiency (DE), PAE and Output Power vs Input Power......... 33
Figure 2.8: Measured Gain and PAE versus Input Signal Frequency 33
Figure 2.9: Output Spectrum at the maximum input power 34
Figure 2.10: Measured PAE and Pout vs VDD 34
Figure 3.1: Traditional Multi-Band PA Topology. 37
Figure 3.2: Proposed Dual Band PA Architecture 38
Figure 3.3: (a) Output matching network at 3.5 GHz (b) Output matching network at 2.4GHz (c) simplified circuit at 3.5GHz (d) simplified circuit at 3.5GHz 39
Figure 3.4: Third frequency operation of the matching network 39
Figure 3.5: Dual Band PA Layout view 40
Figure 3.6: (a)Output Reflection Coefficient of the Dual Band PA(b)Power Gain of the PA 41
Figure 3.7: AM/AM Characteristic of the Dual Band PA Assessed at 2.4GHz/3.5 GHz 42
Figure 3.8: Power Added Efficiency of the Dual Band PA Assessed at 2.4GHz/3.5GHz 42
Figure 3.9: Power Added Efficiency of the Dual Band PA versus supply voltage 43
Figure 3.10: Output matching at 830MHz 43
Figure 4.1: NMOS DC characterization 45
Figure 4.2: PA schematic 46
Figure 4.3: Source/Load Pull Simulation Setup 46
Figure 4.4 Loci of input, output matching network impedances on Smith chart.................... 48
Figure 4.5: Same Impedance Transformation using Different Inductor and Capacitor values49
Figure 4.6: Designed PA using Load/Source Pull simulation 49
Figure 4.7: Parameter sweep. (a) PAE vs Lfeed and C1 (b) PAE vs L1 and C2 50
Figure 4.8: Square spiral inductor 51
Figure 4.9: Q-factor and inductance vs frequency 52
Figure 4.10: S_{11} and S_{22} versus frequency 52
Figure 4.11: Output power versus input power 53
Figure 4.12: Gain versus input power 53

Figure 4.13: PAE, DE versus input power 54
Figure 4.14: Time domain voltage and current at drain 54
Figure 4.15: Output power Spectrum versus frequency 55
Figure 4.16: Power gain, PAE and DE vs supply voltage for constant input power 55
Figure 4.17: Output power versus supply voltage at constant input power 56
Figure 4.18: PAE and Gain versus Frequency 56

List of Tables

Table 1-1 Efficiency comparision of classes of operation 15

Table 1-2 Enabling Features of Galluim Nitride 24

Table 3-1 Values of Dual Band Matching Network elements 40

List of Abbreviations

SDR: Sotware Defined Radio iii
RF: Radio Frequency iii
PA: Power Amplifier iii
MN: Matching Network 3
FPGA: Field Programable Gate Array 3
DSP: Digital Signal Processeor 3
PAE: Power Added Efficiency 3
DE: Drain Efficiency 3
G: Power Amplifier Gain 4
IMN: Input Matching Network 7
OMN: Output Matching Network 7
f_{max}: Maximum Frequency 14
EER: Envelope Elimination and Restoration 17
ET: Envelope Tracking 17
BW: BandWidth 17
HBT: Hetrojunction Bipolar Transistor 18
BST: Base-Station 18
HEMT: High Electron Mobility Transistor 22
HFET: Heterojunction Field Effect Transistor 22
ADS: Advanced Design System 30
PCB: Printed Circuit Board 35
MIMCAP: Metal Insulator Metal Capacitor 51
EM: ElectroMagnetic 51

Chapter 1
Introduction

Wireless networks growth so rapidly and each year new applications are introduced. As a result of this, wireless endusers request for low cost sophisticated radio systems that can support multi applications operation while having long battery life. Addressing these conditions at design level, we have to design radio transceivers

(i) using low cost technologies such as CMOS
(ii) that be very energy efficient
(iii) that be multicarrier, capable of operating at more than one frequency at a time. These frequencies can fall either within the same operation band or into different bands for the multiband radio case.
(iv) that processes several types of standards (multimode) These modes may even need to be run simultaneously in the case of a multicarrier radio.

Knowing that traditional radio architectures fail to satisfy last two features, Software Defined Radio (SDR) is recently introduced to implement a new generation of wireless radios capable of coping with these stringent requirement through software reprogramming. Although the term SDR is widely used, its development has been limited to the investigation of software-based signal processing techniques to satisfy the previously mentioned multi-rate and multimode characteristics. Advances in digital signal processing techniques and digital signal processors' processing power has led to powerful base-band processors, which are capable of supporting a wide variety of modulation schemes and protocols. Hence, the term "SDR", has been by far, referring to only partially upgradeable radios. This is mainly attributed to the inability of most conventional radio architectures to handle a wide spectrum of frequencies. To remedy this limitation, especially in the case where multiple frequencies of operation are desired, the partially upgradeable radios designers have been utilizing multiple parallel RF front-ends as shown in Figure 1.1.

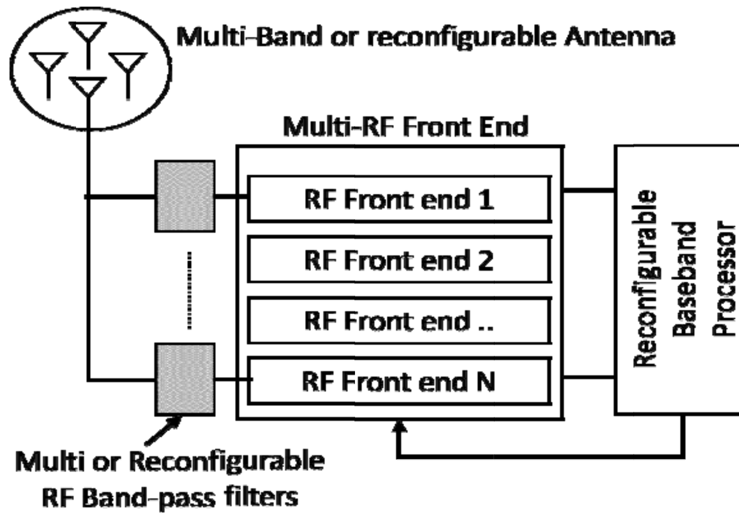


Figure 1.1: Multiband reconfigurable Transceiver

Each one is constructed using static analog/RF circuits including antennas, filters, amplifiers and mixer which are designed for a specific range of frequencies. Hence, current software upgradeable radios meet the multiband requirement; however, their design is not implemented in an efficient way. To adapt the hardware to the targeted standard, a switch command that changes the hardware connections between the RF front-ends and the reconfigurable baseband processor part is being used. Because the building blocks cannot be reused, such radio configurations suffer from increased size, power consumption and bill-of-material. A truly SDR optimizes the size and cost of current multiband multimode radios by utilizing only one RF front-end instead of the parallel paths.

Although truly SDR radio is conceptually simple and convenient, its development poses stringent technological challenges. The baseband processing of a radio system assumes the multimode capability with relatively moderate design constraints. However, it is at the RF front-end stage that it becomes problematic to satisfy the multiband features. Recently, the technological issues related to the development of multiband receivers have been widely investigated [17], [18], [19]. On the other hand, very few R&D initiatives have been geared towards the design of multiband or broadband transmitters.

An example of the new methods used in multiband transmitters is reconfigurable band-switchable matching networks (MN) have been proposed for the design of band-free RF circuits. These circuits employ Single-Pole-Single-Throw (SPST) MicroElectro-Mechanical Systems (MEMS) switches in the MNs to maintain excellent performance levels over multiple bands. Alternatively, electronically tunable devices such as varactors, PN diodes, RF-MEMS, and ferroelectric material have been employed to develop adjustable capacitors and/or inductors, which have enabled the creation of reconfigurable MNs and band-free RF circuits. Despite the fact that various attributes have been achieved in these adjustable devices, a number of serious limitations remain unresolved such as easy integration, high control voltage range. In addition, in the instance where the radio is required to simultaneously operate at multiple frequencies, the band-switchable or tunable MNs designed as a multiband RF circuit strategy are not adequate. To address this major limitation, multimode RF circuitry which includes broadband or multiband matching networks, can be used in the development of multiband radios. So many attempts have been done to investigate these transmitters, but still designing its power amplifier remains a big challenge.

On the other hand, the RF PA is the most power hungry block in the wireless transmitter. It dissipates more than 55% of total power consumption of a transmitter, therefore its efficiency has the major effect in battery life. It also directly affects the quality of transmitted signal. Early RF PAs were only made with microwave components. But recent developments in communication standards and fabrication technologies have increased the demand for the more advanced and complicated PAs. Today, power amplifier is a complex mixture of signal processors, such as Digital Signal Processor (DSP) or Field Programmable Gate Array (FPGA), analog blocks such as amplifiers, regulators and comparators, and RF transistor and passive component. Therefore PA design requires a good understanding of microwave, analog and signal processing and system level concepts. This thesis is mainly focused on microwave design of power amplifier, which remains a major challenge in this field.

There are different parameters to consider in evaluating the performance of a power amplifier. Among them Power Added Efficiency (PAE), Drain Efficiency (DE), 1-dB compression point, harmonic suppression, bandwidth, gain, AM/AM and AM/PM

characteristics, are the most widely used. To have a better understanding of the PA performance, we will first discuss these Figures of Merit (FoM).

1.1 Power Amplifier Figure of Merit

Large amount (more than 60%) of total consumed power in any radio transmitter is devoted to Power Amplifiers [24]. Therefore in evaluating different PAs, the efficiency is always a critical factor. It characterizes the effectiveness of the DC-to-RF power conversion of the PA [4]. It is a measure of amount of power that is dissipated as heat. The low efficiency PAs, require special heat management and imply high electricity cost. They also significantly compromise the reliability and life time of the whole transmitter.

Figure.1.2 shows the block diagram of a power amplifier. The ratio of the fundamental RF power delivered to the load, RL, (P_{LOAD}) to the DC power steered from the VDD, supply voltage, (P_{DC}) is called Drain Efficiency (DE) which depicted in equation (1-1).

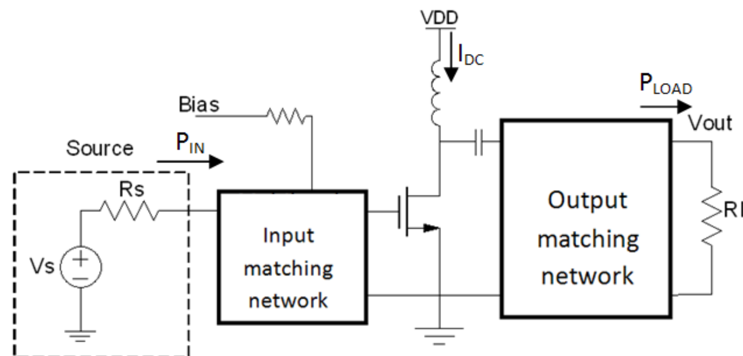


Figure 1.2: Power Amplifier block diagram

$$DE = \frac{P_{LOAD}}{P_{DC}} = \frac{P_{LOAD}}{I_{DC} \times V_{DD}} \quad (1\text{-}1)$$

Transistor has a limited gain (G) which drops at high frequency. Therefore a more inclusive definition for power efficiency should also include the effect of input power (P_{IN}). Power Added Efficiency (PAE) was introduced as Equation (1-2). PAE is always less than DE.

$$PAE = \frac{P_{LOAD} - P_{IN}}{P_{DC}} = \frac{P_{LOAD} - P_{IN}}{I_{DC} \times V_{DD}} = \frac{P_{LOAD}}{I_{DC} \times V_{DD}}\left(1 - \frac{1}{G}\right) = DE\left(1 - \frac{1}{G}\right) \quad (1\text{-}2)$$

Transistor gain is highly dependent on the drain current, and at high power it drops quickly. This behavior causes nonlinearity. This is one of the major problems of power amplifiers, because it directly affects the signal integrity required by wireless standard. Figure 1.3 shows a generic nonlinear behavior of power amplifier. 1-dB compression point is noted on the plot. It is defined as the point where the gain drops by 1 dB compared to the small signal gain.

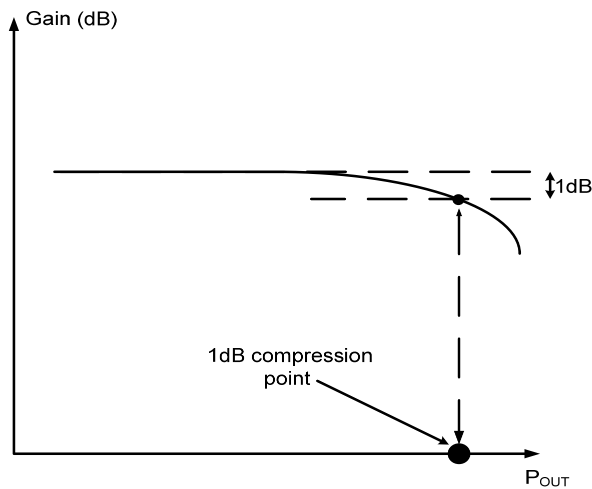


Figure 1.3: Power Gain vs Output power

Transmitted signal out of PA should satisfy both good in-band signal quality and low out of band harmonics emission. Second and third harmonics suppression characterizes the PA nonlinearity and its out of band emission. It is defined as the ratio of power delivered to load at second or third harmonic to power at fundamental frequency while applying a single tone at the input. Figure 1.4 is an example of a measured output spectrum of a PA. Second and third harmonics suppression level are also marked on the plot.

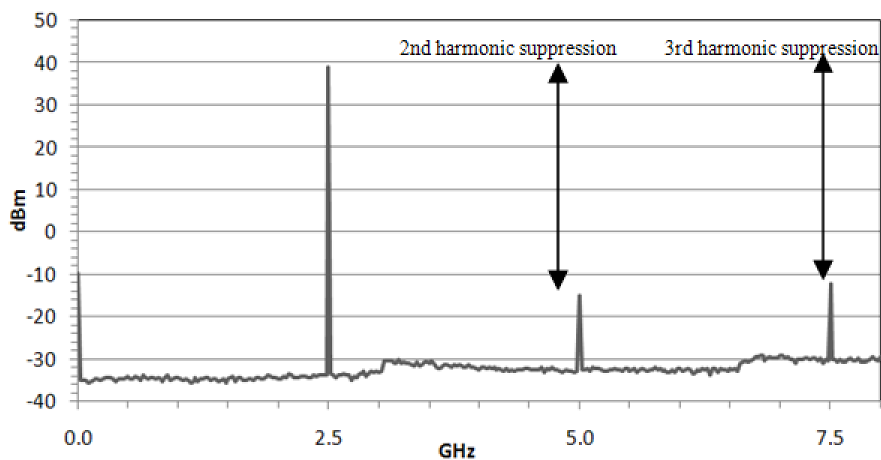


Figure 1.4: An example of measured power amplifier output spectrum

Inter-modulation distortion is another consequence of the PA nonlinearity. In many applications, modulated signal has wide bandwidth and PA nonlinearity introduces new distortion products which fall inside the signal bandwidth. An easy way for characterizing this form of distortion is the measurement of the PA's output signal under Two Tone signal. If two sinusoidal signals, with frequencies equal to f_1 and f_2, are injected at the input of a nonlinear amplifier, the output signal contains additional frequency components called inter-modulation products. Figure 1.5 shows the generation of third-order inter-modulation products [4]. Besides the input signal harmonics, the amplifier generates new frequencies located at nf_2-mf_1 where m and n are integers. Among these products, $2f_2$-f_1 and $2f_1$-f_2, called third order inter-modulation products, are usually the most critical as they may fall within the channel bandwidth and interfere with the signal of interest [4]. The inter-modulation distortion to carrier signal power ratio is usually measured and used to characterize the PA nonlinearity.

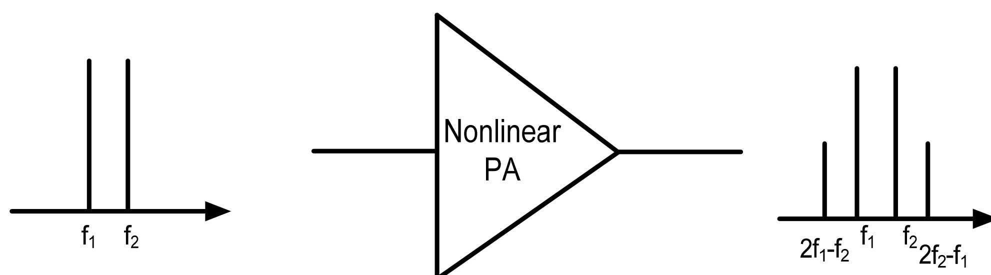


Figure 1.5: Third Order Inter-modulation products

A great deal of efforts has been employed to design high efficiency power amplifier satisfying the required linearity on the transmitter side. Different classes of operation and more advanced transmitter architecture were developed. Following section discusses some of these classes and some advanced topologies like polar transmitter and its derivatives.

1.2. High Efficiency Power Amplifiers

1.2.a Linear classes of power amplifiers

Depending on biasing and matching network topology, different classes of operation exist. Each has its trade off between linearity and efficiency. Among them class-A is the simplest one. It is the most linear PA but least efficient compared to other classes. Figure.1.6 shows the schematic of a class-A amplifier including input and output MNs, (IMN and OMN). I_{DC} is the transistor quiescent current.

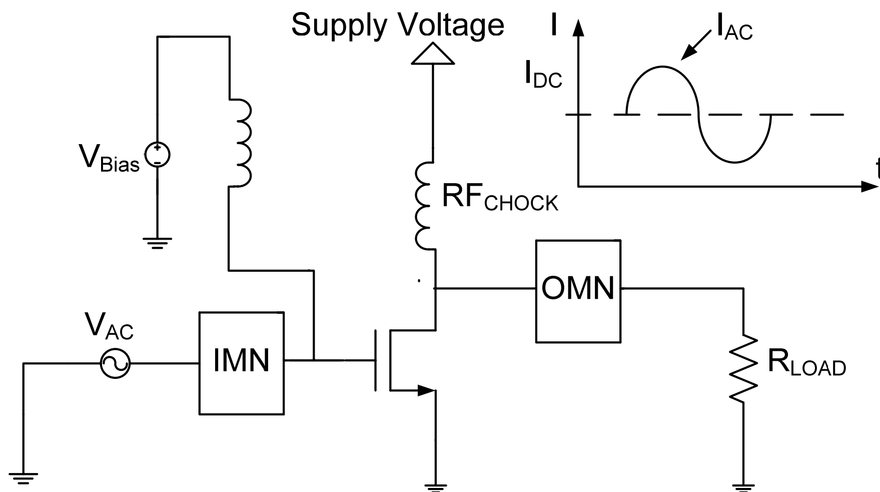


Figure 1.6: Class A amplifier

The main assumption in class-A design is that the bias levels are chosen so that the transistor operates in the linear region and has 360 conduction angles [6]. This condition implies that the transistor passes the entire waveform at the input to the output. In theory, class A does not add any distortion to signal, but in practice the amplifier gain is highly depends on DC current, and the current is a function of gate effective voltage. So large signal swing at gate or base causes gain variation which is a source of distortion.

The matching network between drain and load has an inherent filtering effect which improves the linearity. It also converts the load impedance, 50 Ohm in most of the cases, to the desired impedance at the drain. Maximum output power (Pout) is given in Equation (1-3)

$$P_{MAX} = \frac{V_{DD}^2}{2 \times RL_{OPT}} \tag{1-3}$$

This shows that the maximum output power depends on supply voltage and the impedance presented to the transistor by the matching network. Operating in class A region the best efficiency is achieved by choosing the DC current (I_{DC}) equal to the RF signal amplitude (I_{RF}). Equation (1-4) shows class A drain efficiency under the above conditions.

$$DE = \frac{P_{out}}{P_{DC}} = \frac{I_{RF}^2(R_{opt}/2)}{I_{RF}V_{DD}} = \frac{I_{RF}(R_{opt}/2)}{V_{DD}} \xrightarrow{Max\ I_{RF}R_{opt}} DE = 50\% \tag{1-4}$$

Based on the above formula, to improve the efficiency, the DC current has to be decreased. One method is to decrease the conduction angle of waveform which unfortunately distorts the output signal. Deviating from 360 degree conduction angle changes the class of operation from class A to class AB, B, C, with better efficiency. Figure.1.7 notes different classes of operation depending on quiescent current (I_D). Vgs is DC voltage across transistor gate. Also their efficiency versus conduction angle is plotted in Figure.1.8.

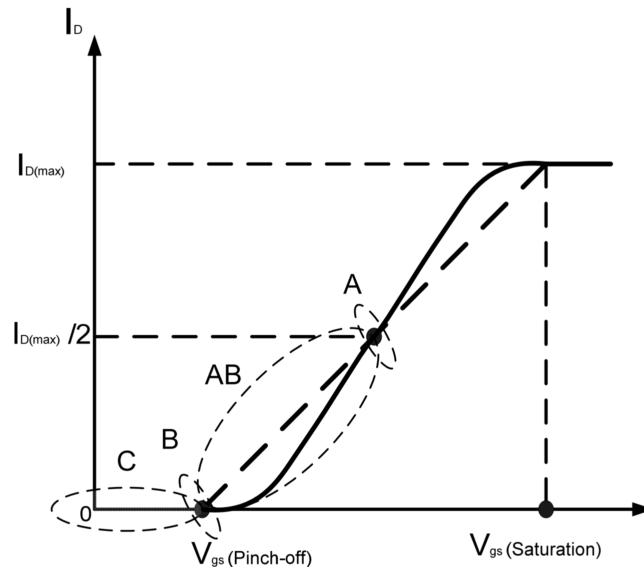


Figure 1.7: The quiescent bias point on the transistor transfer characteristic [4]

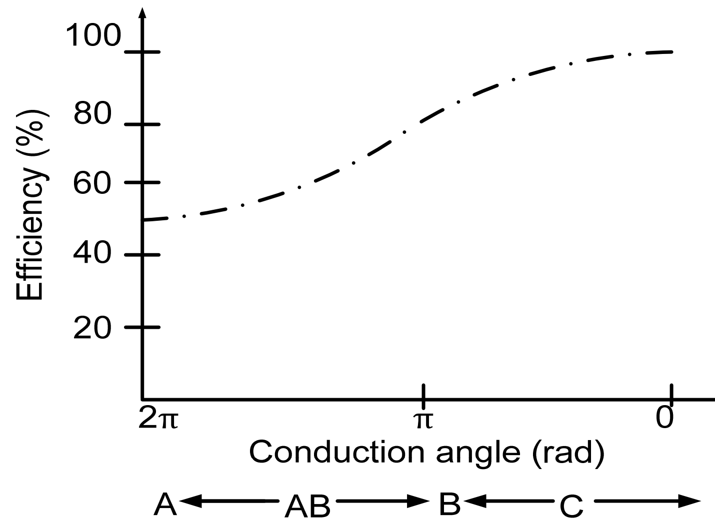


Figure 1.8: PA efficiency vs class of operation

Class C gives the highest efficiency at the cost of significant nonlinearity. Efficiency improvement is also possible with the proper design of matching network. Class F, F^{-1} are the examples of very energy efficient amplifiers which are designed based on output matching network and waveform engineering.

Class F/F^{-1} are designed based on harmonic tuning at the load. An example of inverse class-F circuit is shown in Figure 1.9.

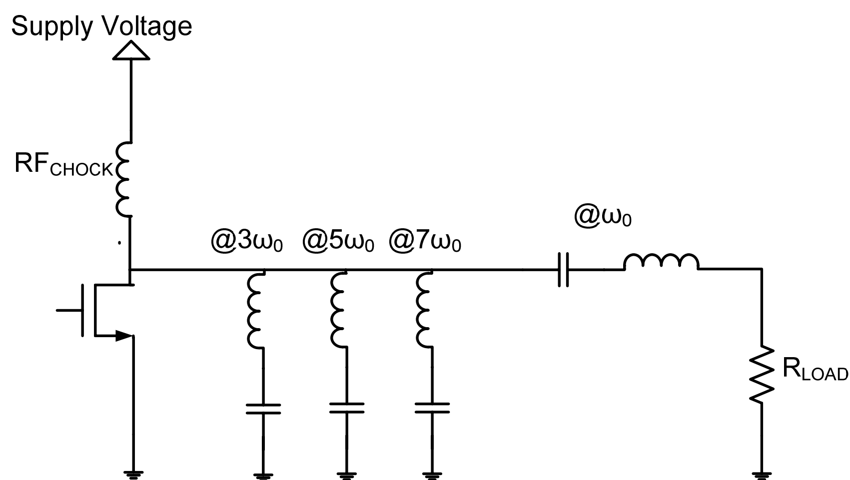


Figure 1.9: Inverse Class F Amplifier

The series LC resonators at the drain act as short circuit at odd harmonics of the center frequency (ω_0). For infinite number of resonators, the drain voltage waveform consequently appears ideally as (half) sinusoid and current waveform as a square wave [6]. Example of a voltage and current waveform at the drain/collector of an ideal inverse class-F amplifier is shown in Figure 1.10. 100% efficiency is ideally achievable. In practice, due to transistor parasitic and finite quality factor of matching component and finite number of resonators this value degrades more than 15%. The factor also depends on the device technology and fabrication process and materials used.

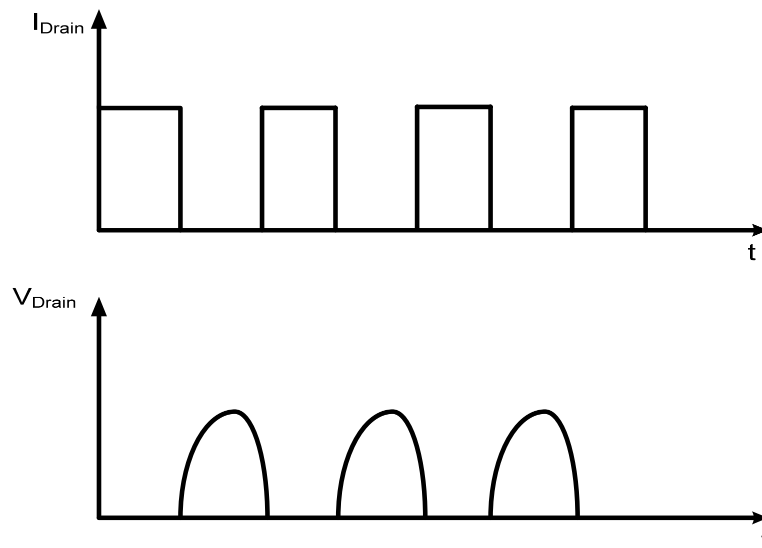


Figure 1.10: Class F drain waveforms

1.2.b Switching mode amplifier

Linear amplifiers like class A, AB, B or C are designed based on current amplification of transistor which is acting as voltage dependent current source. Unlike these classes, in switched mode PAs the transistor is operating as a switching having two states, ON or OFF. In theory they can achieve 100% efficiency by satisfying the following condition; when the transistor is turned ON, the voltage across the switch is almost zero, and high current is flowing through the device. In other words, the transistor acts as a low resistance (closed switch) during this first part of the period. When the transistor is turned OFF, current through the switch is zero, and a high voltage

is applied across the device, i.e. the transistor acts as a high resistance (open switch) during the other part of period [15]. For this reason, SMPAs such as classes D, E are inherently nonlinear but highly efficient. All these classes ideally achieve 100% power efficiency with nonzero output power [4].

1.2.b.1 Class D operation

In class D the active devices introduce either rectangular voltage and sinusoidal current waveforms or rectangular current and sinusoidal voltage waveforms. Figure 1.11 shows the complementary voltage and current switching class D PAs with input and output waveforms [1]. In this topology, the input connection guarantees that only one transistor is driven at a given time, with one transistor handling the positive half-cycles and the other handing the negative half-cycle just as in push-pull class B [6]. A parallel-turned output network (C_0 and L_0) converts the rectangular waveform back into a sinusoidal load voltage or current by cancelling the harmonics. This structure of the class D PA provides high output power. Voltage and current at the gate and drain of transistor is also plotted in Figure 1.12 [1].

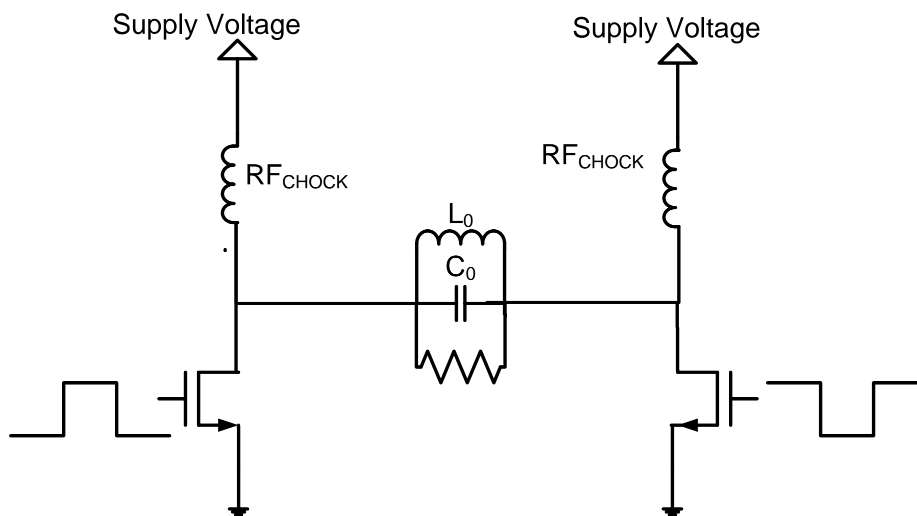


Figure 1.11: Class D amplifier

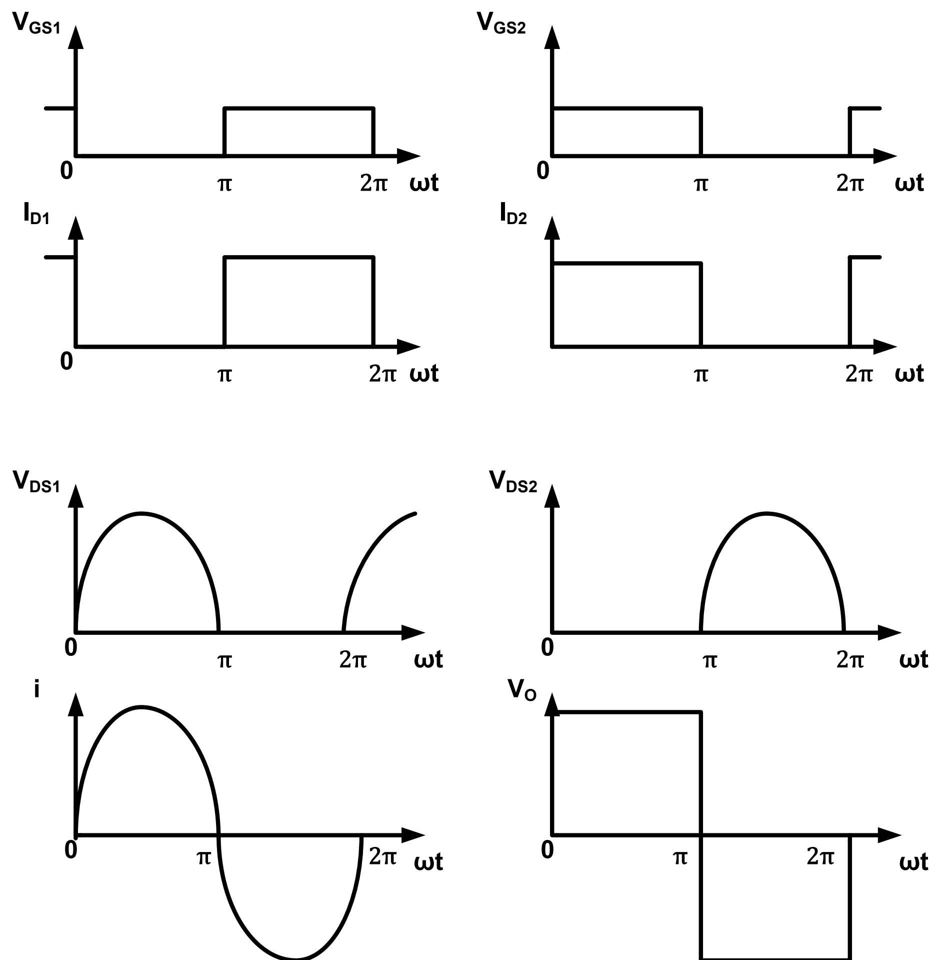


Figure 1.12 Class D amplifier voltage and current waveforms

In practice Class D suffers from some problems that degrade the efficiency. Like any other classes of operation, transistor parasitic and its low drain-source resistance cause DE drop by more than 10%. Also any digital (switching) circuit has some losses which are proportional to switching frequency. Equation (1-5) shows how loss is related to circuit values, where f is switching frequency, C is device capacitor and V is the supply voltage.

$$P_{Loss} \propto fCV^2 \tag{1-5}$$

This equation implies that class D is more appropriate for low frequency applications like audio amplifier, etc.

As indicated in Figure 1.10 class D needs a balun at the input and output to convert single ended signal to differential and vice versa. However it is very difficult to get exact 180 degree phase shift out of the balun. The balun also introduces extra sources of loss, thus decreasing the efficiency and making the design more narrow band.

1.2.b.2 Class E operation

In the Class D example we saw that switched mode amplifiers are capable of providing very high efficiency. Class E is another example of high efficiency switching mode power amplifiers. It solves some problems exhibited by class D amplifiers. Unlike class-D which requires differential input and two transistors, it is designed based on single ended operation and does not need balun or transformer at the input or output. In class D amplifier, at high frequency, the transistor cannot perform perfect switching, which degrades the performance. Class E has higher order matching network, therefore it has control on the voltage and current waveforms. In this way, better efficiency is achievable at high frequency [1].

Two class E amplifiers are discussed in this thesis; hence we will discuss it in more details. Let's take a look at the simplest form of class E topology sketched in Figure 1.13.

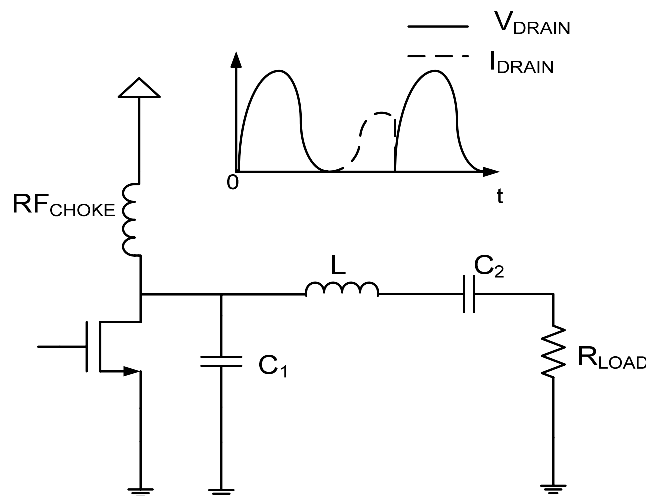


Figure 1.13: Class E amplifier with lumped elements matching network

The RF choke provides a DC path to supply voltage and has very high impedance at high frequency. High efficiency is achievable under zero voltage switching (ZVS) condition. Figure 1.14 shows a simplified class E. The transistor is replaced with a switch and the inductor is split into two inductors L_a and L_b. (L_a-C) resonates at desired center frequency.

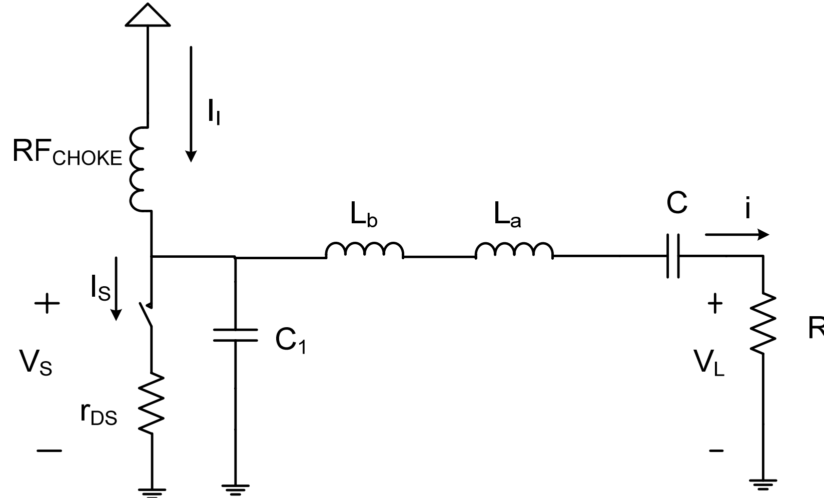


Figure 1.14: Simplified class E amplifier

Referring to the "RF power amplifier" book [1], section 5.6.4, satisfying the ZVS condition results in the following formulas for the inductor and capacitors.

$$C_1 = \frac{8}{\pi(\pi^2 + 4)\omega R} = \frac{0.1836}{\omega R} \tag{1-6}$$

$$L_b = \frac{\pi^2 - 4}{2(\pi^2 + 4)\omega^2 C_1} \tag{1-7}$$

$$P_o = \frac{V^2}{R}\frac{8}{(\pi^2 + 4)} \tag{1-8}$$

Class E operation is not guaranteed for the whole frequency range. There is a maximum frequency (f_{max}) of operation written as:

$$f_{max} = 0.05066\frac{P_o}{V^2 C_o} \tag{1-9}$$

As equation (1-8) shows, the class E output power (P_o) depends on load resistance R. Lower resistance gives higher output power. On the other hand, efficiency goes down as the

resistance decreases. Besides the analyses which are only valid for class E operation, higher impedance transformation results in higher loss in matching network [10]. Figure 1.15 plots the relation between class E efficiency and load resistance.

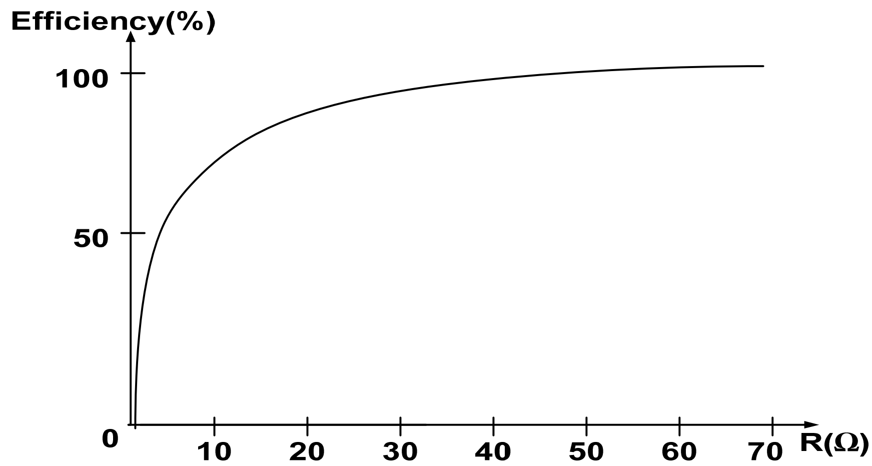


Figure 1.15: Class E efficiency vs load resistance

To summarize the conventional classes discussed above, a comparison between these classes in term of conduction angle, linearity and efficiency is given in Table. 1.1.

Table 1-1: Efficiency comparison of classes of operation

Class	Version	Drain Efficiency [%]	Conduction Angle, φ [rad]
A	Single	50	2π
AB	Single	50 – 78.5	$\pi - 2\pi$
B	push-pull	78.5	π
C	Single	78.5 – 100	$0 - \pi$
D	push-pull	100	2π
E	Single	100	π
F	Single	100	π

1.2.c Drain Modulation Based RF Transmitter

The efficiencies reported in table 1.1 are given for maximum output power. But as the output power decreases, the efficiency goes down as well. A practical example of PA efficiency versus output power is plotted in Figure 1 16.

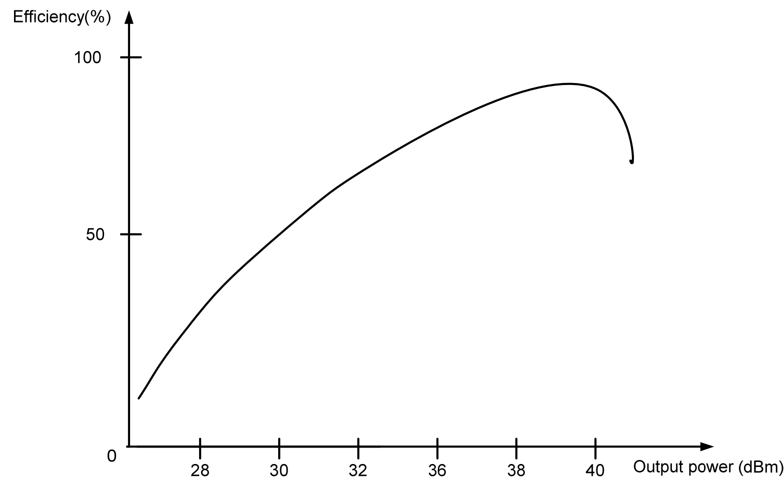


Figure 1.16: An Example of Power Added Efficiency versus Output power

It is easy to explain this mechanism for class-A amplifier. In the case of class-A amplifier, DC current and supply voltage are constant and the efficiency is defined as the ratio of output power to the DC power. Therefore low output power is equal to low efficiency. For constant envelope signals, the efficiency is always at peak, but modern wireless standards like W-CDMA, LTE impose amplitude varying signals. High peak to average signal, more than 9-dB for LTE, reduce the efficiency by more than 30-40% for regular amplifiers.

To overcome this issue, alternative amplification schemes have been sought to improve the power efficiency of the power amplifiers. These schemes rest on the modulation of the transistor drain supply voltage or the load impedance as function of the input signal strength so that high power efficiency operation conditions can be maintained over a large power range. As an example, Doherty technique implemented an automated load impedance modulation using a peaking amplifier. Significant power efficiency, at power back off, has been recently reported [23]. However, Doherty technique is suffering from a very fundamental bandwidth limitation

attributed to the key impedance transformer. Alternative solution, which exploit the drain modulation, such as envelope elimination and restoration (EER), and envelope tracking (ET), are gaining more and more attention. They are particularly suitable for multiband and multimode RF front ends. These two techniques falls under a common family of radio transmitters called Polar Transmitters. Block diagram of the polar transmitter is shown in Figure 1.17.

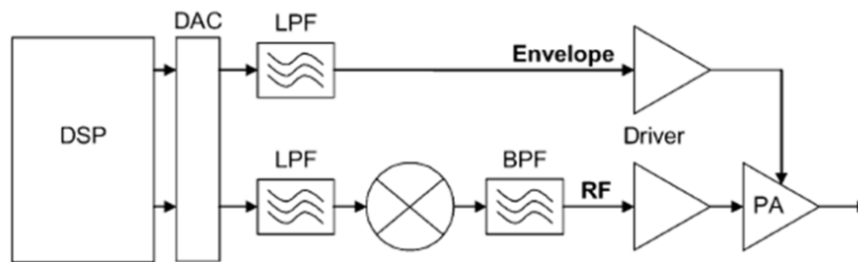


Figure 1.17: Polar transmitter

In contrast to traditional I/Q transmitters, polar transmitters transform the in-phase and quadrature components of the input signal into amplitude and phase representation. The amplitude information is then used to control of the drain supply voltage and consequently the gain (in the case of EER) or the DC power (in the case of ET). The modulated phase signal is a constant amplitude signal (in the case of EER), thus one of the main attributes of EER technique is making possible the deployment of high efficiency PAs, which are strongly nonlinear, while meeting the linearity requirements. The overall efficiency is the PA efficiency multiplied by the Envelope path efficiency. Therefore overall transmitter efficiency reduces at peak power but it is improved at back off signal.

Analog amplifier, buck convertor or mixed analog/digital circuitry are the candidates for the envelope path. Buck convertor has high efficiency, more than 90%, but it has limited bandwidth. It is more applicable for low bandwidth (BW) signals like EDGE/GSM [7]. For large BW signals like W-CDMA and LTE, an analog amplifier is a solution. More advanced architectures are using a combination of buck convertor for low frequencies and analog amplifier for high frequencies [8], [9].

Polar transmitter needs phase (θ) and magnitude (r) information instead of Inphase (I) and Quadrature (Q) signals. I/Q to r/θ transformation is a nonlinear function, which affects signal BW. It increases the phase BW approximately by 20 times and amplitude BW by 5 times comparing to original I/Q signal. That introduces some new issues to the PA design. In this case PA and supply modulator have to be very wideband comparing to regular transmitters.

As mentioned above, nonlinear PA can be used in EER architecture which improves the transmitter's efficiency. But it has two main drawbacks: (i) phase information is more wideband than original signal (ii) high input power leaks to the output and limits the dynamic range of transmitter. On the other hand, ET transmitter is fed by original modulated signal which has less BW and also amplitude modulated input signal which increases the PA dynamic range. Since the input signal has amplitude variation, a linear amplifier has to be used in ET architecture. RF PA of these architectures has to have good performance versus supply voltage variation, while ET amplifier is linear but EER can be a nonlinear PA. This thesis discusses design and implementation of two PAs applicable for ET and EER techniques.

1.3 Transistor Device Choices

As the market for cellular, personal communications services, broadband access are expanding RF & Microwave circuits and amplifiers are getting more attention. Variety of transmitter technologies are vying for market share including CMOS, Si-LDMOS (Lateral-diffused MOS) and Bipolar transistors, GaAs MESFETs, GaAs (or GaAs/InGaP) heterojunction bipolar transistors (HBTs), SiC (Silicon Carbide) MESFETs and GaN HEMTs [11]. Among the mentioned processes, Gallium Nitride and CMOS have some characteristics that offer compelling solutions for the design and manufacture of high performance and robust, RF devices and power amplifier.

Most wireless systems are composed of base-station (BST) and its end-users. BST transmit large amount of power using electricity source covering wide area, and users respond to BST operating at low power using their battery. Depending on the standard, they work at different frequencies. Figure 1.18 shows which technologies are applicable for which frequencies and power level.

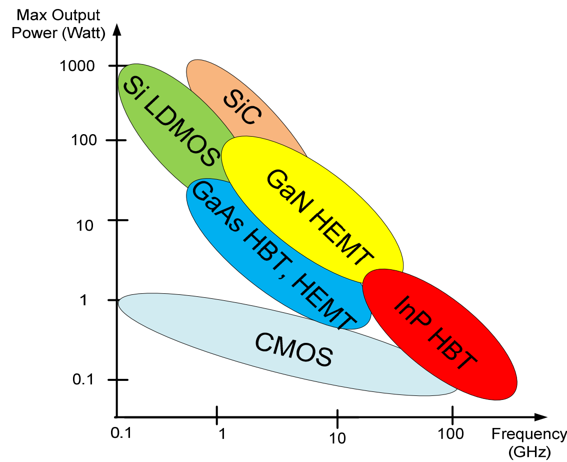


Figure 1.18: Device availability for different frequencies and power levels

Third generation (3G) networks, LTE, WiFi, Worldwide Interoperability for Microwave Access (WiMax), WCDMA and other recent standards are operating in frequency range of 1GHz to 5GHz which increases the demand for GaN, GaAs and CMOS technologies. CMOS offers low cost solution for wide range of frequency but it is just applicable for low power transmitters. Gallium Nitride has unique combination of higher power, higher temperature and wider bandwidth. It is vying GaAs to become the dominant technology for high power applications.

The work presented in this thesis is mainly about design of CMOS PAs, however a discrete-component PA was fabricated because of reasons that are given in the following. CMOS fabrication is a sophisticated process and takes long time and is an expensive process. Therefore design of this PA was used as an intermediate step toward CMOS PA design. Discrete-component PA design take much less times than CMOS. Gallium Nitride technology was selected for the discrete-component PA. Unlike digital circuits, where transistors act as switch and the functionality is not so technology dependent, RF circuit design require good understanding of device operation. The following section discusses the device characteristics of CMOS and GaN as the two technologies that are used in this work.

1.3.a CMOS technology

CMOS was the most widely used technology for integrated circuit (IC) fabrication during last two decades. The key advantage of CMOS is its low static power consumption which made

it popular for digital circuit. It was also used for digital, analog or low power RF circuits like LNA and-mixers. CMOS has very low breakdown voltage, which is a limit for high power application. Nevertheless, many people are trying to employ this process in PA fabrication. The main motivation is the low fabrication cost of CMOS comparing to available PA technologies, like SiGe, GaN and GaAs. As discussed before, almost all of the circuit blocks have been designed in CMOS, so having PA in this technology will result in a single chip transceiver.

To better understanding how a CMOS transistor works, a cross section of NMOS transistor is shown in Figure 1.19.a. Pure silicon is doped with group III or group V materials resulting in p-type or n-type substrate. N-type region has free electrons and p-type region has free holes.

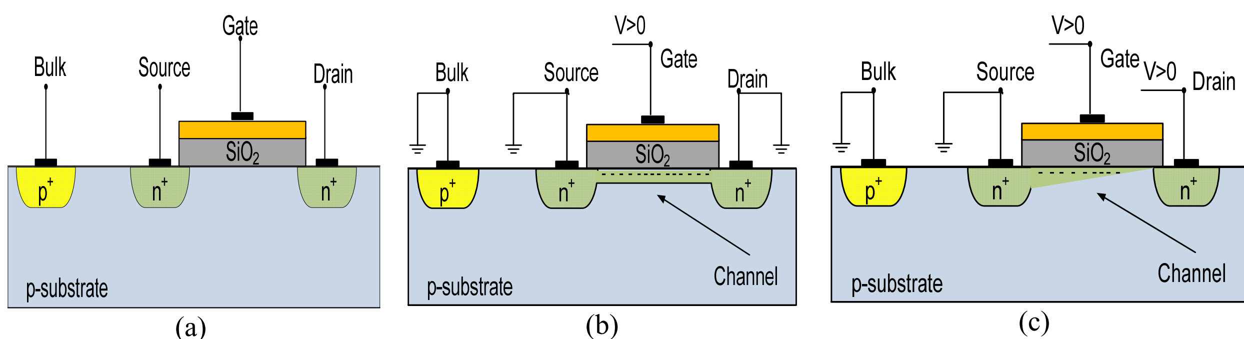


Figure 1.19: NMOS cross sectional

In Figure 1.19.b, source is connected to ground and a positive voltage is applied to the gate. This inverts the region between source and drain from p-type to negatively charged area which has lots of free electrons. A positive voltage across drain and source results in current in Figure 1.19.c. There are some parasitic components between source, drain, bulk and gate which are shown in Figure 1.20.

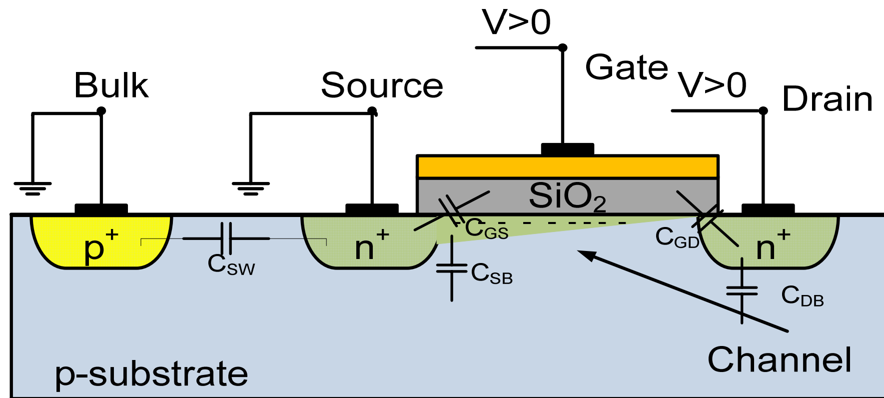


Figure 1.20: NMOS parasitic, cross sectional view

Depending on gate and drain to source voltage, three operational regions are defined for CMOS transistors; i) cut off ii) linear iii) saturation region. For PA application we usually bias NMOS in saturation region, however large signal swing push transistor in linear and cutoff region as well. To have an understanding that how NMOS amplifies the input signal, a simplified small signal model is presented in Figure 1.21 and circuit parameters are discussed in more details in [12] and [13].

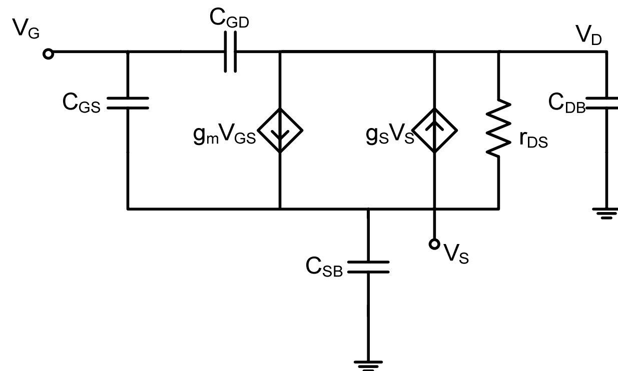


Figure 1.21: NMOS small signal model

Voltage dependent current source plays amplification role and transistor intrinsic gain is equal to $g_m \times Z_{DS}$ where Z_{DS} is r_{DS} parallel with C_{DB}. g_m and r_{DS} are function of DC current and device size and they have opposite behavior respect to drain current. As drain current is increased, the Drain-Source resistance (r_{DS}) decreases but g_m increases [12]. At high frequencies Z_{DS} is more affected by C_{DB} and is very low, therefore having high gain delivering high output power requires large amount of current through the transistor. This decreases the drain-source

resistance, thus larger impedance transformation ratio is needed for best matching between transistor and load matching network. Large impedance transformer is hard to design and increases matching network loss [10]. Low break down voltage also limits CMOS in high power application. Besides the device parasitic shown in Figure 1.20, there is resistive path between drain and bulk. At high frequencies this dissipates large part of the power which degrades the efficiency.

1.3.b GaN High Electron Mobility Transistor

High Electron Mobility Transistor (HEMT) also called heterostructure FET (HFET) is a field effect transistor. Unlike the conventional CMOS where the channel is inside a doped region, the HEMT incorporates a junction between two materials with different band gaps. In NMOS transistor, drain source current flows through an inverted p-type material. Although the channel has lots of free electrons, it still has some holes which can trap electrons in themselves and slow the electron movement. This electron-hole collision degrades the average speed and mobility, resulting in less gain and cut off frequency.

In the following paragraphs, we will discuss how a HEMT structure works and how it overcomes this problem.

A cross section of a GaN HEMT is shown in the Figure 1.22. AlGaN is an n-doped region which has higher bandgap comparing to GaN layer on top of substrate. The bandgap difference is shown in Figure 1.23. As this figure shows, the conduction band of AlGaN is higher than GaN, so electrons drops to GaN conduction layer at the contact point between AlGaN and GaN. These free electrons are shown in Figure 1.22 by dashed lines under AlGaN layer.

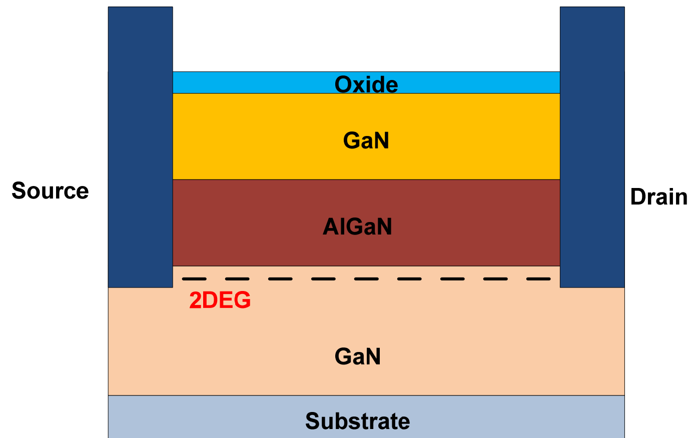


Figure 1.22: GaN HEMT cross-section

These free electrons can flow from source to drain if a positive voltage is applied between drain and source. Channel resistance is also controllable with gate voltage. The key advantage of this device compared to CMOS transistor is that there are no impurities in GaN that can trap mobile electrons and degrade their speed. Thus GaN have high cut off frequency and gain. Also GaN has larger bandgap comparing to silicon which enables high voltage operation for this technology.

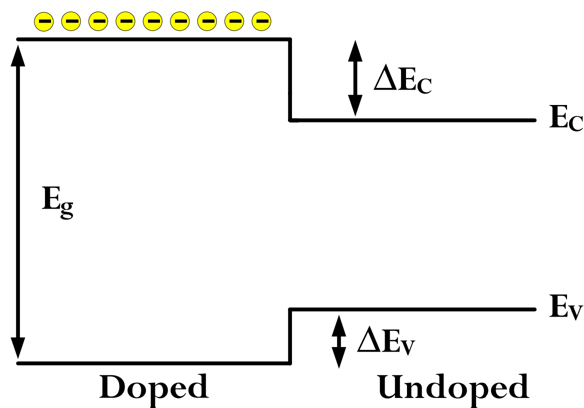


Figure 1.23: GaN and AlGaN bandgap differences.

The resulting competitive advantages of GaN devices and amplifiers for a commercial product are described in Table 1-2.

Table 1-2: Enabling Features of Gallium Nitirde [11]

Need	Enabling Feature	Performance Advantage
High power/ Unit Width	Wide BandGap, High Field	Eliminat/ Reduce Step Down
High Linearity	HEMT Technology	Optimum Band Allocation
High Frequency	High Electron Velocity	Bandwidth, mm-wave
High Efficiency	High Operation Voltage	Power Saving, Reduced Cooling
Thermal Management	SiC Substrate	High power devices with reduced cooling needs
Technology Leverage	Direct Bandgap: Enable for lighting	Driving force for technology low cost

The first column states the required performance benchmarks for any high power devices technology and the second column lists the enabling feature of GaN based devices that fulfill this need. In every single category, GaN devices excel over conventional technology. The last column summarizes the resulting performance advantages at the system level and to the customer. The highlighted features offer the most significant product benefits. The high power per unit width translates into smaller devices that are not only easier to fabricate and also offer much higher impedance. This makes matching network design much easier. The high voltage feature eliminates or at least reduces the need for voltage conversion. Commercial systems (e.g. Wireless Base Station) operate at 28 Volts and a low voltage technology would need voltage step down from 28 V to the required voltage. However, GaN devices can easily operate at 28 V and potentially up to 42 Volts. The higher efficiency that results from this high operating voltage reduces power requirements and simplifies cooling, an important advantage, since cost and weight of cooling systems is a significant fraction of the cost of a high power microwave transmitter. While some of the requirements for RF and Microwave applications are different (such as the need for a Semi Insulating substrate), there is no doubt that exercising the overlapping technologies will contribute in driving down the development cost of RF components and offer leverage up to a certain extent [11].

1.4 Discussion

An introduction to RF power amplifier as a fundamental building block of any radio transmitter is given in the first chapter. Different parameters for evaluating a power amplifier are explained. Based on these figure of merits, few widely used amplifier classes, like class A, AB, E and etc, are introduced and advantages and disadvantages of these classes are discussed. Drain modulated RF transmitters are introduced as a solution to efficiency problem of traditional classes. SDR is also introduced as an idealized method for supporting multi-standard operation. Respect to available technologies, SDR is not practically implementable. Multiband and broadband transceivers are introduced as realistic solutions.

Efficiency and multi-standards capability are mentioned as the main challenges in RF transceiver design. To target both feature at the same time, we ended up with multiband or broadband polar transmitter. Block diagram of this transmitter is shown in 1.24.

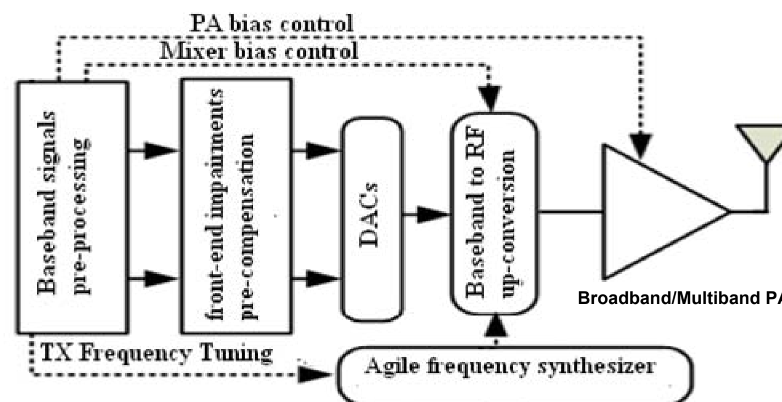


Figure 1.24: Multi/Broad-Band Polar Transmitter

One of the main issues in implementation of these architectures is their RF amplifiers which also have to be highly efficient and broadband/multiband. This work is focused on design of the core RF amplifier for multiband and broadband drain modulated transmitters. As noted above, supporting multi-standard operation, RF PA has to be designed either broadband or multiband. Both types are designed and fabricated in 0.13µm CMOS technology. CMOS has a sophisticated fabrication process and it takes long time, more than seven months. Therefore it is

crucial to avoid any classical mistake in PA design or test procedure. At high frequencies, circuit performance is more sensitive to parasitic, and also its test procedure requires more accuracy and understanding of RF theory. Therefore fabrication experiences would help to get better results in less time. Discrete components circuit fabrication is faster and usually cheaper than CMOS fabrication process, therefore a class E PA using GaN HEMT technology was fabricated and tested. This design was used as an intermediate step towards CMOS fabrication and test. It was also used to validate the idea of nonlinear amplifier `for polar architecture. This GaN based PA is also used to evaluate performance of power amplifier in a drain modulated transmitter. Chapter two discusses this GaN PA in more details.

Having this experience, two integrated RF PAs are designed. Chapter 3 discusses the multiband amplifier for ET application and chapter 4 talks about the nonlinear broadband PA suitable for EER technique.

Chapter 2

High Efficiency Class E Power Amplifiers using Packaged GaN device

Chapter one discussed drain modulated transmitter as a high efficiency solution for recent standards such as LTE, WCDMA WiMax, which have high peak to average amplitude signal. Switched mode PAs (SMPAs) are candidates to be used as the RF amplifier in this architecture. In theory, the output power of a SMPA depends only on the supply voltage. However, in class-A/AB, F, F^{-1} and harmonically tuned amplifiers, the output power is theoretically function of the drain voltage and the input signal power. This characteristic makes SMPA a good candidate for polar transmitters where output power is controlled by supply voltage.

This chapter discusses design procedure of a 10Watt power amplifier operating at 2.5GHz applicable for the drain modulated transmitter. The main object of this design is to become familiar with PA design techniques and then use this experience in CMOS PA design and test. As discussed in the first chapter GaN, GaAs are the best candidate at this frequency. Among them, we chose GaN which is suitable for high power applications.

2.1 Choosing class of operation

Among SMPAs class E is good candidate as it avoids the need for input and output baluns of class D. In addition, higher efficiency can be obtained with class E than voltage mode class D as operation frequency increases. Though class E has a cut off frequency which determines the maximum frequency of where original class E operation is possible [1]:

$$f_{max} \approx 0.05 \frac{P_o}{C_d V_{DD}^2} \tag{2-1}$$

Where P_o, V_{DD} and C_d denote the desired output power, the supply voltage and the transistor drain parasitic capacitor. Furthermore, unlike class F/F^{-1}, class E optimum load

impedance is determined using time domain equations. The two following conditions have to be satisfied by output matching network for maximum efficiency:

(i) The voltage across the transistor is zero when the switch is turned ON.

(ii) The current through the transistor is zero when it is turned OFF [21].

Hence, theoretically voltage and current waveforms don't overlap and consequently 100% efficiency is attainable. However, in practice, transistors' parasitic elements hinder the switch like operation from being achievable. Combined with matching network losses lead to lower realizable efficiency, yet good efficiency can be obtained as will be demonstrated later even at high frequencies.

2.2 Class E Amplifier Design Procedure:

A 10Watt GaN device (CGH40010 from Cree inc.), is used for design of this class E amplifier. At the first step of design, transistor DC characteristics were simulated. Drain current versus supply voltage and gate voltage were plotted. Figure 2.1 shows the obtained I-V curve.

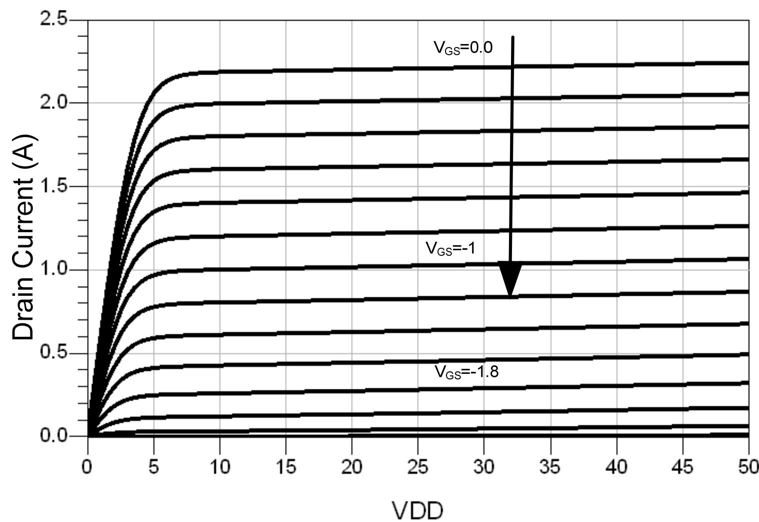


Figure 2.1: GaN transistor DC characteristics.

We chose the transistor's gate voltage equal to -2V resulting in 7mA quiescent current, which means that it is biased very close to class-B region. According to the first chapter

equations, class E operation, with an output power of 10Watt, can only be obtained at a maximum frequency of 425 MHz. To overcome this problem,

a low-pass prototype was used which increases the cut-off frequency, at the cost of reduced power capability is chosen so that higher frequency class E operation can be obtained.

Based on the two mentioned conditions, a lumped element matching network is designed. Lumped element circuits at microwave frequencies have two main drawbacks comparing to transmission line (TL) based circuits; (1) they have low quality factor (2) TL based MN has more control on higher harmonics comparing to lumped elements MN with limited components. On the other hand, transmission line circuits occupy large area, which is not usually tolerable for end-users. For high power applications such as base-station power amplifiers, TL based MN can be employed.

There are equivalent transmission line based circuits for capacitors and inductors, but we did not use them in this design. We simulated the S-parameters of the lumped elements matching network and found the loci of impedances at fundamental frequency and its harmonics on Smith chart and then implemented them using transmission lines. The loci of impedance are shown in Figure 2.2.

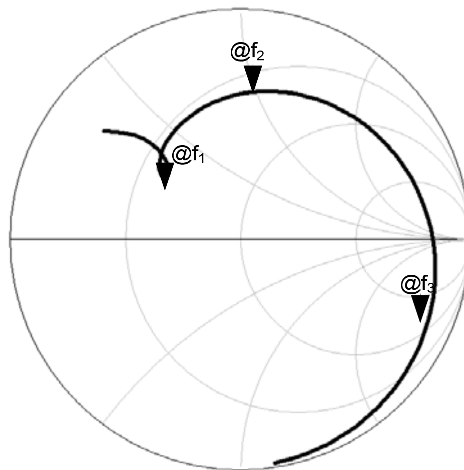


Figure 2.2: Loci of lumped elements matching network's impedances on the Smith chart

The power amplifier designed using these impedances gives high efficiency, close to 64%, assuming that all elements are ideal, but better performance is also achievable if we

optimize the location of impedances on the Smith chart. We have to consider following assumptions in matching network optimization:

(i) Satisfy Class E condition

(ii) Provide low-pass characteristics. 2nd and 3rd harmonics have to be close to the right edge of the Smith chart.

New impedances are obtained using Load/Source Pull simulation [22]. Figure 2.3 shows new load impedances on the Smith chart as Z_L. Fundamental frequency is shown by (f_0) and its 2nd and 3rd harmonics by ($2f_0$ and $3f_0$).

Input matching network is also designed with the aim of Load/Source pull simulation. The loci of impedances are marked as Z_S on Figure 2.3.

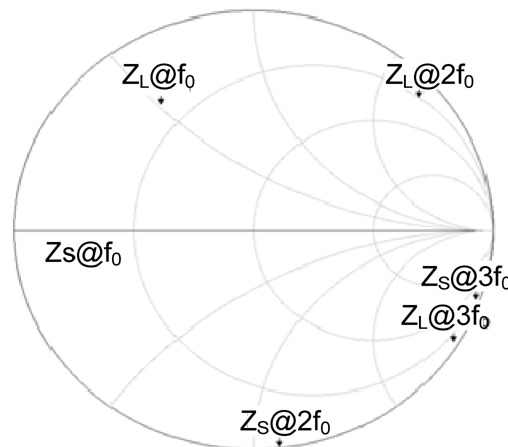


Figure 2.3: Loci of load and source impedances versus frequency.

Obtained impedances are implemented on “Rogers 5870” substrate. Its substrate thickness is 20mil, and the conductor layer, which is copper, has 17um thickness. Advanced Design System (ADS)’s “Line Calc” tool was used to design transmission lines. The layout view of the designed circuit is shown in Figure 2.4.

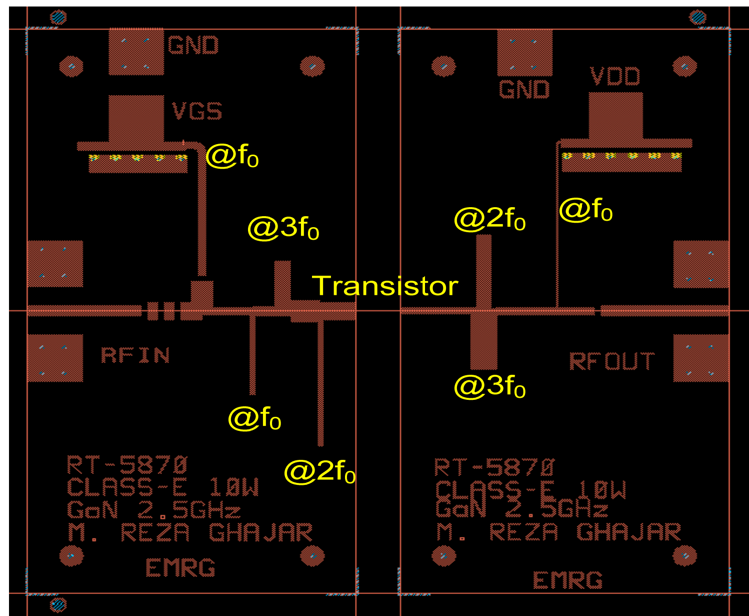


Figure 2.4: Layout view of the Designed Matching Network.

As shown in Figure 2.5, the chosen impedances lead to voltage and current waveforms, at the drain of transistor that is not in agreement with theoretical class E ones. This is mainly attributed to the fact that these waveforms are collected at the transistor terminations and not the current source.

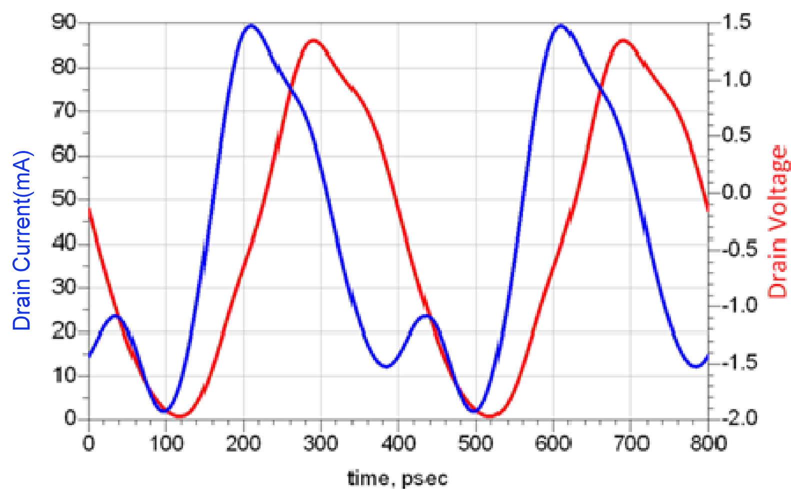


Figure 2.5: Drain voltage and current of Class E PA

Non-square input voltage also degrades PAE in class E. Ideally, square wave is assumed as gate voltage, but in practice it is not easy to drive PA at high frequency using pulse shaped sources. Compensating this effect input matching network is designed to shape sinusoidal input signal to a semi-square wave voltage at the gate. The loci of second and third harmonic impedances' of the input MN are shown on the Smith chart in Figure 2.3.

2.3 Measurement Results

Using Cree 10W GaN device, the class E PA was fabricated on a 508-um Rogers 5870 substrate. The photograph of this design is shown in Figure 2.6. This PA is design for polar transmitter application where the output power is depend on supply voltage. To achieve high PAE, the efficiency is optimized for average output power. In polar architecture, output power is depend on supply voltage. Assuming 4-dB back-off, the PA is designed for maximum efficiency at 28V supply voltage. Maximum supply voltage is high 50V delivering 42dBm with 52 % PAE. Figure 2.7 presents the measured PAE, DE and output power versus input power at 28 V supply voltage. At 2.5GHz, the maximum PAE of 75% and Drain Efficiency of 79% are achieved while delivering 38.3dBm to the load. The gain and PAE versus input frequency are plotted in Figure 2.8.

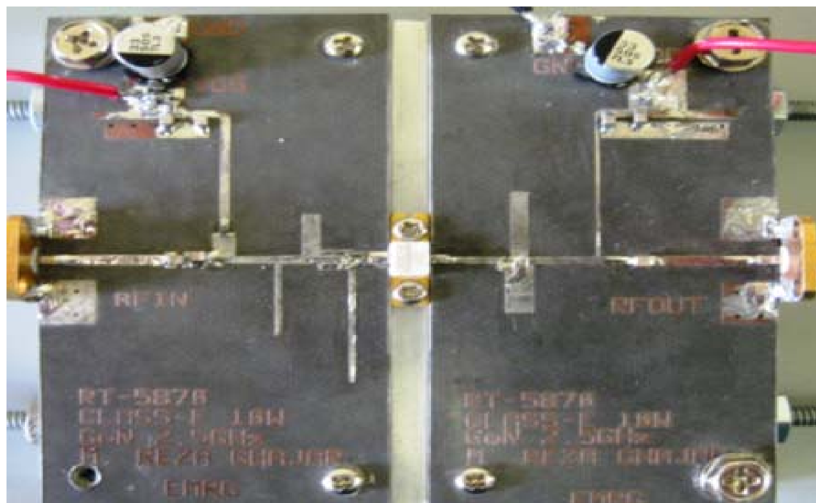


Figure 2.6: Photograph of implemented Class E.

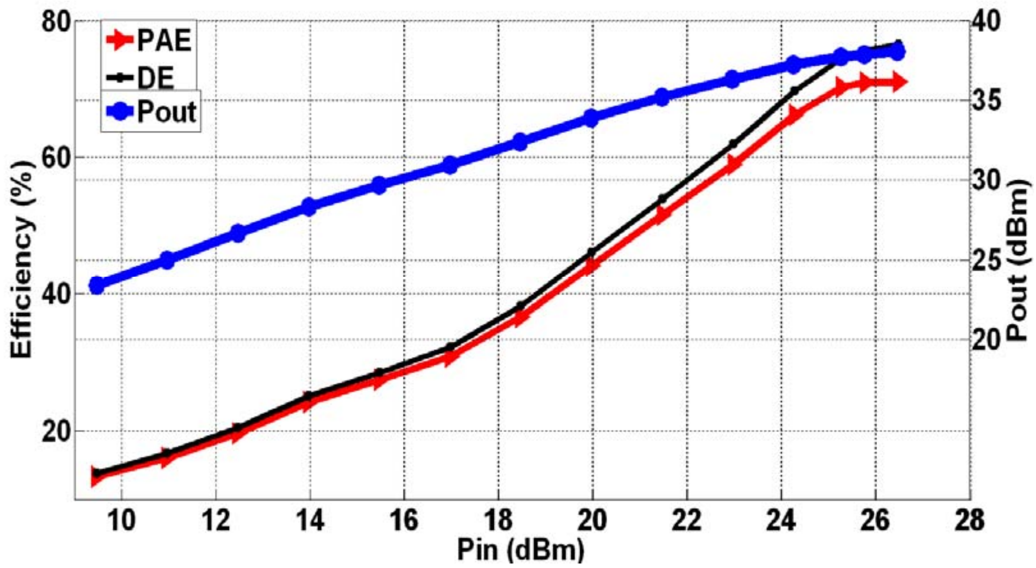


Figure 2.7: Measured Drain Efficiency (DE), PAE and Output Power vs Input Power.

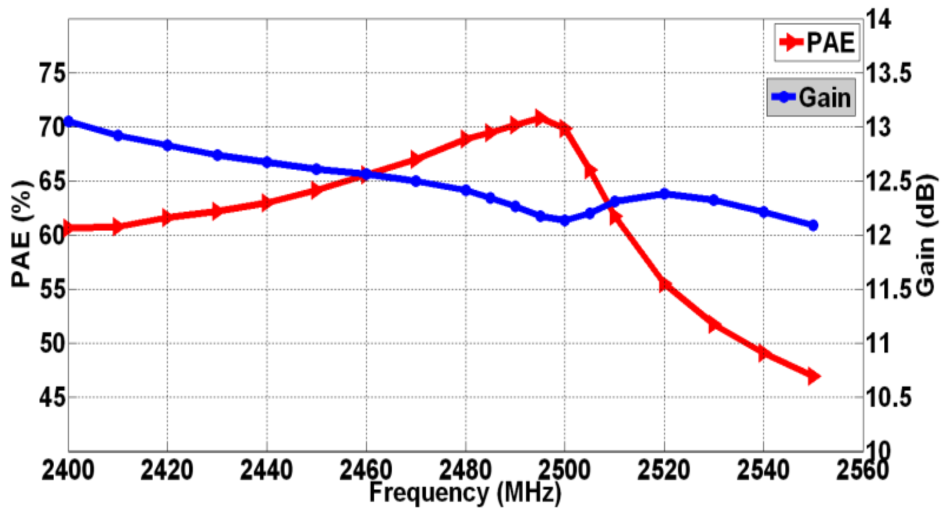


Figure 2.8: Measured Gain and PAE vs Input signal Frequency.

In addition, the low pass topology of the output matching network allowed for good harmonic suppression of better than 50dBc at second and third harmonics. Figure 2.9 plots output power spectrum of the PA.

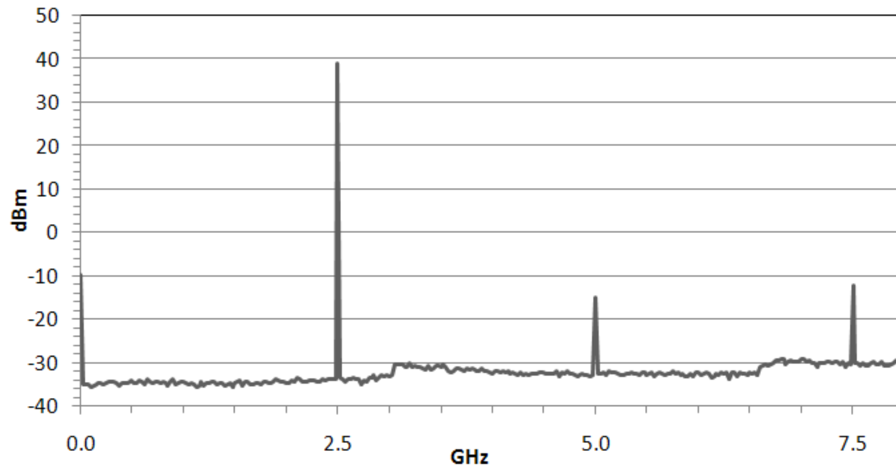


Figure 2.9: Output Spectrum at the maximum input power.

As previously mentioned, Class E is expected to favor the realization of high efficiency polar transmitters. This statement was confirmed by evaluation the output power and the efficiency of the present prototype when the drain supply voltage is swept between 5-50V. According to Figure 2.10 excellent efficiency was maintained over large power back off.

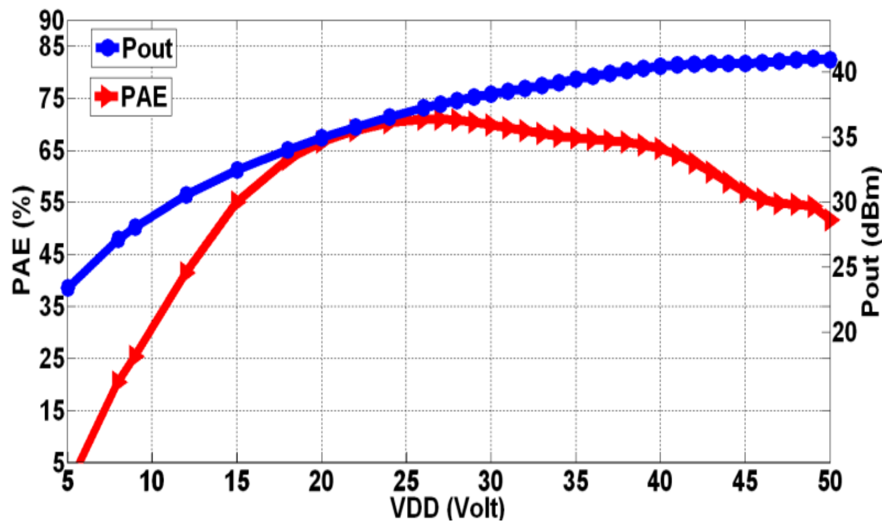


Figure 2.10: Measured PAE and Pout vs VDD.

2.4. Discussion

A high efficiency discrete-component power amplifier applicable for drain modulated transmitters was designed, fabricated and measured. Although fabrication process is more complicated for CMOS than Printed Circuit Board (PCB), successful design and test of both discrete and integrated component PAs require deep understanding of RF amplifier theory. Designing this PA helped us to apply all these theories in practice and prepare ourselves for design and test of integrated circuit PAs. The next two chapters discuss the two CMOS RF amplifiers, designed to be employed in drain modulation based architecture. Both amplifiers support multi standard operation. Chapter 3 discusses a high efficiency multiband, 2.4GHz/3.5GHz PA as the first solution for multi standard radio. Chapter 4 talks about the alternative solution, which is a high efficiency broadband PA.

Chapter 3

Concurrent Dual Band RF Power Amplifier in 0.13µm CMOS Technology

Multiband polar transmitter is introduced as a practical solution for high efficiency multi-standards radio. The main challenge in design of this transmitter is its RF amplifier which has to be multiband and optimized for ET or EER architectures. This chapter proposes an optimized dual band power amplifier design approach for fully integrated CMOS solution where quasi-optimal settings are maintained in each targeted band. This PA is biased in class AB which makes it suitable for ET architecture.

3.1 Power Amplifier Design in CMOS technology

The design of multi band RF circuitry is certainly a complex task. Nevertheless, this complexity, when coupled with extra limitations related to the fabrication technology, can lead to even more challenging design factors. This is particularly true in the case of dual band power amplifier design in sub micron CMOS technologies which is used in our work. Indeed, one of the main obstacles in new CMOS technologies is the low supply voltage that results in very low output power. In addition, this technology is characterized with a very low drain breakdown voltage that prevents adequate implementation of advanced power amplifier classes of operation such as the class E due its excessive peak drain's voltage that can reach as much as $3.5\times V_{DD}$. Furthermore, passive RF components, inductors and capacitors, are another source of challenges in a fully integrated CMOS design. Among others, this manifests in low quality factor of inductors that leads to excessive losses and consequently to power efficiency degradation. In addition the large size of passive components, where compared to the RF transistors, limits the practical output matching network topologies for fully integrated implementation.

To partially surmount the above mentioned problems, an impedance transformation is generally utilized. Indeed, in the case of a simple and ideal of class-A power amplifier with 1.5V supply voltage and terminated to 50 Ohms, the maximum output power (P_{OUT}) can be calculated as following:

$$P_{OUT} = \frac{{V_{DD}}^2}{2R_L} = \frac{1.5^2}{2 \times 50} = 22.5\text{mW} \tag{3-1}$$

Hence to achieve higher output power, for the given load impedance, the drain should be terminated with a lower resistance according to (3-1) that can be realized using an impedance transformer. Using L, ∏, T types of matching network, different impedance can be realized at the drain termination. Nevertheless, as reported in [21], the PA power efficiency is affected by transformer efficiency which in its turn relies on the Q-factor of the used inductors. This efficiency deterioration increases as the transformation ratio rises, which is usually needed.

3.2 Proposed dual-band PA architecture

As previously mentioned, the traditional approach to multi-band power amplifier design consists in using different parallel transistors and matching networks for each selected frequencies and then use a combiner to connect them to the antenna as depicted in Figure 3.1. The circuit of [20], is an example of implemented dual-band PA using this method.

As the previous approach leads to non optimized solution, a multi band matching network and single transistor are used to implement a multiband PA. As an example, a dual band matching networks that uses parallel resonators, resonating at different frequencies, is developed as depicted in Figure 3.2.

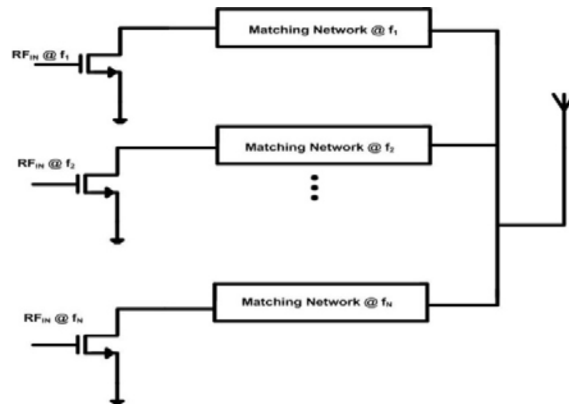


Figure 3.1: Traditional Multi-Band PA Topology.

Based on Figure 3.2, the dual band matching network includes two paths mounted in parallel, each of them block the signal at its resonant frequency. At the other frequency, the

resonator behaves as an inductor or capacitor. Hence, the dual band matching network reduces to a ∏ matching network at each center frequency that would transform the load impedance to the appropriate drain impedance that optimizes the PAE of the transistor.

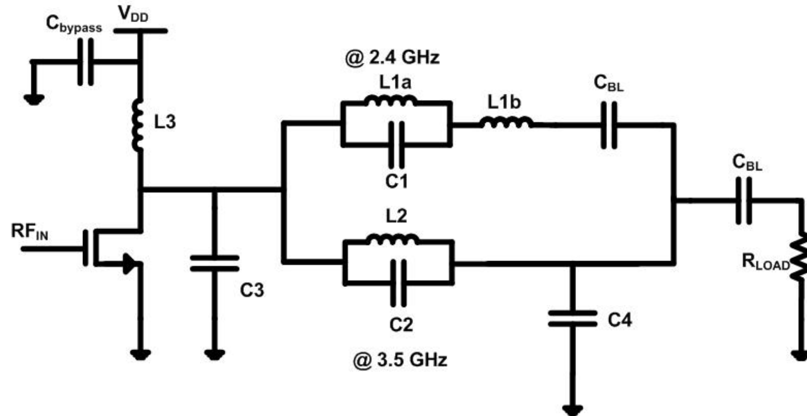


Figure 3.2: Proposed Dual Band PA Architecture.

As an illustration, the circuits in Figure 3.3 shows the operation at 3.5GHz and 2.4GHz. The matching network is optimized to operate at 2.4GHz and 3.5GHz. For that, the bottom LC resonator was determined so that it blocks the signal at 3.5GHz and the top one blocks the signal at 2.4GHz. Figure 3.3.a shows the PA when input signal frequency is around 3.3GHz. Upper resonator blocks the signal at this frequency and results in the simplified circuit of Figure 3.3.c. As can be seen, C_3, C_4 and L act as a ∏ matching network at 3.3GHz. The same method of analysis is valid for the 2.4GHz input signal. At this frequency, lower resonator blocks the input signal and upper branch passes it. In Figure 3.3.d, C_{1b} and L_{1b} together behave as an inductor which introduces a ∏-MN with C_3 and C_4.

The proposed circuit can also operate at a third frequency band. Both (L_{1a}-C_1) and (L_2-C_2) resonators behaves as an inductor at frequencies lower than 2.4GHz. Therefore for input signal lower than 2.4GHz, the PA can be simplified to the circuit of Figure 3.4. L_{1a}, L_{1b} and L_2 can be substituted with an equivalent inductor. This equivalent inductor and C_3 and C_4 behave as ∏ transformer at a third frequency. The inductor values have to be optimized to give the desired third frequency. In this work, 830 MHz was chosen as the third frequency.

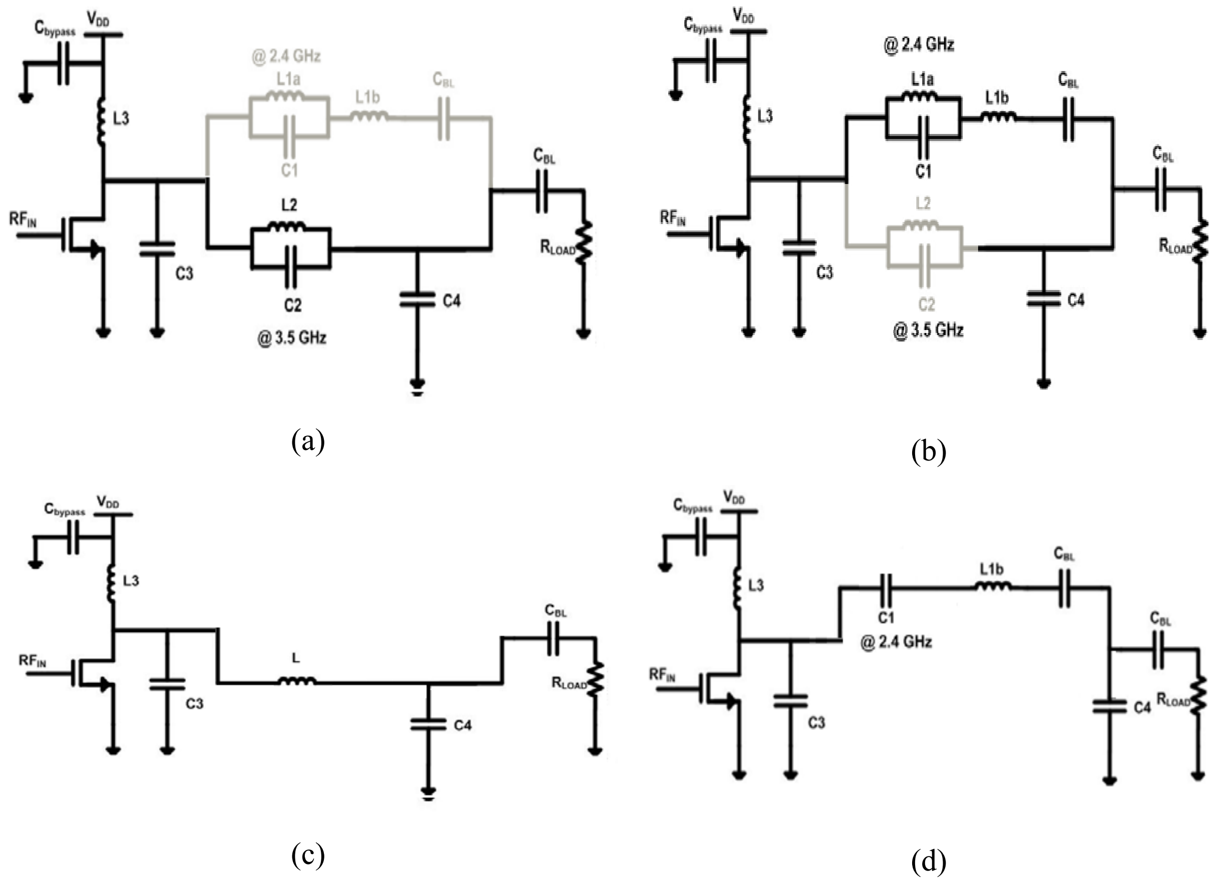


Figure 3.3: (a) Output matching network at 3.5 GHz (b) Output matching network at 2.4GHz (c) simplified circuit at 3.5GHz (d) simplified circuit at 3.5GHz

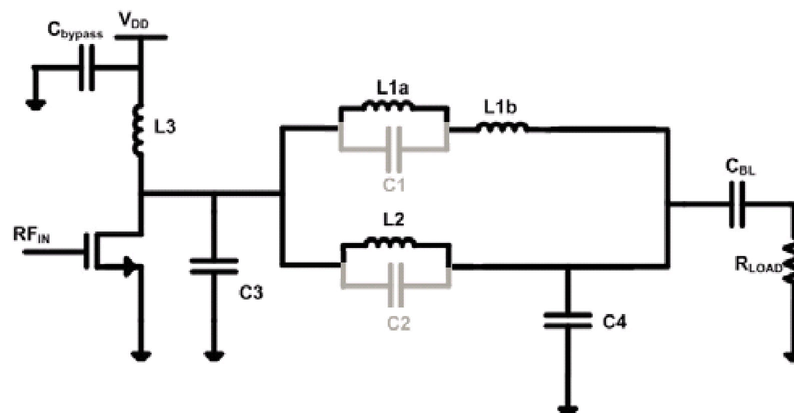


Figure 3.4: Third frequency operation of the matching network.

The initial inductors' and capacitors' values in the Figure 3.2 were subsequently optimized to account for the parasitic effects of interconnects. The transistor is biased to operate in Class AB. The final values of the different elements in the dual band matching network are given in table 3-1.

TABLE 3-1: Values of the Dual band Matching Network Elements

Component	Value	Component	Value
C1 (pF)	2	L1a (nH)	1.5
C2 (pF)	1.8	L1b (nH)	1.3
C3 (pF)	1.5	L2 (nH)	0.75
C4 (pF)	3	L3 (nH)	2.8

3.3 Simulation Results

The proposed circuit was implemented in 0.13µm CMOS using thin gate transistor of the IBM technology. The chip area is 1.5mm×1.5mm. The PA layout is shown in Figure 3.5.

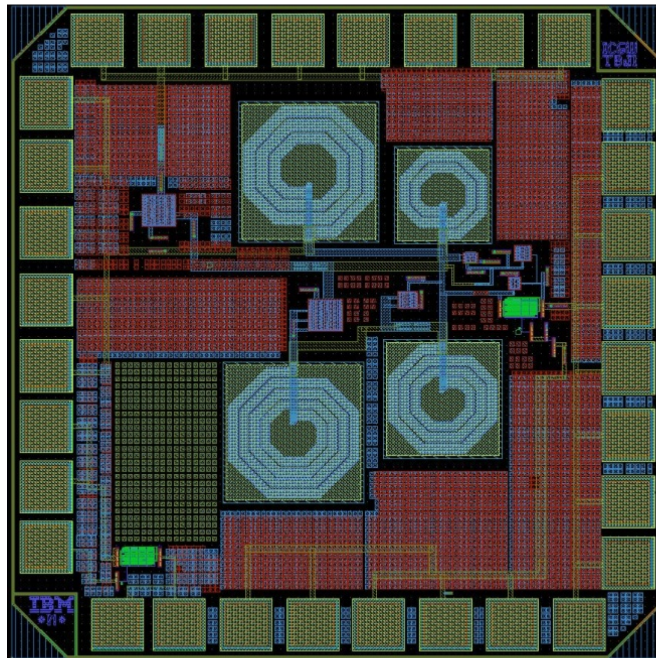


Figure 3.5: Dual Band PA Layout view.

The following results were obtained for a supply voltage equal to 1.5V. At first, the dual band feature of the designed circuit can be easily proven through the Figure 3.6 which reported the output reflection coefficient and the gain of the circuit versus frequency. As one can easily observe, an excellent matching was achieved simultaneously at 2.4GHz and 3.5GHz where the gain also attains its maximum.

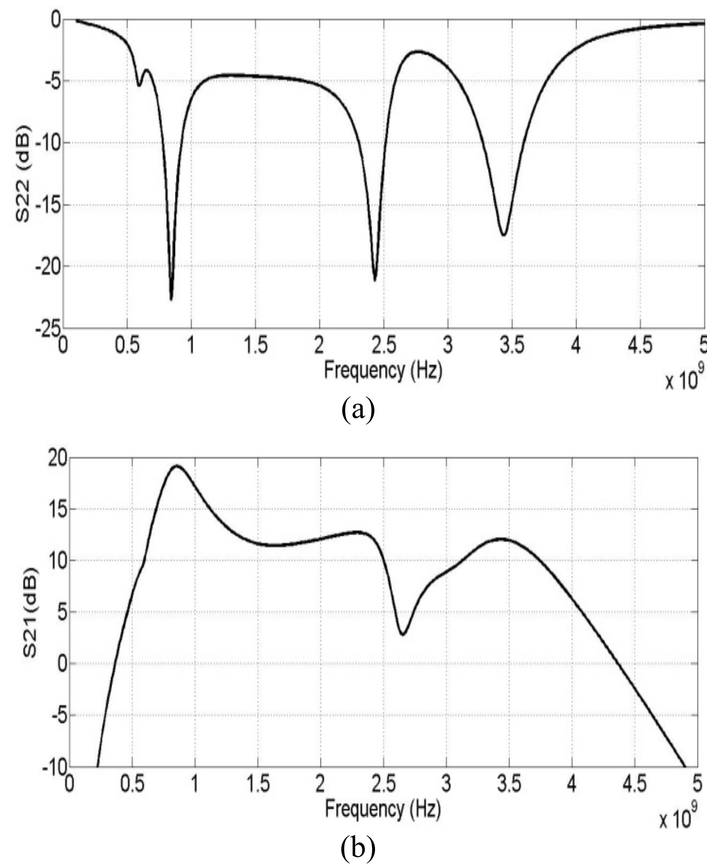


Figure 3.6: (a) Output Reflection Coefficient (S22) of the Dual Band PA (b) Power Gain of the PA (S21)

Furthermore, based on the nonlinear characteristics, shown in Figure 3.7, the designed circuit has a one dB compression point about 18dBm. Figure 3.8 demonstrates a relatively good power added efficiency of the designed circuit of about 43% at both frequencies.

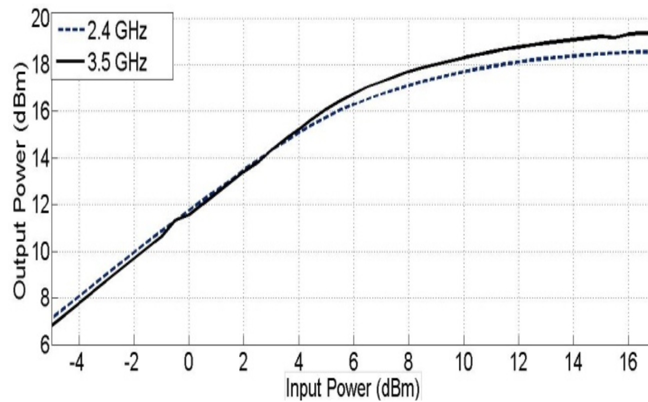


Figure 3.7: AM/AM Characteristic of the Dual Band PA Assessed at 2.4GHz and 3.5 GHz

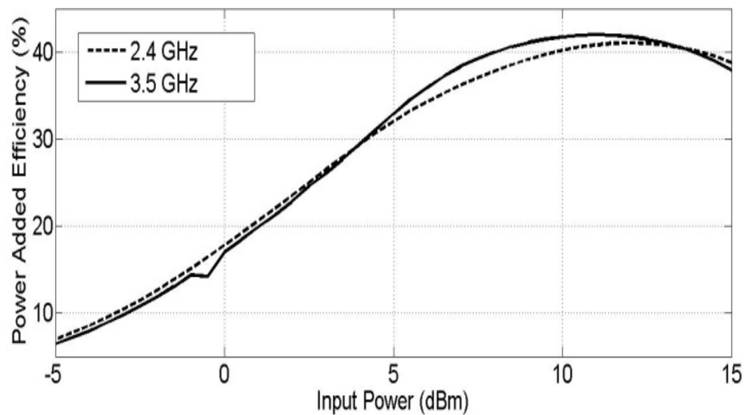


Figure 3.8: Power Added Efficiency of the Dual Band PA Assessed at 2.4GHz and 3.5 GHz.

The performance of the dual band PA was also compared to those obtained using two distinct single band PAs designed for each frequency separately. Indeed, the two single band PAs allowed for a PAE and a P1dB equal to 48% and 18dBm. Hence, the dual band feature of the designed PA was achieved at the cost a drop of 5% in the PAE when compared to the single band PA. This PAE drop is mainly due to low quality factor of two parallel resonators.

As discussed earlier, the dual band PA is designed to be used in drain modulation based transmitter. Therefore PA performance versus supply voltage is simulated. Figure 3.9 shows power added efficiency versus drain voltage for this amplifier at 2.4GHz.

Moderate performance is also achieved at the third frequency band. Good output matching around 830MHz is highlighted in Figure 3.10.

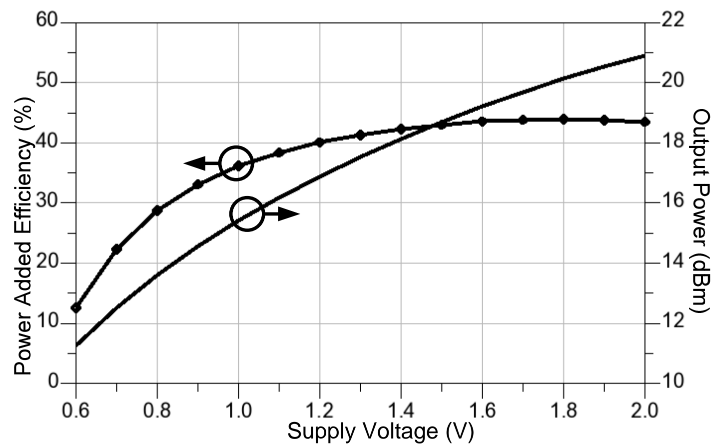


Figure 3.11: Power Added Efficiency and output power versus supply voltage at 2.4GHz.

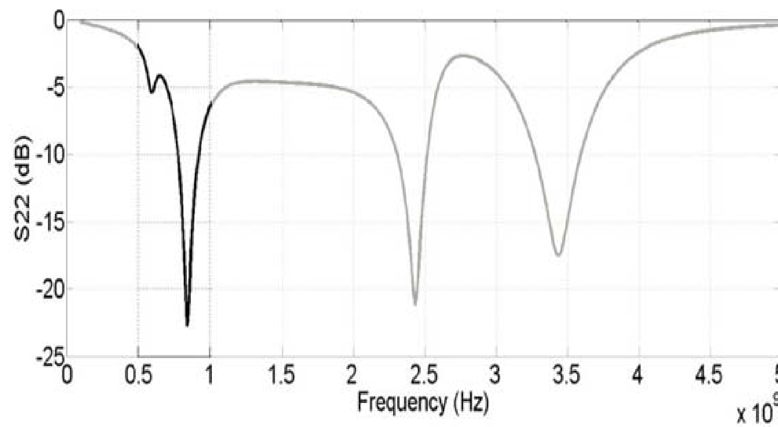


Figure 3.12: Output matching at 830MHz.

More than 30% PAE is obtained at this frequency. This low efficiency is due to the fact that we did not optimize the matching network for this frequency.

3.4. Discussion

A dual band CMOS PA is discussed. As mentioned in Chapter 1, multiband transmitter is one of the practical solutions for multi standard radio. The designed PA operate in class AB region and is more suitable for envelope tracking application. It shows acceptable performance versus supply voltage which is an important requirement for drain modulation based transmitters. The next chapter discusses a nonlinear broadband PA as an alternative solution for high efficiency multi standard radio.

Chapter 4
High Efficiency Broadband Integrated RF Power Amplifier

Many communication standards and applications ask end users to transmit more than 23dBm power through the air. Deep submicron CMOS transistors are working with low supply voltage, between 0.9V to 1.8V, and they have very low break down voltage. These prevent CMOS PAs to deliver enough power to the antenna. To overcome this problem, some techniques like power combining were introduced [10], [14], [15]. PAs that have been built with this method can give enough power, but their efficiency is lower comparing to the classic PAs. This is mainly due to the extra passive components that are added to the circuit. For low power applications, less than 25dBm, thick oxide transistors can be also used.

Chapter 3 discussed multiband PA which is the first solution for multi standard transmitters. Chapter 2 explained a discrete component class E PA operating at 2.5GHz fabricated using GaN HEMT. The main purpose of that design was to expand our knowledge in PA theory and its test procedure. Having experience of that design, a high efficiency broadband PA designed using thick oxide transistors in CMOS 0.13µm IBM technology.

4.1. Design Procedure

CMOS 0.13µm IBM technology is chosen for the design of this high efficiency PA because of

(i) High power capability through using thick oxide transistor and 3.3volts supply voltage

(ii) Good RF performance, high cut off frequency

(iii) Accurate modeling is available for transistors and passive components at RF

Following sections explain design procedure of the high efficiency power amplifier in details.

4.1.a DC Characterization

Thick oxide transistor has minimum gate length of 400nm. To provide enough gain and current, transistor gate width is selected to be 1.6mm. Transistor DC current versus gate and drain voltage is plotted in Figure 4.1.

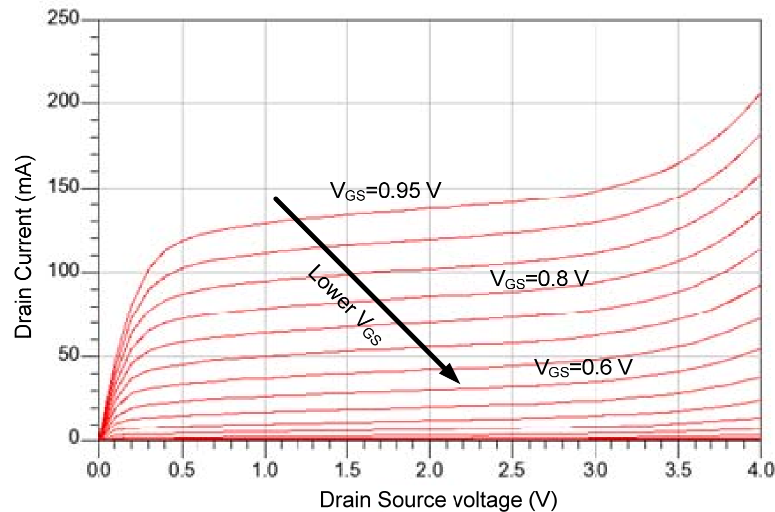


Figure 4.1: NMOS DC characterization

Supply voltage is 3.3Volts. Gate voltage is set to 0.8V which biases the transistor in class AB region with 90mA quiescent current.

4.1.b Load/Source Pull Simulation

The next step is design of matching network converting 50Ohm load to the desired impedance at drain (Z_{OUT}) noted in Figure 4. 2. Maximum power transfer does happen, if we set Z_{OUT} to conjugate value of Z_{DRAIN}.

Satisfying conjugate matching condition does not necessarily give the maximum possible efficiency. As discussed in the first chapter, high efficiency classes like class F, F^{-1}, … are designed based on harmonic tuning in matching network. Another way to design a high efficiency PA is source/load pull simulation. Figure 4.3 shows the source/load pull system which is used in our simulations. The method is based on impedance tuning and is an iterative procedure. The design steps are explained below:

Step I: Set initial values for the load (Z_{OUT}) and source (Z_{IN}) at fundamental frequency and its harmonics (3, 4 harmonics).

Step II: Sweep the fundamental load or source impedance all over the Smith chart and find a point on the Smith chart which gives the maximum PAE.

Step III: Change the load/source impedances to the new point calculated in step II.

Step IV: Sweep the other harmonics and perform step II and III for the harmonics.

Step V: Repeat step III and IV until you find the best possible efficiency.

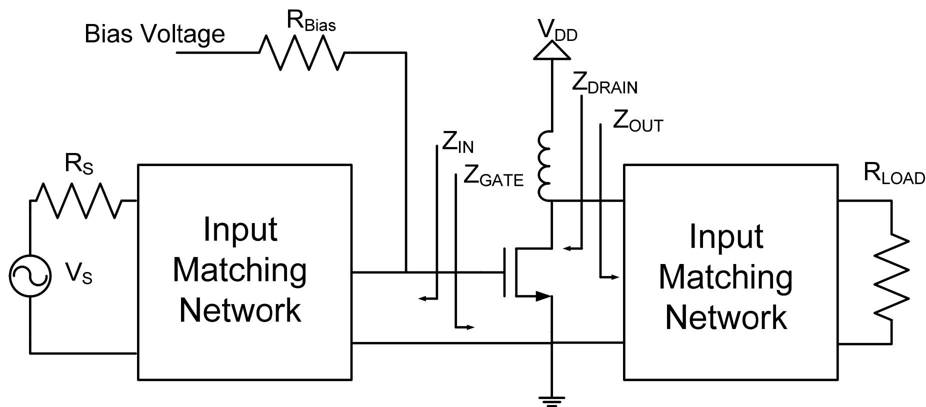


Figure 4.2: PA schematic

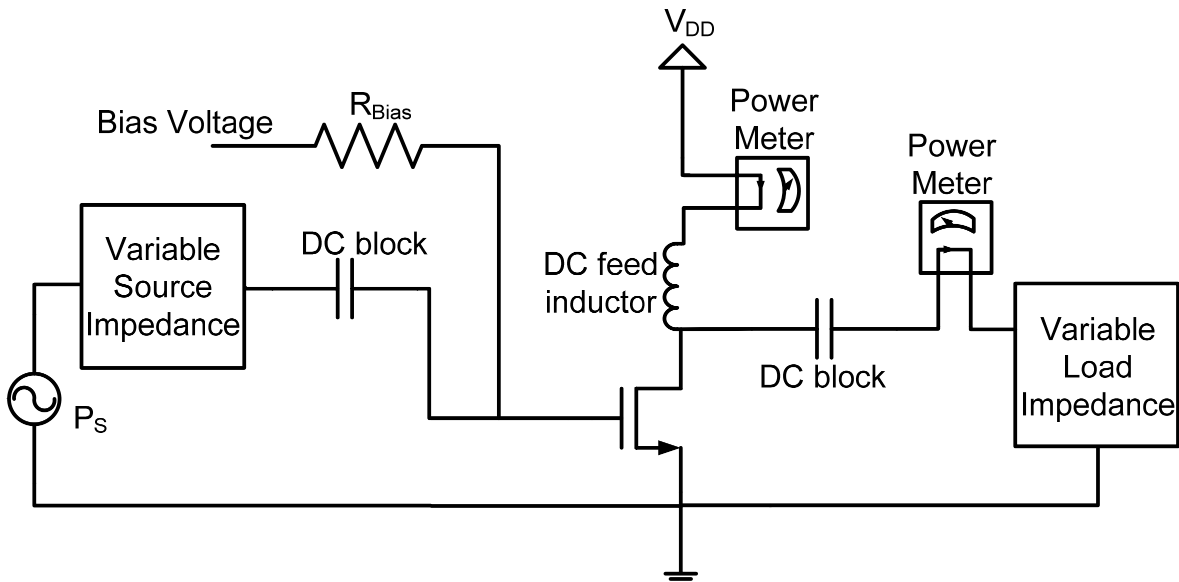


Figure 4.3: Source/Load Pull Simulation Setup

Limited number of passive components and their low quality factor (Q-factor) in CMOS technology impose some limitations to the discussed load/source pull method. Inductors have

very low Q-factor and occupy a large area compared to other components. Therefore designers are not advised to use many of them in integrated circuits. This decreases the control on MN's impedance at 2nd and 3rd harmonics. We applied some small changes to the explained load/source pull method thus it is changed to the following steps:

Step I: Set initial values for variable load (Z_{OUT}) and source (Z_{IN}) at fundamental frequency and its harmonics (3, 4 harmonics).

Step II: Sweep the fundamental load or source impedance all over the Smith chart and then find the point on Smith chart which gives the maximum PAE.

Step III: Design an MN using lumped elements for the new impedance at fundamental frequency.

Step IV: Perform S-parameter analysis for the designed circuit and find the location of harmonics on the Smith chart.

Step V: Update load/source impedance at fundamental and harmonics, based on values calculated in step IV.

Step VI: Repeat step II to V until achieving best possible PAE.

Another difference between fully on-chip CMOS and discrete PA design is the DC feed inductor. Figure 4.2 shows a discrete PA with a DC feed inductor. This inductor has to be very large to isolate supply voltage from RF signal and also have good quality factor to minimize the losses. In integrated PAs, small chip size and low quality factor of inductors suppose designers to choose small value for biasing inductor. This affects RF performance and also has to be considered as a part of matching network. Knowing all these limitations about CMOS power amplifier design, next paragraphs discuss the MN design.

Load/Source pull simulation, including non ideal DC feed inductor, was done in Agilent Design System (ADS). The initial value of DC feed inductor is set to 2.5nH that gives good isolation between RF path and supply voltage and also low insertion loss at 2.4GHz.

Load/Source pull simulation shows that maximum PAE of 65% is reachable for the chosen transistor and DC feed inductor. That requires a MN that presents $Z = 15 + j12$ to the

transistor's drain (including the effect of DC feed inductor) and $Z = 7 + j14$ to the gate. The gate impedance is very close to the edge of the Smith chart. It is hard to convert a 50 ohm to this impedance, and also any small deviation from this point will result in large drop in PAE. Thus $Z = 12 + j21$ is selected as the source impedance which gives few percents less efficiency, 61%, but is more stable against process variation. Figure 4.4 shows location of optimum load and source impedances on the Smith chart.

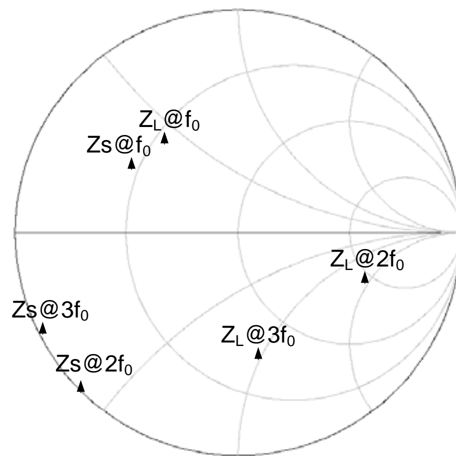


Figure 4.4 Loci of input, output matching network impedances on Smith chart.

4.1.c. Matching network design

Π impedance transformer is used as MN. ADS "Smith chart" tool is used to design a circuit converting 50Ohm to selected points on the Smith chart. MN bandwidth is depending on Q-factor of components and matching network topology. Inductors' Q-factor is assumed to be 15. Different combinations of component values in a Π MN can transform 50Ohm to the targeted point. Figure 4.5 shows some these different possible combinations on the Smith chart.

Solid and dashed lines on the Smith chart show different paths for different values. Shortest path gives the widest bandwidth, but that requires small capacitor values which degrades harmonic suppression. Thus there is a tradeoff between bandwidth and harmonic suppression. The same analysis is used for source side. Input and output MN designed using above method is shown in Figure 4. 6.

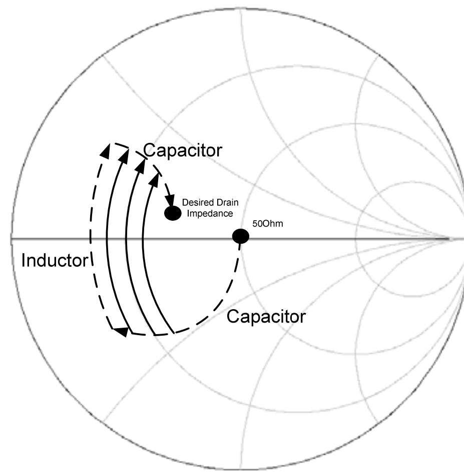


Figure 4.5: Same impedance transformation using different inductor and capacitor values.

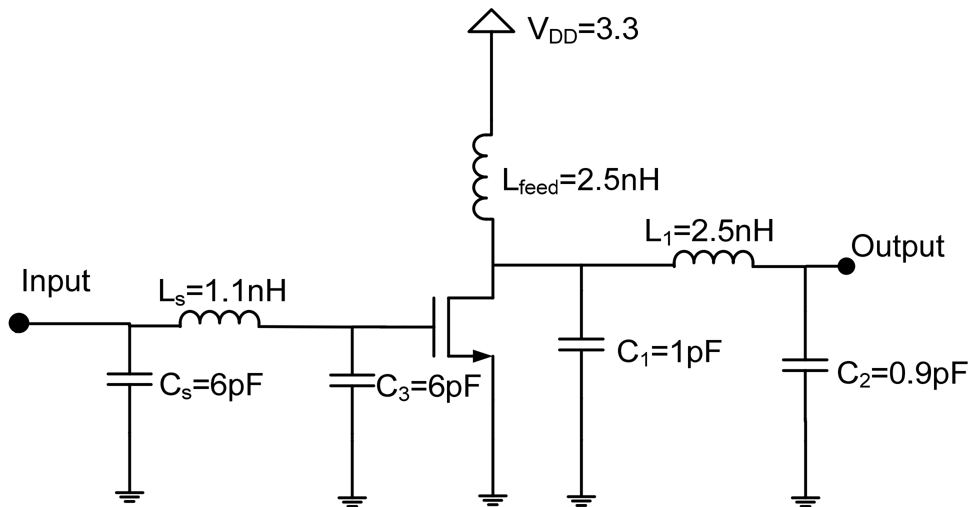


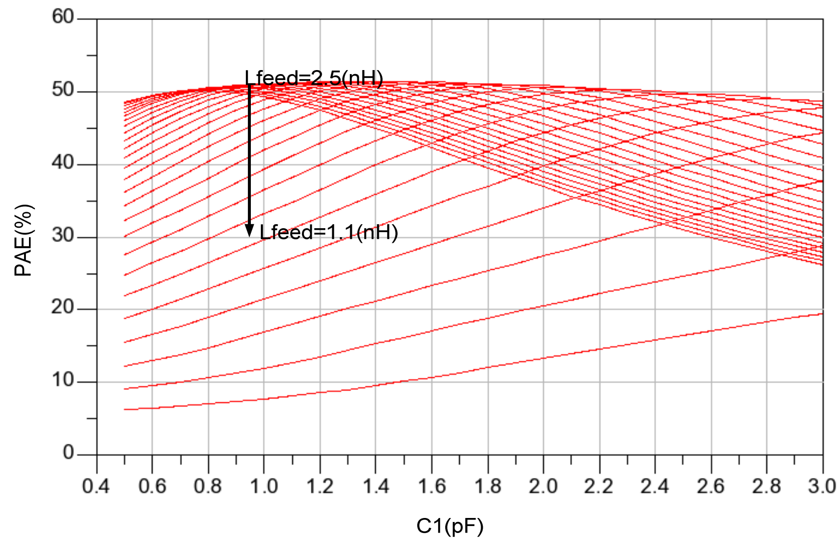
Figure 4.6: Designed PA using Load/Source Pull simulation

The circuit is simulated using ADS Harmonic Balance simulator and 50% PAE is achieved.

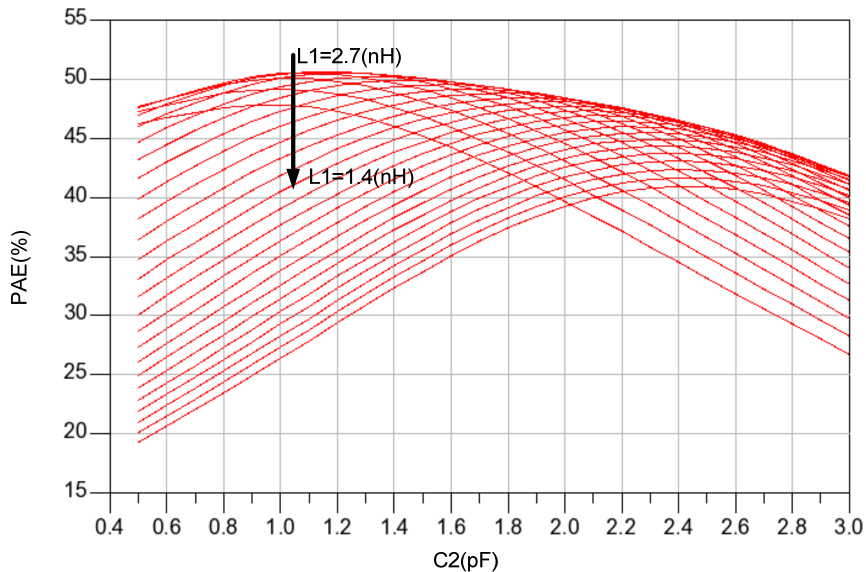
4.1.d Parameter sweep

Load/Source pull simulation assumes that passive components are ideal. But in reality matching network has a limited Q-factor, therefore after designing the MN, PAE degrades both due to losses, and deviation from optimum load. Efficiency drop due to losses is unavoidable, but

we can compensate the effect of deviation from optimum point by sweeping capacitors and inductors values around the initial design guesses. Figure 4.7a plots PAE versus DC feed inductor and C_1. Through this plot best values for C_1 and L_{FEED} are first found. Same process is repeated for C_2 and L_1, Figure 4.7b, till reaching the maximum PAE 53%.



(a)



(b)

Figure 4.7: Parameter sweep. (a) PAE vs Lfeed and C1 (b) PAE vs L1 and C2

4.1.e Passive components

On-chip components are used for matching network design. Capacitors are implemented using Metal-Insulator-Metal Capacitor (MIM-Cap). This kind of capacitor has a good quality factor but occupies more area comparing to Interdigitated capacitors.

Any piece of wire has an electric field around it and acts as an inductor. At microwave frequencies, it is possible to achieve high inductance made with some number of turns of wire. Planar spiral inductor is the most widely used technology in IC fabrication. Different shapes like circular, hexagonal, rectangular … and metal layers can be used for spiral inductors. Top metal layer implementation is the most common one. Layout view of square spiral inductor used in this design is shown in Figure 4. 8. The inductance depends on geometry and material properties of inductor which are discussed in [16].

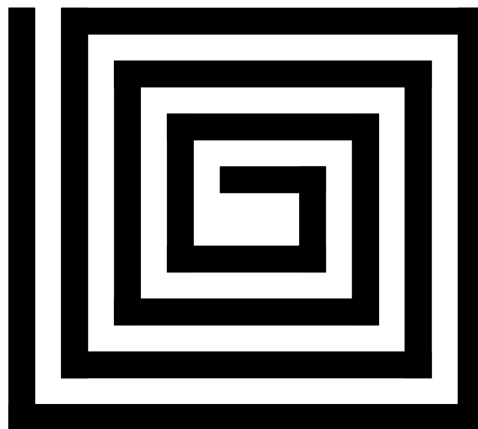


Figure 4.8: Square spiral inductor.

IBM provides reliable modeling for 0.13μm technology spiral inductors. To increase the accuracy Electro-Magnetic (EM) simulation is performed. Also RFIC Dynamic Link feature of ADS, which connects ADS to Cadence, is used to improve inductor Q-factor by playing on size. Inductance and quality factor of inductors versus frequency is plotted in Figure 4.9. As the figure shows, the quality factors of all inductors are above 15.

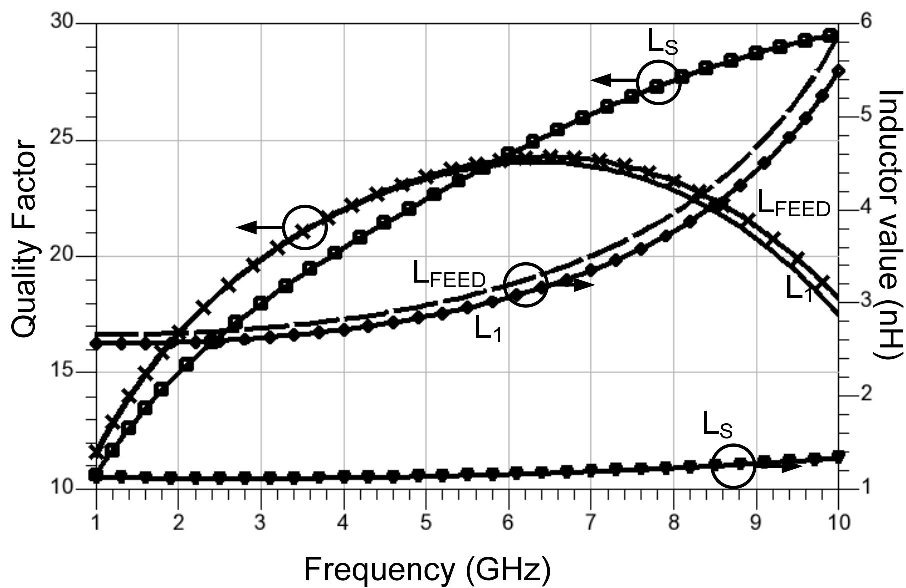


Figure 4.9: Q-factor and inductance vs frequency

4.2 Simulation Result

ADS software is used for PA simulation. S-parameter simulation demonstrates good matching at center frequency of 2.4GHz. S_{11} and S_{22} are plotted in Figure 4.10. Broadband matching at the load is achieved. Output power versus input power is plotted in Figure 4. 11. 1-dB compression point is 12dBm and is marked on the plot.

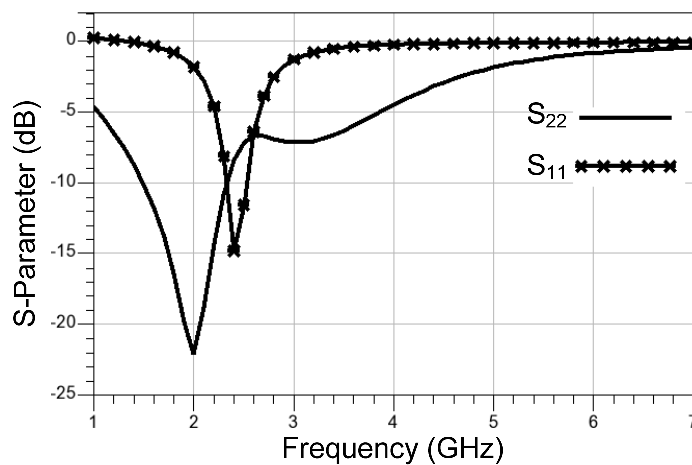


Figure 4.10: S_{11} and S_{22} versus frequency

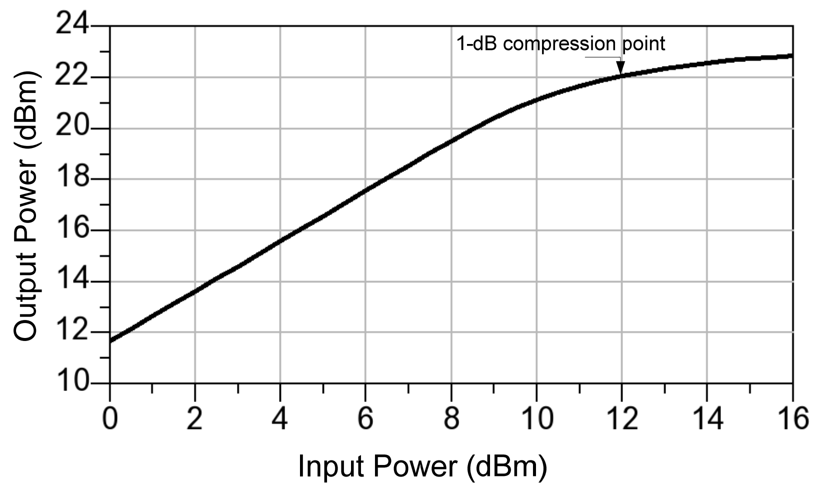


Figure 4.11: Output power versus input power

Power gain versus input power is shown Figure 4. 12. Small signal gain is close to 11.4dB.

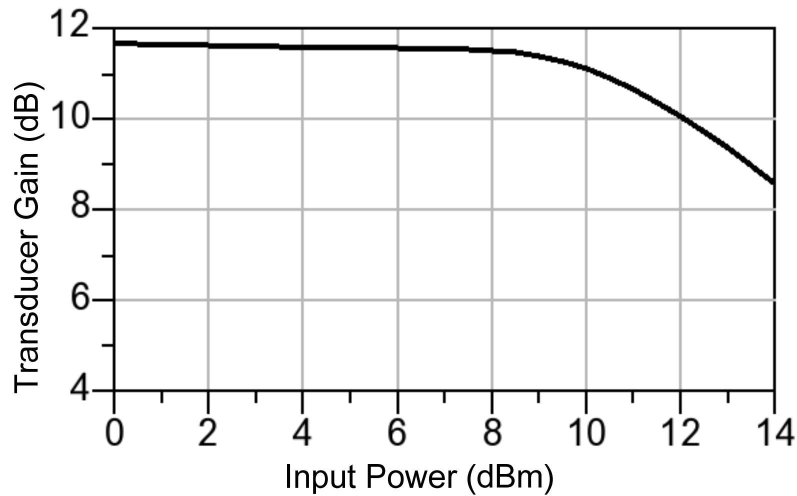


Figure 4.12: Gain versus input power

Figure 4.13 plots Power Added Efficiency and Drain Efficiency versus input power. Maximum PAE of 54% happens at 14dBm input power. Beyond this point Drain Efficiency still goes up, but PAE decreases. This is because the power gain drops very fast for input powers greater than 13dBm.

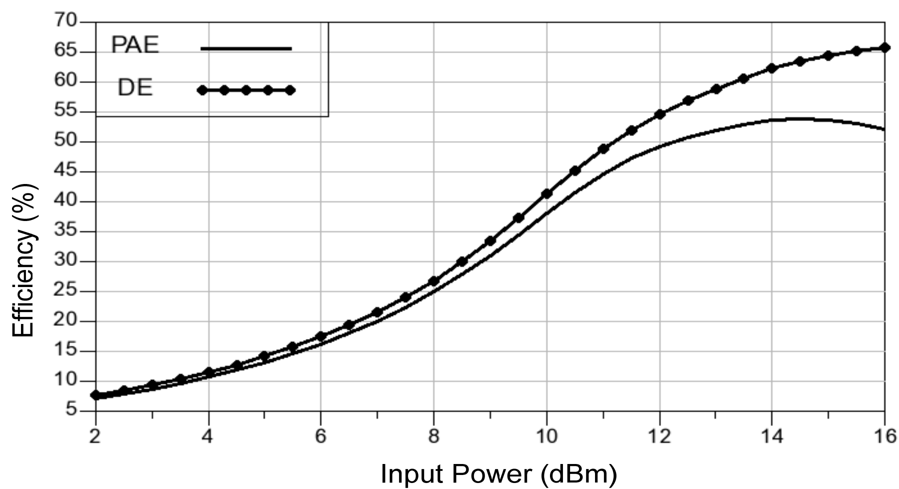


Figure 4.13: PAE, DE versus input power

Time domain voltage and current at the transistor drain is plotted in Figure 4. 14. The waveforms are very close to class E waveforms.

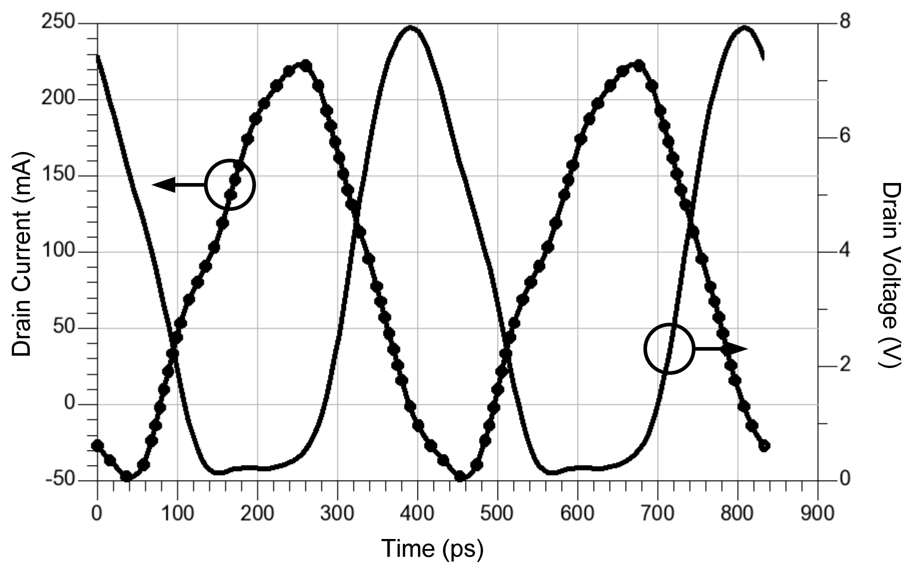


Figure 4.14: Time domain voltage and current at drain

Output power spectrum is shown in Figure 4. 15. Second harmonic suppression is not very good. That is mostly due to the fact that design is optimized for wide band operation.

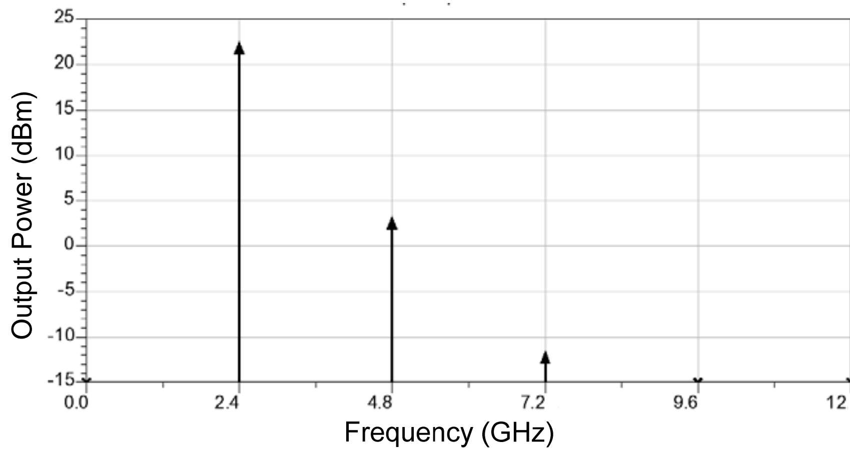


Figure 4.15: Output power Spectrum versus frequency

This PA is designed to be employed in drain modulated architecture. Simulation result demonstrates its good performance over a wide range of supply voltages. Supply voltage is swept from 1v to 4v and PAE, DE and power gain are plotted in Figure 4.16.

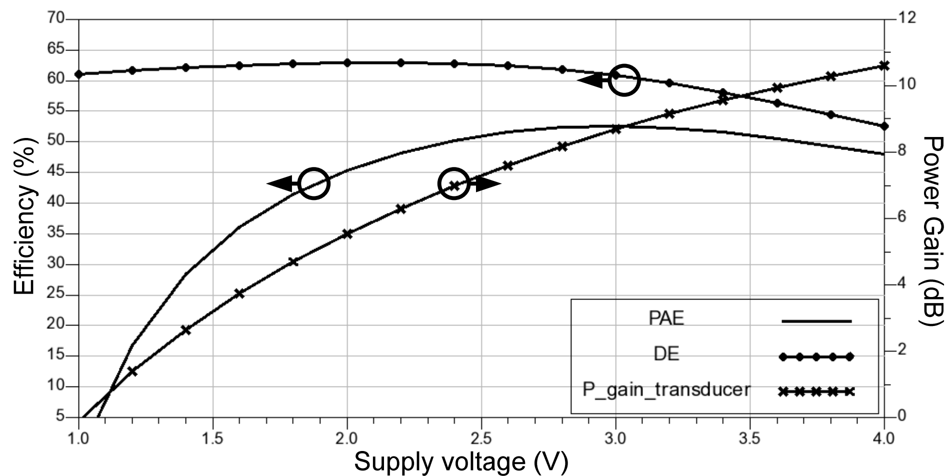


Figure 4.16: Power gain, PAE and DE vs supply voltage for constant input power.

Here, the input power is kept constant, 13dBm, for all supply values. This reduces efficiency at low supply voltages. To compensate for this effect, we can vary the input power at low voltages. Figure 4.17 shows output power (Pout) versus supply voltage at constant input power of 13dBm.

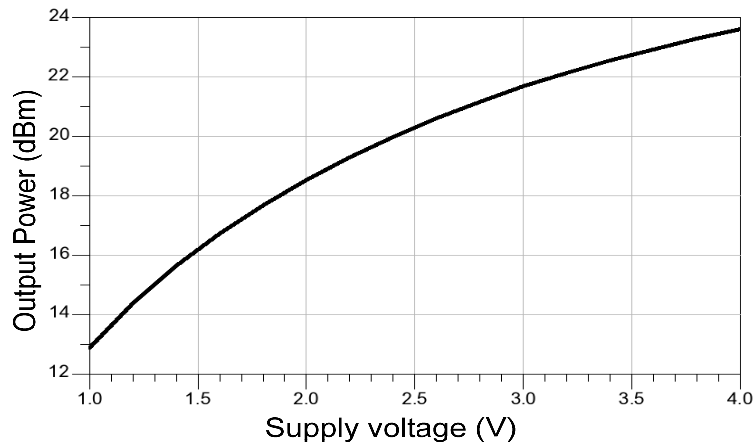


Figure 4.17: Output power versus supply voltage at constant input power.

PA performance versus frequency is also measured. More than 40% PAE is achieved for 600MHz bandwidth. Figure 4.18 shows PAE and gain versus frequency.

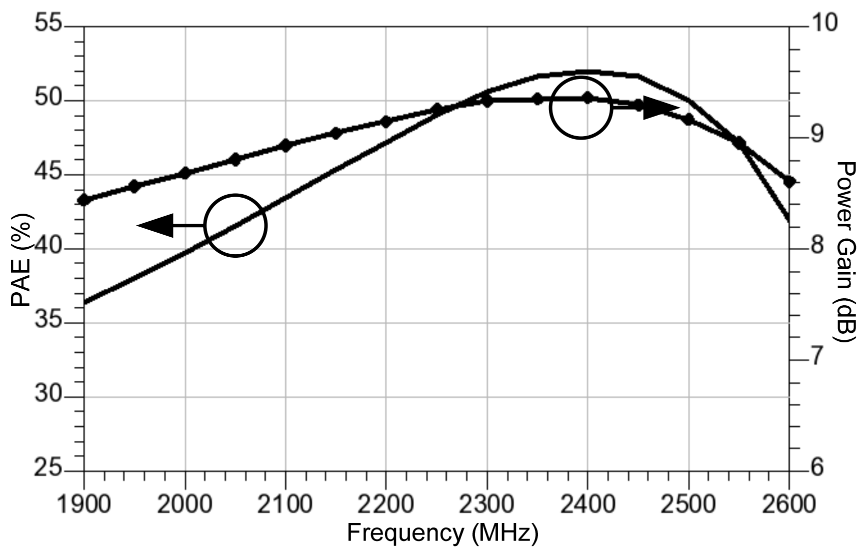


Figure 4.18: PAE and Gain versus Frequency.

Conclusion and Future Work

Multi-standard capability and battery life extension are the main challenging factors in designing modern wireless transceivers. The Software Defined Radio (SDR) is increasingly perceived as the most promising approach to cope with the multi-standard related requirements. Though, its practical implementation rests on the availability of multiband and broadband transceivers. Furthermore, the reduction of the power consumption of the radio systems called for sophisticated power amplification schemes in the transmitter side. This has been achieved using Drain modulation based Polar transmitter architecture and/or Doherty technique. Unfortunately, Doherty amplifier approach is inherently not very suitable for multi-frequency and multi-standard operation as it achieves high efficiency over only narrow frequency band. However, Polar architecture is better suited for multi-standards radio in general and more particularly for the realization of radio frequency power amplifiers that would meet the efficiency requirements. This thesis deals mainly with the design of multiband and broadband power amplifiers, in sub micron CMOS technology, to enable the development of Polar transmitters required for practical implementation of software defined and multi-standards radios. Designing such an amplifier at high frequencies requires good understanding of RF theory and nonlinear microwave circuits design process. PA performance is very sensitive to circuit parasitic; test procedure also can damage the circuit or degrade the performance. Therefore fabrication experiences could help in both test and design steps.

CMOS fabrication is an expensive and time consuming process, thus a discrete component based RF PA suitable for polar architecture is first designed, fabricated and tested. This PA was fabricated using a GaN HEMT transistor and operates at 2.5GHz. Its high measured efficiency versus supply voltage demonstrates that it can be used as a core amplifier in a drain modulation based architecture. Having this experience, two integrated RF CMOS PAs are designed. The first prototype is a concurrent dual-band, 2.4GHz/3.5GHz, PA fabricated in 0.13μm CMOS technology. Traditional multiband power amplifiers make use of a number of distinct single band PAs to serves the different targeted frequency bands. The proposed circuit utilized a single transistor and multiband matching networks to satisfy high efficiency at two separate frequencies. A power added efficiency of more than 40% is achieved at the two targeted

frequencies while delivering 18dBm output power. This PA prototype showed also interesting efficiency vs. supply voltage which confirmed its suitability for drain modulation based transmitters.

The alternative prototype for high efficiency and multi-standard operation was a broadband class E PA. Switching mode PAs are the best candidates for EER architectures. Among the different SMPA classes, we chose class E prototype to achieve broadband characteristics. PA performance versus frequency and supply voltage was simulated. PAE remains above 40% for 600MHz bandwidth. It also shows good performance versus supply voltage which is an important condition for drain modulation based transmitters.

This work could be continued by designing and fabricating the supply modulator for these two PAs. Since both amplifiers are fabricated using the same technology, a comparison between EER and ET methods can be done.

References

[1] Marian K. Kazimierczuk, "RF Power Amplifiers", A John Wiley and Sons, Ltd, Publication, 2008.

[2] Steve C. Cripps, "RF Power Amplifier for Wireless Communications", 2nd edition, Norwood, MA: Artech House, 2006.

[3] Andrei Grebennikov, "RF and Microwave Power Amplifier Design", McGraw-Hill, 2005.

[4] Han Gil Bae, "High-Efficiency Switching-Mode Class E Power Amplifier Using GaN Power transistor", Master of Science Thesis, University of Calgary, December 2007.

[5] Behzad Razavi, "RF Microelectronics", Prentice Hall, November, 1997.

[6] Thomas H Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", second edition, Cambridge University Press, 2004.

[7] Jennifer N. Kitchen, Ilker Deligoz, Sayfe Kiaei, Bertan Bakkaloglu, "Polar SiGe Class E and F Amplifiers Using Switch-Mode Supply Modulation", IEEE Transactions on Microwave Theory and Techniques, vol. 55, No. 5, May 2007.

[8] Feipeng Wang, Donald F. Kimball, Jeremy D. Popp, Annie Hueiching Yang, Donald Y. Lie, Peter M. Asbeck and Lawrence E. Larson, "An Improved Power-Added Efficiency 19-dBm Hybrid Envelope Elimination and Restoration Power Amplifier for 802.11g WLAN Applications", IEEE Transactions on Microwave Theory and Techniques, vol. 54, No. 12, December 2006.

[9] Feipeng Wang, Donald F. Kimball, Donald Y. Lie, Peter M. Asbeck and Lawrence E. Larson, "A Monolithic High-Efficiency 2.4-GHz 20-dBm SiGe BiCMOS Envelope-Tracking OFDM Power Amplifier", IEEE Journal of Solid-State Circuits, vol. 42, no. 6, June 2007.

[10] P. Reynaert and M. Steyaert, "A 2.45-GHz 0.13-µm CMOS PA with Parallel Amplification," in *IEEE Journal of Solid-State Circuits,* vol. 42, pp. 551-562, March 2007.

[11] U.K. Mishra, P. Parikh, Y.F. Wu, "AlGaN/GaN HEMTs: An overview of device operation and applications" Electrical & Computer Engineering Department, Engineering I, University of California, Santa Barbara, Santa Barbara, California 93106.

[12] Paul Grey, Paul, J, Hurst, Stephen, H, Lewis, Robert G Meyer, “Analysis and Design of Analog Integrated Circuits”, John Wiley and Sons Inc.

[13] David Johns, Ken Martin, “analog Integrated Circuit Design”, by John wiley and Sons Inc.

[14] Jongchan Kang, Ali Hajimiri, Bumman Kim, “A Single-Chip Linear CMOS Power Amplifierfor 2.4 GHz WLAN”, IEEE Int. Solid-State Circuits Conference, 2006.

[15] Gang Liu, Peter Haldi, Tsu-Jae King Liu and Ali M. Niknejad, “Fully Integrated CMOS Power Amplifier With Efficiency Enhancement at Power Back-Off”, IEEE Journal of Solid-State Circuits, Vol. 43, No. 3, March 2008

[16] C. P. Yue et al, “On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF ICs”, IEEE J. Solid State Circuits, v33, May 1998, pp. 743-52.

[17] Axel Schmidt and Stéphane Catala, “A Universal Dual Band LNA Implementation in SiGe Technology for Wireless Applications”, IEEE Journal of Solid-State Circuits, Vol. 36, No. 7, July 2001.

[18] Stephen Wu and Behzad Razavi, “A 900-MHz/1.8-GHz CMOS Receiver for Dual-Band Applications”, EEE Journal of Solid-State Circuits, Vol. 33, No. 12, December 1998.

[19] US Patent 6917815 - Concurrent dual-band receiver architecture.

[20] Junxiong Deng, Mark Chew, Sameer Vora, Marco Cassia, Thomas Marra, Kamal Sahota, “A dual-band high efficiency CMOS transmitter for wireless CDMA applications”, IEEE Radio Frequency Integrated Circuits Symposium 2007.

[21] H. G. Bae, R. Negra, S. Boumaiza, M. Ghannouchi, “High-efficiency GaN class-E power amplifier withcompact harmonic-suppression network”, Europian Microwave Integrated Circuit Conference, Munich Germany, October 2007.

[22] F. Giannini,G. Leuzzi, “Nonlinear Microwave Circuit Design”, John Wiley and Sons, Ltd, 2004.

[23] J. Kang, D. Yu, K. Min, and B. Kim, “A Ultra-High PAE Doherty Amplifier Based on 0.13μm CMOS Process”, IEEE Microwave and Wireless Components Letters, vol. 16, No. 9, September 2006.

[24] http://broadcastengineering.com.