Noise Analysis and Measurement for Current Mode and Voltage Mode Active Pixel Sensor Readout Methods

by

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A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Master of Applied Science
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2010

AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

A detailed experimental and theoretical investigation of noise in both current mode and voltage mode amorphous silicon (a-Si) active pixel sensors (APS) has been performed in this study. Both flicker (1/*f*) and thermal noise are considered. The experimental result in this study emphasizes the computation of the output noise variance, and not the output noise spectrum. This study determines which mode of operation is superior in term of output noise. The current noise power spectral density of a single a-Si TFT is also measured in order to find the suitable model for calculating the flicker noise. This experimental result matches Hooge's model. The theoretical analysis shows that the voltage mode APS has an advantage over the current mode APS in terms of the flicker noise due to the operation of the readout process. The experimental data are compared to the theoretical analysis and are in good agreement. The results obtained in this study apply equally well to APS circuits made using polycrystalline silicon (poly-Si) and single crystal silicon.

Acknowledgements

I would like to express profound gratitude to my supervisor, Professor Karim S. Karim for his invaluable support, encouragement, and supervision throughout my graduate study at the University of Waterloo. His moral support and continuous technical guidance enabled me to complete my work successfully. Also, I acknowledge my family for their unconditional support throughout my study period.

Much of the work in this thesis could not have been completed without the help, discussion, and cooperation from the following individuals: Dr. Nader Safavian who proposed this thesis project for me, Mohammad Yazdandoost for his help with the experimental setup, Hadi Izadi who essentially helped me with very aspect of my thesis work, and Amir Golden for his insightful suggestion on measuring methods.

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Chapter 1
Introduction

1.1 Purpose of the Research

The objective of this work is to perform a noise comparison of the three-transistor (3-T) current-mode APS and the 3-T voltage-mode APS. In a previous study by Antonuk [1], circuit simulation was used to show that the effect of flicker noise on charge transfer to the parasitic line capacitance is very low and thus not a limiting factor in noise performance of the voltage-mode APS. The theoretical analysis and experimental measurements reported in this work were carried out to verify these previously reported simulation results.

1.2 Solid State Electronic Imagers

In the early 70s, since the invention of Charge Coupled Devices (CCDs) by Willard Boyle and George E. Smith at AT&T Bell Labs, solid state electronic imaging devices replaced the electronic imaging tube. Two-dimensional arrays of CCDs had the highest image quality and reliability at the time. However, the biggest disadvantage of CCDs is their incompatibility with CMOS technology which makes integration difficult and the imagers expensive.

The idea of an array of Active Pixel Sensor (APS) was developed in late 60s where each pixel has both a sensor and one or more active transistors providing on-pixel gain. APSs succeeded passive pixel sensors (PPS) which have only a single switching transistor within

each pixel. Both PPS and APS circuits are fully compatible with CMOS technology. In 1995, Photobit Corporation became the first company to commercialize the APS technology for CMOS imager sensors.

1.3 Flat Panel Imagers for Large Area Imaging

For most optical imaging systems, optical lenses are usually used to project images of large objects on to smaller image-capturing devices (imagers). Unfortunately, it is more difficult to focus X-rays onto a small area and therefore X-ray imaging systems usually have imagers as large as the objects being imaged (Figure 1).

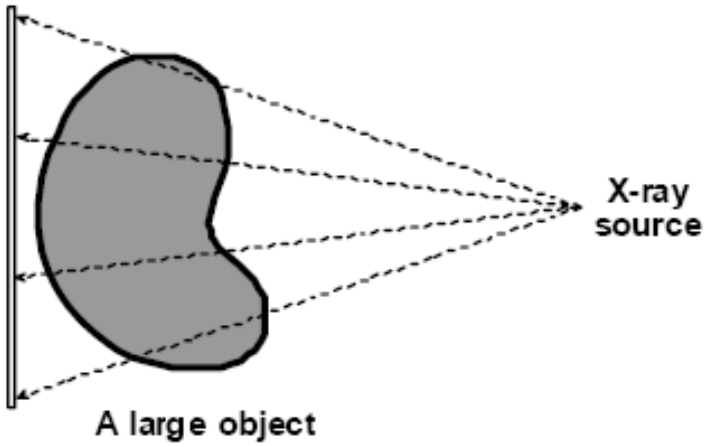


Figure 1: X-ray imaging with large area imager [3]

Today, X-ray imagers continue to use matrix of PPSs where the switching transistors are implemented with thin film transistor (TFT) technology which are connected to an X-ray sensor. These matrices are limited in their size and therefore to image a large object (a human body, for example) requires a number of these matrices to be connected forming a

large-area active matrix flat panel digital imager (AMFPIs) as is shown in Figure 2 (here "active" does not refer to the individual pixels). Currently, there are two architectures employed in large-area AMFPIs. The first is a low-cost linear imager which is used in every-day office electronics such as scanners and photocopiers. This type of imager usually has a very low speed and a complicated mechanical system associated with it. The second is the two-dimensional array architecture which is used in X-ray imagers. Thus, these use a one- or two-dimensional array of pixels, respectively, where the sensor in each pixel converts visible light or X-rays into an electrical charge. This charge is then integrated and stored in the sensor. To read the charge stored, the gate addressing switches are turned on row by row to connect the pixel to its corresponding data lines. The charges from the different columns are amplified by the charge amplifier, multiplexed, and transferred to a computer system for storage, processing, and display.

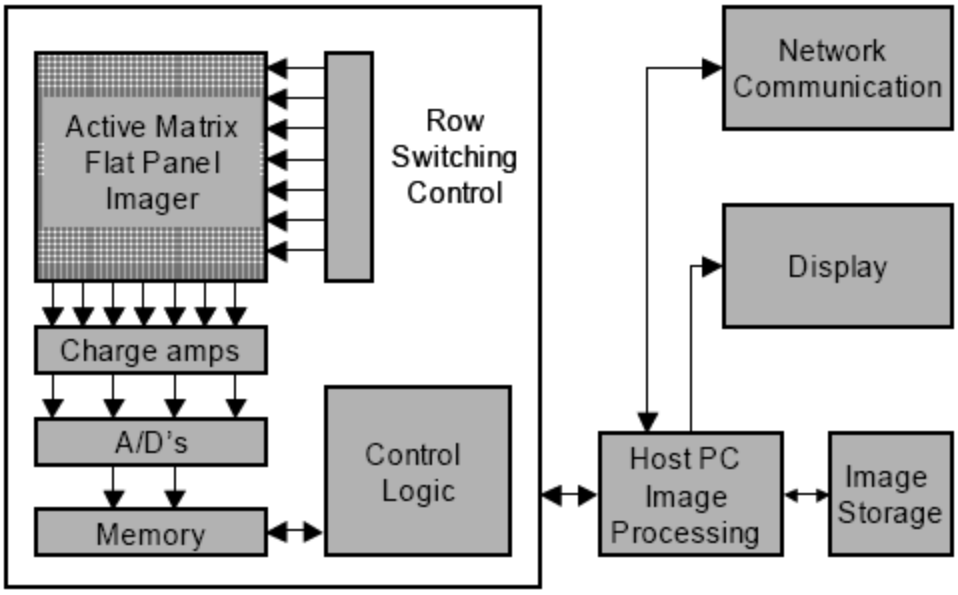


Figure 2: AMFPI Imaging System diagram [2]

To generate an electrical charge from an X-ray photon, two schemes are available. The first, indirect detection, converts the X-ray photon into a visible light photon by a phosphor layer. This visible light photon is then converted to an electrical charge by a photodetector such as a pin diode. The second, direct detection, absorbs the X-ray and converts it directly to an electrical charge by the X-ray photoconductor. The next subsection describes both of these schemes and elaborates upon the need for the indirect detection.

1.4 X-ray and X-ray Detection Schemes

1.4.1 Introduction to X-ray

X-rays are a form of electromagnetic radiation with wavelengths in the range of 10 to 0.01 nm. X-rays are able to penetrate solid objects making them very useful in diagnostic radiography. X-rays can be classified into soft X-rays and hard X-rays depend on their energy level, which is related to its penetration ability.

X-rays are generated by using high voltages to accelerate electrons to a very high velocity and then colliding them with a heavy metal target such as tungsten. When an electron hits the target, an X-ray can be created through two different processes. If there is enough energy associated with the electron to knock an electron from the inner orbit of the target metal, an electron from a higher energy would then fill the vacancy emitting a characteristic X-ray photon with a discrete spectrum. In the second process, the incoming electron collides with the target metal and the radiation is given off by the electron scattering. X-rays produced this way have a continuous spectrum.

1.4.2 Indirect and Direct X-ray Detection

The indirect detection method, as shown in Figure 3, consists of a photodetector integrated with a scintillator layer usually made of phosphor. The layer absorbs an incident X-ray and generates one or more electron-hole pairs. These pairs quickly recombine and emit visible or UV light photon which is then detected by a photodetector underneath the layer. One major problem with using this scheme is that it results in a significant scattering of the photons which greatly reduces the spatial resolution of the indirect detector. To solve this problem, special columnar scintillators are used.

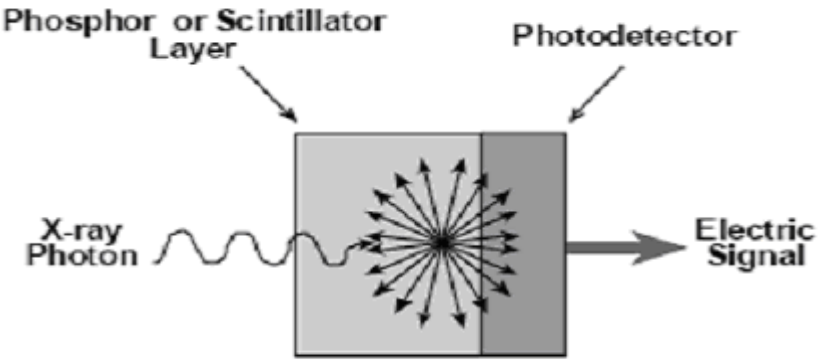


Figure 3: Indirect X-ray detection mechanism [3].

In the direct detection method, shown in Figure 4, a photoconductor is used to convert the X-ray photons directly to electron-hole pairs which are then collected by applying a high-bias voltage across the photoconductor layer. This, unfortunately, requires high voltages in the range of 5-10 kV to form the high electrical field needed to separate the electron-hole pairs. The photoconductor used in the direct detector should have a wide bandgap (> 2eV), a low value of W which is the energy needed to generate one electron-hole pair in the target material, and a higher carrier mobility-time product so that it would have a small value for

the dark current and is also able to generate more electron-hole pairs. Currently, for practical application in medical imaging, amorphous selenium (a-Se) is being widely used in large area flat panel detector. Due to its amorphous prosperities, a-Se based detectors can be made large in area relatively easily and inexpensively. Its electric properties, low dark or leakage current, of a-Se also render it suitable for X-ray imaging use.

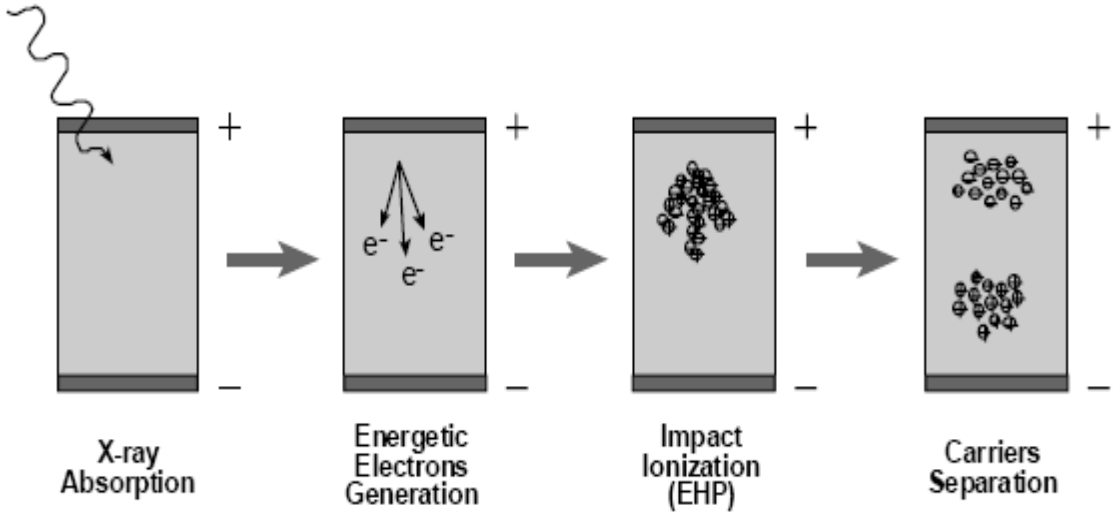


Figure 4: Direct X-ray detection scheme [3]

1.5 Material Properties of Amorphous Silicon

Amorphous-silicon thin-film transistor is commercially used today in large area flat-panel technology due to its flexibility and low cost. Amorphous silicon (a-Si) is different from crystalline silicon in that it lacks periodicity and long range order in the atomic structure. Although each silicon atom in a-Si prefers to bond with four neighbors, the relative angles between the bonds varies. Also not all silicon atoms in a-Si have four Si-Si bounds and thus many voids and incomplete bonds, namely dangling bonds are formed. To solve this problem, hydrogen which has one electron, is used to terminate the dangling bonds in a-Si

materials, as shown in Figure 5. Thus the a-Si materials commercially used are actually hydrogenated a-Si materials.

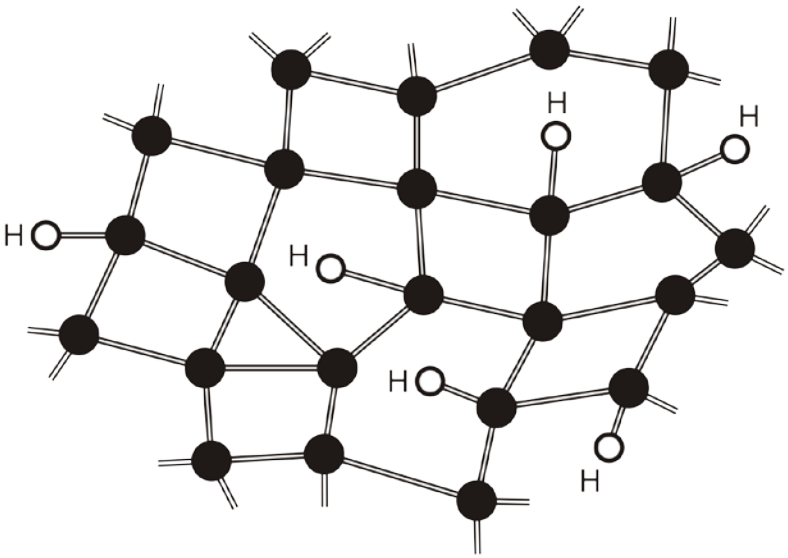


Figure 5: Diagram of amorphous silicon network with hydrogen atom passivation [4]

To better understand the performance and the operation of the a-Si TFTs, two very important points about a-Si must be noted. First, the carrier motilities in a-Si are two orders of magnitude lower compare to the crystalline silicon, with μ_n around 10-20 cm^2/Vs and μ_p around 1-10 cm^2/Vs. Second, there is a continuous distribution of both acceptor-like and donor-like states (together with localized states associated with the dangling bonds), within the forbidden gap of the a-Si. Because in a-Si, the wave functions do not have a well defined momentum, and there is a loss of k-conservation [4]， the energy bands cannot be described by the E-k relations but instead the density of the states versus energy distribution needs to be considered as shown in Figure 6 [5].

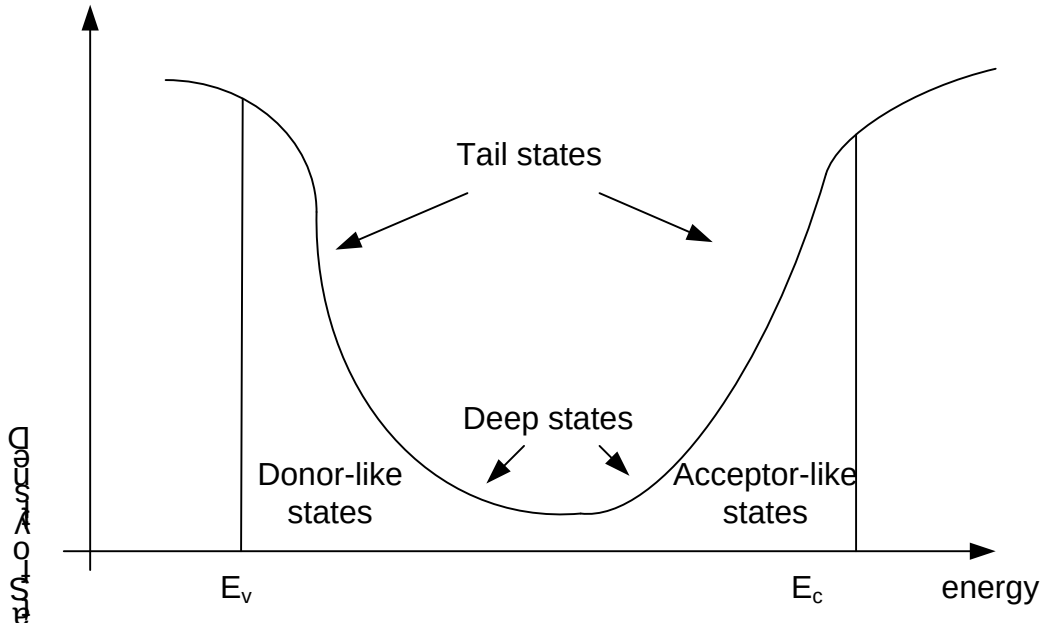


Figure 6: Energy distribution versus density of state

It is clear that the density of state distribution of a-Si is asymmetric, with the conduction band tail states having a narrower distribution than the valence band tail. The distributions of band-tail states are given by [6]:

$$g_{CBa} = g_{ta} \exp\left(\frac{E - E_c}{E_a}\right) \tag{1}$$

$$g_{VBd} = g_{td} \exp\left(\frac{E_v - E}{E_d}\right) \tag{2}$$

where g_{ta} and g_{td} are the densities of conduction band tail and valence band tail states, respectively. E_a and E_d are the slopes of the conduction and valence band tails, respectively. This together with the fact that electron mobility is higher than the hole mobility in a-Si results in *n*-channel transistors being much superior compare to the *p*-channel counterparts.

1.5.1 Metastability

A-Si TFTs exhibit a bias-induced shift (relative to the amount of time the TFTs are under stress) in the TFT threshold voltage V_T, which can have an adverse effect on the circuit performance if the circuit is not properly designed or operated. This problem is not significant when the TFT is used as a switch in applications such as a liquid-crystal display or a passive pixel sensor. However, metastability is one of the biggest challenges to overcome when it comes to the designing of the most analog application today where the TFTs have to withstand prolonged voltage stress on both the drain and gate terminals.

There are two mechanisms today that explain the inherent metastability associated with the TFTs. First, the carrier (charge) trapping in the gate insulator where the high density of defects can cause the charge to be trapped when the gate is stressed. This charge trapping in the insulator layer causes the shift in V_T. The charges are first trapped at the a-Si/SiN interfacial layer and then travel to deeper energy states inside the a-SiN layer. The second mechanism is explained by the point defect creation in the a-Si layer or the a-Si/SiN interface. When electrons accumulate and form a channel at the a-Si/SiN interface, these induced electrons are located in the conduction band tail states. These tail states are weak silicon-to-silicon bonds, when occupied by electrons, will break and form silicon dangling bonds, in

other words, the induced electrons creates deep state defects. These defects again can cause the V_T of the TFT to shift.

Carrier trapping and defect creation can be distinguished: Previous studies have shown [7] that charge trapping occurs at higher bias voltages and longer stress times. The shift in V_T can be either positive or negative depending on the type of the trapped charge (electrons or holes respectively). Alternatively, defect state creation mechanism dominates at the lower stress voltage and at shorter stress time. Studies done by Powell showed that defect state creation in the lower part of the energy gap is caused by positive bias; state removal from the lower part of the gap actually occurs for negative bias voltage [8]. Powell also determined that defect state creation has a power law time dependence and strong dependence on temperature. In contrast, charge trapping has logarithmic time dependence and weak dependence on temperature. The mathematical models for the two metastability mechanism are explained in the following paragraphs.

Defect state creation has a power law dependence over time. This relationship is empirically determined by both Powell and Jackson [7] [9] to be

$$\Delta V_T(t) = A(V_{ST} - V_{Ti})^{\alpha} t^{\beta} \tag{3}$$

where V_{ST} is the gate stress voltage, V_{Ti} is the V_T before the stress is applied, α is unity, and β is the experimental constant which is temperature dependent. Carrier trapping has a logarithmic time dependence which is represented by

$$\Delta V_T(t) = r_d \log(1 + t/t_0) \tag{4}$$

where r_d is a constant and t_0 is the characteristic value for time.

During the circuit operation, for the large area imagers, the gates of the TFTs are usually under pulsed bias stress and not constant DC bias stress. A pulse is characterized by its period and pulse width.

For positive pulse voltages, ΔV_T has been widely reported to be relatively independent of frequency. For a unipolar pulse, the effect of the frequency is just to reduce the total stress time of the TFT. During the off cycle, negative voltage is applied to the TFT to shift the V_T is the opposite direction. A commonly accepted formula [10][11][12] for modeling the frequency and pulse width dependence of ΔV_T on positive pulse bias is given by

$$\Delta V^{+}_{T\_AC}(t) = (T_{ON} / T_{Period}) \Delta V^{+}_{T}(t) \tag{5}$$

where T_{ON} is the ON time of the pulse and T_{period} is the period of the pulse. The formula for a negative pulse bias is more complicated:

$$\Delta V^{-}_{T\_AC}(t) = k_{V_T^-} \Delta V^{-}_{T}(t) \tag{6}$$

where

$$k_{V_T^-} = 1 - \frac{\tau_h}{T_{ON}} + \frac{\tau_h}{T_{ON}} \exp\left(-\frac{T_{ON}}{\tau_h}\right) \tag{7}$$

and τ_h is the effective hole accumulation time constant.

1.5.2 Amorphous Thin Film Transistor Structure

A schematic structure of a-Si TFT is shown in Figure 7 [13]. This structure is the inverted-staggered structure where the source/drain metals are at the opposite sides of the gate metal. Above the source and drain metals is the heavily P-doped (n+) a-Si layer. Next to it is the intrinsic a-Si layer. The gate insulator is usually made of hydrogenated amorphous silicon nitride. The a-Si TFT here works in the accumulation mode. When the positive voltage is applied to the gate metal, electrons will accumulate near the gate insulator to a-Si layer interface to form the conduction channel. If a positive voltage is then applied to the drain electrode, the current will flow from the drain to the source through P-doped (n+) a-Si, intrinsic a-Si, and the channel.

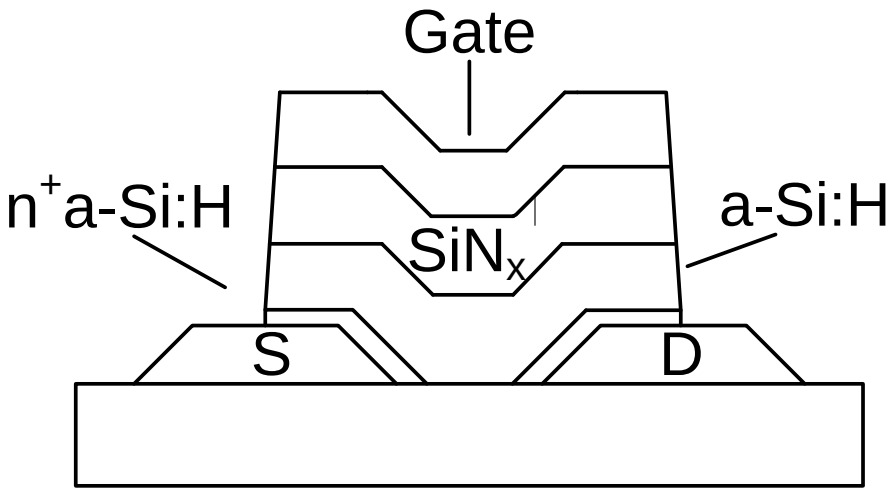


Figure 7: Structure of a top gate a-Si TFT

Chapter 2
Pixel Architectures for Large Area Digital Imaging

2.1 Passive Pixel Sensor Architecture

2.1.1 Introduction

Today, the industry standard architecture for flat panel imagers is the passive pixel sensor (PPS) [14][15]. It is probably the simplest structure and offers very compact design for the high-resolution imaging applications. The PPS shown in Figure 8 consists of a detector, which can be either a photo-diode integrated with a scintillator or a photoconductor, connected to a switch transistor. Here C_{PIX} is the sum of the sensor capacitance and parasitic capacitances (gate to drain capacitance of the switching TFT) at the detector node. It is passive in a sense that the TFT functions as passive switch in the pixel.

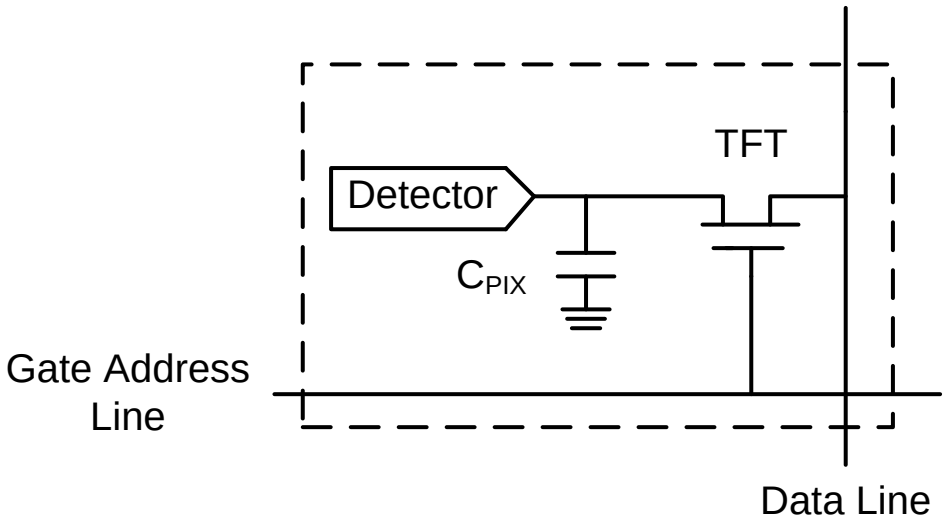


Figure 8: Passive pixel sensor architecture

For the PPS architecture shown in Figure 8, the gate of TFT is connected to a common row gate addressing line where the source of the TFT is connected to the data line. During the readout period, the pixel array is activated row by row. The signal stored in each pixel is then transferred through the data line to the column charge amplifiers.

2.1.2 Operation

PPS operates in two modes: Integration mode and readout/reset mode. The detail descriptions of the operation modes are explained this section.

Integration mode: The switching TFT is OFF and the signal charge generated in the detector as a result of the incident X-rays integrates on the C_{PIX} proportional to the incoming X-ray radiation.

Readout/Reset mode: Following the integration, the TFT is turned ON and the stored signal charge is transferred from C_{PIX} to a column charge amplifier via the data line. At the end of the readout period, the charge on C_{PIX} is reset to zero and the pixel is ready for the next integration. During the integration period, the TFT should be OFF and not conducting. However, a small leakage current in the order of fA for the commercially made a-Si TFTs still flows through the TFT channel and thus changes the voltage across the C_{PIX} and corrupts the signal. The problem with leakage current is more significant for in-house fabricated TFTs. The leakage current can be reduced with proper off voltage applied to the gate. During the readout period, the TFT is biased in the linear region to have a low ON resistance for quick charge transfer.

2.1.3 Readout and Reset Speed

In this section, we will try to estimate the speed of reset and readout of the PPS structure. The circuit diagram and small signal circuit model of a PPS pixel connected a charge amplifier are shown in Figure 9 and Figure 10. The TFT is modeled by its overlap capacitances and the on resistance in linear region. The pixel capacitance is given by

$$C_{PIX} = C_{\det} + C_{st} + C_{gd} \tag{8}$$

where C_{det} is the detector capacitance, C_{st} is the pixel storage capacitance which is added if the total capacitance at the detector node is not large enough to store the charge generated by the incident X-rays (also reduce the voltage level at the detector node), and C_{gd} is the gate to drain capacitance of the TFT.

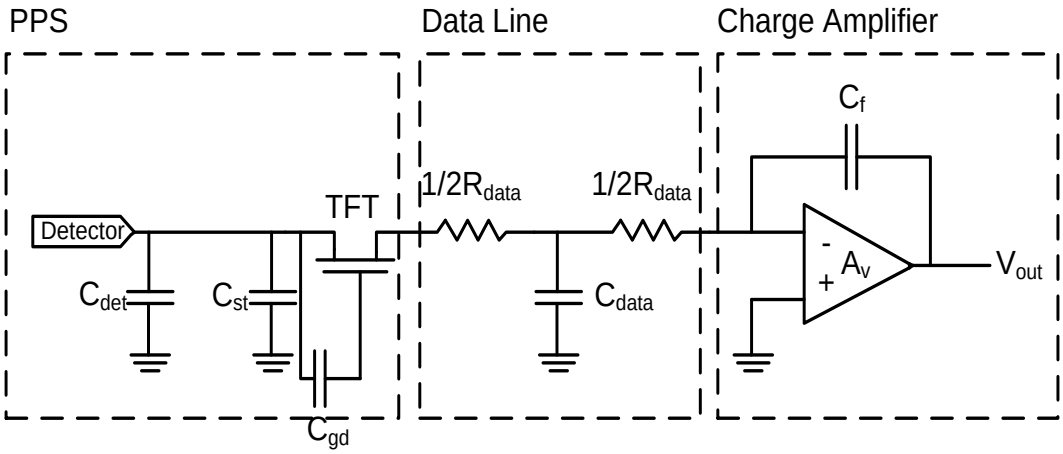


Figure 9: PPS structure connecting to a column charge amplifier

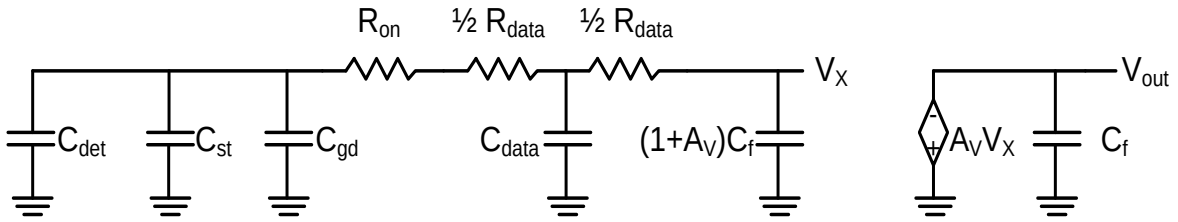


Figure 10: Small signal model for a PPS structure connecting to a column charge amplifier

The data line is modeled by a line resistance and capacitance, that is, R_{data} and C_{data} respectively. A zero-time constant approximation method can be used to estimate the time constant associated with transfer of the charge from pixel capacitor to the charge amplifier feedback capacitor. From Figure 10, the charge transfer time constant is

$$\tau = \sqrt{\tau_1^2 + \tau_2^2} = \sqrt{C_{PIX}^2 (R_{on} + R_{data})^2 + C_{data}^2 R_{data}^2 / 4}\,. \tag{9}$$

The above equation can be further simplified because R_{on} of the TFT is considered to be much larger than the value of R_{data} and therefore

$$\tau = C_{PIX} \times R_{on}\,. \tag{10}$$

The ON resistance of the TFT in linear mode can be approximated by the equation

$$R_{on} = \left[\frac{W}{L} \mu_{EFF} C_G (V_{GS} - V_T) \right]^{-1}. \tag{11}$$

Here W and L are the channel width and length of the TFT, respectively, μ_{EFF} is the effective carrier mobility; C_G is the gate capacitance per unit area; V_{GS} is the gate-source voltage of the

TFT; and V_T is the threshold voltage of the TFT. The photoconductor capacitance C_{det} is given by

$$C_{det} = \frac{\varepsilon_0 \times \varepsilon_{\det} \times A_P}{t_{\det}} \tag{12}$$

where A_P is the pixel area and t_{det} is the thickness of the photoconductor. Assuming the photoconductor here is amorphous selenium (a-Se), typical values are $\varepsilon_0 = 8.85 \times 10^{-12}$F/m, $\varepsilon_{det} = 6.5$, $A_P = 250 \times 250$ μm^2, $t_{det} = 1$ mm would result in a value of around 3 fF for the C_{det}. If a storage capacitor of 1 pF is used, then the total pixel capacitance C_{PIX} would be approximately equal to 1pF. For a W/L = 160 um/20 um, μ_{EFF} = 0.5 cm^2 / Vs, V_{on} = 12 V, V_T = 2 V, C_G = 25 nF/cm^2, and R_{on} is around 1 MΩ. Thus, τ can be calculated to be around 1μs. For a sufficient charge transfer, 5× time constants are generally needed which results in a pixel readout time of 5 μs for each row, which is fast enough for real-time application. However, the main disadvantage of the PPS is that it is very susceptible to the coupling noise from various external components, making it unsuitable for low X-ray dose application such as fluoroscopy.

2.1.4 Voltage Sensing PPS

An inverting voltage amplifier can be used instead of the charge amplifier in the PPS structure shown in Figure 11. [2]. In this configuration, the signal charge is transferred from C_{PIX} to the data line capacitance, $C_{data,}$ is given by

$$Q_{data} = Q_{sig} \times \left[\frac{C_{data}}{C_{data} + C_{PIX}} \right]. \tag{13}$$

In this case, if Cdata is small compared to CPIX, most of the signal charge will not be transferred to Cdata; which will result in signal loss. In order to have good charge transfer efficiency, it is important to have Cdata ≫ CPIX. However, if this is indeed the case, then the voltage developed at the input of the inverting amplifier will be very small, making it vulnerable to noise, thus not suitable for low input signals such as the ones encountered in diagnostic medical X-ray imaging applications.

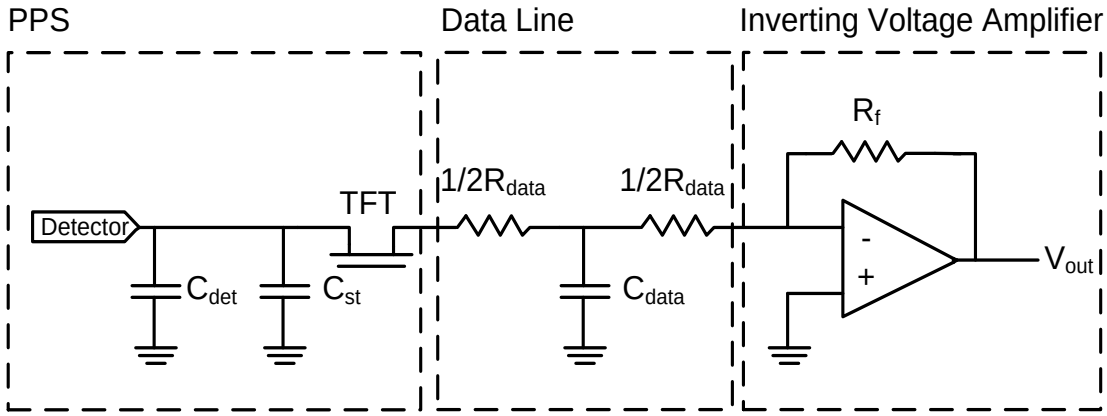


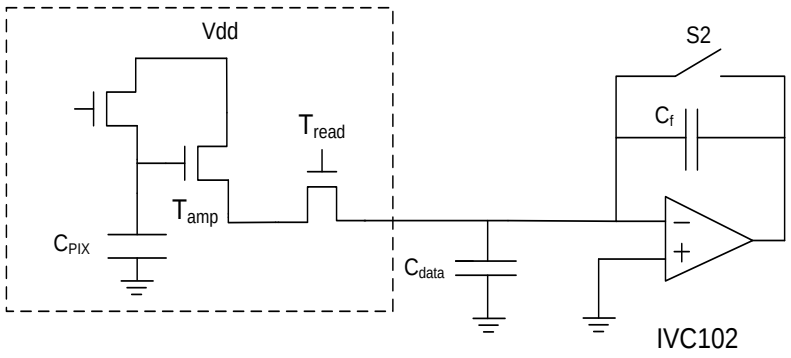
Figure 11: PPS structure connecting to a column voltage amplifier

2.2 Active Pixel Sensor

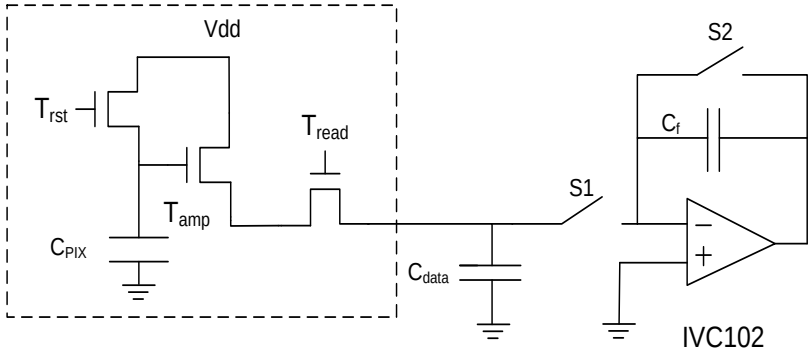
2.2.1 Introduction

To improve the signal-to-noise ratio (SNR), active pixel sensor (APS) circuitry is developed where the signal at the detector node is converted to voltage or current using an on-pixel amplifier which results in improved noise and/or readout speed performance. Currently, there are two common methods for reading out the signal in APS. In one method, the output of the APS is read in terms of current (C-APS) where as in the other method the

output is read in terms of voltage (V-APS). The circuit diagrams of both V-APS and C-APS are shown in Figure 12.



(a)



(b)

Figure 12: (a): circuit diagram of 3-T APS in current mode. (b): circuit diagram of 3-T APS in voltage mode

2.2.2 Current Mode APS

In the C-APS, the source follower circuit generates current which is then integrated by the external charge amplifier. C-APS operates in three modes:

Reset mode: The reset TFT (T_{rst}) is turned on to reset the pixel capacitor (C_{PIX}) to the V_{rst} value. C_{PIX} is a combination of detector capacitance and the gate capacitance of the amplifying TFT (T_{amp}).

Integration mode: After the C_{PIX} node is reset to the proper value, both T_{rst} and T_{read} are then turned off. The incoming X-ray signal discharges the C_{PIX} capacitance by ΔQ and the voltage level on C_{PIX} drops by ΔV that is proportional to ΔQ.

Readout mode: In the read period, T_{read} is turned on and the current that is generated by the APS pixel flows into the charge amplifier. The charge amplifier then integrates this small current on the feedback capacitor (C_f) and the output voltage (V_{out}) of the charge is proportional to both ΔV and the integration time (T_s).

The small signal model for deriving the output current of C-APS is shown in Figure 13. The output current has been derived in previous study [3] to be,

$$i_{out} = \frac{1 + KR_{ON}(V_{PIX} - V_T) - \sqrt{1 + 2KR_{ON}(V_{PIX} - V_T)}}{KR_{ON}^2} \qquad (14)$$

Where $K = C_G \mu_{EFF} W/L$ of the amplifying TFT, V_{PIX} is the voltage at the detector node after the X-ray is absorbed which equals to $V_{rst} - Q_{sig}/C_{PIX}$.

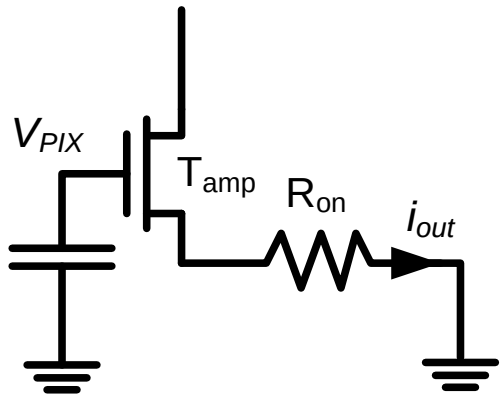


Figure 13: Circuit diagram used to derive the output current for the C-APS

Double sampling is usually used to extract the signal current Δi_{out},

$$\Delta i_{out} = i_{out}\Big|_{Q_{sig}=0} - i_{out}\Big|_{Q_{sig}\neq 0} = \frac{1}{R_{ON}}\left(1-\frac{1}{\sqrt{1+2KR_{ON}(V_{rst}-V_T)}}\right)\frac{Q_{sig}}{C_{PIX}} \tag{15}$$

The gain of the C-APS can then be calculated depending on the type of the column amplifier used. If the charge amplifier is used, the output current is integrated on the feedback capacitor of the charge amplifier. The gain of the C-APS in this case is given by

$$Gain = \frac{\Delta V_{out}}{Q_{sig}} = \frac{t_{\text{int}}}{C_{PIX}C_f R_{ON}}\left(1-\frac{1}{\sqrt{1+2KR_{ON}(V_{rst}-V_T)}}\right). \tag{16}$$

For linearity of the gain, previous study [16] has shown

$$\gamma = \frac{di_{out}}{dh\nu} = \frac{dQ_{sig}}{dh\nu}\frac{dV_{rst}}{dQ_{sig}}\frac{di_{out}}{dV_{rst}} \tag{17}$$

where $h\nu$ is the input illumination and γ is the sensitivity of output current with respect to the illumination representing the linearity. The sensitivity analysis shows that the first term in

equation (17) is constant if the charge generated by the detector is linear with respect to the incoming illumination. The second term is linear if the signal charge is linearly dependent on the voltage charge, i.e.

$$\Delta Q_{sig} = \Delta V_{rst} \times C_{PIX} . \tag{18}$$

In another word, C_{PIX} has to be constant. For the last term in equation (17), the I-V relationship of the TFT has to be linear,

$$i_{out} + \Delta i_{out} = K / 2(V_G + \Delta V_G - V_T)^2 . \tag{19}$$

Expand and collect the small signal term gives

$$\Delta i_{out} = K(V_G - V_T)\Delta V_G + (K / 2)(\Delta V_G)^2 . \tag{20}$$

So for linear operation, the non-linear term in equation (20) has to be sufficiently small, that is $\Delta V_G \gg 2(V_G - V_T)$ which means the change in voltage at the detector node due to the X-ray must be small. This also explains why C-APS is suitable for low dose application such as fluoroscopy but not higher dose modalities.

One problem with non-linear pixel readout is that the correlated double sampling mechanism cannot be performed using hardware as it is typically done with active matrix imagers [2]. A couple of methods can be used to improve the inherent nonlinearity of the C-APS. A possible solution is to implement software correction, where a frame memory is used to store each C-APS pixel's transfer function so the nonlinearity can be corrected. However this means a longer frame time is required to make all the gain adjustments. To make this software

correction even more complicated, the inherent V_T shift problem associated with TFTs will cause the pixel transfer characteristics to shift. This again requires repeated correction of the pixel transfer function at regular basis which further increases the readout time associated with the imager. In section 2.4, a hybrid pixel architecture based on PPS and C-APS is introduced which can operate in both PPS mode and APS mode. It offers on-pixel gain, fast readout, and high dynamic range depending on the mode it operates in.

One thing to consider when using a charge amplifier is to ensure that the bias current does not saturate the charge amplifier. Usually the feedback capacitor of the charge amplifier is chosen to be very small in order to have higher gain. For example, a particular charge amplifier with 1 pF feedback capacitor and maximum output voltage of 15 V will get saturated in 10 μs if the bias current is 1.5 μA. To prevent this problem, a current sink circuitry or current bleeder can be used as shown in Figure 14.

As mentioned in section 2.1.4, a trans-impedance amplifier can also be used instead of a charge amplifier. In this case, the gain of C-APS becomes

$$Gain = \frac{\Delta V_{out}}{Q_{sig}} = \frac{R_f}{C_{PIX} R_{ON}} \left(1 - \frac{1}{\sqrt{1 + 2KR_{ON}(V_{rst} - V_T)}} \right). \quad (21)$$

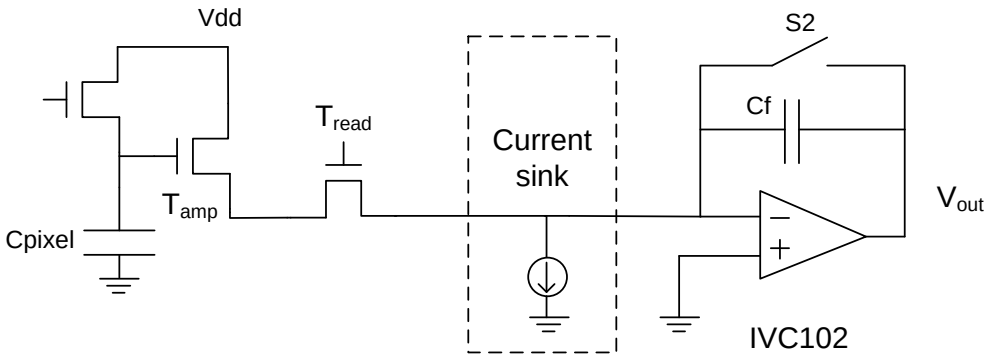


Figure 14: C-APS with column current sink

2.2.3 Voltage Mode APS

The circuitry for V-APS is very similar to the C-APS except one extra switch (see Figure 12 b). V-APS also operates in three modes:

Reset mode: The reset TFT (T_{rst}) is turned on to reset the pixel capacitor (C_{PIX}) to the proper V_{rst} value.

Integration mode: After the C_{PIX} node is reset to the proper value, both T_{rst} and T_{read} are then turned off. The incoming X-ray signal discharges the C_{PIX} capacitance by ΔQ and the voltage level on C_{PIX} drops by ΔV that is proportional to ΔQ.

Readout: There are two phases in the readout period for V-APS. In the first phase, S1 is open, S2 is closed, and T_{read} is turned on so the small current generated by the APS pixel is flowing to the data line capacitor (C_{data}) until it is charged up to $V_g - V_T$ of the two-transistor structure consist of T_{amp} and T_{read}. The time required to charge up the C_{data} depends on the size of C_{data}

and resistance of T_{read}. In the second phase, S1 is closed, S2 is open, and T_{read} is turned off. The charge stored on the C_{data} instantly transfers to the C_f and the output voltage is developed.

The output voltage of the V-APS is approximated by

$$V_{out} = \frac{Q_{sig}}{C_{PIX}} \times A_v \times \left(1 + \frac{C_{data}}{C_f}\right). \tag{22}$$

Here A_v is the voltage gain from detector node to the data line node V_{data} and can be assumed to be unity. So the gain of the V-APS is then given by

$$Gain = \frac{V_{out}}{Q_{sig}} = \frac{1}{C_{PIX}}\left(1 + \frac{C_{data}}{C_f}\right). \tag{23}$$

2.3 Two-Transistor Pixel Architecture

The three-transistor APS architectures introduced in sections 2.2.2 and 2.2.3 have good noise performance, fast readout. However, for some specific applications such as mammography where very high resolution images are required, the pixel size (~50 μm) becomes a challenge for the existing three-transistor APS structure. The two-transistor (2T) APS has been proposed to address this challenge by reducing the number of both transistor and control lines. Currently there are three different types of 2T APS: gate switching, drain switching, and source switching.

2.3.1 Gate Switching 2T APS

The 2T gate switching APS architecture is shown in Figure 15 [3]. It consists of an X-ray detector, a reset TFT, TR, which is used to reset the detector node to proper value, an amplifying TFT, T_A, which is used to provide on-pixel amplification, and a pixel capacitor

C_{PIX}, which is used to store the charge produced by the detector while also provides access to the gate of amplifying TFT.

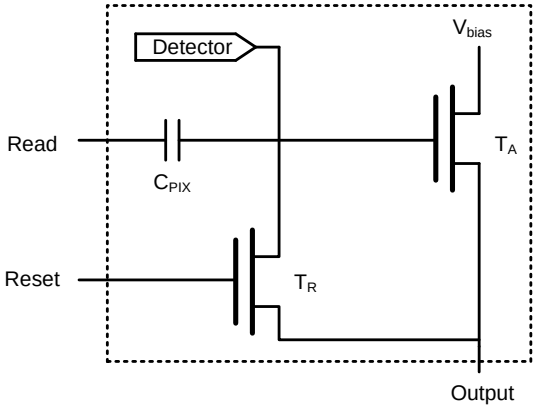


Figure 15: Gate switching 2T APS

Similar to the three-transistor APS, gate switching 2T APS also operates in three modes as shown in Figure 16: resetting, integration, and readout. In the resetting mode, T_R is turned on and T_A is turned off to reset the voltage at the detector node to zero by discharging node to the ground. During the integration mode, both T_A and T_R are kept off and the detector node voltage is modulated by the charged generated by the detector. In the readout mode, a pulse is applied to the read node which is capacitively coupled to the gate of the T_A by the pixel capacitor, C_{PIX}. This in turn increases the gate-source voltage of T_A beyond its threshold voltage while preserving the charge at the gate, which provides a non-destructive readout. The total number of input/output lines for this architecture is four.

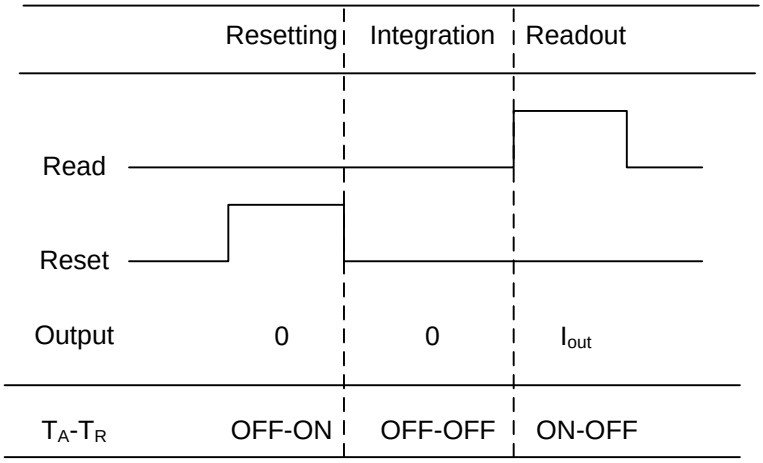


Figure 16: Operation modes for 2T gate switching APS [3]

2.3.2 Source Switching 2T APS

The second configuration for 2T APS is the source switching APS, which is shown in the Figure 17. In this architecture, the read control line is connected to the source of the T_A instead of the C_{PIX} in the case of gate switching. Total number of input/output lines for this architecture is five, which is one more compare to the 2T gate switching APS

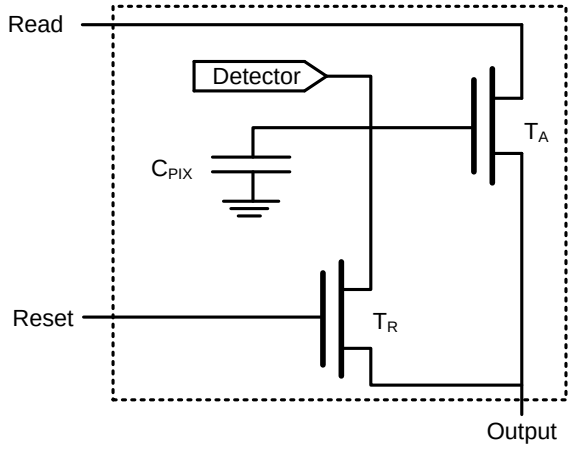


Figure 17: Source switching 2T APS [3]

The circuit also works in the same three operation modes (Figure 18) as the 2T gate switching APS. In the reset mode, T_R is turned on to reset the detector node to a preset voltage V_{RST}, which is controlled by the drain voltage of the T_A. T_A is kept off during the reset period because both the drain and the source of the TFT are kept high. During the integration period, the signal charge created by the detector will change the voltage level at the detector node. Both TFT in this period are kept in the off state. In the readout period, the source voltage is set to zero, which turns on the T_A by making its V_{gs} to be positive. One thing to notice is that the source of the T_A is actually capacitively coupled to its gate through the parasitic capacitance C_{gs}. So when the source of T_A is switched from V_{bias} to zero, there will be a voltage drop of $V_{bias} \times \frac{C_{gs}}{C_{eff}}$ on its gate where C_{eff} is approximated equal to $C_{gs} + C_{PIX}$.

In conclusion, C_{PIX} must be sufficiently large compare to the C_{gs} in order to have large V_{gs} on T_A in readout period. This in turn requires a large physical space for a large C_{PIX}.

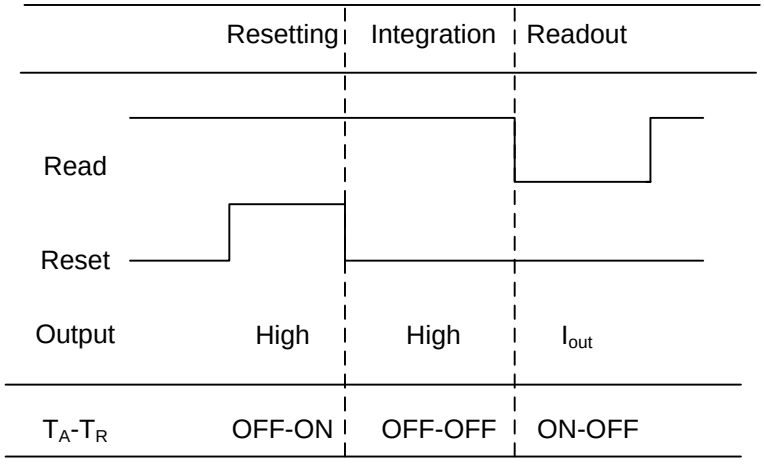


Figure 18: Operation modes for 2T source switching APS [3]

2.3.3 Drain Switching 2T APS

The third type of 2T APS is the drain switching configuration which is shown in Figure 19. In this architecture, the drain and the gate of the T_A are capacitively coupled by the pixel capacitor $C_{PIX.}$ One advantage of this design is that the C_{PIX} can simply be made by extending the gate-drain overlap area of T_A, which saves additional pixel space. This configuration has only three input/output lines, which is the fewest among all the 2T APS introduced in this section. The operation modes of drain switching and gate switching APS are very similar (Figure 20). During the reset period, T_R is turned on to reset the detector node to zero. During the integration period, T_A is kept off since both its drain and the source voltage are kept at zero. For readout, the read signal V_{read} is applied directly to the drain of the T_A which also increase the gate voltage of T_A by $V_{read} \times \frac{C_{PIX}}{C_{eff}}$ where C_{eff} is approximately equal to $C_{PIX} + C_{gd}$ (T_A). One of the advantages of this architecture is that during the integration period, the gate, drain, and source of the T_A are kept at low voltage which prevents the V_T shift of the TFT from happening.

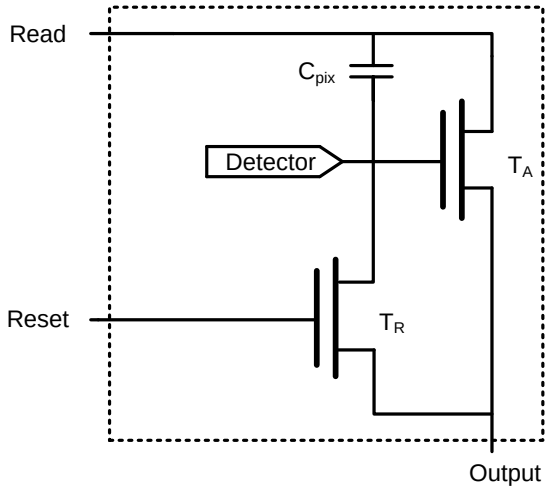


Figure 19: Source switching 2T APS [3]

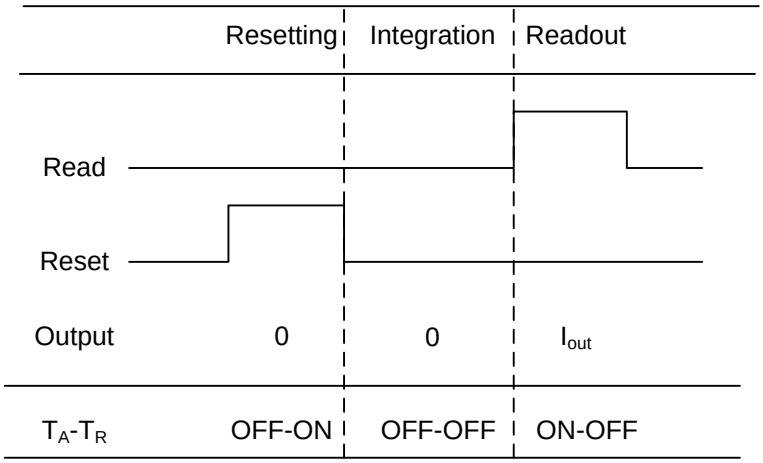


Figure 20: Operation modes for 2T drain switching APS [3]

2.4 Hybrid Pixel Design

The hybrid pixel architecture is developed based on both PPS and C-APS structures. The APS architecture, with the on-pixel gain, is more suitable for low dose medical application such as fluoroscopy. For large dose applications such as radiography and mammography, when the signal charge is large, then the nonlinearity associated with the C-APS becomes a problem, in which case the PPS becomes a better option. The hybrid pixel architecture can provide on-pixel gain, real time readout and high dynamic range depending on which mode it works in. Figure 21 shows the schematic of a hybrid pixel sensor. For the active mode, the RDP TFT is turned off, and the circuit essentially acts as a C-APS. In this mode, the output of the pixel is connected to the column *n*. For the passive operation, both RESET and RDC are kept off, and the hybrid pixel sensor acts as a PPS where the output is connected to column $n - 1$.

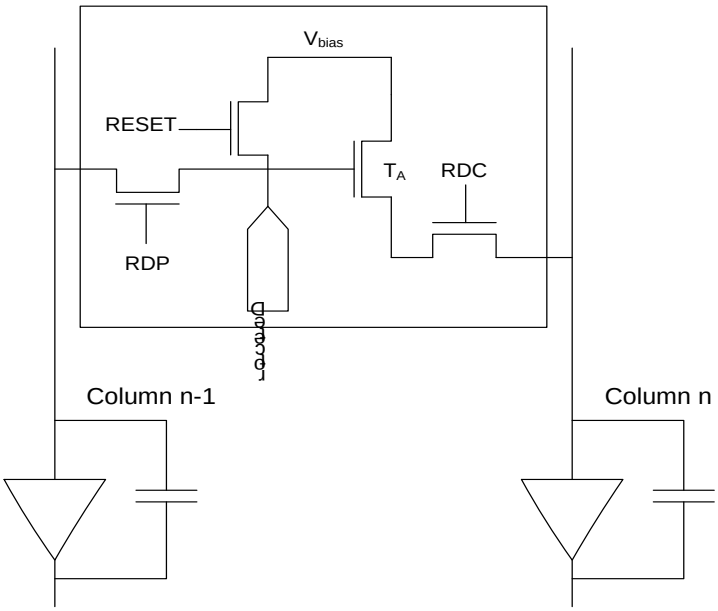


Figure 21: 4T hybrid pixel sensor [18]

2.4.1 Linearity and Gain

The hybrid pixel sensor has the same linearity as the C-APS or PPS depending on which mode it works in. Alternatively, charge gain in the active mode of operation is different compare to the charge gain of the C-APS since for the hybrid pixel sensor, effective C_{PIX} is increased due to the additional parasitic capacitance added by the RDP TFT. According to equation (16), the gain of the pixel will decrease with the increased C_{PIX}. This increase of C_{PIX} can be compensated by minimizing the aspect ratio of the RDP TFT. According to previous study [18], a switching TFT with aspect ratio of 50 μm/10 μm will only add around 20 fF of parasitic capacitance which reduces the charge gain by only 2% and still has a PPS readout time of less than 3μs for a C_{PIX} = 1 pF, V_G = 20 V, V_{T_RDP} = 3.2 V, and μ = 0.8 cm^2/Vs.

Chapter 3
Noise Analysis of Current Mode and Voltage Mode APS

3.1 Introduction

In this section, we first introduce the concept of the electronic noises in circuits. Then we present the theoretical noise analysis for both readout methods: C-APS and V-APS. TFT leakage noise, circuit thermal noise, circuit flicker noise, data line noise and the charge amplifier noise are considered. Other noise sources such as photoconductor shot noise, transistor leakage noise, reset noise are not included in this study partially due to the fact these noise sources are common to both readout methods. Both the photoconductor shot noise and transistor leakage noise are under 100 electrons and the reset noise associated with the APS is around 400 electrons according to previous study [25].

3.2 Introduction to Electrical Noise

The noise analysis done in this thesis study deals only with the electrical noise caused by small current and voltage fluctuations that are generated by the electronic devices.

3.2.1 Thermal Noise

In electronic devices, thermal noise is generated by the random motion of electrons and it is directly proportional to the temperature. For a resistor *R*, the thermal noise can be represented by either a voltage source or a current source:

$$v^2 = 4kTR\Delta f \tag{24}$$

$$i^2 = 4kT\frac{1}{R}\Delta f \tag{25}$$

where k is Boltzmann's constant, T is the temperature in kevin, and Δf is the bandwidth.

For a long channel MOS transistor, because the channel material is resistive, the thermal noise can be represented by a current noise source between the drain and source, that is

$$i_d^2 = 4kT(\gamma gm)\Delta f \tag{26}$$

where γ is a parameter for the transistor that has a value of 1 in the linear region and 2/3 in the saturation region.

For TFT, studies done by Boundry, Antonuk, and Karim [19][20] have shown that thermal noise in TFT is similar to MOS transistor thermal noise and can be modeled by equation (26) where gm in this case is

$$gm = \frac{dI_{DS}}{dV_{DS}} = M(V_{GS} - V_T)^n \tag{27}$$

where n is a process dependent parameter and

$$M = \mu_{EFF} C_G \left(\frac{W}{L}\right). \tag{28}$$

3.2.2 Flicker Noise

Flicker noise is caused by the traps associated with the defects in the crystal structure of the devices. It is always associated with the direct current and has the current spectral density of the form

$$i^2 = K\frac{I^a}{f^b}\Delta f \tag{29}$$

where K is a constant associated with a particular device, f is the frequency, a is a constant in the range between 0.5 to 2 [21], and b lies between 0.8 and 1.4 in general [2]. If b is unity, then the noise spectral density has a $1/f$ frequency dependency (hence the name $1/f$ noise). Thus the flicker noise is most significant in the lower frequency range and at higher frequencies it is usually overshadowed by the thermal noise.

Two different theories which explain the origin of the flicker noise have been developed since its discovery. The first model, which is called the numbers fluctuation model, was proposed by McWhorter [22]. The model states that the cause of the noise is due to the fluctuations in the majority carrier density and interface trap density close to the semiconductor surface. The model, however, does not account for the flicker noise observed in materials that have no interface traps

The second theory was proposed by Hooge and Hoppenbrouwers in the 1960s and is generally known as the mobility fluctuation model [23]. The theory explains the cause of the flicker noise is the mobility fluctuations within a homogenous and conducting medium. Hooge proposed the empirical formula for the noise current power spectral density:

$$i^2 = \alpha_H I^2/(N_{tot} f^a) \tag{30}$$

for the transistor where I is the drain current of the transistor, N_{tot} is the total number of charge carriers in the medium and α_H is the empirical coefficient. The value of this coefficient is dependent on the impurity scattering in a material [24].

The flicker noise densities derived from both theories for TFT are listed in the Table 1 where L is the channel length and V_T is the threshold voltage.

Table 1: Flicker noise spectral densities for number fluctuation and mobility fluctuation models for TFT

	Number fluctuation model	Mobility fluctuation model
i^2_{linear}	$\frac{k}{f}\frac{\mu}{C_{OX}L^2}\left(M\left(V_{GS}-V_T\right)^{n-1}V_{DS}^2\right)$	$\frac{\alpha_H}{f}\frac{q\mu}{L^2}\left(M\left(V_{GS}-V_T\right)^{n}V_{DS}^2\right)$
$i^2_{saturation}$	$\frac{k}{f}\frac{\mu}{C_{OX}L^2}\left(M\left(V_{GS}-V_T\right)^{n+1}\right)$	$\frac{\alpha_H}{f}\frac{q\mu}{L^2}\left(M\left(V_{GS}-V_T\right)^{n+2}\right)$

The experimental results from this study, which are presented in the section 4.1.2, show that the Hooge theory of flicker noise accounts for our in-house fabricated a-Si TFTs.

3.3 Noise in Current Mode APS

The analysis here for the C-APS is a modification of previous work from our group [25]. Figure 22 shows the small signal model used for the noise analysis. The read TFT is modeled by its drain to source resistance. The input capacitance of the charge amplifier is ignored since it is connected to the negative input of the charge amplifier which is the virtual ground in this configuration.

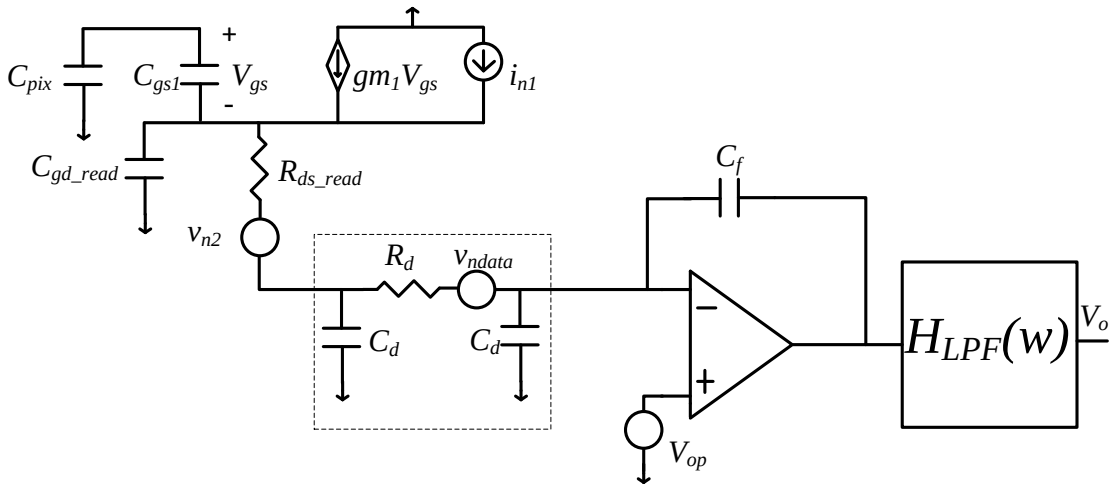


Figure 22: Small signal model of C-APS during readout

Performing the nodal analysis at the source of the amplifying TFT gives

$$V_S sC_{gd\_read} + \frac{V_S .sC_{PIX}C_{gs1}}{C_{PIX}+C_{gs1}} - gm_1V_{gs} + \frac{V_S}{r_o} - i_{n1} = -i_s . \tag{31}$$

factoring out $V_s s$ term gives

$$V_S s\left(C_{gd\_read} + \frac{C_{PIX}C_{gs1}}{C_{PIX}+C_{gs1}}\right) - gm_1V_{gs} + \frac{V_S}{r_o} - i_{n1} = -i_s . \tag{32}$$

The relationship between the output current of the APS and the input current of the charge amplifier can be written as

$$i_s = i_x(s\frac{C_d}{2}R_d + 1). \tag{33}$$

The impedance looking into the read TFT is defined as

$$R_{in} = R_{ds\_read} + \frac{1}{\frac{1}{R_d}+\frac{sC_d}{2}} = \frac{2R_{ds\_read} + R_{ds\_read}sC_dR_d + 2R_d}{2+sC_dR_d}. \tag{34}$$

Since $R_{ds\_read} \gg R_d$, equation (34) can be simplified to

$$R_{in} \approx \frac{2R_{ds\_read} + R_{ds\_read} sC_d R_d}{2 + sC_d R_d} \approx \frac{R_{ds\_read}(2 + sC_d R_d)}{2 + sC_d R_d} = R_{ds\_read}. \tag{35}$$

We then write V_{gs} in term of V_S, that is

$$V_{gs} = \frac{-V_S sC_{PIX} C_{gs1}}{C_{PIX} + C_{gs1}} \left(\frac{1}{sC_{gs1}} \right) = \frac{-V_S C_{PIX}}{C_{PIX} + C_{gs1}} \tag{36}$$

and

$$V_S = i_s R_{ds\_read}. \tag{37}$$

Substitute equation (36) and (37) into (32),

$$si_s R_{ds\_read} \left(C_{gd\_read} + \frac{C_{PIX} C_{gs1}}{C_{PIX} + C_{gs1}} \right) + gm_1 i_s R_{ds\_read} \frac{C_{PIX}}{C_{PIX} + C_{gs1}} + \frac{i_s R_{ds\_read}}{r_o} - i_{n1} = -i_s \tag{38}$$

Re-arrange the equation and substitute equation (33) in,

$$i_x \left(s\frac{C_d}{2} R_d + 1 \right) \left[sR_{ds\_read} \left(C_{gd\_read} + \frac{C_{PIX} C_{gs1}}{C_{PIX} + C_{gs1}} \right) + gm_1 R_{ds\_read} \frac{C_{PIX}}{C_{PIX} + C_{gs1}} + \frac{R_{ds\_read}}{r_o} + 1 \right] = i_{n1}$$

Now we can relate the output voltage with the i_x,

$$i_x = -V_o sC_f \tag{39}$$

Finally, we find the relationship between the noise source i_{n1} and the output voltage V_o,

$$-V_o sC_f \left(s\frac{C_d}{2} R_d + 1 \right) \left[sR_{ds\_read} \left(C_{gd\_read} + \frac{C_{PIX} C_{gs1}}{C_{PIX} + C_{gs1}} \right) + gm_1 R_{ds\_read} \frac{C_{PIX}}{C_{PIX} + C_{gs1}} + \frac{R_{ds\_read}}{r_o} + 1 \right] = i_{n1} \tag{40}$$

Further simplification can be made to equation (40). First of all, the term $\frac{R_{ds\_read}}{r_o}$ can be ignored since $r_o \gg R_{ds\_read}$. Now expand the equation (40),

$$-V_o sC_f\left(s\frac{C_d}{2}R_d+1\right)\frac{\left(sR_{ds\_read}C_{gd\_read}(C_{PIX}+C_{gs1})+sR_{ds\_read}C_{PIX}C_{gs1}+gm_1R_{ds\_read}C_{PIX}+C_{PIX}+C_{gs1}\right)}{C_{PIX}+C_{gs1}}=i_{n1} \tag{41}$$

Then we make some estimation for the capacitance and resistance values. The drain to source resistance has been estimated in section 2.1.3 to be around 1 MΩ. C_{PIX} is the design parameter and in this case is set to 500 fF. C_d and R_d are the data line capacitance and resistance, respectively. C_d is 300 pF and R_d is 26 kΩ in our model. gm_1 is the transconductance of the transistor which has a value in the range of μA/V. the C_{gd_read} is the gate to drain overlap capacitance of the read TFT which can be calculated by,

$$C_{gd\_read}=\frac{\varepsilon_0\varepsilon_{SiN}}{t_{SiN}}A_{overlap}$$

where $\varepsilon_0 = 8.85\times10^{-12}$ F/m, $\varepsilon_{SiN} = 6$, $A_{overlap}$ (read TFT) = 200×10 μm^2, $A_{overlap}$ (amplifier TFT) = 400×10 μm^2, t_{SiN} = 350 nm. Thus the resistance and capacitance values can be calculated and are:

$$R_{ds\_read}\approx 1M\Omega,$$

$$C_{PIX}\approx 500\,fF,$$

$$C_{gd\_read}\approx 300\,fF, \text{ and}$$

$$C_{gs1}\approx 600\,fF.$$

Substitute the values above into the equation (41), it can be simplified to

$$V_o = i_{n1}\frac{C_{PIX}+C_{gs1}}{sC_f(C_{PIX}+C_{gs1}+gm_1R_{ds\_read}C_{PIX})}. \tag{42}$$

Similar analysis is used to get the transfer function for the noise source of the read TFT, v_{n2}.

Now let's consider the noise coming from the data line (Figure 22), which is modeled using a π model composed of a line resistor and two line capacitors. Performing nodal analysis again gives

$$\frac{v_{ndata}}{\left(\frac{1}{s\frac{C_d}{2}+R_d}\right)} = i_x \tag{43}$$

and

$$V_o = i_x \frac{1}{sC_f}. \tag{44}$$

Solving (44) for i_x and substituting it into (43), we get

$$\frac{v_{ndata}\frac{sC_d}{2}}{1+\frac{R_d sC_d}{2}} = V_o sC_f. \tag{45}$$

Solve for V_o, we get

$$V_o = \frac{v_{ndata}C_d}{(2+R_d sC_d)C_f}. \tag{46}$$

The transfer functions of various noise sources referred to the output node are given by the three equations

$$\frac{V_o}{i_{n1}} = \frac{C_{pix}+C_{gs1}}{sC_f(C_{pix}+C_{gs1}+g_{m1}r_{ds\_read}C_{pix})}, \tag{47}$$

$$\frac{V_o}{v_{n2}} = \frac{gm_1 C_{pix}}{sC_f(C_{pix}+C_{gs1}+gm_1 r_{ds\_read}C_{pix})}, \tag{48}$$

$$\frac{V_o}{v_{ndata}} = \frac{C_d}{(2 + R_d SC_d)C_f}. \tag{49}$$

Since the noise sources are independent and uncorrelated, the total thermal noise at the output node of the charge amplifier from the two transistors is given by

$$V_{o,thermal}^2 = \left\{ v_{n2}^2 (gm_1 C_{pix})^2 + i_{n1}^2 (C_{gs1} + C_{pix})^2 \right\} \int \left| \frac{1}{sC_f (C_{pix} + C_{gs1} + gm_1 r_{Ts} C_{pix})} \right|^2 H_{LPF}^2(\omega) df \tag{50}$$

where $H_{LPF}^2(\omega)$ is low pass filter associated with the data acquisition system connected to output of the charge amplifier. The thermal noise sources are given by

$$i_{n1}^2 = 4kT\left(\frac{2}{3} gm_1\right) \tag{51}$$

and

$$v_{n2}^2 = 4kTR_{ds\_read}. \tag{52}$$

For flicker noise, the thermal noise densities can be replaced with the flicker noise densities. Hooge's model for the flicker noise current spectral density in both linear and saturation regimes is given by [26][27],

$$i_{linear,f}^2 = \frac{\alpha_H q \mu_{eff} C_{ox} W (V_{GS} - V_T) V_{DS}^2}{f L^3} \tag{53}$$

$$i_{sat,f}^2 = \frac{\alpha_H q \mu_{eff} C_{ox} W (V_{GS} - V_T)^3}{2 f L^3} \tag{54}$$

For the charge amplifier noise, refer to the small signal model shown in Figure 23.

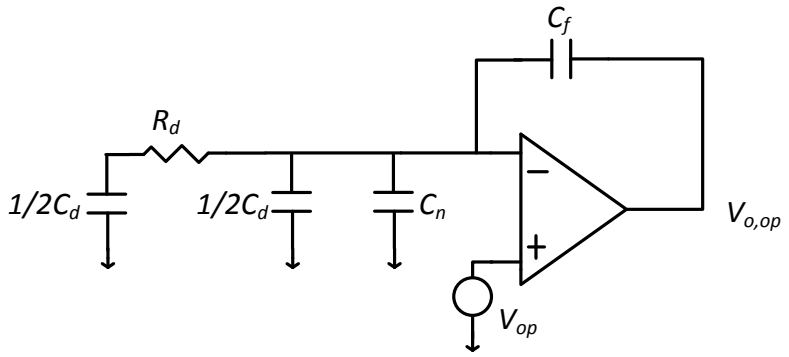


Figure 23: Noise model for the charge amplifier

$$Z_1 = R_d + \frac{1}{1/2sC_d} = \frac{sCR_d + 2}{sC_d} \tag{55}$$

$$Z_2 = \frac{1}{s(1/2C_d + C_n)} \tag{56}$$

$$Z_{in} = \frac{1}{\frac{1}{Z_1} + \frac{1}{Z_2}} = \frac{2(sC_d R_d + 2)}{2sC_d + s(C_d + C_n)}$$

where Z_{in} is the input capacitance at the inverting input of the charge amplifier.

Now the transfer function for a non-inverting amplifier is

$$V_{o,op} = (1 + \frac{Z_f}{Z_{in}})v_{op}, \tag{57}$$

where Z_f is the feedback capacitance.

$$V_{o.op} = \left\{1 + \frac{1}{sC_f}\left(\frac{2sC_d + s(C_d + C_n)(sC_dR_d + 2)}{2(sC_dR_d + 2)}\right)\right\} v_{op} \tag{58}$$

which simplifies to

$$V_{o,op} = \left\{1 + \frac{2C_d + sC_d^2R_d + 2C_d + sC_nC_dR_d + 2C_n}{C_f(2sC_dR_d + 4)}\right\} v_{op}\,. \tag{59}$$

Now, since $2sC_dR_d \ll 4$, equation (59) can be simplified to

$$V_{o,op} \approx \left\{\frac{s(C_d^2R_d + C_nC_dR_d) + 4C_d + 2C_n + 4C_f}{4C_f}\right\} v_{op}\,. \tag{60}$$

Using the same assumption made on page 38, finally we get

$$V_{o,op} = \left(\frac{C_d + \frac{1}{2}C_n + C_f}{C_f}\right) v_{op}\,. \tag{61}$$

So the charge amplifier output noise voltage is given by

$$V_{o,op}^2 = \left\{\left\{V_{op}^2\left(\frac{C_d + \frac{1}{2}C_n + C_f}{C_f}\right)^2\right\} H_{LPF}^2(\omega)df\right. \tag{62}$$

where V_{op}^2 is the charge amplifier noise voltage and is given by

$$V_{op}^2 = \left(1 + \frac{f_c}{f}\right) V_{th}^2 \tag{63}$$

and V_{th}^2 is the thermal noise density and f_c is the corner frequency of the charge amplifier.

After calculating the output noise voltage, we can get the input referred noise in terms of electrons by using

$$\sigma_t = \frac{\sqrt{V_o^2 C_{eff}}}{A_v q} \tag{64}$$

where A_v is the voltage gain, C_{eff} is the effective capacitance at the detector node, and q is the electron charge:

$$A_v = G_m T_s / C_{FB} \tag{65}$$

where G_m is the transconductance of the C-APS circuit, T_s is the integration time, and C_{FB} is the feedback capacitance on the charge amplifier. Table 2 shows the calculated input referred noise based on the analysis shown above.

Table 2: Total input referred noise from different noise source

Input Referred Noise (electrons)	C-APS
T_{amp} thermal noise	140
T_{amp} flicker noise	336
T_{read} thermal noise	125
T_{read} flicker noise	220
Data line thermal noise	749
Charge op-amp thermal noise	228
Charge op-amp flicker noise	319

3.4 Noise in Voltage Mode APS

For the V-APS, Figure 24 shows the equivalent small signal circuit of the pixel during readout mode. In the first phase of the readout period, the data line capacitor will eventually get charged up to $V_{gs} - V_T$ of the T_{amp} and when this steady state is reached, the direct current flowing through the transistors is assumed to be zero. The only noise present is the thermal noise which is stored on the C_{data}, given by

$$V_n^2 = \frac{kT}{C_{data}}. \tag{66}$$

In the second phase of the readout period (Figure 24b), the noise stored on the C_{data} is then transferred to the output node of the charge amplifier. The noise gain function is given by,

$$V_n^2 = \beta V_{o,thermal}^2 \tag{67}$$

where

$$\frac{1}{\beta} = 1 + \frac{C_{data}}{C_f} \tag{68}$$

so the thermal noise at the output of the charge amplifier is given by

$$V_{o,thermal}^2 = \left(1 + \frac{C_{data}}{C_f}\right)^2 \frac{kT}{C_{data}}. \tag{69}$$

One interesting point here is that the output referred noise is proportional to the data line capacitance C_{data}. Assume $C_{data} \gg C_f$, equation (69) can be simplified to

$$V_{o,thermal} \approx \frac{C_{data}}{C_f}\sqrt{\frac{kT}{C_{data}}} \propto \frac{\sqrt{C_{data}}}{C_f}. \tag{70}$$

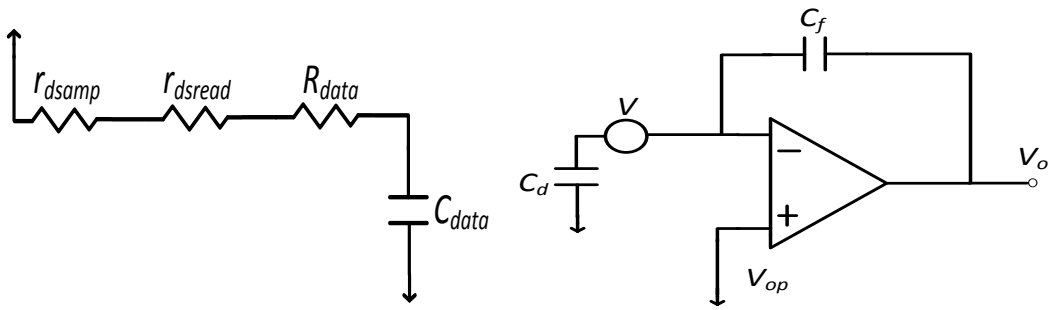
Assuming that the feedback capacitance is constant; a large data line capacitance would give you higher output referred noise according to equation (70). Now let us consider the input referred noise

$$V_{input\_referred\_thermal} = \frac{V_{o,thermal}}{gain} = \frac{\left(1+\frac{C_{data}}{C_f}\right)\sqrt{\frac{kT}{C_{data}}}}{\frac{1}{C_{PIX}}\left(1+\frac{C_{data}}{C_f}\right)} = \frac{\sqrt{\frac{kT}{C_{data}}}}{\frac{1}{C_{PIX}}}. \quad (71)$$

Again, assume that $C_{data} \gg C_f$, and C_{PIX} and C_f are design constant, we can deduce the relationship

$$V_{input\_referred\_thermal} \propto \frac{1}{\sqrt{C_{data}}} \quad (72)$$

between the input referred noise and the data line capacitance. This shows that the input referred noise of the V-APS is actually inversely proportional to the square root of the data line capacitance.



(a) (b)

Figure 24: Small signal model of V-APS during (a) Phase 1 of the readout, and (b) Phase 2 of the readout.

The total input referred noise for V-APS is calculated and summarized in Table 3.

Table 3: Total input referred noise from different noise source

Input Referred Noise (electrons)	C-APS
kT/*C* noise	12
Charge op-amp thermal noise	228
Charge op-amp flicker noise	319

The analysis in this chapter shows that the V-APS has a substantial advantage in term of input referred noise. At the same time it is also shown that the noise in V-APS is independent of the bias voltage for the APS structure, which is another advantage over C-APS.

Chapter 4
Noise Measurement

In this chapter, the measurement setup and the measurement results for both single TFT and APS are presented.

4.1 Noise Measurement of a Single TFT

4.1.1 Measurement Setup

The current noise power spectrum measurements are performed on a single TFT fabricated at the University of Waterloo with the aspect ratio of 400 μm/20μm. The setup for measuring the noise of a single a-Si TFT is shown in Figure 25. High amp hour DC batteries are used to drive the TFT and also to provide the power for the PerkinElmer Model 5182 low-noise current preamplifier. The TFT, batteries, low noise capacitors and low noise resistors are put in a shielded box and the entire system excluding the spectrum analyzer is placed in the Faraday cage. In this setup, a capacitance is used to block the DC current from entering the low noise current preamplifier. This protects the current preamplifier and at the same time also allows us to use the highest gain setting on the current preamplifier. The noise current, which is AC in nature, will flow into the current preamplifier since the input impedance of a current amplifier is much smaller compare to the drain resistance of the TFT under test.

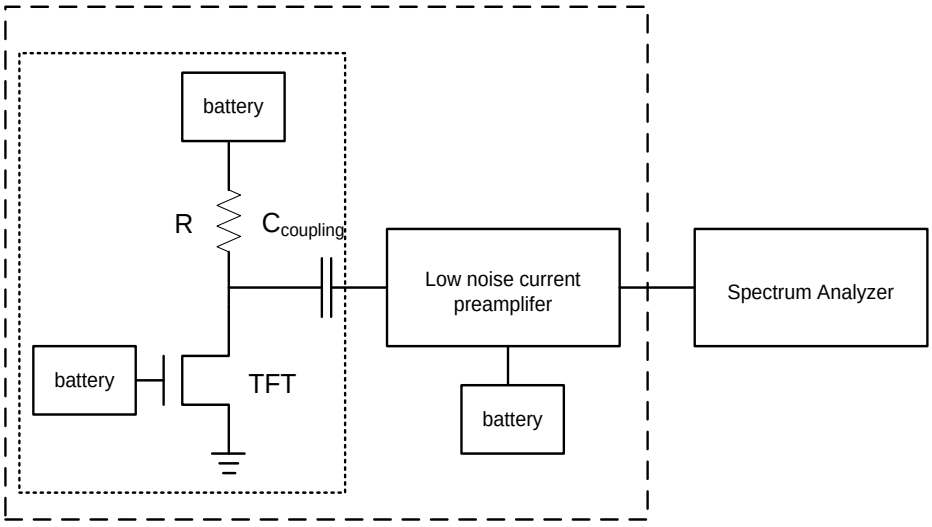
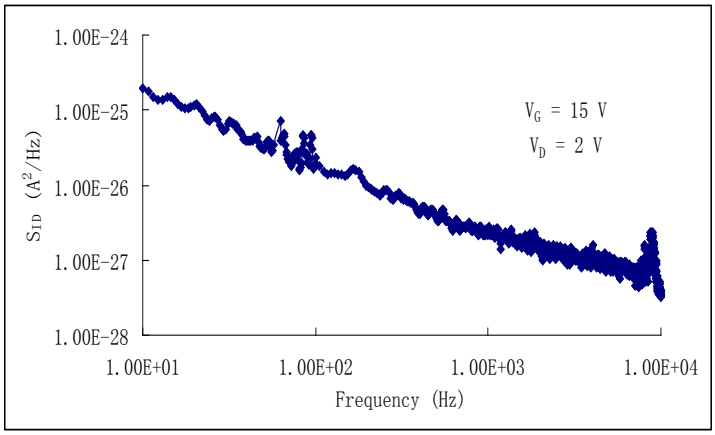


Figure 25: Noise experiment setup for a single TFT

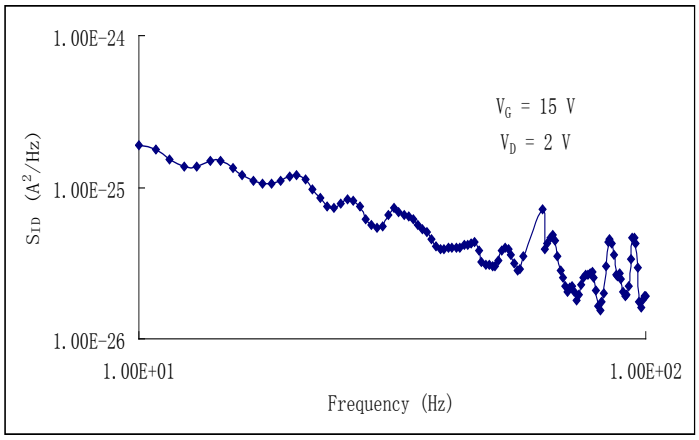
The gate voltage and drain voltage are set to be 15 V and 2 V, respectively. The current noise power spectrum is constructed from narrowband measurement averaged at last 50 times and higher for low frequency measurements. For each measurement, the data acquisition starts after a 15 minutes delay to allow the V_T shift of the TFT to stabilize. The bias current is monitored at the same time as the noise spectrum measurements are taken.

4.1.2 Flicker Noise

The noise current power spectral density of one single TFT is measured using the aforementioned experimental setups and are shown in Figure 26.



(a)



(b)

Figure 26: Noise current power spectral density for an a-Si TFT in the linear mode. (a): Noise spectra ranges from 10 Hz to 1 MHz. (b): Noise spectra in low frequency range (10 Hz to 100 Hz).

From the mobility fluctuation equation list in Table 1 in section 3.2.2, it is clear that

$$i_{linear}^2 \propto (V_{GS} - V_T)^n . \tag{73}$$

Also for a transistor in the linear region

$$i_{d,linear} \propto (V_{GS} - V_T)^n . \tag{74}$$

Then

$$i_{linear}^2 \propto i_{d,linear} \tag{75}$$

Figure 27 shows measurements of the noise power spectrum at 100 Hz. The current noise power spectral density is shown to be proportional to the drain current with a slope of 0.9 which indicates that the flicker noise associated with the in-house fabricated TFTs appears to concur with the mobility fluctuation theory.

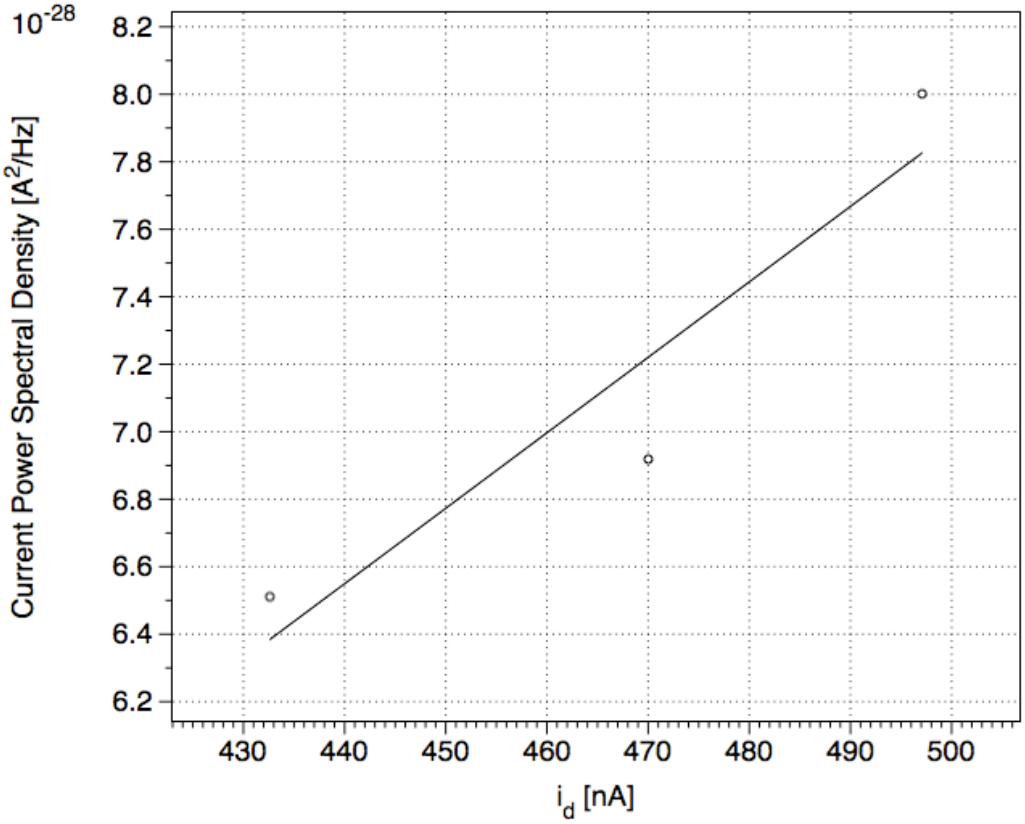
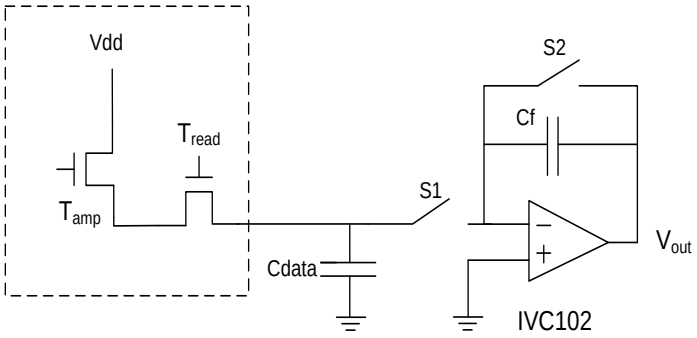


Figure 27: Bias current vs. current power spectral density.

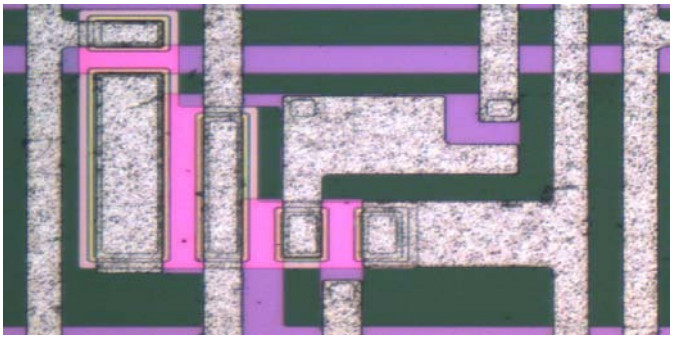
4.2 Noise Measurement for C-APS and V-APS

4.2.1 Test Structure and Measurement Setup

The APS pixel architectures used in this study are shown in Figure 28. The reason we do not include T_{rst} in our analysis is because the reset operation is common to both current and voltage mode APS circuits, thus the reset noise associated is the same for both modes of the operation. The a-Si TFTs used in this study were fabricated in-house at the University of Waterloo. T_{amp} and T_{read} have *W*/*L* ratios of 400 μm/20 μm and 200 μm/20 μm, respectively. The pixel storage capacitance is designed to be 0.5 pF. The line capacitance C_{data} is modeled by using a 400 pF discrete capacitor. Notice this is an over-estimation of the data line capacitance for the worst case scenario. This is also one of the major reasons why the noise measurement results presented in this study are higher than the theoretical calculations. The charge amplifier used here is the low noise IVC 102 with the built-in feedback capacitor set to be 30 pF.



(a)



(b)

Figure 28: (a) Circuit diagram of the device under test (DUT). (b) Micrograph of the in-house fabricated 3 TFT structure

The experimental setup is shown in Figure 30. It consists of a Wavetek model 195 universal wave generator and a National Instrument 6115 data acquisition card (NI card). Voltage buffers powered by batteries are used to reduce the output noise from the wave generator. The system is placed in a Faraday cage and the measurements are recorded under dark conditions at room temperature. Two hundred samples were used for each output noise variance calculation.

In the original experiment, an Agilent oscilloscope is used instead of the NI Card due to its easy of use. The Agilent oscilloscope used has the ability to calculate and display the standard deviation of the waveform. Figure 29 shows an example of battery noise displayed on the screen of an Agilent oscilloscope. The right side of the screen shows the numerical value for the standard deviation of the waveform. The light area on the left side of the screen shows that the noise has a Gaussian distribution.

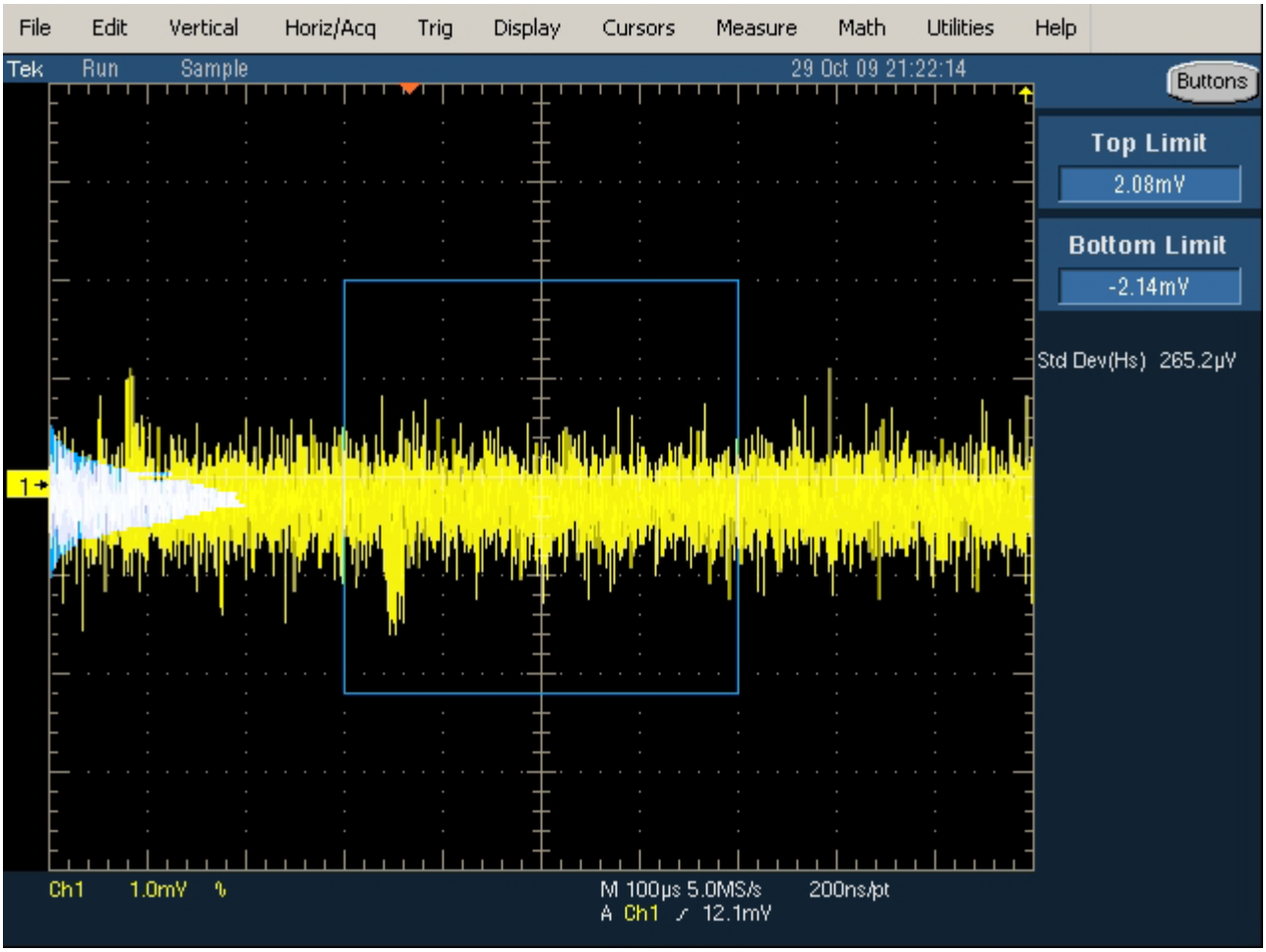
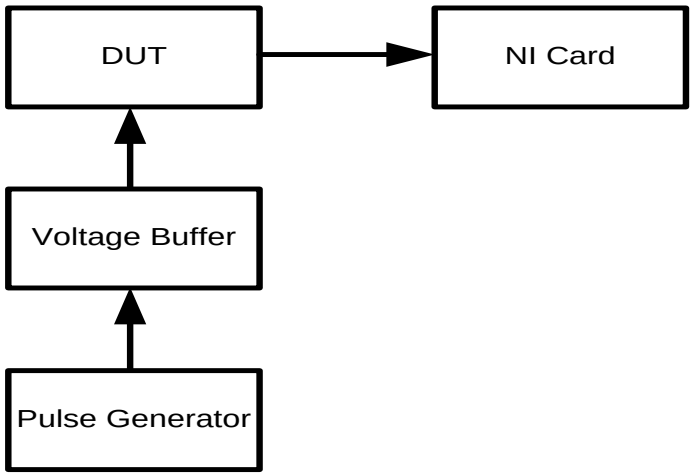
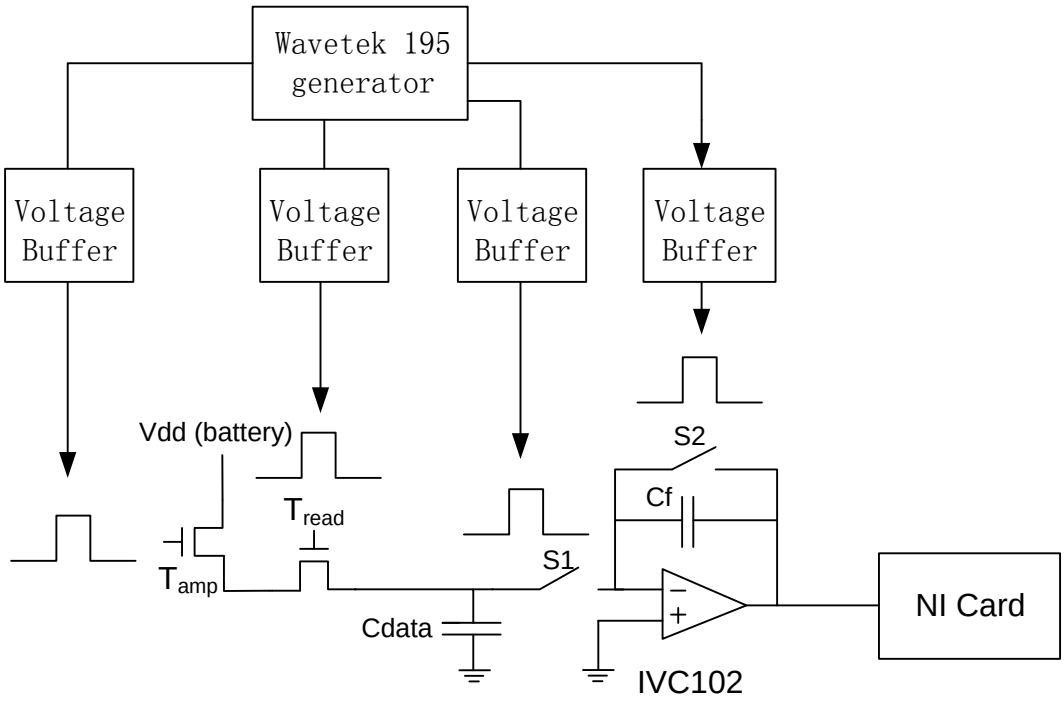


Figure 29: noise of a dc battery displayed on the Agilent oscilloscope

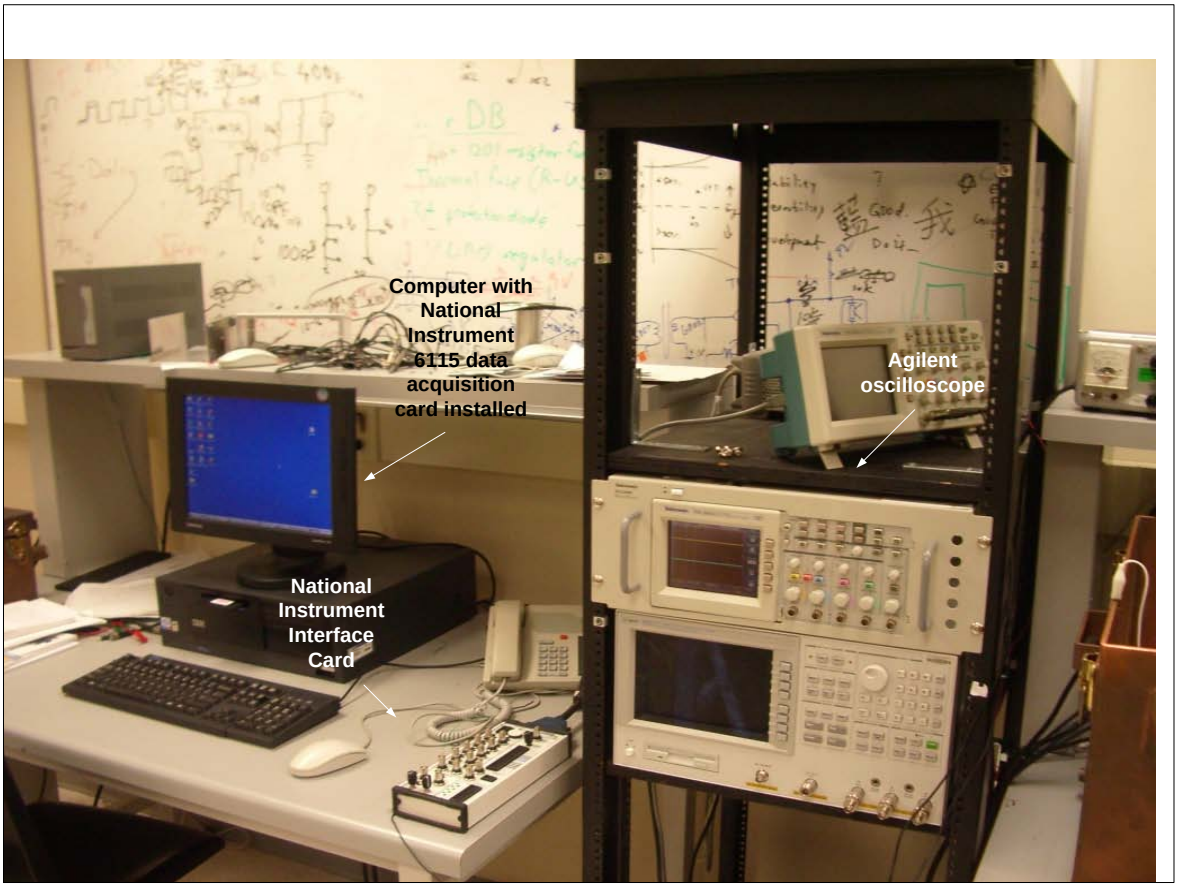
Unfortunately, the maximum resolution of the ADC in this oscilloscope is only 10 bits, which is not sufficient for the proposed study.


DUT
NI Card
Voltage Buffer
Pulse Generator

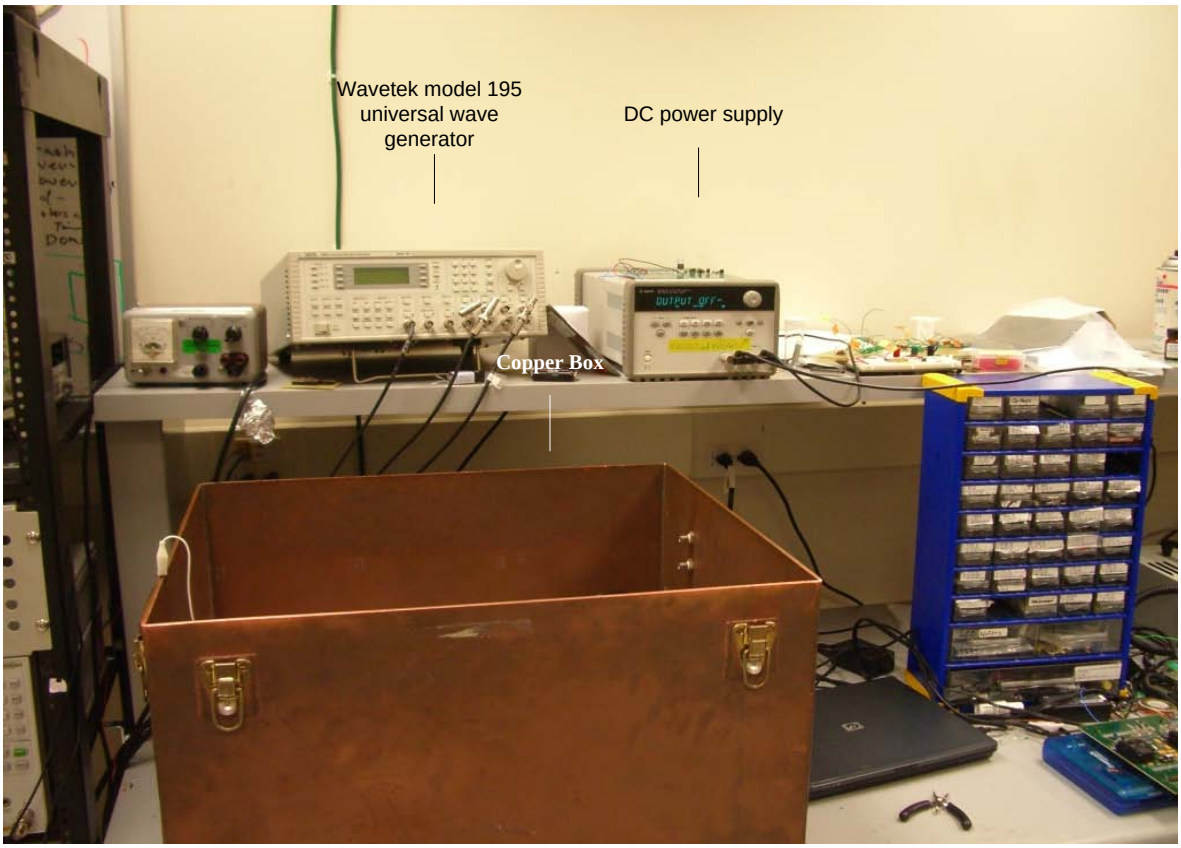
(a)


Wavetek 195 generator
Voltage Buffer
Voltage Buffer
Voltage Buffer
Voltage Buffer
Vdd (battery)
S2
Cf
T read
S1
T amp
Cdata
NI Card
IVC102

(b)


Computer with National Instrument 6115 data acquisition card installed
Agilent oscilloscope
National Instrument Interface Card

(c)



(d)

Figure 30: Experimental set-up used to measure the output noise (a) block diagram. (b) detailed schematic. (c) test setup including NI card and oscilloscope (d) test setup including the Wavetek universal wave generator

The noise measurements are performed using the setup discussed in this section. The detailed experiment results are presented in the next two sections.

4.2.2 Measurement Results for C-APS

The timing diagram and the output wave form for the C-APS is showing in Figure 31 and Figure 32. The period of the signal is 100 μs and the magnitude of the output voltage decreases from around 1 V to less than 0.2 V as we decrease the integration time from 40 μs

to 10μs. T1 in Figure 31 is the readout time (refer to section 2) which is also the period where the current signal is integrated on the C_f of the charge amplifier. The gate drive voltage for both the amplifying TFT and read TFT is 9 V and the drain voltage is constantly at 9 V.

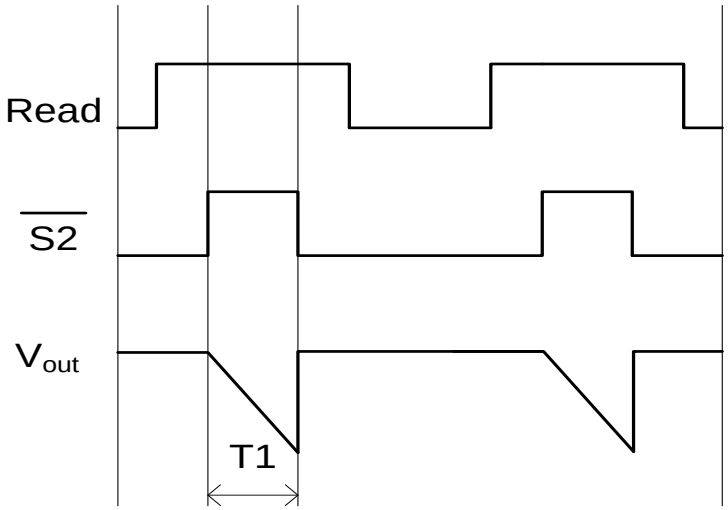
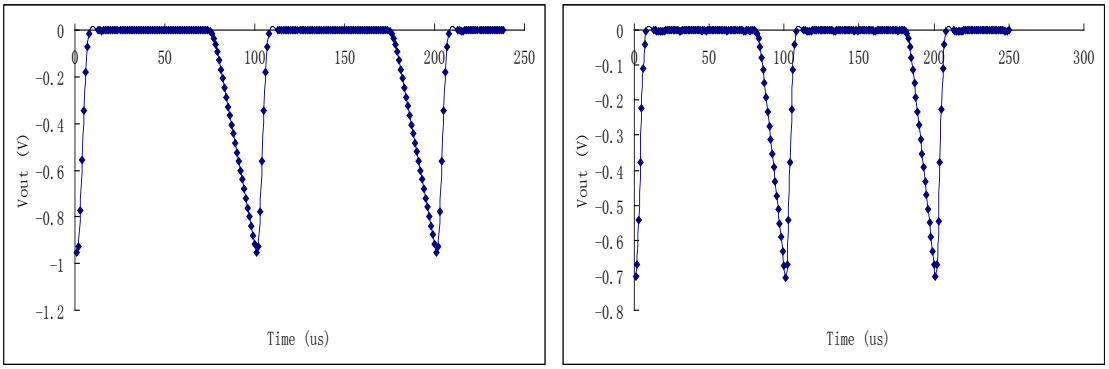
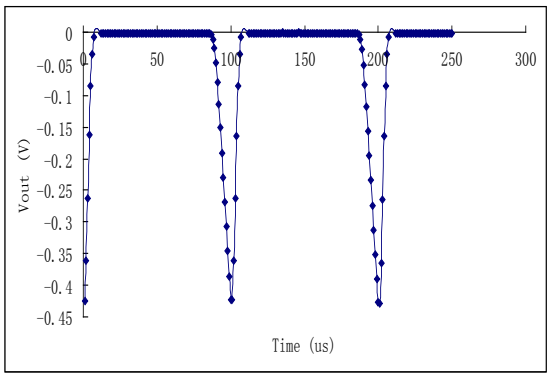
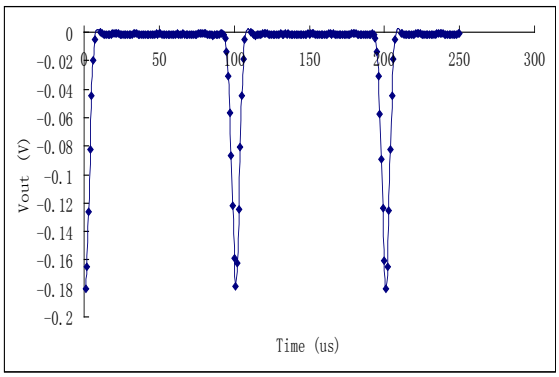


Figure 31: Timing diagram for C-APS



(a) (b)





(c) (d)

Figure 32: Output waveforms for the C-APS. (a) 40 μs readout time. (b) 30 μs readout time. (c) 20 μs readout time (d) 10 μs readout time

The output data is acquired with the NI card and the standard deviation (σ_{output}) of the output voltage is calculated using the following method,

$$\sigma_{output} = \sqrt{\text{var}(V_{out})} \tag{76}$$

Standard deviation and the input referred noise are calculated and presented in Table 4.

Table 4: Integration time vs. noise for C-APS (measured)

Integration Time (μs)	σ of the output voltage (V)	Input referred noise (e^-)
10	0.001248904	7.81×10^4
20	0.001203581	3.76×10^4
30	0.001199779	2.50×10^4
40	0.001299241	2.03×10^4

Due to the limitation of the NI card (which has a 12-bit ADC), to get the desire accuracy, the output voltage level has to be sufficiently small. For example, the resolution of a 12 bit ADC

is 0.244 mV if the full scale output voltage is 1 V. Thus the range of the integration time is chosen to be from 10 μs to 40 μs only. Table 4 shows that although output noise does not change with different integration periods, the input referred noise in term of electrons decreases as the integration time increases. This is as expected because the gain of the circuit is directly proportional to the readout time as discussed in section 3. The input referred noise in term of electrons shown in Table 4 seems very high. But keep in mind that the gain of the circuit under test is not optimized due to the limitation of the ADC in the NI card and the large default feedback capacitor available on the charge amplifier. Another contributing factor for the low gain of the system is the low *gm* of the TFT fabricated which is around 0.15 μA/V. However, by simply increasing the gain of the circuit does not necessarily guarantee the lower input noise. For example, if we blindly increase the gain by increasing the gate drive voltage of the amplifying TFT, both the thermal and flicker noises associated with the TFT would increase at the same time as the gain of the circuit and thus the effect on the total input referred noise cannot be easily determined. Table 5 shows the input referred noise with respect to different gate drive voltage, using an integration time of 40 μs.

Table 5: Gate drive voltage vs. noise for C-APS (measured)

Gate Voltage (V)	σ of the output voltage (V)	Input referred noise (e^-)
9	0.001299241	2.03×10^4
6.5	0.000791202	1.24×10^4
3.5	0.000525523	1.54×10^4

Although the output noise decreases as the gate drive voltage is reduced from 9 V to 3.5 V, the input referred noise does not follow the same trend as the output noise due to the changes in *gm* of the T_{amp}.

A better option to reduce the input referred noise would be increasing the integration time. Table 6 shows the estimated input referred noise with increased integration time. Since measurement results show that output noise is independent of the integration time, the σ of the output voltage is assumed to be around 0.0013 which represents the worst case scenario.

Table 6: Integration time vs. output noise for C-APS (estimated)

Integration Time (μs)	Input referred noise (e^-)
100	8.13×10^3
110	7.39×10^3
120	6.77×10^3
130	6.25×10^3

4.2.3 Measurement Results for V-APS

The timing diagram and the output wave form for the V-APS is showing in Figure 33 and Figure 34.

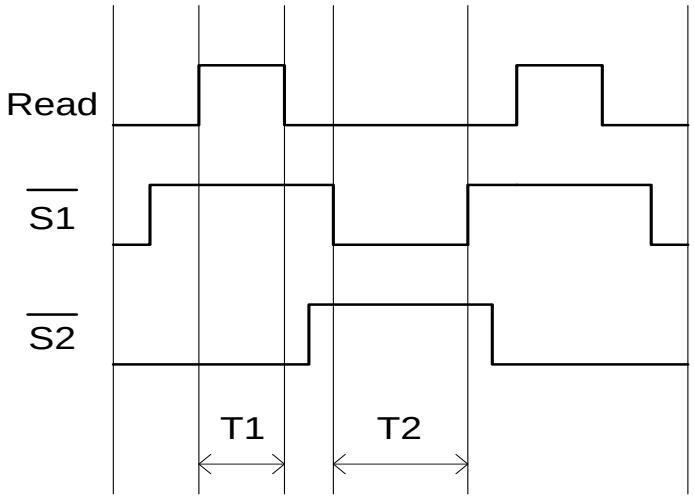
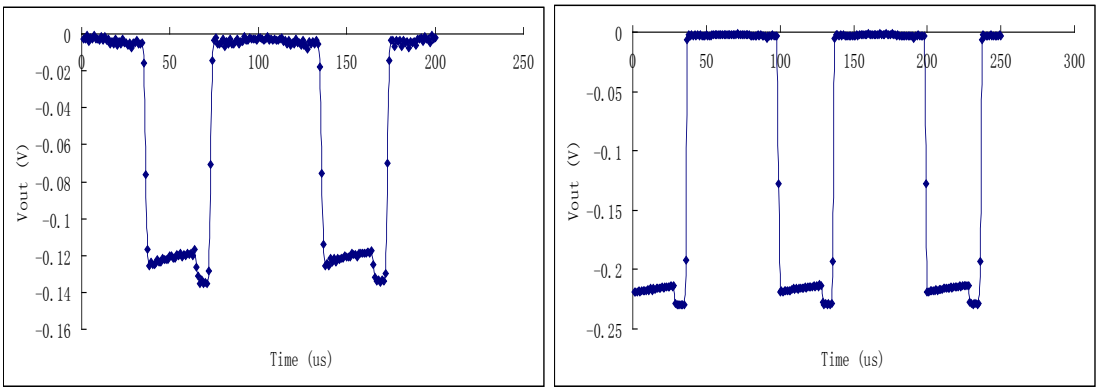
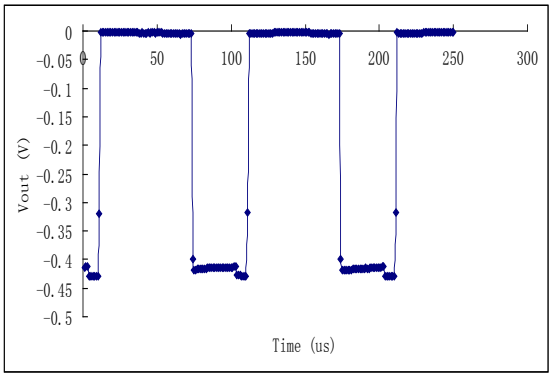


Figure 33: Timing diagram for the V-APS



(a) (b)



(c)

Figure 34: Output waveforms for the V-APS. (a) 100 μs readout time. (b) 200 μs readout time. (c) 400 μs readout time.

For the V-APS, the limitation of the operation in the experiment comes from the IVC102 charge amplifier. The charge amplifier has an internal protection diode with a built-in voltage of around 200mV connecting the input of the S1 (refer to Figure 12b) to the ground. Thus C_{data} can never be charged up to more than 200 mV. In order to be able to fully charge the C_{data} to the $V_g - V_T$ of the 2T structure (refer to the doted area in Figure 12a), the gate drive voltage for the amplifying TFT is reduced to 2.8 V. We then vary the readout time (first phase, refer to section 2 for the definition) of the in order to control the voltage level on the C_{data}. In Table 7, it is shown that the output noise is a function of the readout time.

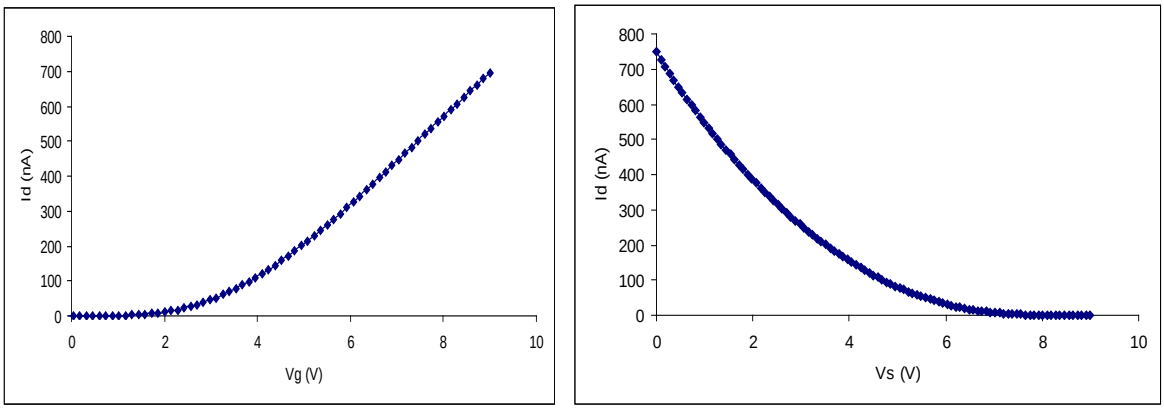
Table 7: Readout time vs. noise for V-APS

Readout Time (μs)	σ of the output voltage (V)	Input referred noise (e^-)
100	0.001537761	3.97×10^2
200	0.000769467	1.99×10^2
400	0.00073137	1.89×10^2

Comparing Table 7 with Table 4, 5, and 6, it is easily seen that the V-APS has significant advantage in term of noise performance while the tradeoff is the readout time. The input referred noise for V-APS is 2.5 to 6.8 times smaller comparing to the C-APS. However, in order to minimize the noise, we have to wait sufficient long enough for the C_{data} to charge up.

The experiment results also match with previously reported study done by L.E. Antonuk [1]. It shows as we increase the readout time, the output noise decreases due to the reduction in the direct current, which is proportional to the flicker noise, flowing through the TFTs. However we also noticed even after the C_{data} is charged up to $V_g - V_T$ of the Tamp, there is

still significant amount of direct current going through the TFTs. To further investigate this problem, the 2T structure is tested using the semiconductor parameter analyzer and the result is shown in Figure 35.



(a) (b)

Figure 35: (a) I_d vs. V_g (b) I_d vs. V_s

Figure 35(a) shows the I_d vs. V_g curve with 9V at the drain of T_{amp} and 9V at the gate of T_{read}. V_T of the structure can be extrapolated to be around 2.5 V. In, Figure 35(b), the gate of T_{amp}, the drain of T_{amp}, and the gate of T_{read} is kept at the 9 V and the source of T_{read} is swept from 0 V to 9 V. It is shown that even when the voltage at the source of T_{read} reaches 7.5V, which is around $V_g - V_T$ of the 2T structure, there is still around 2 nA of current flowing through the transistors. This phenomenon can be explained by comparing the I_d vs V_g curve of the a-Si TFT to that of the crystalline silicon transistor shown in Figure 36. It is shown that for crystalline silicon transistor, the ON-OFF ratio of the current is much higher and V_T can be defined. On the other hand, for a-Si TFT, aside from the high OFF or leakage current, it is also very hard to define the V_T, due to the fact that the corner on the IV curve for a-Si TFT is

not as sharp as the one for crystalline transistor. Thus, for the V-APS, even if the TFTs are OFF, the current will continue to flow and charge up the C_{data} all the way up to V_{dd} (drain voltage of the T_{amp}) if we wait long enough. Thus, for practical purposes, we would not be able to completely eliminate the flicker noise from the circuit and the amount of the flicker noise depends entirely on the leakage level of the TFTs. It is also worth to mention since the leakage current in the poly-silicon (poly-Si) TFT is much higher compare to amorphous TFT [28], the flicker noise in V-APS made from poly-Si is expected to be higher as well.

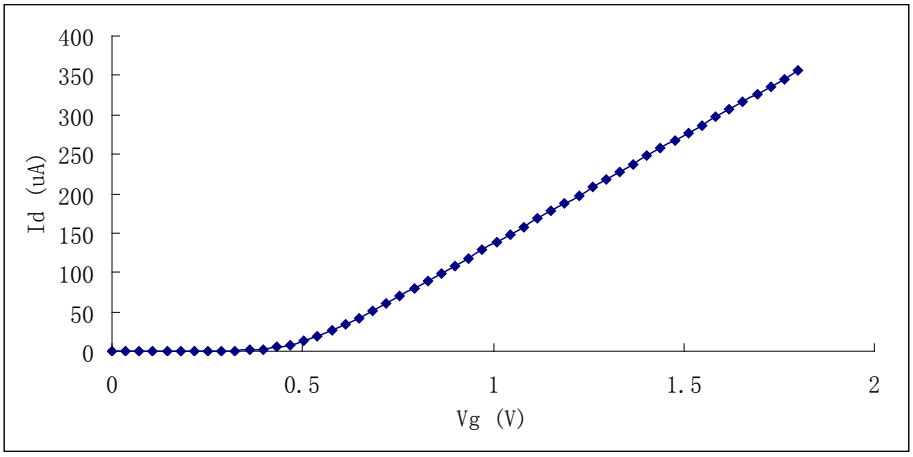


Figure 36: Typical I_d vs. V_g curve for crystalline silicon transistor

Chapter 5
Conclusion

5.1 Summary

Both detailed analytical noise analysis and experimental noise measurements are presented in this thesis. TFT leakage noise, circuit thermal noise, circuit flicker noise, data line noise and the charge amplifier noise are considered. Both theoretical and experimental results obtained in this study verified that V-APS is superior compared to the C-APS circuit in term of the noise performance due to the lower flicker noise in the V-APS circuit. Experiment results show that the input referred noise of V-APS is significantly smaller comparing to C-APS. It is also concluded that the noise level in V-APS is independent of the bias voltage of the circuitry.

Although reduced in V-APS, the flicker noise is still presented and could not be easily eliminated due to the high leakage current presented in a-Si TFTs and even worse, in poly-Si TFTs. The tradeoff for low noise in V-APS is the long readout time, which makes it unpractical for real time imaging system.

5.2 Projected Results

In this section, the best case noise performance and signal to noise ration (SNR) are compared for both C-APS and V-APS made with a-Si and poly-Si technology. The parameters used for the calculation are listed in table 8.

Table 8: Parameters for best case noise calculation

TFT Parameters	a-Si	poly-Si
T_{amp} width (μm)	400	400
T_{amp} length (μm)	20	20
T_{read} width (μm)	200	200
T_{read} length (μm)	20	20
T_{reset} width (μm)	200	200
T_{reset} length (μm)	20	20
Effective channel mobility (cm^2/Vs)	0.5	150
Threshold voltage (V)	2.5	1
Effective pixel capacitor (pF)	1	1

The data line capacitance (C_{data}) and feedback capacitance (C_f) are assumed to be 60 pf and 1 pf, respectively. For more comprehensive results, the reset TFT leakage current shot noise and reset noise (*kTC*) noise are included in this section. The leakage current noise associated with the reset TFT is given by

$$\sigma_{TFT} = \sqrt{\frac{I_{TFT}T}{q}} \tag{77}$$

where ITFT is the TFT leakage current, T is the frame time which equals to 33 ms, and q is the electron charge. For the calculation, we assumed a leakage current of 0.03 fA per micron of gate width for the a-Si, and a leakage current of 1.5 fA per micron of gate width for the poly-Si [25]. Reset noise can be calculated by

$$\sigma_{reset} = \sqrt{\frac{kT}{C_{eff}}} \tag{78}$$

where C_{eff} is the effective detector node capacitance.

Performing the same analysis, which has been done in section 3 with the new parameters, the new results are shown in the table 9.

Table 9: Leakage current noise and reset noise

	a-Si	poly-Si
Reset TFT leakage current noise (electrons)	18	125
Reset (kTC) noise (electrons)	284	284

The total noise for both a-Si and poly-Si are calculated and shown in table 10.

Table 10: Total input referred noise

Input referred noise (electrons)	a-Si	poly-Si
C-APS	527	348
V-APS	286	312

For the real time fluoroscopy application where the inputs signal level is about 1000 electrons. The SNR is calculated and listed in table 11.

Table 11: Total input referred noise

SNR (absolute)	a-Si	poly-Si
C-APS	1.9	2.9
V-APS	3.5	3.2

Other than better noise performance comparing to a-Si, poly-Si also has speed advantage due to its higher electron mobility (100 times of the electron mobility in a-Si). Poly-Si also has high hole mobility so complementary designs can also be achieved with poly-Si. (where it is impossible with a-Si).

5.3 Potential Future Research

Some future work can be done to improve the measurement results obtained in this study in terms of accuracy and completeness. First of all, to get more accurate results for both C-APS and V-APS, better model of NI card with more sophisticated ADC (16bit or higher) should be used. This allows us to have higher output voltage level with the same degree of accuracy when taking noise measurement. Next, to make gain of the circuits higher, discrete feedback capacitor should be used instead of the default ones attached to the IVC102 charge amplifier used in this work. The discrete feedback capacitor should have smaller value compare to the default ones in order to have a lower input referred noise figure. For the V-APS noise measurement, it is necessary to find or design a charge amplifier that does not have such a low input voltage limitation as in the case of IVC102. For more ambitious measurement in the future, double sampling mechanism can be included. This would further reduce the flicker noise figures measured in this study.

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