

# Design of High Efficiency Broadband Adjusted Class AB Power Amplifier

by

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## **AUTHOR'S DECLARATION**

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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## Abstract

This thesis starts with a discussion of different classes of operation of power amplifiers (PAs). Comparing advantages and disadvantages of these classes, class AB is chosen as the best initial candidate for the design of broadband PA.

Different methods for design of matching networks are first discussed. Some of them fall into the group of narrowband matching networks, while others are suitable for a broadband context. Broadband design methodologies are categorized into two groups of real-to-real transformations and complex-to-real transformations. Complex-to-real transformations are the most useful methods for this project, since design of power amplifiers deals with complex loads rather than just real loads.

The design of broadband matching networks exploiting filter theory is presented in this thesis for synthesizing broadband and highly efficient power amplifiers (PAs). Starting with sets of optimum impedances over the targeted frequency band, the matching networks are designed using a systematic approach.

The effects of load termination at the 2<sup>nd</sup> and 3<sup>rd</sup> harmonic on the PA performance (efficiency) are studied. The significance of proper termination, especially at the 2<sup>nd</sup> harmonic, is highlighted. To prevent further complication of the design process, though, specific harmonic termination (stubs) is avoided and special arrangement of the matching network (position of the bias network) is preferred, as it is found to lead to acceptable efficiency.

Two PA prototypes were designed with the proposed methodology using 25W GaN devices. The designs targeted two frequency bands: 1.8 to 2.2 GHz (20% BW) and 1.8 to 2.7 GHz (40% BW). For the former, drain efficiency (DE) of 70% (+/-5%) and output power of 45.5 dBm (+/- 1.0dB) was measured while the latter achieved very promising efficiency of about 60% over the entire bandwidth.

## **Acknowledgements**

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# Chapter 1

## Introduction

Today, wireless communication is an integral part of everyday life. It has been evolving day by day, trying to meet diverse needs and requirements. In this regard, several wireless standards are either deployed right now (such as Global System for Mobile communications (GSM)), or will be introduced in the near future (such as Worldwide Interoperability for Microwave Access (WiMAX) and Long Term Evolution (LTE)). In this context, service providers have to cope with multiple protocols and multiple standards, as they keep the interoperability of both old and new generations simultaneously.

In order to deal with multiple standards, several solutions can be considered, such as multiple, reconfigurable, multi-band, and/or broadband radios. Using multiple radios for coverage introduces additional size and cost of materials, and is not an optimized solution in terms of size and cost. The alternative solution is to deploy reconfigurable radios using PIN diodes, varactors or microelectromechanical systems (MEMS based devices). Although this solution is conceivable and much research in this area is in progress, it is not an optimum solution either. First of all, using electronically tunable devices will introduce extra sources of nonlinearity and loss. Second, it will cause limitations in terms of power handling. In addition to nonlinearity and power handling limitations, elements such as MEMS switches may need high actuation voltage, while having slow switching times (of the order of 10ms). Furthermore, reliability of these systems is quite low [1], [2].

On the other hand, multi-band and broadband structures make one radio operate for more than one standard. In other words, multi-band systems work for multiple narrowband frequency intervals (usually far from each other), while broadband structures aim for a single but wider frequency range trying to target two or more wireless standards. The main challenge of the design of multi-band/broadband structures is to keep the good performance as close as possible to the performance of a single radio operating for a single frequency.

Power amplifiers are one of the important building blocks of wireless systems which are frequency-dependent. It means their performance deviates as the frequency diverges from the target frequency. Therefore, multiband/broadband methodologies should be presented and implemented for multi-band/broadband designs. These methods should be based on maintaining performance in terms of efficiency and linearity, while covering the multiple/broad frequency bands.

Wideband power amplifiers have been designed with different specifications. Some of them are aimed for much higher bandwidths (Ultra-Wideband), while others target bandwidths of about 5 to 30% [2].

For example, a single stage GaN power amplifier has been designed for 0.5 to 2.5 GHz, which has saturated output power of +41 dBm [3]. This power amplifier achieves a minimum drain efficiency of 35% at nominal drain voltage and has minimum drain efficiency of 46% when subjected to drain voltage optimization over frequency.

In another case, a nonlinear CAD approach has been deployed, and targeting frequencies of 0.8 to 4 GHz, an average drain efficiency of about 50%, with an output power higher than 32 dBm in the overall bandwidth, has been achieved [4].

In another approach, a dual-fed distributed design has been used to target 2.6 GHz WiMAX application [5]. Furthermore, controlling gate bias voltage over the 150 MHz bandwidth has been used for optimization purposes. The results show average PAE of about 16% over bandwidth, while the average output power is about 33 dBm.

There are three steps in design of power amplifiers: design of the input matching network, design of the output matching network, and design of the bias network.

Design of the input and output matching networks are important steps of the overall design. Impedance matching provides the maximum RF power available from source to be delivered to the load. It results in sensitivity improvement of the receivers, as well as achieving optimum gain, power efficiency, output power, and dynamic range. It is therefore an integral part of the design [6].

There are several factors that should be considered while choosing topologies for matching networks. For example, desired bandwidth and frequency response determine the required frequency response of the matching networks. Complexity and size of the matching networks are other factors to be limited by circuit requirements. In addition, properties such as insertion loss of the matching networks should be taken into account.

Considering the factor of bandwidth, matching networks can be categorized into three groups as: narrowband matching networks, broadband real-to-real transformations, and broadband complex-to-real transformations. Narrowband matching networks present a limited bandwidth, while broadband transformations work for broader bandwidths. Real-to-real transformations are used for transforming a real impedance into another real impedance, while on the other hand complex-to-real transformations are deployed for transforming a complex load into a real impedance.

Following this chapter, chapter 2 is a brief overview on power amplifiers and different classes of operations. Chapter 3 discusses different broadband methodologies including the main methodology used for this thesis. Chapter 4 describes the design procedure of broadband power amplifier using Advanced Design System software (ADS). Finally, chapter 5 presents the measurement results of the fabricated designs, and will be followed by the conclusion and suggestions for future work.

## Chapter 2

### Overview of power amplifiers

Every wireless communication system requires transmitters, as shown in Fig. 2.1, and as an important component of transmitters, design of power amplifiers for wireless systems is an integral step of the design. Power amplifiers draw the power from a power supply and use it for amplifying the input signal. In other words, the output signal of a power amplifier will be an enlarged version of the input signal.

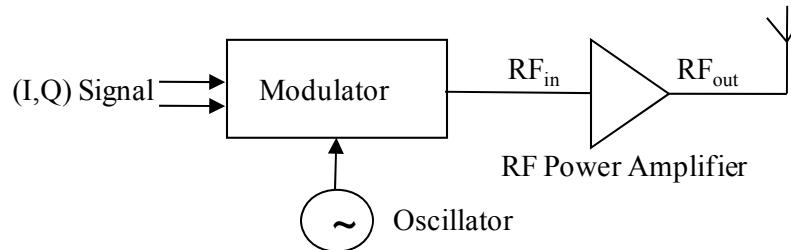


Fig. 2.1. Transmitter block diagram

Two main requirements in design of power amplifiers are linearity and efficiency:

Linear systems exhibit the linear behaviour of  $\text{output} = \text{constant} \times \text{input}$ , thus linear increase at the input results in linear increase at the output of the system. In nonlinear systems, on the other hand, output and input signals have a nonlinear relationship with each other. In other words, the output of a nonlinear system will not only have the fundamental content of the input, but will also contain harmonic contents. There are several figures of merit to determine the linearity of a system, such as 1-dB compression power ( $P_{1\text{dB}}$ ), intercept point power (IP), inter-modulation distortion (IMD), and AM-AM and AM-PM characterization.  $P_{1\text{dB}}$  represents the level of output power at which the transfer characteristic of the system deviates from the ideal linear response by 1 dB. IP refers to the point at which power of a certain harmonic reaches the level of the ideal fundamental power; for example, IIP3 (input intercept point) considers input power for the third harmonic and OIP3 (output intercept point) is for the third harmonic at the output. These factors are shown in Fig. 2.2. IMD shows the difference of power level between fundamental frequency and inter-modulated frequencies. An example of IMD3 is illustrated in Fig. 2.3. In systems with modulated signals, other factors, like adjacent channel power ratio (ACPR) and error vector magnitude (EVM), are considered. ACPR represents the ratio between out-of-band power spectral density to in-band spectral density at specified offset channels. EVM represents the vector difference between ideal and measured signal ( $S_{\text{ideal},r}$  and  $S_{\text{meas},r}$ ) as defined in (2.1),

$$EVM = \left[ \frac{\frac{1}{N} \sum_{r=1}^N |S_{ideal,r} - S_{meas,r}|^2}{\frac{1}{N} \sum_{r=1}^N |S_{ideal,r}|^2} \right]^{1/2}. \quad (2.1)$$

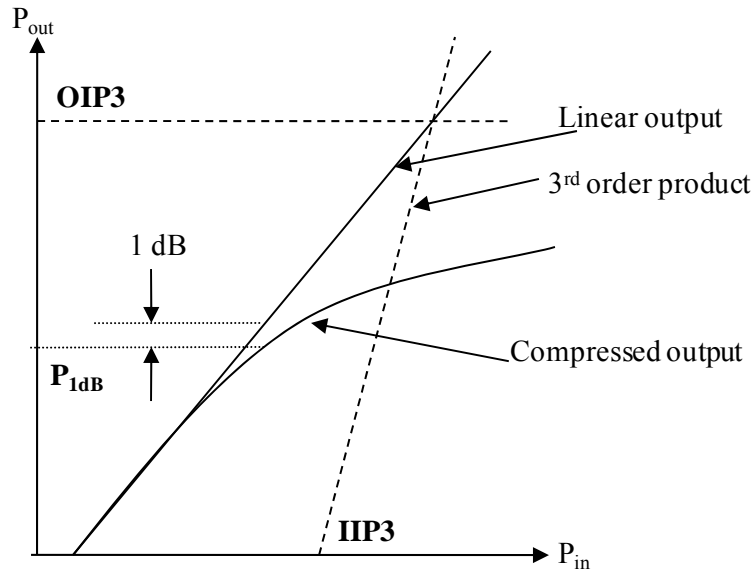


Fig. 2.2. Illustration of  $P_{1dB}$ ,  $IIP3$ , and  $OIP3$

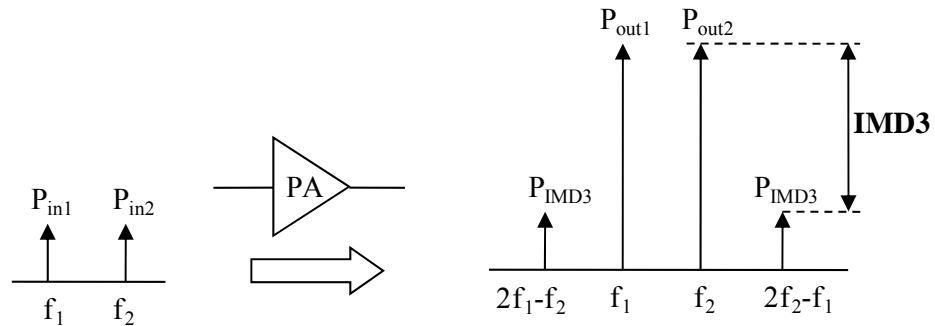


Fig. 2.3. Illustration of  $IMD3$

In order to determine the efficiency of the power amplifiers and find out the power loss, there are some factors, such as drain efficiency (DE) and power added efficiency (PAE), which characterize the performance of a power amplifier. DE is defined in (2.2), and PAE is defined in (2.3),

$$DE = \frac{P_{out}}{P_{DC}}, \quad (2.2)$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}}. \quad (2.3)$$

There are several other properties that we expect to get from power amplifiers. For example, gain of a power amplifier is the ratio of the output signal to input signal, and required gain differs for different applications. Bandwidth of a power amplifier is another property which should be set according to the system requirements. The required bandwidth sets the range of frequencies in which the power amplifier should work efficiently and properly. Another property is the output power of the amplifier, for which we should design the matching networks properly to ensure that most of the input power is delivered to the output.

One of the challenges of design of power amplifiers is the compromise between linearity and efficiency. In other words, there is a tradeoff between efficiency and linearity in power amplifiers: more linear operation leads to less efficient performance. This is shown in Fig. 2.4. In some classes of operation, such as class E, the efficiency is high but the output is very nonlinear (there are a lot of harmonics present in the output). On the other hand, classes such as class A provide high linearity, but poor efficiency (more details on classes of operations are provided in the next sections). Therefore, the class of operation must be chosen according to the efficiency and linearity requirements of the system, given this tradeoff between linearity and efficiency. Furthermore, some efficiency enhancement methods and linearization techniques should be deployed.

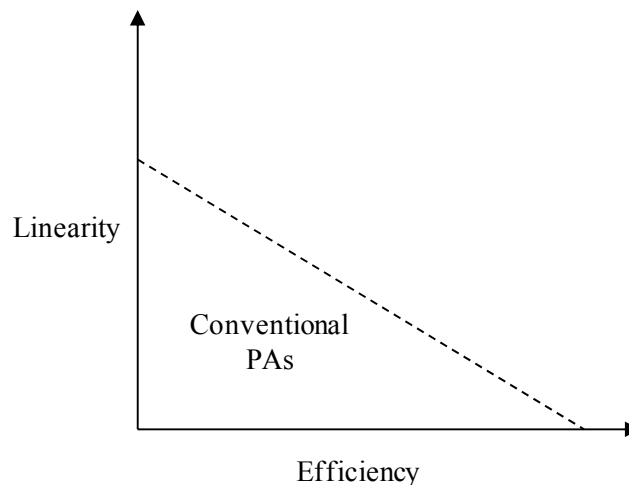


Fig. 2.4. Linearity-efficiency tradeoff for power amplifiers

Power amplifiers can be categorized into two main groups of PAs “working as a current source” and “switching mode” power amplifiers. For the first group, the transistor works as a voltage-controlled current source and the point that the amplifier is biased determines the class of operation. For the switching mode power amplifiers, the transistor acts as a switch, and the passive elements at the output matching network shape the drain voltage and current, and set the class of operation.

In this chapter, an overview of different classes of operation of power amplifiers will be given. Furthermore, load-pull concepts and harmonic terminations will be discussed.

## 2.1 Power amplifiers working as a current source

In PAs working as a current source, different bias points result in different conduction angles, and therefore different classes of operation. For the voltage and current we have,

$$v_{in} = V_b + V_{in} \cos \omega t, \quad (2.4)$$

$$i = I_q + I \cos \omega t \quad \text{for } -\theta < \omega t < \theta; \text{ otherwise } i=0, \quad (2.5)$$

in which  $V_b$  is the bias voltage,  $I_q$  is the quiescent current,  $\theta$  is the half of the conduction angle, and  $V_{in}$  and  $I$  are amplitude of the input voltage and the output current respectively.

Since  $\theta$  is the half of the conduction angle, it can be determined at the moment when current is equal to zero, as shown in (2.6),

$$I_q + I \cos \theta = 0 \Rightarrow \cos \theta = -\frac{I_q}{I} \Rightarrow i = I(\cos \omega t - \cos \theta). \quad (2.6)$$

In order to determine the efficiency for each class of operation, first the DC component of the current and the fundamental component of it should be calculated using (2.7) and (2.8),

$$I_0 = \frac{1}{2\pi} \int_{-\theta}^{\theta} I(\cos \omega t - \cos \theta) d\omega t = \frac{I}{\pi} (\sin \theta - \theta \cos \theta), \quad (2.7)$$

$$I_1 = \frac{1}{2\pi} \int_{-\theta}^{\theta} I(\cos \omega t - \cos \theta) \cos \omega t d\omega t = \frac{I}{\pi} (\theta - \sin \theta \cos \theta). \quad (2.8)$$

Knowing that efficiency is the ratio of power at the fundamental to the power at DC, and assuming an ideal condition of zero saturation voltage (voltage peak factor ( $V_{in}/V_{cc}$ ) is equal to 1, in which  $V_{cc}$  is the DC supply voltage), we have,



$$\eta = \frac{P_1}{P_0} = \frac{1}{2} \cdot \frac{I_1}{I_0} = \frac{1}{2} \cdot \frac{(\theta - \sin \theta \cos \theta)}{(\sin \theta - \theta \cos \theta)} \quad (2.9)$$

Depending on the conduction angle, efficiency and linearity of each class is determined. More details on different classes of operation of this category will be provided in the following sections.

### 2.1.1 Class A power amplifiers

Nonlinear devices are assumed to have linear behavior between cut off and saturation point. If the bias point is picked to be the midpoint of the linear region with voltage not exceeding the boundary values of cut off and saturation point, a sinusoidal drive signal will result in a sinusoidal current without any harmonics. This is how a classical class A amplifier works [7].

The class A amplifier is cheap, because it only requires a single active device. It is biased in the active linear region and amplifies the signal over the entire input cycle. Fig. 2.5 shows how a class A amplifier operates. Its performance is good in terms of linearity (it contains no harmonics at the output), but undesirable in terms of efficiency. In other words, it is very inefficient because it is always conducting even when there is no input signal. According to (2.9) it can obtain a maximum efficiency of 50% ( $\theta=\pi$ ).

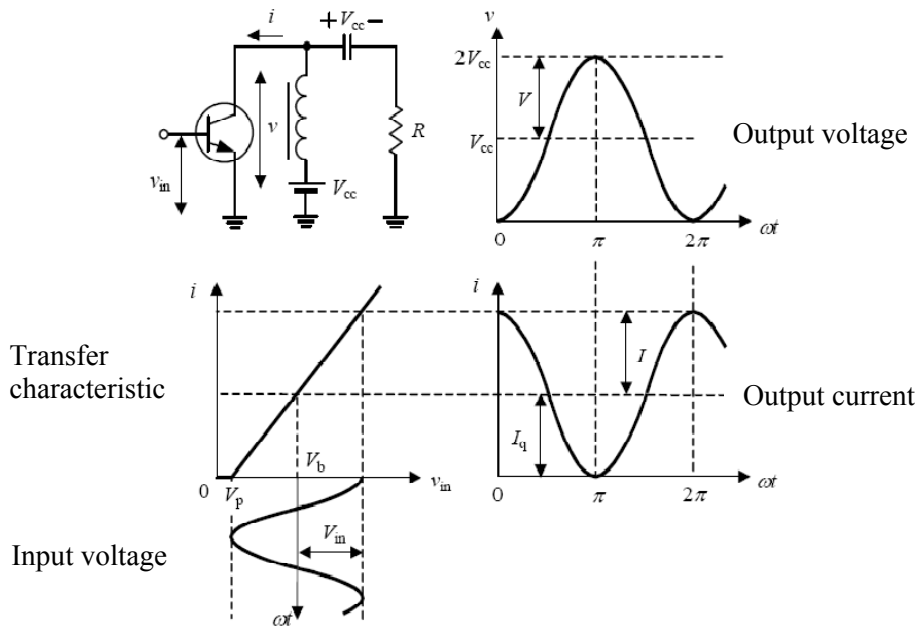


Fig. 2.5. Class A operation

### 2.1.2 Class B power amplifiers

Unlike class A, a class B amplifier amplifies only half of the cycle of the input signal. Its operation is shown in Fig. 2.6. Turning off the amplifier for half of the cycle reduces power dissipation, but on the other hand, increases the harmonic content of the output signal as it is not purely sinusoidal anymore. Therefore, class B is more efficient than class A but less linear. Using (2.9) with  $\theta=90^\circ$  (half the cycle) shows that a maximum efficiency of 78.5% is obtainable for a class B power amplifier.

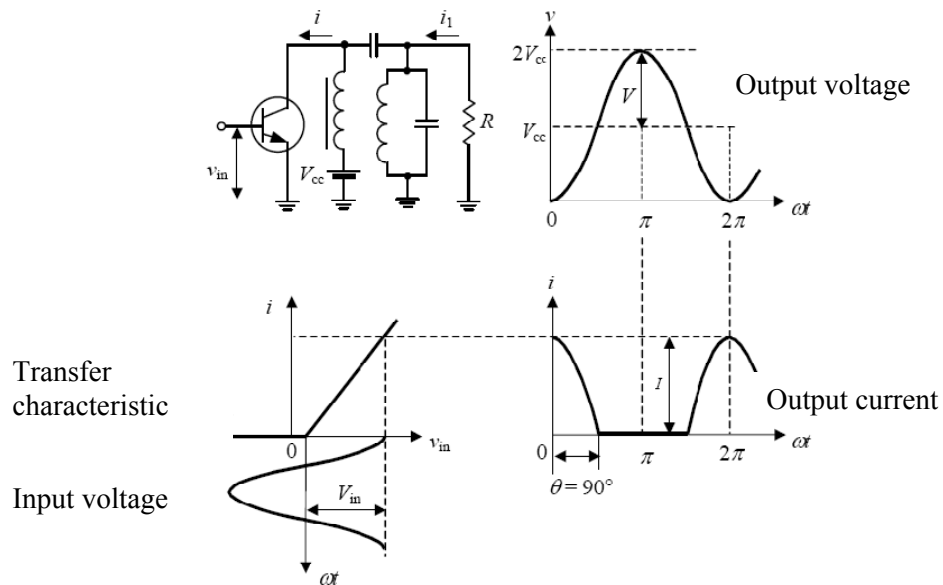


Fig. 2.6. Class B operation

### 2.1.3 Class C power amplifiers

A class C amplifier conducts even less than half of the cycle of the input signal ( $\theta$  is less than  $90^\circ$ ), which makes it more efficient than class B. But it should be noted that the advantage of high efficiency comes with the disadvantage of high distortion at the output.

### 2.1.4 Class AB power amplifiers

The class AB amplifier is a classical compromise, which has higher efficiency than class A, but inevitably increased nonlinearity [8]. In other words, the class AB amplifier is biased somewhere between class A and class B (which means less than full cycle but more than half a cycle conduction). Therefore, the

efficiency will be between 50% and 78.5% (depending on the bias point), and the linearity will be better than a class B, but worse than a class A amplifier.

### 2.1.5 Class F power amplifiers

Class F power amplifiers are analyzed in the frequency domain. In other words, canceling the overlap between current and voltage is done in the frequency domain using harmonic terminations. Ideal current and voltage waveforms of a class F power amplifier are shown in Fig. 2.7.

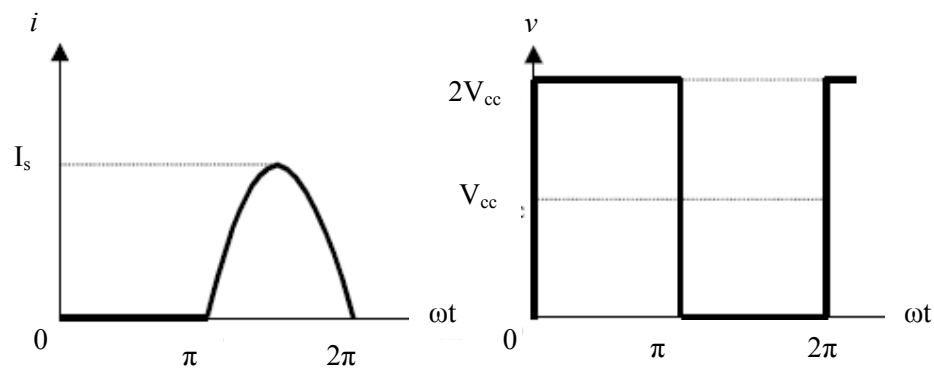


Fig. 2.7. Ideal current and voltage waveforms of class F power amplifier

As shown in Fig. 2.7, the current waveform is half-sinusoidal and the voltage has a square-wave shape. The current contains the even harmonics, while voltage consists of odd harmonics. It results in non-overlapping harmonics and reduction of the power loss due to harmonics. Theoretically, an ideal efficiency of 100% is predicted. One circuit example of class F design is shown in Fig. 2.8. In this example,  $\lambda/4$  transmission line is used in order to present an open circuit to the fundamental frequency and odd harmonics, and short circuit the even harmonics. Furthermore, an LC resonator is used to deliver the power of the fundamental frequency only.

This class of operation has narrow bandwidth, and due to harmonic termination requirements, is not suitable for broadband design. In other words, it is based on a design for a single frequency, and the harmonic termination of that frequency.

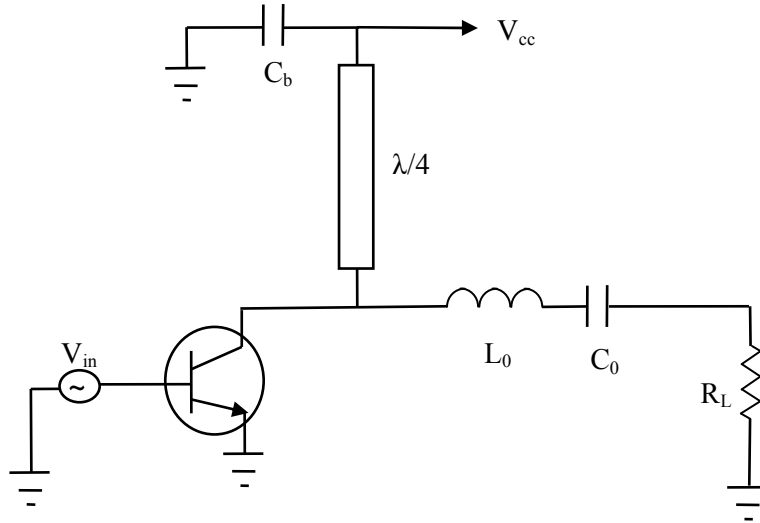


Fig. 2.8. Design example of class F power amplifier

In addition to the class F amplifier, there is the inverse class F amplifier ( $F^{-1}$  class), which uses the same concept for non-overlapping harmonics with interchanged waveforms. In other words, an inverse class F has a current of square-wave and a voltage of half-sinusoidal as shown in Fig. 2.9.

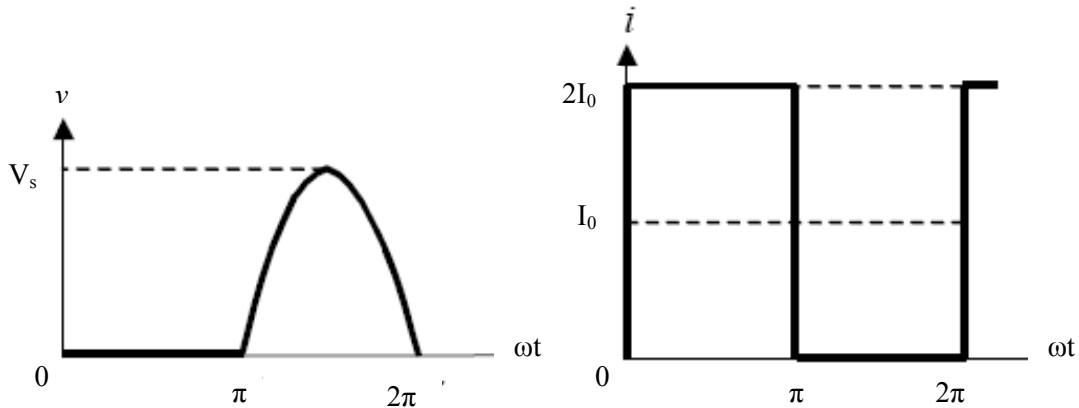


Fig. 2.9. Ideal current and voltage waveforms of inverse class F power amplifier

## 2.2 Switching mode power amplifiers

In this category, power amplifiers are designed so that the transistor acts as an RF switch, rather than as a voltage-controlled current source. In other words, the output networks provide non-overlapping waveforms. Furthermore, efficiency of this category is improved, because of operation in the saturation region at the cost of more complex load networks (which means at lower powers, switching mode power

amplifiers will have poor efficiency). On the other hand, linearity is sacrificed due to operation in a strongly nonlinear region, which results in nonlinear voltage and current waveforms.

A transistor can be modeled as a switch as shown in Fig. 2.10.  $L$  represents package bond wire parasitics,  $R_{on}$  is modeling electron mobility, and  $C$  is for device output capacitance. For ideal operation, the switch should be either off (open circuit, with zero current) or on (short circuit, with zero voltage), and it should go from one state to another instantaneously [7]. But in practical conditions, there is usually leakage current or voltage drop across the switch, so switching is done with a certain time constant. Therefore, although ideal operation of switching mode power amplifiers predicts an efficiency of 100% theoretically, there is always power loss due to non-idealities resulting in efficiencies lower than 100%.

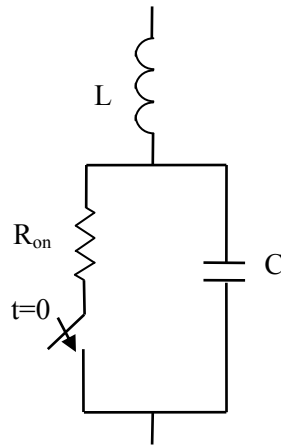


Fig. 2.10. Modeling of the transistor as a switch

More details on different classes of operation of this category is provided in the following sections.

### 2.2.1 Class E power amplifiers

Unlike class F and inverse class F, class E power amplifiers are analyzed in the time domain. Because of the switching behavior of the transistor in this class, the ideal shape of voltage and current waveforms of class E don't overlap in the time domain, which results in no loss and 100% efficiency. But there are always non-idealities, such as non-zero saturation resistance of the transistor or finite switching time, which cause power loss. Practical waveforms of a class E amplifier are shown in Fig. 2.11.

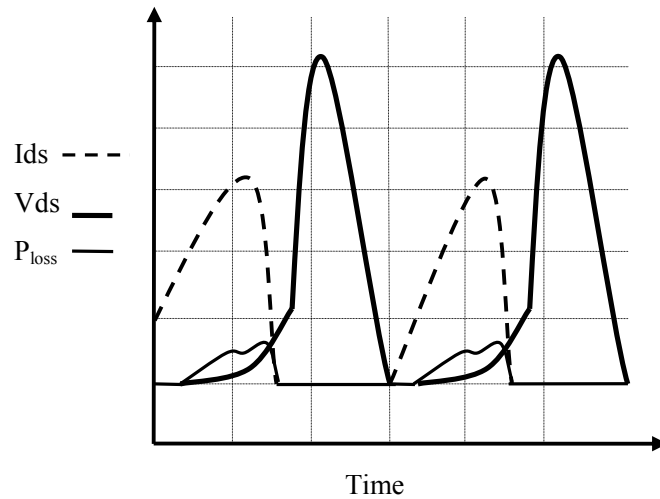


Fig. 2.11. Practical wave forms of class E power amplifier

Class E amplifier design falls into different groups, such as design with shunt capacitance, design with a parallel circuit, or with a transmission line. In each case, design parameters are determined such that zero-current and zero-voltage conditions are satisfied. An example of a class E with shunt capacitance is shown in Fig. 2.12.

Just like class F, the design procedure of this class of operation is based on considering a single fundamental frequency, which makes it narrowband and unsuitable for broadband power amplifiers.

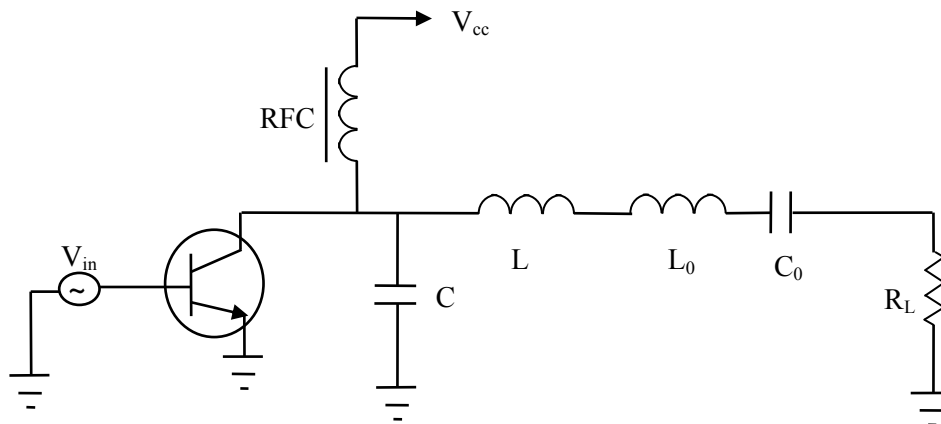


Fig. 2.12. Design example of class E with shunt capacitance

## 2.2.2 Class D power amplifiers

Class D power amplifiers are designed with push-pull configuration of two class F (or inverse class F) amplifiers. They are categorized into two groups: voltage-mode class D and current-mode class D.

In voltage-mode class D, voltage is switched between two transistors resulting in the same waveforms as class F. It is shown in Fig. 2.13. Output capacitance of the transistor ( $C_{ds}$ ) is charged and discharged at each transition resulting in energy loss. Furthermore, there are difficult driver requirements, particularly for the ungrounded transistor.

Current-mode class D has a fully differential structure, in which current is switched instead of voltage, which results in similar behavior to the inverse class F amplifier. It is depicted in Fig. 2.14. This structure eliminates the energy loss of  $C_{ds}$ , but it requires input and output baluns and combiners, which induce extra loss and take up more space.

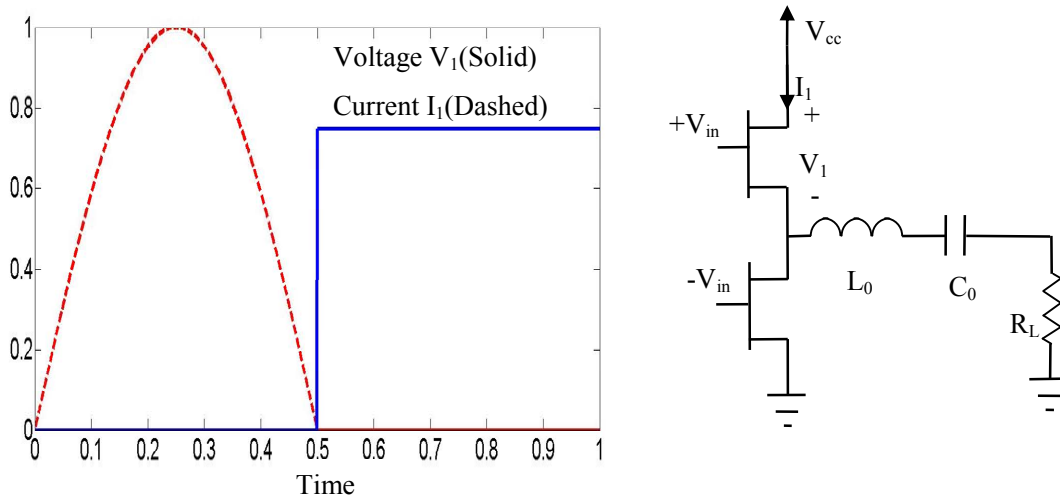


Fig. 2.13. Voltage-mode class D configuration and waveforms

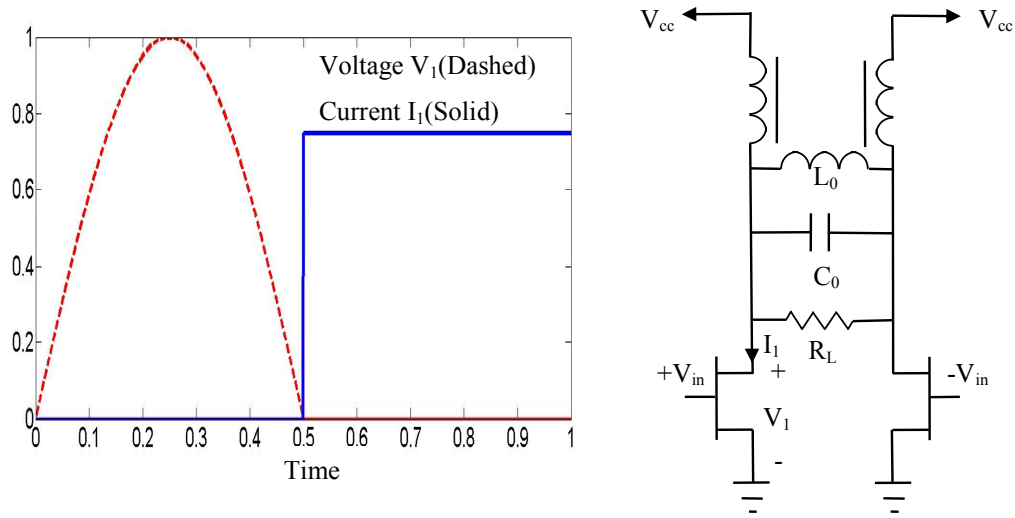


Fig. 2.14. Current-mode class D configuration and waveforms

### 2.3 Load/source pull concepts

As mentioned in chapter 1, design of power amplifiers consists of three main steps, these being design of the input matching network, of the output matching network, and of the bias network as shown in Fig. 2.15.

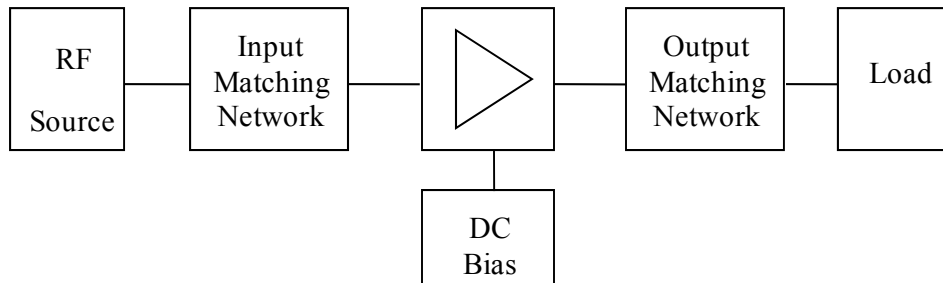


Fig. 2.15. Generic schematic of design of power amplifiers

The first step in design of matching networks for power amplifiers is to determine the impedances for optimum operation. This step is called load/source pull. The process of load/source pull is based on presenting different impedances at the input and output of the device in order to find the optimum operation points. This is a necessary step for devices with nonlinear response.



Different load/source pull methods can be categorized into different groups. For example, it can be either scalar or vector, depending on type of measurement. If measurement equipment such as power meter is used, it will be scalar, but using instruments such as vector network analyzers would make it vector. It can be active or passive, depending on the implementation of the variable load. Furthermore, load/source pull can be based on controlling the fundamental frequency only, or it can take into account effects of harmonic impedances as well.

There are some steps to be followed while studying load/source pull. First, target sets of load and source impedances (or reflection coefficients) should be determined and generated. Furthermore, the device should be biased. Fig. 2.16 shows a simplified schematic of a load-pull setup. After setting the impedances, either simulation or experimental measurements should be done on the device in order to find the desired responses (which can be output power, power gain, efficiency or distortion). Then the related contours can be generated and the optimum points can be determined accordingly [9].

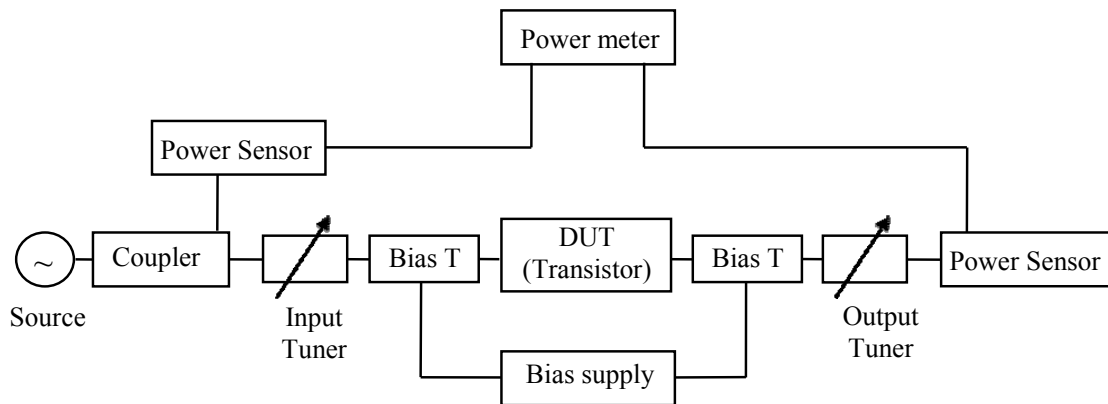


Fig. 2.16. Schematic of load-pull set up

## 2.4 Harmonic Termination

In addition to optimum impedances for fundamental frequency, impedances at the harmonic frequencies can play an important role in performance of power amplifiers. In other words, moving the harmonic impedances from one point of Smith chart to another can affect output power or PAE severely. Therefore, matching networks should not only provide the optimum impedances at fundamental frequency, but should also present the right harmonic terminations at the harmonics.

Variation of PAE and output power for a class AB power amplifier is shown in Fig. 2.17 for different second harmonic impedances. It should be noted that for class AB, unlike for classes such as F and E, harmonic impedances don't have to be at specific points of the Smith chart. In other words, in order to get higher efficiency, harmonics can be set to be in much wider regions than class E or F, meaning that we have a greater degree of freedom in setting them. This property of class AB makes it suitable for broadband design, because in case of need for harmonic adjustments, there won't be limited options, and therefore it will work for multiple frequencies of the broad bandwidth.

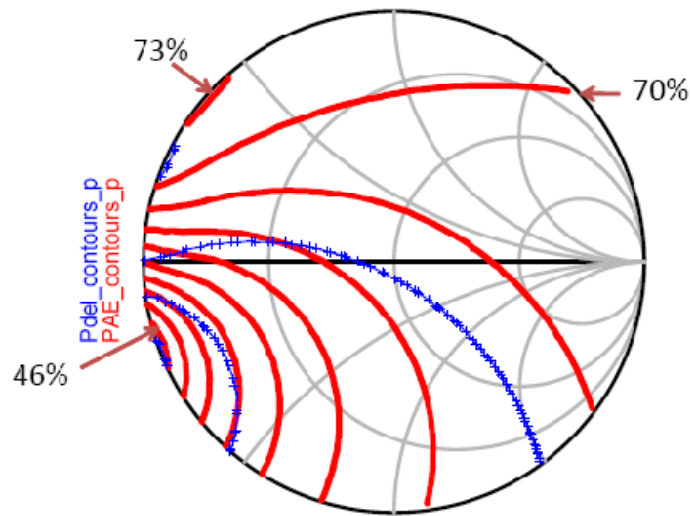


Fig. 2.17. Variation of PAE (solid) and output power (crossed) for a class AB power amplifier

## 2.5 Conclusion

In this chapter, some properties of power amplifiers - such as PAE, DE, and linearity factors - have been discussed. Furthermore, some details on different classes of operation of power amplifiers have been provided. After that, the load-pull concept and its procedure have been presented.

Classes of power amplifiers working as current source mode of operation are summarized in TABLE 2-1; as shown, moving from class A toward class C leads to smaller conduction angle, which results in higher efficiency but lower linearity. As discussed before, class AB has the best tradeoff. The other category, switching mode power amplifiers, although it achieves much higher efficiencies, generates strong nonlinearities. Furthermore, the complexity of their matching networks, and the harmonic terminations requirements for a single design frequency, make them less suitable for broadband power

amplifier design. For the aforementioned reasons, class AB is chosen as the class of operation for this thesis.

**TABLE 2-1.** Operation of power amplifiers working as current source [7]

<b>Mode</b>	Bias point ( $V_b$ )	Quiescent current	Conduction angle	Efficiency	Linearity
A	0.5	0.5	$2\pi$	Very low	High
AB	0-0.5	0-0.5	$\pi - 2\pi$	Medium	Fair
B	0	0	$\pi$	Good	Low
C	<0	0	0- $\pi$	Good	Very low

## Chapter 3

### Broadband power amplifier design approach

The most traditional and conventional ways of designing matching networks are categorized into three groups of matching networks with lumped elements, with mixed lumped and distributed elements, and with transmission lines. These methods are inherently narrowband. In other words, the design process using these methodologies is usually for one single frequency.

Matching networks **with lumped elements** can be in the form of L-transformer,  $\pi$ -transformer, or T-transformer, as shown in Fig. 3.1. They are widely used either as inter-stage or input/output matching networks of narrowband systems [6].

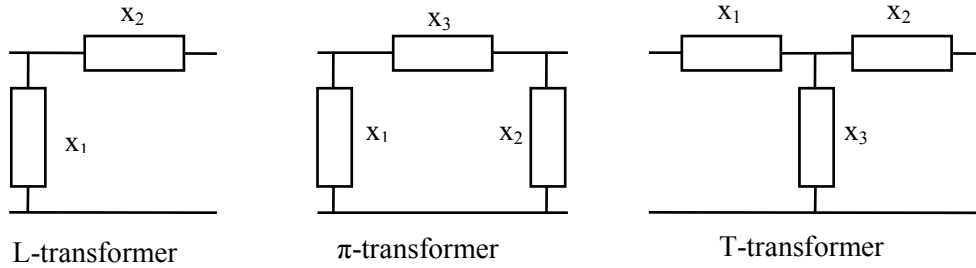


Fig. 3.1. Matching networks with lumped elements

In matching networks **with mixed lumped and distributed elements**, some of the lumped elements are replaced with equivalent transmission lines. Fig. 3.2 is an example for this transformation,

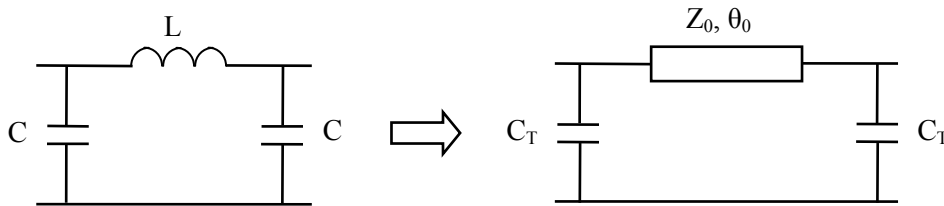


Fig. 3.2. Matching networks with mixed lumped and distributed elements

in which  $Z_0$  and  $C_T$  are defined as in (3.1) and (3.2),

$$Z_0 = \frac{\omega_0 L}{\sin \theta_0}, \quad (3.1)$$

$$C_T = \frac{\cos \theta_0 + \omega_0^2 LC - 1}{\omega_0^2 L}. \quad (3.2)$$

Matching networks **with transmission lines** can be used to transform an impedance to another one for a single frequency, by adjusting the length and characteristic impedance of the line. The input impedance of a transmission line with length of  $l$  and characteristic impedance of  $Z_0$ , which is terminated to impedance of  $Z_L$ , can be calculated using (3.3),

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan \beta l}{Z_0 + jZ_L \tan \beta l}. \quad (3.3)$$

Most common matching network with transmission line is a quarter-wave line, which makes the transformation in (3.4) possible.

$$Z_{in} = \frac{Z_0^2}{Z_L} \quad (3.4)$$

But as mentioned before, deviating from the designed frequency will result in deviation of matching, leading to higher reflection coefficients. As the required impedance ratio increases, this deviation becomes more severe, reducing the bandwidth of the matching network. This is shown in Fig. 3.3.

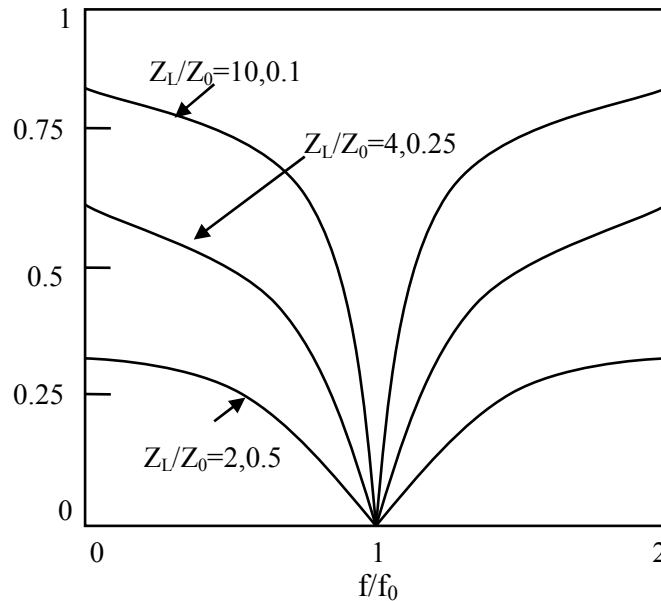


Fig. 3.3. Reflection coefficient vs. freq. of a transmission line (different impedance ratios) [10]

For broadband systems, we need matching networks that work for several frequencies rather than just one. Therefore, the aforementioned narrowband matching networks will no longer be useful, and broadband methodologies must be deployed in order to keep good performance over a broad range of frequencies. The following section concerns different broadband transformations. First a look into real-to-real transformations, and then this chapter will look into details of complex-to-real transformations, followed finally by discussion and comparison of these methods.

### 3.1 Broadband real-to-real transformations

#### 3.1.1 Multi L-section transformation

The first method is based on the Multi L-Section matching networks [2]. Actually, this method has the same structure as a conventional low-pass filter, as shown in Fig. 3.4. The difference is in the terminating resistors ( $R_0$  and  $R_5$ ); in the conventional structure, they are almost equal, but using this method, having different values for them becomes possible [11]. For this purpose, the parameter  $r$  as defined in (3.5) represents the transformation ratio. A large ratio results in severe mismatching at zero frequency, making the circuit behave like a band-pass filter [11], [6]. Another parameter of the design is the relative bandwidth as defined in (3.6).

$$r = R_0 / R_5 \quad (3.5)$$

$$w = 2(f_2 - f_1)/(f_2 + f_1) \quad (3.6)$$

where  $f_2$  and  $f_1$  are the upper and lower frequencies of the target frequency band.

After calculating the parameters of the design,  $g$ -values can be obtained using tables and equations of either [11] or [6].

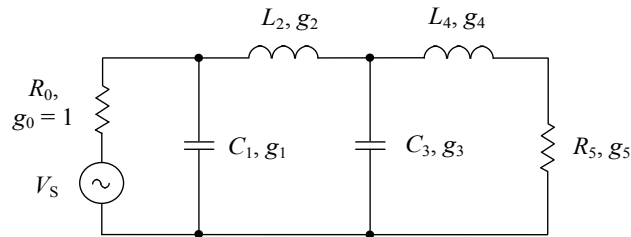


Fig. 3.4. Two section impedance transformer [6]

### 3.1.2 Multi section quarter-wave transformation

Obviously, a quarter-wavelength transmission line is a well-known narrowband impedance transformer, in which bandwidth decreases as the desired impedance ratio increases. Using Multi-Section Quarter-Wave Transformers, as shown in Fig. 3.5, increases the bandwidth. In other words, this method is known as a wideband impedance transformation.

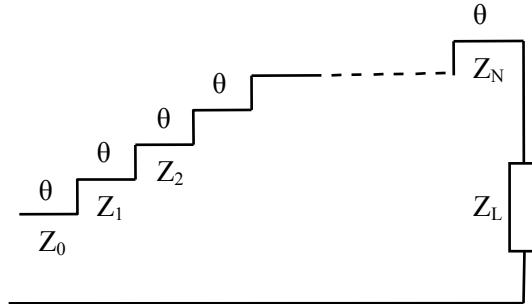


Fig. 3.5. Multi-section quarter-wave transformer

According to Fig. 3.5, load impedance  $Z_L$  is transformed to the source impedance  $Z_0$  using sections of quarter wavelength transmission lines ( $\theta=90^\circ$ ) with different characteristic impedances. Two major categories of these transformers are Binomial and Chebyshev, and characteristic impedances can be calculated according to the profile selected for the characteristic of the transformer [12].

The multi-section quarter-wave transformer results in circuits with large sizes and is therefore not optimum. The alternative solution is to use sections with lengths less than  $\lambda/4$  instead of fixed lengths. In this case, characteristic impedances have to follow certain patterns; for example odd-numbered sections have to be equal to load impedance, while the even-numbered ones should be equal to source impedance. More details and equations on this alternative solution are provided in [6].

### 3.1.3 Tapered transmission line transformation

Tapered transmission line transformation is another method, known as the broadband methodology. Despite that multi-section quarter-wave transformers' characteristic impedances vary discretely, this method deals with characteristic impedances which vary continuously, as shown in Fig. 3.6.

Tapered lines can mainly be categorized in three major groups: exponential tapers, triangular distributed tapers, and Chebyshev tapers, each having different formulas for their characteristic impedances [12], [2].

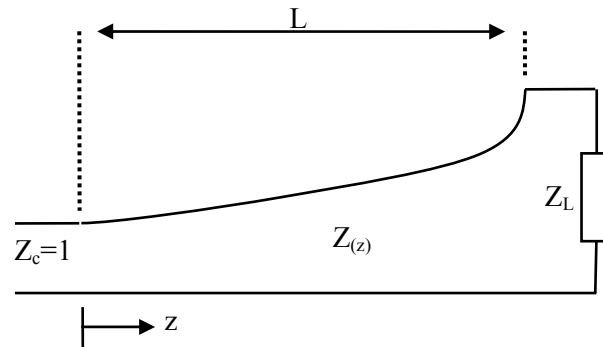


Fig. 3.6. Tapered transmission line transformer

## 3.2 Broadband complex-to-real transformations

### 3.2.1 Multi L-section transformation for complex loads

Multi L-section transformation is used to design the broadband MN, as it is the most suitable approach for complex to real impedance conversion. This approach can be applied for any targeted bandwidth as long as the resulting J-inverters are kept within a reasonable range. Following are more details on this method.

Multi L-section transformation for a complex load is based on Chebyshev filter theory [13], [14]. There are two possible prototypes for a Chebyshev low-pass filter, as shown in Fig. 3.7. The load can either be represented as a resistance and an inductance in series, or a resistance and a capacitor in parallel.



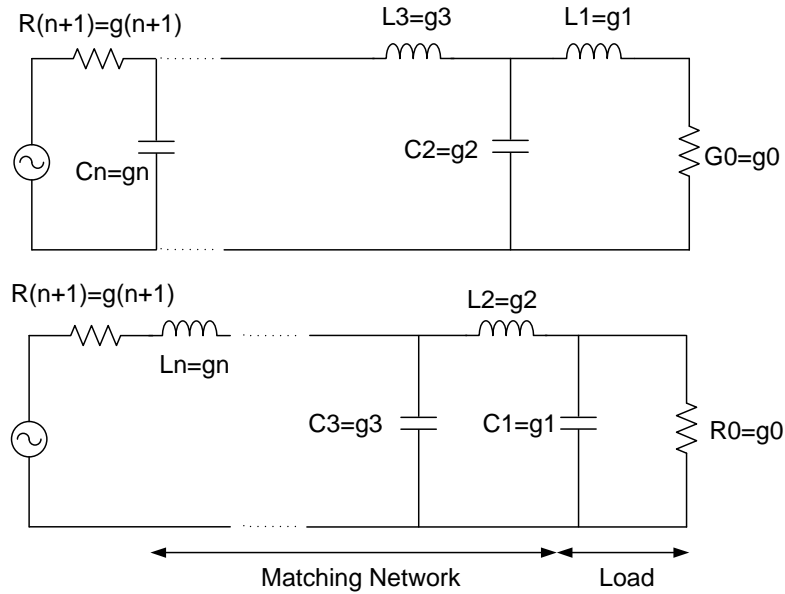


Fig. 3.7. Two possible prototypes for low-pass design [14]

In this method, the reactive part of the load is considered as the first element of the filter. Given the reactive part of the load, a load decrement factor  $\delta$  is calculated using (3.7) [13],

$$\delta = \frac{1}{g_0 g_1 \omega_1'} = \frac{1}{G_0' L_1' \omega_1'} = \frac{1}{R_0' C_1' \omega_1'}, \quad (3.7)$$

in which  $\omega_1'$  is the cut-off frequency.

Knowing  $\delta$ , the  $g$ -values of a low-pass Chebychev prototype can be calculated using either analytical equations as in (3.8) to (3.11) [14] or graphs in [13].

$$D = \frac{d}{\delta \sin(\pi/2n)} - 1 = \frac{g_0 g_1}{g_{n+1} g_n}, \quad (3.8)$$

$$g_1 = \frac{1}{\delta \omega_1' g_0}, \quad (3.9)$$

$$g_j \Big|_{j=2,4,\dots} = \frac{1}{g_{j-1} K_{j-1,j}^2 \omega_1'^2}, \quad (3.10)$$

$$g_{n+1} = \frac{1}{D\delta g_n \omega_1}, \quad (3.11)$$

in which  $n$  is the order of the filter and  $g_0=1$  and  $\omega_1=1$  for a normalized prototype.  $k_{j-1,j}$  are coupling coefficients that can be determined using (3.12):

$$k_{r,r+1} = \left( \frac{\sin^2(r\theta)\cos^2(r\theta) + (\cos^2(r\theta) + D^2\sin^2(r\theta))\sin^2\theta\delta^2}{\sin(2r-1)\theta\sin(2r+1)\theta} \right)^{1/2}, \quad (3.12)$$

in which  $\theta=\pi/2n$ .

However, 50 ohm at the source side is not guaranteed using the low-pass prototype. Therefore, another transformation is needed along with this method; transforming the low-pass to band-pass is the solution to this problem.

In the band-pass design, as shown in Fig. 3.8, the first resonator is part of the load. Others must be chosen to resonate at the center frequency. The values of the J-inverters will be determined using  $g$ -values of the low-pass filter and the slope of the susceptance of the resonators (as in (3.13) to (3.16)). Finally the 50 ohm at the source side can be achieved by setting GB to 50 ohm. The dual of this circuit holds for the loads modeled in series.

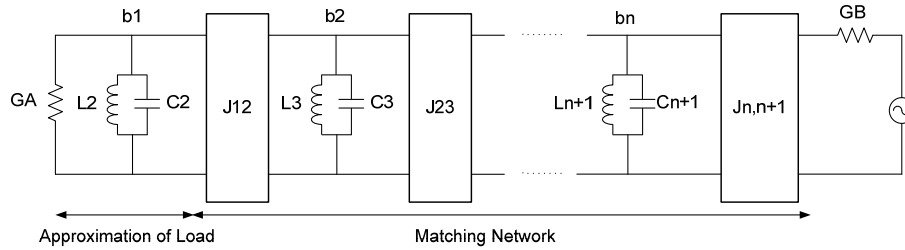


Fig. 3.8. Schematic of band-pass prototype

$$J_{12} = \frac{1}{\omega_1} \sqrt{\frac{wG_A b_2}{g_1 g_2 \delta}} \quad (3.13)$$

$$J_{k,k+1}|_{k=2\text{ton}} = \frac{w}{\omega_1} \sqrt{\frac{b_k b_{k+1}}{g_k g_{k+1}}} \quad (3.14)$$

$$J_{n,n+1} = \sqrt{\frac{G_B b_n w}{g_n g_{n+1} \omega_1}} \quad (3.15)$$

$$b_j = \frac{\omega_0}{2} \frac{\partial B_j(\omega)}{\partial \omega} \Big|_{\omega=\omega_0} \text{ mhos} \quad (3.16)$$

in which  $\omega_0 = \sqrt{\omega_1 \omega_2}$ ,  $w = \frac{\omega_2 - \omega_1}{\omega_0}$ .

The above-mentioned structure works for bandwidths as high as 20%; for higher bandwidths the structure is different in the following ways. For a series-resonated load, there is no J-inverter between the load and the second resonator ( $b_2$  in Fig. 3.8), and  $b_2$  cannot be an arbitrary value. It should be calculated using (3.17). The rest of the structure is the same, as Fig. 3.8 shows, and J-values are calculated using (3.14) and (3.15) [13]. The dual of this structure is used for a shunt-resonated load.

$$b_2 = \frac{\omega_1 g_2}{w g_0 R_A} \quad (3.17)$$

Furthermore,  $\delta$  is calculated differently from (3.7). Considering a series-resonated load  $Z_L$  or a shunt-resonated load  $Y_L$ , we have,

$$R_A = \text{Re}(Z_L|_{f=f_0}), \quad \delta = \frac{R_A}{|\text{Im}(Z_L)|_{f=f_1 \text{ OR } f_2}}, \quad (3.18)$$

$$G_A = \text{Re}(Y_L|_{f=f_0}), \quad \delta = \frac{G_A}{|\text{Im}(Y_L)|_{f=f_1 \text{ OR } f_2}}, \quad (3.19)$$

in which  $f_0$  is the center frequency,  $f_1$  and  $f_2$  are edge frequencies of the band.

### 3.2.2 Direct synthesis method

The direct synthesis method is another way of designing the MNs for transforming the complex load to a real impedance. This method deploys filter theory in order to obtain an expression for  $Z_{22}(s)$  shown in Fig. 3.9.  $Zl(s)$  represents the load impedance versus frequency [15], [2].

It should be noted that this method doesn't guarantee 50 ohm at the source side (R of the Fig. 3.9), and should be combined with another transformation method in order to get 50 ohm.

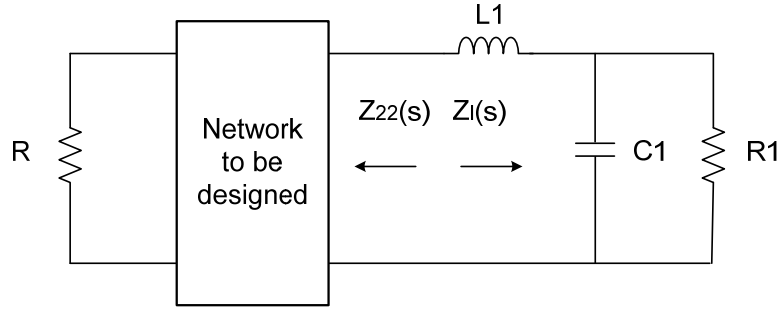


Fig. 3.9. Matching network design using direct synthesis method [15]

In order to use this method, first the transducer power gain (ratio of the output power to the input power) versus frequency response should be chosen, and then required load and source resistances should be determined. After that there are 4 steps to follow:

**First step:** all the  $\omega^2$  terms of the specified transducer power gain ( $G_T(\omega^2)$ ) should be replaced with  $-s^2$  terms. Then  $\rho(s)\rho(-s)$  product (in which  $\rho(s)$  is the reflection coefficient of  $Z_{22}(s)$ ) can be determined using (3.20):

$$\rho(s)\rho(-s) = 1 - G_T(-s^2). \quad (3.20)$$

**Second step:** In order to determine  $\rho(s)$ , all the left half plane holes of  $\rho(s)\rho(-s)$  must be assigned to  $\rho(s)$ , and the zeros should be assigned in conjugate pairs according to the relationship between  $\rho(s)$  and  $\rho(-s)$ .

**Third step:** using (3.21),  $r_l(s)$ , the even part of the load impedance  $Z_l(s)$ , can be found.

$$r_l(s) = 0.5[Z_l(s) + Z_l(-s)]. \quad (3.21)$$

After that, we have (3.22):

$$F(s) = 2r_l(s)A(s). \quad (3.22)$$

in which  $A(s)$  is defined as in (3.23):

$$A(s) = \prod_i [s - s_i] / [s + s_i]. \quad (3.23)$$

In other words,  $A(s)$  is an all-pass system with poles ( $s_i$ ) equal to the open left half plane poles of load impedance,  $Z_l(s)$ .

Knowing  $A(s)$ ,  $F(s)$ , and  $\rho(s)$ ,  $Z_{22}(s)$  can be determined using (3.24):

$$Z_{22}(s) = \frac{F(s)}{A(s) - \rho(s)} - Z_1(s). \quad (3.24)$$

**Fourth step:** Having  $Z_{22}(s)$ , the required network can be synthesized using standard filter theory.

### 3.2.3 Parasitic absorption principle

The Principle of Parasitic Absorption can be used along with some of the real-to-real transformation techniques in order to match a complex load to a real one. When the load impedance can be modeled as a simple RL, RC, or RLC, the parasitic absorption method states that the design procedure can be accomplished by first ignoring the reactive part of the load, and then absorbing the reactive element into the design. For example, if the complex load is modeled by a resistant of 1kohm and capacitance of 1pF, the design will be done for transforming the 1kohm to the desired real impedance. After that, if the designed matching network can be said to have a capacitance of 3pF as the first element, then a 2pF capacitance must be placed, because 1pF is already achieved by the complex part of the load. This method is a possible solution as long as the reactive part of the load doesn't exceed the value of the first reactive element of the design [15], [2].

## 3.3 Discussion

Now that different methods for designing matching networks have been discussed in details, they can be compared in terms of the advantages and disadvantages of each of them.

The narrowband matching networks are convenient to design and simple, with a few elements in their structure, but they are only good for single frequencies, and for broader bandwidths their performance will degrade fast as the frequency deviates from the designed one. Therefore, narrowband matching networks are no longer useful for broadband designs.

In broadband transformations, real-to-real transformations only work for transforming real impedance to another real impedance. In other words, load impedance has to be a real one and can't be complex impedance. However, for optimum operation, most of the transistors are modeled with complex loads. Therefore, real-to-real transformations are not helpful by themselves and complex-to-real transformations should be deployed for design of power amplifiers.

In broadband complex-to-real transformations, the parasitic absorption principle is simple, but only works for simple load models of RC, RL, and RLC. Furthermore, the reactive part of the load is limited to the first reactive element of the design.

On the other hand, the direct synthesis method works for any kind of load, no matter how complex it is. Furthermore, it has no limit on the bandwidth as long as all the elements are lumped. The drawback is it doesn't guarantee the 50 ohm at the source side and makes another real to real transformation necessary along with it.

Multi L-section transformation for complex loads works for simple RC and RL loads. Just like the direct synthesis method, it has no limit on the bandwidth while lumped elements are used. It also doesn't guarantee 50 ohm at the source side, but transforming the low-pass prototype to band-pass one solves this problem.

In conclusion, narrowband matching networks are not good enough for broadband power amplifier design or real-to-real transformations by themselves. Therefore, considering the advantages and disadvantages of different complex-to-real transformations, the **multi L-section transformation for complex load** is chosen as the main methodology used in this work, because it works for a simple RC or RL model of the transistor and can have bandwidths as high as 40% even when transmission lines are used in the structure. Most importantly, the band-pass prototype guarantees the 50 ohm at the source side, which is an important requirement of the design.

## Chapter 4

### Design of broadband power amplifier using ADS

In this chapter, the design procedure followed for design of broadband class AB power amplifiers will be discussed. GaN HEMT technology has many advantages to its choice, because of its high power capability and high drain-source resistance (for easier matching). In this regard, we have picked the transistor of CREE with GaN HEMT technology, CGH40025 (25W device), for this project. A substrate of Rogers RT5870 is also chosen for the realization of the PA prototype. The bias points are chosen to have class AB operation. Furthermore, two frequency ranges of 1.8-2.2 GHz (20% bandwidth) and 1.8-2.7 GHz (40%) are targeted. Subsequently, different steps of the design using Advanced Design System (ADS) are discussed.

#### 4.1 Load-pull simulation

As mentioned in previous sections, the first step in design of power amplifiers is to determine the optimum load and source impedances for their matching networks. Therefore, required load-pull simulations have been done following the steps discussed as in section 2.3. For this, a large-signal model of the transistor (provided by the manufacturer) is used in the simulations. Therefore, all the design procedure and results rely on this model of the transistor.

It should be noted that load-pull simulation is good for one frequency (the frequency which has been set for the load-pull setup), but designing broadband power amplifiers requires finding optimum impedances for sets of frequencies. Therefore, the load-pull simulation must be done separately for several frequencies of the band of interest. With setting the harmonic impedances to 50 ohm, TABLE 4-1 shows the optimum load and source impedances found for different frequencies of the band (1.8-2.7 GHz).

#### 4.2 Impedance modeling

In order to design the matching networks, the first step is to model the input and output of the transistor according to the optimum load and source impedances. In other words, the optimum load and source impedances for different frequencies determines the input and output impedances that the transistor presents at that frequency (which are  $Z_s^*$  and  $Z_L^*$  for the transistor, according to the conjugate match theory, which states that the maximum power transfer occurs when the load is conjugate matched).

As discussed in section 3.2.1, a transistor's input and output impedances can either be modeled as a resistance and an inductance in series, or a resistance and a capacitor in parallel. When the real part of the impedance is more constant than the real part of the admittance, it is better to go with series RL modeling; otherwise, parallel RC is preferred.

**TABLE 4-1.** Optimum load and source impedances (1.8-2.7 GHz)

<b>Freq (GHz)</b>	<b>Z<sub>L</sub>(fundamental)</b>	<b>Z<sub>s</sub>(fundamental)</b>
<b>1.8</b>	12.382+j11.59	4.344-j3.656
<b>1.85</b>	12.867+j10.38	5.627+j1.313
<b>1.9</b>	12.867+j10.38	6.037-j0.75
<b>1.95</b>	11.618+j9.963	5.795-j1.777
<b>2</b>	11.618+j9.963	4.334-j3.656
<b>2.05</b>	11.618+ j9.963	4.334-j3.656
<b>2.1</b>	10.416+j9.568	1.298-j4.451
<b>2.15</b>	10.416+j9.568	3.156-j4.451
<b>2.2</b>	10.416+j9.568	3.156-j4.451
<b>2.3</b>	10.211+j8.600	2.819-j1.348
<b>2.4</b>	9.230 +j8.326	3.375-j2.6
<b>2.5</b>	9.243+j7.272	3.601-j2.937
<b>2.6</b>	9.243+j7.272	3.882-j3.282
<b>2.7</b>	9.287+j6.238	3.882-j3.282

The procedure chosen for modeling is as follows: after choosing between series and parallel structure, for the real part of the impedance (admittance) the average of the real parts of the impedances (admittances) over the target frequency range have been considered. In other words, for series structures, the resistance value of the model has been set to be the average of the real parts of the impedances and for the parallel one, the conductance of the model is equal to average of the real parts of the admittances. For the reactive part of the model, the curve fitting tool of the MATLAB has been used to find the values for L or C that best fit the imaginary part of the impedances and admittances over the frequency band.

At the input of the design with 20% bandwidth, considering  $Z_s^*$  and  $Y_s^*$  values for frequencies of 1.8 to 2.2 GHz, it is found that both the real part of admittances and the real part of impedances are widely variant, which results in poor modeling. In order to solve this problem, the impedances of the transistor along with an ideal transmission line are considered for modeling. The new sets of impedances have less variant real parts and more suitable imaginary parts for fitting. Choosing the series RL structure for the



model, the average of the real part of impedances is  $R=5.22$  ohm. By using the curve fitting tool of MATLAB to fit the imaginary parts of  $Z_L^*$  to  $L\omega$  for different frequencies, it can be found that  $L=0.8$  nH best models the optimum impedances at the source side. In summary, for the 20% bandwidth, input of the transistor along with a piece of transmission line is modeled with  $R=5.22$  ohm and  $L=0.8$  nH in series.

At the output of the design with 20% bandwidth, considering  $Z_L^*$  and  $Y_L^*$  values for frequencies of 1.8 to 2.2 GHz, it is found that the real part of admittances is less variant than the real part of impedances. Therefore, the output of the transistor is modeled with parallel RC. The average of the real part of admittances is 0.048, which means  $R=20.83$  ohm. By using the curve fitting tool of MATLAB to fit the imaginary parts of  $Y_s^*$  to  $C\omega$  for different frequencies, it can be found that  $C=3.427$  pF best models the optimum admittances at the load side. Therefore, for the 20% bandwidth, output of the transistor is modeled with  $R=20.83$  ohm and  $C=3.427$  pF in parallel.

For the design with 40% bandwidth, experiences gained from design with 20% bandwidth are used. Therefore, considering the practical issues such as required long-enough soldering pads right before and after the transistor, transmission lines are added at the input and output of the transistor, right at the beginning of the design procedure, in order to reduce the amount of tuning required in subsequent steps.

For modeling of the input of the transistor for 40% bandwidth, impedances of the transistor along with the transmission line of electrical length  $20^\circ$  are considered from 1.8 to 2.7 GHz. Following the same procedure of taking the average and curve fitting resulted in a series structure with  $R=4.34$  ohm and  $L=1.53$  nH.

The same process for the output of the transistor led to  $R=11.42$  ohm and  $L=1.3$  nH.

Now that the transistor is modeled at the input and output side for both of the designs, we can proceed to the next step of the design, which is design of input and output matching networks. Details of these steps are provided in the next sections.

### **4.3 Design of output matching network for 20% bandwidth**

For design of matching networks using multi L-section transformation for complex loads, the design procedure discussed in section 3.2.1 should be followed. Considering the frequency band of 1.8 to 2.2 GHz, the center frequency of  $f_1'$  is 2 GHz. Having the load model of  $R=20.83$  ohm and  $C=3.427$  pF in parallel according to previous section, and using (3.7), gives:

$$\delta = \frac{1}{20.83 \times 3.427E(-12) \times 2\pi E9} = 1.11$$

Now that  $\delta$  is found,  $g$ -values should be calculated using either the equations of (3.8) to (3.11) or the graphs of [13]. The  $g$ -values for this work are calculated using graphs. Choosing the filter to be of the order of 4 ( $n=4$ ), the graphs shown in Fig. 4.1 are used and the followings are obtained:

$$g_1=0.9, g_2=1.16, g_3=1.34, g_4=0.52, g_5=1.15.$$

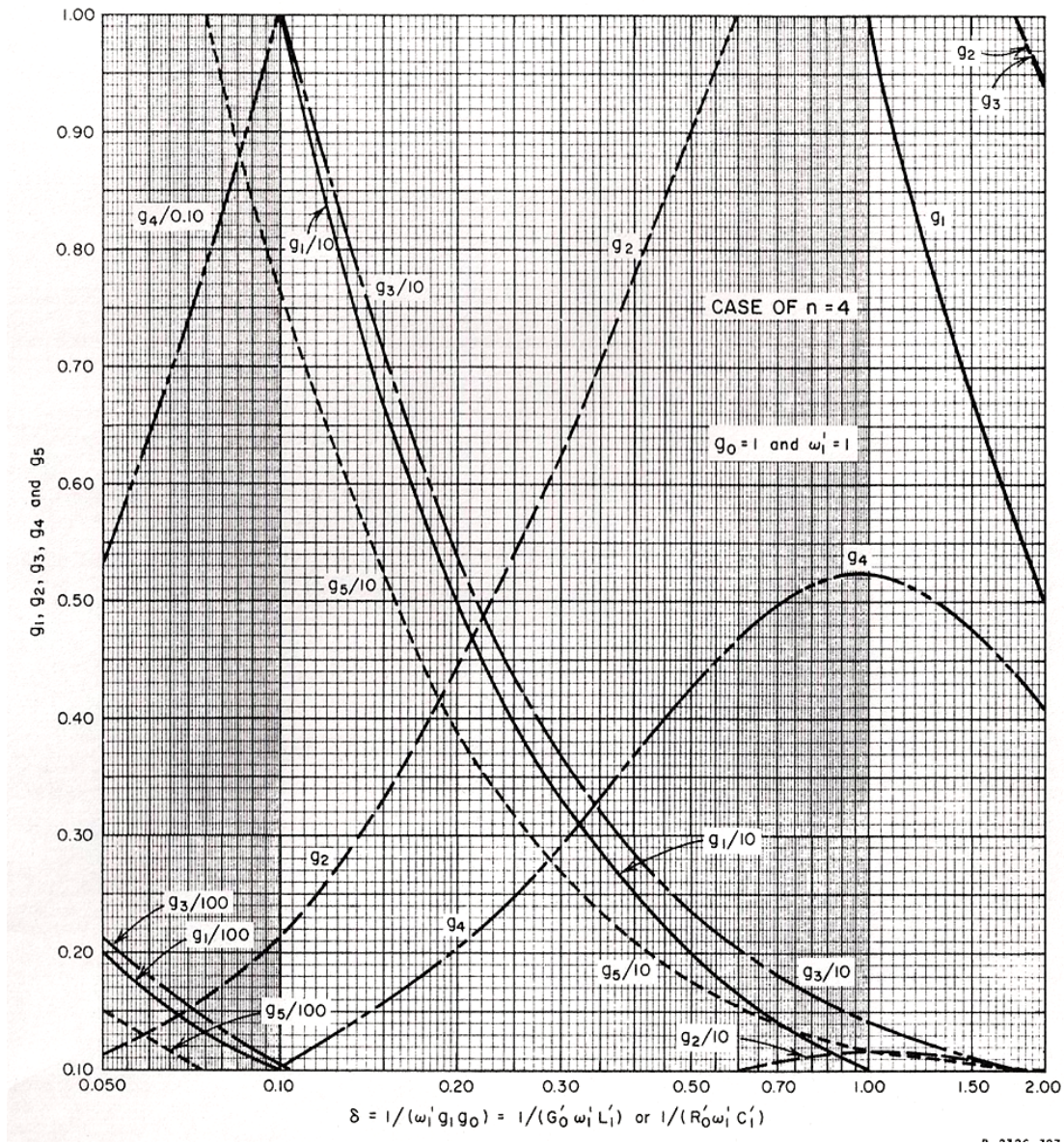


Fig. 4.1.  $g$ -values versus  $\delta$  for 4<sup>th</sup> order low-pass Chebychev filter [13]

Now using the structure of Fig. 3.8 along with the equations of (3.13) to (3.16), J-values for the J-inverters can be calculated. It should be noted that  $w=0.2$  (relative bandwidth) and in this work instead of LC resonators,  $\lambda/4$  short circuit transmission lines are used for  $b_2$  to  $b_n$ . Finally, the ideal output matching network is designed as shown in Fig. 4.2.

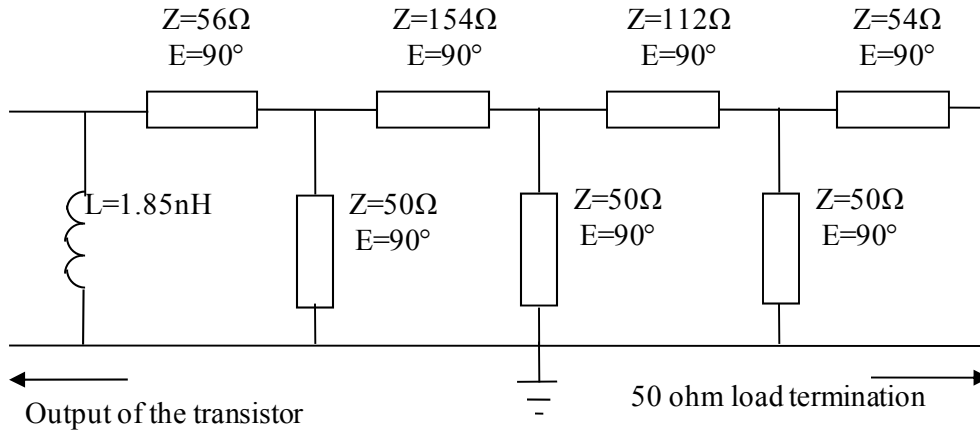


Fig. 4.2. Designed ideal output matching network for 20% bandwidth

Now that the ideal output matching network is designed, some practical issues should be taken into account. Furthermore, while trying to make the simulations as close as possible to the real world results, the ideal circuit should be transformed to its equivalent practical circuit. For example, practically for soldering, transmission lines longer than the transistor ports are required before and after them. Moreover, ideal transmission lines and lumped inductances should be replaced with their equivalent microstrip lines. Tee junctions should be used for intersections of transmission lines and steps should be inserted wherever there is severe impedance difference between two connected transmission lines. All these changes make a lot of tuning necessary.

For more accurate results predicting behavior of the fabricated design, momentum simulation is used along with ADS simulations. Momentum simulation predicts the performance considering almost all the electromagnetic factors that may affect the results. Therefore, good agreement between momentum simulation results and measurement results can be expected. This step requires further tuning which will lead us to the final layout of the output matching network.

#### 4.4 Design of input matching network for 20% bandwidth

Design of the input matching network follows almost the same procedure as that for the design of the output matching network discussed in the previous section. The difference is that unlike the output of the transistor which was modeled with parallel RC, the input of it is modeled with series RL of  $R=5.22$  ohm and  $L=0.8$  nH. Having the load in series means the band-pass structure should be dual of the structure shown in Fig. 3.8. In other words, J-inverters are replaced with K-inverters and series resonators are used instead of parallel resonators. Since this work targets high frequencies, in which lumped elements show poor behavior, lumped resonators should be replaced with equivalent transmission lines. This requires short circuit transmission lines in series, which is not realizable. Therefore, the alternative solution is to use structures for higher bandwidth, which have parallel resonators for the series loads (as discussed in section 3.2.1).  $b_2$  and  $\delta$  are calculated using (3.17) and (3.18). The rest is the same as for the output matching network. With  $\delta=2$ , g-values are found as followed:

$$g_1=0.5, g_2=0.94, g_3=0.94, g_4=0.41, g_5=1.$$

Designed ideal input matching network is shown in Fig. 4.3.

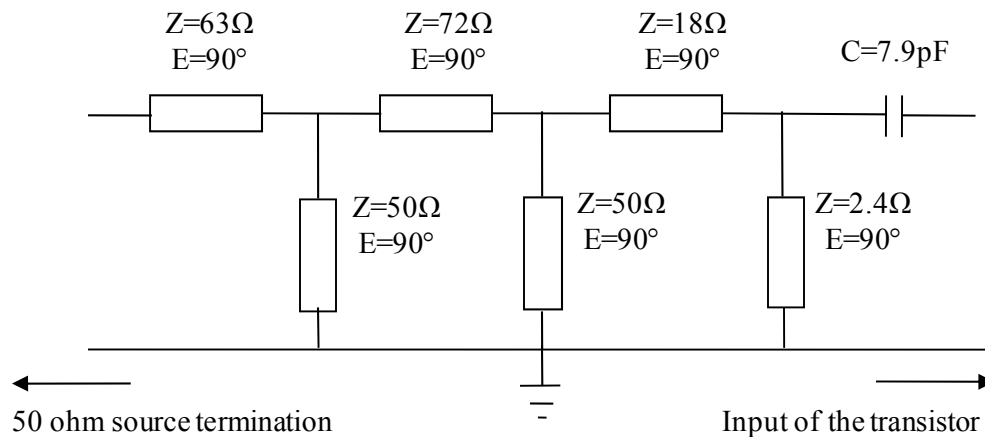


Fig. 4.3. Designed ideal input matching network for 20% bandwidth

#### 4.5 Design of bias network

The traditional way of designing a bias network deploys quarter-wavelength transmission line terminated to capacitances to the ground. With this, DC power will get to the transistor without affecting the matching network at the fundamental frequency. This is because a  $\lambda/4$  transmission line shorted to the ground acts like an open circuit at the fundamental.

For this work, we started with a  $\lambda/4$  transmission line at the center frequency, but due to effects of the harmonics, as discussed in section 2.4, we had to adjust the bias line. Further details on analysis, design and adjustment of the bias network are provided in the next section.

#### 4.6 Simulation results of performance of the designed PA (20% BW)

Now that all three steps of design of the power amplifier are done, more analyses are carried out using ADS to characterize performance of the power amplifier. For example, Fig. 4.4 represents the fundamental impedances of a broadband output matching network in comparison to load-pull based impedances. It is shown that impedances of the broadband matching network (circles in the middle of Smith chart) deviate from load-pull ones (crosses) in the middle of the band, but they are almost the same at the edges of the bandwidth. Furthermore, it should be noted that second harmonic impedances (circles around the Smith chart) show widespread scattering, which may lead to drop of efficiency at some frequencies (as discussed in section 2.4).

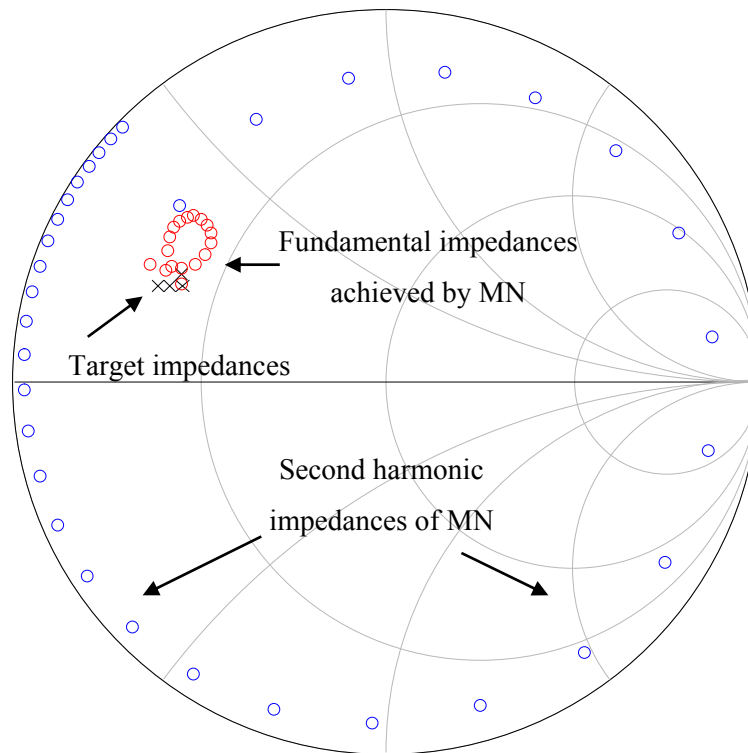


Fig. 4.4. Fundamental and second harmonic impedances over BW before adjustment (20% BW)

Characteristics of the designed power amplifier in terms of PAE and output power are illustrated in Fig. 4.5. According to Fig. 4.5, while PAE is higher than expected in higher frequencies, there is a severe drop of PAE in the middle of the band. Since the fundamental impedances for these frequencies are close to the optimum load values, investigation continued considering the effect of the second harmonic impedances on PAE and output power by examining the device characteristics.

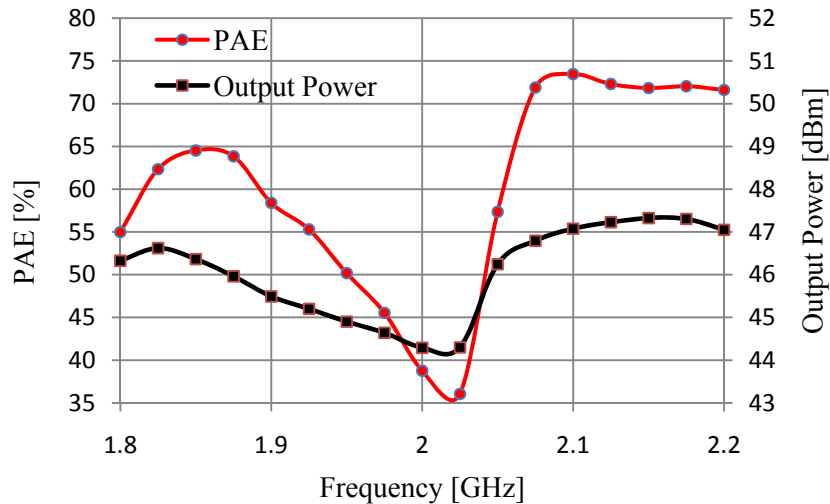


Fig. 4.5. Simulated output power and PAE characteristics of broadband PA before adjustment (20% BW)

At this point, PAE and output power contours for different second harmonic impedances were drawn (similar to ones in Fig. 2.17) for several frequencies. The results show that second harmonic impedances can play a significant role in PAE of the design, so that certain impedance values can cost about 20-30% drop of efficiency. Therefore, next step of the design is dedicated to adjusting the class AB operation by changing the second harmonic impedances while avoiding explicit 2<sup>nd</sup> harmonic termination.

For short circuiting second harmonic impedances, a quarter-wavelength transmission line connected to the ground via capacitances can be used. Having the  $\lambda/4$  transmission line in the bias network eliminates the need for adding an extra stub for adjusting the second harmonic impedances. For adjustment of impedances, moving the  $\lambda/4$  bias line along the series transmission line (connected to the output of the transistor) is used. The effect of this adjustment is shown in Fig. 4.6. It is depicted that second harmonic impedances are much less widespread around the Smith chart and they have been adjusted to be at the points where higher PAE is expected.



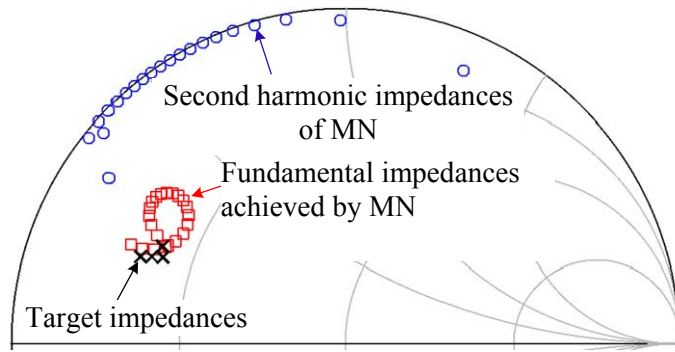


Fig. 4.6. Fundamental and second harmonic impedances over BW after adjustment (20% BW)

With adjusted second harmonic impedances, performance of the power amplifier is investigated once more. The results are illustrated in Fig. 4.7. It is shown that PAE of 65% (+/-5%) is achieved, output power varies between 44.5 and 47.5 dBm, and the severe drop in the middle of the band no longer exists.

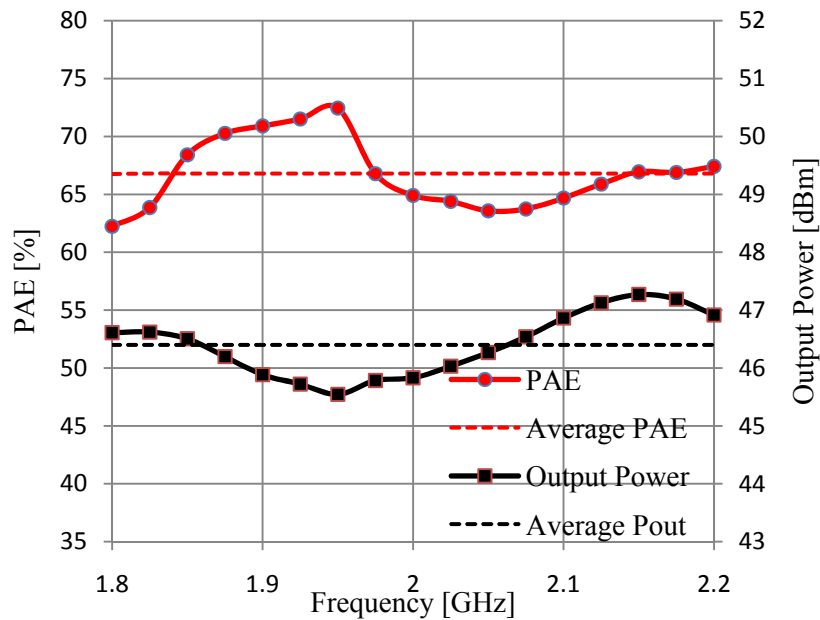


Fig. 4.7. Simulated output power and PAE characteristics of broadband PA after adjustment (20% BW)

Further investigations show that using a tapered line instead of conventional quarter-wavelength transmission line in the bias network results in even less widespread second harmonic impedances, and improved performance accordingly. Therefore, as an alternative adjustment, tapered transmission line is used in the bias network. Fig. 4.8 represents the resultant fundamental and second harmonic impedances over the target bandwidth. Furthermore, Fig. 4.9 shows the power amplifier performance.

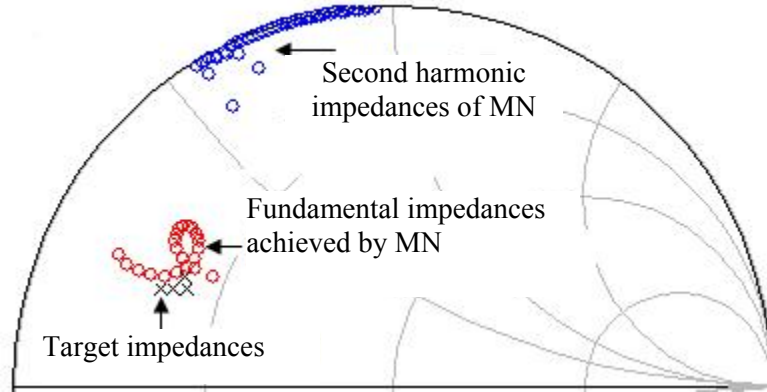


Fig. 4.8. Fundamental and second harmonic impedances over BW using tapered line (20% BW)

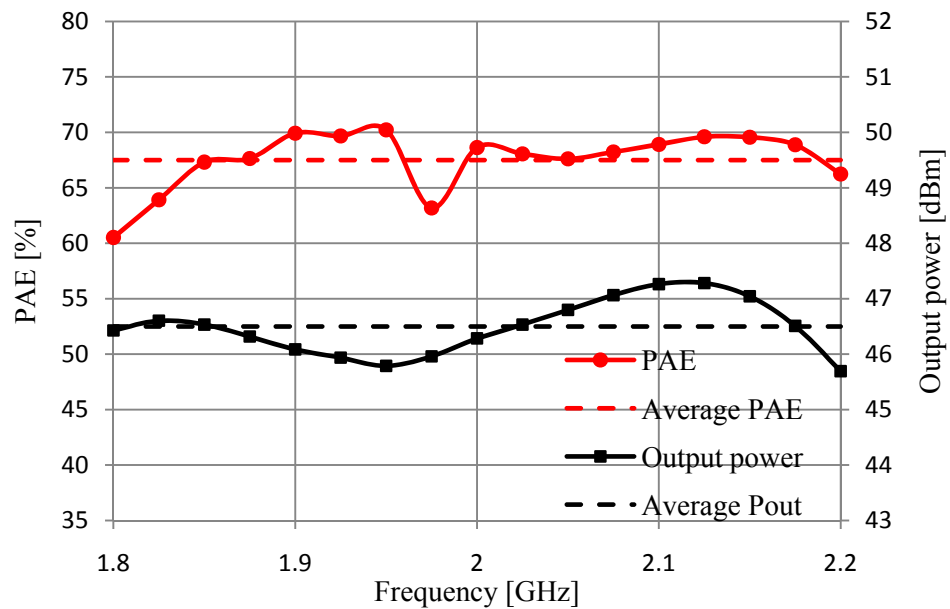


Fig. 4.9. Simulated output power and PAE characteristics of broadband PA using tapered line (20% BW)

After getting promising simulation results for performance of the power amplifiers, final layouts were sent out for fabrication. Fig. 4.10 shows the layout of the input and the output of the design. Some of the transmission lines are bent in order to reduce the size of the circuit. Some extra pads with connection to the ground are added around short circuit stubs in case there was more tuning necessary while measuring. Furthermore, there are holes everywhere in order to connect the PCB to its base firmly.



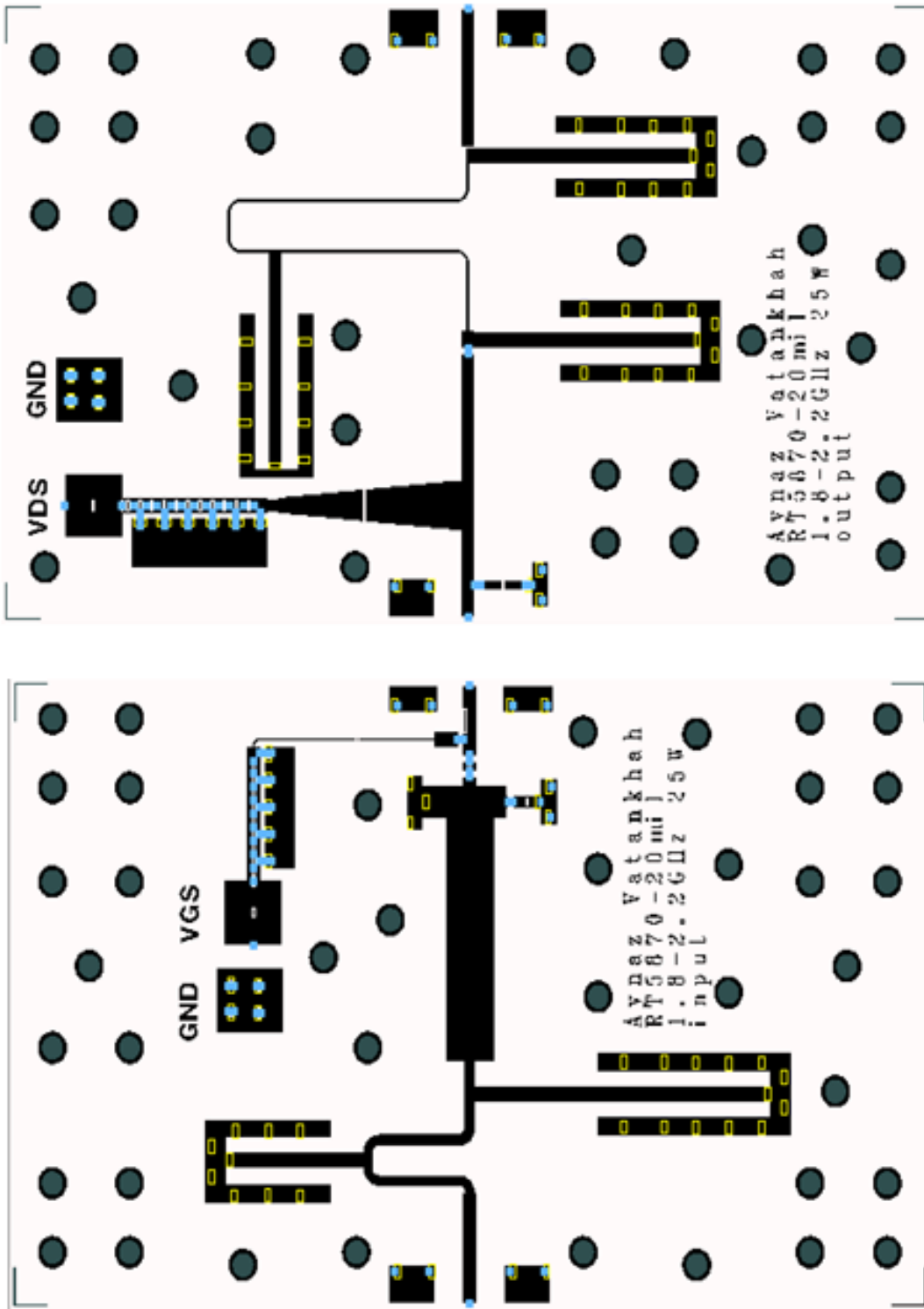


Fig. 4.10. Layout of input (at the bottom) and output (at the top) of the design (20% BW)

### 4.7 Design of output matching network for 40% bandwidth

Design of the output matching network for 40% bandwidth (1.8 to 2.7 GHz) has the same structure used in section 4.4. For this design, the order of the filter has been reduced to 3 instead of 4 in order to reduce the size. Therefore, g-values are determined using a different graph, as shown in Fig. 4.11.

Using (3.18) we get  $\delta=1.5$  and it is followed by these results:

$g_1=0.7, g_2=0.9, g_3=0.55, g_4=0.95$ . Finally it leads to the circuit designed as in Fig. 4.12.

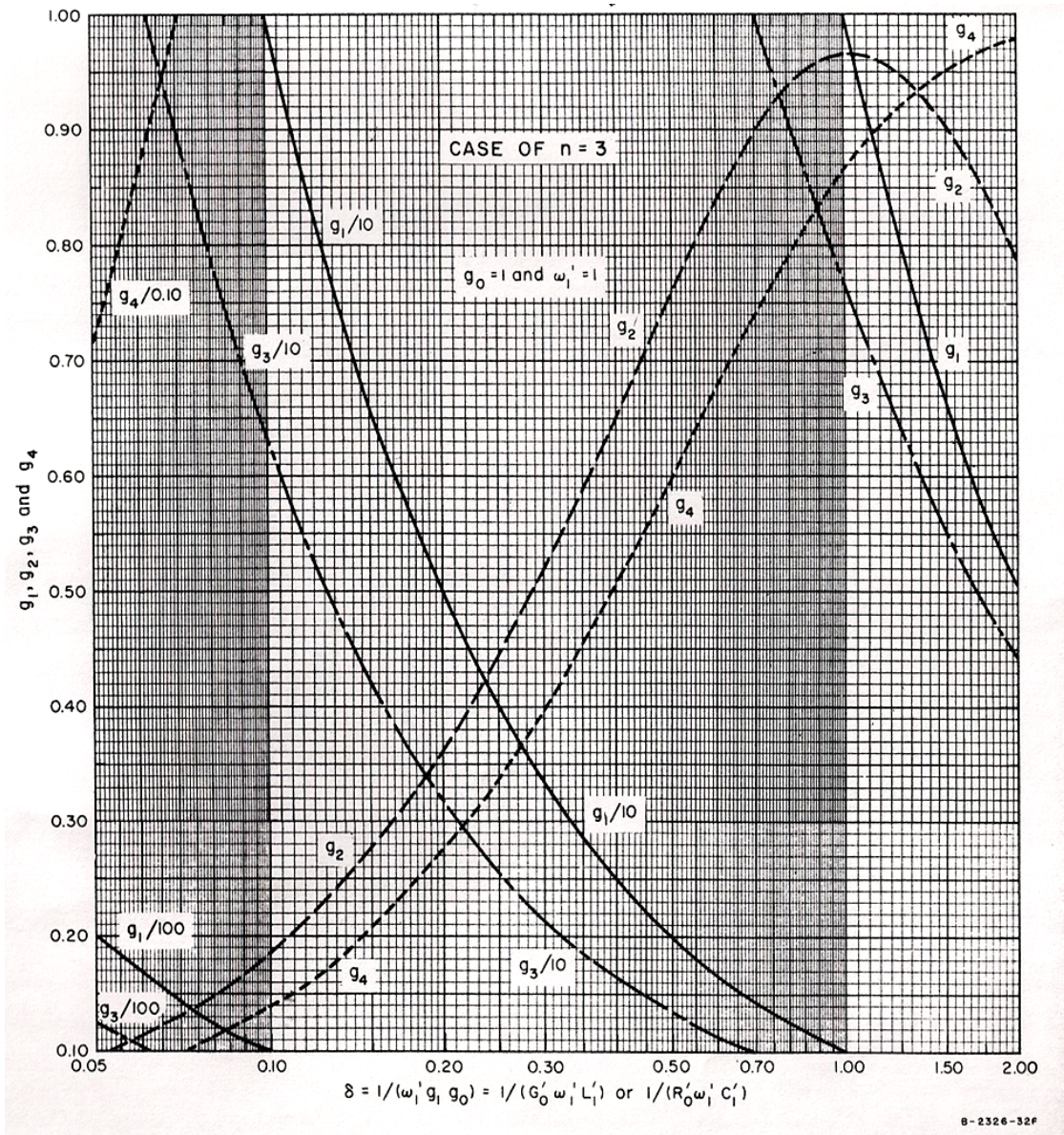


Fig. 4.11. g-values versus  $\delta$  for 3<sup>rd</sup> order low-pass Chebychev filter [13]

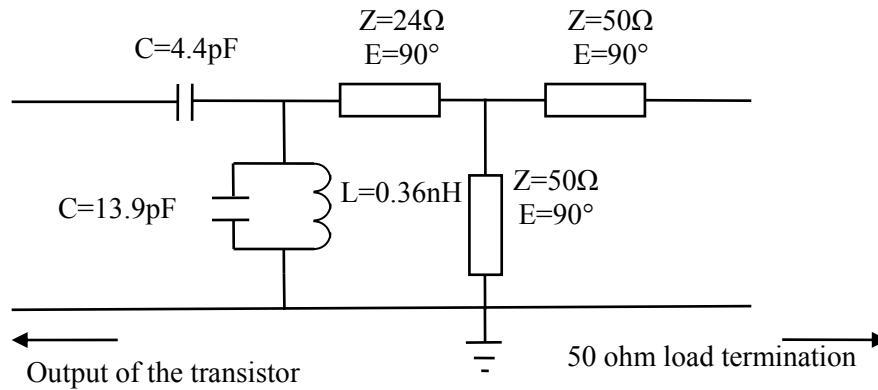


Fig. 4.12. Designed ideal output matching network for 40% bandwidth

#### 4.8 Design of input matching network for 40% bandwidth

Following the same procedure of previous section, with  $\delta=0.49$ ,  $g_1=2$ ,  $g_2=0.75$ ,  $g_3=1.3$ ,  $g_4=0.6$ , the resultant matching network is shown in Fig. 4.13.

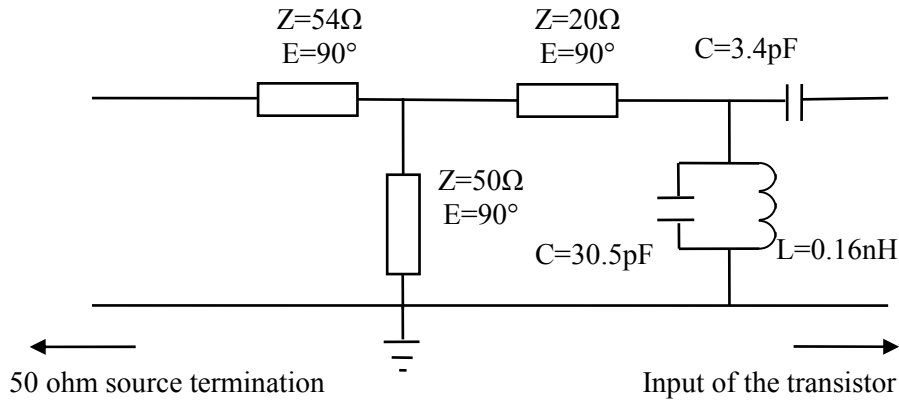


Fig. 4.13. Designed ideal input matching network for 40% bandwidth

#### 4.9 Simulation results of performance of the designed PA (40% BW)

In order to characterize the performance of the power amplifier, the same analyses as in section 4.6 are done. For instance, Fig. 4.14 shows the fundamental impedances of the broadband output matching

network (circles in the middle of Smith chart) in comparison to load-pull based impedances (crosses). Again, second harmonic impedances, circles around the Smith chart, show widespread scattering, which may lead to drop in efficiency at some frequencies.

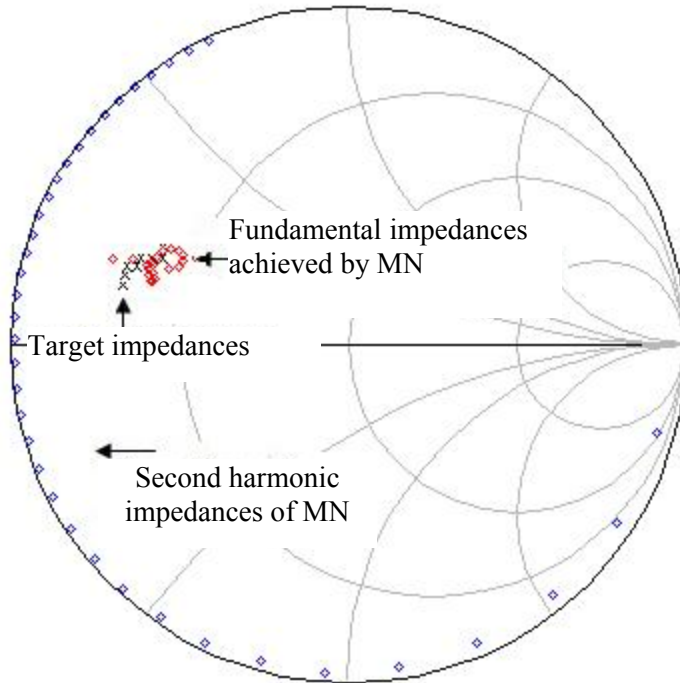


Fig. 4.14. Fundamental and second harmonic impedances over BW before adjustment (40% BW)

Characteristics of the designed power amplifier, in terms of PAE and output power, are illustrated in Fig. 4.15. As predicted, there is a PAE drop off around the frequency of 2.1 GHz. Therefore, second harmonic adjustment is necessary for PAE improvement. The same method of adjustment is used for the design with 40% bandwidth as was done for the design with 20% bandwidth (moving the  $\lambda/4$  bias line along the series transmission line, which is connected to the output of the transistor). This resulted in compressed and shifted second harmonic impedances as shown in Fig. 4.16.

As a result of second harmonic adjustment, the severe drop in efficiency at the middle of the band is eliminated. It is shown in Fig. 4.17. According to simulation results, a PAE of 60%(+/-5%) is achieved over the frequency band of 1.8 to 2.7 GHz. Furthermore, output power varies between 44 and 47 dBm over the entire bandwidth.

Furthermore, use of tapered line instead of conventional transmission line was investigated. Unlike the design with 20% bandwidth, tapered line was not helping much in this case - in other words, performance wasn't improving by using tapered line. Therefore, this design uses conventional transmission line for its bias network.

Finally, layout of the input and output matching networks were sent out for fabrication. Fig. 4.18 shows the layout of the input and output matching networks for the design with 40% bandwidth.

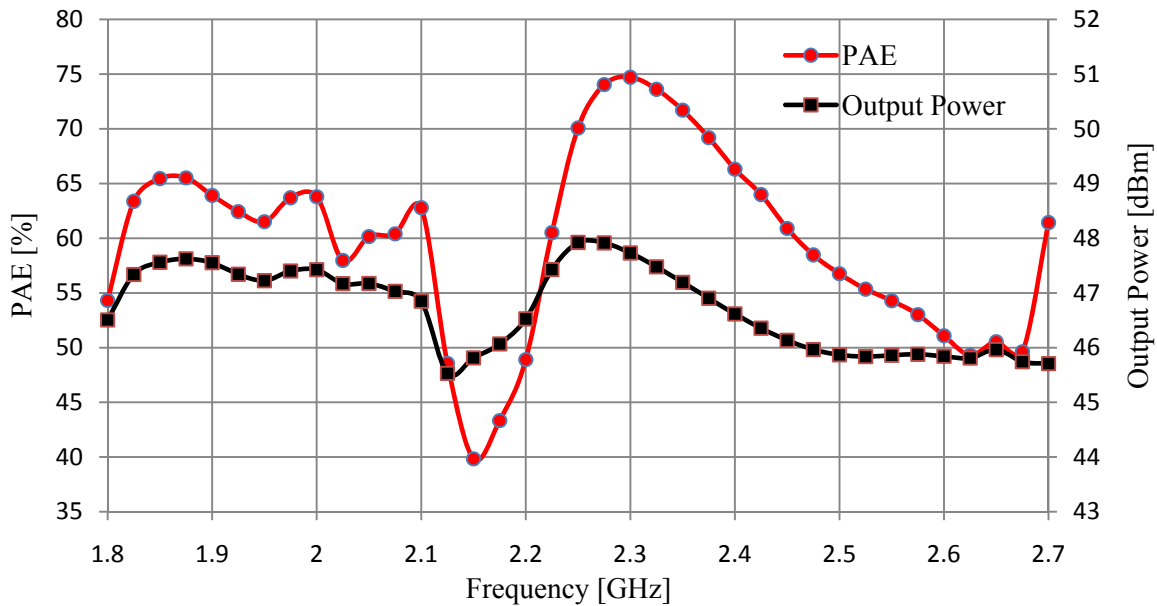


Fig. 4.15. Simulated output power and PAE characteristics of broadband PA before adjustment (40% BW)



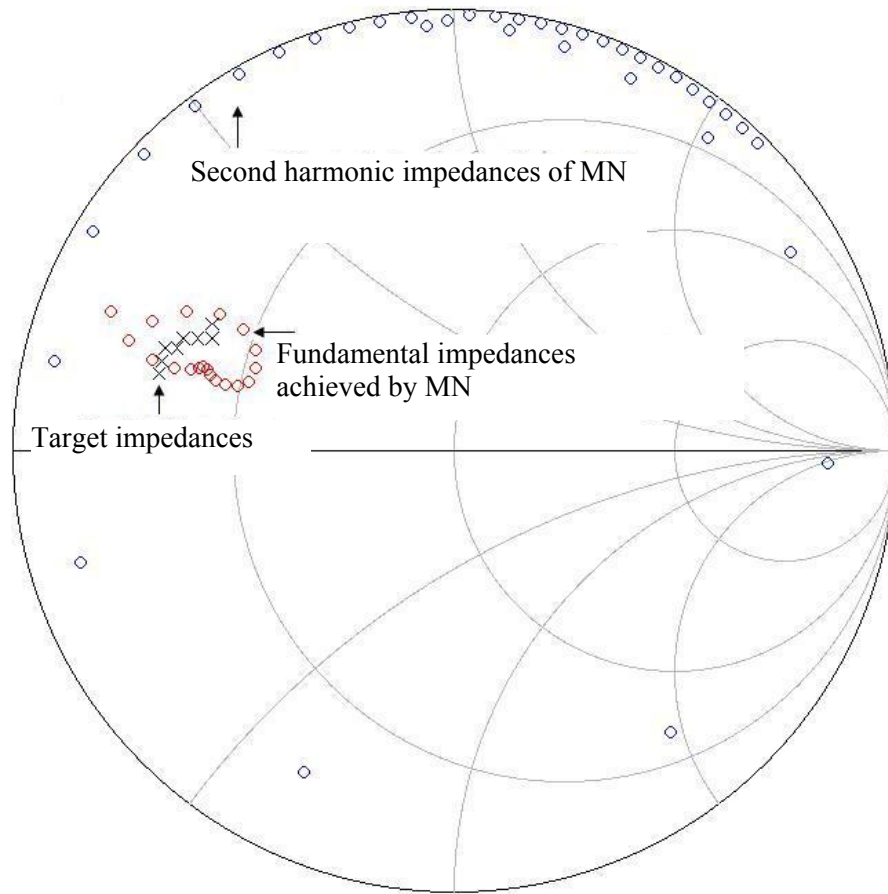


Fig. 4.16. Fundamental and second harmonic impedances over BW after adjustment (40% BW)

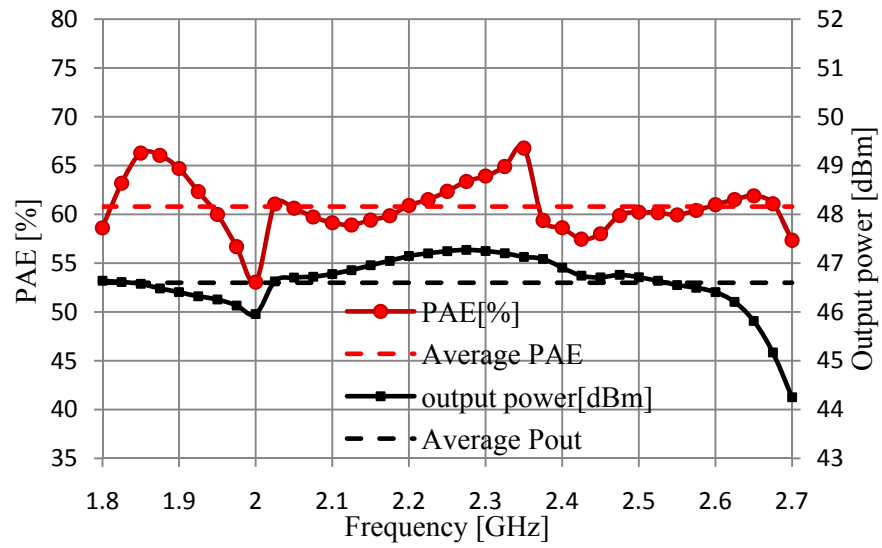


Fig. 4.17. Simulated output power and PAE characteristics of broadband PA after adjustment (40% BW)

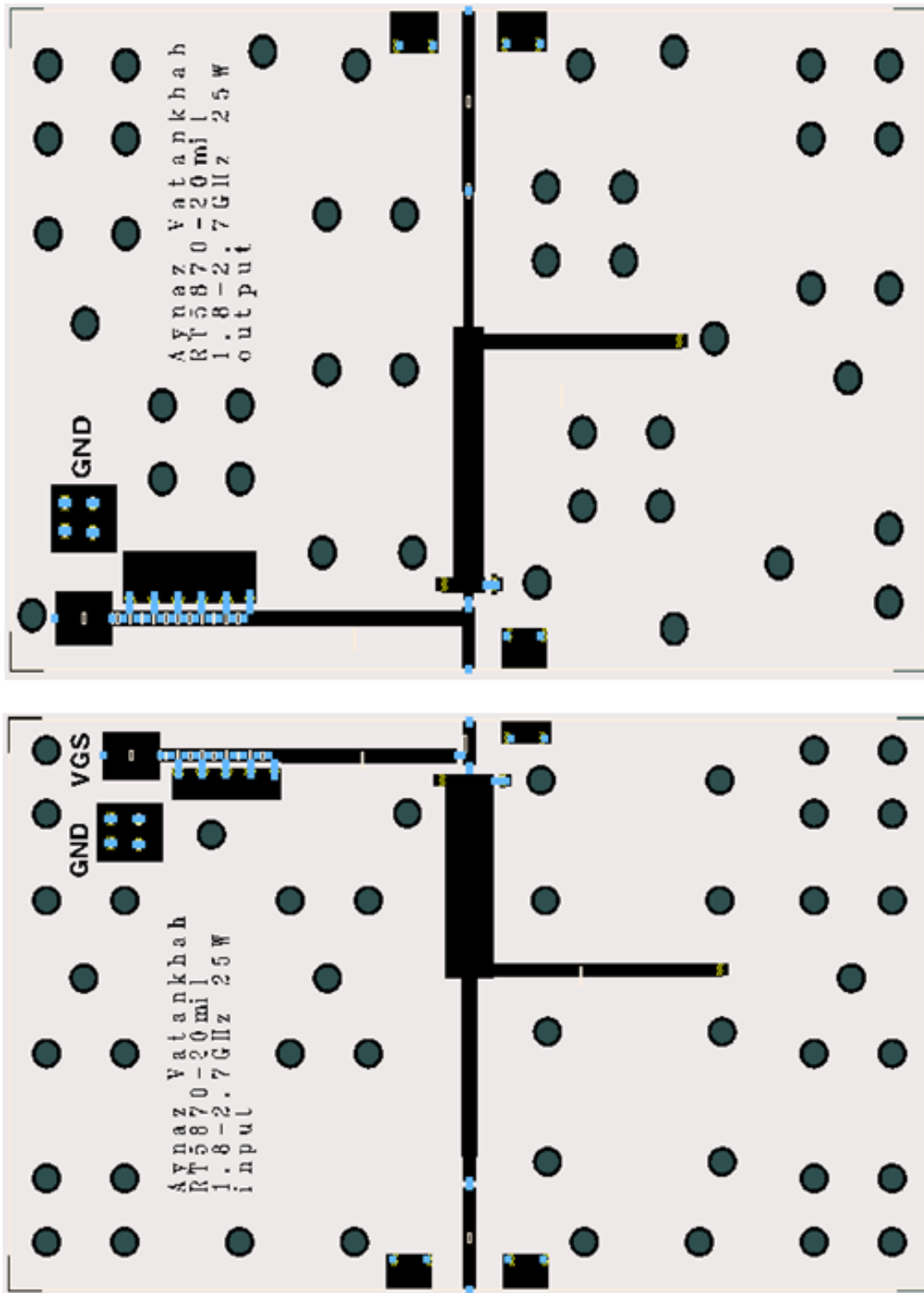


Fig. 4.18. Layout of input (at the bottom) and output (at the top) of the design (40% BW)

## 4.10 Conclusion

In conclusion, for design of a highly efficient class AB broadband power amplifier, the multi L-section method for complex loads is used for design of the input and output matching networks. In order to obtain high efficiency, the matching networks are designed to follow the optimum load and source impedances as closely as possible. In different steps of the design, the ADS simulator is used for analyzing performance of the power amplifiers. Finally, in the last step, momentum simulation is also used in order to predict the behavior as accurately as possible.

Fig. 4.19 and Fig. 4.20 illustrate the comparison of PAE for different steps of the design.

Fig. 4.19 is for the design with 20% bandwidth, which includes the PAE of a narrowband design (for comparison purposes), the PAE of the unadjusted class AB, the PAE of the adjusted class AB with transmission line, and finally the PAE of the design adjusted with tapered line. It is shown that adjustment of second harmonic impedances eliminates the problem of PAE drop at the middle of the band, and adjustment with tapered line gives the best performance. According to the simulation results, a PAE of 65%(+/-)5% and output power of 46(+/-)1.5 dBm is achieved.

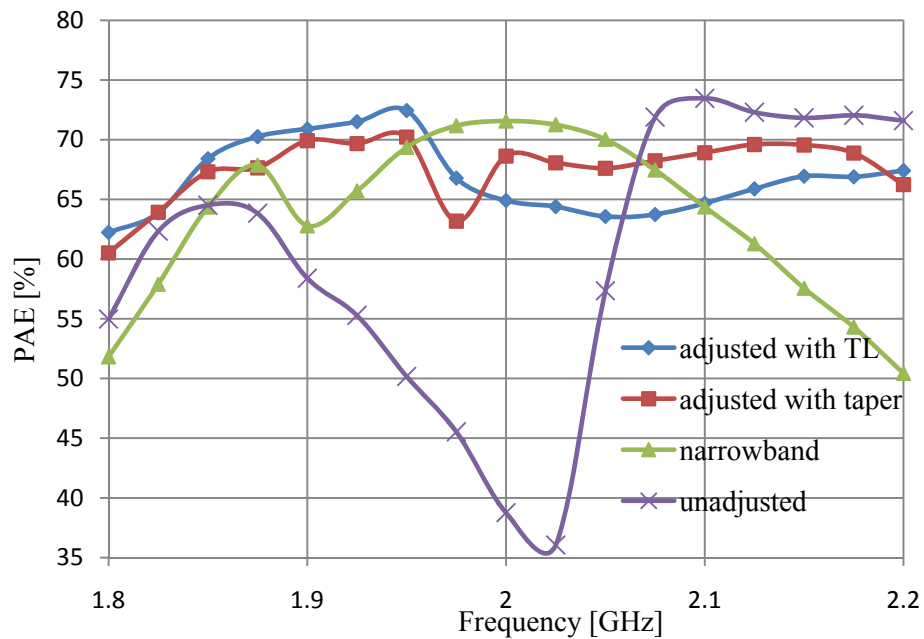


Fig. 4.19. Comparison of PAE for different steps of the design (20% BW)



Fig. 4.20 shows the PAE of different steps of the design for the design with 40% bandwidth. It is illustrated that adjustment of the second harmonic impedances improves the PAE over the bandwidth, but using tapered line instead of conventional transmission line in the bias line is not very advantageous in this case. Therefore, this design uses regular transmission line as its bias line. Simulation results show that a PAE of 60%(+/-)5% and output power of 46.5(+/-)1.5 dBm is obtained.

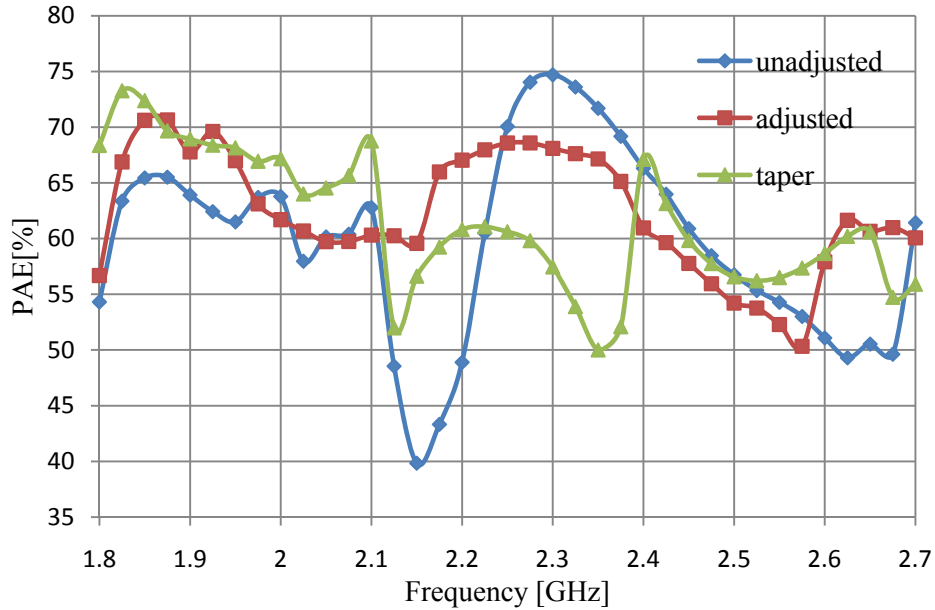


Fig. 4.20. Comparison of PAE for different steps of the design (40% BW)

Now that promising simulation results are obtained, the next step is doing measurement on fabricated power amplifiers. Next chapter includes measurement results.

## Chapter 5

### Measurement results

In order to do measurements on the fabricated power amplifiers, several supplies and measurements devices are required: two DC power supplies for gate and drain bias, one signal generator for providing RF power at different frequencies, a broadband driver, and couplers and attenuators in order to connect the output of the power amplifier to a measurement device such as power meter or spectrum analyzer. Furthermore, a vector network analyzer (VNA) is necessary for S-parameter data measurement.

This chapter includes the results obtained from measurements, and comparison between them and the simulation results achieved in the previous chapter.

#### 5.1 Measurement results for the design with 20% bandwidth

The circuit adjusted with tapered line was modified according to layout considerations and final simulations and tuning were done using momentum co-simulations. Fig. 5.1 contains the measurement results of the fabricated circuit illustrating drain efficiency and output power of 70% $\pm$ 5% and 45.5 dBm  $\pm$ 1.0 dB respectively.

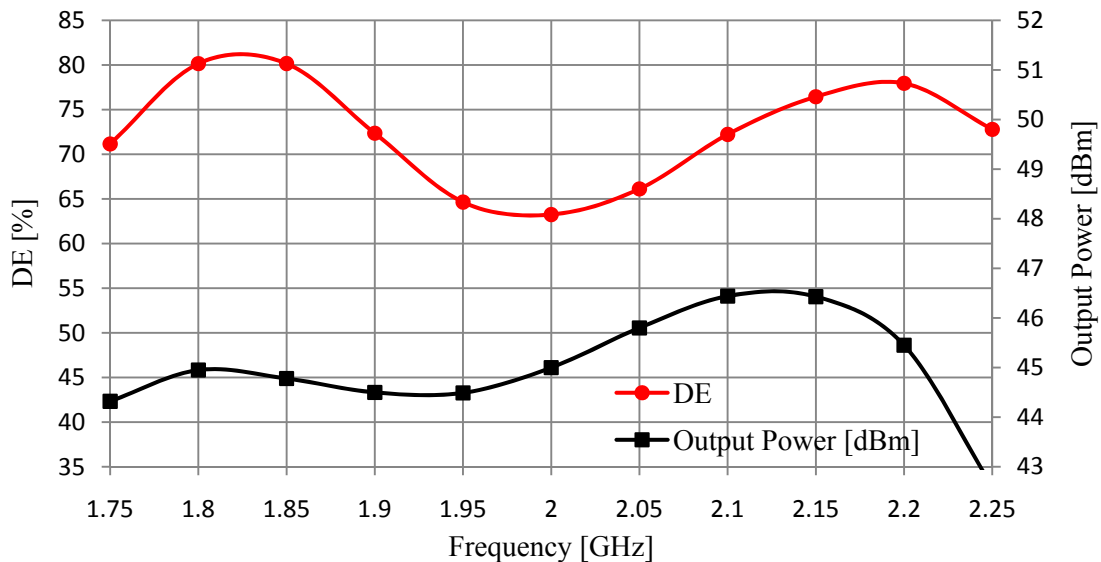


Fig. 5.1. Measured DE and output power (20% BW)

## 5.2 Comparison of measurement and simulation results (20% BW)

Fig. 5.2 and Fig. 5.3 illustrate both measurement and simulation results for comparison purposes. Fig. 5.2 represents the DE and Fig. 5.3 is for the output power. It is shown that measured DE and output power follow almost the same trend as expected from simulation, but the output power is lower at some frequencies resulting in lower DE.

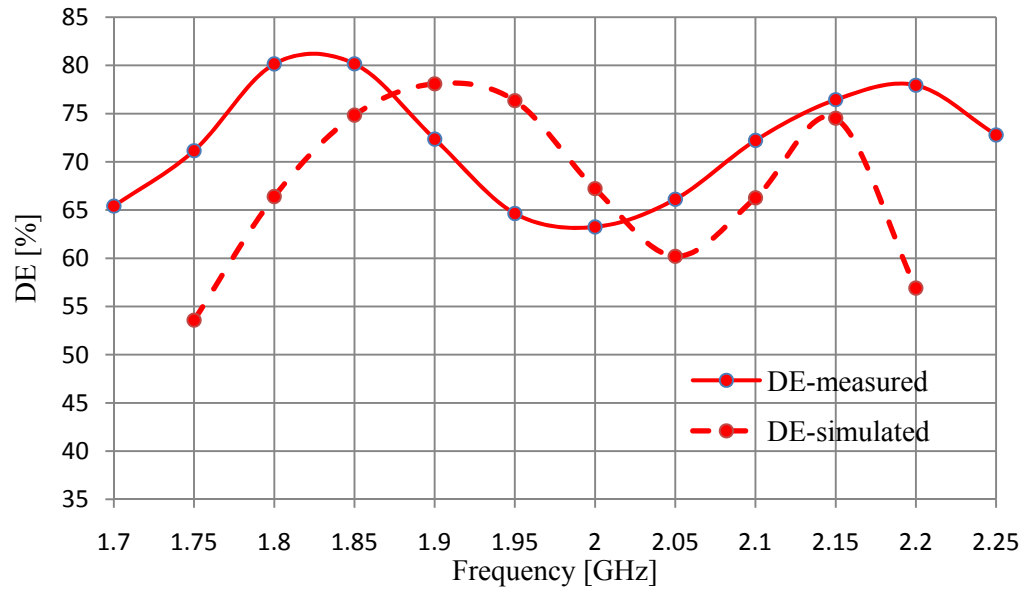


Fig. 5.2. Measured DE (solid) versus simulated (dotted), 20%BW

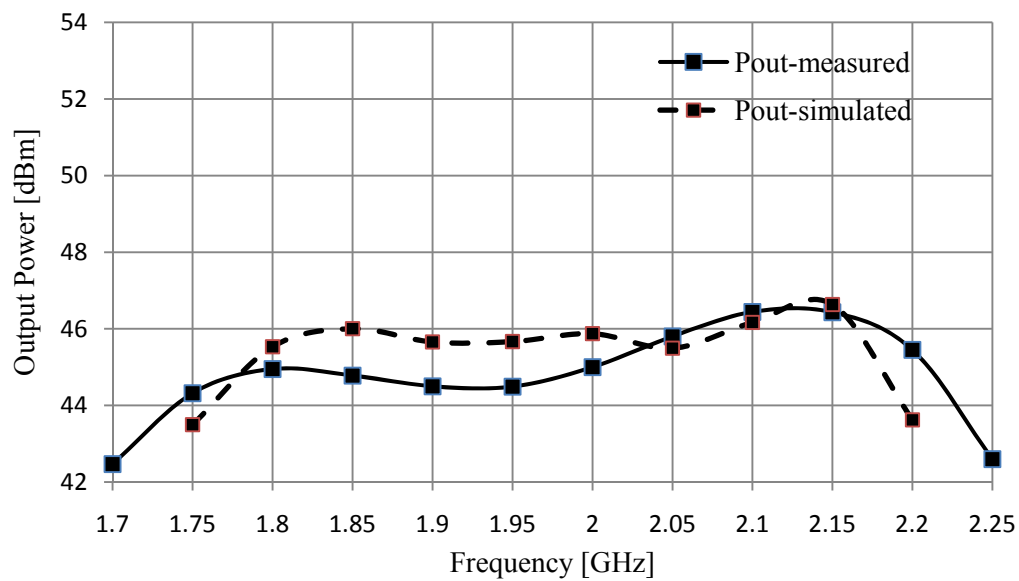


Fig. 5.3. Measured Output power (solid) versus simulated (dotted), 20%BW

The discrepancy between measurement results and simulation results can exist for various reasons. For example, accuracy of modeling of the transistor may affect the simulation results. In other words, if the transistor is not modeled accurately, measurement results will deviate from simulation results. Furthermore, how accurately simulation results agree with measurement results should be investigated. Therefore, we need to see how close the impedances of the fabricated matching networks follow the impedances expected from simulation results (good agreement is expected, since momentum simulation has been used for this design). To check the impedances of the input and output matching network, the design should be fabricated in two different pieces. The initial fabrication was one piece, therefore it was not possible to check the impedances of the input and output matching networks separately. Thus the decision to fabricate the design for 40% BW in separate pieces for input and output was made. By this method, the impedances can be checked before attempting to measure the performance of the power amplifier, and better data on the sources of problems causing drops in efficiency can be studied

Other problems can arise because of non-idealities during the measurement. Measurement setup should present 50 ohm at the fundamental, and shouldn't affect the impedances seen by the transistor. For example, if the correct harmonic impedances are not presented to the circuit, efficiency may change and deviate from simulation results.

Trying to investigate these problems and using the experiences obtained from this step, measurements were continued for the design with 40% BW as well.

### **5.3 Measurement results for the design with 40% bandwidth**

Matching networks were fabricated according to the final layouts. The initial measurements showed that good performance was achieved for the lower half of the bandwidth, but not for the upper half. The problem had to be investigated, to see whether it was a design problem or a problem of modeling the transistor. More details on these investigations and steps of the measurement are provided in next section. Eliminating sources of problems and refabricating the circuit led to better results. Fig. 5.4 shows the final measurement results of the fabricated circuit, illustrating drain efficiency and output power of about 60% and 45.5 dBm +/-0.5 dB respectively. It is seen that both DE and output power are less variant and stay almost constant within the range.

Comparison between simulation results and measurement results is done in the next section.

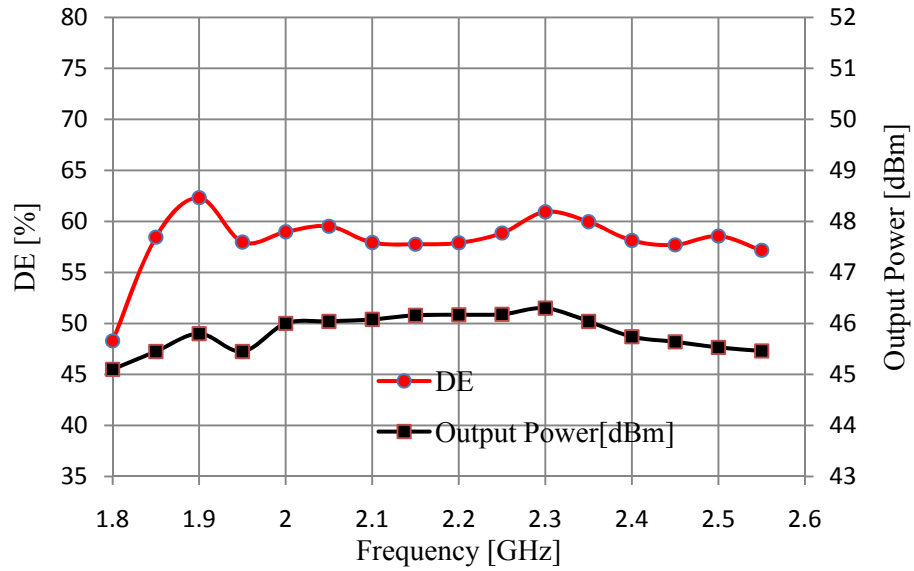


Fig. 5.4. Measured DE and output power (40% BW)

#### 5.4 Comparison of measurement and simulation results (40% BW)

Before measuring PA performance, the input and output impedances of the fabricated matching networks were checked using VNA, to see whether they were in good agreement with simulation results or not. Thus, one of the sources of problems could be eliminated (as discussed in section 5.2). Fig. 5.5 and Fig. 5.6 illustrate the comparison between simulated and measured impedances. Fig. 5.5 contains the results for the input matching network and Fig. 5.6 compares the simulated and measured output impedances. It is shown that they are in good agreement, and that measured impedances follow the simulated impedances very closely with only slight differences. Therefore, the conclusion is that EM simulation results are reliable, meaning that since almost the right impedances have been achieved, almost the same performance for the fabricated power amplifier should be expected.

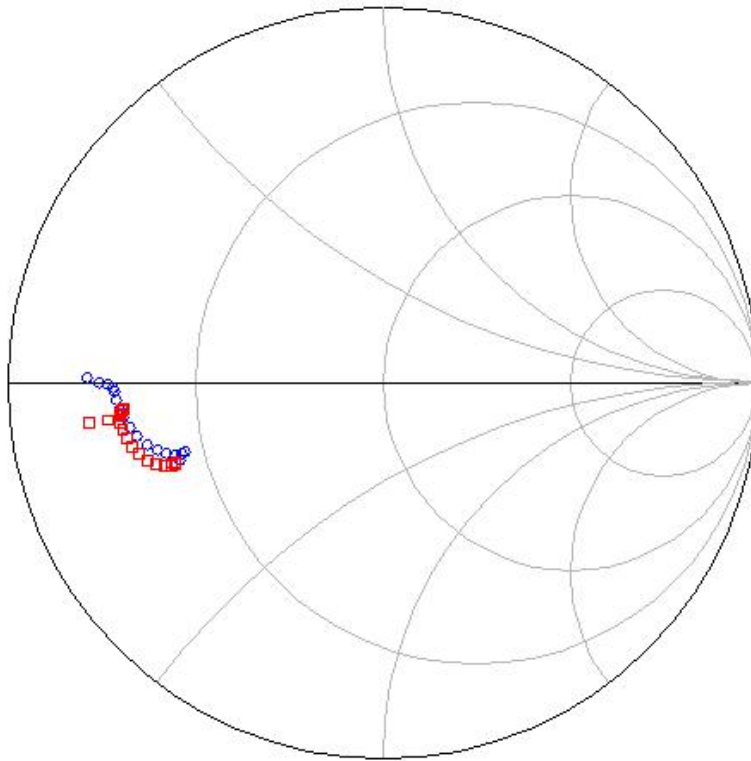


Fig. 5.5. Input impedances, measured (circles) versus simulated (squares)

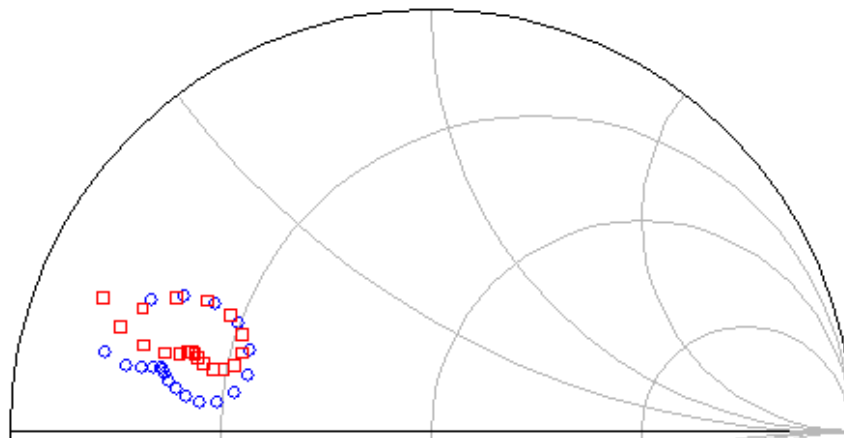


Fig. 5.6. Output impedances, measured (circles) versus simulated (squares)

Knowing the input and output impedances, another test was conducted to confirm that with these impedances good performance should be expected. In this step, the S-parameters of the input and output matching networks (obtained using VNA) were plugged into the ADS simulator, along with the transistor

model. As expected, good performance is achieved. The curve with squares in Fig. 5.8 represents the DE simulated with S2P files of the matching networks.

With results thus confirmed, the next step is measurement of the performance of the fabricated power amplifier. Measured DE and output power is shown in Fig. 5.7. As represented, DE and output power are good for the lower half of the bandwidth, but they start to fall for the upper half of the bandwidth. In other words, performance is poor for half of the bandwidth.

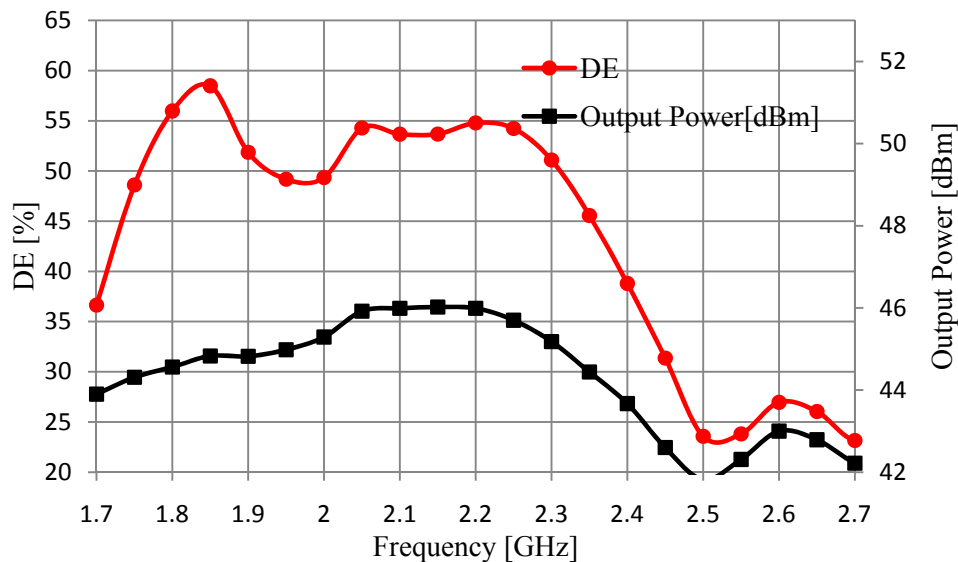


Fig. 5.7. Preliminary measurement results for 40% BW

It was then necessary to investigate possible sources of the problem. Knowing the right impedances and having verification of the simulation results, good results were expected from the measurement. The input and output impedances were checked again to see if everything was still optimal. It was a surprise to discover that the input matching network impedances had changed severely. In other words, the right shape was lost and it was no longer in agreement with the expected impedances.

The new S2P information of the input matching network was plugged into the simulator to confirm whether it was the source of problem or not. With new input impedances, DE starts to drop at the upper half of the bandwidth as shown in Fig. 5.8.

Having all three DE curves in Fig. 5.8, it can be seen that change of the input matching network is the reason for the DE drop, because DE simulated after the input change follows almost the same trend as the measured DE.

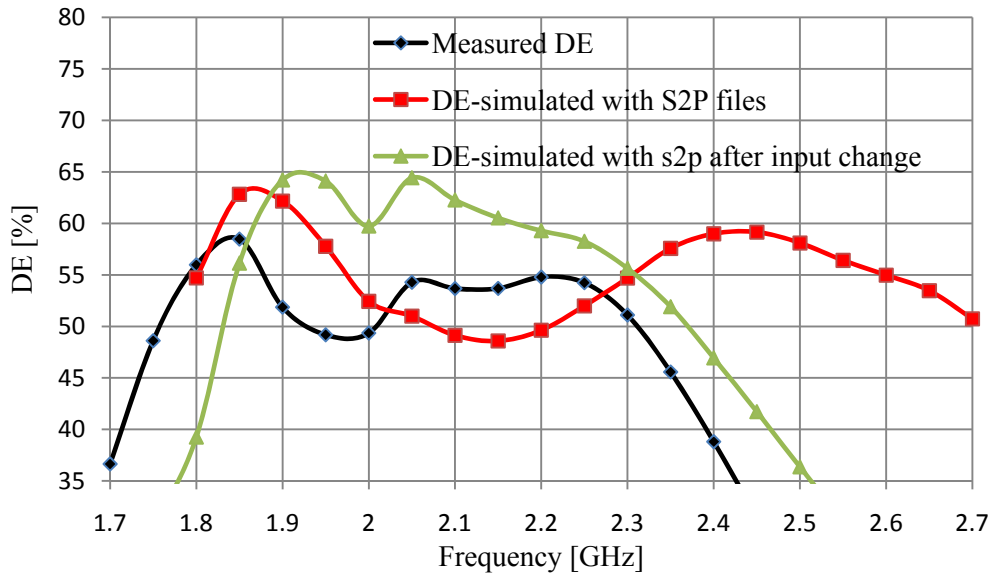


Fig. 5.8. Simulated and measured DE for 40% BW, preliminary tests

Looking for the reasons resulting in the change of impedances, it was found that some of the vias have lost their connection to the ground, and have therefore severely affected the matching network. The design was sent for refabrication, asking for better connection of the vias.

Meanwhile, it was noticed that the coupler being used was for 2-4 GHz, and that this range doesn't cover the harmonics. In other words, correct impedances are not shown to the transistor at harmonics. Therefore, it was replaced with a broadband attenuator, which resulted in more than 1 dB gain at the output power and more than 10% change in DE.

Finally, for the refabricated design, performance of the power amplifier was measured. Comparison of simulated and measured performance, using DE and output power figure of merits, is shown in Fig. 5.9 and Fig. 5.10. It is illustrated that results are in good agreement and there are only small differences between measurement and simulation results, which could be because of different harmonic terminations or model discrepancy of the transistor.



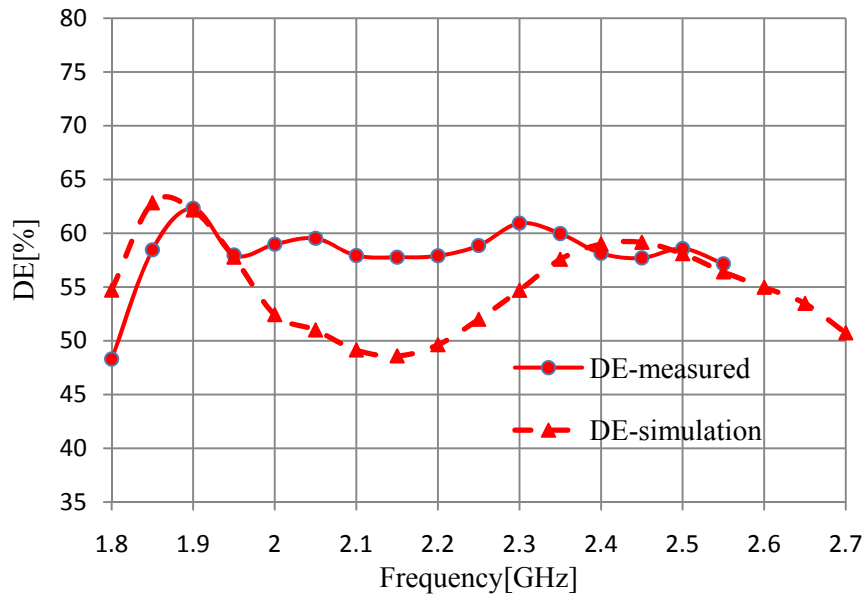


Fig. 5.9. Measured DE (solid) versus simulated (dotted), 40% BW

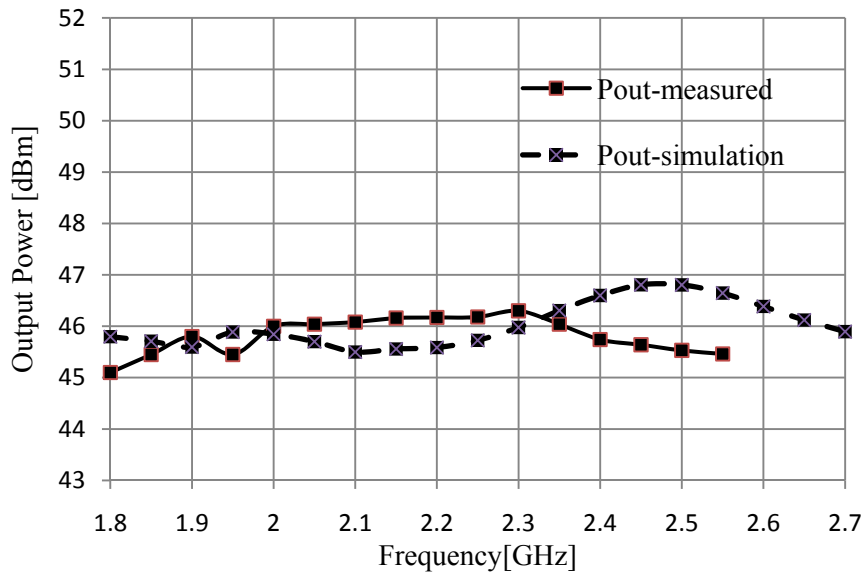


Fig. 5.10. Measured output power (solid) versus simulated (dotted), 40% BW

## Chapter 6

### Conclusion and future work

#### 6.1 Conclusion

Different classes of operation of power amplifiers were investigated. Class AB was chosen to be the best tradeoff for this design because of the following reasons:

- Among classes of operation of the PAs working as current source, the best tradeoff between efficiency and linearity is achieved with using class AB.
- Compared to switching mode power amplifiers, having the simpler configurations in the matching network and more degree of freedom in harmonic tuning make class AB the best option for design of broadband power amplifiers

After picking the class of operation, different matching network topologies and methodologies were studied. Looking for broadband methodologies suitable for power amplifier design, complex-to-real transformations were compared in terms of advantages and disadvantages. The multi L-section method for complex loads was chosen as the method used for this project for its good bandwidth, and its ability to transform the complex impedances to 50 ohm.

Having chosen the class of operation and method of designing matching networks, the model of the CREE GaN HEMT device, CGH40025, was used in ADS simulator in order to determine the optimum load and source impedances and designing the matching networks. Momentum co-simulation was done on the last step. Promising simulation results were achieved.

In conclusion, a systematic approach based on filter theory is used to design the broadband matching networks for power amplifiers. This results in compact matching networks, optimum in terms of size and cost, suitable for multi-standard radios. Two PAs, one for 20% bandwidth and other targeting 40%, were designed and fabricated following this approach. DE of 70% $\pm$ 5% and output power of 45.5 dBm  $\pm$ 1.0 dB was obtained for 20% bandwidth. For the 40% case, DE of about 60% and output power of 45.5 dBm  $\pm$ 0.5 dB was achieved.

#### 6.2 Future work

In this work, reliability of the “multi L-section method for complex loads” was verified for bandwidths up to 40%. It is shown that transmission lines are not limiting elements for bandwidths up to 40% and with

some sacrifice in efficiency, bandwidth may be increased. For example, doubling the bandwidth from 20% to 40% costs about 10% of efficiency. In future, the limits of this method for higher bandwidth should be investigated. In other words, higher bandwidth should be targeted to find out what is the ultimate achievable bandwidth without losing efficiency.

Furthermore, during the measurement, some problems were experienced with the vias on the RF path. Sometimes they were losing their connection with the ground, resulting in severe change of matching networks and deviation of performance. In order to avoid these problems, design of matching networks with open-circuit stubs instead of short-circuit stubs is preferred.

More importantly, deeper analytical investigation of multi L-section transformation for complex loads can lead to better understanding of the advantages and limitations of this method. Specially, use of tapered transmission lines instead of regular microstrip ones should be investigated in order to achieve wider bandwidth due to better wideband performance of non-uniform lines. In this regard, characteristics of tapered lines should be fully analyzed both electrically and magnetically. In addition to analysis, as a systematic approach, filter theories should be developed for circuits using tapered lines for synthesis purposes. In other words, specific equations and tables should be extracted for designs using tapered lines.

In addition to tapered line investigations, new tuning techniques should be developed for matching network tuning. Discrepancy between simulation and measurement always makes the post-fabrication necessary, but it is no longer feasible for broadband structures. Therefore, EM solvers and advanced tuning approaches such as space mapping should be deployed.

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