Investigation of Current Sensing Using Inherent Resistance

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Shahin Solki

Abstract

A novel method of current sensing using resistance of power delivery path is introduced as a mean to measure static or dynamic load current in high-power system-on-chips, where conventional methods deemed inadequate. It is named "IRS" here, and it stands for Inherent Resistance Current Sensing.

To explain its application and to provide motivation beyond this work, pros and cons of conventional techniques are reviewed with a look at previous works done in this area.

It is followed with review of discreet implementation of the sensor (IRS) in chapter three. The measurements results collected using the discrete circuits are included with an in-depth analysis of the results and compensation techniques. It offers insight to effectiveness of the solution and its potential, while highlighting shortcomings and limitation of discrete implementation. This would set the tone to design integrated version of the sensor.

In order to select amplifier architecture, a rundown of common methods to construct the instrumentation amplifier is discussed in chapter 4, primarily based on the latest work already done in this field per cited references. This is to help readers to get an overall view of the challenges and techniques to overcome them.

Finally, the architecture for the integrated version of the sensor (IRS) is presented, with a proof of concept design. The design is targeted for low voltage VLSI systems to allow integration within large SoCs such as GPUs and CPUs. The primary block, the instrumentation amplifier, is constructed using rail-to-rail current conveyers and simulated using TSMC 32nm process node. The simulation results are analyzed and observations are provided.

Acknowledgements

I would like to take this opportunity to thank my supervisor **Dr. Manoj Sachdev** for granting me the chance to participate in this program, and furthermore for his support and guidance thorough out the program until completion.

Here is also a chance to thank **Ming Chen**, who facilitated my participation in this program, and Advanced Micro Devices (**AMD**) that provided the scholarship and a great place to work.

This is a small step forward on the science and technology ladder, and it wouldn't be possible without work of others came before me. I see fit to thank all scientists and authors, who their work and efforts helped me through this investigation, some of which are the references listed in this work.

Special thanks to my wife, **Mojgan,** and my sweet heart **Tina**, who their love and support are my motivation to overcome challenges in life; this is just one of many.

Best Regards,

Shahin Solki

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List of Abbreviations

3D	Three Dimensional
ADC	Analog to Digital Converter
ALU	Arithmetic Logical Unit
ASIC	Application Specific Integrated Circuit
BW	Bandwidth
BOM	Bill Of Material
CM	Common Mode
CMRR	Common Mode Rejection Ratio
CPU	Central Processing Unit
CUT	Circuit Under Test
DAC	Digital to Analog Converter
DM	Differential Mode
GBWP	Gain Bandwidth Product
GPU	Graphics Processor Unit
IA	Instrumentation Amplifier
IC	Integrated Circuits
IR	Voltage drop across a resistive path indicated as IR where "I" is the current multiplied by "R" resistant per ohm's law.
IRS	Inherent Resistance current Sensing
PCB	Printed Circuit Board
PDN	Power Delivery Network
SKU	Stock Keeping Unit
SoC	System on Chip; or SOC
VR	Voltage Regulator

Chapter 1 Introduction

In the modern era of large scale integrated circuits (IC), System-on-Chips (SoCs) are being designed capable of drawing current in excess of 100A at voltage of 1V. The trivial examples of these devices are multi-core Central Processing Units (CPUs) and Graphics Processing Units (GPUs), which are found in personal computers, work stations, servers, laptops and other form of computers.

Once an IC is designed and fabricated, its power consumption depends on:

- Operating parameters such as junction temperature, voltage and frequency.
- Utilization of power containment features such as clock gating, power gating, voltage/frequency islands, and dynamic voltage control.
- Activity factor as how much hardware is utilized and for how long; it mainly depends on the software application used.

In this concept, product requirements such as performance, cost, and form factor along with environmental conditions such as ambient temperature define the bounding conditions for power. An extensive post-design characterization is required to measure and analyze all the above parameters within their practical and feasible range to properly define operating clocks and voltages.

One of the critical parameters to measure is the electrical current itself. Any inaccuracy in the current measurement can impact end product performance, cost or power consumption. As such, an accurate and sophisticated measurement system is required to handle this task.

In this dialogue, post-design characterization, the electrical current is considered as combination of static and dynamic components. It might not be possible to physically separate these two components, yet it allows analyzing them individually.

Static Component
The static component of the load current is defined by silicon leakage when all clocks are turned off and all activities are seized. The leakage is function of:

- Silicon Physics (defined by the technology used)
- Junction Temperature
- Operating Voltage

Dynamic Component
The dynamic component of the load current is function of:

- Operating Frequency
- Operating Voltage
- Activity Factor

In CMOS technology the majority of current consumption is expected to be dynamic component. But, the device leakages are increasing generation over generation, as a result, the proportion of the static load is growing.

The dominant portion of total power consumption and dynamic component in GPUs is application dependent. To a degree that specialized applications are developed to stress GPUs beyond typical conditions that games or 3D application could do.

With this introduction, the question stands what are the methods to measure current and ultimately power consumptions in large size silicon devices?

1.1 Discrete Techniques for Current Sensing

Monitoring power supply current has become an increasingly standard requirement for many circuits and systems, and in particular, for GPUs and CPUs. Conventional techniques for monitoring power supply current rely on board level circuits to provide a signal representing the monitored current. Such a signal is often analog in form or digital , relayed via an interface data bus (like I2C - Inter IC) for the voltage rail, which the current is being monitored (e.g., VCC for bipolar circuits, or VDD voltages for MOS circuits). Such conventional techniques are often problematic. For example, such techniques require special or custom circuit board design or voltage regulator controllers, all of which add to the BOM (Bill Of Material) costs for the overall product and are often impractical for use in a mass production environment. In the following, common methods are discussed.

1.1.1 Voltage Regulator Current Read back

There are commercially available voltage regulators that provide a digital value corresponding to output current. Some may also provide an analog output for on board amplification and conversion to digital signal. As it may sound trivial, the reality is that VR monitors an external signal such as DCR (series resistance) of output stage inductor or R_{DSON} (on-state drain to source resistance) of high-side power MOSFET. Either way, it has practical limitations as follow:

- The external components to voltage regulator are subject to change SKU (Stock Keeping Unit) to SKU. Even functional equivalent component from different vendors can be used on the same SKU, which will require qualification and engineering verification of the solution each and every time a different component is used.

- Manufacturing tolerances (part to part variation) of power inductors can easily reach to 20%. This is too much error to be tolerated in most applications. To put this in perspective, consider that 20% error in a 100A design with a 4-phase regulator means 20A, which is nearly output current of one phase of VR. This could easily change design target to a 3 or 5 phase solution. Tolerance of power MOSFET is less than of inductors (~10%) yet it is still too high given other sources of error.
  Both inductor DCR and MOSFET R_{DSON} have temperature dependency and inherent nonlinearity, which add to the error. Even if it can be calibrated over operating

temperature range it would require temperature sensor of some kind added, which adds to the cost.

- The provided signal has limited effective bandwidth (BW) of less than Kilo-hertz (KHz) in most cases, or few KHz in some cases. This is mainly due to nature of voltage-mode instrumentation amplifier used to eliminate common-mode voltage. This will be reviewed further in this investigation. As such, it is not useful for dynamic load monitoring, where high BW in order of tens of MHz needed.

- Some regulators have integrated power stage. It allows compensating for R_{DSON} variation, to increase the accuracy of current measurement, but they still suffer from low BW, which perhaps can be corrected via architecture proposed in chapter 4. Yet, this type of regulator have premium cost adder that limits their usage to high end products. Aside from cost impact, it still monitors current going through high-side MOSFET as oppose to load behavior. This is a fundamental difference between this method and that of proposed in this thesis.

1.1.2 Series Sense Resistor

Sense Resistor may be placed between output of regulator and the load, in such a case it can provide adequate accuracy for measurement and with right choice of resistor, very low temperature and part-to-part variation can be achieved. Although in high-end CPUs and GPUs, the load current can easily exceed 100A. Even with a $0.1\text{m}\Omega$ resister, there is $>$ 1W power wasted in the resistor. Furthermore, PCBs (printed circuit boards) for such application are designed to minimize power delivery network resistance between source and the load. In a practical case, it is $0.3\sim0.5\text{m}\Omega$, such a series sense resistor yields 20% to 30% negative impact. Therefore, it is counter intuitive to use it. Alternatively, the inherent PCB resistance itself may be used as sense resistor; this indeed is the idea, which will be further reviewed in this thesis.

1.1.3 Hall Sensor

Other technique is to include a HALL sensor on the current path, which yields acceptable error of 5%, but it is challenging to be incorporated into small form factors, and yet has considerable BOM cost increase, and offers limited bandwidth (in KHz range).

Summary
Here is the list of short coming and concerns with conventional discrete current sensing methods:

- Demands special/custom board-level design or voltage regulator controller that adds to the BOM cost and makes it impractical to be used in mass production or in value segment.

- Static current measurement requires calibration, which needs to be done per SKU variant as oppose to ASIC variant. This impacts time to market and increases engineering cost.
- Considerably inaccurate dynamic current measurement due to either inherent amplifier limited gain bandwidth product or monitoring power component's current profile as oppose to actual load current profile.
- Poor accuracy (board to board) even after calibration due to component variation or drift over temperature

1.2 Integrated Techniques for Current Sensing

Built-in current sensors have speed and resolution enhancements over off-chip current sensors, mainly because the large transient currents in the output drivers are bypassed and less parasitic are encountered [2]. In this section, conventional integrated current sensor architectures are reviewed.

1.2.1 High-Side Current Sensing

In this method, the current is typically determined by measuring small voltage drop across a current sense resistor inserted in series within the circuits. The sense-resistor can either be implemented between the negative power supply and the load, which is called Low-Side current-sensing, or between the positive power supply and the load, so called high-side current-sensing. An amplifier is required to measure this voltage drop across the sense resistor [1]. Both methods are implemented in commercially available ICs [1], although the high-side sensing is more popular, as such it is reviewed here.

In a recent work [1], considerable improvements made in the circuit characteristics compared to LTC6102, like reduced offset voltage, reduced power consumption, while increasing CMRR, but there are two fundamental differences between this technique and proposal in this investigation:

- The high-side sensing is effective method for monitoring battery charge, also known as Coulomb counting, which was the purpose of the author as well [1]. But, in most applications, there is some type of voltage regulator between source (battery or otherwise) and the load (GPU or CPU). Therefore, current information extracted by this method doesn't represent load behavior and it depends on voltage regulator design and its performance such as efficiency.

- Despite high CMRR achieved (140dB), it is limited to a relatively narrow frequency range like 10Hz, and as frequency increases the CMRR falls rapidly. At 10 KHz, CMRR is reduced to 110dB (per Figure 1-1). This can also be realized by relatively low Gain Bandwidth Product (GBWP) of the amplifier specified as 1MHz [1]. For dynamic current sensing, high CMRR is required over much wider BW like tens of MHz in order to archive adequate dynamic gain accuracy.

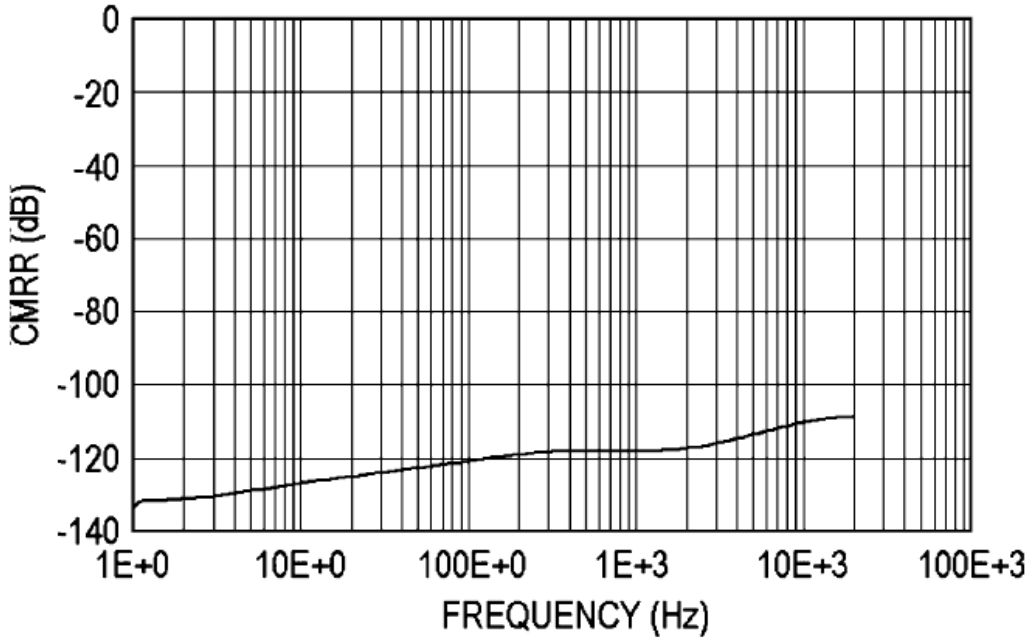

Figure 1-1: CMRR as function of frequency [1]

1.2.2 Iddq Sensing

Iddq current sensing is a known method for local current sensing in the integrated circuits. It can be used to measure quiescent or transient current of the analog or digital circuits. There are both CMOS and Bipolar implementation of *Iddq* sensing. Figure 1-2 is an example of bipolar method [2] intended as a built-in test cell, which is briefly reviewed here.

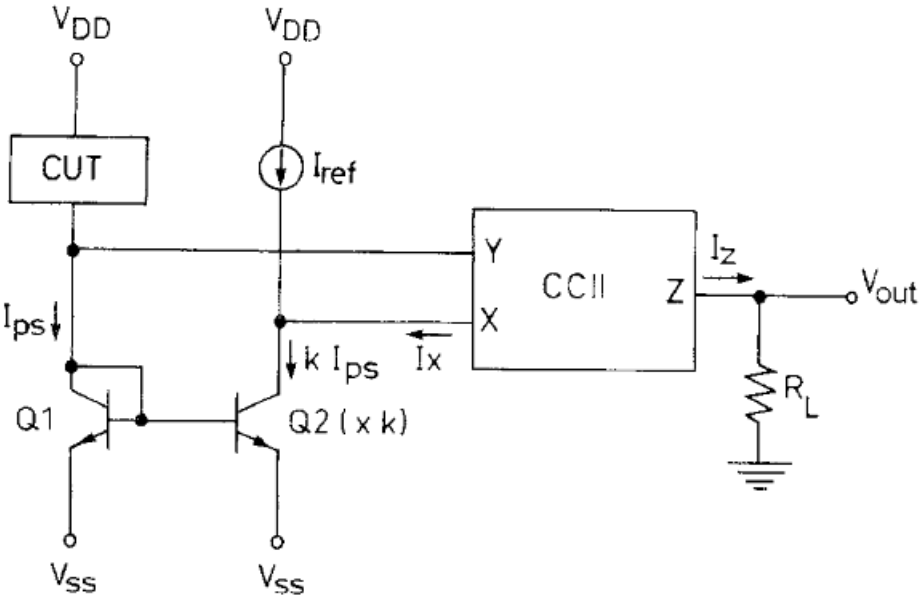

Figure 1-2: Example of Iddq Current Sensing [2]

The proposed circuit, based on a current conveyor second generation (CCII) as signal processing circuit, provides an analogue output proportional to the variation of the $Iddq$ or I_{ps} current of the CUT (Circuit Under Test). The built-in current sensor utilizes a bipolar transistor as a current sink device. The quiescent current I_{ps}, drawn by the detecting transistor, $Q1$, is mirrored and scaled to transistor $Q2$. The current drawn by $Q2$, which is an image of the quiescent current of the CUT, is compared to the reference current to generate the V_{out} [2].

This method is effective, where CUT consumption is low to moderate. For large size silicon devices such as GPUs and CPUs the load current can exceed 100A, where sizing of $Q1$ becomes impractical even during test cycle. The highlight of this implementation is CCII, which is used as amplifier circuit. Advantages offered by CCII are reviewed in chapter 4.

1.3 Criteria for Current Sensor Architecture

Accordingly, it would be desirable to have a technique for monitoring current flow to an IC in a temperature-compensated manner which is not dependent upon individual product designs incorporating the IC to be monitored. Further, or alternatively, it would be desirable to avoid any requirement for adding or using special discrete components, structures or designs within the circuit under test, i.e., to use elements or parameters inherent in the design of the IC being monitored. Further, or alternatively, it would be desirable to have such a technique capable of being integrated into the IC, i.e., the silicon die itself, within which the current is to be monitored. Yet, it must provide adequate bandwidth to allow profiling dynamic behavior of the load.

In this investigation above criteria is used and referred to as the guideline to compare different architectures and solutions to decide about effectiveness and robustness each can offer.

Chapter 2 Inherent Resistance current Sensing (IRS)[1]

2.1 The Concept

In this section, method is provided for monitoring current flow to an integrated circuit (IC), alone or mounted on a substrate, in a temperature-compensated manner. In accordance with a preferred embodiment, a plurality of resistances having substantially equal temperature coefficients establishes a ratio of an output voltage and an internally measured voltage, with the output voltage corresponding to a voltage drop across an inherent resistance within the IC or on the substrate (Figure 2-1).

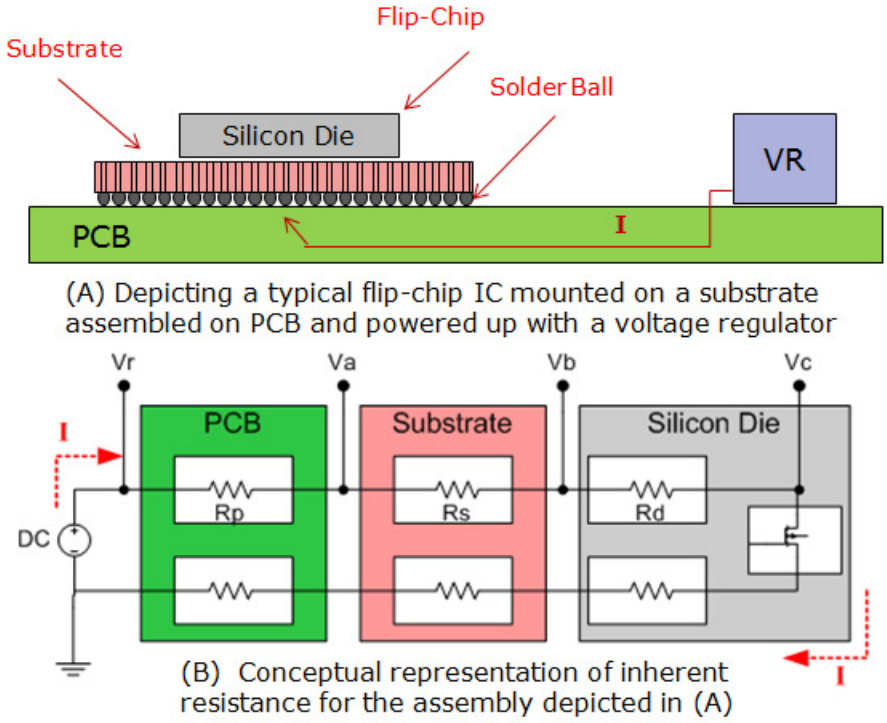

Figure 2-1: Conceptual view of current path

Figure 2-1A depicts a side view of a flip-chip IC mounted on a substrate assembled on PCB and powered up by a voltage regulator (VR). The current '*I*' supplied by VR, flows through PCB power planes, traces and vias to get to substrate. Then it flows through solder balls, substrate's micro-vias to get to the silicon bumps, where it finds its way through metal layers to the silicon devices. Figure 2-1B is a conceptual representation of inherent resistance realized as a lump sum for each individual assembly as follow:

R_p = Equivalent PCB inherent resistance between voltage regulator output and solder balls
R_s = Equivalent substrate inherent resistance between solder balls and silicon bumps
R_d = Equivalent silicon-die inherent resistance between silicon bumps and silicon devices

(2-1)

[1] AMD, Advanced Micro Devices, has filed patent application on this technique (AMD Ref# 090247)

R_p, R_s, and R_d are all function of temperature. Generally, silicon die, substrate and PCB each are fabricated separately and assembled together to build a product. Figure 2-1B also depicts inherent resistance on the return path. It is acknowledged here that such resistance exists and it is an important factor in power delivery network analysis, but it is not evaluated in this investigation. Yet, similar conclusions and methods would apply.

The evaluation of these current delivery paths includes measuring the voltages at the ends of such paths to determine the voltage drop V between them, which is equal to a product of the resistance R of such current path and the current I flowing through such current path per Ohm's law:

$$V = IR \tag{2-2}$$

Referring to Figure 2-1B, this can be better understood by realizing, relative to the circuit reference potential, e.g., circuit ground, a voltage V_a will appear at the substrate electrode, another voltage V_b will appear at the IC electrode and another voltage V_c will appear at the node or electrode connecting the one or more devices. These voltages V_a, V_b, and V_c will be different, albeit slightly, due to voltage drops across the resistances, as such let be:

$$\begin{aligned} V_p &= V_r - V_a = IR_p \\ V_s &= V_a - V_b = IR_s \\ V_d &= V_b - V_c = IR_d \end{aligned} \tag{2-3}$$

Given R_p, R_s, and R_d are minimized by design to reduce power dissipation and improve PDN bandwidth (BW), they are in the order of milliohms or less. Therefore even at high current level like 100A the voltage difference between each pair of electrodes (Figure 2-1B) is in few millivolts or less. Thus, an amplifier circuit, such as instrumentation amplifier (IA), is required with amplification gain of G. Thereby, these voltage differences V_p, V_d, and V_s are amplified to provide GV_p, GV_d and GV_s, which are proportional to the load current I. Then, output voltage of IA can be digitized and calibrated under known load conditions. Now by measuring the output voltage, the equivalent load current can be calculated at any given moment.

Since this method uses inherent resistance of the current carrying material, there is no need for any additional series components, so the circuit performance is not impacted. Yet, the actual current profile can be extracted to provide insight into the circuit behavior, which may not be available otherwise. To achieve this, adequate bandwidth and amplification circuit is required, which is reviewed in chapter 3 and 4. The target is to use substrate or on-die inherent resistances instead of PCB ones, to meet criteria specified in section 1.3. The reason is that once silicon die and substrate designed and verified, R_s and R_d are no longer variable, but several circuit boards usually are designed per application requirement. Therefore, PCB inherent resistance is subject to change (see chapter 3 for further details). Despite simplicity of the idea, there are challenges and details to be considered in order to yield adequate results. One of many is the temperature effect on the material resistance. It is reviewed in details in section 2.2.

2.2 Temperature Dependence of Inherent Resistance

Each equivalent inherent resistance illustrated in Figure 2-1 can be considered as the variable R, which is a function of the geometry and effective temperature coefficient of the materials used to fabricate it. Once the substrate, for given silicon, has been designed, the material and the geometries are no longer variable, with the exception of fabrication tolerances. However, this resistance R will be a function of temperature T, and it can be written as:

$$R(T) = R_0(1 + Coeff\ (T - T_0)) \quad \textbf{(2-4)}$$

Where, R_0 is the resistance at temperature T_0 and $Coeff$ is the equivalent temperature coefficient in percent per degrees Centigrade. For purposes of this investigation, a linear temperature coefficient is presumed.

Example: A typical junction temperature increase of 40℃ (e.g., ranging from 50℃ to 90℃) is expected for a commercially available GPU used in a video card. With copper currently being the dominant conductive material, with temperature coefficient of 0.39% per degree Centigrade the inherent resistance varies by 16% over the specified temperature range. Accordingly, even assuming and ideal IA (with no error) to amplify the voltage difference, the measured current will have up to 16% inaccuracy just due to temperature variation presumed here.

This example shows for IRS to be an effective current measurement technique, need to develop a compensation mechanism for temperature variation. Now, to take into account temperature effect equation 2-2 can be rewritten as:

$$\Delta V\ (t) = I(t)R(T) \quad \textbf{(2-5)}$$

Where, t is time to indicate variation over time is expected, and ΔV can be voltage difference between each pair of electrodes shown in Figuer-1B. ΔV is changing due to both current $I(t)$, and resistance $R(T)$ function of temperature T.

2.2.1 Temperature Compensation Technique

The following methods can be used to compensate for temperature drift:

- Building compensation circuit into the amplifier circuit; referred to as analog compensation in this work.
- Measuring temperature at any given interval that voltage difference is measured to adjust the output voltage numerically afterward; referred to as digital or numerical compensation in this work.

Either method has its own pros and cons. In this section, the analog compensation technique is reviewed. In section 3.2, the digital or numerical method is described.

Since the inherent resistance R is very small (e.g., in the range of milliohm), the change in voltage ΔV is also very small (e.g., in the range of millivolts), thereby it requires amplification of some sort. In order to describe the analog compensation technique a typical instrumentation amplifier, such as in Figure 2-2, with a gain of G is assumed. The characteristics of the amplifier, such as thermal drift, input and output offsets, etc, will affect the overall accuracy of the circuit, although those are circuit design challenges that need to be dealt with regardless of current sensing technique used. Thereby assuming an ideal IA for the evaluation for Figure 2-2, it can be written that:

$$V_{out} = \Delta V G \tag{2-6}$$

Where:

$$G = 1 + R2/R1 + R2/Rg \tag{2-7}$$
$$\Delta V = Vin_+ - Vin\_$$

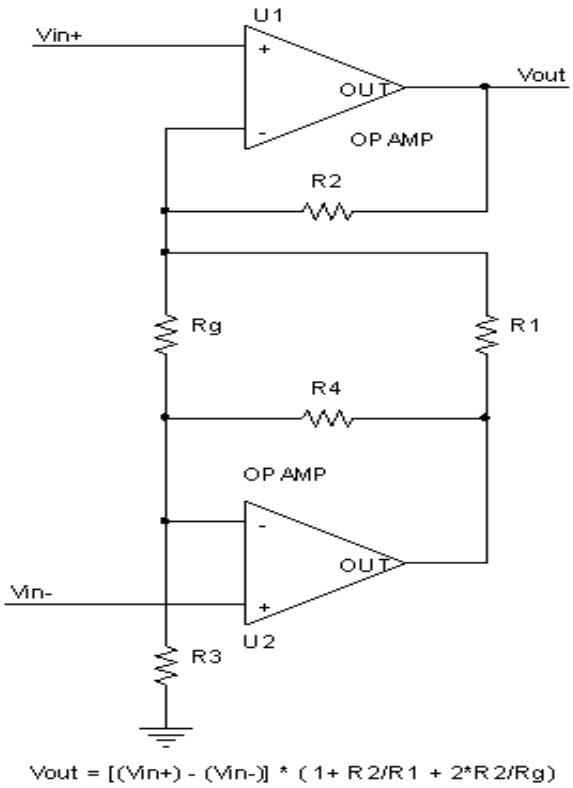

Figure 2-2: Typical Voltage-Mode Instrumentation Amplifier

For IRS, as discussed in section 2.1, the amplifier can be designed to have its gain function of temperature in a way to cancel out variation of ΔV due to temperature. To realize this, the resistances, $R1, R2, R3,$ and $R4$, are established with absolute and mutually relative values as follows:

$$R1 = R2$$
$$R3 = R4 \tag{2-8}$$

By plugging equations (2-8) into (2-7), it yields:

$$G = 2\,(1 + R1/Rg) \quad \textbf{(2-9)}$$

By keeping $G >> 1$, it can be simplified to:

$$G = 2R1/Rg \qquad G >> 1 \quad \textbf{(2-10)}$$

Now by choosing proper type of resistors for $R1$ and R_g, this circuit can be thermally compensated. $R1$ (so as $R2$ to $R4$) must have a negligible change of resistance within target operating temperature range, while Rg must have same temperature coefficient as the inherent resistance material. The nominal value of Rg_0 is selected to provide adequate gain at nominal temperature T_0. It can be expressed as follow:

$$Rg(T) = Rg_0\big(1 + Coeff\,(T - T_0)\big) \quad \textbf{(2-11)}$$

By plugging equations (2-10) into (2-6), the amplified output voltage V_{out} can be expressed as function of temperature as follow:

$$V_{out}(t) = \Delta V(t,T)\,G(T) = \frac{2R1}{Rg(T)}\,I(t)\,R(T) \quad \textbf{(2-12)}$$

Substituting the temperature dependency relationships for the resistances, equations (2-11) and (2-4), the relationship between the inherent resistance $R(T)$, see equation (2-2), and gain resistance $Rg(T)$ can be expressed as follows:

$$\frac{R(T)}{Rg(T)} = \frac{\big[R_0\big(1 + Coeff\,(T - T_0)\big)\big]}{\big[Rg_0\big(1 + Coeff\,(T - T_0)\big)\big]} = \frac{R_0}{Rg_0} \quad \textbf{(2-13)}$$

Substituting this result into equation (2-12) yields:

$$V_{out}(t) = \Delta V(t,T)\,G(T) = 2R1\frac{R_0}{Rg_0}\,I(t) = Kr\,I(t) \quad \textbf{(2-14)}$$

As it can be seen from (2-14) expression, the amplified voltage difference is independent from temperature variations, where Kr is the overall gain of the system.

2.2.2 Using Thermal Chip Sensors as Gain Resistor

In section 2.2.1, it was specified that for adequate analog compensation the gain resistor in the amplifier circuit must have same temperature coefficient as the inherent resistance material. In this section an example is provided to prove practicality of such requirement. Given common material used in PCB and substrate fabrication is copper, the gain resistor temperature coefficient must be same as of copper.

KOA manufactures thin film resistors, LP73 family, with various coefficients so called thermal chip sensors. To compensate for the resistance across copper path, part with the closet coefficient, 0.4%/°C, is selected. The typical gain needed at nominal temperature

defines the nominal value (Rg_0). In this evaluation, gain resistor values of 510Ω and 1KΩ are chosen, which will be used in chapter 3 to review discrete implementation of the circuit (for locations $R4222$ and $R4211$ in Figure 3-1 accordingly). Equation (2-15) is provided in the manufacturer's datasheet to calculate the resistance.

$$R(T) = R_{25}(C_0 + C_1T + C_2T^2) \quad \textbf{(2-15)}$$

Where, T is the ambient temperature in degree Centigrade, $R(T)$ is the resistance value at given T, and R_{25} resistance value at 25°C. For T.C.R 4000ppm (0.4%/°C) parts, the constants are:

$$\begin{aligned} C_0 &= 0.907050 \\ C_1 &= 0.00361010 \\ C_2 &= 4.33462\ x10e-6 \end{aligned} \quad \textbf{(2-16)}$$

Table 2-1 and Table 2-2 provide calculated and measured values for each resistor (510Ω and 1K) at various temperatures. The difference between measured and calculated values is better than ±2%. Given uncertainty in the measurement, temperature stability of the environment, and uncontrolled humidity while performing the test, the yielded results deemed acceptable.

Temperature (°C)	510Ω (Ordinary)	Rg = 510Ω (PTC)		
	MEASURED (Ω)	CALCULATED (Ω)	MEASURED (Ω)	Difference (%)
24.5	508	509.03	518	1.76%
35.0	508	529.74	535	0.99%
45.0	508	549.92	553	0.56%
55.0	508	570.55	572	0.25%
65.0	508	591.61	591	-0.10%
75.0	508	613.12	606	-1.16%

Table 2-1: Characterization result for thermal chip resistor (510Ω)

Temperature (°C)	1KΩ (Ordinary)	Rg = 1KΩ (PTC)		
	MEASURED (Ω)	CALCULATED (Ω)	MEASURED (Ω)	Difference (%)
24.5	998	998.10	1010	1.19%
35.0	998	1038.71	1046	0.70%
45.0	997	1078.28	1083	0.44%
55.0	998	1118.72	1123	0.38%
65.0	997	1160.02	1157	-0.26%
75.0	998	1202.19	1196	-0.51%

Table 2-2: Characterization results for thermal chip resistor (1KΩ)

Both tables also contain measurements for an ordinary resistor at same nominal value, where expected to have a negligible variation over the same temperature range.

Figure 2-3 and Figure 2-4 are plots of the values specified in the Table 2-1 and Table 2-2.

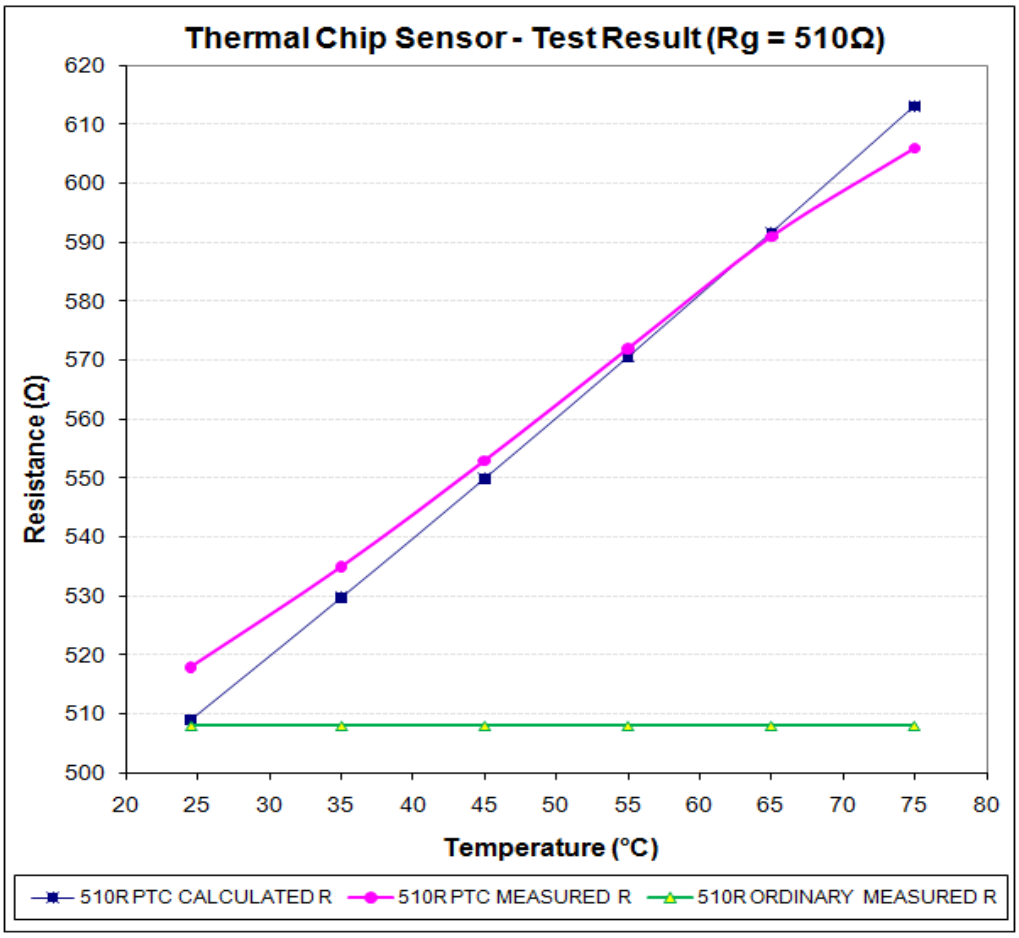

Figure 2-3: Characterization result for thermal chip resistor (510Ω)

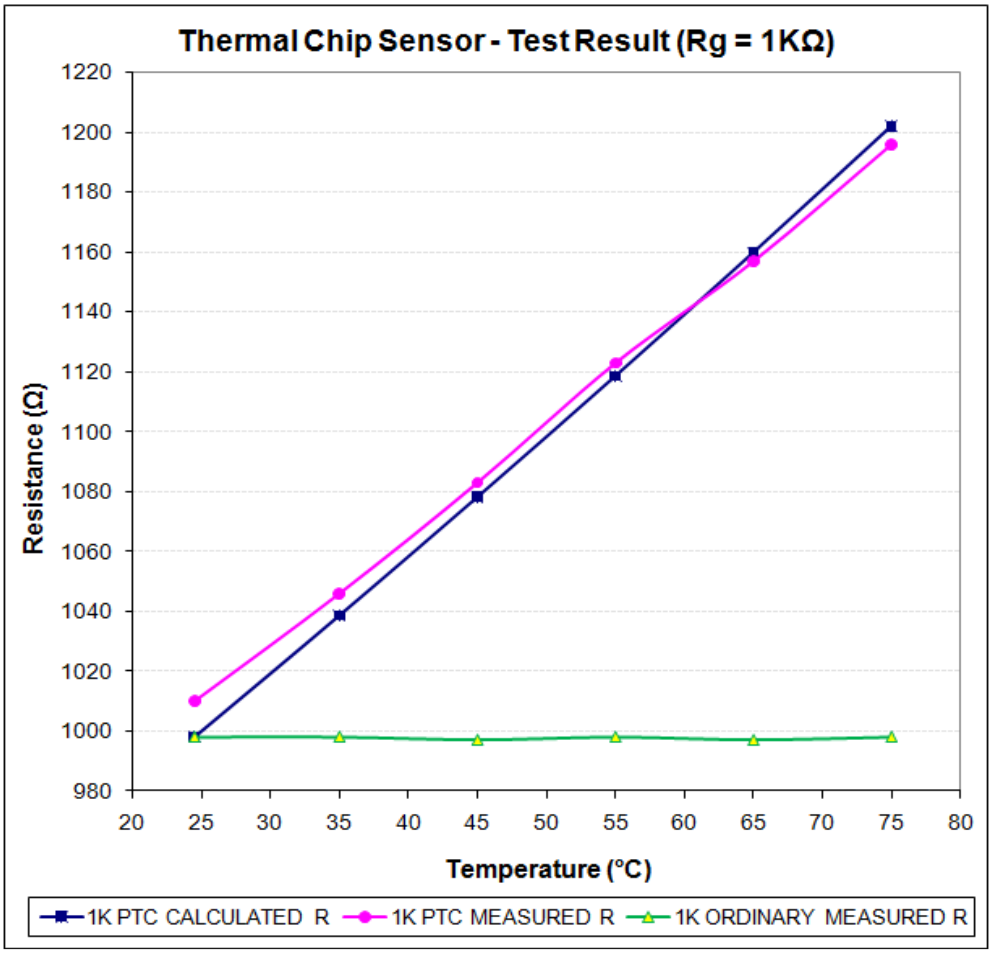

Figure 2-4: Characterization result for thermal chip resistor (1K)

2.3 Conclusions

The concept of current sensing using inherent resistance was described. The temperature dependence of the inherent resistance was indicated as a critical parameter impacting accuracy of this technique. Analog compensation technique was introduced and mathematically proved being effective to compensate for temperature drift within an amplifier circuit (as gain resistor). A practical example of resistor that can provide desired behavior for compensation was given. Further in this work, this technique, inherent resistance current sensing, is referred to as *IRS*.

Chapter 3 Discrete Implementation of IRS

In this chapter, discrete implementation of IRS is reviewed, followed by analysis of the characterization results. The importance of discrete case study is to provide insight to effectiveness of the solution and reveals the challenges to overcome. All at much lower development and fabrication cost compared to an integrated implementation. Despite that, there are systematic limitations in the discrete implementation that will be highlighted at the end of this chapter, which are the motivation to design integrated version of IRS.

3.1 Circuit Schematic

Figure 3-1 is the schematic of IRS discrete implementation. Two instrumentation amplifiers are constructed each using two commercially available operation amplifiers. One IA, labeled as $Config1$, to amplify the voltage drop across PCB, difference between output of voltage regulator and BGA solder balls at PCB. The other IA, labeled as $Config2$, is to amplify the voltage drop across substrate, between BGA solder balls and top of the substrate (accessible via another BGA ball labeled as FB_VDDC). The outputs of the IAs could be monitored via oscilloscope, precision digital multi-meter, on-board 12-bit ADC, or built-in 10-bit ADC as needed. The circuit was tested on two graphics card designs one with a high end GPU capable of consuming typical current of 120A and one mid-range GPU consuming typical current of 80A on core logic (labeled as $VDDC$).

The opamp specs such as noise, input offset and offset drift are crucial to achieve adequate accuracy. In this implementation, MAX4239A was selected primary due to having very low input offset voltage (typical $0.1\mu V$, Max $2\mu V$), low offset drift (typical $50nV/1000hr$) and low input noise ($30nV/\sqrt{Hz}$ @ 1KHz). It also provides adequate GBWP (6.5MHz) and CMRR (Min 120dB, typical 140dB) as good starting point. But it requires minimum closed loop gain of 10 for stability, which can be met.

All resistors R_1 through R_4 are shown as 10K, although in order to maximize the gain they were increased to 14.7K for $Config1$ and to 78.7K for $Config2$. The mismatch between $R_1 \sim R_4$ will add to circuit gain inaccuracy and decreases CMRR. Thus, 0.1% tolerance resistors were used for $R1$ through $R4$ in both IAs. With these settings, two gain resistors R_g (locations $R4211$ and $R4222$) define each amplifier gain and they must also provide thermal compensation as described in section 2.2.1. Hence, thermal chip sensors introduced in section 2.2.2 with same values of 510Ω and 1K used for locations $R4222$ and $R4211$ accordingly. The amplification gain was calculated, using equation (2-7), to be about 31 for $Config1$ and about 310 for $Config2$ at 25℃.

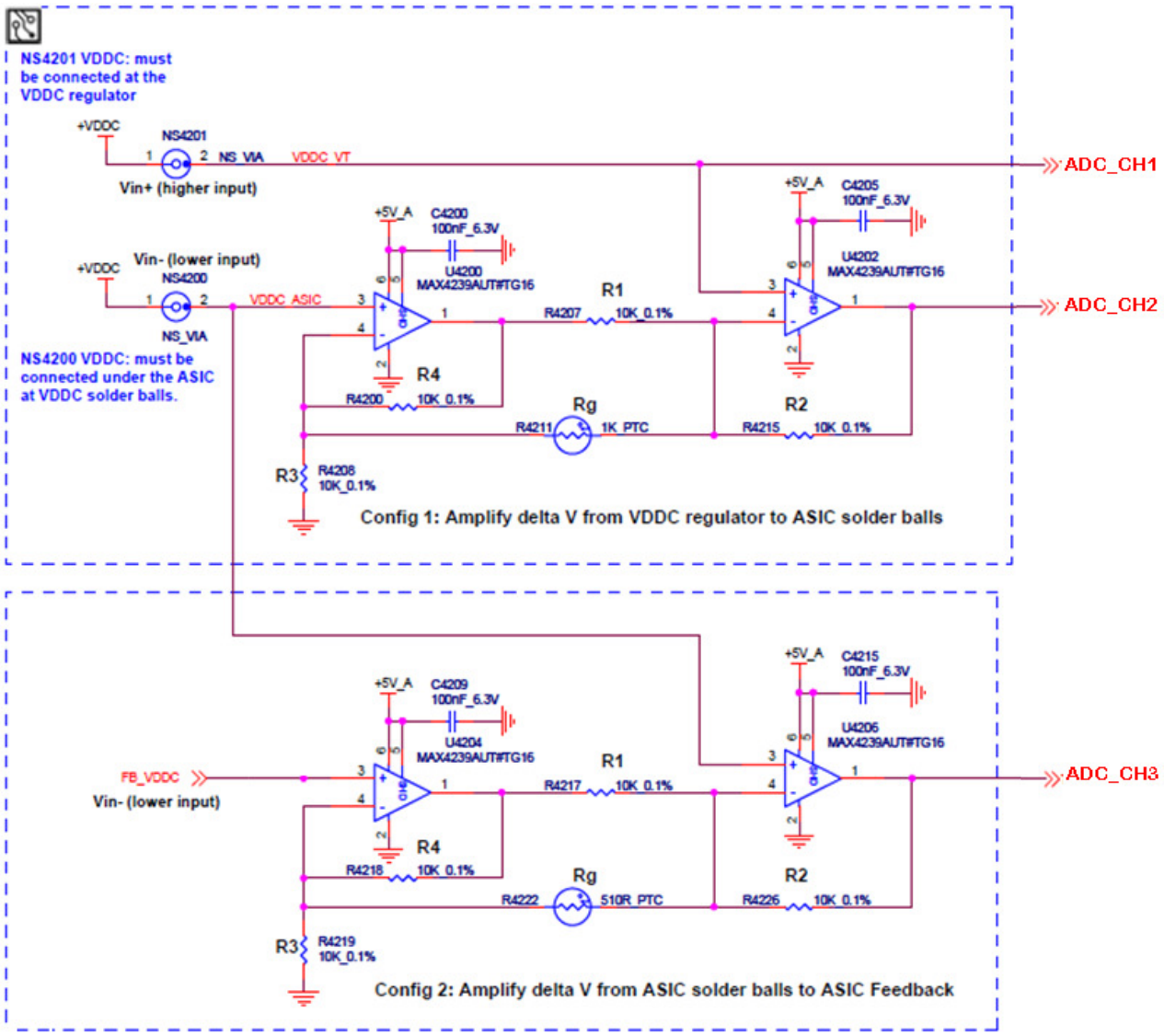

Figure 3-1: Discrete Implementation of the instrumentation amplifier

Per Figure 2-1B, voltage level must be sampled at V_r, V_a, and V_b nodes for current sensing purpose. Based on that and Figure 3-1, the following equations show the mapping of V_r, V_a and V_b to circuit opamp inputs and provide relation between inputs and outputs of IAs:

Voltage at the regulator:

$$ADC\_CH1 \ = \ V_r$$

Voltage drop across PCB power planes:

$$ADC\_CH2 = G_{PCB}\, I\, R_p \ = \ G_{PCB}(V_r - V_a) \quad where\ G_{PCB} \ \cong 31 \qquad (3\text{-}1)$$

Voltage drop across substrate:

$$ADC\_CH3 \ = G_{sub}\, I\, R_s \ = \ G_{sub}\,(V_a - V_b) \ where\ G_{sub} \ \cong 310 \qquad (3\text{-}2)$$

3.2 Characterization Results and Analysis

In this section, characterization results are presented. The analysis of the data gives insight into the circuit performance and load behaviors. Table 3-1 lists inputs, outputs, ASIC junction and PCB temperature at multiple points. It also contains comparison between current measured and reported numbers by the voltage regulator. The GPU under test has four on-die temperature sensors (TS_0 to TS_4) and one external temperature sensor (on-board), which measures the GPU temperature via remote sensing of on-die thermal diode.

The bolded row in Table 3-1 corresponds to midpoint temperature $\sim$73.1°C reported by on-die temperature sensor number zero (TS_0). This row is used as the reference for compensation over temperature in Table 3-2 and Table 3-3. The highlighted numbers, in the red, in Table 3-1 show excess of inaccuracy in the regulator current read back at light loads. This is a known issue with regulator current readout.

Table 3-2 provides first order linearity error in percentage compared to the reference row (midpoint temperature in bold). This hand-calculated indicator can be used to compare effectiveness of a solution without having sophisticated tools for curve fitting. Note must be taken that it is not representing the current readout accuracy; although the better this number gets the better accuracy can be achieved via post numerical calibration. The first column of Table 3-2 represents the actual measured values of PCB IR drop as shown in Table 3-1. The following two columns are calculated effective resistance and linearity error. These sets of data are benefitting from gain adjustment provided by R_g (1K) over temperature range. It shows an overall linearity better than $\pm 6\%$. By calculating R_g (1K) using equation (2-15) and (2-16), the expected output voltage using equation (2-15) and circuit settings the next five columns of Table 3-2 are equated. The calculated error is about $\pm 6\%$ inline with the measurement.

The R_g ($R4211$ in Figure 3-1) is installed on the surface of the PCB and it can monitor temperature of one spot only. However, such arbitrary spot is not necessarily the optimal point (see section 0). To evaluate this matter, PCB temperature was measured at different spots like closer to power plane, where current was flowing through. The results are reported under Plane-1 and Plane-2 columns in Table 3-1. The last five columns of Table 3-2 are calculated in the similar manner described above but instead of using R_g temperature, this time temperature reported under Plane-1 column was used. Comparing the maximum linearity errors, highlighted numbers in **green** and in **red**, it clearly shows a considerable improvement.

VDDC (GPU Core Voltage)				PCB Temperature Measured @				ASIC Junction Temperature Measured By					PCB IR Drop			Substrate IR Drop
Measured @ VR Feedback Point (V)	Measured Current (A)	Current Reported By VR (A)	Current Error (%)	Power (W)	VDDC Plane-1 (°C)	VDDC Plane-2 (°C)	Rg (510R) (°C)	Rg (1K) (°C)	TS0 Average (°C)	TS1 Average (°C)	TS2 Average (°C)	TS3 Average (°C)	EXT TS Average (°C)	Measured Voltage Delta [VDDC_VT - VDDC_ASIC] (mV)	Measured Amplifier Output Voltage (mV)	Calculated Gain (V/V)	Measured Amplifier Output Voltage (mV)
0.9972	9.647	6.132	36.43%	9.620	43.6	43.6	39	41	49.04	50.98	44.09	45.8	53.25	3.27	101	30.89	35.8
1.0473	11.325	9.197	18.79%	11.861	44.9	44.9	40	42	50.85	52.91	45.77	47.78	55.13	3.762	115	30.49	39.8
1.097	13.220	9.197	30.43%	14.502	46.0	46.3	41	43	52.93	54.5	47.43	49.52	57.15	4.34	131	30.18	44.6
1.1603	16.195	15.329	5.35%	18.791	47.8	48.1	42	44	56.43	57.95	50.6	52.99	60.4	5.27	158	29.98	53.5
1.1603	17.176	15.329	10.75%	19.929	48.2	48.6	42	45	56.84	58.42	50.99	53.45	60.89	5.556	166	29.88	55.9
1.1603	18.236	15.329	15.94%	21.160	49.1	49.5	43	45	57.8	59.33	51.95	54.51	61.88	5.86	175	29.86	57.9
1.1603	19.160	15.329	20.00%	22.231	49.3	49.4	43	45	58.5	60.16	52.83	55.23	62.57	6.164	182	29.53	60.6
1.1603	20.091	18.395	8.44%	23.312	49.6	50.1	43	45	59.02	60.72	53.5	55.93	63.14	6.448	190	29.47	63.1
0.9974	22.239	21.461	3.50%	22.182	49.2	49.5	43	45	57.51	59.55	52.36	54.11	61.44	7.048	207	29.37	57.2
0.9973	21.099	21.461	-1.72%	21.042	48.6	49.1	43	45	57	59	51.7	53.6	60.98	6.685	197	29.47	55.8
1.0473	23.785	21.461	9.77%	24.910	50.0	50.5	43	46	59.32	61.59	54.25	56.26	63.33	7.516	220	29.27	61.9
1.097	27.086	27.592	-1.87%	29.714	51.8	52.5	44	47	62.32	64.8	57.2	59.5	66.4	8.593	249	28.98	69.8
1.1604	32.042	30.73	4.09%	37.181	54.7	55.2	45	49	66.7	69.72	61.9	64.13	70.8	10.17	292	28.71	81.6
1.1604	36.320	33.812	6.91%	42.146	56.7	57.8	47	50	69.7	73.35	65.47	67.2	73.8	11.555	331	28.65	89.1
1.1604	**40.677**	**39.862**	**2.00%**	**47.202**	**58.5**	**59.5**	**47**	**51**	**73.1**	**77.07**	**69.01**	**70.62**	**77.19**	**12.99**	**370**	**28.48**	**98.5**
1.1603	44.973	45.987	-2.25%	52.182	61.1	62.0	49	53	76.25	80.6	72.54	73.99	80.23	14.445	408	28.25	107
1.1603	49.415	49.89	-0.96%	57.336	64.0	64.6	51	55	79.6	84.3	75.9	77.1	83.3	15.97	449	28.12	117
1.1603	64.943	64.88	0.10%	75.353	61.6	59.0	46	49	75.6	79.28	71.66	69.61	79.15	20.42	584	28.60	137
1.1604	70.938	70.75	0.26%	82.316	64.3	61.6	48	51	78.5	83.25	75.75	73	82.5	22.7	645	28.41	146
1.1603	77.629	77.77	-0.18%	90.073	67.8	64.3	49	53	82.75	88.5	80.5	76.75	86.125	25.31	709	28.01	155
1.1603	86.676	86.64	0.04%	100.571	72.6	68.5	52	55	88	95	86.75	81.75	91.125	28.88	800	27.70	168
1.1603	96.104	95.43	0.70%	111.510	78.2	72.9	54	58	93.75	101.25	92.75	87.25	96.5	32.52	894	27.49	181

Table 3-1: Characterization results of discrete IRS (circuit in Figure 3-1)

Current Sensor Comparison – PCB IR Drop														
PCB IR Drop				Calculated Output Based on Rg (1K) Temperature					Compensation Using Measured VDDC Plane-1 Temperature					
Measured Amplifier Output Voltage (mV)	ΔV/ΔI (mΩ)	Linearity Error (%)	Rg Calculated (KΩ)	Gain (V/V)	Calculated Output Voltage (mV)	ΔV/ΔI (mΩ)	Linearity Error (%)	Rg Calculated (KΩ)	Gain (V/V)	Calculated Output Voltage (mV)	ΔV/ΔI (mΩ)	Linearity Error (%)		
101	-	-	1.062	29.67	97.04	-	-	1.073	29.41	96.16	-	-		
115	8.163	-5.84%	1.066	29.57	111.25	8.468	-4.58%	1.078	29.28	110.14	8.325	-3.21%		
131	8.395	-3.16%	1.070	29.47	127.90	8.636	-2.68%	1.082	29.16	126.57	8.510	-1.05%		
158	8.705	0.41%	1.074	29.37	154.76	8.816	-0.65%	1.090	28.98	152.75	8.641	0.48%		
166	8.633	-0.41%	1.078	29.27	162.60	8.708	-1.87%	1.091	28.94	160.82	8.587	-0.15%		
175	8.615	-0.62%	1.078	29.27	171.50	8.669	-2.31%	1.095	28.86	169.09	8.490	-1.28%		
182	8.514	-1.78%	1.078	29.27	180.39	8.762	-1.26%	1.096	28.84	177.74	8.575	-0.29%		
190	8.521	-1.71%	1.078	29.27	188.70	8.776	-1.10%	1.097	28.81	185.74	8.576	-0.28%		
207	8.418	-2.90%	1.078	29.27	206.26	8.674	-2.25%	1.095	28.85	203.30	8.508	-1.07%		
197	8.383	-3.30%	1.078	29.27	195.64	8.610	-2.97%	1.093	28.90	193.23	8.476	-1.45%		
220	8.417	-2.91%	1.082	29.16	219.20	8.641	-2.63%	1.098	28.77	216.21	8.491	-1.27%		
249	8.486	-2.11%	1.086	29.06	249.75	8.757	-1.32%	1.106	28.59	245.67	8.573	-0.32%		
292	8.529	-1.62%	1.094	28.87	293.56	8.775	-1.11%	1.117	28.31	287.90	8.562	-0.45%		
331	8.623	-0.53%	1.098	28.77	332.40	8.824	-0.57%	1.126	28.12	324.90	8.575	-0.29%		
370	**8.669**	**0.00%**	**1.102**	**28.67**	**372.40**	**8.874**	**0.00%**	**1.133**	**27.95**	**363.03**	**8.600**	**0.00%**		
408	8.690	0.25%	1.111	28.47	411.29	8.896	0.25%	1.144	27.70	400.18	8.606	0.07%		
449	8.751	0.94%	1.119	28.28	451.63	8.917	0.48%	1.156	27.44	438.15	8.599	-0.01%		
584	8.735	0.76%	1.094	28.87	589.43	8.905	0.35%	1.146	27.66	564.76	8.474	-1.46%		
645	8.876	2.39%	1.102	28.67	650.77	9.034	1.81%	1.157	27.41	622.17	8.582	-0.21%		
709	8.944	3.17%	1.111	28.47	720.65	9.173	3.37%	1.172	27.09	685.67	8.672	0.83%		
800	9.074	4.68%	1.119	28.28	816.73	9.343	5.29%	1.192	26.66	770.07	8.749	**1.73%**		
894	9.172	**5.80%**	1.131	27.99	910.37	9.407	**6.01%**	1.216	26.18	851.38	8.735	1.57%		

Table 3-2: Comparison results of current sensor using PCB IR drop

Current Sensor Comparison – Substrate IR Drop																				
Unadjusted Values			Compensation Using On-Die Temperature Sensor #0			Compensation Using On-Die Temperature Sensor #1			Compensation Using On-Die Temperature Sensor #2			Compensation Using On-Die Temperature Sensor #3			Compensation Using External Sensor		
Amplifier Output Voltage (mV)	ΔV/ΔI (mΩ)	Linearity Error (%)	Adjusted Output Voltage (mV)	ΔV/ΔI (mΩ)	Linearity Error (%)	Adjusted Output Voltage (mV)	ΔV/ΔI (mΩ)	Linearity Error (%)	Adjusted Output Voltage (mV)	ΔV/ΔI (mΩ)	Linearity Error (%)	Adjusted Output Voltage (mV)	ΔV/ΔI (mΩ)	Linearity Error (%)	Adjusted Output Voltage (mV)	ΔV/ΔI (mΩ)	Linearity Error (%)
35.8	-	-	35.80	-	-	35.80	-	-	35.80	-	-	35.80	-	-	35.80	-	-
39.8	2.383	17.9%	42.34	3.894	-6.9%	42.36	3.906	-7.5%	42.31	3.881	-7.61%	42.37	3.912	-6.85%	42.35	3.901	-6.71%
44.6	2.463	21.9%	49.83	3.927	-6.1%	49.76	3.906	-7.5%	49.72	3.896	-7.25%	49.80	3.918	-6.70%	49.84	3.928	-6.08%
53.5	2.703	33.8%	61.90	3.985	-4.8%	61.79	3.970	-6.0%	61.68	3.953	-5.91%	61.85	3.978	-5.27%	61.84	3.976	-4.91%
55.9	2.670	32.1%	65.75	3.978	-4.9%	65.66	3.966	-6.1%	65.52	3.947	-6.04%	65.71	3.973	-5.39%	65.71	3.973	-5.00%
57.9	2.573	27.3%	70.07	3.990	-4.6%	69.96	3.977	-5.8%	69.83	3.961	-5.70%	70.06	3.988	-5.02%	70.04	3.986	-4.68%
60.6	2.607	29.0%	73.82	3.997	-4.5%	73.74	3.988	-5.6%	73.62	3.975	-5.38%	73.82	3.996	-4.84%	73.78	3.993	-4.52%
63.1	2.614	29.4%	77.57	3.999	-4.4%	77.50	3.992	-5.5%	77.40	3.983	-5.20%	77.62	4.003	-4.66%	77.54	3.996	-4.43%
57.2	1.699	-15.9%	85.36	3.935	-5.9%	85.39	3.938	-6.8%	85.29	3.930	-6.45%	85.31	3.931	-6.38%	85.27	3.928	-6.07%
55.8	1.746	-13.6%	80.82	3.931	-6.0%	80.84	3.933	-6.9%	80.71	3.921	-6.66%	80.77	3.927	-6.49%	80.75	3.925	-6.15%
61.9	1.846	-8.6%	91.94	3.971	-5.1%	92.05	3.979	-5.8%	91.89	3.967	-5.56%	92.00	3.975	-5.34%	91.86	3.965	-5.17%
69.8	1.950	-3.5%	105.92	4.020	-3.9%	106.14	4.033	-4.5%	105.85	4.017	-4.39%	106.09	4.030	-4.02%	105.86	4.017	-3.93%
81.6	2.045	1.2%	127.40	4.090	-2.2%	127.92	4.113	-2.6%	127.47	4.093	-2.57%	127.72	4.104	-2.25%	127.35	4.088	-2.25%
89.1	1.998	-1.1%	146.04	4.133	-1.2%	146.98	4.168	-1.3%	146.44	4.148	-1.27%	146.45	4.148	-1.21%	145.98	4.131	-1.22%
98.5	**2.021**	**0.0%**	**165.64**	**4.184**	**0.0%**	**166.88**	**4.224**	**0.0%**	**166.16**	**4.201**	**0.00%**	**166.10**	**4.199**	**0.00%**	**165.56**	**4.182**	**0.00%**
107	2.015	-0.3%	185.25	4.231	1.1%	186.88	4.277	1.2%	186.09	4.254	1.27%	185.91	4.249	1.20%	185.10	4.226	1.06%
117	2.042	1.1%	206.03	4.281	2.3%	208.08	4.332	2.6%	206.96	4.304	2.45%	206.58	4.294	2.27%	205.66	4.271	2.14%
137	1.830	-9.4%	266.88	4.179	-0.1%	268.58	4.210	-0.3%	267.86	4.197	-0.10%	264.20	4.131	-1.63%	266.24	4.167	-0.35%
146	1.798	-11.0%	294.60	4.223	0.9%	297.59	4.271	1.1%	296.94	4.261	1.42%	292.20	4.183	-0.38%	294.38	4.219	0.89%
155	1.753	-13.2%	327.34	4.288	2.5%	331.77	4.354	3.1%	330.48	4.335	3.18%	324.12	4.241	1.00%	326.37	4.274	2.21%
168	1.716	-15.1%	372.31	4.369	4.4%	378.89	4.454	5.4%	377.12	4.431	5.47%	368.40	4.318	2.83%	370.90	4.350	4.03%
181	1.679	-16.9%	421.10	4.456	6.5%	429.11	4.549	7.7%	426.79	4.522	7.65%	416.40	4.402	4.84%	418.99	4.432	5.99%

Table 3-3: Comparison results of current Sensor using substrate IR drop

Table 3-3 contains compensated and uncompensated current sensing results using substrate IR drop. The first three columns are the measured values when R_g ($R4222$ in Figure 3-1) was replaced with an ordinary 510Ω resistor instead of thermal sensor (described in section 2.2.2). The linearity error shows considerable inaccuracy without thermal compensation (more than $+33\%$ and -16%, highlighted numbers in red in Table 3-3). Then, the numerical compensation technique, introduced in section 2.2.1, was used to calculate rest of columns in Table 3-3 using ASIC junction temperature read by each on-die or external temperature sensor. The results, numbers highlighted in **green** in Table 3-3, show consistent and considerable improvement in the linearity (about $\pm 7\%$).

Figure 3-2 plots uncompensated values from Table 3-3 with two attempts of curve fitting. The red line is the linear method and the blue curve is polynomial degree of two (both curves are built-in trend line functions in Microsoft Excel graph). The nonlinearity of the uncompensated data is obvious. The R^2 parameter is R-squared value (also known as the coefficient of determination) a number from 0 to 1 that reveals how closely the estimated values for the trend line correspond to the actual data. The most reliable trend line is with R-squared value as close to 1 as possible. The R^2 parameter is used to compare result of different sets of data in the coming graphs.

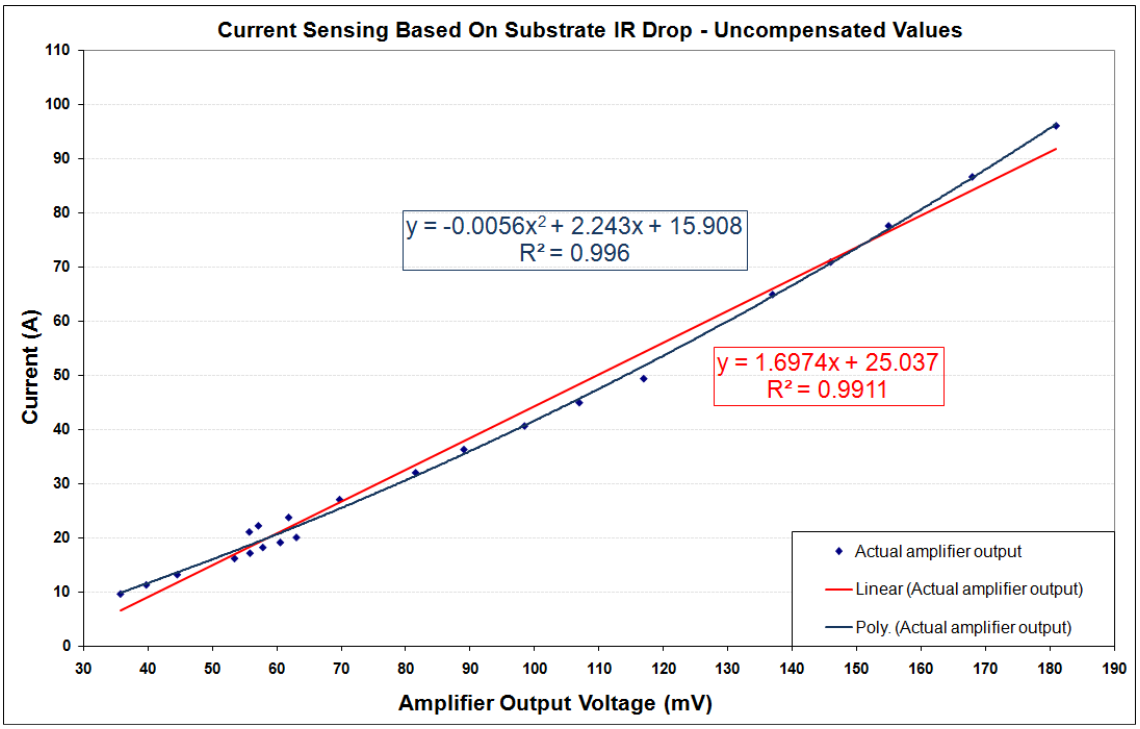

Figure 3-2: Uncompensated result of current sensor based on substrate IR drop

Figure 3-3 and Figure 3-4 are plots of compensated values using TS_0 and TS_3 from Table 3-4 respectively. Both graphs have linear and polynomial trend lines similar to Figure 3-2 as described above. Either from graph or R-squared values, it is clear that linearity has substantially been improved compared to Figure 3-2. It also highlights that thermal

compensation simplifies the curve fitting complexity so that a linear curve fitting mostly is sufficient.

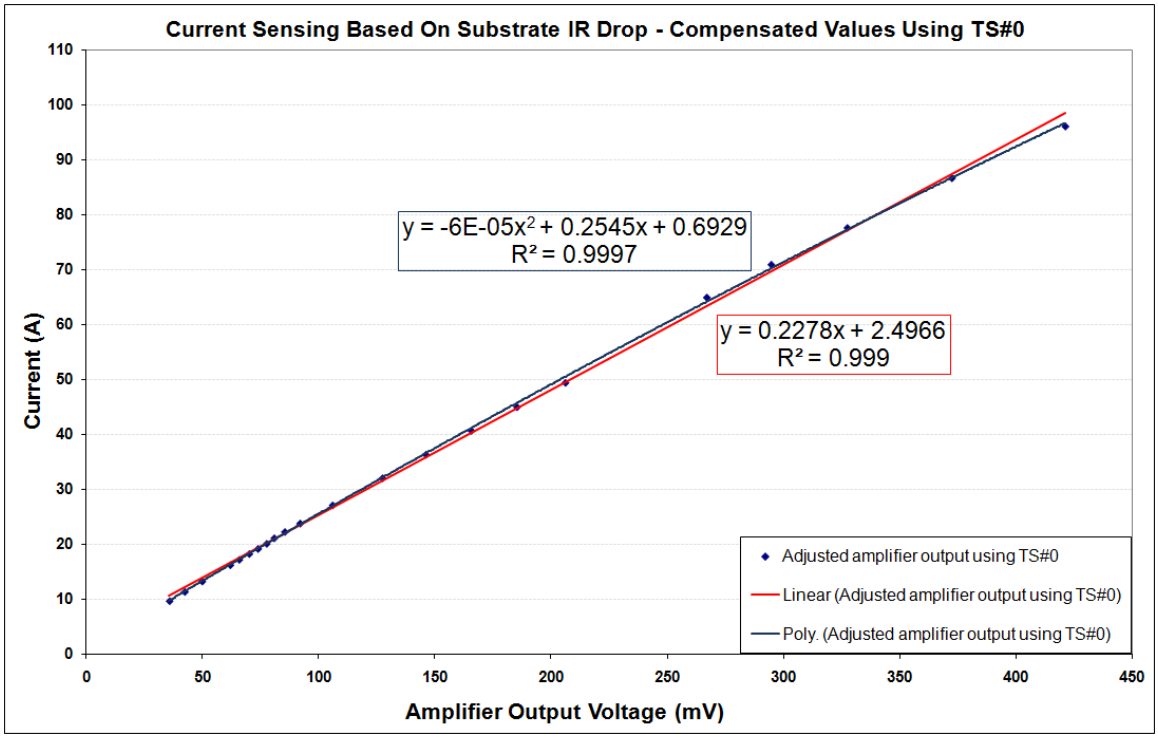

Figure 3-3: TS0 Compensated result of current sensor based on substrate IR drop

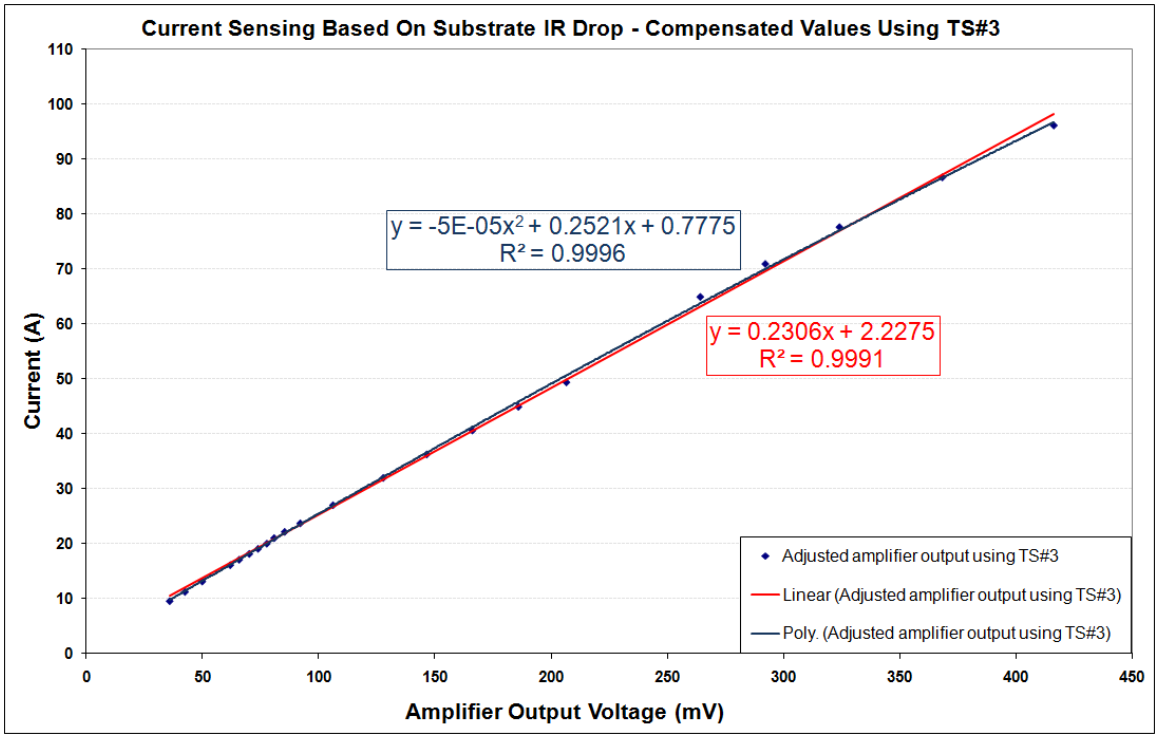

Figure 3-4: TS3 Compensated result of current sensor based on substrate IR drop

In order to calculate accuracy of the solution post calibration, the linear fit is chosen from Figure 3-2, Figure 3-3, and Figure 3-4. Table 3-4 contains accuracy of each case compared to the actual current measured (the first column). Highlighted numbers, in red, indicate the worst case inaccuracy in each column. The compensated values yield better results compared to voltage regulator readout. Despite the improvement still at very light loads (less than 10% of full load) higher accuracy may be needed as those in Table 3-4. To address that, the linear curve can be broken into two or more sections to use piece-wise linear curve fitting.

Comparing Accuracy of Different Methods						
Measured Current (A)	Calculated Current TS#0 Linear Fit (A)	Error (%)	Calculated Current TS#3 Linear Fit (A)	Error (%)	Current Reported By VR (A)	Error (%)
9.65	10.48	-8.67%	10.65	-10.42%	6.13	36.43%
11.32	12.00	-5.93%	12.14	-7.20%	9.20	18.79%
13.22	13.71	-3.72%	13.85	-4.75%	9.20	30.43%
16.19	16.49	-1.82%	16.60	-2.48%	15.33	5.35%
17.18	17.38	-1.19%	17.47	-1.74%	15.33	10.75%
18.24	18.38	-0.81%	18.46	-1.22%	15.33	15.94%
19.16	19.25	-0.47%	19.31	-0.80%	15.33	20.00%
20.09	20.13	-0.17%	20.17	-0.38%	18.40	8.44%
22.24	21.90	1.53%	21.94	1.34%	21.46	3.50%
21.10	20.85	1.17%	20.91	0.91%	21.46	-1.72%
23.78	23.44	1.44%	23.44	1.45%	21.46	9.77%
27.09	26.69	1.46%	26.62	1.71%	27.59	-1.87%
32.04	31.68	1.13%	31.52	1.63%	30.73	4.09%
36.32	36.00	0.89%	35.77	1.53%	33.81	6.91%
40.68	40.53	0.36%	40.23	1.10%	39.86	2.00%
44.97	45.10	-0.28%	44.70	0.61%	45.99	-2.25%
49.42	49.87	-0.91%	49.43	-0.03%	49.89	-0.96%
64.94	63.15	2.76%	63.29	2.54%	64.88	0.10%
70.94	69.61	1.87%	69.61	1.88%	70.75	0.26%
77.63	76.97	0.85%	77.06	0.73%	77.77	-0.18%
86.68	87.18	-0.58%	87.31	-0.73%	86.64	0.04%
96.10	98.25	-2.23%	98.42	-2.41%	95.43	0.70%

Table 3-4: Comparing accuracy of current sensor using substrate IR drop with linear fit

3.3 PCB Temperature None Uniformity

In the analysis of PCB IR sensing, it was expressed that the linearity of the result depends upon location of R_g. To investigate this further, one of the graphic cards under test, which could accommodate two different cooling solutions, was selected. Then using an infrared camera, thermal picture of the PCB was taken with each cooling solution. The function of cooling solution is to keep GPU junction temperature within the set limit. Therefore, both graphic cards were setup to maintain same junction temperature when infrared picture taken (Figure 3-5). Table 3-5 and Table 3-6 summarize PCB surface temperature with each of cooling solutions (Figure 3-5A & B respectively) at three selected areas, identified by Ar1, Ar2 and Ar3.

Despite same ambient temperature, setup and test conditions, there is considerable difference in the PCB surface temperature observed between two cooling solutions. Looking at each of Figure 3-5A and Figure 3-5B alone, there is a PCB temperature difference of nearly 70°C. This poses a practical challenge where to place the gain thermal sense resistor (R_g) to achieve adequate result. Even if by going through an in-depth analysis of all thermal sources and PCB structure to determine the ideal location for R_g, yet any changes to layout, power supply (second main heat source after the GPU) will trigger reevaluation and recalibration of the solution. It is also a common practice in graphics market to replace manufacturer provided cooling solution with the aftermarket heatsinks, it poses another application level limitation to this method of current measurement, where can be impacted post design release.

Area	Min (°C)	Max (°C)	Mean (°C)
Ar1	61.3	89.9	79.4
Ar2	50.8	81	73.7
Ar3	46.9	77.5	68.9

Table 3-5: PCB Surface temperature at different spots marked on Figure 3-5A

Area	Min (°C)	Max (°C)	Mean (°C)
Ar1	77.8	108.1	98.4
Ar2	60.9	102.1	92.3
Ar3	58.3	101.4	91.2

Table 3-6: PCB Surface temperature at different spots marked on Figure 3-5B

Large PCB size (95mm x 210mm), secondary heat sources (DRAMs, VRs), cooling solution, system airflow and ambient temperature are other key factors in determining the PCB temperature variation in addition to the load current. On the other hand, these variables have little or any effect on the substrate IR drop. For instant, typical substrate size for this class of GPU is about 30~45mm x 30~45mm, much smaller than PCB area. There is one heat source, which is the load (GPU itself). The cooling solution function is to keep the junction within specified range, and it doesn't suffer from architecture or design changes made to the cooling solution. Substrate temperature follows GPU junction

very closely compared to PCB temperature. This can be realized by comparing temperature sensors results in Table 3-1, where show temperature variations ~10°C across a very large die size (18mm x 18mm). Portion of this variation is due to sampling time difference between sensors, and inaccuracy of the sensors. Nonetheless, it is much less than PCB temperature variation (Figure 3-5).

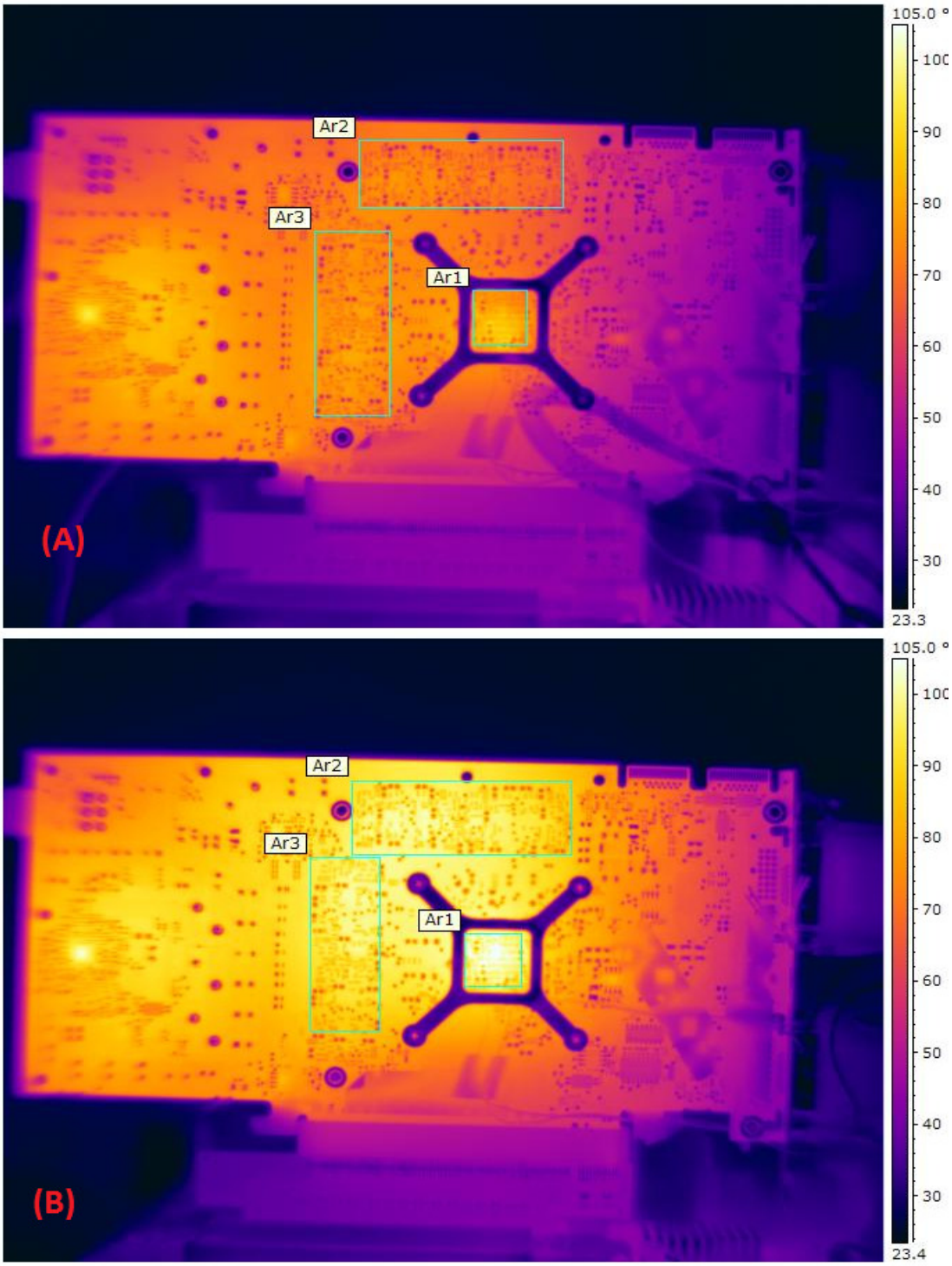

Figure 3-5: Infrared photos of the PCB under test with two different cooling solutions

3.4 Dynamic Behavior Analysis

As described in chapter one, the power consumption in CMOS circuits contains a static portion (mainly induced by device leakage), and dynamic portion. This is from circuit and device point of view. However even for a known leakage, operating voltage, clocks, and junction temperature, there is substantial power consumption change due to hardware utilization level (also known as activity factor), which is software application dependent. In this work, dynamic current refers to portion that is induced by software activity that has much slower rate of change than operating frequency of GPU. To show this, one of sample graphic cards tested under application that stresses the GPU near its peak power consumption yet with little load step (~5% change). After about 30 minutes running, when setup reached thermal equilibrium, the current was measured using substrate IR sensing and compensated using external temperature sensor. The current sensor output was digitized using 10-bit ADC (Analog to Digital Convertor) built into GPU at 1 sample per second. As defined above, this is close to a static load. The sensor was calibrated using Cubic fitting method to yield lowest level of in accuracy. Figure 3-6 plots the result. The upper two curves are IRS output after calibration and the actual load current (the left Y-axis in Amps). These two curves are nearly overlapped, with an error about 0.1% indicated by the lower curve and the right Y-axis in percentage.

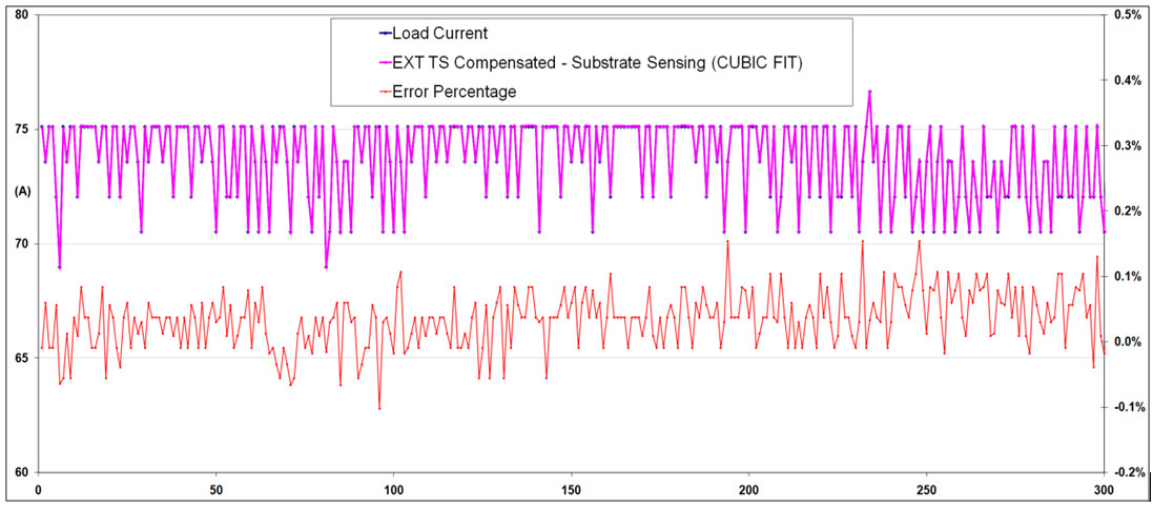

Figure 3-6: Current measurement result using substrate IR drop sensing under static load

The curve fitting parameters were recorded. Then same setup was used to run a different application, which generates a dynamic current profile. The load current was measured and sampled with the same ADC and settings, and after thermal equilibrium. Figure 3-7 illustrates the result. There are two prominent changes; first, the GPU is operating at lower power level, which proves software application's impact on the power consumption. Second, despite that current sensing circuit follows the load pattern very well, per Figure 3-7, yet there is about 5% inaccuracy. Closer examination of the data shows even at similar step change as previous example but near 55A (instead of 75A) there is 5% extra error. It points to a systematic error. By further analysis of the system, it was found that the ADC gain must be adjusted over input voltage range in order to compensate for the error. At first glance, it is expected and as mentioned previously a

piecewise linear calibration must address this concern. Although, it highlights that a static current measurement technique is not necessarily adequate for dynamic load measurement.

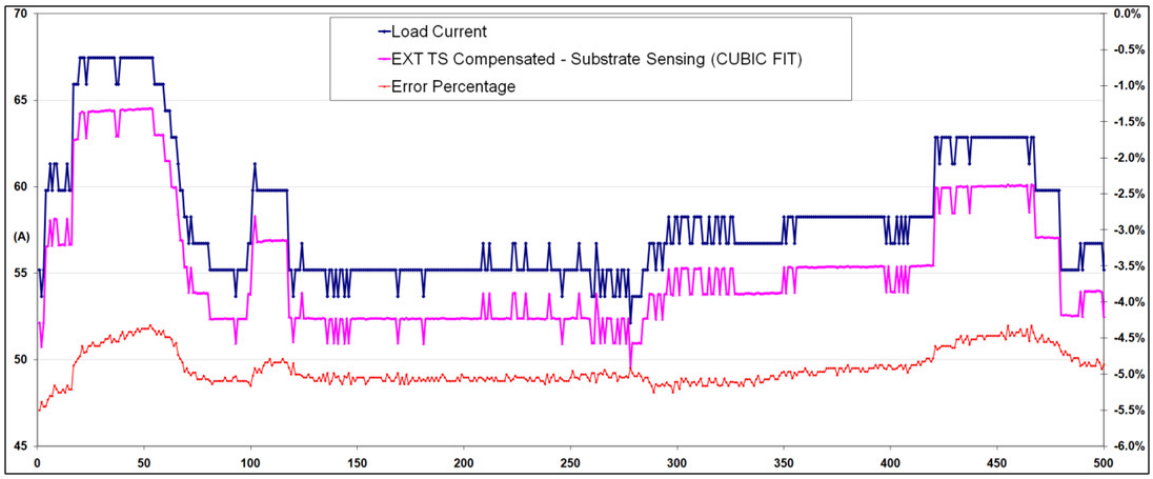

Figure 3-7: Current measurement results using substrate IR drop sensing under dynamic load

Aside from absolute accuracy, this sensing method reveals load behavior under different applications, which can be used to characterize applications or power delivery network. To verify the circuit dynamic behavior, input and output of the instrumentation amplifier was monitored using oscilloscope. Figure 3-8 is the scope capture of the differential input (VT-ASIC) and output of amplifier (VOUT1) under 140A load switching at 2.38MHz. This is within expected behavior of the operational amplifier.

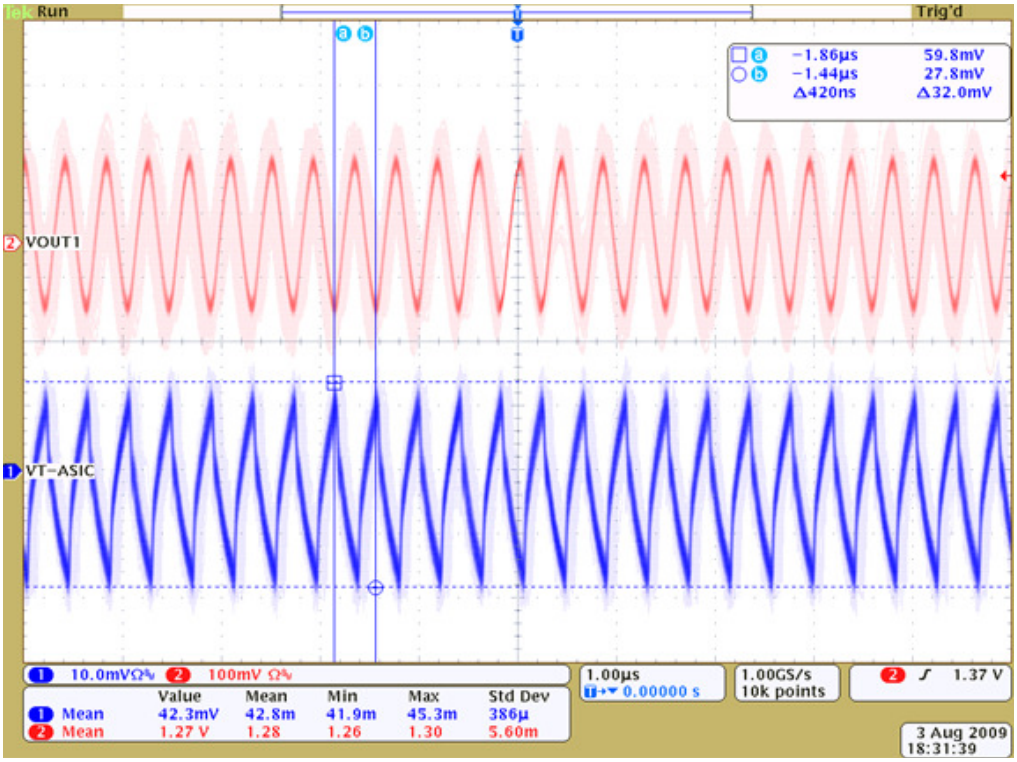

Figure 3-8: IA differential input (VT-ASIC) and output (VOUT1) at 140A/2.38MHz load

3.5 Conclusions

The circuit schematic for discrete implementation of IRS provided along with the description of the circuit settings. The characterization results for both current sensing using PCB and substrate inherent resistances were reviewed. Both methods yielded adequate linearity and accuracy. Both analog and numerical compensation techniques proved to be effective by improving accuracy and linearity of the result. On the other hand, it was shown that uncompensated values have considerable inaccuracy.

Despite that current sensing using PCB IR drop provided very good correlation and linearity, due to its dependency to circuit board layout, cooling solution, and surrounding heat sources, it doesn't meet the criteria established in section 1.3. As such, the substrate (or on-die) resistance current sensing are preferred methods. PCB resistance sensing can be used in controlled environment such as lab or designs that are not subject to change (limited usage).

The high accuracy level achieved under static load doesn't guarantee the accuracy under dynamic load. As such, dynamic behavior of circuit must be considered at design cycle. Additional calibration steps might also be required to support dynamic load.

Given discrete implementation demands highly accurate resistors, and very low offset operation amplifier, the discrete circuit cost is high and it occupies considerable PCB surface area. Both increases bill of material (BOM) cost substantially, which makes it impractical for consumer electronics market. Furthermore, it provides limited BW due to commercially available operation amplifiers and PCB parasitic parameters. Thus, it is recommended to use integrated implementation using adequate amplifier architecture (see chapter 4). Integrated solution also allows automating the calibration process. This reduces test & calibration time, which makes it suitable for high volume production.

Chapter 4 Selecting Instrumentation Amplifier Architecture

Once the current monitoring method is chosen, an amplifier is required to amplify the signal. In this work, inherent resistance is chosen as the sensing method. Thus, there is need to have amplifier that can detect very small voltage difference between two nodes. The most common topology to do this is called instrumentation amplifier (IA). Three major categories of instrumentation amplifiers are reviewed here.

4.1 Voltage Mode Instrumentation Amplifier

One example of this type of IA was shown in Figure 2-2. Three operation amplifiers and a resistor network were used to build an IA as discrete version of the IRS (described in chapter 3).

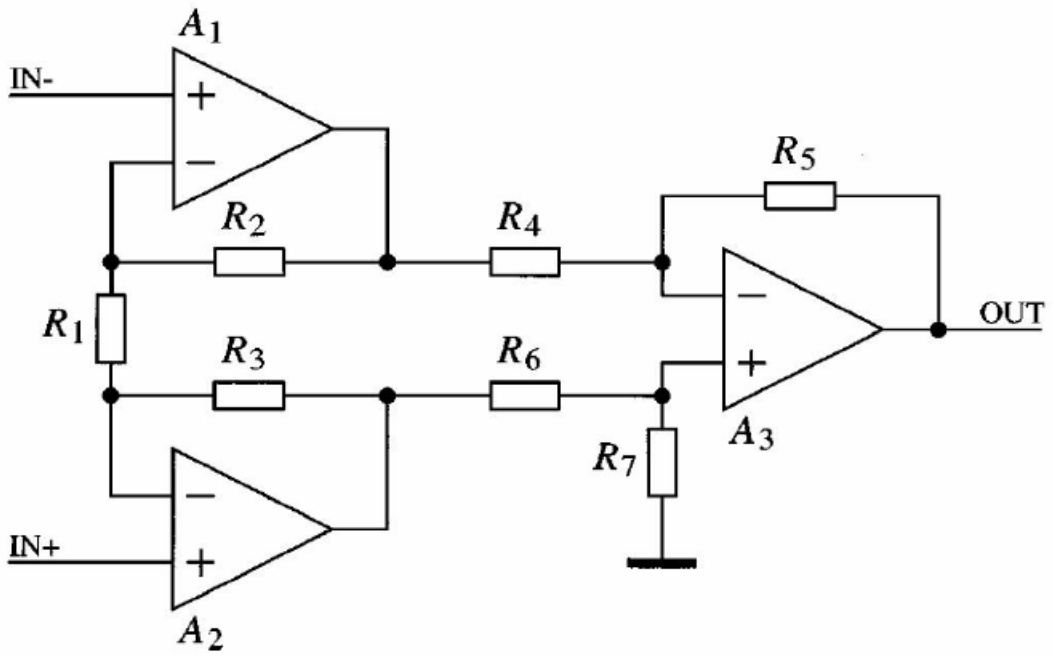

Figure 4-1: Voltage-Mode IA using three operational amplifiers

Figure 4-1 illustrates a well known IA configuration constructed using three operational amplifiers. In this topology, two opamps are used to implement a fully differential buffer, which is followed by a single opamp configured as a differential amplifier. To achieve a high CMRR, all resistors except for gain resistor $R1$ must be very well matched or the resistor ratios must be trimmed. The CMRR is also dependent on the voltage gain of the input stage formed by first two operational amplifiers along with resistors $R1, R2$ and $R3$. Hence, gain must be maximized to improve CMRR [3][4]. Due to the gain bandwidth product limitation of the voltage mode operational amplifier, these high-CMRR instrumentation amplifiers provide relatively low bandwidth, which is not desirable for dynamic load profiling. The example of such limitation was illustrated in

Figure 1-1. Furthermore several other implementations were cited, which all exhibited similar low BW.

Beside limited GBWP of this topology, matching resistors poses another practical challenge. Either highly accurate discrete resistors (0.1% or better, as what was used in the circuit Figure 3-1), or laser-trimmed on-chip resistors are needed. First choice add to pin counts and BOM cost yet reduces the BW further due to parasitic capacitance induced by off-chip routing of intermediate signals. The second choice, laser trimming, is an additional step in IC fabrication that increases unit cost. Still, it is a very non-trivial step, which is not used in most CMOS IC applications (like CPUs and GPUs).

4.2 Current Mode Instrumentation Amplifier

One method to eliminate matched resistor requirement in voltage mode IA (Figure 4-1) is to replace them with current mirrors as shown in Figure 4-2 [5].

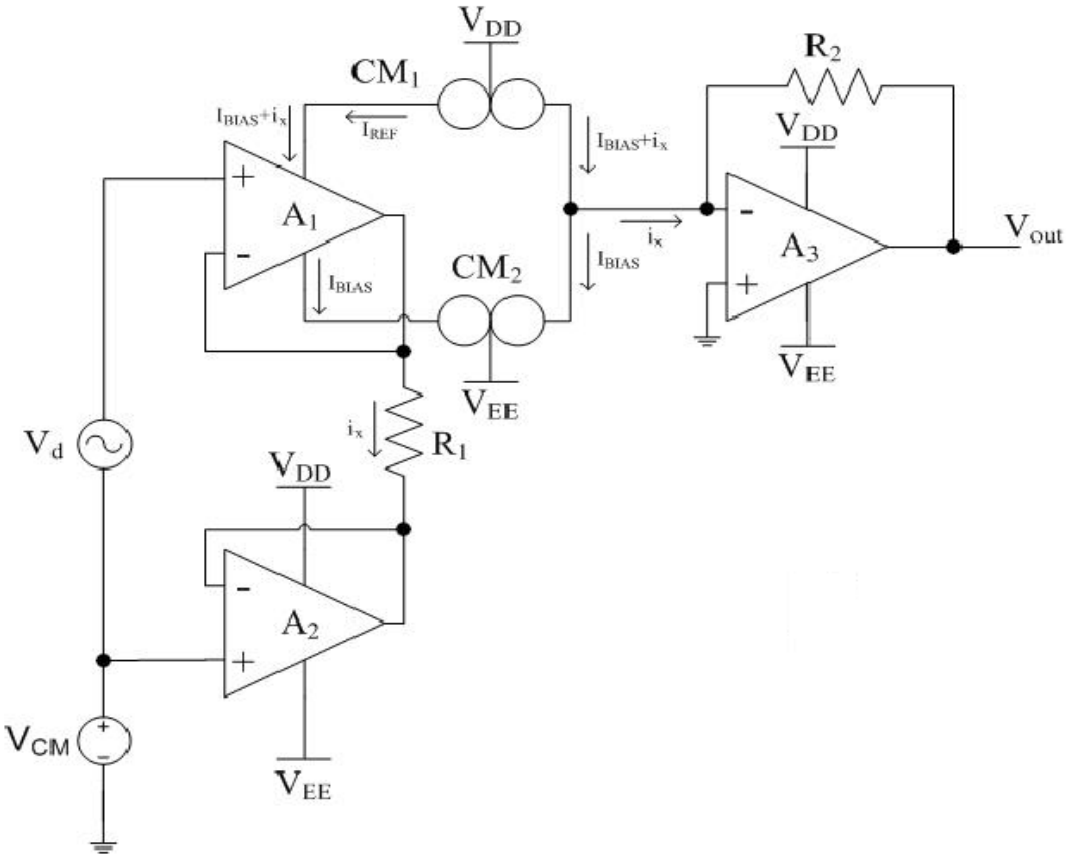

Figure 4-2: Current-mode IA using three operational amplifiers [5]

In this implementation, first introduced by B. Wilson in 1984 [5], the current mirrors, $CM1$ and $CM2$, are used as current summing nodes instead of traditional resistor networks [5]. The input stage is similar to voltage-mode IA with two unity gain operation amplifier to form a differential input stage, which generates input voltage delta of V_d across $R1$. Function of the current mirrors is to copy current going through R1 (induced by V_d) into $R2$. In this case, the amplifier gain is simply defined by ratio of $R2$ and $R1$.

Assuming open loop gain of input stage opamps are A_{o1} and A_{o2}, it can be shown that:

$$CMRR = \frac{A_d}{A_{cm}} = \frac{[A_{o1} + A_{o2} + 2A_{01}A_{02}]}{[A_{o1} - A_{o2}]} \quad (4\text{-}1)$$

Now in order to increase CMRR either the open loop gain of each amplifier must be increased or mismatch between two input stage opamps must be reduced. Given the target is CMOS process, systematic limitation of CMOS amplifier sets limit on the open loop gain that can be achieved. Therefore, the mismatch of the two opamps must be minimized to improve CMRR. Figure 4-3 is the plot of CMRR versus mismatch (in percentages) for various open loop gains.

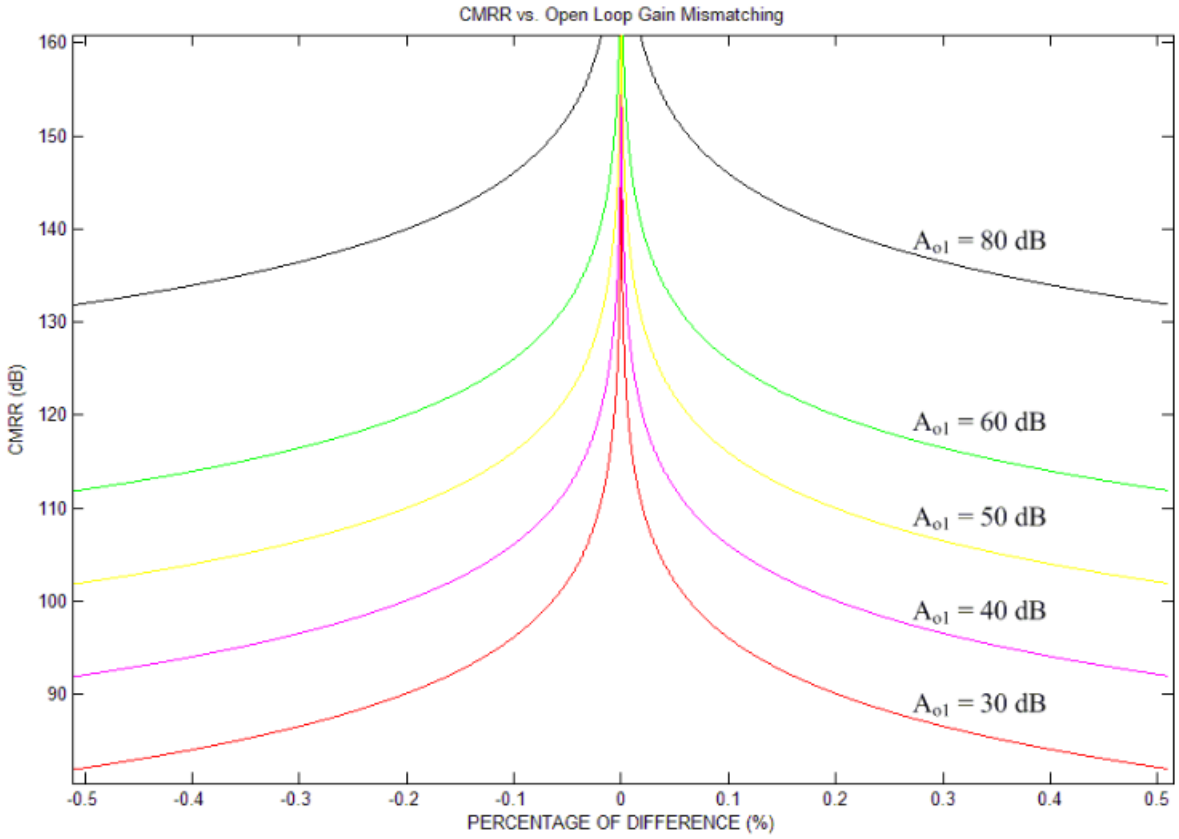

Figure 4-3: CMRR vs. Open Loop Gain Mismatching in CM IA [5]

This technique eliminates matched resistors, but achieving CMRR >120dB poses a challenge in the case of CMOS amplifier. By examining cases like [5] & [10], CMRR in the range of 80 to 120dB seems practical.

Bandwidth of current mode IA remains comparable to the voltage mode, yet insufficient for dynamic current sensing.

4.3 Current Conveyor Based Instrumentation Amplifier

There are three generations of current conveyors. The second generation of the current conveyor, noted as CCII, is only reviewed here.

4.3.1 Current Conveyor – Second Generation (CCII)

The second generation current conveyor (CCII) is represented in Figure 4-4 as a three-port device, where *Y* terminal is input of a voltage follower and *X* is its output, where output current of node *X* is copied into *Z* terminal. Figure 4-5 provides the equivalent circuit of CCII, and its function in the form of matrix. It also implies one can build voltage follower without having a feedback loop [6].

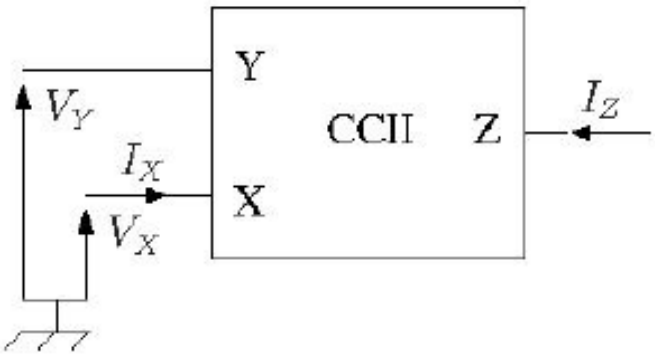

Figure 4-4: Current conveyor second generation (CCII) as a three-port device

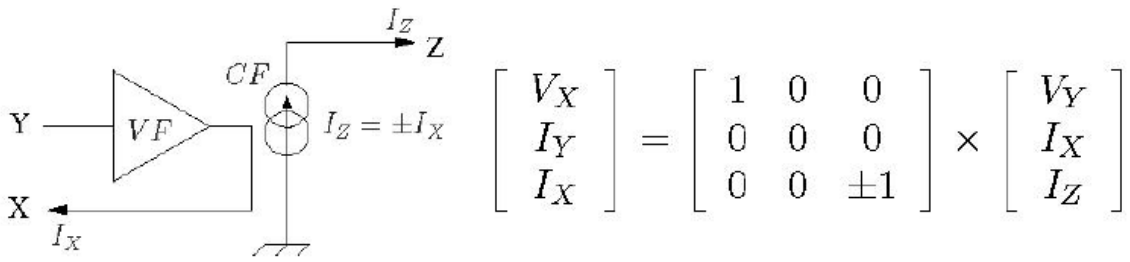

Figure 4-5: Equivalent function of CCII in the form of circuit model and matrix [6]

Depends of the implementation, the current conveyed to *Z* terminal can be inverting (CCII-) or non-inverting (CCII+). CCII functional behavior provides attractive alternative implementation methods to the conventional methods in many applications. CCII has been around for many years, although recently it is being used in variety of applications such as current mode filters, like [30] & [31], current mode multipliers, like [29] & [32], and most often to build various types of amplifiers [3-4][6-7][9][12].

4.3.2 Building Instrumentation Amplifier using CCII+

There are different methods to form an instrumentation amplifier using CCII as building block. In most methods, if not all, the input stage is shaped using two CCII to realize a differential input sensing. An example of this implementation is illustrated in Figure 4-6, where $A1$ and $A2$ forming the input stage. Past input stage, the conventional method is to use an operation amplifier, $A3$ in Figure 4-6, to generate adequate gain (ratio of $R2$ and $R1$) [7]. Several other techniques have been developed to improve CMRR, reduce signal distortion or increase gain beyond conventional method.

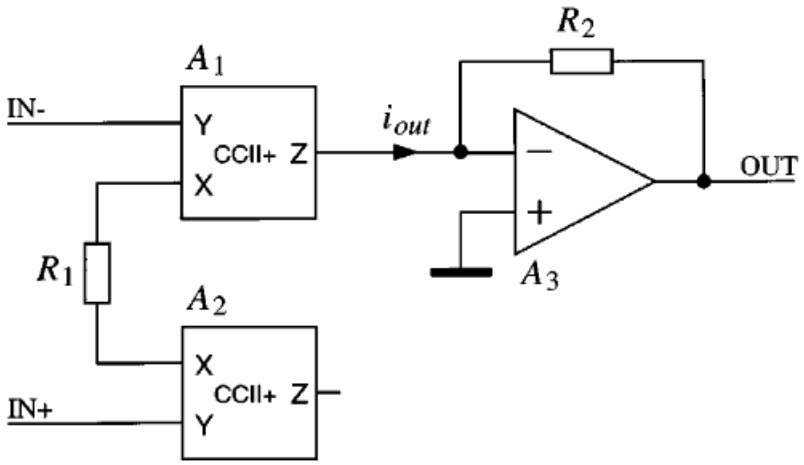

Figure 4-6: Conventional IA using CCII

It is apparent from Figure 4-6 that there is no need for matched resistors, which is another benefit of this technique. Another advantage compared to voltage-mode IA, is that CMRR is independent of the voltage gain [3]. Despite the benefits, typical CMRR achieved using conventional method is ~80dB [7]. Other techniques are used to improve CMRR beyond 100dB such as output current subtraction, which can be done via output stage opamp ($A3$ in Figure 4-6) and by connecting Z terminal of $A2$ to positive input of $A3$ while adding additional resistor from that node to the negative rail. It can also be achieved by adding one additional CCII+ to invert the output current of $A2$ and then summing it with $A1$ output current as Figure 4-7 [7]. The RC network ($C1, R3$) are to compensate for the high-frequency phase shift induced by $A3$.

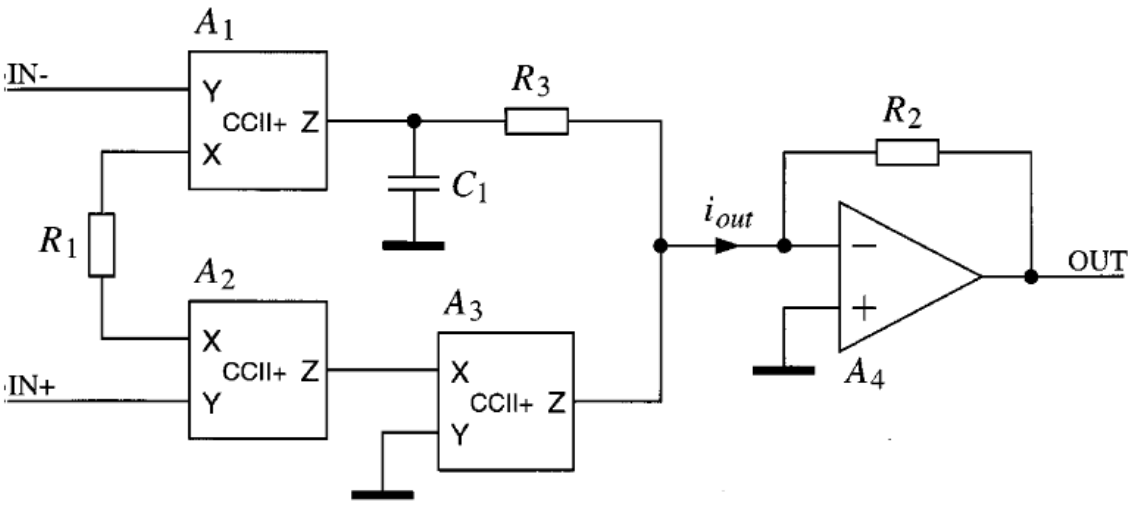

Figure 4-7: Improved CMRR using current inverting technique [7]

Figure 4-8 is a cascade topology to increase gain and improve CMRR up to 140dB [3]. This method increases silicon area needed to implement it, but at the same time offers a robust mechanism to tradeoff performance needed verses silicon area. The function of $C1$ and $R3$ is same as what described for Figure 4-7.

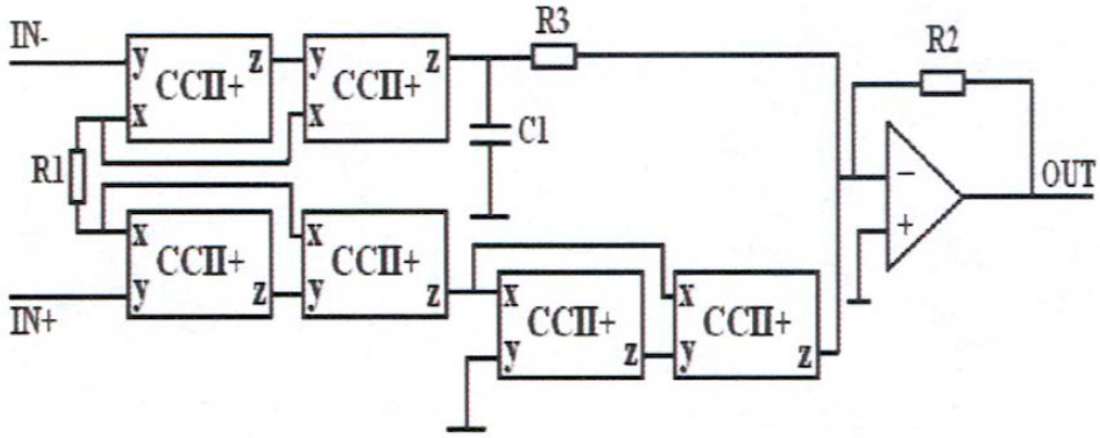

Figure 4-8: High CMRR IA using Cascade CCII [4]

Often a differential output is required to improve noise immunity and to simplify routing, or to connect to a differential analog to digital convertor. Figure 4-9 shows a simple and effective method to achieve that [6]. It eliminates the output stage opamp, yet reduces silicon area needed.

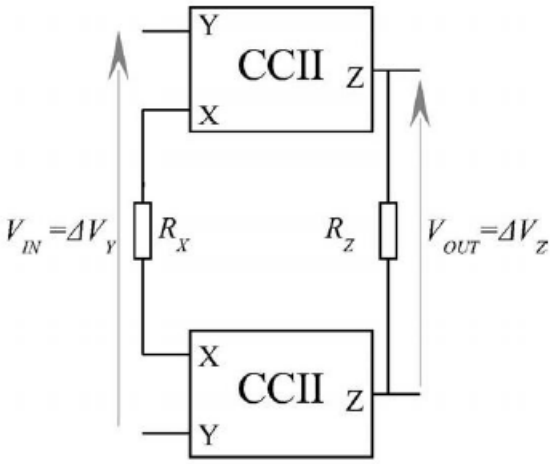

Figure 4-9: Differential input/output IA using CCII [6]

Summary of the advantages [3][6-7]:

- High BW due to open loop operation of amplifier (no gain bandwidth product limitation)
- CMRR is independent of voltage gain
- High CMRR can be achieved
- No matching resistors needed
- Current mode operation makes it less susceptible to noise and crosstalk
- Variety of topologies to choose from

Given benefits and robustness of CCII based IA, this architecture is selected as the preferred choice for current sensing.

4.3.3 CCII Cell Input Stage

In CMOS technology, CCII cell can be realized with NMOS or PMOS input stage. Figure 4-10 illustrates NMOS for X and Y terminal ($M1$ & $M2$) while Figure 4-11 is designed with PMOS ($M1$ & $M2$). A closer look at either circuit shows many similarities with traditional differential pairs that form an operation amplifier. For instant in Figure 4-10 by removing current mirrors formed by $M5/M6$ and $M3/M4$ and connecting drain of $M9$ and $M10$ to each other, it yields a differential pair. $M9$ and $M10$ functions are also similar to that of used in differential pairs to set a tail current I_B.

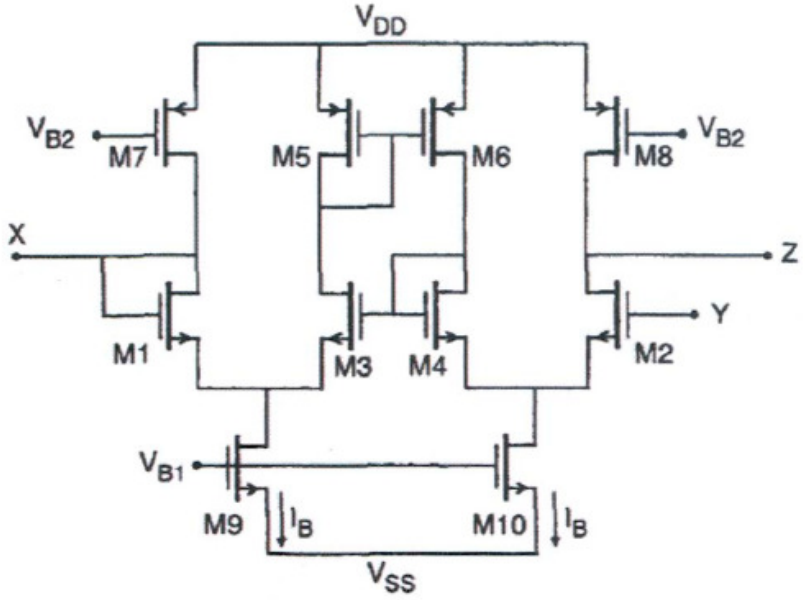

Figure 4-10 CCII Cell with NMOS input stage [4]

Both designs in Figure 4-10 and Figure 4-11 intended for application, where VSS voltage is negative. However, IRS is intended for integration into GPUs and CPUs. In these applications negative voltage is not available. Furthermore, the amplitude of positive supply rail for analog macros is limited to 1.8V in most submicron geometries, and expected to be reduced to 1.5V in 20nm process node and beyond for mixed digital and analog designs. At the same time the input common voltage range in this application is that of standard digital cell can run at (range of 0.7~1.2V pending the process node). Such a variation in the common mode voltage, impacts transconductance of $M1$ and $M2$, which ultimately makes IA gain sensitive to common mode voltage. In advanced power management schemes used in IC with large silicon sizes, the core voltage is adjusted on demand to save power. For instant in case of personal computer sitting idle like a Windows static screen the graphic chip operates at much lower clock and voltage than running a 3D game. Therefore, it is expected to have a variation of ~400mV common-mode voltage as such the input stage must be designed to minimize the gain variation. A linear gain variation that can be adjusted at higher level of abstraction is also viable solution in most cases. This relies on the fact that when GPU or CPU wants to reduce/increase operating voltage/clocks, there is a digital control mechanism in place

(firmware/software based or hardware state machine). Same mechanism can be used to adjust the gain when operating state changes.

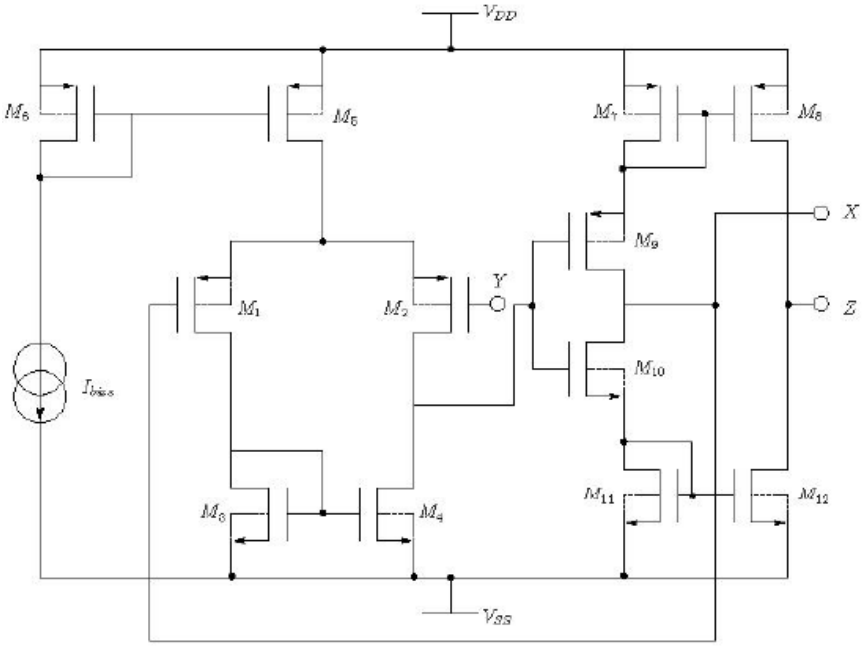

Figure 4-11: CCII Cell with PMOS input stage [6]

To reach negative supply rail PMOS must be used while keeping the drain voltage close to the ground voltage, and to reach the positive supply rail NMOS must be used while keeping the drain voltage close to supply voltage. To achieve a full range, known as Rail-to-Rail, a combination of NMOS and PMOS, with proper sizing, must be used in junction with a method to sum up the current generated by each one. The goal is to maintain constant total current, also known as constant transconductance or constant-gm circuit [14], across input common voltage range [8].

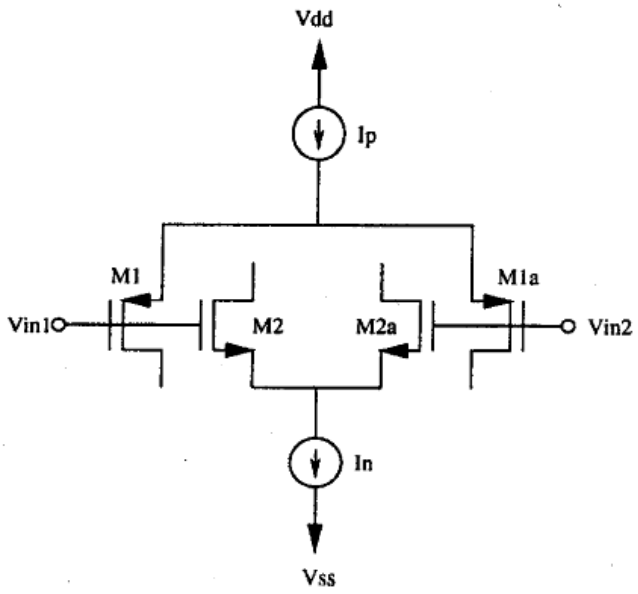

Figure 4-12: Conceptual diagram for rail-to-rail CMOS input stage

Figure 4-12 is the conceptual diagram for a rail-to-rail CMOS input stage. Gate of both $M1$ (PMOS) and $M2$ (NMOS) are connected to $Vin1$. Similarly, gate of both $M1a$ (PMOS) and $M2a$ (NMOS) are connected to $Vin2$. In case of CCII, $Vin1$ is the Y terminal and $Vin2$ is the X terminal. I_p & I_n are tail currents for PMOS and NMOS respectively. In this case the total transconductance (g_{mt}) equals sum of NMOS transconductance (g_{mn}) and PMOS transconductance (g_{mp}). The goal is to keep g_{mt} constant across common mode voltage range. Assuming strong inversion, g_{mn} & g_{mp} can be given by:

$$g_{mn} = \sqrt{2K_n I_n} \qquad K_n = \tfrac{1}{2}\,\mu_n C_{ox}\left(\frac{W}{L}\right)_n \tag{4-2}$$

$$g_{mp} = \sqrt{2K_p I_p} \qquad K_p = \tfrac{1}{2}\,\mu_p C_{ox}\left(\frac{W}{L}\right)_p \tag{4-3}$$

$$g_{mt} = g_{mn} + g_{mt} \tag{4-4}$$

Pending silicon process and fabrication tolerances, if matched NMOS and PMOS can be assumed (by sizing up W/L to compensate for μ_{n/μ_p} ratio), then constant-gm can be achieved via constant I_p & I_n as shown in Figure 4-12. Note must be taken that μ_{n/μ_p} ratio may have batch to batch variation within same process that could reach to $\pm 15\%$, in such a case other mechanism, like [14],[15], [18] and [19], must be used to adjust I_p & I_n accordingly to maintain constant-gm. The downside of rail-to-rail stage is that it requires sum of minimum supply voltage for each PMOS and NMOS inputs, assuming same saturation level for both PMOS and NMOS tail currents the minimum supply range is given by:

$$Vsup_{\min} = 2V_{GS} + 2V_{DSat} \tag{4-5}$$

4.4 Noise and Offset Cancelation Techniques

In many cases the performance of amplifier is dominated by input offset and noise. This is a prominent issue in CMOS amplifier given higher level of flicker noise. Conventional bipolar techniques such as trimming won't help to eliminate flicker noise in CMOS amplifiers [27]. In CMOS technology, often dynamic noise and offset cancellation is used. There are many methods developed to do this, but they can be categorized in two groups that are reviewed in this section.

4.4.1 Auto Zero Technique

This group covers methods so called autozero, self-calibrating opamp, two-signal approach, ping-pong opamp [24], and correlated double sampling [22], which operate on the same principle illustrated by Figure 4-13. It operates based on two phases, first a sampling phase, $\varphi 1$ when the offset is measured and sampled on C_{az} followed by amplification phase, $\varphi 2$, when the sampled offset is subtracted from the input signals and amplified [27].

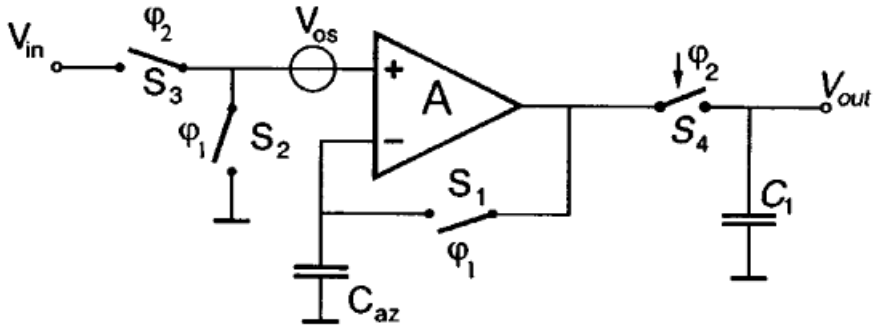

Figure 4-13: Conceptual diagram of autozero [27]

The autozero removes the offset to a good degree since the majority of the offset coming from flicker noise. The residual noise below f_s (sampling frequency) after autozero is white noise, but the level is higher than thermal noise. In another word, autozero increases baseband noise by ratio of unity-gain bandwidth (f_c) to sampling frequency (f_s) [27]. This is shown in Figure 4-14.

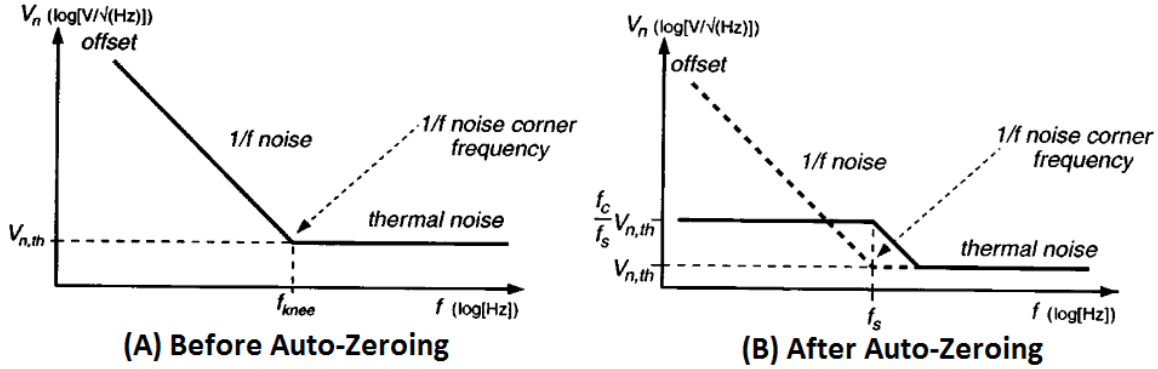

Figure 4-14: CMOS amplifier typical noise profile before and after autozero [27]

It is worth mentioning that correlated double sampling is a particular case of autozero, where sampling is done twice each period [25].

4.4.2 Chopper Technique

In this method, the input signal is modulated by chopping frequency, amplified and then demodulated (Figure 4-15). The offset is shifted over to odd harmonics, which can be removed by low-pass filter at the end. The advantage of this method compared to autozero is that it doesn't add to the baseband white noise. On the other hand, the need for low-pass filter limits the BW of the solution, which is not preferred.

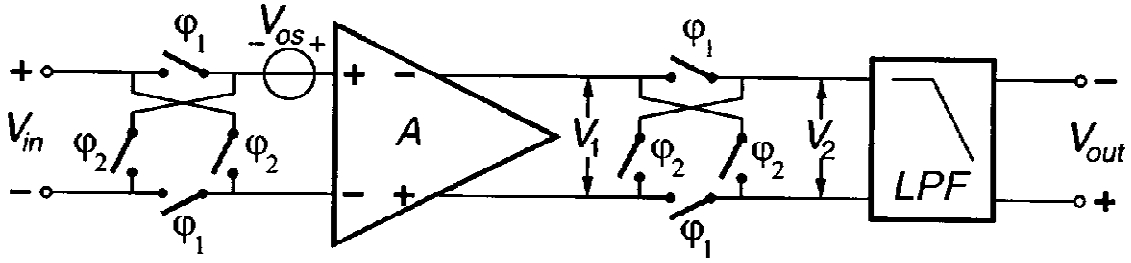

Figure 4-15: Conceptual diagram of chopper technique [27]

This technique is also known as chopper amplifier, synchronous detection, chopper-stabilized amplifier, or dynamic element matching.

Furthermore, in very noise sensitive application, such as bio-detection [26], combination of autozero and chopper technique used, so called nested loops.

4.5 Conclusions

Three major methods, voltage-mode, current-mode and CCII based, to construct instrumentation amplifier were described. Given low gain but high BW requirement for IRS, CCII based instrumentation amplifier is selected.

Input stage impact was discussed, and rail-to-rail input stage is chosen for the integrated implementation of IA.

For noise and offset cancelation, a nested loop is preferred, if static current measurement is sufficient, although to study dynamic behaviors, chopper techniques can't be used due to low pass filter stage.

Chapter 5 Integrated Implementation of IRS

5.1 Design Targets

In order to design the integrated version of the current sensor a sets of design targets need to be developed. Table 5-1 provides an empirical guideline. Note must be taken these values can easily change and could differ system to system. Given data measured using discrete implementation in chapter 3 and V_{out} range, a target gain of about 10~30 is sufficient to cover V_p and V_d in most cases. Note must be taken that in power aware chip designs the IR drop is minimized to reduce power loss as such a 100mV loss across die generally can cause other issues (10% voltage drop given VDDC range), yet it is possible. In case of substrate, higher gain 100 to 200 is required. The lower drop across flip-chip substrate is realized when surface current transfer is minimized or eliminated by having BGA solder balls for main power rails right under solder bumps (see Figure 1-1). This is also apparent by measurement provided in chapter 3. The minimum voltage drop is normally defined by idle condition of IC under test, when lowest load is expected.

Symbol	Description	MIN	TYP	MAX	Unit
VDDC	Core logic voltage, applicable to 40nm to 28nm process nodes. This sets common mode voltage range (V_{CM})	0.75	0.9	1.05	V
VDD	Supply voltage for the amplifier design		1.8		V
V_{out}	Output Voltage range of amplifier	0		1	V
V_s	Voltage drop across inherent resistance of substrate in flip-chip case	0.1		2	mV
V_d	Voltage drop across silicon die (die IR drop)	1	50	100	mV
V_p	Voltage drop across PCB power planes	1	30	100	mV

Table 5-1: Input and output targets for integrated circuit of IRS

In order to define the required accuracy, first the next stage after current sensor must be selected. In case of analog to digital convertor, a 10-bit ADC is feasible as such 1mV output accuracy is sufficient, where it would yield no more than 1 LSB error.

5.2 Conceptual Block Diagram

Figure 5-1 is the conceptual block diagram of the integrated current sensor. The primary block is the instrumentation amplifier, which is constructed using two current conveyors. The bias circuit may have auto calibration built into it to compensate for process variation. Such a block is usually a common macro within SoCs, and since it is not topic of this work, it is considered already designed circuit. However, during analysis of IA effect of the biasing are evaluated, and dependencies are highlighted.

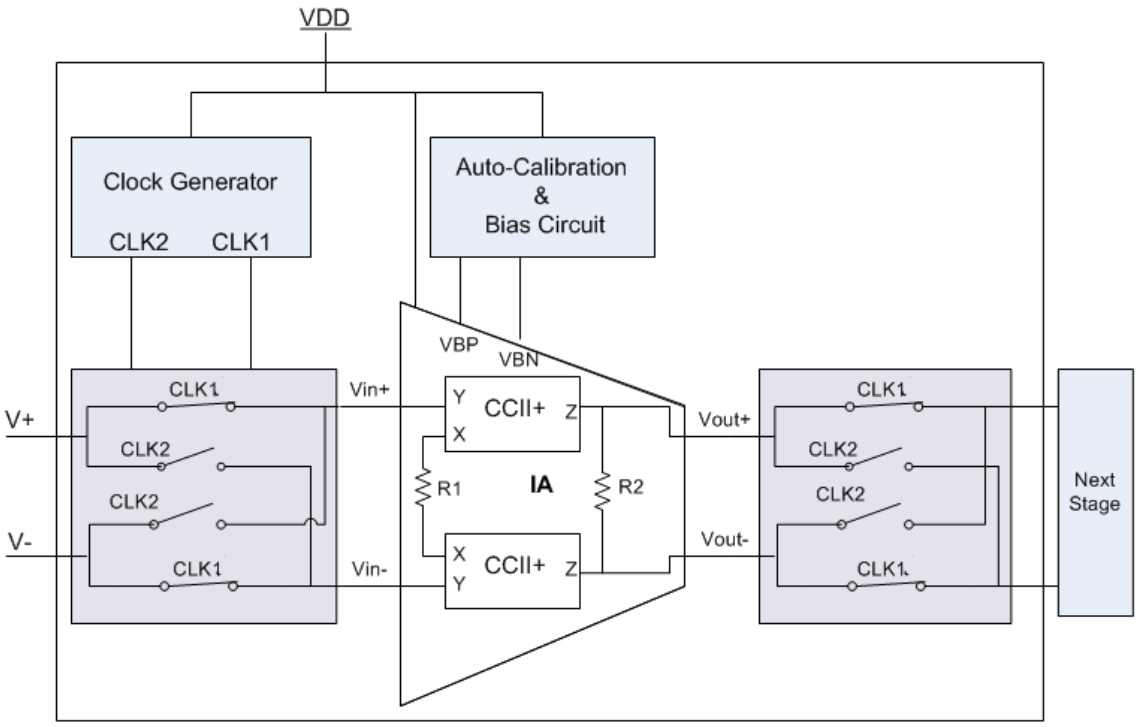

Figure 5-1: Conceptual Block Diagram for Integrated Implementation of IRS

The clock generator block is to generate two sources of clocks with same frequency and adequate phase shift for autozero. It is to remove flicker noise and reduce the amplifier output offset. The input to IRS (V+ and V-) can be connected to anywhere on the power delivery path that meets design targets.

In large systems, a switch-bar can be inserted to select more than two points. Figure 5-2 illustrates a conceptual diagram, where VDDC is supplying various clouds of logic and multiple spots for sampling the voltage. The *Y* input port of current conveyers are gate of MOSFETS as such there is little loading effect if any. This allows connection even to sensitive rails. Furthermore, since the *X* and *Z* terminals both are operating in current mode, which makes them less susceptible to surrounding circuit noise. This allows to place the two current conveyers some distance away either from each other or from the next stage, where needed.

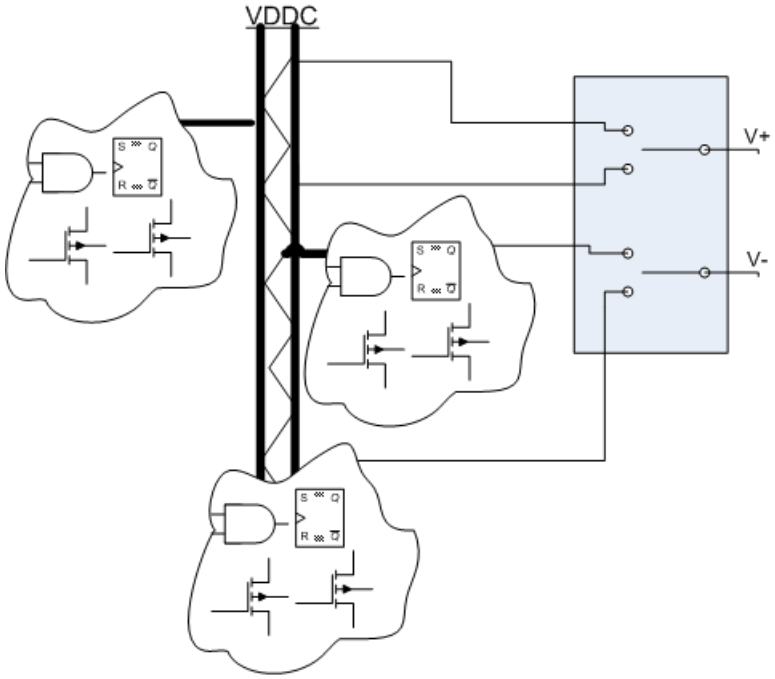

Figure 5-2: Conceptual view of VDDC power path and monitoring points

The next stage can be an analog to digital convertor with sample and hold, or other means of control systems as application may require.

Since IRS is intended for CPUs and GPUs, it must operate with a positive low voltage like 1.8V. It is expected that this value will be further reduced (potentially to 1.5V) in lower geometries (20nm or beyond). It would require a rail-to-rail input and output stage.

5.3 Rail-to-Rail CCII Schematic Cell View (ccii_r2r)

Figure 5-3 illustrates schematic for cell view (ccii_r2r) implemented in Virtuoso Cadence design tools. Y_{in}, X_{in}, and Z_{out} are the CCII ports (see section 4.3.1 for details). VBN and VBP are bias voltages to set tail currents. VDD and gnd are the supply voltage and circuit ground (return path) accordingly.

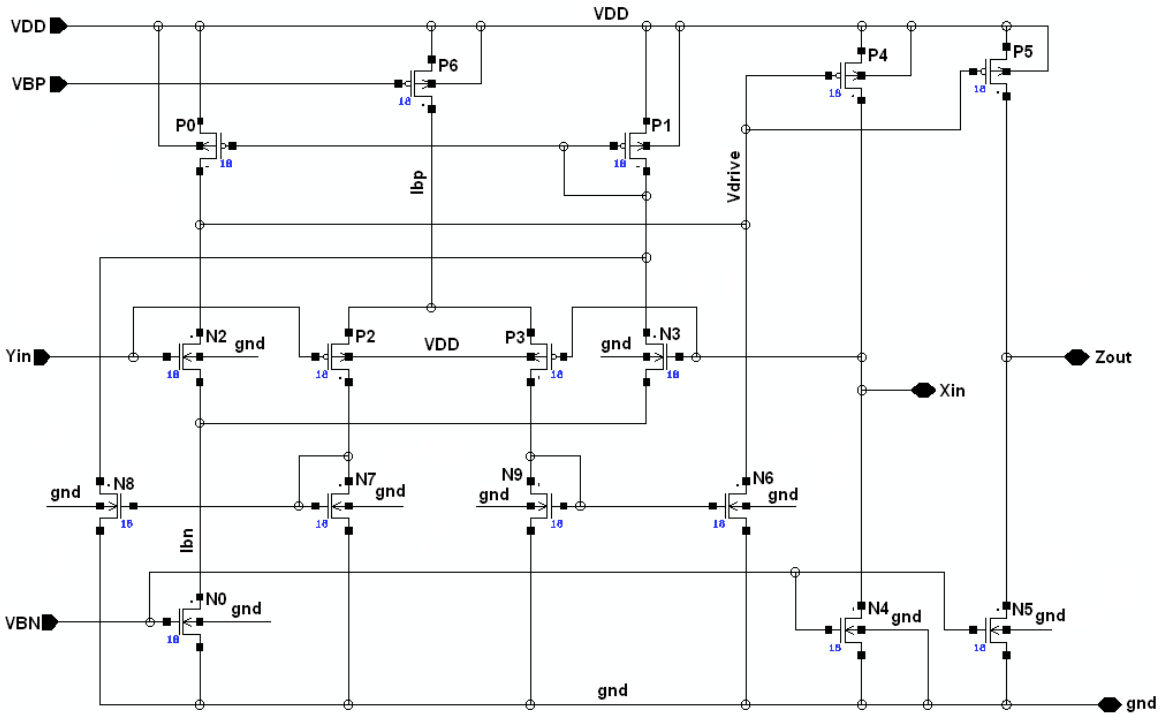

Figure 5-3: Schematic Cell View of rail-to-rail CCII (ccii_r2r)

$P2, P3$ and $N2, N3$ are forming rail-to-rail input stage as described in section 0. $N0$ and $P0$ are setting the tail current for each of input NMOS and PMOS pairs. $N6$ to $N9$ are to sum up drain currents induced by each input pairs. Ultimately, the current at node X_{in} is conveyed to Z_{out} via $P5, N5$. Table 5-2 lists suggested transistor sizes based on 1.8V device library from TSMC for 32nm node. All transistors W/L ratios are parameterized to allow DC sweep in higher level of abstraction. Estimated area is about $54\mu m^2$.

MOSFET	$\left(\frac{W}{L}\right)$ Ratio	Parameter	Values
$N0$	$\left(\frac{2}{1}\right) N0W$	$N0W$	5
$N2, N3$	$\left(\frac{2}{1}\right) N2W$	$N2W$	37
$N4$	$\left(\frac{2}{1}\right) N4W$	$N4W$	36
$N5$	$\left(\frac{2}{1}\right) N5W$	$N5W$	73
$N6, N7, N8, N9$	$\left(\frac{2}{1}\right) N6W$	$N6W$	5
$P0, P1$	$\left(\frac{2}{1}\right) P1W$	$P1W$	11
$P2, P3$	$\left(\frac{2}{1}\right) P2W$	$P2W$	47
$P4$	$\left(\frac{2}{1}\right) P4W$	$P4W$	61
$P5$	$\left(\frac{2}{1}\right) P5W$	$P5W$	117
$P6$	$\left(\frac{2}{1}\right) P6W$	$P6W$	11

Table 5-2: Suggested transistor sizing for Figure 5-3

5.4 Instrumentation Amplifier Schematic Cell View (ia_r2r)

Figure 5-4 is the schematic cell view of the target instrumentation amplifier constructed using two CCII blocks ($I2$ and $I3$ instances of ccii_r2r) as was described in section 4.3.2. VDD_18 is to provide supply voltage, while VP_BIAS and VN_BIAS setting VBP and VBN for CCII blocks. The $I1$ opamp is an ideal opamp for simulation purpose only and not part of the design. The differential output nodes are labeled as $zout\_p$ (positive node) and $zout\_n$ (negative node).

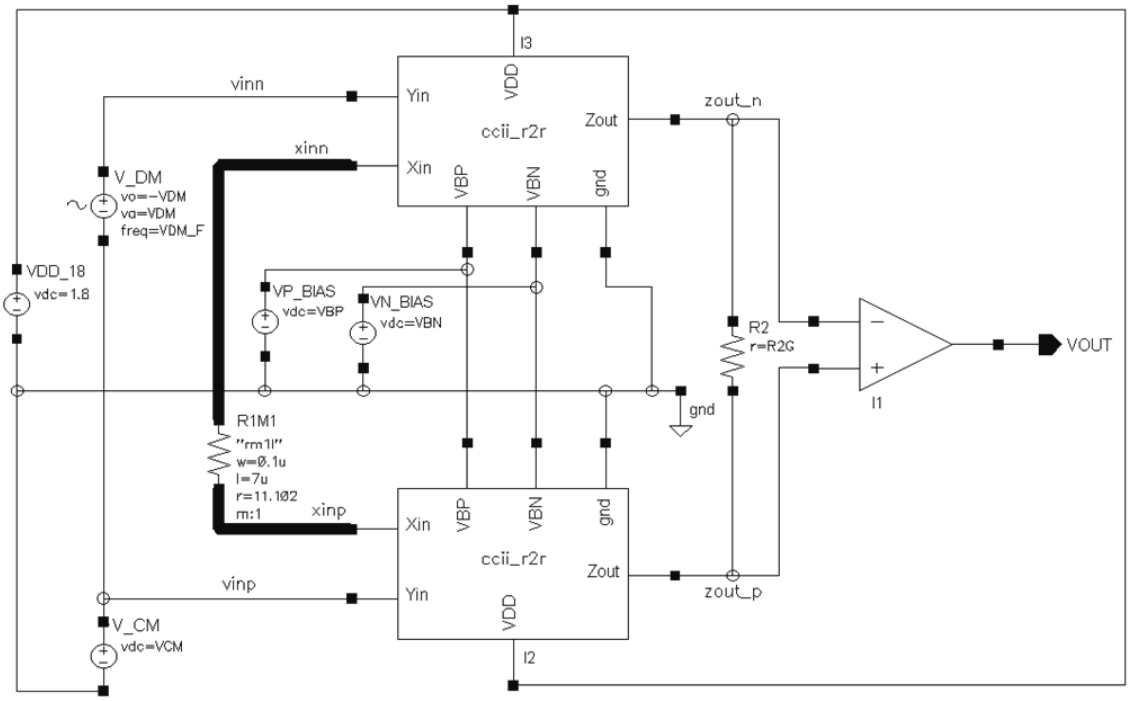

Figure 5-4: Schematic Cell View of the instrumentation amplifier (ia_r2r)

$vinn$ and $vinp$ nets are input nodes of the instrumentation amplifier. Since it is meant to measure voltage drop across power path, the positive input node must be connected to location closer to the supply, and the negative node connected to closet point to the load. In simulation, IR drop is realized by a common mode voltage, V_CM source, and a differential mode voltage, V_DM source. The frequency of VD_M source is to simulate load current variation. In this study, sinusoidal input source is used throughout the simulation. Thus, pulse response may also be useful, but not covered here. The common mode voltage is indicated by VCM and differential voltage, the voltage drop, is referred to as VDM in this work. All sources are parameterized to allow voltage sweep in simulation stage.

$R2$ and $R1M1$ are to adjust the instrumentation amplifier gain. $R2$ can be a poly-type resistor or an external one pending SoC resources and limitations. The overall gain is proportional to the ratio of $R2/R1M1$, thus to implement analog temperature compensation described in section 2.2.1, $R1M1$ must be with same thermal coefficient as the inherent resistant material. For that reason, it is shown as a resistor generated on

metal layer ($M1$). $M1$ is normally used to power core devices. Per section 3.2, numerical compensation is as effective as analog method, pending SOC resources such as on-die temperature sensor; therefore, $R1M1$ can be any kind of resistor. Increasing $R2$ alone doesn't increase the gain indefinitely, it is proven by sweep of $R2$ later in this chapter, as such decreasing $R1M1$ substantially is required to yield gain in order of 100. As such, in the simulation $R1M1$ is reduced to ~5Ohm to achieve gain of 100 for moderate value of $R2$. Such resistor can be realized as wire resistance in metal layer. This enables circuit designer to use same macro to achieve a variable gain. It can be achieved via dynamically changing $R2$. There are different methods to do it such as switching in/out several weighted poly-type resistors [23]. In this work, $N4$ and $P4$ are sized to about half of output stage $N5$ and $P5$ (see Table 5-2) to further increase the gain. This technique, in junction with very low resistance at $R1M1$ location allow achieving higher gain up to 100, which differentiate this work compared to [6] and [9].

5.5 Simulation Results

The circuit in Figure 5-4 was simulated and the result is reviewed in this section. The output voltage is referred to as $delta\_VZout$ or $VZout$ in the graphs and the text indicating the differential output ($Vzout\_p - Vzout\_n$). Similarly, the differential input ($vinn - vinp$) voltage is referred to as $delta\_Vin$ (Vdm or VDM). As described in section 5.1, potentially two different amplification gain may be needed pending the usage. Therefore, circuit is evaluated under two different gains, one ~30 as "low gain" and ~100 as "high gain". Where noticeable result is found, both results are presented and compared to each other.

5.5.1 Transient Response

The transient response of the circuit is plotted in Figure 5-5 for $VCM = 900\text{mV}$, $VDM = 1\text{mV}$ and gain of 30 at 50MHz. The power consumption of the amplifier is about 10.7mW @ 1.8V supply. Given the application target is for high power GPUs and CPUs, it is negligible. Hence, it can be reduced by converting the output stage to an AB type.

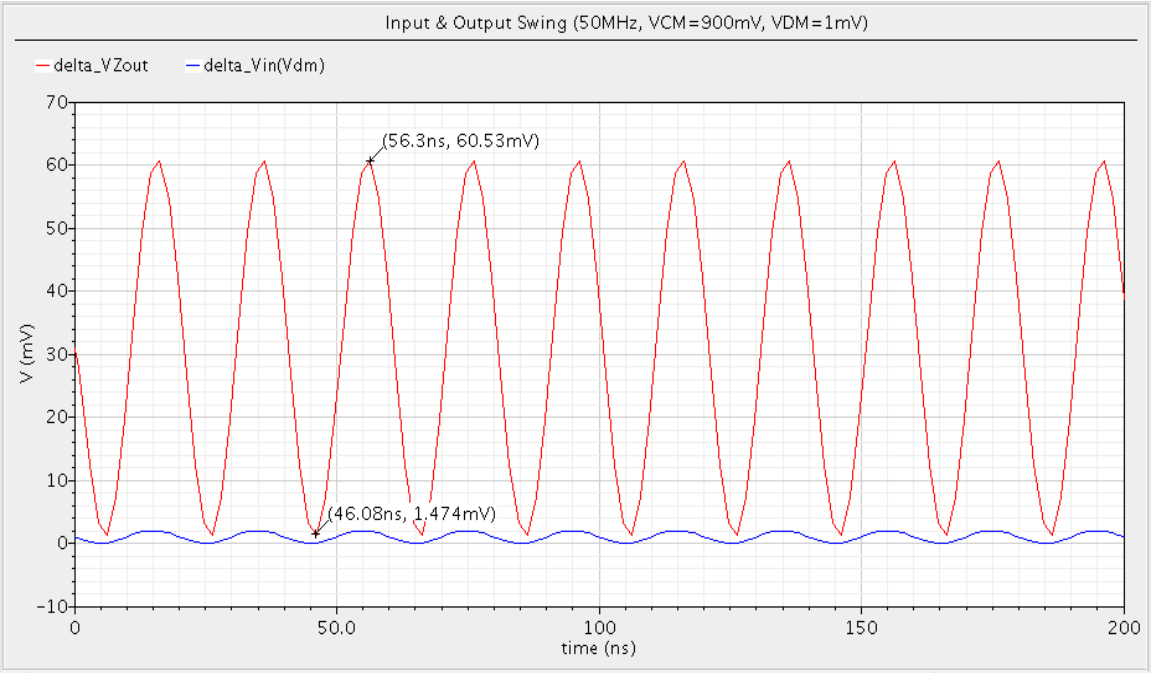

Figure 5-5: Transient response of the IA

5.5.2 Differential Mode Voltage (VDM) Sweep

The circuit performance, output voltage and current, was evaluated under input voltage range of 0.1mV to 5mV, and the results illustrated in Figure 5-6, Figure 5-7, Figure 5-8, and Figure 5-9.

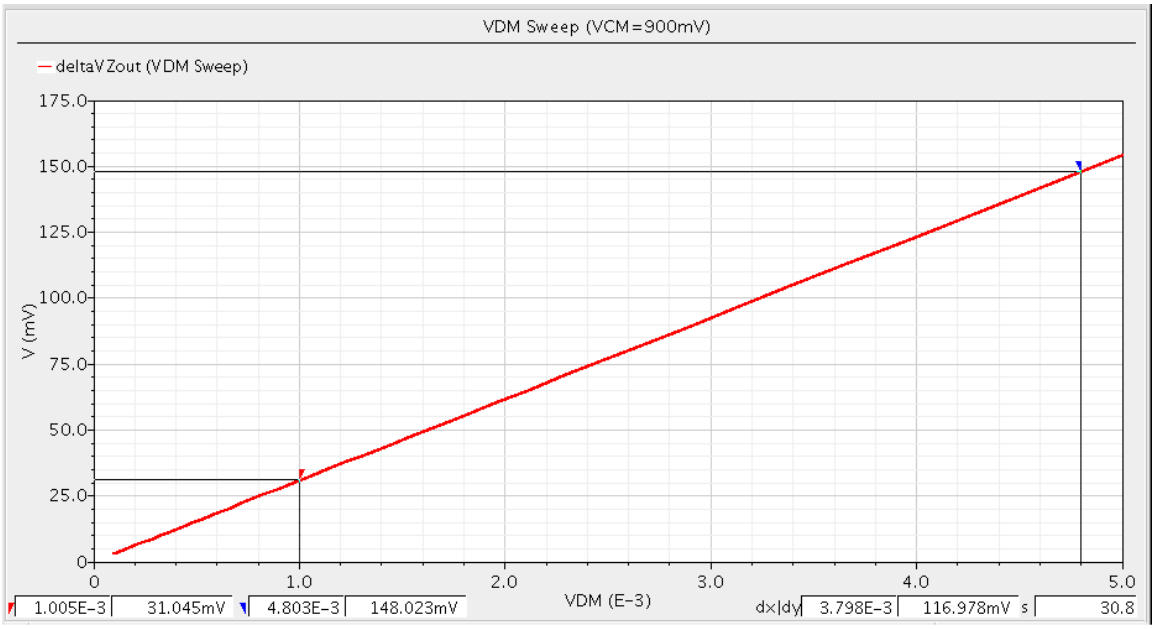

Figure 5-6: Output Voltage vs. VDM @ Gain=30

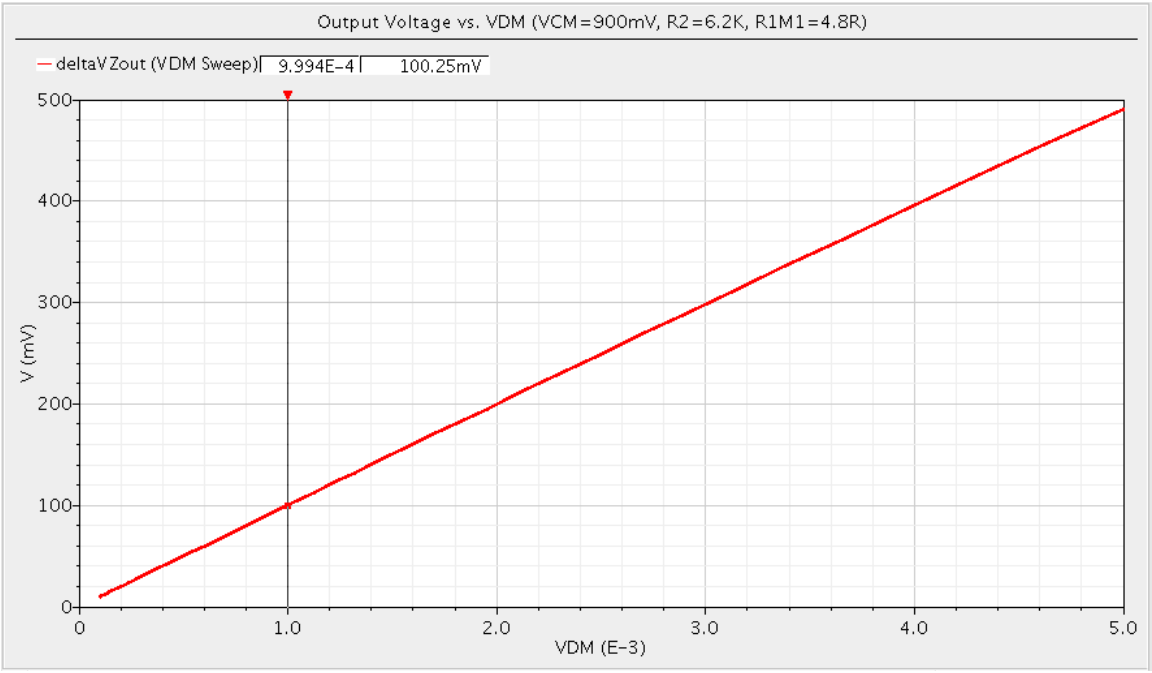

Figure 5-7: Output Voltage vs. VDM @ Gain=100

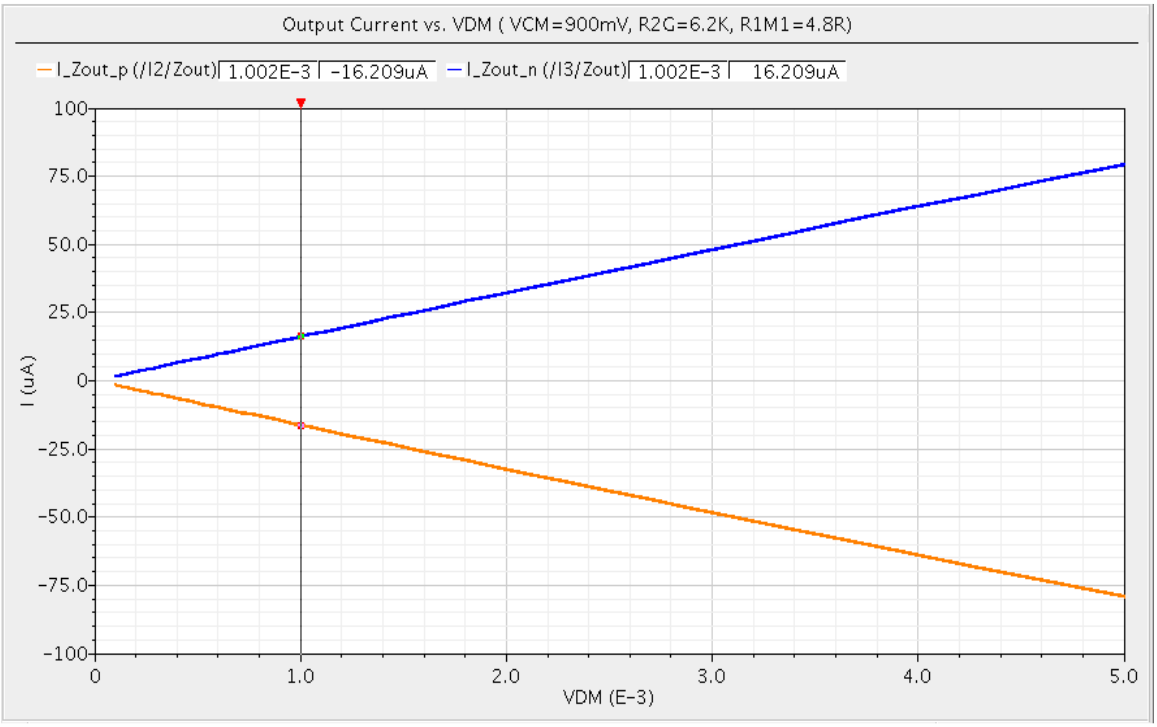

Figure 5-8: Output Current vs. VDM @ Gain=100

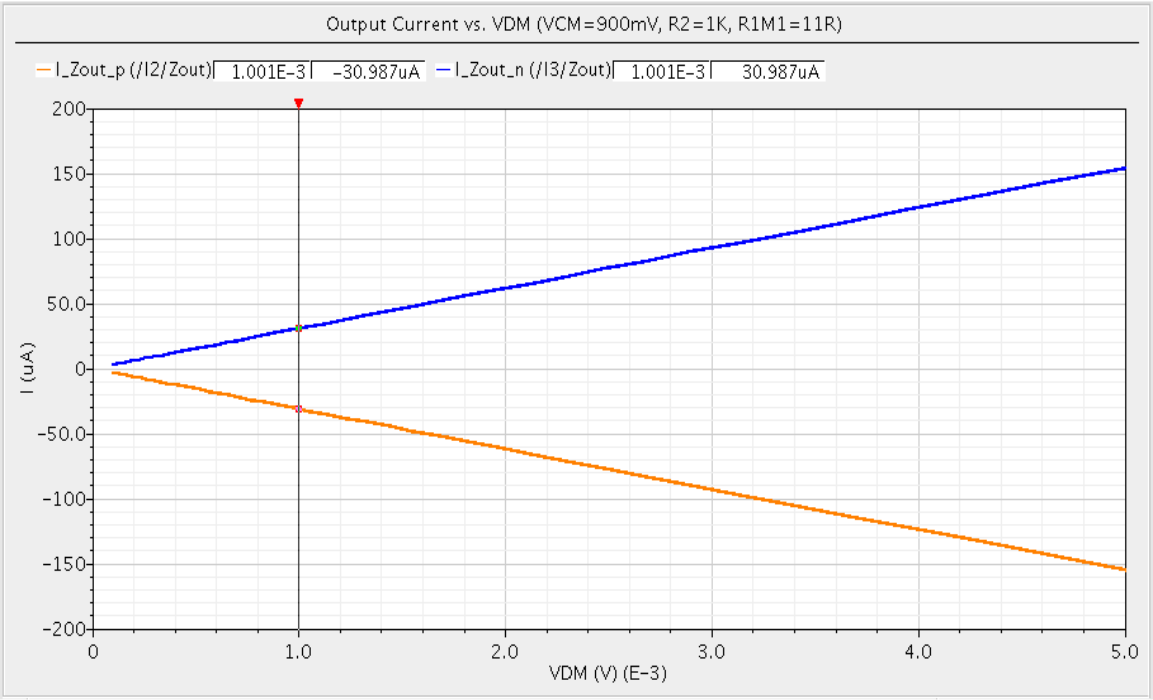

Figure 5-9: Output Current vs. VDM @ Gain=30

Figure 5-10 illustrates gain versus differential input voltage at high gain setting (100). The delta cursor is set to measure the gain error. The result is 0.324%/mV. Similarly, the gain error for low gain condition (~30) was extracted from Figure 5-11, and the result is 0.032%/mV, which is nearly 10 times less. Despite both numbers are very small and negligible, but it indicates that the lowest appropriate gain must be selected to reduce the circuit gain inaccuracy, wherever possible.

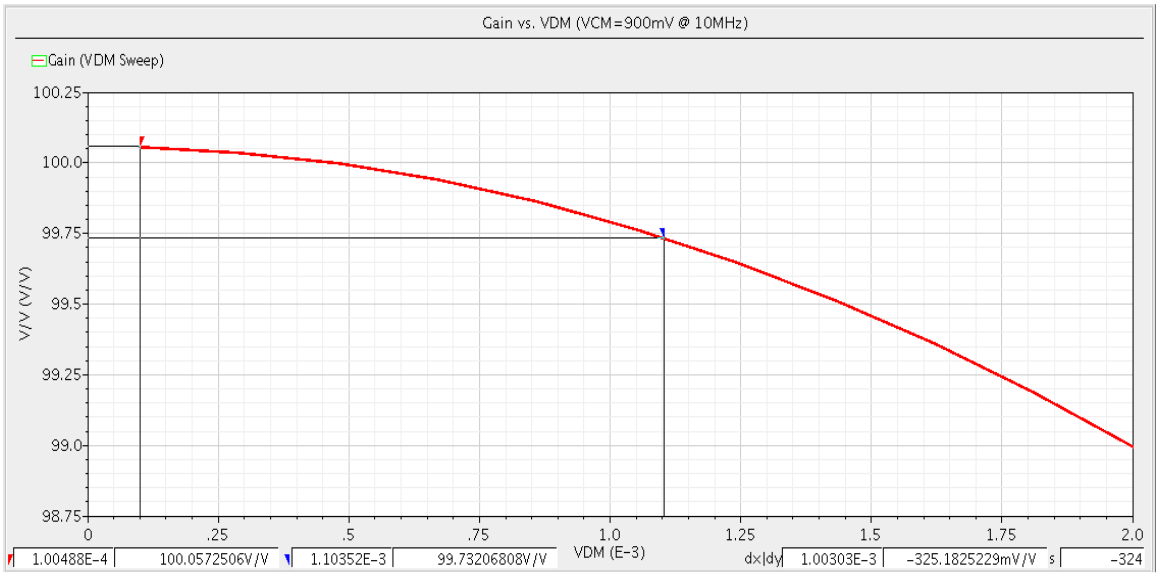

Figure 5-10: Gain vs. VDM at 10MHz with gain 100

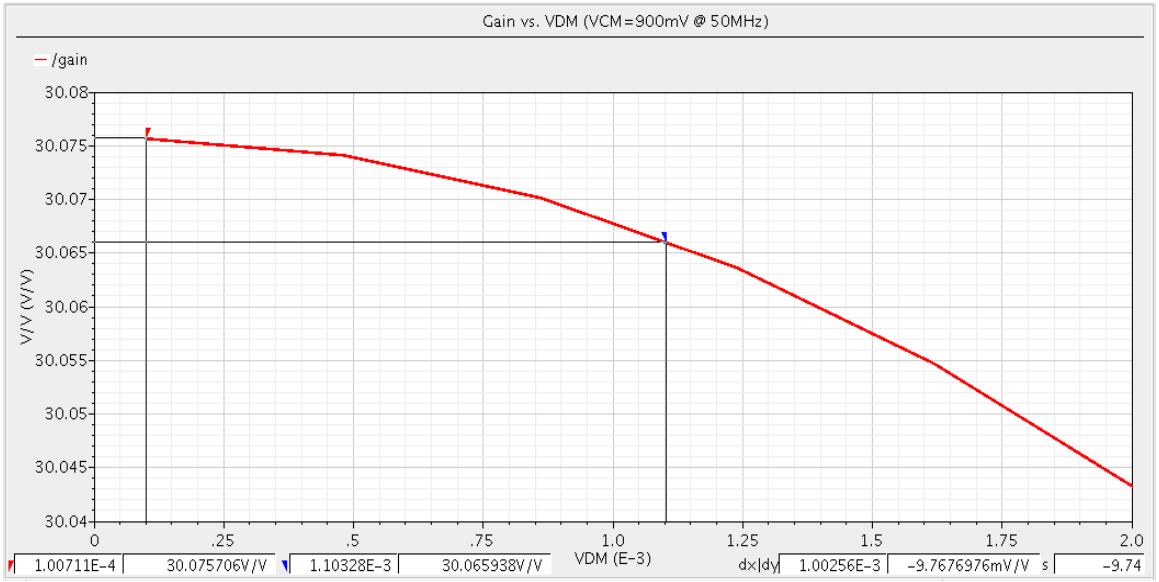

Figure 5-11: Gain vs. VDM at 10MHz with gain 30

5.5.3 Common Mode Voltage (VCM) Sweep

As described, the common mode voltage dependency of the gain is a concern. Rail-to-rail input stage was used to reduce such a dependency. Figure 5-12 illustrates VCM effect on output voltage for a target differential voltage gain of 31 @ 900mV (29.8dB). Delta-cursors are set on the minimum and maximum output voltages, which show an output voltage variation of 685uV (2.21%) over VCM range and worst case differential gain of 30.15. It shows a worst case common mode gain of $3.46e-3$ over VCM range and. Given CMRR definition, see Equation (4-1), it yields CMRR of 78.8dB @ 50MHz, which is attractive given the frequency point.

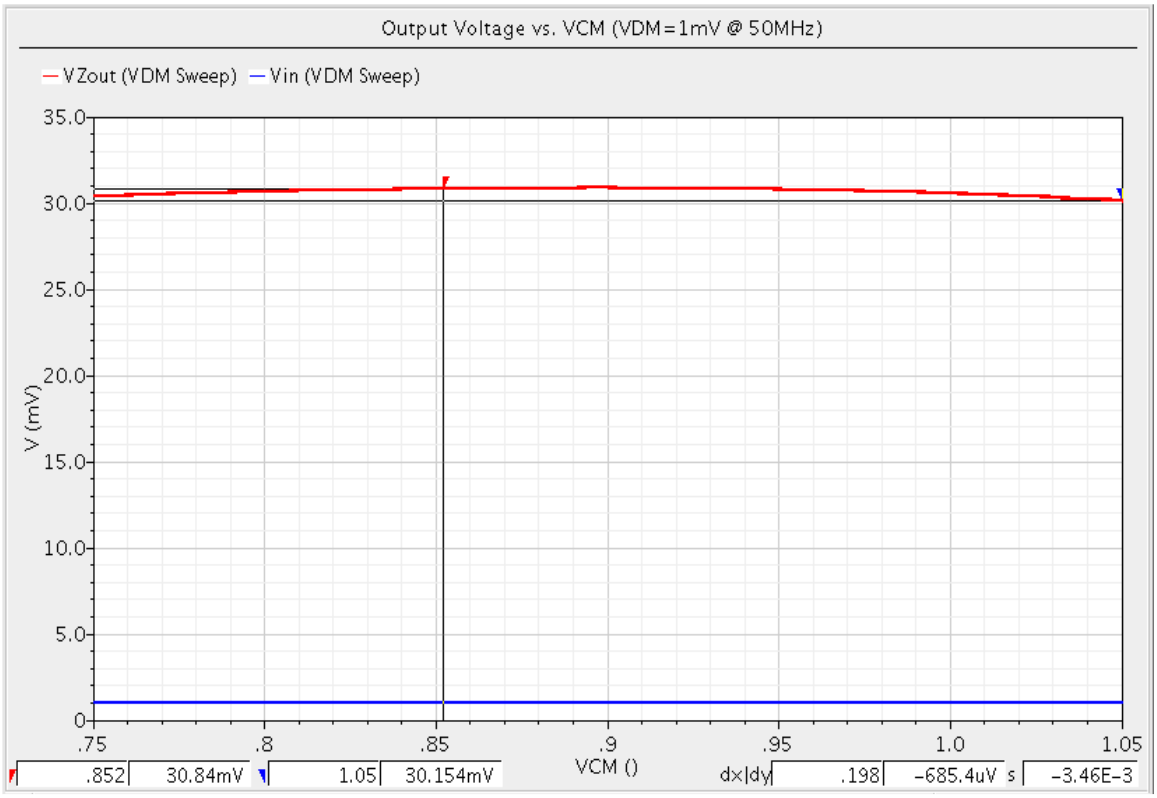

Figure 5-12: Output Voltage vs. VCM @ Gain=30, 50MHz

It must be noted that increasing the gain by only changing $R1M1$ and $R2$, can impact CMRR. This matter is shown in Figure 5-13, where can look up a worst case variation of 3.794mV for 150mV change in VCM (A_{CM} of 0.0253) with worst case differential gain (A_{DM}) of 96. It yields a CMRR of 71.5dB @ 10MHz. It indicates that if higher gain is needed it may require a piecewise linear look up table for the gain correction factor. This is practical in current sensing application target of this work, since the common mode voltage is the logic core voltage as described in section 5.1, and many other actions such as clock frequency change must be done prior to increase or decrease of core voltage. As such, gain correction factor can be applied via a change in the circuit gain, bias or in a form of numerical post measurement calculation.

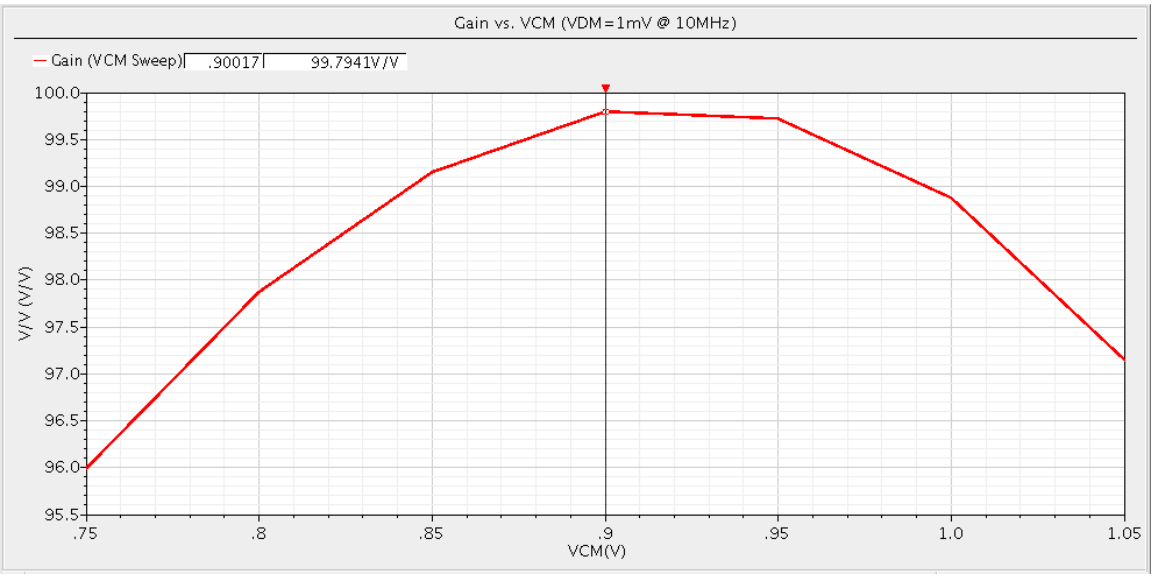

Figure 5-13: Gain vs. VCM @ Gain=100, 10MHz

5.5.4 Gain Resistor (R2) Sweep

Figure 5-14 plots output voltage versus gain resistor $R2$. The marker shows the circuit setting (see Figure 5-15 for zoomed in version). It clearly shows for this given circuit, increasing $R2$ will increase the gain, although not indefinitely. It is due to output impedance of the amplifier.

On the other hand, the nonlinear behavior, points that the gain accuracy will substantially be dependent upon accuracy of $R2$. Therefore, if a poly-type resistor is used, which expected to have considerable process and fabrication variations, it is recommended to implement an auto-calibration mechanism to trim the gain (see Figure 5-1).

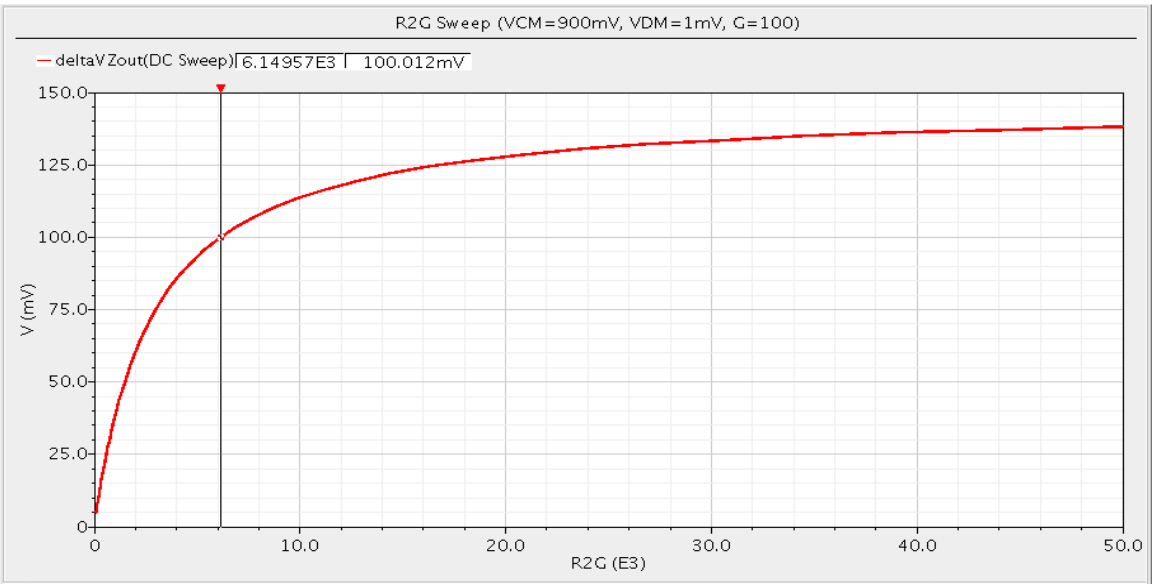

Figure 5-14: Output Voltage vs. Gain Resistor (R2)

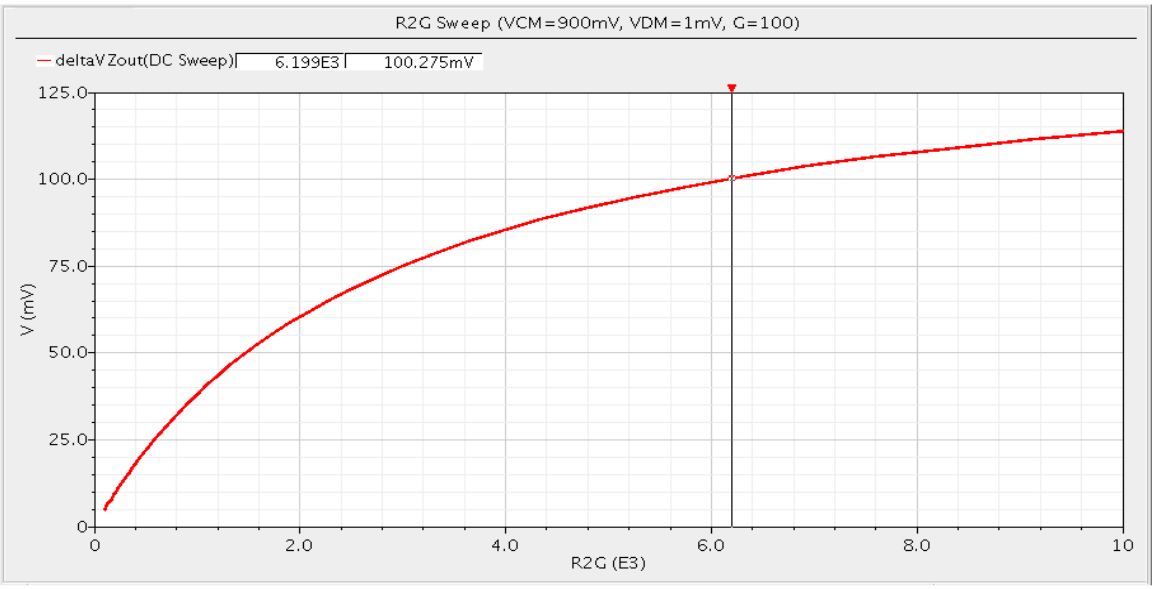

Figure 5-15: Output Voltage vs. Gain Resistor (R2) – Zoomed in

5.5.5 Bias Voltage Sweep

Figure 5-16 and Figure 5-17 illustrate DC sweep of VBP and VBN voltages respectively. Change in VBP has less effect on the gain. It is set in the middle of range allowing for fine adjustment of the gain if need be. On the other hand, VBN variation impacts the gain considerably. As specified in section 5.2, the bias voltages are expected to be generated via a band-gap based circuit, which must provide adequate stability.

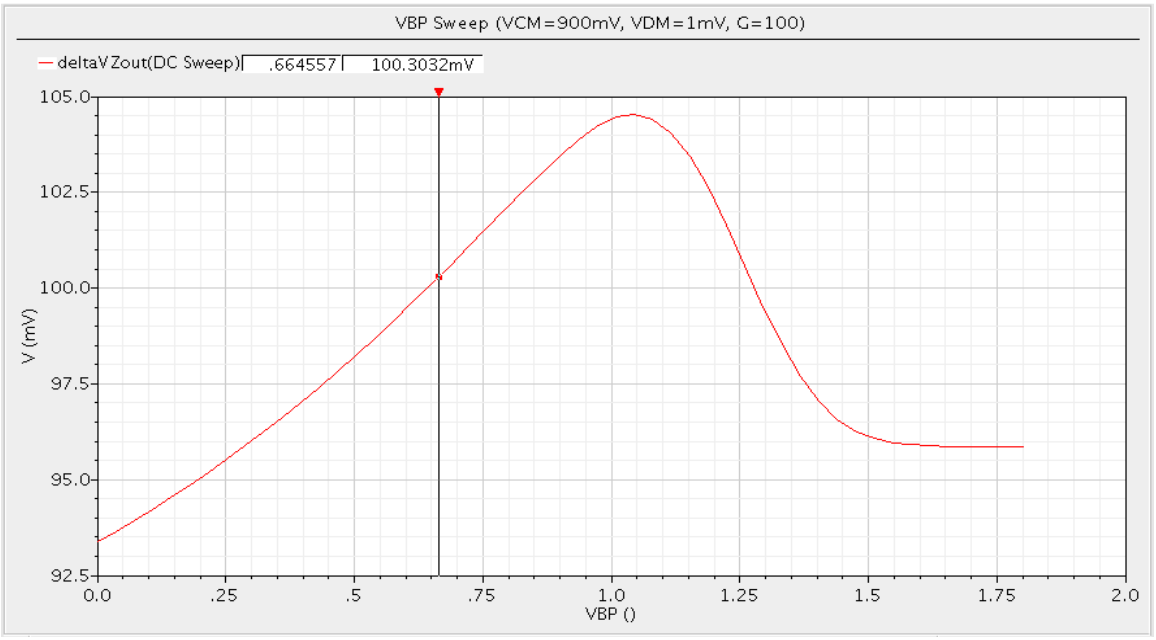

Figure 5-16: PMOS Bias (VBP) Sweep

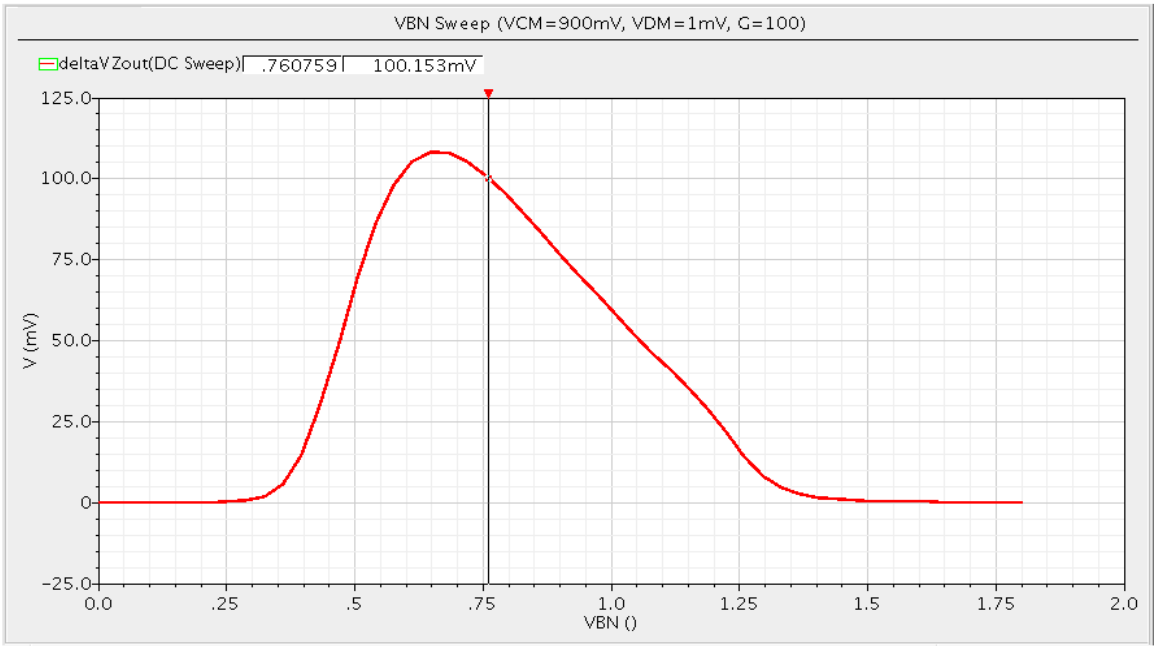

Figure 5-17: NMOS Bias (VBN) Sweep

5.5.6 Temperature Sweep

The actual operating condition of GPUs is in the range of 47℃ to 107℃ given most computers are used at room temperature. Thus to evaluate the circuit behavior and to optimize its accuracy, the nominal temperature in all simulation was set to 77℃ . Here, Figure 5-18, is the temperature sweep for the entire range (0 to 125℃).

The typical gain of 100 is observed at 77℃. The amplifier overall gain has a temperature dependence of −0.25%/℃. Since the amplifier gain is inversely proportional to the temperature (negative slope), it can be used to compensate partially for the increase in the inherent resistance of the current path as described in 2.2. Yet, the temperature dependence profile is linear, thereby it simplifies the compensation method, if need be.

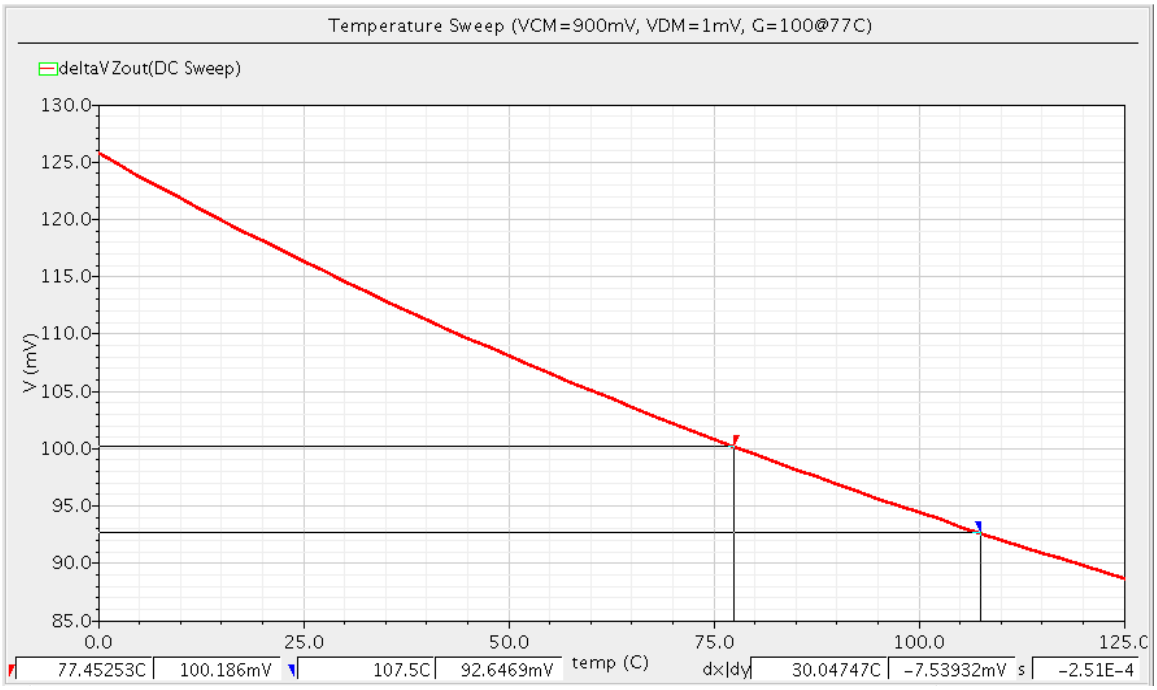

Figure 5-18: Output Voltage vs. Temperature @ Gain=100

The noise analysis is done in section 5.5.7, the temperature impact on the noise level is reviewed here just for completeness. Figure 5-19 shows the input noise, gain and output noise versus temperature. The input noise is expected to rise due to thermal noise, although since the amplifier gain is reduced at higher rate the overall output noise is reduced.

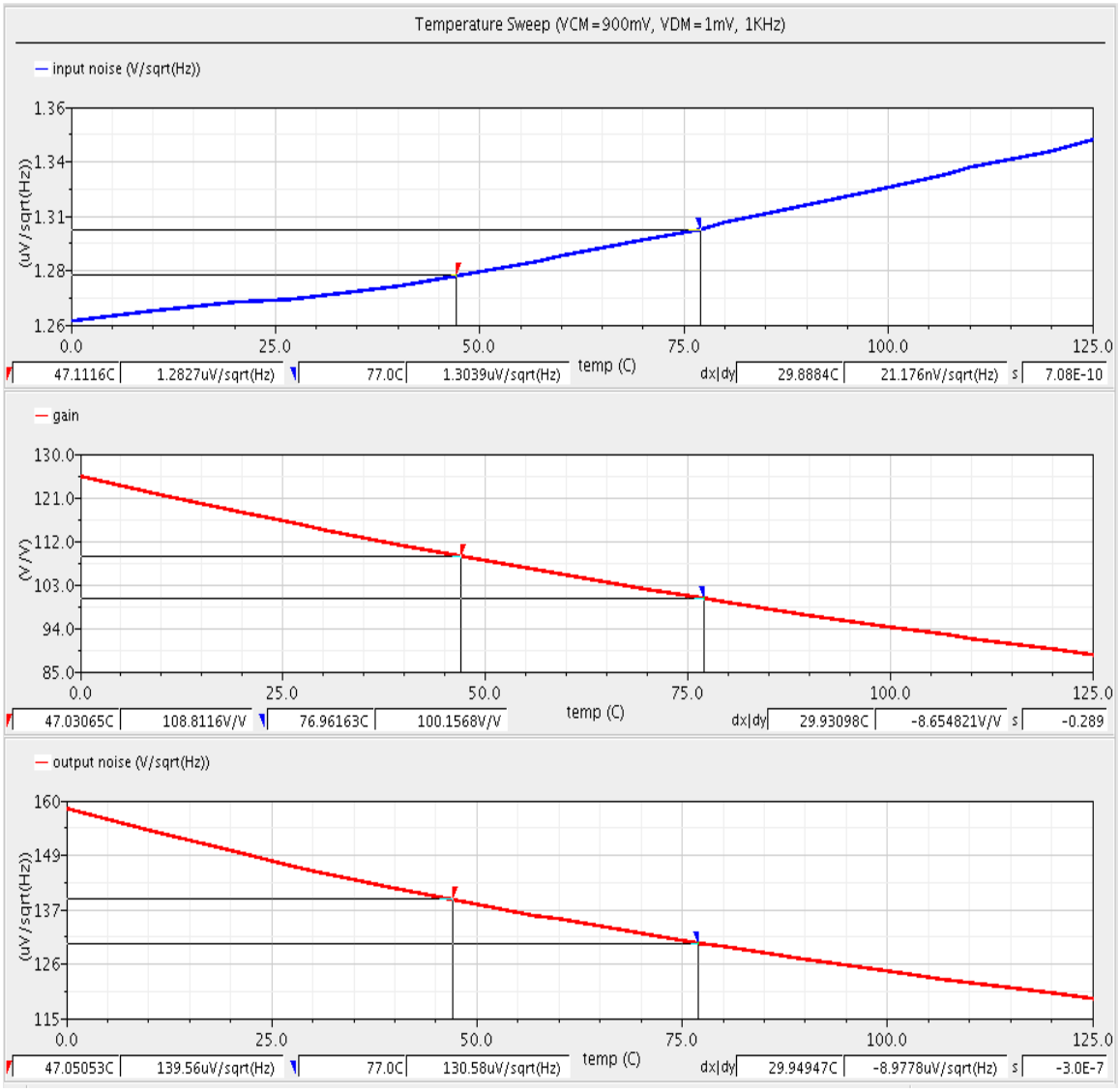

Figure 5-19: Input noise, gain and output noise at Gain=100

5.5.7 Noise Analysis

The noise analysis was performed to evaluate effect of VDM, VCM, and temperature on the output noise. The temperature effect was reviewed in section 5.5.6, which showed the gain plays the dominant role in the output noise. As such, all simulations were performed at high-gain configuration (gain of 100).

Figure 5-20 is the output noise versus frequency at VDM ranging from 0.1mV to 2mV. As expected, the flicker noise, of up to $4.4\text{mV}/\sqrt{\text{Hz}}$, is dominating at low frequencies. In case of amplifying substrate inherent resistance, this level of noise is too high. Thereby an autozero as described in chapter 4 must be implemented (see Figure 5-1). The suggested frequency of about 100KHz (marked by vertical cursor in Figure 5-20) is recommended for autozero.

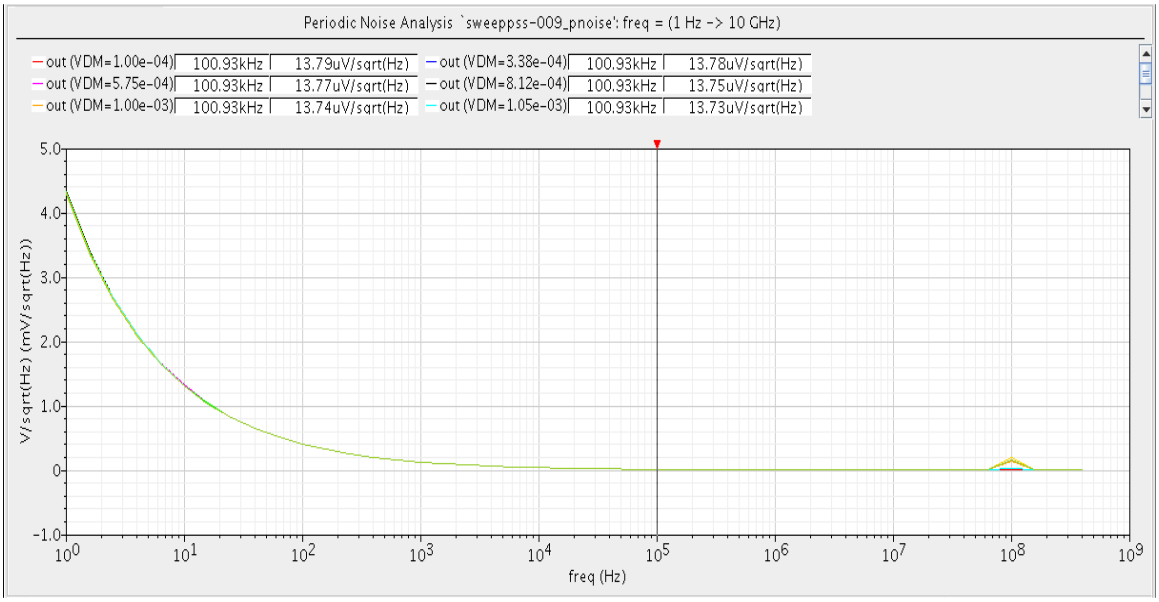

Figure 5-20: Output Noise vs. Frequency for VDM 0.1mV to 2mV

In order to evaluate the VDM effect in more details, frequency of 10MHz was chosen to be well above corner frequency while circuit can still operate at that frequency with high-gain setting (it was verified by transient response simulation). The noise analysis was then performed at 10MHz with typical gain of 100.

The input noise result versus VDM is plotted in Figure 5-21, and output noise results in Figure 5-22. The input noise linearly increases with increase in VDM with a slope of about $2.52e-9$ (1mV change induces $2.52\text{pV}/\sqrt{\text{Hz}}$ change in the input noise level). This input noise is amplified and transferred to output by the gain. However, it was indicated in section 5.5.2 that amplifier gain is dropping as VDM increasing, this behavior can also be observed in output noise. The output noise non-linearity is similar to that of gain in Figure 5-10.

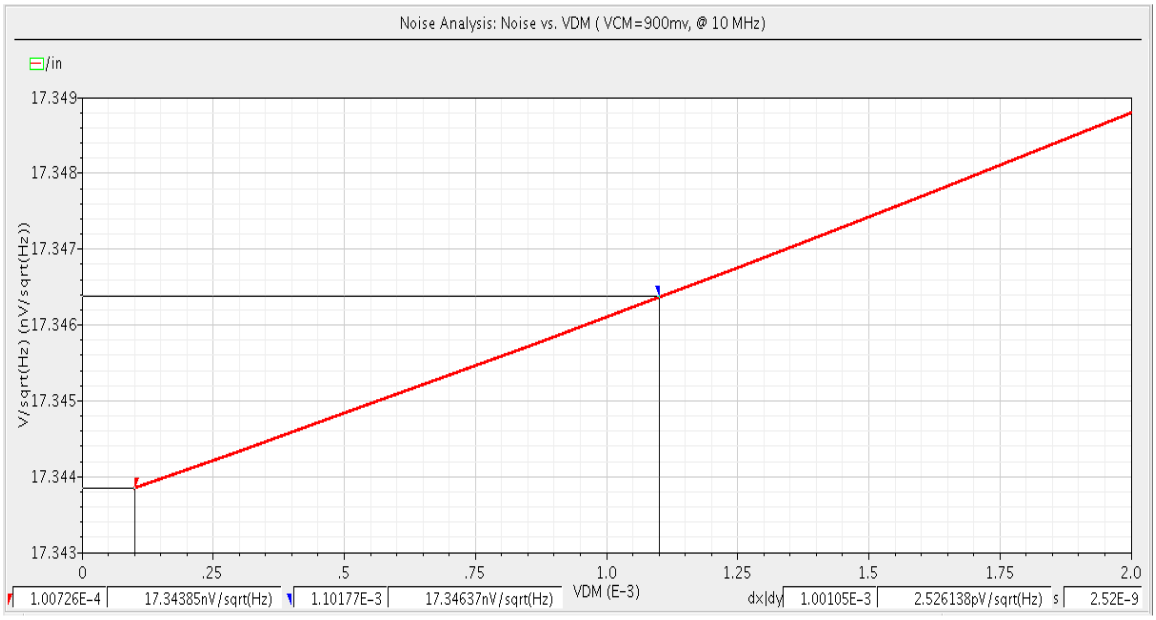

Figure 5-21: Input Noise vs. VDM at 10MHz, Gain=100

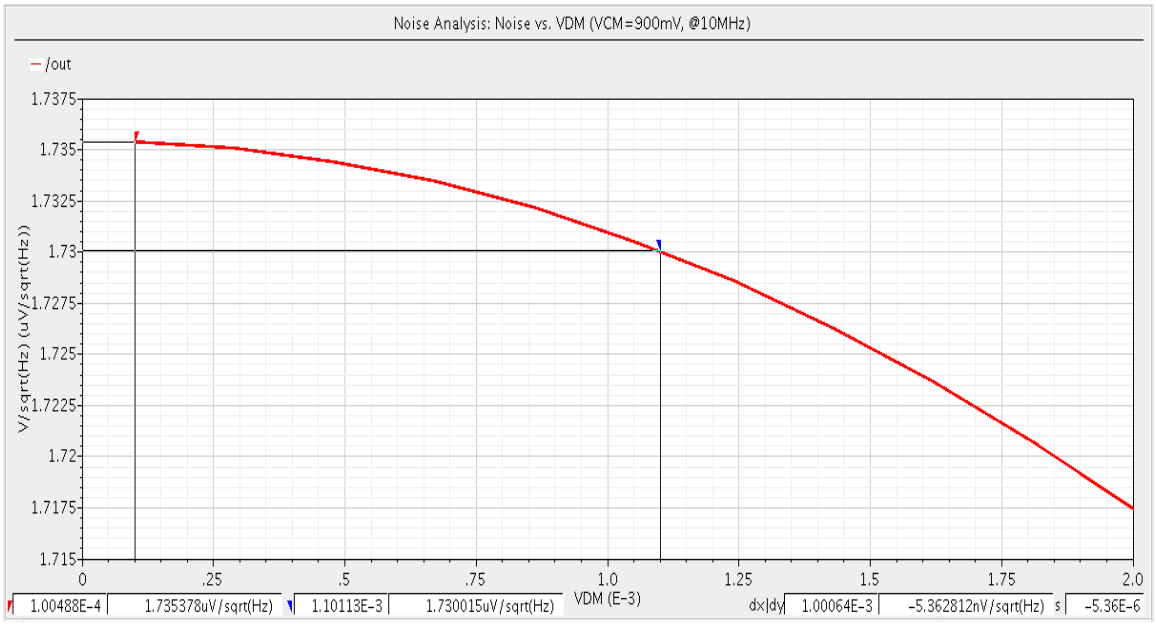

Figure 5-22: Output Noise vs. VDM at 10MHz, Gain=100

The noise analysis was repeated by keeping VDM constant at 1mV, and sweeping VCM. Figure 5-23 is the result at 1Hz. The flicker noise stands out at this frequency. The input noise is reduced as VCM is increased. The vertical marker is set on 0.9V, where is the middle point of VCM. The circuit is optimized to provide target gain of 100 at this point This will reduce the gain error to about half over VCM range. As it can be seen, the output noise remains more flat at VCM below 0.9V.

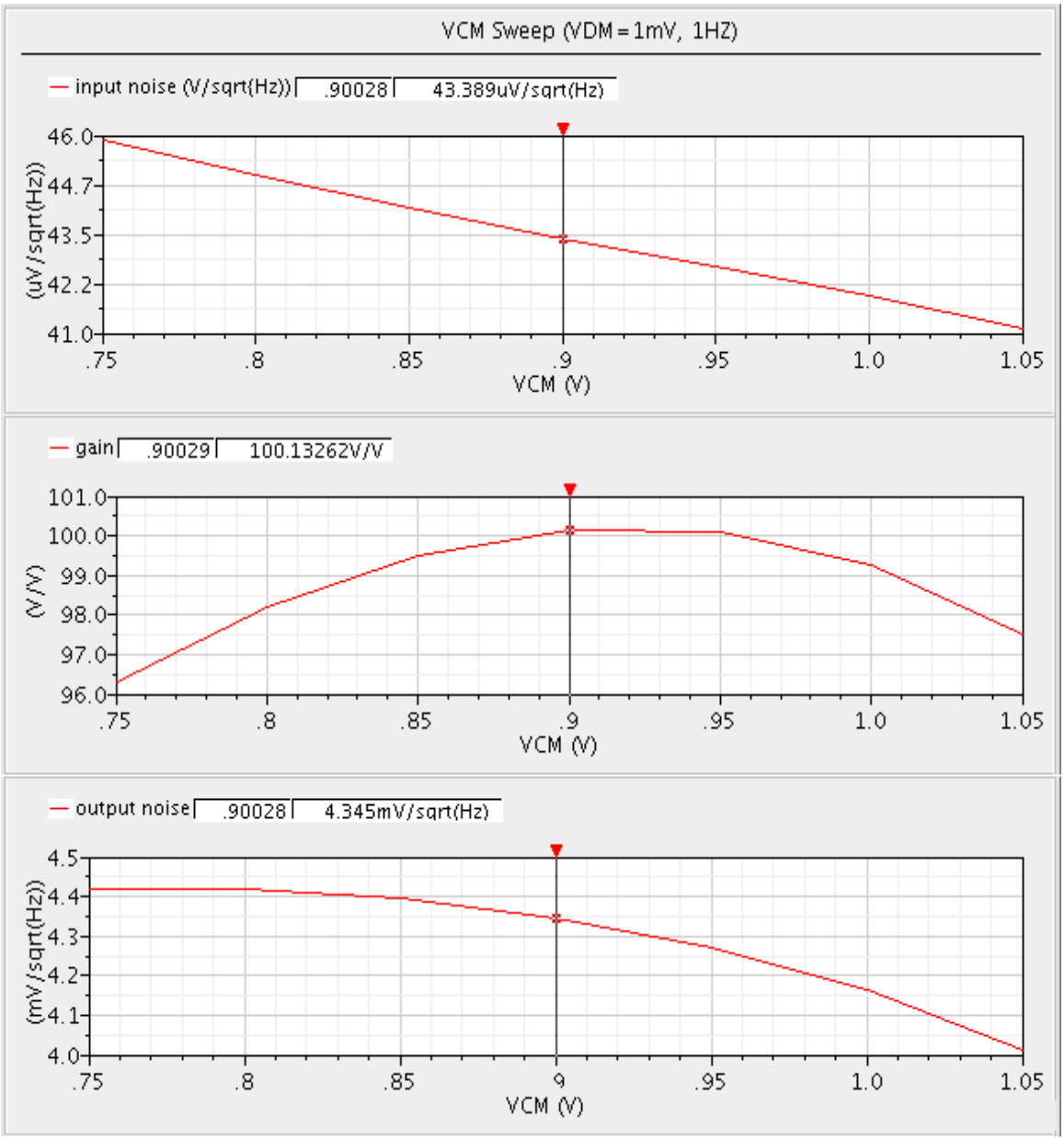

Figure 5-23: Input noise, gain and output noise vs. VCM @ 1Hz Gain=100

Figure 5-24 and Figure 5-25 show similar behaviors at 10MHz and 100MHz respectively. The noticeable differences are that flicker noise is no longer prominent, and the amplifier gain has considerably dropt at 100MHz. This was also observed in section 5.5.3.

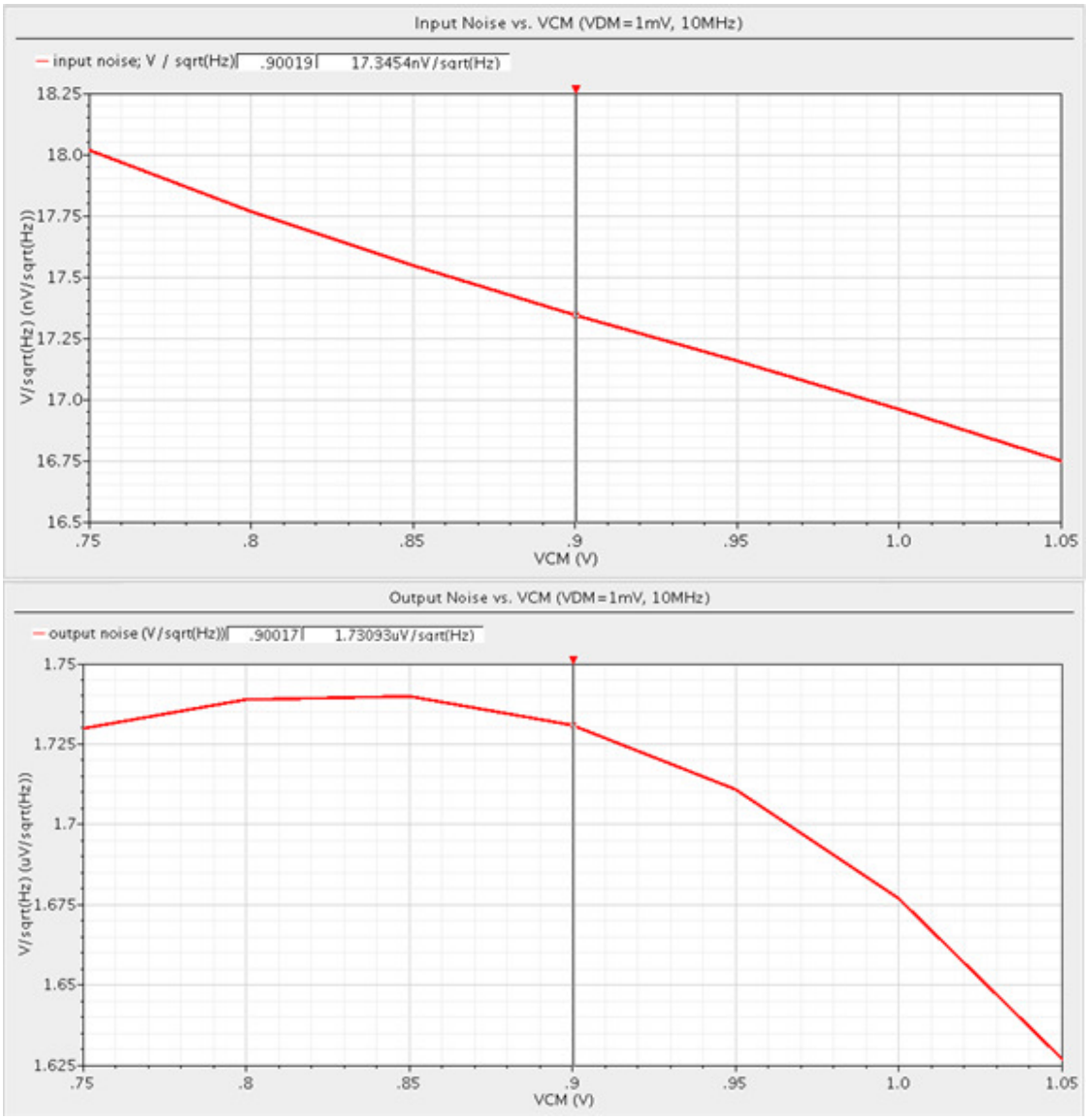

Figure 5-24: Input and output noise vs. VCM at 10MHz, Gain=100

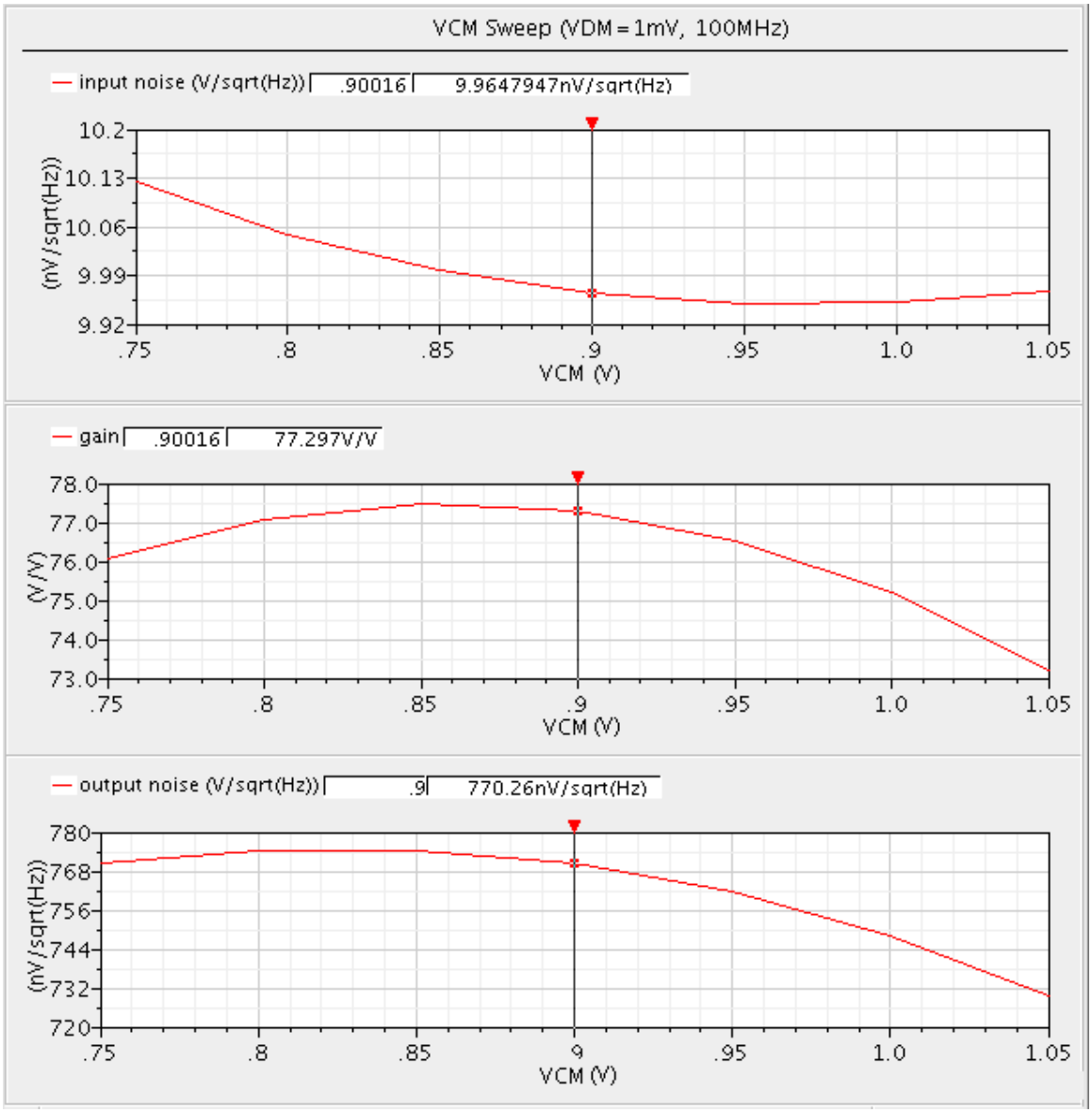

Figure 5-25: Input noise, gain and output noise vs. VCM @ 100MHz Gain=100

5.6 Conclusions

The architecture of integrated current sensor using inherent resistance was provided. A proof of concept design was presented based on the expected typical range of inputs and outputs. The design intended for low voltage VLSI systems to allow integration within large SoCs such as GPUs and CPUs. The primary block, instrumentation amplifier, was constructed using rail-to-rail current conveyer and simulated using TSMC 32nm process node. The results were analyzed and observations were provided.

The key factor in the performance of the solution was the overall necessary gain. A gain of up to 30 provided an excellent bandwidth of at least 50MHz with a gain error of only $0.032\%/\text{mV}$ over VDM and a CMRR of about 78.8dB. This gain is sufficient for on-die or PCB IR drop amplification. Although, it might not be sufficient for flip-chip substrate IR drop amplification.

Higher gain can be realized in this architecture at reduced CMRR. The circuit was simulated at a gain of 100, which resulting a CMRR of 71.5dB @ 10MHz. The gain inaccuracy is also decreased over VDM range to $0.324\%/\text{mV}$.

The flicker noise is dominant at low frequency as expected. Thus, circuitry needed for noise and offset cancellation. Increase in temperature, VDM and VCM all increased the input noise.

The temperature gain coefficient of about $-0.25\%/℃$ is observed with a linear profile. This can be used as partial compensation for inherent resistance increase over temperature.

It also demands future work to add noise and offset cancellation circuit to verify its effectiveness.

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