Integrated Circuit and Antenna Technology for Millimeter-Wave Phased Array Radio Front-End

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

Ever growing demands for higher data rate and bandwidth are pushing extremely high data rate wireless applications to millimeter-wave band (30-300GHz), where sufficient bandwidth is available and high data rate wireless can be achieved without using complex modulation schemes. In addition to the communication applications, millimeter-wave band has enabled novel short range and long range radar sensors for automotive as well as high resolution imaging systems for medical and security. Small size, high gain antennas, unlicensed and worldwide availability of released bands for communication and a number of other applications are other advantages of the millimeter-wave band. The major obstacle for the wide deployment of commercial wireless and radar systems in this frequency range is the high cost and bulky nature of existing GaAs- and InP-based solutions. In recent years, with the rapid scaling and development of the silicon-based integrated circuit technologies such as CMOS and SiGe, low cost technologies have shown acceptable millimeter-wave performance, which can enable highly integrated millimeter-wave radio devices and reduce the cost significantly. Furthermore, at this range of frequencies, on-chip antenna becomes feasible and can be considered as an attractive solution that can further reduce the cost and complexity of the radio package.

The propagation channel challenges for the realization of low cost and reliable silicon-based communication devices at millimeter-wave band are severe path loss as well as shadowing loss of human body. Silicon technology challenges are low-Q passive components, low breakdown voltage of active devices, and low efficiency of on-chip antennas.

The main objective of this thesis is to investigate and to develop antenna and front-end for cost-effective silicon based millimeter-wave phased array radio architectures that can address above challenges for short range, high data rate wireless communication as well as radar applications. Although the proposed concepts and the results obtained in this research are general, as an important example, the application focus in this research is placed on the radio aspects of emerging 60 GHz communication system. For this particular but extremely important case, various aspects of the technology including standard, architecture, antenna options and indoor propagation channel at presence of a human body are studied.

On-chip dielectric resonator antenna as a radiation efficiency improvement technique for an on-chip antenna on low resistivity silicon is presented, developed and proved by measurement.

Radiation efficiency of about 50% was measured which is a significant improvement in the radiation efficiency of on-chip antennas. Also as a further step, integration of the proposed high efficiency antenna with an amplifier in transmit and receive configurations at 30 GHz is successfully demonstrated. For the implementation of a low cost millimeter-wave array antenna, miniaturized, and efficient antenna structures in a new integrated passive device technology using high resistivity silicon are designed and developed.

Front-end circuit blocks such as variable gain LNA, continuous passive and active phase shifters are investigated, designed and developed for a 60GHz phased array radio in CMOS technology. Finally, two-element CMOS phased array front-ends based on passive and active phase shifting architectures are proposed, developed and compared.

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Dedication

To my beloved wife, *Leila*,

To my parents

To my teachers

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Chapter 1 Introduction

In the ever growing demands of higher data rate for wireless communications and to enable emerging applications, researchers and industries are becoming increasingly interested in millimeter-wave and the sub-terahertz spectrum. In these bands more bandwidth [1]-[10] for applications such as Gb/s wireless USB(Universal Serial Bus), HD(High Definition), WPAN(Wireless Personal Area Network), WLAN(Wireless Local Area Network) is available. Furthermore, the advantages of millimeter-wave and terahertz for emerging applications can be exploited. The advantages of millimeter-wave are higher available bandwidth, small size and high gain antenna, unlicensed and worldwide availability of some of released bands. However there are also challenges for the realization of low cost and reliable communication devices at millimeter-wave and the challenges grow with the frequency. Severe path loss and shadowing of human body are among main propagation channel difficulties in this range of frequencies as compared to low frequency microwave bands.

The new license-free bands (i.e., 24 GHz, 60 GHz, 77 GHz, and beyond 100 GHz) could be exploited by applications such as WLAN [11] , WPAN[12]-[13], car radar [14]-[15]. Standardization of 60GHz band under IEEE802.15.3c[16] for WPAN, Wireless HD[17] for uncompressed high definition video transfer and WiGig[18] for WLAN upon having compatible standards could bring 60GHz into many existing consumer electronic, portable and handheld devices.

The major obstacle for wide deployment of commercial wireless systems in this range of frequency is the high cost and bulky nature of existing GaAs and InP solutions. In recent years with the rapid scaling and development of silicon integrated circuit technologies such as CMOS (Complementary Metal Oxide Semiconductor) and SiGe (Silicon Germanium), low cost technologies have shown acceptable millimeter-wave performance which can enable highly integrated millimeter-wave radio devices. However, the silicon technology challenges are low quality factor passive components, low efficiency on-chip antennas, and low breakdown voltage devices. Minimum noise figure of silicon devices reduces with scaling; however it is still higher or comparable with GaAs devices at this band.

There are also challenges in packaging and antenna integration for realization of low cost miniaturized transceiver modules. Miniaturized integrated antenna/radio device is an essential part of the implementation of any novel intelligent multi-antenna radio at millimeter-wave. System-On-Chip (SOC), System-In-Package (SIP), and System-On-Package (SOP) architectures have been proposed to integrate radio front-end circuits, the IF section, and digital base-band section of the transceiver into a miniaturized package, however a key challenge that needs to be investigated and resolved is the integration of the antenna and its interaction with the rest of the radio circuit on the same chip or very close to it. At the millimeter-wave band, on-chip antenna becomes feasible and looks like an attractive solution. The challenges with the on-chip antennas are low radiation efficiency and high silicon cost.

The main objectives of this research are to explore and develop novel concepts of efficient millimeter-wave on-chip antennas and radiation efficiency improvement techniques, to develop key circuit blocks of a phased array such as variable gain LNA and continuous phase shifter in CMOS technology, and to investigate radio architectures that can address the above mentioned challenges.

This chapter explains the main motivations, applications, and objectives of this research.

1.1 Why Millimeter-wave?

The millimeter-wave band (30-300GHz) has several advantages for communication, imaging, and UWB (Ultra Wide Band) radar applications. From a communication perspective, high available bandwidth (such as 7GHz unlicensed band at 60GHz), compact antenna and radio module, and less interference are the main advantages. For radar applications higher frequency and bandwidth increase the image resolution or range resolution for distance measurement.

On the other hand the challenges of millimeter-wave for enabling high volume markets are high free space loss, dielectric and metal loss, severe shadowing loss, and high cost of existing semiconductor technology and system solutions. Addressing these challenges with low cost solutions will enable high volume markets such as automotive radar sensors, high data rate wireless devices as well as emerging applications in the field of imaging and radar.

1.1.1 Existing MMW Frequency Bands and Applications

1.1.1.1 Automotive Radar Sensors

Currently 24 GHz and 77 GHz frequency bands have been proposed or allocated in different countries for narrow band and ultra wide band (UWB) short range and long range radars used in automotive applications. Table 1.1 shows the status of car radar frequency bands in different countries. 24GHz is allocated for short range auto radar, and as a blind spot detection and parking aid.

The 76-77 GHz band is used for forward-looking vehicular radar. Such radar is also called "adaptive cruise control" or "collision avoidance" radar, and would provide drivers useful warnings about obstacles in their path. This radar would be an evolutionary step towards intelligent traffic systems. Some of these radar systems are currently developed with high-cost existing technologies and available in the market within high-end cars. However, low cost integrated solutions are required to make such technology available to all types of cars in the near future.

Table 1.1: Status of frequency bands for automotive radar in different countries[19].

	24GHz (Narrow-band)	**24GHz UWB Short Range Radar**	**26GHz UWB Short Range Radar**	**77GHz Long Range Radar**	**79GHz Long Range Radar**
Europe	200MHz	5GHz Until 2013	4GHz Proposed	1GHz	4GHz
USA/ Canada	100/250MHz	7GHz 22-29GHz		1GHz	No Activity
Japan	76MHz	Under study	Proposed	0.5GHz	Under study

1.1.2 60GHz for Gb/s Radio Devices and Networks

As shown in Figure 1.1 large bandwidth sections in the frequency range between 57-66 GHz have been allocated for unlicensed wireless communication globally. A 60 GHz link could be used to replace various cables used in the home or office. It can also be used for fast data transfer between portable devices. While other standards such as 802.11n and UWB have been trying to address Gbps data rate demands, 60 GHz seems to be the most viable option. The intended range of WPANs is 10m or less, which is suitable for most offices, medium-size conference rooms, and rooms in the home. Wireless PANs could link various electronic devices, including laptops, cameras, cell phones, PDAs, and monitors. Applications include wireless HD, wireless docking station, and wireless data streaming from one device to the other.

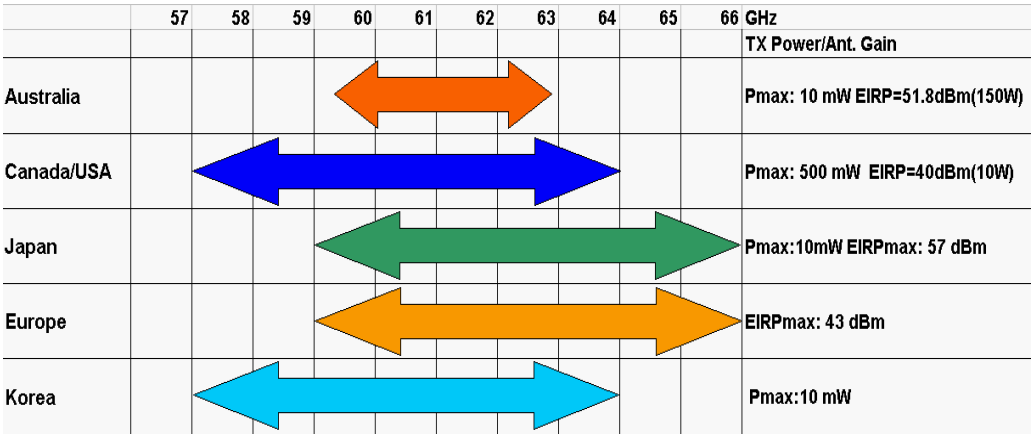


Figure 1.1: Frequency allocation and radiated power limitation at 60GHz band in different countries.

The 60 GHz unlicensed band provides the following advantages:

- Sufficient bandwidth for Gb/s (Typically 7 GHz in U.S. and Canada).
- High radiated power allowed. Unlike the strict transmit power restrictions on ultra wide band, the millimeter-wave band allows a high Effective Isotropic Radiated Power (EIRP) which is typically +40 dBm at 60 GHz in US and Canada [20].
- Clean spectrum, no interferer. There are not any widely deployed 60 GHz radio systems in the home or office, so there is less chance of having interferer signals.
- Small antennas at 60 GHz make the overall system packaging more compact and convenient. Small apertures in 60 GHz can generate high radiation gains.

- Standardization of the 60 GHz under IEEE.802.15.3c for WPAN applications, and Wireless HD Consortium by defining a wireless protocol to create a 60 GHz wireless video network for consumer electronic audio and video devices and WiGig for high data rate WLAN/WPAN and mobile applications.

1.1.2.1 Millimeter-Wave WPAN/WLAN

Typically, WPAN is a wireless network for interconnecting devices around person's workspace. In general, a WPAN uses short range radio technology (about 10 meters). There is a fast growing demand for ultra-broadband wireless electronic devices which can communicate with a high data-rate within a short range. The current WLAN and WPAN solutions (e.g., 802.11 and 802.15.1/Bluetooth) can only satisfy low data rate applications. However most of the emerging ultra wideband applications cannot be served with the current standards and state-of-art radio technologies. The standards for gigabit-level applications are still in development phase. The proposed applications cover a wide range of uses such as data, high-definition (HD) media, and transportation [17].

The new ultra-broadband systems will replace some of the existing wireline technologies. Moreover, a common requirement for all of these emerging applications is that the solution cost must be similar to the wired solution that it is replacing. The new ultra-broadband applications of WPAN include but not limited to [21]:

- Up to 6.5 Gb/s Wireless Networking (IEEE802.15.3c standard)
- Video Source to Projector Connection
- Uncompressed Baseband High-Definition Video or Audio
- High-Bandwidth Data Transfer (USB/1394/SATA)
- Low-Power Mobile Applications

1.1.3 E-band

E-band is allocated for point-to-point communications and could be used for telecommunications backhauls or point-to-point local-area networks. In the US, specified bands are 71-76, 81-86 GHz, and 92-95 GHz. License requirement for these bands limits the interference. Also as compared to 60 GHz these bands are free from oxygen absorption. The

developed low cost technologies for the 60GHz high volume market could be used for such services too, which will lower the cost of such systems significantly.

1.2 Why Silicon Millimeter-wave?

Wide-spread wireless applications utilizing the spectrum below 10 GHz have grown extensively over the past 10 years, due to the demand of the market and the rapid growth of silicon-based technologies such as CMOS, and SiGe. Figure 1.2 shows ITRS semiconductor roadmap including emerging millimeter-wave applications as well as transition to applications in sub-THz region beyond 100 GHz. With the availability of the low cost devices with f_{max} of above 200 GHz and high integration possibility, advanced CMOS and SiGe technologies are becoming the main technology options for development of low cost millimeter-wave systems, enabling fast market growth for low cost ultra broadband technologies.

As compared to III-V devices, silicon carrier mobility is relatively low. Furthermore, low-resistivity requirement of silicon substrates in CMOS and SiGe results in poorer isolation and higher losses in interconnects and passive devices. Each of these issues presents serious challenges to implementing millimeter-wave functions in silicon. However, with the geometry scaling and technology improvements, performance parameters such as f_T, and f_{max} have dramatically increased and NF_{min} has decreased in both CMOS and SiGe HBTs[23]. The ability of implementing a large number of digital gates in the minimum possible chip area and thereby enabling the on-chip integration of sophisticated control logic for performance tuning and/or digital signal processing are other advantages of the silicon technologies for system integration.

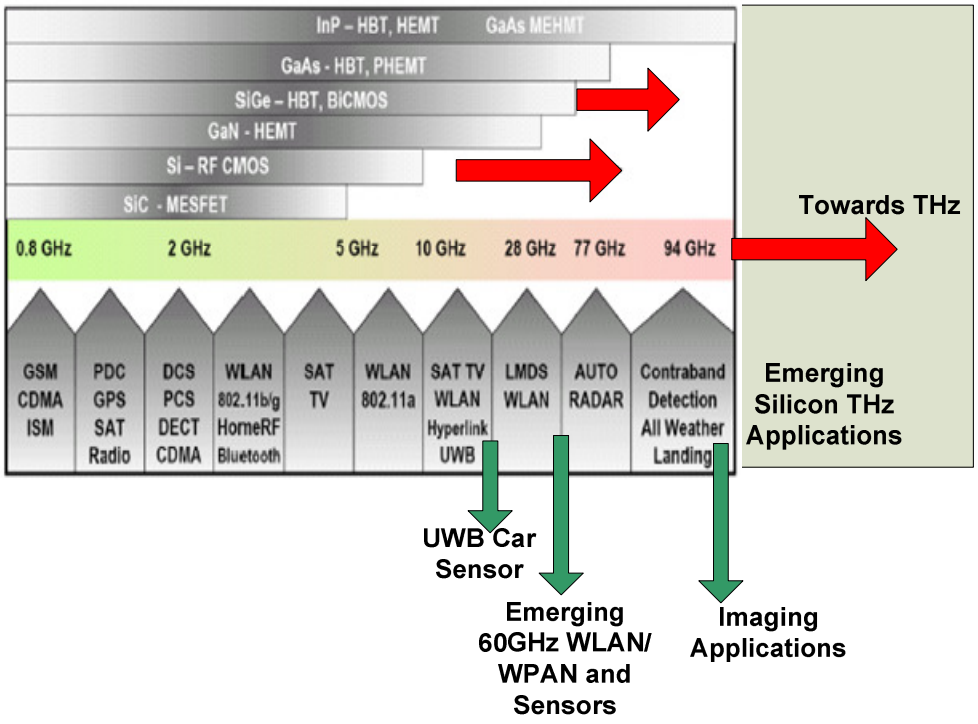


Figure 1.2: Modified ITRS semiconductor roadmap and future perspective [22].

1.3 Why Phased Arrays?

A phased-array system is a special class of adaptive multi-antenna systems where signals from different antennas are phase shifted and combined coherently in the receiver and on transmit side, signals with different phases are applied to the transmitter antennas. Phased arrays have a wide range of applications in satellite communications[24], radar[25], radio astronomy [26], and optics [27].

Variable phase shifter, time delay element, amplitude control devices, and a low loss feed circuit are the key hardware components of a phased array used for beamfoming/beamsteering and pattern shaping. Having multiple antenna elements, phased arrays provide precise control on the radiation pattern and sidelobes.

Phased array technology can impact the silicon based millimeter-wave radio by providing the following advantages:

- **Spatial power combining in the transmitter:**

RF power generation in the higher frequencies is a challenge. The high substrate and conductor loss reduces the efficiency of the power generation/amplification by RF sources. The situation becomes worse with the scaling of the silicon technologies as the breakdown voltage of the devices reduces, which limits the maximum voltage swing at the output of power amplifier.

To alleviate these difficulties, one common approach for power generation is to combine the power generated by a number of sources. Power combining within the planar circuit suffers from the intrinsic losses of dielectrics and metals. Spatial power combining is an efficient solution for signal combining with maximum efficiency. Furthermore using phased array architecture, the radiated signals can be combined in-phase toward a certain direction. By changing the phase of the signals the radiation beam can be steered.

- **Transmitter EIRP (Effective Isotropic Radiated Power) improvement**

EIRP is the amount of power that would have to be radiated by an isotropic antenna to produce the peak power density observed in the direction of maximum antenna gain.
If the transmitter output power is P Watts and the antenna gain is $G(\theta,\varphi)$ then

$$EIRP(\theta,\varphi) = P.G(\theta,\varphi)$$

In an N element transmitter array, if each element radiates P Watts, then in the target direction, EIRP will be improved by $20LogN$.

- **SNR improvement in receiver**

Having multiple antennas in a phased array configuration can improve the SNR of the received signal ideally by $10LogN$. This can improve the communication range assuming a fixed power at the transmitter. It can also reduce the power consumption assuming a fixed communication range.

- **SNR improvement in NLOS channel:**

As will be shown in chapter 2, in the case of shadowing within the channel, a phased array configuration is able to find maximum received signals from the reflections in a room or in an office.

1.4 Statement of the Problem

Millimeter-wave band will be hosting future silicon based communication, radar, imaging and sensor devices. Silicon technology is scaling down further and the target is set to achieve 500 GHz f_{max} devices in SiGe technology in the next few years [28].

The challenges of millimeter-wave are high free space and shadowing channel loss, high substrate loss and passive component loss due to low resistivity silicon, and output power limitation resulting from scaling of silicon technologies. To be able to address these challenges and enable the emerging applications, exploration and development of efficient integrated antennas and radio front-end architectures are the keys.

1.5 Thesis Objectives

Different aspects of silicon millimeter-wave radio research are shown in Figure 1.3. In the front-end part, integrated antenna, radio architecture, silicon integrated circuit design, and technology are the main elements.

The purpose of this dissertation is to explore cost-effective, high performance and efficient silicon based antenna/front-end solutions. Particularly on the antenna part, the focus of this research is placed on the investigation and development of high efficiency on-chip antenna in a low resistivity silicon substrate and integration of the proposed antenna with radio front-end.

With the radio architecture and circuit aspects of the front-end, the focus is placed on the investigation and development of cost-effective millimeter-wave phased array architectures, and CMOS-based circuit blocks.

The outcome of this research could be exploited for realization of:

- Low power millimeter-wave radio for line of sight and short range Gbps data transfer.
- Compact and low cost phased array solutions for a Non Line of Sight (NLOS) channel.
- Silicon-based phased array radar devices.

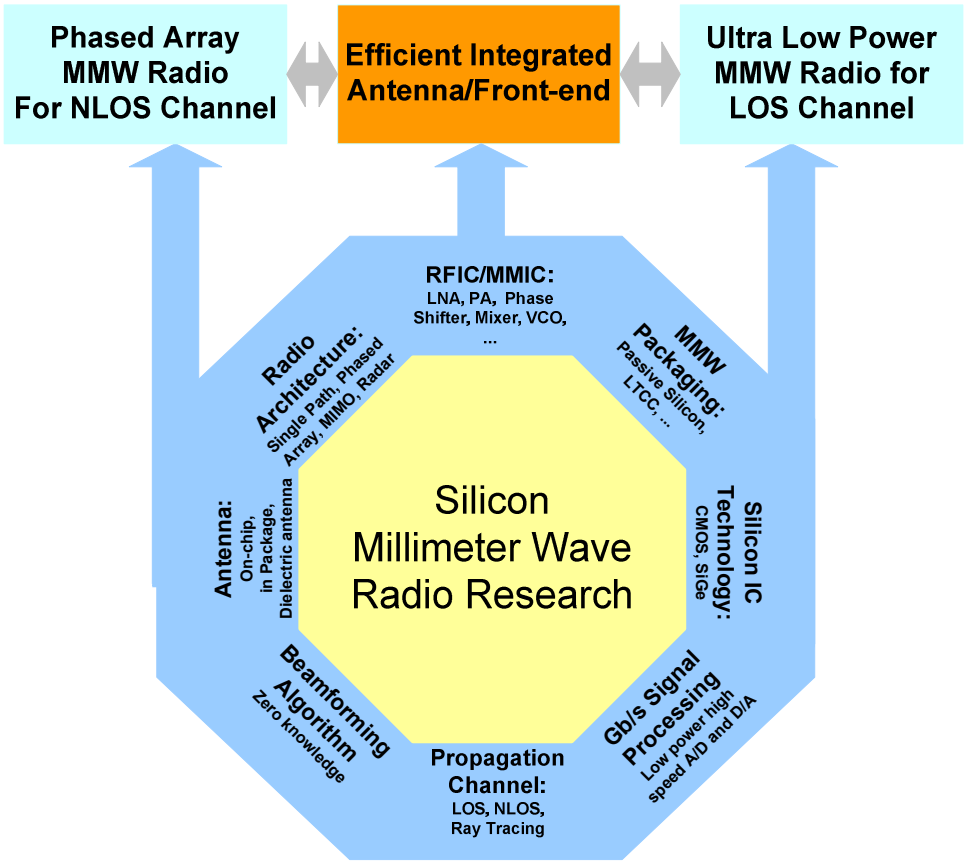


Figure 1.3: Silicon millimeter-wave radio and objectives of this research.

1.6 Outline of this Research

Chapter 2 of this dissertation presents the radio system analysis and architecture study for fixed-antenna single-channel and phased array radio at 60 GHz. The effect of human body in the 60 GHz channel has been investigated and it has been shown how a phased array receiver can improve the SNR in a NLOS condition for a typical application of 60 GHz WPAN.

Chapter 3 focuses on high efficiency on-chip millimeter-wave antenna and radiation efficiency improvement techniques.

Chapter 4 presents design of a millimeter-wave phased array front-end. First, key circuit blocks of a 60 GHz phased array such as a low noise amplifier, active and passive phase shifters and a mixer in CMOS technology have been presented.

Furthermore this chapter describes the proposed receiver architecture and presents two approaches for RF phase shifting based on active and passive phase shifting as well as power combining. Finally, Chapter 5 concludes this research and proposes directions for future research.

Chapter 2 Phased Array Radio for 60GHz Wireless Communication

2.1 Introduction

Currently, different millimeter-wave bands have been specified for radar and communication applications. The 60 GHz frequency band has been released and proposed for short-range wireless applications such as WPAN[12]-[13], and wireless multimedia/HD streaming. IEEE task group 3c (TG3c) is working on standardization of this frequency band for WPAN applications. At the same time, Wireless HD Consortium has defined a wireless protocol to create a 60 GHz wireless video network for consumer electronic audio and video devices [17]. WiGig alliance is also working on defining a 60 GHz standard for different 60 GHz applications of consumer electronic, portable and handheld devices.

Upon the convergence of different standards, high-volume markets for 60 GHz systems are predictable. For this to happen, compact, low cost, and high performance transceivers are the key.

Nanoscale CMOS technology, such as 130 nm, 90 nm, 65 nm and 45 nm, offers commercial millimeter-wave solutions for short range and high data rate applications. However, several system and circuit level challenges such as lack of the efficient and low cost antenna and packaging solutions, low output power and nonlinearity of power amplifiers, severe path loss, shadowing loss, limited gain of the Low Noise Amplifier (LNA) and its high noise figure, must be addressed.

For a wide range of emerging applications in the 60 GHz spectrum, (as will be discussed in this chapter) use of multiple antennas with beamsteering capabilities is an important enabling technology. However the efficiency of a phased array depends on the performance of antenna, LNA, phase shifter, and feed circuit loss. Furthermore, to lower the overall cost, all the components must be implemented in a low-cost technology and possibly on a single chip.

So far, the reported millimeter-wave systems at 52, 60 and 77 GHz bands on CMOS and SiGe are either a single receiver [5]-[6], [29], two-element receiver[30], single transmitter[31]-[32] , or transceivers which are not able to meet some of the above

mentioned challenges [2],[33]. Moreover, the reported phased array systems [7][30] have difficulties lowering power consumption and reducing silicon area. Integration of the transceiver chip with an antenna especially for phased array has not been fully addressed yet. The need for new solutions is more critical if a large number of array elements are required to meet the link budget and network coverage specification.

In this chapter, first, 60 GHz radio front-end specification requirements will be derived from standard specifications. Then, the radio architectures for single antenna and antenna array systems are presented. The indoor 60 GHz propagation channel is studied and a test set-up for measuring the shadowing loss of a human body is described.

Furthermore, it is shown that a 9 or 16 element CMOS phased array can achieve the required signal to noise ratio for multi-Gb/s wireless communication in a picocell (such as a regular office). Nevertheless, a robust and efficient beamforming algorithm is essential to realize the phased array potentials. Such algorithms have subject of intensive research by other researchers in CIARS (Center for Intelligent Antenna and Radio System) at the University of Waterloo[62].

2.2 802.15.3c[16]/ECMA 60 GHz Standards[34]

Based on standard specifications, application, technology strengths and limitations, the required parameters of a communications link such as antenna gain, transmitter power, receiver noise figure, etc., can be determined. For 60 GHz short-range wireless communications, three main standard drafts have been released which are referred to as IEEE 802.15.3c and ECMA (European Computer Manufacturer's Association) 387 and WirelessHD.

From the RF channelization perspective, as shown in Table 2.1 and Figure 2.1, 4 channels with the BW of 2.16 GHz have been defined in all of the above standards.

The standard specifies four frequency channels each with a symbol rate of 1.728 Giga-Symbols/second and with a separation of 2.160 GHz. All device types follow the same frequency plan. Under this frequency plan, the standards support bonding of up to four adjacent channels. The channel bonding allows achieving higher data rates, or the same data rates while using smaller, more efficient constellations. This configuration needs a wideband front-end with the bandwidth of at least 8 GHz at 60 GHz.

Table 2.1: Channel assignment of 60GHz band

Channel ID	Start Frequency	Center Frequency	Stop Frequency
1	57.240GHz	58.320GHz	59.400GHz
2	59.400GHz	60.480GHz	61.560GHz
3	61.560GHz	62.640GHz	63.720GHz
4	63.720GHz	64.800GHz	65.880GHz

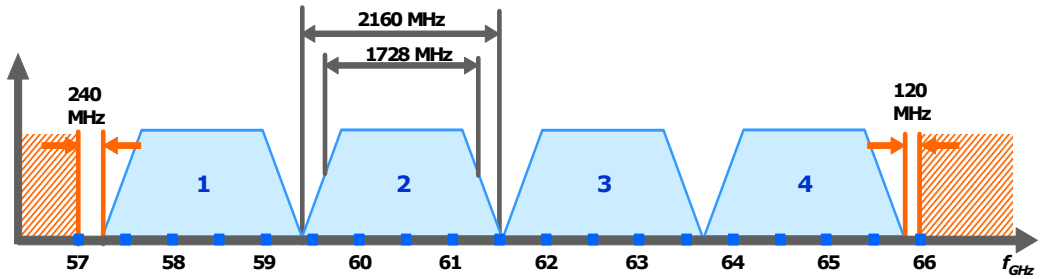


Figure 2.1: RF channelization at 60GHz band [34]

IEEE 802.153c defines three classes of modulation and coding schemes for the Single Carrier (SC) mode in millimeter-wave physical layer (PHY) summarized in Table 2.2, for different wireless applications[16]:

- Class 1 is specified to address the low-power low-cost mobile market while maintaining a relatively high data rate of up to 1.5 Gb/s.
- Class 2 is specified to achieve data rates up to 3 Gb/s.
- Class 3 is specified to support high performance applications with data rates in excess of 5 Gb/s.

Table 2.2: Summary of 60 GHz device classification in IEEE802.15.3c

Parameter	Class 1	Class 2	Class 3
Data Rate	<1Gb/s	1.5Gb/s<Data Rate<3Gb/s	3Gb/s<Data Rate<5.5Gb/s
Receiver Sensitivity	-65 dBm	-58 dBm	-50 dBm
Modulation	π/2 BPSK/GMSK	π/2 QPSK	π/2 8PSK, π/2 16QAM
Number of Modes	7	5	2

Similar to IEEE 802.15c, ECMA 387 defines three types of devices for 60 GHz spectrum based on the operational requirements such as maximum range, bit rate and system

complexity. These types are called Type *A*, Type *B* and Type *C*. Several operational modes have been proposed for each type.

Table Table 2.3 summarizes these different classes.

- Type A, high end and high performance device, offers live video streaming and WPAN applications in 10 meter range in both LOS and NLOS multipath environments.
- Type B, the ”economy” device , trades off range and NLOS performance in favor of low cost implementation and low power consumption.
- Type C, the bottom-end type, providing simplest implementation, lowest cost and lowest power consumption.

Table 2.3: Summary of 60GHz device classification in ECMA 387

Parameter	**Type A**	**Type B**	**Type C**
Maximum Range	10m NLOS	3m LOS	1m LOS
Data Rate	3.97-6.35Gb/s	0.794-3.175Gb/s	0.8-3.2Gb/s
Receiver Sensitivity	-60 dBm	-60.7 dBm	-62.2 dBm
Modulation	BPSK/QPSK /8QAM/16QAM	DBPSK/DQPSK/	OOK/4ASK
Number of Modes	14	5	3

2.3 Link Budget for LOS Propagation Channel

In this section we perform the link budget calculation for a noise-limited system where the thermal receiver noise dominates. The sensitivity of a receiver depends on the noise performance of its receiver front-end, given Bit Error Rate (BER), and modulation scheme. For a non-fading AWGN channel, analytic expressions for the BER of different modulation schemes versus SNR are given in [35]. Figure 2.2 shows the BER versus SNR for the AWGN channel. It is seen that an SNR of at least 12 dB must be delivered to the base-band receiver by the RF front-end to keep the BER below 10^{-6} for most of the modulation schemes. For a fading channel various diversity techniques (time, frequency or space) can be applied to improve the performance.

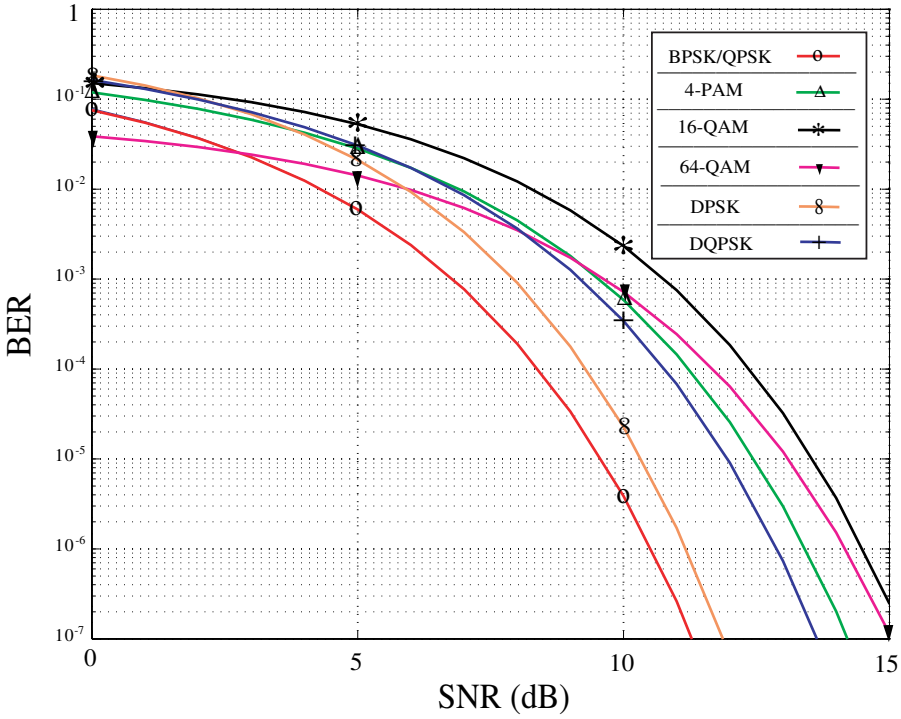


Figure 2.2: Bit Error Rate versus SNR for different modulation schemes.

Assuming other parameters are known, Friis free space transmission formula and the receiver sensitivity specification determines required antenna gain as well as receiver NF (Noise Figure) :

$$G_T + G_R > P_L + S_{\min} - P_T \qquad (2.1)$$

$$NF < 174^{dBm/Hz} + S_{\min} - 10LogBW - SNR_{\min} \qquad [36]\ (2.2)$$

Where

G_T: Gain of the transmitter antenna in dBi

G_R: Gain of the receiver antenna in dBi

P_L: Free space path loss in dB, which is equal to $\left(\frac{\lambda}{4\pi R}\right)^2$ where λ is the wavelength and R is the distance between transmitter and receiver

S_{min}: Receiver sensitivity in dBm

P_T: Transmitter power in dBm

NF: Receiver noise figure in dB

BW: Channel bandwidth in Hertz

SNR_{min}: Minimum signal to noise ratio at the input of demodulator in dB

In equation (2.1) it is assumed that there is no impedance mismatch as well as no polarization mismatch between the transmitter and receiver antennas. In case of polarization and impedance mismatches the following equation should be used instead of (2.1):

$$\frac{P_r}{P_t} = (1-|\Gamma_t|^2)(1-|\Gamma_r|^2)e_t e_r |\hat{\rho}_t.\hat{\rho}_r|^2 \left(\frac{\lambda}{4\pi R}\right)^2 D_t(\theta_t,\varphi_t) D_r(\theta_r,\varphi_r) \quad (2.3)$$

Where

P_r : Received power

$|\Gamma_t|$: Magnitude of transmitter antenna input reflection coefficient

$|\Gamma_r|$: Magnitude of receiver input reflection coefficient

e_t : Radiation efficiency of transmitter antenna

e_r : Radiation efficiency of receiver antenna

$|\hat{\rho}_t.\hat{\rho}_r|^2$; Polarization mismatch factor

$D_t(\theta_t,\varphi_t)$: Transmitter antenna directivity

$D_r(\theta_t,\varphi_r)$: Receiver antenna directivity

Assuming communication ranges of 10 m, 3 m, and 1 m, no polarization and impedance mismatch, specified sensitivity of the receiver in the standard, transmit power of 2 dBm and BW of 2 GHz, Table 2.4 shows the required transmitter and receiver antenna gain and receiver noise figure for different classes of devices defined in the 60 GHz standards.

For type C and class 1, assuming the same antenna on the receiver and transmitter sides respectively, a minimum antenna gain of 0.5 dBi for each side is required. Also NF of less than 4 dB is needed to meet standard requirements. These could be achieved using proposed improved on-chip antenna in this thesis in a 90 nm or 65 nm CMOS technology or 130 nm SiGe technology. However to have some margin, higher transmitter power is also required.

For type B and class 2, antenna gain of at least 8 dBi on each side is required. Ideally, this can be achieved by a 2 element patch antenna. However considering the feed loss and link margin a higher antenna gain and transmitter power may be required.

Table 2.4: Required antenna gain and receiver NF for different classes of devices

Link Parameters	Type A Class 3	Type B Class 2	Type C Class 1
D	10 m	3 m	1 m
P_L (LOS)	88 dB	77.6dB	68 dB
S_{min}	-60 dBm	-60.7 dBm	-65 dBm
P_T	2 dBm	2 dBm	2 dBm
$G_T + G_R >$	26 dBi	15.6 dBi	1 dBi
BW	2 GHz	2 GHz	2 GHz
SNR_{min}	15 dB	12 dB	12 dB
NF<	6 dB	8.3 dB	4 dB

For type A and class 3, gain of at least 13 dBi on each side is required which is achievable with 6 element patch antenna array. Practically, higher antenna gain and transmitter power will be required to overcome the feed, packaging loss to have sufficient margin for the link.

2.4 NLOS Indoor Propagation Channel Modeling and Measurement

Indoor propagation at millimeter-wave frequencies can be modeled using Geometrical Optics (GO) ray-tracing method enhanced by uniform asymptotic diffraction theories and experimental models. It has been confirmed by measurements that channel characterization results obtained by accurate ray-tracing method at microwave frequencies are quite reliable [37][39]. For indoor applications at 60 GHz, the high penetration loss of the partition/wall material isolates adjacent rooms, and significantly limits the received interference. Only those objects inside the room need to be included in the ray-tracing simulation. In this in-room propagation channel, both Line of Sight (LOS) and Non Line of Sight (NLOS) rays must be considered. The NLOS rays are caused by reflections from the wall/ceiling/floor, and objects inside the room as well as some significant first order diffracted rays. Furthermore, propagation loss in the ray-tracing modeling consists of the free-space loss

according to Friis transmission formula, gaseous loss, and reflection, transmission and diffraction losses.

In this section, a 3D ray-tracing modeling (GO plus diffraction) is employed to assess the signal coverage at 60 GHz for a regular office area. The CAD Laboratory, located on the third floor of the EIT building at the University of Waterloo, is used as a typical indoor wireless environment (see Figure 2.3(a)). The lab is furnished with tables, chairs and shelves mostly constructed of wooden and plastic material. The walls consist of layers of different material such as plasterboard, concrete, and wood.

Moreover, various electronic equipment such as computers, printers and test devices are placed in this lab. The empirical data reported in [40] and [41] is used to calculate the reflection coefficients of the material. Moreover, to evaluate the human body shadowing effect, the measured permittivity data for biological tissues in [42] is used. Table I summarizes the measured permittivity data at 60 GHz used in this ray tracing simulation.
The transmitter antenna in Figure 2.4 is located 10 cm below the center of the ceiling (facing down) which is 3.45 m above the floor. The receiver is located on a wooden table 75 cm above the floor. To simulate the shadowing effect, a human-body blocks the LOS path between the transmitter and the receiver as shown in Figure 2.3(b). To model a mobile scenario, the receiver antenna moves within a 2 ×1.75 m grid located 1m above the floor (25 cm above the table). The resolution of the grid cells varies from λ/5 to λ /2.

Table 2.5: MEASURED PERMITTIVITY OF INDOOR MATERIALS AT 60 GHZ [40]-[41]

Type	**Complex ε_r**
Acrylic Glass	2.5298-j2.5298
Chipboard	2.8556-j0.3014
Glass	5.2839-j0.2538
Plasterboard	2.8096-j0.0461
Concrete	6.1326-j0.3014
Wood	1.5671-j0.0962
Human Body	13.2-j10.4

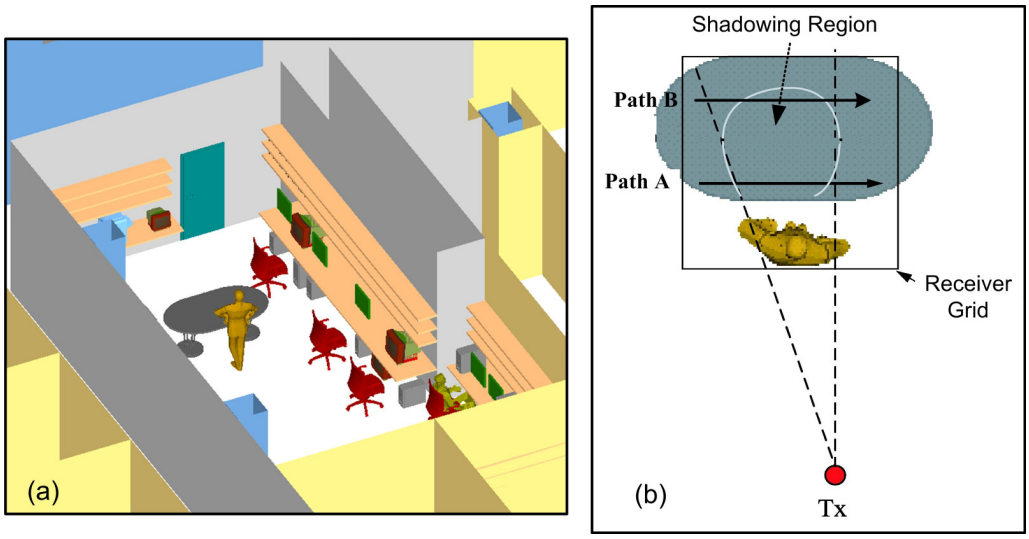


Figure 2.3: (a) Simulated 3D view, and (b) top view of the propagation environment (CAD Lab at the University of Waterloo).

Figure 2.4 demonstrates the results of the accurate ray-tracing at 60 GHz for the described grid in front of the human body in Figure 2.3. The human body model is 1.8 m tall centered at (-0.5 m, 1.4 m, 2.54 m) relative to the transmitter antenna. The white area in Figure 2.4(a) illustrates the opaqueness of the human body at 60 GHz. The transmitter antenna was a 2×2 microstrip patch array with a maximum gain of 10 dBi (see Section 2.6 for the radiation pattern of the antenna) and the input power to the antenna was 2 dBm. An isotropic antenna was used as the receiver. Figure 2.4(b) shows the received power on two horizontal lines, named *Path A* and *Path B*, in the region shown in Figure 2.4(a). Path A and Path B are respectively 20 cm and 80 cm away from the human body and 1.7 m and 2.3 m away from the projected transmitter position in Figure 2.3(b).

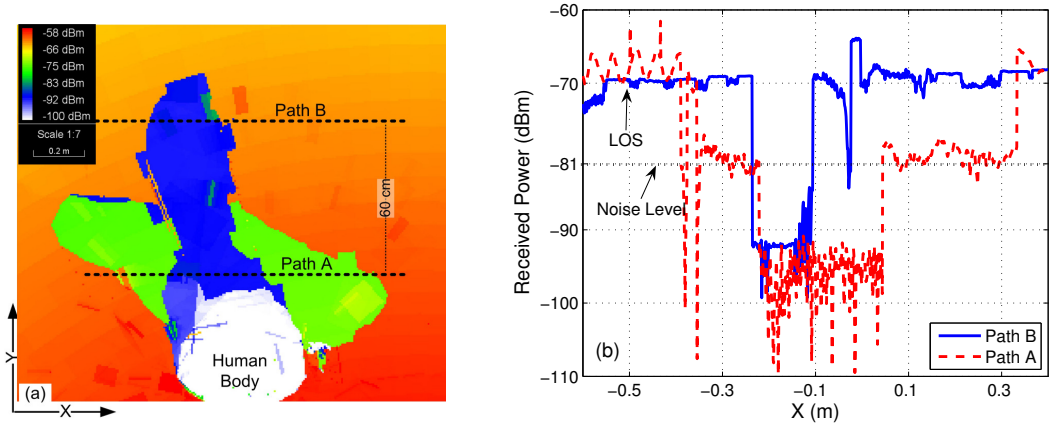


Figure 2.4: (a) Received power for the large grid in Figure 2.3 which surrounds the human body model, (b) received power on Path A and Path B shown in Figure 2.3 (b).

The human body shadowing attenuates the received power level by 10 to 40 dB for Path A and by 15 to 30 dB for Path B. The other objects in the room cause up to ±5 dB fluctuations in the received signal level. In calculating the received power, the time-delay and phase of all rays for which magnitudes are above -120 dBm, have been considered. This threshold is almost 40 dB below the thermal noise power integrated over a 2.16 GHz equivalent bandwidth.

2.4.1 Channel Measurements

Figure 2.5(a) demonstrates the developed test set-up to measure the shadowing loss of human body over the frequency range of 50-75 GHz. Two rectangular horn antennas with 24 dBi gain at 60 GHz and 10º beamwidth were used as the transmitter (Tx) and receiver (Rx) antennas respectively. An Agilent E8267D programmable signal generator connected to an E8257DS15 millimeter-wave source module was used as a source signal. On the receiver side, an Agilent E4448A spectrum analyzer connected to an 11974*V* external mixer was used to measure the spectrum of the received signal. The transmitted power was around 12 dBm. Wave absorbers with 40 dB attenuation were used to weaken the reflections from the source module and the mixer. The Tx and Rx antennas were installed at the height of 135 cm and 130 cm, respectively. The horizontal distance between the Tx and Rx antennas in Figure 2.5(b) was 3 m. The Tx antenna was fixed, but the Rx antenna was moved along a horizontal line in steps of 5 cm (the orientation of the Rx antenna was kept unchanged).

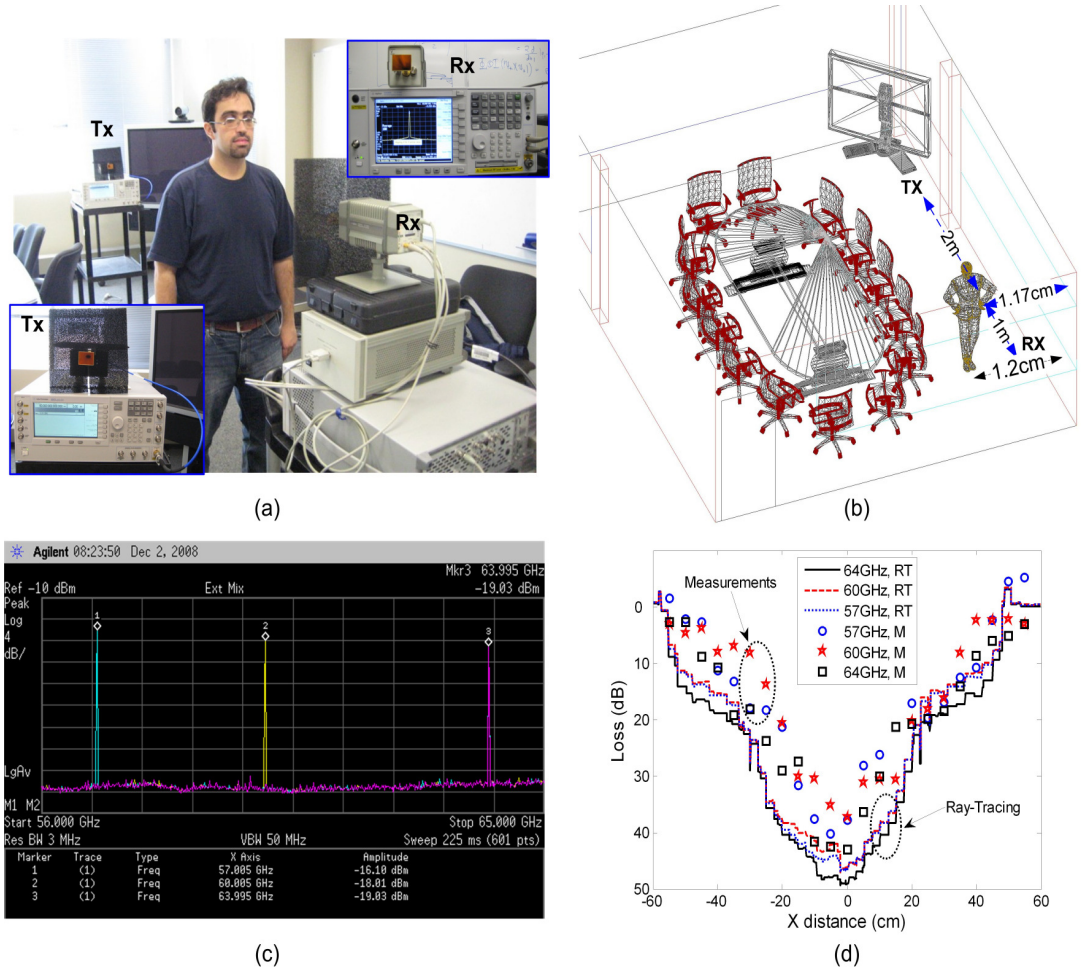


Figure 2.5: Measurement environment and results. (a) Test set-up with transmitter and receiver. (b)Tx and Rx antenna locations in the room. (c) One sample of the measured spectrum at 57, 60 and 64 GHz. (d) Comparison of the measured and simulation results.

At each point the received power spectrum was measured (after calibration) at three frequencies, i.e. 57, 60 and 64 GHz. For each spectral measurement, the average of 100 successive frames was taken to smooth the instantaneous fluctuations. Figure 2.5(c) shows the LOS (no shadowing) measured spectrum at one of these Rx locations. It is seen that the measured power level reduces as the frequency increases, due to the larger path loss at the higher frequencies. Figure 2.5(d) compares the measured shadowing loss with ray-racing results for the same room. There is a good agreement between simulation and measurement from x=-20 to x=60 cm. The maximum shadowing loss is around 40 dB which occurs when the human body blocks the LOS path completely. Ray-tracing results show that at deep shadowing region all LOS rays are absorbed by the human body, so the measured received

power is the combination of NLOS rays. This result has been verified by the measurements in Figure 2.5(d). A phased array receiver, as will be discussed in Section 2.7, has the potential of steering the array beam to the direction of the strongest NLOS ray when the receiver is inside the deep shadowing region.

2.5 MMW Transceiver Architectures

Depending on the class of application, required communication range, and channel condition, either single antenna or multiple antenna radio architecture may be used for the radio implementation. This section describes the advantages and disadvantages of different radio architectures for single and multi antenna implementation of the transceiver.

2.5.1 Single Antenna Transceiver Architectures

2.5.1.1 Direct Conversion Architecture

Figure 2.6 shows the direct conversion transceiver architecture. Direct conversion 60GHz transceivers have been reported in [9][43][44]. In this architecture, the received RF signal is directly down-converted to baseband. This architecture has many attractive features and since there is no IF, the overall cost and size of the transceiver is reduced. The channel filtering is implemented in the baseband. The configuration of a direct conversion transceiver looks simpler than heterodyne architectures, but the implementation is much more difficult. The main challenges with this architecture are minimizing the leakage of LO to RF path and accurate quadrature LO generation. The isolation becomes more critical at 60 GHz since the leakage at this frequency is high and strong LO signal can leak to the input of the LNA. Depending on the level of leakage, this can desensitize the LNA. Inaccuracy in phase and amplitude of the quadrature LO signals limits the image rejection of the architecture. The transmitter side is less challenging as long as high LO to RF isolation can be achieved.

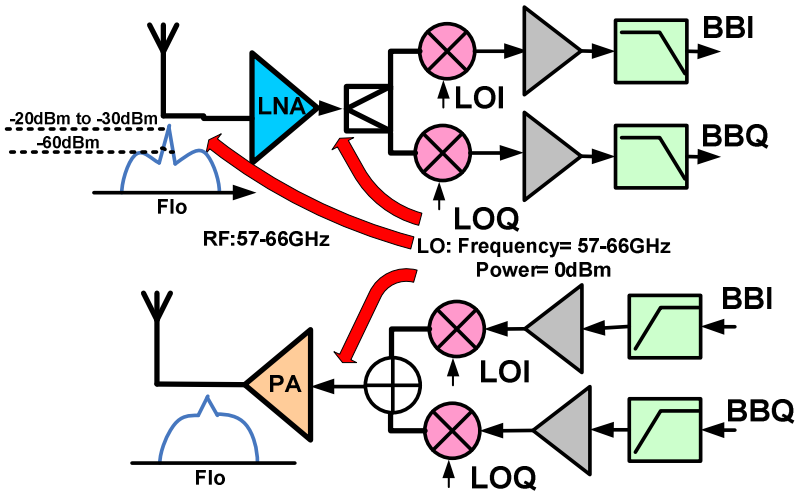


Figure 2.6: Direct conversion transceiver.

2.5.1.2 Variable-IF Heterodyne Architecture

Demonstrated in Figure 2.7, a common heterodyne architecture is a dual conversion with single first stage mixer and an image reject mixer for the second stage of the conversion[2],[45]. In this architecture $M.F_{LO}$ is applied to the first mixer and F_{LO}/N is applied to the second stage. The LO frequency applied to the first mixer is lower than the RF frequency and therefore leakage of LO to the input of first mixer or LNA is not important. This is because the LNA has small gain at that frequency. Also, the generated offset due to LO self mixing can be filtered at IF. The quadrature LO generation is required at a much lower frequency compared to the direct conversion architecture and this improves the accuracy of quadrature generation and thereby higher image rejection ratio of the receiver.

To reduce the local oscillator and synthesizer complexity in direct conversion and dual conversion architecture, half-RF architecture is proposed in [46]. Illustrated in Figure 2.8, the architecture requires only one 30GHz LO. One disadvantage of this architecture is having equal first-IF and LO frequencies which requires a high LO to IF isolation for the first mixer. Furthermore an accurate, wideband, and low loss quadrature generator is still required at RF frequency.

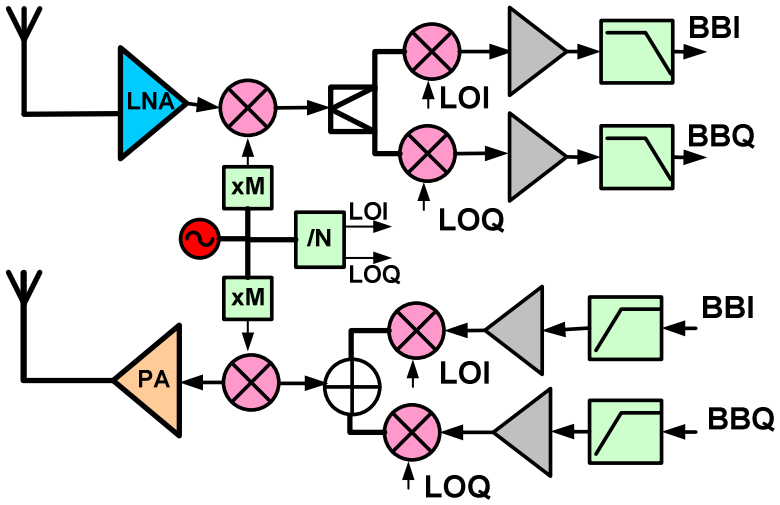


Figure 2.7: Variable IF dual conversion architecture[2],[45].

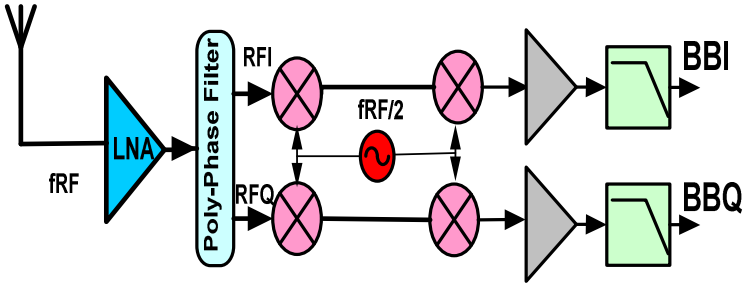


Figure 2.8: Half-RF architecture presented in [46]

2.5.2 Phased Array Transceiver Architectures

2.5.2.1 Array Antenna

Consider N arbitrary antenna elements with the same orientation but arbitrary locations in the space as shown in Figure 2.9. In general, the excitation (amplitude and phase) of each element, called *weight*, is denoted by a complex number, W_i . The electric Field of a reference antenna located at the origin with a unity weight is [47],[131]:

$$\overline{E}_0(\overline{R}) = f_0(\theta,\phi)\frac{e^{-jk_0R}}{4\pi R}\hat{u} \qquad (2.4)$$

where $f_0(\theta,\phi)$ is the E-Field radiation pattern of the reference element, $\overline{R}$ is the distance vector from the element (located at origin), and $k_0 = \frac{2\pi}{\lambda}$ denotes the wave constant. The distance from the i^{th} antenna to the desired far field point (P in Figure 2.9), i.e. R_i, is given by

$$R_i = R - \hat{r} \cdot r_i \qquad (2.5)$$

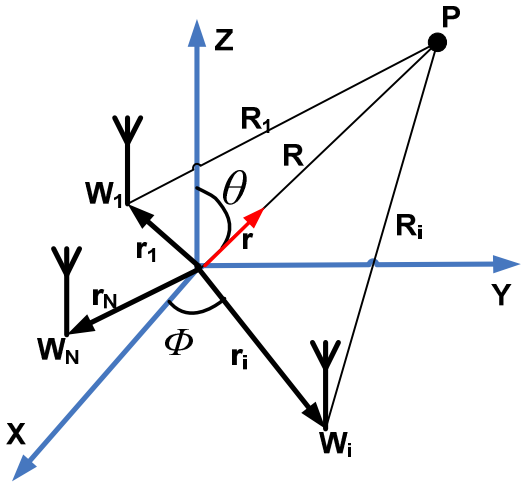


Figure 2.9: Array Antenna[131].

where $\hat{r}$ is the unit vector along R. At far field where $|R| >> |r_i|, \forall i$, the magnitude of R_i is approximated with R in the denominator of the spherical wave propagation factor in (2.4). Based on superposition principle the total E-field generated by all antennas at point P is the vector sum of the individual electric fields [48]:

$$E(r) = \frac{e^{-jk_0R}}{4\pi R}\sum_{i=1}^{N} W_i f_i(\theta,\phi) e^{jk_0\hat{r}\cdot r_i} \qquad (2.6)$$

It is noted that for phase calculation (argument of the spherical wave propagation factor in (2.4)), more accurate "paraxial" approximation in (2.5) has been used.

If *identical* elements are used in the array, then:

$$E(r) = [\frac{e^{-jk_0R}}{4\pi R} f(\theta,\phi)][\sum_{i=1}^{N} W_i e^{jk_0\hat{r}\cdot r_i}] \qquad (2.7)$$

Equation (2.6), also known as the *Principle of Pattern Multiplication*, is the product of two terms: the element pattern given in (2.3) and a summation called *array factor,* which is:

$$AF(\theta,\phi) = \sum_{i=1}^{N} W_i e^{jk_0 \hat{r}\cdot r_i} \qquad (2.8)$$

Array factor in (2.8) depends on the geometry of the array and the excitation weights. For a fixed array constellation, the antenna system radiation pattern can be steered by changing the excitation phases. This property is known as electronically scanning or beam-steering. The array antenna capable of changing the excitation phases is called a *phased array antenna*. Phase shifters or delay lines are used to adjust such weights. Also having a variable gain or amplitude control for each path accommodates compensation of phase shifter gain or loss variations as a function of control voltage when shaping the pattern. A beamforming algorithm calculates the required weights (phases or time-delays and amplitudes) to shape or steer the beam.

2.5.2.2 Phased Array Transceiver Architectures

To steer the main beam of the phased array antenna, phase shifters can be incorporated in different stages of a receiver or transmitter and hence, different phased array configurations can be obtained. These configurations, which are shown in Figure 2.10, are based on RF phase-shifting [48], Local Oscillator (LO) phase-shifting [49], IF phase shifting [50] or digital beamforming [51].

In the RF phase shifting architecture depicted in Figure 2.10 (a), signals in different RF paths are phase shifted and then combined at RF frequency. The combined signal is then down-converted to the IF or baseband. In this architecture the spatial filtering of the strong undesired signals is performed at the combination point prior to the mixer. Hence, the upper dynamic range requirement of the mixer is relaxed and the level of unwanted in-band inter-modulations after mixer decreases. The design of the phase shifter on silicon, however, remains a challenge in this architecture. In addition, the insertion loss variation with phase-shifting should be small; otherwise, the array factor is deteriorated [52].

LO phase shifting architecture is displayed in Figure 2.10 (b). The main advantage of this architecture over RF phase shifting of Figure 2.10 (a), is that the phase shifter loss, non-linearity, and noise performance do not directly affect the receiver performance.

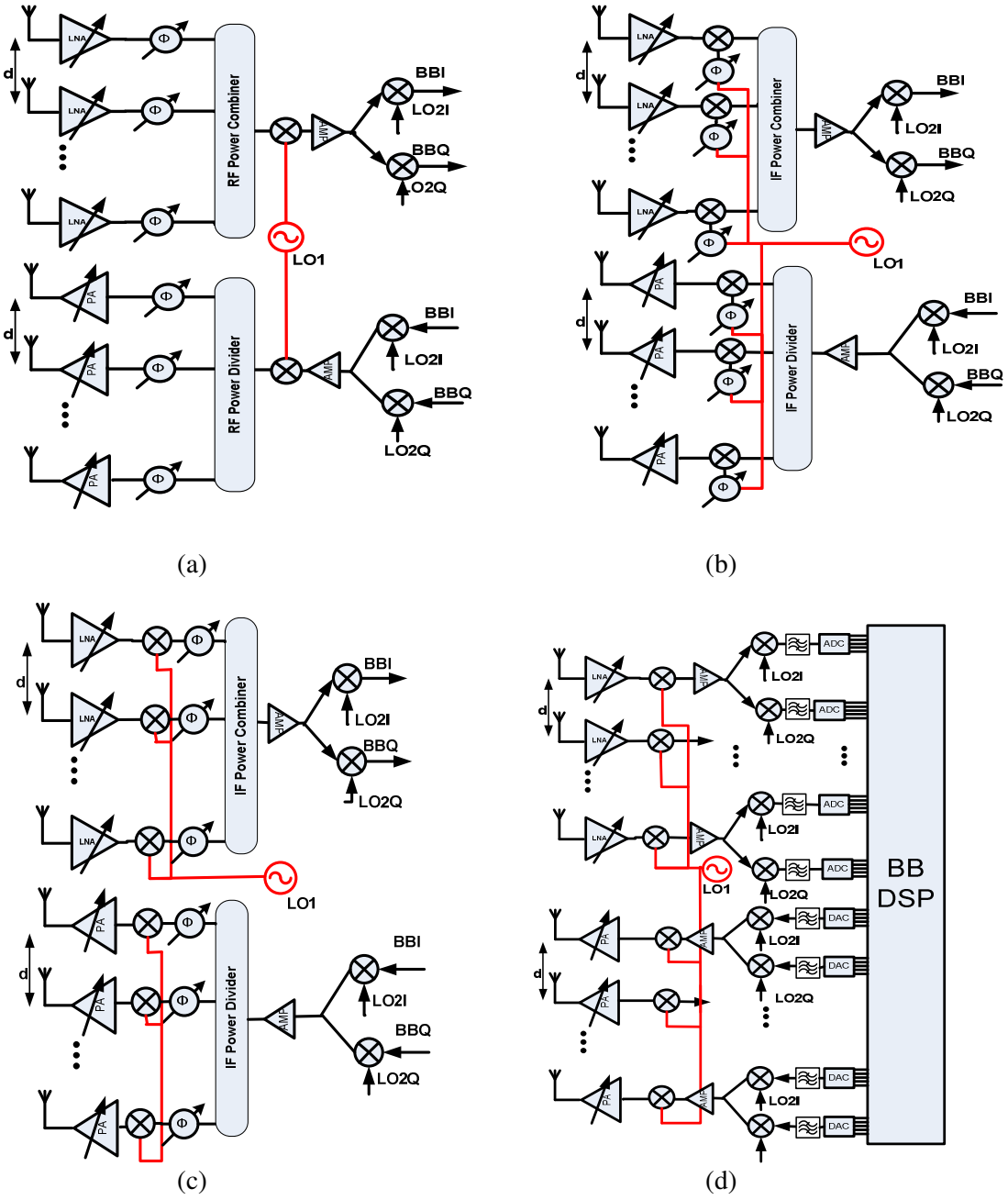


Figure 2.10**:** Different phased array configurations (a) RF phase shifting, (b) LO phase shifting (c) IF phase shifting, and (d) digital beamforming array.

However, as compared with the RF phase-shifting architecture, the number of components is larger. This leads to more silicon chip area and therefore higher cost. Since the combining of signals and beamforming are performed after mixers, in-band inter-modulations are stronger.

Also, the upper dynamic range of the mixer must be high enough to stand strong interference signals.

Figure 2.10 (c) shows the IF phase shifting architecture. The phase shifters are placed at the first IF stage. The phase-shifted IF signals are combined before down-conversion to baseband. As compared to RF phase shifting architecture, some of the challenges in phase shifter design are relaxed. However, since it needs multiple mixers, this architecture is not a proper option for low cost and low power phased array transceiver.

Figure 2.10 (d) illustrates digital array architecture. Down-converted to a suitable IF frequency, each RF path is digitized by an Analog-to-Digital Converter (ADC) and all outputs are passed to a Digital Signal Processing (DSP) unit, which executes all tasks of beamforming and recovering the desired signal from the noise and undesired interferences. The dynamic ranges of mixers and ADCs must be high enough to withstand the probable strong interferences. In case of WPAN since the data rate may exceed 2 Gbps, very high-speed ADC's are required and to accommodate the required dynamic range each ADC must have a large number of bits which increases the ADC cost and power consumption extensively.

Table 2.6 summarizes the comparison of different phased array architectures in terms of power consumption, chip area and design challenges. To overcome the high path loss and shadowing loss as well as CMOS output power and noise figure limitations at 60 GHz, multiple antennas and phase shifters are required. Considering Table 2.6 the most appropriate configuration to lower the cost and power consumption and achieve a compact CMOS phased array transceiver is the RF phase shifting architecture. However, designing an efficient front-end as well as developing fast, efficient beamforming algorithms are the keys to overcome the phase shifter non-idealities and challenges in RF path.

Table 2.6: Overall Comparison of phased array architectures

Array Architecture	Chip Area(Cost)	Power Consumption	Design Challenge
RF Phase Shifting	Lowest	Low	Efficient Front-End, Low Loss and Linear and continuous Phase Shifter, Variable Gain LNA `
LO Phase Shifting	High	High	Mixer Linearity, LO distribution, On-chip Coupling
IF Phase Shifting	High	High	Linearity, LO Distribution, On-chip Coupling
Digital Array	Highest	Highest	ADC Dynamic Range

2.5.3 On-chip versus Off-chip Antenna

Very short wavelength and therefore the possibility of highly efficient miniaturized antennas is important advantages of the millimeter-wave and sub-millimeter-wave range of frequencies, particularly for the application where the total dimensions of the radio should be very small. This has motivated huge interest in exploring on-chip antenna structures.

Figure 2.11 compares two antenna options, off-chip antenna and on-chip antenna, for a particular millimetre wave link: communications between two integrated wireless devices. In the off-chip configuration, the input of LNA is connected to the antenna through the pad, bonding, and a feed line. In the conventional design approach, the input impedance of the chip and antenna are matched to 50 Ω which in some cases introduces further loss between the antenna and the active part of the system due to adding extra matching elements between the antenna and active element. The challenges in this approach are designing a low loss antenna feed line and overall packaging of the wireless device.

On-chip antenna (especially at millimetre wave frequency bands) where the antenna size is comparable to the chip dimension, becomes an attractive option which eliminates pad and bonding parasititcs from the sensitive nodes of the circuit i.e. receiver input and transmitter output. In Figure 2.11a LNA is directly connected to an on-chip antenna through a minimized matching circuit. This removes the extra loss between the LNA and antenna

which directly contributes to lower the overall noise figure of the system and increases the power amplifier efficiency.

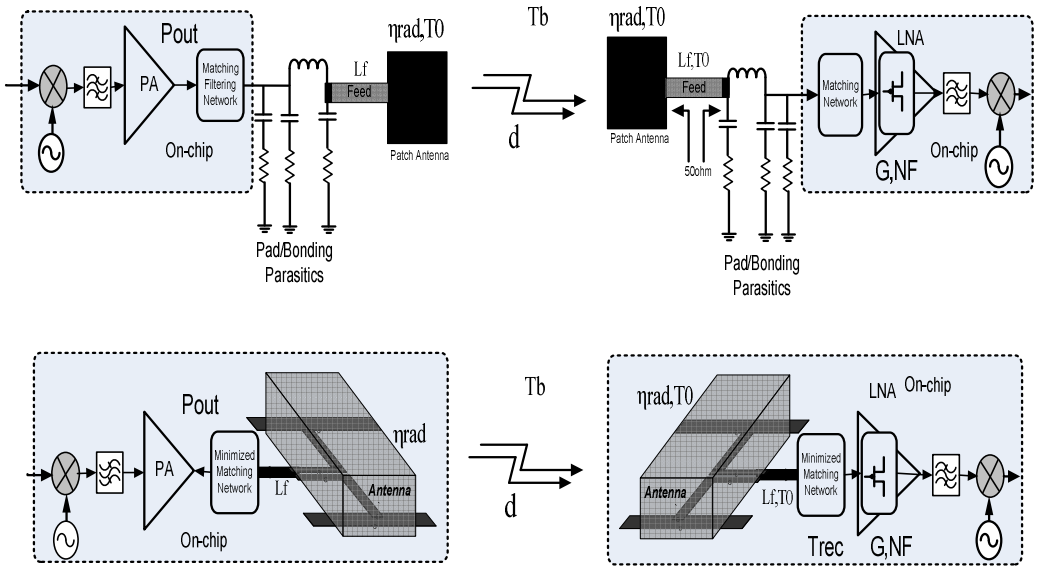


Figure 2.11: On-chip and off-chip millimeter-wave antenna options.

An important feature of this approach is the possibility of direct-matching between the LNA and antenna in the receiver side or the PA and antenna in the transmitter side. This technique further minimizes the required matching circuit components between the antenna and the transceiver and therefore minimizes the associated loss with the matching and feed line between antenna and transceiver. Therefore this improves the system noise figure and power amplifier efficiency. However the challenges are designing a high efficiency antenna on a low resistivity silicon substrate and minimizing the antenna field interaction with the RF circuit on the same substrate. One major obstacle with the on-chip antenna for the lower millimetre wave band is silicon area. The silicon area can be justified for a single antenna and an antenna array of up to 4. However, for an array with a large number of elements is not suitable for on-chip configuration. In these cases integration of the antenna array in the chip package(off-chip) is more feasible. Chapter 3 discusses on-chip antenna in details.

2.6 Off-chip 60GHz Array Antenna

Millimeter-wave antennas have been studied extensively [2],[53][56]. For Fixed Wireless Access (FWA) applications, a high gain antenna is preferred to relax the performance requirements of the front-end elements. A high gain antenna has a narrow beam. Thus, for mobile applications where wide antenna coverage is required, a single high-gain antenna is not an appropriate choice. For millimeter-wave wireless networking applications (R_{max} < 10 m), assuming the base station has been located at the center of the ceiling, almost 2.5 m above the user, the antenna beam coverage should be greater than ±65º to cover almost the entire room or office area. Wide beam coverage and high radiation gain cannot be achieved at the same time unless a *phased array antenna* with beam steering capability is used. Even in this case the 3 dB beamwidth of each array element must be more than 65º to avoid beam steering loss. For such beamwidth the element gain cannot exceed 10.2 dBi [57]. A single rectangle patch antenna which is excited by its fundamental mode (TM_{10}) has about 7 dBi gain and more than 100º beamwidth [58]. A patch antenna is considered a planar radiator that can be integrated easily with the rest of the system; hence, it is widely used for wireless applications. To obtain higher gains one can use an array of the patches. In this section, two different 2 x 2 arrays of patch antennas are designed and compared. The first antenna is designed for the maximum gain and the second one for the maximum beamwidth. A very low loss substrate (RT/duroid -5880) is chosen with tanδ = 0.0009.

Figure 2.12 shows the structures of both antennas. In the first design, the patches are placed at a distance of 0.7λ from each other. The gain of the 2x2 array is 13.1 dBi, and the HPBW of the structure is only 36º. In the second design, the gain is reduced by 3 dB to achieve a wider beamwidth. The gain of the second structure is 10.1 dBi while the HPBW is 65º. Figure 2.12 also shows the polar plots of the gain of both structures in both E-plane and H-plane respectively. Further analysis shows that the radiation efficiency of the wide-beam antenna excluding the matching network is around 90% over the frequency range of 57–63 GHz. Such high values for efficiency have already been reported for millimeter-wave antennas [59].

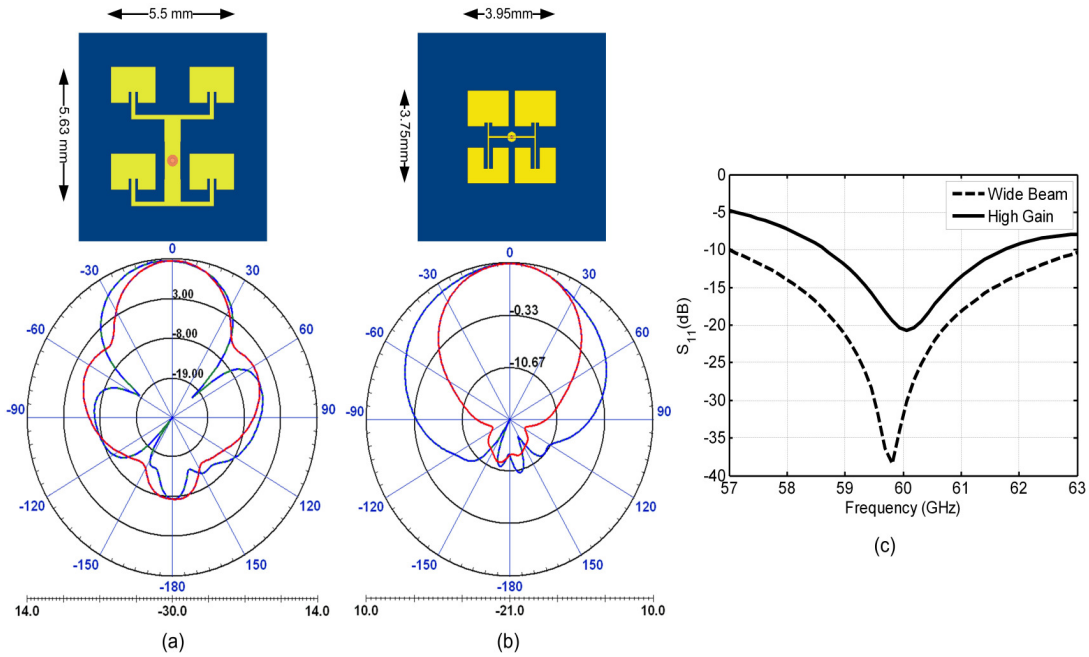


Figure 2.12 Radiation pattern and S11 of 2x2 patch array

2.7 BEAMFORMING

The goal of the beamforming algorithm is to increase the array factor and consequently provide the required *SNR* determined by Bit Error Rate (BER) constraints. The maximum of the array factor for common array systems is equal to the number of array elements; however, as it will be shown, the practical array factor is smaller than this limit due to the variable insertion loss of phase shifter.

In this section, results of two beamforming algorithms for the millimeter-wave receiver phased array antenna are described, and the achieved improvements in the signal to noise ratio at the array output are presented. The details of algorithm has been described in [60][61]. A brief description of the algorithms is presented in Appendix A.

2.7.1 Beamforming Results for LOS Propagation

Figure 2.13 demonstrates the results of the *Aided Beamforming* algorithm using a 3x3 square phased array with ¸ (5 mm) spacing. It is assumed that the equivalent noise bandwidth is 2.16 GHz, the receiver noise figure is 7 dB, the output power of the PA is 2 dBm, and the antenna element is the 2x2 patch array shown in Figure 2.12b. It is also

assumed that the user is moving away from the transmitter while both receiver and transmitter antenna axes are parallel (to the vertical axis). Figure 2.13 compares the results of ideal, fast and slow beamforming for a 9-element array. Slow beamforming is the case where during one iteration of the algorithm user moves more than 1 cm, while in fast beamforming the user's displacement is less than 1mm. In the ideal beamforming the array factor is always equal to 9. The difference between the ideal and fast beamforming when the user is close to the transmitting node r= 3 m is 2 dB. As the distance increases to r= 9 m this difference raises to more than 3.5 dB.

Another important result of Figure 2.13 is that the beamforming gain depends on the received power. So, as the distance between the portable receiver and the transmitting node increases, the performance of the beamforming degrades. Moreover, the beamforming speed also affects the beamforming gain. A version of this algorithm has been successfully applied to a 34 element Ku-band phase array antenna [62]. The duration of each beamforming iteration was measured to be less than 5 ms when a 125 KHz Analog-to-Digital convertor was used.

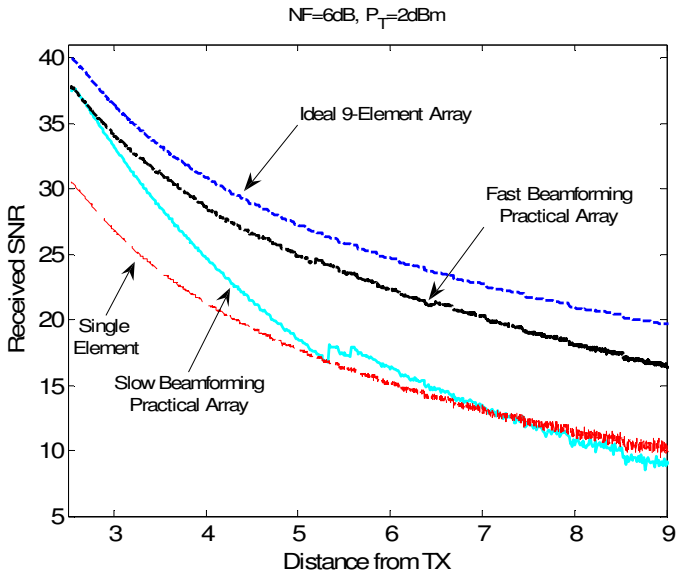


Figure 2.13 Received SNR by a 3×3 square phased array antenna for different beamforming scenarios.

2.7.2 Beamforming Results for NLOS Propagation

In this case, location information is not available and the receiver seeks for the strongest signal by running a beam-search mode (acquisition phase). A direction finding method has been proposed in [63]. Figure 2.14 shows the results of beamforming using a 4×4-element phased array (with λ spacing), when the receiver moves along Paths A and B shown in Figure 2.3. When the receiver is close to the human body (Path A) the width of the fading region is larger (x = -0.4 m to x = 0.35 m) and the shadowing loss varies from 10 dB to 40 dB. Figure 2.14 (a) illustrates that the array output SNR is always above 12 dB. Figure 2.14 (b) shows the improvement in SNR after applying the proposed beamforming algorithm to the phased array antenna. This improvement is due to three factors: using a 16-element array at the access point to increase *EIRPT* , using a 2×2 patch antenna element at the receiver (instead of an isotropic antenna), and the beamforming gain (array factor). While for the LOS section the improvement is 28 dB, it increases up to 42 dB in the shadowing region, implying that the proposed beamforming algorithm has an *excess gain* (up to 14 dB) when shadowing occurs.

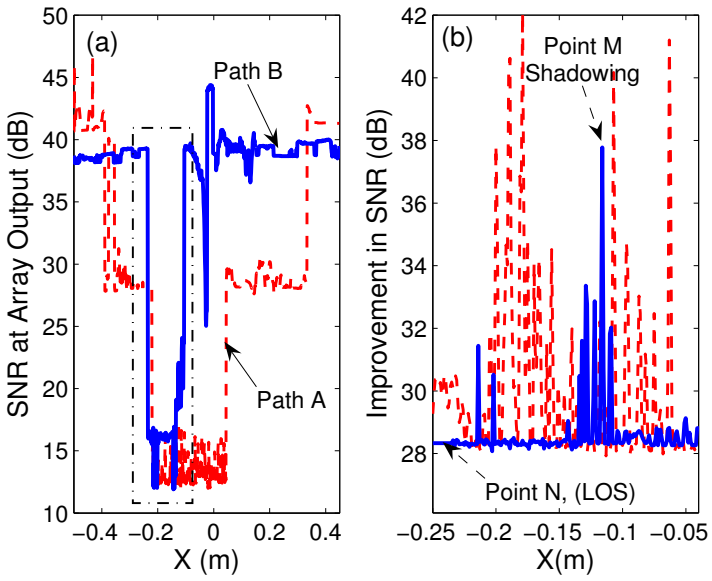


Figure 2.14: Beamforming results for a 4×4 square array with λ spacing. The dashed and solid curves correspond to the receiver location on Path A and Path B in Figure 2-2 (a) SNR at the array output after beamforming. (b) The improvement in SNR due to using phased array for the region shown by a rectangle in Figure 2.14 (a).

Figure 2.15 illustrates how the beamforming algorithm for NLOS propagation works. In this figure the strongest received rays for two receiver positions on Path B, namely *Point M* and *Point N* shown in Figure 2.14 (b), are depicted. Point M is in the shadow region; hence its strongest ray arrives 21 ns later and is 26 dB weaker than that of the point N. Figure 2.15 (b) and (c) show the directions of the two strongest rays which are resolvable in their θ coordinates. If the signal level drops suddenly, the beamforming algorithm finds the strongest ray and steers the array beam to its direction.

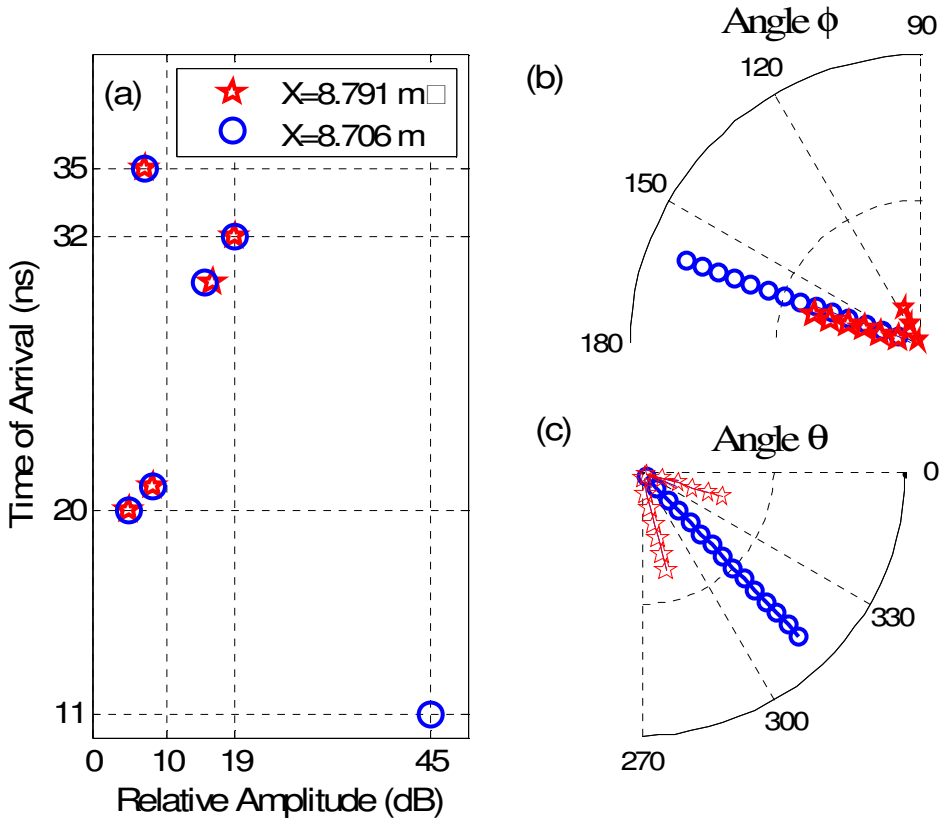


Figure 2.15: characteristics of the strongest received ray for two positions.

2.8 Conclusion

CMOS is a promising technology for low-cost high volume 60 GHz transceivers. However, the fundamental limitations of nanoscale CMOS technology, such as low amplifier gain and output power as well as the fairly high noise figure severely restrict the performance of the single-antenna 60 GHz CMOS systems. It was shown that the adaptive

(intelligent) integrated phased array antenna/ radio system (at both ends) is the most viable approach to provide the required SNR for reliable millimeter-wave network operation. Moreover, radio architectures for single antenna and phased array transceivers were studied. The RF-phase shifting array configuration is a practical and low-cost architecture for 60 GHz applications.

To find the main system design parameters, the propagation of the MMW signal in an indoor environment was studied for LOS and NLOS scenarios, and verified by measurements. It was found that the shadowing loss of a human body can be as high as 40 dB. In this case all LOS rays are absorbed by the human body and only NLOS rays are received.

Simulation results of a fast beamforming algorithm were presented to demonstrate the potentials of phased array for both LOS and multipath signal propagation. In the case of shadowing, the applied beamforming algorithm seeks for the strongest ray, hence an excess gain up to 14 dB can be obtained.

Chapter 3
On-Chip Millimeter-Wave Antennas

3.1 Introduction

Partly or fully on-chip antennas are essential for implementing fully integrated radio systems. An on-chip antenna significantly simplifies the matching network and improves the system performance through reducing the front end loss and noise figure. Thus, considerable amount of research efforts have been devoted to this area [53][64]-[82]. Many of these efforts take advantage of low-cost semiconductor processing technologies, such as SiGe and CMOS aiming to provide fully integrated system solutions at millimeter-wave ultimately [59][82]. So far, most of the reported on-chip antennas have low radiation gains (below -5 dBi) or low radiation efficiency (below 10%). Hence, designing a high-efficiency on-chip antenna is a crucial step towards realizing system-on-chip solutions. To radiate the maximum amount of the input power or to extend the battery life the efficiency of the antenna must be as high as possible, while the antenna size must be as small as possible.

In the low-cost silicon technology the low resistivity of the silicon substrate (0.01-20 Ω-cm) is the main source of loss for passive integrated elements and RF leakage through the substrate. This leakage not only causes crosstalk between noisy digital circuits and sensitive RF and analog circuits, but also reduces the radiation efficiency of the antenna system. Existing integrated antennas on low resistivity silicon substrates [57],[68], [72] are not efficient radiating elements for most wireless communication applications (see **Error! Reference source not found.**). In addition to the silicon low resistivity, restriction on chip area limits the aperture size, and thereby reducing the radiation gain of antenna.

At millimeter-wave band antenna dimension is comparable to the chip-size. Therefore, monolithic integration of active and passive millimeter-wave components on semiconductor substrates become an attractive and practical option. As shown in Table 3.1, the size of a resonant antenna on SiO_2 or Si substrate is reasonable for integration. However the main challenge is low resistivity of silicon substrate which reduces the antenna efficiency. Therefore improving radiation efficiency is one of the challenges. In case of phased array, having the array antenna on the same substrate as transceiver is not a cost-

effective solution unless for frequencies above 100 GHz. Therefore a challenging task is to develop a low cost antenna solution that can be integrated with the transceiver chip easily.

Table 3.1: Resonance antenna dimension on silicon for the new license-free frequency bands

	Free Space $\lambda_0/2$	***Si(ε_r=11.9)*** $\lambda_{eff}/2$	***Sio_2(ε_r=4)*** $\lambda_{eff}/2$
24 GHz	6.25 mm	1.8 mm	3.1 mm
60 GHz	2.5 mm	0.7 mm	1.25 mm
77 GHz	1.85 mm	0.65 mm	0.9 mm
94 GHz	1.6 mm	0.46 mm	0.8 mm
120 GHz	1.25 mm	0.36 mm	0.61 mm

This chapter presents a high radiation efficiency on-chip antenna structure on low resistivity silicon. It also demonstrates the operation of the proposed antenna with an integrated CMOS amplifier at 30 GHz in a TX-RX configuration. Extension of the proposed antenna to a 2×2 array at 60 GHz is described. For the higher number of array antenna elements, an efficient antenna structure on high resistivity silicon for array antenna is presented. The proposed antenna technology can be integrated with the transceiver chip as a low cost packaging solution.

3.2 Silicon IC Substrate Limitations for On-chip Antenna

Figure 1.1 demonstrates the cross section of a typical silicon IC technology. The Si thickness could vary between 300-700 μm. All the metal layers are placed on top of the silicon and embedded in silicon dioxide. The maximum distance between the lowest metal and top metal varies between 7 to 15 μm. The biggest disadvantage of the silicon IC substarte for implementation of passives elements including antenna is low resistivity of substrate. This is the main source of loss in the passive components. Some on-chip antenna configurations can be isolated from the low resistivity silicon by using the lowest metal as a

shield layer, however the limited distance between the bottom and top metal is another limitation for the antenna implementation.

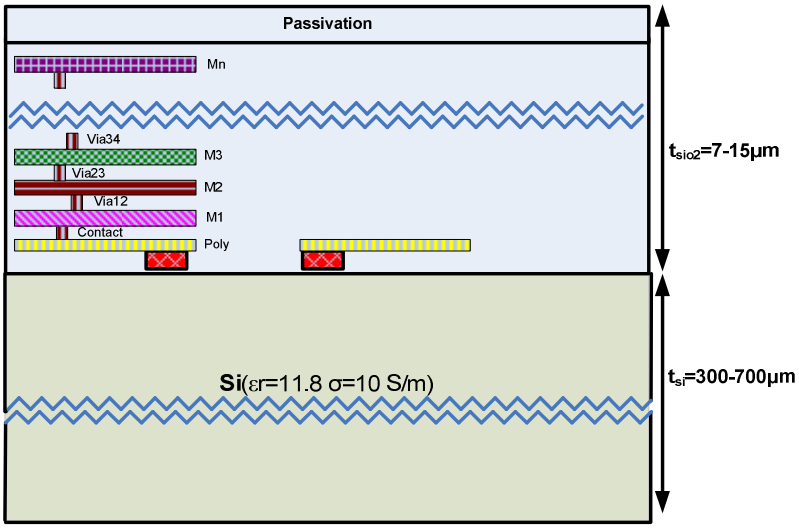


Figure 3.1: Cross section of a typical silicon process.

Radiation efficiency of an antenna, η, is defined as:

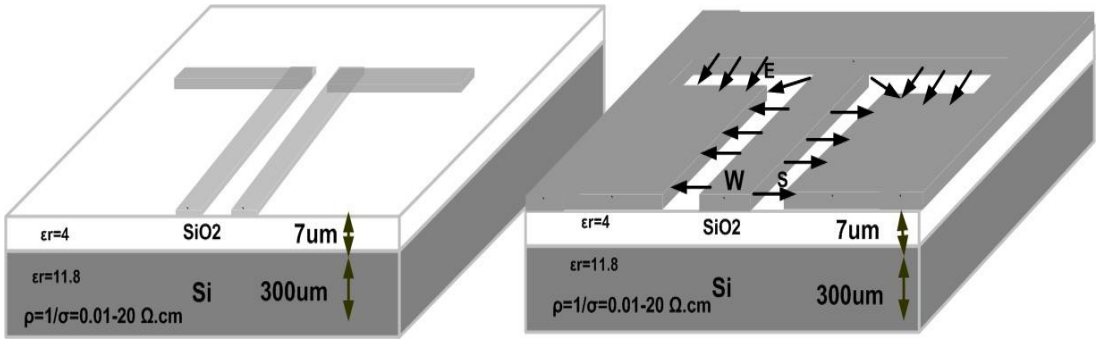
$$\eta = \frac{P_{rad}}{P_{in}} \qquad (3\text{-}1)$$

Where, P_{rad} and P_{in} denote the radiated power and the input power to the antenna, respectively. Radiation efficiency is one of the important characteristics of an antenna, which represents the percentage portion of the input power delivered to the outer space by antenna. Any improvement in the antenna efficiency results in a larger transmission range for a fixed input power, or less power consumption (more battery life) for a fixed transmission range.

3.2.1 On-chip Dipole versus On-chip Slot Antenna

In a planar multi layer substrate such as integrated circuit technologies, two common techniques for implementing the antennas are dipole and slot antenna. The slot antenna consists of a radiator formed by cutting a narrow slot in a large metallic surface. Its complimentary (dual) structure is a dipole antenna formed by two metallic traces. Important differences exist between the dipole antenna and its complementary, slot antenna. The electric and magnetic fields are interchanged. In the case of the dipole antenna, the electric lines are horizontal while the magnetic lines form loops in the vertical plane. With the slot

antenna, the magnetic lines are horizontal and the electric lines are vertical. The electric lines are built up across the narrow dimensions of the slot. Assuming a half wave dipole and slot antenna are integrated directly on a silicon substrate as shown in Figure 3.2 , radiation efficiency of dipole and slot versus substrate resistivity and thickness are extracted using ADS Momentum and shown in Figure 3.3.



(a) (b)

Figure 3.2 Two common configurations for integrated antenna on silicon. (a) Dipole Antenna. (b) Slot Antenna.

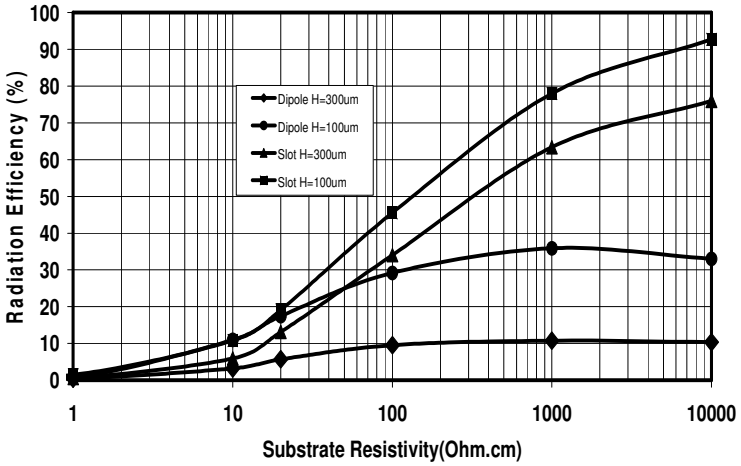


Figure 3.3 Radiation efficiency of a 30 GHz dipole and slot antenna versus substrate resistivity and thickness (H)

3.3 Common Structures for On-Chip Antennas

Figure 3.4 illustrates two common configurations for the implementation of the integrated antenna on a low-resistivity silicon substrate: (a) antenna fabricated on normal substrate, and (b) antenna on micro-machined substrate. The main drawbacks of the first approach are the low radiation efficiency due to the substrate loss and leakage to other RF circuits on the same substrate through the low-resistivity silicon substrate. Reported numbers for the radiation efficiency of this configuration are less than 10% [72][75]. To improve the radiation efficiency of the on-chip antenna part of the lossy silicon substrate is removed by bulk micro-machining techniques, as shown in Figure 3.4 (b) [81]-[82]. It requires a more complex fabrication process and can cause cross-talk to other RF circuits on the same substrate. Also the antenna size increases and consequently increases the silicon cost.

Thus, a new structure is proposed to prevent the drawbacks of the conventional structures. The proposed structure is described in the next Section.

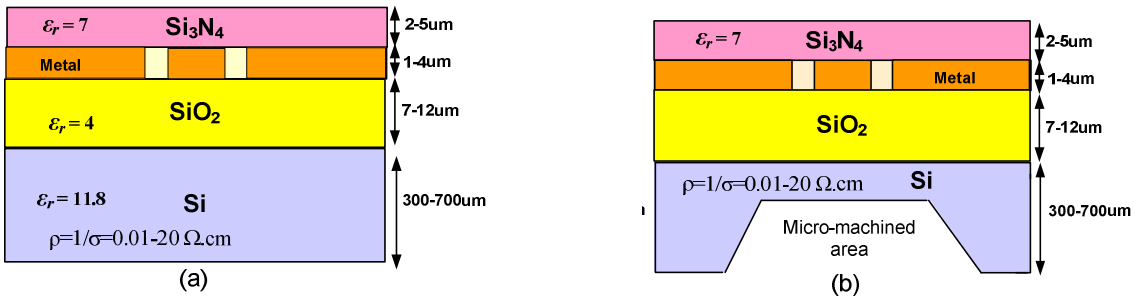


Figure 3.4: Two common configurations for integrated antenna on silicon. (a) Antenna on normal substrate. (b) Antenna on micro-machined substrate.

3.4 Proposed On-Chip Antenna Structure

Figure 3.5 illustrates the proposed configuration for the integrated on-chip antenna. The proposed structure consists of:

- Silicon substrate
- Cavity and shield layer
- H-Slot aperture
- Passivation layer
- Dielectric Resonator

The thickness of silicon substrate is about 300 μm after back grinding. The slot aperture is implemented on the top metal layer (MT) of the silicon technology. The lowest metal layer (M1) is connected to the top ground plane through via holes and behaves like a shield. By shielding the antenna from lossy silicon substrate, the antenna substrate is limited to silicon dioxide (SiO_2) and the intermediate dielectric layers between metal layers. Also a cavity is formed under the slot antenna. In integrated silicon technologies, usually up to 9 metal layers and thin film silicon dioxide in between exist for the interconnection and routing. The maximum distance between the top and bottom metal layer depending on the process technology and metallization option varies from 7 to 15 μm. Thus the maximum thickness of cavity in the proposed antenna configuration is limited. Generally, a silicon nitride (Si_3N_4) layer for passivation purpose with the thickness of 2-5 μm is placed on top of all layers except input/output pads to isolate and protect top level interconnections from outside world. In this work, it is shown that the antenna part of the chip can be treated as pads and passivation layer can be removed for more efficient coupling to the dielectric resonator. Finally, a dielectric layer with a large permittivity is placed on top of the chip to increase the radiation efficiency and improve the antenna matching.

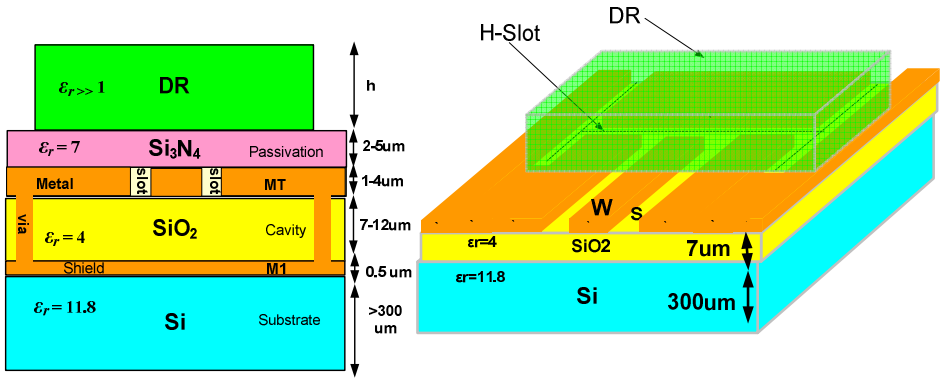


Figure 3.5: On-chip cavity backed slot antenna with dielectric resonator on top. Cross section and 3D structure.

3.4.1 DR Resonance Frequency and Analysis of Different Modes

The proposed antenna structure operates as a dielectric resonator antenna, excited by the on-chip slot radiator. Although the idea of dielectric resonator antenna is not new, the novelty of the proposed structure is applying the DRA to overcome the challenge of low radiation efficiency in lossy silicon substrate in millimeter-wave band. Dielectric resonators (DRs) made of high dielectric constant material are well known as a high Q-factor circuit element. Therefore, they have been used as resonators in microwave filters and oscillators. DRs have also been used as an antenna element. It has been proven experimentally that these elements are efficient radiators [86].

The proposed structure is a dielectric resonator antenna (DRA) structure, excited by a slot radiator. The main advantages of this approach are:

1) Isolation from the substrate.
2) Radiation efficiency enhancement.
3) Miniaturized size. This feature is achievable by using high dielectric constant materials for DR part of the antenna. The DR can be considered as part of the chip package.
4) A DRA can be fabricated in various shapes such as rectangular, cylindrical, hemispherical, etc., which allows more flexibility in antenna and package design.
5) In a DRA structure, the dielectric contains the antenna's near field and therefore, prevents it from interfering with other nearby antennas or circuits, making it suitable for miniaturized integrated antenna transceiver and array applications.

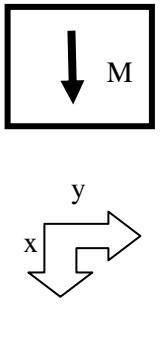
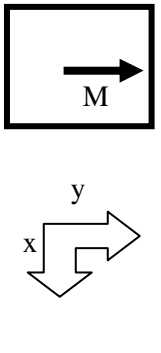
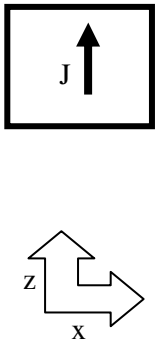
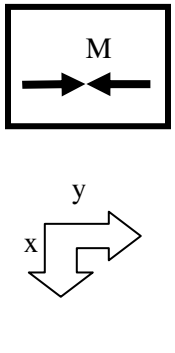
One of the attractive features of a DRA is that it can assume any simple shapes such as circular and rectangular. Rectangular DRA is easier to fabricate and the most versatile since it has three degrees of freedom. For any given resonant frequency and fixed dielectric constant, two of three dimensions of the rectangular DRA can be chosen independently.

To achieve a good efficiency, proper modes have to be excited. Therefore, the proper excitation must be used, which requires knowledge of the field distribution of the desired mode to the proper excitation mechanism. HFSS eigen mode analysis was used to find the resonant modes and field distribution. Then, by using the dipole representation of modes

presented by [87], one can easily predict the radiation and non radiation modes, radiation pattern, and appropriate coupling method to these modes.

Table 3.2 shows the resonant modes for three different heights of 1.15×1.6×h of a rectangular DR with ε_r=38.

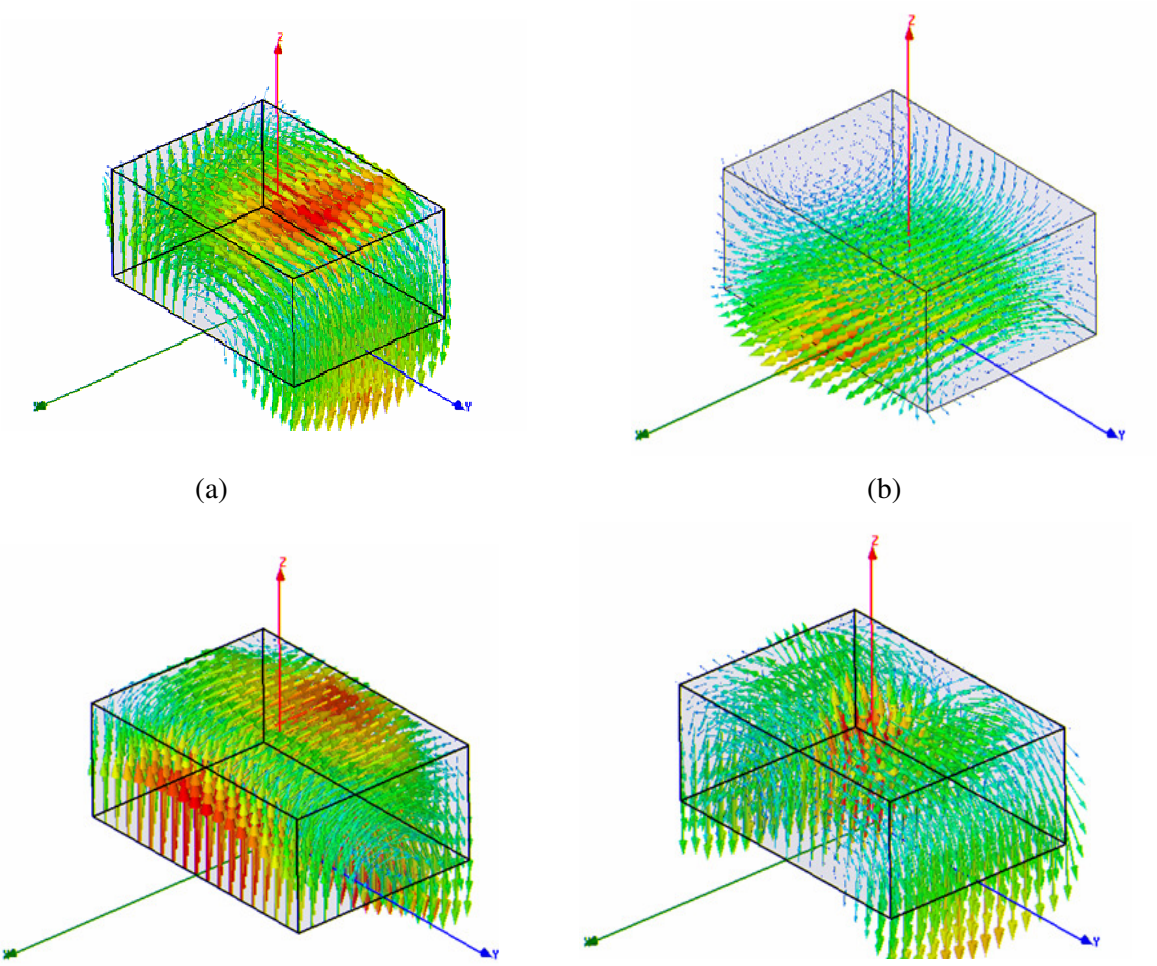
Table 3.2: Resonant modes for three different heights (1.15×1.6×h) of a rectangular DR (εr=38)

Resonance Modes	1	2	3	4	5
F(GHz) h=0.6 mm	28.63	31.42	39.44	39.76	42.2
F(GHz) h=0.55 mm	30	32.57	40.54	40.75	43.96
F(GHz) h=0.5 mm	31.43	34	41.69	41.89	45.63
					

The variation of antenna dimensions strongly influenced resonant mode formation in the rectangular DRAs. Increasing the DRA height causes a decrease in the resonant frequency of the mode without altering the nature of the mode. For example, changing the height from 0.5 mm to 0.6 mm causes a decrease in the resonant frequencies by about 2.5 GHz, and this effect can be very useful for tuning the frequency of the desirable modes in a DRA. In addition, an increase of the DRA height also causes a weakening of some of the

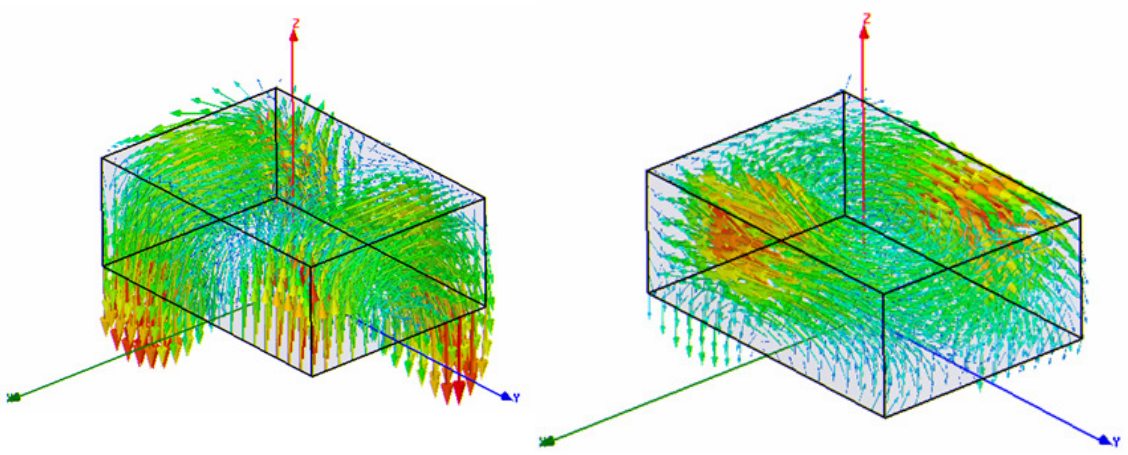
modes. Increasing the DRA width not only decreases the resonant frequencies, but also causes additional new modes to appear.

Figure 3.6(a) and (b) shows the electric and magnetic field distribution of the first mode of the DR on PEC with h=0.55 mm. The electric field distribution of the higher order modes (m=2-5) are represented in Figure 3.6(c) to (f).



(a) (b)

(c) (d)



(e) (f)

Figure 3.6: Rectangular DR modes: (a) Electric field distribution. (b) Magnetic field distribution. (c) Electric field distribution of the second mode. (d) Electric field distribution of the third mode. (e) Electric field distribution of the fourth mode. (f) Electric field distribution of the fifth mode.

3.5 H-Slot Antenna and Dielectric Resonator

H-slot is an aperture-type electrically small antenna. A slot aperture can be end-loaded to reduce its overall length at a given resonance frequency [88]. For example, in this work the maximum size of the slot antenna is 1.15 mm and the measured resonance frequency is 35 GHz. Thus, the overall length of the antenna is almost $\lambda_0/8$, or 4 times smaller than a half-wavelength dipole operating at the same frequency. The radiation efficiency of such an electrically small antenna is negligible (less than 1%). To improve the radiation efficiency of the integrated antenna, a layer of high dielectric constant material is added on top of the slot aperture to create a rectangular DR antenna [79][86]. The slot behaves like a magnetic current, which excites the first order mode of the dielectric resonator in the proposed structure. Thus, the integrated antenna can radiate a larger portion of the input power.

Placing DR improves the radiation efficiency through the following mechanisms:

1) High dielectric constant material on top changes the field distribution and therefore the field will be concentrated in dielectric material on top.

2) Dielectric resonator acts as an antenna excited by slot if designed and configured properly.

3) Dielectric resonator with high dielectric constant tends to confine near-field energy inside dielectric and therefore reduces the field intensity and loss inside the lossy substrate. This feature also reduces the mutual coupling between adjacent elements in an array of such antenna elements. Amongst different shapes of DR, the rectangular DR has practical advantages because it is easier to fabricate and has four design parameters, i.e. length, width, height, and dielectric constant [86],[89]. The length, width, height, and dielectric constant of the DR used in this work, are respectively 1.65 mm, 1.1 mm, 0.5 mm, and 38.

3.5.1 Simulation Results

The H-slot was designed and optimized to have a resonance frequency close to that of the rectangular DR. Figure 3.7 shows the *E* field distribution of the whole antenna structure including the DR simulated by HFSS. It is seen that the DR is strongly excited by the H-slot antenna, and the majority of the *E* field has been confined in the DR. Figure 3.8(a) shows the simulated reflection coefficient of the on-chip antenna with DR. The resonant frequency is 34.5 GHz which is 1.4 GHz less than the resonant frequency of an isolated DR with the same size as the one used in this work. This difference is caused by the coupling between the chip and antenna, and the finite ground plane. Furthermore, Figure 3.8 (a) shows that the 10 dB bandwidth of the on-chip antenna is 3 GHz. The 3-D radiation pattern and the 2-D radiation pattern (in the φ=0 plane of the antenna) are shown in Figure 3.8 (b) and (c). It is seen that the antenna pattern covers the upper half plane and the maximum gain of the antenna structure is 1.06 dBi. Furthermore, the half-power beamwidth of the on-chip antenna exceeds 140º.

It is interesting to calculate the theoretical minimum quality factor, or Chu's limit for this antenna structure, given by [91]:

$$Q_{Chu} = \frac{1}{(kL)} + \frac{1}{(kL)^3} \qquad (3\text{-}2)$$

where L is the (largest) antenna size. For L =1.15 mm and k= $2\pi/\lambda_0$ at 34.5 GHz, the Chu's limit is 2.9. Replacing L by 1.6 mm which is the largest DR size, gives Q_{Chu}=1.6. The measured Q factors in next section are above the Chu's limit.

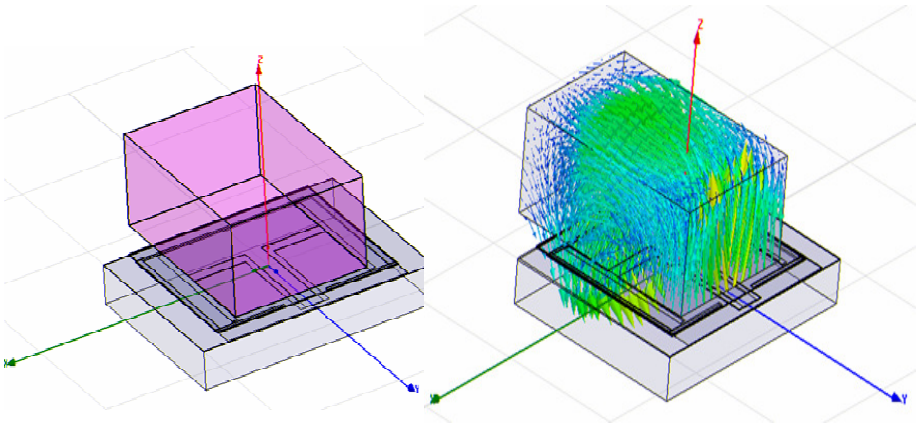
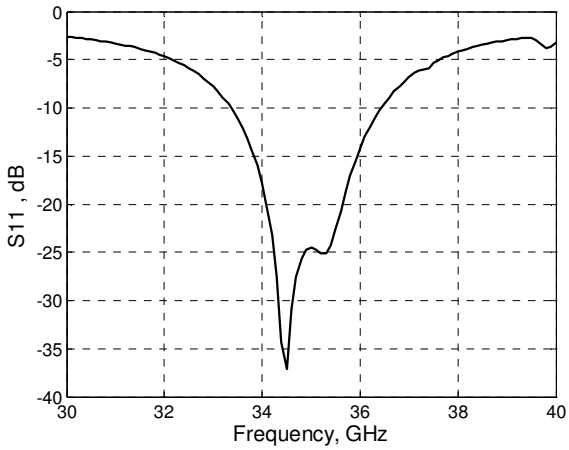
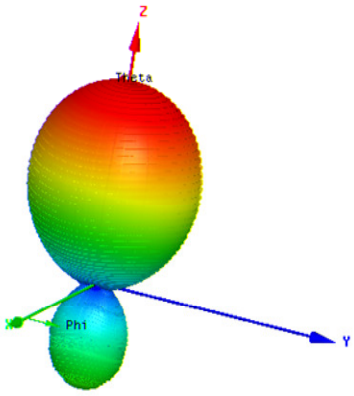


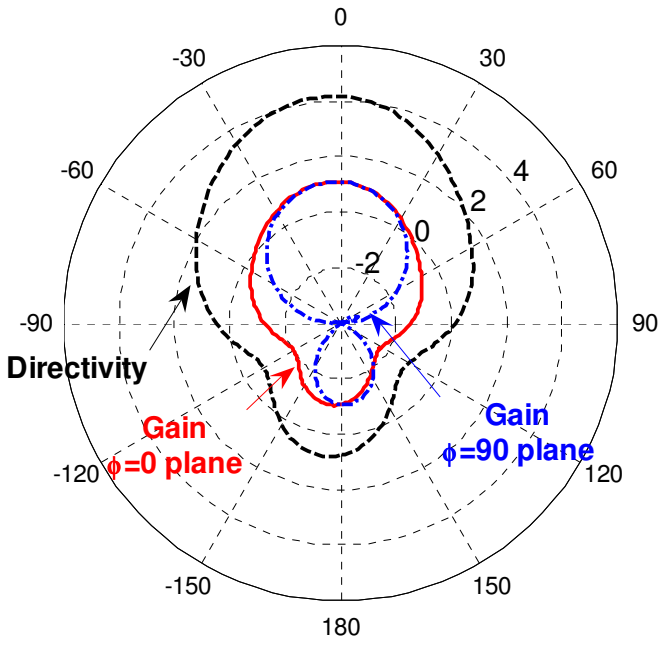
Figure 3.7: (a) Modeling the on-chip H-slot antenna with DR. (b) The E field distribution which shows the radiating mode has been excited.



(a)



(b)



(c)

Figure 3.8: (a) Simulated reflection coefficient of the on-chip antenna. (b) 3D radiation pattern of on-chip antenna at 34.5 GHz. (c) 2D radiation pattern and directivity of the on-chip antenna.

3.6 Measurement Results

Figure 3.9(a) shows the die micrograph of the fabricated H-slot antenna, probed by Cascade Micro-Tech CPW probe. The H-slot antenna was implemented using IBM SiGe5AM process, described in Figure 3.5. The dimensions of the H-slot are shown in this figure. Two vertical slots in Figure 3.9 (a), which constitute the radiating section of the antenna, have 500 μm length and 100 μm width. The horizontal sections on top and bottom, which load the radiating slots, are 1 mm long and their width is 50 μm. While the allocated silicon area for the implementation of antenna is 2 mm×1.5 mm, the largest antenna dimension is only 1.15 mm. The feed network, shown in Figure 3.9 (a), is a CPW line with 850 μm length which is probed with Micro-tech CPW probes for test purpose. In the final on-chip transceiver configuration, the input CPW line of the antenna will be connected to on-chip LNA/ power amplifier. This can be done through an on-chip switch if the device is operating as a transceiver with a single antenna.

In Figure 3.9 (b) a rectangular high dielectric constant layer is placed over the passivation layer to improve the radiation efficiency. The DR used in this work is S38 by TRAK Ceramics with a dielectric constant of 38±1 and a size of a=1.6 mm, b=1.15 mm, and h= 0.5 mm [90]. Nine samples of on-chip antenna were fabricated and measured: four samples with Passivation Layer (PL) and five without this layer. In the following, the measured results of the different parameters of the fabricated antennas are presented.

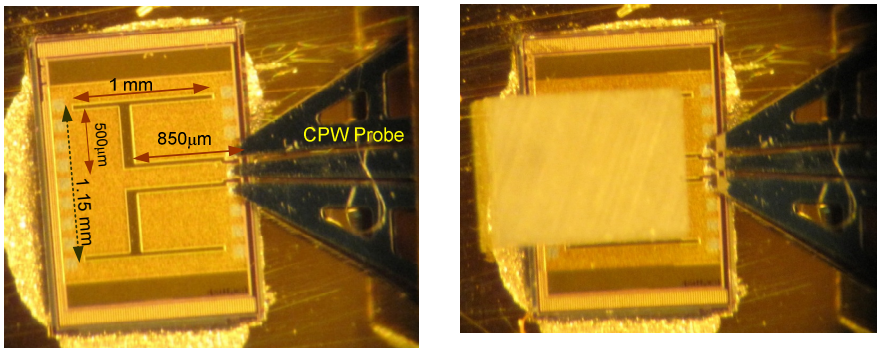


Figure 3.9: (a) The dimensions of the slots on the metal. (b) Die micrograph of the H-shape slot with DR

3.6.1 Resonance Frequency

The first test aimed to find the resonance frequency of the antenna with and without the dielectric resonator. Figure 3.10 shows the measured reflection coefficient (S_{11}) of different samples of on-chip antenna with Passivation Layer (PL) over the frequency range of 20-40 GHz. The resonance frequency of the H-slot antenna *without* DR for all samples varied from 36.7 to 36.9 GHz. The 10 dB bandwidth varied from 2.2 to 2.4 GHz. Placing DR reduced the resonance frequency by more than 1.6 GHz, when the DR covered both arms of the H-slot aperture as shown in Figure 3.9 (b). The resonance frequency in this configuration varied from 35 to 35.4 GHz.

Figure 3.11 shows the effect of PL on the resonance frequency of the on-chip antenna. Removing PL decreases the resonance frequency. The resonance frequency of the sample without PL shown in this figure is 34.8 GHz with DR and 36.5 GHz without DR.

Furthermore, as had been predicted, a better matching at the resonant frequency is observed which is predictable.

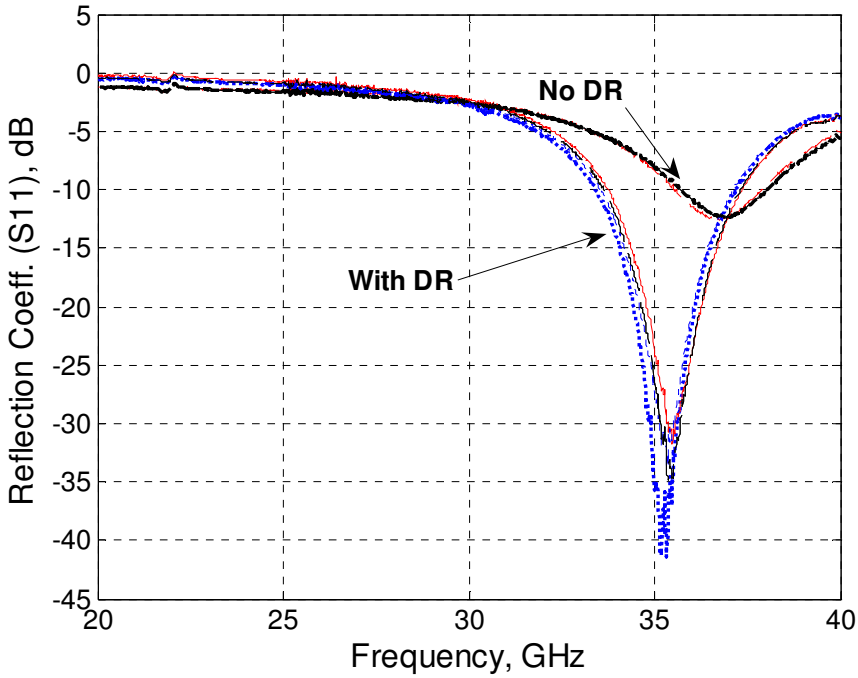


Figure 3.10: Measured reflection coefficient of the on-chip antenna with and without DR for the configurations shown in Figure 3.9 (b).

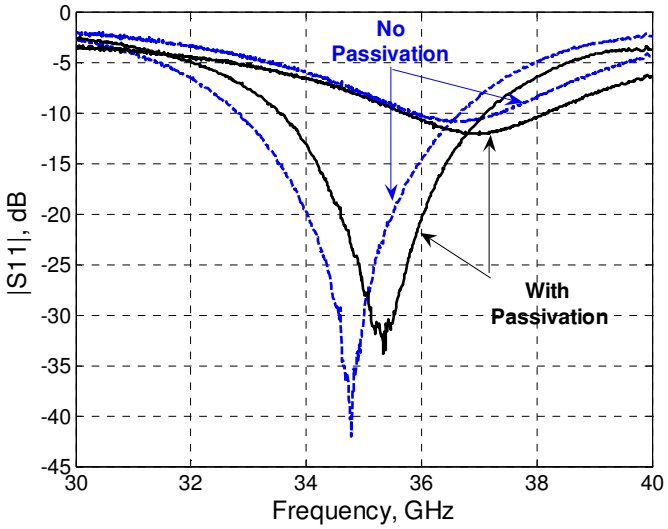


Figure 3.11: Measured reflection coefficient of the on-chip antenna with and without Passivation Layer (with and without DR).

3.6.2 Changing the DR Position

The resonance frequency and the bandwidth of the antenna are both sensitive to the DR position. Figure 3.12 shows that by changing the DR position atop the H-slot antenna (mainly rotating the DR around the axis normal to antenna plane) the resonance frequency varies from 33.5 to 36.4 GHz (more than 8%). Furthermore, it is possible to see more than one resonance frequency for certain positions of DR.

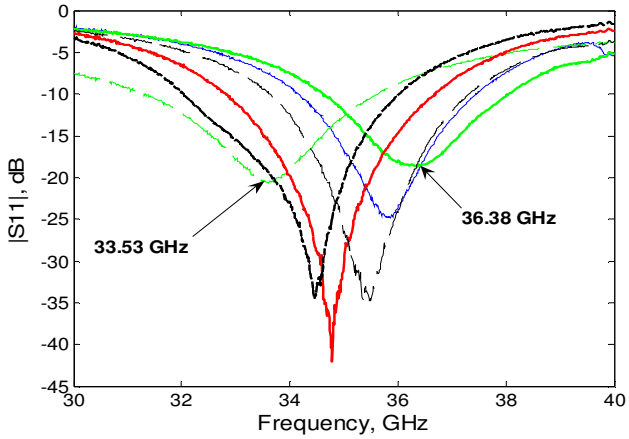


Figure 3.12: Shift of the resonance frequency by changing the DR position.

3.6.3 Radiation Pattern Measurement

Since the CPW measurement probe is mounted on the chip and the whole structure is fixed, the antenna cannot be rotated for the pattern measurement. To measure the radiation pattern one can rotate the Standard Gain Horn antenna (SGH) above the chip and measure the received signal at different angles. The radiation pattern measurement setup is shown in Figure 3.13.

The power level of the received signal by the horn antenna was recorded for different angular positions. The recorded data was calibrated using the SGH pattern, to find the radiation pattern of the desired structure. The rods and everything around the measurement setup were covered with wave absorbers to avoid any reflected signal. With this method, only the upper-hemisphere radiation pattern of the antenna can be measured. Using the described test set-up the forward radiation pattern at φ=90º plane (y-z plane) was measured. The simulation and measurement results, shown in Figure 3.14, are in good agreement. The measured half-power beamwidth of the on-chip antenna is close to 110° compared to the

simulated value of 140°. Part of this difference is due to the larger ground size of the fabricated samples. The rest can be explained by the limited number of the measured points (15 points), and the measurement error.

3.6.4 Measured Gain and Improvement in the Radiation Gain and Matching

The set-up shown in Figure 3.13 was used to measure the approximate gain of the antenna. The size of the SGH aperture used in this test was 2.33 cm ×1.73 cm. For these dimensions the Fraunhofer distance ($d = 2D^2/\lambda, \quad D^2 = x^2 + y^2$) at 35 GHz is 19.5 cm [92]. Thus, the distance between the horn antenna and the on-chip antenna was set to 20 cm to satisfy the far-field condition. Port 1 of the network analyzer was connected to SGH via a coaxial to waveguide adaptor, and Port 2 to the CPW probe which fed the on-chip antenna. All scattering parameters were measured with and without the DR (Figure 3.15). The return loss of SGH was below 10 dB over 30-40 GHz range. The measured S_{12} could be increased significantly by overlaying the DR on the H-slot antenna. Figure 3.16(a) shows the improvement in the received power within the 10 dB bandwidth of the on-chip antenna (33-37 GHz). The improvement varied from 6 dB to 17 dB (after removing the effect of the measurement background noise). The average improvement over the whole 10 dB bandwidth was 12.7 dB with PL and 13.7 dB without PL. The S-parameter measurements in Figure 3.15 were used to estimate the gain of the on-chip antenna through the following relation [94]:

$$\frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} = G_{Horn}\, G_{On-Chip} \left(\frac{\lambda}{4\pi R}\right)^2 \qquad (3\text{-}3)$$

In (3-3) it has been assumed that all sources of insertion loss from port 1 to port 2 of VNA have been compensated, otherwise the uncompensated insertion loss in the test set-up must be added to right-side of (3-3).

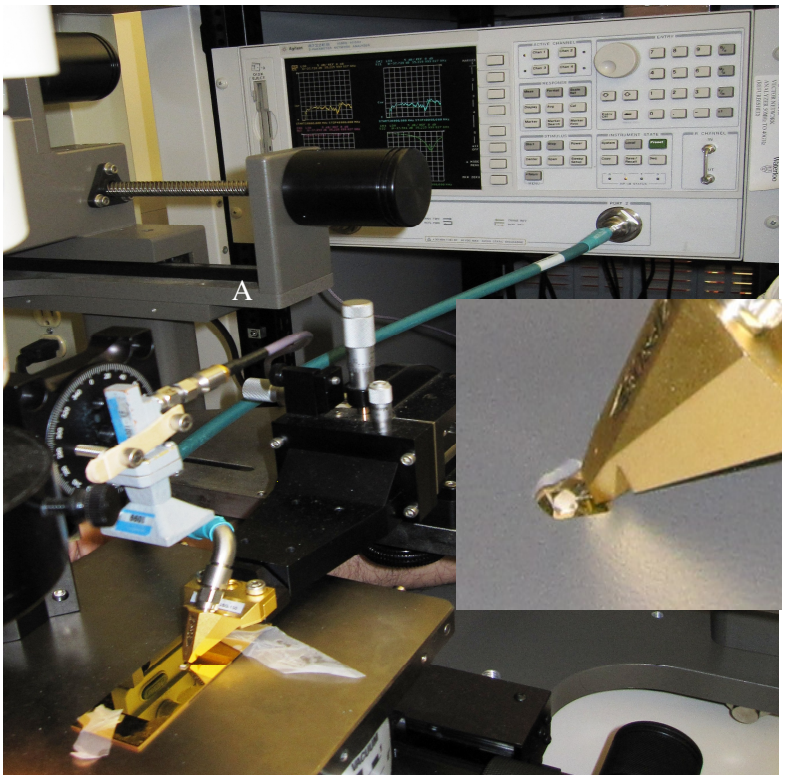


Figure 3.13: Radiation pattern measurement set-up for the on-chip antenna. The inset shows the CPW probe coupled to the antenna under test surrounded by wave absorber.

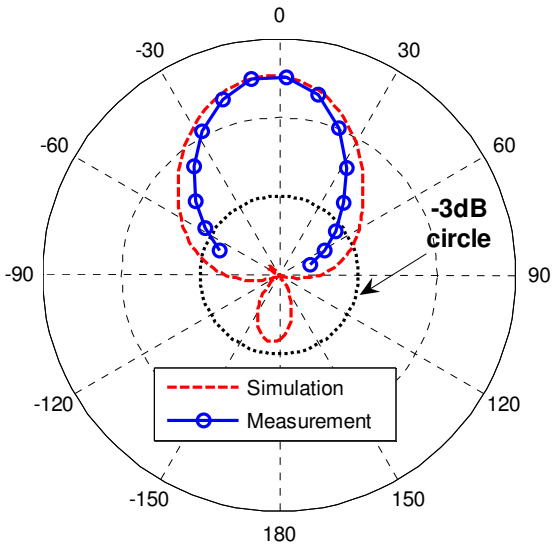


Figure 3.14: Measured and simulated radiation patterns of the on-chip antenna at yz plane at 35 GHz.

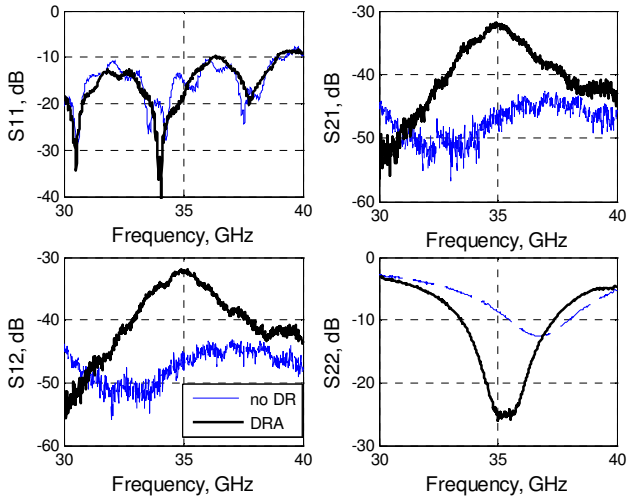
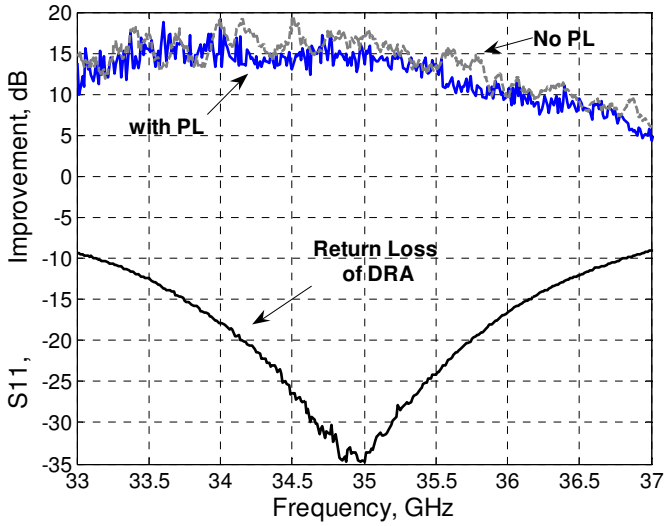
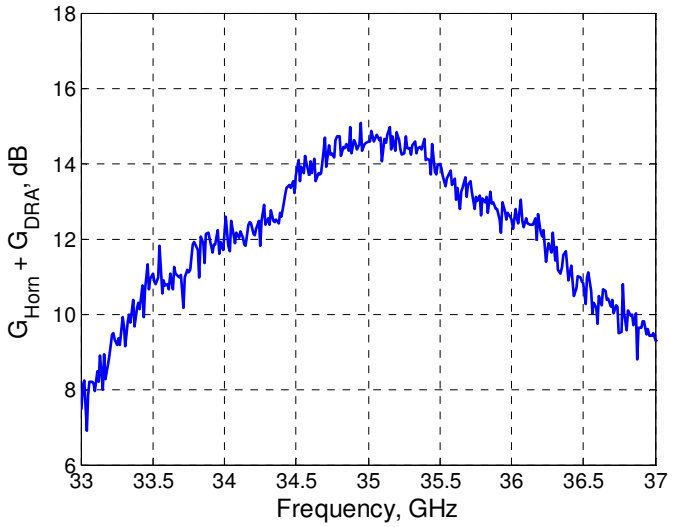


Figure 3.15: Measured scattering parameters of the horn and on-chip antenna with/without DR.

Figure 3.16(b) shows the unbiased product of horn and on-chip antenna gains derived from (3-3) and Figure 3-17, which is 15 dBi at 35 GHz. The maximum gain of horn antenna at 35 GHz is 15.5 dBi. However, considering polarization mismatch and 1 dB insertion loss for the coaxial to waveguide adaptor which connects the horn antenna to the RF cable of the VNA port 1, the measured gain of the on-chip antenna at 35 GHz is certainly above 0.5 dBi, which is in good agreement with the simulated gain of 1.06 dBi in Figure 3.8(c).



(a)

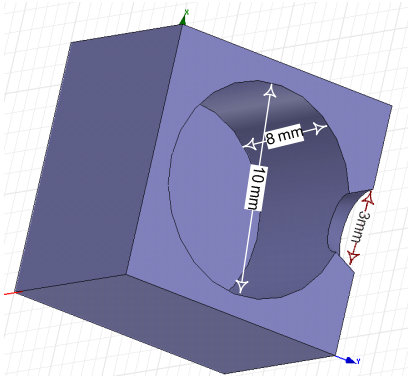


(b)

Figure 3.16: (a) Measured improvement in the received power by the horn antenna after laying the DR on the H-slot, over the 10 dB bandwidth of the antenna. (b) Summation of horn gain and on-chip antenna gain derived from S-parameter measurements in Figure 3.15.

3.6.5 Efficiency Measurement

In this test, Wheeler method is used to measure the efficiency of the on-chip antenna [83][85]. This is an approximate method for electrically small antennas (especially for CPW-fed antennas). The Wheeler cap used in this work was comprised of a cylindrical cavity, with 10 mm diameter and 8 mm depth, grooved in an Aluminum cube (Figure 3.17). A small opening was made for the CPW probe which was contacted to ground lines during measurements.



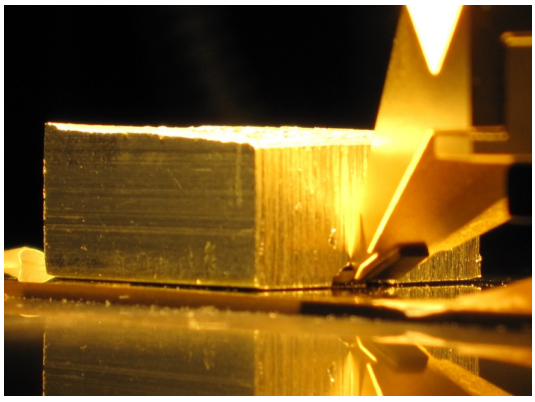


Figure 3.17: (a) The Wheeler cap design used for the efficiency measurement experiment. (b) Wheeler cap placed on the antenna.

To apply Wheeler method for antenna efficiency measurement, the reflection coefficient (S_{11}) of the on-chip antenna system (with DR) was measured twice: with and without the Wheeler cap. Then 10 dB fractional bandwidth of the antenna (*BW*) was calculated in each case, and then the *Q* factor was found from the following relation [93].

$$Q. = \frac{v-1}{\sqrt{v}BW} \tag{3-4}$$

where *v* is the Voltage Standing Wave Ratio (VSWR), which is related to the return loss (RL) by:

$$v = VSWR = \frac{\sqrt{RL}+1}{\sqrt{RL}-1} \tag{3-5}$$

For RL =10 dB, *v* is equal to 1.925 (~2). Let Q_W and Q_0 denote the *Q* factors of the DR antenna with and without Wheeler cap. Then the efficiency at the resonance frequency is calculated from [86]:

$$\eta = 1 - \frac{Q_0}{Q_W} \tag{3-6}$$

Figure 3.18 shows the results of the efficiency measurement test for the antenna with PL. The 10 dB fractional bandwidth of the DR antenna is 12% (4.15 GHz bandwidth). With Wheeler cap on the antenna this bandwidth reduces to 7.6%. The values of Q_0 and Q_W are calculated as 5.4 and 8.7. Thus, the efficiency for the DR antenna with PL is more than 38%.

Figure 3.19 shows the results of efficiency measurement test for the antenna without PL. The 10 dB fractional bandwidth of the DR antenna reduced to 11.2 %. With Wheeler cap this bandwidth reduced to 5.8%. The values of Q_0 and Q_W are calculated as 5.9 and 11.5. Thus the radiation efficiency is more than 48%. These results show that removing the passivation layer increases the on-chip antenna efficiency by approximately 10%.

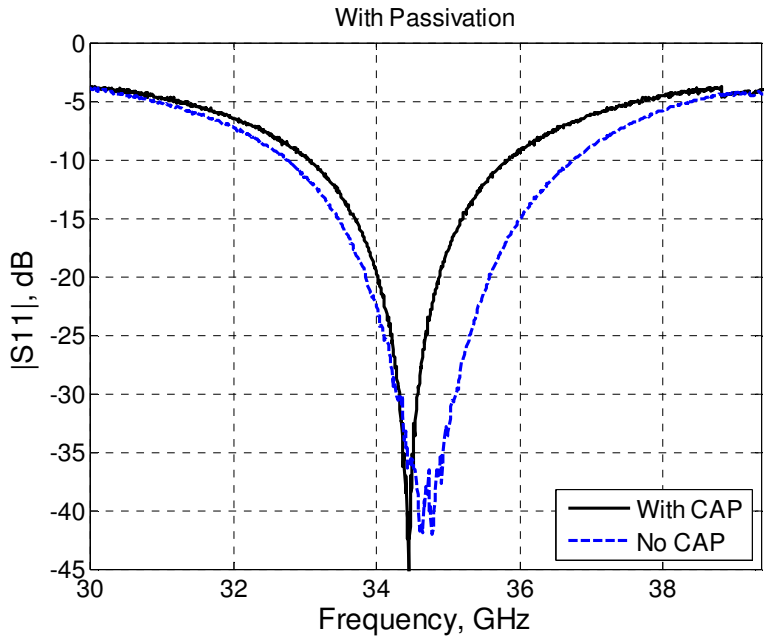


Figure 3.18: Wheeler test results for the on-chip antenna with PL.

To find the efficiency of the proposed on-chip antenna at other frequencies, an EM simulator (HFSS) is used which can integrate the received power on a closed surface. Measured results were used to modify the antenna model. Figure 3.20 shows the simulated efficiency with and without PL for a frequency range of 33 to 37 GHz. The maximum efficiency with PL is 49% at 35 GHz and without PL it is 59% which happens at 34.9 GHz. In full agreement with measured results the efficiency increases by 10% if the PL is removed.

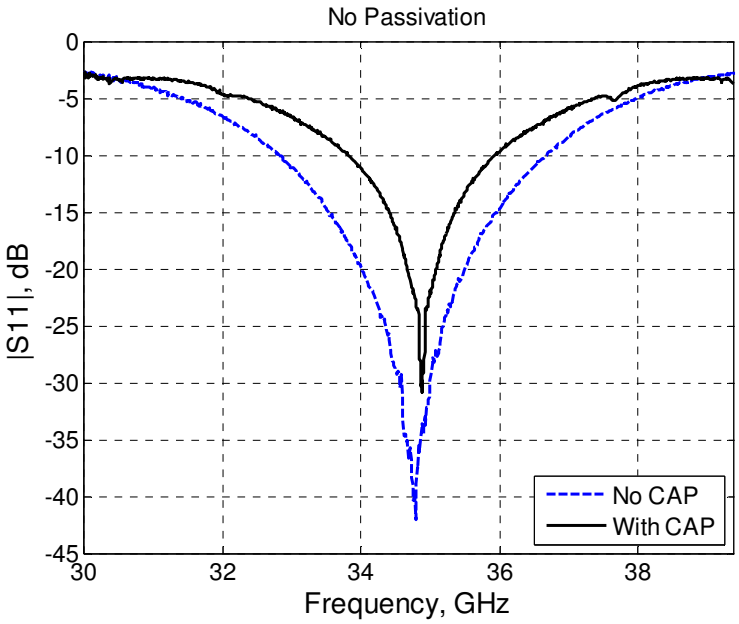


Figure 3.19: Wheeler test results for the on-chip antenna without PL.

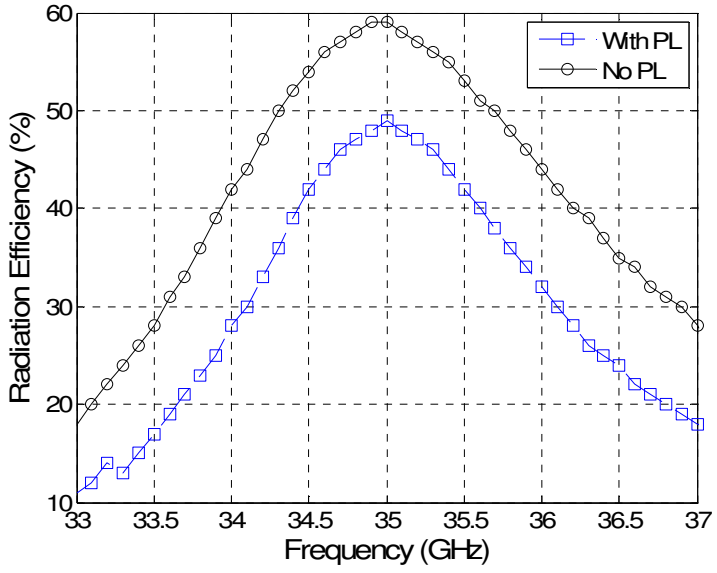


Figure 3.20: Radiation efficiency of the entire structure (DR antenna plus chip) which shows a maximum at the resonance frequency

3.6.6 Discussion

Error! Reference source not found. presents a summary and comparison of some of reported on-chip antennas with the proposed antenna structure.

Table 3.3: Comparison of the proposed on-chip antenna with other reported on-chip antennas

Antenna Type	**Substrate**	**Freq. (GHz)**	**L/λg**	**Antenna Gain or Efficiency**	**REF**
Dipole	Si 10 Ω.cm	18	0.42	-56 dB (Transmission gain)	**[64]**
Dipole	Si 5 Ω.cm	18	0.42	-65 dB (Transmission gain)	[66]
Dipole	Si 20 Ω.cm	24	0.55	-45 dB (Transmission gain)	[67]
Dipole	Si 10 Ω.cm	24	0.85	-8 dBi	[68]
Inverted F	Si 10 Ω.cm	61	1.4	-19 dBi η=3.5%	[72]
CPW Fed Yagi	Si 10 Ω.cm	55-65	0.77	-10 dBi η=10%	[73]
Dipole	Si 10 Ω.cm over undoped Si	77	1.02	-8 dBi	[74]
Monopole	Si 10 Ω.cm	40	0.41	-6 dBi	[75]
Spiral Slot	Si 10 Ω.cm	9	0.1	-10 dBi	[69]
Micro-machined Inverted F	Si 11-15 Ω.cm	24	0.5λair (6.6 mm)	-0.7 dBi	[70]
On-chip DRA	Si 13.5 Ω.cm	35	0.28 (slot) 0.37 (DR)	>0.5 dBi η=48%	This work

In the following the performance of the designed on-chip antenna is evaluated in terms of miniaturization factor and maximum transmission range.

1-*Miniaturization Factor*: In [95] a figure of merit (FOM) for miniaturized antenna has been defined which relates the efficiency, fractional bandwidth and size of the antenna

$$\gamma = 10\log_{10}\left(\eta.\frac{\Delta f}{f_C}.\frac{\lambda}{L}\right) \qquad (3\text{-}7)$$

Where Δf is the -10 dB antenna bandwidth, f_C is the center frequency and L is the largest antenna dimension. For example, for a half-wavelength dipole antenna with 5% bandwidth and 98% efficiency, γ=-10.09 dB. For this on-chip antenna with $\eta \approx$ 59%, $(\Delta f/f_C) \approx$

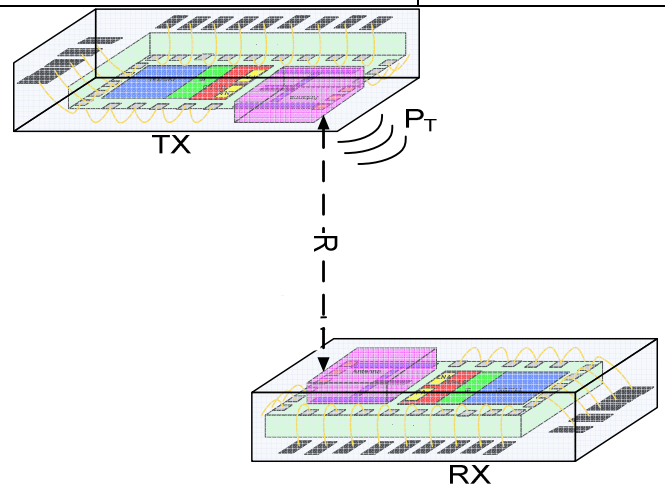
12%, λ=8.5mm, and L=1.15 mm, the calculate FOM is -2.82 dB which is 7.3 dB (almost 5 times) better than a half-wavelength dipole antenna. For L=1.6 mm (DR length) the above FOM is -4.25 dB, 5.8 dB better than the dipole.

2- Maximum Transmission Range:

Assume two of these 35 GHz on-chip antennas are used to establish 1 Gbps data link with the parameters shown in Table 3.4. Figure 3.21 plots the signal to noise ratio delivered by the receiver RF section to the IF section. It is shown that for the Binary Phase Shift Keying (BPSK) modulation with a bit-error-rate of 10^{-5} the maximum transmission range of this configuration is more than 2.5 m for a transmitted power of 0 dBm.

Table 3.4 Link Budget Parameters

Transmitter Output Power	**0 dBm**
Center Frequency	**34.5 GHz**
Receiver Noise Figure	**5 dB**
Bit Rate	**1 Gbps**
IF Bandwidth	**500 MHz**
Modulation	**BPSK**
Bit Error Rate	**10^{-5}**
Antenna Gain	**1 dBi**



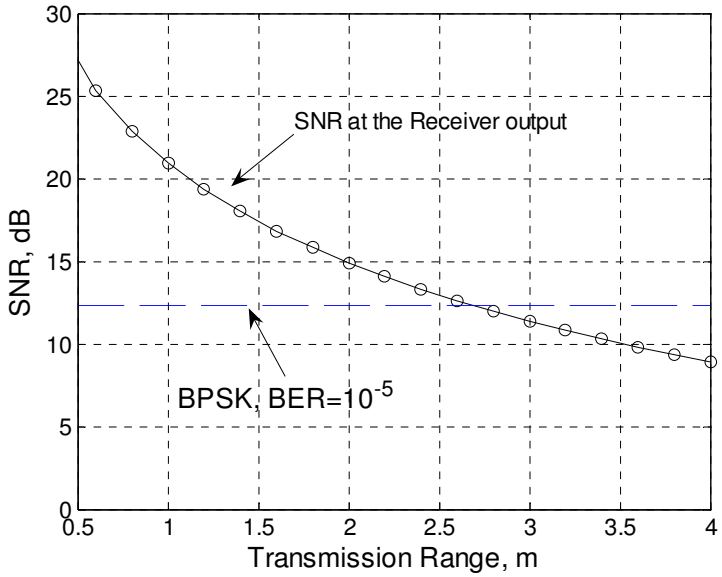
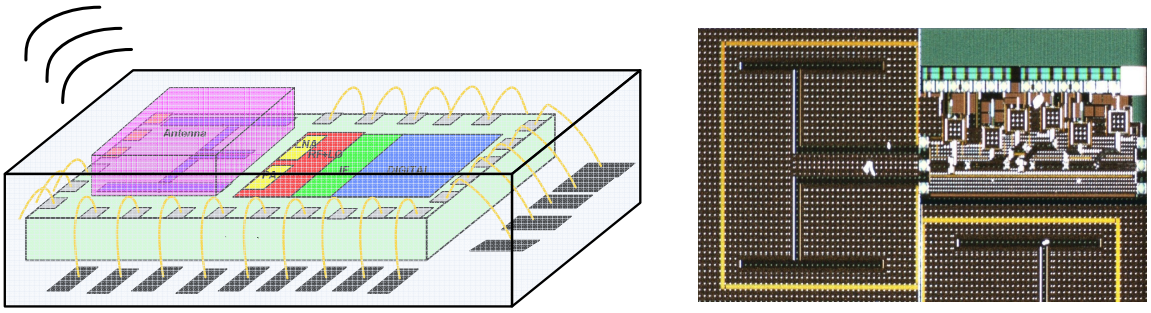


Figure 3.21: Signal to noise ratio at the receiver output versus the maximum transmission range.

3.7 Integrated DRA-Amplifier

3.7.1 Packaging Configuration

The proposed on-chip radio system configuration is illustrated in Figure 3.22a. The on-chip antenna consists of two parts. First part, which is an H-slot aperture, is integrated on the silicon chip with the whole transceiver including the RF, IF and digital circuits. The other part is a Dielectric Resonator (DR), which improves the radiation efficiency and gain, and can be integrated inside the package. The proposed single package structure can integrate the radio and part of the antenna on CMOS or SiGe technology, eliminate the pad, bonding, and package parasitics of the Low Noise Amplifier (LNA) input and Power Amplifier (PA) output, and minimizes the feed-loss between these blocks and antenna and therefore improves the efficiency of the wireless link. Figure 3.22b shows a die photo of proposed on-chip antenna integrated with an amplifier on 0.18 μm technology as front-end of a millimeter-wave transceiver at 30 GHz.



(a) (b)

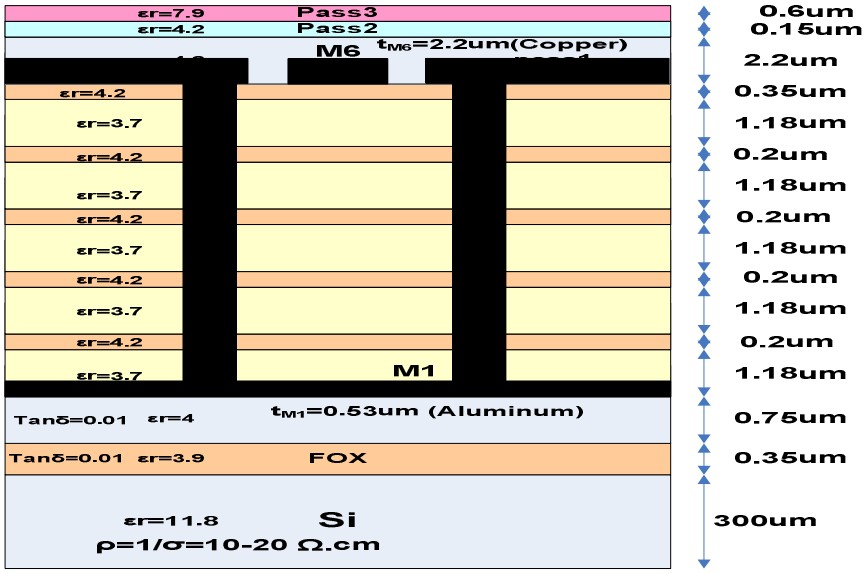
Figure 3.22: (a) Diagram of a single package micro/millimeter-wave radio using the proposed on-chip antenna configuration (b) Fabricated on-chip DRA integrated with amplifier in thick metal CMOS 0.18μm technology.

3.7.2 Implementation

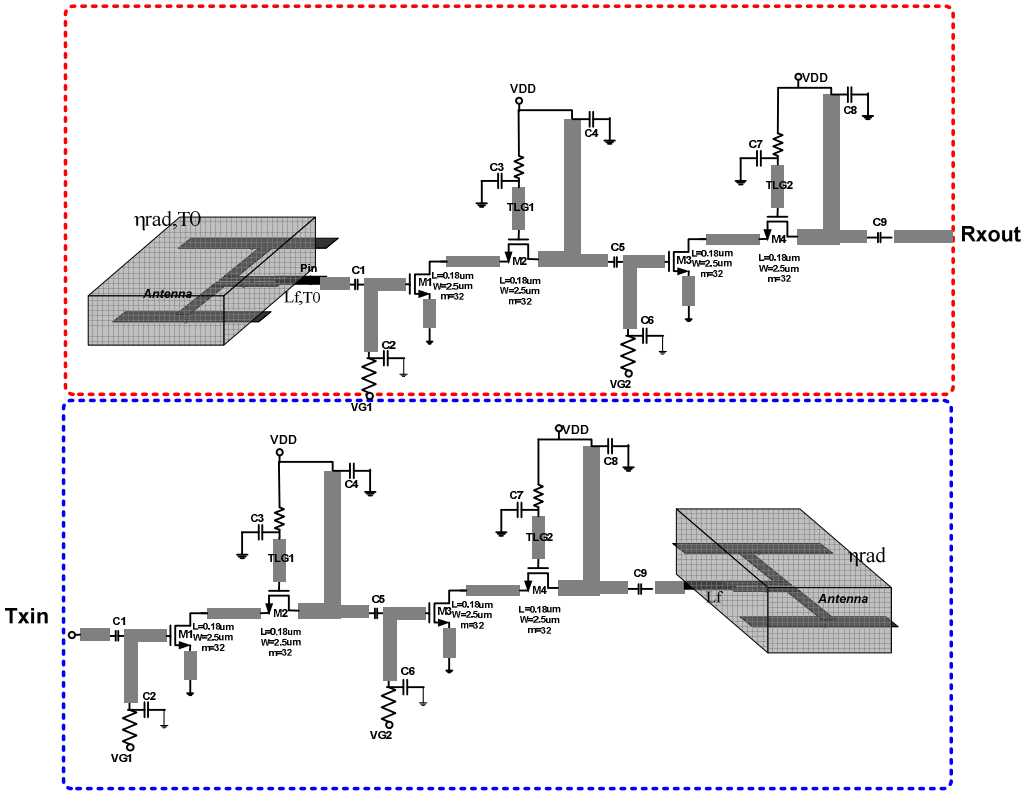
Figure 3.23 demonstrates the BEOL (Back End of Line) cross section of thick metal 0.18 μm CMOS technology used for implementation of integrated DRA-amplifier in transmit/receive configuration. A two stage cascode amplifier was designed in this technology. The antennas and inter stage matching elements were implemented on M6 metal layer. M1 was used as a ground plane of the transmission line and shielding layer under the antenna.

The amplifier shows up to the maximum of 23 dB gain at 29.5 GHz. The details of design and specifications of a standalone version of the same amplifier are discussed in Chapter 4. The gain can be controlled by varying the bias of cascode devices and bias current in each stage.

The antenna has the same structure as the characterized single antenna in previous section and designed for the input matching and maximum efficiency at around 30 GHz.



(a)



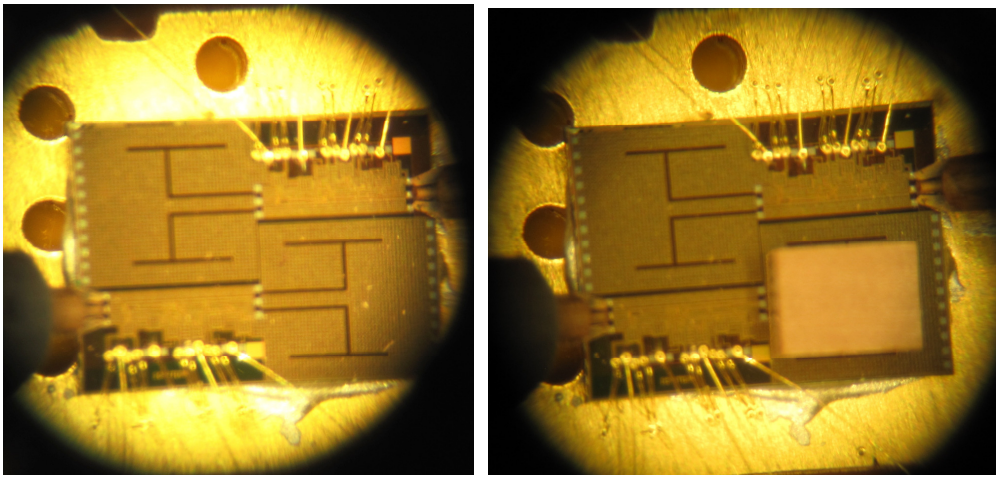
(b)

Figure 3.23: (a) Thick metal 0.18μm CMOS BEOL cross-section (b) Schematic diagram of Tx and Rx front-end

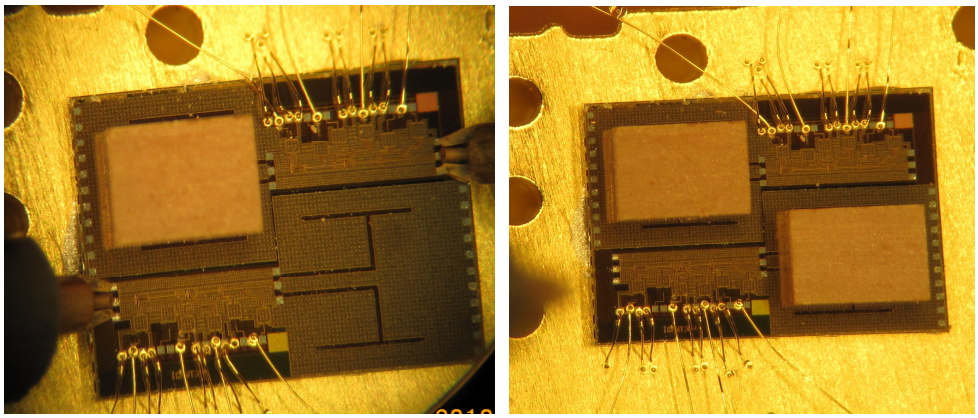
3.7.3 Experimental Results of integrated DRA-Amplifier

3.7.3.1 Near field coupling measurement

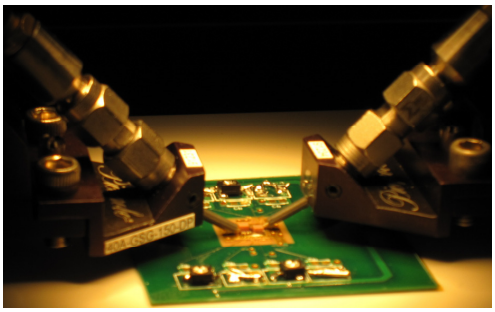
Figure 3.24 shows four different cases in a two-port measurement between the Tx and Rx front-end. The input of the Tx was connected to the port 1 of the VNA and the output of the Rx was connected to the port 2 of the VNA. This experiment is mainly conducted to demonstrate the radiation improvement by the DR. Figure 3.24(a) is the test with no DR on Tx and Rx antennas. Figure 3.24 (b) and (c) are the test cases with DR on Tx and Rx respectively and finally in Figure 3.24 (d) DR was placed on both Tx and Rx sides. The dimension of the DR used in this measurement was 1.55×1.2×0.7 mm with the dielectric constant of 36. Figure 3.25 represents the measured S_{21} of the above mentioned test cases in dB. Improvement in S_{21} by adding DR on each side is presented in Table 3.5. Adding DR on both sides improves the S_{21} by about 28 dB.



(a) (b)



(c) (d)



(e)

Figure 3.24: Four different scenarios of two port measurements (a)No-DR (b) DR on Tx (c) DR on Rx (d) DR on both Tx and Rx (e) Measurement Configuration

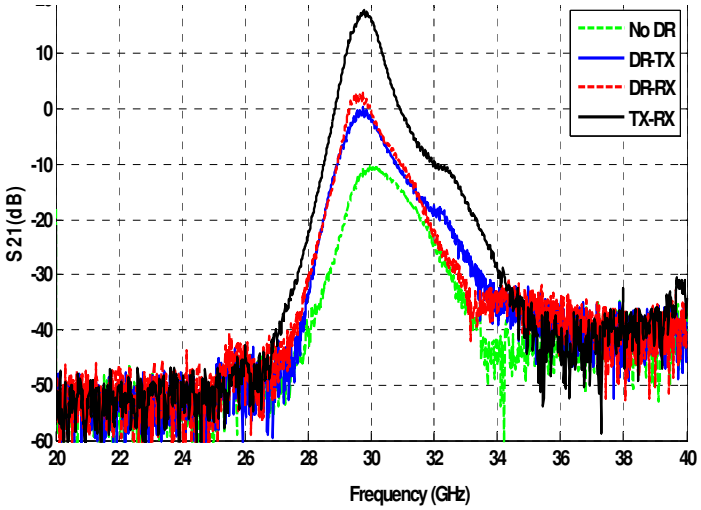


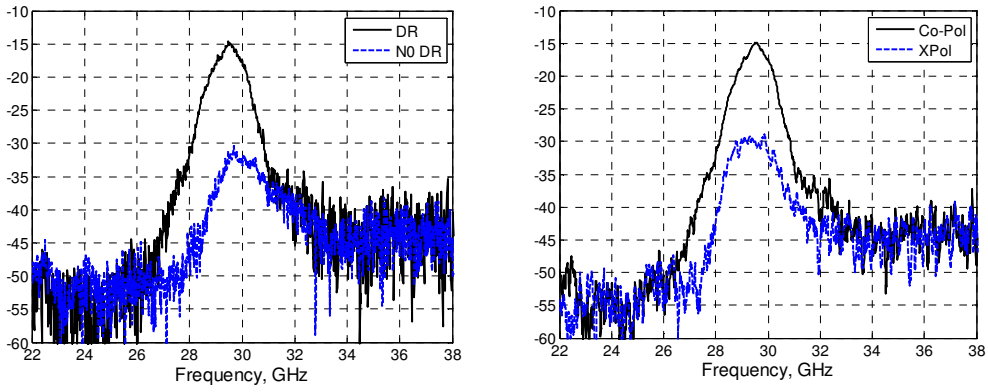
Figure 3.25: Measured dB(S_{21}) of the test cases in Figure 3.24

Table 3.5: Improvement in S_{21} by adding DR to each side of the link

	f_0 (GHz)	Max(S_{21}) dB	Improvement (dB)
No DR	29.9500	-10.4	0
DR on Tx	29.7500	0.19	10.5816
DR on Rx	29.5500	2.95	13.3469
DR on Tx and Rx	29.7500	17.83	28.2196

3.7.3.2 Far field measurement with horn antenna

In this measurement, a set-up similar to the one described in Figure 3.13 was used to measure the antenna radiation with and without DR. Also co-polarization and cross polarization of Tx antenna was measured. The horn antenna was connected to port 2 of network analyzer and port 1 was connected to the input of the Tx amplifier-DRA chip. Figure 3.26 presents the results of this experiment. The S_{21} was improved by 17 dB in this case for the case of having DR on the chip versus no-DR. This is a combination of radiation efficiency and matching improvement. Figure 3.26b shows that the cross polarization is about 15 dB lower that the co-polarization component of the radiated field.



(a) (b)

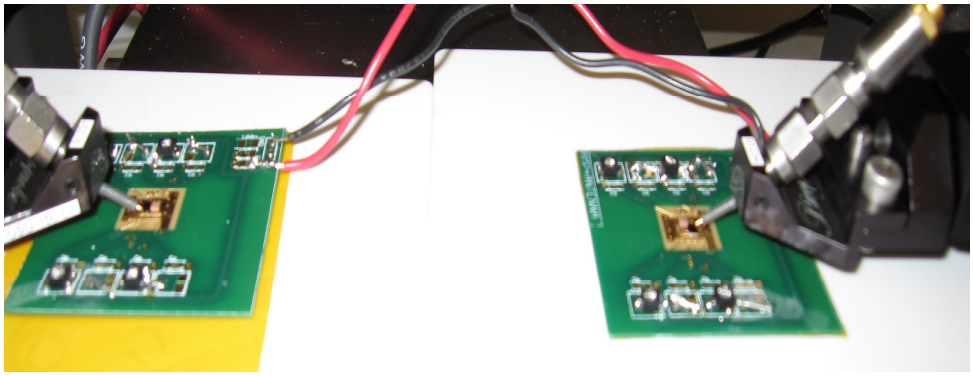
Figure 3.26: (a) Radiation improvement by adding DR (b) Co-polarization and cross polarization measurement result

3.7.3.3 Tx- board/ Rx-board set up

Figure 3.27 demonstrates the set up used for the board to board measurement. The distance between the two antennas is about 12 cm and limited to the CPW probe working space in the station. VNA port 1 was connected to the Tx input and port 2 was connected to the output of Rx. Figure 3.28 shows the S_{21} of this set up in dB. Peak S_{21} of -2 dB was measured when both DRs are placed on Tx and Rx side. The free space loss is 43.5 dB.

$$G_{Txamp}+G_{Txant}\text{-}3\text{ dB}\text{-}43.5\text{ dB} + G_{Rxant}\text{-}3\text{ dB} + G_{Rxamp}=\text{-}2\text{ dB}$$

Based on the stand-alone measurement of the amplifier, for the same bias conditions in this measurement, amplifier gain should be about 22-23 dB. Assuming equal gain for Tx and Rx antennas, and considering the fact that antennas are not placed at the direction of maximum radiation, antenna gain of 0.75-1.75 dBi can be obtained from the above equation. Figure 3.29 depicts the improvement in received power level on Rx side by adding DR on each side of the link. In case of having DR on both sides of the link, 31.7 dB improvements in the link performance was measured versus 28.2 dB in the near filed measurement. The results of this measurement are summarized in Table 3.6.



Tx board Rx board

Figure 3.27: Tx board to Rx board measurement

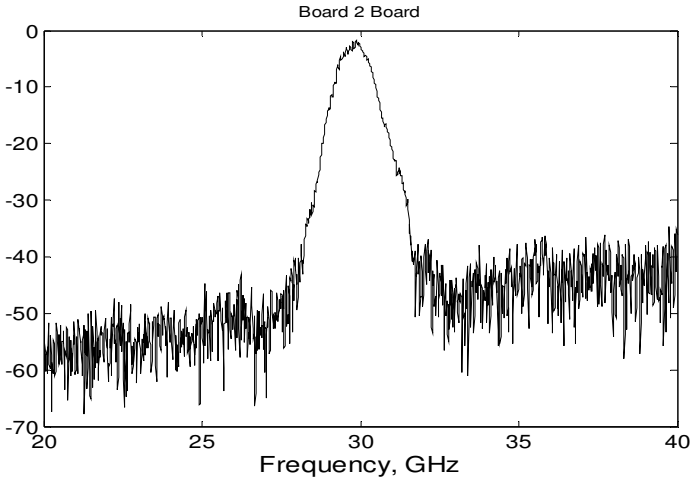


Figure 3.28: S_{21}(dB) of board to board setup at distance of 12 cm.

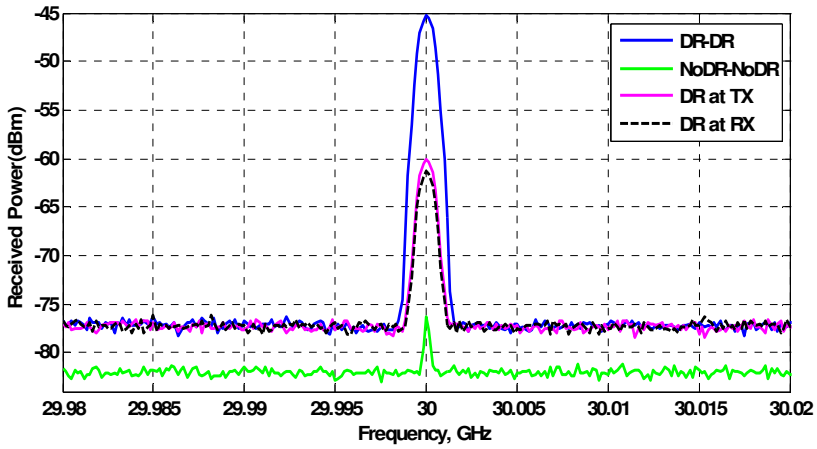


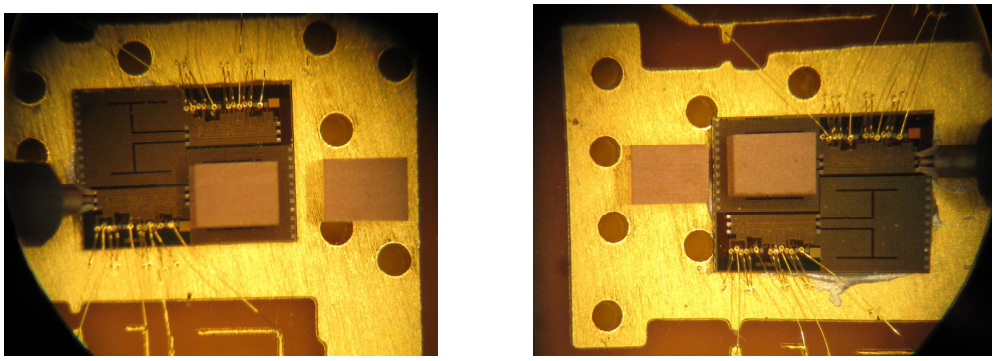
Figure 3.29: Radiation efficiency improvement by adding DR to Tx and Rx board in board to board set up.

Table 3.6: Improvement in the received power level by adding DR t each side of the link.

	Amplitude (dBm)	Improvement(dB)	SNR (dB)
No DR	-76.29	0	5.52
DR on TX	-61.3	15	15.81
DR on RX	-59.34	16.95	17.66
DR on both	-45.28	31	31.68

3.7.3.4 Parasitic Array Configuration

The board to board setup, described in 3.7.3.3 was used for parasitic array configuration experiment. Figure 3.30 shows the parasitic dielectric resonators placed on the ground plane and fed by parasitic coupling. Figure 3.31 shows the improvement in S21(dB) resulting from adding parasitic resonators on the ground plane. The result of this experiment is summarized in Table 3.7. By adding the first parasitic DR, 2.6 dB improvement in S21 was observed. Adding another parasitic element on the receiver side, improved the S_{21} by another 2 dB.



(a) (b)

Figure 3.30: parasitic array configuration (a) Tx (b) Rx

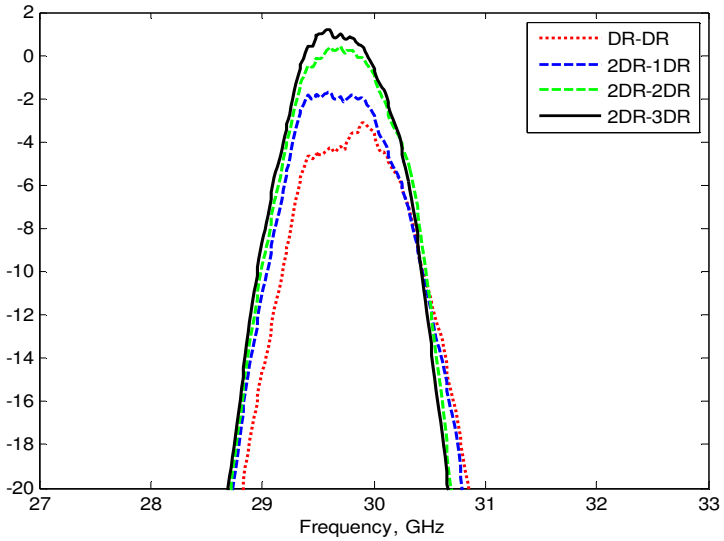


Figure 3.31: S_{21} (dB) by adding parasitic array elements on each side.

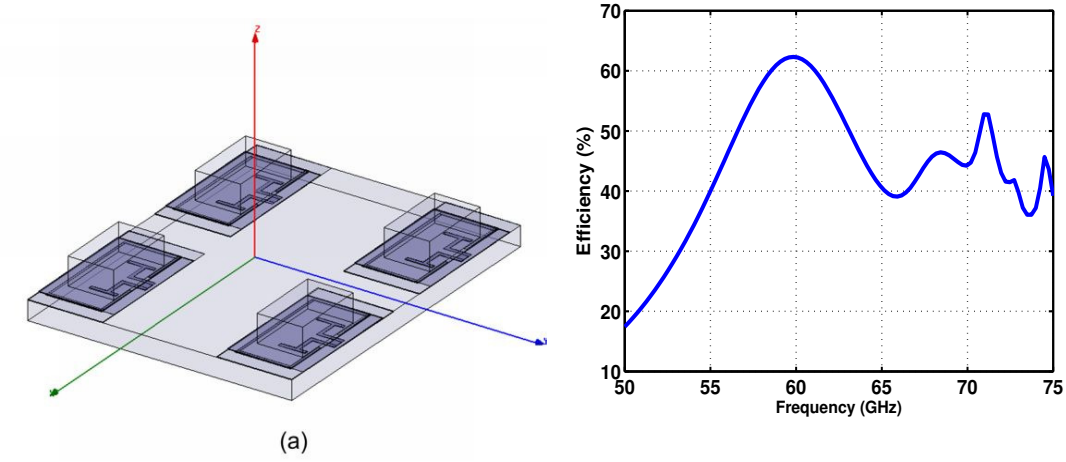
Table 3.7: Improvement in S21 by adding parasitic elements

TX-RX	At resonance	Improvement
1DR-1DR	-4.25	
2DR-1DR	-1.65	2.6 dB
2DR-2DR	0.37	4.62 dB
2DR-3DR	1.2	5.45 dB

3.8 60 GHz 2x2 On-chip Slot Array Antenna

Based on the proposed on-chip DRA structure in previous sections of this chapter, a 2x2 array antenna at 60 GHz was designed on silicon substrate.

Figure 3.32 shows the diagram of the array, radiation efficiency, and radiation pattern of the antenna. Assuming the total area of the transmitter or receiver chip is 4x4 mm, a 4 element antenna transceiver can be implemented. Each antenna takes about 1.5 mm^2 and the rest of the area can be used for the active part of the transceiver. Taking into account, all dielectric and metallic losses, radiation efficiency of about 62% has been achieved. A 2×2 array of this antenna has a maximum gain of 7 dBi and HPBW of 60º. The 2×2 array can be used as a fixed or phased array antenna for a single receiver/transmitter.



(a)

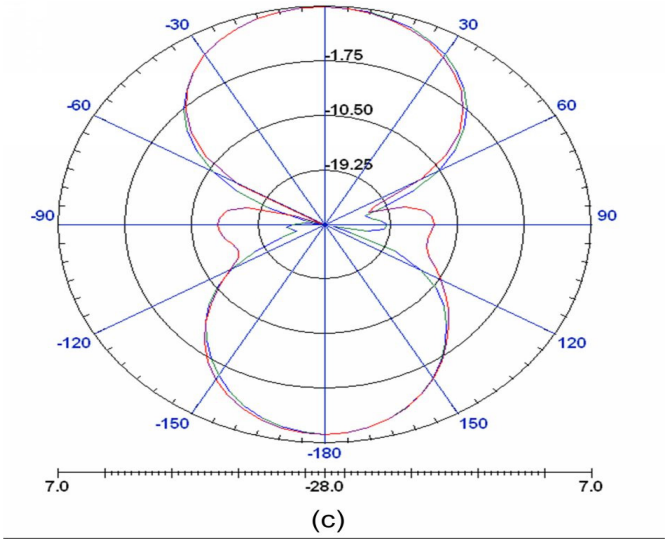


Figure 3.32: 2×2 slot array antenna. (a) Configuration (b) efficiency, and (c) Radiation patterns.

3.9 On-chip Antenna on Integrated Passive Silicon Technology

The major obstacles for 60 GHz on-chip antenna array in CMOS and SiGe technologies are low efficiency and high silicon cost. The performance can be improved by on-chip DRA technique however the cost limits the number of on-chip antennas that can be used on the same substrate where the transceiver is implemented. One viable approach is to implement the antenna in a low cost technology that can be package it with the transceiver chipset.

Different passive technologies such as LTCC and IPD (Integrated Passive Devices on high resistivity substrate) have been developed for RF applications. IPD is a high resistivity silicon process that has been developed for implementation of high Q passive components, filters, baluns and transformers. Such promising application of this technology can be considered as a very promising approach for implementation of miniaturized millimeter-wave antennas and their integration with the transceiver chip.

3.9.1 60 GHz Antennas on High Resistivity Silicon

IPD technology provides a unique integrated platform for implementation of low loss and high-Q and low profile passive elements and RF components such as filters, baluns, and duplexers on silicon. This technology employs high resistivity silicon as the substrate versus the low resistivity silicon substrates in CMOS and SiGe technologies. Figure 3.33 shows the cross section of the metal layers and the silicon of this technology provided by ON Semiconductor Company. The technology consists of two thick metal layers (5 μm copper layer) and a thin metal layer (2 μm copper layer) on a high resistivity silicon substrate with σ =0.1 S/m and thickness of 280 to 700 μm.

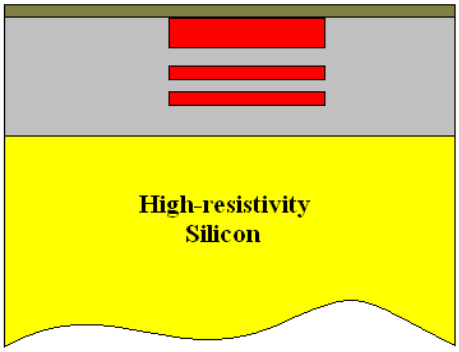


Figure 3.33: Cross section of the IPD technology with three metal layers.

Depending on the application, size constraints, and gain and radiation pattern requirements, different types of antennas need to be investigated, designed and developed. In this technology, two classes of antennas were investigated.

3.9.1.1 F Shaped Antenna

The F-antenna is in fact the predecessor of the famous class of planar inverted F-antennas PIFAs that are widely utilized in compact wireless devices. The F-shaped antenna is a bent monopole (the center feed line), with a connection to the ground pad to establish a transmission line-like mode. This enables a compact size of the center-signal line (at nearly quarter of a wavelength at the operational frequency). Figure 3.34 shows the schematic of implemented on the top metal layer of the IPD technology. The antenna die size is 1.6×0.8

mm. Figure 3.35 demonstrates the simulation results for the F antenna. A single antenna element shows a gain of 2.4 dBi and 10 dB bandwidth of 4 GHz.

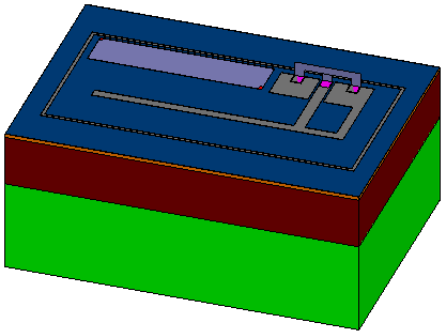
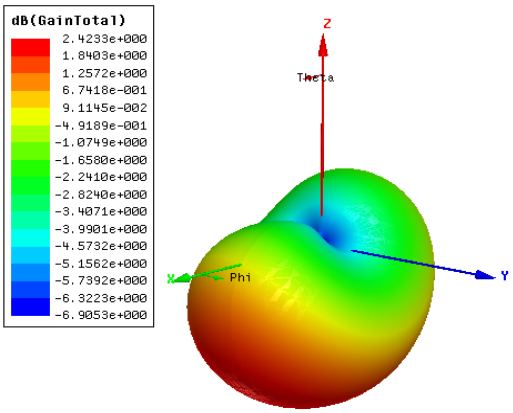


Figure 3.34: F shaped antenna implemented in IPD substrate



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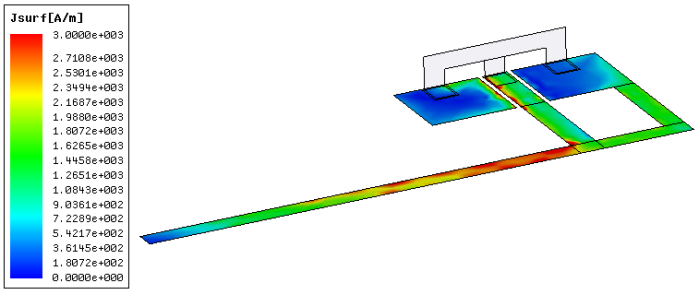

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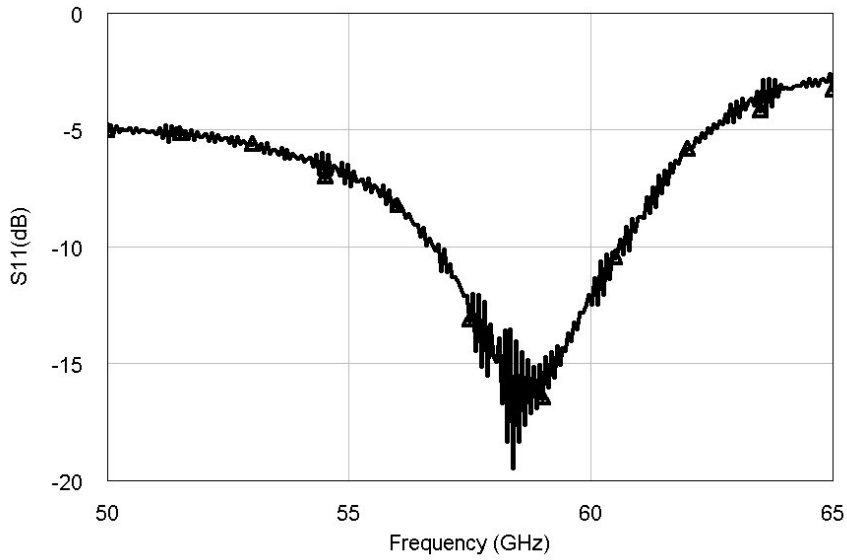


(c)

Figure 3.35: Simulation results for F-shaped antenna implemented in IPD technology (a) 3D radiation pattern (b) Surface current distribution (c) Measured S_{11}

3.9.1.2 Slot Antenna

Another type of antenna that was investigated in this technology is a slot radiator [96][97] with a microstrip line excitation. Figure 3.36 shows the top view of the designed antenna. The microstrip line has been implemented on M_1 and M_3 layers where signal is on M_3 and the ground is on the M_1. The thickness of the SiO_2 (dielectric of the microstrip line), M_1 and M_3 are 14 μm, 2 μm and 5 μm respectively. Therefore, the width of microstrip line was chosen to be 8μm to set the characteristic impedance of the line to 50 Ω. The power delivered in the microstrip line couples into the slot line which is implemented in the microstrip line ground plane. The slot will deliver most of the coupled power into the high resistive Silicon substrate. The thickness of the substrate is 280 μm, the relative permittivity is ε_r =11.9 and the conductivity is σ =0.1 S/m. The entire structure has been optimized in ANSOFT HFSS to have a good matching at the microstrip line input as well as maximum radiation efficiency at 60 GHz.

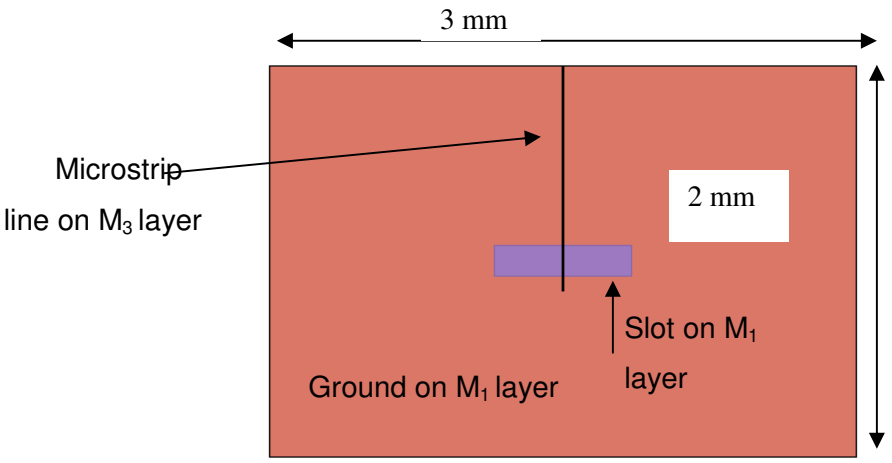


Figure 3.36: The top view of the slot radiator on the M1 (the bottom metal) layer and the microstrip line on M3 (the top metal) layer.

The length of the slot is $\lambda_g/2$; where $\lambda_g = \frac{c}{\sqrt{\varepsilon_{eff}}}$. The slot is over the silicon with ε_r=12; therefore $\varepsilon_{eff} \approx \varepsilon_r$ and $\lambda_g \approx 1.45$ mm. The optimized dimension of the slot is 700 μm × 150 μm.

3.9.1.3 Simulation Results

Figure 3.37 shows the simulated gain pattern of the antenna at φ=0º and φ=90º planes, respectively. As expected, since the Silicon substrate is at the bottom of the antenna, most of the power would be radiated through the Silicon and the maximum gain is along θ=180º. The simulations show that the maximum gain of the antenna is 3.5 dBi and the beamwidth of the antenna is 90º and 100º at φ=0º and φ=90º planes, respectively.

The S_{11} and the efficiency of the antenna are shown in Figure 3.38. The HFSS simulations show that the structure has a resonance at 60 GHz. The antenna shows return loss better than 10 dB over the frequency band 58-62.5 GHz. Theoretically, the gain of a slot radiating in free space is 1.5 dBi. In this structure, it is shown that using the benefits of the

high-resistivity silicon one can improve the gain of the single element by 2 dB. The efficiency of the antenna is better than 64% over the aforementioned range of frequency while the radiation efficiency is 72% at 60 GHz.

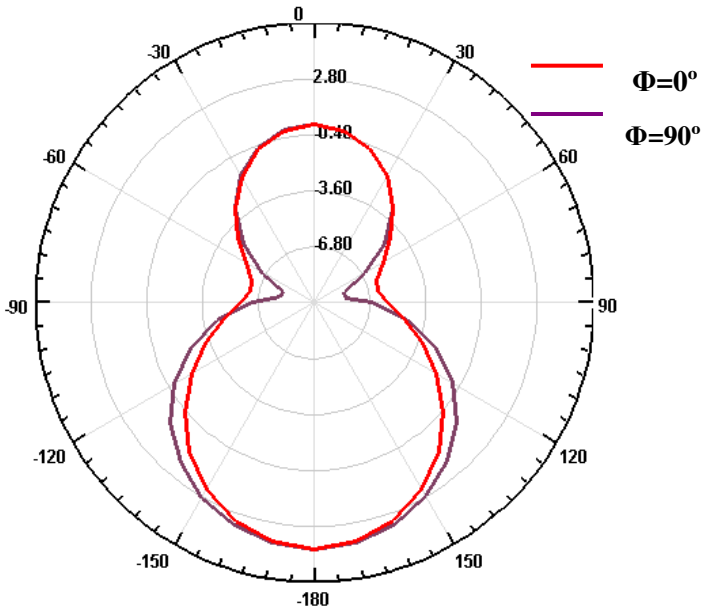


Figure 3.37: Simulated gain of the antenna at φ=0° and φ=90° planes.

As a conclusion, a microstrip-fed slot antenna in IPD technology has been designed and optimized. The simulation results show that the antenna which operates in the frequency range 58-63 GHz, has 3.5 dBi gain and the radiation efficiency at 60 GHz is 72%.

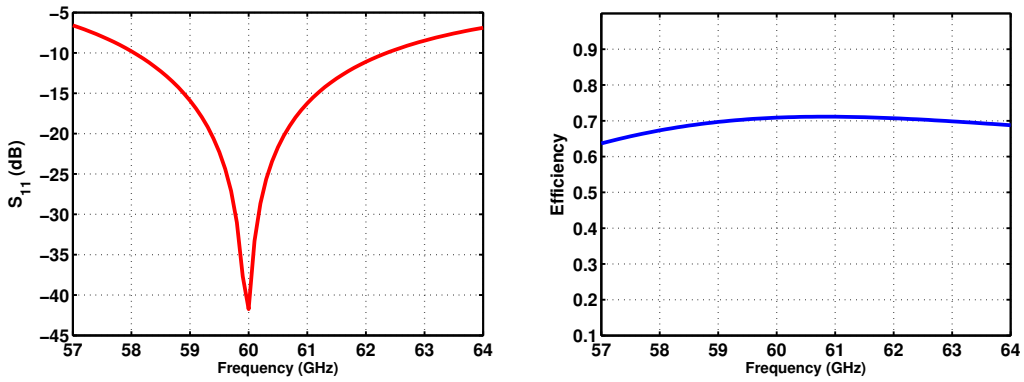
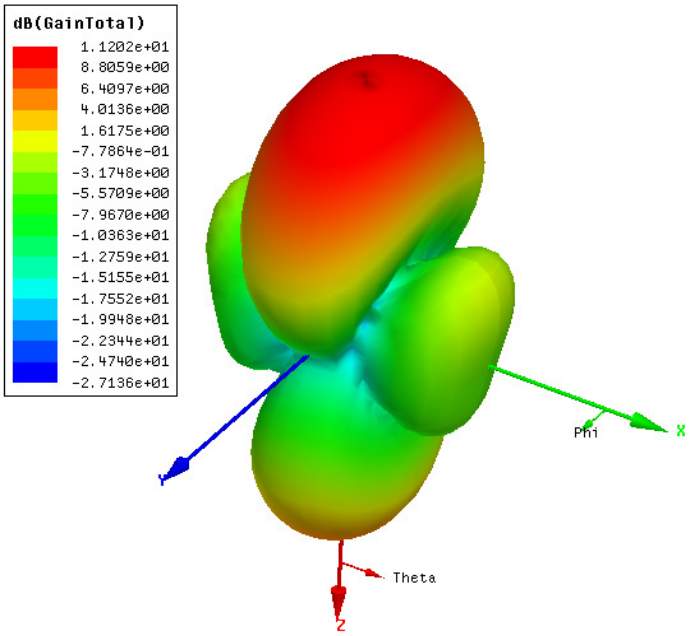
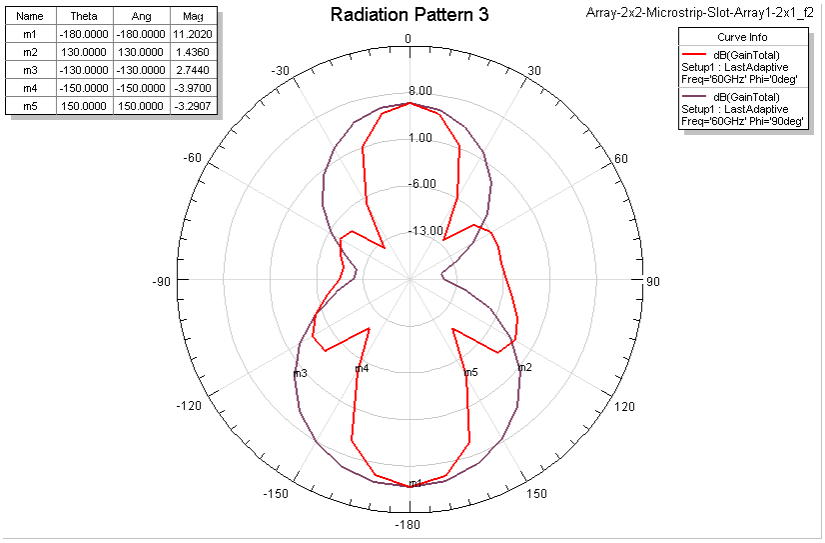


Figure 3.38: S_{11} and efficiency of the antenna over frequency.

Figure 3.39 shows the simulation results for an 8 element array of slot antenna which consumes a silicon area of 8 x 4 mm in IPD technology. The antenna array shows a total gain of 11.2 dBi.



(a)



(b)

Figure 3.39: Simulated radiation pattern and gain for a 60 GHz 8 element antenna array in IPD (a) 3D radiation pattern (b) 2D radiation pattern

3.10 Conclusion

This chapter introduced a high-efficiency on-chip antenna structure in low resistivity silicon technology. The antenna consisted of an H-slot antenna implemented on the top metal layer of IC process and a rectangular dielectric resonator. First a single antenna at 35 GHz was presented. The maximum size of antenna chip, DR and the radiating slot antenna are respectively $0.23\lambda_0$, $0.18\lambda_0$ and $0.13\lambda_0$. The maximum radiation efficiency was 59% which is a remarkable value for an integrated antenna in low-resistivity silicon. This electrically small antenna has a relatively large bandwidth of 12% operating from 33 to 37 GHz. It was shown that adding the high-permittivity rectangular DR, which could be a part of the antenna in package, improves the efficiency and matching of the antenna structure by 17 dB. Moreover, it was shown that removing the passivation layer on top of the slot improves the coupling between DR and H-slot antenna which increases the radiation efficiency by 10%. This result was confirmed by measurements and simulations.

As a further step towards a fully integrated in-package millimeter-wave transceiver, a 30 GHz integrated DRA-amplifier in both Tx and Rx configuration was developed in 0.18 μm CMOS technology. When DR was used on both Tx and Rx sides of the link, about 30 dB improvement in the wireless link was measured compared to the no-DR on both sides. Moreover, a parasitic array configuration on both transmit and receive improved the link performance by another 5.2 dB.

Due to the limitation of antenna measurement setup frequency to 40 GHz, on-chip DRA antennas were designed and implemented at frequencies below 40 GHz. The antennas designs are scalable to 60 GHz. Simulation results at 60 GHz shows radiation improvement up to 60% , however as the frequency of operation increases, the sensitivity of the design to fabrication tolerances increases. This need to be considered in the design of the antennas at higher frequencies by considering enough margins in the bandwidth and gain of the antenna to meet the specified requirements.

Based on the experiments on 35GHz and 30GHz prototypes and different DR samples, DR surface roughness is an important factor in coupling to the on-chip slot radiator.

This investigation shows that on-chip antennas with high-efficiency, acceptable gain and sufficient bandwidth for short-range broadband wireless applications at millimeter-wave

frequency range are realizable.

Furthermore, for the implementation of a low cost and efficient antenna array, on-chip antennas in an integrated passive device technology have been investigated. Simulation results show that efficient, low profile, compact, and low cost antennas are quite feasible in the passive silicon technology.

Chapter 4 Millimeter-wave Phased Array Front-end Design

4.1 Introduction

As discussed in chapter 2, RF phase shifting architecture with continuous phase shifters is the most compact and power efficient array architecture. The receiver front-end of this architecture consists of an LNA, phase shifter, and power combiner. The combined signal will be delivered to the down-conversion mixer. On the transmitter side, after the up-converter mixer the signal is splitted between different paths using a power divider. In each path, RF signal will pass through one phase shifter and power amplifier.

This chapter describes and discusses the design and development of key blocks of a millimeter-wave phased array receiver including LNA, passive and active phase shifter circuits as well as down converter mixer. The key requirements of the LNA are enough gain, low noise figure, variable gain and relatively wide bandwidth for 60 GHz band. The phase shifter needs to be linear, low loss, and preferably with 360º phase shift range. Section 4.2 is a brief review of narrow band and broadband CMOS amplifier topologies. Section 4.3 describes the design of a 30 GHz high gain cascode amplifier in 0.18 μm CMOS technology used for integration with 30 GHz on-chip DRA. Section 4.4 presents a 3 stages cascode amplifier in 0.13 μm CMOS technology. Lumped and distributed 90º couplers used for balanced amplifier configuration and phase shifter have been presented.

Section 4.5 is design and development of passive and active CMOS phase shifters. Section 4.6 presents the results of a developed double balanced down conversion mixer in 0.13 μm CMOS technology.

In section 4.7 details of phased architecture and frequency plan is described. Active and passive RF-phase shifting front-ends have been presented in section 4.8. Section 4.9 demonstrates the measurement results of a two element RTPS based array front-end. Finally, architecture and measurement results of a two-element active phase shifting front-end in 0.13 μm CMOS technology is presented in section 4.8.3.

4.2 Amplifier Topologies for Millimeter-wave

4.2.1 Gain cells (CS, CG, Cascode)

Different CMOS LNA topologies such as common-gate [43], common-source, and Cascode [97]-[98],[6] are utilized and implemented for millimeter-wave receivers including 60 GHz band. Figure 4.1 depicts transistor common source and a single transistor common gate topology.

Common-gate (CG) amplifier provides a wideband input matching with good reverse isolation, however, the noise figure of the CG LNA is considerably larger than that of the CMOS common-source or cascode LNAs.

Compared to the common-source (CS) or common-source (CG) topologies, the cascode topology allows for a better stability. Higher gain can be achieved however, the noise figure would be higher due to the extra noise introduced by the cascode transistor. In fact the cascode topology can be considered as two cascaded CS and CG stages.

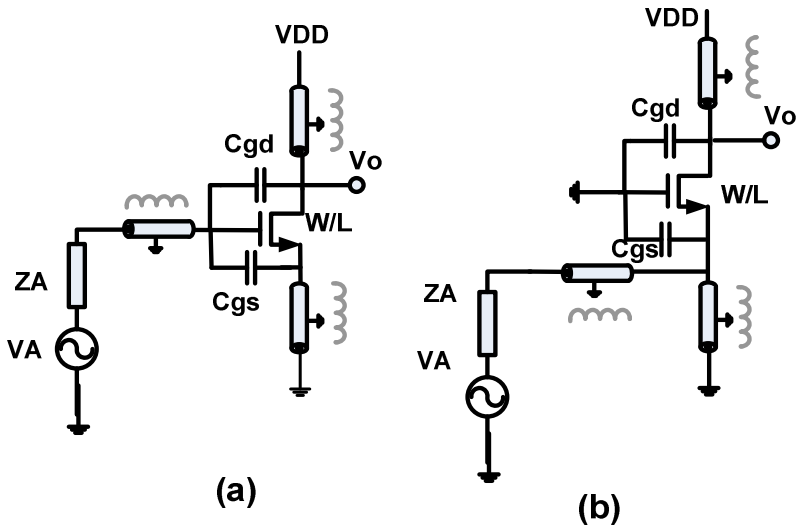


Figure 4.1: Different single transistor CMOS amplifier topologies a) Common Source b) Common Gate

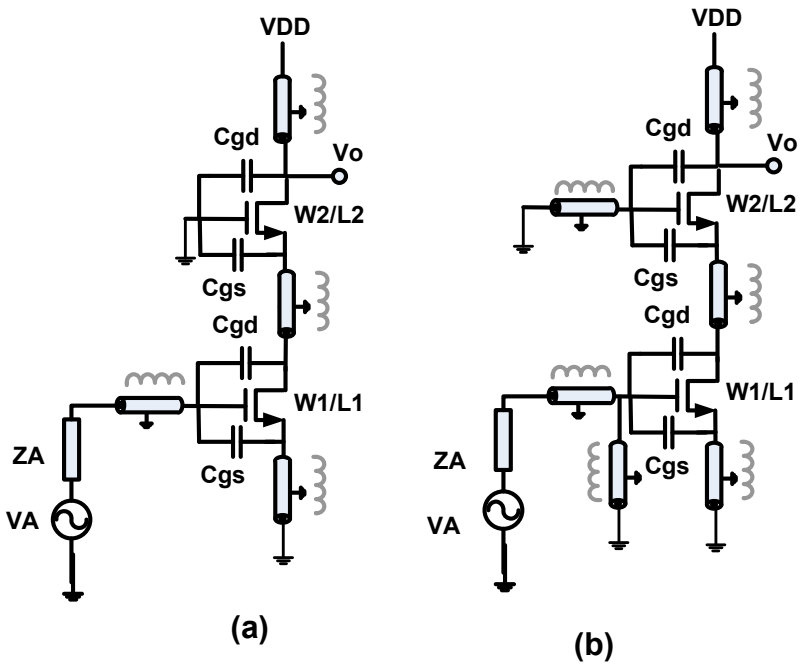


Figure 4.2: Different cascode CMOS amplifier topologies a) most common topology b) optimal topology

Figure 4.2 shows the two possible cascode topologies. The first circuit illustrates the most common cascode, with inductive degeneration at source. The inductor at the source of the CS device facilitates the input matching however it lowers the gain. Inter-stage inductor has been used to improve the matching between the CS and cascode transistors. Figure 4.2b shows a proposed topology that can presents higher gain by adding an inductor at the gate of the cascode transistor. The added inductor pushes the achievable gain of the cascode amplifier to its limit which is MSG (Maximum Stable Gain). Biasing of drain and gate of the transistors has been provided through the lumped elements that are also part of the matching circuit.

4.2.2 Broadband topologies

The topologies presented in the previous section are not able to provide broadband amplification for some of the future broadband applications in millimeter-wave band. Distributed amplifier is one of the techniques to achieve broadband amplification[132][133]-[134]. Compared to lumped circuits, higher power consumption and larger chip area are the

main concerns in regards to distributed amplifier topologies. Figure 4.3 shows a general diagram of a distributed amplifier that has been designed to have a broadband band-pass frequency response. The gain cells could have a CS or cascode configuration.

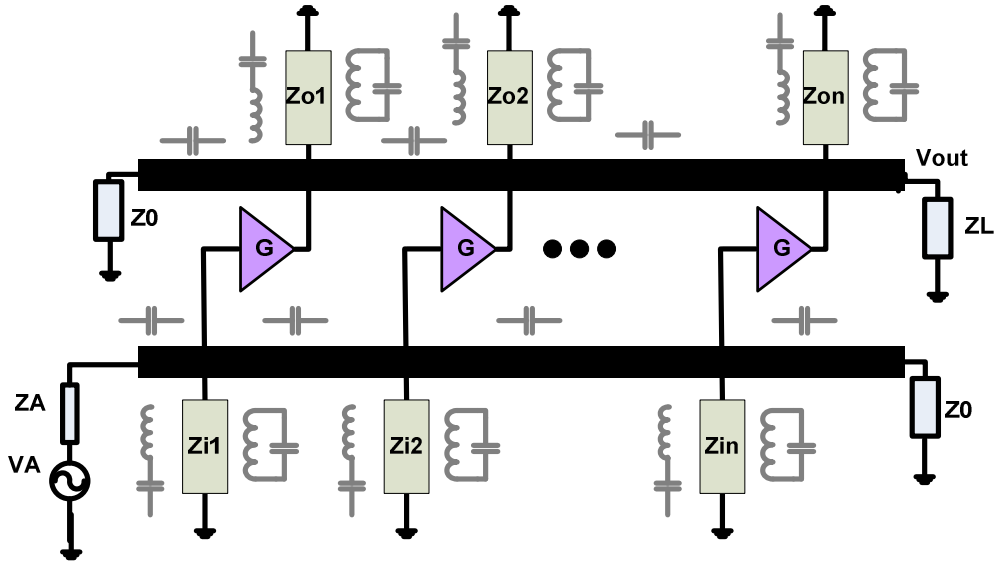


Figure 4.3: A general diagram of a band-pass distributed amplifier

Another technique for implementing broadband amplifier with flat gain and good input and output matching is balanced amplifier[136]. Figure 4.4 demonstrates the balanced amplifier configuration. It consists of two input and output couplers and two identical amplifiers in each branch. The input 90º coupler works as a divider and the output coupler as a combiner. Port 4 of the input and output couplers are terminated with 50 Ω loads.

As illustrated in Figure 4.4, the input signal is divided into two components by the input coupler with an equal power splitting, but a 90º phase difference. Both signals are amplified separately in each path and then combined by the output coupler with a reversed 90º phase shift to obtain the overall output. In each path, part of the signal can be reflected back due to impedance mismatch. After passing through the 90 coupler again, the reflected signals from both paths appearing at input port have a 180º phase difference, which cancel each other resulting in an unconditionally matched condition at the input. On the other hand, the reflected signals with a 0º phase difference are superimposed at the isolated port and terminated by a 50 Ω resistor. Compared to a single amplifier, the balanced amplifier configuration needs two couplers and two amplifiers, resulting in larger power consumption

and chip area. However, the output 1 dB gain compression point is 3 dB higher than that obtained from a single amplifier.

One limiting factor in the bandwidth of the amplifier is bandwidth of the 90º couplers. Hence a broadband 90º coupler should be used to increase the bandwidth. This will be discussed in 4.4.1.

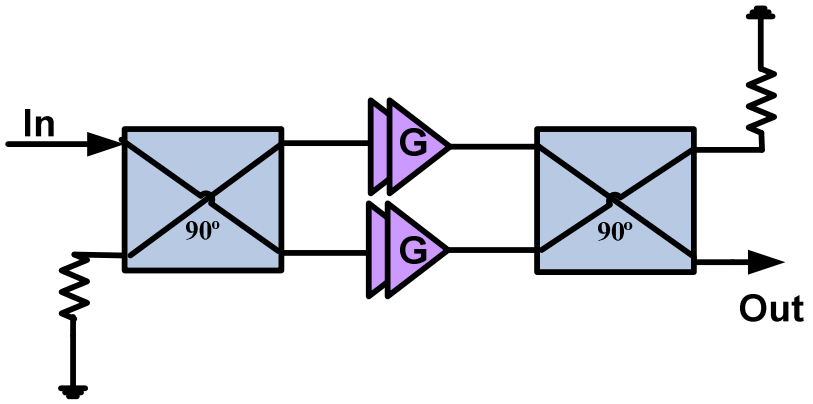
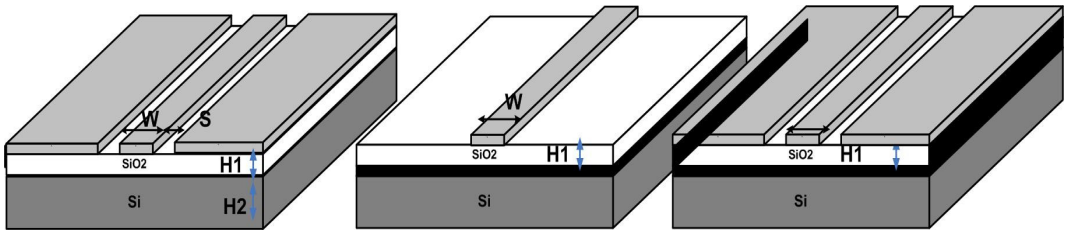


Figure 4.4: Balanced amplifier topology

4.2.3 Matching Circuit Elements

Lumped and distributed elements are two choices for matching circuit elements. The chip dimensions and the length of interconnects, as compared to the wavelength, determines whether lumped elements models are still valid for on-chip elements. As we move to higher frequencies at around 60 GHz and beyond, the transmission line effects in the interconnections should be modeled. In this range of frequencies where inductors become small, transmission lines have higher quality factor. Figure 4.5 shows different transmission lines structures in silicon technology. The structures are coplanar waveguide (CPW), microstrip, and coplanar waveguide with a ground plane (CPWG). A CPW structure uses the top level metal layer of the technology. Because the substrate is low resistivity, this structure shows higher loss compared to MS (Micro-Strip) and CPWG counterparts which use the lowest metal layer above low resistivity silicon as their ground plane. Another advantage of a MS and CPWG is the reduced coupling of RF signal to other circuit blocks on the same substrate. Either CPWG or micro-strip are appropriate options for millimetre wave circuit design in silicon.



(a) (b) (c)

Figure 4.5: Different transmission line structures on silicon a) CPW b) Micro-strip c) CPWG

Figure 4.6 shows the different transmission line structures implemented in 0.18 µm CMOS technology. Length of each transmission line is 1 mm and the lines are designed to present the characteristic impedance of 50 Ω. Measurement results of the lines are shown in Figure 4.7. As can be seen, the CPW line shows an insertion loss of about 2.4 dB/mm at 30 GHz while this number is 1.25 dB/mm for CPWG and MS line structures. S_{11} of the lines is below -16 dB over the frequency range of 20 to 40 GHz.

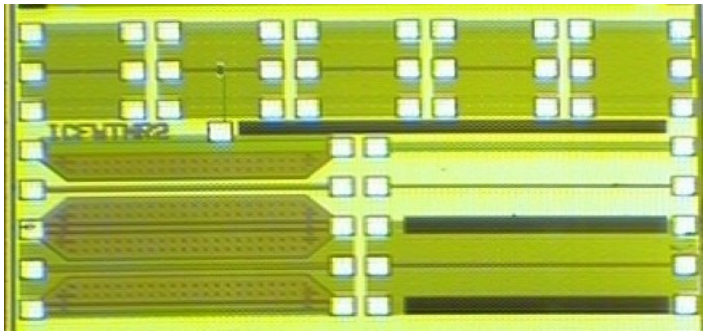
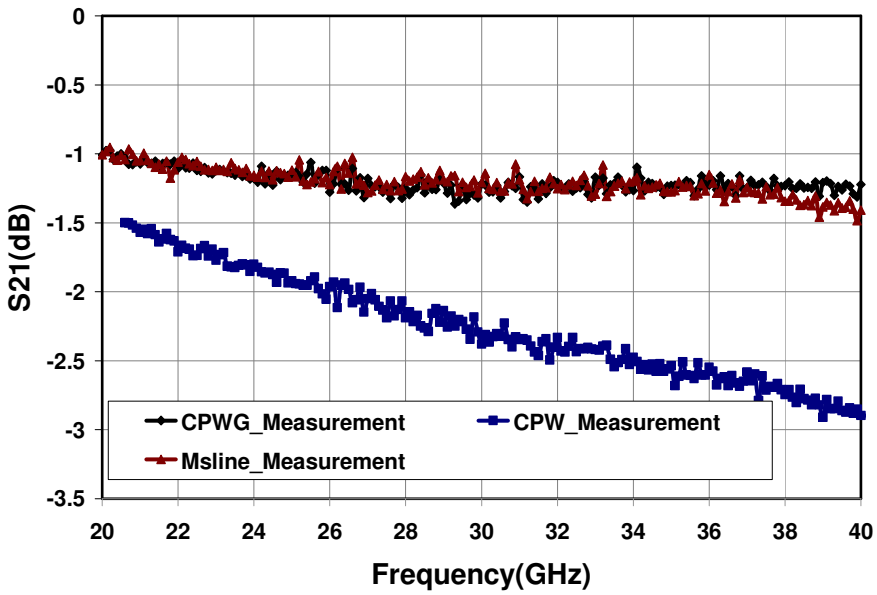


Figure 4.6: implemented transmission line test structures in thick metal CMOS 0.18 µm technology



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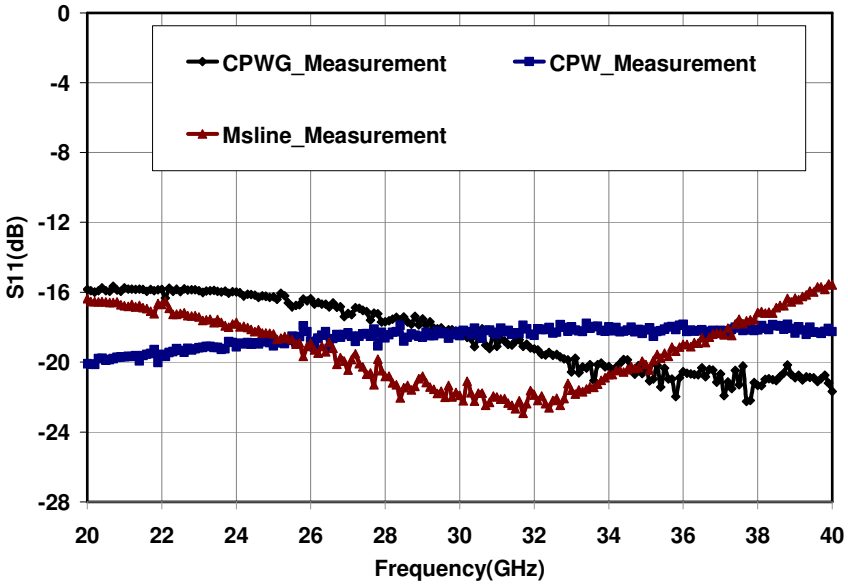
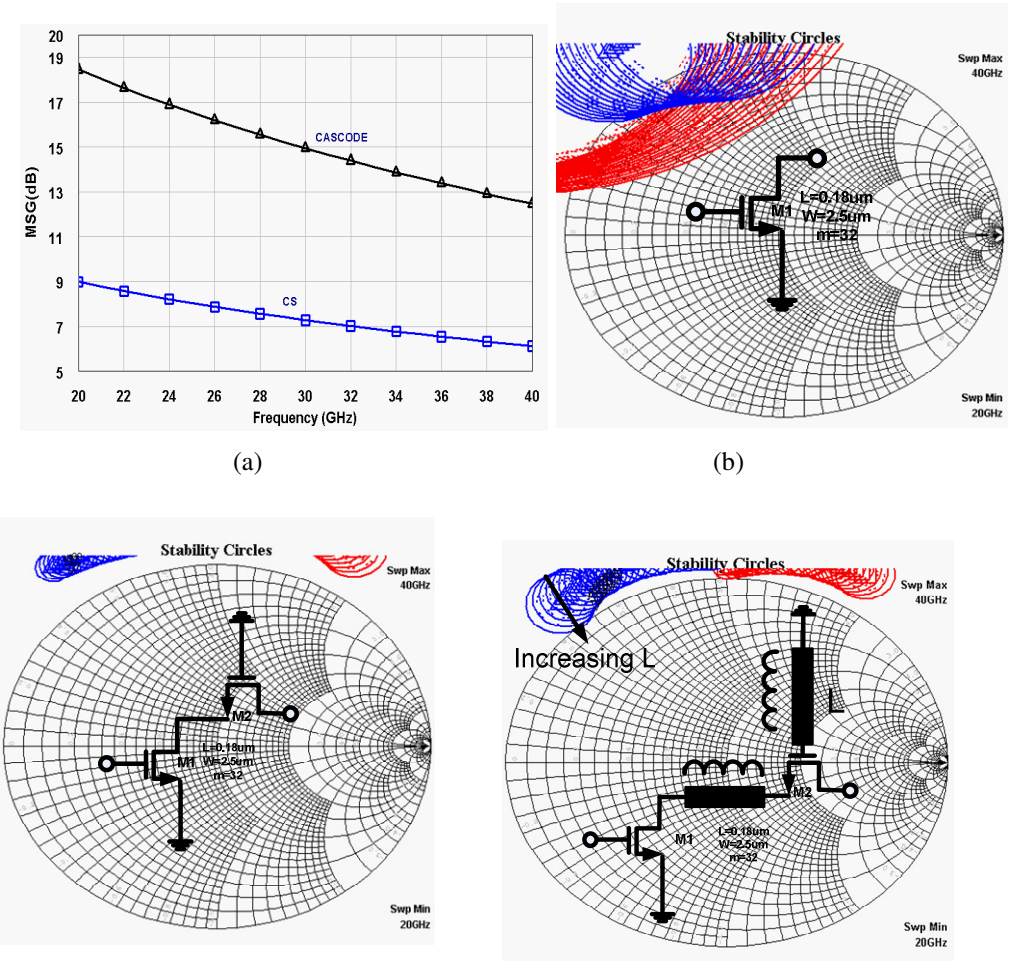


(b)

Figure 4.7: Measured results of implemented transmission lines with length of 1 mm in 0.18 µm CMOS technology. (a) S_{21}(dB) (b) S_{11}(dB)

4.3 30 GHz Cascode Amplifier

As part of the integrated DRA-amplifier chip presented in chapter 3, a 30 GHz cascode amplifier was designed in thick metal 0.18 µm CMOS technology. The MOS transistors for this amplifier are sized and biased for maximum f_{max}. The device is sized to W/L=80/0.18 and each cascode stage consumes about 15 mA form 1.8 V supply. Figure 4.8 shows a comparison between CS and cascode in terms of MSG figure of merit as well as stability.

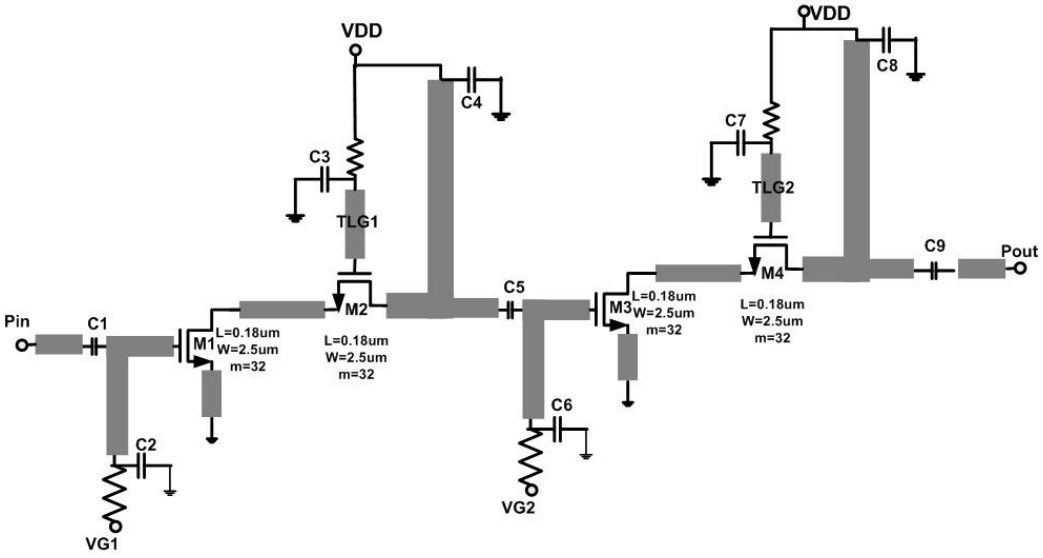


(a) (b)

(c) (d)

Figure 4.8: Comparison of CS and cascode in terms of MSG and stability.(a) MSG of cascode versus CS (b) Source and load stability circles for the CS gain cell (c) Source and load stability circles for gain cell (d) The effect of adding an inductive line in the gate of the cascode device on stability.

Adding an inductive transmission line to the gate of cascode transistor pushes the maximum available gain towards maximum stable gain limit and lowers the margin to stability as shown in Figure 4.8d compared to Figure 4.8c .In this design for a two-stage cascode amplifier, a maximum gain of about 24 dB with an input matching better than 15 dB at 30 GHz was achieved. Figure 4.9 shows the schematic diagram and die photo of the fabricated amplifier. The die area is 0.8 mm^2 excluding the pads .



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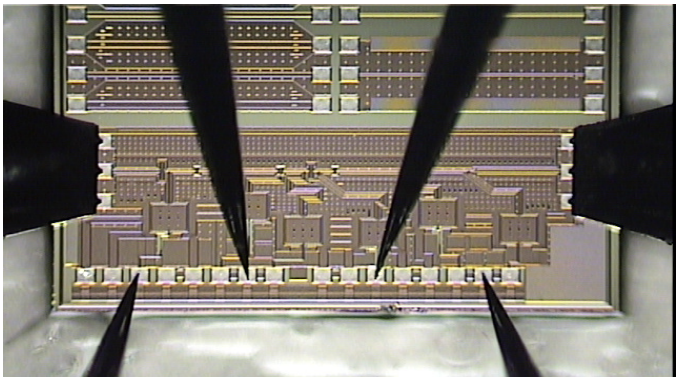


(b)

Figure 4.9: The designed two-stage cascode amplifier at 30 GHz in CMOS 0.18 μm technology (a) Schematic (b) Die micrograph under test

Figure 4.10 shows the measured scattering parameters of the amplifier over the frequency range of 25 to 35 GHz. In principle, the gain of the cascode amplifier can be controlled by varying the applied bias to the gate of cascode device. In this design the bias for the gate of cascode was tied to the power supply. Therefore, the gain control observed in Figure 4.10 is resulting from varying the main supply of the circuit as well as bias of the cascode device. A brief comparison between this design and similar amplifiers in 0.18 μm technology is brought in Table 4.1. The achieved gain per stage in this design is than the reported designs in this technology.

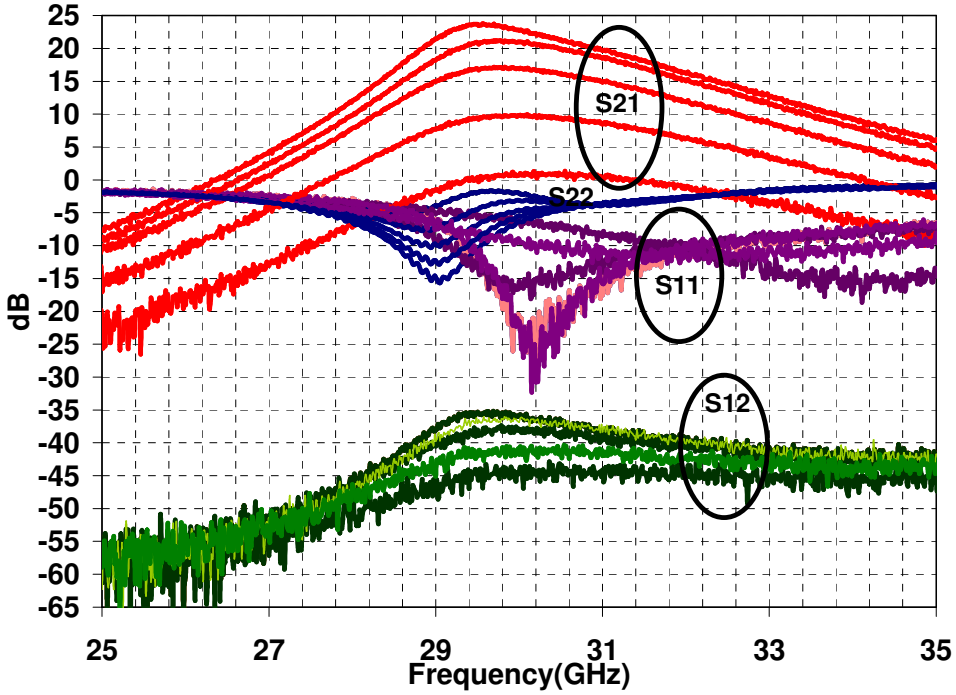


Figure 4.10: Measured s-parameters of the amplifier versus cascode transistor bias and supply.

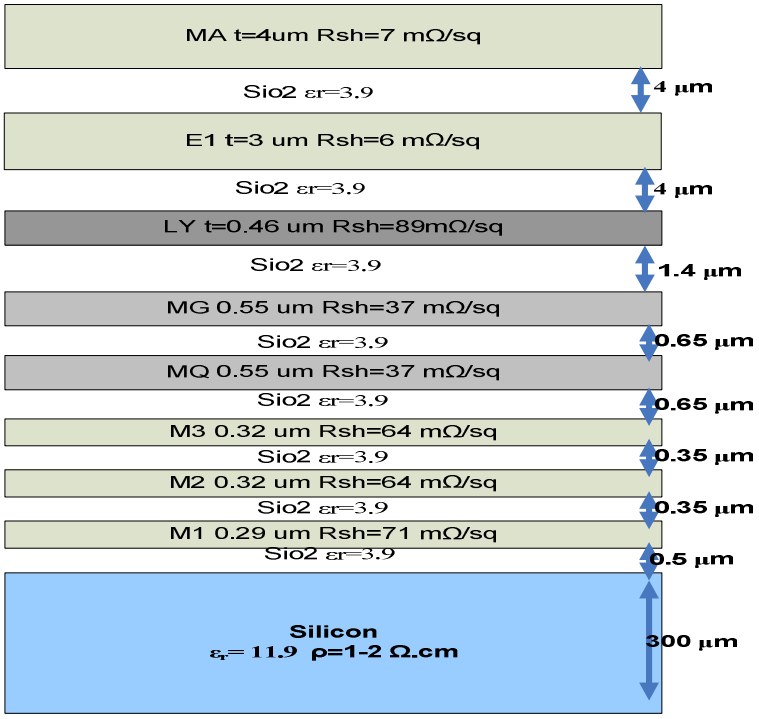
Table 4.1: Comparison of this design with similar amplifiers in CMOS technology

Process	CMOS 0.18 µm	CMOS 0.18 µm	CMOS 0.18 µm	CMOS 0.18 µm	Thick Metal CMOS 0.18 µm
Frequency (GHz)	24	21.8	25.7	22.5	29.5
Gain (dB)	13	15	8.9	5.5	24
Gain per Stage (dB)	6.5	5	2.9	5.5	12
Chip Size (mm^2)	0.34	--	0.735	0.56	0.8 (Excluding Pads)
Input/ Output Return Loss	15/20	-/-	14/12	15/10	10/3
P_{DC}(mW)	14	24	54	54	56
Power Supply	1	1.5	1.8	1.8	1.8
Circuit Topology	2-stage CS	3-stage CG,CS	3-stage CS	Cascode single-stage	Cascode two-stages
Ref	**[100]**	**[100]**	**[102]**	**[102]**	**This design**

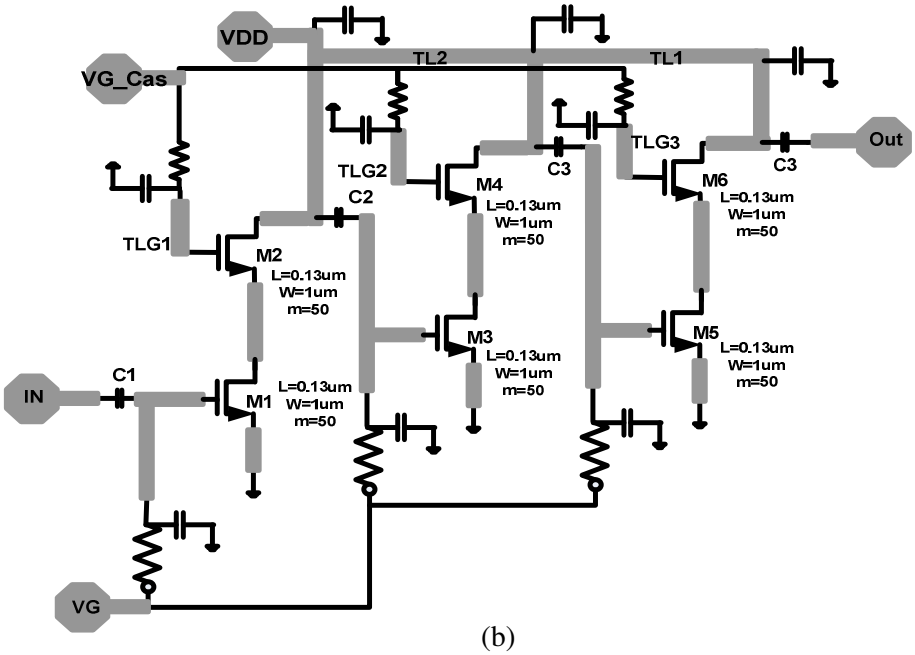
4.4 60 GHz Low Noise Amplifier in 0.13 µm CMOS Technology

One of the key blocks in a 60 GHz phased array receiver is low noise amplifier. A gain of at least 20 dB is required for the LNA to overcome the noise of following stages. Figure 4.11, shows the cross section of BEOL (Back End of the Line) layers and a schematic diagram of the 3 stages cascode low noise amplifier based on the cascode topology presented in Figure 4.2b. Matching components were implemented using micro-strip transmission lines. MA (top) metal layer was used for signal and M_1, M_2 and M_3 were connected together and used as the ground plane. Transmission lines TL_{G1}, TL_{G2}, TL_{G3} (See Figure 4.11) were used to increase the gain of the cascode amplifier.

Also by proper design for good isolation between bias lines and V_{DD} of the gain stages, single V_{DD}, VG and V_G_Cascode were implemented for biasing the amplifier.The transistor is sized and biased (W/L= 50/0.13 um and bias current=7 mA) for achieving minimum noise figure [103] at 60 GHz. As illustrated in Figure 4.12, gain control of about 13 dB (between 10 to 23 dB) was achieved through the variation of the bias of the cascode transistor of each stage.



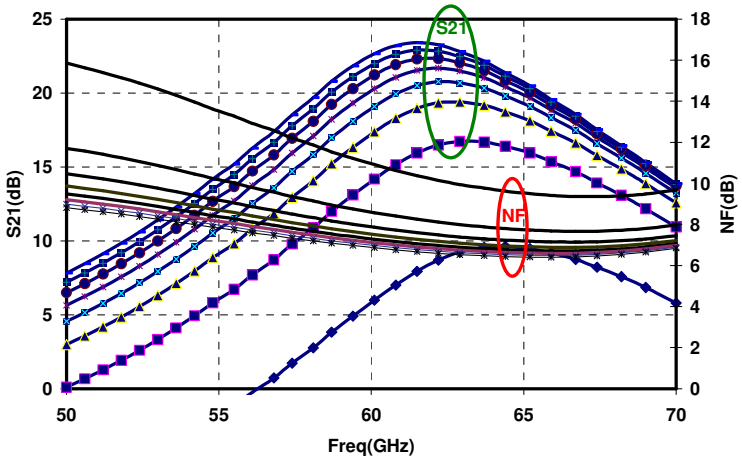
(a)



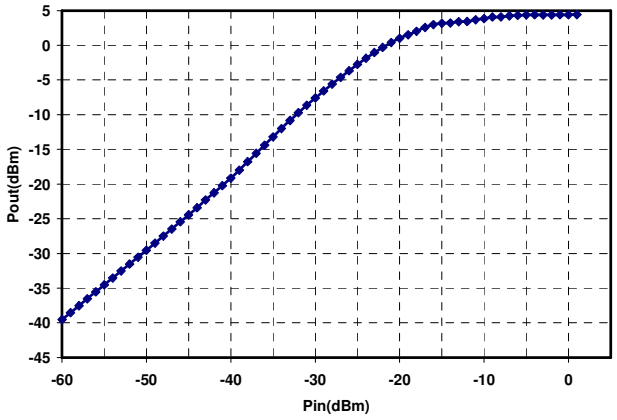
(b)

Figure 4.11: (a) Process BEOL cross section (b) 3 stages cascode amplifier in 0.13 µm CMOS at 60 GHz.

The LNA gain control can be used by beam-forming controller to adjust the gain of each path and compensate the phase shifter insertion loss variation in the array configuration. Figure 4.12b shows the P_{out} versus P_{in} characteristic of the amplifier. The input P_{1dB} of the amplifier is -16.8 dBm and the saturated output power of the amplifier is about 5 dBm. The simulated noise figure of the amplifier is 6.7 dB under typical process condition. Figure 4.12c illustrates the IP_3 simulation results for the designed amplifier. IIP_3 of the amplifier is -7.13 dBm.



(a)



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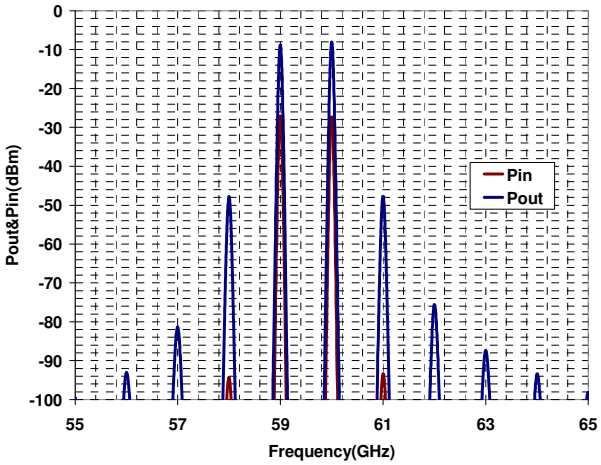
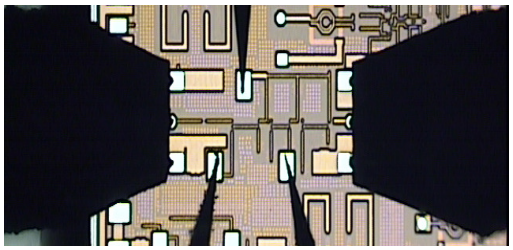
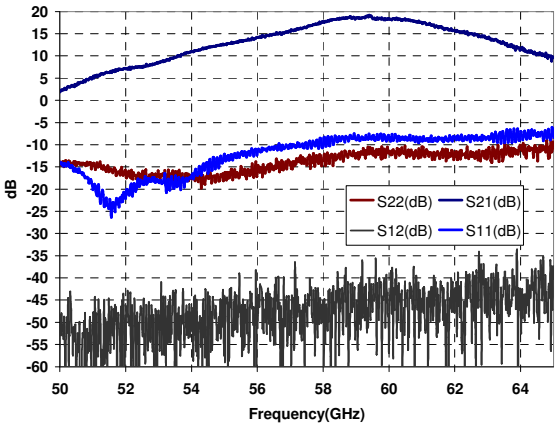


(c)

Figure 4.12: (a) Simulated Gain and NF variation versus control voltage (cascode bias). (b) Pout versus Pin (Input P_{1dB}=-16.8dBm) (c) IP_3 simulation (IIP_3=-7.13dBm)

Figure 4.13 shows the die micrograph and two port measurement results of the amplifier. Maximum measured gain of about 19 dB at 59.5 GHz at V_{DD}=2 V was achieved. Measured input and output return loss over 57 to 66 GHz was better than 9 dB. The 3 dB bandwidth of the LNA is about 5 GHz around the center of 59.5 GHz.





(a) (b)

Figure 4.13: (a) Die photo of 60 GHz CMOS amplifier in 0.13um CMOS technology (b) Measured S parameters of the amplifier.

4.4.1 90º Hybrid for Balanced Amplifier and Phase Shifter

Quadrature coupler is an essential element of many microwave and millimeter-wave circuits such as balanced amplifiers, image reject mixers, and phase shifters. Many of these applications require broadband 3 dB couplers which are realized either by using tightly coupled interdigitated multi-conductor lines such as the Lange coupler, or by using broadside coupled lines[104]-[105]. Figure 4.14 shows the lumped element model of Branch line (capacitvely coupled) and Lange (inductively coupled) quadrature couplers. For a given characteristic impedance and operating frequency, one can calculate the value of lumped elements in the models[105]-[108]. At microwave frequency (below 30 GHz), lumped element quadrature couplers considerably save the silicon area compared to their distributed counterparts. Generally, Lumped circuits presented in Figure 4.14 are not able to provide enough bandwidth for ultra-wideband or broadband applications.

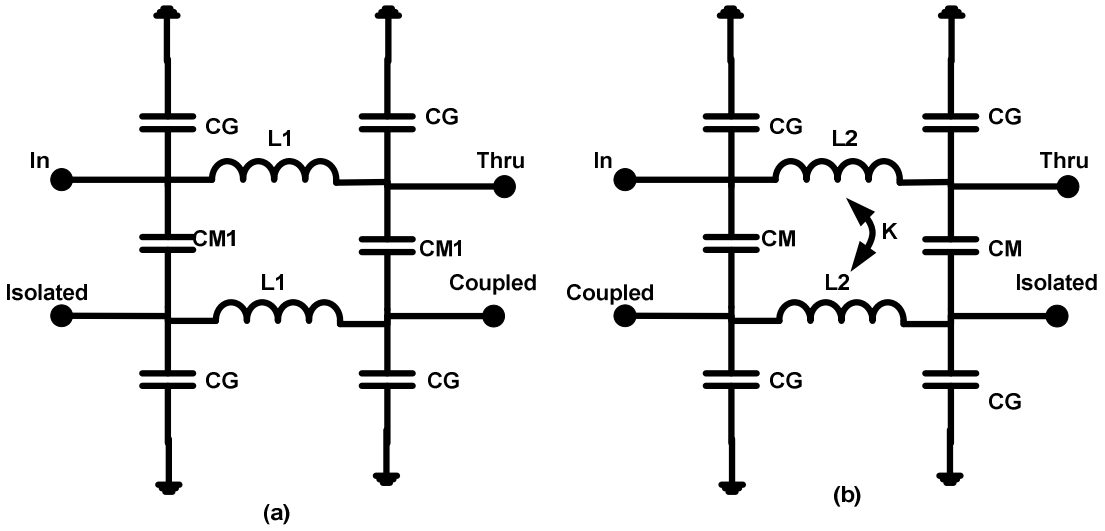


Figure 4.14: lumped element model of (a) capacitvely and (b) inductively coupled hybrids

For a relative broadband 90^o hybrid that can be used in the design of both balanced amplifier and phase shifter, a broadside coupler is used. Broadside couplers are composed of two parallel microstrip lines which are implemented at different layers in a multi-layers transmission line. The structure presents a broadband behavior as a 90^o coupler[110].

A broad-side coupler was designed in 0.13 μm CMOS technology. The structure is implemented on the thick top metals (MA and E_1 in Figure 4.11b) of this process as shown in Figure 4.15. By choosing W=10 μm and Δ=1 μm, one can design a broadband 90º hybrid

over the frequency band 50-70 GHz. 3D EM simulation results of hybrid are demonstrated in Figure 4.16.

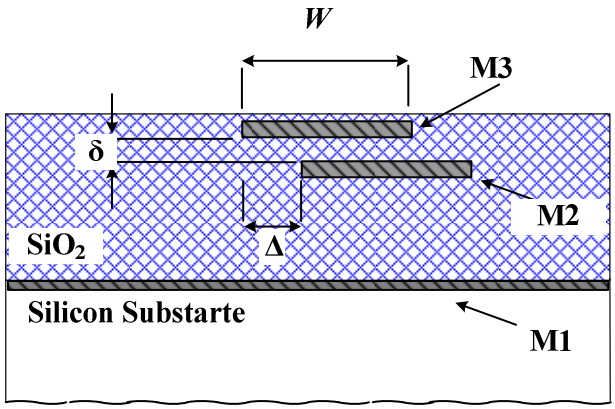


Figure 4.15: A cross section of 90º broadside coupler (M2=E_1, M3=MA in IBM 0.13 µm Technology)

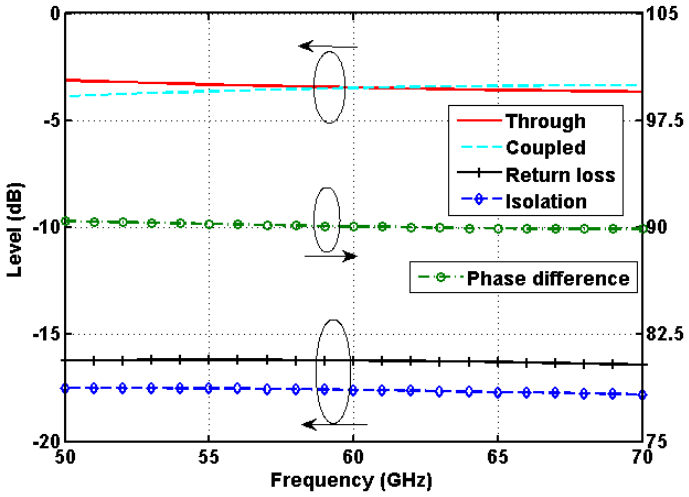
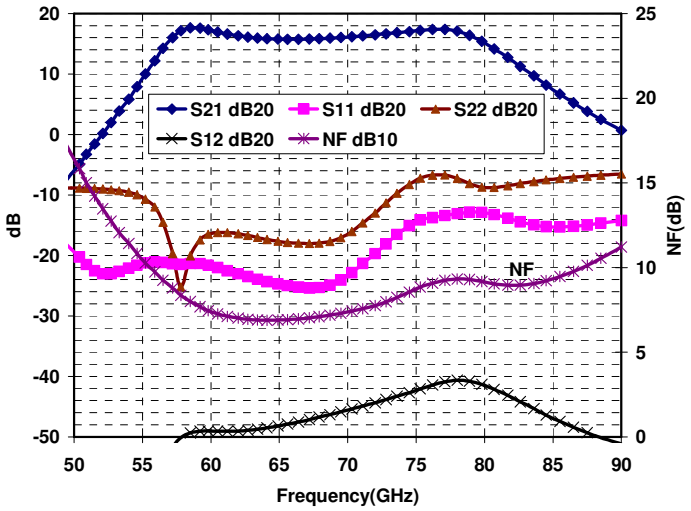


Figure 4.16: Simulated phase difference, coupling level, isolation, and return loss of the designed broadband 90º coupler.

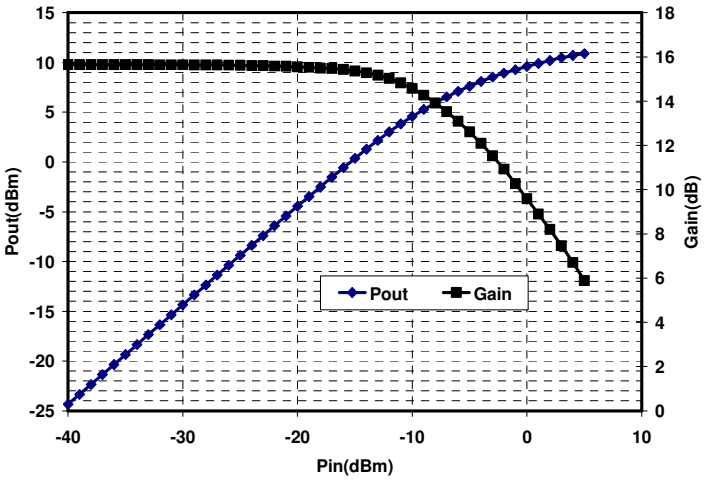
4.4.2 60 GHz Balanced Amplifier

Using the designed coupler in section 4.4.1 and a two stage cascode amplifier, a balanced amplifier was designed to cover the whole band of 57-66 GHz for a wideband

front-end option. This design has enough bandwidth to tolerate the effect of layout parasitics and process variation on the bandwidth. Simulation results of this amplifier are shown in Figure 4.17. The amplifier has a gain of above 15 dB over a wide range of frequency from 57 GHz to 77 GHz. The input and output return losses are better than 13 dB and 7 dB respectively over the whole range of frequency. The minimum noise figure of amplifier is about 7.5 dB and below 10 dB over the whole band. The input P1db is -10.3 dBm at 60 GHz and the output saturates around 12 dBm.



(a)



(b)

Figure 4.17: (a) Simulated gain, matching, Isolation, and noise figure (b) Linearity (Input P_{1dB}=-10.3 dBm) of the designed balanced amplifier.

4.5 Millimeter-wave Phase Shifters

In general, phase shifters can be classified into digital and analog types. In digital phase shifter, multi stages of fixed phase shift stages are cascaded. These stages are either utilized or by-passed by switches. Although, the linearity of a digital passive phase shifter is fairly good, the main difficulty is the loss associated with the switches [112],[116],[117]. Moreover, digital phase shifters do not provide continuous phase shifting. This results in high side-lobe level in the array radiation pattern and creates beam pointing error with no on-chip calibration/correction flexibility. It also requires a more complex beamforming algorithm as well as array calibration.

Different phase shifter architectures such as switched transmission lines, High-pass/Low-pass phase shifters, and analog phase shifters (i.e. vector summing phase shifters and reflective-type phase shifters (RTPS) have been proposed and used in various microwave and mm-wave integrated circuits [105],[111]-[115].

The high-pass/low-pass phase shifter is basically functioning by taking the difference between the phase from the high-pass filter path and the low-pass filter path of a particular bit. By arranging the CMOS switches to permit switching between low-pass and high-pass, it becomes possible to make a certain phase shift between two states [111],[118][119]. Like switched transmission line phase shifter, however the linearity of the phase shifter is good but the insertion loss of the overall phase shifting is quite high.

Analog phase shifters vary the phase continuously. This type of phase shifter in a phased array transceiver can support an important class of beam-forming algorithm called "zero knowledge beam-forming algorithms" [60]. This type of algorithm does not need calibration and knowledge of the phase shifter variations in each path due to fabrication process, supply and temperature variations. Two well-known analog structures are vector summing phase shifters and reflective-type phase shifters (RTPS).

The most common configuration for an active phase shifter is the vector/sum architecture [111],[114],[119] shown in Figure 4.18. The input signal is converted to two components with a 90º phase difference. Then, by changing the gain of VGA (Variable Gain

Amplifier) in each path and combining the two components, different phase shift in one quadrant can be achieved. To select the different quadrants, one 0/180º phase shift circuit is used in each path.

The advantage of this architecture is that it can achieve 360º phase shift. The disadvantages are complexity of phase shift control from an algorithm perspective, a large silicon area, and linearity [120]-[121].

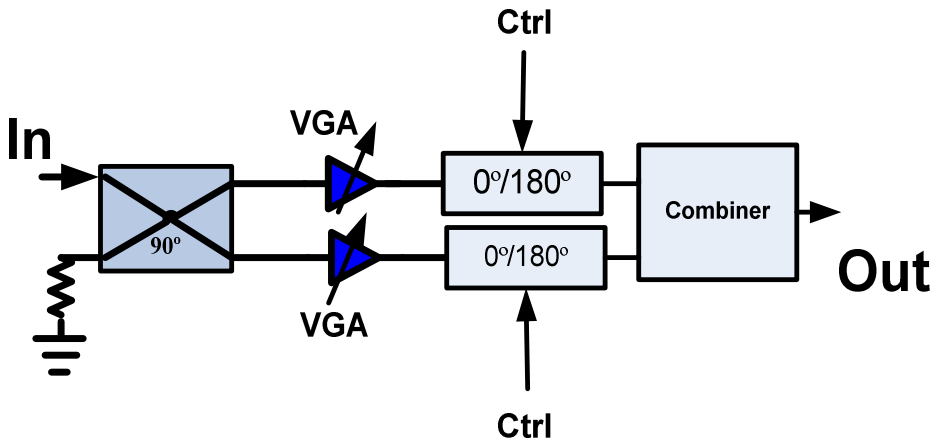


Figure 4.18: A block diagram of vector/sum phase shifter

4.5.1 Continuous Reflective Type Phase Shifter

Figure 4.19 shows the general block diagram of the RTPS, which employs a 4-port 90º hybrid and two similar purely imaginary (reflective) loads. The through and coupled ports of the hybrid are terminated to the reflective loads and the isolated port is used as the output.

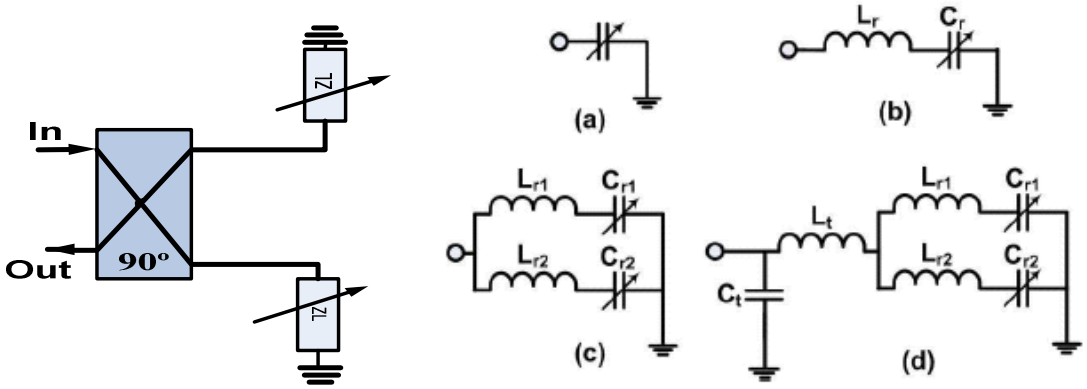


Figure 4.19: A block diagram of reflective type phase shifter and reflective load options.

The reflection coefficient at the reflective load is:

$$\Gamma = \frac{jB - Z_0}{jB + Z_0} = 1\angle\phi$$

$$\phi = -2\tan^{-1}\frac{B}{Z_0}$$

The reflective loads are varied electronically by changing the control voltage of the varactor. Thus, the phase of the reflection coefficient at the through and coupled ports changes, which results in the phase shift of the output signal. The amount of the phase shift depends on the load reactance.

A single varactor cannot provide a phase shift more than 75º in practice [105]. Adding a series inductor can increase the phase shift up to 180º. To achieve a complete 360º phase shift one should use dual resonant loads[105]. The RTPS, being fundamentally passive, shows linear input-output characteristics [122]. The main challenge in the integrated CMOS based RTPS design is the loss. The main sources of loss in an RTPS are the transmission-line loss in the 90º hybrid and the loss in the reflective terminations.

To reduce phase shifter loss, active, negative resistance circuits have been used in RTPS designs [115]. This, however, limits the linearity and noise performance of the RTPS.

The insertion-loss variation can also be minimized by using an equalization resistance and modification of the 90º hybrid [123].

4.5.1.1 60 GHz RTPS in CMOS Technology

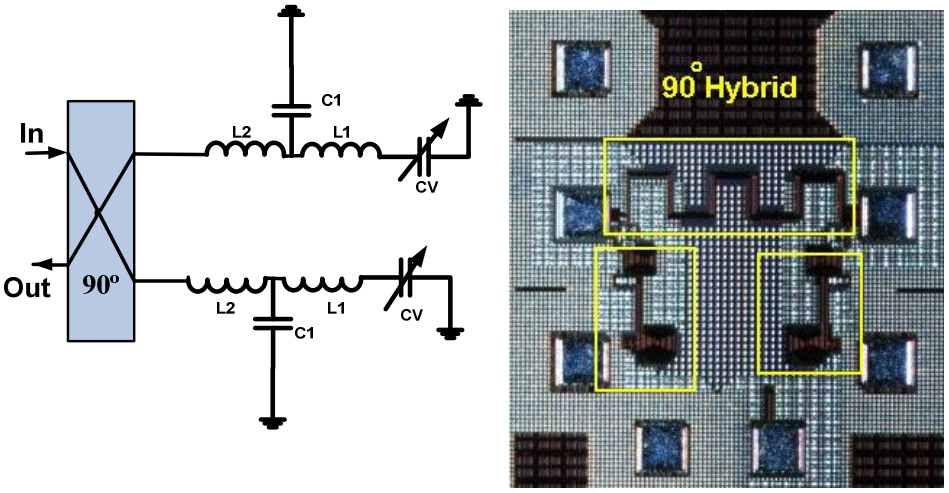
In the integrated RTPS design, varactors are used as the main component in the design of the reflective loads. An RTPS was designed and fabricated in ST 90 nm CMOS technology. Varactors in the reflective load were implemented by NMOS transistor in which the *Source* and *Drain* terminals are connected together. A transistor with W=28 μm (n_f=28 W_f=1 um) and L=0.37 μm. At 60 GHz frequency, by varying the applied DC voltage from 0 to 1 V, the capacitance of the varactor varies between ($C_{v,min}$) of 49 fF and 150 fF. The proposed reflective load is shown in Figure 4.20. This load contains two inductors, a capacitor and a varactor. The input impedance of this load, where the inductors and capacitors are ideal elements with pure imaginary impedance is given by

$$Z_{in} = j\left(\frac{\omega^2 L_1 C_v - 1}{\omega C_v + \omega C_1 - \omega^3 C_v C_1 L_1} + \omega L_2\right) \qquad (4\text{-}1)$$

where C_v denotes the varactor capacitance and C_1, L_1 and L_2 are the capacitance and inductance of the matching elements shown in Figure 4.20a. The phase of the reflection coefficient can be expressed as

$$\theta = -2\tan^{-1}\left(\frac{\mathrm{Im}(Z_{in})}{Z_0}\right) \qquad (4\text{-}2)$$

The output phase of the phase shifter changes with θ, which itself depends on varactor capacitance, C_v. By setting $L_1=(\omega^2 C_{v,min})^{-1}$, $C_1=C_{v,max}/(\omega^2 L_1 C_{v,max}-1)$ and L_2=0, the output phase changes from 0° to 180º. In practice, the resistive parts of the inductors and capacitors limit the overall phase shift of the phase shifter and add to the insertion loss. By optimizing L_1, L_2 and C_2, (at 170 pH, 60 pH and 60 fF, respectively) an optimum load with minimum loss and more than 90º phase shift over the frequency range of interest is attained.



(a) (b)

Figure 4.20: RTPS (a) Circuit diagram (b) Die photo

The die micrograph of the fabricated phase shifter is shown in Figure 4.20b, where the chip area excluding pads is 0.3×0.25 mm^2. Using on-chip measurements with Cascade probes, the phase shifter was tested from 50 to 65 GHz. The insertion loss versus the control voltage is shown in

, for a set of frequencies. With only small changes in insertion loss over frequency, this phase shifter demonstrates approximately 3.5 dB of loss variation across all control voltage values. As discussed in [52] the variation in insertion loss is an intrinsic characteristic of passive or digital phase shifters but it can be compensated to a large extent by an efficient beamforming algorithm.

Figure 4.22 shows the measured phase-shift of the phase shifter versus frequency for different control voltages. The phase varies linearly over 50-65 GHz frequency range. At each frequency the 90º continuous phase shift is obtained by changing the control voltage.

Figure 4.23 depicts the insertion loss and input matching of the phase shifter over the entire bandwidth of 15 GHz. The maximum insertion loss is 8 dB (at 0.4 V control voltage).

The return loss of the phase shifter is more than 12 dB at all phase states. Figure 4.24 depicts the measured output power versus input power at 0.4 V control voltage, which verifies the linear performance of the device. Thus, the P_{1dB} point of this device is higher than 4 dBm.

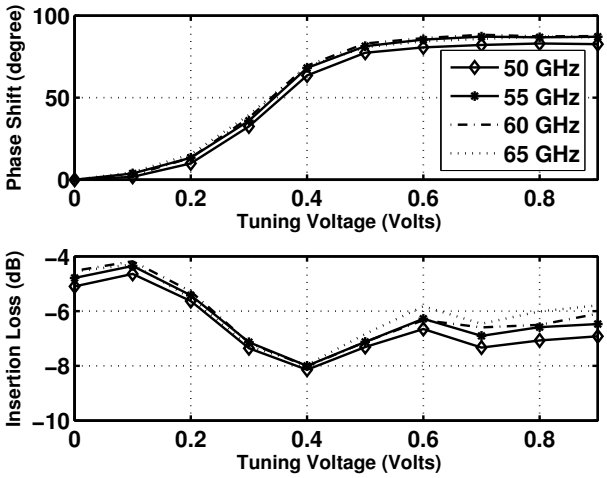


Figure 4.21: Measured relative phase shift and insertion loss of the phase shifter versus control voltage at 50, 55, 60 and 65 GHz.

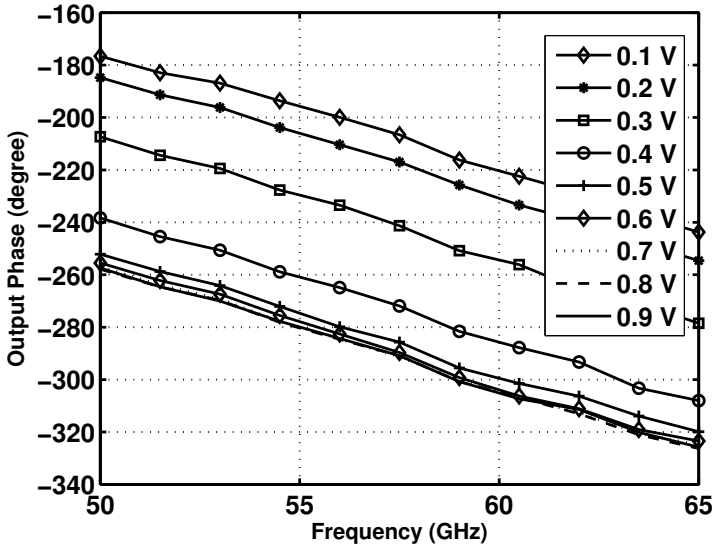


Figure 4.22: Measured output phase of the phase shifter versus frequency for various varactor control voltages.

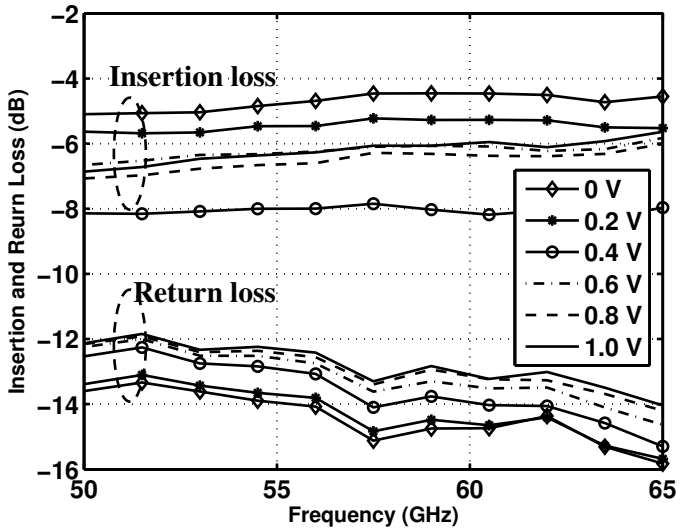


Figure 4.23: Measured insertion loss and input return loss of the phase shifter versus frequency for various control voltages.

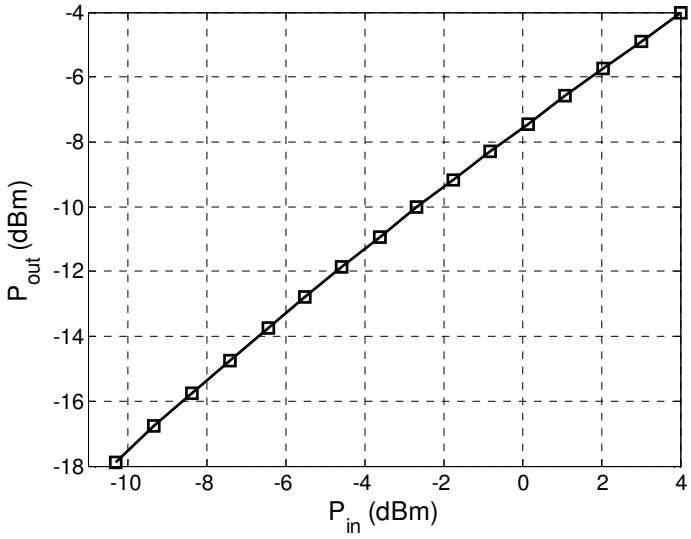


Figure 4.24: Measured output power versus input power at 0.4 V control voltage.

Table 4.2: Comparison of this work with other mm-wave CMOS phase shifters

Reference	[124]	[125]	[126]	[111]	This Work
Technology	CMOS	CMOS	CMOS	CMOS	CMOS

	130 nm	65 nm	90 nm	130 nm	90 nm
Frequency (GHz)	15-26	55-65	40- 75	60	50-65
Phase shifter type/ Step	VM 4-bit	Digital 4-bit	VM Cont's	VM 4-bit	RTPS/ Cont's
Phase shift	360°	180°	360°	360°	90°
Die Area	0.14mm^2	0.2 mm^2	0.4 mm^2	0.95 mm^2	0.08 mm^2
Power Consumption	11.7 mW	~0 mW	30 mW	72 mW	~0 mW
Insertion loss (dB)	3.5± 2.5	9.4± 3.1	18 ± 2	N/A	6.25 ± 1.75

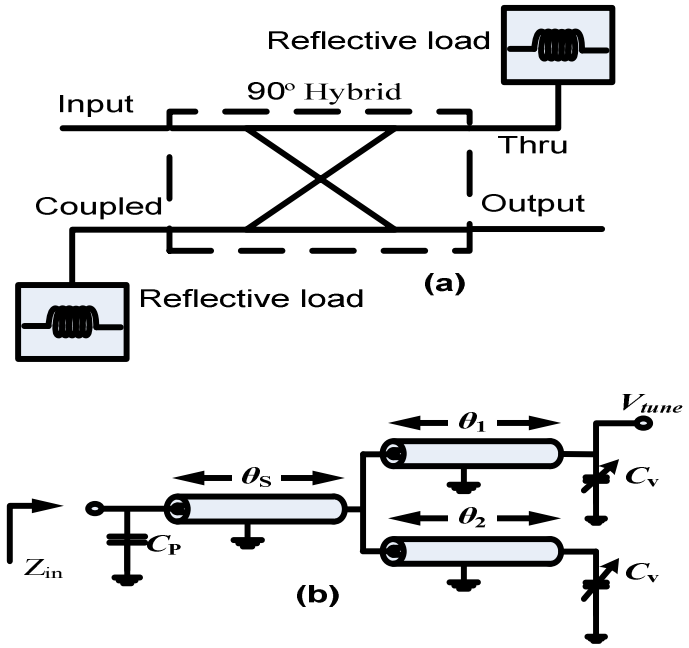


Figure 4.25: (a) RTPS. (b) Reflective load.

To achieve maximum phase shift range, a dual resonance load was used in 0.13 μm IBM CMOS technology.

Figure 4.26 shows the simulated Q and capacitance of a NMOS varactor (W=2.5um L=0.24um and m=16) in 0.13 um IBM CMOS technology. The Q versus control voltage drops to as low as 5 at 60 GHz. The effect of limited Q is lowering the phase shift and increasing the insertion loss variation of the phase shifter versus tuning voltage. Therefore,

an impedance transformer has been used to minimize the insertion loss variation while maximizing the phase shift. Using RTPS topology and the described varactor,

simulated phase shift of more than 270º and insertion loss of 10 ±1 dB was achieved (Figure 4.27).

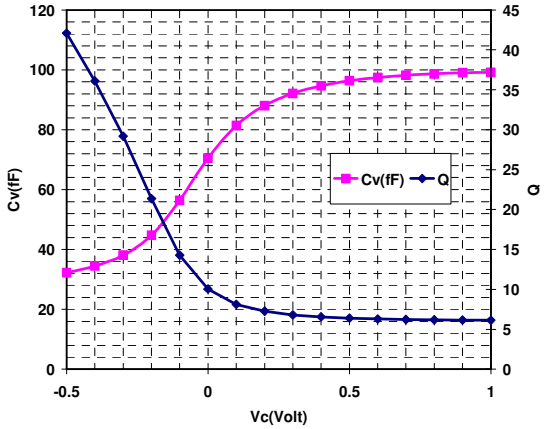


Figure 4.26: Quality factor and varactor capacitance versus control voltage at 60 GHz

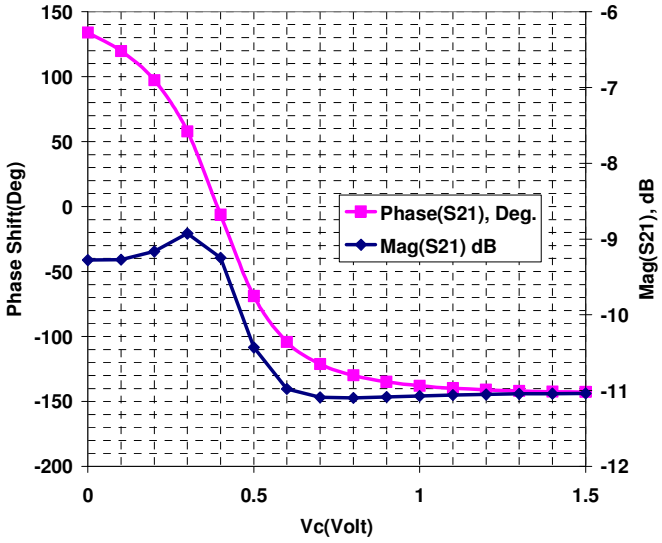
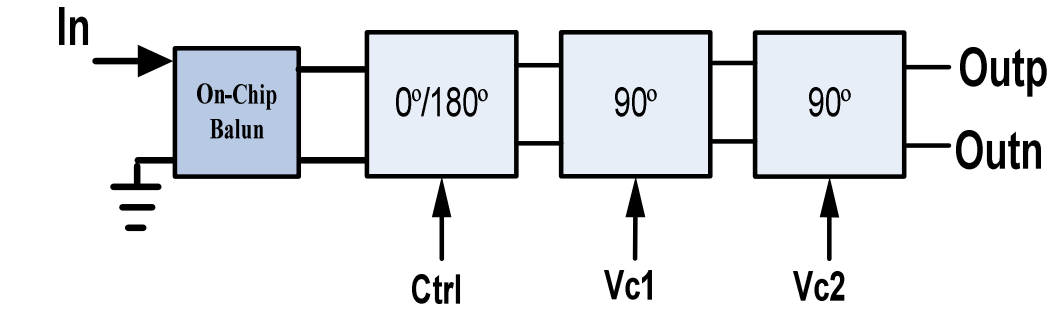


Figure 4.27: Insertion loss and phase shift versus control voltage at 60 GHz

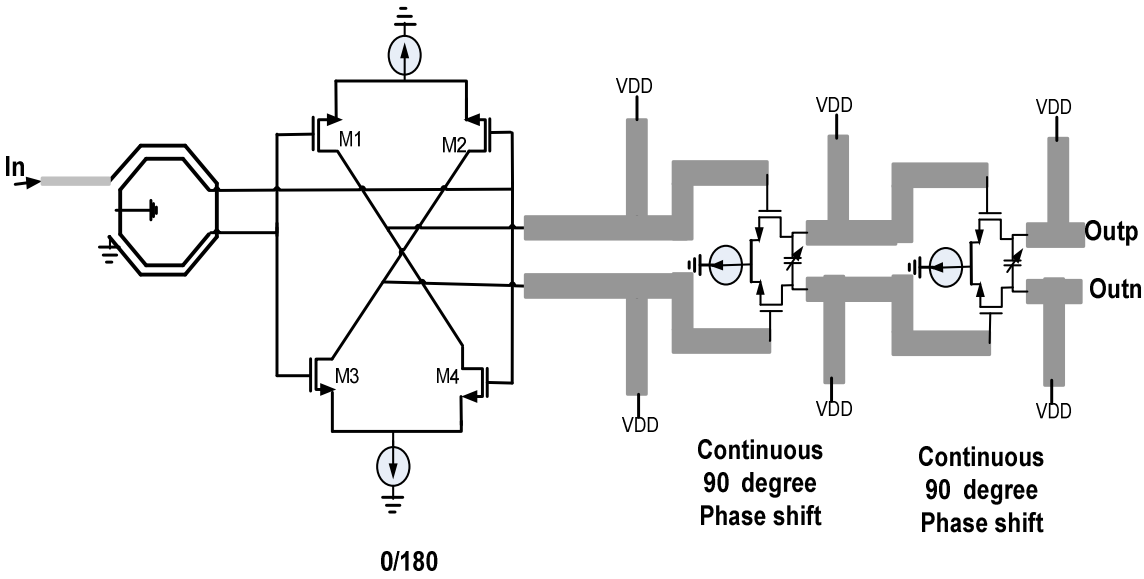
4.5.2 Proposed Continuous Active Phase Shifter

4.5.2.1 Resonance based Phase Shifter

Considering the ultimate operational requirement of the front-end in a System on Chip (SoC) environment, it is highly advantageous to have a differential front-end at the expense of more area and higher power consumption.



(a)

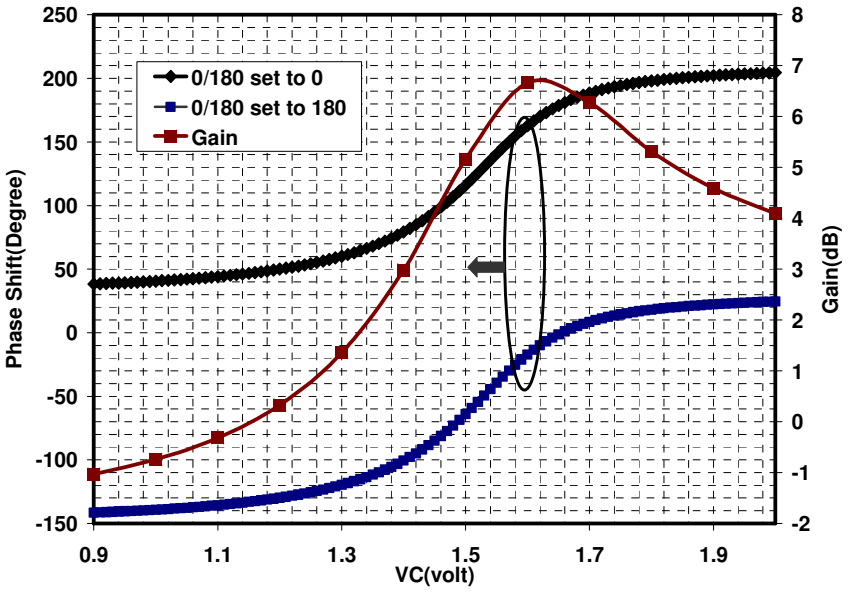


(b)

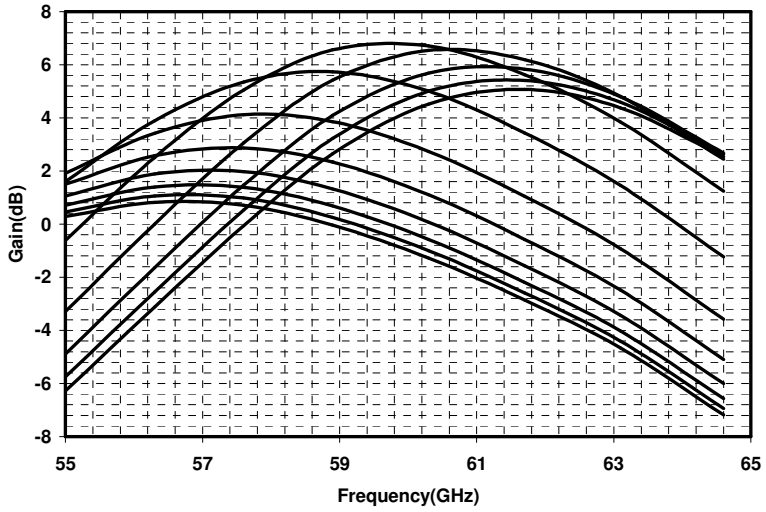
Figure 4.28: 360º phase shifter architecture based on resonance based (a) Blok diagram (b) implementation

A differential 360º phase shifter is proposed and designed based on a resonance based architecture. Using the sharp phase transition nature of a resonance circuit at its resonance and by varying the resonance frequency using a varactor at the output, phase of the output related to the input signal can be varied. Considering the loss of inductive loads and varactors a phase shift of 90º per stage is achievable. Figure 4.28a shows the arrangement of 360º phase shifter. First the single ended input signal is converted to differential through an on-chip balun. Then the differential signal passes through a one bit 0/180º phase shifter followed by two continuous 90º phase shifter. Circuit implementation of the phase shifter is demonstrated in Figure 4.28b. The 0/180º phase shift is implemented by switching the output of a differential amplifier circuit. All the loads and interconnections between the blocks use micro-strip transmission lines.

Simulation results of the designed phase shifter with this topology in IBM 0.13 µm CMOS technology are shown in Figure 4.29 and Figure 4.30. IIP_3 of the designed phase shifter is 17 dBm.



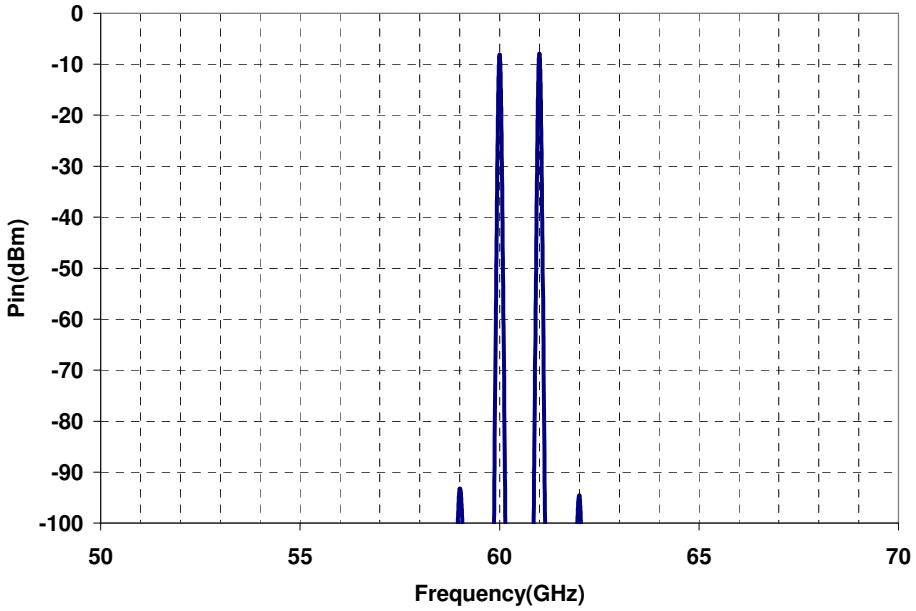
(a)



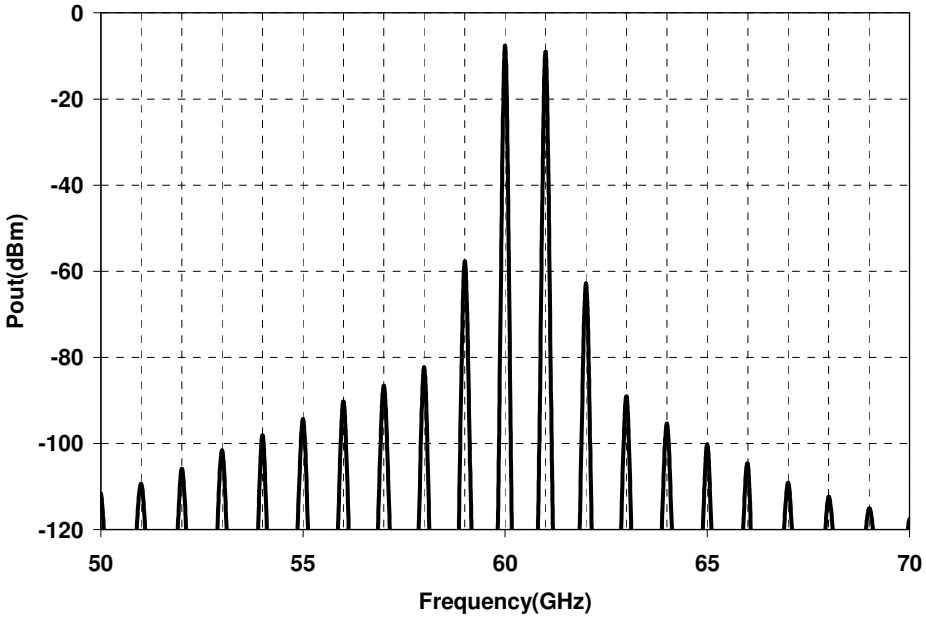
(b)

Figure 4.29: (a) Phase shift and gain variation versus control voltage at 60 GHz

(b) Gain variation versus control voltage over the range of 55-65 GHz



(a)



(b)

Figure 4.30: (a) Two tones at 60 and 61 GHz at the input of phase shifter

(b)Two tones and the generated inter-modulation products at the output of phase shifter

4.5.2.2 All Pass Type Phase Shifter

From the beam-forming algorithm simplicity and maximizing array factor perspectives, minimum gain or insertion loss variation is a desirable feature for the phase shifter.

Ideally, all-pass filters present a constant amplitude characteristic and a variable phase response over the frequency range of interest. At millimeter-wave frequencies, active approaches are preferred to reduce the loss or even have some gain for the phase shifter. Based on the active all-pass topology concepts presented in [127][128], a 60 GHz phase shifter was designed to achieve full range. Figure 4.31 shows the circuit diagram of the implemented phase shifter. The all pass stage provides a continuous 0 to 180º phase shift. A 0/180º switch is implemented to provide the phase shift from 180 to 360º part of the range. Figure 4.32 demonstrates the phase shift range and gain variation at 60 GHz as well as gain variation over the frequency range of 55 to 65 GHz. This phase shifter shows gain variation of about 5 dB and consumes less power consumption compared the resonance based phase shifter.

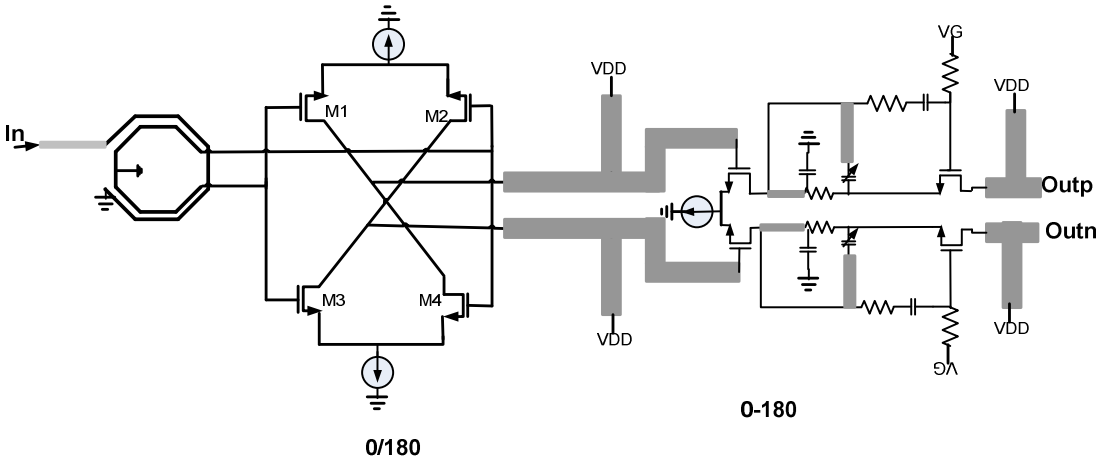
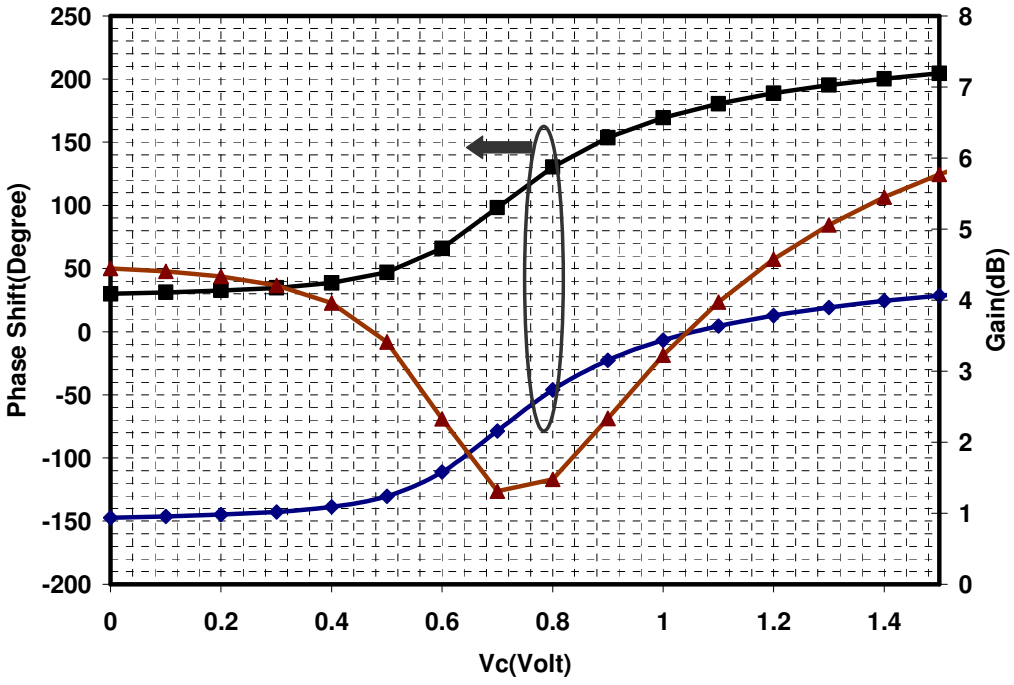


Figure 4.31: 360º all-pass type phase shifter architecture



(a)

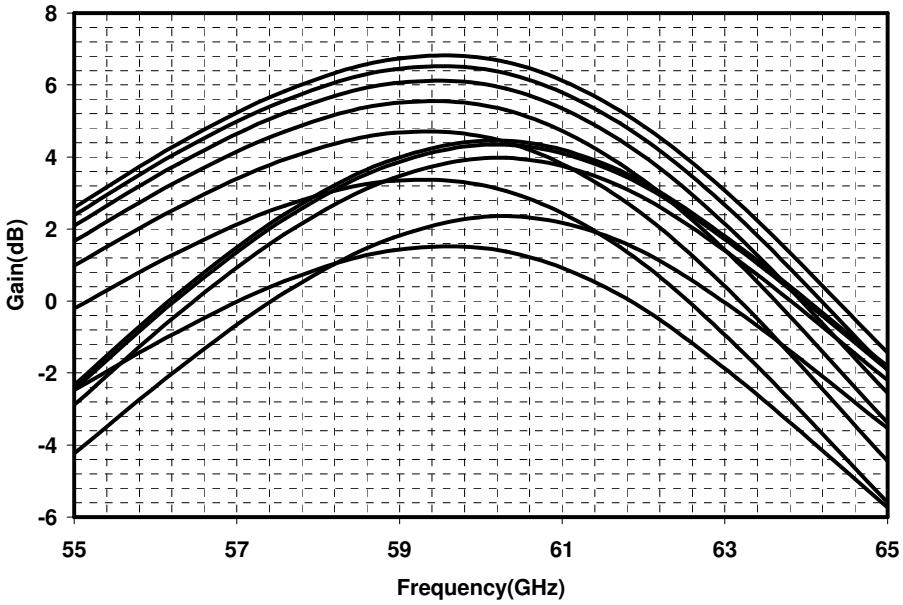


Figure 4.32: (a) Phase shift and gain versus control voltage at 60 GHz

(b) Gain variation versus control voltage over frequency

4.5.3 Comparison and discussion

In the previous sections, different phase shifter architectures were designed and developed. The following table shows a qualitative comparison of the phase shifter parameters such as linearity, chip area, power consumption and insertion loss variation for the three proposed phase shifter architectures.

Phase shifter Type	Linearity	Chip area	Power Consumption	Insertion loss variation
RTPS	Highest	Medium	Lowest	Lowest
Resonance Based	Medium	Medium	Highest	Highest
All-pass type	Low	Lowest	Medium	Medium

4.6 60 GHz Double Balanced Mixer

In RF-phase shifting array architecture the signals from different antennas are combined in the front-end and the combined signal will be applied to a down-conversion mixer. For common mode noise reduction in a system on chip environment, it is preferred to have differential architecture to reduce the coupled noise from noisy parts such as digital to sensitive RF circuits. The details of possible receiver front-end architectures and frequency plan of a RF phase shifting receiver are discussed in section 4.7. As part of the receiver architecture, a double balanced mixer was designed in 0.13 μm CMOS technology. The double-balanced structure in Figure 4.33 provides higher LO to RF isolation compared to the single gate mixers [129] or single balanced mixers[29]. In the proposed architecture, with RF frequency of 57 to 64 GHz and LO frequency of 45.6 to 51.2 GHz, the IF center frequency varies between 11.4 to 12.8 GHz.

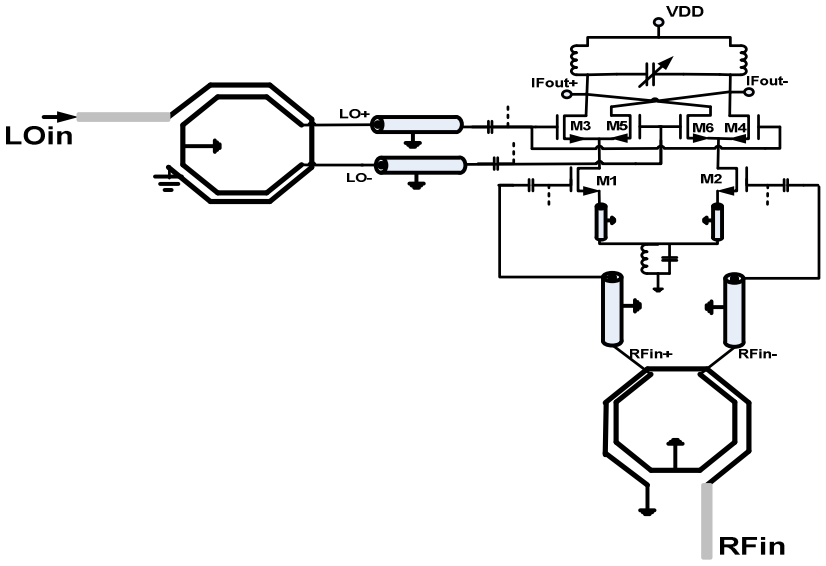


Figure 4.33: 60 GHz double-balanced mixer with two passive baluns.

RF	LO	IF
57 GHz	45.6 GHz	11.4 GHz
60 GHz	48 GHz	12 GHz
64 GHz	51.2 GHz	12.8 GHz

Two passive baluns are used to provide single-ended to differential conversion at the RF and LO inputs of the mixer. The balun has a relatively small footprint at 60 GHz (83 × 83 μm^2) and is implemented in the top two metals (MA as signal layer and E_1 as the ground layer). Metal width, spacing, number of turns and sizing are all optimized to provide low insertion loss and maximum voltage swing at the output port by using HFSS.

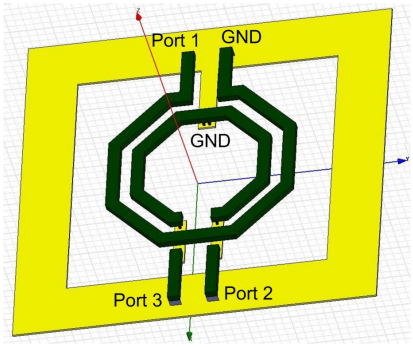


Figure 4.34:: 60 GHz passive transformer.

4.6.1 Simulations and Measured Results

The mixer is fabricated in IBM 0.13 μm CMOS technology that has 8-metal layers (3 thin, 2 thick copper layers and 3 RF layers). An output buffer using the shunt peaking technique is implemented in order to drive the 50 Ω load of the measurement instruments. The measured results presented in this section reflect the performance of the mixer and the subsequent buffer. For these measurements (Figure 4.35) DC probes, and two signal generators and spectrum analyzer are used. The die micrograph of the fabricated mixer is shown in Figure 4.36. The overall system, including the two on-chip baluns, test PADs,

mixer and the buffer, occupies an area of 1100 × 746 μm^2. Electro-static-discharge (ESD) protection has been added to all PADs.

Figure 4.37 shows the spectrum of the mixer IF output. The output power at the frequency of 12.2 GHz is equal to −44 dBm. By excluding the 7.2 dB loss due to the IF cable and 1.5 dB loss due to the probe, the output power at the IF of 12 GHz is equal to −35 dBm.

Also, at the RF port, excluding a 15 dB loss due to RF cable, and a 1.5 dB loss due to the probe, the RF signal level at the input of the mixer is equal to −36.5 dBm. Therefore, the conversion gain of the mixer is equal to 1.5 dB. Considering all the losses at the LO port the input LO signal is 1.5 dBm. Based on the measurement results, the IF output covers a 2.3 GHz bandwidth. The center frequency of IF can be tuned by a varactor in parallel with the inductive load.

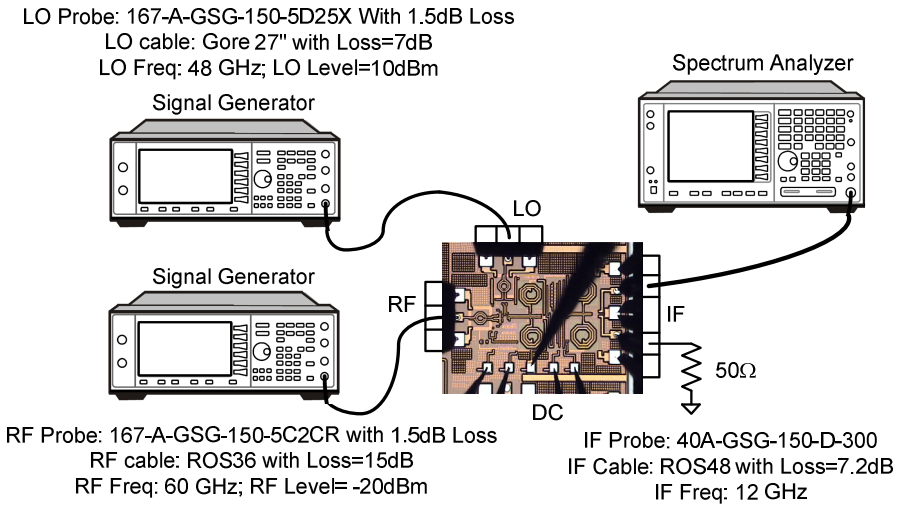


Figure 4.35: The measurement setup.

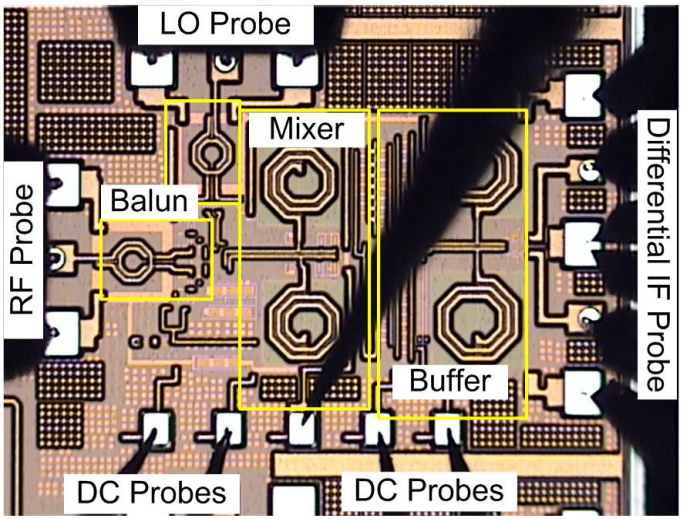


Figure 4.36: Die micrograph of mixer chip including the PADs, buffer, and baluns.

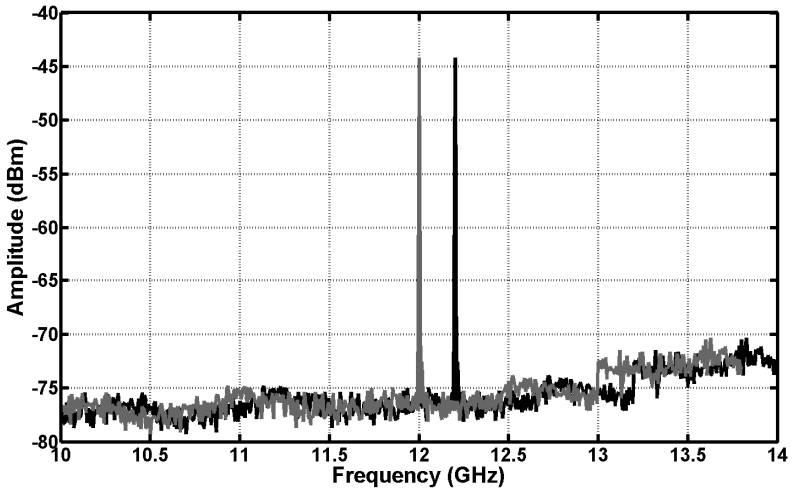


Figure 4.37: The measured output spectrum at IF.

Figure 4.38 depicts the interpolated measured (diamonds are measured points) conversion gain variation over the IF frequency range. As shown on this figure, the IF bandwidth is about 2.3 GHz.

The simulated IIP_3 of this mixer by applying the same amplitude of RF and LO as the measurement situation, is equal to 14.2 dBm (See Figure 4.40). Moreover, the mixer core works from a 1.5-V voltage supply and consumes 6 mW. The buffer needs a 1.5-V supply and consumes 7.8 mW. The overall chip including the buffers consumes 13.8 mW. Measured IF power versus RF power (RF frequency=60 GHz LO frequency= 48 GHz) is shown in Figure 4.39.

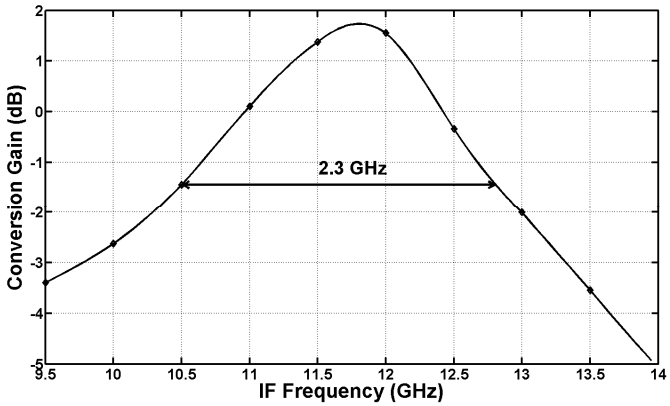


Figure 4.38: Measured conversion gain by sweeping LO and RF frequency by adding the total losses.

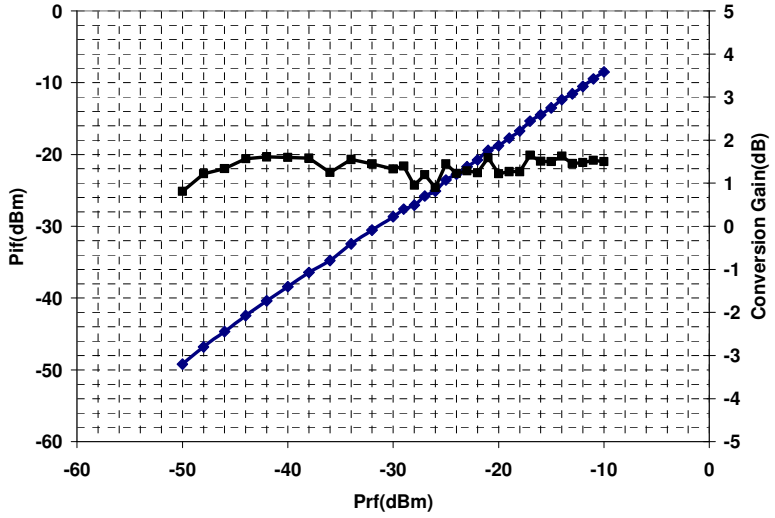
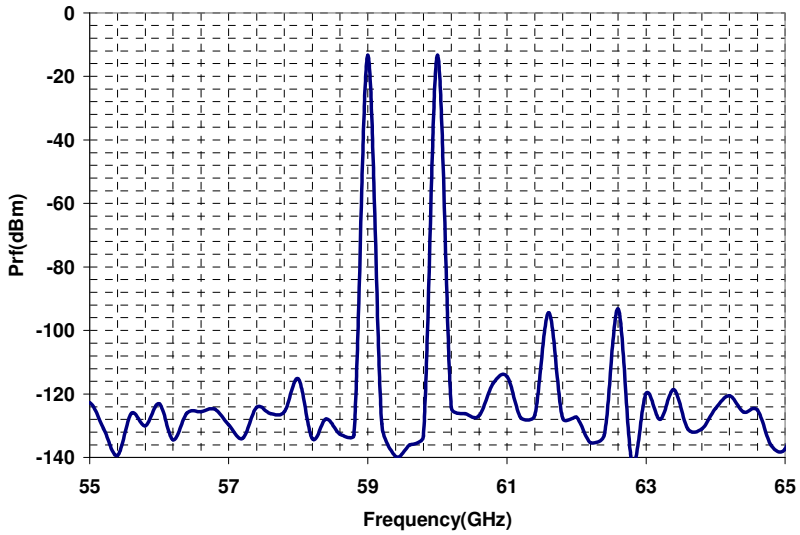
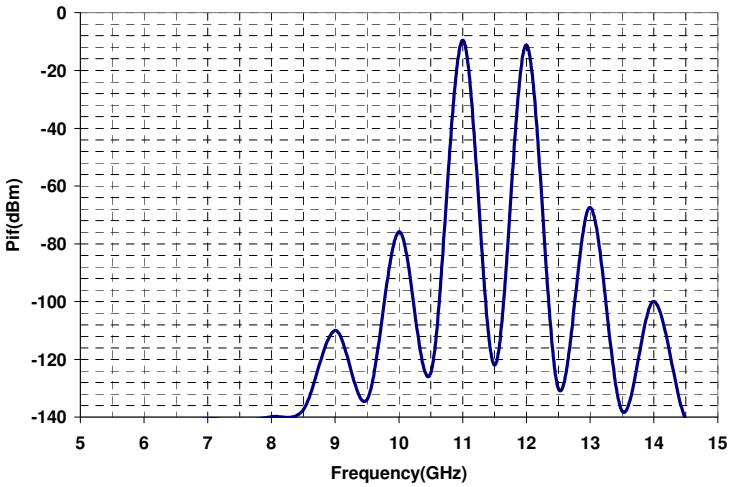


Figure 4.39: Measured power at IF versus RF input power (RF Frequency =60GHz and IF frequency =12GHz)



(a)



(b)

Figure 4.40: Linearity Simulation (a) Input RF tones at 59 and 60 GHz (b) IF tones and generated inter-modulation products (LO=48 GHz)

4.7 Proposed Phased Array Architecture

Different single antenna and antenna array architectures were discussed in chapter 2. Phased array radios are required for radio operation in an NLOS channel. Furthermore, phased array transceiver systems improve the received SNR and transmit EIRP. Radio architecture selection is a trade off between several criteria such as complexity of LO generation and distribution, power consumption, chip area, image rejection, and modulation scheme.

Recently, CMOS technology has received a great amount of attention to implement a single chip phased array at 60 GHz [136][140].

Phase shifting can be done in RF, LO, or IF sections of the receiver or transmitter. RF phase shifting architecture consumes less chip area and has the lowest LO routing complexity. However design of a low loss and linear front-end is challenging. Some of the developed phased array chips use low-resolution digital phase shifters, such as 2-bit phase shifters, to steer the antenna beam [137][138]. Use of continuous (analog) phase shifters increases the beam-space resolution and ERIP in the desired direction.

A variable IF dual conversion RF phase shifting architecture was proposed for the receiver and transmitter. Figure 4.41 demonstrates the proposed block diagram of an RF phase shifting 60 GHz phased array transceiver.

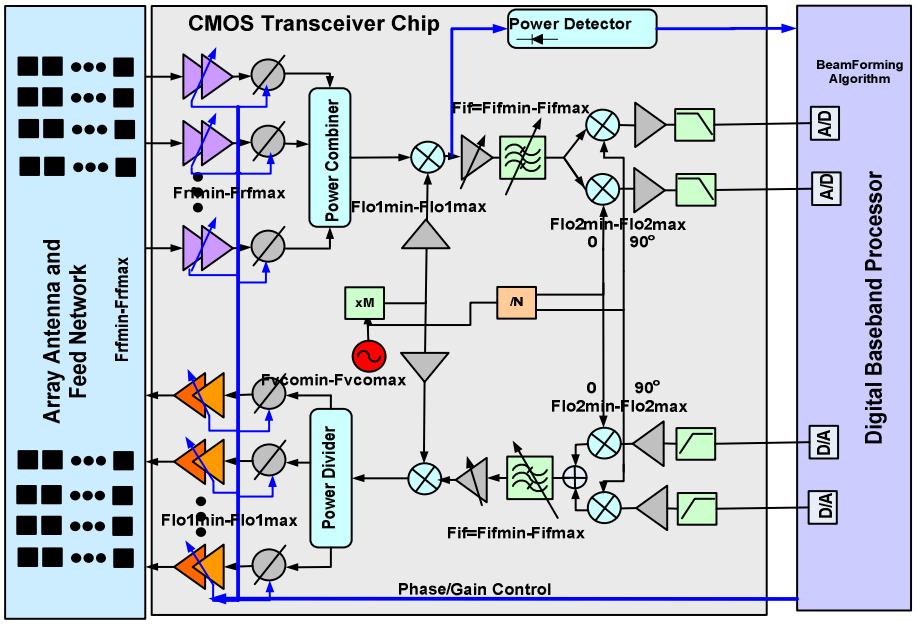


Figure 4.41: A block diagram of proposed phased array transceiver

For this architecture VCO frequency, frequency of applied LO to the first mixer, IF frequency and image frequency are calculated and given in Table 4.3.

This assumes a wideband front-end that covers 57-66 GHz, and a low noise amplifier which amplifies 57 GHz. Based on the amplifier results in Chapter 4, the amplifier has gain of above 5 dB at 52 GHz. From the front-end desensitization and image filtering perspectives, lower F_{LO1} is desirable. On the other hand, a high frequency VCO and IF are not desirable options. Considering all the trade offs analyzed as well as taking into account the phase noise performance of the VCO given in Table 4.4, option II shown in the table below seems the best frequency plan choice for the architecture.

Table 4.3: Different frequency plans for the transceiver architecture

	F_{RF}	M	N	$f_{LO1}=$ $(MN/MN+1)f_{RF}$	$f_{Image}=$ $(MN-1)f_{RF}/(MN+1)$	$f_{VCO}=$ $(N/NM+1)f_{RF}$	$F_{IF1}=F_{LO2}=$ $f_{RF}/(MN+1)$
I	57-66 GHz	1	2	38-44 GHz	19-22 GHz	38-44 GHz	19-22 GHz
II	**57-66 GHz**	**2**	**2**	**45.6-52.8 GHz**	**34.2-39.6 GHz**	**22.8-26.4 GHz**	**11.4-13.2 GHz**
III	57-66 GHz	3	2	48.9-56.6 GHz	40.7-47.1 GHz	16.3-18.9 GHz	8.1-9.4 GHz
IV	57-66 GHz	4	2	50.7-58.7 GHz	44.3-51.3 GHz	12.7-14.7 GHz	6.3-7.3 GHz
V	57-66 GHz	1	4	45.6-52.8 GHz	34.2-39.6 GHz	45.6-52.8 GHz	11.4-13.2 GHz
VI	57-66 GHz	2	4	50.7-58.7 GHz	44.3-51.3 GHz	25.3-29.3 GHz	6.3-7.3 GHz
VII	57-66 GHz	3	4	52.6-60.9 GHz	48.2-55.8 GHz	17.5-20.3 GHz	4.4-5.1 GHz
VIII	57-66 GHz	4	4	53.6-62.1 GHz	50.3-58.2 GHz	13.4-15.5 GHz	3.4-3.9 GHz

Table 4.4: Comparison of VCO phase noise for different architecture assuming fixed current consumption

Band Option	Simulated VCO Tuning Range	Simulated Phase Noise @1MHz	
II	**22.5-29.2 GHz**	**24 GHz**	**-95.48** dBc/Hz
III	16.3-21.2 GHz	17 GHz	-98.35 dBc/Hz
V	44.25-53.75 GHz	48 GHz	-86.4 dBc/Hz

With an architecture using frequency plan II, the first mixer downconverts the combined RF signals form the different antennas to the first center IF frequency of 11.4-13.2 GHz. The second I and Q down-conversion converts the IF signal directly to the baseband. The analog baseband signal is amplified and after filtering and further amplification will be converted to a digital signal by two high speed A/D converters in I and Q channels. A fraction of the IF signal goes to a power detector to provide an estimate of the power level to the beamforming algorithm. The algorithm adjusts the phase shifters (and gain of each LNA if required). In the transmit section, both I and Q digital signals are converted to the analog domain by two high speed D/A converters. Harmonics of converted signals and spurious signals are rejected by two low pass filters. The filtered signal is then up-converted to the 12 GHz IF by the first I and Q up-conversion stage. The LO feed-through at the first up-conversion stage can be minimized by calibration techniques implemented in the DSP. After another stage of filtering and amplification, the signal is up-converted to 60 GHz. LO feed-through and generated spurious at the output of the second mixer are filtered out by the band pass filter centered at 60 GHz. The 60 GHz signal is then divided and applied to a number of paths. The signal in each path passes through a phase shifter block. The phase shifted signals are then amplified by power amplifier stages and applied to the transmit antenna array.

4.8 Passive and Active Phase Shifting Front-ends

Figure 4.42 demonstrates two front-end array architectures based on passive and active phase shifter and power combining approaches. In Figure 4.42a, the phase shifter uses passive RTPS topology. All the circuit blocks up to the first down-conversion mixer are single ended circuits. The estimated loss of phase shifter is 10 to 15 dB. The power combining is based on passive power combining networks such as Wilkinson. To compensate for the loss of phase shifter and power combining network, another gain stage is required after the power combiner. Then, the combined signal is converted to a differential signal using an on-chip balun. A double balanced mixer downconverts the signal to the first IF. The second approach shown in Figure 4.42b uses an active phase shifter topology, described in Chapter 4. After the amplification by a single-ended LNA, the single ended signal will be converted to a differential signal through an on-chip balun in each path.

Differential phase shifter architecture described in this chapter is used. Signals from each path are combined through an active power combing network.

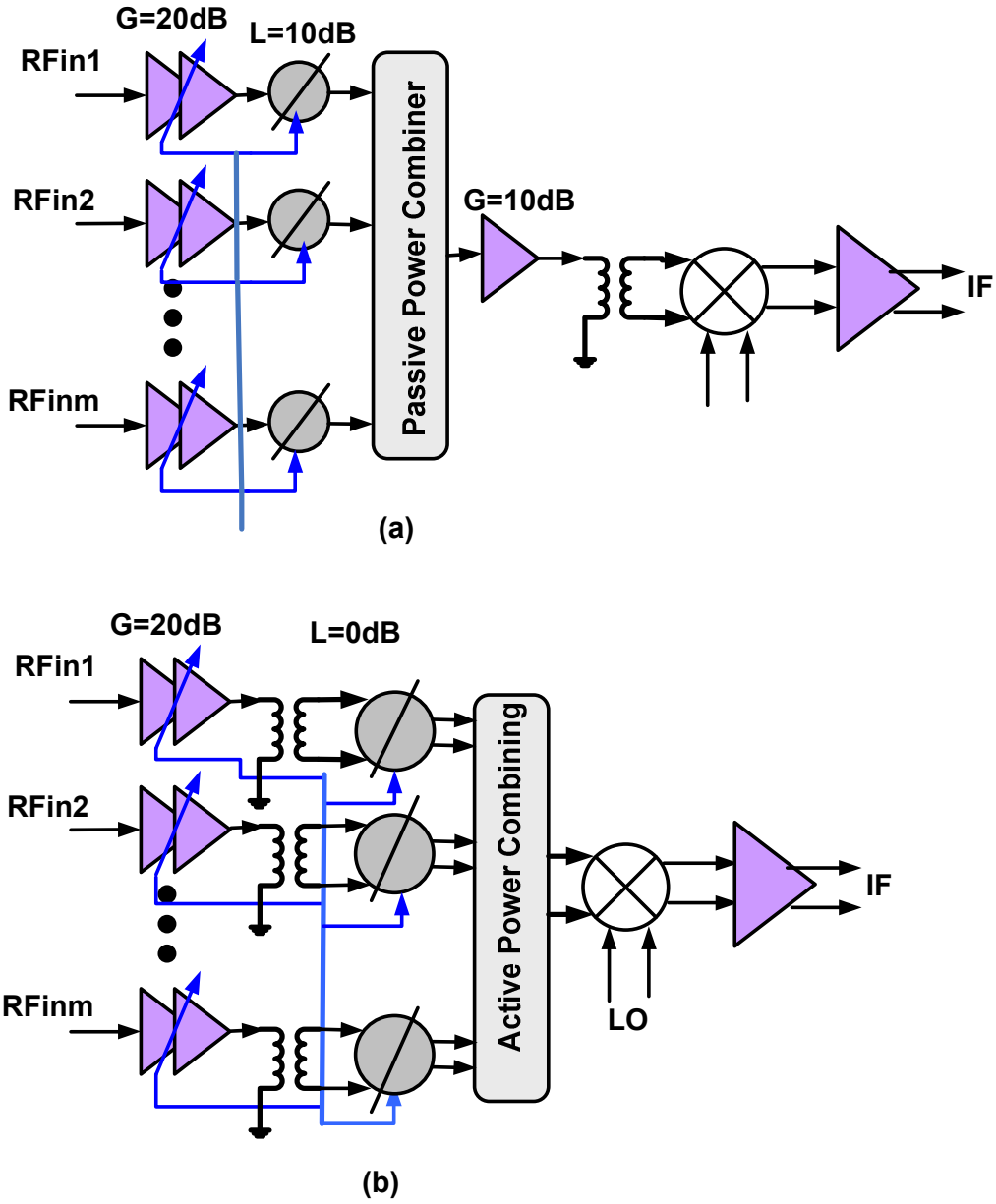
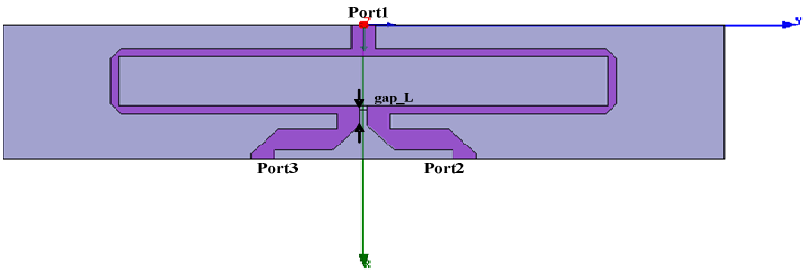


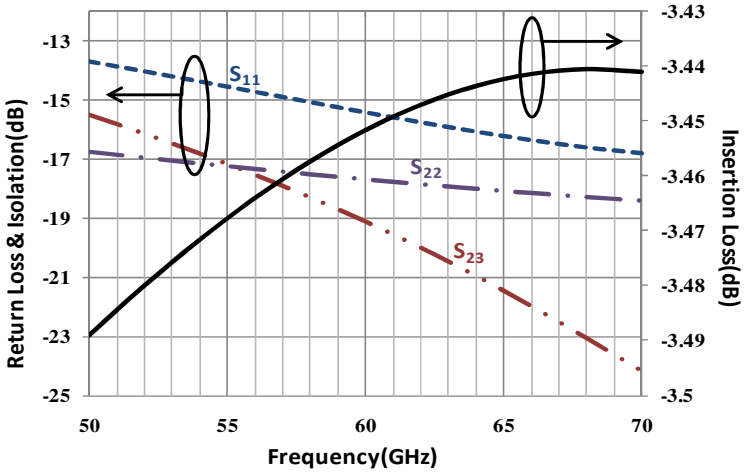
Figure 4.42: RF phase shifting receiver front-end based on (a) passive phase shifting (b) active phase shifting

4.8.1.1 Passive Power Combiner

To combine the two signals coming from the LNAs and phase shifters, a microstrip Wilkinson power divider/combiner implemented in the top metal layer of the technology is designed. The bottom metal layer was used as a ground plane. For realizing the desired 100 Ω resistor between the arms of combiner, a resistive layer with a sheet resistance of 60 Ω/square was used. The quarter-wavelength lines are meandered for reducing the size. The important parameter in the design of such a power combiner for improving the return loss is the optimization of the gap length between two closed arms (the gap width is fixed by the length of on-chip resistor). The power combiner was designed and optimized using the ANSOFT HFSS environment. Figure 4.43 shows the insertion loss and return loss graphs. The maximum insertion loss in the desired bandwidth is 0.45 dB (considering the loss tangent of 0.01 for all dielectric layers).



(a)



(b)

Figure 4.43 (a): Top view of the Wilkinson combiner. (b) Insertion and return loss of Wilkinson combiner/divider.

4.8.1.2 Active power combiner

Figure 4.51a shows an active combiner. In this architecture the voltage is converted to current and the currents are combined into a load. As long as the length of current combining network is smaller than the wavelength, this approach could be a power and area efficient combining technique. The disadvantage of this approach is nonlinearity of voltage to current converter.

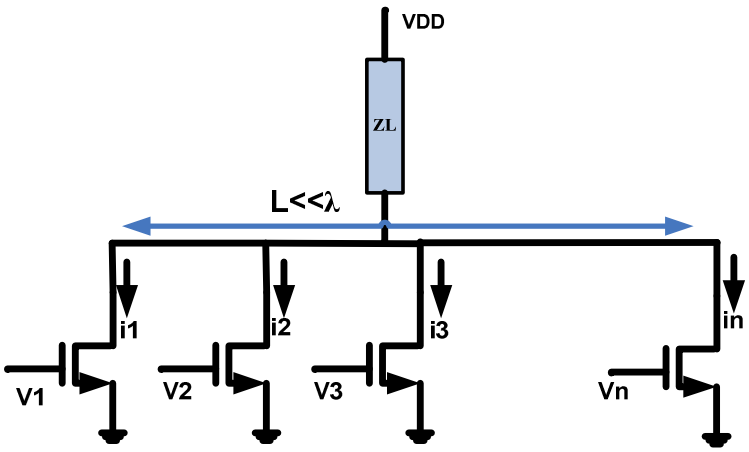


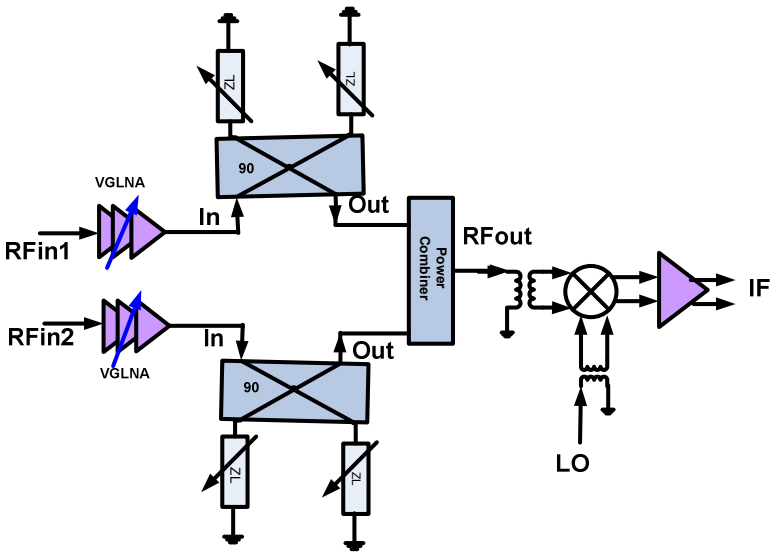
Figure 4.44: Active power combining

4.8.2 RTPS-based Phased Array Front-end

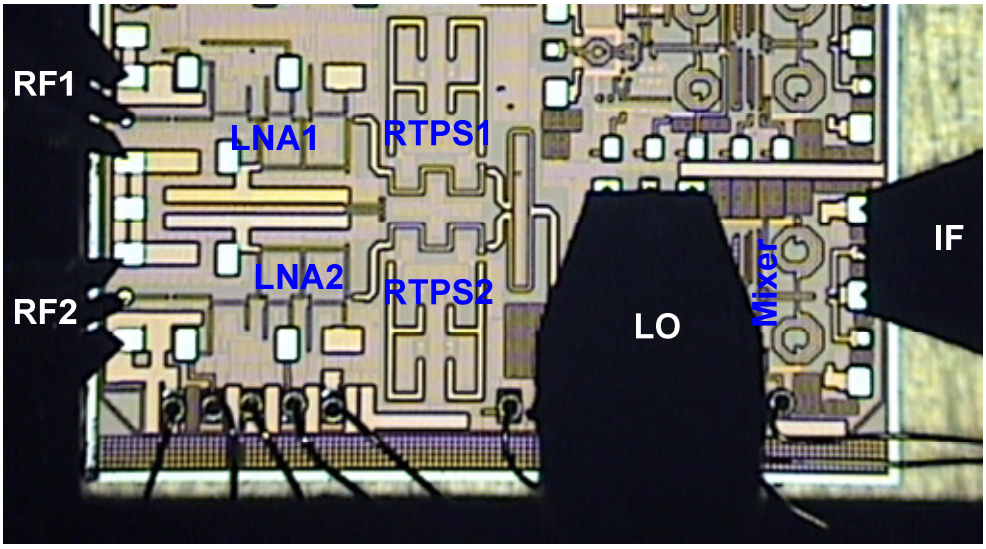
Passive and active continuous phase shifting approaches were discussed in this chapter. Figure 4.45a shows a two element receiver front-end including down-conversion mixer based on RTPS implemented in 0.13 μm CMOS technology. A 3-stage cascode amplifier was used as low noise amplifier block. The LNA block is followed by a RTPS and the outputs of the two paths are combined using a Wilkinson power combiner. The combined signal is converted to a differential signal using a balun. Details of the LNA design and RTPS are explained in sections 4.4 and 4.5. Described power combiner in 4.8.1.1 was used to combine the signals from two paths. The advantages of this approach are linearity, lower power consumption and a wideband front-end. The front-end is easily scalable to

higher number of array elements. In that case, each path is repeated and the 2x1 power combiner will be replaced by an Nx1 power combiner.

The receiver array die under test is shown in Figure 4.45b. Excluding the pads, the two element front end including the mixer occupies 2.2 mm^2 silicon area.



(a)



(b)

Figure 4.45: A two element phased array front-end based on RTPS phase shifter (a) block diagram (b) Die micrograph

4.8.2.1 Measurement Results

Figure 4.46 shows the measurement set up used for the characterization of the two elements array chip. A power splitter used to divide the RF signal between the two inputs. At 60 GHz, the measured phase and amplitude mismatch between the two RF paths applied to the RF probes are 6º and 0.68 dB respectively. The total loss of each cable from the input of signal generator to the input of RF probes is about 20 dB. GGB 110H dual probe with adjustable distance between tips was used to apply the 60 GHz signals to the input pads. The die was attached on printed circuit board. The bias pads were bonded to the printed circuit board. All the required bias levels for the chip were applied through the printed circuit board and wire bonded pads. 48 GHz LO signal was applied to the LO pads through a CPW probe. IF signal was monitored through another CPW probe connected to the spectrum analyzer.

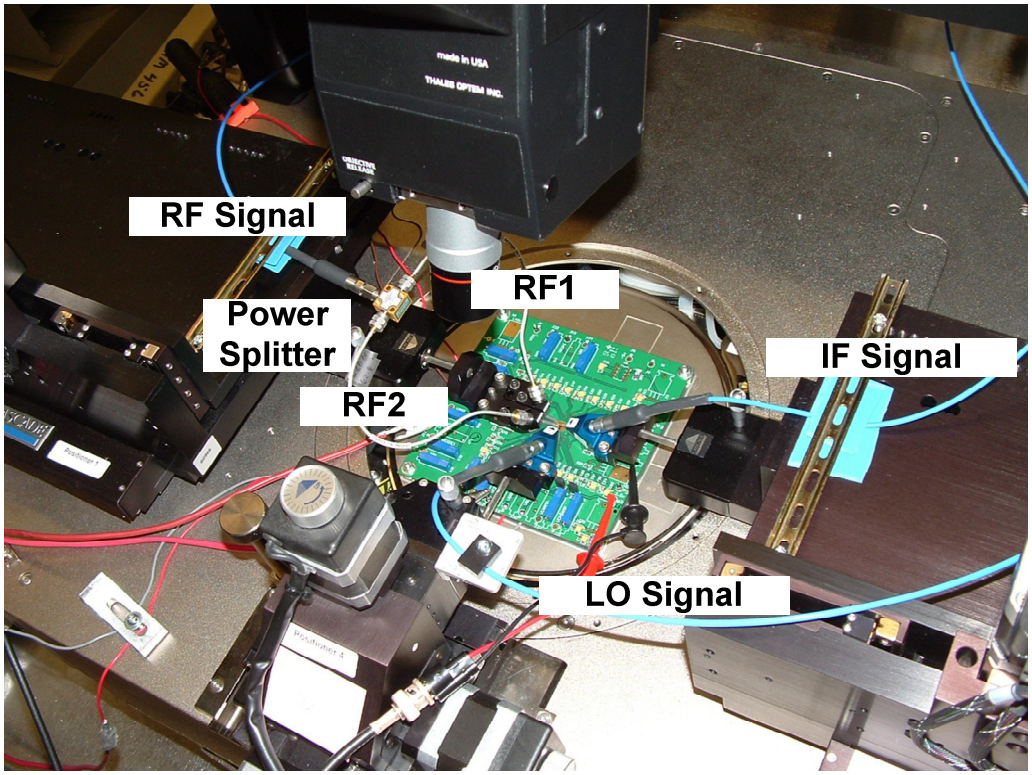


Figure 4.46: Measurement set up at 60 GHz

Figure 4.47 presents the measured combined power at the IF output when two in phase RF signals are connected to the RF inputs. For this measurement, control voltage for one channel was fixed at 0 V and the control voltage for the second channels varied between 0 to 1.5 V. As the voltage control of the channel 2 increases, the power level at IF decreases due

to the added phase shift in one path. Out of phase cancelation of about 15 dB was measured. This number is limited to the amplitude mismatch between the two paths as a result of phase shifter insertion loss variation.

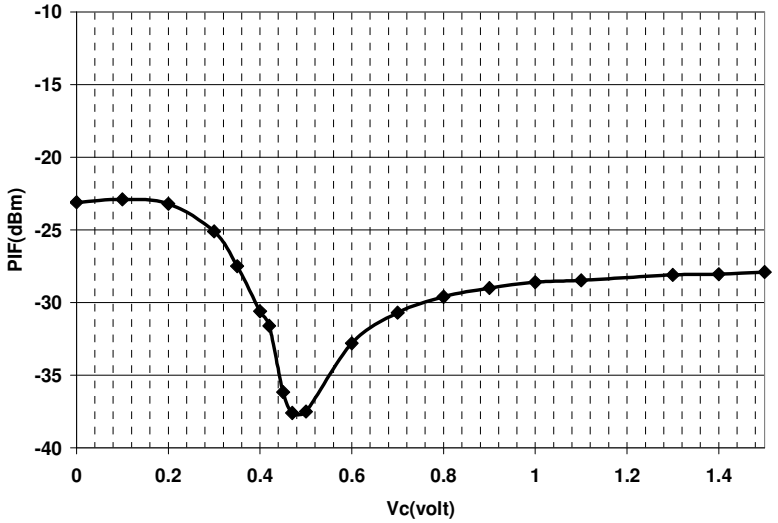


Figure 4.47: Measured IF power versus V_{C2} (F_{RF}=60 GHz F_{LO}=48 GHz, P_{RF1}=P_{RF2}=-30 dBm V_{C1}=0 V_{C2} varies from 0 to 1.5 V)

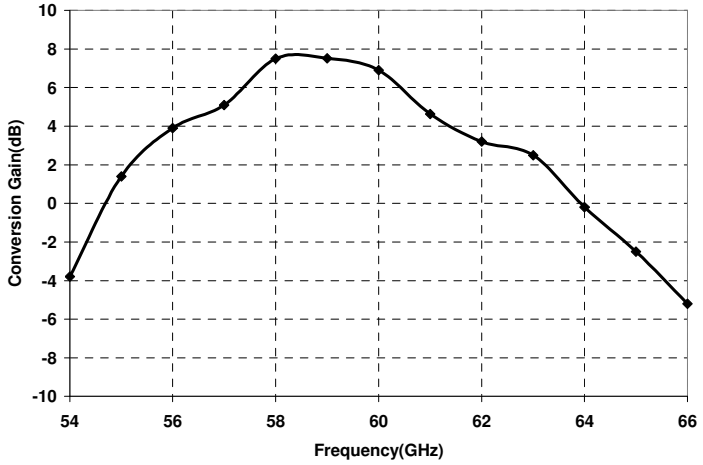


Figure 4.48: Measured maximum receiver conversion gain versus RF frequency (V_{C1}=V_{C2}=0 V)

Figure 4.48 presents the conversion gain versus RF frequency while the IF was fixed at 12 GHz by sweeping the LO and RF simultaneously. RF and LO frequencies were swept

from 54 to 66 GHz and 42 to 54 GHz respectively. This measurement shows a 3 dB bandwidth of 4.5 GHz for the front-end. Channel to channel isolation versus frequency is shown in Figure 4.49. The isolation is better than 45 dB over the frequency range of 55 to 66 GHz. Figure 4.50 illustrate the LO to RF and LO to IF isolation versus frequency. LO to RF isolation is better than 50 dB over the frequency range of 50 to 64 GHz. LO to IF isolation varies between 17 to 13 dB for the LO frequency range of 45 to 50 GHz. This can be easily filtered out since the receiver IF is centered around 12 GHz.

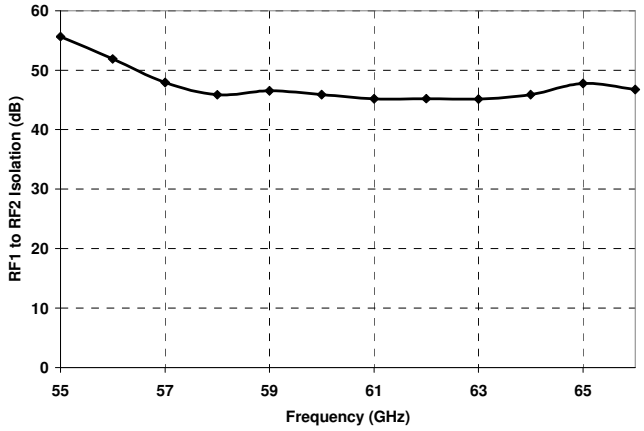


Figure 4.49: Measured On-chip channel to channel isolation

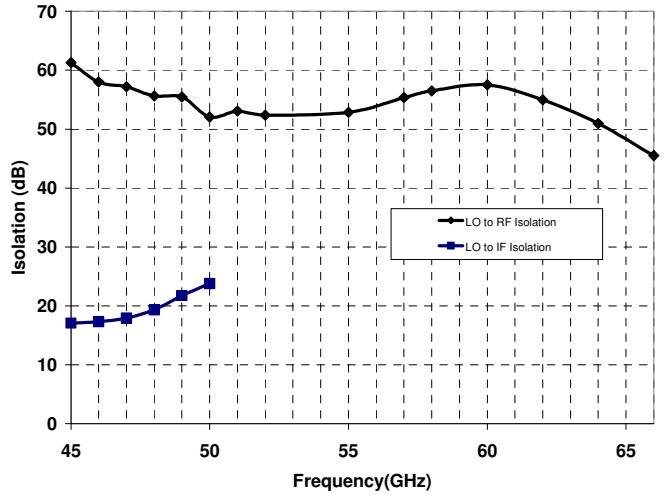


Figure 4.50: Measured LO to RF and LO to IF Isolation versus frequency

4.8.3 Active Phase Shifter Array Front-end

One limitation of the RTPS topology is the amount of phase shift that can be achieved with low Q varactors and lossy passive elements in silicon technology. To increase the beam steering a full range phase shifter is required. Also there should be enough margin in the amount of phase shift to cover the process and temperature variation. To achieve a 360º phase shift, active phase shifters are proposed in 4.5.2.

A two element beamforming front-end using the resonance based phase shifter architecture was shown in Figure 4.51a. In this architecture the LNA is a single ended amplifier. The single ended signal after the LNA is converted to differential signal using an on-chip balun. A single bit 0/180º switch is implemented by swapping the output of two differential amplifiers after the input balun. This block is followed by two 90º continuous phase shifters based on the resonance based phase shifter architecture described in Chapter 44.5.2.1. Figure 4.53 shows the phase variation versus control voltage over the frequency range of 55 to 65 GHz. Voltage gain variation versus control voltage is shown in Figure 4.53.

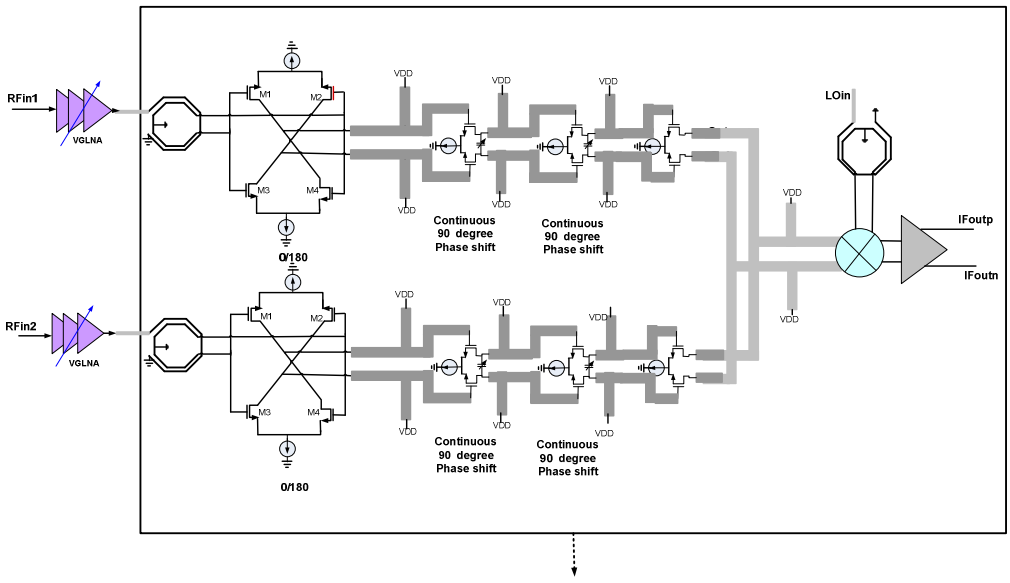


Figure 4.51: Phased array front-end based on active phase shifter Measurement Results

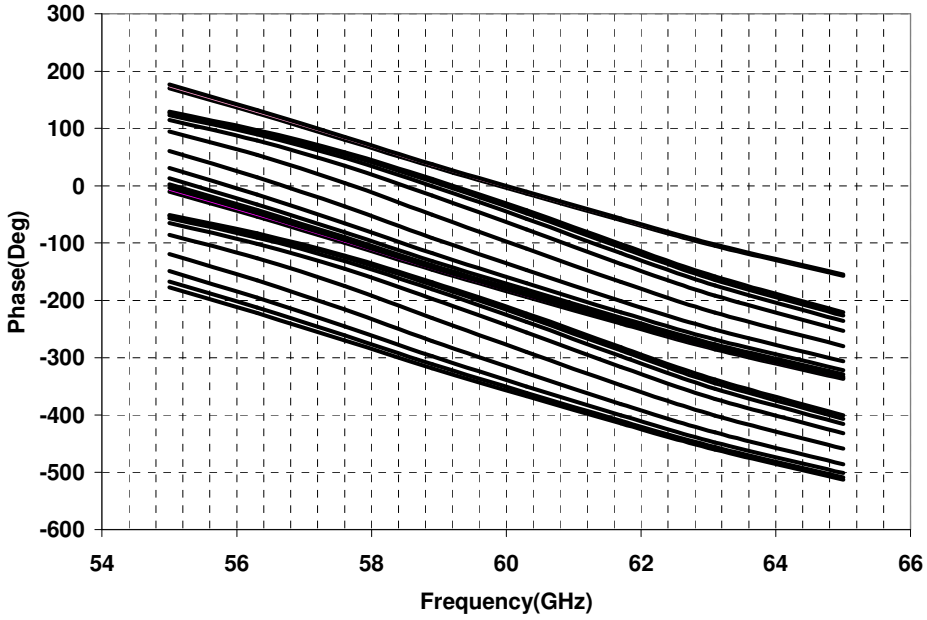


Figure 4.52: Simulated phase change versus control voltage over frequency range of 55 to 65 GHz

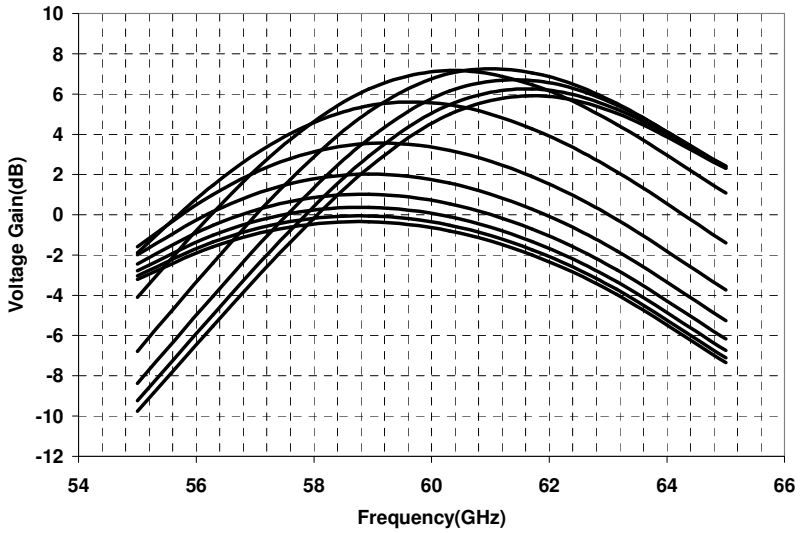


Figure 4.53: Simulated voltage gain variation versus phase shifter control voltage over frequency range of 55 to 65 GHz

Table 4.5 shows the summary of results for the architecture. The active front-end parameters are simulated.

Table 4.5: SUMMARY OF RESULTS

Parameter	Active PS	RTPS	Unit
RF Frequency Band	**57 to 64**	**57 to 64**	**GHz**
Front End BW_{3dB}	**4(Simulated)**	**4.5**	**GHz**
LNA Peak Gain	**19**	**19**	**dB**
NF	**<7 (Simulated)**	**<7 (Simulated)**	**dB**
Channel to channel isolation	**-**	**>45**	**dB**
Max Front-end Gain	**17 (Assuming the designed 3 stage LNA is used before the phase)**	**8**	**dB**
Number of antennas per chip	**Two(Scalable)**	**Two(Scalable)**	
Front-end Current Consumption	**42 (Assuming LNA will be added)**	**21**	**mA/ path**
Phase controller voltage	**0.9-2**	**0 to 1.5**	**V**
Phase shifter (range)	**0-345 (Simulated)**	**0 to 270 (Simulated)**	**°**
Supply Voltage	**1.5**	**1.5**	**V**
Chip area	**0.64**	**1.12**	**mm^2/ path**
Technology	**IBM 0.13µm CMOS**		

4.9 Conclusion

This chapter presented design and development of the key blocks of a phased array front-end. Different amplifier topologies for narrow band and broadband application were studied. A two stage high gain 30 GHz cascode amplifier was developed and integrated with an on-chip dielectric resonator antenna which was presented in chapter 3. Passive and active millimeter-wave phase shifter architectures were presented. Active phase shifter architectures were proposed to achieve 360º phase shift range. Moreover a double balanced mixer was developed to downconvert the RF signal between 57-64 GHz to 11.4-12.8 GHz.

Details of a phased array receiver in terms of architecture and frequency plan were studied and described. Based on passive and active phase shifting techniques, two front-end options were proposed. Two element front-ends were implemented in 0.13 μm CMOS technology. The measurement results for the passive and simulation results for active phase shifting approaches were presented.

Chapter 5 Conclusion, Future Works and Directions

5.1 Contribution and Conclusion

This section presents a summary of the contributions of each chapter of this thesis.

In chapter 2, system aspects of a millimeter-wave phased array radio for operation at 60 GHz were presented. The 60 GHz standards were analyzed and radio front-end specifications were derived. Radio architectures and antenna options for single antenna and phased array antenna transceiver were discussed. Channel measurement at 60 GHz was performed and the effect of human body in 60 GHz channel was investigated. As a part of this research through accurate ray-tracing method, a NLOS scenario was fully simulated. Moreover, it was shown how a phased array radio can significantly improve the SNR under NLOS condition.

In chapter 3, a high efficiency on-chip antenna structure on low resistivity silicon substrate was proposed, fabricated, and measured. Using Wheeler method, a radiation efficiency of 48% was measured. Compared to an on-chip antenna with 5% radiation efficiency, the proposed technique, improves the wireless link performance by at least 10 dB. Moreover, an integrated on-chip DRA-amplifier was implemented in CMOS technology. As compared to the case where DR was absent, about 30 dB improvement in the link was achieved by adding DR on both transmit and receive sides of the link. The proposed structure can be used for single antenna or phased array millimeter-wave transceiver in system in package (SiP) configuration. Furthermore, towards the implementation of low cost, miniaturized and efficient off-chip antenna array, on-chip antennas on a passive high resistivity silicon technology were investigated.

Although the proposed antenna structure was fabricated at 35GHz and 30GHz, the same idea can be implemented at 60GHz by scaling of slot and dielectric resonator dimensions. Simulations in section 3.8 shows the radiation efficiency of about 60% at

60GHz can be achived with the proposed architecture. This is in agreement with our simulations and measurements at 35GHz.
For integration with the transceiver, everything needs to be transferred to 0.13μm CMOS technology or below. This was done in chapter 4 for the amplifier and other active circuits such as amplifier and phase shifter. Integrated antenna uses metal stack of the IC technology and due to the similarity of the BEOL for the different silicon technologies, proposed antenna can be implemented in any silicon technology. The structure can be scaled and optimized for desirable frequency.

In chapter 4, key circuit blocks of a phased array front-end such as variable gain amplifier, passive and active phase shifters were investigated. High gain cascode amplifier in CMOS technology was implemented. To overcome the limited phase shift range of a passive phase shifter due to the low quality varactor and passive components, two active phase shifter architectures which can achieve 360º phase shift, were proposed. Moreover, a double balanced downconversion mixer for the proposed phased array architecture was developed.

Phased array front-end architectures based on passive and active phase shifters were investigated, designed, and compared. A two elements passive phase shifting front-end and a two element active phase shifting front-end integrated with a down conversion mixer were developed in 0.13 μm CMOS technology.

In Summary the major contributions of the author can be listed as follow:

1-Successful demonstration of radiation efficiency improvement from less than 5% to about 50% for a millimeter wave on-chip antennas on lossy silicon using above-IC dielectric resonator technology.
2-Integration and demonstration of the proposed antenna with the active circuit block at 35 GHz.
3-Extensive measurement and characterization of on-chip antennas and millimeter-wave circuit blocks.
4-Radiation efficiency measurement of on-chip millimeter wave antenna.

5- Implementation of efficient high gain antennas in a new passive silicon technology at 60GHz.

6-Implementation of high gain CMOS amplifier at 35GHz and 60GHz
7-Design of full range active phase shifters in CMOS technology

8-Implementation and demonstration of a two element 60GHz phased array front-end in low cost CMOS technology.

5.2 Future Research Directions

Integrated millimeter-wave multi antenna transceiver is an essential part of the future silicon based wireless communication and radar devices. Multi-antenna transceivers are able to address the millimeter-wave band challenges such as high free space propagation and material loss as well as silicon technology limitations such as limited output power due to technology scaling. With the advancement of silicon technologies towards one terahertz f_{max} transistors, millimeter-wave array transceivers will become a hot research and technology development area especially for frequencies above 100 GHz. This will become a highly multi-disciplinary research field which will cover diversified areas such as on-chip and in-package multi antenna research, investigation of silicon millimeter-wave circuits and systems, and research and development of ultra wide band (multi-GHz) signal processing systems. The future research directions are:

- **Miniaturized high efficiency on-chip/in-package antennas**

High efficiency requirement will remain an important demand for on-chip antennas. To reduce the silicon cost, miniaturization of on-chip antennas while keeping the efficiency high is a challenging problem.

Dielectric antenna is a promising and high potential antenna technology for millimeter-wave. The research in this thesis was focused on rectangular dielectric resonator antenna. Investigation of different dielectric resonator shapes, and suitable radiation modes considering the limitations of silicon technologies and chip area could be further investigated as a continuation of this research. Furthermore, effect of package material on the performance of the antenna is an important problem.

- **Integrated in-package antenna array transceiver.**

In 60 GHz band and lower, on-chip antenna array is not a cost-effective solution for phased array transceivers with the high number of elements. As part of this research, different off-chip antenna array designs and concepts have been investigated. Integration of

the array antenna with the transceiver into a single package and investigation of packaging effect on the performance of the antenna array is an ongoing research.

- **Ultra Low power phased array transceivers**

Ultra low power phased array transceivers are required to enable millimeter-wave portable applications. High efficiency antennas, high gain, and low noise amplifiers, efficient power amplifiers, and low power radio architectures are the main elements of an ultra low power transceiver. Migrating this research to 65 nm or 45 nm CMOS technology nodes is a necessary step to lower the power consumption and chip area significantly. Furthermore, the effects of process and temperature variation on the performance of the millimeter-wave circuits need to be investigated and compensated to increase the production yield.

Investigation of the Low power, compact and low loss phase shifters will remain an important research challenge. Low loss and area efficient power combining techniques are required and should be investigated further when large numbers of antenna elements are required.

References

[1] K. Ohata, et al., “Sixty-GHz-band ultra-miniature monolithic T/R modules for multimedia wireless communication systems,” *IEEE Trans. Microwave Theory Tech.*, vol. 44, no. 12, pp. 2354p-2360, Dec 1996.

[2] S. Reynolds, et al., “A silicon 60GHz receiver and transmitter chipset for broadband communications,” *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2820-2830, Dec 2006.

[3] Sten E. Gunnarsson, et. al, “60 GHz single-chip front-end MMICs and systems for multi-Gb/s wireless communication," *IEEE J. Solid-State Circuits*,” vol. 42, no. 5, pp. 1143-1157, May 2007.

[4] E. Laskin, M. Khanpour, S.T. Nicolson, A. Tomkins, P. Garcia, A. Cathelin, D. Belot, and S.P. Voinigescu, “Nanoscale CMOS Transceiver Design in the 90-170 GHz Range, “, *EEE Trans. MTT, Vol.57,* in press , Dec. 2009.

[5] T. Mitomo, et. al, “A 60-GHz CMOS receiver front-end with frequency synthesizer,” *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 1030-1037, April 2008.

[6] C.H. Doan, S. Emami, A.M. Niknejad, and R.W. Brodersen, “Millimeter- wave CMOS design,” *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144-155, Jan. 2005.

[7] A. Babakhani, et al., “A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2795-2806, Dec. 2006.

[8] B. Razavi, “Gadgets gab at 60 GHz," *IEEE Spectrum*, vol. 45, no. 2, pp.46-58, Feb. 2008.

[9] A. Tomkins, et al., “A Zero-IF 60GHz 65nm CMOS Transceiver with Direct BPSK Modulation Demonstrating up to 6Gb/s Data Rates Over a 2m Wireless Link,” *IEEE Journal of Solid State Circuits*, Vol.44, No.8, pp. 2085-2099, August 2009.

[10] Kamerman and L. Monteban, “WaveLAN-II: A high-performance wireless LAN for the unlicensed band,” in *Bell Labs Technical Journal*, Summer 1997, pp. 118-133.

[11] Yukio Takimoto,”Recent Activities on Millimeter-Wave Indoor LAN System Development in Japan,” in *n Proceedings of IEEE Microwave System Conference*, 1995, pp. 7-10.

[12] P. Smulders, “Exploiting the 60 GHz band for local wireless multimedia access: prospects and future directions," *Communications Magazine, IEEE*, vol. 40, no. 1, pp. 140-147, Jan 2002.

[13] C. Park and T. Rappaport, “Short-range wireless communications for next generation networks: UWB, 60 GHz millimeter-wave WPAN, and ZigBee,” I*EEE Wireless Commun.*, vol. 14, no. 4, pp. 70-78, Aug. 2007.

[14] A. Natarajan, A. Komijani, X. Guan, A. Babakhani, and A. Hajimiri, “A 77-ghz phased-array transceiver with on-chip antennas in silicon: transmitter and local lo-path phase shifting," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2807-2819, Dec. 2006.

[15] Gresham, I., et al., "Ultra-wideband radar sensors for short-range vehicular applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol.52, no.9, pp. 2105- 2122, Sept. 2004.

[16] http://www.ieee802.org/15/pub/TG3c.html

[17] http://www.wirelesshd.org/

[18] http://wirelessgigabitalliance.org/

[19] ETSI TR 102 664 V1.1.1 (2009-04) Technical Report.

[20] F. C. C. (FCC), *Millimeter-Wave Propagation: Spectrum Management Implications*. FCC document, 1997.

[21] Tapan K. Sarkar, Robert Mailloux, Arthur A. Oliner, Magdalena Salazar Palma, Dipak L. Sengupta , *History of Wireless*. Wiley-IEEE Press, 2006.

[22] http://www.itrs.net/

[23] Andreia Cathelin and John J. Pekarik, Silicon Technologies to Address mm-Wave Solutions. Springer, 2008.

[24] T. Iida, Satellite Communications: System and Its Design Technology. IOS Press, 2000.

[25] M. I. Skolnik, Radar Handbook. McGraw-Hill, 2008.

[26] B. F. Burke and F. Graham-Smith, An Introduction to Radio Astronomy, 2002.

[27] J. G. Webster, Wiley Encyclopedia of Electrical and Electronics Engineering. Cambridge University Press, 1999.

[28] http://www.dotfive.eu/

[29] B. Razavi, “A 60-GHz CMOS receiver front-end,” *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 17–22, Jan 2006.

[30] J. B. P. W. Karen Scheir, Stephane Bronckers and Y. Rolain, "A 52 GHz phased-array receiver front-end in 90 nm digital cmos," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2651–2659, Dec 2008.

[31] S. R. Alberto Valdes-Garcia and Jean-Oliver Plouchart, "60 GHz transmitter circuits in 65nm CMOS," in *IEEE Radio Frequency Integrated Circuits Symposium*, June 2008, pp. 641–644.

[32] A. P. M. Boers and N. Weste, "A 60GHz transmitter in 0.18*μm* Silicon Germanium," in *Wireless Broadband and Ultra Wideband Communications*, 27-30 Aug. 2007, pp. 36–36.

[33] B. Razavi, "CMOS transceivers for the 60-GHz band," in *IEEE Radio Frequency Integrated Circuits Symp.*, June 2006.

[34] http://www.ecma-international.org/memento/TC48-M.htm

[35] D. Tse, and P. Viswanath, *Fundamentals of Wireless Communication*. Cambridge University Press, 2005.

[36] Behzad Razavi, RF microelectronics, Prentice-Hall, Inc., Upper Saddle River, NJ, 1998.

[37] T. Manabe, Y. Miura, T. Ihara, "Effects of antenna directivity and polarization on indoor multipath propagation characteristics at 60 GHz", IEEE selected areas in communications, 1996, Vol. 14, No. 3, pp.1441–448.

[38] C.-P. Lim, M. Lee, R. J. Burkholder, J. L. Volakis and R. J. Marhefka, "60 GHz indoor propagation studies for wireless communications based on a ray-tracing method," *EURASIP Jour. Wireless Commun. and Net.*, 2007, article ID 73928.

[39] P. Smulders, C. F. Li, H. Yang, E. Martijn and M Herben, "60 GHz indoor radio propagation comparison of simulation and measurement results," in *IEEE 11th Symp. on Commun. and Vehi. Tech.*, 2004.

[40] B. Langen, G. Lober and W. Herzig, "Reflection and transmission behaviour of building materials at 60 GHz," in *IEEE Int. Symp. Personal, Indoor and Mobile Radio Commun.*, 1994, pp. 505–509.

[41] L. M. Correia and Paul O. Frances, "Estimation of materials characteristics from power measurements at 60 GHz," in *IEEE Int. Symp. Personal, Indoor and Mobile Radio Commun.*, 1994, pp. 510–513.

[42] C. M. Alabaster, "Permittivity of human skin in millimetre wave band," *Electron. Letters*, vol. 39, no. 21, pp. 1521–1522, Oct. 2003, article ID 73928.

[43] B. Razavi, “A 60-GHz direct-conversion CMOS receiver,” in *IEEE ISSCC. Proc.*, Feb. 2005, pp. 400–401.

[44] Marcu, C., et al., "A 90nm CMOS low-power 60GHz transceiver with integrated baseband circuitry," *Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International* , vol., no., pp.314-315,315a, 8-12 Feb. 2009.

[45] Zargari, et al., "A single-chip dual-band tri-mode CMOS transceiver for IEEE 802.11a/b/g WLAN," *ISSCC. 2004* , vol., no., pp. 96- 515 Vol.1, 15-19 Feb. 2004.

[46] Parsa, A.; Razavi, B.; , "A New Transceiver Architecture for the 60-GHz Band," *Solid-State Circuits, IEEE Journal of* , vol.44, no.3, pp.751-762, March 2009.

[47] Robert E. Collin, *Antennas and Radiowave Propagation*. McGraw-Hill, 1985.

[48] Robert J. Mailloux, *Phased Array Antenna Handbook- Chapter 1*, 2nd ed. Artech House, 2005.

[49] H. Hashemi, X. Guan, A. Komijani, and A. Hajimiri, “A 24-GHz SiGe phased-array receiver LO phase-shifting approach,” *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 2, pp. 614 – 626, 2005, feb.

[50] S. Raman, N. Barker, and G. Rebeiz, “A W-band dielectric-lens-based integrated monopulse radar receiver,” *IEEE Trans. Microwave Theory Tech.*, vol. 46, no. 12, pp. 2308–2316, Dec. 1998.

[51] R. Miura, T. Tanaka, I. Chiba, A. Horie, and Y. Karasawa, “Beamforming experiment with a DBF multibeam antenna in a mobile satellite environment,” *IEEE Trans. Antennas Propagat.*, vol. 45, no. 4, pp. 707–714, Apr 1997.

[52] M. Fakharzadeh, P. Mousavi, S. Safavi-Naeini, and S.H. Jamali, “The effects of imbalanced phase shifters loss on phased array gain,” *IEEE Antennas Wireless Propagat. Lett.*, vol. 7, pp. 192–196.

[53] T. Zwick, Duixian Liu; and B.P. Gaucher , “Broadband planar superstrate antenna for integrated millimeterwave transceivers”, IEEE Transaction on Antenna and Propagation, 2006, vol. 54, no. 10, pp. 2790 – 2796.

[54] E. Ojefors, H. Kratz, K. Grenier, R. Plana, and A. Rydberg, “Micromachined loop antennas on low resistivity silicon substrates,” *IEEE Trans. Antennas Propagat.*, vol. 54, no. 12, pp. 3593–3601, Dec. 2006.

[55] C. Karnfelt, P. Hallbjorner, H. Zirath, and A. Alping, “High gain active microstrip antenna for 60-GHz WLAN/WPAN applications,” *IEEE Trans.Microwave Theory Tech.*, vol. 54, no. 6-Part 2, pp. 2593 – 2603, June 2006.

[56] A. Lamminen, J. Saily, and A.R. Vimpari, "60-GHz patch antennas and arrays on LTCC with embedded-cavity substrates," *IEEE Trans. Antennas Propagat.*, vol. 56, no. 9, pp. 2865–2874, Sept. 2006.

[57] R.C. Johnson, and H. Jasik, *Antenna Engineering Handbook*. McGraw-Hill, 1961.

[58] J.R. James, and P.S. Hall, *Handbook of Microstrip Antennas*. Institution of Electrical Engineers (IEE), 1989.

[59] R.A. Alhalabi, and G.M. Rebeiz, "High-efficiency angled-dipole antennas for millimeter-wave phased array applications," *IEEE Trans. Antennas Propagat.*, vol. 56, no. 10, pp. 3136–3142, Oct. 2008.

[60] M. Fakharzadeh, S. Safavi-Naeini, S.H. Jamali and P. Mousavi, "Zero-knowledge beamforming of phased array antennas based on simultaneous perturbation gradient approximation ," in *IEEE AP-S Int. Symp. Antennas Propagat.*, Albuquerque, NM, July 2006, pp. 537–540.

[61] P. Mousavi, M. Fakharzadeh, S.H. Jamali, K. Narimani, M. Hossu, H. Bolandhemmat, and S. Safavi-Naeini, "A low-cost ultra low profile phased array system for mobile satellite reception using zero-knowledge beam-forming algorithm," *IEEE Trans. Antennas Propagat.*, vol. 56, no. 12, pp. 3667–3679, Dec. 2008.

[62] M. Fakharzadeh, S.H. Jamali, P. Mousavi, and S. Safavi-Naeini, "Fast beamforming for mobile satellite receiver phased arrays: Theory and experiment," *IEEE Trans. Antennas Propagat.*, vol. 57, no. 6, pp. 1645–1654, June 2009.

[63] H. Bolandhemmat, M. Fakharzadeh, P. Mousavi, S.H. Jamali, G. Rafi, and S. Safavi-Naeini,, "Active stabilization of vehicle-mounted phased-array antennas," *IEEE Trans. Veh. Technol.*, vol. 58, no. 6, pp. 2638–2650, July 2009.

[64] K. Kihong, H. Yoon, and K. K. O, "On-chip wireless interconnection with integrated antennas," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2000, pp. 485–488.

[65] Changhua Cao, Yanping Ding, Xiuge Yang, Jau-Jr Lin, A. Verma, Jenshan Lin, F. Martin, and K. O, "A 24-GHz Transmitter with an On-Chip Antenna in 130-nm CMOS," *VLSI Circuits, 2006. Digest of Technical Papers. 2006 Symposium on*, 2006, pp. 148-149.

[66] K. Kim and K. K. O, "Characteristics of integrated dipole antennas on bulk, SOI, and SOS substrates for wireless communication," in *Proc. IEEE Conf. Interconnect Tech.*, Jun. 1998, pp. 21–23.

[67] R. Li, W. Bomstad, J. Caserta, X. Guo, and O. Kenneth, "Evaluation of integrated antennas for wireless connection between an integrated circuit and an off-chip antenna," in *Proc. IEEE Interconnect Technology Conf.*, Jun. 2003, pp. 120–122.

[68] A. Shamim, L. Roy, N. Fong, and N. Garry Tarr, "24 GHz On-Chip Antennas and Balun on Bulk Si for Air Transmission," *IEEE Trans. Antennas Propag.*, vol. 56, no. 2, Feb. 2008, pp. 303 – 311.

[69] N. Behdad, D. Shi, Wonbin Hong, K. Sarabandi, M.P Flynn, "A 0.3mm^2 Miniaturized X-Band On-Chip Slot Antenna in 0.13μm CMOS", 2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 3-5 June 2007, pp. 441 – 444.

[70] I. K. Itotia and R. F. Drayton, "Aperture coupled patch antenna chip performance on lossy silicon substrates," in *Proc. IEEE Antennas Propag. Symp.*, Jul. 2005, vol. 1B, pp. 377–380.

[71] P.V. Bijumon, Y. Antar, A.P. Freundorfer, and M. Sayer, "Dielectric Resonator Antenna on Silicon Substrate for System On-Chip Applications", *IEEE Trans. Antennas Propag.*, vol. 56, no.11, Nov. 2008, pp.3404 – 3410.

[72] Y. P. Zhang, M. Sun, and L. H. Guo, "On-chip antennas for 60-GHz radios in silicon technology," *IEEE Trans. Electron Devices*, pp. 1–5, Jul. 2005.

[73] Shun-Sheng Hsu; Kuo-Chih Wei; Cheng-Ying Hsu; Huey Ru-Chuang, "A 60-GHz Millimeter-Wave CPW-Fed Yagi Antenna Fabricated by Using 0.18- μm CMOS Technology", *IEEE Electron Device Lett.,* vol. 29, no. 6, June 2008, pp. 625 – 627.

[74] A. Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2795–2806, Dec. 2006.

[75] K. T. Chan *et al.*, "Integrated antennas on Si with over 100 GHz performance, fabricated using an optimized proton implantation process," *IEEE Microw. Wireless Compon. Lett.*, pp. 487–489, Nov. 2003.

[76] T. Yao, L. Tchoketch-Kebir, O. Yuryevich, M. Gordon, and S. Voinigescu, "65GHz Doppler Sensor with On-Chip Antenna in 0.18μm SiGe BiCMOS," *Microwave Symposium Digest, 2006. IEEE MTT-S International*, 2006, pp. 1493-1496.

[77] Chao-Shiun Wang, Juin-Wei Huang, Shon-Hang Wen, Shih-Huang Yeh, and Chorng-Kuang Wang, "A CMOS RF front-end with on-chip antenna for V-band broadband wireless communications," *Solid State Circuits Conference, 2007. ESSCIRC 2007. 33rd European*, 2007, pp. 143-146.

[78] R. van Dijk, A. Neto, J. Akkermans, and J. Mills, "EBG-Based 60 GHz On-Chip Antenna in Passive Silicon," *Microwave Conference, 2008. EuMC 2008. 38th European*, 2008, pp. 682-685.

[79] M. Nezhad Ahamdi and S. Safavi-Naeini, "On-chip antennas for 24, 60, and 77GHz single package transceivers on low resistivity silicon substrate," *2007 IEEE Antennas and Propagation Society International Symposium*, pp. 5059-5062.

[80] S. Gunnarsson, et al., "A 220 GHz Single-Chip Receiver MMIC With Integrated Antenna," *IEEE Microwave and Wireless Components Lett.*, vol. 18, 2008, pp. 284-286.

[81] E. Öjefors , F. Bouchriha , K. Grenier and A. Rydberg "24 GHz ISM-band antennas on surface micromachined substrates for integration with a commercial SiGe process," *Proc. Eur. Conf. Wireless Technology* Munich, Germany, 2003.

[82] E. Ojefors, H. Kratz, K. Grenier, R. Plana, A. Rydberg, "Micromachined Loop Antennas on Low Resistivity Silicon Substrates," *IEEE Trans. Antennas Propag.*, vol.54, no.12, pp.3593-3601, Dec. 2006.

[83] H.A. Wheeler, "The Radiansphere around a Small Antenna" Proc. IRE, vol. 47, No. 8, Aug. 1959, pp. 1325 – 1331.

[84] E. Newman, P. bohly, C. Walter, "Two Methods for the measurement of antenna efficiency," *IEEE Trans. Antennas Propag.,* vol 23, no 4, Apr. 1975, pp. 457-461.

[85] G. S. Smith, " An analysis of the Wheeler method for measuring the radiating efficiency of antennas," *IEEE Trans. Antennas Propag.,* vol 25, no 7, July 1977, pp. 552-556.

[86] K.M. Luk, K. W. Leung, Dielectric Resonator Antennas, Research Studies Press, June 2002.

[87] E. Semouchkina, G. Semouchkin, Raj Mittra, and Wenwu Cao, "Finite-Difference Time-Domain Simulation of Resonant Modes of Rectangular Dielectric Resonators ", MICROWAVE AND OPTICAL TECHNOLOGY LETTERS Vol. 36, No. 3, February 5 2003.

[88] B.G. Porter, S.S. Gearhart, "Impedance and Polarization Characteristics of H and IHI Slot Antennas" *IEEE Trans. Antennas Propag.*, vol 48, no. 8, Aug. 2000, pp. 1272-1274.

[89] R.K. Mongia and A. Ittipiboon, "Theoretical and experimental investigations on rectangular dielectric resonator antennas", *IEEE Trans. Antennas Propag.* vol. 45, no.9, pp.1348 –1356, Sept. 1997.

[90] Dielectric substrates data sheet, http://www.magneticsgroup.com/pdf/p30-31%20Dielect2.pdf

[91] R.C. Hansen, *Electrically small, super-directive, and superconducting antennas*, John Wiley & Sons, Inc., Hoboken, New Jersey, 2006.

[92] C.A. Balanis, *Antenna theory: analysis and design*, John Wiley & Sons, Inc., Hoboken, New Jersey, 3rd edition, 2005.

[93] A.D. Yaghjian, S.R. Best, "Impedance, bandwidth, and Q of antennas," *IEEE Trans. Antennas Propag.*, vol 53, no. 4, Apr. 2005, pp. 1298 - 1324.

[94] K. Payandehjoo, R. Abhari, "Characterization of on-chip antennas for millimeter-wave applications" 2009 Int. Symp. Antennas Propag., 1-5 June 2009.

[95] A. Buerkle, K. Sarabandi, H. Mosallaei, "Compact slot and dielectric resonator antenna with dual-resonance, broadband characteristics," *IEEE Trans. Antennas Propag.*, vol 53, no 3, March 2005, pp. 1020-1027.

[96] M. Kahrizi, et. al "Analysis of a wide radiating slot in the ground plane of a microstrip line," *IEEE Trans. on Microwave Theory and Techniques,* vol. 41, 1993, pp. 29-37.

[97] B. Das and K. Joshi, "Impedance of a radiating slot in the ground plane of a microstrip line," *IEEE Trans. on Antennas and Propagation,*, vol. 30, pp. 922-926, 1982.

[98] T. Yao, M.Q. Gordon, K.K.W. Tang, K.H.K. Yau, M-T Yang, P. Schvan, and S. P. Voinigescu, "Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio," *IEEE Journal of Solid State Circuits*. Vol.42, No.5, pp.1044-1057, May. 2007.

[99] B. Heydari, P. Reynaert, E. Adabi,M. Bohsali, B. Afshar, M.A. Arbabian and A.M. Niknejad, "A 60-GHz 90-nm CMOS cascode amplifier with inter-stage matching," IEEE J.SOLID-STATE CIRCUITS, vol. 42, no. 12, pp. 2893–2904, Dec. 2007.

[100] K. Yu, Y. Lu, D. Chang, V. Liang and M. Frank Chang; "K-Band Low-Noise Amplifiers Using 0.18 μm CMOS Technology", IEEE Microwave and Component Letters, vol. 14, No. 3., March 2004, pp. 106-108.

[101] X. Guan and A. Hajimiri; "A 24-GHz CMOS Front-End", IEEE Journal of Solid State circuits, Vol. 39, No.2, February 2004, pp. 368-373.

[102] S. Shin, M. Tsai, R. Liu, K. Lin and H. Wang; "A 24-GHz 3.9-dB NF Low-Noise Amplifier Using 0.18 μm CMOS Technology", IEEE Microwave and Component Letters, vol. 15, No. 7., July 2005, pp. 448-450.D.Pienkowski,G. Boeck, "22 GHz Amplifier using a 0.12 μm CMOS Technology", International Conference on Microwaves, Radar & Wireless Communications, MIKON 2006.

[103] S.P. Voinigescu, T.O. Dickson, M. Gordon, C. Lee, T. Yao, A. Mangan, K. Tang, and K. Yau, "RF and Millimeter-Wave IC Design in the Nano-(Bi)CMOS Era," in *Si- based Semiconductor Components for Radio-Frequency Integrated Circuits (RF IC),* pp.33-62, Editor: Will Z. Cai, Transworld Research Network, 2006 ISBN:81-7895-196-7

[104] Gi-Hyon Ryu, Dae-Hyun Kim, Jae-Hak Lee, and Kwang- Seok Seo, "A Novel 3-dB Coupler for MMIC Using Air-Gap Stacked Microstrip Lines", *IEEE Microwave and Guided Wave Letters*, vol. 10, no.1, January 2000, pp. 1-3.

[105] Tacar Gokdemir, I.D. Robertson, Q.H. Wang, and A.A.Rezazadah, "K/Ka band Coplanar Waveguide Directional Couplers Using Three-Metal-Level MMIC process", *IEEE Microwave and Guided Wave Letters*, vol. 6, no.2, February 1996, pp. 76-78.

[106] F. Ellinger, et al., "Ultracompact reflective-type phase shifter MMIC at C-band with 360° phase-control range for smart antenna combining," IEEE J Solid-State Circuits, vol. 37, pp. 481-486, April 2002.

[107] J. Lange, "Interdigitated stripline quadrature hybrid," IEEE Trans. Microwave Theory and Techniques, vol.. MTT-17, pp. 1150-1151, Dec. 1969.

[108] R.C. Frye, et al., "A 2-GHz quadrature hybrid implemented in CMOS technology," IEEE J Solid-State Circuits, vol. 38, pp. 550-555, March 2003.

[109] Ozis, D.; Paramesh, J.; Allstot, D.J.; , "Analysis and design of lumped-element quadrature couplers with lossy passive elements," *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on* , vol., no., pp.4 pp.-2320.

[110] Hiroshi Okazaki and Tetsuo Hirota, “Multilayer mmic broad-side coupler with a symmetric structure," *IEEE Microwave and Guided Wave Letters*, vol. 7, no. 6, pp. 145{146, Jun. 1997.

[111] S. Alalusi and R. Brodersen, “A 60GHz Phased Array in CMOS," in Proc. of the 2006 IEEE Custom Integrated Circuits Conf., Sep. 2006, pp. 393-396.

[112] Byung-Wook Min, and Gabriel M. Rebeiz, “Ka-Band BiCMOS 4-Bit Phase Shifter with Integrated LNA for Phased Array T/R Modules," in *IEEE MTT-S Int. Microwave Symp.*, June 2007, pp. 479-482.

[113] G. M. R. T. M. Hancock, “A 12-GHz SiGe phase shifter with integrated LNA," *IEEE Trans. Microwave Theory Tech.*, vol. 53- part1, no. 3, pp. 977-983, Mar. 2005.

[114] Pei-Si Wu; Hong-Yeh Chang,; Ming-Fong Lei,; Bo-Jr Huang,; Huei Wang,; Cheng-Ming Yu,; Chern, J.G.J., “A 40-74 GHz amplitude/phase control MMIC using 90-nm CMOS technology," in *European Microwave Integrated Circuits Conference*, Munich, Germany, Oct 2007, pp. 115-118.

[115] H. Zarei and D. J. Allstot, \A low-loss phase shifter in 180 nm CMOS for multiple-antenna receivers," in *IEEE Int. Solid-State Circuits Conference*, Feb 2004, pp. 382-534.

[116] X. Guan, H. Hashemi, and A. Hajimiri, “A fully integrated 24-ghz eight- element phased-array receiver in silicon," IEEE Solid State Circuits, vol. 39, no. 12, pp. 2311-2320, Dec. 2004.

[117] R. V. Garver, “Broad-band diode phase shifters," *IEEE Trans. Microwave Theory Tech.*, vol. 20, no. 5, pp. 314-323, May 1972.

[118] J. D. C. M. M. M. Morton, J. P. Comeau and J. Papapolymerou, “ Sources of Phase Error and Design Considerations for Silicon-Based Monolithic High-Pass/Low-Pass Microwave Phase Shifters," IEEE Trans. Microwave Theory Tech., vol. 54, no. 12, pp. 4032-4040, Dec. 2006.

[119] Kwang-Jin Koh and Gabriel M. Rebeiz, “An X- and Ku-Band 8-Element Linear Phased Array Receiver," in Proceedings of the 2007 IEEE Custom Integrated Circuits Conference, Sep. 2007, pp. 761-764.

[120] A. Natarajan, A. Komijani, and A. Hajimiri, “A fully integrated 24-ghz phased-array transmitter in cmos," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2502{2514, Dec. 2005.

[121] J. Buckwalter, A. Babakhani, A. Komijani, and A. Hajimiri, “An integrated subharmonic coupled-oscillator scheme for a 60-ghz phased-array transmit-ter," *IEEE Trans. Microwave Theory Tech.*, vol. 54, no. 12, part2, pp. 4271-4280, Dec. 2006.

[122] B. Biglarbegian, M. R. Nezhad-Ahmadi, M. Fakharzadeh, and S. Safavi-Naeini, “Millimeter-wave reflective-type phase shifter in CMOS technology,”*Accepted for IEEE Microwave and Wireless Components Letters*, 2009.

[123] C.S. Lin, S.F. Chang, C.C. Chang, and Y.H. Shu, “Design of a reflection-type phase shifter with wide relative phase shift and constant insertion loss,”*IEEE Trans. Microwave Theory Tech.*, vol. 55, no. 9, pp. 1862–1868, Sept. 2007.

[124] Kwang-Jin Koh, G.M. Rebeiz, “0.13-µm CMOS Phase Shifters for X-, Ku-, and K-Band Phased Arrays”, *IEEE J.Solid-State Cir* , vol. 42, no 4, pp. 2535-2546, Nov 2007.

[125] Yikun Yu; P. Baltus, A. van Roermund, D. Jeurissen, A. de Graauw, E. van der Heijden, R. Pijper, “A 60GHz digitally controlled phase shifter in CMOS,” *34th European Solid-State Circuits Conference, (ESSCIRC 2008)*, pp250-253 .

[126] Pei-Si Wu, *et al.*, "A 40-74 GHz amplitude/ phase control MMIC using 90-nm CMOS technology," *European Microwave integrated circuit conference*, 2007. 8-10 Oct., pp 115 – 118.

[127] D. Viveiros, Jr., et al., "A tunable all-pass MMIC active phase shifter," *IEEE Trans. on Microwave Theory and Techniques*, vol. 50, pp. 1885-1889, Aug. 2002.

[128] Zarei, H.; Ecker, A.; Jinho Park; Allstot, D.J.; , "A full-range all-pass variable phase shifter for multiple antenna receivers," *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, vol., no., pp. 2100- 2103 Vol. 3, 23-26 May 2005.

[129] S.Emami, C.H.Doan, A.M.Niknejad, and R.W.Brodersen, "A 60-GHz down-converting CMOS single-gate mixer," *IEEE Radio Frequency integrated Circuits (RFIC) Symposium*, pp. 163 – 166, June 2005.

[130] M. Fakharzadeh, M.R. Nezhad-Ahmadi, B. Biglarbegian, J. Ahmadi-Shokouh, and S. Safavi-Naeini, "*CMOS Phased Array Transceiver Technology for 60 GHz Wireless Applications* ", To be appeared in Antennas and Propagation, IEEE Transactions on , , no.99, 2010.

[131] M. Fakharzadeh, “Optical and Microwave beamforming for phased array antennas,” Ph.D. dissertation, Univ. Waterloo, Waterloo, ON, Canada, 2008.

[132] Mehta, N.P.; Shastry, P.N.; , "Design guidelines for a novel bandpass distributed amplifier," *Microwave Conference, 2005 European* , vol.1, no., pp. 4 pp., 4-6 Oct. 2005.

[133] Arbabian, A.; Niknejad, A.M.; , "Design of a CMOS Tapered Cascaded Multistage Distributed Amplifier," *Microwave Theory and Techniques, IEEE Transactions on* , vol.57, no.4, pp.938-947, April 2009.

[134] Thijs, S.; Linten, D.; Pavageau, C.; Scholz, M.; Groeseneken, G.; , "Center balanced distributed ESD protection for 1–110 GHz distributed amplifier in 45 nm CMOS technology," *EOS/ESD Symposium, 2009 31st* , vol., no., pp.1-6, Aug. 30 2009-Sept. 4 2009.

[135] G. Gonzalez. Microwave Transistor Amplifier Analysis and Design, Prentice Hall 1996.

[136] S. Pinel, et al., “60GHz Single-Chip CMOS Digital Radios and Phased Array Solutions for Gaming and Connectivity”, *IEEE J. Selected areas Commun.*, vol 27, no. 8, Oct 2009, pp 1347-1357.

[137] S. Kishimoto, et al., “A 60-GHz Band CMOS Phased Array Transmitter utilizing Compact Baseband Phase Shifters”, *2009 IEEE Radio Frequency Integrated Circuits Symposium*, pp 215–218.

[138] E. Cohen, C. Jakobson, S. Ravid, and D. Ritter, A bidirectional TX/RX four element phased-array at 60GHz with RF-IF conversion block in 90nm CMOS process, *2009 IEEE Radio Frequency Integrated Circuits Symposium*, pp 207–210.

[139] Y. Yu, et al., A 60GHz Digitally Controlled RF-Beamforming Receiver Front-end in 65nm CMOS, *2009 IEEE Radio Frequency Integrated Circuits Symposium*, pp 211–214.

[140] [6] Chao-Shiun Wang, et al. “A 60-GHz Phased Array Receiver Front-End in 0.13-μm CMOS Technology,” *IEEE* Trans. Circuits Sys., Vol. 56, NO. 10, Oct. 2009, pp 2341–2352.

Appendix A:
Beamforming Algorithms for MMW Receiver Phased Array[130]

The goal of the beamforming algorithm is to increase the array factor and consequently provide the required *SNR* determined by Bit Error Rate (BER) constrains. The ideal limit of the array factor is equal to the number of array elements; however, as it will be shown, the practical array factor is smaller than that due to the variable insertion loss of phase shifter.

1) Signal Model: Let $X(t) = [X_1(t)\ X_2(t)\ \ldots\ X_N(t)]$ denote the received signals by all elements of the array. Then it consists of three parts: source signal $X_S(t)$, interference $X_I(t)$, and background noise $n(t)$,

$$X(t) = X_S(t) + X_I(t) + n(t) \qquad \text{(A-1)}$$

The background noise is assumed to be spatially white. Assume the source (transmitter) is located at direction $r = (\theta_T, \Phi_T)$ in the receiver array coordinate system, transmitting RF signals at frequency $f0$. The RF signal received by an element of the array located at (x_n, y_n, z_n) is given by

$$x_{ns}(t) = s_0(t)G_e(r)\ x \exp\left[jk_0(x_n \sin\theta_T \cos\Phi_T + y_n \sin\theta_T \sin\Phi_T + z_n \cos\theta_T)\right] \qquad \text{(A-2)}$$

where k_0, and $s_0(t)$ are respectively the RF wave number and the source waveform. The path loss is included in $s_0(t)$. The array output for a RF phase shifting architecture array (Figure 4(a)) is

$$y(t) = w^H X(t) \qquad \text{(A-3)}$$

where w is the array weights vector and *H* denotes the Hermitian operator. If analog phase shifters, such as the one will be described in chapter 5, were used to adjust the array weights for beamforming the weight vector would be

$$w(v_1, v_2, \cdots v_N) = [f(v_1)e^{j\psi(v_1)} f(v_2)e^{j\psi(v_{21})} \cdots f(v_N)e^{j\psi(v_{N1})}] \qquad \text{(A-4)}$$

where v_i is the control voltage of the i^{th} phase shifter, and f and Ψ *de*note the amplitude (insertion loss) and phase-shift functions of the phase shifter. The total received power by the array is then

$$P(t) = y^H y \qquad \text{(A-5)}$$

2) Statement of the Problem: In the absence of co-channel interference, beamforming for a MMW receiver array is a constrained optimization problem with the objective of maximizing the total received power by the array. The voltage dependent characteristics of the phase shifters form the constrains of the problem. Hence, the beamforming problem can be stated as:

$$\text{Maximize } P(w_1, w_2, \cdots, w_N) \qquad \text{(A-6)}$$

$$\text{Subject to: } w_i = f(v_i)e^{j\Psi(v_i)} \text{ for each phase shifter}$$

$$v_{\min} \le v_i \le v_{\max} \quad \textit{for each phase shifter}$$

An efficient method to solve this problem is to use gradient estimation methods such as zero-knowledge beamforming algorithm [60][62]. In this case the control voltages are updated in an iterative manner,

$$v(n+1) = v(n) + 2\mu \nabla v P(n) \qquad \text{(A-7)}$$

where μ is an internal algorithm parameter called the *step size*, and $\nabla v P(n)$ is the gradient of power with respect to v. Since the exact calculation of the gradient is not practical it is replaced by an estimated vector:

$$\nabla v P(n) \cong [\hat{g}_1(n)\hat{g}_2(n)\cdots\hat{g}_N(n)] \qquad \text{(A-8)}$$

where each component $\hat{g}_k(n)$ is the approximate partial derivative of $P(n)$ w.r.t. $vk(n)$.

3) Reverse-Channel Aided Beamforming: The size and cost constrains of the receiver do not allow for incorporating a complex processor in the portable node. However, the access point

(fixed node) can handle more elaborate signal processing tasks. Moreover, in MMW networking standards such as WPAN, 50 MHz of the spectrum is reserved for the reverse channel to carry the control signals between the access points and mobile nodes. Access point can be equipped with direction-of arrival

(DOA) estimation unit. This unit calculates the relative position of the mobile nodes and sends this information to them. Each mobile node can use this information to adjust its beam. This method of beamforming is referred to as *Aided Beamforming*.

Although this method is very fast, in the case of shadowing it is not efficient. In this case the beamformer must be able to maintain the array beam on the direction of the strongest component of the multipath signal.

Appendix B:

A rectangular DR has three independent dimensions. The modes of a DR can, therefore, be TE to any of three dimensions. Referring to the DRA and coordinate system shown in Figure 1a, the modes with lowest order indexes are TE^{x}_{111}, TE^{y}_{111}, and TE^{z}_{111}. For the TE^{z}_{111} and TE^{x}_{111} modes of an isolated rectangular DRA, as shown in Figure 1a, the plane y=0 acts as an electric wall. For these modes, the rectangular DRA of height b/2 placed on a ground plane, is equivalent to an isolated DRA of height b. The resonant frequencies and radiation Q factors of TE^{z}_{111} and TE^{x}_{111} of the structure shown in Figure 1a are, therefore, the same as those of the corresponding modes of an isolated DRA.

For a rectangular DRA with dimensions *a, b* > *d*, the lowest order mode will be $TE^{z}_{11\delta}$. Using the dielectric wave guide model, this leads to the simplest approximate representations for the fields within the DRA [89] :

$$H_x = \frac{(k_x k_z)}{j\omega\mu_0} A \sin(k_x x)\cos(k_y y)\sin(k_z z) \qquad \text{(A-9)}$$

$$H_y = \frac{(k_y k_z)}{j\omega\mu_0} A \cos(k_x x)\sin(k_y y)\sin(k_z z) \qquad \text{(A-10)}$$

$$H_x = \frac{(k_x^2 + k_y^2)}{j\omega\mu_0} A \cos(k_x x)\cos(k_y y)\cos(k_z z) \qquad \text{(A-11)}$$

$$E_x = A k_y \cos(k_x x)\sin(k_y y)\cos(k_z z) \qquad \text{(A-12)}$$

$$E_y = -A k_x \sin(k_x x)\cos(k_y y)\cos(k_z z) \qquad \text{(A-13)}$$

$$E_z = 0 \qquad \text{(A-14)}$$

where A is an arbitrary constant and k_x, k_y, and k_z denote the wave-numbers along the x, y, and z directions, respectively, inside the DR. Simplest type of approximate boundary conditions for a high dielectric constant DR is based on the perfect magnetic conductor

(PMC) wall model for some of the DR boundary surfaces and dielectric waveguide model for other boundary surfaces. Enforcing the magnetic wall boundary condition $\vec{E}\cdot\hat{n}=0$ at the surfaces of the resonator, i.e., at |x|=a/2 and |y|=a/2, the following equations are obtained for the wave-numbers k_x, and k_y:

$$k_x=\frac{\pi}{a};\quad k_y=\frac{\pi}{b}. \tag{A-15}$$

Further, by using the dielectric waveguide model [86], the following transcendental equation is obtained for the wave-number k_z:

$$k_z\tan(k_z d/2)=\sqrt{(\varepsilon_r-1)k_0^2-k_z^2}. \tag{A-16}$$

The wave-numbers k_x, k_y, and k_z also satisfy the separation or dispersion equation:

$$k_x^2+k_y^2+k_z^2=\varepsilon_r k_0^2 \tag{A-17}$$

where k_0 denotes the free-space wave-number corresponding to the resonant frequency.

Therefore, the resonance frequency of the DRA can be determined by:

$$\begin{aligned}
&f_0=\frac{c}{2\pi\sqrt{\varepsilon_r}}\sqrt{k_x^2+k_y^2+k_z^2}\\
&k_x=\frac{\pi}{a}\\
&k_y=\frac{\pi}{b}\\
&\frac{k_z}{\tan^{-1}\left(\frac{k_{z0}}{k_z}\right)}=\frac{2}{d}\\
&k_{z0}=\sqrt{k_x^2+k_y^2}.
\end{aligned} \tag{A-18}$$

In the case of high permittivity DR antenna, it has been shown in [86] that the resonance frequency can be estimated using the approximate analytical expression for the resonance frequency of the TE_{111} mode in a rectangular resonator with PMC (Perfect Magnetic Conductor) walls given by:

$$f_0 = \frac{c}{2\pi\sqrt{\varepsilon_r}}\sqrt{\left(\frac{\pi}{a}\right)^2 + \left(\frac{\pi}{b}\right)^2 + \left(\frac{\pi}{d}\right)^2}. \qquad \text{(A-19)}$$

For low profile DR where $a, b > d$ and the above equation further simplifies to

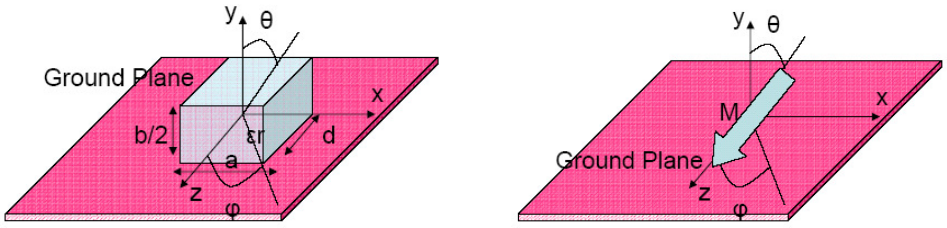
$$f_0 = \frac{c}{2d\sqrt{\varepsilon_r}}, \quad \text{(A-20)}$$

Which indicates that the resonance frequency is almost independent of the DR lateral dimensions.

Radiation Model

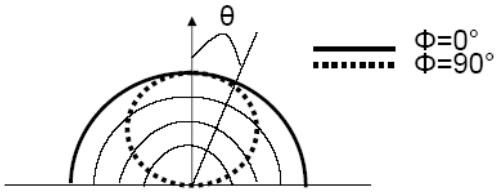
The field distribution of the lowest order mode of the rectangular DRA, determined by the dielectric waveguide model equations, is similar to that of a short magnetic dipole [86]. The radiation pattern generated by the DRA can therefore be approximated using the short magnetic dipole.

Figure 3-7 depicts the equivalent model for a rectangular DRA mounted on infinite ground plane and excited in the $TE^{z}_{11\delta}$ mode. This corresponds to a horizontal magnetic dipole aligned along the z-axis. A good approximation for resulting radiation patterns can be obtained assuming that the DRA is mounted on an infinite ground plane. For practical applications, DRAs are mounted on finite ground planes, which will have an effect on the radiation patterns due to diffraction from the edges.



(a) (b)

(c)



(c)

Figure 1: (a) Physical DRA (b) Equivalent model of $TE^{z}_{11\delta}$ mode (c) Radiation pattern [86]