Multi-mode Pixel Architectures for Large Area Real-Time X-ray Imaging

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

The goal of this work is to extend the state-of-the-art in digital medical X-ray imaging as it pertains to real-time, low-noise imaging and multi-mode imager functionality. One focus of this research in digital flat-panel imagers is to increase the detective quantum efficiency, particularly at low X-ray exposures, in order to enable low-noise imaging applications such as fluoroscopy or tomographic mammography. Another focus of this research is in the creation of a multi-mode imager, such as a combined radiographic and fluoroscopic (R&F) imager, which will reduce hospital costs, both in terms of equipment acquisition and storage space.

To that end, we propose a novel three-transistor multi-mode digital flat-panel imager with a dynamic range capable for use in R&F applications, with a particular focus on noise optimization for low-noise real-time digital flat-panel X-ray fluoroscopy. This work involves the derivation and optimization of the total input referred noise of an active pixel sensor (APS) in terms of the on-pixel thin-film transistor device dimensions. It is determined that in order to minimize noise, all non-transistor capacitances at the pixel sense node needed to be minimized. This leads to a design where the on-pixel storage capacitance is eliminated; and instead the gate capacitance of the sense-node transistor is used to store the incoming X-ray converted charge. This work allows researchers to gain insight into the fundamental noise operation of active pixels used in medical imaging, and to appropriately choose device dimensions. Due to the inherent large feature sizes of thin-film transistors, active pixel flat-panel X-ray medical imagers offer lower resolution than their film-screen counterparts. By demonstrating the desirability of smaller device dimensions for reduced noise and the elimination of a storage capacitor, this research frees some of the area constraints that exist in active pixel flat-panel imagers, allowing for smaller pixels, and thus higher resolution medical imagers. The noise analysis and optimization as a function of pixel TFT device dimensions in this work is applicable to any amorphous silicon (a-Si) based charge-sensitive pixel, and is easily extended to other device technologies such as polysilicon (poly-Si).

In addition, experimental results of a 64x64 pixel four-transistor APS imaging array fabricated in a-Si technology and mated with an a-Se photoconductor for use in medical X-ray imaging is presented. MTF results and transient response in the presence of X-rays (image lag) for the APS array are poor, which is ascribed to high charge trapping at the silicon nitride/a-Se interface. Improvements to the silicon nitride passivation layer and pixel layout are suggested to reduce this charge trapping. The prototype imager is compared directly with a state-of-the-art a-Si PPS imaging array and demonstrates good SNR performance for X-ray exposures down to 1.5μR. Pixel design and fabrication process improvements are suggested for low-exposure APS testing and improved low-noise performance.

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1 Introduction

X-ray images allow us to see what cannot be seen by the naked eye. In medicine, it provides valuable information, allowing radiologists to diagnose everything from broken arms to breast cancer. X-rays, however, are a form of ionizing radiation that damages cellular tissue. In order to increase patient safety during diagnostic medical X-ray imaging procedures, the X-ray dosage needs to be minimized while maintaining adequate diagnostic image quality.

Digital flat-panel imagers have allowed for a reduction in X-ray dosages at medium dose ranges due to their inherently superior detective quantum efficiency over conventional film-screen imagers; however, the large readout noise associated with large-area flat-panel imagers has compromised their use in low-dose real-time imaging applications such as fluoroscopy. The amplified pixel architectures previously proposed to allow for low-dose large area fluoroscopic applications have suffered from low dynamic range, prohibiting their use in radiography. A single X-ray imager that is capable of both radiographic and fluoroscopic applications can reduce hospital costs, both in terms of equipment acquisition and storage space. Furthermore, there has been no fundamental assessment of how to design amplified amorphous silicon (a-Si) imaging pixels in order to optimize for low-noise (referred to the input of imaging pixel) performance, especially as it concerns transistor device dimensions.

The work in this thesis is focused on large-area flat panel imagers in a-Si technology, though the circuits proposed and the noise analysis and optimization as a function of pixel TFT device dimensions performed is easily extended to other device technologies such as polysilicon (poly-Si). A-Si technology was chosen primarily due to its prevalence in current commercial digital flat-panel imagers and due to the ability to fabricate such devices in-house.

This chapter will give a background on some fundamentals of medical X-ray imaging of importance to this thesis, particularly as it relates to imager noise. In addition, current avenues of research for digital flat-panel X-ray imagers are presented. Finally, an outline of

the topics to be discussed in this thesis is presented in relation to the overall goal of producing a low-noise optimized, multi-mode (radiography and fluoroscopy) X-ray imager.

1.1 Fundamentals of X-Ray Imaging

In this section some of the basics of X-ray imaging will be introduced, with a specific focus on those elements that are fundamental to this research.

1.1.1 How X-rays Work in the Body and in Detectors

X-rays are a form of ionizing radiation in the electromagnetic spectrum. For diagnostic medical imaging, the range of X-ray energies incident upon patients runs from 10 keV to 150 keV, which corresponds to wavelengths of approximately 0.12 nm to 0.008 nm respectively [1].

Diagnostic X-rays interact with matter by depositing energy, and in some cases the X-ray will exist after the initial interaction in the form of a scattered X-ray or characteristic X-ray. The types of interactions include the photoelectric effect, Compton scattering, Rayleigh scattering, pair production, and triplet production. Since pair and triplet production occur well above diagnostic imaging X-ray energies, they will not be discussed further.

In photoelectric interaction, an incident X-ray imparts energy to an electron bound to an atom. As a result, the atom is ionized, and a single electron is ejected with kinetic energy equal to the difference between the incident X-ray energy and the binding energy of the electron to the nucleus. A photoelectric interaction is impossible below the binding energy of the electron, and is most probable when the X-ray energy is equal to the electron binding energy. The probability of photoelectric interaction decreases with increasing X-ray energy above the binding energy. For this reason, for diagnostic imaging modalities such as fluoroscopy and radiography which occur typically at X-ray energies of 70 kVp (kiloelectron volts peak) and 120kVp, respectively, the photoelectric effect is not a probable mode of X-ray interaction within the body. Conversely, for mammography where X-ray energies are

typically 10-30 keV, the photoelectric effect is the dominant form of X-ray interaction within the body. Since in medical imaging the X-rays first interact with a patient who is composed mostly of hydrogen (atomic number (Z) = 1), carbon (Z = 6), nitrogen (Z = 7), and oxygen (Z = 8), most of the X-rays released from excited atoms (when electrons fill the vacancies caused by the photoelectric interaction) do not travel very far before being absorbed. This is because for low Z materials, the energy of the released X-ray is quite low. Even for calcium (Z = 20), the K-shell binding energy is only 4 keV. To put this in perspective, the mean free path of a 4 keV X-ray in muscle tissue is about 135 μm. Thus, most characteristic X-rays that are produced within the body are reabsorbed by neighbouring tissues. Additionally, the photoelectric effect is the dominant form of interaction of diagnostic X-rays with high Z materials such as the photoconductors and phosphors present in X-ray detectors, which are discussed in a later chapter.

In Compton scattering, there is an exchange of energy from the incident X-ray to the medium, producing a scattered X-ray photon, an electron, and an ionized atom. Compton scattering typically occurs when the energy of the incident X-ray photon is much greater than the binding energy of the atomic electron. Therefore in X-ray imaging modalities such as fluoroscopy and radiography, Compton scattering is the dominant form of X-ray interaction within the body which is filled with lower atomic number materials.

In Rayleigh scattering, there is no exchange of energy from the incident X-ray to the medium, which results in no ionization of the atom, and no energy loss in the scattered X-ray. However, the scattered X-ray does experience a change in trajectory, making it an undesirable form of interaction for imaging applications. Rayleigh scattering is mostly likely for low-energy X-rays and high-Z materials.

Photoelectric interactions and Compton scattering interactions result in the attenuation of the photon beam as it passes through matter. The number of X-ray photons removed from the X-ray beam will depend on the medium in the path of the beam, and the remainder X-ray photons will reach the detector.

In the next section, a general overview of the noise in X-ray imaging systems will be discussed.

1.1.2 Detective Quantum Efficiency (DQE) and Noise of an Imager

The detective quantum efficiency (DQE) of an imaging system is a measure of noise propagation through the system, and thus describes the overall signal-to-noise ratio (SNR) performance of the system. As such, DQE is a quantity that cannot be changed with post-processing of the image, unlike the modulation transfer function, MTF, and thus it represents a fundamental quantity of the incident spectrum and the detector design [2]. DQE is an indicator of the dose efficiency of an X-ray detector system, thus a detector with high DQE is able to use a lower dose than a detector with low DQE to produce an image with equivalent noise performance.

There are two main types of random noise in a digital X-ray flat-panel integrating detector: X-ray quantum noise and electronic noise. X-ray quantum noise can be determined by the fact that X-ray counting statistics follow a Poisson distribution. With a Poisson distribution, knowing the mean number of photons, N, one knows the standard deviation, σ, as well, where the two are related as follows:

$$\sigma = \sqrt{N} \tag{1.1}$$

Thus, the X-ray quantum noise is given by the root of the average number of detected photons, N [3].

The other source of random noise is electronic noise, which is introduced by the detector. Electronic noise in a flat-panel detector has many components, which include:

- KTC (reset) noise associated with the pixel capacitance
- Shot noise associated with the photodiode leakage current or the photodetector layer, depending on whether indirect or direct detection is used.
- Flicker and thermal noise of the pixel thin-film transistors (TFTs)
- thermal noise associated with the resistance of the data lines

- noise associated with the read-out amplifiers
- noise associated with the image calibration procedures

Fixed pattern noise, which is deterministic in nature, can be removed with double sampling and is not considered in the following DQE formulations. Gain fluctuation noise of the detector, *I*, often referred to as Swank noise, will be incorporated in the DQE.

DQE and SNR are related by:

$$DQE(f) = \frac{SNR_{out}^2}{SNR_{in}^2} \tag{1.2}$$

SNR_{out} and SNR_{in} are given by the following equations:

$$SNR_{out}^2 = \frac{k^2\{MTF(f)\}^2}{NPS(f)} \tag{1.3}$$

$$SNR_{in}^2 = \left(\frac{Signal}{Noise}\right)^2 = \left(\frac{N}{\sqrt{N}}\right)^2 = N \tag{1.4}$$

where *k* is the measured sensitivity of the detector at a given exposure, *MTF(f)* is the spatial frequency dependent modulation transfer function, *NPS(f)* is the spatial frequency dependent noise power spectrum, and *N* is the incident X-ray quanta per unit area (mm^2) also known as the fluence , Φ[1]. Thus,

$$DQE(f) = \frac{k^2\{MTF(f)\}^2}{NPS(f)\Phi} \tag{1.5}$$

The DQE drops rapidly as the additive noise from the electronics begins to dominate the total noise of the system. Ideally, the electronic noise should be significantly less than the signal from a single incident X-ray (minimum noise from X-ray counting statistics), such that it is a "quantum noise limited" system. A quantum noise limited system indicates that the noise is

[1] MTF and NPS are further described in Section 6.3

irreducible, since it is dominated by the random arrival of X-rays and no further efforts to reduce noise can improve the image quality [4].

The noise power spectrum can be separated into electronic (system) noise and quantum noise

$$NPS = NPS_q + NPS_s \tag{1.6}$$

where NPS_q is the quantum noise and NPS_s is the system noise.

It has been experimentally determined for a flat-panel detector that the system noise is independent of spatial frequency and X-ray exposure, *X*, whereas the quantum noise depends on both. Thus equation (1.6) can be written as [5]

$$NPS(f, X) = X \cdot NPS_{qx}(f) + NPS_s \tag{1.7}$$

where $NPS_{qx}(f)$ is the exposure independent spatial quantum noise power spectrum. Separating the exposure related term from the quantum noise allows us to see the overall effect of increasing or decreasing exposure on the DQE and its relation to the system noise.

The sensitivity *k* is directly proportional to the X-ray absorption fraction, η, the incident X-ray fluence, Φ, and the signal produced per absorbed X-ray, *K*.

$$k = K\eta\Phi \tag{1.8}$$

We can normalize the quantum NPS with respect to *K*, η, *I*, and Φ [4]

$$NPS_q(f, \Phi) = \frac{\eta\Phi K^2 NPS_{qn}(f)}{I} \tag{1.9}$$

where NPS_{qn} is the normalized quantum noise power spectrum.

Inserting equations (2.6), (2.8), and (2.9) into equation (2.5), we get the following expression for DQE:

$$DQE(f) = \frac{\Phi^2 (K\eta)^2 \{MTF(f)\}^2}{\Phi(\frac{\eta\Phi K^2 NPS_{qn}(f)}{I} + NPS_s)} \tag{1.10}$$

Rewriting (2.10) as (2.11)

$$DQE(f) = \frac{I\eta\{MTF(f)\}^2}{NPS_{qn}(f) + \frac{I \cdot NPS_s}{\eta \Phi K^2}} \tag{1.11}$$

The difficulty of obtaining a quantum noise limited system is exacerbated for imaging modalities such as tomosynthesis where multiple exposures are required. If each exposure in a multi-exposure modality is kept the same as a single exposure modality, then no image quality problems result; however, patient safety is compromised since the total dose received by the patient has increased. Ideally, the total dosage in a multiple exposure modality (e.g. tomosynthesis) should be the same as the total dosage in a single exposure modality. Keeping the total dosage the same, however, will decrease DQE in cases where the system is no longer quantum noise limited. As seen in (1.11), as the X-ray fluence, Φ, and hence dosage, is decreased, the effect of the system (electronic) noise is increased, causing DQE to decrease. Additionally, as NPS_s increases, the DQE will degrade at higher X-ray exposures.

In addition, we want to have as many exposures as possible in order to have a high resolution image along the z-axis (depth), which results in an even smaller exposure per image. For these reasons, it is imperative to keep the electronic noise to a minimum for low exposure modalities such as fluoroscopy and tomosynthesis.

One goal of this thesis is to reduce the total input referred electronic noise (not including the photoconductor) of the system such that at low exposure (and hence low quantum noise levels), the DQE of the system remains sufficiently large to produce viewable images. For this reason, within the thesis, the desirability of improving the low-noise performance of the imager is often discussed.

1.2 X-Ray Imagers

X-ray images allow us to see what cannot be seen by the naked eye. In medicine, it provides valuable information, allowing radiologists to diagnose everything from broken arms to

breast cancer. In the next section we will give a background on the operation of conventional film-screen X-ray imagers, computed radiography, X-ray image intensifiers, and digital flat-panel X-ray imagers.

1.2.1 Film-Screen

Film-screen imagers are comprised of an X-ray film and an intensifying screen. The X-ray film is usually composed of silver bromide crystals suspended in a gelatin matrix. Electrons are released in the silver bromide crystals when they are exposed to ionizing radiation or visible light. The electrons are trapped at "sensitivity centers" in the crystal lattice of the silver bromide granules. The trapped electrons attract and neutralize mobile silver ions in the lattice, resulting in the deposition of silver metal along the surface of the granules. When the film in placed in a developing solution, additional silver is deposited at the sensitivity centers, resulting in an image.

For diagnostic X-rays, only about 2% to 6% of the total energy in a direct X-ray beam is absorbed by the X-ray film. For this reason, an intensifying screen is coupled to the X-ray film to make more efficient use of the X-ray energy. The intensifying screen converts X-rays into photons of wavelength that can be more easily absorbed by the X-ray film. For instance, gadolinium oxysulfide is often used as a fluorescent screen with X-ray films. Gadolinium oxysulfide, absorbs about 60% of the incoming X-ray photons, and has a conversion efficiency (amount of absorbed energy converted to light) of 20%, with a peak emission of 550 nm [1].

1.2.2 Computed Radiography

Computed radiography (CR) is a digital imaging modality that has gradually replaced traditional film-screen technology in many hospital radiology departments as the move to an all-digital environment has advanced. In computed radiography, an imaging plate made from a photostimulable phosphor, such as BaFBr or BaFI, is used to store energy from absorbed X-rays. The imaging plate is then taken to a reader unit where it moves across a stage and is

scanned by a red laser light. The laser light stimulates the emission of trapped energy from the phosphor in the form of blue-green light. The emitted phosphor light is collected by a fibre optic light guide and strikes a photomultiplier tube, where is produces an electronic signal.

1.2.3 Image Intensifier

An imager intensifier is used in fluoroscopic applications in order to increase the brightness of the image. The X-ray image intensifier "intensifies" the image by two processes: (1) minification, where the number of light photons emanates from a smaller area, and (2) flux gain, where electrons are accelerated by high voltages to produce more light when they strike a fluorescent screen. Figure 1.1 illustrates the general principle involved in image intensifiers.

Incoming X-rays impact a phosphor screen, typically made of cesium iodide (CsI), which then emits visible light photons. The photons then impact a photocathode which then emits electrons. The electrons are accelerated towards the anode at the opposite end of the vacuum tube, whereupon they impact a smaller output phosphor screen which fluoresces as a result. The output screen can then be viewed through an optical system either directly, or through a charge coupled device (CCD) coupled to a video monitor.

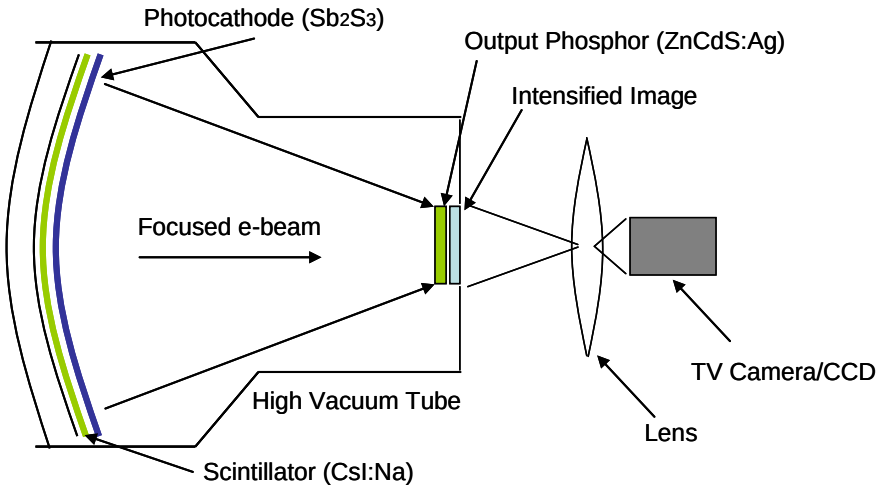


Figure 1.1. Basic Image Intensifier

1.2.4 Digital Flat-Panel Imagers

Digital flat-panel detectors are comprised of two main components. The first component, the X-ray detector, converts X-rays to electrical charge, while the second component stores and transfers the electrical charge to off-panel circuitry. There are currently two main methods of X-ray detection used in flat panel imagers. Systems that incorporate a photoconductor to produce electrical charges on detection of an X-ray are known as *direct* conversion X-ray detectors, whereas those that incorporate a phosphor to produce visible wavelength photons on detection of an X-ray are referred to as *indirect* conversion X-ray detectors.

In direct conversion, a photoconductor material is deposited on top of the flat panel array, such that it is in direct electrical contact. When the incident photons hit the photoconductor, they produce electron-hole pairs that are drawn to electrodes sandwiching the photoconductor material. A voltage is placed across the electrodes in order to attract the electrons and holes. One of these electrodes is connected to a storage element on the pixel, so the accumulated photoconductor charge is shared between the photoconductor and pixel capacitances. Figure 1.2 shows a flat panel direct detector.

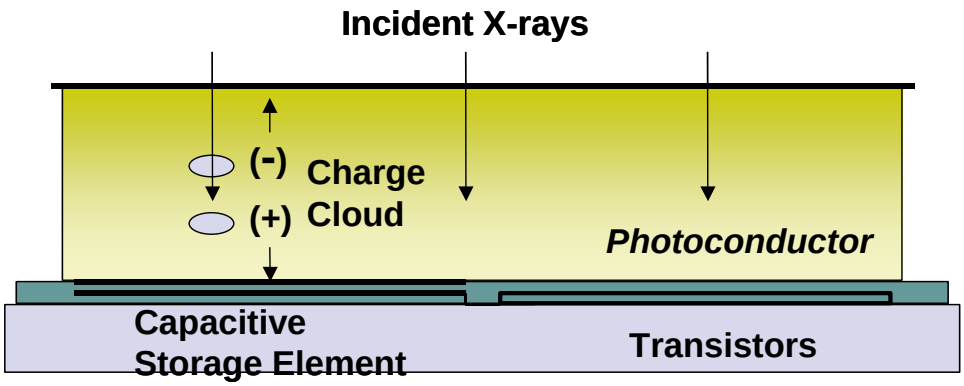


Figure 1.2. Direct Detection [6]

In indirect conversion, a phosphor screen or structured scintillator is placed in intimate contact with a flat-panel detector, as shown in Figure 1.3.

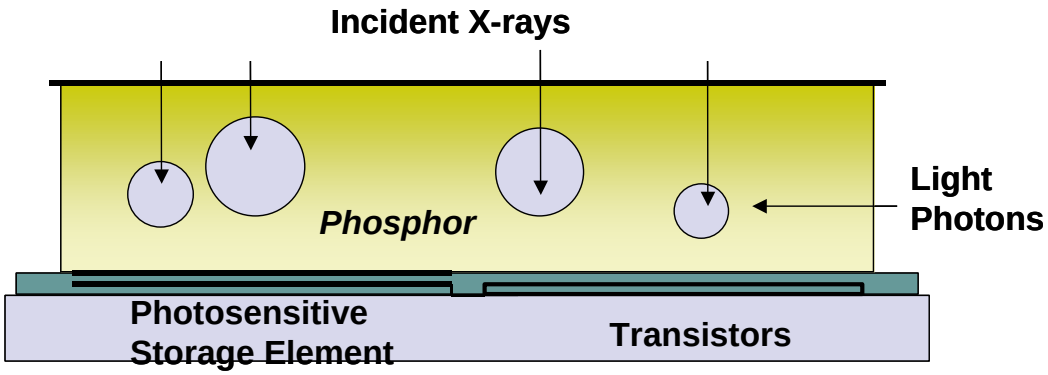


Figure 1.3. Indirect Detection [6]

When X-rays hit the phosphor, they are absorbed and light photons are emitted. The light photons are then converted to electrical charge by an on-pixel photosensitive element, such as a p-i-n photodiode. Depending on the depth at which the light photon is emitted within the phosphor, the degree to which it spreads or scatters is affected. This scattering decreases image resolution, as some photons from adjacent pixels are detected by the photosensitive elements. One method to reduce the impact of light scattering is to employ a structured phosphor such as Cesium Iodide (CsI). When evaporated under the correct conditions, a layer of CsI will condense in the form of needle-like closely packed crystallites. This columnar structure has some properties like a fibre-optic light guide because of the difference in refractive index between CsI (n=1.78) and air (n=1) [6]. Owing to these properties, CsI has become prevalent as a phosphor in medical imaging applications.

In the next section, the benefits of flat-panel imagers compared to conventional X-ray imaging methods are discussed, and their potential areas of improvement are highlighted.

1.2.5 Conventional Systems vs. Flat Panel systems

Over the last decade there has been a push towards large area digital flat-panel X-ray imaging systems due to the many potential advantages they offer over traditional film-screen, computed radiography, and II-video/CCD systems. Some advantages over film-screen technology include less handling and immediate image viewing, higher contrast images,

reduced radiation exposure, computer-aided diagnosis, tele-radiology through satellite or internet, and more convenient archival, retrieval, and management on digital media rather than in film stacks. As seen earlier, an important measure of the dosage performance of an imager is the DQE. Film-screen imagers have a DQE(0) of approximately 25%, whereas flat-panel imagers typically have a DQE(0) of at least 65% [1], which allows for lower dose imaging. DQE(0) is the zero spatial frequency DQE in which reductions in SNR due spatial frequency dependent MTF (i.e. image contrast loss at higher resolution/larger spatial frequency) is not taken into account.

Since computed radiography is a digital imaging modality, some of the advantages that digital flat-panel detectors have with respect to film-screen imagers (such as computer aided diagnosis and tele-radiology) do not exist. However, flat panel imagers have considerably better DQE than CR systems. In fact, flat-panel detectors can reduce radiation dose by about twofold to threefold for adult imaging, compared with CR for the same image quality, due to the better quantum absorption and conversion efficiency associated with flat-panel detectors [3]. In addition, flat-panel imagers have better spatial frequency than their CR counterparts [3].

In fluoroscopic applications, flat panel imagers do not suffer from image distortion caused by optical lenses, unlike II–video/CCD systems [7]. In addition, flat panel imagers can achieve better contrast image quality using only 80 percent of the radiation dose [8]. Furthermore veiling glare (or flare) is substantially smaller in the flat panel-based system. Flat-panel imagers have also been shown to exhibit higher DQE compared to II-CCDs, and, more importantly, a constant DQE over a wide dose range. The flat-panel DQE, however, drops below that of II-CCD systems at the lowest fluoroscopic exposure ranges due to detector read out noise [9].

In addition to increased contrast and reduced dosage benefits, digital flat-panel X-ray imaging also offers the potential for advanced X-ray modalities such as digital subtraction angiography and tomographic mammography.

Flat-panel imagers have been successfully applied to digital mammography and clinical trials have shown them to be at least equivalent to standard film screening mammography. Conventional screening mammography has its limitations, though, as overlapping breast tissues can hide cancers and can produce shadows which mimic a lesion. In tomographic mammography, multiple images are taken from several angles to reconstruct the image into multiple cross-sections. The multiple cross-sections allow radiologists to distinguish lesions that would otherwise be hidden with conventional mammography. Conversely, breast tissues can be mistaken for lesions in conventional mammography, creating false positives. In fact, false positives account for almost 25 percent of the instances when women are recalled for additional imaging. Tomosynthesis has been shown to reduce the number of false positives by approximately 85 percent [10].

Studies using a-Si flat-panel imagers to perform circular and cone-beam tomosynthesis have reported positive results where twenty and eleven low-dose images were used to reconstruct the image, respectively [11], [12]. Although the results have been promising, there are several deficiencies in the present systems including: large pixel size, long exposure times, high dose, and poor image quality in the reconstructed cross sections. In order to improve image quality and increase patient safety, the number of images taken should be increased, and the total exposure decreased to at least that of conventional screening mammography. Decreasing the exposure per image, however, makes the image more susceptible to system (electronic) noise.

For conventional mammography, the exposure ranges from 0.6mR to 240mR [13]. Assuming 33 images are required for a tomographic image, the range scales to 0.018mR to 7.2mR. Extrapolating from data presented in [14], the quantum noise at an exposure of 0.018mR is 850 electrons, while the quantum noise at the mean exposure of 0.36mR is 3800 electrons.

Current state-of-the-art digital X-ray detectors for mammography have noise levels much higher than those desirable for tomosynthesis applications. An a-Se flat-panel imager for screening mammography produced by the Anrad Corporation has the electronic noise of the detector at around 4500 electrons [15]. An optimized a-Si/CsI based flat panel detector for

mammography produced by General Electric has an electronic noise level of 6 X-rays [2]. Even if a modest conversion efficiency of 700 electrons per X-ray photon is assumed, it yields 4620 electrons of noise.

So while digital flat-panel detectors have many advantages over conventional film-screen technologies and II-video/CCD technologies, their largest deficiency stems from their poor low-noise performance. Improving the low-noise performance of digital flat-panel imagers will facilitate their use in fluoroscopy and next generation low-exposure modalities such as tomographic mammography. In the next section, the current state of research of flat panel imagers will be presented.

1.3 Current State of Research of Digital Flat Panel Detectors

As discussed in section 1.2.4, digital flat-panel detectors are comprised of two main components. The first component converts the incoming X-rays into electrical charge and the second component stores and transfers the electrical charge to off-panel circuitry. In order to improve the low-noise performance of the flat-panel detector, one could either increase the signal, or reduce the noise, or both increase the signal and reduce the noise. Increasing the signal can be accomplished by increasing the charge conversion efficiency of the photodetector (photoconductor or phosphor-photodiode). Alternatively, one could increase the gain of the pixel circuit in order to increase the signal. In order to reduce the noise, all the noise sources need to be identified, at which point pixel circuit design techniques could be used to minimize noise contributions from the imaging array and associated circuitry. We will present the various methods being used to potentially solve the low-noise performance problem of flat-panel imagers.

1.3.1 Detector Improvements

One potential avenue of research is to improve the performance of the X-ray detector such that one X-ray generates an increased number of electrons, thereby increasing the input

signal. We will look at various direct and indirect detectors and methods of increasing the charge conversion efficiency in both cases.

1.3.1.1 Direct Detectors

In order for a candidate photoconductor material to be successfully integrated into a direct detection flat-panel imager, the following material requirements must be satisfied [16]:

- Chemistry of the material must be compatible with the active matrix to prevent chemical reactions.
- Deposition process must be compatible in order to promote good surface morphology, such as the elimination of voids.
- Good temporal signal properties so as to promote prompt extraction of the X-ray-generated charge.
- Pixel-to-pixel signal uniformity so that non-uniformities are dominated by X-ray statistics.
- High gain
- Low dark current to minimize dark noise contributions and to maximize the exposure range of the device
- Low degree of charge trapping in between the pixels, at any interfaces, or in trapping states in the bulk of the material
- Signal response of the pixels to radiation should be linear over a considerable fraction of the pixel signal range.

The most commonly used solid-state photoconductor in medical X-ray imaging is amorphous selenium (a-Se). Amorphous selenium has the advantage of simple deposition over large areas. The dark current density, $J_{a\text{-}se,dark}$, has been given as 1 pA/mm^2 at an electric field of 10 V/μm [4,17], though values as low as 7 fA/mm^2 have been reported for thick a-Se photoconductor layers at an electric field of 14 V/μm [18].

One disadvantage of a-Se is its need for high electric fields of about 10V/μm in order to adequately collect charge. This translates into 10,000 volts for a layer of 1mm thickness,

which is a typical thickness for X-rays at fluoroscopic energies [14]. Because of this high voltage, precautions must be taken in order to prevent damage to the flat panel imager. Since the pixel capacitance is in direct contact with the photoconductor, it must be ensured that the majority of the 10,000 volts is dropped across the a-Se capacitance. This is accomplished by designing the pixel such that the effective resistance of the pixel is substantially smaller than the resistance of the a-Se layer. Care must also be taken to ramp-up the high voltage slowly in order to prevent voltage spikes that could damage the in-pixel electronics.

Another disadvantage of a-Se is that it uses a low Z (34) element to stop X-rays, which translates into poor absorption (and hence charge conversion) of higher energy X-rays used in fluoroscopy and radiography (though it is very good at stopping the lower energy X-rays used for mammography).

Lastly, a-Se has only a modest charge gain efficiency of about 1000 electrons/X-ray at X-ray energies of 70kVp as used in fluoroscopy. The charge gain places an upper limit on the total electronic noise, such that the electronic noise should be much less than 1000 electrons for a quantum limited X-ray imager.

Due to the very large voltage required, modest charge gain, and low X-ray stopping ability of a-Se, there has been research into various different materials to combat these problem areas. Since flat-panel X-ray detectors cover a large area, crystalline semiconductor photoconductors like cadmium zinc telluride (CZT) are still too expensive. Thus research has been focused on polycrystalline modifications of high-Z (atomic number) materials, the most promising candidates being HgI_2 [16, 19-23], PbI_2 [20,21], poly-CZT [24] and PbO [25-27]. Table 1 lists the various different materials being used or studied for direct detection of X-rays. The important performance parameters for high frame rate modalities such as fluoroscopy include the image lag after one frame, the dark current density, and the effective energy (W_{eff}) required to liberate an electron-hole pair. In order to be feasible for X-ray medical imaging applications, the photoconductor must have a dark current of less than or equal to 10 pA/mm^2, and a lag after one frame of less than 15% [19]. The increase in charge

gain of the various photoconductors compared to a-Se is inversely proportional to W_{eff}. For instance, the charge gain for PbO is approximately seven times that of a-Se.

Table 1. Performance parameters of various direct detectors for fluoroscopy

Material	W_{eff}	**Lag after 1 frame (at 30 fps)**	**Dark Current Density**
a-Se	45 eV @ 10 V/μm	1 %	$\leq$ 1 pA/mm^2
HgI_2	5 eV @ 0.7 V/μm	7.1 %	10 pA/mm^2
PbO	6 eV @ 1 V/μm	7 %	110 pA/mm^2
Poly-CdZnTe	7 eV @ -0.8 V/μm	70 %	114 pA/mm^2

Of all the *alternate* materials, HgI_2 shows the greatest promise for use in fluoroscopy, though there are still many obstacles that must be overcome such as consistent performance in the following areas: chemical inertness, homogeneity of sensitivity over the entire imager array and low dark current.

The next section will discuss the methods currently being used to improve the low-noise performance of indirect detectors.

1.3.1.2 Indirect Detectors

One method to increase the signal from indirect detectors is to increase the signal collection efficiency of the associated photodiodes through geometrical fill factor increases. Many commercial flat-panel detectors incorporate the photodiode and TFT on the same plane, which can drastically reduce the collection efficiency for small pixel sizes. By using a continuous photodiode design such that the photodiode resides on a layer above the TFT, geometrical fill factors of greater than 85 percent can be achieved, resulting in an increase in simulated DQE(0) of up to approximately 0.2. However, even with near 100 percent fill factor, the simulated DQE(0) does not rise above 0.2 for the lowest fluoroscopy exposures (< 0.3 μR) [16].

Another novel way to increase the signal from an indirect detector is to couple it to a light-sensitive photoconductor such as a-Se instead of a photodiode. In order to get good gain from

the device, the a-Se photoconductor is operated in avalanche mode [28]. Amorphous selenium (a-Se) photoconductors have been successfully used in avalanche multiplication mode in broadcast applications; however, the detector has only been a maximum of two inches in diameter [29]. The main problem with operating in avalanche multiplication mode is that the gain changes as a function of the photoconductor thickness. A four percent variation in photoconductor thickness results in gain differences of 2-3 times, possibly the maximum that can be handled by post gain correction algorithms [29]. This small tolerance in the variation of the photoconductor thickness over a full-size imager poses fabrication challenges.

Instead of detector improvements, one could increase the gain of the pixel circuit in order to increase the signal. At the same time the noise of the pixel circuit could be reduced or optimized such that the SNR is maximized, or in other words, the total input referred noise is minimized. The main focus of this thesis is to analyze and optimize a novel pixel circuit architecture for low-noise performance capable of high dynamic range for use as a dual imager for radiography and fluoroscopy. The next section will detail the organization of this thesis with respect to the goal of producing such a pixel circuit.

1.4 Thesis Organization

The main focus of this thesis is to analyze and optimize a novel pixel circuit architecture for low-noise performance capable of high dynamic range for use as a dual imager for radiography and fluoroscopy (R&F).

Chapter 2 discusses various pixel architectures in a-Si technology for X-ray imaging devices, and presents a novel active pixel sensor (APS) architecture able to meet the needs of both low-noise, real-time fluoroscopy and high dynamic range radiography.

Chapter 3 discusses the fabrication of the single TFTs, TFT circuits, and TFT arrays used for this thesis. Material characterization of the various TFT layers is discussed along with an outline of the fabrication process. Fabrication issues related to the TFT design are considered

for the application of X-ray imaging in light of minimizing the total input referred noise, such as minimizing stray capacitances at the input sense node.

Chapter 4 develops a circuit noise model for the proposed R&F pixel using existing thermal and flicker noise TFT models. The circuit noise model also includes the charge amplifier readout, and presents simulated data for the total circuit noise referred to the input of the pixel. The pixel TFT device dimensions are optimized for low noise performance in a-Si technology. Finally, the effect of varying electronic noise and incident X-ray exposure on the DQE of an imaging system using an a-Se photoconductor for fluoroscopy applications is presented.

Chapter 5 presents the results of single transistor flicker and thermal noise tests in order to validate and extract parameters to be used in the a-Si TFT thermal and flicker noise models presented in Chapter 4. The R&F pixel tests are conducted in order to experimentally verify the noise optimization model using the thermal and flicker noise parameters extracted from the single TFT tests.

Chapter 6 presents the integration, testing, and results from a 64x64 pixel prototype a-Si APS pixel imaging array mated with an a-Se photoconductor for use in medical X-ray imaging. Modulation transfer function (MTF), transient response, and SNR results of the APS array in the presence of X-rays are presented. Measured data and images from the prototype imager are compared directly with a state-of-the-art commercially available a-Si PPS X-ray imager using an RQA5 standard fluoroscopic characterization beam. Pixel design and fabrication process improvements are suggested for low-exposure APS testing and improved low-noise performance.

Chapter 7 concludes this research and summarizes the contributions of this thesis to the field of medical X-ray imaging. In addition, suggestions are made regarding design and fabrication improvements for future work.

2 Pixel Architectures

This section discusses various pixel architectures in a-Si technology for X-ray imaging devices, and presents a novel pixel architecture able to meet the needs of both low-noise, real-time fluoroscopy and high dynamic range radiography.

2.1 PPS

The most widely used architecture in flat-panel imagers is a passive pixel sensor (PPS) [30-32], which consists of a detector element and a readout switch. The detector element, as shown in Figure 2.1, is a photodiode sensor as used in an indirect X-ray detection scheme; however, the detector could also be an on-pixel storage capacitance as in the case of a direct X-ray detection scheme.

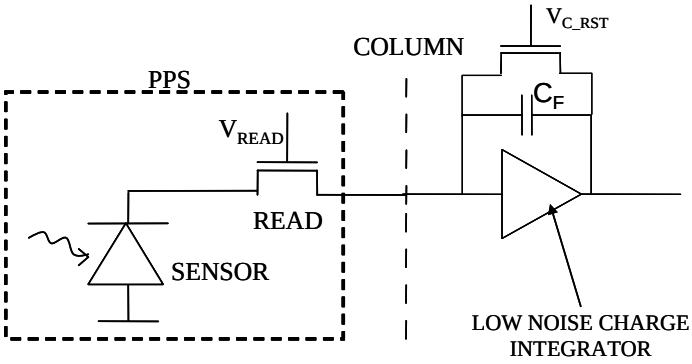


Figure 2.1. PPS Circuit

The readout switch is an a-Si TFT, which along with (primarily) the capacitance of the detector element, determine the readout speed of the PPS pixel. The time constant associated with the PPS pixel is given by

$$\tau_{PPS} = R_{ON} C_{PIX} \tag{2.1}$$

where R_{ON} is the resistance associated with the open a-Si TFT switch, and C_{PIX} is the total pixel capacitance at the sense node. Assuming that full charge readout occurs after $5\tau_{PPS}$, and that R_{ON} = 0.5MΩ and C_{PIX} = 0.5pF, the minimum readout time is 1.25μs which is well

within the 66μs row time limit required for real-time (30Hz) fluoroscopy (assuming 1000 rows per array, and that readout is performed from both sides of the array).

While the PPS circuit has the advantage of being compact and amenable toward high-resolution imaging, small PPS output signals are swamped by external column charge amplifier and data line thermal noise, which reduce the minimum readable sensor input signal.

2.2 V-APS

In order to increase the signal-to-noise ratio (SNR) of low-dose X-ray images, it has been proposed to have amplifiers within the pixels themselves. The pixel circuit shown Figure 2.2 in is referred to as an active pixel sensor (APS) and had been proposed for use in CMOS technology in the early 1990s [33]. Simple CMOS buffers can also be used instead of the complicated opamp buffer depicted in Figure 2.2.

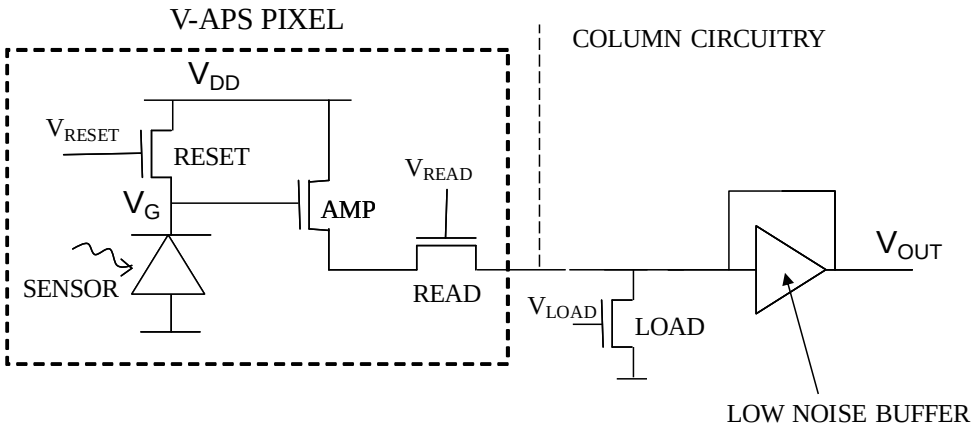


Figure 2.2. V-APS Circuit

While such a circuit is useful in CMOS technology, its use is not feasible in a-Si technology due to very long readout times. In order to effectively transfer voltage from the sense node to the output node, the resistance of the LOAD transistor should be large such that the transistor is biased in the saturation regime. The effective time constant associated with this topology is given by

$$\tau_{V-APS} = R_{LOAD} C_{LINE} \tag{2.2}$$

where R_{LOAD} is the resistance associated with the LOAD a-Si TFT, and C_{LINE} is the line capacitance from the pixel output to the column LOAD TFT. Both R_{LOAD} and C_{LINE} are typically at least an order of magnitude larger than R_{ON} and C_{PIX} of a PPS switch, respectively, resulting in readout times two orders of magnitude larger. Such long readout times make real-time imaging impossible.

This pixel is referred to as a V-APS (voltage APS) circuit since it transfers voltage from the sense node to the output, in contrast to a C-APS (current APS) circuit which transfers charge (current) to the output.

2.3 C-APS

One way to increase the signal-to-noise ratio (SNR) at low X-ray doses in a-Si technology without sacrificing readout speed is to employ pixel amplifiers where the signal is read-out as a current [34]. These current-mediated active pixel sensor (C-APS) circuits, as shown in Figure 2.3, have the potential to reduce the readout noise to levels that can meet even the stringent requirements of low-noise digital X-ray fluoroscopy (< 1000 noise electrons).

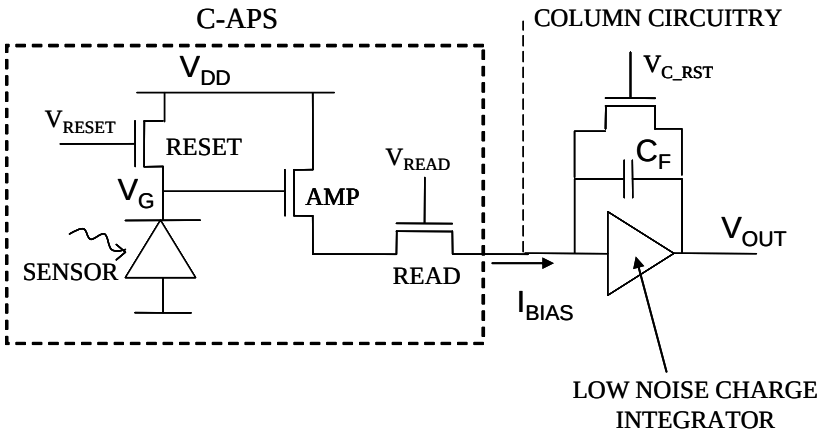


Figure 2.3. C-APS Circuit

A challenge with the C-APS circuit, however, is the presence of a small-signal input linearity constraint. While using such a pixel amplifier for real-time fluoroscopy (where the exposure level is small) is feasible, the voltage change at the amplifier input is on the order of 100 times larger for radiography due to the larger X-ray exposure levels, which causes the C-APS output to be non-linear. One way to solve this problem is to use a hybrid amplified pixel architecture based on a combination of PPS and amplified pixel designs that, in addition to low noise performance, also results in large signal linearity and consequently higher dynamic range [35, 36]. The focus of this research will be the development of a multi-mode amplified pixel sensor (M-APS) array, which will be analyzed in the next section.

2.4 M-APS

One current area of research is in the creation of multi-mode imagers, such as combined radiographic and fluoroscopic (R&F) devices, which will reduce hospital costs, both in terms of equipment acquisition and storage space. To meet the high dynamic range requirements of radiography, the existing PPS architecture is mated with the C-APS. In order to maintain the same number of pixel transistors, and hence keep the pixel area small, the reset transistor of the C-APS is also used as the PPS readout switch. This combined PPS and C-APS architecture is named a multi-mode active pixel sensor (M-APS) due to its ability to be used for multiple X-ray imaging modalities. Another objective of this research is to optimize the pixel architecture for low-noise performance. This will allow for improved image quality at low-doses, as well as the potential for a reduction of X-ray doses, resulting in increased patient safety. This section will discuss the proposed M-APS architecture as well as the array level pixel design and implementation. Pixel-level analysis, simulation, and optimization for low-noise performance is discussed in a later chapter.

The multi-mode active pixel sensor (M-APS) architecture for several array pixels with timing diagram is shown in Figure 2.4. For radiographic operation, the RDP pixel transistor is operated while the RDC transistor is kept OFF and the circuit effectively operates as the PPS. Reading out a PPS circuit also acts to reset the charge node. We can take advantage of this PPS characteristic by using the PPS switch transistor, RDP, to also reset the pixel when

operating in C-APS mode. By using the PPS switch to reset the pixel, we are also in effect reading out the photodetector charge in PPS mode regardless of whether we are operating in C-APS mode or not. Hence, we have the advantage of dual-mode readout of the photodetector charge, which could be used to potentially increase the signal to noise ratio of the system. When operating in PPS mode, a fixed charge is transferred and accumulated on the feedback capacitor of the column charge amplifier, C_F, while in the case of APS mode, a fixed current is used to accumulate charge across the column charge amplifier for a specified integration time.

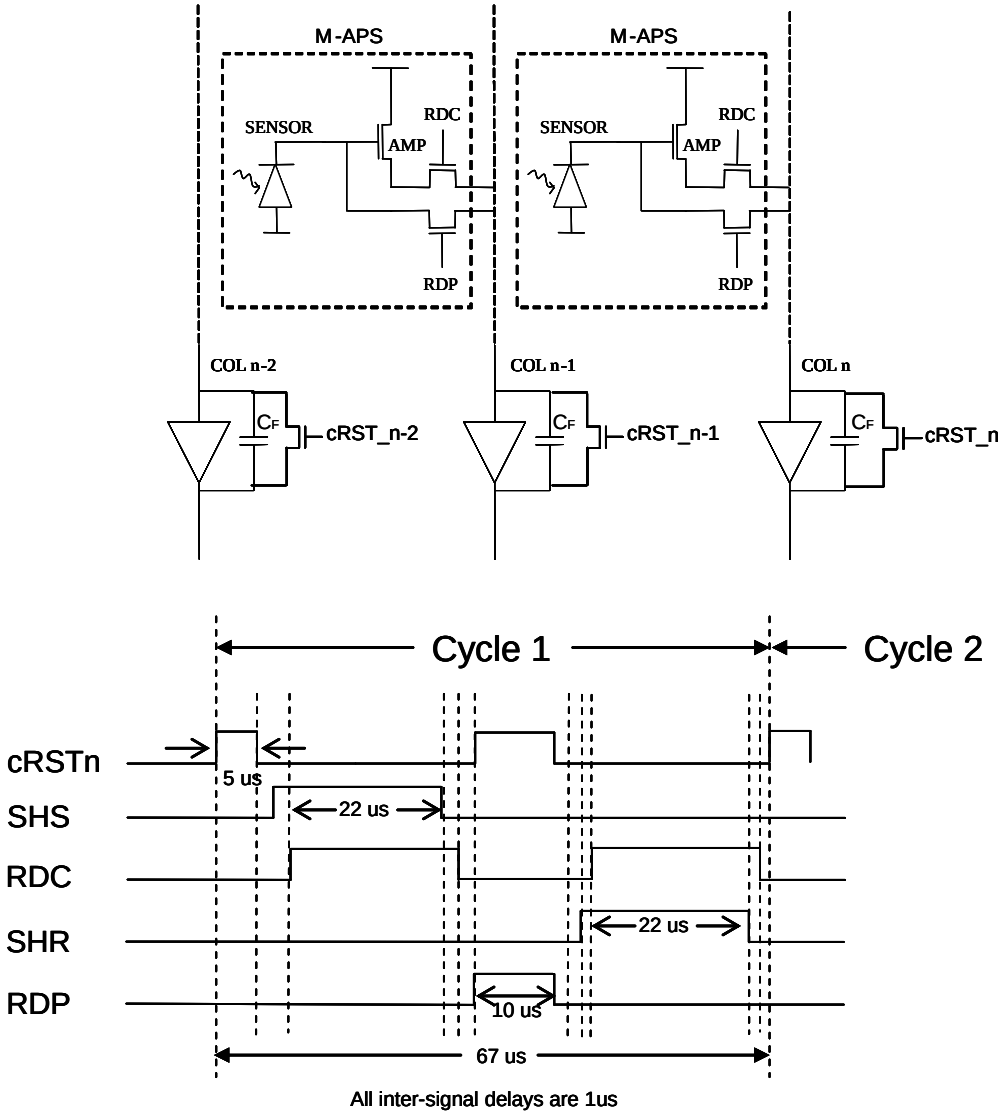


Figure 2.4. Three transistor M-APS pixel circuit and C-APS mode timing diagram

The timing diagram of Figure 2.4 shows the implementation of hardware double sampling. Here the sense node charge is readout twice; the first read operation transfers a current proportional to the X-ray modified sense node charge to the column charge amplifier. The pixel is then reset through the RDP transistor, and a second read operation transfers a baseline current to the column charge amplifier.

The voltage at the output of the charge amplifier for pixel number one of an array is given as

$$V_{o1} = \frac{Q_{o1}}{C_F} = \frac{i_{D1} T_{\text{int}}}{C_F} \tag{2.3}$$

where Q_{o1} is the charge across the feedback capacitor C_F, i_D is the current flowing through the AMP and RDC TFTs (and into the column charge integrator), and T_{int} is the integration time. Subtracting the reset sample, V_{o12}, from the signal sample, V_{o11}, we have

$$V_{o1} = V_{o12} - V_{o11} = \frac{i_{D12} T_{\text{int}}}{C_F} - \frac{i_{D11} T_{\text{int}}}{C_F} = \frac{I_{D1} T_{\text{int}}}{C_F} - \frac{(I_{D1} - i_{d1}) T_{\text{int}}}{C_F} = \frac{i_{d1} T_{\text{int}}}{C_F} = \frac{T_{\text{int}}}{C_F}\left(G_{m1} \frac{Q_{in1}}{C_{eff1}}\right) \tag{2.4}$$

Thus, the difference between the reset sample output current, i_{D12}, and signal sample output current, i_{D11}, is simply the small-signal output current, i_{d1}, that results from the small-signal voltage change at the input of the AMP TFT gate due to the incoming X-ray converted charge, Q_{in1}. Here G_{m1} is the transconductance of the C-APS pixel and C_{eff1} is the effective sense node capacitance of the pixel.

2.4.1 Linearity

The linearity of the C-APS circuit is determined by the linearity of the charge gain, G_i, which in turn has two parameters which are dependant upon the amplifier TFT input gate voltage, namely the circuit transconductance, G_m, and the effective input (sense node) capacitance, C_{eff}. Maintaining strongThe charge gain, G_i, of the amplified pixel-charge integrator circuit combination is given by [13]

$$G_i = G_m T_{int}/C_{eff}. \quad (2.5)$$

Here G_m is the transconductance of the C-APS circuit given by

$$G_m \approx \frac{g_{m1}}{1 + g_{m1} r_{ds2}} \quad (2.6)$$

where g_{m1} is the transconductance of the AMP transistor and r_{ds2} is the ON resistance of the RDC transistor.

The effective sense node capacitance, C_{eff}, is smaller than the total capacitance of the sense node due to the AMP TFT parasitic feedback capacitance, C_{gs1}. The effective capacitance at the detection node is given by [37]

$$C_{eff} = C_{PIX} + (1 - A_{v0})C_{gs1} \quad (2.7)$$

where C_{PIX} is the pixel node capacitance from the gate of the AMP TFT to ground and A_{v0} is the DC gain of the AMP TFT taken from the source to the gate of the AMP TFT.

The linearity of the C-APS circuit also depends strongly upon the dimensions of the AMP and RDC TFTs as both G_m and C_{eff} are dependent upon the transistor dimensions. The value of the transconductance, G_m, depends on the aspect ratios (W/L values) of the AMP and RDC TFTs, while C_{eff} is dependent not only on the aspect ratios of the AMP and RDC TFTs (due to its dependence upon A_{v0}) but also on the absolute value of the AMP dimensions due to its effect on C_{gs1}.

It should be noted that good linear charge gain performance of the C-APS is aided by the negative feedback introduced by the RDC TFT. As the voltage at the gate of the AMP TFT decreases, it causes a decrease in bias current. The decrease in bias current reduces the voltage at the source of the AMP TFT, thus stabilizing the AMP transconductance, g_{m1}, and hence the charge gain.

For the purposes of our a-Si C-APS linearity simulation, we have fixed the RDC TFT dimensions $(W/L)_2$ at 25um/15um as well as the AMP TFT length, L_1, at 10um while varying

the AMP TFT width W_1. A summary of the parameters used for the linearity simulation is shown in Table 2.1.

The percentage change in charge gain as a function of the input signal in electrons is illustrated in Figure 2.5. The optimal device dimensions for charge gain linearity depend strongly on the aspect ratios of the C-APS circuit transistors. For instance, for a W_1 of 80 um or 100 um, more than 10 x 10^4 signal electrons can arrive before the charge gain of the C-APS will deviate by more than 0.05 percent, whereas for a W_1 of 44 um, less than 2 x 10^4 signal electrons can arrive before the same charge gain deviation is reached; a difference in input signal electrons of approximately an order of magnitude.

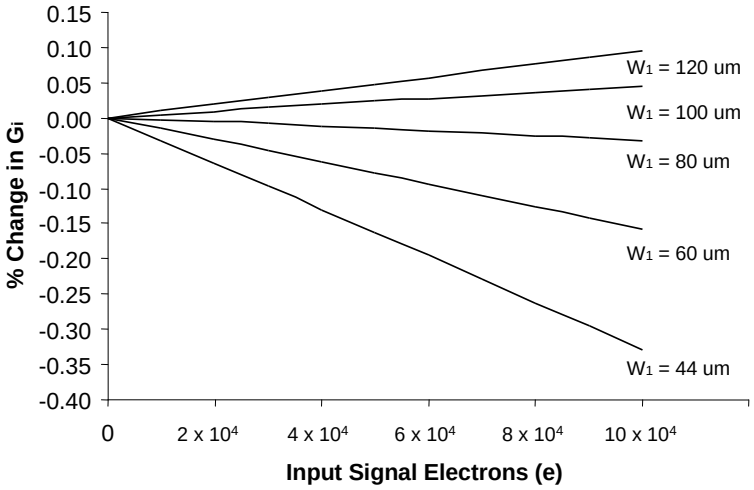


Figure 2.5. Percentage change in charge gain, G_i, vs. input signal electrons for $(W/L)_2$ = 25um/15um, L_1 = 10um, and nominal V_G = 10 V.

Table 2.1 Parameters for linearity simulation of the C-APS circuit

TFT Simulation Parameters	a-Si
V_{DD} (V), DC power rail	10
V_G (V), Nominal AMP gate voltage	10
V_{RDC} (V), RDC gate voltage	15
μ_{eff} (cm^2/Vs), Effective channel	0.5
V_T (V), TFT threshold voltage	4
C_{eff} (pF), effective pixel node capacitance	0.49

Figure 2.5 illustrates the full exposure range (incident on the detector) for fluoroscopy, where the mean (geometric) exposure is 1 x 10^4 signal electrons, and the maximum exposure is 10 x 10^4 signal electrons. The maximum tolerable nonlinearity of the C-APS will likely need to be determined experimentally based on image quality; however, there are steps that can be taken to reduce the nonlinearity without having to increase device dimensions excessively, which would potentially result in large increases in input referred noise and pixel area. For instance, by decreasing the gate voltage of the RDC TFT, we can increase the TFT on-resistance, and hence improve the negative feedback to help stabilize the gain (at the cost of reduced charge gain). Thus, by changing V_{RDC} in Table 4 from 15 Volts to 12 Volts, we can improve the linearity from a charge gain deviation of 0.33 percent at 10 x 10^4 signal electrons to a charge gain deviation of only 0.067 percent. This reduction in V_{RDC} (and hence charge gain) would only cause an increase in input referred noise of 9 electrons, from 401 electrons to 410 electrons. In the case where the input signal electrons cause a charge gain deviation of more than 0.1 percent (for example), the M-APS can be operated in PPS mode, where perfect signal linearity is expected. Thus, one can use the C-APS portion of the M-APS for low-level sensor inputs (fluoroscopy) where charge gain is necessary for good signal-to-noise ratio, and use the PPS portion for high-level sensor inputs (radiography), thus achieving high linearity for all signal ranges.

2.4.2 Area and Metastability

Unlike a conventional PPS, which has only one TFT switch, there are three TFTs in the M-APS pixel, the same as the conventional C-APS pixel. In an effort to optimize fill factor, one could design the TFTs to be embedded under the sensor as in other fully overlapped direct and indirect sensor architectures [38]. In the case of using a direct a-Se sensor, it has been shown that a pixel with an electrode of 66 percent fill factor has nearly 100 percent fill factor due to the high electric field strength [39]. Using the SFU cleanroom TFT process with a minimum channel length of ten microns, we conservatively designed a non-overlapped 4-TFT M-APS circuit (to be discussed in the next section) to fit within a 250 μm pitch square pixel with 57 percent electrode fill factor. By using a more advanced 5 μm process, it will be possible to fabricate a 3-TFT M-APS circuit for R&F applications within a 135 μm pitch square pixel with 65 percent fill factor. A fluoro-dedicated pixel can be fabricated with a 135

μm pixel pitch and 71 percent fill factor, or with a 100 μm pixel pitch and 60 percent fill factor. Studies have shown that the optimal pixel size for fluoroscopic applications is between 100 μm - 200 μm, with values closer to 100 μm being optimal for direct detection schemes [40,41].

The metastability of the C-APS pixel has been previously reported to cause a shift in G_m of less than 2 percent over 10,000 hours [42]. The negative feedback action of the RDC TFT minimizes the impact of ΔV_T variations in the same manner that the charge gain in stabilized.

2.4.3 Imaging Array Implementation

A prototype 64×64 pixel a-Si APS imaging array was fabricated in order to better assess the real-world performance of an a-Si APS imager. Testing was originally to be carried out in-house, and in order to facilitate easier testing, several changes were made to the array design based on the parts and equipment that were available to us. In addition, an update was made to the pixel design which is not reflected in the fabricated array. This newest design is shown in Figure 2.4, and allows for a simpler layout and the reduction of one column charge amplifier from our fabricated array design. The three main differences between the fabricated array as shown in Figure 2.6 and the pixel shown in Figure 2.4 are:

- pixel contains 4-TFTs instead of 3-TFTs
- array readout scheme uses one less data line
- array consists of one additional column charge amplifier due to different pixel layout

The 4-TFT design was chosen to allow for easy mating with the charge amplifiers we could easily procure. In the case of the 3-TFT design, one way to operate the pixel reset is to have the charge amplifier shift its reference voltage depending on whether it is integrating charge from the RDC TFT or whether the sense node is being reset through the RDP TFT. In the case of the 4-TFT pixel, a separate RESET TFT is used, thus removing the level shifting requirement of the column charge amplifier.

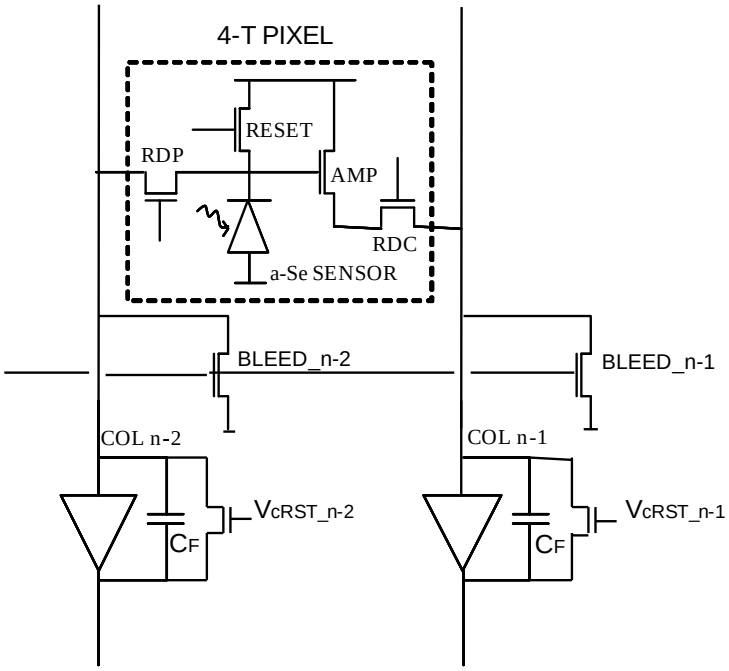


Figure 2.6. Circuit schematic of the 4T a-Si pixel with on-panel BLEED TFTs and off-panel CMOS column charge amplifiers.The dashed line represents a 4-T pixel on the array.

Because hardware double sampling was not possible with the synchronous gate drivers that we were able to obtain, we opted for a simpler readout scheme, which also allowed for the removal of one data line. In this readout scheme, the RDC_m and RESET_m-1 (i.e. the RESET TFT from the previous row) share the same gate line. In this way, while the signal is being read-out through RDC, the previous row of pixels are also being reset as shown in Figure 2.7. Such a design allows for a smaller pixel area, a reduction in the required number of gate drivers, and increase in pixel reliability owing to the simpler pixel design.

The cost of such a readout scheme is that hardware double-sampling is made more difficult (assuming the gate drivers allow for such an option) requiring three timing pulses instead of two. The other option is to implement a form of double-sampling in software, where a dark field image is used to correct for any fixed pattern noise in the array and recover the signal (from the bias). If multiple dark field images are averaged, then the white noise will be considerably reduced, such that the thermal noise and reset noise of the dark field image are

negligible. Thus, in the case of software double sampling, the thermal noise and reset noise variances would not be doubled as they are for hardware double-sampling. The downside of software double-sampling is that the bandpass filtering effect on the low-frequency flicker noise is all but negated due to the long time interval between the dark field image and the signal image.

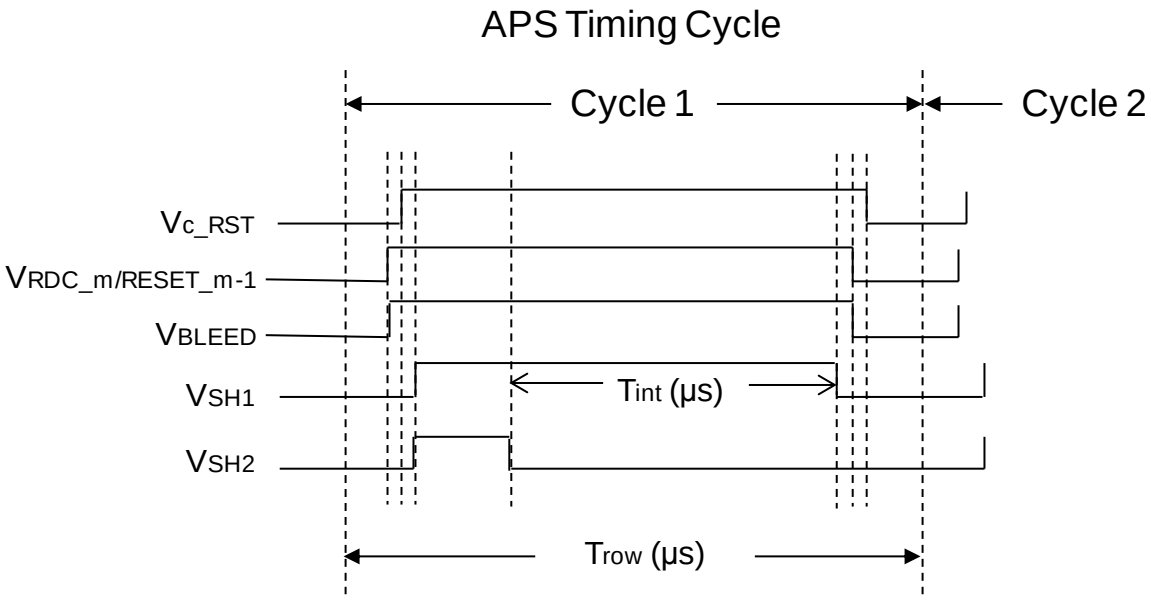


Figure 2.7. Timing diagram for C-APS operation of fabricated 4-TFT imaging array

Testing of the 64×64 pixel imaging array with results will be presented in Chapter 6. The next chapter will cover fabrication aspects of the thin film transistors and pixel arrays to be tested.

3 Fabrication of TFT circuits and arrays

This chapter discusses the fabrication of the single TFTs, TFT circuits, and TFT arrays used for this thesis. First, material characterization of the various TFT layers is discussed. Second, the TFT design is considered for the application of X-ray imaging. Third, the fabrication process is outlined in detail. Lastly, TFT parameter characterization and extraction is presented. All of the devices discussed in this chapter were characterized and fabricated at Simon Fraser University. Appendix A contains additional information on material characterization and TFT fabrication performed at the University of Waterloo.

3.1 Material Characterization of TFT layers

The materials used in the TFT array process are: aluminum, phosphorous doped microcrystalline silicon (n+ μc-Si), hydrogenated amorphous silicon (a-Si:H), hydrogenated silicon nitride (SiN_x:H), and polyimide. A cross-section of the TFT array process including the amorphous selenium (a-Se) photoconductor and top electrode is shown in Figure 3.1.

As can be seen from Figure 3.1, aluminum is used exclusively for the metallization layers which form the source/drain contacts, gate/interconnect metal, and the a-Se bottom electrode. The metal used in the TFT process is 1% silicon doped aluminum (Al/Si 1%). The doping helps prevent the aluminum from spiking into silicon [43], which would be a problem if metal from the source/drain aluminum contacts spiked into the a-Si channel and thus formed a Schottky contact. It should be noted that for relatively low-temperature TFT processes, such as ours, where the maximum substrate temperature is about 250ºC, such spiking is not a problem. Additionally, silicon doping does not harden the aluminum appreciably, thus it does not decrease wire bonding performance.

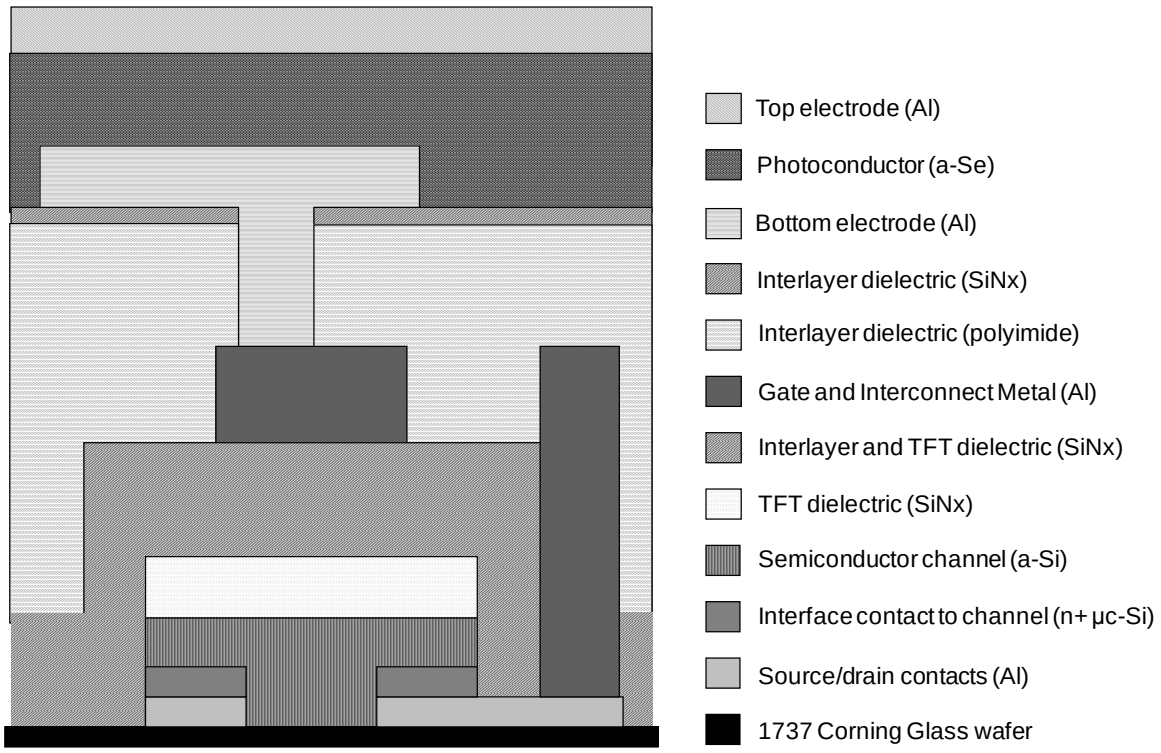


Figure 3.1 Cross-section of the APS X-ray imager fabrication process

All aluminum metal layers are deposited using DC plasma sputtering with the following deposition parameters: Power = 50W, DC Bias = 240V-340V, chamber baseline pressure < 1.5 x 10^{-6} T, chamber deposition pressure ~ 5mT, substrate-target spacing = 11cm. Based upon the above sputtering process parameters, the deposition rate was measured to be ~8nm/min, and the resistivity was measured to be 6.6 x 10^{-8} Ω-m for 80nm thick samples (pure Al bulk resistivity is 2.8 x 10^{-8} Ω-m).

All the silicon based films of the TFT process (n+ µc-Si, a-Si:H, SiN_x:H) are deposited using a standard 13.56MHz RF plasma enhanced chemical vapour deposition (PECVD) cluster tool system designed by MVSystems. The RF electrode area is 12cm x 12cm and the substrate-electrode spacing is 1.37cm. Table 3.1 lists the process parameters for the films deposited by PECVD.

For the n+ µc-Si film the conductivity was measured to be 15 S/cm for 60 nm thick films. The n+ µc-Si film is based primarily on the work of Lee [44], though the process has been

simplified in that instead of using a multi-step/layer process with a seed layer, only a single-step/layer process is used. The deposition rate of the n+ layer is approximately 10 nm/min.

Table 3.1. Process parameters for PECVD deposited films

	n+ μc-Si	a-Si:H	SiN_x:H	SiN_x:H (low temp)
Substrate Temp	250 ºC	250 ºC	250 ºC	200 ºC
Pressure	1.9 Torr	0.5 Torr	1 Torr	1.3 Torr
Power	20 W	1 W	20 W	20 W
Flow rates	PH_3: 1.0	SiH_4: 3.0	NH_3: 16	NH_3: 16
(sccm)	SiH_4: 1.0	H_2: 20	SiH_4: 4	SiH_4: 4
	H_2: 200		H_2: 200	H_2: 100

The a-Si:H film composition gases include silane diluted with hydrogen. It has been shown that a-Si films diluted with hydrogen can posses electron mobilities ~4 times larger, and lifetime-mobility products 2-3 times larger than standard a-Si films produced from silane alone [45,46]. Table 3.1 illustrates the process parameters used for the a-Si:H film deposition. Measurements on the a-Si:H film showed a minimum dark conductivity of 4×10^{-9} S/cm, and a maximum photo to dark conductivity ratio of 6.2×10^{4} for a 120 nm thick a-Si film. A bandgap of 1.85 eV was extracted using the Tauc method, along with a dark Fermi level of 0.65 eV. In addition, the hydrogen content of the film was estimated to be 15-18% [47] and the deposition rate was measured to be 5.4 nm/min.

Two recipes were used for the silicon nitride—a dense silicon nitride for the gate dielectric, and a lower-temperature silicon nitride to cap the polyimide. The silicon nitride used for the gate dielectric is designed to ensure a high electric field breakdown, low leakage current, low density of interface traps which leads to high TFT mobility, and good uniformity over an area large enough to produce a prototype 64x64 pixel imaging array. For our nitride, we measured a breakdown electric field of more than 5 MV/cm, a relative permittivity of 7.6, a uniformity is ±2.9% over an area of 22.8 cm^2, an etch rate of 14nm/min in buffered hydrofluoric acid solution (BHF), a refractive index of 1.96, and a leakage current of less than 0.3 fA/μm of gate width at gate voltages of 20V. The deposition rate was measured to be 13.1 nm/min.

The silicon nitride layer that caps the polyimide functions to protect the softer underlying polyimide layer from the atmosphere (prior to a-Se deposition). In addition, the process is required to be low-temperature so that it does not further cure the polyimide or adversely affect underlying TFTs by acting as a high temperature anneal leading to hydrogen devolution from underlying films. The deposition rate was measured to be 15 nm/min. Table 3.1 lists the process parameters used for both silicon nitride films.

For our process, polyimide was chosen as the interlayer dielectric between the TFTs and the bottom contact/electrode of the a-Se photoconductor. In order to achieve close to 100% effective fill factor, the geometrical fill factor (actual area) of the bottom a-Se electrode needs to be approximately 60% or greater. Thus, in order to minimize the parasitic capacitances between the bottom electrode and the underlying TFTs, the capacitance of the dielectric layer should be minimized. In addition, as will be seen in the next chapter, minimizing this capacitance also plays an important role in reducing the total input referred noise of the pixel. The capacitance can be minimized by choosing a dielectric layer with a low relative permittivity and/or a large film thickness. Silicon nitride is a poor choice on both counts, since it has a relatively high permittivity of approximately 7.5, and depositing thick layers (>1μm) of silicon nitride by PECVD are very difficult due to the high film stresses. Instead, we chose to use a low-stress, low moisture uptake polyimide (PI-2611) manufactured by HD MicroSystems with a relative permittivity of 2.9 and the ability to deposit layers as thick as 8 μm. Our measured polyimide thickness was 3.1 μm, and the relative permittivity was 3.6.

The a-Se photoconductor and top metal electrode layers were evaporated onto the completed TFT array by Anrad Corp. of Montreal. The a-Se layer has a thickness of 1mm in order to effectively stop the 70 kVp fluoroscopy X-rays. Finally, a high voltage encapsulation layer is deposited over the top metal electrode in order to prevent arcing which could otherwise damage equipment or pose personal safety risks.

In order to improve the TFT array device performance, further attempts were made at fabricating TFT arrays at the University of Waterloo, leading to additional material characterization. The modified fabrication process parameters are described in Appendix A.

3.2 TFT Design

A top gate TFT design structure was chosen in order to remove the need for a separate metal shield over the TFT channel layers. The bottom electrode of the a-Se layer can act as a second (top) gate in the case where bottom gate TFTs are used. This second gate can partially turn on the readout transistors (a parasitic back channel forms which degrades the TFT leakage characteristics) corrupting the desired readout signal. A non-overlapped (bottom electrode does not fully overlap the pixel) structure is used to minimize parasitic capacitance between the bottom electrode and the control/data lines and TFTs. A downside of using top gate TFTs is that they are less prevalent in industry, and for in-house fabrication they pose considerable challenges with respect to minimization of contact resistance between the source/drain metals and the a-Si channel layer.

The TFT design incorporates a double gate/interlayer nitride in order to decrease the number of process steps through the elimination of an additional interconnect metal layer. With a double nitride layer, the gate metal can also be used as an interconnect metal to the underlying source/drain metal. The disadvantage of using a double gate nitride is in the reduced flexibility for the interlayer dielectric thickness, which is limited by the desired gate nitride thickness. This reduced flexibility means less control over the parasitic capacitances arising from crossing source/drain and gate metal lines.

In designing the TFT layers, appropriate layer thicknesses should be chosen in order to optimize the TFT performance. The source-drain metal and n+ layer thickness are chosen to be relatively thin at 60nm primarily to prevent step coverage problems with respect to the overlying a-Si layer, while being thick enough to give sufficient conductivity. Based on in-house experiments, a 70 nm a-Si layer was determined to be near optimal thickness for a gate length of 10 μm, which coincides well with previously published reports [48]. The silicon nitride gate dielectric thickness was chosen small enough in order to provide current in the

range of microamperes with moderate W/L values and gate overdrive voltages as well as to prevent excessive mechanical stress in the film, while at the same time being large enough to prevent pinholes in the dielectric and to allow for sufficient distance between overlapping metal layers (to reduce parasitic capacitances). Layer thicknesses for the implemented TFT process are shown in Table 3.2.

Table 3.2. TFT Process Parameters for APS Array

TFT Process Parameters	Value
Gate/Source-Drain overlap	5 μm
Source/Drain metal thickness	60 nm
N+ layer thickness	60 nm
Amorphous Silicon layer thickness	70 nm
Gate nitride thickness	250 nm
Gate Metal thickness	250 nm
Isolation polyimide thickness	3 μm
Isolation nitride thickness	200 nm
Bottom metal electrode thickness	650 nm
a-Se thickness	1 mm

Gate/source-drain overlap lengths of 5 μm were chosen to allow for successful alignment on the equipment available in the in-house cleanroom, as well as to prevent current crowding (which causes effective carrier mobility degradation) [48].

A guard ring that surrounds the pixel array was designed in the metal #3 layer (top metal layer) with a minimum width of 3.4mm. The purpose of the guard ring is to attract any charges outside the pixel area that are created within the a-Se layer in order to prevent "blooming" of the outer array pixels.

3.3 Mask Design

The TFT array is fabricated using a six-mask process on a 4 inch diameter, 0.7mm thick, 1737 Corning glass substrate. Five inch chrome masks were designed using Cadence Virtuoso and fabricated at the nanofabrication facility of the University of Alberta. Table 3.3 lists the masks steps with a brief description of their function.

Table 3.3. Mask steps for TFT array fabrication

Mask Number	Function	Description
1	Pattern metal #1 and n+ layers	Define source-drain contacts; output and VDD lines
2	Pattern a-Si and SiN_x #1 layers	Define TFT islands
3	Via #1	Interconnect opening between metal #1 and metal #2
4	Pattern metal #2	Define gate metal, interconnect metal, and READ and RESET lines
5	Via #2	Interconnect opening between metal #2 and metal #3
6	Pattern metal #3	Define a-Se bottom electrode, guardring, and bondpads

The individual masks are shown in Appendix B. The layout of a single pixel within the 64×64 pixel prototype array is shown in Figure 3.2. The die micrograph of a 2×2 region of the 64×64 a-Si APS X-ray imaging array is shown in Figure 3.3. The bottom right pixel of the figure shows the full TFT process up to and including the bottom photoconductor electrode, while the other pixels only show the process up to the gate metal in order that the underlying TFTs are visible. Each pixel contains 4 TFTs, namely AMP, RDC, RDP, and RESET, with W/L ratios of 40μm/10μm for all TFTs except for RESET which has a W/L ratio of 20μm/10μm. Device dimensions for AMP and RDC were chosen in order to minimize the input referred noise of the APS circuit while trying to maintain a small pixel area. The pixel dimensions are $250\times250\mu m^2$ and the geometric fill factor is 57%.

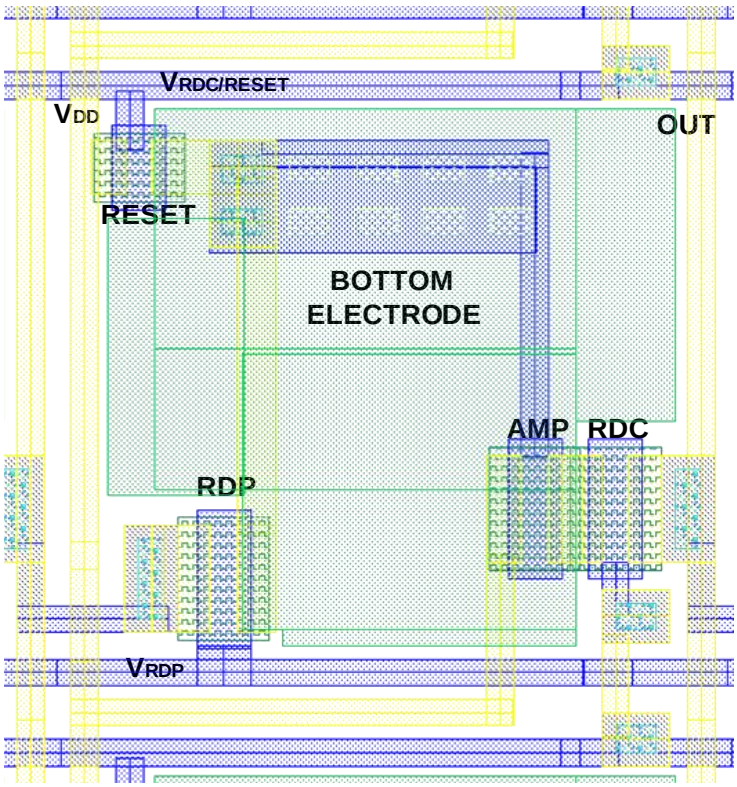


Figure 3.2. Layout of single pixel within 64×64 pixel array.

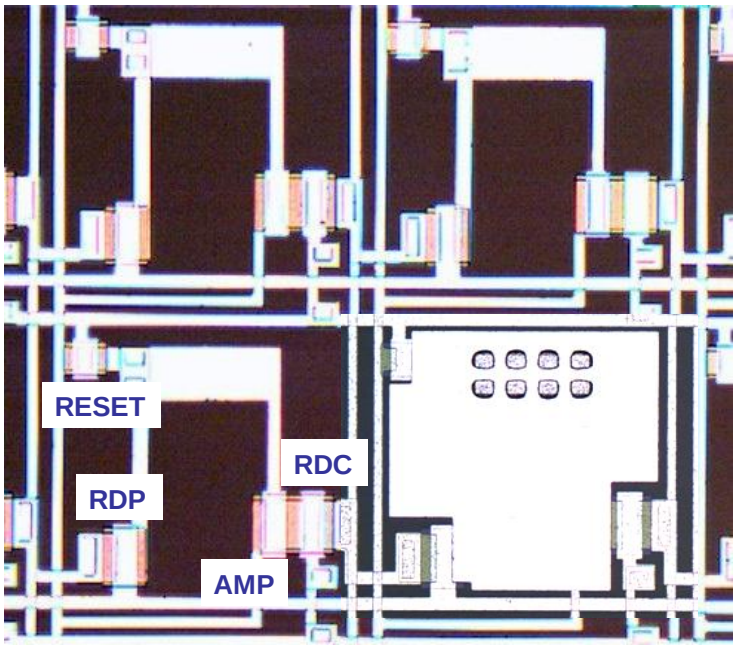


Figure 3.3. Die micrograph of APS imager with and without bottom photoconductor electrode

The fabricated 64×64 a-Si APS pixel array is shown in Figure 3.4. A guard ring surrounds the array and the charge amplifier and gate driver pads are below and to the left of the array respectively.

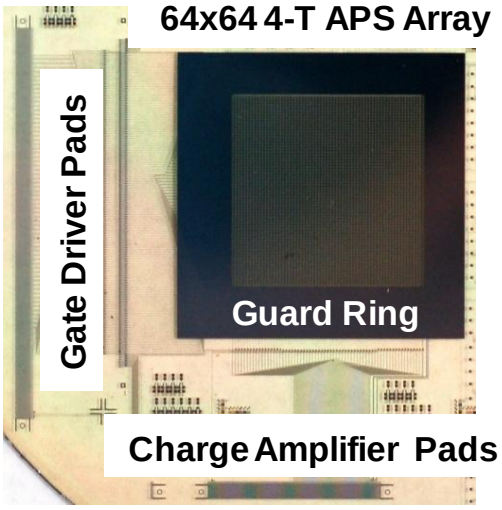


Figure 3.4. In house 64 x 64 pixel imaging array

3.4 Fabrication Steps

The main fabrication steps required for the 64 x 64 pixel imaging array are shown in Table 3.4. All plasma enhanced dry etching was performed in a reactive ion etcher (RIE) with the following characteristics: electrode diameter 23cm, electrode spacing 2.54cm (1”).

The n+ µc-Si film was dry etched using XeF_2 gas instead of using the RIE in order to prevent plasma damage to the sensitive interface. The wafer was placed in a glass petri dish to reduce turbulence (due to opening and closing of the process chamber valve) and hence reduce/prevent non-uniform etching of the sample. The gas pressure was set at 1Torr and the sample was exposed to seven 10s gas pulses. Given that etching with gas is an isotropic etch process (unlike dry etching in an RIE) and somewhat difficult to control, an overetch of approximately 1.8 µm was noticed. In order to limit the amount of overetch, several pieces of crystalline silicon wafer were placed into the glass petri dish alongside the process wafer. Overetch of the n+ film with the added silicon pieces was not visible.

For the polyimide used in the process, the manufacturer's instructions call for the last bake to be at 350 °C for 30 minutes in order to complete crosslinking of the polymer chains; however, we were forced to cure at a lower temperature of 250 °C in order to not damage the underlying TFTs. As a result, our final cure was for a longer period of time (1.5 hours) [49].

Table 3.4. Fabrication steps for TFT array fabrication

Step Number	Procedure	Description
1	Clean 4" round 0.7mm thick Corning 1737 glass wafers	RCA1 clean, dry with N_2 gun
	MASK 1: Define source-drain contacts; output and VDD lines	
2	Sputter aluminum	DC sputter aluminum, pump chamber below 1.5 µTorr, deposition pressure 4.5mT
3	PECVD n+ µc-Si	See Table 3.1
4	Spincoat photoresist (PR)	Shipley 1813 PR, 4000rpm spin, 30s
5	Softbake PR	13 min @ 100 °C in oven, or 90s @ 100 °C on hotplate
6	Pattern PR	UV exposure, 9 sec; Shipley MF-319 developer, 30 sec
7	Dry etch n+ µc-Si	XeF_2 gas chamber,1Torr, 10s pulse, 7 pulses.
8	Wet etch aluminum	Transene Al etchant, ~15s @ 45 °C
9	Remove PR	Soak in acetone 3 min, rinse with fresh acetone, rinse IPA, dry with N_2 gun, dry 30s @ 120 °C in oven , ASH: 100mT, 50W, 30 sccm O_2, 30 sec
10	Remove surface oxide	HF dip in 50:1 ($HF:H_2O$) for 5s, DI water rinse, dry with N_2 gun, dry 30s @ 120 °C in oven
	MASK 2: Define TFT islands	
11	PECVD a-Si:H	See Table 3.1
12	PECVD SiN_x:H	See Table 3.1
13	Spincoat photoresist (PR)	Shipley 1813 PR, 4000rpm spin, 30s
14	Softbake PR	13 min @ 100 °C in oven, or 90s @ 100 °C on hotplate

15	Pattern PR	UV exposure, 11 sec; Shipley MF-319 developer, 30 sec
16	Dry etch a-Si:H, SiN_x:H, n+ µc-Si	RIE: 100mT, 100W, 50sccm CF_4, 5sccm O_2, 4m30s
17	Remove PR	Soak in acetone 3 min, rinse with fresh acetone, rinse IPA, dry with N_2 gun, dry 30s @ 120 °C in oven , ASH: 100mT, 100W, 30 sccm O_2, 4 min
	MASK 3: Interconnect opening between metal #1 and metal #2	
18	PECVD SiN_x:H	See Table 3.1
19	Spincoat photoresist (PR)	Shipley 1813 PR, 4000rpm spin, 30s
20	Softbake PR	13 min @ 100 °C in oven, or 90s @ 100 °C on hotplate
21	Pattern PR	UV exposure, 12 sec; Shipley MF-319 developer, 35 sec
22	Dry etch SiN_x:H	RIE: 100mT, 100W, 50sccm CF_4, 5sccm O_2, 3m30s
23	Remove PR	Soak in acetone 3 min, rinse with fresh acetone, rinse IPA, dry with N_2 gun, dry 30s @ 120 °C in oven , ASH: 100mT, 100W, 30 sccm O_2, 4 min
	MASK 4: Define gate metal, interconnect metal, and READ and RESET lines	
24	Sputter aluminum	DC sputter aluminum, pump chamber below 1.5 µTorr, deposition pressure 4.5mT
25	Spincoat photoresist (PR)	Shipley 1813 PR, 4000rpm spin, 30s
26	Softbake PR	13 min @ 100 °C in oven, or 90s @ 100 °C on hotplate
27	Pattern PR	UV exposure, 9 sec; Shipley MF-319 developer, 35 sec
28	Wet etch aluminum	Transene Al etchant, ~1 min @ 45 °C
29	Remove PR	Soak in acetone 3 min, rinse with fresh acetone, rinse IPA, dry with N_2 gun, dry 30s @ 120 °C in oven , ASH: 100mT, 100W, 30 sccm O_2, 4 min
	MASK 5: Interconnect opening between metal #2 and metal #3	

30	Spincoat polyimide (PI)	Spin at 500 rpm for 5s, ramp to 7000 rpm in 20 sec, leave at 7000 rpm for 30 sec
31	Cure PI	4 min at 80°C + 3 min at 150°C, ramp to 250°C at 240 °C/h, set timer at 2 hours, allow to cool to room temp
32	PECVD SiN_x:H (low temp)	See Table 3.1
33	Spincoat photoresist (PR)	Shipley 1827 PR, 1800rpm spin, 30s
34	Softbake PR	20 min @ 100 °C in oven
35	Spincoat photoresist (PR)	Shipley 1827 PR, 1800rpm spin, 30s
36	Softbake PR	20 min @ 100 °C in oven
37	Pattern PR	UV exposure, 99 sec; Shipley MF-319 developer, 4 min
38	Hardbake PR	10 min @ 120 °C in oven
39	Dry etch SiN_x:H	RIE: 100mT, 100W, 50sccm CF_4, 5sccm O_2, 4min
40	Dry etch PI	RIE: 100mT, 250W, 10sccm CF_4, 50sccm O_2, 20min
41	Remove PR	Soak in acetone 3 min, rinse with fresh acetone, rinse IPA, dry with N_2 gun, dry 30s @ 120 °C in oven , ASH: 100mT, 100W, 30 sccm O_2, 5 min
	MASK 6: Define a-Se bottom electrode, guardring, and bondpads	
42	Sputter aluminum	DC sputter aluminum, pump chamber below 1.5 μTorr, deposition pressure 4.5mT
43	Spincoat photoresist (PR)	Shipley 1813 PR, 4000rpm spin, 30s
44	Softbake PR	13 min @ 100 °C in oven, or 90s @ 100 °C on hotplate
45	Pattern PR	UV exposure, 9 sec; Shipley MF-319 developer, 30 sec
46	Wet etch aluminum	Transene Al etchant, ~2 min @ 45 °C
47	Remove PR	Soak in acetone 3 min, rinse with fresh acetone, rinse IPA, dry with N_2 gun, dry 30s @ 120 °C in oven , ASH: 100mT, 100W, 30 sccm O_2, 4 min

3.5 TFT Parameter Characterization and Extraction

TFT characterization involved three main sets of tests from which all TFT parameters were extracted: drain current versus drain voltage (I_D-V_D), drain current versus gate voltage (I_D-V_G), and quasi-static capacitance voltage (QSCV). An Agilent 4156C or an Agilent 4155C semiconductor parameter analyzer (SPA) was used in conjunction with a Signatone triaxial probe station for TFT characterization. Unless otherwise stated, all figures presented were obtained using a 4155C SPA at the University of Waterloo. Measurements made with the 4156C SPA were performed at Simon Fraser University.

I_D-V_D characteristics are presented in Figure 3.5 and Figure 3.6 for TFTs with W/L ratios of 100µm/10µm and 100µm/50µm, respectively. Both curves show a small dip near low VD indicating a non-negligible source-drain contact resistance to the a-Si channel.

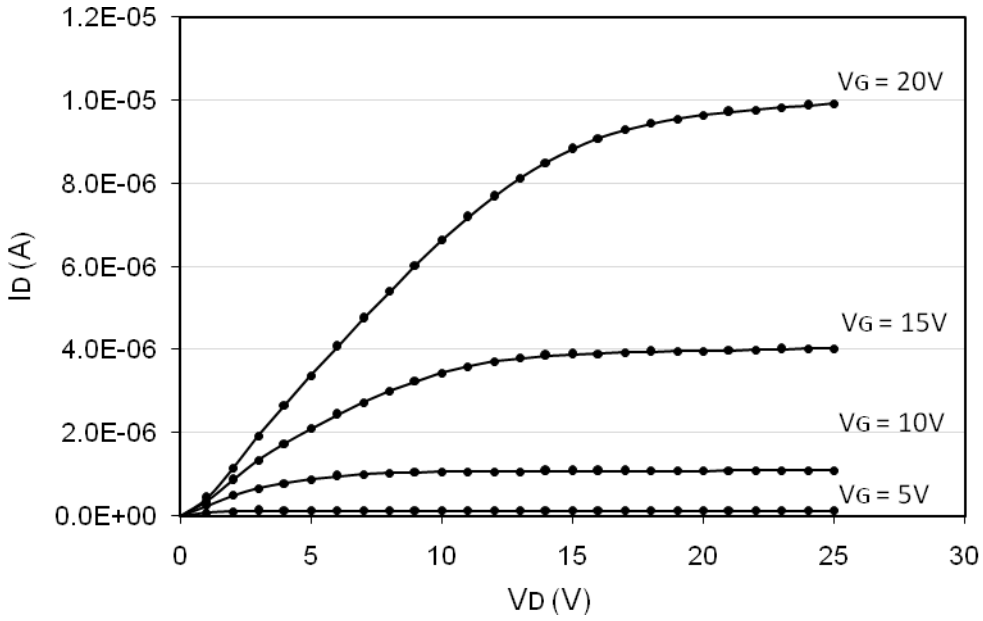


Figure 3.5. I_D-V_D curve for fabricated a-Si TFT, W/L = 100µm/10µm

I_D-V_G characteristics are presented in Figure 3.7 and Figure 3.8 for TFTs with W/L ratios of 100µm/10µm and 100µm/50µm respectively. Because the 4155C SPA that was used had a limitation on low-current detection of about 1-10pA, it was not possible to extract the

ON/OFF ratio, or leakage currents from these curves. A 4156C SPA had previously been used to measure the same devices as shown in Figure 3.9. An ON/OFF ratio of 6.4 x 10^7 was measured at a drain voltage of 11 V for the device with a W/L of 100µm/50µm. Drain off currents were on the order of 50fA, and gate leakage currents were typically 30 fA or less, including at gate voltages greater than 20V. Values of ON/OFF ratios were higher for TFTs with smaller gate lengths due to larger ON currents. For instance, an ON/OFF ratio of 1.13 x 10^8 was measured for a TFT with W/L = 100µm/30µm.

The field effect mobility, μ_{eff}, is extracted in both the linear (V_{DS}=1V) and saturation (V_{DS}=V_{GS}) regimes from the slope of normalized drain current with respect to the gate voltage. The x-intercept of the straight line approximation of the slope gives the threshold voltage, V_T [50]. Figure 3.10 illustrates extracted mobility and threshold voltage from a device in saturation with W/L = 100µm/50µm.

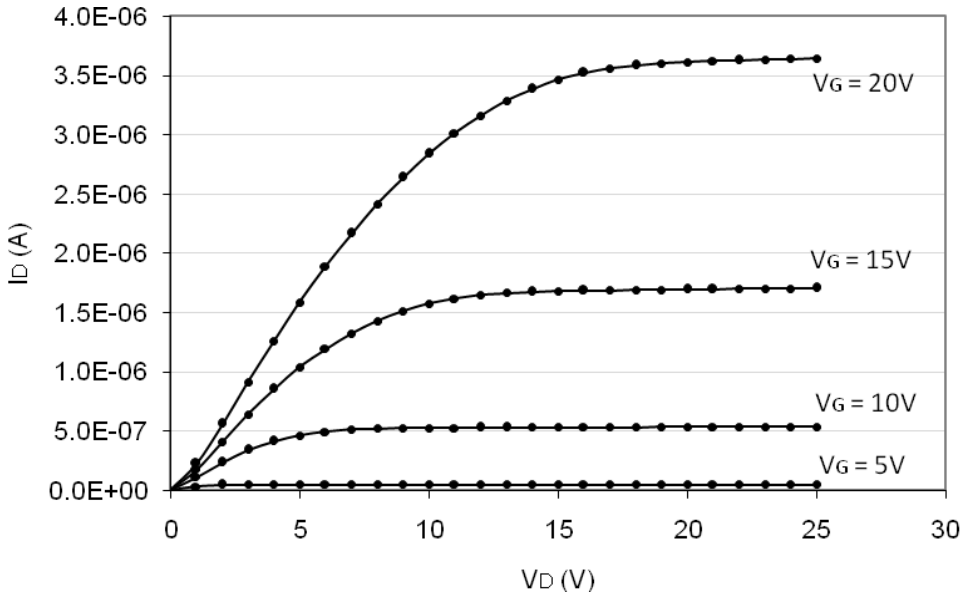


Figure 3.6. I_D-V_D curve for fabricated a-Si TFT, W/L = 100µm/50µm

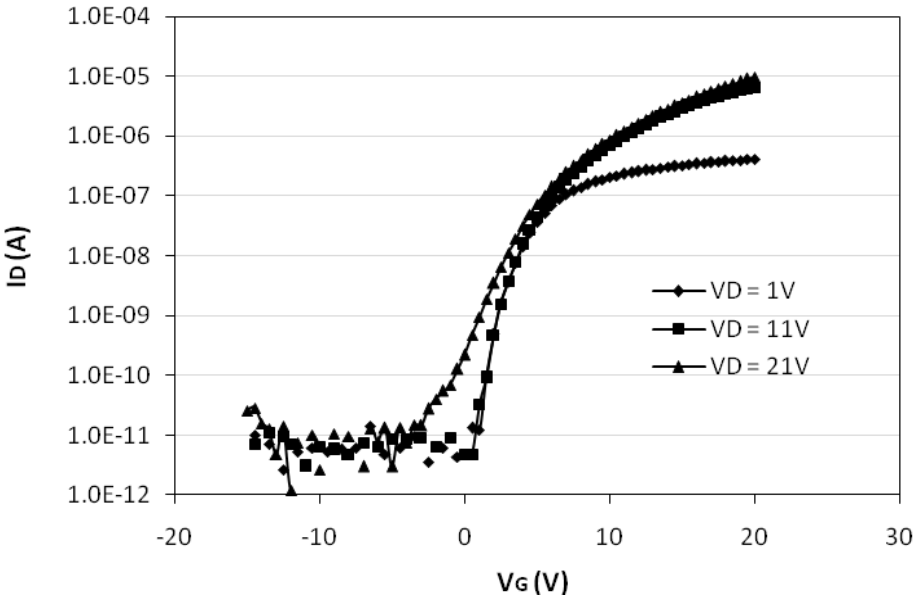


Figure 3.7. I_D-V_G curve for fabricated a-Si TFT, W/L = 100µm/10µm

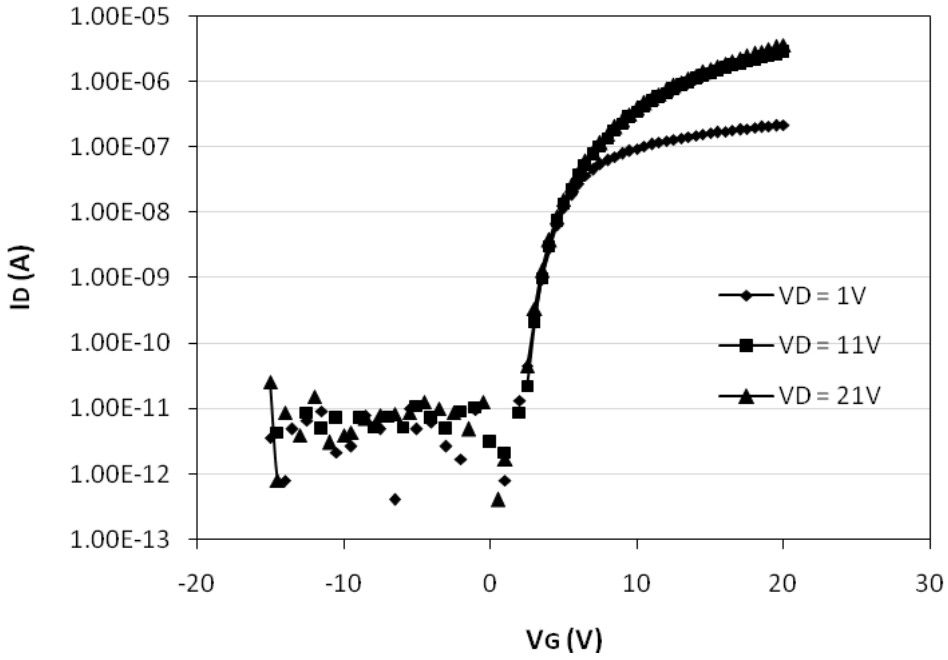


Figure 3.8. I_D-V_G curve for fabricated a-Si TFT, W/L = 100µm/50µm

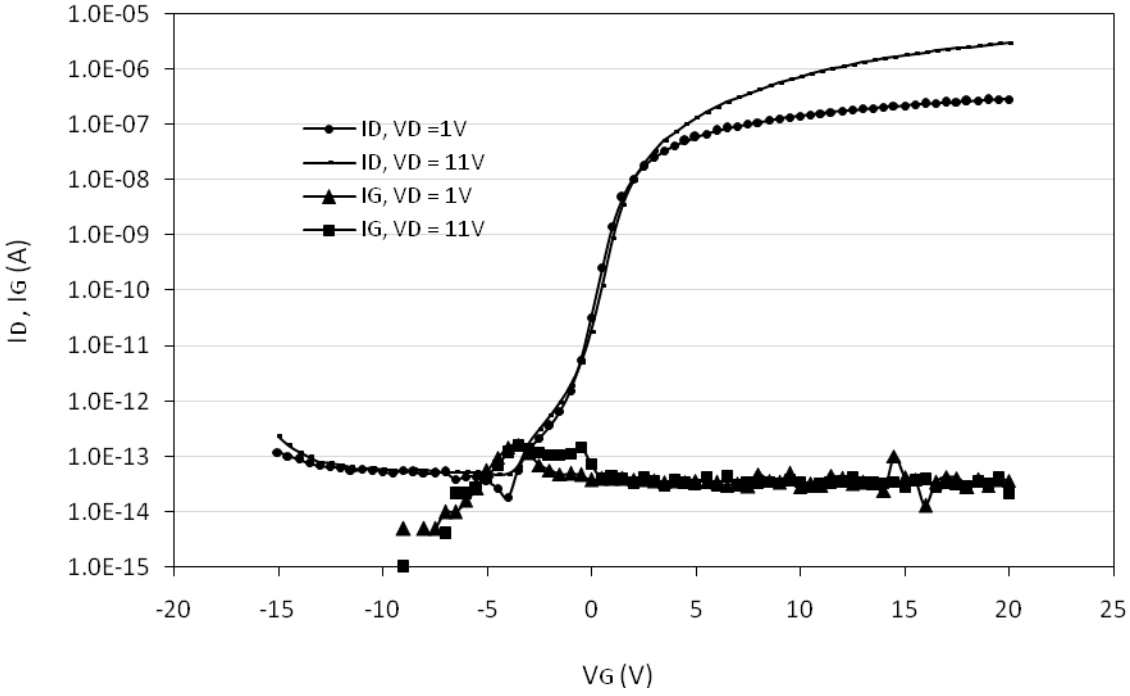


Figure 3.9. I_D,I_G-V_G curve using HP4156C SPA for fabricated a-Si TFT, W/L = 100µm/50µm

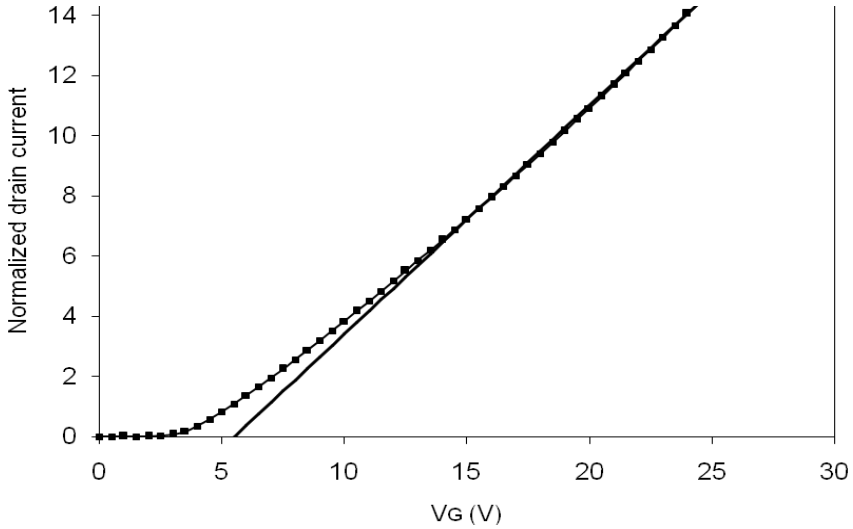


Figure 3.10. Extraction of $\mu_{eff,sat}$ and $V_{T,sat}$ from TFT with W/L = 100µm/50µm

As can be seen in Figure 3.10, the slope of the normalized drain current curve, and hence the mobility, is not constant and is a function of the gate voltage. Similarly, the effective threshold voltage depends on the gate voltage. This dependence on gate voltage is due to the large drain-source contact resistance which, in the case of a TFT in saturation, causes a portion of the gate-source voltage to be lost across the source contact resistance. In order to determine the effective intrinsic channel field effect mobility and effective intrinsic threshold voltage absent the effects of the source-drain contact resistance we notice that the total TFT ON resistance, R_T, can be written as [50]

$$R_T = \frac{\partial V_{DS}}{\partial I_D} = r_{ch}L + 2R_{SD} = \frac{L}{\mu_{eff} C_{ox} W\left(V_{GS} - V_T - V_{DS}\right)} \tag{3.1}$$

where r_{ch} is the channel resistance per unit length and R_{SD} is the source-drain contact resistance. The slope of the plot of ON resistance versus gate length gives r_{ch}, which can be written as [50]

$$r_{ch} = \frac{1}{\mu_{effi} C_{ox} W\left(V_{GS} - V_{Ti} - V_{DS}\right)} \tag{3.2}$$

where μ_{effi} is the intrinsic channel field effect mobility and V_{Ti} is the intrinsic threshold voltage. Plotting the reciprocal of r_{ch} versus gate voltage gives μ_{effi} for the slope and V_{Ti} for the x-intercept. Using this technique we find μ_{effi} = 0.511 cm^2/Vs and V_{Ti} = 4.6 V for the above devices.

Quasi-static capacitance-voltage (QSCV) measurements are taken in order to determine the gate capacitance per unit area of the device and the relative permittivity of the gate nitride. Figure 3.11 shows a C-V curve for the device with W/L = 100µm/50µm. The ripples in the C-V curve are a result of short integration times being used in the measurement. The C-V curve shows an increase in capacitance with gate voltage since the TFT is an accumulation mode device. For gate voltages lower the ~-5V, the only capacitance measured is due to the gate to source/drain overlap capacitances, and any stray capacitances due to the measurement equipment. As the gate voltage increases and electrons fill the channel, the gate channel

capacitance is also sensed. Thus the difference between the ON and OFF capacitance values gives the gate channel capacitance.

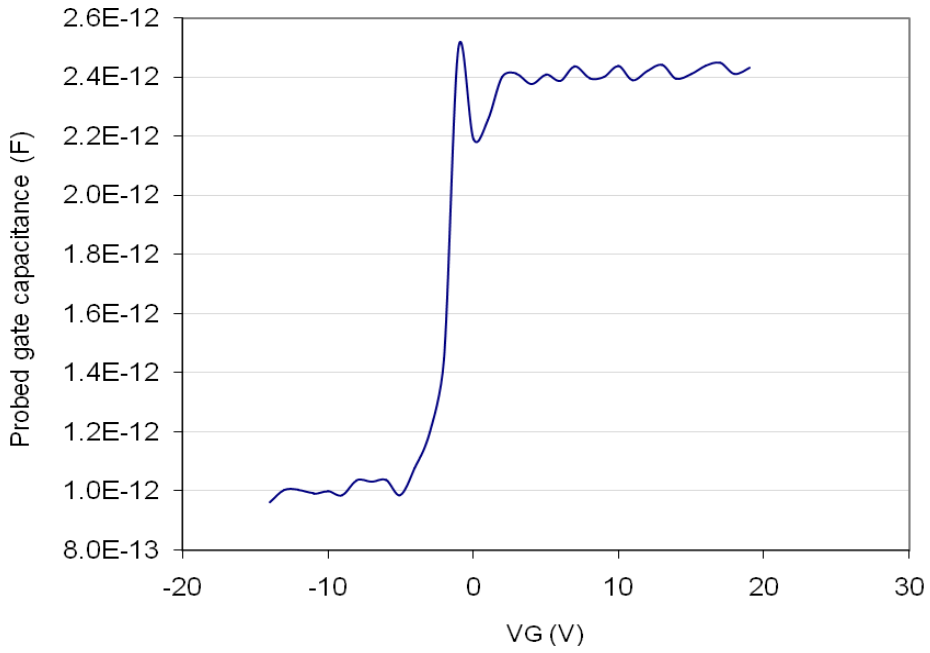


Figure 3.11. QSCV curve for fabricated a-Si TFT, W/L = 100µm/50µm

As the device dimensions decrease, fringing field capacitance tends to give a false reading for the calculated gate capacitance per unit area and hence the relative permittivity. In addition, the accuracy of the measurement decreases as the difference between ON and OFF capacitance decreases. To help alleviate this problem, we can plot the total probed gate capacitance (when the TFT is ON) versus gate length for a fixed gate width of W = 100µm as shown in Figure 3.12. The slope of the best line fit gives the gate capacitance per unit length for a width of 100µm, and the x-intercept gives the fixed capitances associated with measurement equipment, the overlap capacitances, and any common fringing field capacitance. As shown in Figure 3.12, the slope of the best line fit is 2.69 x 10^{-2} pF/µm for a gate width of 100µm, which gives a C_{ox} = 2.69 x 10^{-8} F/cm^2. Given that the gate nitride thickness is ~250nm, we can calculate the relative permittivity $\varepsilon_r \sim 7.6$.

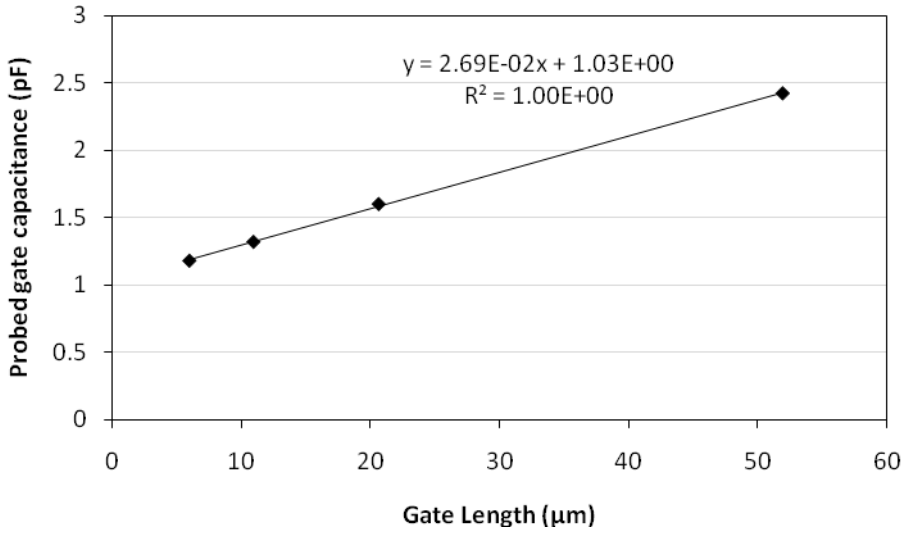


Figure 3.12. Probed gate capacitance versus gate length for fabricated TFTs

The subthreshold slope, *SS*, is defined as the voltage required to increase the drain current by a factor of 10, and is given by [50]

$$SS = dV_G/d(\log I_D) \tag{3.3}$$

From the straight line approximation of the maximum slope in the transfer curve of Figure 3.7 and Figure 3.8 the *SS* is calculated to be 0.692 V/decade and 0.515 V/decade, respectively. From the subthreshold slope the density of interface traps, D_{it}, can be calculated using [50]

$$D_{it} = \left(\frac{SS \log(e)}{kT/q} - 1 \right) \frac{C_{ox}}{q} \tag{3.4}$$

where C_{ox} is the gate capacitance per unit area (F/cm^2), k is Boltzmann's constant, q is electron charge, and T is the tempeature in Kelvins. Using the above calculated *SS*, this gives us a range of 1.33 x 10^{12} to 1.85 x 10^{12} for D_{it}.

Note that for all calculations actual measured values for device dimensions were used as opposed to the device dimensions drawn on the masks.

4 Noise and DQE

In the first section of this chapter, the various electronic noise sources considered in our circuit noise model are briefly introduced. We next develop a noise model for our pixel, up to and including the charge amplifier readout, and simulate the total input referred noise. Next, we optimize the pixel TFT device dimensions for low noise performance. Finally, we simulate the effect of varying electronic noise and incident X-ray exposure on the DQE of an imaging system using an a-Se photoconductor for fluoroscopy applications.

4.1 Electronic Noise Background

In this section, we concentrate on those noise sources which have their source in the random motion of the atomic constituents of the matter comprising the circuit devices used. Macroscopically observable physical phenomena, such as electrical current, are not continuous, but are only averages over a large number of particles. When observed precisely, the random nature of the current manifests as fluctuations about an average value. The sections that follow describe the different types of electronic noise which arise due to the different atomic level phenomena within the devices used.

4.1.1 Shot Noise

Shot noise was first described by Walter Schottky in 1918 through his work with vacuum tubes. Shot noise is always associated with direct current flow, or in other words, the electrical carriers which are the source of the shot noise must be constrained to flow in only one direction past some observation point [51]. The charge carriers entering the observation point must do so randomly and independent of any other carriers crossing this point, and such are described by Poisson statistics. If the charge carriers are not constrained in this manner, then the shot noise will not be observed and instead thermal noise will dominate [52]. A physical system where shot noise is observed is a *pn* junction. Due to the energy barrier that exists in the depletion layer of a *pn* junction, carriers are confined to travel in only one direction. Other devices where shot noise is observed include MOSFETs in the subthrehsold region, BJTs, and vacuum tubes.

Shot noise follows Poisson counting statistics, and it has a current power spectral density described by

$$S_I(f) = 2qI\left[\frac{\sin(\pi f\tau)}{\pi f\tau}\right]^2 \tag{4.1}$$

Here the cutoff frequency is at $f=1/\tau$, q is the electric charge in Coulombs, and I is the average current. In the case of *pn* junction, τ is the transit time associated with the charge carriers crossing the depletion region (e.g. 10ps), giving a cutoff frequency of 100 GHz. Thus, the power spectral density of shot noise is white for most frequencies of interest. In addition, the amplitude distribution is Gaussian.

4.1.2 Thermal Noise

Thermal noise in electronic devices is the result of the random motion of charge carriers in thermal equilibrium with the crystal lattice. Einstein first predicted that the Brownian motion of charge carriers would cause a voltage across the ends of a resistance in thermal equilibrium in 1906. In 1928, Johnson first observed thermal noise, whose spectral density was then formulated by Nyquist in the same year [52]. Thermal noise has a white noise spectrum for most frequencies of interest with the current power spectral density given as:

$$S_I(f) = \frac{4kT}{R} \tag{4.2}$$

Where k is Boltzmann's constant, T is the absolute temperature, and R is the resistance.

In the early 1960s, the thermal noise current power spectral density in long channel MOSFETs was formulated by Van der Ziel as follows [53]:

$$S_I(f) = (\gamma)4kTg_{ds0} \tag{4.3}$$

Here γ is a scale factor of 1 or 2/3 depending on whether the device is in linear regime or saturation regime respectively, g_{ds0} is the zero drain bias channel conductivity, k is Boltzmann's constant, T is the absolute temperature. We can rewrite (4.3) in the saturation and linear regimes as:

$$S_I(f) = \frac{8}{3} KTg_m \tag{4.4}$$

$$S_I(f) = \frac{4KT}{r_{ds2}} \tag{4.5}$$

The above equations for long channel MOSFETs can be used with a-Si TFTs with reasonable accuracy.

4.1.3 Flicker or *1/f* Noise

The *1/f* noise is a random, non-stationary process observed in many physical systems and described by the shape of its power spectral density, *S(f)* given by [54]

$$S(f) = \frac{k}{|f|^{\gamma}} \tag{4.6}$$

Where k is a constant and γ is a value between 0 and 2, usually close to 1.

Being non-stationary implies that *1/f* noise is a process with memory in that past events affect present behaviour. The *1/f* noise has been observed in a variety of physical phenomenon including: the voltage and current in vacuum tubes, transistors and diodes; the resistance of semiconductors, metallic thin-films, and aqueous ionic solutions; the weather: average rainfall, average temperatures; the voltage across nerve membranes; the loudness and pitch of music. Being so ubiquitous has led some researchers to believe that there exists some profound law of nature that applies to all non-equilibrium systems and results in *1/f* noise.

From (4.6) we can see that integrating the power spectral density down to zero frequency will lead to infinite noise power (noise variance). This has lead researchers to examine if the

shape of the noise spectrum holds for very low frequencies, since if the shape flattens at low frequencies, the integral would converge. One group of researchers measured the *1/f* noise in MOSFETs down to $10^{-6.3}$ Hz or l cycle in 3 weeks. Another group, using geological techniques, measured the *1/f* noise in weather data down to $l0^{-10}$ Hz or 1 cycle in 300 years. In both cases, no change in the shape of the power spectral density at low frequencies was observed [54]. In practice, this is not a problem because most observations of flicker noise do not last very long and because flicker noise is a non-stationary process.

A model for *1/f* noise in semiconductors was first described by McWhorter in 1955. Referred to as the carrier number fluctuation model, McWhorter attributed the *1/f* noise observed to fluctuations in the number of majority carriers that get trapped and released in the slow surface states between the oxide and semiconductor. This model has been useful in predicting the *1/f* noise in surface channel devices such as MOSFETs [54, 55].

Hooge noticed that the mechanism to describe the origin of *1/f* in MOSFETs was not universal, as his work with aqueous ionic solutions that have no surface traps and where the concentration of carriers is constant also revealed the presence of *1/f* noise. Hooge postulated that the origin of the *1/f* noise was not due to fluctuations in the number of carriers, but instead due to the fluctuations in the mobility of the carriers within the bulk [55].

Current noise spectral densities for the carrier number fluctuation model (McWhorter, Δn) and the carrier mobility fluctuation model (Hooge, $\Delta\mu$) for TFTs in the linear and saturation regime are shown in Table 4.1.

Table 4.1. *1/f* noise spectral densities for McWhorter and Hooge models in TFTs

	Δn model	$\Delta\mu$ model
$S_{I(lin)}(f)$	$\frac{k^* \mu_{eff}^2 W V_{DS}^2}{f L^3}$	$\frac{\alpha_H q \mu_{eff}^2 C_{ox} W (V_{GS} - V_T) V_{DS}^2}{f L^3}$
$S_{I(sat)}(f)$	$\frac{k^* \mu_{eff}^2 W V_{DS} (V_{GS} - V_T)}{2 f L^3}$	$\frac{\alpha_H q \mu_{eff}^2 C_{ox} W (V_{GS} - V_T)^3}{2 f L^3}$

Here k^* is a parameter that takes into account the electron tunnelling between insulator traps near the interface and the conducting channel. Also, α_H, referred to as the Hooge parameter, is a constant for a given technology and can be considered a quality indicator.

While McWhorter's model is useful for describing MOSFETs, it has proved less useful for a-Si TFTs where the charge carrier concentrations are lower. Instead, experiments by Rigaud, Rhayem and Valenza have shown the Hooge model to agree well with measured *1/f* noise in a-Si TFTs with a Hooge parameter of $1\text{x}10^{-2}$, a value two to three orders of magnitude larger than values obtained in crystalline silicon MOSFETs [56-58].

Interestingly, in poly-Si TFTs, the measured *1/f* noise appears to follow a mixture between the Hooge and McWhorter models (though more closely aligned with the McWhorter model) [57, 59-62]. This is not entirely surprising since poly-Si TFTs can lie somewhere between a-Si and c-Si transistors in terms of their structural composition and performance. One could speculate that *1/f* noise results from both carrier and mobility fluctuations, but depending on the structure, one noise source may dominate over the other.

4.1.4 Reset or *kTC* Noise

When charge is transferred through a switch onto a capacitor, there is some uncertainty as to the final amount of charge on the capacitor. This uncertainty in charge is due to the random thermal motion of charge on the capacitor, and once the switch is open, the charge on the capacitor is frozen. If the same procedure were repeated multiple times, the variance in the amount of charge on the capacitor would be *kTC*, where *k* is Boltzmann's constant, *T* is absolute temperature, and *C* is capacitance. From thermodynamic equilibrium principles, the thermal energy per degree of freedom is $\frac{1}{2}kT$. If we equate the thermal energy with the energy on a capacitor, we have:

$$\frac{1}{2}CV^2 = \frac{1}{2}C\left(\frac{Q}{C}\right)^2 = \frac{1}{2}kT, \quad Q^2 = kTC \text{ or } V^2 = \frac{kT}{C} \tag{4.7}$$

It has been shown that reset noise can be larger than that given by *kTC* in some cases. For medical imaging applications, and for small pixel capacitances, it has been shown that a charge variance of *kTC* is a good approximation [63].

In the next section, a thorough noise analysis will be performed on the C-APS portion of the M-APS. We will ignore the noise of the PPS circuit since it has been thoroughly examined previously [18,33,34], and only the C-APS portion of the circuit will be used in the low-noise regime.

4.2 C-APS Noise Model

We will consider the following noise sources for a direct conversion imaging system: photodetector shot noise, transistor leakage noise, reset (*kTC*) noise, circuit thermal noise, circuit flicker noise, data line noise, and charge amplifier noise. The small signal circuit noise model used for this analysis is shown in Figure 4.1. We have two additional blocks in Figure 4.1 not shown in the circuit diagram of Figure 2.4 which shape our output noise spectrum, namely $H_{LPF}(\omega)$ and $W(\omega)$, which represent a low-pass filter and a double-sampling (DS) operation respectively.

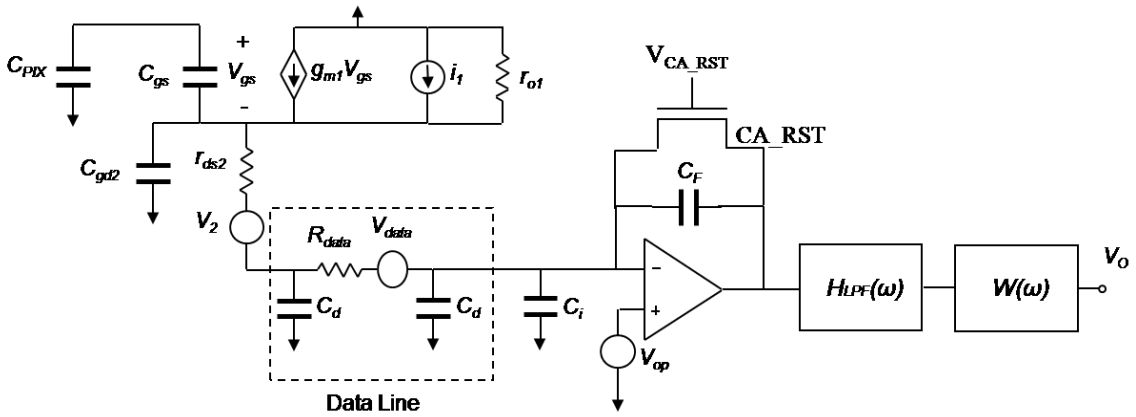


Figure 4.1. Small-signal circuit for noise analysis.

The low-pass filter single pole power spectral transfer function is given by:

$$H_{LPF}^2(\omega) = \frac{1}{1+\omega^2\beta^2} \tag{4.8}$$

where β is the low-pass filter time constant. The effect of the low-pass filter is to limit the bandwidth in order to reduce the thermal noise of the system. Since the integrator itself acts as a low-pass filter, an additional external low-pass filter is often not necessary. The integrator, in practice, does not behave as a continuous time filter since it is constantly being reset by transistor CA_RST. The charge amp is open for the integration period, T_{int}. Finding the frequency response to a pulse of width T_{int} gives us the following low-pass filter transfer function for the integrator. [64, 65]

$$H_{LPF}(\omega) = T_{\text{int}} e^{-j\omega T_{\text{int}}/2} \frac{\sin\left(\frac{\pi\omega}{\omega_{\text{int}}}\right)}{\left(\frac{\pi\omega}{\omega_{\text{int}}}\right)} = T_{\text{int}} e^{-j\omega T_{\text{int}}/2} \text{sinc}\left(\frac{\pi\omega}{\omega_{\text{int}}}\right) \tag{4.9}$$

where $\omega_{int} = 2\pi/T_{int}$. The above filter essentially behaves as a first order low pass filter with a time constant $\beta = T_{int}/2\pi(0.44)$. The power spectral transfer function of the integrator is found by taking the square of the magnitude of the transfer function and is given by

$$H_{LPF}^2(\omega) = \left| T_{\text{int}} e^{-j\omega T_{\text{int}}/2} \frac{\sin\left(\frac{\pi\omega}{\omega_{\text{int}}}\right)}{\left(\frac{\pi\omega}{\omega_{\text{int}}}\right)} \right|^2 = T_{\text{int}}^2 \text{sinc}^2\left(\frac{\pi\omega}{\omega_{\text{int}}}\right) \tag{4.10}$$

The double sampling operation power spectral transfer function is given loosely by[2] [18]

$$W^2(\omega) = 2\{1-\cos(\omega\tau)\} \tag{4.11}$$

where τ is the double sampling separation time (the time between the signal and reset samples). The double sampling operation not only removes fixed pattern noise from the circuit, but it also has a noise shaping effect that can reduce low-frequency flicker noise.

[2] For a more detailed and accurate derivation of the transfer function for double sampling, see Appendix C

For an a-Se photoconductor, the associated dark current shot noise is given by

$$q_{a-Se} = \sqrt{\frac{A_{ph} J_{a-Se,dark} T_F}{q}} \tag{4.12}$$

where T_F is the frame time and A_{ph} is the effective photoconductor area per pixel. The dark current noise density, $J_{a\text{-}se,dark}$, has been given as 1 pA/mm^2 at an electric field of 10 V/μm [4,17], though values as low as 7 fA/mm^2 have been reported for thick a-Se photoconductor layers at an electric field of 14 V/μm [18]. For the purposes of our simulation, the pixel area is equal to the photoconductor area, $J_{a\text{-}se,dark}$ = 1 pA/mm^2, and T_F = 33ms.

The transistor current leakage shot noise at the detection node is due to the RDP TFT, and is given by

$$q_{TFT,L} = \sqrt{\frac{I_{TFT,L} T_F}{q}} \tag{4.13}$$

where $I_{TFT,L}$ is the transistor leakage current. For our a-Si simulations we used a leakage current of 0.03 fA per micron of gate width [66].

Reset noise is given by

$$q_{reset}^2 = \frac{kTC_{eff}}{q^2} \tag{4.14}$$

for the amplified pixel, where C_{eff} is the effective sense node capacitance, which is smaller than the total capacitance of the sense node due to the AMP TFT parasitic feedback capacitance, C_{gs1}. The effective capacitance at the detection node is given by [37]

$$C_{eff} = C_{PIX} + (1 - A_{v0})C_{gs1} \tag{4.15}$$

where C_{PIX} is the pixel node capacitance from the gate of the AMP TFT to ground and A_{v0} is the DC gain of the AMP TFT taken from the source to the gate, V_{s1}/V_{in}, as shown in Figure 4.2, and is described by

$$A_{v0} = \frac{g_{m1}}{1/(r_{ds2} + R_{data}) + g_{m1} + g_{ds1}} \tag{4.16}$$

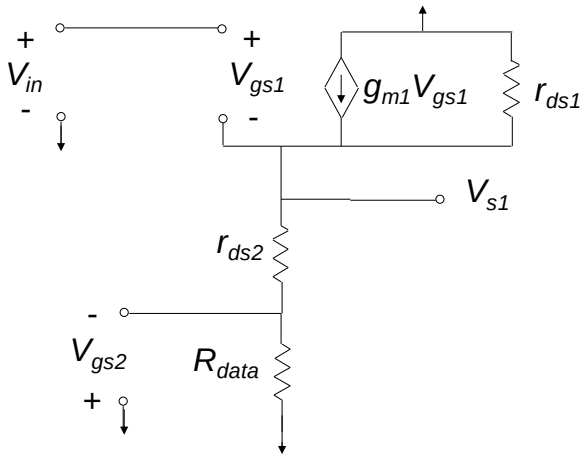


Figure 4.2. Small-signal circuit for DC gain analysis.

In addition, if double sampling is implemented, the reset noise voltage variance doubles to give $q_{reset}^2 = \frac{2kTC_{eff}}{q^2}$.

Performing a nodal analysis using Figure 4.1 and only taking into account the noise sources of the AMP and RDC TFTs, which are independent and uncorrelated, the total noise at the output of the double sampling operation from the two transistors can be described by (see Appendix C)

$$\overline{V_o^2} = \left\{\overline{V_2^2}(g_{m1}C_{PIX})^2 + \overline{i_1^2}(C_{gs}+C_{PIX})^2\right\}\int_0^\infty \left|\frac{1}{C_F(C_{PIX}g_{m1}r_{ds2}+C_{PIX}+C_{gs1})}\right|^2 H_{LPF}^2(\omega)W^2(\omega)df \quad (4.17)$$

Here we assumed that the time constants associated with the poles and zeroes formed by the capacitive elements C_{PIX}, C_{gs}, C_{gd2}, and C_d are much smaller than the LPF time constant such that they can be neglected, and that $r_{ds2} >> R_{data}$. In addition, we have neglected the capacitances C_i (charge amp input capacitance) and C_d (portion of modeled data line capacitance adjacent to C_i) in our derivation, since they are shunted to ground through the virtual ground of the op-amp. We can solve for the above integral using numerical integration methods or using a mathematical solver such as Maple.

In order to determine the flicker noise of the AMP and RDC TFTs, we simply need to replace the generic noise densities, $\overline{V_2^2}$ and $\overline{i_1^2}$, with the flicker noise densities and solve using numerical integration methods. The flicker noise current spectral densities for a-Si in the saturation and linear regimes are modeled respectively using the mobility fluctuation model as [56, 57]

$$\overline{i_{1,f}^2} = \frac{\alpha_H q \mu_{eff}^2 C_{ox} W (V_{GS} - V_T)^3}{2 f L^3} \tag{4.18}$$

$$\overline{i_{2,f}^2} = \frac{\alpha_H q \mu_{eff}^2 C_{ox} W (V_{GS} - V_T) V_{DS}^2}{f L^3} \tag{4.19}$$

where α_H is a constant for a given technology. For the purposes of our simulation, we have chosen $\alpha_H = 1 \times 10^{-2}$. [57]

The thermal noise current spectral densities for a-Si TFTs in the saturation and linear regimes are modeled respectively as

$$\overline{i_{1,th}^2} = \frac{8}{3} KT g_{m1} \tag{4.20}$$

$$\overline{i_{2,th}^2} = \frac{4KT}{r_{ds2}} \tag{4.21}$$

The data line is modeled using a π-model composed of two capacitors (C_d) and a single resistor (R_{data}) which gives a more accurate noise response than a lumped RC model. We have estimated the data line capacitance, C_{data}, to be 66 pF and the data line resistance, R_d, to be 26 kΩ. Assuming readout is performed from both sides of the array, we can halve both the capacitance and resistance of the data line. Thus, in our model C_d = 16.5 pF and R_{data} = 13 kΩ.

Assuming the RDC TFT is off, the data line thermal noise is given by

$$\overline{V_{o,data}^2} = \overline{V_{data}^2} \left(\frac{C_d}{C_F} \right)^2 \int_0^\infty \left| \frac{1}{(1 + sC_d R_{data})} \right|^2 H_{LPF}^2(\omega) W^2(\omega) df \tag{4.22}$$

If $\beta >> C_d R_{data}$, our output referred data line thermal noise voltage is reduced to (see Appendix C)

$$\overline{V_{o,data}^2} = \overline{V_{data}^2}\left(\frac{C_d}{C_F}\right)^2 \frac{1}{2\beta} \tag{4.23}$$

The charge operational amplifier output noise voltage assuming the RDC TFT is off is given by

$$\overline{V_{out,op}^2} = \int_0^\infty \left|\frac{4(C_F + 2C_d + C_i) + s4R_{data}C_d(C_d + C_i + C_F)}{C_F(4 + sC_d R_{data})}\right|^2 H_{LPF}^2(\omega)W^2(\omega)\cdot\overline{V_{op}^2}df \tag{4.24}$$

Notice that C_i and C_d cannot be neglected in the derivation since the noise originates from the opamp, and hence the inverting terminal of the opamp is no longer at virtual ground. If we again assume that $\beta >> C_d R_{data}$ then (4.24) can be simplified to (see Appendix C)

$$\overline{V_o^2} = \left\{\overline{V_{op}^2}\left(\frac{C_F + 2C_d + C_i}{C_F}\right)^2\right\}\int_0^\infty \frac{2(1-\cos(\omega\tau))}{1+\omega^2\beta^2}df \tag{4.25}$$

The op-amp noise voltage can be described in terms of its thermal and flicker noise components as

$$\overline{V_{op}^2} = \left(1 + \frac{f_{ce}}{f}\right)\overline{V_{th}^2} \tag{4.26}$$

where V^2_{th} is the thermal noise density and f_{ce} is the $1/f$ corner frequency of the charge amplifier. The thermal noise voltage of the op-amp is given as

$$\overline{V_{o,th}^2} = \overline{V_{op}^2}\left(\frac{C_F + 2C_d + C_i}{C_F}\right)^2 \frac{1}{2\beta} \tag{4.27}$$

Substituting the flicker noise component of (4.26) into (4.25) gives us the following flicker noise voltage

$$\overline{V_{o,op,f}^2} = \left\{ f_{ce} \overline{V_{th}^2} \left(\frac{2C_d + C_i + C_F}{C_F} \right)^2 \right\} \int_0^\infty \frac{2(1-\cos(\omega\tau))}{f(1+\omega^2\beta^2)} df \tag{4.28}$$

We can solve for the flicker noise component using numerical integration methods.

In order to quantify the total noise of our system, we refer it to the input node. For example, the circuit thermal noise referred to the input node in electrons is given by,

$$q_{in,th} = \frac{\sqrt{\overline{V_{o,th}^2}} C_{eff}}{A_v \cdot q} = \frac{\sqrt{\overline{q_{o,th}^2}}}{G_i} \tag{4.29}$$

where A_v is the voltage gain and G_i is the charge gain of the amplified pixel-charge integrator circuit combination [13] given by

$$A_v = G_m T_{int}/C_F. \tag{4.30}$$

$$G_i = G_m T_{int}/C_{eff}. \tag{4.31}$$

Here G_m is the transconductance of the C-APS circuit given by

$$G_m \approx \frac{g_{m1}}{1 + g_{m1} r_{ds2}} \tag{4.32}$$

Since our noise sources are uncorrelated, the individual mean-squared noise voltages can be simply added in quadrature to form the total output noise voltage. Alternatively, we can add the input referred noise in electrons squared from our various noise sources such that the total input referred noise (in electrons squared) becomes

$$q_{in,total}^2 = q_{in,th}^2 + q_{in,f}^2 + q_{in,data}^2 + q_{in,op}^2 + q_{reset}^2 + q_{a-Se}^2 + q_{TFT,L}^2 \tag{4.33}$$

Noise simulations were performed on an a-Si circuit using the C-APS architecture. By changing the aspect ratios of the AMP and RDC TFTs, it is possible to optimize the noise. Table 4.2 summarizes the C-APS circuit parameters used in the noise simulations. The choice of TFT parameters, particularly the aspect ratio, was chosen to give good noise performance.

Table 4.2 Parameters for noise testing of the C-APS circuit

TFT Simulation Parameters	a-Si
W_1 (μm), AMP TFT width	100
L_1 (μm), AMP TFT length	10
W_2 (μm), RDC TFT width	100
L_2 (μm), RDC TFT length	10
ΔL (μm), Gate-source overlap	2
t_{ox} (nm), Gate insulator thickness	250
V_{DD} (V), DC power rail	15
V_G (V), Nominal AMP gate voltage	15
V_{RDC} (V), RDC gate voltage	15
μ_{eff} (cm^2/Vs), Effective channel	0.5
V_T (V), TFT threshold voltage	4
C_{eff} (pF), effective pixel node capacitance	0.49
T_{int} (μs), integration time	22

The total input referred noise for the C-APS circuit is summarized in Table 4.3.

Table 4.3. Total input referred noise from different noise sources

Input Referred Noise (electrons)	a-Si
AMP TFT thermal noise	56
AMP TFT flicker noise	738
RDC TFT thermal noise	43
RDC TFT flicker noise	371
Data line thermal noise	26
Charge op-amp thermal noise	61
Charge op-amp flicker noise	38
a-Se dark current shot noise	68
Reset TFT leakage current shot noise	25
Reset (kTC) noise	390
Total noise	923

Large flat panel imagers in a-Si using PPS architectures have been reported to exhibit noise levels on the order of 1600-2000 electrons [18, 67]. In order to produce low-noise images for X-ray modalities like fluoroscopy throughout the exposure range, the total electronic noise should be less than the quantum noise, which is approximately 1000 electrons for a-Se photoconductors at electric fields of 10 V/μm at fluoroscopy energy levels (70kVp).

The total input referred noise for the a-Si C-APS circuit is as little as half of the previously reported noise values of large flat panel imagers in some cases, and is quantum noise-limited (below 1000 electrons). As seen from Table 4.3, the major noise contributors in the C-APS imager are the flicker noise of the AMP and RDC TFTs, and the reset noise. The charge gain associated with the C-APS circuit greatly reduces the impact of the data line thermal noise and external op-amp noise, which are major noise sources in conventional PPS designs. The input referred noise (in electrons) decreases as we reduce the sense node capacitance due to a reduction in reset noise and an increase in charge gain G_i. We can plot the total input referred noise in electrons as a function of C_{eff} for both C-APS and PPS circuits as shown in Figure 4.3, noticing that the noise of the a-Si C-APS circuit exceeds the noise of the PPS circuit when C_{eff} is approximately 900 fF.

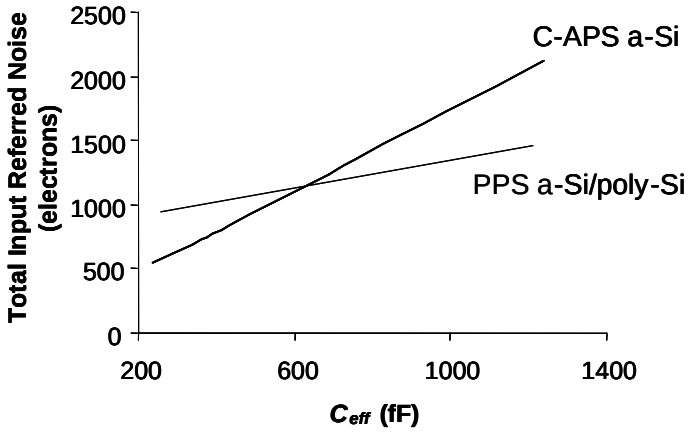


Figure 4.3. Total input referred noise vs. effective sense node capacitance

It should be noted that by optimizing the TFT device dimensions, it is possible to reduce the total input referred noise for the C-APS architecture below the values listed in Table 4.3. Using the a-Si technology parameters from Table 4.2 as an example, and keeping the RDC TFT fixed at W/L = 100/10μm, we can see from Figure 4.4 that varying the AMP TFT aspect ratio will have a large impact on the total input referred noise, and that there is an optimal value for TFT device dimensions that will give minimum input referred noise.

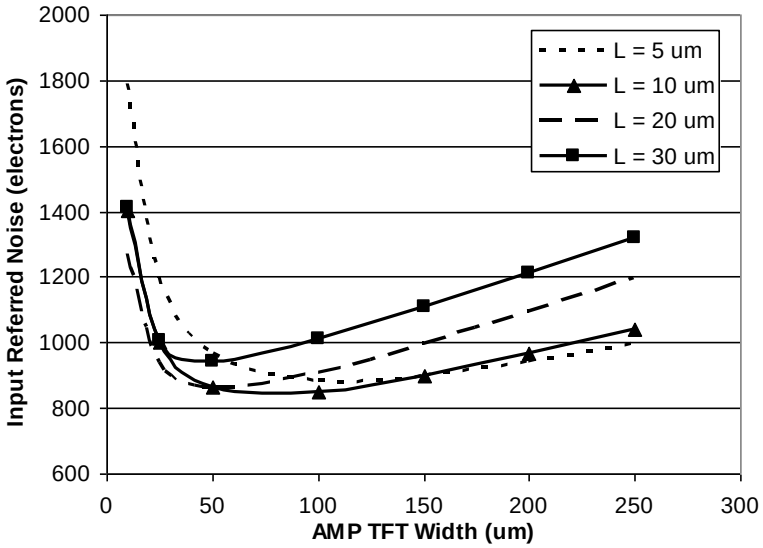


Figure 4.4 AMP TFT width vs. total input referred noise for various gate lengths

In the next section, it will be demonstrated how device dimensions can be optimized to achieve low-noise performance.

4.3 Noise Optimization

In this section the reset noise, and the AMP and RDC TFT flicker and thermal noise components are derived in terms of device dimensions and optimized for low-noise performance. The AMP and RDC TFT flicker and thermal noise can be normalized and simplified in terms of device dimensions, giving the following for input referred noise in electrons (see Appendix C for derivations).

The normalized input referred AMP TFT flicker noise charge in mean-squared electrons is given by

$$\overline{q_{fl,N1}^2} = \frac{\alpha_H \left(C_{gs1} + C_{PIX}\right)^2 (V_{GS1} - V_{T1})}{C_{ox} W_1 L_1 q} \tag{4.34}$$

The normalized input referred RDC TFT flicker noise charge in mean-squared electrons is given by

$$\overline{q_{fl,N2}^2} = \frac{2C_{PIX}^2 \alpha_H (V_{GS2} - V_{T2}) V_{DS2}^2}{qC_{ox} W_2 L_2 (V_{GS2} - V_{T2} - V_{DS2})^2} \tag{4.35}$$

The normalized input referred AMP TFT thermal noise charge in mean-squared electrons is given by

$$\overline{q_{th,N1}^2} = \frac{8kT\left(C_{gs1} + C_{PIX}\right)^2 L_1}{3q^2 T_{\text{int}} \mu_{eff} C_{ox} W_1 \left(V_{GS1} - V_{T1}\right)} \tag{4.36}$$

The normalized input referred RDC TFT thermal noise charge in mean-squared electrons is given by

$$\overline{q_{th,N2}^2} = \frac{4kTr_{ds2}C_{PIX}^2}{q^2 T_{\text{int}}} = \frac{4kTC_{PIX}^2 L_2}{q^2 T_{\text{int}} \mu_{eff} C_{ox} W_2 \left(V_{GS2} - V_{T2} - V_{DS2}\right)} \tag{4.37}$$

Since the input referred noise electrons are a function of the sense node capacitance, it is important to determine the various sources of capacitance at the input sense node in order to optimize the noise. As indicated in (4.15), the effective pixel sense node capacitance, C_{eff}, is comprised of a capacitance from the sense node to ground, C_{PIX}, and a capacitance from the sense node to the source of the AMP transistor, C_{gs1}. The capacitances that comprise C_{PIX} and C_{gs1} are enumerated below and illustrated in Figure 4.5.

$$C_{PIX} = C_{gd1,ch} + C_{gd1,ov} + C_{gd3,ch} + C_{gd3,ov} + C_s + C_{pd} + C_{stray} \tag{4.38}$$

$$C_{gs1} = C_{gs1,ch} + C_{gs1,ov} \tag{4.39}$$

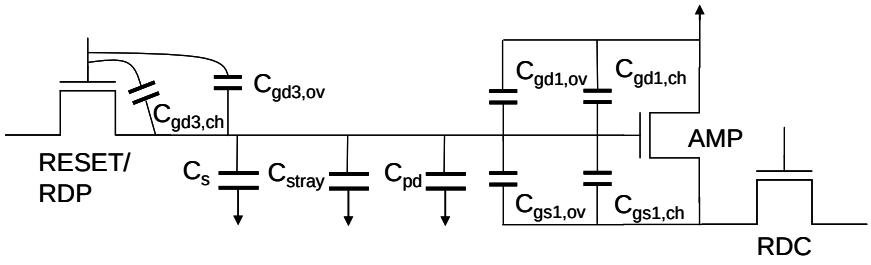


Figure 4.5 Input sense node capacitances.

Here $C_{gd1,ch}$, $C_{gd1,ov}$, $C_{gd3,ch}$, and $C_{gd3,ov}$ represent the gate-drain capacitance associated with the channel and overlap capacitances of the AMP and RESET/RDP transistors respectively. Similarly, $C_{gs1,ch}$ and $C_{gs1,ov}$ represent the gate-source channel and overlap capacitances of the

AMP transistor. The quantities C_s, C_{pd}, and C_{stray} represent the storage, photodetector-photodiode, and stray capacitances respectively.

In the analysis that follows, two scenarios are considered. The first scenario, called the "ideal case", assumes that C_{PIX} and C_{gs1} are solely comprised of the AMP transistor channel capacitance. As we will see later, the ideal case gives the lowest possible input referred noise, and the smallest device dimensions. Furthermore, by studying the ideal case first, we can see how the device dimensions of the amplifier portion of the circuit (AMP and RDC TFTs) affect the various major noise sources, and give greater insight into the noise behaviour of the pixel in two complementary ways:

1. Our noise equations are simplified allowing for greater intuitive understanding
2. The effect of other sense node capacitances are removed allowing for greater focus on the effects of changing device dimensions.

The second scenario, called the "non-ideal case", takes into account all the sense node capacitances [68].

4.3.1 Ideal case: C_{eff} only a function of the AMP TFT

Although the "ideal case" does not exist, a situation in which the AMP transistor channel capacitance dominates other sources of pixel node capacitance exists for real-time digital X-ray fluoroscopy systems using a direct detector such as amorphous selenium. Because of the large thicknesses of a-Se required to effectively stop most of the incoming X-rays (>0.2 mm), the capacitance C_{pd} can be less than 5 fF. In addition, if the high voltage across the a-Se layer is ramped slowly, the need for a storage capacitor is obviated. Finally, with self-aligned, or low gate-source/drain overlap transistors, the effect of overlap transistor capacitances becomes negligible, and we begin to approach the ideal scenario.

For the following analysis (4.38) and (4.39) become

$$C_{PIX} = C_{gd1,ch} = bC_{ox}W_1L_1 \tag{4.40}$$

$$C_{gs1} = C_{gs1,ch} = aC_{ox}W_1L_1 \tag{4.41}$$

where a and b are constants.

4.3.1.1 Reset noise

Returning to the case of reset noise, the effective sense node capacitance, C_{eff}, can be rewritten by first simplifying the DC gain A_{v0}, by noting that $g_{ds,data} >> g_{ds2} >> g_{ds1}$. Thus, (4.16) can be simplified to

$$A_{v0} \approx \frac{g_{m1}}{g_{ds2} + g_{m1}} = \frac{g_{m1} r_{ds2}}{1 + g_{m1} r_{ds2}} \tag{4.42}$$

By combining (4.15) and (4.42), the sense node capacitance can be rewritten as

$$C_{eff} = \left(C_{PIX} + \frac{C_{gs1}}{1 + g_{m1} r_{ds2}} \right) \tag{4.43}$$

Substituting for g_{m1} and r_{ds2}, and inserting (4.40) and (4.41), (4.43) can be rewritten as

$$C_{eff} = \left(bC_{ox} W_1 L_1 + \frac{aC_{ox} W_1 L_1}{1 + \frac{W_1}{W_2} \cdot \frac{V_{gs1} - V_{T1}}{V_{gs2} - V_{T2} - V_{ds2}}} \right) \tag{4.44}$$

Here L_1 and L_2 have been assumed equivalent. Equation (4.44) can be further simplified by noting that $V_{g1}=V_{g2}$, $V_{T1}=V_{T2}$, $V_{S2}=0$, and $V_{S1}=V_{D2}$, and by rearranging we have,

$$C_{eff} = C_{ox} L_1 \left(bW_1 + \frac{aW_1 W_2}{W_1 + W_2} \right) \tag{4.45}$$

From the first term, and the first term in brackets, we can see that minimizing L_1 and W_1 will reduce C_{eff} and thus the reset noise. From the second term in brackets, we can see that W_1 and W_2 are like two resistors in parallel, where the smaller term will dominate. Thus by minimizing the AMP TFT device dimensions, the reset noise can be minimized, and the width of the RDC TFT, W_2, can be made large.[3]

[3] Of course, having a smaller W_2 will reduce the noise more than having a large W_2. Furthermore, there are pixel area constraints, so W_2 can not be increased unreasonably.

4.3.1.2 TFT flicker noise

In the case of the AMP TFT flicker noise, (4.34) can be simplified by substituting in (4.40) and (4.41) such that

$$\overline{q_{fl,N1}^2} = \frac{\alpha_H (a+b)^2 C_{ox} W_1 L_1 (V_{GS1} - V_{T1})}{q} \tag{4.46}$$

What is interesting to note is that while it is true that the flicker noise of a TFT decreases with increasing device dimensions, since it is inversely proportional to WLC_{OX}, it can not be concluded that larger device dimensions lead to less equivalent input noise as evidenced by (4.46). In fact, under the ideal condition where the sense node capacitance is comprised solely by the AMP transistor channel capacitance, minimizing the device dimensions of the AMP transistor reduces the input referred flicker noise.

Substituting for C_{PIX} in (4.35) with (4.40) gives the following for RDC flicker noise

$$\overline{q_{fl,N2}^2} = \frac{2b^2 C_{ox} W_1^2 L_1^2 \alpha_H (V_{GS2} - V_{T2}) V_{DS2}^2}{q W_2 L_2 (V_{GS2} - V_{T2} - V_{DS2})^2} \tag{4.47}$$

It can also be noticed that V_{GS2}-V_{T2} is a constant, and that in order to minimize the noise, V_{DS2} should be minimized. In the case where V_{G1}-V_{T1} = V_{G2}-V_{T2} = V_{GT}, V_{DS2} is given by

$$V_{DS2} = V_{GT}\left(1 - \sqrt{\frac{W_2 / L_2}{W_1 / L_1 + W_2 / L_2}}\right) \tag{4.48}$$

Thus V_{DS2} can be reduced by increasing W_2/L_2 and/or decreasing W_1/L_1. Assuming that V_{GT} >> V_{DS2}, and making a simplifying assumption that $V_{DS2} \propto \sqrt{\frac{L_2}{W_2} \cdot \frac{W_1}{L_1}}$, (4.47) can be rewritten as

$$\overline{q_{fl,N2}^2} \propto \frac{2b^2 C_{ox} \alpha_H W_1^3 L_1}{q W_2^2 (V_{GS2} - V_{T2})} \tag{4.49}$$

Thus by minimizing the AMP gate device dimensions, or increasing the width of the RDC gate, the RDC input referred flicker noise charge is minimized.

4.3.1.3 TFT thermal noise

For the AMP TFT, substituting (4.40) and (4.41) into (4.36) gives us the following for the input referred thermal noise

$$\overline{q_{th,N1}^2} = \frac{8kT(a+b)^2 C_{ox} W_1 L_1^3}{3q^2 T_{\text{int}} \mu_{eff} (V_{GS1} - V_{T1})} \tag{4.50}$$

Thus, the thermal noise can be reduced by minimizing the AMP TFT device dimensions.
For the RDC TFT, substituting (4.41) into (4.37) gives us the following for the input referred thermal noise

$$\overline{q_{th,N2}^2} \propto \frac{4kTb^2 C_{ox} W_1^2 L_1^2 L_2}{q^2 T_{\text{int}} \mu_{eff} W_2 (V_{GS2} - V_{T2})} \tag{4.51}$$

Once again, the thermal noise can be reduced by minimizing the AMP TFT device dimensions and RDC gate length, or by increasing the RDC TFT gate width.

In summary, for minimum noise under ideal conditions where sense node capacitance is comprised solely of AMP gate channel capacitance, it is desirable to minimize the AMP TFT gate dimensions, L_1 and W_1, and to maximize the RDC width, W_2. Figure 4.6 illustrates the input referred noise as a function of the AMP TFT gate width, W_1, for various gate lengths in the ideal case. In the simulation both AMP TFT and RDC TFT gate lengths were adjusted simultaneously (i.e. $L_1 = L_2$), and the RDC TFT gate width, W_2, was fixed at 100um. As can be seen, the input referred noise decreases monotonically as the AMP TFT device dimensions decrease. It should be emphasized that the ideal case is always sought (where any non-AMP TFT channel capacitances are minimized), as this will lead to the lowest input referred noise and the smallest device dimensions.

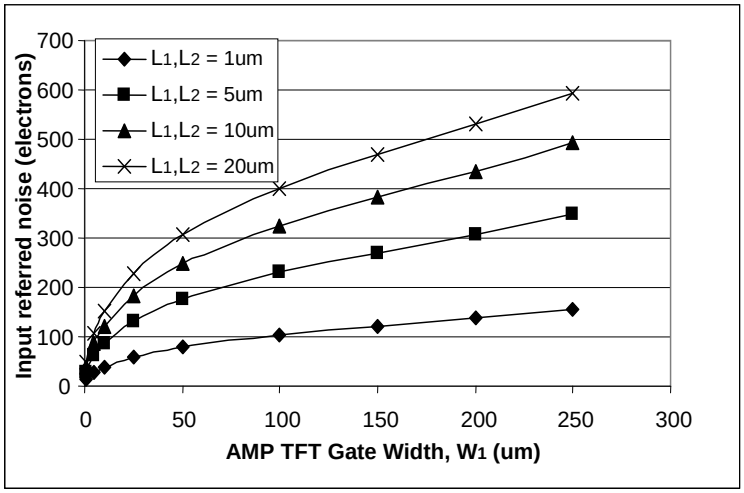


Figure 4.6 Input referred noise vs. AMP TFT gate width, W1, for various gate lengths, when L1 = L2, W2 = 100um.

4.3.2 Non-ideal case: C_{eff} comprised of all sense node capacitances

Under non-ideal conditions, where C_{eff} is comprised of all the sense node capacitances as given by (4.38) and (4.39), the minimum noise will no longer be achieved by minimizing L_1 and W_1, and maximizing W_2 for all noise sources. In the case of the AMP flicker noise, the optimal device dimensions can be re-derived by inserting (4.38) and (4.39) into (4.34).

$$\overline{q_{fl,N1}^2} = \frac{\alpha_H \left\{W_1\left[(a+b)C_{ox}L_1 + 2C_{ov}L_{ov}\right] + C_i\right\}^2 (V_{GS1} - V_{T1})}{qC_{ox}W_1L_1} \tag{4.52}$$

Here we have used $C_{PIX} = C_i + C_{gd1,ch} + C_{gd1,ov} = C_i + bC_{ox}W_1L_1 + C_{ov}W_1L_{ov}$, where C_i represents all the capacitances at the sense node that are independent of the AMP TFT device dimensions, C_{ov} is the overlap capacitance per unit area, and L_{ov} is the gate-drain (or gate-source) overlap length. Similarly $C_{gs1} = aC_{ox}W_1L_1 + C_{ov}W_1L_{ov}$.

Unlike the noise equation in the "ideal case", it is not entirely obvious how to adjust the device dimensions in order to minimize the input referred AMP TFT flicker noise by glancing at (4.52). Taking the derivative of (4.52) with respect to the gate width and setting to zero, as shown in (4.53), gives the optimal AMP TFT gate width for low noise. The gate length was made constant in order to allow for a simple optimization, and given that gate

lengths are often constant for a given process technology, the choice in optimizing the gate width is a practical one.

$$\frac{\partial\overline{q_{fl,N1}^2}}{\partial W_1}=\frac{\alpha_H V_{GS1}-V_{T1}}{C_{ox}L_1 q}\cdot\frac{W_1\left[(a+b)C_{ox}L_1+2C_{ov}L_{ov}\right]-C_i^2}{W_1^2}=0,\quad C_{g1}=W_1\left[(a+b)C_{ox}L_1+2C_{ov}L_{ov}\right]=C_i \tag{4.53}$$

Equation (4.53) indicates that the noise is no longer monotonically decreasing with respect to device dimensions, and that there is now a non-zero device dimension corresponding to the minimum noise value. Furthermore, this optimum value occurs when the AMP TFT capacitances exactly balance the AMP TFT independent capacitances, C_i.

Since our noise sources are uncorrelated, the individual mean-squared noise electrons can be simply added in quadrature to form the total input referred noise (in electrons squared). The optimized noise is determined by taking the derivative of the total noise with respect to the AMP TFT gate width, W_1, leaving the other device dimensions L_1, L_2, and W_2 as constants, and setting to zero.

$$\frac{\partial\overline{q_{in,total}^2}}{\partial W_1}=\frac{\partial\overline{q_{reset}^2}}{\partial W_1}+\frac{\partial\overline{q_{fl,1}^2}}{\partial W_1}+\frac{\partial\overline{q_{fl,2}^2}}{\partial W_1}=0 \tag{4.54}$$

Here we have for the derivative components of (5.47)

$$\frac{\partial\overline{q_{reset}^2}}{\partial W_1}=\frac{\partial C_{PIX}}{\partial W_1}+\frac{aC_{ox}L_1+C_{ov}L_{ov}}{1+\dfrac{W_1L_1}{W_2L_2}}-\frac{\left(aC_{ox}W_1L_1+C_{ov}W_1L_{ov}\right)L_1}{\left(1+\dfrac{W_1L_1}{W_2L_2}\right)W_2L_2} \tag{4.55}$$

$$\frac{\partial\overline{q_{fl,1}^2}}{\partial W_1}=\frac{\alpha_H I(x)C_t}{2q}\left[\frac{2\left(2C_{ov}L_{ov}+(a+b)C_{ox}L_1\right)V_{eff1}}{C_{ox}W_1L_1}+\frac{C_t}{C_{ox}W_1L_1}\frac{\partial V_{eff1}}{\partial W_1}-\frac{C_tV_{eff1}C_{ox}I}{\left(C_{ox}W_1L_1\right)}\right] \tag{4.56}$$

$$\frac{\partial\overline{q_{fl,2}^2}}{\partial W_1}=\frac{2\alpha_H I(x)V_{GT2}C_{PIX}V_{DS2}}{qC_{ox}W_2L_2\left(V_{GT2}-V_{DS2}\right)^2}\left[V_{DS2}\frac{\partial C_{PIX}}{\partial W_1}+\frac{C_{PIX}V_{DS2}}{V_{GT2}-V_{DS2}}\frac{\partial V_{DS2}}{\partial W_1}+C_{PIX}\frac{\partial V_{DS2}}{\partial W_1}\right] \tag{4.57}$$

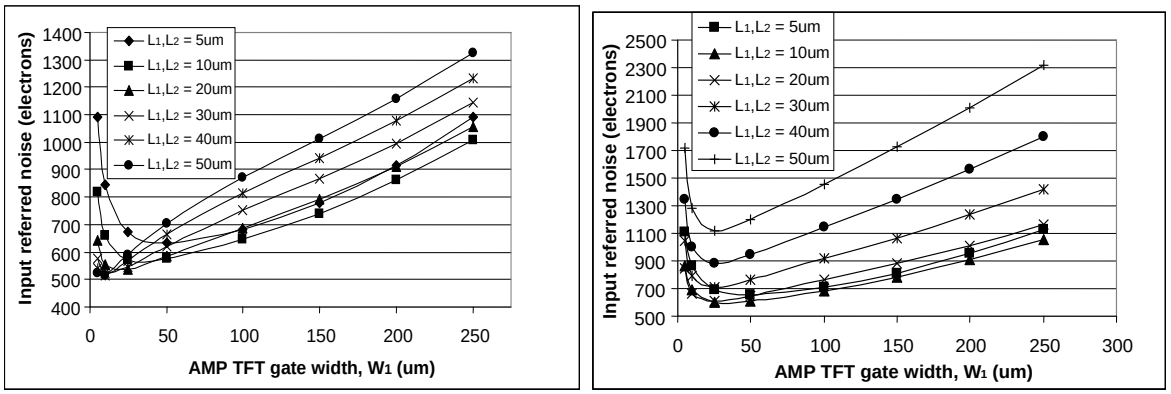
Where $V_{eff1}=V_{GT1}-V_{DS2}$ and $C_t=C_{PIX}+C_{gs1}$.

Equation (4.54) neglects the effect of the TFT thermal noise sources, as our earlier work has shown that the total input referred noise is dominated by the reset noise and the TFT flicker

noise components in the case where the charge gain is sufficiently large (i.e. greater than ten).

Figure 4.7(a) illustrates the input referred noise of the reset and TFT flicker noise (three major noise sources) as a function of the AMP TFT gate width, W_1, for varying gate lengths when C_i = 100fF, W_2 = 100um, and L_{ov} = 3um. As can be seen, for this non-ideal case, there is an optimal non-zero AMP TFT gate width value corresponding to the lowest noise for a given gate length.

Figure 4.7(b) shares the same simulation conditions as Figure 4.7(a), except that it also includes the additional noise sources (photodetector shot noise, transistor leakage noise, TFT thermal noise), including the external noise sources such as the op-amp noise and data line noise. Here the higher gate length devices neither exhibit the same level of low noise, nor the same optimal gate width value, W_1 as in Figure 4.7(a). This is due to the very low charge gain exhibited at large gate lengths, which causes the external noise to have a significant impact on the total noise of the device. Under more moderate gate lengths, the optimal AMP TFT gate width, W_1, is largely determined by the reset noise and TFT flicker noise, with the other noise sources contributing less to the overall noise.



(a) (b)

Figure 4.7 (a) Input referred noise (3 major noise sources) vs. AMP TFT gate width, W_1.

(b) Total input referred noise vs. AMP TFT gate width, W_1. Simulation parameters of varying gate lengths when C_i = 100fF, W_2 = 100um, and L_{ov} = 3um.

Using equation (4.54), the optimal gate width is plotted versus C_i (the non-AMP TFT related portions of C_{PIX}) for various AMP gate lengths in Figure 4.8. As can be seen, the optimal gate width increases with increasing C_i, regardless of the gate length chosen. The simulations were performed with W_2 = 100um, and L_2 = 10um.

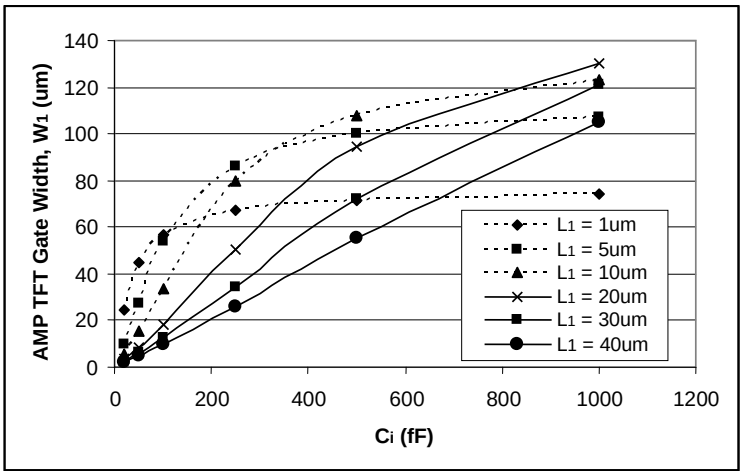


Figure 4.8. Optimal TFT gate width, W_1 vs. C_i for various AMP gate lengths, L_1, when W_2 = 100um, and L_2 = 10um.

From the simulations, we can determine that by minimizing all non-gate channel capacitances (i.e. moving towards ideal scenario), the total input referred noise is minimized. Furthermore, with moderate gate lengths (ie. L = 10um), the total input referred noise is primarily a function of the reset and TFT flicker noise, and all other noise sources can be neglected when finding an optimal gate width for minimizing noise. With these points in mind, we can proceed to design an active pixel sensor that is optimized for low-noise performance. In Table 4.4, the design parameters for an optimal low-noise R&F design are listed for the case of a typical fabrication process, and a state-of-the-art (optimistic) process that incorporates all fabrication techniques beneficial to a low-noise design.

As the optimization process has shown, minimum noise performance is obtained when the pixel sense node capacitance is decreased; however, in order to preserve a dynamic range large enough to accommodate radiography, the pixel sense node capacitance and/or the reset

voltage at the pixel node should be large. Figure 4.9 illustrates the total input referred noise for an optimal low-noise design for various pixel sense node capacitances with the required AMP TFT gate voltage to produce a dynamic range adequate to accommodate the full exposure range of radiography. In the case of the optimistic design process, values as low as 306 electrons of total input referred noise can be realized, which is less than a third of the original design presented in Table 4.3. It should be noted that although a C_{PIX} value of 150 fF gives the lowest noise design, it is may be more appropriate to choose a value of 250 fF in order to lower the AMP TFT gate voltage, and thus increase the stability of the circuit (stability with respect to threshold voltage degradation).

Table 4.4 Parameters for noise testing of the C-APS circuit

TFT Simulation Parameters	Typical	Optimistic
W_1 (μm), AMP TFT width	44	42
L_1 (μm), AMP TFT length	10	10
W_2 (μm), RDC TFT width	25	25
L_2 (μm), RDC TFT length	15	15
ΔL (μm), Gate-source overlap	3	1.5
t_{ox} (nm), Gate insulator thickness	250	250
V_{DD} (V), DC power rail	10.2	12.9
V_G (V), Nominal AMP gate voltage	10.2	12.9
V_{RDC} (V), RDC gate voltage	15	17
μ_{sat} (cm^2/Vs), saturation regime mobility	0.5	0.8
μ_{lin} (cm^2/Vs), linear regime mobility	0.5	0.7
α_H, Hooge flicker noise coefficient	1×10^{-2}	0.7×10^{-2}
V_T (V), TFT threshold voltage	2	2
C_i (fF), extraneous sense node capacitance	50	30
C_{pix} (fF), total pixel node capacitance	200	150
Pixel pitch (μm), square pixel	150	150
Total input referred noise (electrons)	401	306

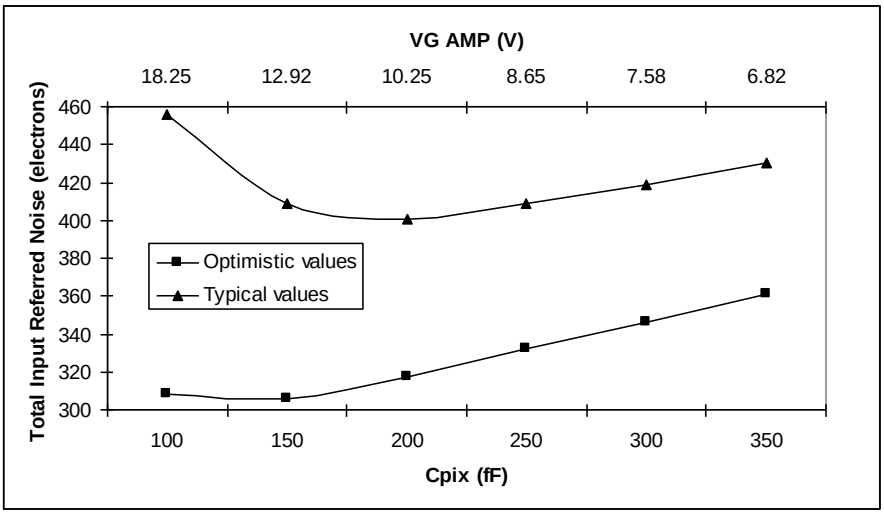


Figure 4.9. Optimized total input referred noise vs. C_{PIX} and V_G AMP for an R&F imager using typical and optimistic fabrication processes.

If an ultra-low noise imager is desired for low-dose real-time applications like fluoroscopy without the dynamic range constraints imposed by radiography (as in the case of a dual R&F imager), the noise floor can be decreased further by at least 100 electrons as shown in Figure 4.10.

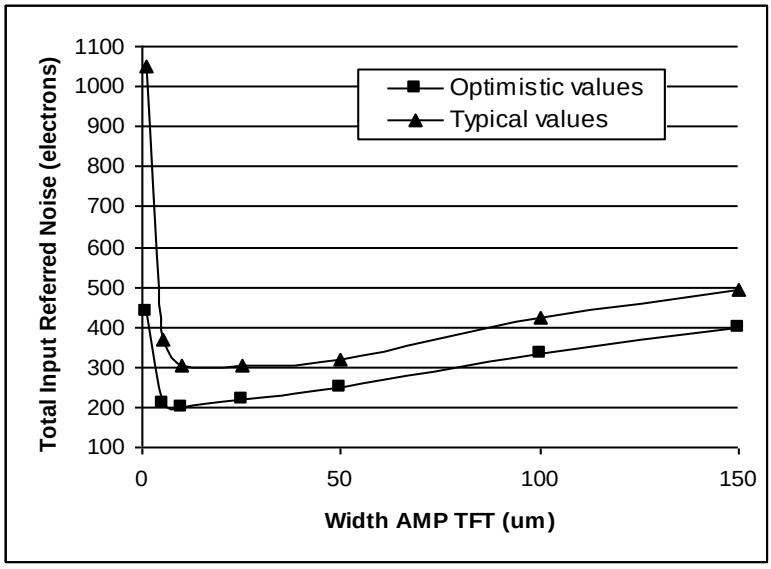


Figure 4.10. Optimized total input referred noise vs. W_1 for a single-mode fluoroscopic imager using typical and optimistic fabrication processes.

Table 4.5 indicates the input referred noise from the various noise sources along with the total input referred noise. As before, the major noise sources of the pixel are the TFT flicker noise and the reset noise for the case of a dual-mode R&F imager; however, the leakage current of the reset transistor begins to play a more dominant role in the total noise (a more realistic leakage current of 1 fA per micron of gate width is used in the noise optimization simulations). For the case of a purely fluoroscopic imager, other noise sources play a more dominant role, however, this is purely due to the fact that the gate length was limited to 10um. If smaller gate lengths were used in the simulation, the major noise sources would have remained the reset and flicker noise.

Table 4.5. Total input referred noise from different noise sources with double sampling

Input Referred Noise (electrons)	R & F		Fluoro Only	
	Typical	Optimistic	Typical	Optimistic
AMP TFT thermal noise	26	14	53	29
AMP TFT flicker noise	300	208	163	90
RDC TFT thermal noise	19	10	21	14
RDC TFT flicker noise	115	94	5	5
Data line thermal noise	16	6	102	49
Charge op-amp thermal noise	19	8	125	60
Charge op-amp flicker noise	12	5	78	37
a-Se dark current shot noise	68	68	68	68
Reset TFT leakage current shot	96	94	46	46
Reset (kTC) noise	204	166	156	126
Total noise	401	306	305	198

In the next section, we briefly extend the noise analysis to pixels incorporating indirect X-ray detectors and pixels employing poly-Si transistors.

4.4 Noise analysis with indirect detectors and poly-Si transistors

As seen in the previous section, in order to minimize the total input referred noise, a concerted effort should be made to minimize all capacitances at the input sense node, particularly those not associated with the AMP TFT channel capacitance. In the case of a

direct photoconductor like a-Se, where the material thicknesses used for stopping X-rays are typically quite large (>200μm), the capacitance added is minimal. For instance, in the case of a fluoroscopic imager where the a-Se thickness is 1mm, and the pixel pitch is 150μm, the capacitance of the selenium layer is a very negligible 1.2 fF. In the case of indirect detectors, however, the capacitance of the pixel photodiode required to convert the incoming light photons generated by the adjacent scintillator (such as CsI) can be quite large. Assuming a fully-overlapped photodiode is employed in order to maximize the light collection of the pixel, and using a 1μm thick a-Si photodiode with a pixel pitch of 75μm, the capacitance is 547 fF. This is a significant and dominant capacitance which serves to reduce the charge gain of the pixel, thereby increasing the total input referred noise. In addition, the increase in pixel capacitance increases the reset noise.

For poly-Si, a combination of the carrier number and mobility fluctuation noise models are used such that the flicker noise current spectral density is

$$\overline{i_f^2} = \left[1 + \alpha_S \mu_{eff} C_{ox} \frac{I_D}{g_m}\right]^2 g_m^2 \cdot \overline{i_{Vb,f}^2} \qquad (4.58)$$

$$\text{with} \quad \overline{i_{Vb,f}^2} = \frac{q^2 kT\lambda N_t}{WLC_{ox}^2 f}$$

where λ is the tunnel attenuation distance (approx. 0.1 nm) and N_t is the slow oxide trap density ($cm^{-3}eV^{-1}$). Here α_S is a constant correlated with the sensitivity of the mobility to the interface charge Coulomb scattering, and is equal to zero for cases where the flicker noise follows a purely carrier number fluctuation model. For the purposes of our simulation, we have chosen $N_t = 3.7 \times 10^{18}$ and $\alpha_S = 2 \times 10^4$ [59]. By substituting the flicker noise spectral density for poly-Si given by (4.58) into (4.17), we can simulate the total input referred noise in the case of poly-Si TFTs. The simulation parameters used for the poly-Si TFTs for both indirect and direct detection schemes, along with the simulation parameters for a-Si TFTs using an indirect detection scheme are shown in Table 4.6. The pixel parameters given by Table 4.6 allow for R&F operation.

Table 4.6 Parameters for noise testing of direct and indirect a-Si and poly-Si pixels

TFT Simulation Parameters	a-Si indirect	poly-Si indirect	poly-Si direct
W_1 (μm), AMP TFT width	100	100	59
L_1 (μm), AMP TFT length	10	10	10
W_2 (μm), RDC TFT width	25	25	25
L_2 (μm), RDC TFT length	15	15	15
ΔL (μm), Gate-source overlap	3	1	1
t_{ox} (nm), Gate insulator thickness	250	150	150
V_{DD} (V), DC power rail	4	4	10.2
V_G (V), Nominal AMP gate voltage	4	4	10.2
V_{RDC} (V), RDC gate voltage	15	15	15
μ_{sat} (cm^2/Vs), saturation regime mobility	0.5	150	150
μ_{lin} (cm^2/Vs), linear regime mobility	0.5	150	150
α_H, Hooge flicker noise coefficient	1×10^{-2}	N/A	N/A
α_S, Coulomb scattering coefficient	N/A	2×10^4	2×10^4
λ (nm), tunnel attenuation distance	N/A	0.1	0.1
N_t ($cm^{-3}eV^{-1}$), slow oxide trap density	N/A	3.7×10^{18}	3.7×10^{18}
V_T (V), TFT threshold voltage	2	2	2
C_i (fF), extraneous sense node capacitance	700	656	50
C_{pix} (fF), total pixel node capacitance	937	857	200
Pixel pitch (μm), square pixel	75	75	75
Total input referred noise (electrons)	865	681	279

The total input referred noise for direct and indirect a-Si and poly-Si pixels with double sampling is shown in Table 4.7.

Table 4.7. Total input referred noise for direct and indirect a-Si and poly-Si pixels

Input Referred Noise (electrons)	Direct detector		Indirect detector	
	a-Si	poly-Si	a-Si	poly-Si
AMP TFT thermal noise	26	2	209	11
AMP TFT flicker noise	300	145	519	448
RDC TFT thermal noise	19	1	167	9
RDC TFT flicker noise	115	47	113	44
Data line thermal noise	16	0	192	1
Charge op-amp thermal noise	19	0	235	1
Charge op-amp flicker noise	12	0	146	0
Detector dark current shot noise	68	68	68	68
Reset TFT leakage current shot	96	111	144	144
Reset (kTC) noise	204	195	506	486
Total noise	401	279	865	681

The total input referred noise for the indirect detectors could be reduced by employing a pixel topology that eliminates pixel level reset noise (though at the cost of an additional transistor) and/or using a photodiode with a material that allows larger thicknesses and/or lower relative permittivity to lower the added capacitance (such as an a-Se photodiode). The latter method (reducing the capacitance added by photodiode) would have the additional benefit of reducing other noise sources as well.

4.5 DQE(0) Simulation and analysis

In previous chapters we have seen that it is imperative to keep the electronic noise of the system to a minimum for low dosage modalities such as fluoroscopy and tomosynthesis. In this section we simulate the effect of varying electronic noise and incident X-ray exposure on the DQE of an imaging system using an a-Se photoconductor for fluoroscopy applications.

Recall that the detective quantum efficiency (DQE) of an imaging system is a measure of noise propagation through the system, and thus describes the overall signal-to-noise ratio (SNR) performance of the system. The DQE and SNR are related by:

$$DQE(f) = \frac{SNR_{out}^2}{SNR_{in}^2} \tag{4.59}$$

where f represents spatial frequency, and SNR_{in} and SNR_{out} represent the signal-to-noise ratio at the input and output of the detector, respectively.

For simplicity, we will examine the zero spatial frequency detective quantum efficiency, DQE(0), for an a-Se photoconductor using a cascaded linear system model presented by Kabir et al. [69] that takes into account the following stages: (1) X-ray attenuation, (2) the generation of charge carriers (conversion gain), (3) charge collection, (4) the addition of electronic noise. The block diagram of the cascaded system is shown in Figure 4.11.

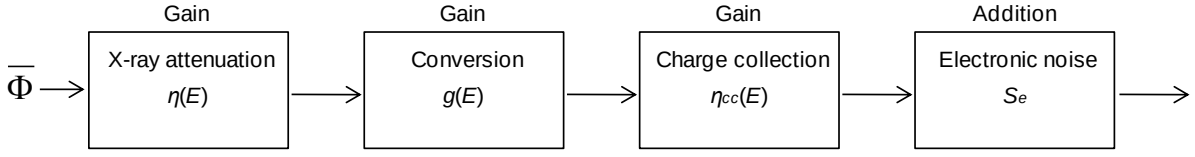


Figure 4.11. Block diagram of cascaded linear system used for DQE(0) calculation.

The first three stages of the system are gain stages, and the last stage is an additive noise stage. For the APS, the last stage is in reality both a gain stage and an additive noise stage; however, for simplicity of comparison with the PPS, we assume unity gain, and instead use the value of input referred noise for the additive electronic noise.

For the case of monoenergetic X-rays, and neglecting k-fluorescence reabsorption, the zero spatial frequency detective quantum efficiency is given as [69]

$$DQE(0) = \left[\frac{1}{\eta} + \frac{1}{\eta \bar{g}} + \frac{\sigma_c^2}{\eta \bar{g} \eta_{cc}^2} + \frac{S_e}{\eta^2 \bar{g}^2 \eta_{cc}^2 \bar{\Phi}} \right]^{-1} \tag{4.60}$$

where η is the X-ray quantum efficiency, $\bar{g}$ is the mean conversion gain, η_{cc} is the charge collection efficiency, σ_c^2 is the variance of the charge collection efficiency, $\bar{\Phi}$ is the mean incident X-ray quanta, and S_e is the electronic noise power.

The electron-hole pair creation energy, $W_{\pm}$, has a strong dependence on electric field and a weak dependence on X-ray photon energy in a-Se. By fitting the experimental data of Blevis et al. [70], Yunus obtained the following empirical expression for $W_{\pm}$ [71].

$$W_{\pm} = \left(6 + \frac{15 \times 10^6}{F^{0.8}} \right) \times \left(0.72 + 0.56 \exp\left(- E_{ph} / 62700 \right) \right) \tag{4.61}$$

Here F is the electric field in V/m, and E_{ph} is the X-ray photon energy in eV.

For the purposes of our simulations we assumed an amorphous selenium hole mobility of 0.13 cm^2/Vs, electron mobility of 0.003 cm^2/Vs, hole lifetime of 50 μs, electron lifetime of 200 μs, and a 70 kVp X-ray spectrum with average energy of 52.12 keV (RQA5 beam quality of IEC1267 standard [72]). Simulations were performed for X-ray exposures of 0.1μR to 10μR, additive electronic noise (N_e) of 0 to 2000 electrons (per pixel), and pixel areas ranging from 100μm x 100μm to 250μm x 250μm.

Figure 4.12 and Figure 4.13 present graphs of DQE(0) as a function of additive electronic noise (N_e) and detector thickness for a exposure of 0.1 μR and a pixel area of 150μm x 150μm. The data of Fig. 2 is at a constant high voltage bias of 10kV, while Fig. 3 is at a constant electric field of 10V/μm.

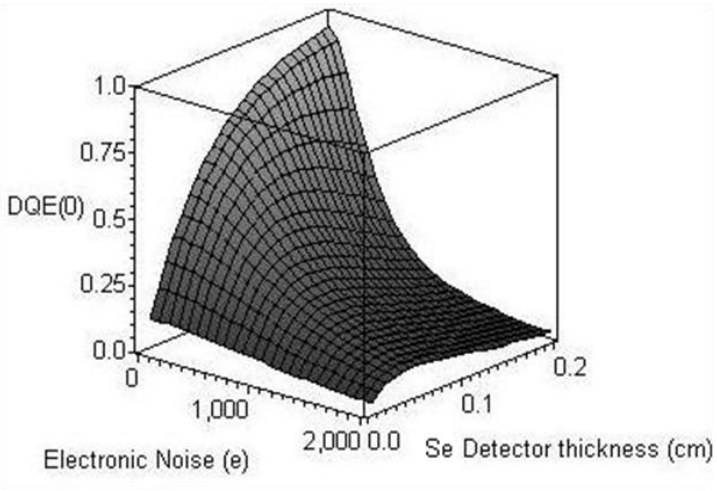


Figure 4.12. DQE(0) versus electronic noise and Se detector thickness at a constant bias of 10kV and a exposure of 0.1 μR.

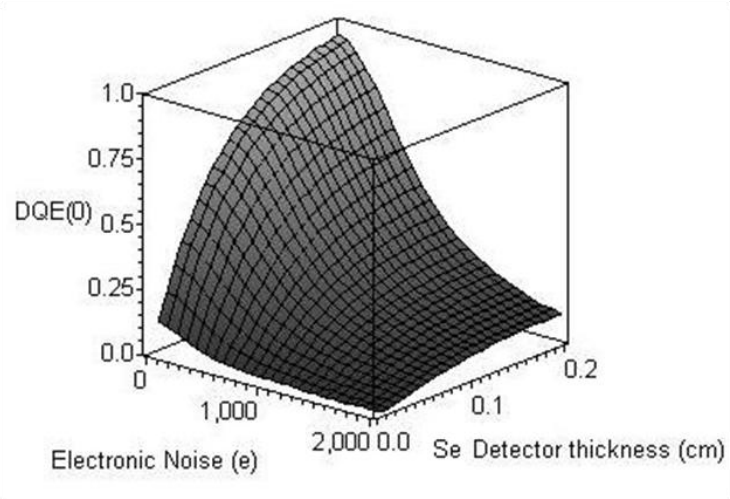


Figure 4.13. DQE(0) versus electronic noise and Se detector thickness at a constant field of 10V/μm and a exposure of 0.1 μR.

Figure 4.14 presents a graph of DQE(0) as a function of electronic noise (N_e) and exposure for a pixel area of 150µm x 150µm, a detector thickness of 1mm, and an electric field of 10V/µm.

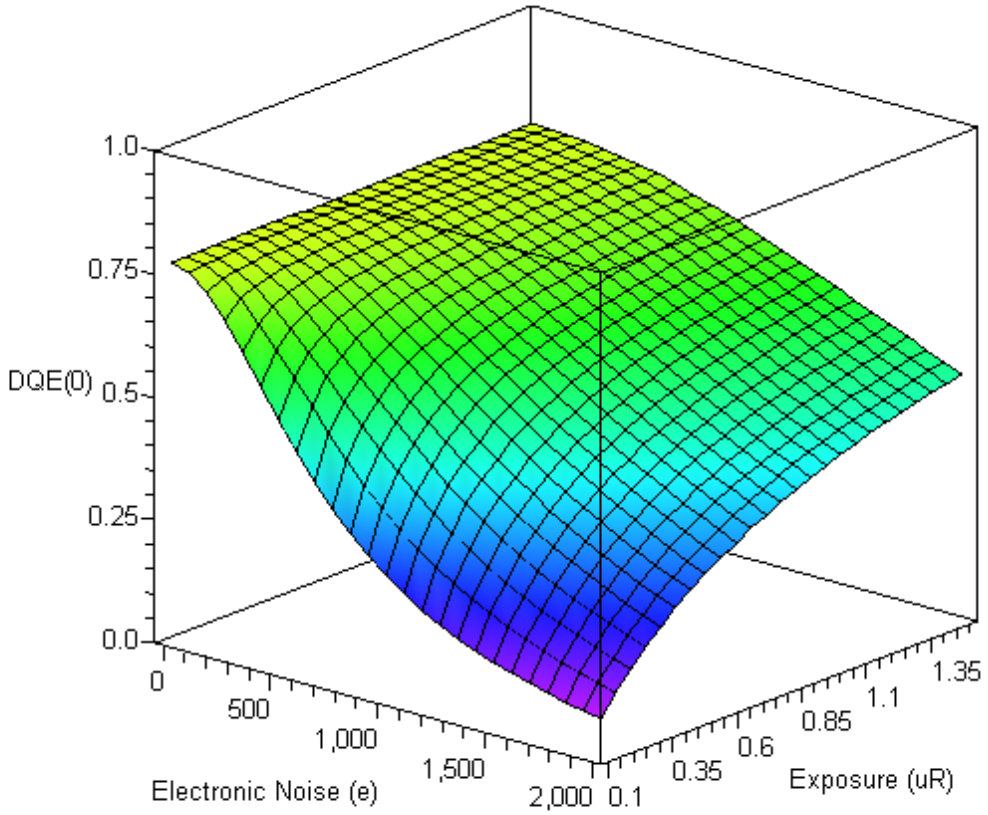


Figure 4.14. DQE(0) versus electronic noise and exposure for an electric field of 10V/µm and a pixel area of 150µm x 150µm.

Figure 4.15 and Figure 4.16 present cross-sections of Figure 4.14 for various levels of electronic noise and exposure, respectively. Both graphs are plotted for a pixel area of 150µm x 150µm, a detector thickness of 1mm, and an electric field of 10V/µm. As can be seen from Figure 4.14 and Figure 4.15, considerable improvements in DQE(0) can be obtained at all fluoroscopic exposures for electronic noise levels of 500 electrons and below.

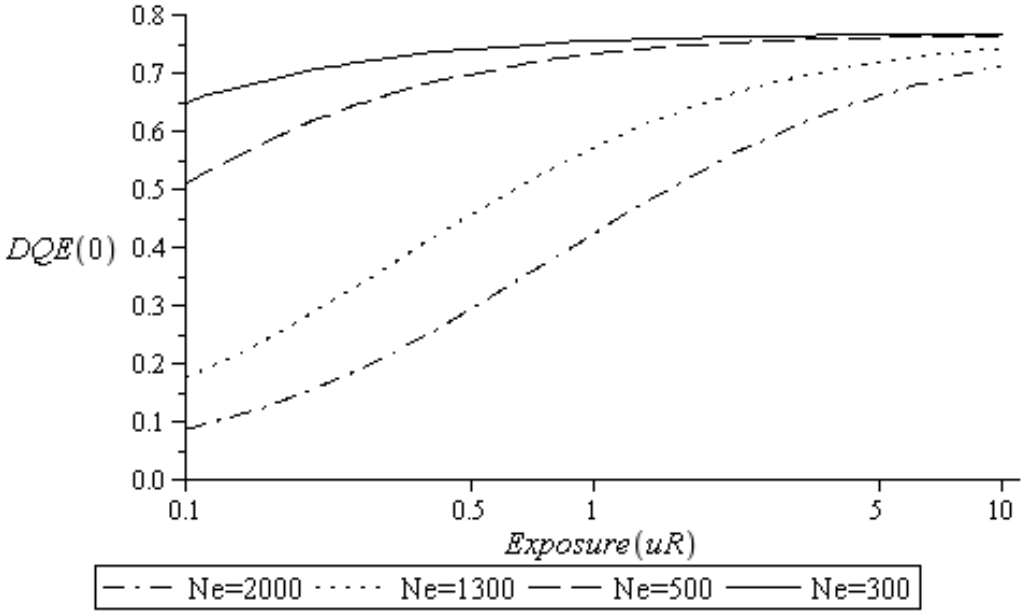


Figure 4.15. DQE(0) versus exposure for electronic noise levels of 2000, 1300, 500, and 300 electrons.

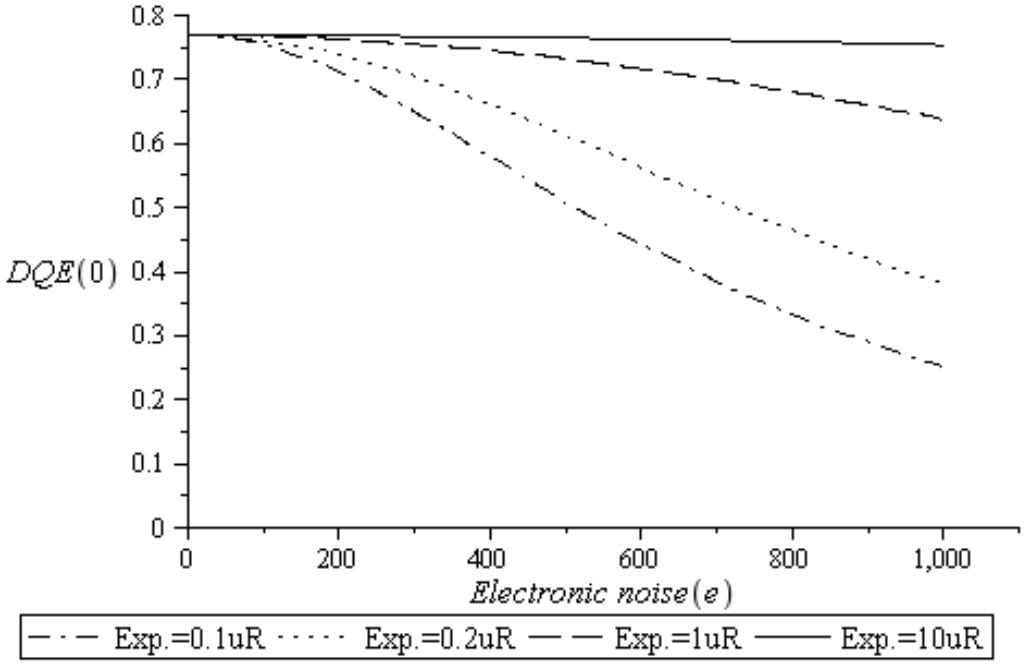


Figure 4.16. DQE(0) versus electronic noise for X-ray exposures of 0.1, 0.2, 1, and 10µR.

Figure 4.17 presents a graph of DQE(0) as a function of X-ray exposure for electronic noise levels of 400 electrons and 1300 electrons for various pixel areas. A detector thickness of 1mm and an electric field of 10V/µm are used for all the curves of Figure 4.17. At the lowest fluoroscopic exposure of 0.1µR, a detector with 400 electrons of electronic noise (input referred) and a pixel area of 100µm x 100µm outperforms a detector with 1300 electrons of electronic noise and a pixel area of 250µm x 250µm (more than 6x greater area).

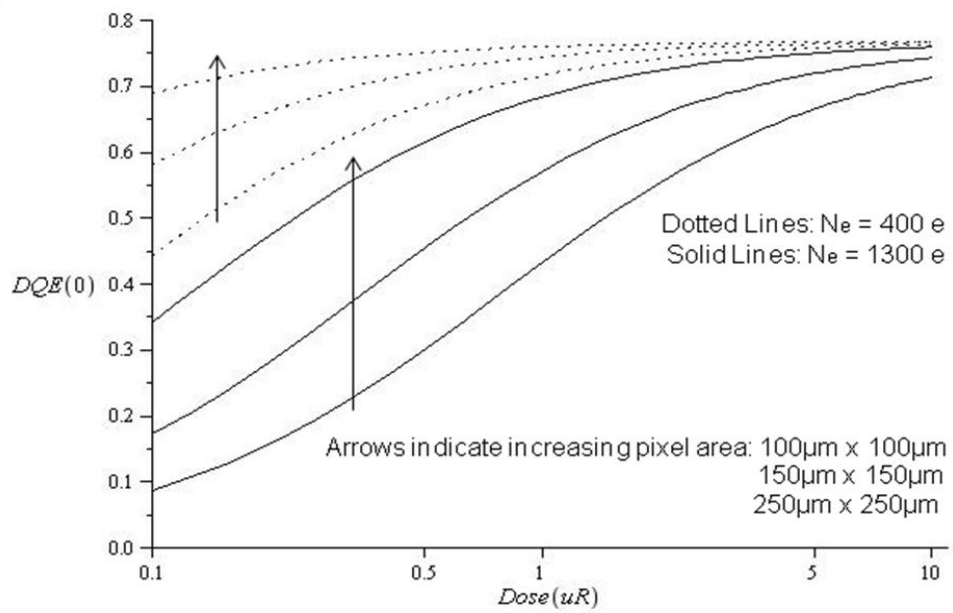


Figure 4.17. DQE(0) versus exposure for electronic noise levels of 400 and 1300 electrons using pixel areas of 100µm x 100µm, 150µm x 150µm, and 250µm x 250µm.

In the next section, TFT and pixel level noise testing are discussed.

5 TFT and Pixel Noise Testing

The following test structures have been designed for experimental verification of the noise optimization theory and simulations:

- Single transistor tests with varying W/L ratios
- 3-TFT pixel tests with varying W/L ratios and storage capacitances, C_s

Single transistor tests are used in order to validate and extract parameters to be used in the a-Si TFT thermal and flicker noise models previously presented. The 3-TFT pixel tests are conducted in order to experimentally verify the noise optimization model previously presented using the thermal and flicker noise parameters extracted from the single TFT tests.

5.1 Single TFT Noise Testing

Single TFT tests have been designed with the following W/L ratios (in microns) to characterize thermal and flicker noise: 100/50, 100/20, 100/10, 100/5. The sections that follow present the methodology used to calibrate the test setup, the TFT device parameters used to extract noise parameters, and the test setup, methodology and results for single TFT thermal and flicker noise tests.

5.1.1 Calibration of Test Setup

In order to calibrate the test setup, low-noise metal film resistors with known resistance values were measured for their thermal noise contribution. The metal film resistor was placed in a metal shield with the shield grounded in order to protect the setup from 60 Hz power line noise and from the surrounding electromagnetic interference. One end of the resistor was grounded, while the other end was connected, through a BNC cable, to the input of a low-noise transimpedance (current) amplifier (EG&G 5182). The transimpedance amplifier was operated using rechargeable NiMH batteries to reduce the noise (particularly power line noise). The AC output of the transimpedance amplifier was then connected to an Agilent 4395A spectrum analyzer. Attempts were made to limit the lengths of all BNC connections in order to reduce undesirable noise. The test setup is illustrated in Figure 5.1.

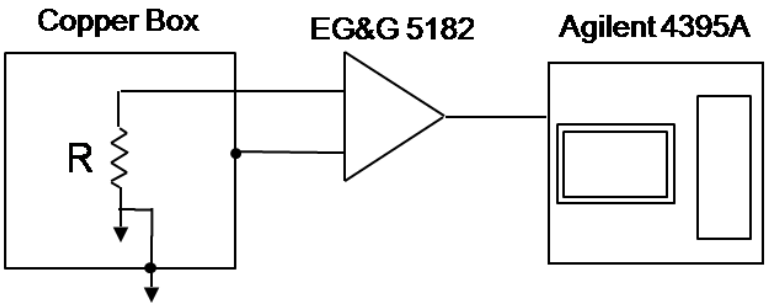


Figure 5.1. Noise calibration test setup

Four resistor values were used in the calibration of the test setup: R = 15.33 kΩ, 106.8 kΩ, 955.4 kΩ, 7.49 MΩ (the 7.49 MΩ resistor was not a low-noise metal film resistor, but instead a regular ceramic resistor). To test the noise floor of the transimpedance amplifier the input was grounded. The highest gain setting of the transimpedance amplifier (10^{-8} A/V) also corresponds to the lowest background noise setting (15fA/Hz$^{-1/2}$), however, this setting is bandlimited by the 3dB frequency of the transimpedance amplifier to about 1 kHz; therefore, noise measurements were taken at 800Hz. The thermal noise of the resistors was calculated in Volts/Hz$^{-1/2}$ to match the output setting chosen on the spectrum analyzer. The noise voltage of the resistors can be calculated as follows:

$$\bar{v} = \sqrt{\overline{i^2}}\, A_{trans} A_{sa} = \sqrt{\frac{4kT}{R}} \frac{1}{10^{-8}} \frac{1}{10} \quad \text{V/Hz}^{-1/2} \tag{5.1}$$

where k is Boltzmann's constant, T is the temperature in Kelvins, R is the resistance, A_{trans} is the transimpedance gain, and A_{sa} is the gain (attenuation) from the transimpedance output to the spectrum analyzer input. The measured noise voltage spectral density for the four test resistors agrees well with the calculated (expected) values as shown in Table 5.1.

Table 5.1. Noise spectral density measurement results of resistors for calibration of test setup

Resistance	Calculated Noise Spectral Density	Measured Noise Spectral Density
Input shorted	150 nV/Hz$^{-1/2}$ (from datasheet)	61.6 nV/Hz$^{-1/2}$
7.49 MΩ	464 nV/Hz$^{-1/2}$	490 nV/Hz$^{-1/2}$
955.4 kΩ	1.3 μV/Hz$^{-1/2}$	1.35 μV/Hz$^{-1/2}$
106.8 kΩ	3.9 μV/Hz$^{-1/2}$	4.05 μV/Hz$^{-1/2}$
15.33 kΩ	10.3 μV/Hz$^{-1/2}$	10.2 μV/Hz$^{-1/2}$

5.1.2 Extracting TFT device parameters for noise testing

The single TFTs used for noise testing included the devices presented in section 3.5. As previously mentioned, the device dimensions used for parameter extraction and subsequent calculations were based on actual device dimensions measured after fabrication as presented in Table 5.2.

Table 5.2. Device dimensions measured on fabricated TFTs used for noise testing

	Drawn (µm)	Measured (µm)
Length (L)	5	5.9
	10	10.9
	20	20.6
	50	51.9
Width (W)	100	99.1

Thermal noise tests were conducted in the linear regime and the device parameters were extracted before tests were conducted. Device parameters were extracted at a drain-source voltage value of 0.5V. Because actual thermal noise tests were conducted at a drain-source voltage of 0V, the effect of mobility degradation due to gate voltage changes was not taken into account for thermal noise calculations.

Table 5.3. Extracted parameters at V_{DS} = 0.5V for thermal noise calculations

Length drawn (µm)	$\mu_{eff,lin}$ (cm^2/Vs)	$V_{T,lin}$ (V)
5	0.049	4.6
50	0.310	4.45

Due to the non-negligible source-drain contact resistances, the mobility and threshold voltage of the TFTs change as a function of gate voltage. Flicker noise tests were conducted in the linear regime at a source-drain voltage of 1.0V, and in the saturation regime for $V_{DS} = V_{GS}$. Table 5.4 and Table 5.5 list the extracted mobility and threshold voltage for different TFT device dimensions as a function of gate voltage in the linear and saturation regimes, respectively.

Table 5.4. Extracted parameters at V_{DS} = 1.0V for flicker noise calculations

Length drawn (μm)	V_G (V)	$\mu_{eff,lin}$ (cm^2/Vs)	$V_{T,lin}$ (V)
5	6.92	0.077	4.00
	9.63	0.066	5.90
	15.31	0.037	4.00
	18.8	0.045	5.90
10	5.3	0.132	4.00
	6.92	0.138	4.00
	9.63	0.118	4.00
	15.31	0.079	4.00
	18.8	0.071	5.50
20	6.92	0.193	4.30
	9.63	0.187	5.80
	15.31	0.108	4.30
	18.8	0.119	5.80
50	5.3	0.318	4.40
	6.92	0.318	4.40
	9.63	0.282	4.40
	15.31	0.224	4.40
	18.8	0.183	4.40

Table 5.5. Extracted parameters at V_{DS} = V_{GS} for flicker noise calculations

Length drawn (μm)	V_G (V)	$\mu_{eff,sat}$ (cm^2/Vs)	$V_{T,sat}$ (V)
5	4.75	0.09	2.00
	9.45	0.194	2.70
	14.21	0.36	5.20
	19.11	0.563	7.40
10	9.45	0.16	4.60
	14.21	0.303	6.70
	19.11	0.49	9.00
20	9.45	0.23	3.50
	14.21	0.336	4.90
	19.11	0.49	6.90
50	9.45	0.423	4.10
	14.21	0.49	4.70
	19.11	0.578	5.60

5.1.3 Thermal noise

Thermal noise measurements were only conducted for TFTs in the linear regime since it was not possible to bias the TFTs with a large drain source voltage while attempting to read the thermal noise. Due to the very small noise current produced by the TFTs (due to their very large on resistances), it was necessary to use the largest gain/lowest noise setting of our low-noise current amplifier. The maximum allowable DC bias current is 90 nA for the largest gain setting, which did not allow for thermal noise measurements in the saturation regime where bias currents were orders of magnitude higher. Based on the results of the thermal noise measurements in the linear regime, which closely followed theory, one can expect that the saturation regime would similarly produce predictable results.

Even with small DC voltages (0.5 V) connected to the drain of the TFT, the flicker noise dominated thermal noise as expected. From the flicker noise measurements, frequencies where the flicker noise would approach the thermal noise level would occur at approximately 100 kHz-1 MHz, depending on the biasing conditions and TFT device dimensions. Such large frequencies were not within the 3dB frequency of the low-noise current amplifier, and would make some of the thermal noise measurements impossible as they would fall below the noise floor of the amplifier. Thus, in order to measure the thermal noise we grounded the drain of the TFT and connected the source to the virtual ground of the low-noise current amplifier.

The gate bias of the TFT was then modulated with two 9V alkaline batteries connected in series through a network of low-noise metal film transistors. The effect of the gate bias is to change the channel resistance of the TFT by modulating the number of charge carriers within the channel, and thus changing the thermal noise detected by the spectrum analyzer. Seen in this way, our setup is identical to that used to initially calibrate our test setup with the various test resistors. The voltages were applied to the TFTs directly on the fabricated wafer through micropositioners (i.e. using a triaxial probe station). The measurement setup for determining the TFT thermal noise is shown in Figure 5.2.

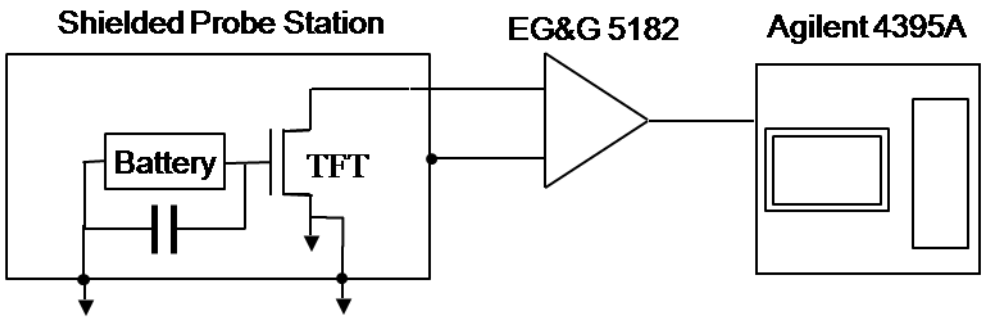


Figure 5.2. Test setup for measuring TFT thermal noise

Noise measurements were made at a frequency of 500 Hz and averaged over 50 samples. Using the noise voltage spectral density values measured, the resistance in the linear regime was found according to (3.1) and compared to the values calculated from the equation for resistance in the linear regime as shown in (5.2).

$$r_{ds} = \frac{L}{\mu_{eff,lin} C_{ox} W \left(V_{GS} - V_{T,lin}\right)} \tag{5.2}$$

The TFT parameters used in the calculations for r_{ds} were previously shown in Table 5.2 and Table 5.3. The calculated long-channel transistor resistance (L=50μm) and the short-channel transistor resistance (L=5μm) from the extracted I-V parameters follows the thermal noise measured resistance values very well, which is demonstrated in Table 5.6 and Table 5.7.

Table 5.6 Calculated Value from extracted parameters from IV curve

Channel Length (μm)		Resistance (Ω)			
Drawn	Measured	V_G=5.17 V	V_G=9.63 V	V_G=14.17 V	V_G=18.8 V
5	5.9	7.66×10^7	8.69×10^6	4.56×10^6	3.08×10^6
50	51.88	8.37×10^7	1.16×10^7	6.20×10^6	4.20×10^6

Table 5.7 Measured Value using thermal noise measurements with Spectrum Analyzer

Channel Length (μm)		Resistance (Ω)			
Drawn	Measured	V_G=5.17 V	V_G=9.63 V	V_G=14.17 V	V_G=18.8 V
5	5.9	7.77×10^7	7.98×10^6	5.62×10^6	3.74×10^6
50	51.88	8.20×10^7	1.12×10^7	8.46×10^6	4.20×10^6

5.1.4 Flicker noise

Due to the low frequency nature of flicker noise, samples were acquired at a much slower rate with the spectrum analyzer. The sweep/sample rate for the spectrum analyzer was ~ 11s, and the frequency bandwidth was from 1 Hz to 1000 Hz. Tests were run for 30 min (>100 samples), during which time the bias current was monitored. Transistor characteristics were taken before and after flicker noise measurements. During the period of testing, the bias current and threshold voltage changed by at most 10% on some devices. To compensate for the change, the bias currents and threshold voltages were averaged over the duration of the tests for the noise coefficient calculations. The test setup used for the flicker noise tests is identical to the thermal noise tests except that now a voltage is applied to the drain of the TFTs of either V_D=1V (linear) or V_D=V_G (saturation). The purpose of these tests is to characterize the flicker noise in the linear and saturation regimes for our TFTs in order to apply them to the noise model simulations used to compare to the pixel and array noise measurements. This characterization includes a determination of whether the TFTs follow the mobility fluctuation (Hooge) model or the number carrier fluctuation (McWhorter) model, followed by an extraction of the appropriate model parameters to enable noise prediction using our theoretical model.

5.1.4.1 Linear regime

Flicker noise measurements were conducted in the linear regime for the gate voltages indicated in Table 5.4. The drain current power spectral density, $S_{ID}(f)$, is plotted as a function of frequency for several values of gate-source voltage, V_{GS}, for the TFT with gate length L=10 μm as shown in Figure 5.3.

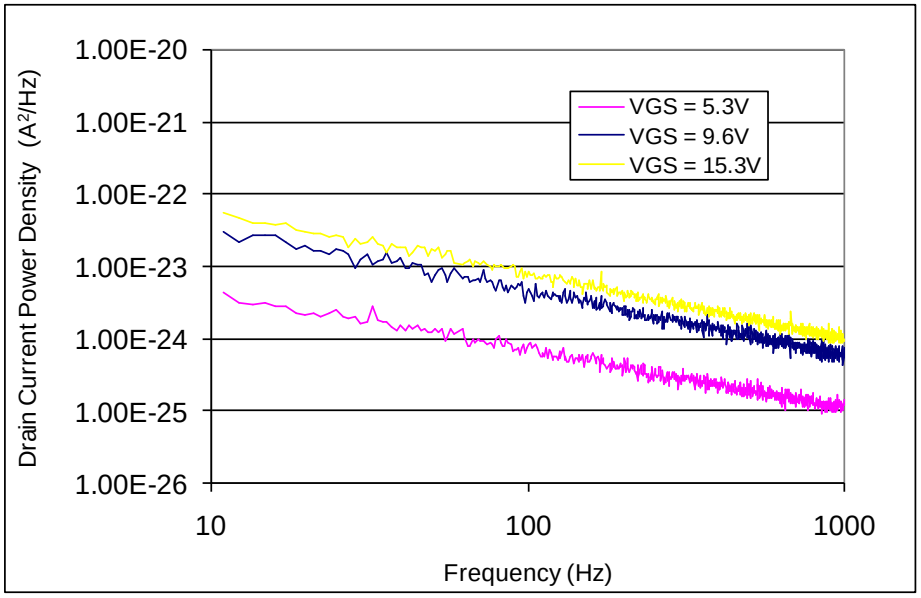
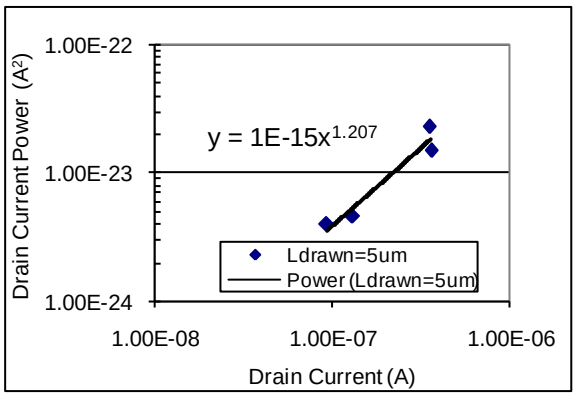
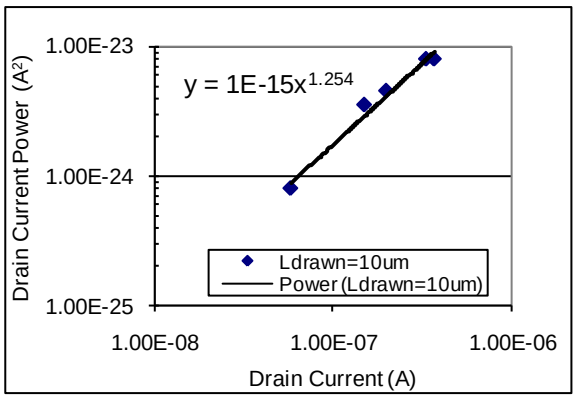


Figure 5.3. Drain current power spectral density vs. frequency for several values of gate-source voltage, V_{GS}, for a TFT with gate length L=10 µm

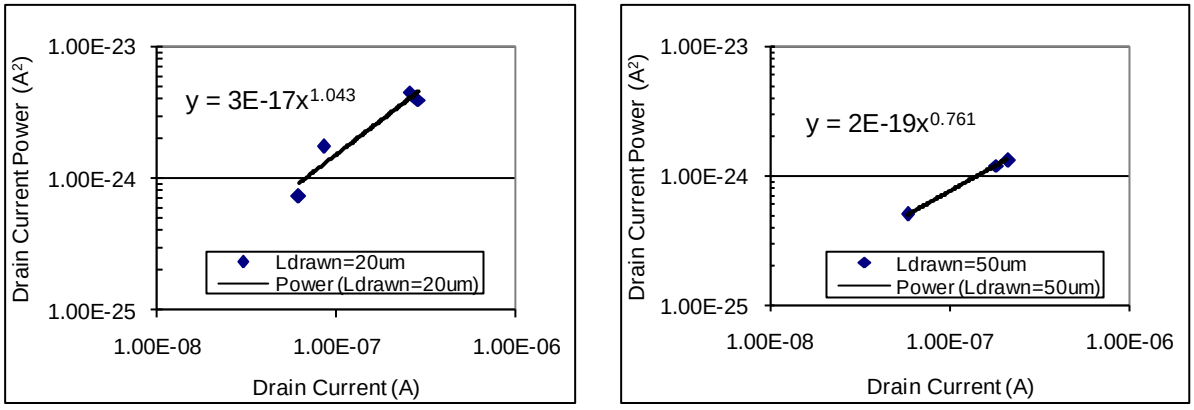
In order to determine what noise model our TFTs follow, we plot the drain current flicker noise power, S_{ID}, at a frequency of 100Hz versus the measured TFT drain bias current, I_D. We expect a linear relationship between drain current and the drain current flicker noise power (slope of 1.0 for power series) for devices that follow Hooge's theory (mobility fluctuation model). As seen in Figure 5.4, the relationship between drain current and drain current power varies from $x^{0.76}$ to $x^{1.25}$ for different gate lengths.



(a)



(b)



(c) (d)

Figure 5.4. S_{ID} vs. I_D at a frequency of 100Hz for different gate lengths. (a) L= 5 µm (b) L=10 µm (c) L=20 µm (d) L=50 µm.

To further test if indeed our flicker noise results predominantly from mobility fluctuations (Δµ) or carrier number fluctuations (Δn), it is suggested that from the plots of $S_{ID}(f)/I_D^2$ vs. I_D and $(g_m/I_D)^2$ vs. I_D, one can discriminate between the different noise origins [73]. If the two plots are parallel (have the same power series slope), then the *1/f* noise is due to fluctuations in the number of carriers. When the two plots diverge, the departure of the noise level from the $(g_m/I_D)^2$ plot is attributed to extra correlated mobility fluctuations model**,** Δn-Δµ. Finally, if the normalized noise varies as the inverse of the drain current form weak to strong inversion, then the mobility fluctuations dominate.

Plots of $S_{ID}(f)/I_D^2$ vs. I_D give a slope ranging from -0.74 to -1.23 for devices of varying gate length, while the plots of $(g_m/I_D)^2$ vs. I_D give a slope ranging from -2.08 to -3.08, as shown in Figure 5.5 and Figure 5.6, respectively. Clearly the two plots are not parallel, so we can rule out the origin of the noise being attributed to the carrier number fluctuation model. Furthermore, taking a look at $S_{ID}(f)/I_D^2$ vs. I_D, we see that the slope averages around -1.13 for all test devices (i.e. varies as inverse of drain current), and thus mobility fluctuations dominate.

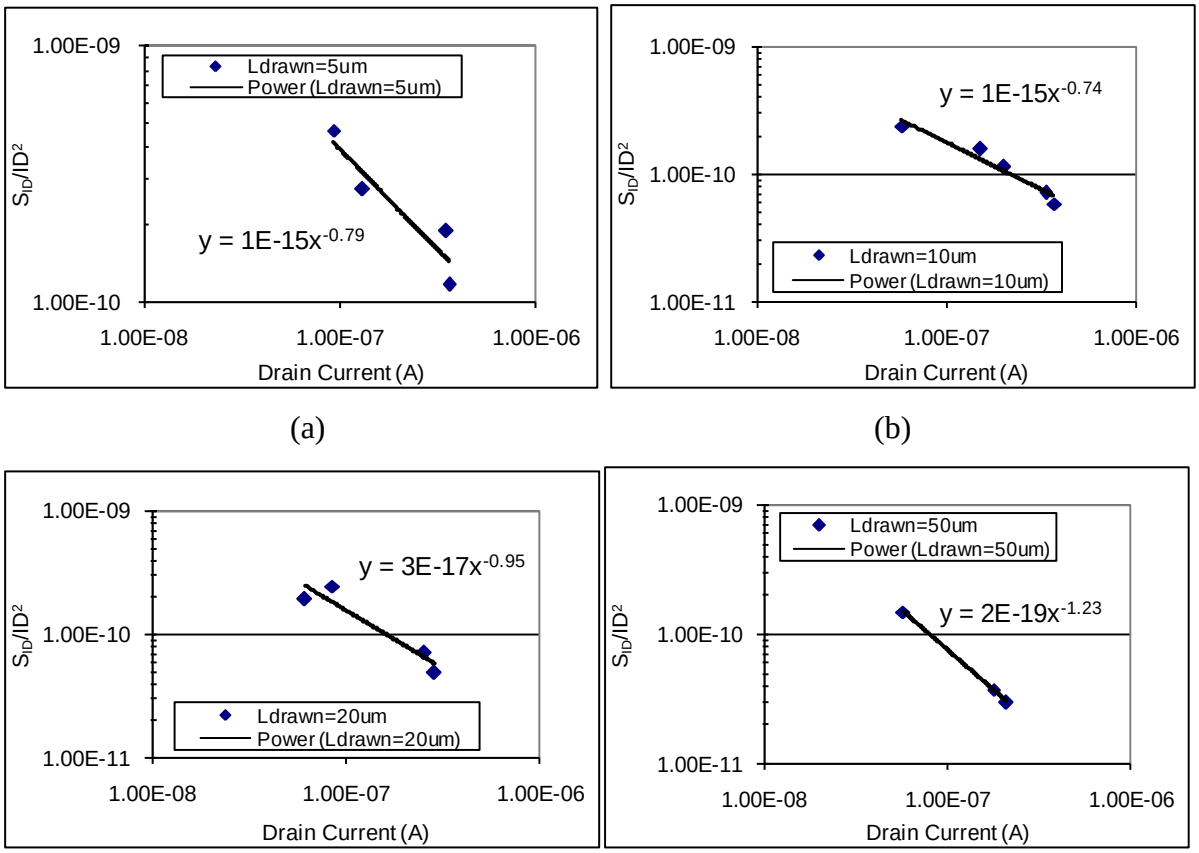
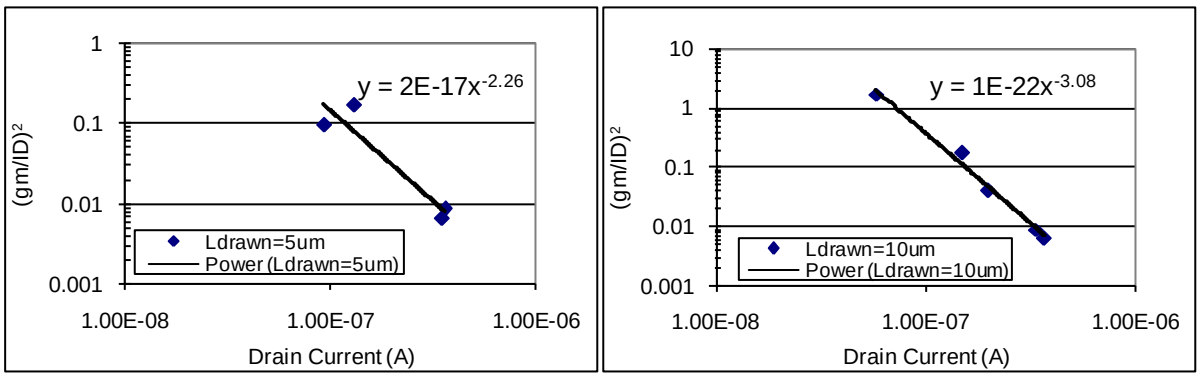
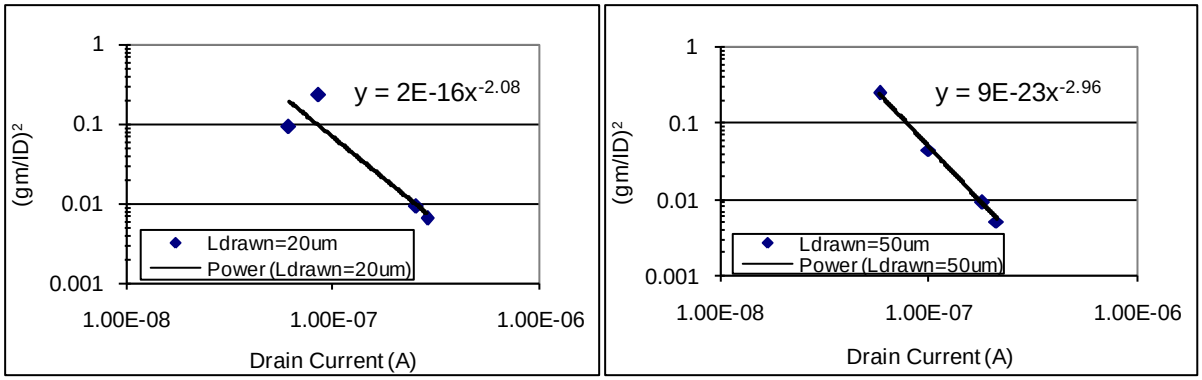


Figure 5.5. $S_{ID}(f)/I_D^2$ vs. I_D at a frequency of 100Hz for different gate lengths. (a) L= 5 µm (b) L=10 µm (c) L=20 µm (d) L=50 µm.





(c) (d)

Figure 5.6. $(g_m/I_D)^2$ vs. I_D at a frequency of 100Hz for different gate lengths. (a) L= 5 µm (b) L=10 µm (c) L=20 µm (d) L=50 µm.

Plotting the Hooge parameter for the linear regime, $\alpha_{H,lin}$, versus the applied gate voltage gives the plot of Figure 5.7. As can be seen from the plot, the Hooge parameter varies considerably with changing gate length, which is likely due to the high source/drain contact resistance.

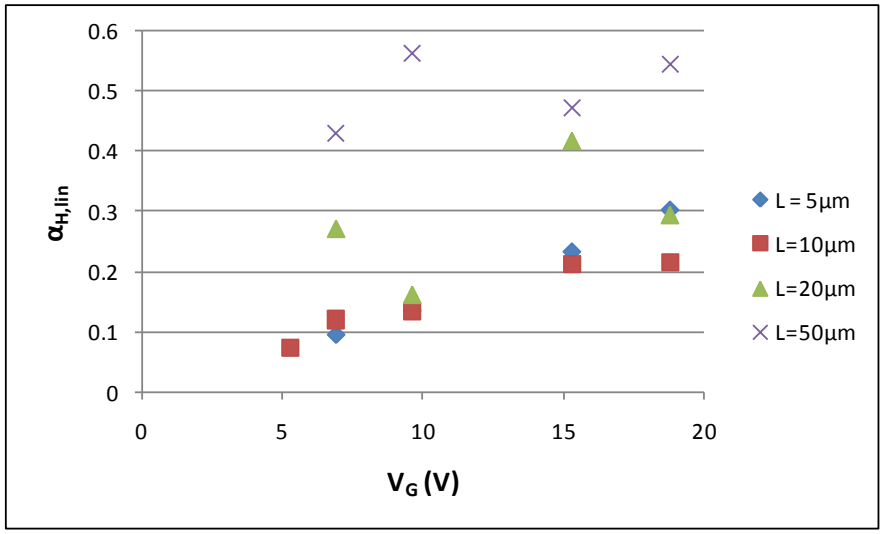


Figure 5.7. Hooge parameter for the linear regime vs. applied gate voltage for TFTs with varying gate lengths.

For gate lengths from 5µm to 10µm, we can average the Hooge parameter to be around 0.2, which is an order of magnitude larger than reported in literature [57]. The cause for such a high Hooge parameter value is unknown. The mobility fluctuation model that has been used

to predict flicker noise and extract the Hooge parameter has not fully taken into account the channel access resistances (series drain and source resistances).

We can plot the drain current noise power against V_{GS}-V_T to see if channel access resistance plays an important role in determining the overall flicker noise density.

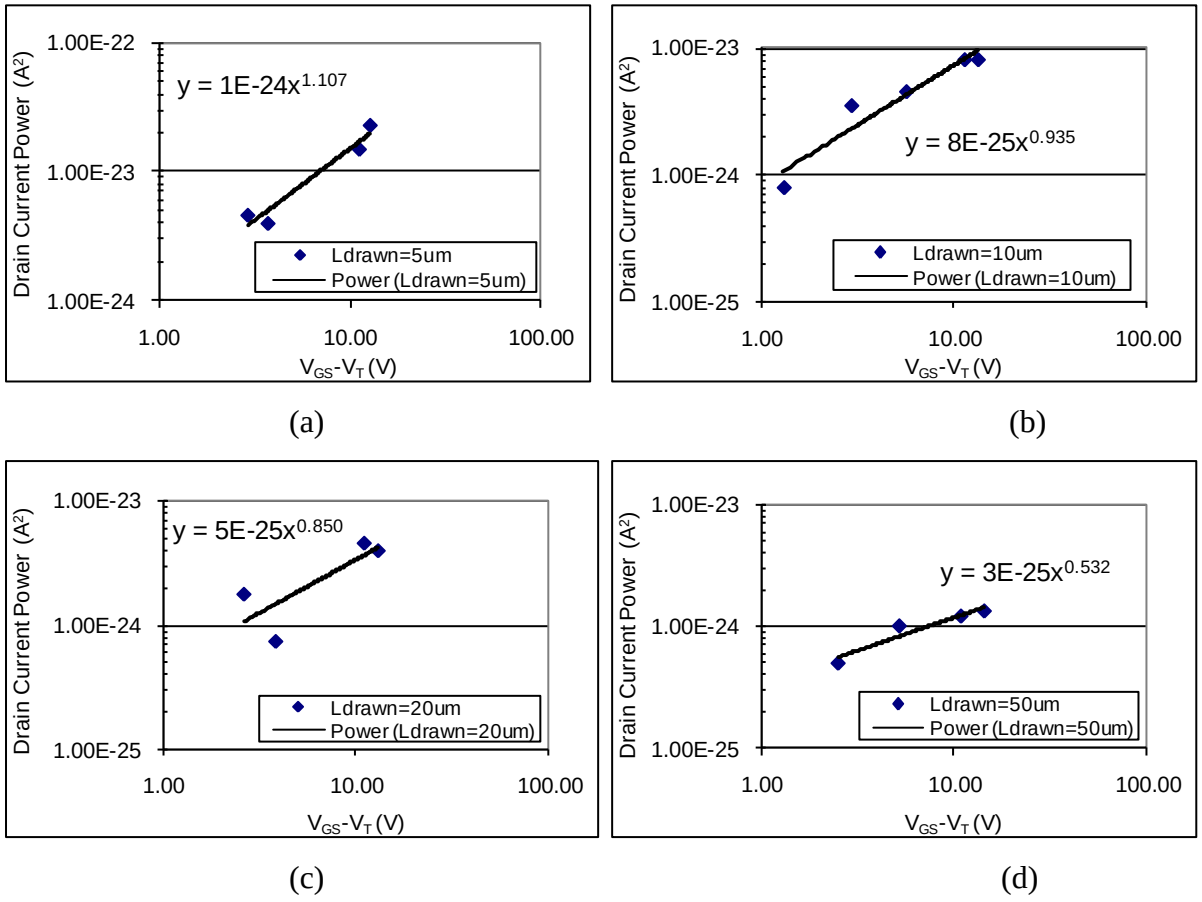


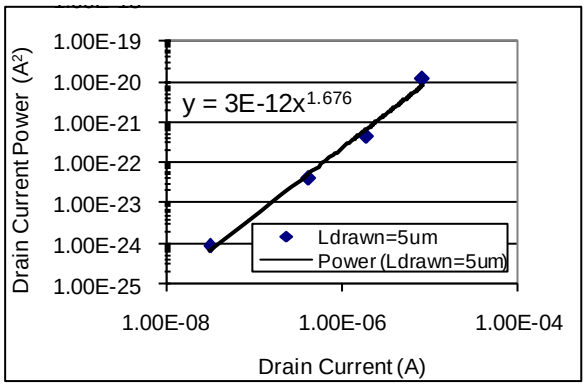
Figure 5.8. S_{ID} vs. V_{GS}-V_T at a frequency of 100Hz for different gate lengths. (a) L= 5 µm (b) L=10 µm (c) L=20 µm (d) L=50 µm.

When channel access resistance flicker noise plays a role in the overall flicker noise density, it has been noticed that the slope of drain current power curve increases with increasing V_{GS}-V_T [57]. As evidenced by the plots of Figure 5.8, this is not the case, which could indicate that the intrinsic channel contribution to the flicker noise dominates the overall flicker noise in all regimes (i.e. from weak inversion to strong inversion); however, given that the Hooge parameter is supposed to be a constant for a given technology independent of the device

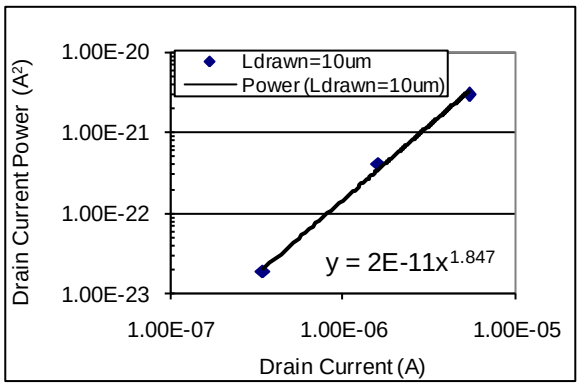
dimensions, it would appear from the Hooge parameter distribution plot of Figure 5.7 that access resistance does play a significant role at low V_{DS} values. Such a conclusion is consistent with our previous measurements which indicate a significant contact resistance for our TFTs.

5.1.4.2 Saturation regime

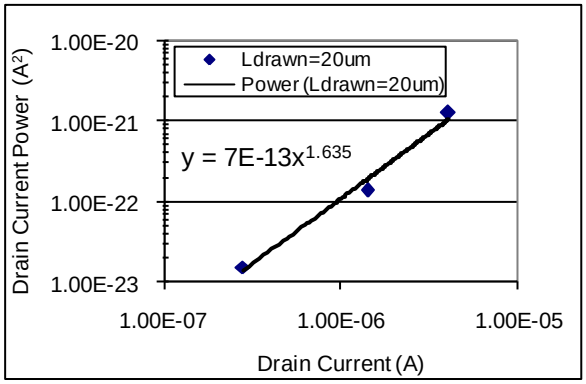
Flicker noise measurements were conducted in the saturation regime for the gate voltages indicated in Table 5.5. According to the mobility fluctuation model, S_{ID} varies as $I_D^{3/2}$ in the saturation regime, whereas according to the carrier number fluctuation model S_{ID} varies as I_D in the saturation regime. For most of the transistors tested, the slope of I_D varied from 1.64 to 1.85 in the saturation regime, while for one device the value was closer to 0.83 as shown in Figure 5.9. The value around 0.83 more closely resembles the carrier number fluctuation model; however, since the same transistor did not exhibit behaviour associated with the carrier number fluctuation model for linear regime tests, it is less likely that in the saturation regime carrier number fluctuations would be the dominant *1/f* noise source. The discrepancy is likely due to a poor data point. The other measurements, while slightly higher than predicted by the model, could be attributable to *1/f* access resistance noise.



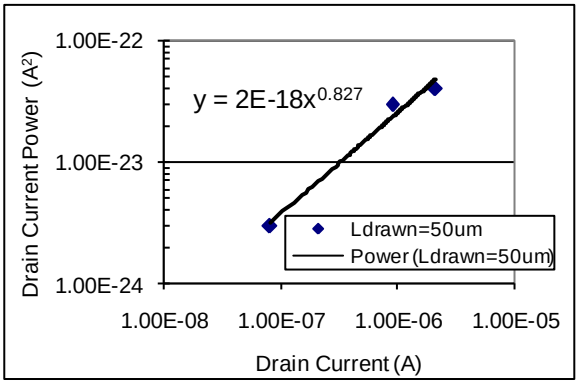
(a)



(b)



(c)



(d)

Figure 5.9. S_{ID} vs. I_D at a frequency of 100Hz for different gate lengths in saturation. (a) L= 5 µm (b) L=10 µm (c) L=20 µm (d) L=50 µm.

Plotting the Hooge parameter for the saturation regime, $\alpha_{H,sat}$, versus the applied gate voltage gives the plot of Figure 5.10. As can be seen from the plot, the Hooge parameter is around 0.1 for all gate lengths, which is an order of magnitude larger than reported in literature [57]. Since the Hooge parameter is constant for a given technology, it is considered as a quality indicator. The results show that the quality of the fabricated TFTs' intrinsic channel is poor since the Hooge model reflects bulk mobility fluctuations. Furthermore, the high access resistance noise cannot be ruled out as the cause of the large value of the Hooge parameter.

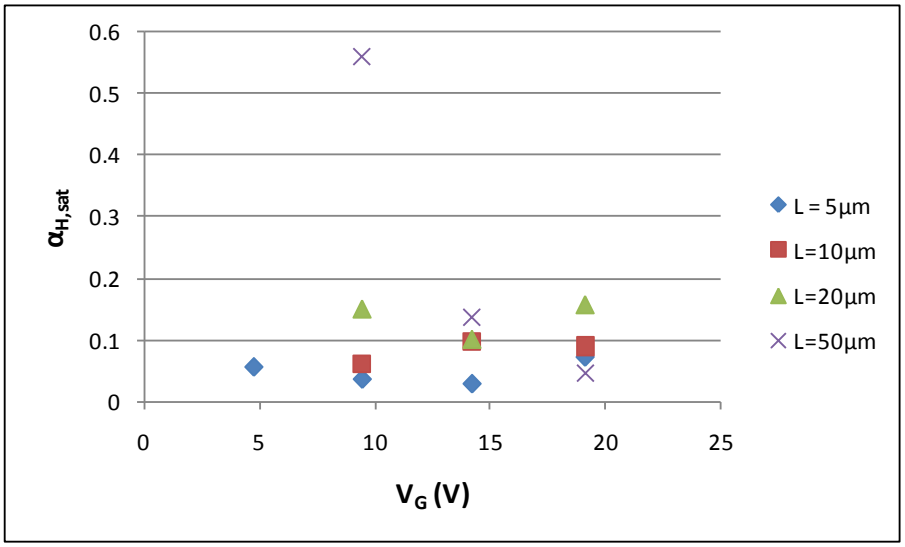


Figure 5.10. Hooge parameter for the saturation regime vs. applied gate voltage for TFTs with varying gate lengths.

5.2 Single Pixel Noise Testing

The 3-TFT pixels have constant RDP and RDC W/L ratios of 50/10 and 100/10, respectively. The AMP TFT has varying W/L ratios of: 10/20, 25/20, 50/20, 100/20; 10/10, 25/10, 50/10 100/10, 200/10; 5/5, 10/5, 25/5, 50/5, 100/5. Each AMP TFT pixel configuration is further varied with storage capacitances of 0, 25 fF, 100 fF, 500 fF, and 1000 fF.

5.2.1 Test Setup

In order to test the 3-TFT pixels, a PCB was designed to provide the various voltage levels and digital tests signals. There are many aspects to proper PCB design, and entire books have been written on the subject [74], however, for this work we were only concerned with a general methodology for the given application of pixel level testing. The design of the PCB is made considerably simpler since the pixels operate at relatively low frequencies (less than 10 MHz). This allows us to get by with a four-layer board, where the layers consists of a signal layer, ground layer, power layer, and signal layer as viewed from top to bottom.

The PCB has a multiple split power plane for the various different voltage levels required by the TFT pixel and readout circuitry. This is performed by laying down "tracks" ("tracks" are empty spaces on power planes) from near the input power connector or main filter capacitors and the opposite edge of the board. "Tracks" are also placed completely around the outer edge of board (i.e. no copper on outer edge). There is a separate analog and digital ground to prevent coupling of digital line noise into sensitive analog components. For components sharing the same ground plane, ground connections are stitched straight through to the ground plane in order to minimize track length. Lastly, surface mount components are used whenever possible in order to minimize interruption of power and ground planes. A block diagram of the main PCB along with a smaller external vector board for the charge amplifier and the NI card breakout board is shown in Figure 5.11.

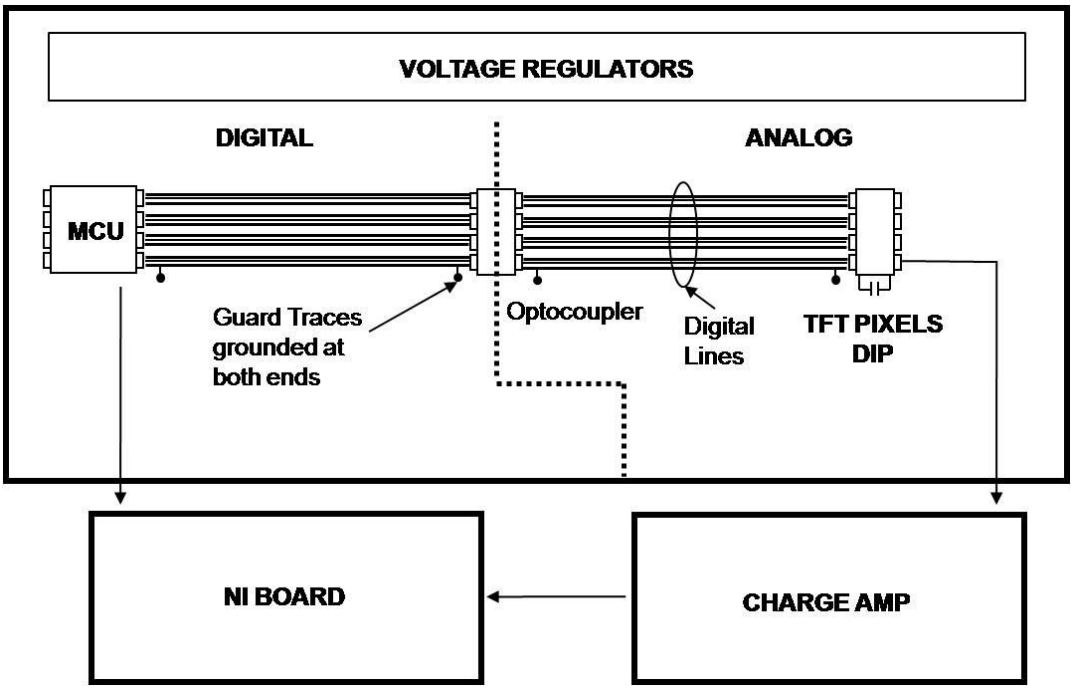


Figure 5.11. PCB Block Diagram

An external vector board was used for the charge amplifier since the PCB was originally designed to contain an IC charge amp array. Following the charge amp is the National Instruments (NI) breakout board which connects to an NI-6115 card containing a differential sample and hold, buffers, and 12-bit ADCs. A Freescale MC68HC908MR32 microcontroller unit (MCU) is used to generate the digital control/timing signals to the test pixels, charge amplifier, and NI card. HPCL-314J optocouplers are used to upconvert the 5V timing signals from the MCU to adjustable voltages up to 20V for use with the TFT pixels. The charge amp used is a Burr-Brown IVC102 surface mount device. The PCB test setup is shown in Figure 5.12 and a circuit diagram for the test setup is shown in Figure 5.13.

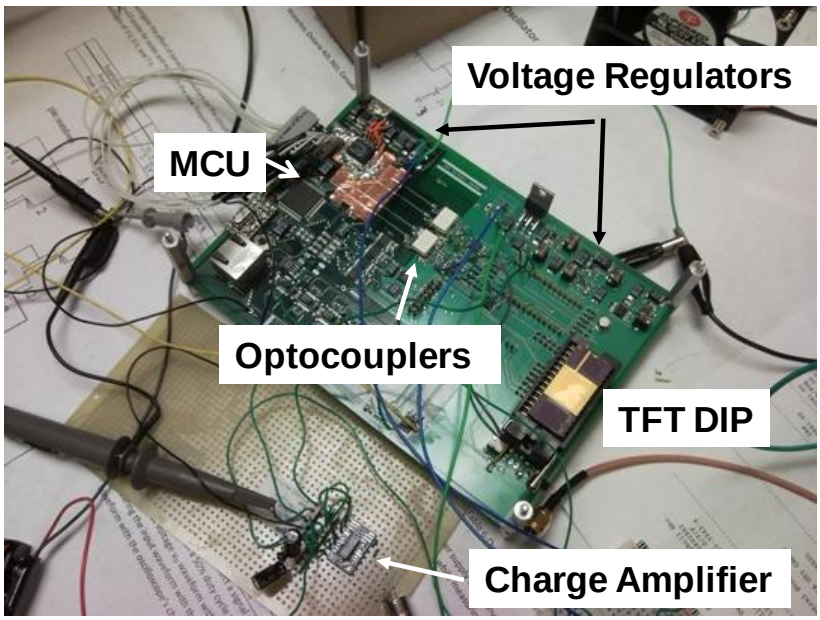


Figure 5.12. PCB Test setup

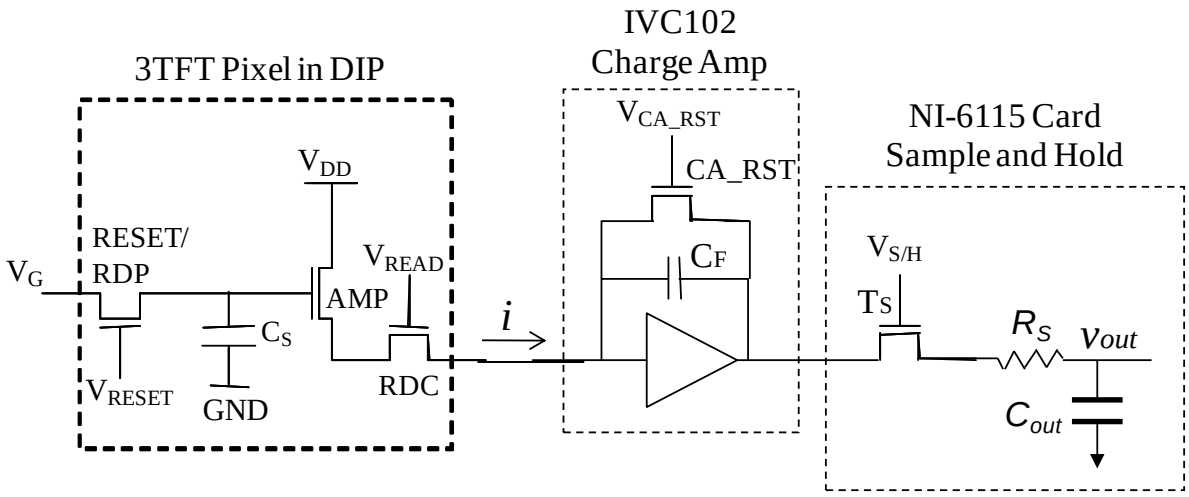


Figure 5.13. Circuit diagram for single pixel tests

The PCB was powered with high amp-hour rechargeable lead-acid batteries in order to minimize noise. The batteries, PCB, and charge amplifier were placed in a grounded large copper box to act as an electromagnetic shield (shown with lid open). The NI card breakout box and data acquisition card were located outside the copper box as shown in Figure 5.14.

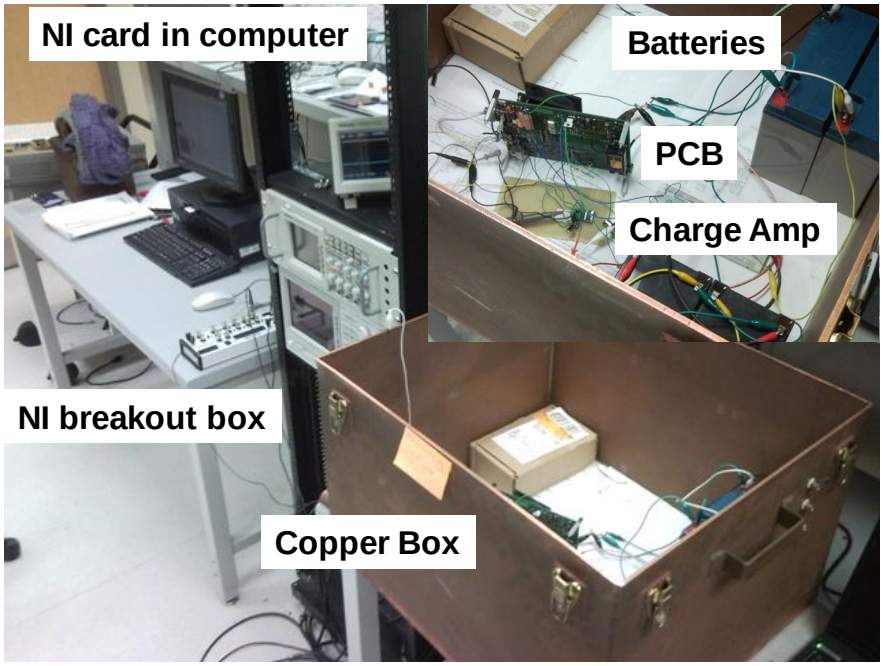


Figure 5.14. Full TFT Pixel Test Setup

Conventional double sampling, referred to in this thesis as double integration single sampling (DISS) (see Appendix C), was not possible because of the large amount of random noise generated by the charge amplifier after it was reset. Thus, only single integration double sampling (SIDS) (see Appendix C) was possible, which is not the sort of double sampling that would act to reduce flicker noise from sample to sample.

By far the largest noise source was from the charge amplifier and dataline itself. In order to separate the charge amplifier and dataline noise from the pixel noise, noise measurements were taken with the pixel readout switch RDC turned off and subtracted from noise measurements taken with the pixel readout switch RDC turned on.

5.2.2 Noise Results

In order to assess the performance of the noise model, noise results were obtained for transistors with six different W/L ratios (in microns): 10/10, 25/10, 50/10 100/10, 50/20 and 25/5. Table 5.8 illustrates simulated input referred pixel noise versus measured input referred pixel noise. The value of the Hooge parameter used for all the devices in the simulation was 0.06. The simulated flicker noise contribution of the AMP transistor dominates over all other

noise sources, so discrepancies between measured noise and simulated noise for the devices with W/L ratios of 25/5 and 50/20 are likely due to variations in flicker noise magnitude. The integration time used for the measurements and simulations was 30 μs. For the measured input referred noise values, output noise was measured, and the input referred noise values were calculated based on measured pixel parameters.

Table 5.8 Simulated input referred pixel noise versus measured input referred pixel noise for various W/L ratios.

Input Referred Noise (electrons)	**TFT W/L Ratio and Pixel Storage Capacitance**					
	25/5 C_s = 0 fF	**50/20 C_s = 25 fF**	**50/10 C_s = 25 fF**	**10/10 C_s = 25 fF**	**25/10 C_s = 0.5 pF**	**100/10 C_s = 0.5 pF**
AMP Thermal	67	180	156	65	399	393
AMP Flicker	2342	2409	3038	2628	10230	5063
RDC Thermal	11	18	17	17	59	74
RDC Flicker	15	19	20	13	63	79
Reset (KTC)	157	269	234	147	328	411
Reset Leakage Shot	72	102	102	48	72	144
Total pixel noise (simulated)	2348	2434	3052	2634	10249	5103
Measured pixel noise	1302	1639	2779	2745	14589	4869

The effect of integration time on the total input referred noise was also analyzed for the device with W/L ratio of 10/10 as shown in Table 5.9. Here the Hooge parameter was adjusted to a value of 0.075 to better fit the data.

Table 5.9 Simulated pixel noise versus measured pixel noise for various integration times.

Input Referred Noise (electrons)	**Integration Time (μs)**				
	3.5	**15**	**30**	**62**	**82**
AMP Thermal	193	93	65	62	54
AMP Flicker	3383	3172	3065	2724	2565
RDC Thermal	51	24	17	12	10
RDC Flicker	48	45	43	19	17
Reset (KTC)	147	147	147	147	147
Reset Leakage Shot	48	48	48	48	48
Total pixel noise (simulated)	3393	3177	3070	2728	2569
Measured pixel noise	3816	3533	2745	2433	2250

As can be seen from Table 5.9, longer integration times resulted in lower input referred noise due to the reduction in noise bandwidth. Table 5.9 illustrates simulated input referred pixel noise versus measured input referred pixel noise.

From Table 5.8 and Table 5.9, we can see that the measured and modelled pixel noise results are in reasonably good agreement. Taking the simulation results from Table 5.8 and applying double sampling (SIDS) yields lower noise results as shown in Table 5.10. By assuming a standard Hooge coefficient, α, of 0.01 instead of 0.06, the simulated noise results for our fabricated TFTs are reduced further as shown in the last row of Table 5.10.

Table 5.10 Simulated pixel noise improvements with double sampling and flicker noise reduction.

Total Noise from Pixel (electrons)	**TFT W/L Ratio and Pixel Storage Capacitance**					
	25/5 C_s = 0 fF	**50/20 C_s = 25 fF**	**50/10 C_s = 25 fF**	**10/10 C_s = 25 fF**	**25/10 C_s = 0.5 pF**	**100/10 C_s = 0.5 pF**
Single sample	2348	2434	3052	2634	10249	5103
Double sample (SIDS)	964	1033	1825	1657	6441	3235
SIDS with α = 0.01	625	705	791	696	2689	1441

It should be emphasized that the above results and extrapolated simulated results are for our fabricated TFTs. Simulated noise results based on TFTs with typical and optimal device characteristics gave better noise results as discussed in the previous chapter.

6 Imaging Array

This chapter presents the integration, testing, and results from the 64x64 pixel prototype APS pixel imaging array. All of the array-level testing in this chapter was carried out in collaboration with and at ANRAD Corp. of Montreal, Canada.

6.1 APS Imaging System Integration

Figure 6.1 shows the circuit schematic of the 4T a-Si pixel along with the interaction of the X-ray with the a-Se photoconductor, illustrating the charge readout from the collection electrode on the pixel (bottom electrode) to the charge amplifier.

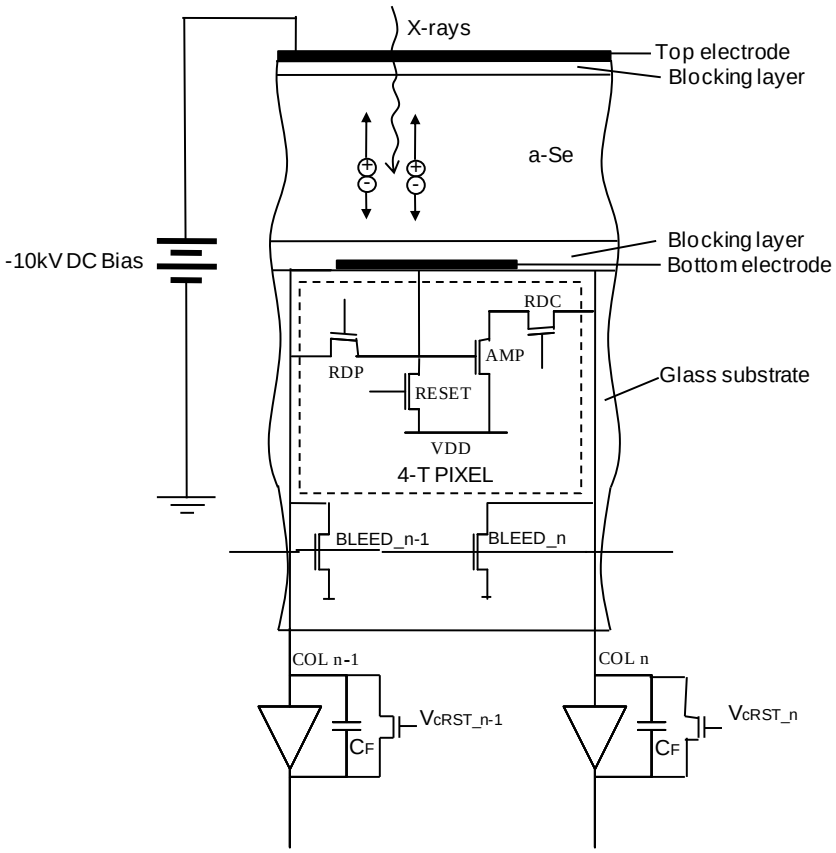


Figure 6.1. Circuit schematic of the 4T a-Si pixel with on-panel BLEED TFTs and off-panel CMOS column charge amplifiers.

The dashed line in represents a single 4-T pixel on the array. Charge is created within the a-Se due to X-ray interaction, which is then collected at the bottom electrode due to the presence of the electric field from the -10kV bias. The accumulated charge is then readout to external column charge amplifiers. The hole and electron blocking contact layers are designed to prevent charge injection into the a-Se layer, while allowing charge to exit the a-Se layer. Such blocking contacts thus serve to minimize excessive dark current which would otherwise drown out the signal charge at low X-ray doses. Column transistors labelled BLEED are incorporated onto the glass substrate with the a-Si pixel array in order to remove a large portion of the bias current to prevent the external CMOS column charge amplifiers from saturating.

The pixel array is coated with a 1mm thick layer of a-Se, followed by a top aluminum electrode, and a high voltage encapsulation layer. The pixel array is then bonded through bondpads on the glass substrate to external charge amplifier (CA) and gate driver (GD) chips using an anisotropic conductive film (ACF) process. The CA chips contain 128 separate column charge amplifiers along with 16-bit comparator based ADCs. The GD chip which has 256 separate TFT control lines (all of which are not used) provides two inputs to each pixel on the array. The external CA and GD chips are in turn plugged into sockets on a PCB which contains several FPGAs and associated control electronics for the CA and GD. The PCB outputs digital data to a frame grabber which interfaces with a computer to provide real-time imaging array data on a monitor. The block diagram for the APS imaging system is shown in Figure 6.2.

The major noise source in a-Si APS circuits is from the flicker noise of the TFTs. One way to reduce the magnitude of the flicker noise is to use hardware double sampling. In the readout scheme chosen, illustrated in Figure 6.3, RDC_m and RESET_m-1 (i.e. the APS READ TFT from the present row and RESET TFT from the previous row) share the same gate line. In this way, while the signal is being read-out through RDC, the previous row of pixels are also being reset. Such a design allows for a smaller pixel area, a reduction in the required number of gate drivers, and an increase in pixel reliability owing to the simpler pixel design. The cost of such a readout scheme is that pixel-level hardware double-sampling is not possible for the

gate drivers selected; therefore, software double-sampling must be employed using a dark field image to correct for any fixed pattern noise in the array and recover the signal (from the bias).

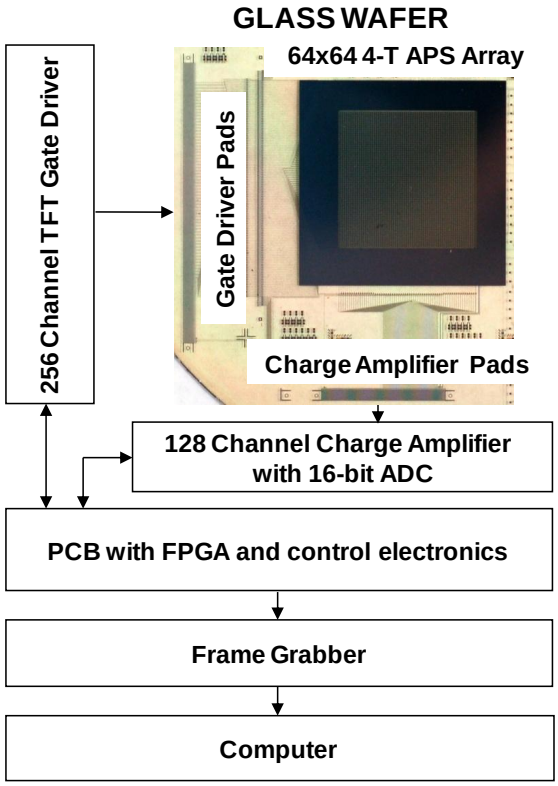


Figure 6.2. Block Diagram of APS Imaging System

In the present readout scheme, single integration double sampling (SIDS) is performed on the signal and the dark field image separately, and the difference between the two is accomplished in software. If multiple dark field images are averaged, then the white noise will be considerably reduced, such that the thermal noise and reset noise of the dark field image are negligible. The downside of software double-sampling is that the bandpass filtering effect on the low-frequency flicker noise is all but negated due to the long time interval between the dark field image and the signal image. The timing diagram of Figure 6.3 shows the output of the charge amplifier being sampled twice by signals V_{SH1} and V_{SH2}. The time difference of V_{SH1} and V_{SH2} determines the effective charge integration time, T_{int}, and the voltage difference is amplified by an adjustable gain differential amplifier whose output goes to a 16-bit ADC. Although SIDS does not reduce the effect of flicker noise in each

individual signal sample, it does perform correlated double sampling to remove the reset noise that appears across the charge amplifier feedback capacitor, C_F, which can be set at either 0.5pF, 1pF, 5pF, or 10pF.

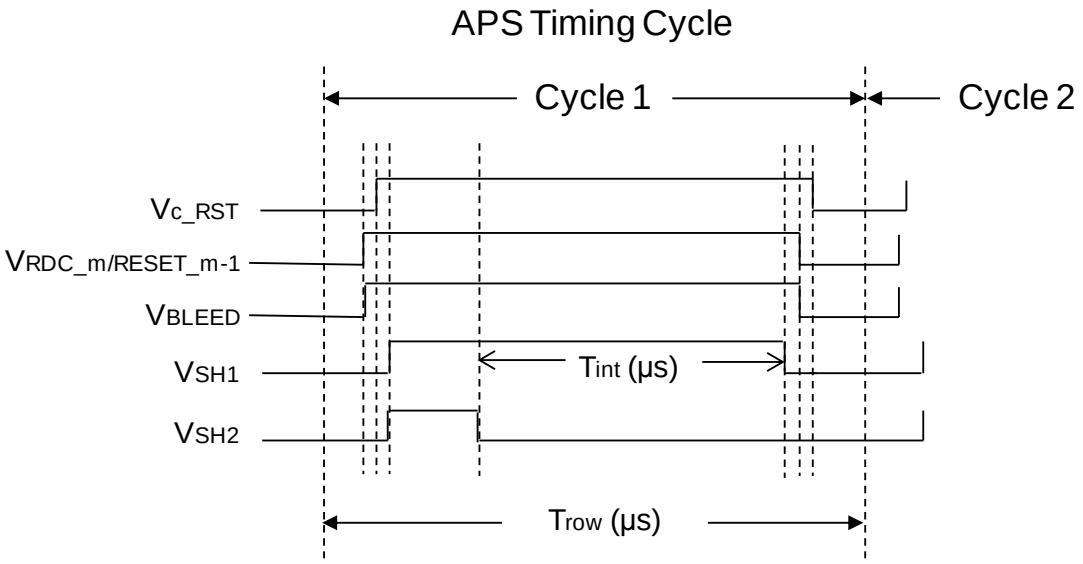


Figure 6.3. APS Readout Timing Diagram

6.2 Array Pixel Characterization

Thin-film transistor (TFT) device characteristics were extracted from test devices in proximity to the array prior to a-Se deposition using a probe station and an Agilent 4156C semiconductor parameter analyzer. Figure 6.4 and Figure 6.5 show device characteristic curves for a typical TFT with a W/L ratio of 40µm/10µm in close proximity to the lower part of the array (actual measured values shown in Table II). The I_D-V_D curves of Figure 6.4 indicate the presence of a non-negligible resistance between the source-drain contacts and the a-Si channel. The I_D/I_G-V_G curves of Figure 6.5 show low gate leakage current and low off currents on the order of 30fF, and an ON/OFF ratio of almost 10^8. TFT parameters extracted from Figure 6.4 and Figure 6.5 are summarized in Table 6.1. Note that the value for $\mu_{sat,eff}$ is extracted using voltages at which array noise measurements are taken and cross-referenced with the output bias current of the pixels used for noise calculations.

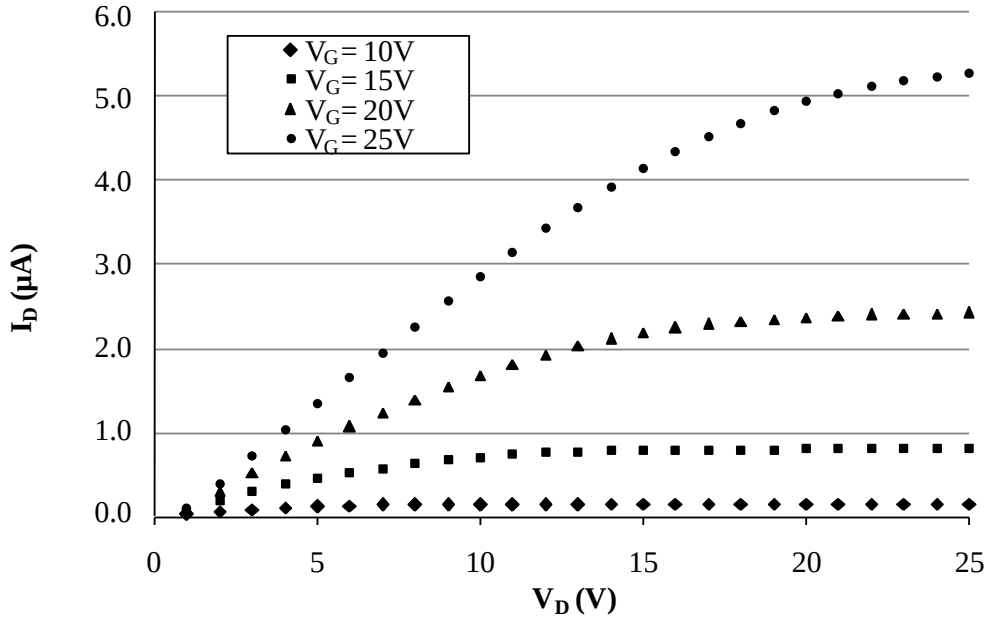


Figure 6.4. Typical I_D-V_D curve for TFTs on prototype array. Actual measurement is taken for a stand-alone TFT with a W/L ratio of 40μm/10μm in close proximity to the lower part of the array.

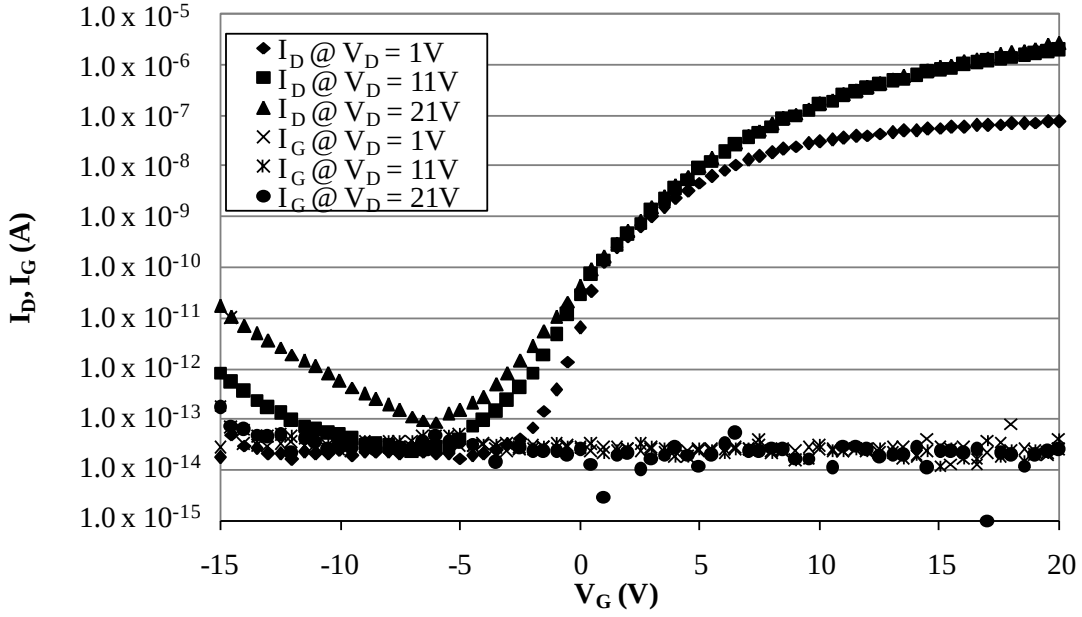


Figure 6.5. Typical I_D/I_G -V_G curve for TFTs on prototype array. Actual measurement is taken for a stand-alone TFT with a W/L ratio of 40μm/10μm in close proximity to the lower part of the array.

Table 6.1. Typical measured TFT device parameters from test pixels

Measured TFT Parameters	Value
W (μm), Gate Width	42
L (μm), Gate Length	15
ΔL (μm), Gate-Source/Drain overlap	5
$\mu_{eff,sat}$ (cm^2/Vs), Effective channel mobility in saturation regime	0.137
$\mu_{eff,lin}$ (cm^2/Vs), Effective channel mobility in linear regime	0.111
$V_{T,sat}$ (V), TFT threshold voltage in saturation regime	3.6
$V_{T.lin}$ (V), TFT threshold voltage in linear regime	4.5
C_{ox} (F/cm^2), Gate insulator capacitance	1.7×10^{-8}

6.3 Imaging Array Testing

Imager quality characterization tests that are typically performed include the modulation transfer function (MTF), noise power spectrum (NPS), and detective quantum efficiency (DQE). All of these measurements assume that the systems tested are linear and spatially invariant (stationary). Where this is not the case, linearization of data can be performed and other necessary approximations employed.

The MTF is used to characterize the spatial resolution of an imager, and is a well-known metric to avid photographers. It is a measure both of the contrast sensitivity and sharpness of an imager. There are several methods of determining the MTF of a digital X-ray imager, and the two most common methods are obtained through the use of a slit or edge device [50]. In the edge method, an opaque object with a straight polished edge is placed in very close proximity to the detector under test. Care is taken to ensure that the polished edge is aligned with the focal spot of a collimated X-ray beam, both of which are perpendicular to the surface of the receptor. The resulting image is read into a computer and forms the edge

spread function (ESF) of the imager. The ESF is then differentiated to generate the line spread function (LSF), which is in turn run through a fast Fourier transform (FFT) algorithm to end up with the MTF as described by (6.1) below [75].

$$MTF(u) = FFT\{lsf(x)\} = FFT\left\{\frac{d}{dx}[esf(x)]\right\} \tag{6.1}$$

In the slit method, an opaque object with a narrow slit, typically less than 100μm in width, is placed in very close proximity to the detector under test. Instead of an ESF, the slit method directly produces an LSF, which is then used to calculate the MTF of the imager [76].

The NPS is used to characterize the spectral content and magnitude of noise of an imaging system, including X-ray shot (quantum) noise and imager (system) noise. The NPS provides an estimate of the spatial frequency dependence of the pixel-to-pixel fluctuations in an imager. As such, the NPS is a more complete description of the image noise than single pixel noise characterization tests, because it provides information on the distribution in frequency (spatial) space of the noise power. For instance, excess high frequency noise in a digital mammogram NPS would indicate the imager's poor ability to resolve fine features such as micro-calcifications, which would be visible only at high spatial frequencies (i.e. at high resolutions) [77].

The one dimensional (1D) NPS can be either measured using a one dimensional method such as the scanned slit method, or from a two dimensional (2D) NPS image. In the scanned slit method a long, narrow slit is scanned, in steps, in one dimension across an imager. Each scan is averaged, and the series of averaged scans is then squared. The modulus of the Fourier transform of the squared series of averaged scans gives the 1D NPS. Alternately, one can extract a slice from along one of the primary axis from a 2D NPS image.

As we saw in (1.5), repeated as (6.2) below for ease, the DQE can be calculated once the MTF and NPS are known.

$$DQE(f) = \frac{k^2\{MTF(f)\}^2}{NPS(f)\Phi} \tag{6.2}$$

The DQE is described fully by three independent variables, namely two spatial coordinates, and X-ray exposure. Thus the DQE represents a four-dimensional picture, which is not easy to visualize. For this reason, DQE is presented one dimension at a time, and thus partly explains why the MTF and NPS are often only calculated in 1D instead of 2D.

6.3.1 Array Uniformity

Initial array tests are conducted without X-rays and reveal large gain non-uniformity due to process variations as shown in the raw pixel data of Figure 6.6. Only an area of 59 columns by 39 rows is shown as many rows and columns are lost during the ACF bonding process of the gatedriver and charge amplifier chips, and due to process defects.

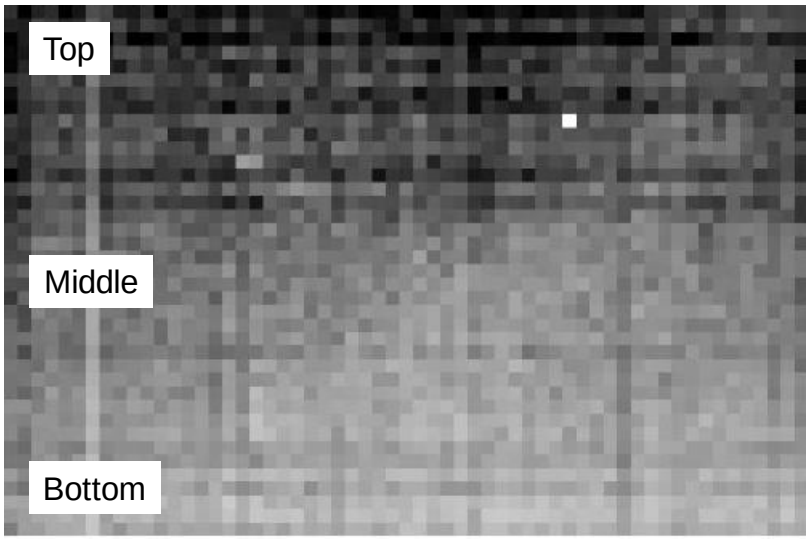


Figure 6.6. Raw APS array image showing gain non-uniformity due to TFT process variations.

To explore the array non-uniformity, we averaged the outputs of the top, middle, and bottom portions of the array. Figure 6.7 shows the charge amplifier output voltage as a function of charge amplifier integration time, T_{int}. From the slope of the graph, the pixel output bias current can be determined since we have $V_{out} = I_D T_{int}/C_F$. From the bias current, the pixel transconductance, G_m, and pixel charge gain, G_i, can be extracted. The top portion of the

array has an output current of 4.3x the bottom portion of the array showing a large gain non-uniformity of this specific die. Commercial a-Si flat-panel imagers have gain non-uniformities on the order of a few percent.

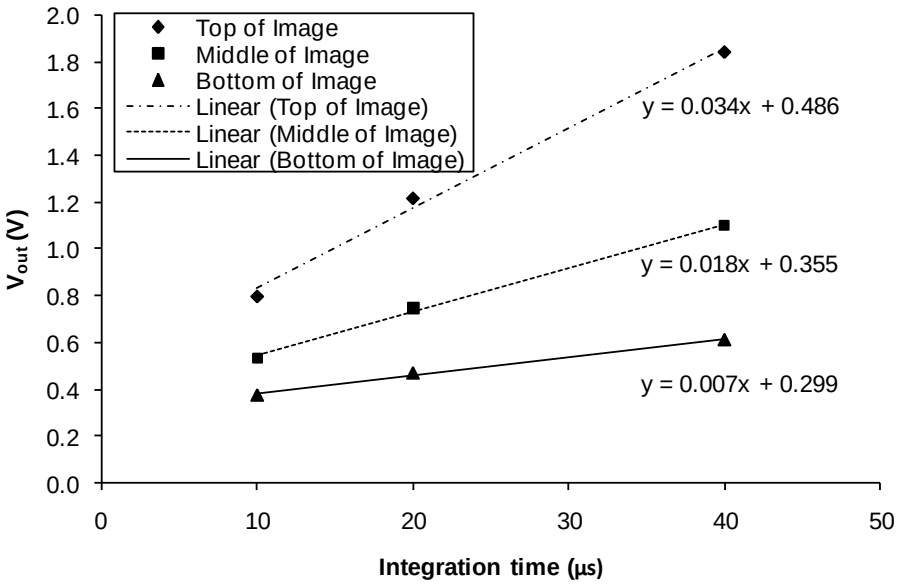


Figure 6.7. Gain variability in different regions of APS array are indicated by slope of straight line fit which corresponds to output bias current.

Array tests with X-rays are conducted with the beam source at 70kVp and filtered with Al to meet the standard X-ray beam quality RQA5 in IEC 1267. The source to target distance is set at 2.3m and tested to ensure a linear response over the full range of exposures. With a 1mm thick layer of a-Se, a -10kV bias is applied to the top a-Se electrode to produce an electric field of 10V/μm to ensure good X-ray to charge conversion. Figure 6.8 shows the prototype a-Si 64x64 pixel array along with a portion of the test setup.

Due to non-uniformities throughout the imaging array, each pixel will have a different gain, which will lead to fixed pattern noise (deterministic noise) if not corrected. In order to correct for gain variations, each pixel gain will need to be normalized. We can perform this gain correction by exposing the entire array to the same amount of signal at a fixed X-ray exposure, known as a light field exposure. With a light field exposure, if there were no gain

variations throughout the array, the output of each pixel would be identical; where as in practical cases the pixel output will be different. The response of the pixels in the array to a fixed exposure light field image is stored in a gain table. At all subsequent exposures, the pixels are normalized by dividing their output by their values in the gain table. If the X-ray source and pixel response are linear at all the X-ray exposures tested, then only a single gain table at a fixed exposure is required. Based on our experiments, there was no noticeable difference between using a single gain table at a fixed exposure, versus multiple gain tables at varying exposure. The gain table was calculated by subtracting an average of 120 dark field images (images without X-rays) from an average of 120 light field images (images with X-rays), thus performing software double sampling. The gain table in mathematical form is

$$G = \overline{S_{X120}} - \overline{O_{X120}} \tag{6.3}$$

where G is the gain table, $\overline{S_{X120}}$ is the averaged signal (light field image) from 120 samples at exposure X, and $\overline{O_{X120}}$ is the averaged offset (dark field image) from 120 samples.

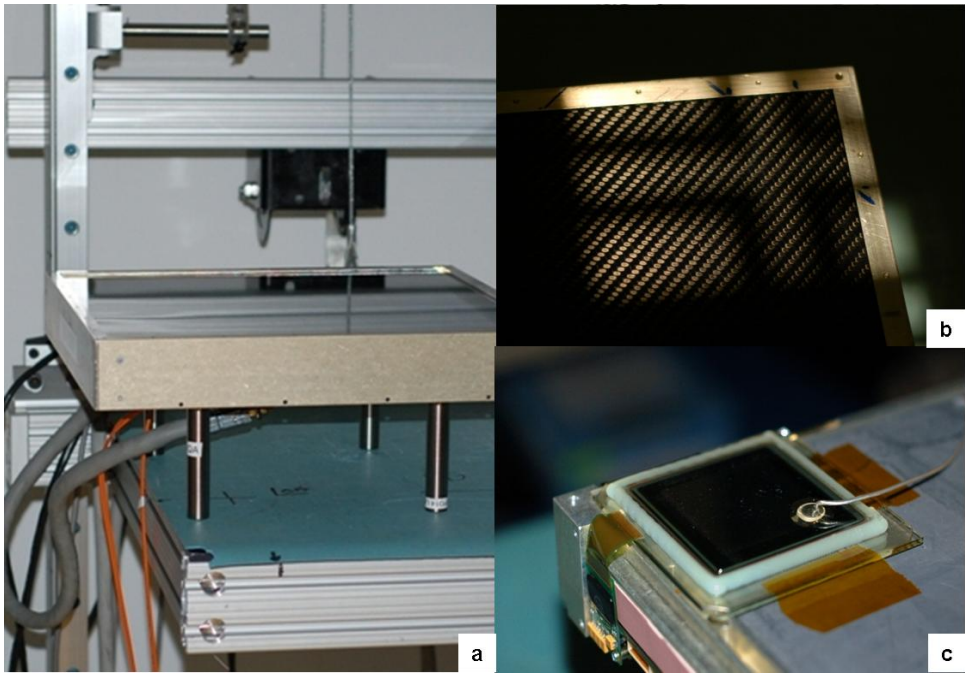


Figure 6.8. (a) FPD14 test fixture on X-ray table. (b) X-ray beam is collimated and positioned over prototype imaging array. (c) Prototype a-Si 64x64 APS array sitting in FPD14 test fixture (with cover off for viewing purposes).

6.3.2 Modulation Transfer Function and Image Lag

APS experimental results from the prototype imager are compared with a state-of-the-art commercially available 14" flat-panel X-ray detector (FPD14 [78]) PPS imaging array under the same X-ray beam conditions. X-ray line resolution results are shown in the center of the images of Figure 6.9 (a) and Figure 6.9 (b) for the FPD14 PPS (300 μm pixels) and the prototype APS imager (250 μm pixels) at 1.6 lp/mm and 2.0 lp/mm, respectively. The line resolution target is shown in Figure 6.9 (c). Pixel-level gain correction has been applied to the line resolution images of both imagers to correct for pixel gain non-uniformities. The effective fill factor of our prototype is close to 100% as evidenced by the ability of the pixels to image 2.0 lp/mm which corresponds to twice the width of a 250 μm pixel pitch.

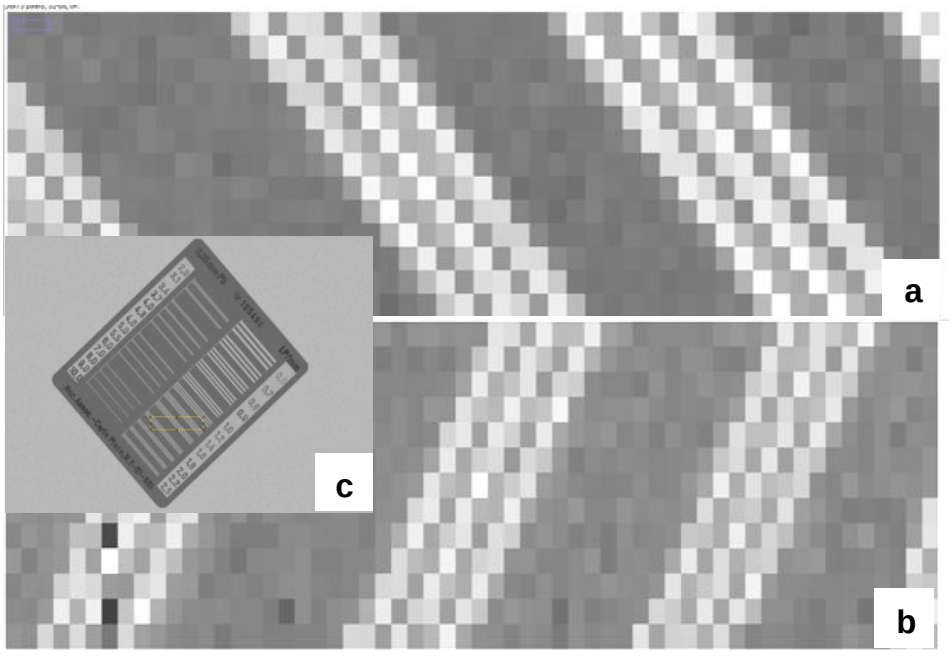


Figure 6.9. Resolution image test from (a) FPD14 PPS array at 1.6 lp/mm shown in center of image (b) prototype 64x64 APS array at 2.0 lp/mm shown in center of image (c) Resolution target.

To better assess the effective fill factor and gain insight on the resolution and imaging capabilities of the imager we conducted modulation transfer function (MTF) experiments.

MTF tests are conducted on the prototype APS array and the FPD14 array using the slit method [76] with a slit of width 40 μm. Figure 6.10 shows the MTF for both arrays normalized with respect to pixel pitch and compared with an ideal MTF result (which is the magnitude of a sinc pulse). The null for the APS array occurs at a value corresponding to approximately 4.23 lp/mm indicating an effective fill factor of approximately 94.5%, which is reasonable for a geometric fill factor of 57%. In the case of an a-Se sensor, it has been shown that a pixel with an electrode of 66% geometric fill factor has nearly 100 percent effective fill factor due to the high electric field strength [39]. The MTF of the array exhibits a large concave shape, which indicates poor spatial frequency resolution, and is most likely caused by charge trapping at the silicon nitride/a-Se interface. This charge trapping will effectively lead to a blurring of the image at medium spatial frequencies as charge builds up and migrates to neighbouring pixels.

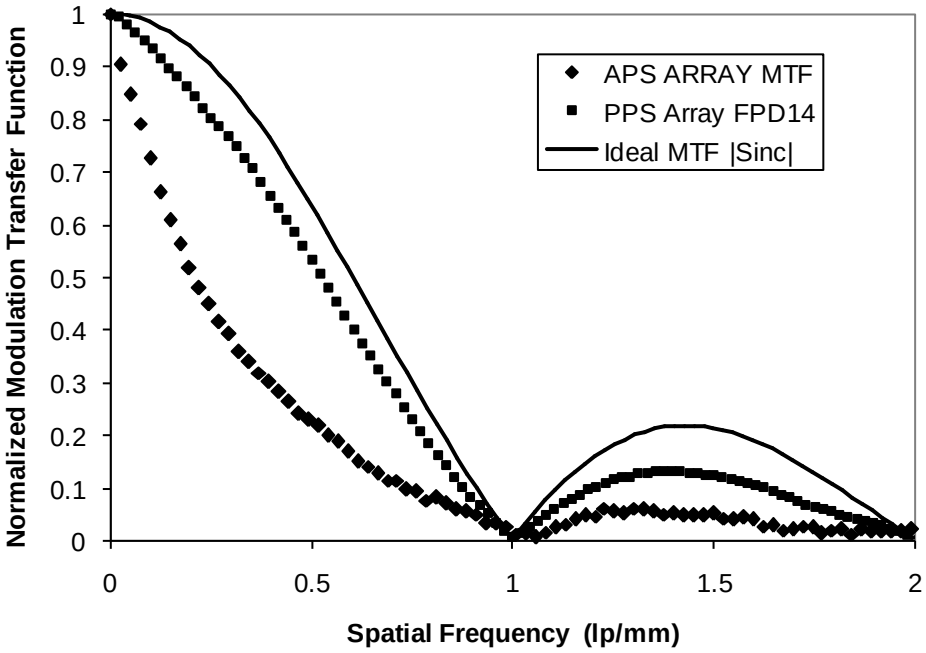


Figure 6.10. Normalized modulation transfer function of APS and FPD14 imagers.

The transient response of the imaging array shows a very pronounced image lag due to charge build-up in the presence of X-rays further pointing to charge trapping at the silicon nitride/a-Se interface. Figure 6.11 illustrates the transient charge build-up in the presence of

X-rays. In order to reduce image lag caused by charge trapping at the silicon nitride/a-Se interface, an improved silicon nitride passivation layer needs to be developed along with better surface preparation prior to a-Se deposition. In addition, increasing the area of the bottom a-Se electrode will decrease the amount of passivation material exposed to a-Se, thus reducing charge trapping, however, at the expense of increased parasitic capacitance between the a-Se photoconductor and underlying transistors and data/control lines.

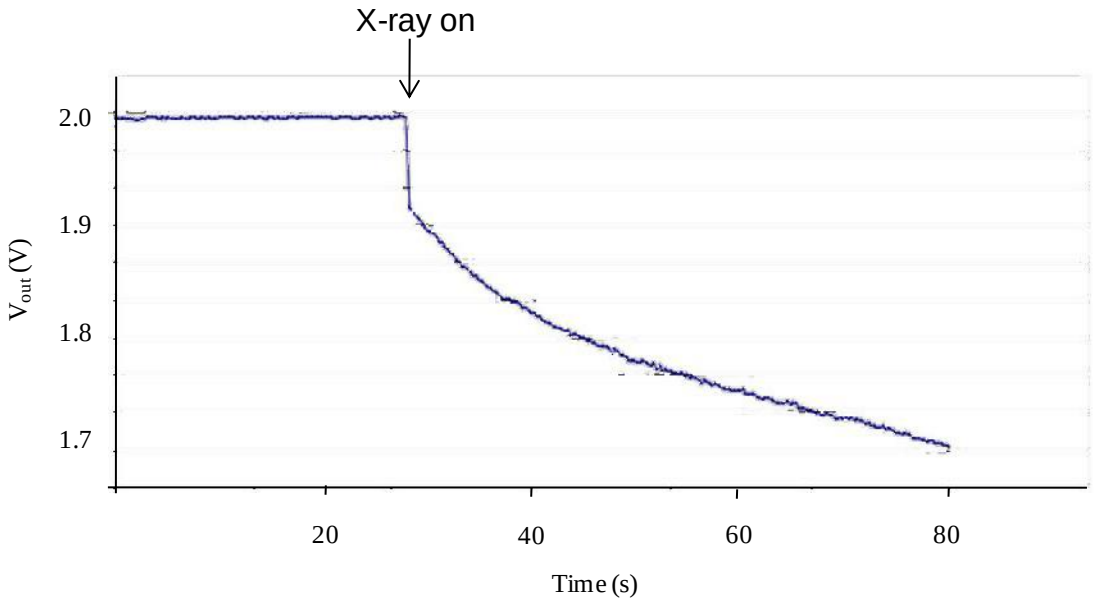


Figure 6.11. APS X-ray image lag transient shown as a function of charge amplifier output voltage.

6.3.3 Array Signal-to-Noise Ratio

In order to test the array at low X-ray exposures, the CMOS readout chain (charge amplifier, differential amplifier, and A/D converter) was required to operate at a high sensitivity setting where it introduced less noise to the system. Due to the large non-uniformity of the test array, operating at high sensitivity meant that there were few pixels that were functioning within a readable output range under a given set of biasing conditions (usually due to column charge amplifier saturation). As a result, we were unable to obtain a large enough working pixel area to carry out meaningful NPS(f) experiments, and thus were also unable to calculate the

DQE(f) for the imager. Instead, output signal-to-noise ratio (SNR) experiments were conducted over test areas of eight to twenty pixels to test the low X-ray dose performance of the imagers. For each pixel within the test area, an average of eighty offset images, $\overline{O_{Y80}}$, was subtracted from the i_{th} pixel signal sample, $S_{i,Y}$, taken at exposure *Y*. The result was then normalized by the corresponding pixel value in the gain table, *G*. This procedure was averaged over eight samples for each pixel and is shown in the equation below. Averaging over eight samples helps to reduce the noise introduced by the image lag in our signal.

$$\overline{S_Y} = \frac{\sum_{i=1}^{8} \frac{S_{i,Y} - \overline{O_{Y80}}}{G}}{8} \tag{6.4}$$

To calculate the SNR over an area of several pixels, the average of each pixel $\overline{S_Y}$, was averaged over all *N* pixels in the test area to form the 'signal' component. The standard deviation, *SD*, of all *N* pixel averages in the test area formed the 'noise' component. The SNR is thus given by

$$SNR = \frac{\sum_{j=1}^{N} \frac{\overline{S_{Y,j}}}{N}}{SD\left\{\overline{S_{Y,j}}\right\}} \tag{6.5}$$

For example, in the case of a test region of 2×2 pixels, shown in Figure 6.12, the SNR would be

$$SNR = \frac{\sum_{j=1}^{4} \frac{\overline{S_{Y,j}}}{4}}{SD\left\{\overline{S_{Y,1}}, \overline{S_{Y,2}}, \overline{S_{Y,3}}, \overline{S_{Y,4}}\right\}}$$

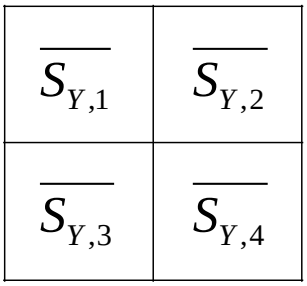


Figure 6.12. Gain normalized average values for a test region of 2×2 pixels

The FPD14 imager is used as a baseline for the prototype APS imager. The total input referred noise for the FPD14 is determined to be 2016 electrons by measuring the standard deviation of the output signal as described above. In the case of the APS imager, the bleed transistors which are meant to limit the input bias current to the column charge amplifiers were not functional. As a result, our APS experiments are conducted under lower than optimal gain settings with a quantization noise error of 5844 electrons, which makes measuring the true output noise and hence input referred noise not possible. Based on bias current values measured from the APS pixel outputs, and process parameters extracted from test devices (see Table 6.2), we simulated an input referred noise of 1671 electrons based on our conservative APS noise model.

Table 6.2. Measured and simulated pixel parameters

Measured and Simulated Pixel Parameters	Value
V_{DD} (V), DC power rail	22
$V_{RDC,eff}$ (V), effective RDC gate voltage	25
I_D (nA), measured pixel output bias current	33.7
α_H, Hooge flicker noise coefficient	1×10^{-1}
G_m (nA/V), Pixel transconductance	18.2
G_i (C/C), Pixel charge gain	2.0
q_{in} (e), Pixel simulated input referred noise	1671

Output SNR^2 is plotted as a function of exposure for both the FPD14 and APS array in Figure 6.13. Due to the difference in pixel size, Figure 6.13 also contains a plot of APS results adjusted for higher expected dose for a 300 μm pixel pitch.

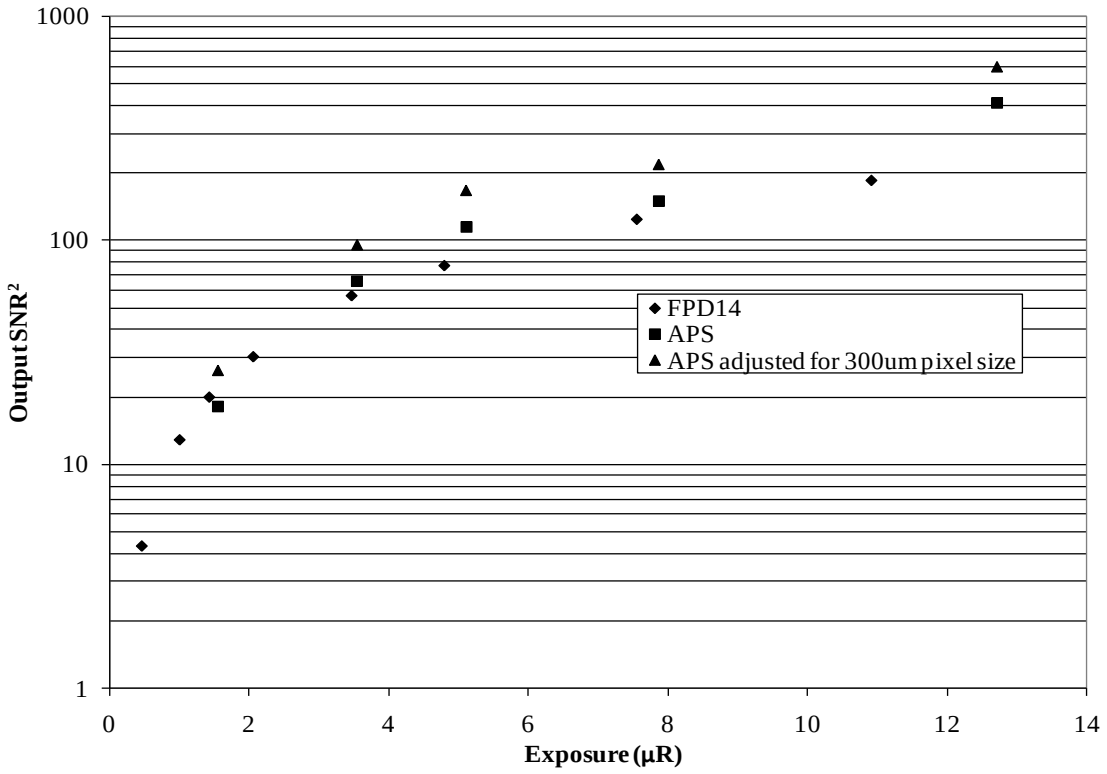


Figure 6.13. Output SNR^2 as a function of exposure for APS imager and FPD14 PPS imager.

Output SNR^2 results are quite promising for the prototype APS array, though further testing at exposures below 1.5 μR are required for future arrays where signal saturation, due to inoperative bleed transistors, are not an issue. Additional improvements in output SNR can be had by: employing hardware double sampling, which would reduce flicker noise, though at the cost of an additional control/gate driver line per pixel; an improved TFT process with higher carrier mobility and thus increased pixel gain; an improved gate nitride and a-Si with fewer traps to reduce the flicker noise coefficient by an order of magnitude [57]; a better passivation nitride at the a-Se interface leading to fewer traps that could potentially act as a source of flicker and shot noise.

7 Conclusions and Contributions

Digital flat-panel imagers offer numerous advantages over conventional X-ray imaging systems, the most important being a superior detective quantum efficiency (DQE), which allows for reduced X-ray dosages for the patient. One focus of this research in digital flat-panel imagers is to further increase the DQE, particularly at low X-ray exposures. Another focus of this research is in the creation of a multi-mode imager, such as a combined radiographic and fluoroscopic (R&F) imager, which will reduce hospital costs, both in terms of equipment acquisition and storage space.

To that end, we have proposed a novel multi-mode digital flat-panel imager with a dynamic range capable for use in R&F applications, with a particular focus on noise optimization for low-noise real-time digital flat-panel X-ray fluoroscopy. This work involved the derivation and optimization of the total input referred noise of an active pixel sensor in terms of the on-pixel thin-film transistor device dimensions. It was determined that in order to minimize noise, all non-transistor capacitances at the pixel sense node needed to be minimized. This lead to a design where the on-pixel storage capacitance was eliminated; and instead the gate capacitance of the sense-node transistor was used to store the incoming X-ray converted charge. This work has allowed researchers to gain insight into the fundamental noise operation of active pixels used in medical imaging, and to appropriately choose device dimensions. Due to the inherent large feature sizes of thin-film transistors, active pixel flat-panel X-ray medical imagers offer lower resolution than their film-screen counterparts. By demonstrating the desirability of smaller device dimensions for reduced noise and the elimination of a storage capacitor, this research has freed some of the area constraints that exist in active pixel flat-panel imagers, allowing for smaller pixels, and thus higher resolution medical imagers.

In addition, a 64x64 4T APS imaging array has been fabricated in a-Si technology and mated with an a-Se photoconductor for use in medical X-ray imaging. MTF results and transient response in the presence of X-rays (image lag) for the APS array are poor which is ascribed to high charge trapping at the silicon nitride/a-Se interface. Improvements to the silicon

nitride passivation layer and pixel layout are suggested to reduce this charge trapping. The prototype imager is compared directly with a state-of-the-art a-Si PPS imaging array and demonstrates good SNR performance for X-ray exposures down to 1.5μR. Pixel design and fabrication process improvements are suggested for low-exposure APS testing and improved low-noise performance.

The original contributions of the research presented in this thesis to the field of large area digital imaging are listed below:

Circuit Design and Noise Analysis

- First three transistor low-noise, high dynamic range multi-mode pixel architecture capable of use in fluoroscopy and radiography was designed.
- Original circuit noise analysis and optimization as a function of pixel TFT device dimensions applicable to any a-Si based charge-sensitive pixel, and easily extended to other device technologies such as poly-Si.
- Noise optimization allowed for elimination of separate storage capacitance, smaller transistors, and thus smaller pixels for higher resolution imaging with a-Si flat panels.

Array Design and Process

- First demonstrated APS array (or single pixel) to work with measured X-ray signals as low as 1.5 μR in either a-Si or poly-Si technology.
- APS array demonstrates good SNR performance for X-ray exposures down to 1.5 μR compared to a state-of-the-art a-Si PPS imaging array.
- Fabrication process improvements are suggested for low-exposure APS testing and increased low-noise performance.

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Appendix A Fabrication at University of Waterloo

This appendix discusses process parameters and TFT fabrication steps at the University of Waterloo insofar as it differs from similar research performed at Simon Fraser University. All the films used in the TFT fabrication process were modified and recharacterized at the University of Waterloo (UW). Table A.1. shows the process parameters for the PECVD films grown at UW.

For the PECVD at the University of Waterloo, the RF electrode area is 17cm x 17cm and the substrate-electrode spacing is ~1" (2.54cm). For the RIE, the electrode diameter is 19.9cm and the electrode height is ~6" (15.45 cm).

Table A.1 Process parameters for PECVD deposited films at UW

	n+ µc-Si (seed)	n+ µc-Si (bulk)	a-Si:H	SiN_x:H	SiN_x:H (low temp)
Substrate Temp	250 ºC	250 ºC	250 ºC	250 ºC	200 ºC
Pressure	1.9 Torr	1.9 Torr	0.4 Torr	1.5 Torr	1.0 Torr
Power	10 W	30 W	2 W	40 W	15 W
Flow rates (sccm)	PH_3: 0.5 SiH_4: 1.0 H_2: 250	PH_3: 1.0 SiH_4: 2.5 H_2: 250	SiH_4: 20	NH_3: 16 SiH_4: 4 H_2: 100	NH_3: 40 SiH_4: 2 H_2: 80
Deposition rate	0.44 Å/s	1.48 Å/s	1.60 Å/s	3.70 Å/s	2.00 Å/s

The fabrication steps undertaken at UW are very similar to those at SFU with mostly minor adjustments due to availability of developers, etchants, and fabrication equipment. Two significant process changes include:

- chromium replaces aluminum as the metal #1 layer due to the poor surface roughness of the aluminum at UW,

- chromium is primarily used as a mask for the polyimide etching instead of photoresist due to the ease of availability of chromium which simplifies the process.

The fabrication steps are shown in Table A.2.

Table A.2 Fabrication steps for TFT array fabrication at UW

Step Number	Procedure	Description
1	Clean 4" round 0.7mm thick Corning 1737 glass wafers	RCA1 clean, dry with N_2 gun
	MASK 1: Define source-drain contacts; output and VDD lines	
2	Sputter chrome	DC sputter chrome, pump chamber below 3 µTorr, deposition pressure 3.1mT, power 300W
3	PECVD n+ µc-Si	See Table 3.1
4	Spincoat photoresist (PR)	AZ 3312 PR, 4000rpm spin, 30s
5	Softbake PR	60s @ 100 °C on hotplate
6	Pattern PR	UV exposure, 3 sec; AZ MIF-300 developer, 30 sec
7	Dry etch n+ µc-Si	RIE: 50mT, -80V, 50sccm SF_6, 5sccm O_2, 11s
8	Wet etch chromium (Cr)	Cr etchant, 1m30s @ 45 °C
9	Remove PR	Soak in acetone 3 min, rinse with fresh acetone, rinse IPA, dry with N_2 gun, dry 1min @ 100 °C on hotplate , ASH: 100mT, 30W, 30 sccm O_2, 30 sec, -300V
10	Remove surface oxide	HF dip in 50:1 ($HF:H_2O$) for 5s, DI water rinse, dry with N_2 gun, dry 1min @ 100 °C on hotplate
	MASK 2: Define TFT islands	
11	PECVD a-Si:H	See Table 3.1
12	PECVD SiN_x:H	See Table 3.1
13	Spincoat photoresist (PR)	AZ 3312 PR, 4000rpm spin, 30s
14	Softbake PR	60s @ 100 °C on hotplate
15	Pattern PR	UV exposure, 3.1 sec; AZ MIF-300 developer, 30 sec
16	Dry etch a-Si:H, SiN_x:H, n+ µc-Si	RIE: 50mT, -80V, 50sccm SF_6, 5sccm O_2,

		25s
17	Remove PR	Soak in acetone 3 min, rinse with fresh acetone, rinse IPA, dry with N_2 gun, dry 1min @ 100 °C on hotplate , ASH: 100mT, 30W, 30 sccm O_2, 30 sec, -300V
	MASK 3: Interconnect opening between metal #1 and metal #2	
18	PECVD SiN_x:H	See Table 3.1
19	Spincoat photoresist (PR)	AZ 3312 PR, 4000rpm spin, 30s
20	Softbake PR	60s @ 100 °C on hotplate
21	Pattern PR	UV exposure, 3.1 sec; AZ MIF-300 developer, 30 sec
22	Dry etch SiN_x:H	RIE: 50mT, -80V, 50sccm SF_6, 5sccm O_2, 60s
23	Remove PR	Soak in acetone 3 min, rinse with fresh acetone, rinse IPA, dry with N_2 gun, dry 1min @ 100 °C on hotplate , ASH: 100mT, 30W, 30 sccm O_2, 90 sec, -300V
	MASK 4: Define gate metal, interconnect metal, and READ and RESET lines	
24	Sputter aluminum	DC sputter aluminum, pump chamber below 2.5 μTorr, deposition pressure 9mT
25	Spincoat photoresist (PR)	AZ 3312 PR, 4000rpm spin, 30s
26	Softbake PR	60s @ 100 °C on hotplate
27	Pattern PR	UV exposure, 3.1 sec; AZ MIF-300 developer, 30 sec
28	Wet etch aluminum	Al etchant, ~1 min @ 45 °C
29	Remove PR	Soak in acetone 3 min, rinse with fresh acetone, rinse IPA, dry with N_2 gun, dry 1min @ 100 °C on hotplate , ASH: 100mT, 30W, 30 sccm O_2, 60 sec, -300V
	MASK 5: Interconnect opening between metal #2 and metal #3	
30	Spincoat polyimide (PI)	Spin at 500 rpm for 5s, ramp to 7000 rpm in 20 sec, leave at 7000 rpm for 30 sec
31	Cure PI	Place on hotplate at 80°C and ramp to 150°C at 450 °C/h, ramp to 250°C at 240 °C/h, set timer at 2 hours, allow to cool to room temp
32	PECVD SiN_x:H (low temp)	See Table 3.1

33	Sputter chrome	DC sputter chrome, pump chamber below 3 μTorr, deposition pressure 3.1mT, power 300W
34	Spincoat photoresist (PR)	AZ 3312 PR, 4000rpm spin, 30s
35	Softbake PR	60s @ 100 °C on hotplate
36	Pattern PR	UV exposure, 3.1 sec; AZ MIF-300 developer, 30 sec
37	Hardbake PR	60s @ 120 °C on hotplate
38	Wet etch chromium (Cr)	Cr etchant, 1min @ 45 °C
39	Dry etch SiN_x:H	RIE: 300mT, 130W, 50sccm CF_4, 5sccm O_2, 120s
40	Dry etch PI	RIE: 300mT, 130W, 5sccm CF_4, 50sccm O_2, 800s
41	Remove Cr	Cr etchant till Cr removed
	MASK 6: Define a-Se bottom electrode, guardring, and bondpads	
42	Sputter aluminum	DC sputter aluminum, pump chamber below 0.5 μTorr, deposition pressure 6mT
43	Spincoat photoresist (PR)	AZ 3312 PR, 4000rpm spin, 30s
44	Softbake PR	60s @ 100 °C on hotplate
45	Pattern PR	UV exposure, 3 sec; AZ MIF-300 developer, 30 sec
46	Wet etch aluminum	Al etchant, ~4m15s @ 45 °C
47	Remove PR	Soak in acetone 3 min, rinse with fresh acetone, rinse IPA, dry with N_2 gun, dry 1min @ 100 °C on hotplate , ASH: 100mT, 30W, 30 sccm O_2, 60 sec, -300V

Appendix B Masks

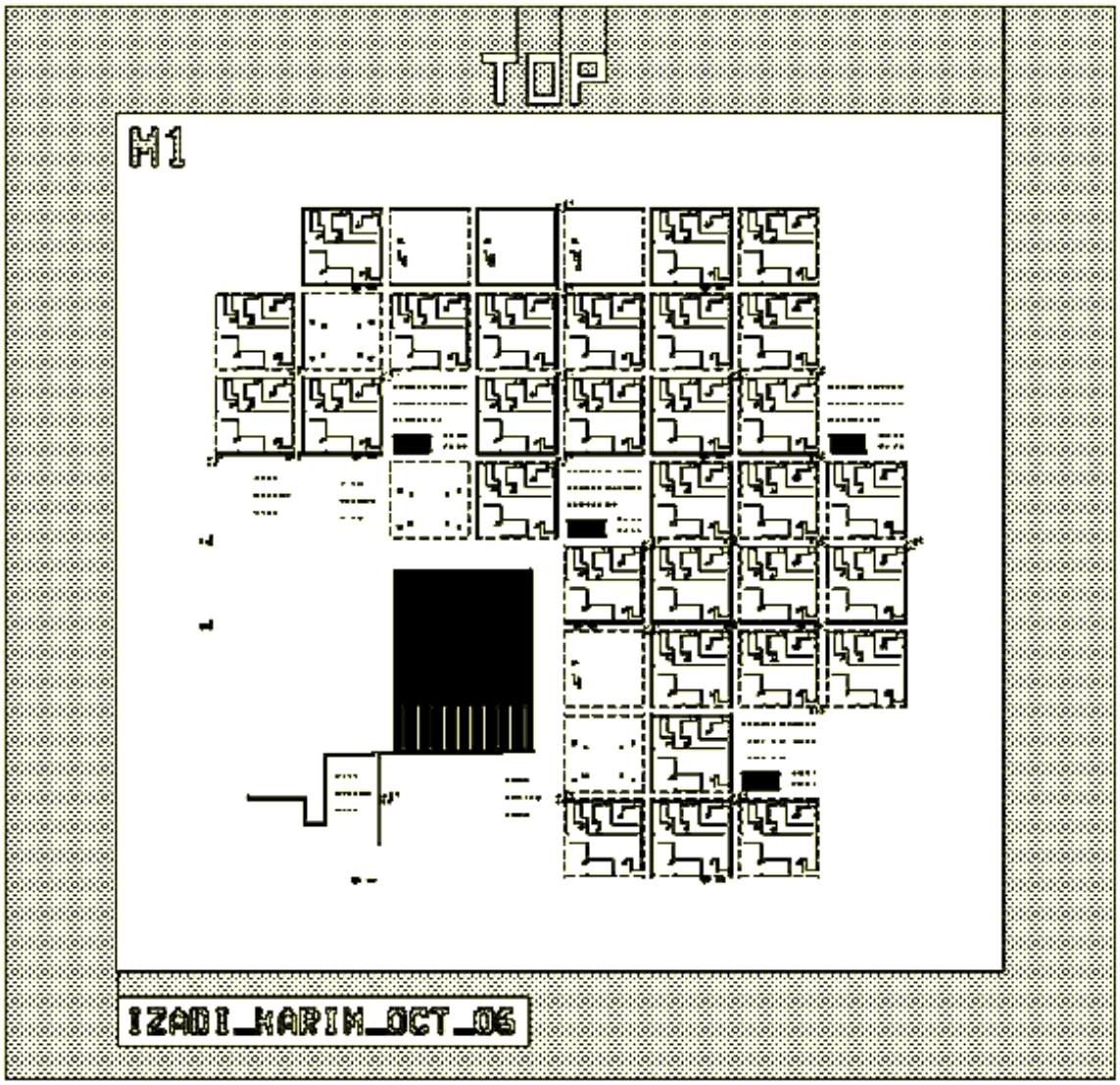

Figure B.1. Mask 1: Define source-drain contacts; output and VDD lines

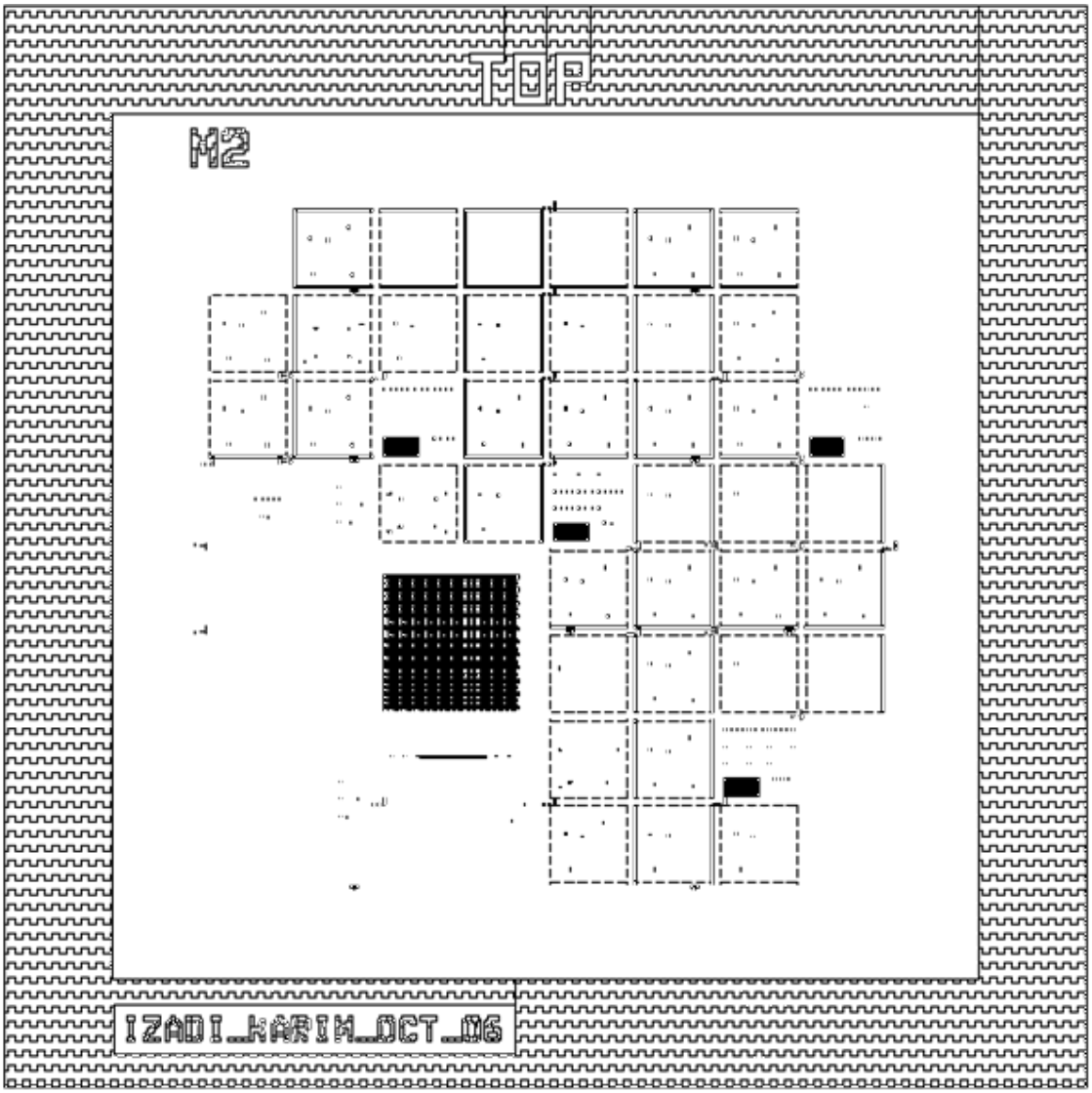

Figure B.2. Mask 2: Define TFT islands

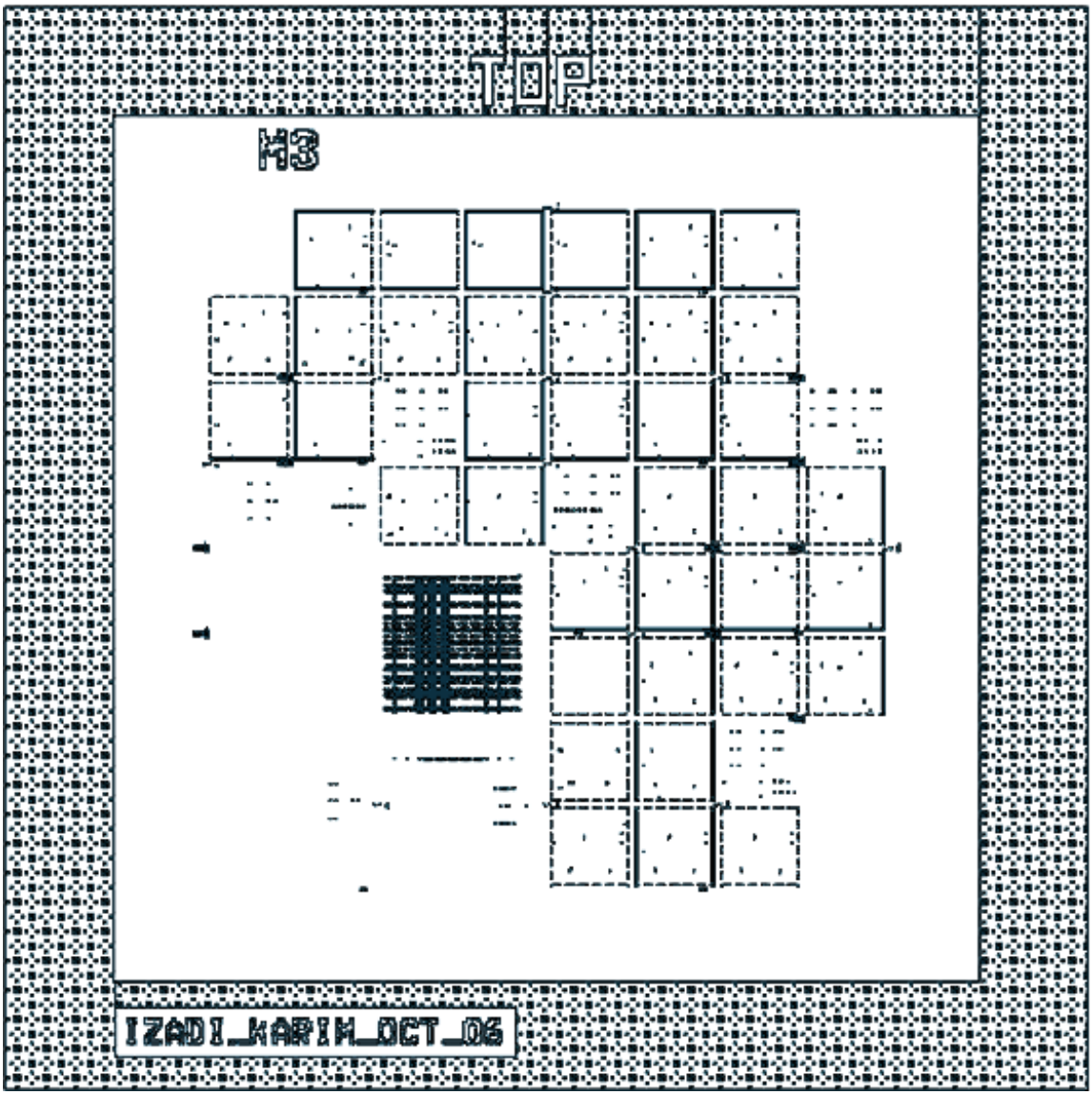

Figure B.3. Mask 3: Interconnect opening between metal #1 and metal #2

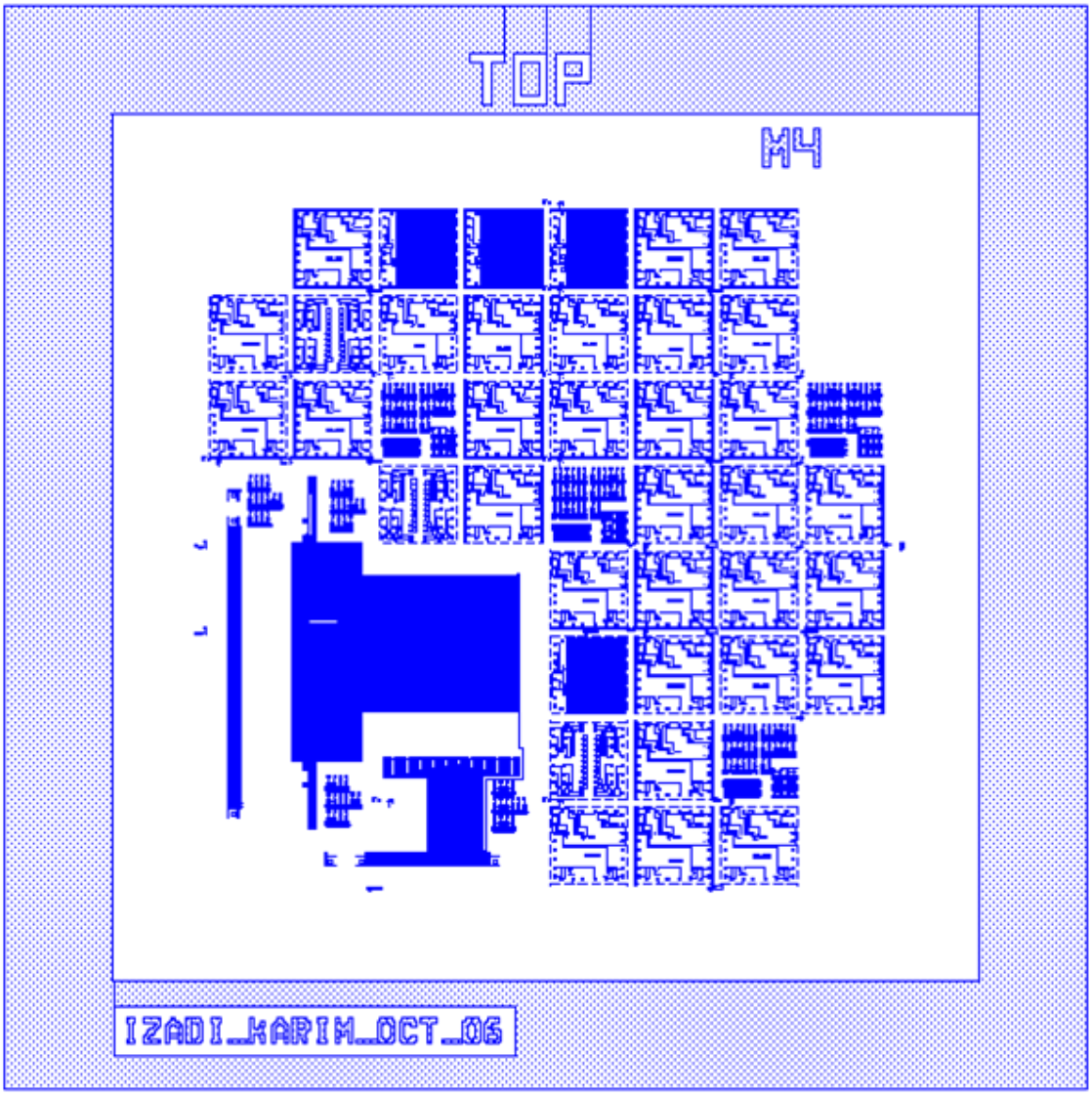

Figure B.4. Mask 4: Define gate metal, interconnect metal, and READ and RESET lines

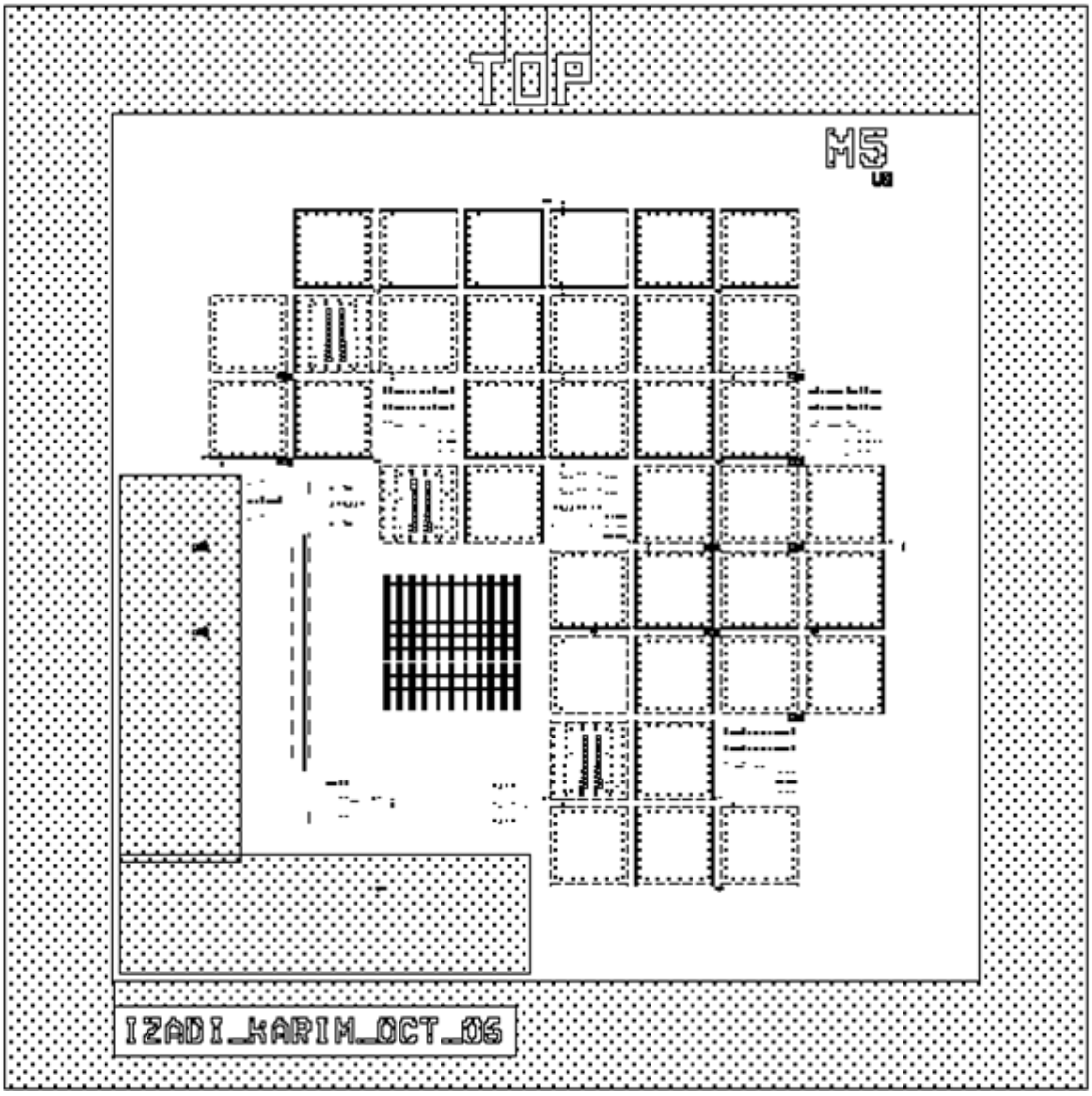

Figure B.5. Mask 5: Interconnect opening between metal #2 and metal #3

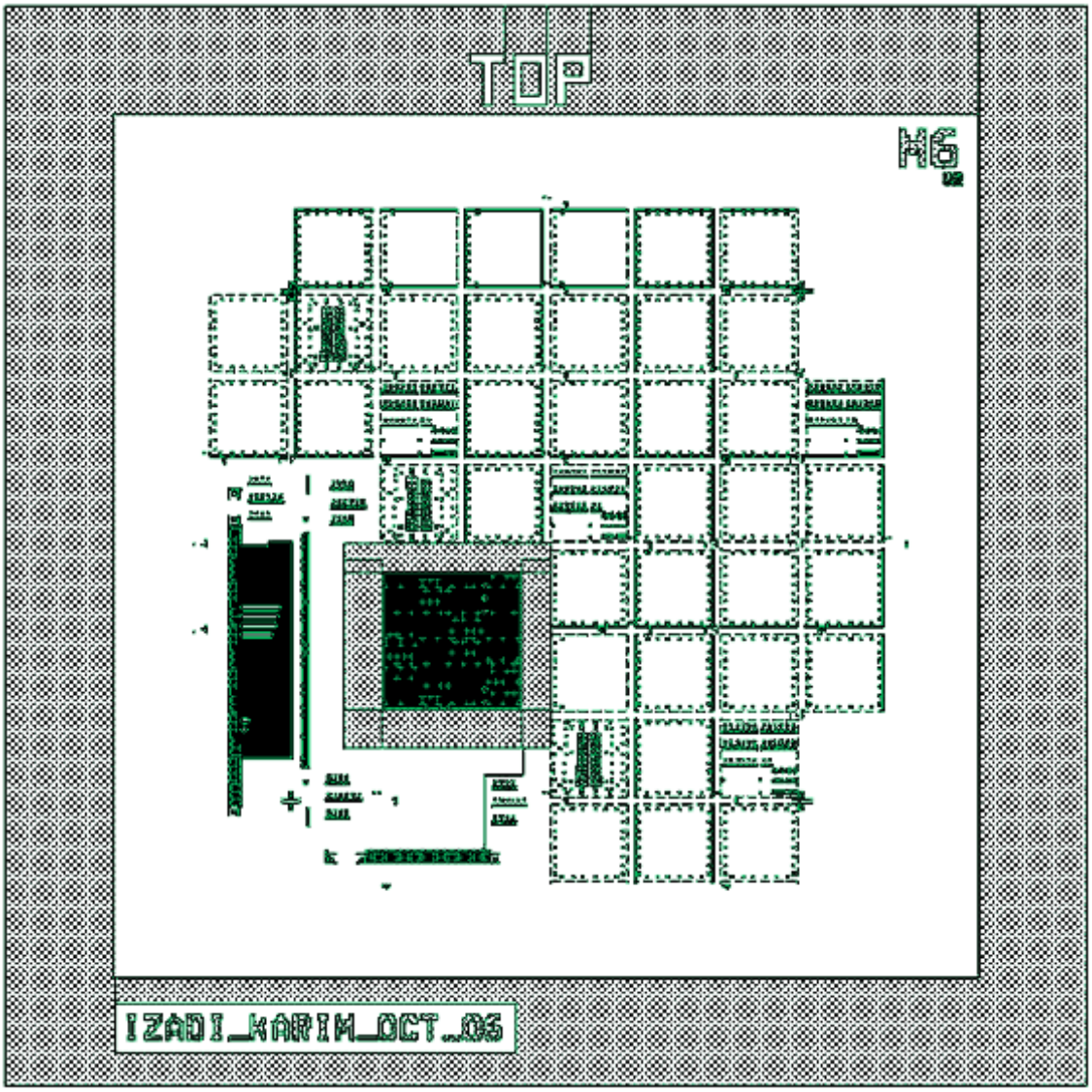

Figure B.6. Mask 6: Define a-Se bottom electrode, guardring, and bondpads

Appendix C Noise Analysis Derivations

All of the derivations in this appendix are the author's original work.

C.1. Noise Double Sampling

Every readout scheme that is described in this thesis involves some form of double sampling. Double sampling is inherent to the C-APS pixel architectures discussed in this thesis in order to separate the signal sample (the sample with X-rays) from the reset sample (the sample without X-rays). Two forms of double sampling are discussed in this thesis which are referred to as single integration double sampling (SIDS) and double integration single sampling (DISS). Figure C.1 shows a block diagram of the double sampling circuit used in the analysis of both sampling schemes. It is assumed that the time constant associated with the sample and hold is considerably smaller than the time constant associated with the integrator, thus we do not include it in any of our noise derivations. The effect on thermal and flicker noise for these two sampling schemes are discussed next.

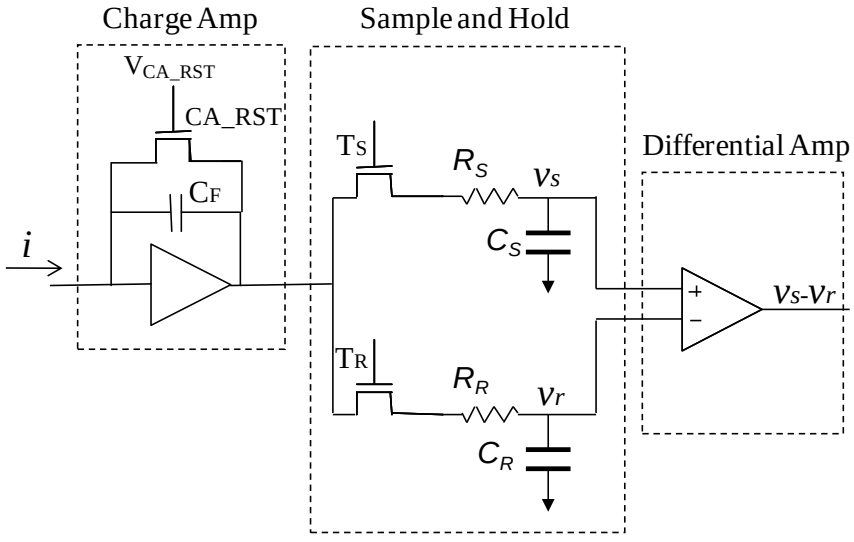

Figure C.1. Double sampling circuit for noise analysis.

C.2. Double Integration Single Sampling

The timing diagram for double integration single sampling is shown in Figure C.2. In this double sampling method, both the signal sample (v_s) and the reset sample (v_r) are taken after a charge integration time of $T=T_1=T_2$. The charge integrator is reset between the signal and reset samples, and the time separation between the signal sample and reset sample is given by τ.

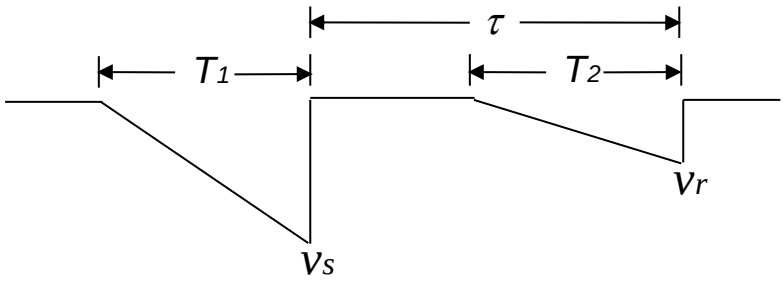

Figure C.2. Timing diagram for double integration single sampling.

Referring to Figure C.1, the output of the opamp for the noise associated with the signal sample, $n_s(t)$, can be defined as,

$$n_s(t) = \frac{-1}{C_F}\int_0^t i(t)dt \qquad \text{(C.1)}$$

Similarly, the noise associated with the reset sample, $n_r(t)$, is given by

$$n_r(t) = \frac{-1}{C_F}\int_0^t i(t)dt \qquad \text{(C.2)}$$

We wish to find the noise variance (noise power) associated with our sampled signal, n_{DISS}, the latter being given by

$$n_{DISS}(t) = n_s(t) - n_r(t) \qquad \text{(C.3)}$$

The variance of $_{DISS}$ is given by

$$\sigma^2_{n_{DISS}} = E\left[n^2_{DISS}(t)\right] - E\left[n_{DISS}(t)\right]^2 = E\left[n^2_{DISS}(t)\right] \tag{C.4}$$

assuming that the expected (mean) value of the noise is zero.

Substituting (C.3) in to (C.4) gives us for the variance of n_{DISS}

$$E\left[n^2_{DISS}(t)\right] = E\left[\left(n_s(t) - n_r(t)\right)^2\right] = E\left[n_s^2(t) - 2n_s(t)n_r(t) + n_r^2(t)\right] = E\left[n_s^2(t)\right] - 2E\left[n_s(t)n_r(t)\right] + E\left[n_r^2(t)\right] \tag{C.5}$$

Squaring both sides of (C.1) gives us

$$n_s^2(t) = \frac{1}{C_F^2}\int_0^t \int_0^t i(x)i(y)dxdy \tag{C.6}$$

Taking the expectation of (C.6) gives us

$$E\left[n_s^2(t)\right] = \frac{1}{C_F^2}\int_0^t \int_0^t E\left[i(x)i(y)\right]dxdy \tag{C.7}$$

where x and y belongs to the time interval T_1, and $t = T_1$. Similarly we have for $E\left[n_s(t)n_r(t)\right]$ and $E\left[n_r^2(t)\right]$ we have

$$E\left[n_s(t)n_r(t)\right] = \frac{1}{C_F^2}\int_0^{t_2} \int_0^{t_1} E\left[i(x)i(y)\right]dxdy \tag{C.8}$$

where x belongs to the time interval T_1, $t_1 = T_1$, y belongs to the time interval T_2, $t_2 = T_2$,

$$E\left[n_r^2(t)\right] = \frac{1}{C_F^2}\int_0^t \int_0^t E\left[i(x)i(y)\right]dxdy \tag{C.9}$$

where x and y belongs to the time interval T_2, and $t = T_2$.

C.2.1. Thermal Noise

If the single-sided power spectral density for thermal white noise is defined as is given by $\overline{i_{th}^2}$, then the autocorrelation is given as [79]

$$E[i(x)i(y)] = \frac{\overline{i_{th}^2}}{2}\delta(x-y) \tag{C.10}$$

Substituting (C.10) into (C.7) gives

$$E[n_s^2(t)] = \frac{1}{C_F^2}\int_0^t\int_0^t \frac{\overline{i_{th}^2}}{2}\delta(x-y)dxdy = \frac{\overline{i_{th}^2}}{2C_F^2}\int_0^{t_1}\delta(y-y)dy = \frac{\overline{i_{th}^2}\cdot t_1}{2C_F^2} \tag{C.11}$$

Similarly, we have

$$E[n_r^2(t)] = \frac{\overline{i_{th}^2}\cdot t_2}{2C_F^2} \tag{C.12}$$

Since the signal and reset sample time intervals do not overlap, then the cross-correlation is zero. With T_1=T_2=T, and substituting (C.11) and (C.12) into (C.5), we have for the thermal noise power

$$\sigma_{n_{DISS}}^2 = E[n_{DISS}^2(t)] = 2E[n_s^2(t)] = \frac{\overline{i_{th}^2}\cdot T}{C_F^2} \tag{C.13}$$

Thus the thermal noise variance in the case of double sampling is twice the single sampled noise variance, which is the expected result for uncorrelated noise variances.

C.2.2. Flicker Noise

The autocorrelation function for a real valued function is given by the real Fourier transform of the power spectral density according to the Wiener-Khinchin theorem [80].

$$E[i(x)i(y)] = \mathrm{Re}\left\{\int_0^\infty S_i(f)e^{j\omega(x-y)}df\right\} = \int_0^\infty S_i(f)\cos(\omega(x-y))df \tag{C.14}$$

The flicker noise power spectral density is given as

$$S_i(f) = \frac{\overline{i_{fl}^2}}{|f|} \tag{C.15}$$

Substituting (C.15) and (C.14) into (C.7) give

$$E[n_s^2(t)] = \frac{1}{C_F^2}\int_0^t\int_0^t\int_0^\infty S_i(f)\cos(\omega(x-y))dfdxdy = \frac{1}{C_F^2}\int_0^\infty \frac{\overline{i_{fl}^2}}{f}df\int_0^{t1}\int_0^{t1}\cos(\omega(x-y))dxdy \tag{C.16}$$

Solving for (C.16) we have

$$E[n_s^2(t)] = \frac{\overline{i_{fl}^2}}{C_F^2}\int_0^\infty \frac{df}{f}\frac{2(1-\cos(\omega t_1))}{\omega^2} \tag{C.17}$$

Similarly, we have

$$E[n_r^2(t)] = \frac{\overline{i_{fl}^2}}{C_F^2}\int_0^\infty \frac{df}{f}\frac{2(1-\cos(\omega t_2))}{\omega^2} \tag{C.18}$$

For the cross-correlation we find

$$E[n_s(t)n_r(t)] = \frac{\overline{i_{fl}^2}}{C_F^2}\int_0^\infty \frac{df}{f}\frac{(\cos(\omega(t_1-t_2)) - \cos(\omega t_2) - \cos(\omega t_1) + 1)}{\omega^2} \tag{C.19}$$

Substituting (C.17), (C.18), and (C.19) into (C.5) gives

$$\sigma^2_{n_{DISS}} = E\left[n^2_{DISS}(t)\right] = \frac{\overline{i_{fl}^2}}{C_F^2}\int_0^\infty \frac{df}{f}\frac{2(1-\cos(\omega\tau))}{\omega^2} \tag{C.20}$$

where $\tau = t_1 - t_2$.

We can notice that the $1/\omega^2$ term results naturally from the $1/s$ ideal transfer function of the continuous time integrator. In practice we know an op-amp integrator only behaves ideally within a specific range of frequencies. At very low frequencies, the ideal integrator behaviour will be limited by the open-loop gain of the op-amp, a_0, and at high frequencies by the unity gain frequency, f_t, such that the $1/s$ term is more appropriately written as [81]:

$$\frac{a_0}{\left(1+sC_F a_0\right)\left(1+\frac{s}{2\pi f_t}\right)} \tag{C.21}$$

The integrator as used, however, does not behave as a continuous time filter since it is constantly being reset by transistor CA_RST of Figure C.1. The charge amp is open for the integration period, T_{int}. Applying the Fourier transform to a pulse of width T_{int} gives us the following low-pass filter transfer function for the integrator. [64, 65]

$$H_{LPF}(\omega) = T_{\text{int}} e^{-j\omega T_{\text{int}}/2}\frac{\sin\left(\frac{\pi\omega}{\omega_{\text{int}}}\right)}{\left(\frac{\pi\omega}{\omega_{\text{int}}}\right)} = T_{\text{int}} e^{-j\omega T_{\text{int}}/2}\text{sinc}\left(\frac{\pi\omega}{\omega_{\text{int}}}\right) \tag{C.22}$$

where $\omega_{int} = 2\pi/T_{int}$. The above filter essentially behaves as a first order low pass filter with a time constant $\beta = T_{int}/2\pi(0.44)$. The power spectral transfer function of the integrator is found by taking the square of the magnitude of the transfer function and is given by

$$H^2_{LPF}(\omega) = \left| T_{\text{int}}\frac{\sin\left(\frac{\pi\omega}{\omega_{\text{int}}}\right)}{\left(\frac{\pi\omega}{\omega_{\text{int}}}\right)}\right|^2 = T^2_{\text{int}}\text{sinc}^2\left(\frac{\pi\omega}{\omega_{\text{int}}}\right) = T^2_{\text{int}}\text{sinc}^2\left(\pi f T_{\text{int}}\right) \tag{C.23}$$

Substituting (C.23) for the $1/\omega^2$ term of (C.20) leaves us with the following flicker noise power

$$\sigma^2_{n_{DISS}} = E\left[n^2_{DISS}(t)\right] = \frac{2 \cdot T^2_{\text{int}} \overline{i^2_{fl}}}{C^2_F} \int_0^\infty \frac{df}{f} \left(1 - \cos(\omega\tau)\right) \text{sinc}^2\left(\pi f T_{\text{int}}\right) \tag{B.24}$$

C.3. Single Integration Double Sampling

The timing diagram for single integration double sampling is shown in Figure C.3. In this double sampling method, both the signal sample (v_s) and the reset sample (v_r) are taken within the same integration cycle, though with different integration lengths of T_1 and T_2, respectively. The time separation between the signal sample and reset sample is given by τ.

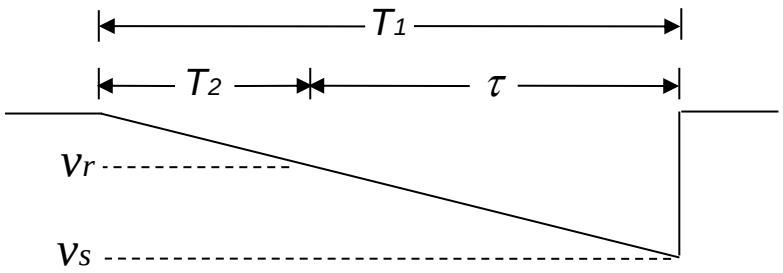

Figure C.3. Timing diagram for single integration double sampling.

C.3.1. Thermal Noise

Following the same methodology as in section C.2.1 we have once again

$$E\left[n^2_s(t)\right] = \frac{\overline{i^2_{th}} \cdot t_1}{2C^2_F} \text{ and } E\left[n^2_r(t)\right] = \frac{\overline{i^2_{th}} \cdot t_2}{2C^2_F} \tag{C.25}$$

In this instance, the signal and reset sample time intervals overlap during the time interval T_2 so the cross-correlation is no longer zero. Instead we have for the cross-correlation

$$E\left[n_s(t)n_r(t)\right]=\frac{1}{C_F^2}\int_0^{t_1}\int_0^{t_2}\frac{\overline{i_{th}^2}}{2}\delta(x-y)dxdy=\frac{\overline{i_{th}^2}}{2C_F^2}\int_0^{t_2}\delta(x-y)dy=\frac{\overline{i_{th}^2}\cdot t_2}{2C_F^2} \quad \text{(C.26)}$$

Substituting (C.25) and (C.26) into (C.5) gives for the thermal noise variance

$$E\left[n_{SIDS}^2(t)\right]=E\left[n_s^2(t)\right]-2E\left[n_s(t)n_r(t)\right]+E\left[n_r^2(t)\right]=\frac{\overline{i_{th}^2}}{2C_F^2}\left(t_1-2t_2+t_2\right)=\frac{\overline{i_{th}^2}}{2C_F^2}\left(t_1-t_2\right)=\frac{\overline{i_{th}^2}}{2C_F^2}\tau \quad \text{(C.27)}$$

Thus the thermal noise variance in the case of single integration double sampling is determined solely by the time difference between the two integrations since during the time interval T_2 the samples are completely correlated.

C.3.2. Flicker Noise

Since during the time interval T_2 the samples are completely correlated, the flicker noise resulting from the difference of the two samples depends only upon the time difference between the two integrations. In essence, the flicker noise is the same as in the case where we only integrate for time τ. Thus, we can obtain the flicker noise power by directly integrating the power spectral density giving us

$$\sigma_{n_{SIDS}}^2=\frac{\tau^2\overline{i_{fl}^2}}{C_F^2}\int_{f_{min}}^{\infty}\frac{df}{f}\mathrm{sinc}^2\left(\pi f\tau\right) \quad \text{(C.28)}$$

where f_{min} is the lower limit of integration.

Degerli [37] proposes that f_{min} is equal to $1/T_{obs}$, referring to Keshner [54], where T_{obs} is the observation time of the signal, which in this case would be equal to τ. However, such a formulation is neither qualitatively nor quantitatively true. Qualitatively speaking, when determining the variance of the flicker noise, we use many samples taken over a time interval longer than the observation time associated with the sample and hold pulse. In other words,

noise fluctuations at frequencies lower than $1/T_{obs}$ are contributing to the overall flicker noise. Quantitatively speaking, the worst case scenario for double sampling should be equal to the case where no correlation between signal samples exist, yet using $f_{min} = 1/T_{obs}$ gives a flicker noise power much less than in the case of partially correlated double sampling. Thus solely using (C.28) and equating T_{obs} to the pulse width of the S/H, or in our case, the length of the integration is incorrect. Keshner's original formulation included an additional term to account for frequencies below $1/T_{obs}$, given as [54]

$$\sigma^2_{n_{SIDS}} = \frac{\tau^2 \overline{i_{fl}^2}}{C_F^2} \int_0^{f_{\min}} S(f)df = \frac{\tau^2 \overline{i_{fl}^2}}{C_F^2} \cdot 2\left[\ln \frac{4T_{obs,total}}{T_{obs}} + 2\right] \tag{C.29}$$

Where $T_{obs,total}$ is the total observation time over which the entire sample set is taken from the point at which observations started.

Another method to deal with the inaccuracy of equating f_{min} with $1/T_{obs}$ in (C.28) is to instead use the reciprocal of the total observation time, $1/T_{obs,total}$, in place of f_{min}. In this case, the additional term given by (C.29) would not be used.

Recently, Meyer has shown that the variance of a particular sequence of N samples $\{s_n\}$, is given by [82]

$$\overline{Var\{s_n\}} = \frac{\tau^2 \overline{i_{fl}^2}}{C_F^2} \cdot 2\sum_{m=1}^{N-1} \frac{N-m}{N^2} \left\{ \ln\left|m^2\gamma^2 - 1\right| + m^2\gamma^2 \ln\left(\frac{\left|m^2\gamma^2 - 1\right|}{m^2\gamma^2}\right) + 2m\gamma \ln\left(\frac{m\gamma + 1}{\left|m\gamma - 1\right|}\right)\right\} \tag{C.30}$$

Where $\gamma = T/\tau$, T being the inter-sample time interval, and τ the integration time per sample.

C.4. Output Referred Noise in the C-APS

Using Figure 4.1, redrawn as Figure C.4 for ease, we can perform nodal analysis using superposition to determine the contribution of various noise sources at the output.

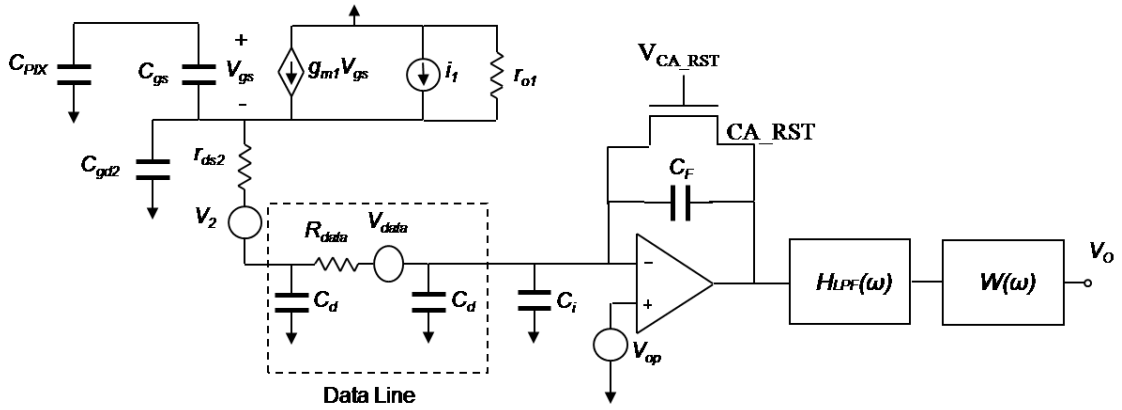

Figure C.4. Small-signal circuit for noise analysis.

C.4.1. AMP TFT noise

Using superposition, Figure C.4 is redrawn in Figure C.5 with only the AMP TFT noise source present, and all other voltage noise sources short-circuited. In addition, we have neglected the capacitances C_i (charge amp input capacitance) and C_d (portion of modeled data line capacitance adjacent to C_i), since they are shunted to ground through the virtual ground of the op-amp.

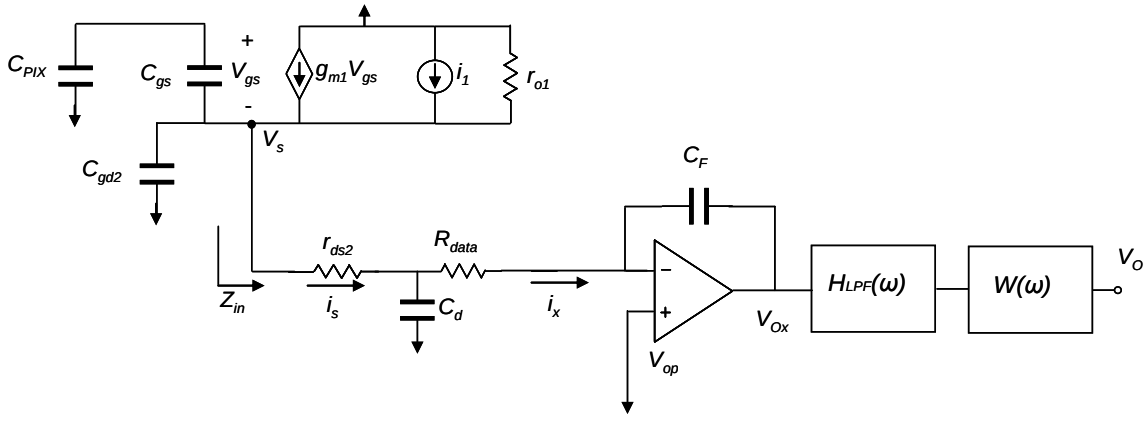

Figure C.5. Small-signal circuit for AMP TFT noise analysis.

Solving for the noise current i_x and substituting into (C.13) and (C.24) gives us the thermal and flicker noise contributions from the AMP TFT, respectively.

Performing nodal analysis at V_s, we have the following equations:

$$V_s \cdot \frac{sC_{pix}C_{gs1}}{C_{pix}+C_{gs1}} + V_s \cdot sC_{gd2} - g_{m1}V_{gs} + \frac{V_s}{r_{o1}} - i_1 = -i_s \tag{C.31}$$

$$V_s = i_s \cdot Z_{in} \tag{C.32}$$

where

$$i_s = i_x\left(1+sC_d R_{data}\right) \approx i_x \tag{C.33}$$

$$Z_{in} = \frac{r_{ds2}+R_{data}+sC_d R_{data} r_{ds2}}{1+sC_d R_{data}} \approx \frac{r_{ds2}\left(1+sC_d R_{data}\right)}{1+sC_d R_{data}} = r_{ds2}\text{, since } r_{ds2} >> R_{data} \tag{C.34}$$

The LPF refers to the filtering effect of the charge integrator. The time constant, β, associated with our LPF is set at 2 μs, which corresponds to an integration time of 5.5 μs. In our model, C_d = 16.5 pF and R_{data} = 13 kΩ. Thus, since $\beta >>$ s$R_{data}C_d$ for frequencies of interest, we can ignore the pole introduced by the dataline and $i_s = i_x$.

The voltage at the output of the integrator (op-amp) is given by:

$$\left|V_{ox}\right| = i_x \cdot \frac{1}{sC_F} \tag{C.35}$$

Writing V_{gs} in terms of V_s we have:

$$-V_{gs} = V_s \cdot \frac{C_{pix}}{C_{pix}+C_{gs1}} \tag{C.36}$$

Substituting (C.35) into (C.31) and gathering terms we have:

$$V_s \cdot \left\{ \frac{s\left[C_{pix}C_{gs1} + C_{gd2}\left(C_{pix}+C_{gs1}\right)\right] + C_{pix}g_{m1}}{C_{pix}+C_{gs1}} + \frac{1}{r_{o1}} \right\} + i_s = i_1 \tag{C.37}$$

Substituting for V_s and i_s with (C.32) and (C.33), and for i_x with (C.35), then (C.37) can be rewritten as:

$$|V_{ox}| = \frac{1}{sC_F} \cdot \frac{\left(C_{pix} + C_{gs1}\right) r_{o1} \cdot i_1}{s\left[C_{pix}C_{gs1} + C_{gd2}\left(C_{pix} + C_{gs1}\right)\right] r_{o1} r_{ds2} + C_{pix} g_{m1} r_{o1} r_{ds2} + \left(C_{pix} + C_{gs1}\right)\left(r_{o1} + r_{ds2}\right)} \quad \text{(C.38)}$$

Once again, by comparing the normalized frequency dependent term in (C.38) with β, we see that it can be neglected, and thus (C.38) is reduced to:

$$|V_{ox}| = \frac{1}{sC_F} \cdot \frac{\left(C_{pix} + C_{gs1}\right) r_{o1} \cdot i_1}{C_{pix} g_{m1} r_{o1} r_{ds2} + \left(C_{pix} + C_{gs1}\right)\left(r_{o1} + r_{ds2}\right)} = \frac{1}{sC_F} \cdot \frac{\left(C_{pix} + C_{gs1}\right) \cdot i_1}{C_{pix} g_{m1} r_{ds2} + \left(C_{pix} + C_{gs1}\right)} \quad \text{(C.39)}$$

where we have used $r_{o1} >> r_{ds2}$.

Hence, we have

$$i_x^2 = \left| \frac{\left(C_{pix} + C_{gs1}\right)}{C_{pix} g_{m1} r_{ds2} + \left(C_{pix} + C_{gs1}\right)} \right|^2 i_1^2 \quad \text{(C.40)}$$

To find the flicker or thermal noise contributions of the AMP TFT at the output, we simply need to replace $\overline{i_1^2}$ with the corresponding thermal and flicker noise spectral density, and place $\overline{i_x^2}$ into equations (C.13) and (C.24) respectively.

C.4.2. RDC TFT noise

Using superposition, Figure C.4 is redrawn in Figure C.6 with only the RDC TFT noise source present, and all other voltage noise sources short-circuited.

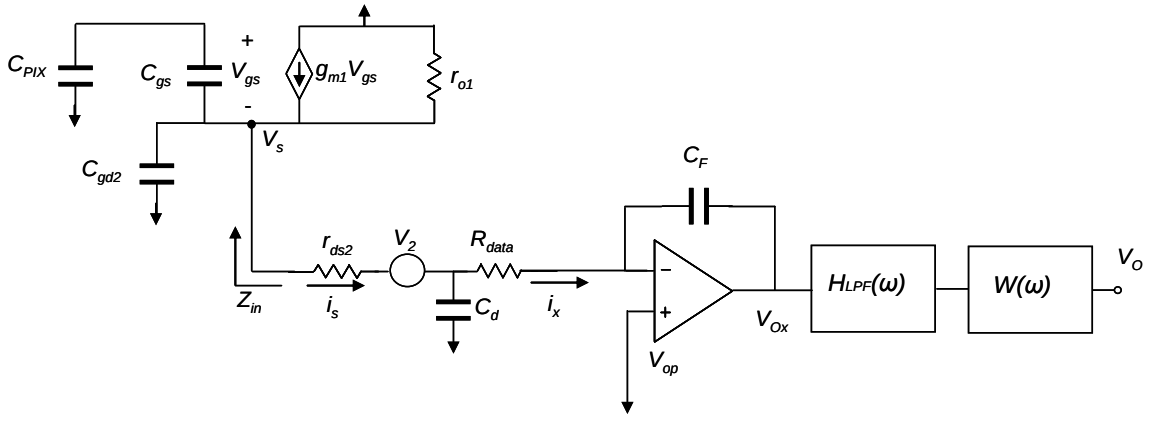

Figure C.6. Small-signal circuit for RDC TFT noise analysis.

By using a Thevenin equivalent voltage at V_s and performing a nodal analysis, we determine Z_{in} to be

$$Z_{in} = \frac{\left(C_{pix} + C_{gs1}\right) r_{o1}}{s\left[C_{pix}C_{gs1} + C_{gd2}\left(C_{pix} + C_{gs1}\right)\right] r_{o1} + C_{pix} g_{m1} r_{o1} + \left(C_{pix} + C_{gs1}\right)} \qquad \text{(C.41)}$$

By comparing the normalized frequency dependent term in (C.41) with β, we see that it cannot be completely ignored as it is on the same order of magnitude. In order to simplify our derivation, however, we will neglect its effect, which is not without warrant. The frequency dependent term only serves to reduce the amount of thermal noise contributed by the RDC TFT by restricting the bandwidth. Thus, by removing the frequency dependent term we are overestimating the effect of the RDC TFT thermal noise. As we have already seen though, the thermal noise contribution of the RDC TFT is negligible compared to the major noise sources (TFT flicker and KTC noise). By including the frequency dependent term, we would make its contribution simply less than it already is. In addition, we find that $C_{pix}g_{m1}r_{o1} >> (C_{pix} + C_{gs1})$. Taking these points into account, we can simplify Z_{in} to be

$$Z_{in} = \frac{C_{pix} + C_{gs1}}{g_{m1} C_{pix}} \qquad \text{(C.42)}$$

By making use of (C.33) and (C.34), and incorporating (C.42), Figure A.3 can be simplified and is redrawn in Figure C.7.

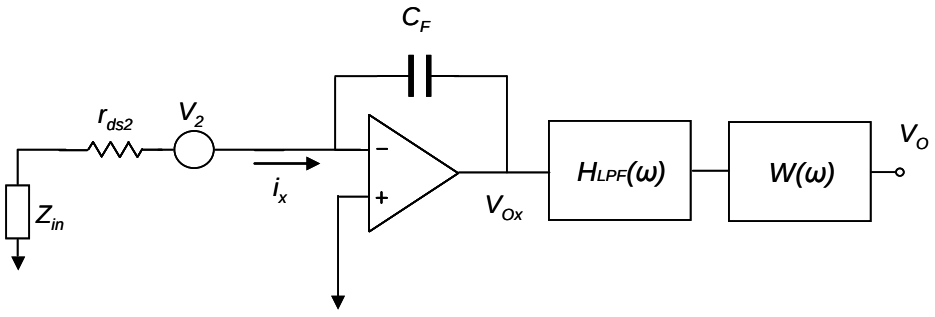

Figure C.7. Simplified small-signal circuit for RDC TFT noise analysis.

Using Figure C.7, solving for the input noise current psd can be quickly determined as

$$i_x^2 = \left| \frac{g_{m1} C_{pix} r_{ds2}}{C_{pix} g_{m1} r_{ds2} + \left(C_{pix} + C_{gs1}\right)} \right|^2 i_2^2 \qquad \text{(C.43)}$$

To find the flicker or thermal noise contributions of the RDC TFT at the output, we simply need to replace $\overline{i_2^2}$ with the corresponding thermal and flicker noise spectral density, and place $\overline{i_x^2}$ into equations (C.13) and (C.24) respectively.

C.4.3. Dataline noise

The data line is modeled using a π-model composed of two capacitors (C_d) and a single resistor (R_{data}) which gives a more accurate noise response than a lumped RC model. Assuming the RDC TFT is off (which gives the worst-case scenario as it results in a larger noise bandwidth), Figure C.4 is redrawn in Figure C.8 with only the dataline noise source present, and all other voltage noise sources short-circuited.

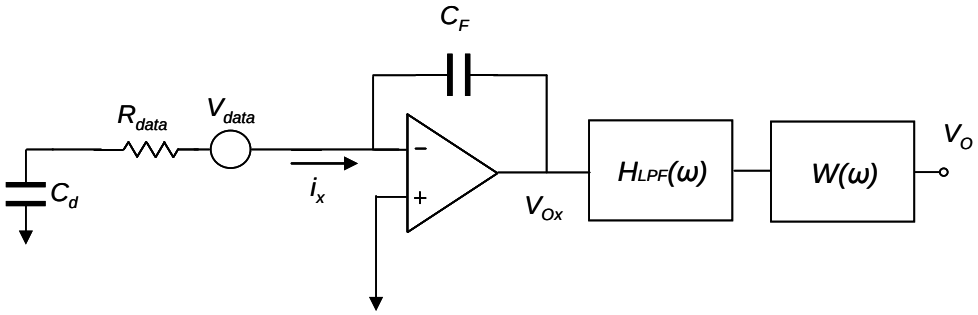

Figure C.8. Small-signal circuit for dataline noise analysis.

A quick analysis using Figure C.8 allows us to solve for the output noise voltage variance to be

$$\overline{V_o^2} = \overline{V_{data}^2} \left(\frac{C_d}{C_F} \right)^2 \int_0^\infty \left| \frac{1}{(1 + sC_d R_{data})} \right|^2 H_{LPF}^2(\omega) W^2(\omega) df \qquad \text{(C.44)}$$

If $\beta >> C_d R_{data}$, then we can once again ignore the pole introduced by the dataline, and we have

$$\overline{V_o^2} = \overline{V_{data}^2}\left(\frac{C_d}{C_F}\right)^2 \int_0^\infty H_{LPF}^2(\omega) W^2(\omega) df = \overline{V_{data}^2}\left(\frac{C_d}{C_F}\right)^2 \int_0^\infty \frac{1}{1+\omega^2\beta^2} \cdot 2\{1-\cos(\omega\tau)\} df \tag{C.45}$$

Here we have replaced the discrete time filter with its continuous time pseudo-equivalent for ease of notation. Also, recall that $\beta = T_{int}/2\pi(0.44)$ for the discrete time filter, and that the double sampling operation only serves to double the thermal noise due to the uncorrelated nature of white noise. Using the well known formula for the integral of the squared value of first order low pass filter, namely,

$$\overline{V_{LPF}^2} = \int_0^\infty H_{LPF}^2(\omega) = \int_0^\infty \frac{1}{1+\omega^2\beta^2} = \frac{\pi}{2} f_0 = \frac{1}{4\beta} \tag{C.46}$$

our output referred data line thermal noise voltage with double sampling is reduced to

$$\overline{V_o^2} = \overline{V_{data}^2}\left(\frac{C_d}{C_F}\right)^2 \frac{1}{2\beta} \tag{C.47}$$

C.4.4. Op-amp noise

Assuming the RDC TFT is off, Figure C.4 is redrawn in Figure C.9 with only the op-amp noise source present, and all other voltage noise sources short-circuited. Notice that C_i and C_d cannot be neglected in the derivation since the noise originates from the op-amp, and hence the inverting terminal of the op-amp is no longer at virtual ground.

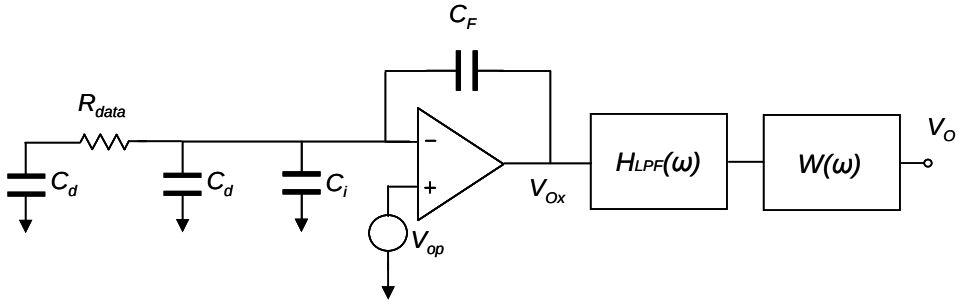

Figure C.9. Small-signal circuit for op-amp noise analysis.

Simplifying Figure C.9 into the form of Figure C.10, we can apply the typical non-inverting op-amp formula, (C.48), to determine the op-amp noise voltage variance contribution at the output.

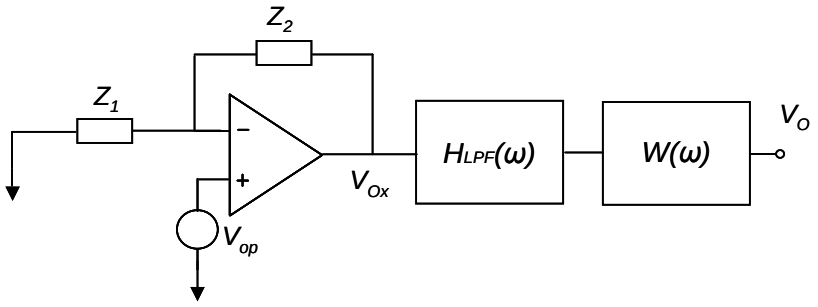

Figure C.10. Simplified small-signal circuit for op-amp noise analysis.

$$V_{ox} = \left(1 + \frac{Z_2}{Z_1}\right) V_{op} \tag{C.48}$$

where

$$Z_1 = \frac{1 + sR_{data}C_d}{s(2C_d + C_i) + sR_{data}C_d(C_d + C_i)} \text{ and } Z_2 = \frac{1}{sC_F} \tag{C.49}$$

Inserting (C.49) into (C.48) and gathering terms gives us

$$V_{ox} = \frac{(C_F + 2C_d + C_i) + sR_{data}C_d(C_F + C_d + C_i)}{C_F(1 + sC_dR_{data})} V_{op} \tag{C.50}$$

If we again assume that $\beta >> C_dR_{data}$ then (C.50) can be simplified to

$$V_{ox} = \frac{(C_F + 2C_d + C_i)}{C_F} V_{op} \tag{C.51}$$

Adding our low-pass filter (LPF) and double-sampling (DS) transfer functions, taking the square of both sides, and integrating over all frequencies gives our total noise variance as:

$$\overline{V_o^2} = \left\{ \overline{V_{op}^2} \left(\frac{C_F + 2C_d + C_i}{C_F} \right)^2 \right\} \int_0^\infty \frac{2(1 - \cos(\omega\tau))}{1 + \omega^2\beta^2} df \tag{C.52}$$

The op-amp noise voltage can be described in terms of its thermal and flicker noise components as

$$\overline{V_{op}^2} = \left(1 + \frac{f_{ce}}{f}\right) \overline{V_{th}^2} \tag{C.53}$$

where V^2_{th} is the thermal noise density and f_{ce} is the $1/f$ corner frequency of the charge amplifier. Using the same analysis as was performed for the dataline noise to determine the value of the integral in (C.52), the output thermal noise voltage variance of the op-amp is given as

$$\overline{V^2_{o,th}} = \overline{V^2_{op}}\left(\frac{C_F + 2C_d + C_i}{C_F}\right)^2 \frac{1}{2\beta} \tag{C.54}$$

Substituting the flicker noise component of (C.53) into (4.25) gives us the following flicker noise voltage

$$\overline{V^2_{o,op,f}} = \left\{ f_{ce}\overline{V^2_{th}}\left(\frac{2C_d + C_i + C_F}{C_F}\right)^2 \right\} \int_0^\infty \frac{2(1-\cos(\omega\tau))}{f(1+\omega^2\beta^2)} df \tag{C.55}$$

We can solve for the flicker noise component using numerical integration methods.

C.5. Noise Optimization as a Function of TFT Aspect Ratio

In order to optimize our circuit for low-noise performance as a function of TFT aspect ratio, we must first simplify our derived noise equations in terms of TFT aspect ratio.

C.5.1. TFT Flicker noise

The AMP and RDC transistor noise components can be combined by substituting (C.40) and (C.43) into (C.24), then adding and collecting terms gives (C.56) below

$$\overline{V_o^2} = \frac{2\cdot T_{\text{int}}^2}{C_F^2}\left\{\overline{i_2^2}(r_{ds2}g_{m1}C_{PIX})^2 + \overline{i_1^2}(C_{gs}+C_{PIX})^2\right\}\int_0^\infty \frac{df}{f}\left|\frac{1}{(C_{PIX}g_{m1}r_{ds2}+C_{PIX}+C_{gs1})}\right|^2 (1-\cos(\omega\tau))\text{sinc}^2(\pi f T_{\text{int}}) \tag{C.56}$$

In order to express the AMP and RDC TFT flicker noise in terms of device dimensions, we can begin by simplifying (C.56) such that

$$\overline{V^2_{o,fl}} = \frac{2\cdot T_{\text{int}}^2\left\{\overline{i^2_{2,fN}}(r_{ds2}g_{m1}C_{PIX})^2 + \overline{i^2_{1,fN}}(C_{gs1}+C_{PIX})^2\right\}}{C_F^2(C_{PIX}g_{m1}r_{ds2}+C_{PIX}+C_{gs1})^2} I_f(\lambda) \tag{C.57}$$

and $I_f(\lambda)$ is given by

$$I_f(\lambda) = \int_0^\infty \frac{df}{f}\left(1-\cos(\omega\tau)\right)\mathrm{sinc}^2\left(\pi f T_{\mathrm{int}}\right) \tag{C.58}$$

Here $\overline{i_{2,fN}^2}$ and $\overline{i_{1,fN}^2}$ represent the flicker noise voltage and current densities with the $1/f$ component removed and incorporated into $I_f(\lambda)$. The flicker noise can now be normalized with respect to the integral portion, $I_f(\lambda)$, which is independent of the device dimensions and thus can be ignored in our following optimizations.

The normalized AMP transistor flicker noise is then given by

$$\overline{V_{o,fl,N1}^2} = \frac{\overline{i_{1,fN}^2}(C_{gs1}+C_{PIX})^2 2T_{\mathrm{int}}^2}{C_F^2(C_{PIX}g_{m1}r_{ds2}+C_{PIX}+C_{gs1})^2} \tag{C.59}$$

The flicker noise can simplified by rewriting part of the denominator,

$$C_{PIX}g_{m1}r_{ds2}+C_{PIX}+C_{gs1} = C_{gs1}+(1+g_{m1}r_{ds2})C_{PIX} = C_{gs1}+\frac{g_{m1}}{G_m}C_{PIX} \tag{C.60}$$

where G_m is the circuit transconductance, and is given by

$$G_m = \frac{g_{m1}}{1+g_{m1}r_{ds2}} \tag{C.61}$$

The normalized input referred flicker noise charge in mean-squared electrons is given by

$$\overline{q_{fl,N1}^2} = \frac{\overline{V_{o,fl,N1}^2}C_F^2}{G_i^2 q^2} \tag{C.62}$$

where G_i is the circuit charge gain, and is given by[2]

$$G_i = \frac{G_m T_{\mathrm{int}}}{C_{eff}} \tag{C.63}$$

By combining (4.43) and (C.61), the sense node capacitance can be rewritten as

$$C_{eff} = \frac{G_m}{g_{m1}}\left(\frac{g_{m1}}{G_m}C_{PIX}+C_{gs1}\right) \tag{C.64}$$

Substituting (C.64) into (C.63), the charge gain can be rewritten as

$$G_i = \frac{g_{m1}T_{\mathrm{int}}}{C_{gs1}+\frac{g_{m1}}{G_m}C_{PIX}} \tag{C.65}$$

Substituting (C.59), (C.60), and (C.65) into (C.62) gives

$$\overline{q_{fl,N1}^2} = \frac{2\overline{i_{1,fN}^2}\left(C_{gs1} + C_{PIX}\right)^2}{g_{m1}^2 q^2} \tag{C.66}$$

Substituting (4.18) into (C.66) gives

$$\overline{q_{fl,N1}^2} = \frac{\alpha_H \left(C_{gs1} + C_{PIX}\right)^2 (V_{GS1} - V_{T1})}{C_{ox} W_1 L_1 q} \tag{C.67}$$

The normalized RDC transistor flicker noise is given by

$$\overline{V_{o,fl,N2}^2} = \frac{\overline{V_{2,fN}^2} (g_{m1} C_{PIX})^2 2T_{\text{int}}^2}{C_F^2 (C_{PIX} g_{m1} r_{ds2} + C_{PIX} + C_{gs1})^2} \tag{C.68}$$

Following the same methodology as for the AMP transistor, and substituting $\overline{V_{2,fN}^2} = r_{ds2}^2 \overline{i_{2,fN}^2}$ gives the input referred flicker noise charge as

$$\overline{q_{fl,N2}^2} = \frac{2\overline{i_{2,fN}^2}(r_{ds2} C_{PIX})^2}{q^2} \tag{C.69}$$

Substituting (4.19) into (C.69) and writing r_{ds2} in terms of device dimensions gives

$$\overline{q_{fl,N2}^2} = \frac{2C_{PIX}^2 \alpha_H (V_{GS2} - V_{T2}) V_{DS2}^2}{q C_{ox} W_2 L_2 (V_{GS2} - V_{T2} - V_{DS2})^2} \tag{C.70}$$

C.5.2. TFT Thermal noise

In order to express the AMP and RDC TFT thermal noise in terms of device dimensions, we can begin by substituting (C.40) and (C.43) into (C.13), then adding and collecting terms gives (C.71)

$$\overline{V_{o,th}^2} = \frac{\left\{\overline{i_{2,th}^2}(r_{ds2} g_{m1} C_{PIX})^2 + \overline{i_{1,th}^2}(C_{gs1} + C_{PIX})^2\right\} T_{\text{int}}}{C_F^2 (C_{PIX} g_{m1} r_{ds2} + C_{PIX} + C_{gs1})^2} \tag{C.71}$$

The AMP transistor thermal noise is then given by

$$\overline{V_{o,th1}^2} = \frac{\overline{i_{1,th}^2}(C_{gs1} + C_{PIX})^2 T_{\text{int}}}{C_F^2 (C_{PIX} g_{m1} r_{ds2} + C_{PIX} + C_{gs1})^2} \tag{C.72}$$

Performing similar substitutions as for the case of flicker noise and substituting for g_{m1}, we find the input referred AMP transistor thermal noise in mean-squared electrons is given by

$$\overline{q_{th1}^2} = \frac{8kT\left(C_{gs1} + C_{PIX}\right)^2 L_1}{3q^2 T_{\text{int}} \mu_{eff} C_{ox} W_1 \left(V_{GS1} - V_{T1}\right)} \tag{C.73}$$

The RDC transistor thermal noise is then given by

$$\overline{V_{o,th,N2}^2} = \frac{\overline{i_{2,th}^2} (r_{ds2} g_{m1} C_{PIX})^2 T_{\text{int}}}{C_F^2 (C_{PIX} g_{m1} r_{ds2} + C_{PIX} + C_{gs1})^2} \tag{C.74}$$

Through substitution, we find the normalized input referred RDC transistor thermal noise in mean-squared electrons is given by

$$\overline{q_{th,N2}^2} = \frac{4kTr_{ds2} C_{PIX}^2}{q^2 T_{\text{int}}} = \frac{4kTC_{PIX}^2 L_2}{q^2 T_{\text{int}} \mu_{eff} C_{ox} W_2 \left(V_{GS2} - V_{T2} - V_{DS2}\right)} \tag{C.75}$$