Multipath Miller Compensation for Switched-Capacitor Systems

by

Zhao Li

A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Master of Applied Science
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2011

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

A hybrid operational amplifier compensation technique using Miller and multipath compensation is presented for multi-stage amplifier designs. Unconditional stability is achieved by the means of pole-zero cancellation where left-half zeros cancel out the non-dominant poles of the operational amplifier. The compensation technique is stable over process, temperature, and voltage variations.

Compared to conventional Miller-compensation, the proposed compensation technique exhibits improved settling response for operational amplifiers with the same gain, bandwidth, power, and area. For the same settling time, the proposed compensation technique will require less area and consume less power than conventional Miller-compensation. Furthermore, the proposed technique exhibits improved output slew rate and lower noise over the conventional Miller-compensation technique.

Two-stage operational amplifiers were designed in a 0.18 μm CMOS process using the proposed technique and conventional Miller-compensated technique. The design procedure for the two-stage amplifier is applicable for higher-order amplifier designs. The amplifiers were incorporated into a switched-capacitor oscillator where the oscillation harmonics are dependent on the settling behaviour of the op amps. The superior settling response of the proposed compensation technique results in a improved output waveform from the oscillator.

Acknowledgements

I would like to thank all the people who helped me along the way. First, I would like to thank my supervisor, David Nairn, for providing advice, encouragement, and most of all patience. I am deeply grateful for the academic freedom he afforded me, but also for reining me in whenever I strayed too far from the objective.

I would also like to thank the rest of the group including Noman, Jason, and Adam. It was a pleasure discussing various circuit and non-circuit topics with you.

Many people outside the group have helped me through my Master's. I would like acknowledge my friends at the university for keeping me sane over the last two years. Special thanks to Melissa for her help with editing this dissertation.

Finally, I am indebted to my parents for their unconditional support for my endeavours. This thesis would not have been possible without them.

Dedication

To the two most important women in my life: my mother for putting up with all my antics and my paternal grandmother for raising me.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

The operational amplifier, or op amp, is the main building block in almost all analog circuits. The performance of most analog and mixed-signal systems are limited by the op amp. For example, the resolution of pipelined ADCs is determined by the gain of its op amps [1, 2]. The push for increasingly large scale integration has forced analog and mixed-signal designers to use advanced CMOS processes that suffer from lower transistor gain and supply voltage. A common technique to increase the gain of an op amp is through cascoding (vertical gain enhancement). Cascode circuits require additional voltage headroom but that has not been a major issue in past designs [3]. However, with the aggressive voltage scaling in advanced CMOS processes, it will become increasingly challenging for designers to realize high gain op amps using only the technique of cascoding.

Another method for increasing gain is to cascade multiple amplifiers in series (horizontal gain enhancement). Although cascading does not consume voltage headroom, the presence of additional poles can compromise the stability of the system, once the amplifier is placed in a feedback loop. Pole splitting is the most common technique for stabilizing multi-stage

op amps. However, stability is achieved at the expense of bandwidth. In this work, the effects of feedforward compensation are examined and circuit techniques for overcoming the bandwidth restriction due to pole splitting are developed.

1.1 Outline

The thesis is structured as follows: Chapter 2 reviews the simple one-pole model for op amps and provides background information on multi-stage op-amps. Popular techniques for frequency compensating multi-stage op-amps are also discussed. Chapter 3 discusses how feedforward paths can be added to improve the performance of frequency compensated op-amps. In Chapter 4, the system-level design of a switched-capacitor oscillator is introduced. The oscillator is used to compare the performance of op-amps with and without the feedforward paths enabled. Chapter 5 describes the circuit design of the oscillator in a 0.18 μm CMOS technology. Improvements to the design are presented in Chapter 6. Chapter 7 concludes the thesis and discusses future work in the area of feedforward compensation.

Chapter 2

Background Information

In the majority of integrated circuit applications, the op amp is used to drive on-chip capacitive loads. In this thesis, the focus will be on the operational transconductance amplifier (OTA) which is the most popular form of op amp for integrated circuit designs [4,5]. Unlike op-amps, OTAs are amplifiers with a high output impedance. This is sufficient for most applications where the load is capacitive.

This chapter will provide background information on the op amp. Section 2.1 reviews the relationship between system-level specifications and op amp specifications. Section 2.2 discusses the fundamentals of amplifier stability. Characteristics and mathematical models of the single- and two-stage op amps are presented in Section 2.3 and 2.4, respectively. Finally, Section 2.5 reviews multistage op amp architectures.

2.1 Amplifier Requirements

Op amps are commonly found in negative feedback systems. Negative feedback is particularly desirable as it can desensitize the gain, improve linearity, increase bandwidth, and reduce noise in a system [6]. A common feedback configuration is the inverting amplifier as depicted in Fig. 2.1. The transfer function of the system is

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = -\frac{C_{\text{I}}/C_{\text{F}}}{1 + \frac{1+C_{\text{I}}/C_{\text{F}}}{A(s)}} \tag{2.1}$$

where A(s) is the op amp gain. If A(s) is very large, Eq. 2.1 becomes approximately

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx -\frac{C_{\text{I}}}{C_{\text{F}}} \tag{2.2}$$

The above equation shows that if the gain of the op amp is sufficiently large, the closed-loop transfer function of a system will be independent of the op amp's characteristics.

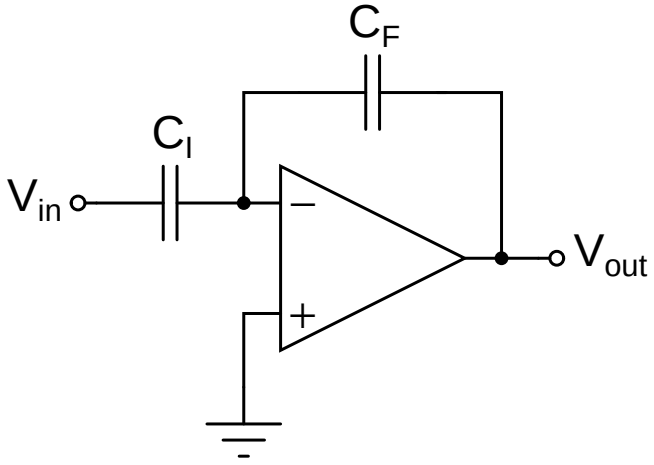


Figure 2.1: An inverting amplifier configuration commonly found in integrated circuits.

2.1.1 DC Gain

Unless an op amp has infinite gain, there will be some error in the system's transfer function. For the inverting amplifier in Fig. 2.1, its transfer function, Eq. 2.1, can be rewritten as

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\left(\frac{C_{\text{I}}}{C_{\text{F}}}\right)\left(\frac{1}{1+\frac{1+C_{\text{I}}/C_{\text{F}}}{A_0}}\right) \tag{2.3}$$

where A_0 is the DC gain of the op amp. Eq. 2.3 can be approximated by its first-order Maclaurin series as

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx -\left(\frac{C_{\text{I}}}{C_{\text{F}}}\right)\left(1-\frac{1+C_{\text{I}}/C_{\text{F}}}{A_0}\right) \tag{2.4}$$

The error of the closed-loop gain is thus

$$\epsilon = \frac{1+C_{\text{I}}/C_{\text{F}}}{A_0} = \frac{1}{\beta A_0} = \frac{1}{L_{\text{g,0}}} \tag{2.5}$$

where β is the feedback factor and is defined as the ratio between C_F and the sum of all the capacitances connected to the inverting node of the op amp. In many systems, β is dimensionless and frequency independent. In this amplifier configuration, the feedback factor is

$$\beta = \frac{C_{\text{F}}}{\Sigma C_i} = \frac{C_{\text{F}}}{C_{\text{F}}+C_{\text{I}}} \tag{2.6}$$

The term βA_0, or $L_{\text{g,0}}$, is a dimensionless parameter known as the DC loop gain. As will be demonstrated later in this chapter, the loop gain ($L_{\text{g}} = \beta A$) is a very important parameter in feedback systems.

In data converter systems, the gain error, ϵ, is generally expressed in terms of the number of bits, N, where

$$\epsilon = \frac{1}{2^{\text{N}}} \tag{2.7}$$

Substituting Eq. 2.7 into Eq. 2.5 yields the minimum loop gain required to achieve N-bits of accuracy.

$$L_{\text{g}} \geq 2^N = 6.02N \text{ [dB]} \tag{2.8}$$

which means that higher resolution data converters require higher op amp DC gain.

2.1.2 Bandwidth

In many applications, such as in switched-capacitor circuits, the maximum speed in which the circuit can operate is determined by its settling time. As illustrated in Fig. 2.2, settling time is defined as the time it takes for the output to settle to within a specified error range. In linear systems, settling time is dependant on the bandwidth or more specifically the gain-bandwidth product of the op amp.

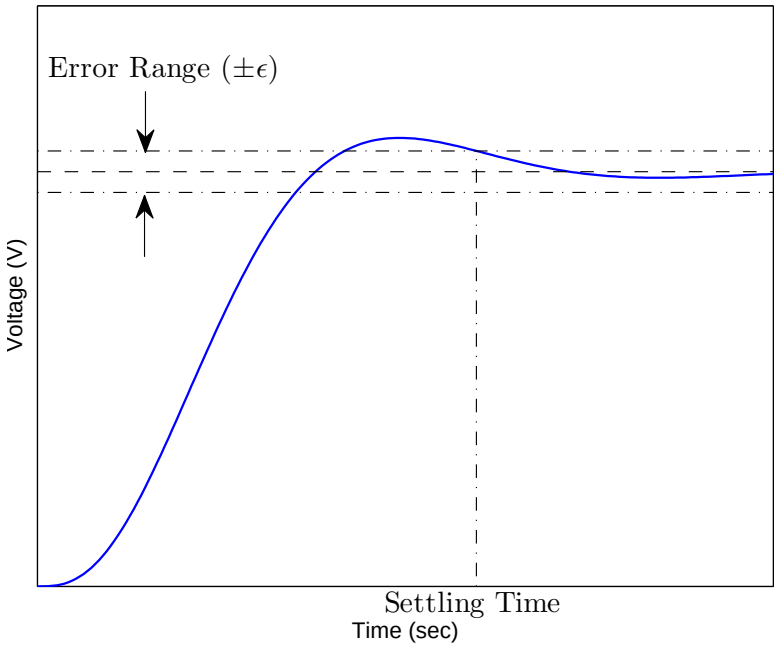


Figure 2.2: Step response characteristics of a linear system.

The transfer function of an one-pole op amp is

$$A(s) = \frac{A_0}{1 + s/\omega_b} \tag{2.9}$$

where ω_b is the bandwidth (and pole frequency) of the open-loop op amp.

When the op amp is placed in a negative feedback loop, its high DC gain is traded off for much higher bandwidth. In systems where the frequency of interest is much greater than the open-loop bandwidth, the op amp can be accurately modelled as an integrator [5, 7] where

$$A(s) \approx \frac{A_0}{s/\omega_b} = \frac{\omega_{\mathrm{T}}}{s} \tag{2.10}$$

where ω_{T} is the gain-bandwidth product and is defined as

$$\omega_{\mathrm{T}} = A_0 \omega_b \tag{2.11}$$

Substituting Eq. 2.10 into Eq. 2.1 leads to

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = -\frac{C_{\mathrm{I}}/C_{\mathrm{F}}}{1 + \frac{(1+C_{\mathrm{I}}/C_{\mathrm{F}})s}{\omega_{\mathrm{T}}}} = -\frac{C_{\mathrm{I}}/C_{\mathrm{F}}}{1 + \frac{s}{\beta\omega_{\mathrm{T}}}} \tag{2.12}$$

where

$$\beta\omega_{\mathrm{T}} = \left(\frac{C_{\mathrm{F}}}{C_{\mathrm{F}} + C_{\mathrm{I}}}\right)\omega_{\mathrm{T}} \tag{2.13}$$

is the closed-loop bandwidth.

For a first-order system characterized by Eq. 2.12, the step response is

$$V_{\mathrm{out}} = -\frac{C_{\mathrm{I}}}{C_{\mathrm{F}}}\left(1 - e^{-t\beta\omega_{\mathrm{T}}}\right) V_{\mathrm{in}} \tag{2.14}$$

where the exponential term is the settling error. From Eq. 2.14, the required $\beta\omega_{\mathrm{T}}$ for a specified settling time (shown in Fig. 2.2), T, and error, ϵ, is

$$\beta\omega_{\mathrm{T}} = \frac{-\ln\epsilon}{T} \tag{2.15}$$

In data converter systems where the output signal generally has to settle to within the least-significant-bit in one half of the clock period (i.e. $\mathrm{T} = \frac{1}{2f_{\mathrm{clk}}}$), the required closed-loop

bandwidth can be obtained by substituting Eq. 2.7 into 2.15

$$\beta\omega_{\mathrm{T}} = 2Nf_{\mathrm{clk}}\ln 2 \tag{2.16}$$

The above equation shows that the necessary op amp closed-loop bandwidth, and hence the gain-bandwidth product, increases for higher resolution or higher sampling rate data converters.

2.2 Stability

When an op amp is placed inside a negative feedback loop, it is possible for the system to become unstable. If a system's transient response to a bounded input is bounded, the system is considered to be BIBO (bounded-input-bounded-output) stable. For linear systems, a necessary and sufficient condition for BIBO stability is if all the poles of the closed-loop system are in the left-hand side of the s-plane [8]. Poles are determined by the roots of the denominator of the system transfer function. A system is conditionally stable if a pair of poles is on the imaginary axis while all other poles are in the left-half plane.

It is extremely difficult and time-consuming for circuit designers to obtain the exact closed-loop transfer function of a system. The problem is compounded when process, temperature, and voltage (PVT) variations need to be accounted for. Fortunately, methods, such as the Nyquist stability criterion and phase margin, have been developed to assess the stability of a system without needing to determine its transfer function.

2.2.1 Nyquist Stability Criterion

The Nyquist stability criterion is a graphical technique for ascertaining the stability of a feedback system by observing its Nyquist plot. A Nyquist plot is generated by plotting

the magnitude and phase response of an open-loop system in polar coordinates as the frequency is varied [6], if the feedback factor, β, is unity for all frequencies. When β is not unity for all frequencies, the plot should be of the loop gain, $L_g(j\omega) = \beta(j\omega)A(j\omega)$, instead of simply just the op amp's open loop gain $A(j\omega)$. An exemplary Nyquist plot is shown in Fig. 2.3. According to the Nyquist stability criterion, a system is stable if the number of clockwise encirclements at the point $(-1, 0)$ is exactly $\aleph = -\mathrm{P}$, where P is the number of open-loop poles (i.e. poles of $L_g(s)$) in the right-half plane.

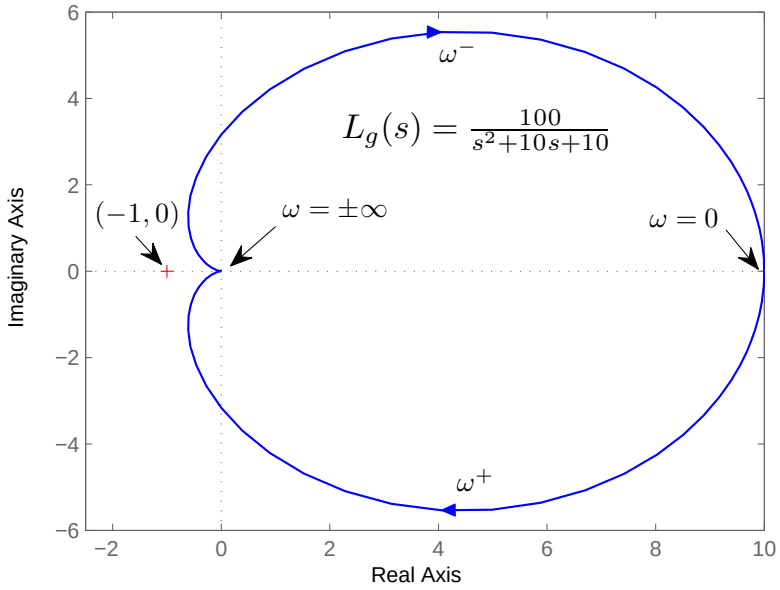


Figure 2.3: An example Nyquist plot. The system is stable as there are no encirclements at the point $(-1, 0)$.

In the usual case where $P = 0$[1] [8], the Nyquist criterion can be simplified to the following statement: A feedback system is stable, based on the Nyquist criterion, if the Nyquist plot of $L_g(j\omega)$ has no encirclements at the point $(-1, 0)$. The point $(-1, 0)$ marks

[1]In most feedback designs with op amps, $P = 0$ since op amps are generally open-loop stable (no poles on the right-half plane).

where the magnitude response is 1 V/V (0 dB) and the phase response is $-180°$.

2.2.2 Phase Margin

Based on the above observations, a linear system's stability can be determined directly from its Bode plot. To ensure no encirclements at the point (-1, 0) in the Nyquist plot, the phase of $L_g(j\omega)$ must be no less than $-180°$ at its unity-gain frequency. Phase margin (PM) is defined as the amount of additional phase lag required of $L_g(j\omega)$ so that the system becomes unstable [8]. It is measured by adding 180° to the phase of $L_g(j\omega)$ at the frequency where $|L_g(j\omega)| = 1$. This is illustrated in Fig. 2.4. A positive phase margin indicates that the system is stable. Phase margin is a means of not only determining the stability of a system but also its relative stability. A higher phase margin is indicative of a system that is more stable and one that is also more robust to PVT variations. In typical op amp designs, a minimum phase margin of 45 degrees is desired [9, 10].

2.3 Single-Stage Op Amps

The single-stage op amp is the most basic op amp structure. Its block diagram and a simplified transistor implementation are shown in Fig. 2.5. With only one dominant pole, the single-stage op amp can achieve one of the highest gain-bandwidth products amongst all op amp architectures. However, the architecture suffers from very low DC gains, especially in advanced CMOS processes. The DC gain can be improved through cascoding, but this comes at the expense of reduced voltage headroom and stability margin [11, 12]. Reduced voltage headroom is highly undesirable as it degrades the system's signal-to-noise ratio and increases sensitivity to PVT variations. Furthermore, the reduced supply voltage in

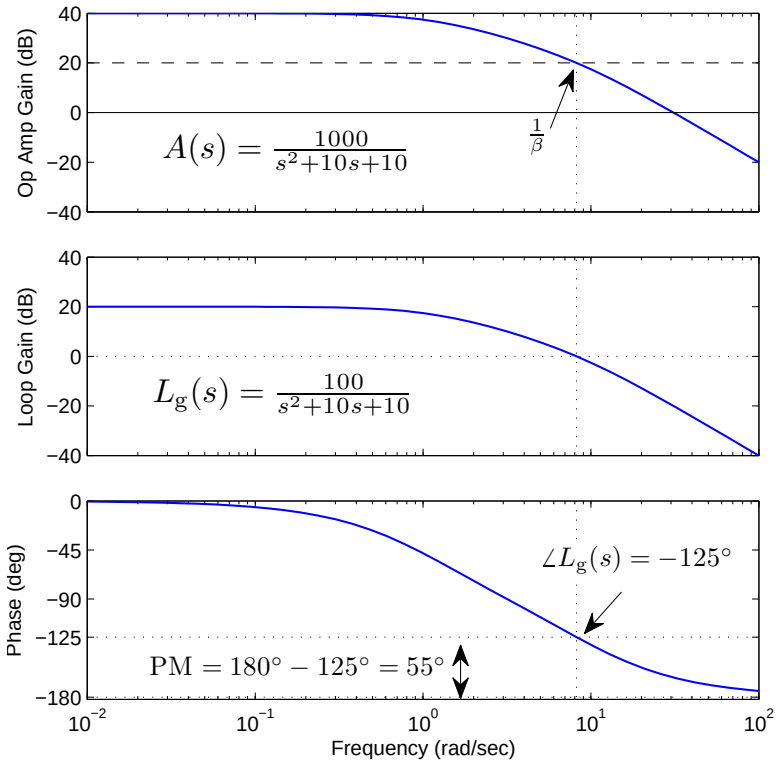


Figure 2.4: An example phase margin measurement. The feedback factor, β, is 0.1 and is frequency independent.

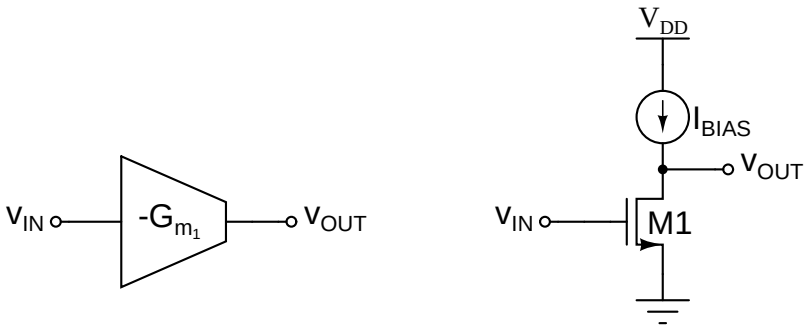
advanced CMOS processes acts as another obstacle to using vertical gain enhancement to meet a specified DC gain requirement.

Fig. 2.6 shows the low-to-medium frequency small-signal model of the op amp depicted in Fig. 2.5. The transfer function of the op amp, when driven by a low-impedance source, is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = A(s) = -\frac{g_{m_1} r_{o_1}}{1 + s r_{o_1} C_L} \tag{2.17}$$

where the DC gain is

$$A_0 = -g_{m_1} r_{o_1} \tag{2.18}$$



(a) Block Diagram. (b) Transistor Implementation.

Figure 2.5: Block diagram and simple transistor implementation of a single-stage op amp.

The op amp bandwidth is set by the pole at

$$\omega_{p1} = \frac{1}{r_{o_1} C_L} \tag{2.19}$$

and the gain-bandwidth product is

$$\omega_{\mathrm{T}} = \frac{g_{m_1}}{C_L} \tag{2.20}$$

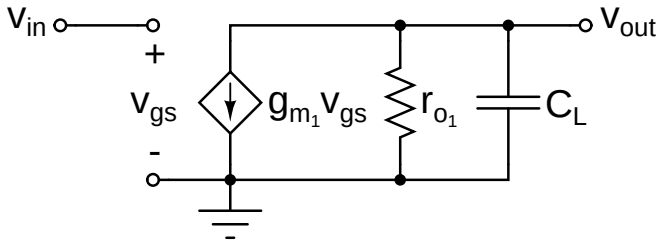


Figure 2.6: Small-signal model of a single-stage op amp.

The advantage of the single-stage op amp lies in its stability and predictability. Since its transfer function has only one pole, the phase response, for all frequencies, will never drop below $-90°$. This means that the phase margin will always be positive and the amplifier

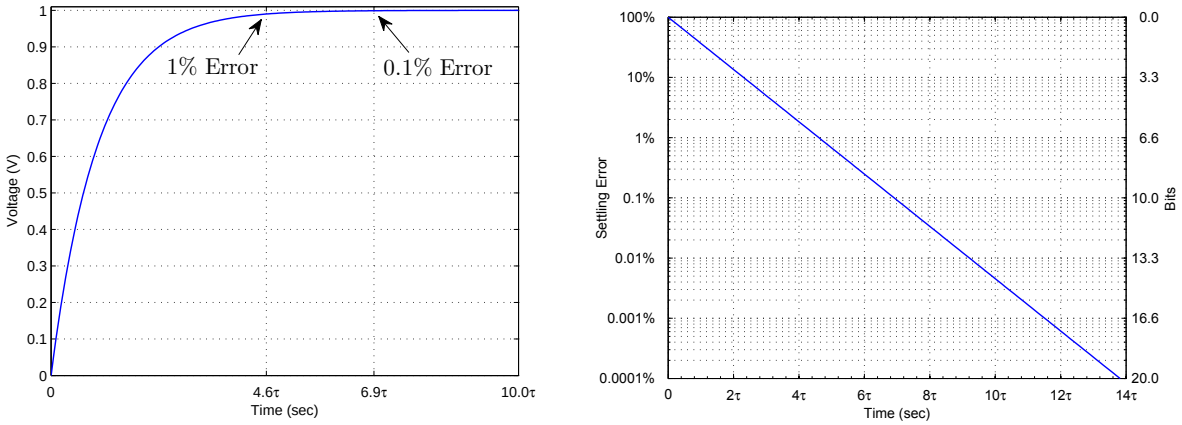
will be stable for all values of β. The closed-loop step response of 2.17 is

$$\begin{aligned} V_{\text{out}} &= A_{\text{CL}} \left(1 - e^{-t\beta\omega_{\text{T}}}\right) V_{\text{in}} \\ &= A_{\text{CL}} \left(1 - e^{-\frac{t}{\tau}}\right) V_{\text{in}} \end{aligned} \tag{2.21}$$

where A_{CL} is the closed-loop gain of the amplifier and

$$\tau = \frac{1}{\beta\omega_{\text{T}}} \tag{2.22}$$

is the closed-loop time constant. The first-order settling behaviour of the circuit implies predictable settling behaviour. As illustrated in Fig. 2.7a, it takes 4.6τ to reach 1% settling accuracy and 6.9τ to reach 0.1% settling accuracy. Fig. 2.7b plots the settling accuracy versus settling time of first-order systems, normalized to $\tau = unit1\text{s}$.



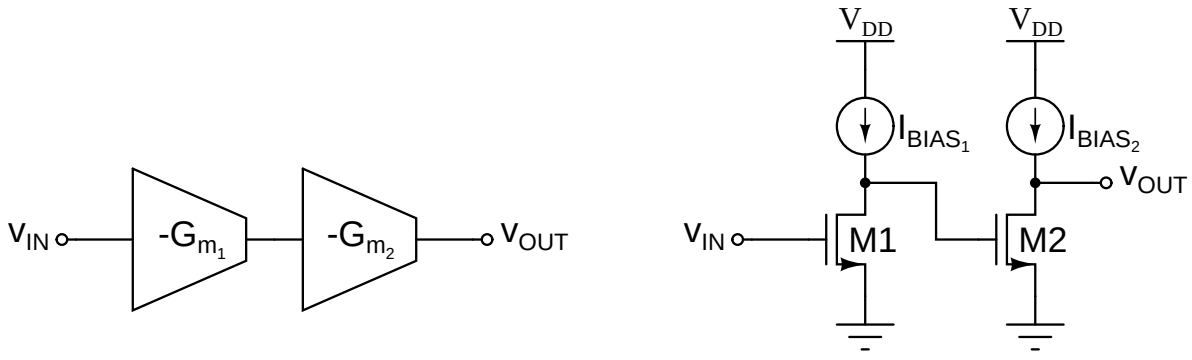
(a) Step response of a first-order system.

(b) Settling accuracy versus settling time.

Figure 2.7: Settling behaviour of a first-order system

2.4 Two-Stage Op Amps

The two-stage op amp is a very popular approach for realizing high gain amplifiers. This classic architecture is found in many state-of-the-art analog and mixed-signal circuits [13–16]. Fig. 2.8 shows the block diagram and a simple transistor realization of the two-stage op amp. Aside from increasing the DC gain, the two-stage architecture also allows more flexibility in the op amp design. In most two-stage op amps, the second stage is designed to provide high output swing in order to maximize the signal-to-noise ratio. The output swing of the first stage can then be reduced without adversely affecting the system's noise performance. This makes it feasible for designers to use vertical-gain enhancement, or cascoding, in their designs, as long as there is adequate voltage headroom for the transistors to remain in saturation.



(a) Block Diagram. (b) Transistor Implementation.

Figure 2.8: Block diagram and simple transistor implementation of a single-stage op amp.

The low-to-medium frequency small-signal model of the two-stage op amp is shown in Fig. 2.9. The transfer function of the circuit, neglecting the gate-to-drain capacitance C_{gd} of M2, is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = A(s) = \frac{g_{m_1} r_{o_1} g_{m_2} r_{o_2}}{(1 + s r_{o_1} C_1)(1 + s r_{o_2} C_L)} \tag{2.23}$$

where C_1 is the capacitance at the output of the first stage and C_L is the output load capacitance. The DC gain of the op amp is

$$A_0 = g_{m_1} r_{o_1} g_{m_2} r_{o_2} \tag{2.24}$$

The two poles of the op amp are located at

$$\omega_{p_1} = \frac{1}{r_{o_1} C_1} \tag{2.25}$$

$$\omega_{p_2} = \frac{1}{r_{o_2} C_L} \tag{2.26}$$

Assuming $\omega_{p_1} < \omega_{p_2}$, the gain-bandwidth product is

$$\omega_{\text{T}} = \frac{g_{m_1} g_{m_2} r_{o_2}}{C_1} \tag{2.27}$$

which is a factor of $g_{m_2} r_{o_2}$ higher than that of the single-stage op amp.

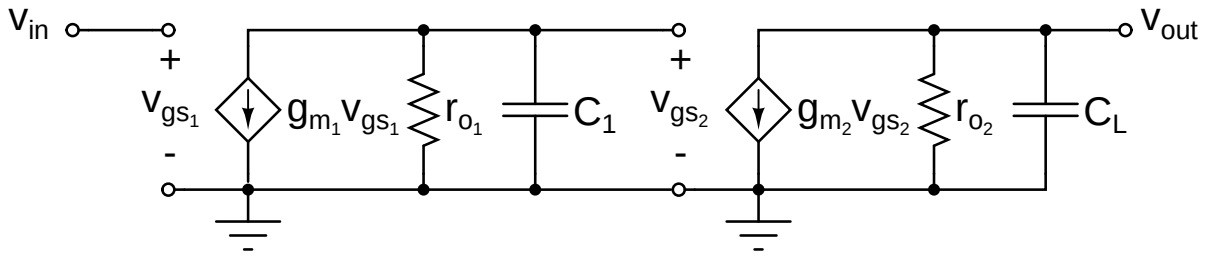


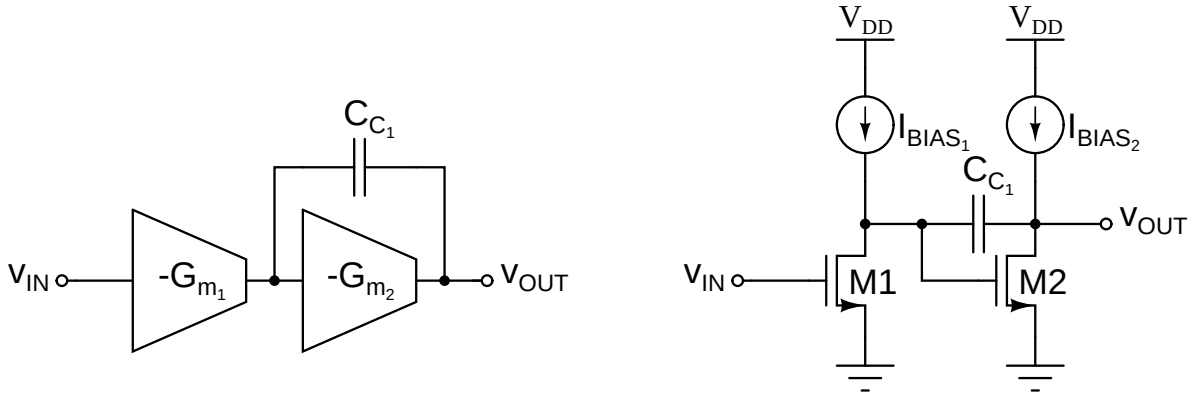
Figure 2.9: Small-signal model of a two-stage op amp.

The main drawback of the two-stage op amp is the decreased stability margin due to the presence of two dominant poles. The op amp should always be stable as there are only two poles in the circuit. However, the desire to maintain a phase margin greater or equal

to 45°, along with high-frequency parasitic poles and RHP (right-half plane) zeros, which were ignored in the above analysis, can degrade the loop gain's phase margin to below 0°. Stability can be improved with frequency compensation techniques but, as will be shown below, at the expense of a lower gain-bandwidth product.

2.4.1 Miller Compensation

A two-stage op amp can be stabilized using a variety of compensation techniques [10]. The most popular, and practical, approach is the Miller compensation technique. In this method, a compensation capacitor, C_{C_1}, is placed between the input and output of the second stage amplifier, as shown in Fig. 2.10. Stability is improved by exploiting the phenomenon of pole splitting [17]. Pole splitting has the effect of pushing one of the two dominant poles to a lower frequency and pushing the other dominant pole to a higher frequency.



(a) Block Diagram. (b) Transistor Implementation.

Figure 2.10: Block diagram and simple transistor implementation of a single-stage op amp.

The low-to-medium frequency small-signal model of the two-stage Miller-compensated

op amp is shown in Fig. 2.11. With the assumption that C_1 is negligible, the transfer function of the op amp is approximately

$$\frac{V_{\text{out}}}{V_{\text{in}}} = A(s) \approx \frac{g_{m_1} r_{o_1} g_{m_2} r_{o_2} \left(1 - s\frac{C_{C_1}}{g_{m_2}}\right)}{\left(1 + s r_{o_1} g_{m_2} r_{o_2} C_{C_1}\right)\left(1 + s\frac{C_L}{g_{m_2}}\right)} \tag{2.28}$$

The DC gain of Eq. 2.28 is exactly the same as that of Eq. 2.23. However, there is a significant change in the locations of the poles. When the compensation capacitor is introduced, the pole of the first amplifier stage, ω_{p_1}, is pushed down from $\frac{1}{r_{o_1} C_1}$ to $\frac{1}{r_{o_1} g_{m_2} r_{o_2} C_{C_1}}$ by the Miller effect [17]. Meanwhile, the pole of the second amplifier stage, ω_{p_2}, is pushed up from $\frac{1}{r_{o_2} C_L}$ to $\frac{g_{m_2}}{C_L}$. The compensation capacitor also introduces a right-half plane (RHP) zero located at $\omega_z = \frac{g_{m_2}}{C_{C_1}}$. The gain-bandwidth product of the op amp, as defined in Page 15, is

$$\omega_{\text{T}} = \frac{g_{m_1}}{C_{C_1}} \tag{2.29}$$

which is similar to the gain-bandwidth product of the single-stage op amp (Eq. 2.20).

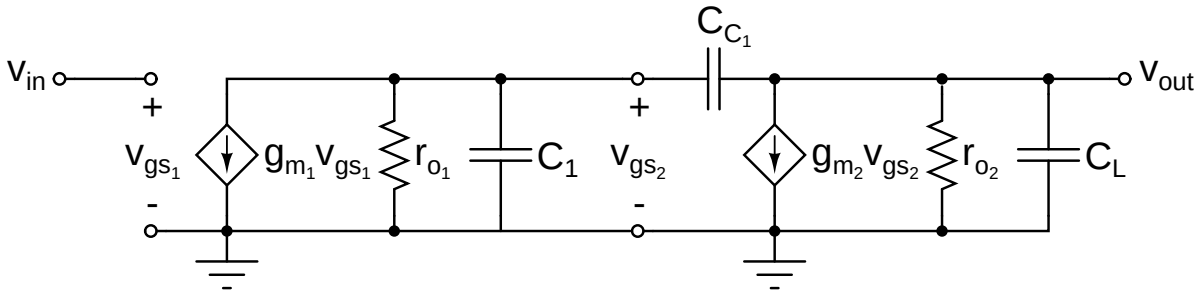


Figure 2.11: Small-signal model of a two-stage miller-compensated op amp.

To obtain a desired phase margin, the required separation between the second pole, ω_{p_2}, and the closed-loop bandwidth, $\beta\omega_{\text{T}}$, is given by [5]

$$\frac{\omega_{p_2}}{\beta\omega_{\text{T}}} = \frac{1}{\tan\left(90^\circ - \text{PM}\right)} \tag{2.30}$$

Eq. 2.30 highlights the most significant drawback to pole splitting. In order to obtain adequate stability margin, the closed-loop bandwidth must be lower than the second pole by a certain factor. Since the ω_{p_2} is near the same frequency as ω_{T} of the single-stage op amp (Eq. 2.20), the maximum achievable closed-loop bandwidth of the two-stage op amp will always be lower than that of the single-stage op amp with a first-order transfer function.

The settling time of a second-order system is difficult to compute and predict as it is highly dependent on both its gain-bandwidth product and its phase margin. As illustrated in Fig. 2.12, the settling time can vary significantly for second-order systems with the same gain-bandwidth product. The phase margin for optimum settling time is approximately given by [18]

$$\mathrm{PM}_{\mathrm{opt}} \approx 90^\circ - \tan^{-1}\left[\frac{1+\left(\frac{\pi}{\ln\epsilon}\right)^2}{4}\right] \tag{2.31}$$

In most applications, a phase margin between 70° to 76° will provide the shortest closed-loop settling time [5]. To meet this requirement, based on Eq. 2.30, ω_{p_2} should be placed 3 to 4 times higher than $\beta\omega_{\mathrm{T}}$. If ω_{p_2} is placed at the maximum possible frequency, then the gain-bandwidth product will have to be 3 to 4 times lower than the limits of a given technology. In contrast, the gain-bandwidth product of the single-stage op amp can always be set to the maximum possible frequency of the technology.

The previous analysis neglects the RHP zero in the op amp transfer function (Eq. 2.28). The zero can severely degrade the phase margin and should not be disregarded in the design process. Fortunately, various circuit techniques have been developed to deal with the effects of the Miller zero [19–22].

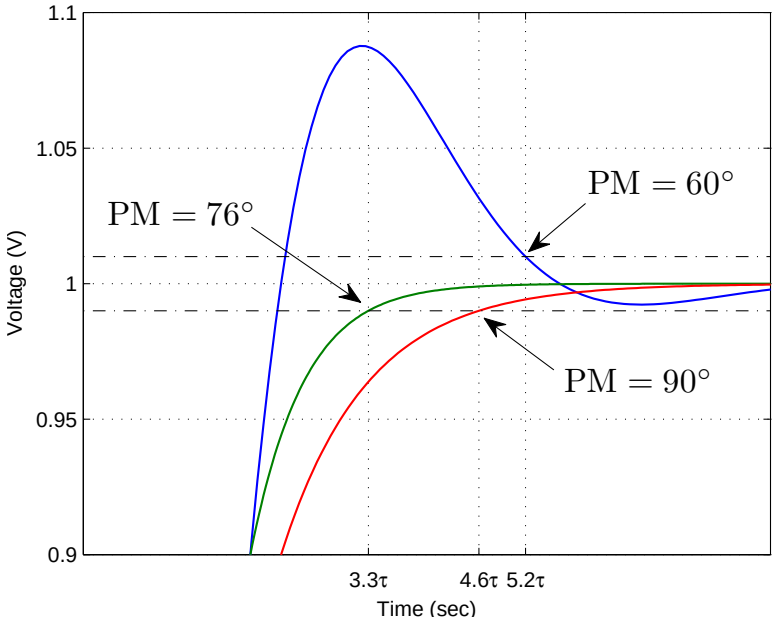


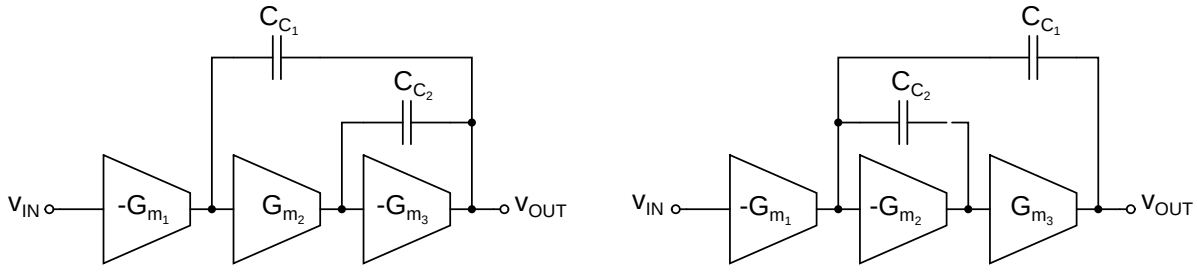
Figure 2.12: Settling behaviour of a second-order system. The error range is 1% ($\epsilon = 0.01$).

2.5 Multi-Stage Op Amps

In an advanced CMOS process where intrinsic transistor gain and supply voltage are low, it may be necessary to cascade three or more amplifier stages to meet a specified DC gain requirement. As with the two-stage op amp, stability is a major concern for multi-stage op amps. Techniques for stabilizing multi-stage op amps have been the focus of much research over the last decade. Multi-stage compensation techniques tend to fall into two categories: nested-Miller [23–31] and feedforward [32–34]. In the former, the op amp is stabilized by the means of pole splitting with Miller capacitors. In the latter, stability is achieved through pole-zero cancellation.

2.5.1 Nested-Miller Compensation

The pole-splitting principle behind two-stage Miller compensation can be extended to stabilize op amps of more than two horizontal gain stages. A popular multi-stage Miller compensation technique is the nested-Miller compensation (NMC) method. Fig. 2.13a describes a conventional third-order NMC op amp. Like two-stage Miller compensation, NMC aims to split the dominant poles so that one pole is pushed to a lower frequency while the others are pushed to higher frequencies. An obvious drawback with the conventional NMC topology is an increased capacitive load since all the Miller capacitors load the output. A larger output capacitance is undesirable since it degrades the op amp bandwidth. The reversed nested-Miller topology, shown in Fig. 2.13b, operates on the same pole-splitting principle as the NMC but provides bandwidth improvement since only the outer Miller capacitor loads the output [23, 30, 35].



(a) Nested-Miller Compensation.

(b) Reversed Nested-Miller Compensation.

Figure 2.13: Block diagrams of three-stage nested-miller compensated op amps.

Fig. 2.14 shows the low-to-medium frequency small-signal model of the three-stage NMC op amp in Fig. 2.13a. Assuming C_1 and C_2 are small so that they can be neglected,

the transfer function of the op amp can be approximated with [23, 24, 31, 36, 37]

$$\frac{V_{\text{out}}}{V_{\text{in}}} = A(s) \approx \frac{g_{m_1} r_{o_1} g_{m_2} r_{o_2} g_{m_3} r_{o_3} \left(1 - s\frac{C_{C_2}}{g_{m_3}} - s^2 \frac{C_{C_1} C_{C_2}}{g_{m_2} g_{m_3}}\right)}{(1 + s r_{o_1} g_{m_2} r_{o_2} g_{m_3} r_{o_3} C_{C_1}) \left(1 + s\frac{C_{C_2}}{g_{m_2}} + s^2 \frac{C_{C_2} C_L}{g_{m_2} g_{m_3}}\right)} \tag{2.32}$$

$$\approx \frac{\frac{g_{m_1}}{C_{C_1}} \left(1 - s\frac{C_{C_2}}{g_{m_3}} - s^2 \frac{C_{C_1} C_{C_2}}{g_{m_2} g_{m_3}}\right)}{s \left(1 + s\frac{C_{C_2}}{g_{m_2}} + s^2 \frac{C_{C_2} C_L}{g_{m_2} g_{m_3}}\right)} \tag{2.33}$$

The DC gain is

$$A_0 = -g_{m_1} r_{o_1} g_{m_2} r_{o_2} g_{m_3} r_{o_3} \tag{2.34}$$

which is higher than the DC gain of the single- and two-stage op amp. The poles and zeros of the op amp are located at

$$\omega_{p_1} = \frac{1}{r_{o_1} g_{m_2} r_{o_2} g_{m_3} r_{o_3} C_{C_1}} \tag{2.35}$$

$$\omega_{p_2} \approx \frac{g_{m_2}}{C_{C_2}} \tag{2.36}$$

$$\omega_{p_3} \approx \frac{g_{m_3}}{C_L} \tag{2.37}$$

$$\omega_{z_1} \approx -\frac{g_{m_3}}{C_{C_2}} \tag{2.38}$$

$$\omega_{z_2} \approx \frac{g_{m_2}}{C_{C_1}} \tag{2.39}$$

It is important to note that the first zero (ω_{z_1}) is a RHP zero and the second zero (ω_{z_2}) is a LHP zero. The gain-bandwidth product of Eq. 2.33 is

$$\omega_{\text{T}} = \frac{g_{m_1}}{C_{C_1}} \tag{2.40}$$

which is the same as Eq. 2.29.

According to current literature, there is no simple design procedure for obtaining optimum settling response for multi-stage op amps [38–40]. The most common design approach

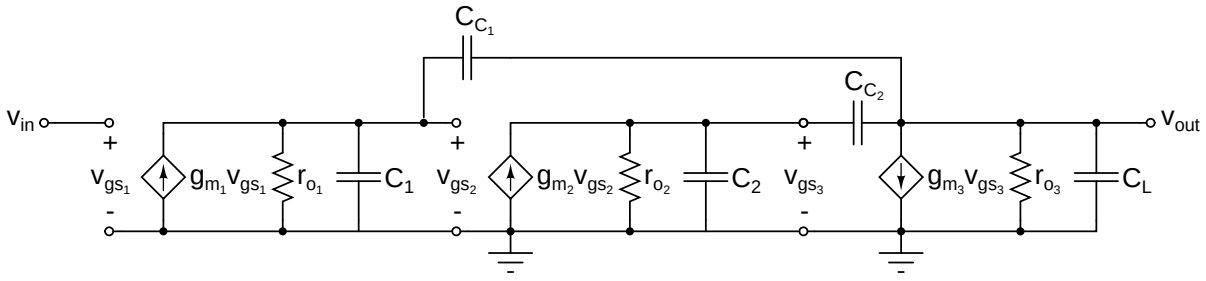


Figure 2.14: Small-signal model of a three-stage nested miller-compensated op amp.

is to aim for a closed-loop frequency response that is maximally flat (i.e. a Butterworth filter). For a three-stage op amp, the closed-loop unity-gain transfer function should be

$$A_{\mathrm{CL}}(s) = \frac{A(s)}{1 + A(s)} = \frac{1}{\left(1 + s\frac{2}{\omega_0} + s^2\frac{2}{\omega_0^2} + s^3\frac{1}{\omega_0^3}\right)} \tag{2.41}$$

where $A_{\mathrm{CL}(s)}$ and $A(s)$ are the transfer functions of the closed-loop amplifier and the op amp, respectively. From Eq. 2.41, the desired op amp transfer function is

$$A(s) = \frac{A_{\mathrm{CL}}(s)}{1 - A_{\mathrm{CL}}(s)} = \frac{\frac{\omega_0}{2}}{s\left(1 + s\frac{1}{\omega_0} + s^2\frac{1}{2\omega_0}\right)} \tag{2.42}$$

Comparing the coefficients of Eq. 2.33 without the zeros, with Eq. 2.42 yields the following pair of design equations:

$$\beta\omega_{\mathrm{T}} = \frac{1}{4}\frac{g_{m3}}{C_L} \tag{2.43}$$

$$\frac{g_{m2}}{C_{C_1}} = \frac{1}{2}\frac{g_{m3}}{C_L} \tag{2.44}$$

Compared with Eq. 2.20, the maximum $\beta\omega_{\mathrm{T}}$ will be a factor of 4 lower than that of the single-stage op amp. The step response of Eq. 2.41 is shown in Fig. 2.15. From the figure, it is evident by the transient overshoot that the settling response is not optimum for $\epsilon < 0.08$. To obtain near-optimum settling time where $\epsilon < 0.01$, the separation between $\beta\omega_{\mathrm{T}}$ and $\frac{g_{m3}}{C_L}$ can be tuned numerically but their ratio must be greater than 4.

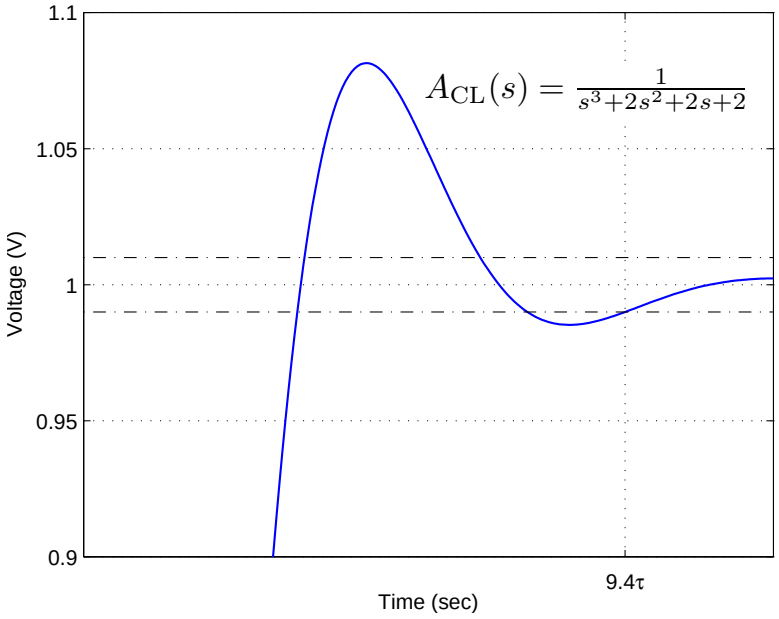


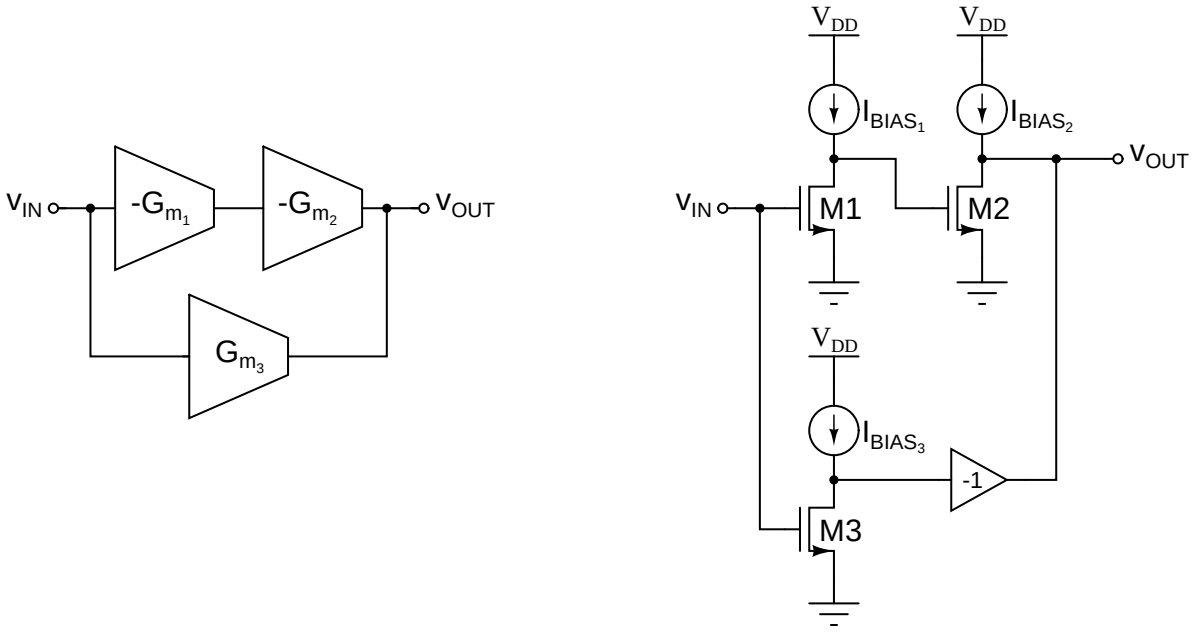
Figure 2.15: Settling behaviour of a third-order low-pass butterworth filter. $\omega_0 = 1$ rad/s and $\epsilon = 0.01$.

The previous analysis neglected the two zeros in Eq. 2.32. Since only one of the zeros is in the RHP, the overall effect of the zeros on stability is small [31]. However, the presence of Miller zeros cannot be discounted in higher-order amplifiers as they can degrade the stability margin [26, 28]. A number of nested-Miller topologies have been published in literature to offset the effects of the zeros [25–31], most of which are based on the principles referenced in Section 2.4.1.

2.5.2 Feedforward Compensation

Feedforward compensation aims to improve amplifier stability by introducing feedforward gain stages. A two-stage feedforward-compensated op amp is depicted in Fig. 2.16. This compensation topology creates left-half plane zeros that can be used to offset the negative

phase shift from the dominant poles [32–34]. More specifically, the zeros can be placed so that they cancel out all but one of the dominant poles. After pole-zero cancellation, the multi-stage op amp should have the same frequency and transient response as that of a single-stage op amp. Feedforward compensation has two distinct advantages over Miller compensation. Firstly, feedforward op amps do not suffer from the gain-bandwidth product limitations that are inherent with the Miller compensation architecture. Secondly, these amplifiers can be implemented in less area as they do not require compensation capacitors.



(a) Block Diagram.

(b) Conceptual Transistor Implementation.

Figure 2.16: Block diagram and simple transistor implementation of two-stage feedforward op amp.

Fig. 2.17 shows the low-to-medium-frequency small-signal model of the two-stage feedforward-

compensated op amp in Fig. 2.16. The op amp transfer function is

$$\begin{aligned}\frac{V_{\text{out}}}{V_{\text{in}}} = A(s) &= \frac{(g_{m_1} r_{o_1} g_{m_2} r_{o_2} + g_{m_3} r_{o_2}) \left(1 + s\frac{g_{m_3} C_1}{g_{m_1} g_{m_2}}\right)}{(1 + s r_{o_1} C_1)(1 + s r_{o_2} C_L)} \\ &\approx \frac{g_{m_1} r_{o_1} g_{m_2} r_{o_2} \left(1 + s\frac{g_{m_3} C_1}{g_{m_1} g_{m_2}}\right)}{(1 + s r_{o_1} C_1)(1 + s r_{o_2} C_L)} \end{aligned} \tag{2.45}$$

the DC gain is

$$A_0 = g_{m_1} r_{o_1} g_{m_2} r_{o_2} \tag{2.46}$$

Assuming $r_{o_1} C_1 > r_{o_2} C_L$, the gain-bandwidth product is

$$\omega_{\text{T}} = \frac{g_{m_1} g_{m_2} r_{o_2}}{C_1} \tag{2.47}$$

The above two parameters are virtually identical to that of the two-stage op amp (Eq. 2.24 and Eq. 2.27). The open-loop poles and zeros of the op amp are located at

$$\omega_{p_1} = \frac{1}{r_{o_1} C_1} \tag{2.48}$$

$$\omega_{p_2} \approx \frac{1}{r_{o_2} C_L} \tag{2.49}$$

$$\omega_z \approx \frac{g_{m_1} g_{m_2}}{g_{m_3} C_1} \tag{2.50}$$

To obtain an open-loop single-pole response for the op amp, the frequency of the left-half plane zero, ω_z, should match the frequency of the second pole, ω_{p_2}. This means that

$$\frac{g_{m_1} g_{m_2}}{g_{m_3} C_1} = \frac{1}{r_{o_2} C_L} \tag{2.51}$$

Thus, the transconductance of the feedforward stage should be

$$g_{m_3} = \frac{g_{m_1} g_{m_2} r_{o_2} C_L}{C_1} = k g_{m_1} \tag{2.52}$$

where k is the transconductance ratio between G_{m_3} and G_{m_1} in Fig. 2.16a. With proper pole-zero cancellation, the two-stage op amp has only one dominant pole and it can be modelled simply as a one-stage op amp. This method can then be repeated to realize an n-stage op amp, as is shown in Fig. 2.18.

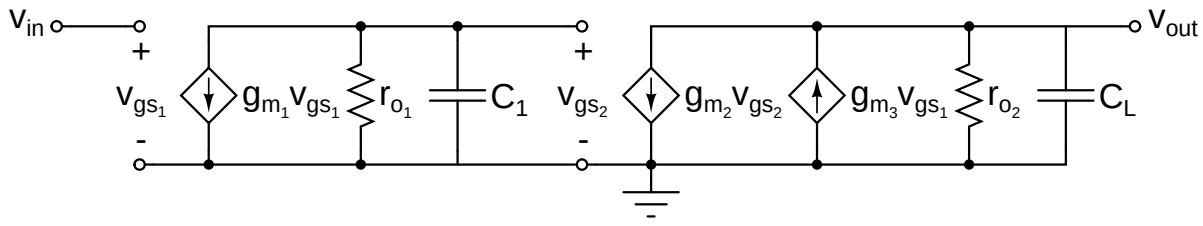


Figure 2.17: Small-signal model of a two-stage feedforward-compensated op amp.

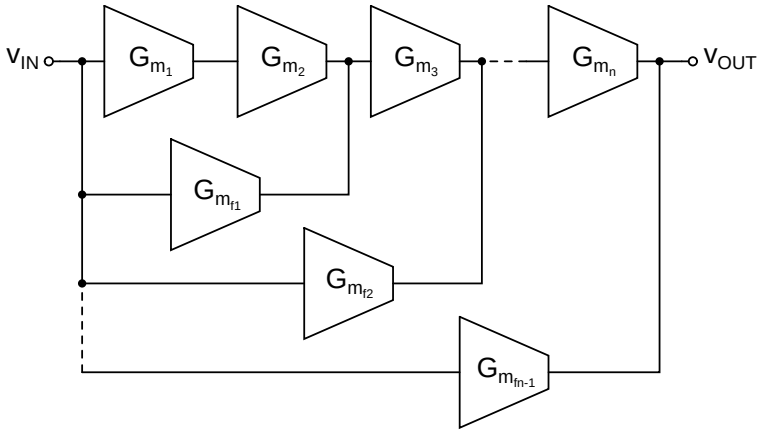


Figure 2.18: Block diagram of a n-stage feedforward op amp.

There are two major drawbacks to open-loop pole-zero cancellation. Firstly, the technique scales poorly since the factor k in Eq. 2.52 increases exponentially with each additional stage in the op amp. In multi-stage op amps, the transconductance ratio between G_{m_3} and G_{m_1} can be several orders of magnitude. This makes implementing higher-order op amps highly impractical. Secondly, the op amp is highly sensitive to PVT variations

since the location of the zero is dependent on the value of the parasitic capacitor C_1. Inexact pole-zero cancellation leads to pole-zero doublets that may degrade the settling time [41]. Pole-zero doublets are not a problem for continuous-time circuits, but may lead to long start-up transients and increased susceptibility to coupling of clock signals if the pole-zero spacing is left unregulated.

An alternative method for obtaining a single-pole response is to perform pole-zero cancellation after the op amp is placed in feedback [34]. If the condition

$$\frac{4\beta C_L g_{m_1} g_{m_2}}{C_1 \left(\beta g_{m_3} + 1/r_{o_2}\right)^2} = \frac{4\beta k}{r_{o_2} \left(\beta g_{m_3} + 1/r_{o_2}\right)^2} < 0.5 \tag{2.53}$$

is satisfied, then the approximate locations of the closed-loop poles and zero are

$$\omega_{\mathrm{p}_1} \approx \frac{\beta g_{m_1} g_{m_2}}{C_1 \left(\beta g_{m_3} + 1/r_{o_2}\right)} \tag{2.54}$$

$$\omega_{\mathrm{p}_2} \approx \frac{\beta g_{m_3} + 1/r_{o_2}}{C_L} \tag{2.55}$$

$$\omega_{\mathrm{z}} \approx \frac{g_{m_1} g_{m_2}}{g_{m_3} C_1} \tag{2.56}$$

which means that the zero will always be in proximity of the first closed-loop pole. Unlike open-loop pole-zero cancellation, this scheme is insensitive to PVT variations as both ω_{z} and ω_{p_1} have the same dependence on the parasitic capacitance. However, this scheme still requires a high transconductance ratio between G_{m_1} and G_{m_3}. In [34], a two-stage feedforward-compensated op amp was implemented using closed-loop pole-zero cancellation where the transconductance ratio between A_{v_3} and A_{v_1} was over three orders of magnitude. Another drawback with this scheme is the complex design procedure since the closed-loop poles and zeros must be determined. For higher order op amps, the increased design complexity makes this compensation scheme very unattractive.

2.6 Discussion

Vertical and horizontal gain-enhancement are two techniques for improving op amp gain. Vertical gain-enhancement improves gain by increasing the output resistance of the op amp. This technique does not affect the op amp's gain-bandwidth product since ω_T is not a function of the output resistance (Eq. 2.20). On the other hand, horizontal gain-enhancement improves gain by increasing the effective transconductance of the op amp. As was observed in Section 2.4, this has the effect of increasing both the gain and gain-bandwidth product. While it is possible to increase the op amp ω_T beyond the limits of a technology, such an op amp cannot have a first-order frequency response. Because of stability and settling time considerations, the ω_T of horizontal gain-enhanced op amps should not exceed the maximum ω_T of the technology.

Chapter 3

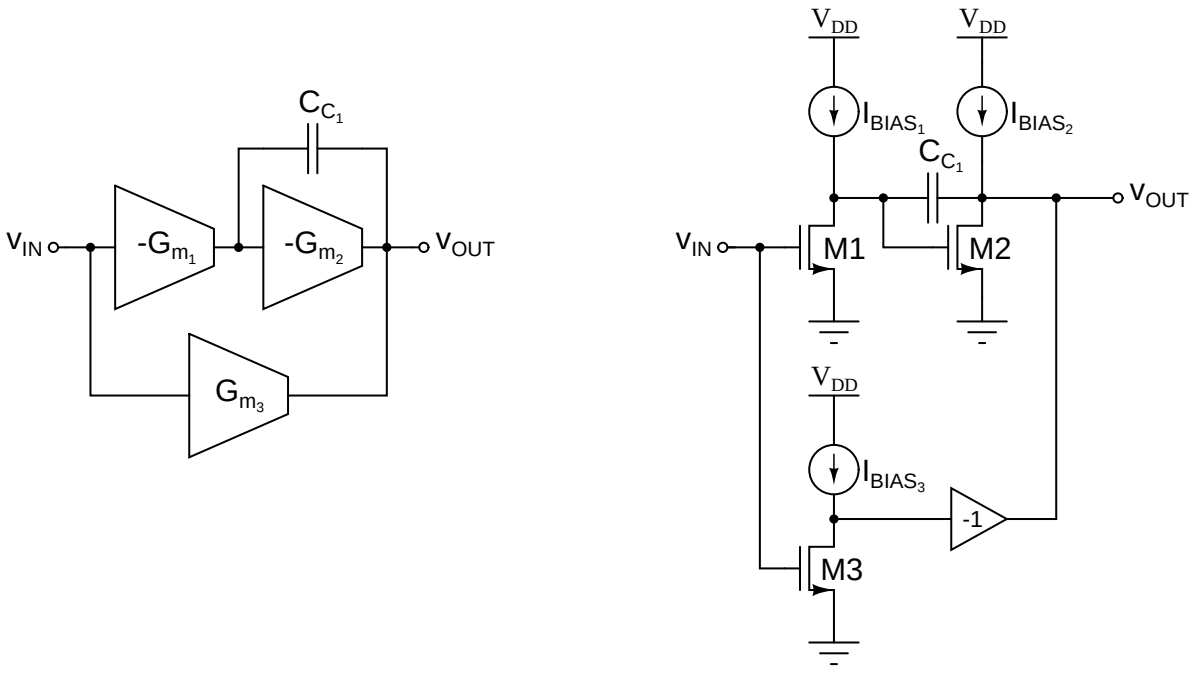
Multipath Miller Compensation

The two techniques for stabilizing multi-stage op amps – nested-miller and feedforward compensation – both have inherent disadvantages. The disadvantage of nested-Miller compensation lies with the non-dominant poles that limit the op amp's gain-bandwidth product. The disadvantage of feedforward compensation lies with the PVT-sensitive zero location and the impractically high transconductance required of the feedforward gain stage.

This chapter discusses the operation of op amps that incorporate both compensation capacitors and feedforward gain stages, which can overcome the limitations of nested-miller and feedforward compensation. Section 3.1 explains the operation of two-stage op amps with a multipath Miller compensation topology. Section 3.2 explores multi-stage implementations of the topologies. Section 3.3 proposes a transistor implementation of a two-stage op amp with this compensation technique.

3.1 Two-Stage Op-Amp

Compensation capacitors can be combined with feedforward gain stages to form a hybrid compensation topology. Fig. 3.1 depicts a two-stage op amp incorporating this compensation technique. In the past, this topology has been used to offset the effects of RHP zeros in miller- and nested-miller compensated op amps [23–25, 36]. By varying the transconductance of the feedforward path, it is possible to create LHP zeros that can be used, in the same fashion as feedforward compensation, to cancel the non-dominant poles of a multi-stage op amp [23, 37].



(a) Block Diagram.

(b) Transistor Implementation.

Figure 3.1: Block diagram and simple transistor implementation of two-stage miller with feedforward-compensated op amp.

The low-to-medium frequency small-signal model of the compensation topology is shown in Fig. 3.2. Assuming C_1 is negligibility small, the transfer function of the op amp is approximately

$$\frac{V_{\text{out}}}{V_{\text{in}}} = A(s) \approx \frac{g_{m_1} r_{o_1} g_{m_2} r_{o_2} \left(1 - s\frac{C_{C_1}\left(g_{m_1} - g_{m_3}\right)}{g_{m_1} g_{m_2}}\right)}{\left(1 + s r_{o_1} g_{m_2} r_{o_2} C_{C_1}\right)\left(1 + s\frac{C_L}{g_{m_2}}\right)} \tag{3.1}$$

The DC gain and gain-bandwidth product of the transfer function are identical to those of the two-stage Miller-compensated op amp. The DC gain is

$$A_0 = g_{m_1} r_{o_1} g_{m_2} r_{o_2} \tag{3.2}$$

and the gain-bandwidth is

$$\omega_{\text{T}} = \frac{g_{m_1}}{C_{C_1}} \tag{3.3}$$

The poles the op amp are located at

$$\omega_{p_1} = \frac{1}{r_{o_1} g_{m_2} r_{o_2} C_{C_1}} \tag{3.4}$$

$$\omega_{p_2} \approx \frac{g_{m_2}}{C_L} \tag{3.5}$$

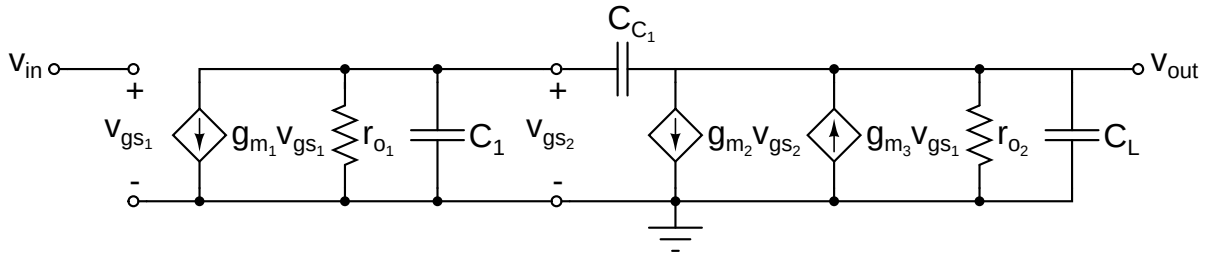


Figure 3.2: Small-signal model of a two-stage miller with feedforward-compensated op amp.

The frequency of the zero in Eq. 3.1 is at

$$\omega_{\mathrm{z}} = \frac{g_{m1}g_{m2}}{C_{C_1}\left(g_{m_1} - g_{m_2}\right)} = \frac{g_{m2}}{C_{C_1}\left(\frac{g_{m_3}}{g_{m_1}} - 1\right)} = \frac{g_{m2}}{C_{C_1}\left(k-1\right)} \tag{3.6}$$

where k is the transconductance ratio between A_{v_3} and A_{v_1}. By setting $g_{m_3} = g_{m_1}$ $(k = 1)$, the RHP zero can be eliminated. Since the transconductance of A_{v_1} and A_{v_3} can be matched very accurately in integrated circuits, this is an effective method for offsetting the effects of Miller zeros. More interestingly, by setting $g_{m_3} > g_{m_1}$ $(k > 1)$, the RHP zero can turned into a LHP zero for the purpose of pole-zero cancellation. To cancel the non-dominant pole, ω_{p_2}, with ω_{z}, the transconductance of the feedforward stage should be

$$g_{m_3} = \left(\frac{C_L}{C_{C_1}} + 1\right) g_{m_1} = k_1 g_{m_1} \tag{3.7}$$

Unlike the conventional feedforward compensation technique, the zero from this compensation scheme depends only on parameters that are insensitive to PVT variations. As mentioned previously, the transconductance of gain stages can be matched very accurately. The capacitance of the compensation and load capacitor can also be matched very accurately (on the order of 0.1%) by using MIM (metal-insulator-metal) or MOM (metal-oxide-metal) capacitors, which are commonly available as a technology add-on in advanced CMOS processes [42–44]. Multi-stage op amps incorporating this compensation topology can operate significantly faster than op amps compensated with the conventional nested-miller technique since the gain-bandwidth product of the former is not limited by the frequencies of the non-dominant poles.

3.1.1 Miller Capacitor with Lead Compensation

The aforementioned multipath Miller compensation technique can be improved by combining it with other techniques that offset the effects of RHP Miller zeros. Fig. 3.3 illustrates

such an example. In this op amp, a resistor of value $R_C = \frac{1}{G_{m_2}}$ is placed in series with the compensation capacitor C_{C_1}. This resistor forms a lead compensator and has the effect of reducing the transconductance of A_{v_3} for pole-zero cancellation.

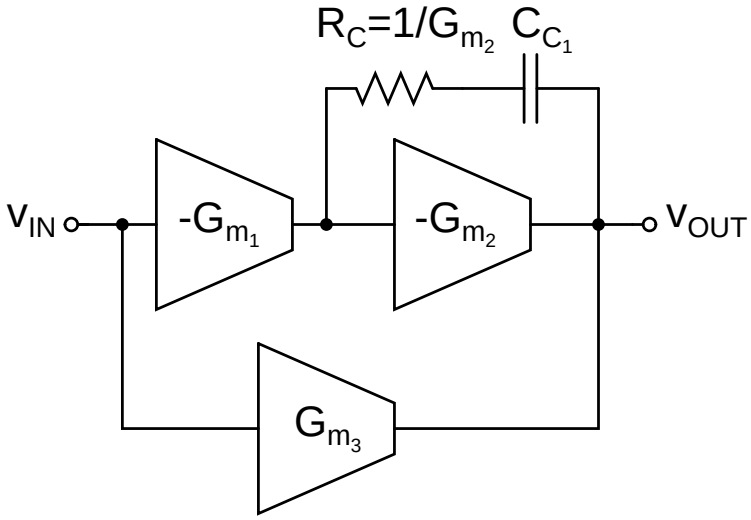


Figure 3.3: Block digram of a two-stage multipath Miller-compensated op amp with lead compensation.

The transfer function of the circuit in Fig. 3.3 is approximately

$$\frac{V_{\text{out}}}{V_{\text{in}}} = A(s) \approx \frac{g_{m_1} r_{o_1} g_{m_2} r_{o_2} \left(1 + s\frac{g_{m_3} C_{C_1}}{g_{m_1} g_{m_2}}\right)}{\left(1 + s r_{o_1} g_{m_2} r_{o_2} C_{C_1}\right)\left(1 + s\frac{C_L}{g_{m_2}}\right)} \tag{3.8}$$

The complete derivation of the above transfer function can be found in Appendix A. The DC gain, gain-bandwidth product, and poles of Eq. 3.8 are identical to those of Eq. 3.1. However, the location of the zero has shifted to

$$\omega_{\text{z}} = \frac{g_{m_2}}{C_{C_1}\frac{g_{m_3}}{g_{m_1}}} \tag{3.9}$$

A third LHP pole exists in the op amp at

$$\omega_{\text{p}_3} = \frac{1}{R_C C_1} \tag{3.10}$$

This pole was neglected in the above calculations as it is at a very high frequency relative to ω_{p_2}, assuming C_1 is much smaller than C_L.

The necessary feedforward transconductance for pole-zero cancellation is

$$g_{m_3} = \frac{C_L}{C_{C_1}} g_{m_1} = k_2 g_{m_1} \tag{3.11}$$

which is smaller than the necessary feedforward transconductance of the op amp without lead compensation (Eq. 3.7). The necessary feedforward transconductance for pole-zero cancellation can be further reduced by choosing a larger R_C. However, a larger R_C will lower ω_{p_3}, which may lead to a reduced stability margin and degraded settling response.

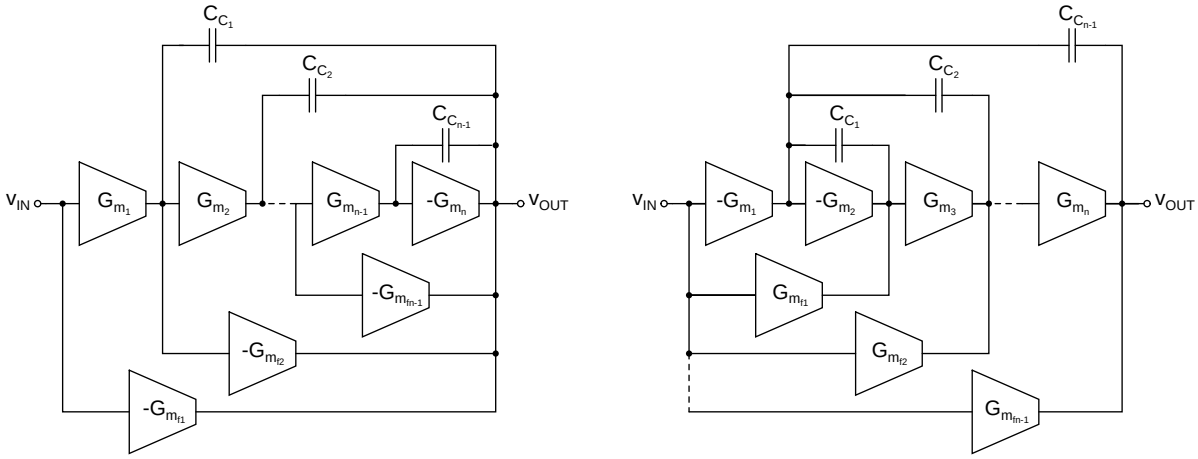
3.2 Multi-Stage Op-Amps

Fig. 3.4 depicts two possible multi-stage implementations of multipath Miller compensation.

The compensation topology in Fig. 3.4a is a direct extension of the two-stage multipath Miller compensation scheme shown in Fig. 3.1a. The advantage of this topology lies in its simple design procedure. It can be shown that the necessary transconductance of each feedforward amplifier for pole-zero cancellation is

$$g_{m_{fn}} = \left(\frac{C_L}{C_{C_n}} + 1 \right) g_{m_n} \tag{3.12}$$

which is the same as the design equation for the two-stage multpath Miller compensation scheme (Eq. 3.7). The main drawback to this topology is an increased capacitive load since all the Miller capacitors and the feedforward amplifier's output capacitors load the output. An increased load capacitance will not affect the op amp's gain-bandwidth product



(a) Conventional Nested Miller with Feedforward. (b) Reverse Nested Miller with Feedforward.

Figure 3.4: Block diagrams of multi-stage miller with feedforward compensated op amps.

($\omega_{\mathrm{T}} = \frac{g_{m1}}{C_{C_1}}$), but will require more current since the necessary feedforward transconductance for pole-zero cancellation is proportional to the load capacitance, C_L.

The compensation topology Fig. 3.4b operates on the same pole-zero cancellation principle as the reverse nested Miller with feedforward compensation scheme. The advantage of the reverse nested Miller with feedforward compensation topology is a lower capacitive load at the output, which makes this topology well suited for low-power applications. However, the design process is more complex since the locations of the feedforward zeros cannot be easily determined.

3.3 Proposed Design

Fig. 3.5 illustrates a possible transistor implementation of a two-stage multipath Miller compensated op amp with lead compensation in Fig. 3.3. Like most op amps in integrated

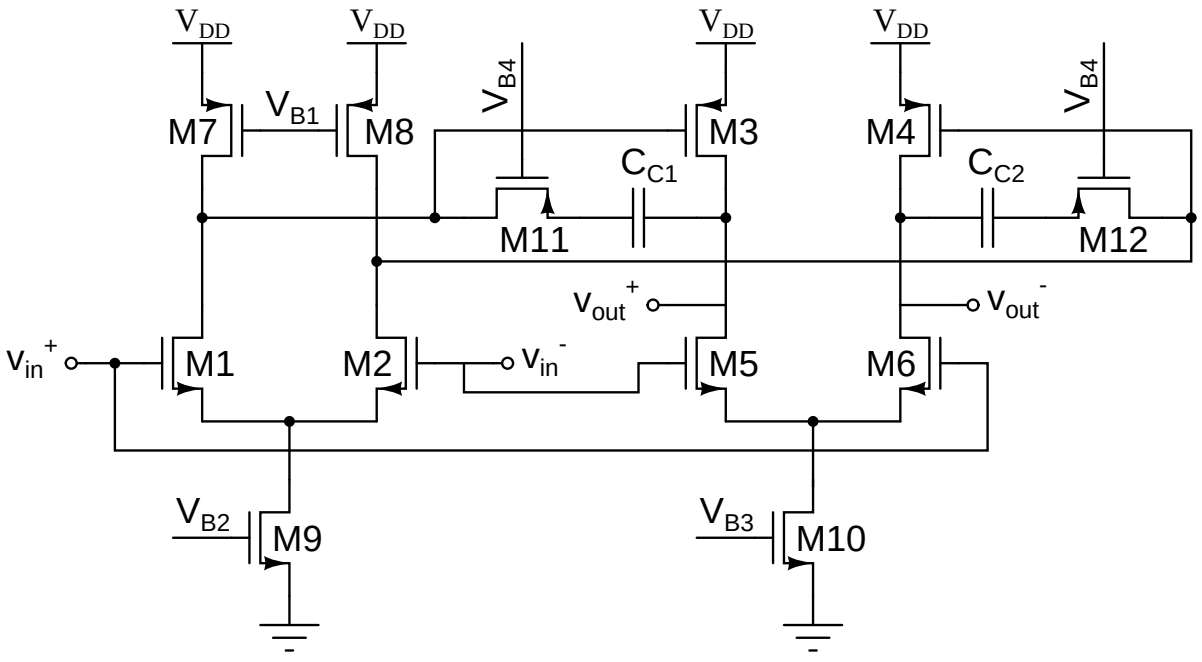


Figure 3.5: A transistor implementation of a two-stage miller and feedforward compensated op amp with lead compensation.

circuits, this op amp was made fully differential in order to take advantage of the benefits of differential signalling, such as improved tolerance to common-mode noise, removal of even-order harmonics, and increased output voltage range [45].

In Fig. 3.5, transistors M1 and M2 form the first transconductance stage G_{m_1}. Transistors M7 and M8 form the active load of G_{m_1}. The second transconductance stage, G_{m_2}, is implemented by transistors M3 and M4. In a conventional two-stage op amp, the output of G_{m_1} would be connected to the gates of M5 and M6 while M5 and M6 would be biased at a constant gate voltage so that they form the active loads of G_{m_2}. However, in this op amp, the gates of M5 and M6 are connected to the input so that they form the feedforward transconductance stage G_{m_3} while the output of G_{m_1} is connected to the gates

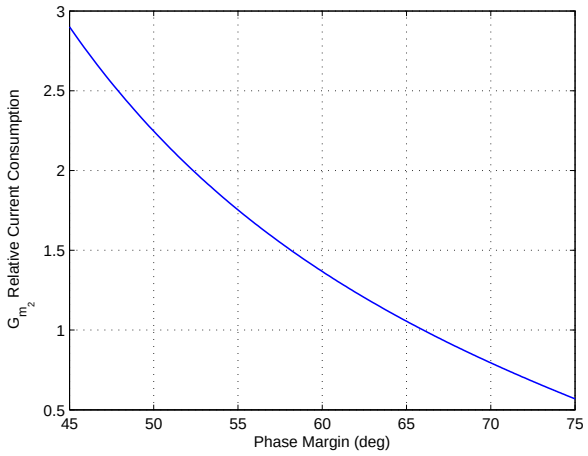
of M3 and M4. Combining the active load with the feedforward transconductance stage has a number of advantages over op amps where the two elements are implemented using separate transistors, as in Fig. 2.16b. Firstly, the addition of the feedforward amplifier will not increase the power consumption or area of the op amp. Secondly, the class-AB output increases op amp efficiency and output slew rate. Transistors M9 and M10 implement the tail current sources for G_{m_1} and G_{m_2}/G_{m_3}, respectively. These tail current sources are used to increase the common-mode rejection ratio (CMRR) of transistor pairs M1/M2 and M3/M4. Since transistors M3 and M4 are configured as a pseudo differential amplifier, they are very sensitive to common-mode disturbances at the output of G_{m_1}. This issue can be resolved by regulating the output common-mode of G_{m_1} with a common-mode feedback (CFMB) circuit. Transistors M11 and M12, biased in the linear region, implement the resistor R_C in Fig. 3.3. In integrated circuits, transistors biased in the linear region are often used instead of physical resistors as they can be biased such that their resistance will track the transconductance of G_{m_2} across process and temperature variations [5].

3.4 Comparison with Conventional Two-Stage Miller-Compensated Op Amps

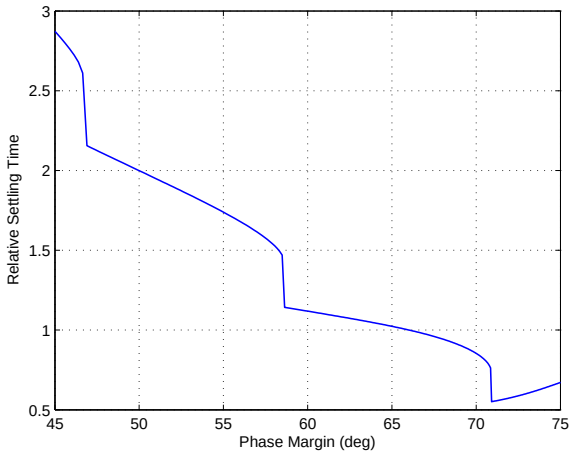
3.4.1 Settling Response

Based on the previous analysis, it was determined that two-stage multipath Miller-compensated op amps have the same DC gain and gain-bandwidth product equations as conventional two-stage Miller-compensated op amps for the same power consumption. However, the closed-loop settling responses of the two types of op amps can be quite different. For the same DC gain and gain-bandwidth product, two-stage multipath Miller-compensated

op amps have a constant linear settling time whereas conventional Miller-compensated op amps have a linear settling time that is a function of its phase margin. For moderate-to-low phase margins, the latter will need to consume more current in order to obtain the same linear settling time as the former. This is illustrated in Fig. 3.6a where for the same linear settling time, the second stage of a conventional two-stage Miller-compensated op amp with a 45° phase margin will need to consume almost three times as much current and area as that of a two-stage multipath Miller-compensated op amp. Fig. 3.6b shows that for the same power consumption, the settling time of the conventional two-stage Miller-compensated op amp is almost three times higher than the two-stage multipath Miller-compensated op amp.



(a) G_{m_2} Relative Current Consumption vs. Phase Margin.



(b) Relative Settling Time vs. Phase Margin.

Figure 3.6: Performance improvement as a function of phase margin. $A_0 = 80$ dB and $\epsilon = 0.01$ (1%).

Fig. 3.7 illustrates the power and settling time trade-off two-stage conventional Miller-compensated op amps. In the plot, it is assumed that at 45° phase margin, the power

consumption of the first and second op amp stage are identical. If the power consumption of the second stage is increased by a factor of 3, then the overall relative power consumption is increased by a factor of 2. The black dashed line in Fig. 3.7 indicates the relative power and settling time achievable with a two-stage multipath Miller-compensated op amp in which a feedforward path is added to a two-stage conventional Miller-compensated op amp with 45° phase margin.

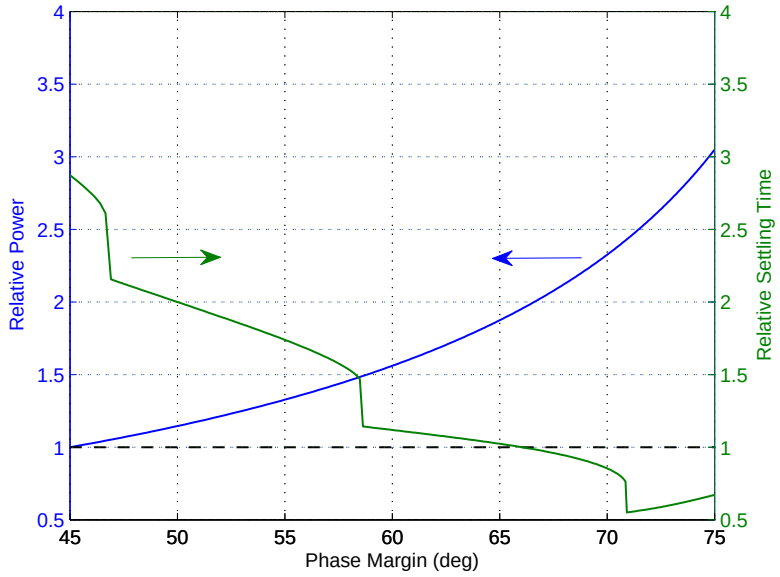


Figure 3.7: Power and settling time trade-off for two-stage conventional Miller-compensated op amps.

3.4.2 Noise

The total output noise of a two-stage conventional Miller-compensated op amp in feedback shown in Fig. 3.8 is

$$\overline{v_{\text{out}_{\text{tot}}}^2} = \frac{2kT\gamma\left(1+\frac{g_{m_7}}{g_{m_1}}\right)}{\beta C_{C_1}}\left(1+\frac{\beta C_{C_1}\left(1+\frac{g_{m_5}}{g_{m_3}}\right)}{(C_{C_1}+C_L)\left(1+\frac{g_{m_7}}{g_{m_1}}\right)}\right) \tag{3.13}$$

where k is the Boltzmann constant, T the is temperature in kelvin, and γ is the effective channel resistance, which is approximately 2/3.

The total output noise of a two-stage multipath Miller-compensated op amp in feedback shown in Fig. 3.9 is

$$\overline{v_{\text{out}_{\text{tot}}}^2} = \frac{2kT\gamma\left(1+\frac{g_{m_7}}{g_{m_1}}\right)\beta}{\beta C_{C_1}\left(1+\frac{\beta g_{m_5}}{g_{m_3}}\right)}\left(1+\frac{\beta C_{C_1}\left(1+\frac{g_{m_5}}{g_{m_3}}\right)}{(C_{C_1}+C_L)\left(1+\frac{g_{m_7}}{g_{m_1}}\right)}\right) \tag{3.14}$$

Eq. 3.14 and 3.13 assume that the transistors have infinite output resistance ($r_o = \infty$) and that the effects of the Miller capacitor is unilateral (i.e. the Miller zero is neglected). The complete derivation of the total output noise for the two op amps can be found in Appendix C.

The lower total input-referred noise for the multipath Miller-compensated op amp, by a factor of $1 + \beta g_{m_5}/g_{m_3}$, can be explained by observing the approximate input-referred noise spectral density plots of the two op amps, which are shown in Fig. 3.10 where the transistors are assumed to have finite output resistance. At low frequencies, the noise of the second stage for both op amps is attenuated by the gain of the first stage, A_1. Beyond the frequency ω_z, the gain of the first stage will decrease and hence the noise of the second stage will increase. For the conventional Miller-compensated op amp, the noise of the

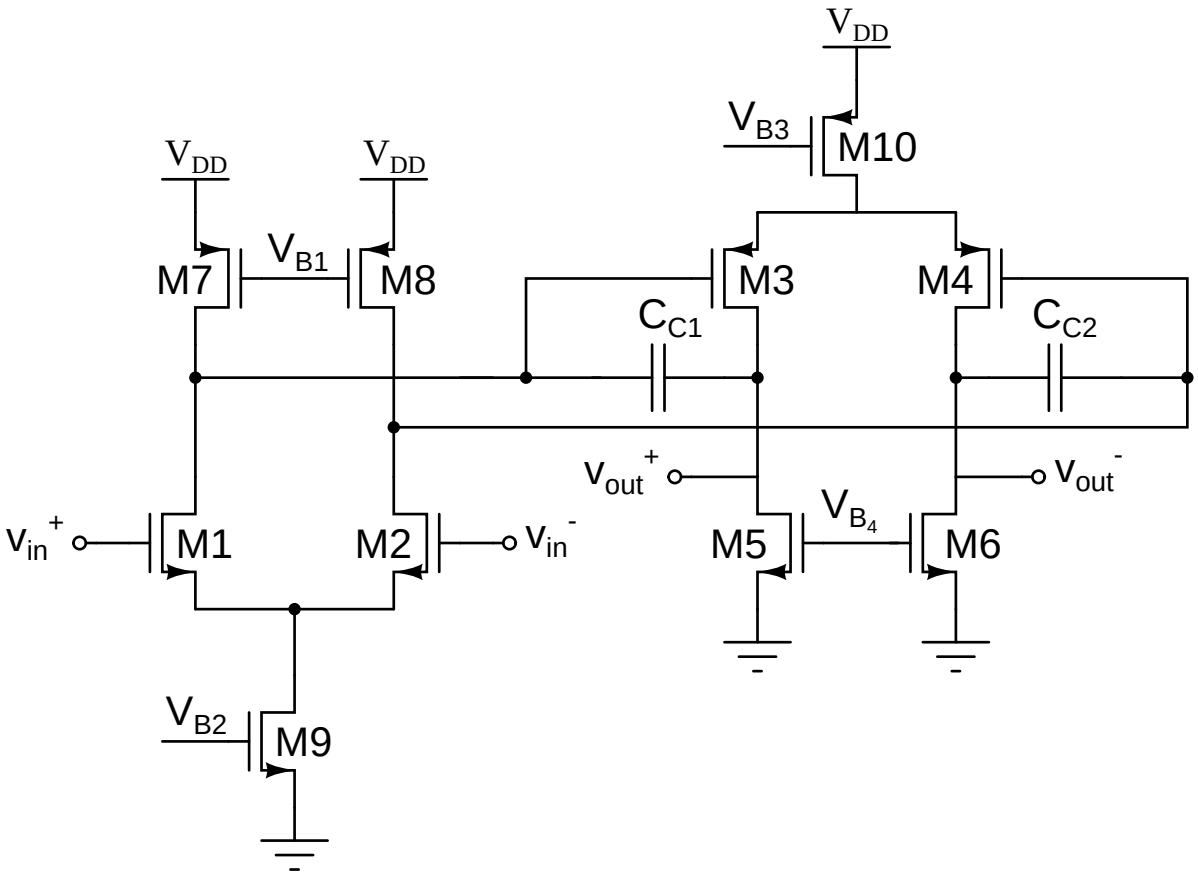


Figure 3.8: Circuit diagram of a two-stage conventional Miller-compensated op amp.

second stage will increase for all frequencies since the gain of the first stage collapses at high frequencies. It should be noted that the total input-referred noise itself is bounded because the noise bandwidth (NBW) is finite. For the multipath Miller-compensated op amp, the noise of the second stage will increase beyond the frequency ω_z but will flatten at the frequency ω_p because after ω_p, the noise is input-referred through the feedforward stage instead of the first op amp stage.

Noise simulations were performed on complete transistor implementations of a two-

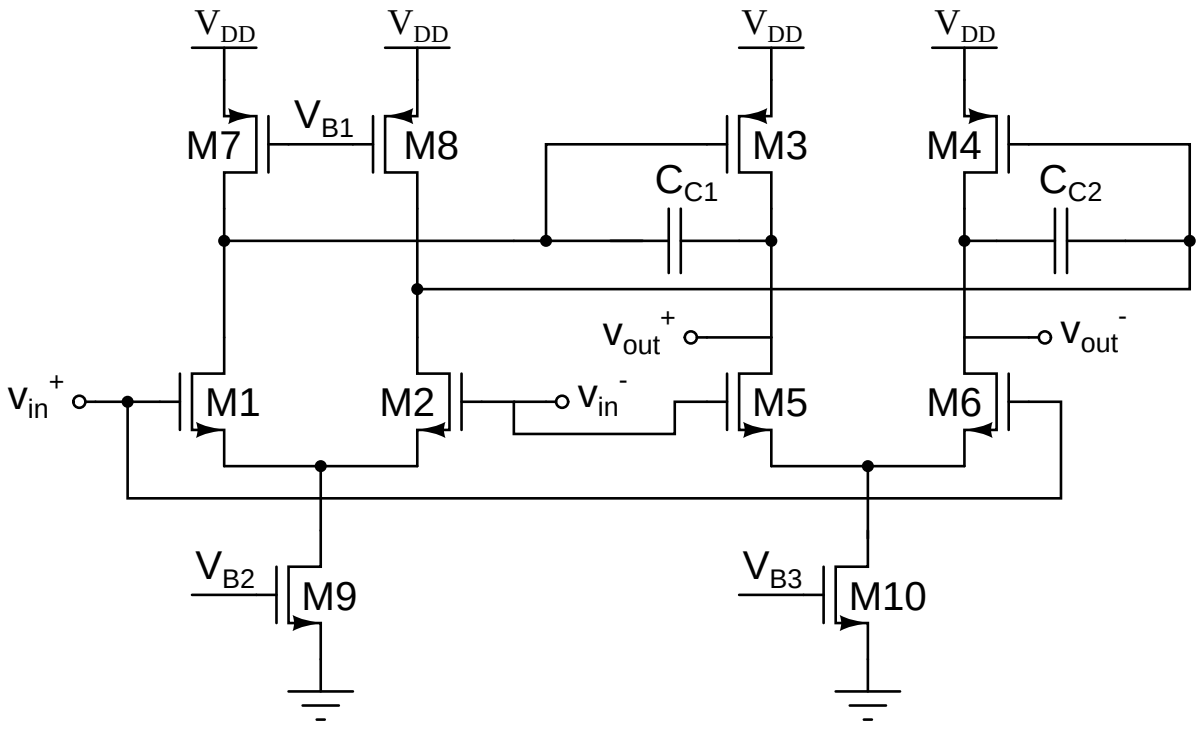
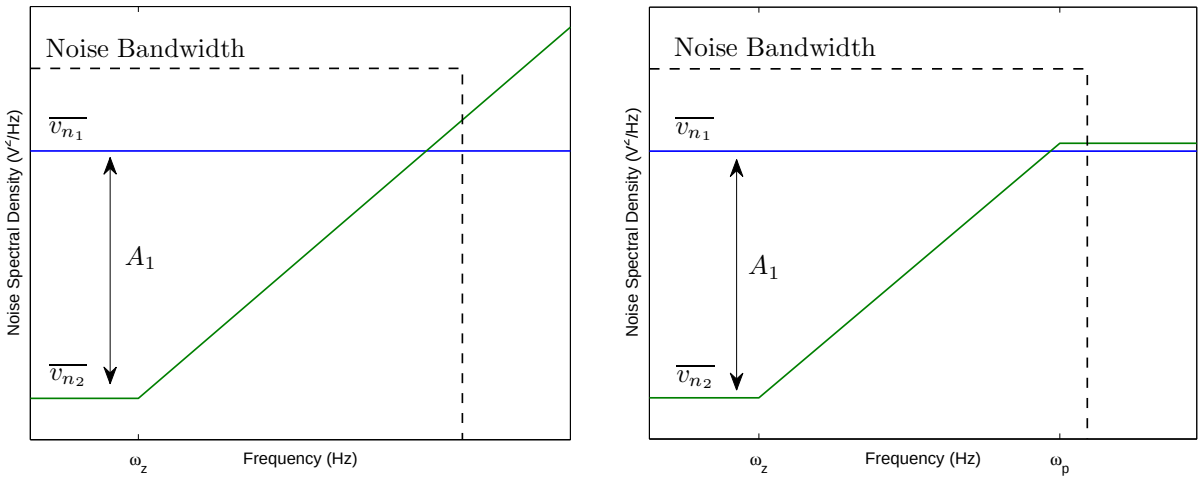


Figure 3.9: Circuit diagram of a two-stage multipath Miller-compensated op amp.

stage conventional and multipath Miller-compensated op amp and the results are plotted in Fig. 3.11. For the latter op amp, the ratio of $\beta g_{m_5}/g_{m_3}$ was determined to be 1.1. According to Eq. 3.13-3.14, the total output noise power of the multipath Miller-compensated op amp should be approximately half that of the conventional Miller-compensated op amp. The results of the noise simulations, shown in Fig. 3.11, agree with the above noise analysis.

3.4.3 Output Slew Rate

Fig.3.12 shows the output stage of a two-stage conventional Miller-compensated op amp when it is slewing. In this condition, one of the input transistors is turned off and all the



(a) Conventional Miller-compensated op amp.

(b) Multipath Miller-compensated op amp.

Figure 3.10: Approximate input-referred noise spectral density of two-stage op amps in feedback.

tail bias current flows through the other transistor. Since the load transistors will conduct a constant current of $I_B/2$ on both branches, the maximum differential output slew current is $I_B/2$.

Fig.3.13 shows the output stage of a two-stage multipath Miller-compensated op amp when it is slewing. In this condition, one of the input transistors is turned off and all the tail bias current flows through the other transistor. Furthermore, one of the *load* transistors is also turned off while the opposite *load* transistor will conduct a current of I_L, where $I_L \geq I_B/2$. The imbalance of currents flowing through the output will cause the common-mode feedback (CMFB) circuit to force the tail current I_B to be equal to I_L by adjusting the voltage V_{CMFB}. Hence, the maximum output slew rate is I_L. Since I_L can be more than an order of magnitude higher than $I_B/2$, the slew rate of a two-stage multipath Miller-compensated op amp should be much higher than that of a two-stage conventional

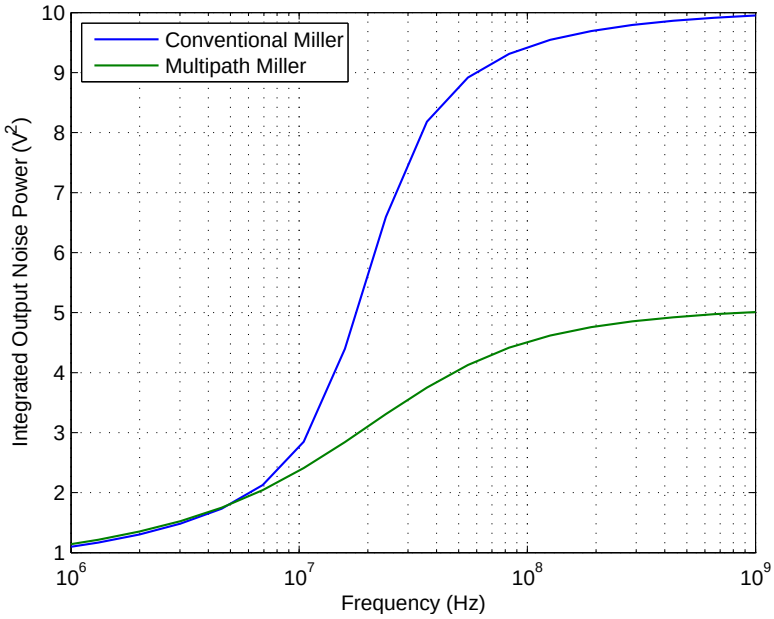


Figure 3.11: Simulated integrated output noise power of two two-stage op amps.

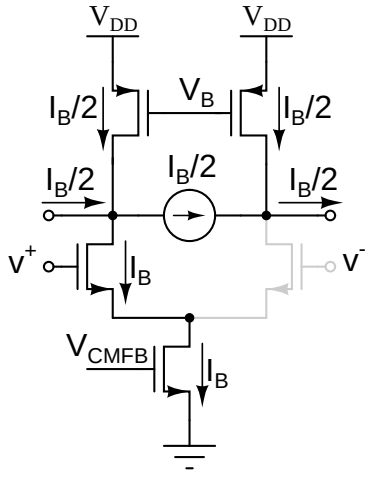


Figure 3.12: A two-stage conventional Miller-compensated op amp exhibiting slew-limited behaviour.

Miller-compensated op amp. The exact value of I_L depends on the bias conditions of the *load* transistors.

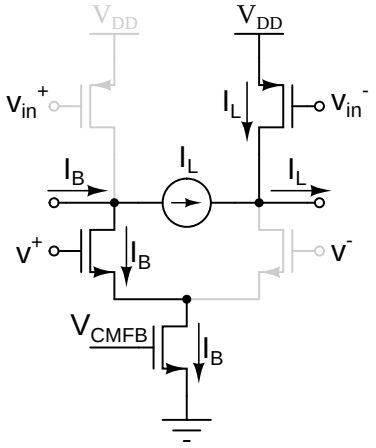


Figure 3.13: A two-stage multipath Miller-compensated op amp exhibiting slew-limited behaviour.

3.5 Summary

Multipath Miller-compensated op amps improve stability by introducing a feedforward path in the op amp topology. By tuning the transconductance of this feedforward path, it is possible to place LHP zeros to cancel out the effects of non-dominant poles in multi-stage op amps. Since the locations the LPH zeros and poles are set by ratios of transconductors and capacitors, this scheme is insensitive to PVT variations.

The proposed two-stage multipath Miller-compensated op amp architecture, as discussed in Section 3.3, can reduce power consumption and improve closed-loop settling time over two-stage conventional Miller-compensated op amps. The proposed multipath

op amp also has the benefits of reduced closed-loop input-referred noise and increased output slew rate. Finally, the proposed feedforward transconductance stage can be implemented without any power or area penalty.

Chapter 4

System-Level Design

This chapter explores a circuit that illustrates the benefits of multipath Miller-compensation over the conventional Miller-compensation topology. From the analysis in Section 2.4.1 and 3.1, it was determined that a multipath Miller compensation topology is superior to the conventional Miller topology in terms of stability margin, maximum achievable gain-bandwidth product, closed-loop settling time, and power. This work examines the differences in the settling behaviour of a two-stage multipath Miller and a two-stage conventional Miller compensated op amp with identical DC gain and gain-bandwidth product.

Multipath Miller compensation is only feasible when the load capacitance, C_L, is fixed and known beforehand. A settling-optimized conventional Miller compensated op amp also requires a fixed and known load capacitance since the location of the non-dominant pole (w_{p_2}), which determines the closed-loop settling behaviour (Fig. 2.12), depends on C_L. It is difficult to achieve first-order settling behaviour with multipath Miller compensated op amps designed for discrete circuit applications since packaging and fixture parasitic capacitance, which are not known prior to design, will shift the location of ω_{p_2} and reduce

the effectiveness of pole-zero cancellation. In most integrated circuit systems, however, the load capacitance is constant and known. This presents a suitable environment for implementing multipath Miller compensated op amps.

The performance of a number of systems, such as a 10-bit pipeline ADC or a $\Delta\Sigma$ modulator, are set by the performance of their op amps. While such systems can be built to illustrate the advantages of the proposed op amp topology, they are often very large and complex. The advantages of multipath Miller-compensation are explored through the design of a novel switched-capacitor sinusoidal oscillator where its output harmonics are determined primarily by the settling behaviour of its op amps. A switched-capacitor circuit consists of four basic building blocks: op amps, capacitors, switches, and non-overlapping clocks. Section 4.1 describes the operation and design process of the oscillator. Section 4.2 presents Matlab behavioural simulations of the system.

4.1 Switched-Capacitor Sinusoidal Oscillator Design

A switched-capacitor sinusoidal oscillator generates a stable sinusoidal tone that is a function of the clock frequency. Fig. 4.1 illustrates a possible method for generating a sinusoidal wave with only switched-capacitor circuits. In this circuit, a switched-capacitor resonator, tuned for a specific centre frequency, is connected to a comparator. Assuming the circuit is oscillating, the comparator generates a square wave of the same frequency as the output sinusoidal wave. The switched-capacitor resonator then filters out the harmonics of the square wave and thus maintains the output sinusoidal wave. The quality factor (Q) of the resonator should be sufficiently high (about 10) in order to suppress the tones of the input square wave. As will be demonstrated in this chapter, the harmonic distortion of the output sinusoidal wave is strongly affected by the settling behaviour of the op amps inside

the switched-capacitor resonator.

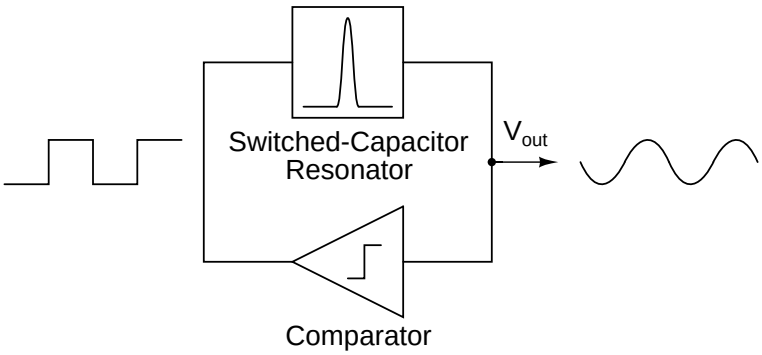


Figure 4.1: Conceptual diagram of a switched-capacitor sinusoidal oscillator.

This switched-capacitor system was chosen for comparing the settling behaviour between nested and conventional Miller compensated op amps for various reasons. Firstly, the system requires no input signals except for the clock, reference, and control signals thus simplifying the complexity of the test board and setup. Secondly, the system is free-running and does not need to be stabilized. Finally, the most important performance parameter, harmonic distortion, can be easily measured and characterized without requiring specialized testing equipment.

4.1.1 Architecture

An implementation of a switched-capacitor sinusoidal oscillator is shown in Fig. 4.2 [46]. Here, the switched-capacitor resonator is realized using a second-order damped biquad filter and a comparator. The biquad filter makes use of the well-known parasitic-insensitive inverting and non-inverting integrator configurations, which are shown in Fig. 4.3. Referring to Fig. 4.2, it should be noted that for the subsequent analysis, the integrator with

OA_1 is treated as an inverting integrator. The continuous-time comparator and DFF (d flip-flop) in Fig. 4.2 sample on ϕ_2 and generate signals x and $\overline{\text{x}}$, which set the input of the resonator to either $V_{\text{ref}+}$ or $V_{\text{ref}-}$. The node V_{x} is the band-pass output of the biquad whereas V_{out} is the low-pass output of the biquad. The low-pass output is chosen as the output of the oscillator because it exhibits less distortion [46]. However, the input to the comparator must be taken at node V_{x} since it is in-phase with V_{in} (V_{out} is shifted by $-\pi/2$). The output of the continuous-time comparator is connected to a DFF for the purpose of synchronizing the signals x and $\overline{\text{x}}$ with ϕ_2. This guarantees that the transients associated with switching V_{in} from $V_{\text{ref}+}$ to $V_{\text{ref}-}$, and vice versa, will have had sufficient time to settle before the end of ϕ_2. The continuous-time comparator and the DFF can be replaced with a latched comparator for better performance. Without a start-up circuit, the circuit in Fig. 4.2 may not oscillate when powered is applied. Section 4.1.5 describes the design of the start-up circuit for this type of switched-capacitor sinusoidal oscillators. The performance of the resonator, and hence that of the overall oscillator, is determined by the closed-loop settling response of its op amps.

Fig. 4.4 shows the signal flow graph of the resonator with ideal op amps (infinite gain and bandwidth) and capacitors $C_A = C_B = 1$. The transfer function for the signal flow graph is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = H_{\text{LP}}(z) = \frac{C_1 C_2}{z^2 + z\left(C_2 C_3 + C_2 C_4 - 2\right) + \left(1 - C_2 C_3\right)} \tag{4.1}$$

Switched-capacitor circuits are more sensitive to the effects of finite op amp bandwidth if the inputs to the op amps are not steps functions [47]. In the circuit in 4.2, it is clear that on ϕ_1, op amp OA_1 receives an input from OA_2 through C_4. Since both OA_1 and OA_2 receive their inputs during ϕ_1, the output of OA_2 will be be seen as an exponential ramp, not a step, at the input of OA_2. This problem can be resolved by interchanging the

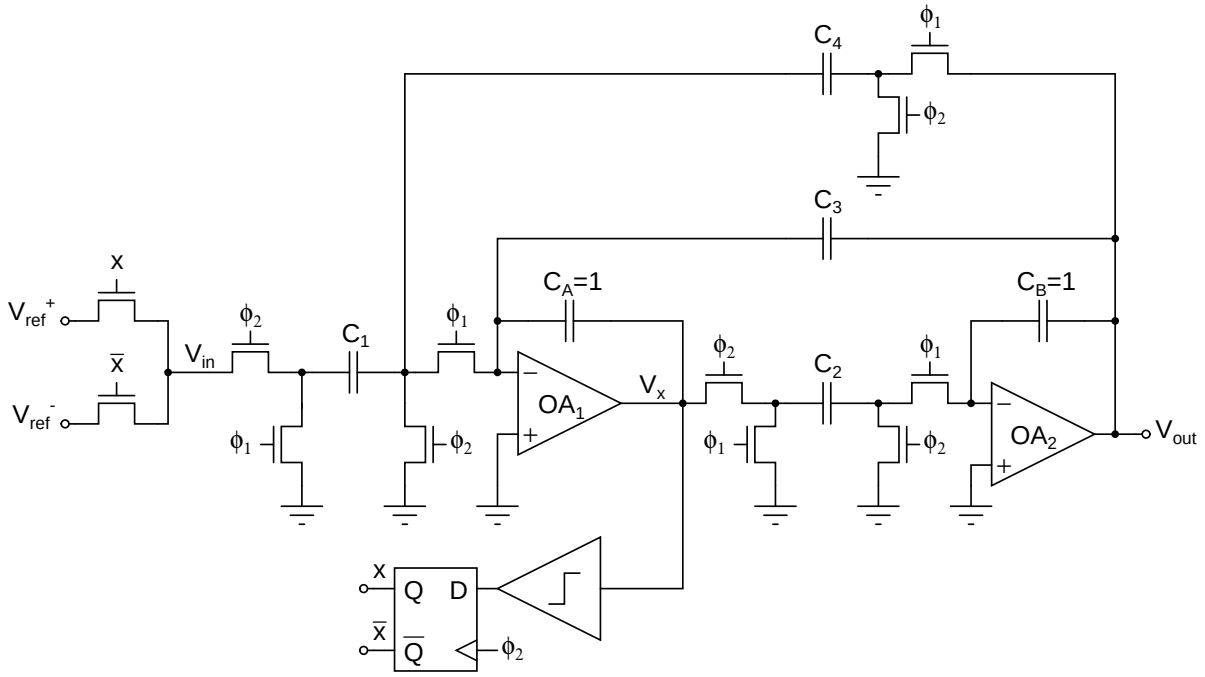
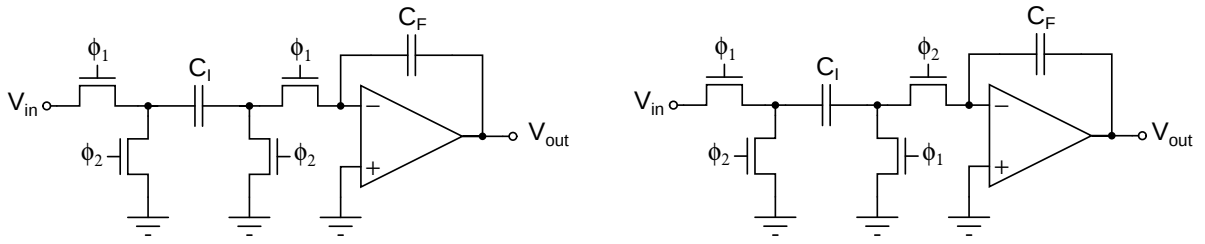


Figure 4.2: A switched-capacitor sinusoidal oscillator.



(a) Inverting integrator.

(b) Non-inverting integrator.

Figure 4.3: Two parasitic-insensitive switched-capacitor integrator configurations. Output is sampled at the end of ϕ_1.

sampling phases of OA_2 so that it receives its input on ϕ_2 instead of ϕ_1. Fig. 4.5 highlights the necessary changes to the circuit. The damping capacitor C_3 will always receive an

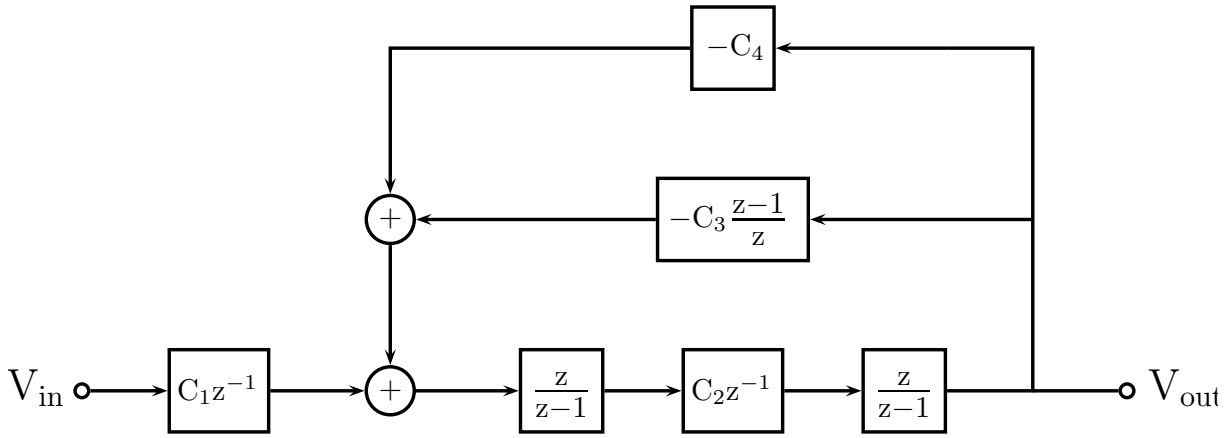


Figure 4.4: Signal flow graph of the switched-capacitor resonator in Fig. 4.2.

exponential input from OA_2 but this is generally not a problem since OA_1 has an entire clock period to respond to this input.

With ideal op amps and capacitors $C_A = C_B = 1$, the transfer function of the modified resonator is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = H_{\text{LP}}(z) = \frac{C_1 C_2}{z^2 + z\left(C_2 C_3 + C_2 C_4 - 2\right) + \left(1 - C_2 C_3\right)} \tag{4.2}$$

which is the same as the transfer function (Eq. 4.1) as the original resonator in Fig. 4.2.

4.1.2 Analysis

The input square wave to the switched-capacitor resonator can be expressed as a summation of its frequency components:

$$V_{\text{in}}(t) = \frac{4}{\pi} V_{\text{ref}} \sum_{n=1}^{\infty} \frac{1}{2n-1} \sin\left(\left(2n-1\right)\omega_0 t\right) \tag{4.3}$$

where ω_0 is the fundamental frequency of the square wave expressed in radians per second.

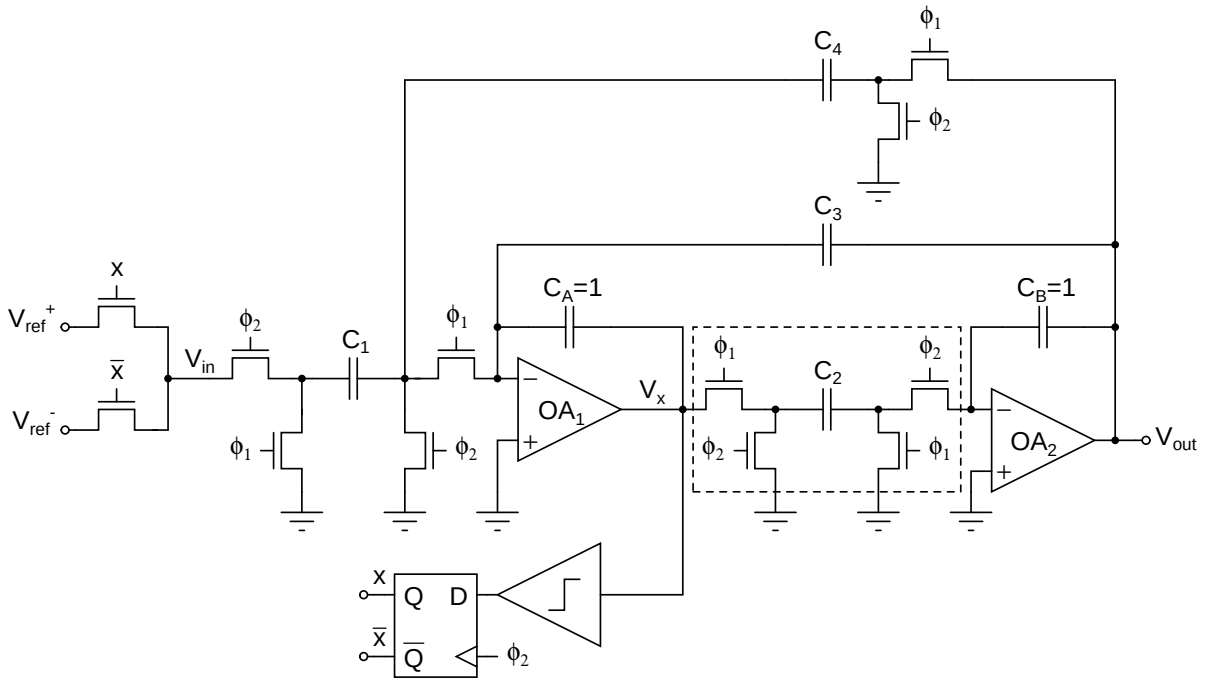


Figure 4.5: A switched-capacitor sinusoidal oscillator with reduced sensitivity to finite op amp bandwidth.

The transfer function of the resonator can be analysed in the frequency domain by substituting $z = e^{j\omega}$, where ω is in the range from and including $-\pi$ to π. The DC gain of the resonator can be found by setting $z = e^{j0}$ in Eq. 4.2

$$\left|H_{\mathrm{LP}}(e^{j0})\right| = \frac{C_1 C_2}{1 + (C_2 C_3 + C_2 C_4 - 2) + (1 - C_2 C_3)} = \frac{C_1}{C_4} \tag{4.4}$$

At the resonant frequency, ω_0, the gain of the resonator is approximately

$$\left|H_{\mathrm{LP}}(e^{j\omega_0})\right| \approx \frac{C_1}{C_4} Q \tag{4.5}$$

The amplitude of the output fundamental sinusoidal wave can be found by combining 4.3 with 4.4

$$|V_{\mathrm{out}}(j\omega_0)| \approx \frac{4}{\pi} V_{\mathrm{ref}} \frac{C_1}{C_4} Q \tag{4.6}$$

At frequencies greater than the resonant frequency, the gain of the resonator follows the behaviour of a second-order low-pass system, decreasing by approximately $-40\,\mathrm{dB}$ per decade from the DC gain. Using the second-order low-pass asymptotic approximation, the resonator's response to the nth order harmonic component of the input square wave is [46]

$$\left|H_{\mathrm{LP}}(e^{jn\omega_0})\right| \approx \frac{4}{\pi} V_{\mathrm{ref}} \frac{1}{n} \frac{C_1}{C_4} \cdot \frac{1}{n^2} \approx \frac{1}{n^3} \cdot \frac{4}{\pi} V_{\mathrm{ref}} \frac{C_1}{C_4} \tag{4.7}$$

The nth order harmonic amplitude can be found by dividing Eq. 4.7 by Eq. 4.5

$$\mathrm{HD}^{(\mathrm{n})} \approx \frac{1}{n^3 Q} \tag{4.8}$$

Hence, the quality of the oscillator can be assessed by the relative levels of these harmonics.

4.1.3 Effects of Finite Op-Amp Gain and Bandwidth

The quality factor of a switched-capacitor biquad filter is strongly affected by the settling behaviour of its op amps. The effective quality factor, Q_e, is related to the ideal Q by [47]

$$Q_e \approx \frac{Q}{1 + Q\left(\theta_1\left(\omega_0\right) + \theta_2\left(\omega_0\right)\right)} \tag{4.9}$$

where $\theta_1\left(\omega_0\right)$ and $\theta_2\left(\omega_0\right)$ are the respective phase errors of op amps OA_1 and OA_2 at the biquad filter's resonant frequency. The effects of finite op amp gain and gain-bandwidth product on $\theta\left(\omega_0\right)$ are discussed below.

Effects of Finite Op Amp DC Gain

The phase error due to finite op amp gain for both the inverting and non-inverting integrator configuration is given by [47]

$$\theta\left(\omega_0\right) = \frac{\frac{C_I}{C_F}}{2A_0 \tan\left(\frac{\omega_0}{2f_c}\right)} \tag{4.10}$$

where f_c is the clock frequency, C_I is the sum of all input capacitances, and ω_0 is the unity-gain frequency of the integrator. The unity-gain frequency is given by [47]

$$\omega_0 = 2f_c \sin^{-1}\left(\frac{C_1}{2C_F}\right) \tag{4.11}$$

If $\frac{\omega_0}{2f_c} << 1$, the Eq. 4.10 becomes approximately [47]

$$\theta(\omega_0) \approx \frac{1}{A_0} \tag{4.12}$$

In the typical case of $C_I < C_F$, Eq. 4.12 can be further approximated to

$$\theta(\omega_0) \approx \frac{1 + C_I/C_F}{A_0} \approx \frac{1}{L_{g,0}} \tag{4.13}$$

which is the same as the gain error associated with the inverting amplifier (2.5).

Effects of Finite Op Amp Gain Bandwidth Product

The phase error due to finite op amp gain-bandwidth product, ω_T, for the inverting and non-inverting integrator configurations are described in Table 4.1 [47]. If the magnitude of

Table 4.1: Phase error due to finite op amp gain-bandwidth product.

Inverting Integrator	Non-Inverting Integrator
$\phi(\omega_0) \approx -e^{-\frac{\beta\omega_T}{2f_c}} \beta \sin\left(\frac{\omega_0}{f_c}\right)$ (4.14) $\beta = \frac{C_F}{C_I + C_F}$	$\phi(\omega_0) \approx 0$

the phase error in an integrator is small, the total phase error is determined by summing the individual phase errors associated with finite op amp bandwidth and gain (Eq. 4.13 and either Eq. 4.10 or 4.13 accordingly).

4.1.4 Choice of Filter Coefficients

The switched-capacitor oscillator for the sinusoidal oscillator should have a modest Q of about 10 ($\mathrm{HD}^{(3)} = -48.63$ dBFS) in order to suppress the tones of the input square wave. The resonant frequency was chosen to be near $f_c/50$ so that the effects of finite op amp bandwidth on the resonator's quality factor can be ignored. Also, a lower resonant frequency allows the frequency component of the clock to be easily filtered out while preserving the harmonics of the oscillator. The following transfer function was generated in Matlab that satisfies the above requirements

$$H_{\mathrm{LP}}(z) = \frac{1}{z^2 - z1.972 + 0.9875} \tag{4.15}$$

By setting $C_2 = C_3$ and $C_A = C_B = 1$, the following capacitor values for Eq. 4.2 were determined

$$\begin{aligned} C_2 &= 0.112 \\ C_3 &= 0.112 \\ C_4 &= 0.139 \end{aligned}$$

C_1 sets only the DC gain (Eq 4.4) of the resonator and its value can be chosen arbitrarily. To simplify design and layout, capacitors C_1, C_2, C_3, and C_4 were all set to 0.125. The transfer function of the resonator becomes

$$H_{\mathrm{LP}}(z) = \frac{0.015625}{z^2 - z1.969 + 0.9844} \tag{4.16}$$

which shifts ω_0 from $f_c/50$ to $f_c/49.87$ and Q from 10 to 7.97. The frequency response of Eq. 4.15 and 4.16 are plotted in Fig. 4.6.

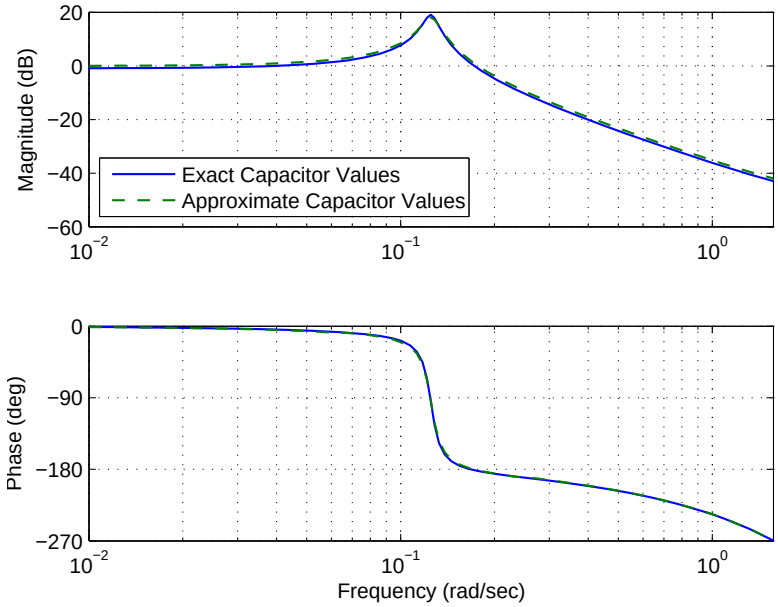


Figure 4.6: Frequency response (normalized to $\pi/2$) of two resonators. The solid line represents Eq. 4.15 and the dashed line represents Eq. 4.16.

4.1.5 Start-Up Circuit

When power is applied to the switched-capacitor sinusoidal oscillator in Fig. 4.5, there is no mechanism in place to ensure that the circuit will oscillate. Fig. 4.7 shows the oscillator with a start-up circuit consisting of capacitors C_5 - C_8, transistors $M1$ - $M5$, and a digital buffer [46]. If the system is not oscillating, transistor $M1$ will be off and the circuit will begin to oscillate through positive feedback provided by capacitors C_5 and C_6. Once the circuit starts to oscillate, transistor $M1$ is turned on, thus grounding node V_X and hence removing the positive feedback capacitors from the system.

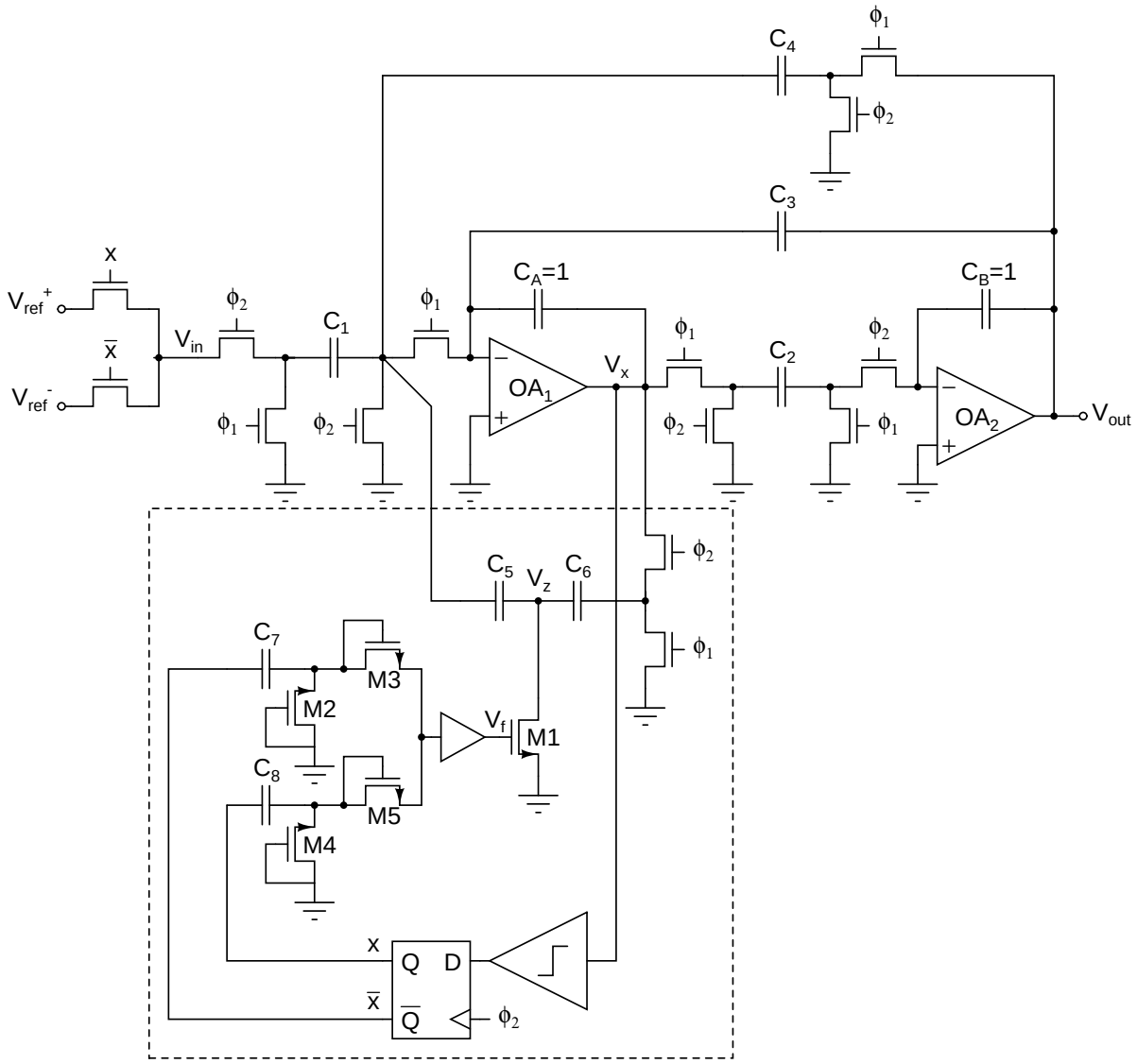


Figure 4.7: A switched-capacitor sinusoidal oscillator with start-up circuitry.

Fig. 4.8 shows the signal flow graph of the resonator with the positive feedback capacitors. In the signal flow graph, capacitors C_5 and C_6 are combined into capacitor C_Z

($C_Z = C_5||C_6$). The transfer function for the signal flow graph is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = H_{\text{LP}}(z) = \frac{C_1 C_2}{z^2 + z\left(C_2C_3 + C_2C_4 - 2 - C_Z\right) + \left(1 - C_2C_3 + C_Z\right)} \tag{4.17}$$

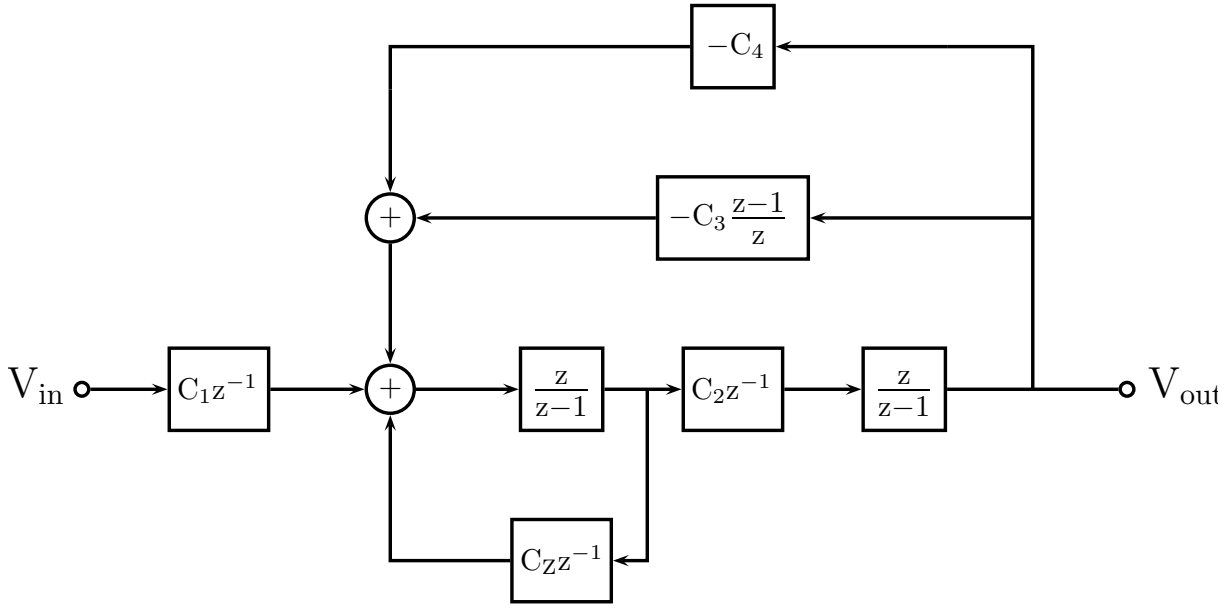


Figure 4.8: Signal flow graph of the switched-capacitor resonator with start-up circuit.

If the poles of the transfer function are placed outside the unit circle, the circuit will start to oscillate due to positive feedback. If $C_Z = 0.125$ is chosen, the transfer function, with the filter coefficients determined in Section 4.1.4, becomes

$$H_{\text{LP}}(z) = \frac{0.015625}{z^2 - z2.094 + 1.109} \tag{4.18}$$

and the poles of the above transfer function are at

$$p_{1,2} = 1.047 \pm j0.116 \tag{4.19}$$

which are outside the unit circle. Hence, the start-up circuit should provide the initial oscillation for the system.

4.2 Matlab Simulation Results

The effects of finite op amp gain and bandwidth on the quality factor of switched-capacitor resonators, described in Section 4.1.3, is only applicable for integrators with a first-order settling response, such as ones that use single-stage or multipath Miller compensated op amps [47]. For integrators exhibiting higher-order settling behaviours, such as ones that use conventional or nested Miller compensated op amps, the effects of the non-idealities cannot be accurately predicted using the analysis described in Section 4.1.3. Thus, Matlab behavioural simulations were performed to compare the differences in the quality factor of the resonator in Fig. 4.5 that makes use of second-order multipath or conventional Miller compensated op amps with the same DC gain and gain-bandwidth product. Fig. 4.9 shows the block diagram of the switched-capacitor resonator where the ideal lossless integrators are replaced with lossy integrators. The factor $p = 1 - \epsilon$ accounts for errors due to the effects of both finite op amp gain and bandwidth [48]. By replacing the ideal integrator blocks $\frac{z}{z-1}$ with $\frac{pz}{z-p}$, the resonator's transfer function becomes

$$H_{\mathrm{LP}}(z) = \frac{p^2 C_1 C_2}{z^2 + z\left(p^2 C_2 C_3 + p^2 C_2 C_4 - 2p\right) + \left(p^2 - p^2 C_2 C_3\right)} \tag{4.20}$$

Op amps with a DC loop gain of 60 dB and a gain-bandwidth product of 1 rad/s were chosen for the Matlab simulations. The phase margins of the multipath and conventional Miller compensated op amps were chosen to be 90° and 60°, respectively. Fig. 4.10 shows the step responses of the two op amps.

With reference to Fig. 4.10, it is expected that the resonator's quality factor will exhibit greater sensitivity to clock frequency variation in integrators with 60° phase margin than integrators with 90° phase margin. The results of the simulation, shown in Fig. 4.11a,

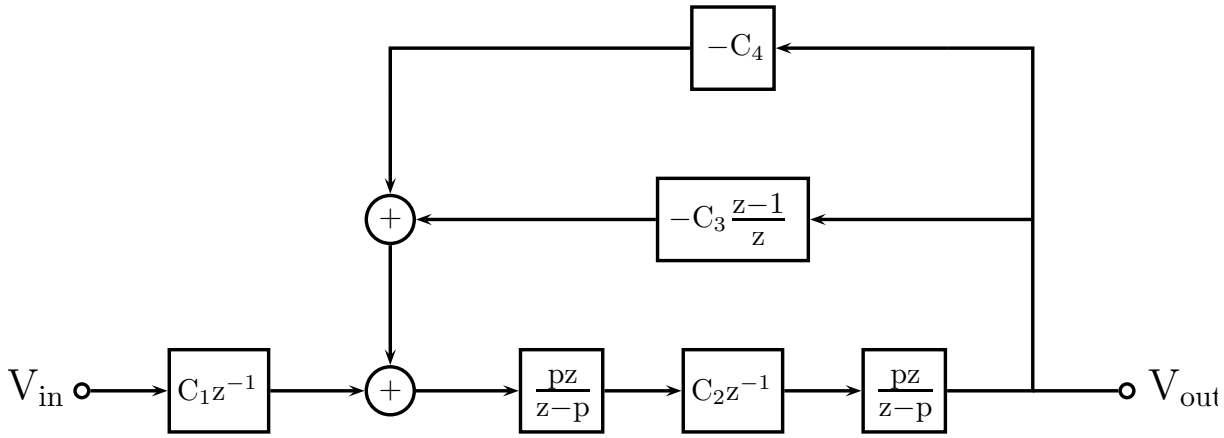


Figure 4.9: Signal flow graph of the switched-capacitor resonator with non-ideal op amps.

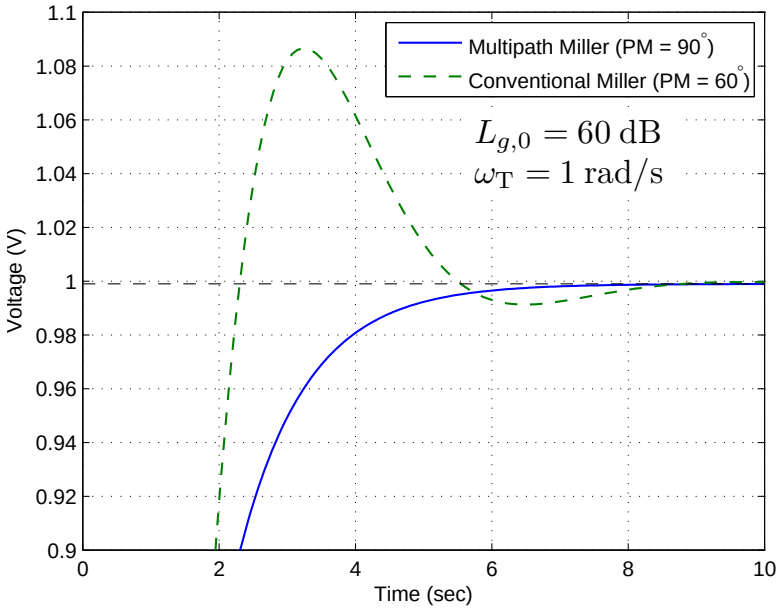


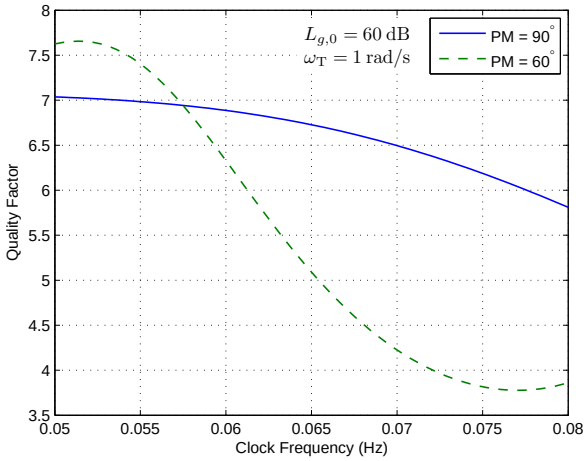
Figure 4.10: Step response of multipath Miller (PM = 90°) and conventional Miller PM = 60° op amps.

confirms that resonators using conventional Miller compensated op amps are indeed more sensitive to clock frequency variation than resonators using multipath Miller compensated

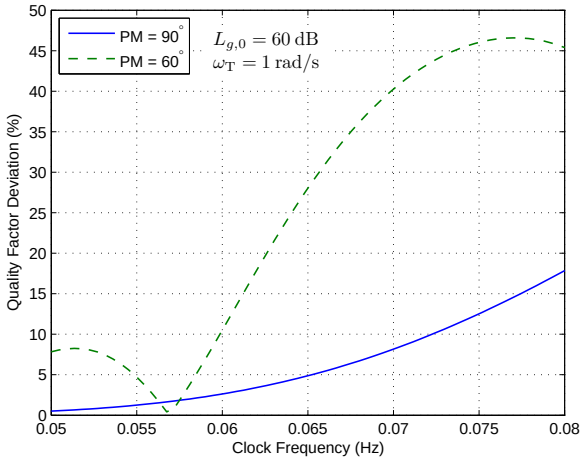
op amps. At low clock frequencies and with finite op amp gain, a resonator's quality factor may be higher with conventional Miller compensated op amps because the op amp's settling overshoot will bring the output voltage closer to its ideal settling value. At very low clock frequencies ($\omega_{\mathrm{T}}/f_c \to \infty$) where the op amp output completely settles, the resonator's quality factor was determined from simulation to be 7.07, whereas from the analysis in Section 4.1.3, a quality factor of 7.85 was expected. This discrepancy appears because the analysis in Section 4.1.3 models switched-capacitor integrators more accurately using frequency-domain analysis. Despite the inaccuracies in the Matlab model, the simulation result should be sufficiently accurate for comparing the performance of resonators with each type of op amps.

Fig. 4.11b shows the percentage variation of the quality factor from the expected Q when the outputs of the op amps have completely settled ($\omega_{\mathrm{T}}/f_c \to \infty$). This plot shows that multipath Miller compensated op amps exhibit more predictable resonator behaviour than conventional Miller compensated op amps if the degradation of the resonator's quality factor due to finite op amp gain is accounted for in the system-level design.

The differences in the quality factors as the clock frequency is increased should result in noticeable differences in the resonator's third-order distortion performance. For example, based on the above Matlab simulations at $\omega_{\mathrm{T}}/f_c = 0.075$, the quality factor for the resonator with multipath and conventional Miller-compensated op amps is expected to be at 6.18 and 3.82, respectively. Using Eq. 4.8, the third-order distortion components was computed to be at -44.45 dBFS and -40.26 dBFS, respectively.



(a) Quality factor versus clock frequency.



(b) Percentage quality factor deviation versus clock frequency.

Figure 4.11: Matlab simulations of a switched-capacitor resonator's quality factor as the clock frequency is varied.

4.3 Summary

A switched-capacitor oscillator incorporating a second-order biquad and a comparator is used to illustrate the benefits of the proposed multipath Miller-compensation over conventional Miller-compensation. The oscillator was designed for a nominal oscillation frequency of $f_0 = f_c/50$ and $Q = 8$. The amplitude of output harmonics, and hence the quality of oscillation, is determined by the performance of the op amps in the resonator. Based on Matlab simulations, it was found that an oscillation incorporating multipath Miller-compensated op amps exhibited significantly lower third-order distortion at $\omega_T/f_c = 0.075$ than the same op amps with conventional Miller-compensations.

Chapter 5

Circuit Design

This chapter discusses the design of a switched-capacitor oscillator incorporating conventional and multipath Miller-compensated op amps. In order to make a fair comparison, both op amp topologies are implemented on a single op amp such that the feedforward mode can toggled on or off. Section 5.1 describes the design of the switched-capacitor oscillator, including the choice of capacitor and switch sizes. The design of the op amp, which includes both multipath and conventional Miller-compensation, is discussed in Section 5.2. Section 5.3. briefly describes the design of the ancillary circuits in the system, such as the comparator, non-overlapping clock generator, and output buffers.

5.1 Switched-Capacitor Oscillator Design

Table 5.1 summarizes the system-level specifications for the switched-capacitor oscillator in Chapter 4.1.1. The choices for the resonant frequency and quality factor were previously described in Section 4.1.4. The relative low clock frequency of $1 - 10$ MHz allows the

chip to be placed in the dual in-line package (DIP) so that it can be tested on solderless breadboards. The signal-to-noise ratio was chosen to be greater than 48 dB so that the oscillator's third-order harmonic, $HD^{(3)}$, can be easily distinguished from thermal noise on a spectrum analyser without requiring signal averaging. With a nominal supply voltage of 1.8 V in the 0.18 μm process, a peak differential output voltage of 1.0 V was determined to be quite feasible for the two-stage op amp topology shown in Section 3.5.

Table 5.1: Switched-capacitor oscillator specifications

Specification	Value
Resonant Frequency (f_0)	$f_c/50$
Quality Factor (Q)	7.97
Clock Frequency (f_c)	$1 - 10$ MHz
Signal-to-Noise Ratio (SNR)	> 48 dB
Peak Differential Output Voltage ($V_{o_{\text{pk}}}$)	1.0 V

In switched-capacitor circuits, the size of the op amps and switches are determined by size of the capacitors. The capacitors, in turn, are determined by the thermal noise specifications of the system.

5.1.1 Capacitor Sizing

Fig. 5.1 shows the equivalent circuit model for MIM capacitors without the shield structure in the 0.18 μm process. The minimum capacitor dimensions for the process is 4 μm by 4 μm but capacitors with dimensions 5 μm by 5 μm were chosen as unit capacitor cells for this design as they are better characterized [49].

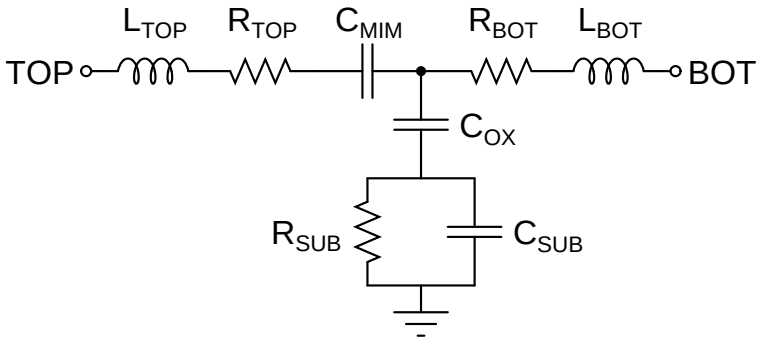


Figure 5.1: Equivalent circuit model for the MIM capacitor without shield structure.

The minimum capacitor size is determined by signal-to-noise considerations. For the switched-capacitor oscillator circuit shown in Fig. 4.5, the overall noise of the system is dominated by thermal noise from capacitor C_1. The mean-square value of the output noise is related to the peak output signal, V_s, and desired signal-to-noise ratio, SNR, by

$$\overline{V_n^2} = \frac{\overline{V_s^2}}{2 \cdot 10^{\mathrm{SNR}/10}} \tag{5.1}$$

The approximate relationship between mean-square value of the output noise and capacitance of C_1 is

$$\overline{V_n^2} = \frac{2 \cdot 2 \cdot Q^2 \cdot kT}{C_1} \tag{5.2}$$

where Q is the quality factor of the resonator. In the above equation, the first factor of two accounts for thermal noise in differential circuits and the second factor of two accounts for the fact that sampling noise and hold noise are distinct and uncorrelated [50, 51]. Eq. 5.2 overestimates the thermal noise contribution from capacitor C_1 since it assumes the resonator has a gain of Q for all frequencies. Eq. 5.1 and 5.2 are combined to obtain the necessary capacitance of C_1 for given system specifications

$$C_1 = \frac{8 \cdot Q^2 \cdot kT \cdot 10^{\mathrm{SNR}/10}}{\overline{V_s^2}} \tag{5.3}$$

For a switched-capacitor resonator with $Q = 8$, $V_s = 1.0$ V, SNR = 48 dB, and $T = 25$ °C, the minimum capacitance of C_1 is 132.98 fF which can be implemented with five unit capacitors (5×30.5 fF = 152.5 fF). Table 5.2 summarizes the size of the capacitors for the switched-capacitor oscillator shown in Fig. 4.7. Their values were determined based on the capacitor ratios described in Sections 4.1.4 and 4.1.5.

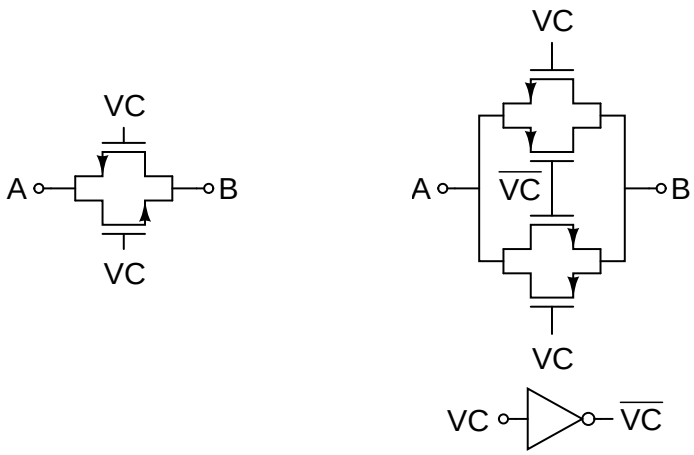
Table 5.2: Capacitance of capacitors in Fig. 4.7

Capacitor	C_A	C_B	C_1	C_2	C_3	C_4	C_5	C_6
Value	1.22 pF	1.22 pF	152.5 fF	152.5 fF	152.5 fF	152.5 fF	305 fF	305 fF

5.1.2 Switch Sizing

The switched-capacitor oscillator makes use of both NMOS and CMOS (transmission gate) switches, which are shown in Fig. 5.2. The switches are implemented as symmetric pairs in order to remove asymmetric switching behaviour from the BSIM3 transistor model [52]. In this design, CMOS switches are used where high-swing signals are involved, such as at the input and output of op amps.

In this switched-capacitor design, the switch bandwidth must be much higher than the clock frequency so that the performance of the oscillator is determined solely by that of its op amps. By making the op amps the performance-limiting factor in the design, one can ascertain the settling behaviour of the op amps directly from the distortion performance of the oscillator. Fig. 5.3 shows the simulated frequency response of a minimum-sized (W = 2×0.42 µm, L = 0.18 µm) NMOS switch driving capacitors C_{1-4}, whose values were determined in Section 5.1.1. As Fig. 5.3 shows, the bandwidth of the switch is 293 MHz, which is much higher than the maximum clock frequency of 10 MHz.



(a) NMOS Switch. (b) CMOS Switch.

Figure 5.2: Schematic of NMOS and CMOS switches.

Switch Booster

Boosted switches are necessary for reducing distortion from the switches at the output of the op amps. Otherwise, distortion from the varying on-resistance of the switches will dominate the overall system distortion. The schematic of the switch booster is shown in Fig. 5.4 [53]. This switch booster circuit requires only one PMOS transistor with a floating body connection (M4) and guarantees that the gate-source voltage (V_{gs}) of all transistors do not exceed V_{DD}. When CK is low, the circuit is off and the output voltage V_{boost} is 0 V. In this phase, a voltage of V_{DD} is applied across capacitor C_3. When CK switches high, the bottom plate of C_3 is connected to the input signal V_{in} and the output voltage will nominally be $V_{\mathrm{in}} + V_{\mathrm{DD}}$.

Due to charge sharing, the V_{boost} in the on phase will never be exactly $V_{\mathrm{in}} + V_{\mathrm{DD}}$.

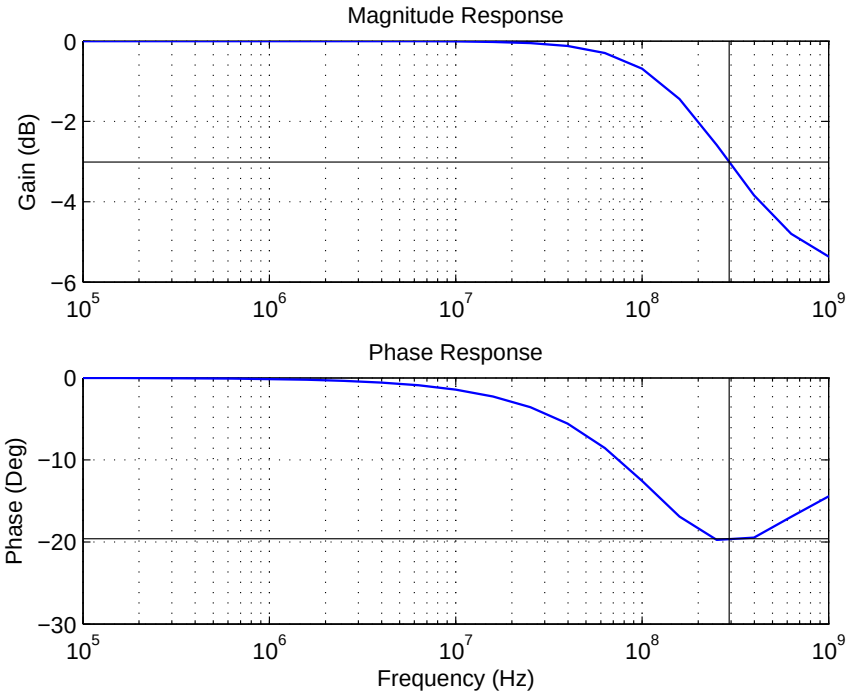


Figure 5.3: Frequency response of NMOS switch.

Instead, the V_{boost} will be approximately [53]

$$V_{\text{boost}} \approx V_{\text{in}} + \frac{C_3}{C_3 + C_p} V_{\text{DD}} \tag{5.4}$$

where C_p is the total parasitic capacitance at to the top plate of C_3 in the on phase. To keep the effects of C_p small, C_3 was chosen to be 1.22 pF and C_1 and C_3 were chosen to be one-fourth of C_3 (305 fF). The simulated output voltage for the minimum and maximum input voltage were found to be 1.758 V and 1.755 V, respectively. The boosted voltage is not constant because C_p is dependent on the output voltage. The difference in the boosted voltage is small enough that it will not affect the overall system distortion.

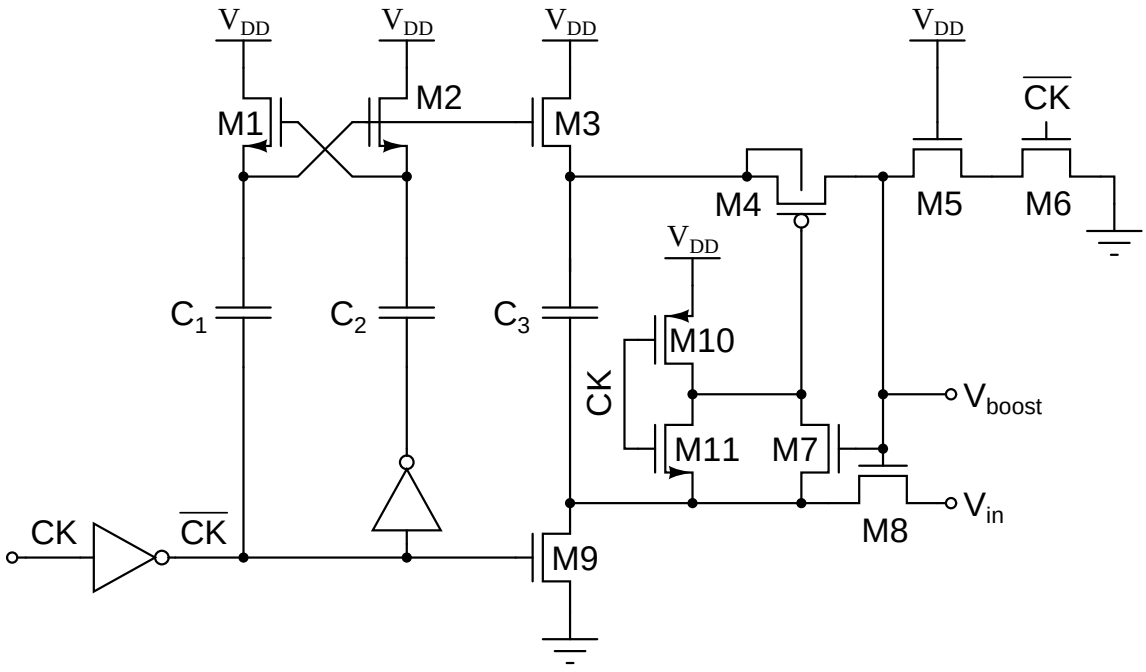


Figure 5.4: Schematic of clock bootstrap circuit.

5.1.3 Complete Circuit Implementation

The complete implementation of the switched-capacitor oscillator is shown in Fig. 5.5. Switches surrounded by a dashed rectangle are CMOS switches and switches surrounded by circles are boosted NMOS switches. When turned on, boosted NMOS switches will have a constant gate-to-source voltage of 1.8 V. The circuit uses bottom plate sampling where clocks ϕ_{1+} and ϕ_{2+} have their falling edges appear slightly earlier than clocks ϕ_1 and ϕ_2, respectively. By turning off specific switches earlier, the effects of signal-dependent charge injection is significantly reduced. A pair of CMOS switches are included in the start-up circuit. The switches will disconnect positive feedback capacitors C_5 and C_6 from the oscillator once the system starts to oscillate. This is done to reduce the capacitive loading of op amp OA_1. Track-and-hold amplifiers (THAs) are inserted at the outputs of

both OA_1 and OA_2 for the purpose of isolating the resonator's op amps from packaging and fixture parasitics, which are not known before design. Strictly speaking, OA_1 does not need a THA since it is not the output of the oscillator. Nonetheless, a THA was included for OA_1 so that the oscillator's band-pass output can be measured for debugging purposes. In addition, this simplifies the op amp design since the outputs of OA_1 and OA_2 will be loaded with similar amounts of capacitance.

5.2 Op Amp Design

In switched-capacitor circuits, the design of the op amps is strongly dependent on the values of the capacitors. As discussed in the previous chapter, the distortion performance of the switched-capacitor oscillator is strongly affected by its op amps. The DC gain of the op amps should be high enough so that the resonator's quality factor is not significantly degraded by the effects of finite op amp gain. In this design, it was decided that the resonator Q should not degrade by more than 1% due to finite op amp gain. The gain-bandwidth products for the op amps must be carefully chosen. If f_T is too high, the differences between the settling behaviours of a multipath and a conventional Miller compensated op amp cannot be easily distinguished. On the other hand, if f_T is too low, the oscillator will exhibit unpredictable behaviour due to incomplete settling. In this design, the minimum unity loop gain frequency, βf_T, was chosen to be $3.2 \times f_{c_{\min}}$ to give the op amps 10τ to settle at the lowest clock frequency (1 MHz). The maximum βf_T was chosen to be $2.2 \times f_{c_{\max}}$ to allow the op amps to settle to within 0.1% accuracy (6.9τ) at the highest clock frequency (10 MHz), assuming the op amps have a first-order settling response.

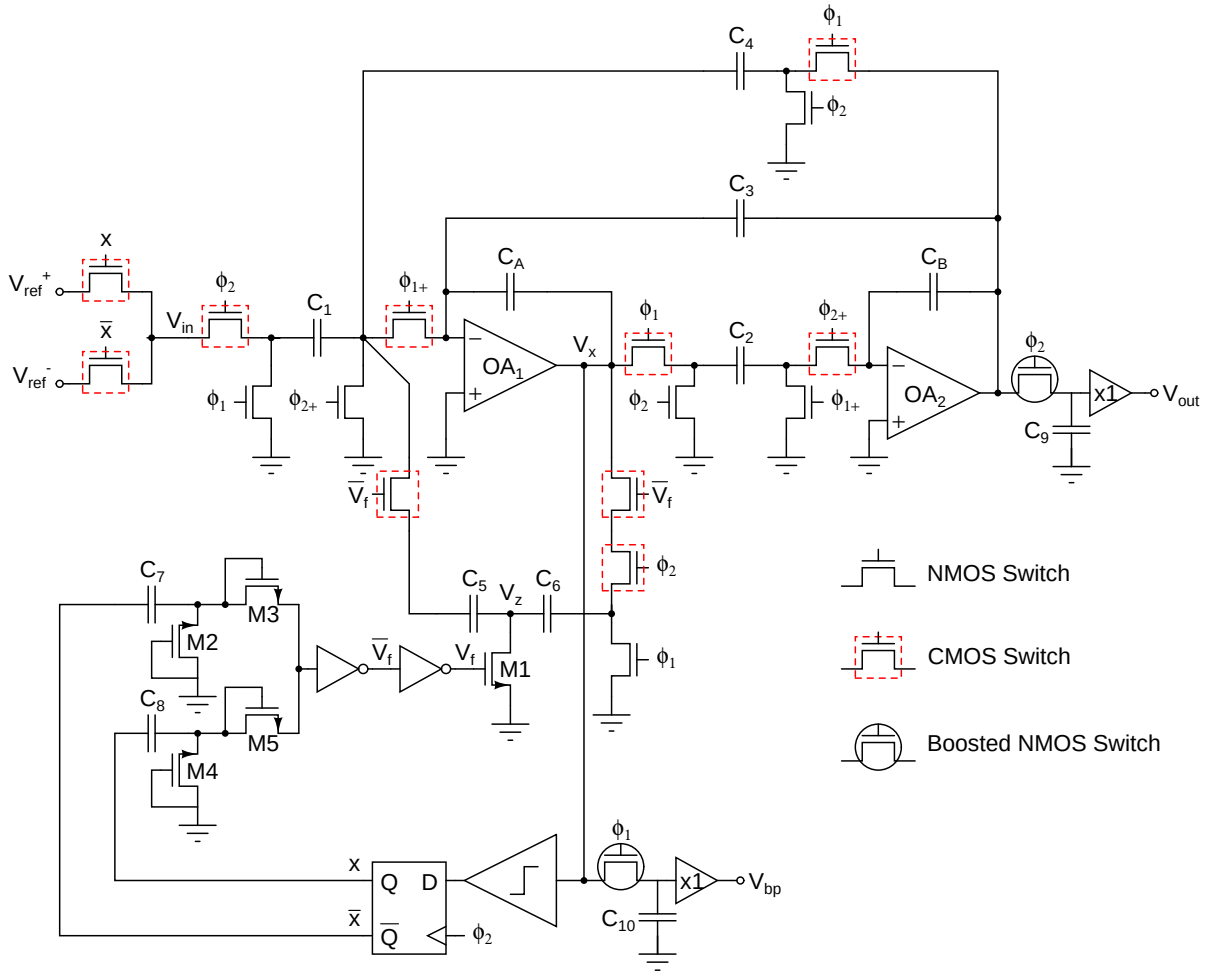


Figure 5.5: Complete schematic of switched-capacitor oscillator. The actual circuit is completely differential.

5.2.1 Gain

For any switched-capacitor biquad filter, Eqs. 4.9 and 4.13 can be used to determine the minimum DC loop gain, $L_{g,0}$, necessary for a given effective quality factor (Q_e) and desired quality factor (Q). Assuming both op amps in the resonator have the same $L_{g,0}$, the

minimum $L_{g,0}$ with $Q_e = 0.99 \times Q$ and $Q \approx 8$ is

$$L_{g,0_{\min}} = \beta A_0 \approx 64 \text{ dB} \tag{5.5}$$

The minimum open-loop op amp gain of this design is simply $L_{g,0_{\min}}/\beta$. During ϕ_2, the feedback factor, β, for op amp OA_1 is

$$\beta_{\text{OA}_1} = \frac{C_A}{C_A + C_1 + C_3 + C_4 + C_p} \tag{5.6}$$

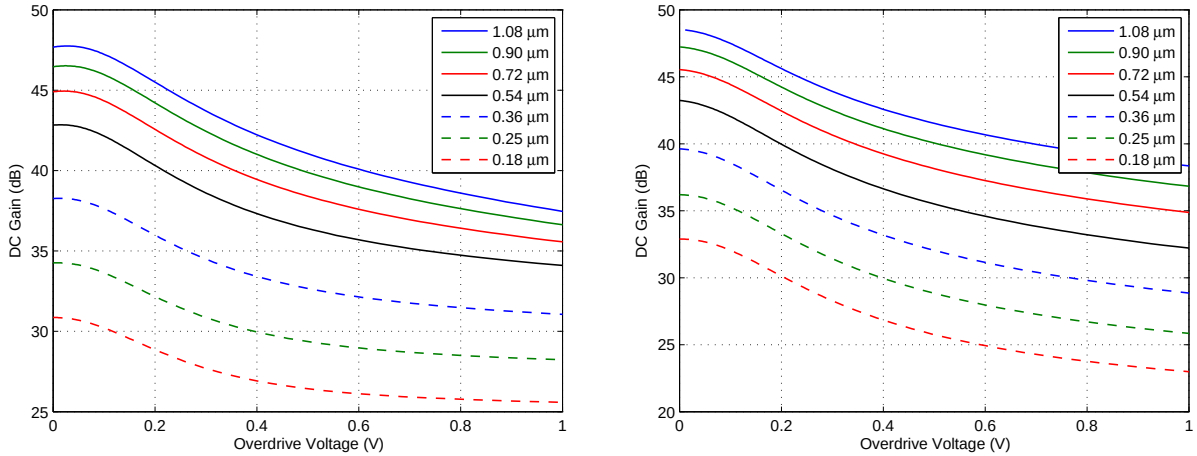
where C_p represents all the parasitic capacitors at the summation node of OA_1. Assuming C_p is approximately 10% of $C_A + C_1 + C_3 + C_4$, the feedback factor becomes

$$\beta_{\text{OA}_1} = \frac{1.22 \text{ pF}}{1.1\,(1.22 \text{ pF} + 152.5 \text{ fF} + 152.5 \text{ fF} + 152.5 \text{ fF})} \approx 0.36 = -3.59 \text{ dB} \tag{5.7}$$

The feedback factor for OA_2 is slightly higher than the above value. For the sake of simplicity, it is assumed that both op amps have the same feedback factor of $\beta = 0.36$. Thus, the minimum DC gain is

$$A_{0_{\min}} = \frac{L_{g,0_{\min}}}{\beta} = 67.59 \text{ dB} \tag{5.8}$$

Fig. 5.6 plots the DC gain versus overdrive voltage ($V_{\text{OV}} = V_{\text{GS}} - V_{\text{T}}$) of NMOS and PMOS transistors with different channel lengths in this 0.18 μm process. In real op amps the gain will be reduced by around 6 dB for every gain stage since replacing the ideal loads with active loads will decrease the output resistance, and hence the DC gain, by approximately a factor of 2. When biased at less than 200 mV of overdrive voltage, transistors with $L = 0.54$ μm have sufficient gain to meet the gain requirements for a two-stage op amp. In this work, the transistors in the op amps were biased at 150 mV. The extra 3 dB of DC gain provides some gain headroom in case the feedback factor of the loop changes.



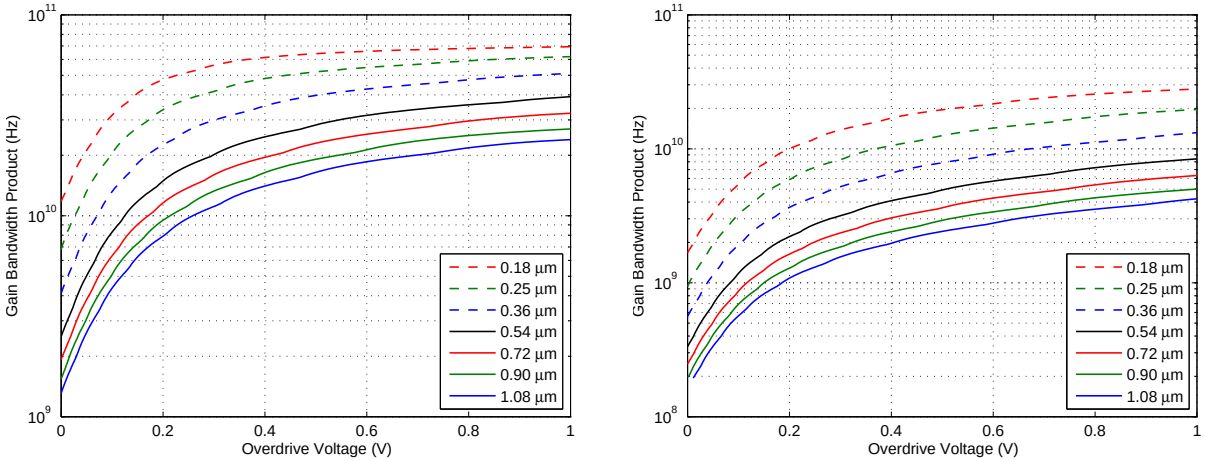
(a) NMOS.

(b) PMOS.

Figure 5.6: DC gain versus overdrive voltage for different transistor lengths.

5.2.2 Bandwidth

Based on previous analysis in this section, the op amp unity loop gain frequency, βf_{T}, should be between 3.2 MHz and 22 MHz. For a feedback factor of $\beta \approx 0.36$, it should be possible to design a two-stage Miller compensated op amp with a unity loop gain frequency, βf_{T}, that is approximately 1/50 of the output stage transistor f_{T} [31]. Fig. 5.7 plots the gain-bandwidth product versus overdrive voltage of NMOS and PMOS with different channel lengths in this 0.18 µm process. At $L = 540$ nm and $V_{\mathrm{OV}} = 150$ mV, both NMOS and PMOS transistors have the sufficient f_{T} to meet the unity loop gain frequency specifications. If the unity loop gain frequency is too high, it can reduced without changing the loop gain phase margin by proportionally increasing the miller capacitor, C_C, and the load capacitor, C_L.



(a) NMOS.

(b) PMOS.

Figure 5.7: Gain bandwidth product versus overdrive voltage for different transistor lengths.

5.2.3 Topology

In most two-stage Miller compensated op amps, the input stage is implemented with PMOS transistors while the output stage is implemented with NMOS transistors. This is done to obtain the greatest separation between ω_{p_1} and ω_{p_2}. Since the location of ω_{p_2} limits the maximum achievable op amp f_{T} for a fixed phase margin, as evident with Eq. 2.30, the NMOS output stage allows for one to maximize the frequency of the second pole, which will in turn maximize the op amp gain-bandwidth product. Furthermore, the op amp slew rate is improved when using a PMOS input stage [5]. As to be discussed in Section 5.2.6, the slew rate for this design is not very important.

In this design, the topology is reversed such that the input stage is implemented with NMOS transistors and the output stage is implemented with PMOS transistors. This was done for two reasons. Firstly, by using PMOS transistors for the output stage, the

op amp f_{T} will be significantly reduced. Reducing the op amp f_{T} is important because there is a maximum βf_{T} specification. If NMOS transistors are used for the output stage, the system would require excessively large load capacitors to push the op amp unity loop gain frequency below the maximum βf_{T}. Secondly, this topology better demonstrates the advantages of multipath Miller compensation over conventional Miller compensation. In this configuration, the separation between ω_{p_1} and ω_{p_2} is reduced. Hence, the phase margin of the conventional two-stage Miller compensated op amp will be degraded while the phase margin of the multipath Miller op amp will remain unaffected.

5.2.4 Op Amp Implementation

Fig. 5.8 depicts the schematic of the two-stage op amp with both a two-stage multipath Miller and a conventional Miller op amp. Sharing transistors between the two op amp topologies has the benefit of reducing area and eliminating any mismatch between the two topologies. Furthermore, the op amps are guaranteed to be biased at the same DC operating conditions. The feedforward control signal, FF, determines the mode of operation of the op amp. If FF = 1.8 V, transistors M13 and M14 will connect the differential input signals to the feedforward transistors M5 and M6. Hence, the op amp behaves as a two-stage multipath Miller compensated op amp. If FF = 0 V, transistors M15 and M16 will force transistors M5 and M6 to become active loads by driving the gates of the two transistors to the input common mode voltage, V_{CM}. This configuration turns the op amp into a two-stage conventional Miller compensated op amp.

In the feedforward mode, the finite on resistance of transistors M13 and M14 will affect the switch bandwidth. The two transistors were sized to ten times the nominal switch size ($W = 8.2$ µm) to ensure that this will not significantly affect the switch bandwidth.

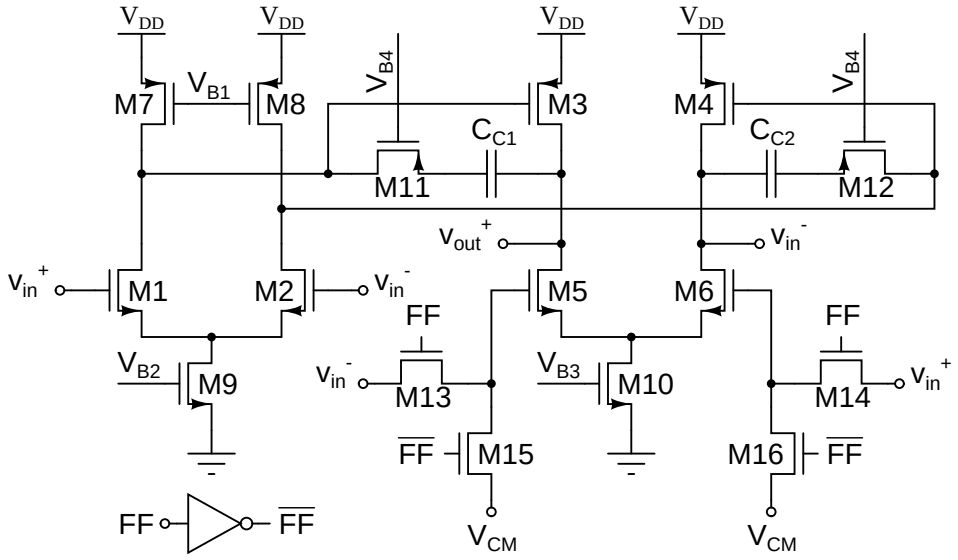


Figure 5.8: Schematic of the two-stage op amp used in this design.

This op amp, in both multipath and conventional Miller mode, requires two CMFB loops. One CMFB loop is necessary for the output stage to regulate the output common mode. Another CMFB loop is necessary for the input stage to regulate the output common mode of G_{m_1}. The latter loop is needed because transistors M3 and M4, which forms G_{m_2}, are pseudo-differential pairs and are extremely sensitive to variations in input common-mode.

5.2.5 Positive Feedback (Neutralizing) Capacitors

In the feedforward mode (FF = 1.8 V) there exists an additional feedforward signal path through the gate-drain capacitor (C_{gd}) of transistors M5 and M6. The presence of this capacitor causes a change in the ideal closed-loop gain. Since C_{gd} is in parallel with the

feedback capacitor C_F in Fig. 2.1, it changes the closed-loop gain the system to

$$A_{\mathrm{CL},0} = -\frac{C_I/\left(C_F + C_{gd}\right)}{1 + \frac{1+C_I/\left(C_F+C_{gd}\right)}{A}} \tag{5.9}$$

For a feedback system without C_{gd}, the expected closed-loop gain is

$$A_{\mathrm{CL},0} = -\frac{C_I/C_F}{1 + \frac{1+C_I/C_F}{A}} \tag{5.10}$$

The presence of C_{gd} can be treated as an apparent reduction in the loop gain in Eq. 5.10 by α, where α is

$$\alpha \approx \frac{1}{1 + L_{g,0}\frac{C_{gd}}{C_F+C_{gd}}} \tag{5.11}$$

α can significantly decrease the apparent loop gain, even for low values of C_{gd}. The complete derivation of α can be found in Appendix B.

The effects of C_{gd} can be removed by cascoding transistors M5 and M6. Cascoding is not feasible in this design since it will use up voltage headroom and is not practical in advanced CMOS processes. Another solution is reduce C_F so that $C_F + C_{gd}$ adds up to the expected C_F. This solution is also not very feasible since C_F and C_{gd} cannot be made to track one another. Fig. 5.9 illustrates another technique for neutralizing the effects of the gate-drain capacitor of transistors M5 and M6 [54]. Here, two transistors, M17 and M18, are placed in a positive feedback configuration. The gate-drain and gate-source capacitors of these transistors, placed in positive feedback, will counteract the negative feedback capacitors C_{gd_5} and C_{gd_6}. If the width of M17 and M18 are made exactly half of the width of M5 and M6 then the undesirable effects of C_{gd_5} and C_{gd_6} are completely neutralized [54]. Since the positive feedback capacitors are implemented with MOSFETs, this neutralizing technique is insensitive to process and temperature variations. The main disadvantage of this technique is the increased capacitive loading at the output resulting

from the drain-body and source-body capacitors of M17 and M18. However, this is not an issue in this design since the op amps are expected to operate at low bandwidths.

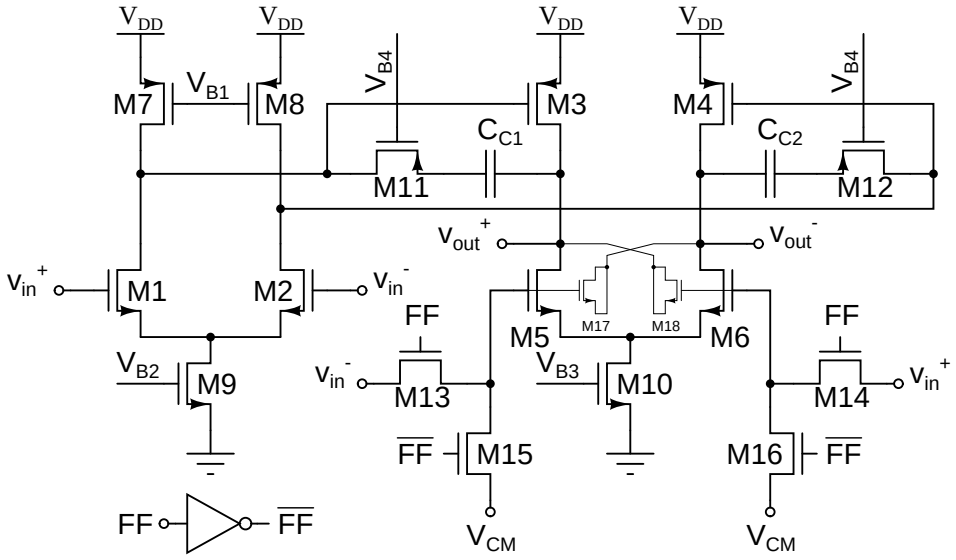


Figure 5.9: Schematic of op amp with neutralizing capacitors.

5.2.6 Slew Rate

The op amp in Fig. 5.9 has an internal and external slew rate [31]. The internal slew rate is relate to the charging of the compensation capacitor C_{C_1} by the op amp's input stage. The external slew rate pertains to the charging of the load and feedback capacitors, C_L and C_F, by the op amp's output stage. In this op amp topology, the compensation capacitors will likely be much larger than the load and feedback capacitors. Hence, it is expected that the internal slew rate will limit the settling response of the op amp. In this design, slewing is not a major concern since both the multipath Miller and conventional Miller op amps will experience the same slewing. Nonetheless, op amp slewing should not be ignored as it

may lead to unforeseen consequences.

Assuming the op amp has a first-order settling response, the minimum bias current to prevent slewing is

$$I_{\text{slew}} = C_{C_1} \beta \omega_{\text{T}} \max\left(\Delta V_{out}\right) \tag{5.12}$$

where $\max(\Delta V_{out})$ is the maximum change of the output during one clock cycle. The frequency of oscillation in this design is $f_c/50$ so the maximum phase change of the sinusoidal output is $360^\circ/50 = 7.2^\circ$ per clock period. Therefore, the output voltage varies the most when the phase transitions from 176.4° to 183.6° in one clock cycle, which is a 6.25 % change in the full-scale output voltage.

Assuming the compensation capacitor C_{C_1} of the op amp is 8 pF and a full-scale differential output voltage swing of 2 V, the minimum bias current for each branch of the input stage when the op amp is operating at the maximum $\beta\omega_{\text{T}} = 138$ Mrad/s is

$$\begin{aligned} I_{\text{slew}} &= 8 \text{ pF} \times 0.0625 \times 1 \text{ V} \times 138 \text{ Mrad/s} \\ &= 69 \ \mu\text{A} \end{aligned} \tag{5.13}$$

The bias current of 84 μA, for each branch, was chosen for the input stage of both OA_1 and OA_2. This value was chosen to be higher than necessary to make allowance for changes in the compensation capacitance. For the sake of simplicity, the bias current of the output stage was also set to 84 μA.

5.2.7 Output Common-Mode Feedback

The common mode of fully differential op amps is not always defined. In the op amp shown in Fig. 5.9, a common mode feedback (CMFB) circuit is necessary for defining the

common mode levels. Fig. 5.10 shows a CMFB circuit that is popular with switched-capacitor circuits [5, 10, 12, 55, 56]. The output signal V_{CMFB} controls the bias voltage of a tail or load transistor. On ϕ_1, the voltage across capacitor C_1 is charged to $V_{\text{CM}} - V_{\text{BIAS}}$, where V_{CM} is the desired common mode voltage and V_{BIAS} is the nominal bias voltage of a transistor. On ϕ_2, C_2 is connected in parallel with C_1 and the two capacitors will experience charge sharing. Over time, the voltage across C_2 will also be $V_{\text{CM}} - V_{\text{BIAS}}$. Once the circuit has reached this steady-state condition, the output voltage during ϕ_2 becomes

$$V_{\text{CMFB}} = \left(\frac{v_{\text{OUT}^+} + v_{\text{OUT}^-}}{2} - V_{\text{CM}} \right) - V_{\text{BIAS}} \tag{5.14}$$

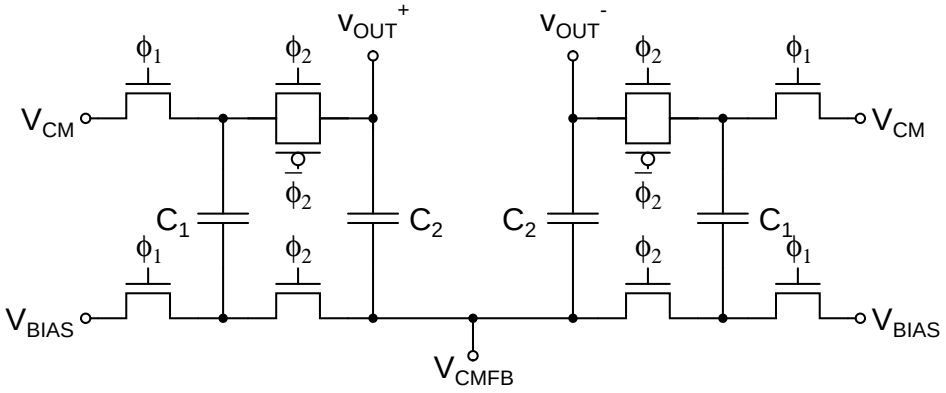


Figure 5.10: Switched-capacitor common mode feedback circuit.

In Fig. 5.10, C_1 is usually chosen to be between one-quarter to one-tenth the size of C_2 [5]. C_2 should be large enough so that it is not severely affected by charge injection from the switches. Since speed is not an issue in this design, C_1 and C_2 were set to 122 fF and 1.22 pF, respectively. The switches were set to the minimum dimensions ($W = 2 \times 0.42$ µm and $L = 0.18$ µm) in order to minimize the effects of charge injection on V_{CMFB}.

The switched-capacitor CMFB circuit in Fig. 5.10 is used to stabilize common mode of the input and output stages of the op amp. While only one CMFB loop is necessary for controlling the output common-mode, the design uses two CMFB loops for ease of stabilization. Referring to Fig. 5.9, the first CMFB loop stabilizes the common mode of the input stage by controlling V_{B1} (M7 and M8) while the second CMFB loop stabilizes the output common mode by controlling V_{B3} (M10). During start up, the input common mode may be low enough for transistor M9 to enter the triode/linear region. The first CMFB loop is connected to PMOS transistors as they will always remain in saturation. As summarized in Table 5.3, both loops are stable and have similar gain-bandwidth products.

Table 5.3: CMFB loop gain simulation results

CMFB Loop	Gain-Bandwidth Product	Phase Margin	Unity Loop Gain Frequency
CMFB 1	11.38 MHz	133.5°	16.54 MHz
CMFB 2	15.44 MHz	141.5°	164.4 MHz

5.2.8 Input Common-Mode Feedback

The op amps in Fig. 5.5 do not have a defined input common mode voltage. One possible solution is to dampen the integrator by introducing a resistor (real or switched-capacitor) in parallel with C_A and C_B. Both approaches are undesirable as they would require a redesign of the resonator's coefficients. Fig. 5.11 illustrates the input common mode feedback circuit in this design. In this configuration, transistors M1 and M2 are used as source-followers. Any change in the input common mode can be detected by sensing the tail voltage of the op amp's input stage. Two op amps, operating in open-loop configurations, continuously compare the tail voltage with the reference tail voltage. If a large enough deviation is

detected, V_{CTRL} is set to 1.8 V and the input common mode is reset to the desired value. The detection threshold is determined by the gain of the op amp and the switching threshold ($\mathrm{V_m}$) of the digital buffers. A pair of DFFs clocked on ϕ_2 are included to ensure that the input common reset occurs only on ϕ_2. Since ϕ_2 corresponds to the *hold* phase of this switched-capacitor circuit, the distortion caused by resetting the input common mode voltage is reduced compared to resetting on ϕ_1. Furthermore, the two DFFs ensure that common mode glitches caused by switches turning on/off will not inadvertently trigger the reset signal.

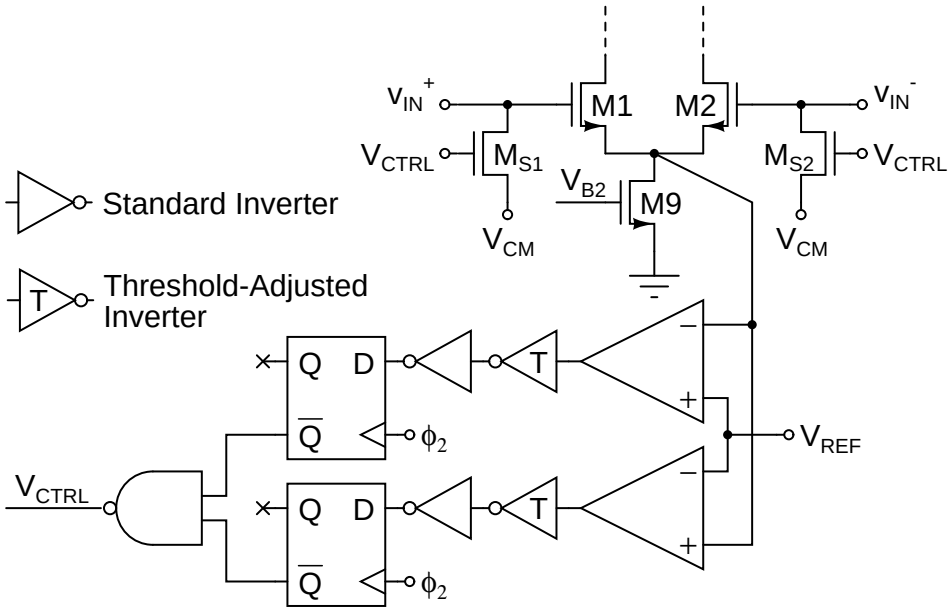


Figure 5.11: Technique for setting input common mode.

A schematic of the open-loop op amps are shown in Fig. 5.12. Here, the input signals are level-shifted with PMOS source followers M1 and M2.

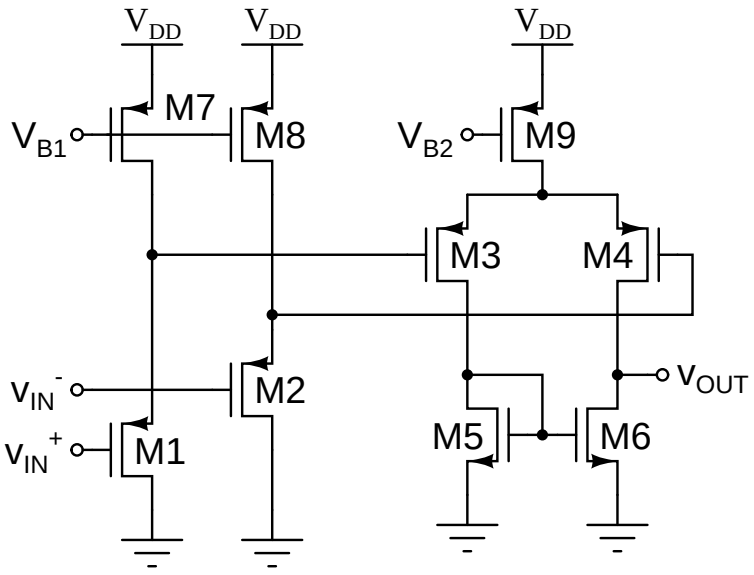


Figure 5.12: Schematic of the op amp in the input CMFB circuit (Fig. 5.11).

5.2.9 Simulation Results

Table 5.4 describes the transistor dimensions and bias currents of OA_1 and OA_2. The op amps were made identical in order to simplify layout. The transconductance of the feedforward stage, consisting of M5 and M6, was increased by $\sqrt{2}$ to relax the design equation Eq. 3.11. The capacitance of the Miller capacitor and load capacitor (effectively C_9 and C_{10} in Fig. 5.5) are found in Table 5.5. The capacitors are larger for OA_2 because the feedback factor for the op amp is larger.

Fig. 5.13 plots the magnitude and phase response of OA_1 and OA_2 in multipath and conventional Miller mode. As discussed in Section 5.2, the second pole in multipath Miller mode arises from the finite resistance of switches M13 and M14. Fig. 5.14 plots the steps response of the two op amps. It is clear that the op amps exhibit superior settling behaviours in multipath Miller mode compared to conventional Miller mode.

Table 5.4: OA_1 and OA_2 transistor dimensions and bias currents

Transistor(s)	Width	Length	Current
M1, M2	20×0.42 µm	0.54 µm	84 µA
M3, M4	44×1.26 µm	0.54 µm	84 µA
M5, M6	40×0.42 µm	0.54 µm	84 µA
M7, M8	44×1.26 µm	0.54 µm	84 µA
M9, M10	80×0.42 µm	0.54 µm	168 µA
M11, M12	44×1.26 µm	0.54 µm	0 µA
M17, M18	20×0.54 µm	0.54 µm	0 µA

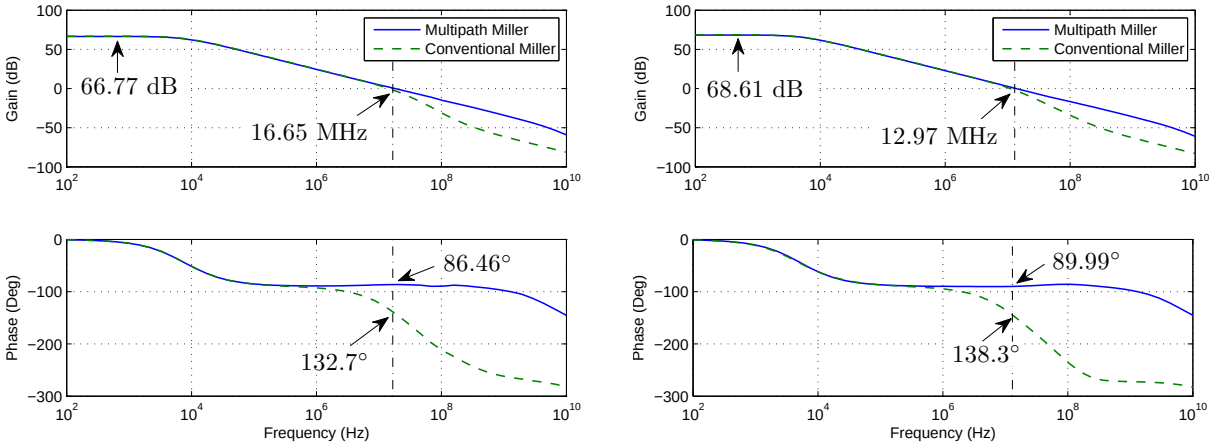
Table 5.5: Miller and load capacitor values for OA_1 and OA_2

Capacitor	OA_1	OA_2
C_{C_1}	5.06 pF	7.63 pF
C_L (C_9/C_{10})	2.59 pF	5.185 pF

5.3 Ancillary Circuits

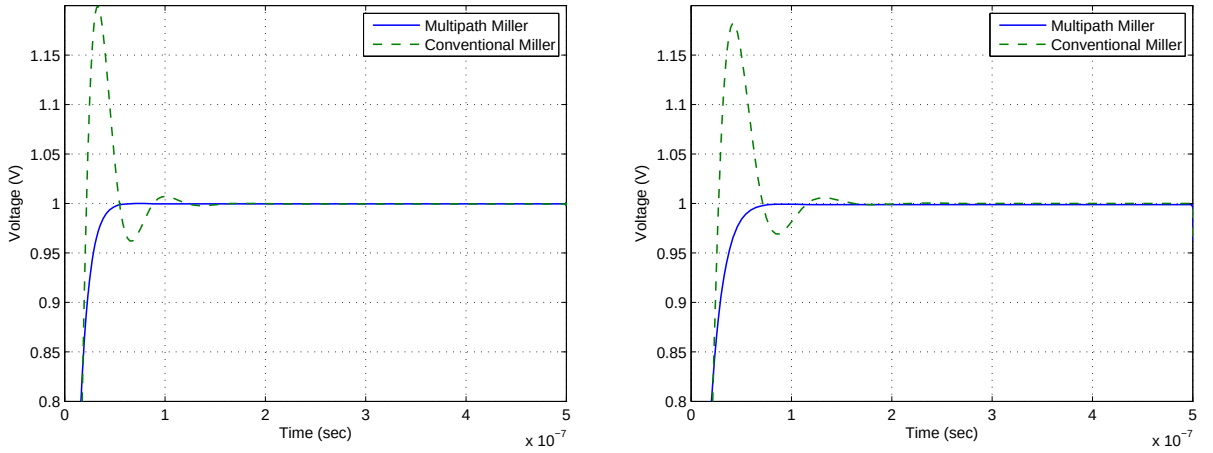
5.3.1 Dynamic Comparator

This switched-capacitor oscillator design uses a dynamic comparator for generating the input square wave to the resonator. The schematic of the comparator is shown in Fig. 5.15 consisting of a pre-amplifier and a track-and-latch stage [13]. The comparator is in reset mode when CK = 0 V. Transistors M7 and M8 are off and a crowbar switch will short the differential outputs. Static current flowing from M5/M6 to M9/M10 sets the comparator to its trip point. In this phase, both comparator output signals are logic low but are not



(a) OA_1. (b) OA_2.

Figure 5.13: Loop gain of OA_1 and OA_2.



(a) OA_1. (b) OA_2.

Figure 5.14: Transient response of OA_1 and OA_2.

at 0 V. The comparator enters the regeneration phase when CK transitions from low to high. The pre-amplifier amplifies the input signal and after a short delay, the crowbar

switch opens and forces the cross-coupled transistors M9 and M10 to regenerate. After another short delay, M7 and M8 are turned on to speed up the regeneration process. M7 and M8 are not cross-coupled since the extra capacitance at the output will slow down the regeneration process [13]. Furthermore, capacitor mismatch between the output nodes, which are a source of comparator offsets, is reduced if the PMOS transistors are not cross-coupled.

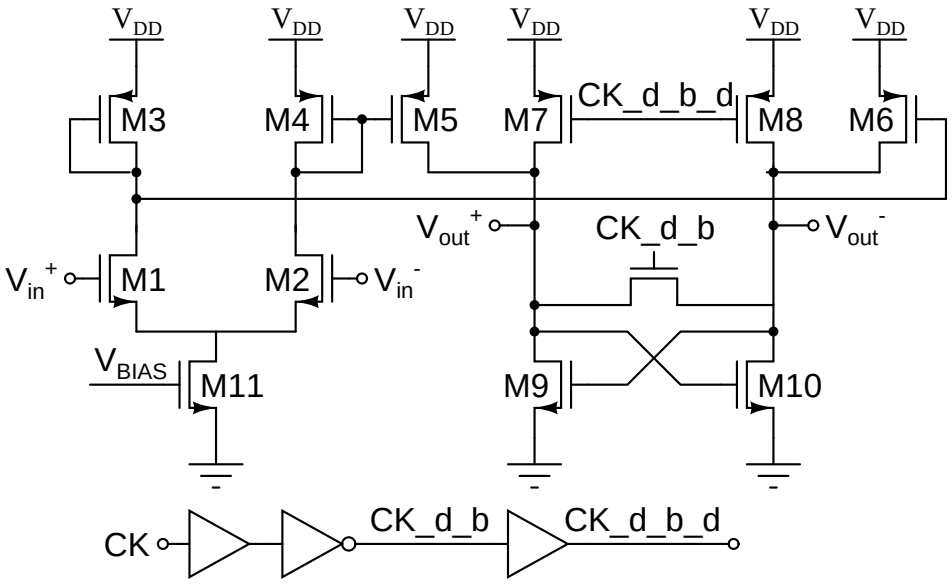


Figure 5.15: Dynamic comparator schematic.

5.3.2 Comparator Sampling Network

The comparator system including the comparator sampling network and output SR (Set-Reset) latch are illustrated in Fig. 5.16. The comparator sampling network consists of capacitors C_{in} and C_{ref} connected to a few switches [57].

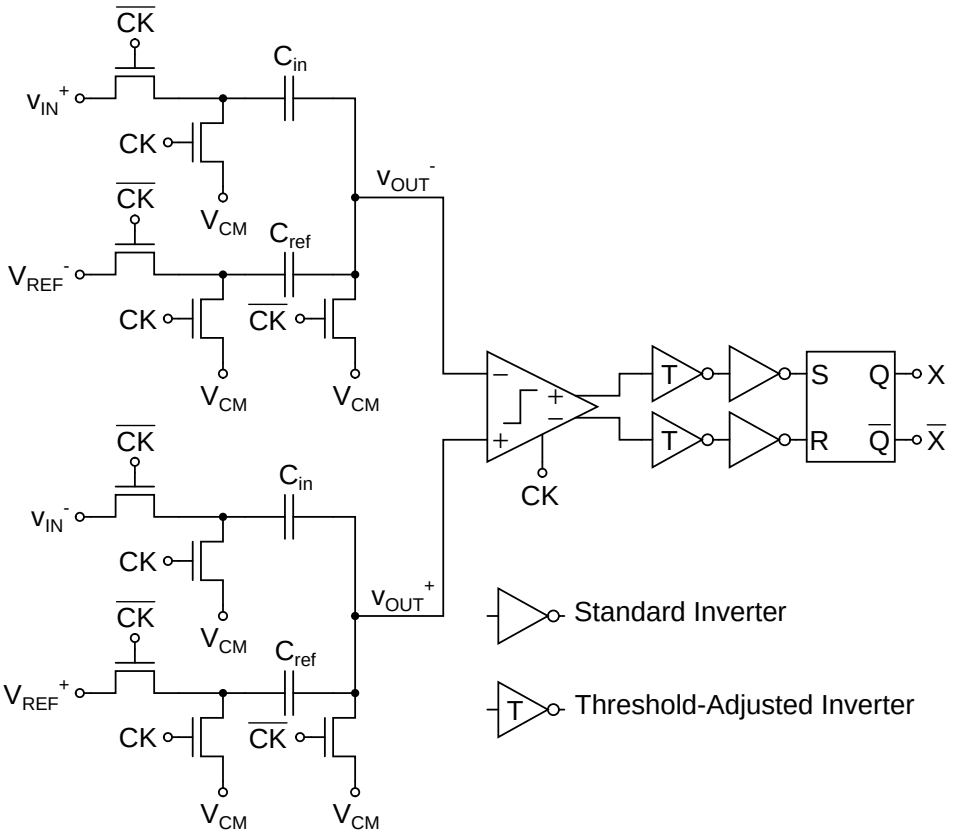


Figure 5.16: Dynamic comparator sampling network. All switches are minimum sized ($W = 2 \times 0.42$ µm, $L = 0.18$ µm) CMOS switches.

The SR latch in Fig. 5.16 is intended to hold the comparator's previous output during the sampling phase (CK is low). Two inverters, acting as buffers, are inserted between the comparator and the SR latch for the purpose of reducing kickback. The switching threshold of the first inverter had to be adjusted because the output of the dynamic comparator in the sampling phase, which never reaches 0 V, would have caused excessive leakage current with standard threshold inverters. The transistor dimensions of the threshold-adjuster inverters are $W_p/L_p = 4.2$ µm/0.18 µm and $W_n/L_n = 0.42$ µm/0.36 µm. Post-layout

simulations with extracted parasitic capacitors indicate that the entire comparator system has a layout-induced deterministic offset of 4 mV.

5.3.3 Non-Overlapping Clock Generator

The schematic of the non-overlapping clock generator is shown in Fig. 5.17 [58]. Here, the separation between the clock edges are set by the delays of the buffers. Large output buffers are used to drive the clock signals to the various switches in the system. The width of the buffers are progressively increased by a factor of 2 with the final size of 64 times the unit buffer size. SPICE-level simulations indicate the separation between the edges of ϕ_1 – ϕ_2 and ϕ_1 – $\phi_{1'}$ to be 130 ps and 107 ps, respectively. Both delays should be sufficient to allow for complete charge settling in the switches.

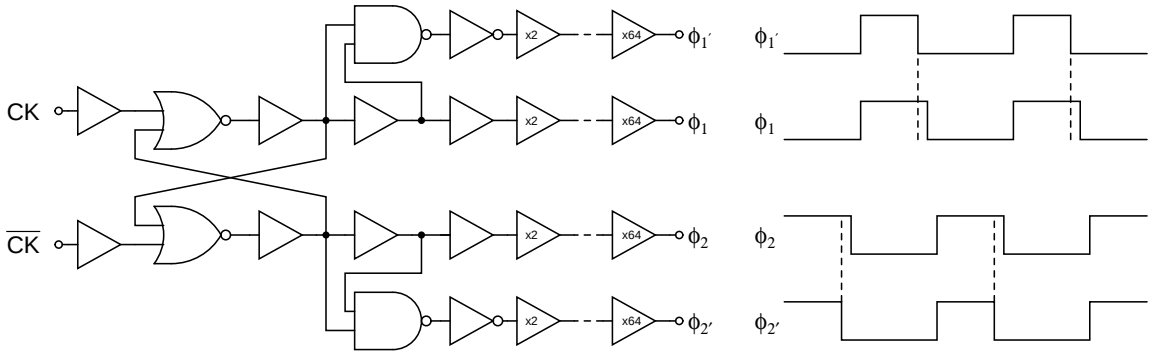


Figure 5.17: Schematic of the non-overlapping clock generator.

5.3.4 Output Buffer

As discussed in Section 5.1.3, output buffers are needed for isolating the switched-capacitor resonator's op amps from packaging and fixture parasitics. In this design, it is important

that the distortion of the buffers are much lower than the distortion of the oscillator. Hence, the buffer's third-order harmonic distortion must be less than −46.69 dBFS. While fixture parasitics are not known a priori, there exist circuit models for the packaging parasitics. Fig. 5.18 shows the equivalent circuit model of the bondpad parasitics in the DIP40 package, which is the package of choice for this design. The values of these parasitics vary significantly depending on the package pin. The lowest parasitic values are associated with pins 10, 11, 30, and 31 [59].

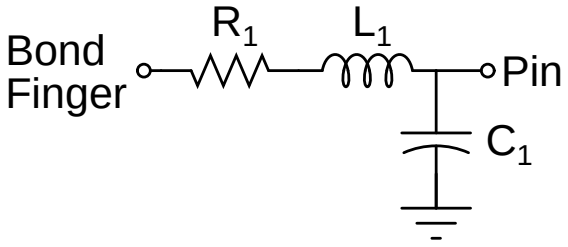


Figure 5.18: Equivalent circuit model of DIP40 bondpad parasitics.

The low speed of the system, relative to the achievable f_T of the technology, allows an op amp in a unity-gain feedback configuration to act as the output buffer. Fig. 5.19 shows the schematic of the output buffer consisting of a standard two-stage Miller compensated op amp in a unity-gain feedback configuration. The op amp uses the conventional PMOS input and NMOS output topology for maximizing the op amp gain-bandwidth product. The transistor dimensions and bias currents of the buffer are summarized in Table 5.6.

The op amp bode plot and full-scale distortion performance are shown in Fig. 5.20a and 5.20b, respectively. Although the fixture capacitance is expected to be under 2 pF, the buffer was designed to be stable for capacitive loads of at least 50 pF. As shown in Fig. 5.20b, at the maximum oscillation frequency of 200 kHz, the output buffer's third-order harmonic distortion is more than 10 dB lower than that of the switched-capacitor

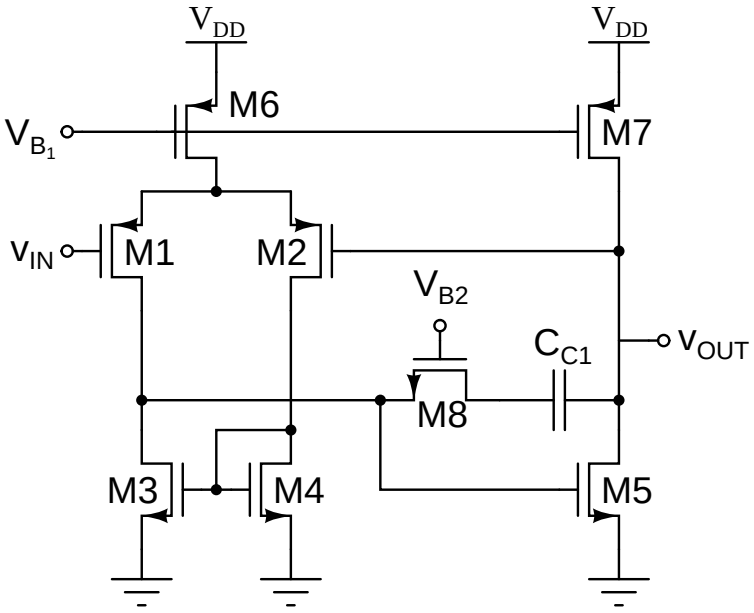
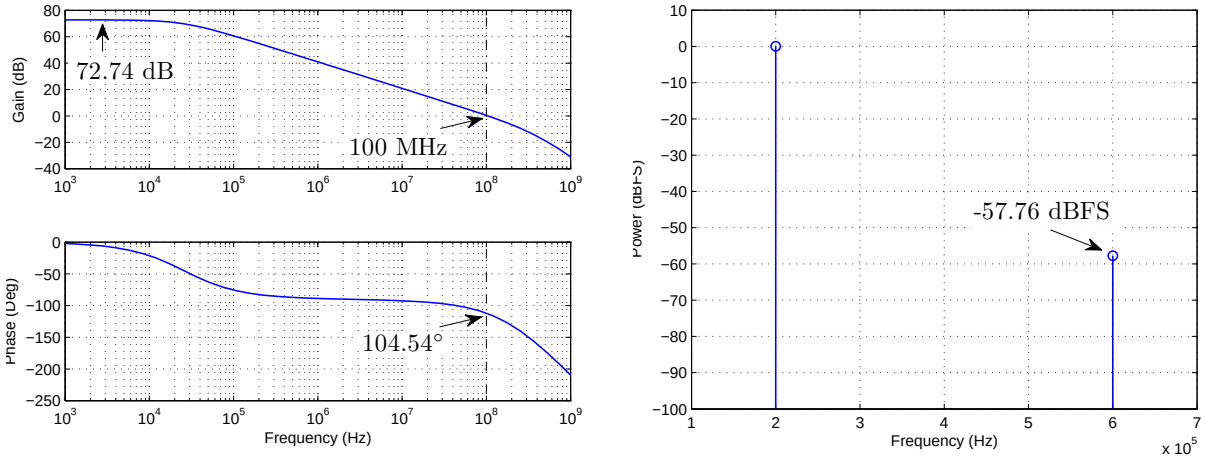


Figure 5.19: Schematic of output buffer.

Table 5.6: Output buffer transistor dimensions and bias currents.

Transistor(s)	Width	Length	Current
M1, M2	66×4 µm	0.54 µm	400 µA
M3, M4	40×1 µm	0.54 µm	400 µA
M5	80×1 µm	0.54 µm	800 µA
M6, M7	144×4 µm	0.54 µm	800 µA

oscillator.



(a) Loop Gain.

(b) Harmonic Distortion.

Figure 5.20: Output buffer bode and distortion plots.

5.3.5 Bias Circuit

The design uses a master bias circuit to provide bias currents for the entire system. The schematic of the master bias circuit is shown in Fig. 5.21 where current sources I_{B1} and I_{B2} are off-chip reference current sources. The circuit uses a low-voltage cascode topology [10] where transistors M1 and M2 bias M3 so that M4 is close to the edge of the linear region. Transistors M5 and M6 perform the same function as M1 and M2 for the PMOS cascode circuit.

Random device mismatch will limit the accuracy of the output currents generated from the master bias circuit. If transistors M4 and M7 are biased in saturation, it can be shown that the output current mismatch is approximately [60, 61]

$$\frac{\sigma\left(\Delta I_D\right)}{I_D} \approx 2\sqrt{\frac{\mu C_{\text{ox}}}{I_D}} \times \frac{A_{VT}}{L} \tag{5.15}$$

where A_{VT} is the 1σ threshold mismatch parameter and L is the length of transistor M4.

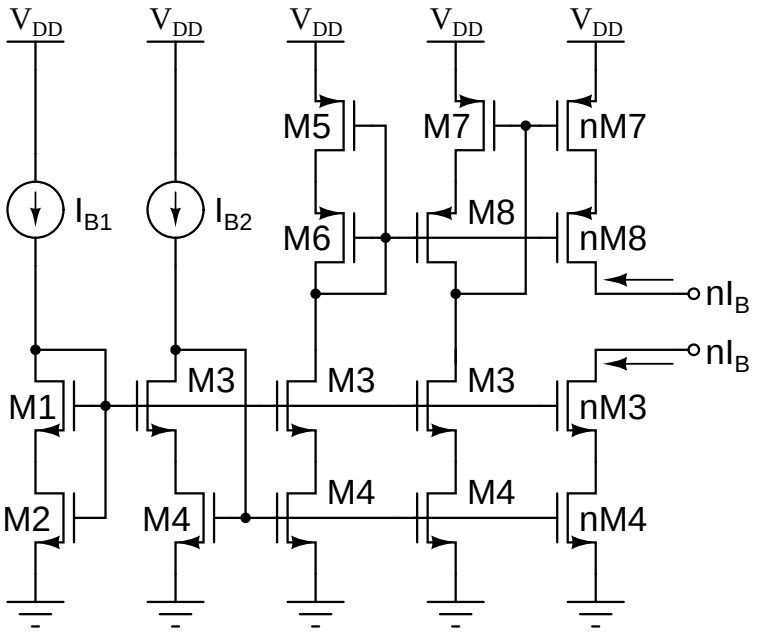


Figure 5.21: Schematic of master bias circuit.

Device mismatch in the cascode transistors M3 and M6 will have an insignificant effect on the output current mismatch. In this design, the 1σ output current mismatch should be kept under 1% ($\sigma(\Delta I_D)/I_D < 0.01$) for $I_{B1} = I_{B2} = 100\ \mu\text{A}$. For this 0.18 μm process, it is assumed that $\mu_N C_{\text{ox}} = 250\ \mu\text{A/V}^2$ and $A_{VT_N} = 5\ \text{mV}\mu\text{m}$ [60]. Using the previous information with Eq. 5.15, the minimum length for M4 is 1.58 μm. In the final circuit implementation, the length was increased to 1.8 μm to ensure that the PMOS 1σ output current mismatch is also below 1%.

The lead compensation transistors M11 M12 in Fig. 5.8 are biased using a process and temperature insensitive technique that is shown in Fig. 5.22. If the conditions

$$\frac{(W/L)_{11}}{(W/L)_3} = \sqrt{\frac{(W/L)_2}{(W/L)_1}} \tag{5.16}$$

$$\frac{I_{D1}}{(W/L)_1} = \frac{I_{D3}}{(W/L)_3} \tag{5.17}$$

are satisfied, then resistance of lead compensation transistor is inversely matched to the transconductance of the second op amp stage [5]. The same technique is used to bias the lead compensation transistor of the output buffers.

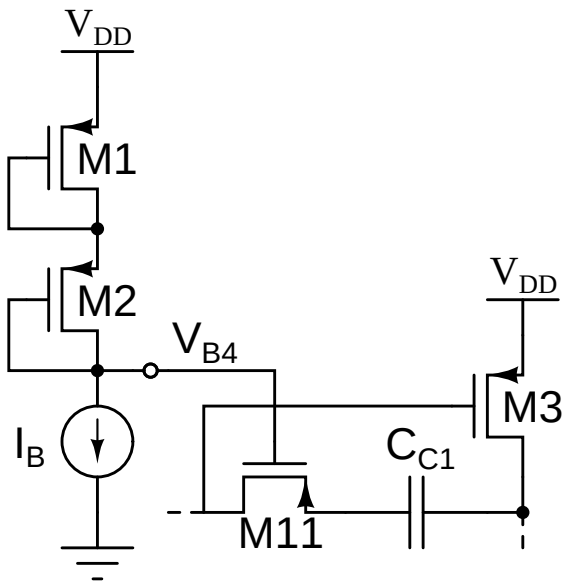
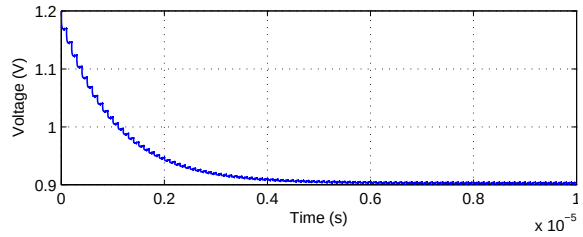


Figure 5.22: Schematic of lead compensation bias circuit.

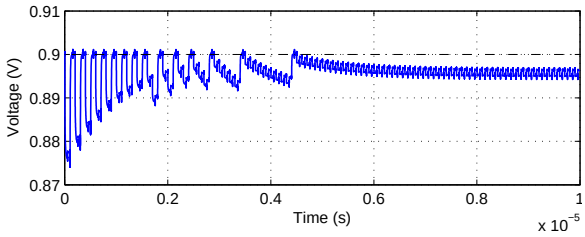
5.4 System Simulation

The entire switched-capacitor oscillator system was simulated in Cadence Spectre. Fig. 5.23 plots the input and output common mode voltages of OA_2 during the initial start-up period. Initially, the output common mode voltage is higher than the desired 0.9 V. As evident in Fig. 5.23a, the output CMFB will slowly push the output common mode voltage to the desired voltage. Any change in the output common mode will cause a proportional change

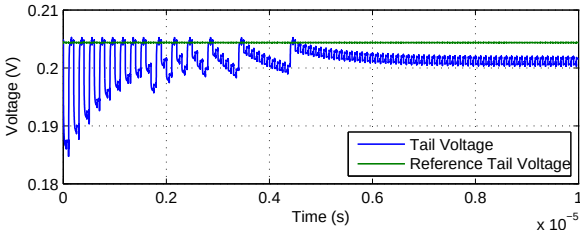
to the input common mode through feedback capacitor C_B and this is shown in Fig. 5.23b. When the input common mode moves outside a certain range, the input common mode control signal (Fig. 5.23d) switches high and resets it back to the desired voltage. The control signal becomes inactive when the common mode signals reach their desired values.



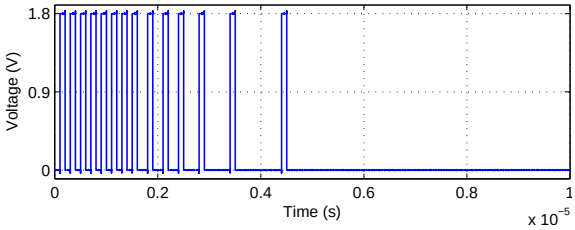
(a) Output Common Mode Voltage.



(b) Input Common Mode Voltage.



(c) Tail and Reference Voltage.



(d) Input Common Mode Control Voltage.

Figure 5.23: OA_2 common mode settling simulations.

The output of the oscillator during the start-up period is plotted in Fig. 5.24. From the figure, it is clear that the start-up circuit, discussed in Section 4.1.5, induces the oscillation in the circuit and shuts off once oscillation commences. Fig. 5.25 plots the oscillator's output after the start-up transients have settled and Fig. 5.26 plots its spectrum. The oscillator was simulated at the minimum clock frequency ($f_c = 1$ MHz). The oscillation frequency is approximately $f_c/50$ in both the multipath and conventional Miller mode. The oscillator exhibits significant overshoot in the conventional Miller mode. On the other

hand, the oscillator exhibits a first-order response in the multipath Miller mode. As the clock frequency is increased, the oscillator's quality factor is expected to degrade more predictably in the multipath Miller mode than in the conventional Miller mode.

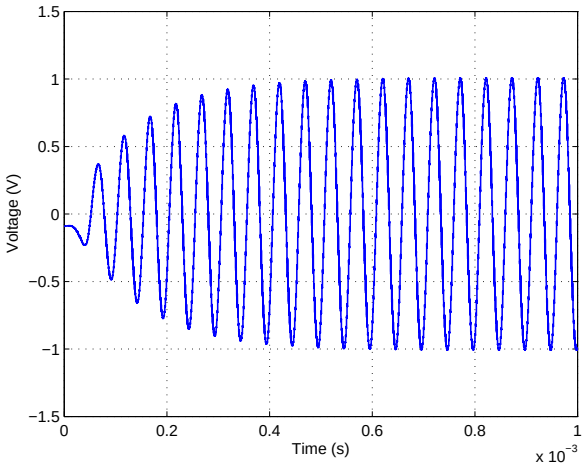
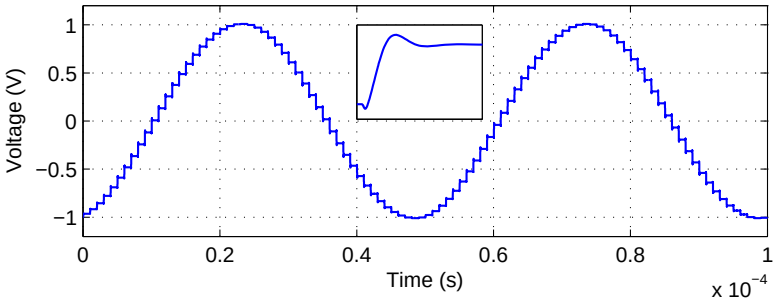
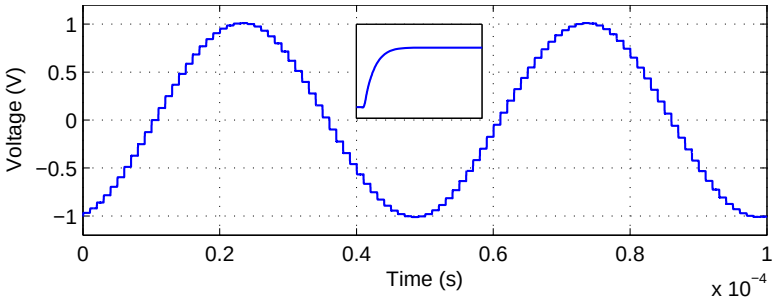


Figure 5.24: Oscillator during start-up.



(a) Conventional Miller.



(b) Multipath Miller.

Figure 5.25: Oscillator output after start-up transients have settled.

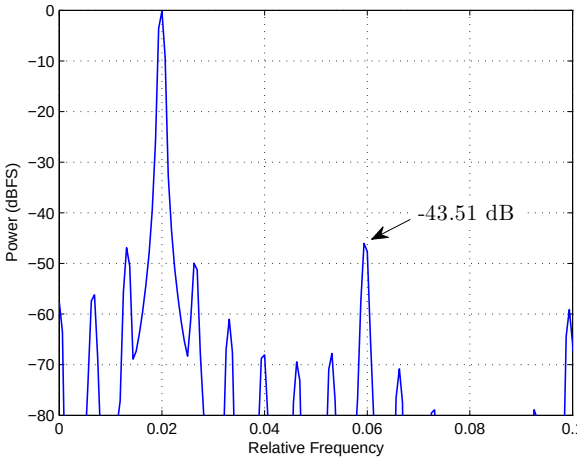


Figure 5.26: Oscillator spectrum with a 1600-point Hann window.

Chapter 6

Test Results and Improvements

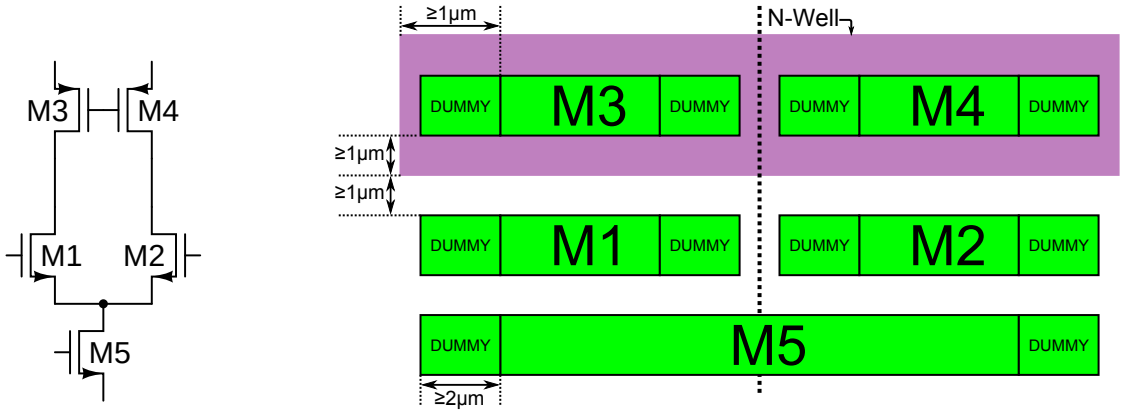
6.1 Test Results

A test chip was designed and fabricated in a 0.18 μm 1-poly-6-metal CMOS process. The purpose of the test chip was to compare the differences in 3rd-order distortion of a switched-capacitor oscillator with multipath or conventional Miller-compensated op amps. The design used the technology's mixed-signal option, which enables MIM capacitors with a density of approximately 1 fF/μm^2.

6.1.1 Layout

Matched devices, such as differential pairs in op amps, were laid out using a symmetry-at-block-level style instead of a common-centroid style. The symmetry-at-block-level layout style, as illustrated in Fig. 6.1 for a single-stage op amp, was chosen for its reduced complexity and lower interconnect capacitance compared to the common-centroid layout style.

For improving matching of sensitive devices, dummy transistors extending at least 2 µm on source/drain sides of the transistor were used to ensure uniform poly etching and to reduce stress gradients[1] caused by shallow trench isolation (STI) around the active transistors. Similarly, gates of active transistors were kept at least 1 µm apart from n-well edges to reduce well proximity effects[2]. It is expected that any residual proximity effects will be matched by using the symmetry-at-block-level layout style.



(a) Schematic. (b) Layout.

Figure 6.1: Example single-stage op amp layout using the symmetry-at-block-level style.

MIM capacitors were laid out in an array as shown in Fig. 6.2. The capacitors are constructed using integer multiples of a unit capacitor, which in this design is a 5 µm×5 µm capacitor with a 30.5 fF of capacitance [49]. The capacitors were not laid out in a common-centroid style as this was deemed unnecessarily complex. Dummy capacitors form a ring around the capacitor array to improve matching. Matching is further improved by ensuring that no devices or metal layers are placed under the MIM capacitors. It is expected that

[1]Transistors under stress will experience a shift in both mobility and threshold.

[2]Transistors close to n-well edges will experience more ion implantation, which leads a shift in both mobility and threshold

process gradients, which would have been compensated for with a common-centroid layout structure, will introduce coefficient errors in the system. Coefficient errors are not a concern in this design because the test chip is meant to compare the performance of the oscillator in the multipath or conventional Miller mode; any global errors will affect both oscillator modes equally and hence will not affect the comparison.

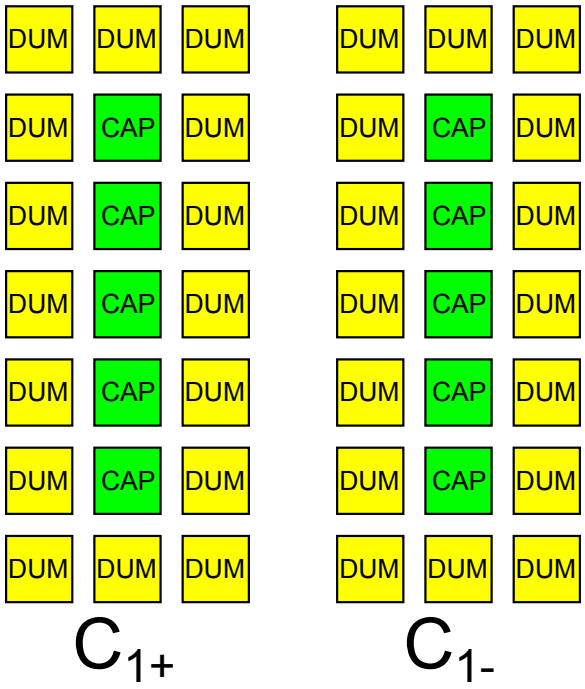


Figure 6.2: Layout of capacitor C_1 consisting of an array of unit transistors and a ring dummies.

The top-level layout of the test chip is shown in Fig. 6.3. The dimensions of the layout are 1.7 mm $\times$ 0.9 mm. The outputs of the THAs (V_{out} and V_{bp} in Fig. 5.5) are connected to pins 10, 11, 30, and 31 as they have the lowest package parasitics [59].

6.1.2 Test Board

A breadboard test setup is sufficient for testing the fabricated chip because of the chip's slow clock rate of 1-10 MHz. Two breadboards were used in the test setup. The first breadboard, shown in Fig. 6.4, generates the reference voltages for the test chip. A low-dropout regulator generates a constant 5 volts. This 5 V is stepped down through voltage dividers to generate the supply voltage (1.8 V), the common-mode voltage (0.9 V), and oscillator input voltages $V_{\text{ref}+}$ and $V_{\text{ref}-}$. Resistors R13 and R14 can be made adjustable if the common-mode voltage of $V_{\text{ref}+}$ and $V_{\text{ref}-}$ strays too far from the expected common-mode voltage. The second breadboard, shown in Fig. 6.5 contains the fabricated chip. Resistors R1 and R2 are used to generate the reference bias currents I_{B_1} and I_{B_2} for the master bias circuit. All control signals use an open collector style of logic; the control signals default to logic high (Vdd) unless pulled to logic low (ground) through a low impedance path. Clock signals are buffered locally to sharpen their edges.

6.1.3 Results

The fabricated test chip was placed in the configuration described in Section 6.1.2 and powered on. Resistors R1 and R2 in Fig. 6.5 were adjusted until the expected bias currents were supplied to the test chip. Table 6.1 describes the expected and measured bias voltages of the master bias circuit.

The analog current consumption of the test chip can be found in Table 6.2. The measurements were performed by turning off the clock signals and applying the appropriate power down signals. With the clock signals enabled, voltage spikes at the clock frequency were observed on the positive supply.

Table 6.1: Expected and measured bias voltages.

Voltage	Expected Voltage	Measure Voltage
$\mathbf{V_{B_1}}$	0.99 V	1.03 V
$\mathbf{V_{B_2}}$	0.61 V	0.64 V

Table 6.2: Expected and measured analog current consumption.

Block	Expected Current	Measured Current
Amplifiers	10.06 mA	10.10 mV
Comparator	1.20 mA	1.64 mV
Total	11.26 mA	11.74 mA

The output resistance of the track-and-hold amplifiers were measured to be 67.8 Ω, which indicates that the THAs are operating correctly. Unfortunately, it was not possible to obtain additional measurement results. It is believed that the lack of electrostatic discharge (ESD) protection and the disregard of latch-up prevention guidelines [62] in the layout led to problems that limited the ability to further evaluate the circuit.

6.2 Improvements

A number of ways to improve the design were noted during the design process. Due to time and layout area constraints, it was not possible for these improvements to be incorporated in the first prototype chip.

6.2.1 Electrostatic Discharge and Latchup

Integrated circuit transistors, especially the gate oxide of MOSFETs, are extremely sensitive to electrostatic discharge. Without the necessary precautions, ESD can cause irreversible damage to unprotected transistors. Hence, ESD protection devices, such as ESD diodes and silicon-controlled rectifiers (SCRs), should be placed at all chip pads. Alternatively, pads with built-in ESD protection can be used in place of the existing non-ESD pads.

Latchup is a failure mechanism in CMOS processes where a low-impedance path between the positive and negative supply rails is created by parasitic BJTs (bipolar junction transistors) [12]. Circuits with voltages outside the supply rails or with PMOS transistors where the N-well is not connected directly to the positive supply rail are especially sensitive to latchup. The foundry's recommended layout guidelines on latchup should be followed to ensure the design is protected from latchup.

6.2.2 Decoupling Capacitors

Wherever there is space, decoupling capacitors should be placed on all DC signal lines. Signals reference to the positive supply, such as bias voltages for PMOS transistors, should be decoupled to the positive supply and signals referenced to the negative supply should be decoupled to the negative supply. This ensures that noise, clock signals, and spurious tones are not coupled to important parts of the system. The decoupling capacitors can be created by overlapping MOSFET and MIM capacitors on top of each other, where the former occupies the bottom metal layers and the latter occupies the top metal layers.

6.2.3 Analog Multiplexers

Analog multiplexers provide a pin-efficient method of probing bias signals inside the chip. Fig. 6.6 shows a possible implementation of this block. The decoder block converts the binary-coded input into an one-hot coded signal where only a single bit is high at a time. The switches should be implemented as T-switches to improve high-frequency input-output isolation when the switches are off.

6.2.4 Power and Area

The primary objective of the design was to investigate the advantages of the multipath Miller-compensation technique, hence power efficiency was not optimized. A power-efficient design reduces die area and this is attractive in many aspects. Firstly, manufacturing costs are lowered with a reduced die area. Secondly, component mismatch due to silicon gradients are reduced. Finally, layout is simplified which will reduce signal skew and parasitics.

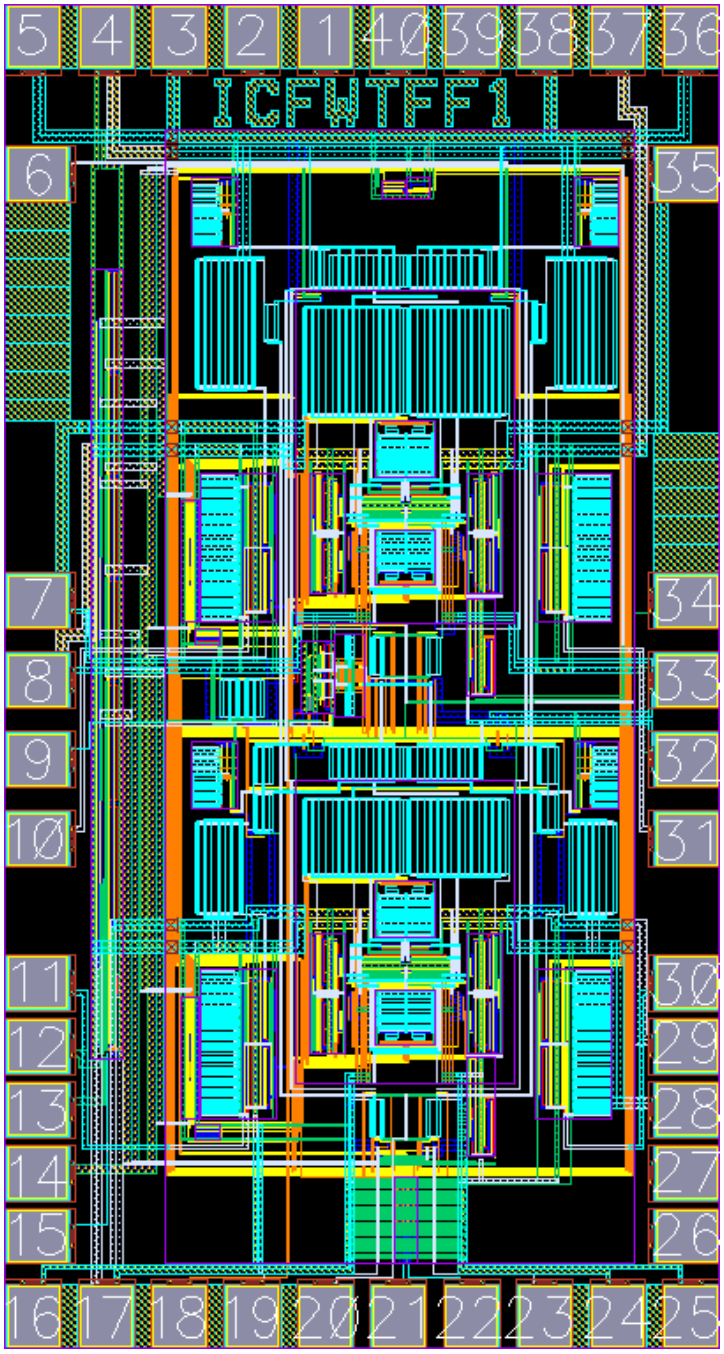


Figure 6.3: Test chip top-level layout.

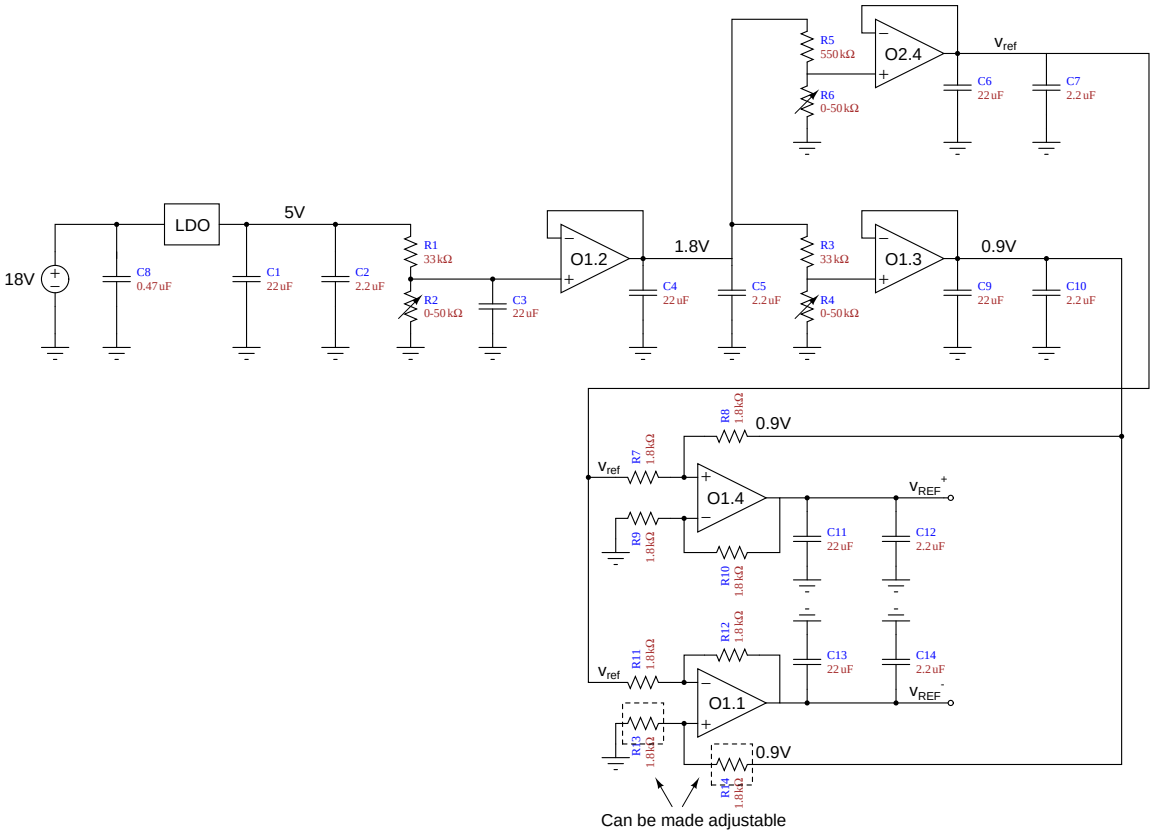


Figure 6.4: Test board for generating reference voltages.

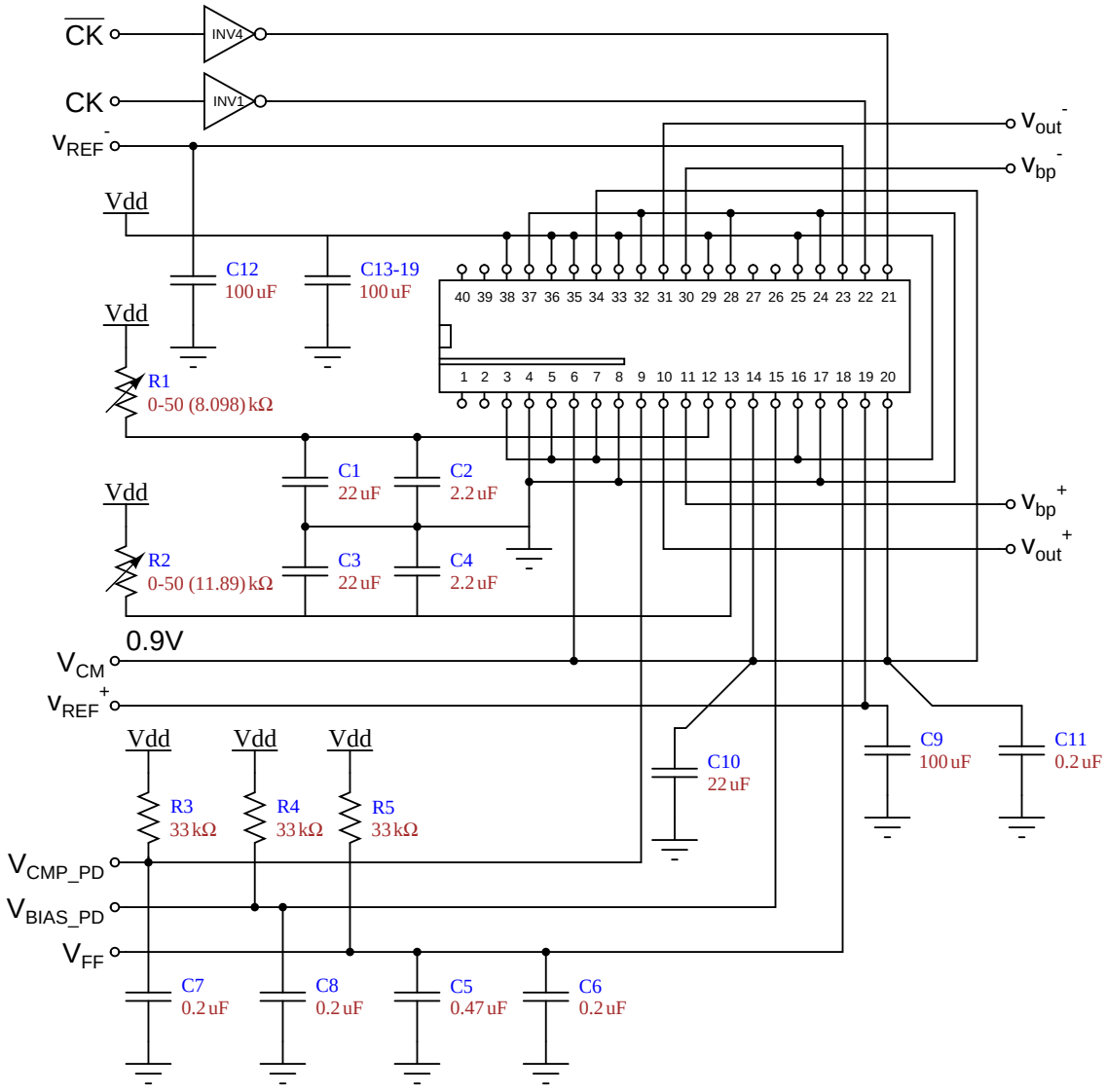


Figure 6.5: Test board for testing the fabricated chip.

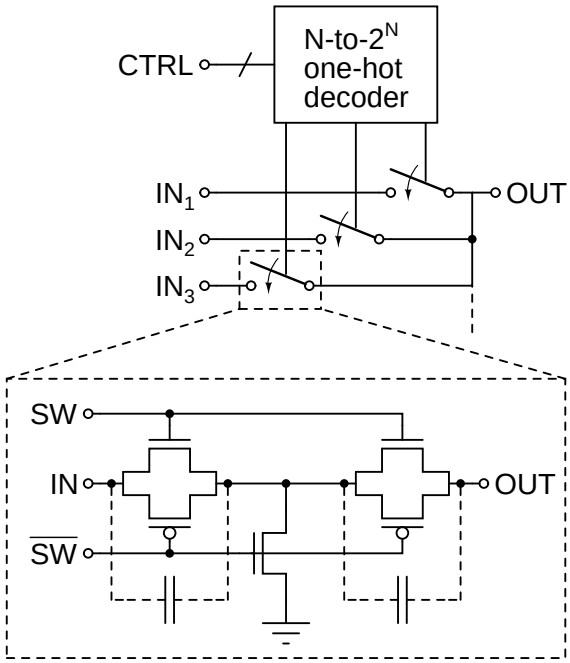


Figure 6.6: Schematic of an analog multiplexer with T-switches.

Chapter 7

Conclusions

A two-stage Miller-based op amp compensation topology incorporating a feedforward path was investigated. For the same DC gain, gain-bandwidth product, area, and power consumption, an op amp with the multipath Miller-compensation scheme was demonstrated to have improved closed-loop settling response over an op amp with conventional Miller-compensation. When high-order designs are considered, an op amp compensated with multipath Miller can achieve a higher maximum gain-bandwidth product than with conventional Miller-compensation because the latter must ensure that its gain-bandwidth product is a factor lower than its non-dominant poles. A test chip with multipath Miller-compensated op amps was designed, laid out, and fabricated in a 0.18 μm CMOS process.

In Chapter 3 it was shown that a two-stage multipath Miller-compensated op amp has a lower settling time for similar power consumption as compared to an op amp with conventional Miller-compensation at low phase margins. At high phase margins for the conventional Miller-compensated op amp, the op amp with multipath Miller-compensation will require less power for the same settling time. Two-stage multipath Miller-compensated

op amps can be implemented without consuming additional area and power compared to conventional Miller-compensated op amps. However, the former can have a significantly higher output slew rate and will exhibit lower noise depending on the design.

In Chapter 4, it was determined that third-order harmonics of a switched-capacitor oscillator, consisting of a second-order biquad filter and a comparator, is a determined by the quality factor of the system. Subsequent analysis has shown that the quality factor of oscillation is primarily determined by closed-loop settling response of the op amps. As shown in Chapter 5, the quality of oscillation for the oscillator with multipath Miller-compensated op amps is indeed better than the same oscillator with conventional Miller-compensated op amps at higher clock frequencies.

7.1 Contributions

Multipath Miller-compensation with lead compensation for the purpose of pole-zero cancellation was introduced in this dissertation. Unlike conventional pole splitting techniques, this topology stabilizes a closed-loop system without limiting an op amp's gain-bandwidth product. Compared with past pole-zero cancellation techniques, the new technique provides a closed-loop settling response that is insensitive to process, temperature, and voltage variations. Furthermore, the lead compensation resistor relaxes the amount of feedforward transconductance necessary for pole-zero cancellation.

An improvement to the switched-capacitor oscillator by [46] was presented. The modified system has the same transfer function as the original implementation but is less sensitive to finite op amp bandwidth. An input common-mode adjustment circuit was introduced. This feedback system can correct the input common-mode voltage of a switched-capacitor integrator without having to reset the integrator.

7.2 Future Work

The advantages of multipath Miller-compensation over conventional Miller-compensation can be demonstrated in a more complex switched-capacitor system such as a pipeline ADC or a $\Delta\Sigma$ modulator. Since the accuracy of these converters is determined by the performance of its op amps, the advantages of multipath Miller-compensation can be directly ascertained by the relative accuracy of the system. Op amps stabilized with multipath Miller-compensation should also be investigated in continuous-time systems. Although the op amp closed-loop settling response is not crucial to the performance of these systems, the first-order response multipath Miller-compensated op amps may lead to other benefits such as improved or more predictable system behaviour.

Design strategies of higher order multipath Miller-compensated op amps can also be investigated. With more than two transconductance stages, a designer has the choice of using a nested or reverse-nested topology for realizing multi-stage op amps. Furthermore, a number of hybrid topologies, where the nested and reverse-nested topologies are combined, may also provide benefits to specific applications.

APPENDICES

Appendix A

Derivation of Multipath Miller Transfer Function

Fig. A.1 shows the block diagram of a two-stage multipath Miller-compensated op amp with lead compensation. The small signal model of this op amp is shown in Fig. A.2. Applying Kirchhoff's current law (KCL) at nodes 1 and 2 results in

$$g_{m_1} v_{\text{in}} + \frac{v_{\text{x}}}{r_{o_1}} = (v_{\text{out}} - v_{\text{x}}) \frac{s g_{m_2} C_{C_1}}{s C_{C_1} + g_{m_2}} \tag{A.1}$$

$$g_{m_3} v_{\text{in}} = \frac{s g_{m_2} C_{C_1} (v_{\text{out}} - v_{\text{x}})}{s C_{C_1} + g_{m_2}} + g_{m_2} v_{\text{x}} + \frac{v_{\text{out}}}{r_{o_2}} + s C_L v_{\text{out}} \tag{A.2}$$

Isolating for v_{x} in Eq. A.2 yields

$$v_{\text{x}} = \frac{g_{m_3} v_{\text{in}}}{g_{m_2} \left(1 - \frac{s C_{C_1}}{s C_{C_1} + g_{m_2}}\right)} - \frac{v_{\text{out}} \left(s C_L + \frac{1}{r_{o_2}} + \frac{s C_{C_1} g_{m_2}}{s C_{C_1} + g_{m_2}}\right)}{g_{m_2} \left(1 - \frac{s C_{C_1}}{s C_{C_1} + g_{m_2}}\right)} \tag{A.3}$$

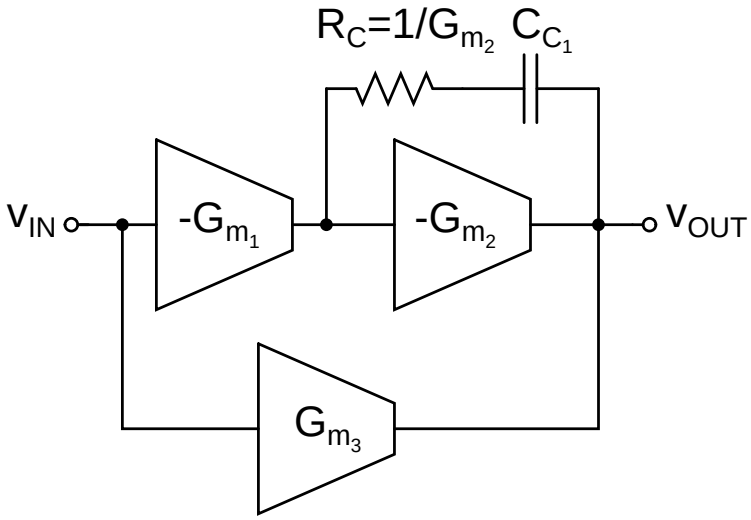


Figure A.1: Block digram of a two-stage multipath Miller-compensated op amp with lead compensation.

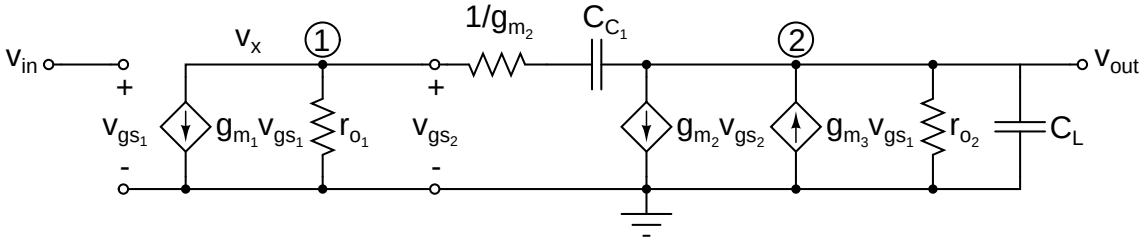


Figure A.2: Small signal digram of a two-stage multipath miller compensated op amp with lead compensation.

Substituting Eq. A.2 into Eq. A.1 yields

$$\left[\frac{-g_{m_3}v_{\text{in}}}{g_{m_3}\left(1-\frac{sC_{C_1}}{sC_{C_1}+g_{m_2}}\right)}+\frac{v_{\text{out}}\left(sC_L+\frac{1}{r_{o_2}}+\frac{sC_{C_1}g_{m_2}}{sC_{C_1}+g_{m_2}}\right)}{g_{m_2}\left(1-\frac{sC_{C_1}}{sC_{C_1}+g_{m_2}}\right)}\right]\left(\frac{g_{m_2}sC_{C_1}}{sC_{C_1}+g_{m_2}}+\frac{1}{r_{o_1}}\right)$$
$$=g_{m_1}v_{\text{in}}-\frac{v_{\text{out}}\left(g_{m_2}sC_{C_1}\right)}{sC_{C_1}+g_{m_2}} \quad \text{(A.4)}$$

where Eq. A.4 simplifies to

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{g_{m_1}g_{m_2}r_{o_1}r_{o_2}+sg_{m_3}C_{C_1}r_{o_1}r_{o_2}+s\frac{g_{m_3}}{g_{m_2}}C_{C_1}r_{o_2}+g_{m_3}r_{o_3}}{sC_{C_1}g_{m_2}\left(1-\frac{sC_{C_1}}{sC_{C_1}+g_{m)2}}\right)r_{o_1}r_{o_2}+sC_{C_1}r_{o_1}\left(sC_Lr_{o_2}+1+\frac{sC_{C_1}g_{m_2}r_{o_2}}{sC_{C_1}+g_{m_2}}\right)+\left(sC_Lr_{o_2}+1+\frac{sC_{C_1}g_{m_2}r_{o_2}}{sC_{C_1}+g_{m_2}}\right)\left(\frac{sC_{C_1}}{g_{m_2}}+1\right)} \tag{A.5}$$

The location of the poles do not change with the introduction of the feedforward amplifier. Hence, the poles of Eq. A.5 will be identical to the poles of the conventional two-stage Miller-compensated op amp with lead compensation [5, 10]. The numerator of Eq. A.5 can be rewritten as

$$Z(s) = g_{m_1}g_{m_2}r_{o_1}r_{o_2}\left(1+\underbrace{\frac{g_{m_3}}{g_{m_1}g_{m_2}r_{o_1}}}_{\text{small}}+s\left(\frac{g_{m_3}C_{C_1}}{g_{m_1}g_{m_2}}+\underbrace{\frac{g_{m_3}C_{C_1}}{g_{m_1}g_{m_2}^2r_{o_1}}}_{\text{small}}\right)\right) \tag{A.6}$$

By eliminating the small terms in Eq. A.6, the numerator of Eq. A.5 is approximately

$$Z(s) \approx g_{m_1}g_{m_2}r_{o_1}r_{o_2}\left(1+s\left(\frac{g_{m_3}C_{C_1}}{g_{m_1}g_{m_2}}\right)\right) \tag{A.7}$$

Appendix B

Derivation of Effective Gain Equation

The DC transfer function for the simple inverting amplifier shown in Fig. B.1a is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{C_{\text{I}}/C_{\text{F}}}{1+\frac{1+C_{\text{I}}/C_{\text{F}}}{A_0}} \tag{B.1}$$

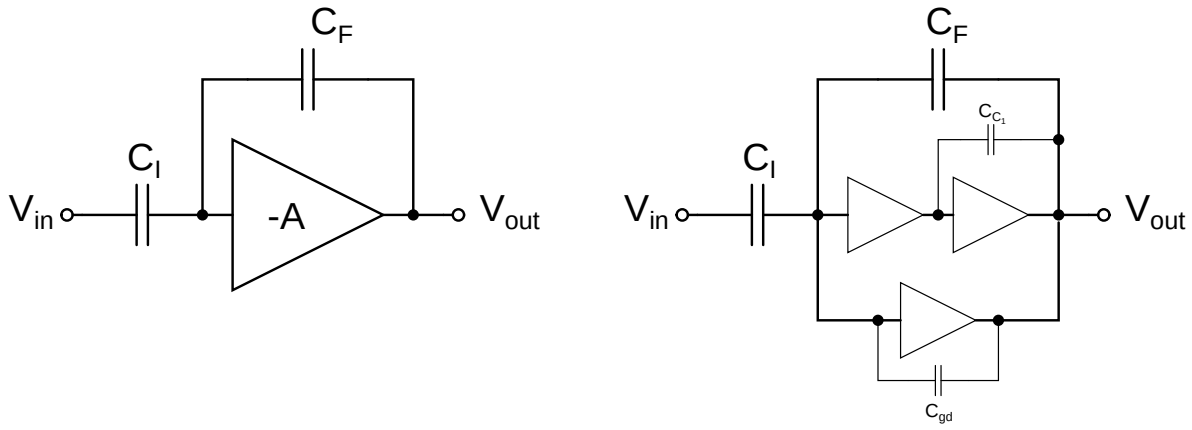
When the op amp is replaced with a second-order multipath miller op amp, as shown in Fig. B.1b, the parasitic gate-to-drain capacitor C_{gd} of the feedforward amplifier will reduce the DC transfer function to

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{C_{\text{I}}/C_{\text{F}}}{1+\frac{1+C_{\text{I}}/\left(C_{\text{F}}+C_{gd}\right)}{A_0}} \tag{B.2}$$

The change in the DC transfer function caused by C_{gd} can be mapped to a reduction in the op amp gain, A, in Eq. B.1 with the equality

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{C_{\text{I}}/C_{\text{F}}}{1+\frac{1+C_{\text{I}}/C_{\text{F}}}{\alpha A_0}} = -\frac{C_{\text{I}}/C_{\text{F}}}{1+\frac{1+C_{\text{I}}/\left(C_{\text{F}}+C_{gd}\right)}{A_0}} \tag{B.3}$$

where α is the effective gain loss due to C_{gd}.



(a) Inverting Amplifier.

(b) Inverting Multipath Miller Amplifier.

Figure B.1: Block diagrams of iGDnverting amplifiers.

Eq. B.3 can be approximated by its first-order Maclaurin series as

$$\frac{C_{\mathrm{I}}}{C_{\mathrm{F}}}\left(1-\frac{1+C_{\mathrm{I}}/C_{\mathrm{F}}}{\alpha A_0}\right)\approx\frac{C_{\mathrm{I}}}{C_{\mathrm{F}}+C_{gd}}\left(1-\frac{1+C_{\mathrm{I}}/\left(C_{\mathrm{F}}+C_{gd}\right)}{A_0}\right) \tag{B.4}$$

By expanding and collecting similar terms, the Eq. B.4 can be simplified to

$$\frac{1}{\alpha}\approx A_0\left(\frac{C_{\mathrm{F}}}{C_{\mathrm{F}}+C_{\mathrm{I}}}\right)\left(\frac{C_{gd}}{C_{\mathrm{F}}+C_{gd}}\right)+\underbrace{\left(\frac{C_{\mathrm{F}}}{C_{\mathrm{F}}+C_{gd}}\right)^2\left(\frac{C_{\mathrm{F}}+C_{\mathrm{I}}+C_{gd}}{C_{\mathrm{F}}+C_{\mathrm{I}}}\right)}_{\approx 1} \tag{B.5}$$

Since C_{gd} is usually small compared to C_F, the second term on the right-side of the above equality is approximately 1. With $\beta = C_{\mathrm{F}}/\left(C_{\mathrm{F}}+C_{\mathrm{I}}\right)$, Eq. B.5 becomes

$$\frac{1}{\alpha}\approx 1+A_0\beta\left(\frac{C_{gd}}{C_{\mathrm{F}}+C_{gd}}\right)=1+L_{g,0}\left(\frac{C_{gd}}{C_{\mathrm{F}}+C_{gd}}\right) \tag{B.6}$$

and hence α is

$$\alpha\approx\frac{1}{1+L_{g,0}\left(\frac{C_{gd}}{C_{\mathrm{F}}+C_{gd}}\right)} \tag{B.7}$$

Appendix C

Derivation of Output Noise

The noise bandwidth of a second order low-pass transfer function with a right-half plane zero is given by [63]

$$\int_0^\infty \left| \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_0 Q}+\frac{s^2}{\omega_0^2}} \right|^2 df = \frac{\omega_0 Q}{4}\left(1+\frac{\omega_0^2}{\omega_z^2}\right) \tag{C.1}$$

where ω_0 is the undamped pole frequency, Q is the quality factor, and ω_z is the zero frequency.

C.1 Two-Stage Conventional Miller-Compensated Op Amps

Fig. C.1 shows the circuit diagram of a two-stage conventional Miller-compensated op amp. The transistors are assumed to have infinite output resistance ($r_o = \infty$) and the effects of the Miller capacitor is assumed to be unilateral (i.e. the Miller zero is neglected). The

small-signal noise model of this op amp is shown in Fig. C.2 where $\overline{v_{out}}$ is the output noise spectral density.

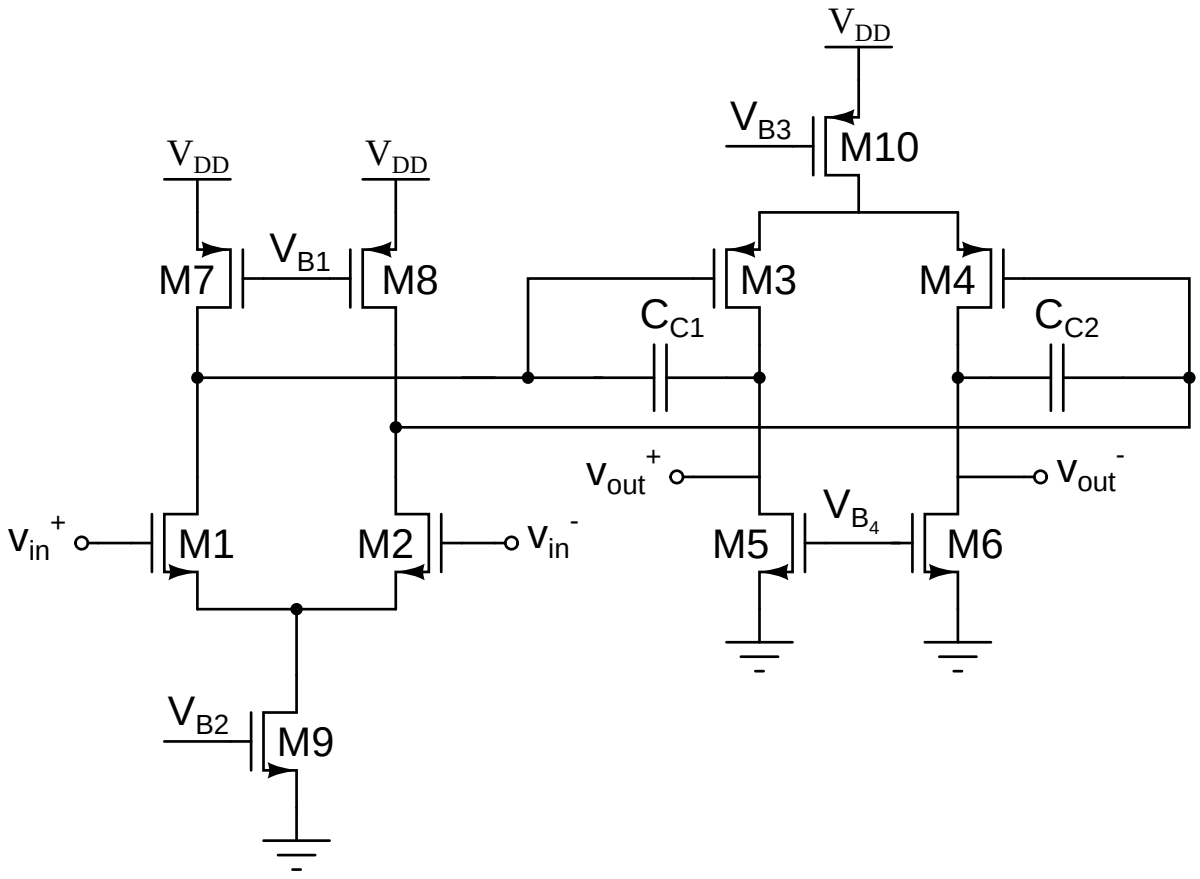


Figure C.1: Circuit digram of a two-stage conventional Miller-compensated op amp.

The nodal equation describing the noise in the first op amp stage is

$$\overline{v_{\text{in}}} = \overline{v_{\text{out}}} + \frac{\overline{i_{n_1}}}{sC_{C_1}} + \beta\frac{g_{m_1}\overline{v_{\text{out}}}}{sC_{C_1}} \tag{C.2}$$

The nodal equation describing the noise in the second op amp stage is

$$\overline{v_{\text{out}}}s\left(C_{C_1} + C_L\right) = -g_{m_3}\overline{v_{\text{in}}} + \overline{i_{n_2}} \tag{C.3}$$

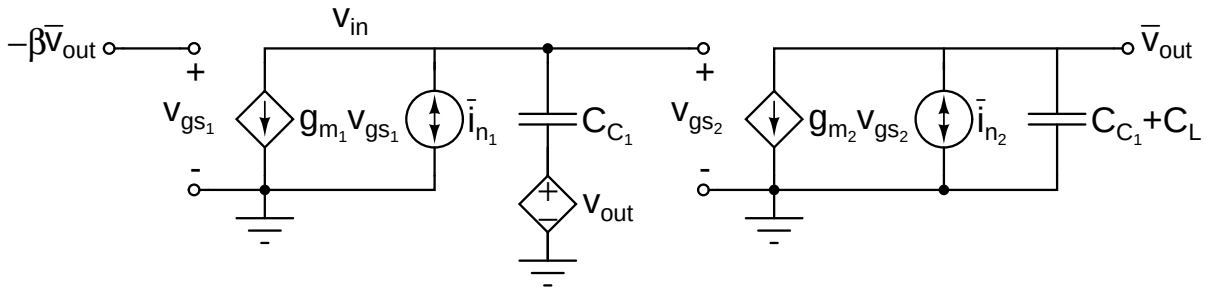


Figure C.2: Small-signal noise model a two-stage conventional Miller-compensated op amp.

The noise currents, i_{n_1} and i_{n_2}, are

$$\overline{i_{n_1}} = \sqrt{8kT\gamma g_{m_1}\left(1+\frac{g_{m_7}}{g_{m_1}}\right)\Delta f} \tag{C.4}$$

$$\overline{i_{n_2}} = \sqrt{8kT\gamma g_{m_3}\left(1+\frac{g_{m_5}}{g_{m_3}}\right)\Delta f} \tag{C.5}$$

where k is the Boltzmann constant, T the is temperature in kelvin, and γ is the effective channel resistance, which is approximately 2/3. Substituting Eq. C.2 into Eq. C.3 yields

$$\overline{v_{\text{out}}} = \frac{\overline{i_{n_1}}}{\beta g_{m_1}} \frac{1+s\frac{\overline{i_{n_2}}C_{C_1}}{\overline{i_{n_1}}g_{m_3}}}{1+s\frac{C_{C_1}}{\beta g_{m_1}}+s^2\frac{\left(C_{C_1}+C_L\right)C_{C_1}}{\beta g_{m_1}g_{m_3}}} \tag{C.6}$$

where

$$\omega_0^2 = \frac{\beta g_{m_1}g_{m_3}}{\left(C_{C_1}+C_L\right)C_{C_1}} \tag{C.7}$$

$$\omega_0 Q = \frac{\beta g_{m_1}}{C_{C_1}} \tag{C.8}$$

$$\omega_z = \frac{\overline{i_{n_1}}g_{m_3}}{\overline{i_{n_2}}C_{C_1}} \tag{C.9}$$

Substituting Eq. C.7–C.9 into Eq. C.1 yields a noise bandwidth of

$$\text{NBW} = \frac{\beta g_{m_1}}{4C_{C_1}}\left(1+\frac{\beta C_{C_1}\left(1+\frac{g_{m_5}}{g_{m_3}}\right)}{\left(C_{C_1}+C_L\right)\left(1+\frac{g_{m_7}}{g_{m_1}}\right)}\right) \tag{C.10}$$

Hence the total output noise power is

$$\begin{aligned}\overline{v_{\text{out}_{\text{tot}}}^2} &= \frac{\overline{i_{n_1}^2}}{\beta^2 g_{m_1}^2} \times \text{NBW} \\ \overline{v_{\text{out}_{\text{tot}}}^2} &= \frac{2kT\gamma\left(1+\frac{g_{m_7}}{g_{m_1}}\right)}{\beta C_{C_1}}\left(1+\frac{\beta C_{C_1}\left(1+\frac{g_{m_5}}{g_{m_3}}\right)}{\left(C_{C_1}+C_L\right)\left(1+\frac{g_{m_7}}{g_{m_1}}\right)}\right)\end{aligned} \tag{C.11}$$

C.1.1 Two-Stage Multipath Miller-Compensated Op Amps

Fig. C.3 shows the circuit diagram of a two-stage multipath Miller-compensated op amp. Again, the transistors are assumed to have infinite output resistance and the effects of the Miller capacitor is assumed to be unilateral. The small-signal noise model of this op amp is shown in Fig. C.4.

The nodal equation describing the noise in the first op amp stage is

$$\overline{v_{\text{in}}} = \overline{v_{\text{out}}} + \frac{\overline{i_{n_1}}}{sC_{C_1}} + \beta\frac{g_{m_1}\overline{v_{\text{out}}}}{sC_{C_1}} \tag{C.12}$$

The nodal equation describing the noise in the second op amp stage is

$$\overline{v_{\text{out}}}s\left(C_{C_1}+C_L\right) = -g_{m_3}\overline{v_{\text{in}}} - \beta g_{m_5}\overline{v_{\text{out}}} + \overline{i_{n_2}} \tag{C.13}$$

Substituting Eq. C.12 into Eq. C.13 yields

$$\overline{v_{\text{out}}} = \frac{\overline{i_{n_1}}}{\beta g_{m_1}}\frac{1+s\frac{\overline{i_{n_2}}C_{C_1}}{\overline{i_{n_1}}g_{m_3}}}{1+s\frac{C_{C_1}\left(1+\frac{\beta g_{m_5}}{g_{m_3}}\right)}{\beta g_{m_1}}+s^2\frac{\left(C_{C_1}+C_L\right)C_{C_1}}{\beta g_{m_1}g_{m_3}}} \tag{C.14}$$

where

$$\omega_0^2 = \frac{\beta g_{m_1}g_{m_3}}{\left(C_{C_1}+C_L\right)C_{C_1}} \tag{C.15}$$

$$\omega_0 Q = \frac{\beta g_{m_1}}{C_{C_1}\left(1+\frac{\beta g_{m_5}}{g_{m_3}}\right)} \tag{C.16}$$

$$\omega_z = \frac{\overline{i_{n_1}}g_{m_3}}{\overline{i_{n_2}}C_{C_1}} \tag{C.17}$$

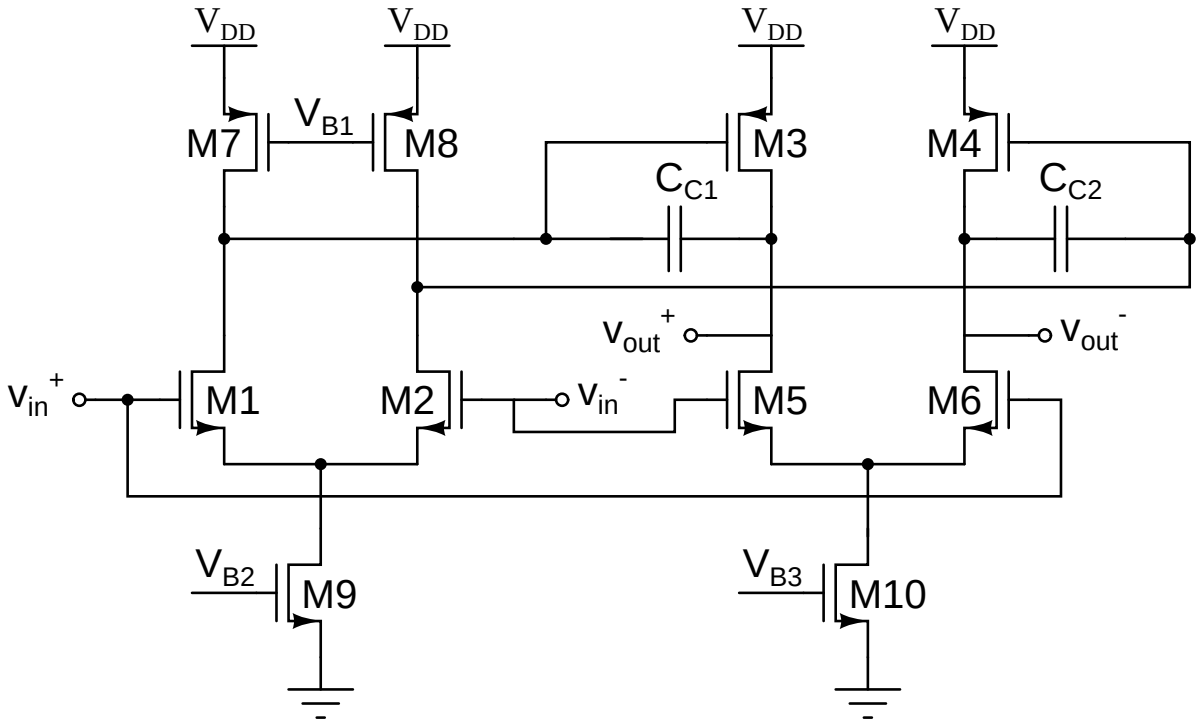


Figure C.3: Circuit digram of a two-stage multipath Miller-compensated op amp.

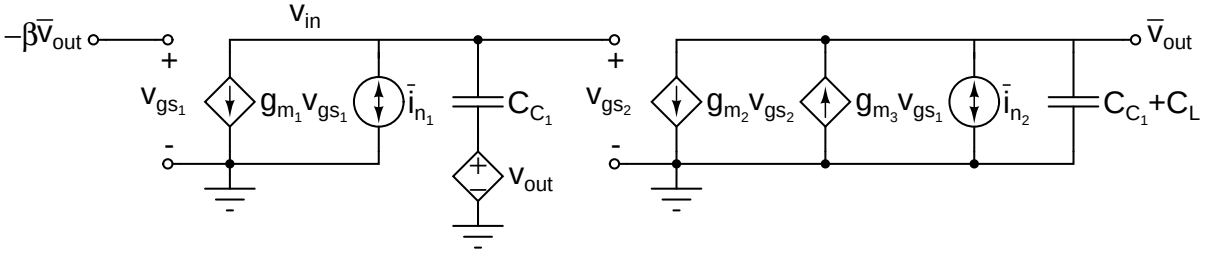


Figure C.4: Small-signal noise model a two-stage multipath Miller-compensated op amp.

Substituting Eq. C.15–C.17 into Eq. C.1 yields a noise bandwidth of

$$\text{NBW} = \frac{\beta g_{m_1}}{4C_{C_1}\left(1+\frac{\beta g_{m_5}}{g_{m_3}}\right)}\left(1+\frac{\beta C_{C_1}\left(1+\frac{g_{m_5}}{g_{m_3}}\right)}{(C_{C_1}+C_L)\left(1+\frac{g_{m_7}}{g_{m_1}}\right)}\right) \tag{C.18}$$

Hence the total output noise power is

$$\begin{aligned}
\overline{v_{\text{out}_{\text{tot}}}^2} &= \frac{\overline{i_{n_1}^2}}{\beta^2 g_{m_1}^2} \times \text{NBW} \\
\overline{v_{\text{out}_{\text{tot}}}^2} &= \frac{2kT\gamma\left(1+\frac{g_{m_7}}{g_{m_1}}\right)}{\beta C_{C_1}\left(1+\frac{\beta g_{m_5}}{g_{m_3}}\right)}\left(1+\frac{\beta C_{C_1}\left(1+\frac{g_{m_5}}{g_{m_3}}\right)}{(C_{C_1}+C_L)\left(1+\frac{g_{m_7}}{g_{m_1}}\right)}\right)
\end{aligned} \tag{C.19}$$

References

[1] D. G. Nairn, "A 10-bit, 3v, 100ms/s pipelined adc," in *Proc. IEEE Custom Integrated Circuits Conf.*, (Orlando, Florida), pp. 257–260, May 2000.

[2] P. Malcovati, L. Picolli, L. Crespi, F. Chaahoub, and A. Baschirotto, "A 90-nm cmos, 8-bit pipeline adc with 60-mhz bandwidth and 125-ms/s or 250-ms/s sampling frequency," *Analog Integr. Circ. Sig. Process.*, vol. 64, pp. 159–172, December 2009.

[3] S. H. Lewis, H. S. Fetterman, G. F. Gross Jr., R. Ramachandran, and T. R. Viswanathan, "A 10-b 20-msample/s analog-to-digital coverter," *IEEE J. Solid-State Circuits*, vol. 27, pp. 351–358, March 1992.

[4] P. R. Gray and R. G. Meyer, "Mos operational amplifier design – a tutorial overview," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 969–982, December 1982.

[5] D. Johns and K. Martin, *Analog Integrated Circuit Design.* Hoboken, New Jersey: John Wiley & Sons, Inc., 1996.

[6] A. S. Sedra and K. C. Smith, *Microelectronic Circuits.* New York City, New York: Oxford University Press, fifth ed., 2004.

[7] D. G. Nairn, "Relating op amp specs to system specs," in *ECE 636 Analog MOS and Bipolar Integrated Circuits*, University of Waterloo, October 2009.

[8] R. C. Dorf and R. H. Bishop, *Modern Control Systems*. Reading, Massachusetts: Addison-Wesley Publishing Company, seventh ed., 1995.

[9] K. Warwick, *An Introduction to Control Systems*. Singapore: World Scientific Publishing Co. Pte. Ltd., second ed., 1996.

[10] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. Hoboken, New Jersey: John Wiley & Sons, Inc., fourth ed., 2001.

[11] K. Bult and G. J. G. M. Geelen, "A fast-settling cmos op amp for sc circuits with 90-db dc gain," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1379–1384, December 1990.

[12] B. Razavi, *Design of Analog CMOS Integrator Circuits*. New York City, New York: McGraw-Hill, 2001.

[13] S. Devarajan, L. Singer, D. Kelly, S. Decker, A. Kamath, and P. Wilkins, "A 16-bit, 125 ms/s, 385 mw, 78.7 db snr cmos pipeline adc," *IEEE J. Solid-State Circuits*, vol. 44, pp. 3305–3313, December 2009.

[14] A. Panigada and I. Galton, "A 130 mw 100 ms/s pipelined adc with 69 db sndr enabled by digital harmonic distortion correction," *IEEE J. Solid-State Circuits*, vol. 44, pp. 3314–3328, December 2008.

[15] C. T. Peach, U.-K. Moon, and D. J. Allstot, "An 11.1 mw 42 ms/s 10 b adc with two-step settling in 0.18 /*mu*m cmos," *IEEE J. Solid-State Circuits*, vol. 45, pp. 391–400, February 2010.

[16] A. M. A. Ali, A. Morgan, C. Dillon, G. Patterson, P. Scott, P. Bhoraskar, H. Dinc, M. Hensley, R. Stop, S. Bardsley, D. Lattimore, J. Bray, C. Speir, and R. Sneed, "A 16b 250-ms/s if sampling pipelined adc converter with background calibration," *IEEE J. Solid-State Circuits*, vol. 45, pp. 2602–2612, December 2010.

[17] J. E. Solomon, "The monolithic op amp: A tutorial study," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 314–332, December 1974.

[18] H. C. Yang and D. J. Allstot, "Considerations for fast settling operational amplifiers," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 326–334, March 1990.

[19] Y. P. Tsividis and P. R. Gray, "An integrated nmos operational amplifier with internal compensation," *IEEE J. Solid-State Circuits*, vol. SC-11, pp. 748–753, December 1976.

[20] D. Senderowicz, D. A. Hodges, and P. R. Gray, "High-performance nmos operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 760–766, December 1978.

[21] W. C. Black Jr., D. J. Allstot, and R. A. Reed, "A high performance low power cmos channel filter," *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 929–938, December 1980.

[22] B. K. Ahuja, "An improved frequency compensation technique for cmos operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 629–633, December 1983.

[23] R. G. Eschauzier and J. H. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*. Dordrecht, The Netherlands: Kluwer Academic Publishers, 1995.

[24] R. Hogervorst and J. H. Huijsing, *Design of Low-Voltage, Low-Power Operational Amplifier Cells*. Dordrecht, The Netherlands: Kluwer Academic Publishers, 1996.

[25] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "Multistage amplifier topologies with nested G_M-C compensation," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2000–2011, December 1997.

[26] K. N. Leung, P. K. T. Mok, and W.-H. Ki, "Right-half-plane zero removal technique for low-voltage low-power nested miller compensation cmos amplifier," in *Proc. IEEE Int. Conf. Electronics, Circuits, and Systems*, vol. 2, (Pafos, Cyprus), pp. 599–602, September 1999.

[27] N. K. Leung, P. K. T. Mok, W.-H. Ki, and J. K. O. Sin, "Three-stage large capacitive load amplifier with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 35, pp. 221–230, February 2000.

[28] G. Palumbo and S. Pennisi, "Design methodology and advances in nested-miller compensation," *IEEE Trans. Circuits Syst. I*, vol. 49, pp. 893–903, July 2002.

[29] X. Peng and W. Sansen, "Transconductance with capacitances feedback compensation for multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 40, pp. 1514–1520, July 2005.

[30] A. D. Grasso, G. Palumbo, and S. Pennisi, "Advances in reversed nested miller compensation," *IEEE Trans. Circuits Syst. I*, vol. 54, pp. 1459–1470, July 2007.

[31] W. M. C. Sansen, *Analog Design Essentials*. Dordrecht, The Netherlands: Springer, 2008.

[32] A. Thomsen, D. Kasha, and W. Lee, "A five stage chopper stabilized instrumentation amplifier using feedforward compensation," in *Proc. Symp. VLSI Circuits*, (Honolulu, Hawaii), pp. 220–223, June 1998.

[33] M. E. Schlarmann, E. K. F. Lee, and R. L. Geiger, "A new multipath amplifier design technique for enhancing gain without sacrificing bandiwdth," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 2, (Orlando, Florida), pp. 610–615, July 1999.

[34] B. K. Thandri and J. Sílva-Martinez, "A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no miller capacitors," *IEEE J. Solid-State Circuits*, vol. 38, pp. 237–243, February 2003.

[35] F. Zhu, S. Yan, J. Hu, and E. Sánchez-Sinencio, "Feedforward reversed nested miller compensation techniques for three-stage amplifiers," in *Proc. IEEE Int. Symp. Circuits and Systems*, (Kobe, Japan), pp. 2575–2578, May 2005.

[36] R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing, "A 100-mhz 100-db operational amplifier with multipath nested miller compensation structure," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1709–1717, December 1992.

[37] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Trans. Circuits Syst. I*, vol. 48, pp. 1041–1056, September 2001.

[38] A. Marques, Y. Geerts, M. Steyaert, and S. W., "Settling time analysis of third order systems," in *Proc. IEEE Int. Conf. Electronics, Circuits, and Systems*, vol. 2, (Lisboa, Portugal), pp. 505–508, September 1998.

[39] A. Pugliese, G. Cappucino, and G. Cocorullo, "Design procedure for settling time minimization in three-stage nested-miller amplifiers," *IEEE Trans. Circuits Syst. II*, vol. 55, pp. 1–5, January 2008.

[40] A. Pugliese, F. A. Amoroso, G. Cappuccino, and G. Cocorullo, "Settling time optimization for three-stage cmos amplifier topologies," *IEEE Trans. Circuits Syst. I*, vol. 56, pp. 2569–2582, December 2009.

[41] B. Y. Kamath, R. G. Meyer, and P. R. Gray, "Relationship between frequency response and settling time of operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 347–352, December 1974.

[42] Taiwan Semiconductor Manufacturing Co., LTD, *Mixed Signal & RF Technology Brochure*, March 2010.

[43] United Microelectronics Corporation, *28 Nanometer Brochure*, May 2010.

[44] GlobalFoundries, "65nm logic process." `http://www.globalfoundries.com/technology/65logic_process.aspx`, January 2010.

[45] J. Karki, *Fully-Differential Amplifiers*. Texas Instruments, January 2002.

[46] P. E. Fleischer, A. Ganesan, and K. R. Laker, "A switched capacitor oscillator with precision amplitude control and guaranteed start-up," *IEEE J. Solid-State Circuits*, vol. SC-20, pp. 641–647, April 1985.

[47] K. Martin and A. S. Sedra, "Effects of the op amp finite gain and bandwidth on the performance of switched-capacitor filters," *IEEE Trans. Circuits Syst.*, vol. CAS-28, pp. 822–829, August 1981.

[48] A. Leuciuc and C. Mitrea, "On the effect of op-amp finite gain in delta-sigma modulators," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 3, (Geneva, Switzerland), pp. 754–757, May 2000.

[49] Taiwan Semiconductor Manufacturing Co., LTD, *TSMC 0.18UM MIXED SIGNAL 1P6M SALICIDE 1.8V/3.3V RF SPICE MODELS*, September 2004.

[50] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Hoboken, New Jersey: John Wiley & Sons, Inc., 2005.

[51] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes, "Design-orient estimation of thermal noise in switched-capacitor circuits," *IEEE Trans. Circuits Syst. I*, vol. 52, pp. 2358–2368, November 2005.

[52] J. He, X. Xi, M. Dunga, M. Chan, and A. M. Niknejad, "Bsim5: An advanced charge-based mosfet model for nanoscale vlsi circuit simulation," *Solid-State Electronics*, vol. 51, pp. 433–444, February 2007.

[53] A. M. Abo and P. R. Gray, "A 1.5-v, 10-bit, 14.3-ms/s cmos pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, pp. 599–606, May 1999.

[54] P. M. Figueiredo and J. C. Vital, "Low kickback noise techniques for cmos latched comparators," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 1, (Vancouver, Canada), pp. I–537 – I–540, May 2004.

[55] D. Senderowicz, S. F. Dreyer, J. H. Huggins, C. F. Rahim, and C. A. Laber, "A family of differential nmos analog circuits for a pcm codec filter chip," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 1014–1023, December 1982.

[56] R. Castello and P. R. Gray, "A high-performance micropower switched-capacitor filter," *IEEE J. Solid-State Circuits*, vol. SC-20, pp. 1122–1132, December 1985.

[57] L. Sumanen, M. Waltari, V. Hakkarainen, and K. Halonen, "Cmos dynamic comparators for pipeline a/d converters," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 5, (Scottsdale, Arizona), pp. V–157 – V–160, May 2002.

[58] K. Martin and A. S. Sedra, "Switched-capacitor building blocks for adaptive systems," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. ASSP-29, pp. 736–744, June 1981.

[59] MOSIS, *Package Handbook*, May 1993.

[60] P. R. Kinget, "Device mismatch and tradeoffs in the design of analog circuits," *IEEE J. Solid-State Circuits*, vol. 40, pp. 1212–1224, June 2005.

[61] A. Zirger, "Random offset in cmos ic design," in *ECEN4827/5827 Analog IC Design*, University of Colorado at Boulder, 2007.

[62] R. G. Wu, *TSMC 0.18UM LOGIC 1P6M SALICIDE 1.8V/3.3V DESIGN RULE*. Taiwan Semiconductor Manufacturing Co., LTD, May 2006.

[63] E. Alon, "Lecture 6: Noise analysis techniques," in *EECS240 - Advanced Analog Integrated Circuits*, The University of California, Berkeley, 2010.