Photon Quantum Noise Limited Pixel and Array architectures in a-Si Technology for Large Area Digital Imaging Applications

by

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Abstract

A Voltage Controlled Oscillator (VCO) based pixel and array architecture is reported using amorphous silicon (a-Si) technology for large area digital imaging applications. The objectives of this research are to (a) demonstrate photon quantum noise limited pixel operation of less than 30 input referred noise electrons, (b) theoretically explore the use of the proposed VCO pixel architecture for photon quantum noise limited large area imaging applications, more specifically protein crystallography using a-Si, (c) to implement and demonstrate experimentally a quantum noise limited (VCO) pixel, a small prototype of quantum noise limited (VCO) pixelated array and a quantum noise limited (VCO) pixel integrated with direct detection selenium for energies compatible with a protein crystallography application.

Electronic noise (phase noise) and metastability performance of VCO pixels in low cost, widely available a-Si technology will be theoretically calculated and measured for the first time in this research. The application of a VCO pixel architecture in thin film technologies to large area imaging modalities will be examined and a small prototype a-Si array integrated with an overlying selenium X-ray converter will be demonstrated for the first time.

A-Si and poly-Si transistor technologies are traditionally considered inferior in performance to crystalline silicon, the dominant semiconductor technology today. This work aims to extend the reach of low cost, thin film transistor a-Si technology to high performance

analog applications (i.e. very low input referred noise) previously considered only the domain of crystalline silicon type semiconductor. The proposed VCO pixel architecture can enable large area arrays with quantum noise limited pixels using low cost thin film transistor technologies.

Index terms – Voltage Controlled Oscillator, Ring Oscillator, Amorphous silicon, thin film transistor, active pixel sensor, medical imaging, quantum noise, large area electronics.

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List of Abbreviations

PPS	Passive Pixel Sensor
APS	Active Pixel Sensor
VCO	Voltage Controlled Oscillator
RVCO	Ring Voltage Controlled Oscillator
TFT	Thin Film Transistor
VAPS	Voltage mediated Active Pixel Sensor
CAPS	Current mediated Active Pixel Sensor
LC	Inductance Capacitance
CMOS	Complementary Metal Oxide Semiconductor
PAN	Phosphoric - Acetic - Nitric

1 Introduction

Many pixel architectures have been proposed to date for active matrix flat panel imagers (AMFPIs). These include passive pixel (i.e. TFT switch based) [1][2] or active pixels (i.e. pixel level amplifier based) [3]. Both types of pixel designs are based on converting the collected charge at the input into an output voltage or current and require either a charge or trans-impedance amplifier in the off-panel readout circuit to extract the output signal and make it suitable for further processing.

SNR (Signal to Noise Ratio) is an important metric for AMFPIs. The signal component consists of the X-ray generated charge in the X-ray sensor, while the noise component consists of two independent noise sources [4]: photon shot noise (i.e. photon quantum noise) added in quadrature with electronic noise (consisting of flicker, thermal, and reset noise) from the various semiconductor devices in the readout circuit. The goal for the ideal imaging pixel is to minimize electronic noise such that SNR is a function only of photon shot noise (i.e. a fundamental limit). In considering pixel readout circuits and the related electronic noise, input referred electronic noise is a design parameter that is of interest. Input referred electronic noise in digital imaging pixels is the electronic noise at the output of the pixel divided by the pixel gain. The goal of this thesis is to demonstrate a pixel and a sample array architectures in amorphous silicon (a-Si)

technology that have a negligible input referred electronic noise and therefore, the pixel noise is dominated by only the photon shot or quantum noise.

An alternate oscillator a-Si pixel design to PPS and APS architectures was introduced in 2006 [5]. In the oscillator pixel architecture, a voltage controlled oscillator (VCO) plays a central role in signal conversion and transfer. The impinging X-ray beam produces a charge in a pixel level capacitor and the change in the voltage on that capacitor due to the impinging X-ray beam controls the frequency of oscillation of the VCO. The key difference between the previously reported PPS and APS designs and the proposed design is that now the output signal is a frequency. In this thesis, we extend the VCO architecture [5] for X-ray quantum noise limited applications for large area digital imaging. The schematic of the VCO pixel is shown in Figure 1. Since the output of the circuit is frequency and not voltage or current, and also because of the use of an on-pixel buffer, the input referred electronic noise of the pixel is very low, making the pixel suitable for quantum noise limited imaging applications. This is discussed in detail in next chapters. A number of off-panel circuit architectures have been proposed and tested in this thesis.

Figure 1. Ring Voltage Controlled Oscillator Pixel Schematic.

The off-panel readout circuit architecture suitable for in lab testing of the VCO based pixel and array are given as well. Note that the off-panel circuit is used to detect the output of the pixel and storing it for further image reconstruction processes.

In designing the VCO pixel, noise, power consumption, tuning range, pixel area, and frequency of oscillations [6] were considered. Given the range of parameters and primarily the need for simplicity, a ring VCO was fabricated in a-Si technology [5]. The reported ring-oscillator VCO pixel architecture (referred to as RVCO henceforth) is designed to interface with a detector. The choice of a detector is flexible: an indirect detection a-Si PIN photodiode coupled to an X-ray scintillator [7] can be used or alternately, an overlying a-Se direct detection layer [8].

The ultimate goal of this research is to demonstrate via measurements that the input referred electronic noise for the fabricated a-Si pixel oscillator is negligible, making it ideal to detect even single photon interactions in protein crystallography applications (i.e. 6 keV X-ray photons) when used with an amorphous selenium layer as the detector. The second purpose is to simulate and measure the stability and input referred electronic noise for the in-house fabricated RVCO pixel and array. The third target is to optimize the off-panel readout circuitry in order to reduce the fix pattern noise and fringing effects.

1.1 Novelty and Application

The circuit proposed in this thesis is aiming to do Protein Crystallography. Therefore, in this chapter general concepts and requirements of the Protein Crystallography are given. In 2009

a novel way for Protein Crystallography using a-Si TFT flat panel imagers was introduced in [36], which is briefly, using the Avalanche a-Se for the detector level and using the traditional PPS a-Si pixels as the flat panel imager. This approach is not scalable and hence it is challenging to make a large area low cost Avalanche a-Se. The scalability issue in this proposal is addressed by using the ordinary a-Se detector layer and using the proposed RVCO as the pixels in the flat panel imager.

1.1.1 Protein Crystallography

Protein Crystallography is a way to resolve the atomic structure of protein using the intensity distribution of its X-ray diffraction pattern [35]. A conventional crystallography is done by putting the protein crystal inside a thin walled capillary and using a mono energetic X-ray beam of 6 – 20 keV (which has the wavelength of 2.1 to 0.6 angstrom which is comparable to the protein crystal's inter-atomic distances) [36]. The setup is shown in Figure 2. This mono energetic X-ray beam is applied to the crystal structure and a diffracted pattern is formed on the 2D flat panel imager. In order to get a 3D image out of the crystal, several hundred diffraction patterns are recorded in the computer and will be reconstructed using a signal processing software (The protein crystal is rotated around an axis perpendicular to the X-ray beam so that every atomic plane can be exposed to X-rays) [36]. The intensity of the diffracted beam is maximized when it satisfies Bragg's law. Each recorded pattern contains several thousand diffraction maxima, commonly known as Bragg peaks [37]. These peaks are used to reconstruct the crystal structure in the software. An image of a diffraction pattern containing a Bragg peak is shown in Figure 3.

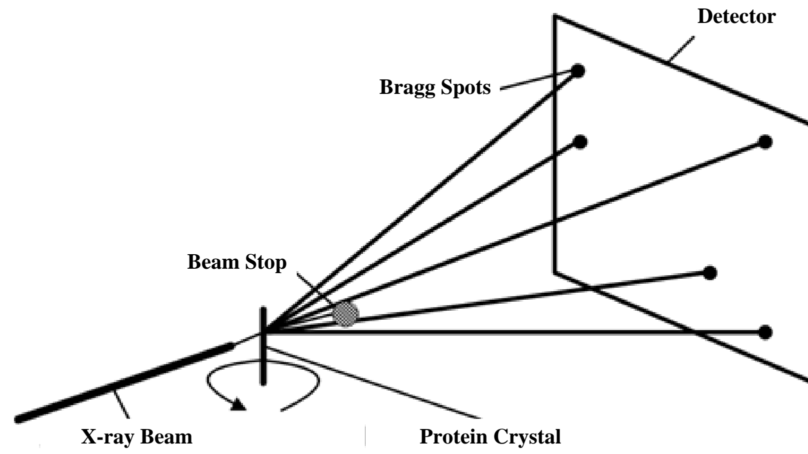


Figure 2. Setup for a typical protein crystallography experiment [36].

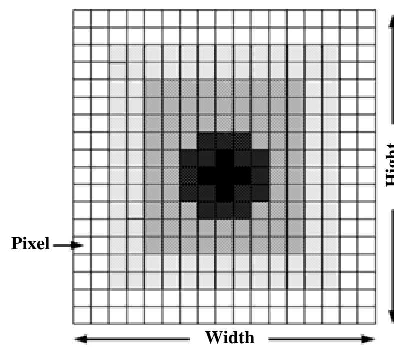


Figure 3. Image of a diffraction pattern containing a Bragg peak [36].

1.1.2 Requirements of a Protein Crystallography Detector

There are some requirements that have to be considered for a detector so that it can be used in Protein Crystallography applications. These requirements are detector area, dynamic range, sensitivity, readout time and spatial resolution (pixel size) [37][38].

1.1.2.1 Detector Area

The imaging area is the area required for an ideal detector to collect all the diffraction data with a specified resolution [38]. The detector has to be a large area detector because of two reasons. First, the first 100 orders of diffraction data contain useful data about the protein crystal, therefore a 20 by 20 cm^2 detector area is sufficient to collect all the data about the protein crystal [38][39]. Secondly, background X-ray scatter noise is reduced by using a large area detector farther from the protein crystal. This is because the background X-ray scatter noise drops with the square of the crystal-to-detector distance [39].

1.1.2.2 Dynamic Range

The pixel has to be capable of reading the weak and the strong diffraction spots (one X-ray photon per pixel all the way to 1.2×10^5 X-ray photon per pixel) [39][40]. Most of the pixels have to detect the weak spots and a few should detect strong spots.

1.1.2.3 Sensitivity

The protein crystals diffract the X-ray photons weakly, typically less than 0.1% of the incident X-ray beam scatters from the crystal. Therefore, the intensity of the diffracted X-ray is very low [41]. Moreover, radiation damage to the protein crystal might result in a gradual degradation of the resolution of the diffracted pattern [42]. Therefore, the dose of exposure has to be diminished to prevent the protein crystal damage due to the X-ray exposure. So, a very

sensitive pixel is mostly required to detect the small diffraction signal generated from low dose X-ray. Ideally, the detector should detect 1 absorbed X-ray photon. Low quantum energy X-ray photon used in protein crystallography can produce as few as 120 electrons.

1.1.2.4 Readout Time

Readout time is the time required by the detector to read the charge integrated on the detector to the external circuitry. The readout time of the detector should be in the range of seconds to minimize the total X-ray exposure time as well as radiation damage to protein [36].

1.1.2.5 Spatial Resolution

The pixel size of the detector should be in a way that a few pixels (typically 3 to 5) can hold each Bragg peak. Therefore, to resolve two adjacent Bragg peaks, there should be about five pixels between them [38][39].

For instance, a 12 keV X-ray source (wavelength about 1 angstrom) and a unit cell dimension of 20 nm in protein crystal and the crystal-to-detector distance of 20 cm, result in Bragg peaks of 100-300 µm. Therefore, a 50-150 µm pixel size is needed [37].

1.2 Thesis Organization

The rest of the thesis is organized as follows. First, a brief introduction to Active Matrix Pixels is given followed by a brief discussion on different structures of oscillators and the suitable structure for being fabricated in a-Si technology (which is the RVCO). Next, the design of the RVCO single pixel and its operation as a pixel and an array are discussed. After that, an ultra low noise RVCO architecture is given and discussed, which has less input referred electronic noise compared to the RVCO architecture given in Figure 1. Then, the fabrication process is described followed by measurements of phase noise and metastability and also measured results of the single RVCO pixel implemented without and with an amorphous selenium (a-Se) layer as the detector for protein crystallography X-ray ranges for an in-house developed RVCO pixel. After that, measurement results of a sample in-house fabricated array of RVCOs are given and discussed. Lastly, Detective Quantum Efficiency (DQE) for the proposed structure (RVCO) is analyzed followed by the conclusion and contributions.

2 Active Matrix Pixels

In this chapter a brief background on different structures of Active Matrix Pixels which are passive pixel sensors (PPS) [1][2] or active pixel sensors (APS) [3] are presented.

2.1 PPS

The passive pixel was first proposed by Gene Weckler in 1967. In a PPS structure as it is shown in Figure 4 (a), the charge induced on the pixel capacitor in the integration time is converted to an output voltage in the readout time by means of a TFT switch. Figure 4 (b) shows the operation cycle of the PPS. There are many important factors in designing a PPS structure such as gain and linearity, readout rate and input referred noise (detector noise and electronic noise) [9]. **Gain and linearity**: the passive pixel readout circuit is just a simple switch, therefore it does not provide any gain to the signal on the charge detection node. A voltage gain can be achieved by means of off-panel charge amplifier. This will increase the electronic noise as well. The TFT switch works in the linear mode of the TFT and as a result if the X-ray sensor (Here is a-Se in Figure 4) behaves linearly, the pixel's operation is linear [9]. **Readout rate**: this rate is characterized by the RC time constant of the pixel which is $R_{on}C_{Pix}$. For a complete charge readout (95% - 99.3%), about 3-5 time constants are usually sufficient. Given this factor and the

number of rows in a pixelated array of PPS, one can design C_{Pix} and R_{on} to achieve the desired frame rate (frames/second) [9]. **Input referred noise**: Based on simulations and measurements in [2] the smallest input referred electronic noise measured for a PPS pixel is around 1000 electrons. This makes PPS to be suitable for applications with higher incoming level of X-ray signals such as chest radiography.

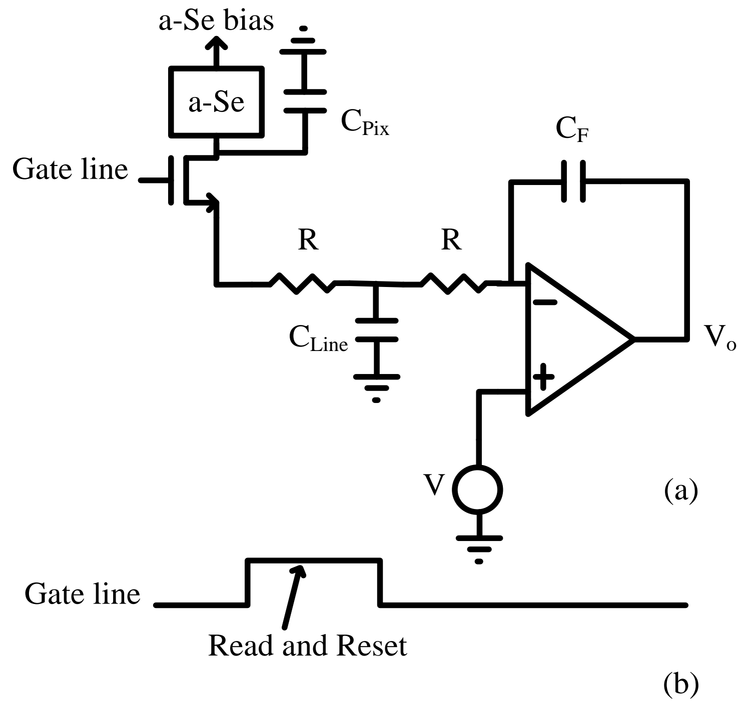


Figure 4. PPS architecture (a) and operation cycle (b).

2.2 APS

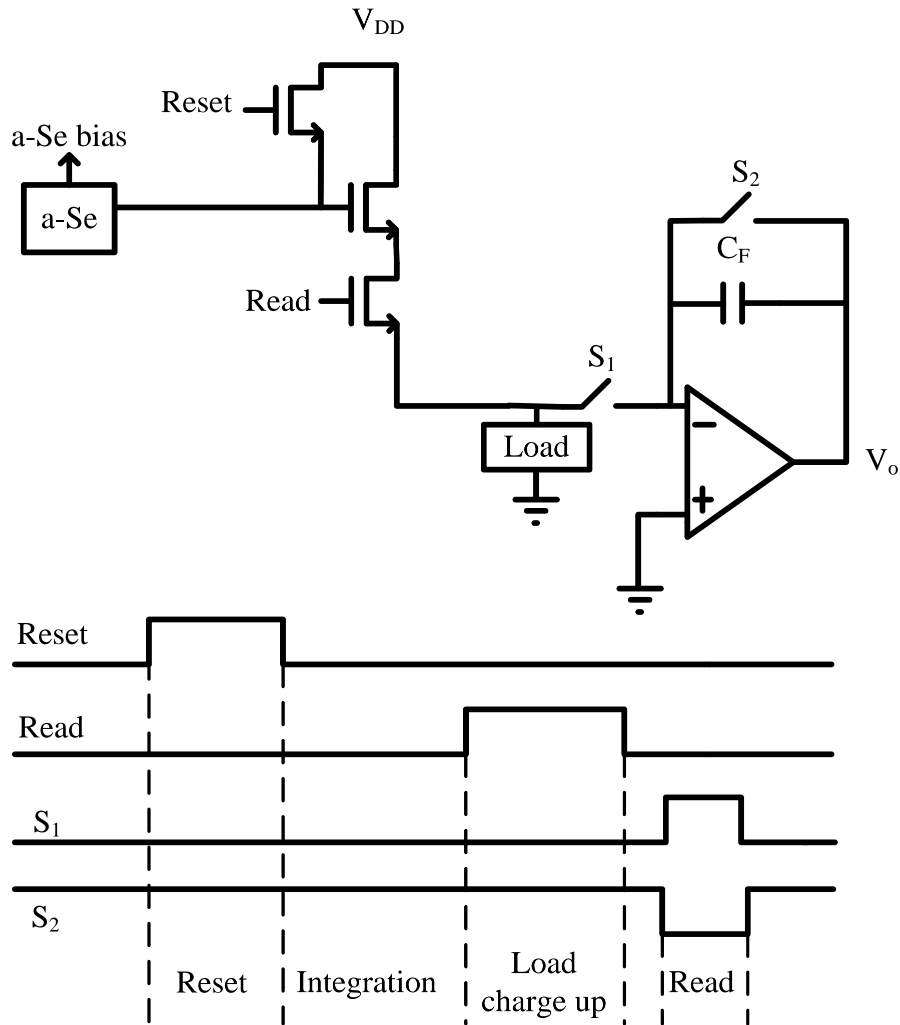
APS was first imported from crystalline Silicon (c-Si) to a-Si technology by Dr. Karim S. Karim in 2001 [3]. He proposed a 3 Thin film transistor (TFT) structure (Figure 5) that extends a-Si TFT technology from traditional switching applications to on-pixel small signal amplification for diagnostic digital medical imaging applications. This a-Si pixel amplifier offers improved signal-to-noise ratios, lower cost, and less off-panel circuit complexity compared to its traditional a-Si switch counterpart (passive pixel sensor). This structure can be used for large area real-time imaging for low-noise fluoroscopic medical imaging that is not viable with current a-Si switch based pixels. More significantly, the pixel (because of its circuit gain) offers potentially reduced patient x-ray doses for other medical imaging modalities, hence improving the safety standards associated with current x-ray imaging practices [3]. Later on, some other researchers proposed other APS structures, each targeted for a specific application.

There are some known different architectures of APS to date. 3-TFT APS structure, 2-TFT APS structure, Hybrid APS structure and Current programmed APS structure. RVCO pixel is novel type of APS pixel which will be discussed in details later on.

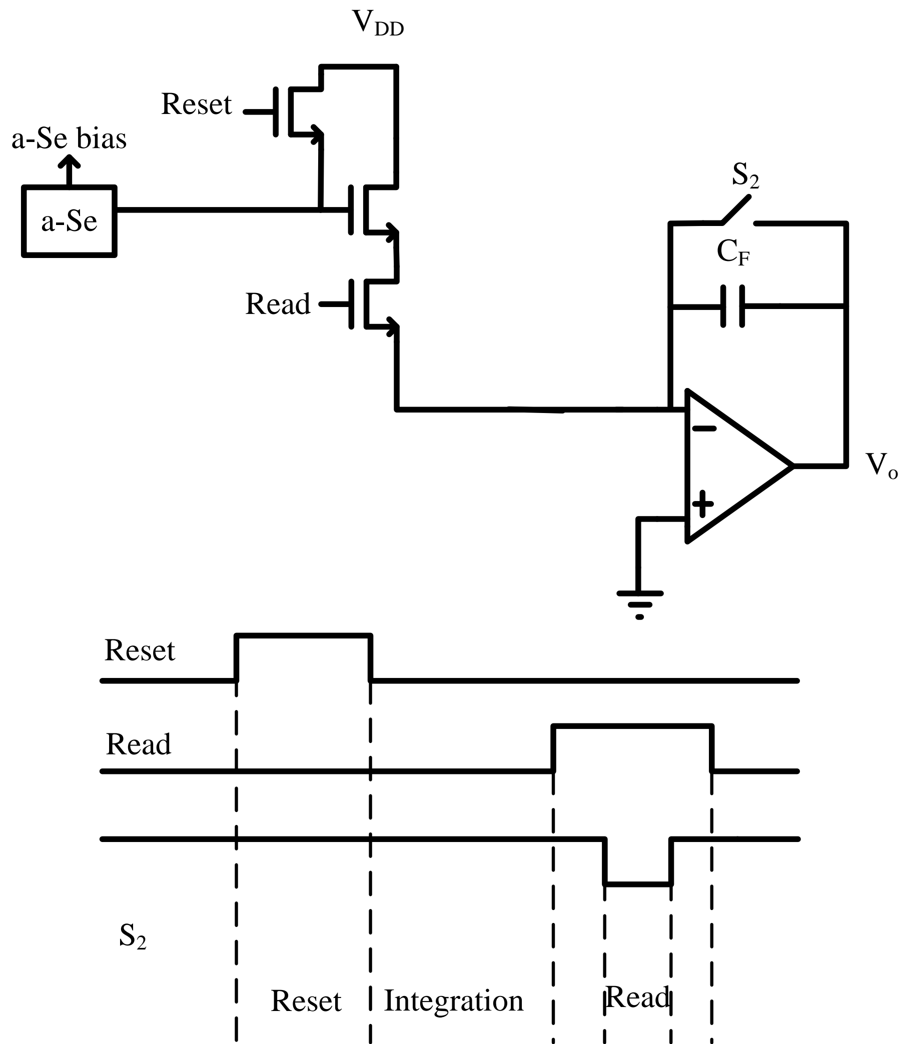
2.2.1 3-TFT APS structure

There are two commonly used architectures of 3-TFT APS structures: voltage mediated active pixel sensor (V-APS) [10] and current mediated active pixel sensor (C-APS) [10]. Figure 5 shows these two structures and their timing diagram. Each of these structures has their own benefits as well as some disadvantages which make each of them suitable for specific digital medical imaging applications. For instance it has been shown in [11][12] that the V-APS

structure has a relatively lower electronic noise compared to C-APS architecture. However, V-APS suffers from a constant change of the signal integrated on the line capacitor due to the leakage current of the OFF pixels.



(a)



(b)

Figure 5. V-APS architecture and timing diagram (a), C-APS architecture and timing diagram (b) (S_1 and S_2 are active high).

After the invention of 3-TFT APS, this technology (APS) was carried on in different ways. Each way focused on a specific target such as: higher resolution, higher speed, lower noise, hybrid readout and V_t shift compensated APS structures.

2.2.2 2_TFT APS structure

The next APS structure was proposed by Dr. Farhad Taghibakhsh in 2008 (Figure 6) [28]. This architecture uses 2 TFTs aiming at relatively higher resolution and lower noise compared to 3-TFT structure. The advantages over 3-TFT APS are less complexity, smaller pixel pitch, increased pixel gain and higher speed. These advantages make the 2-TFT APS promising for low noise, high resolution and fast digital medical imaging applications including emerging medical imaging modalities, such as mammography tomosynthesis and cone beam computed tomography [28]. The timing and readout of this pixel is exactly the same as the readout of the current mediated active pixel sensor (C-APS).

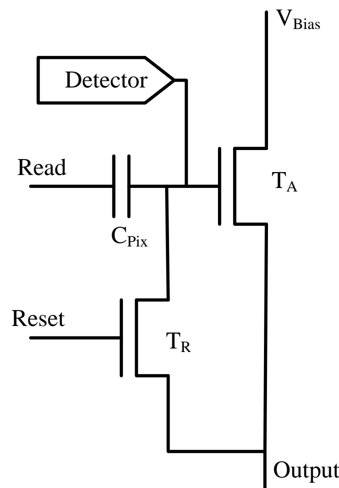


Figure 6. 2-TFT APS structure [28].

2.2.3 Hybrid APS structure

Dr. Mohammad Hadi Izadi in 2006 reported a hybrid amplified pixel architecture based on a combination of PPS and amplified pixel designs (Figure 7) that, in addition to low noise performance, also resulted in large-signal linearity and consequently higher dynamic range [43]. He showed that this architecture increases the large signal linearity. This is because in traditional APS structure compared to Passive Pixel Sensor (PPS) structure, the output signal suffers from nonlinearity due to higher pixel level input (control) voltages. This research also showed input referred noise levels less than 1000 electrons in real world is approachable [43], making the proposed architecture suitable for low noise digital X-ray fluoroscopy. This pixel's readout is the same as 3-TFT structure and PPS structure if it is used in APS and PPS readout modes, respectively.

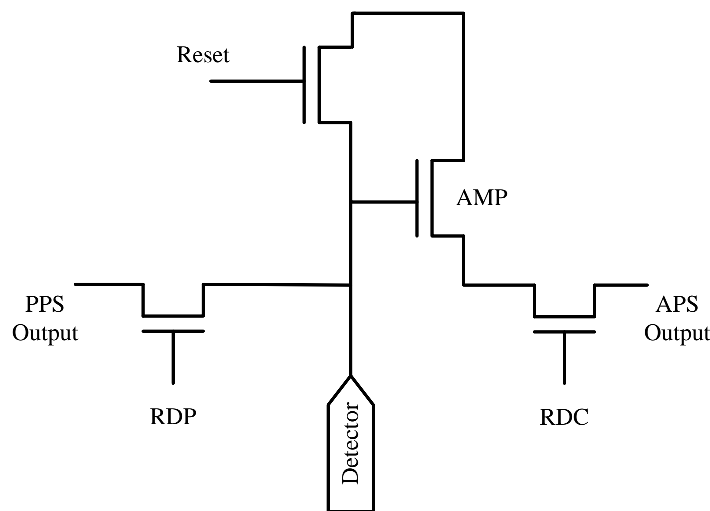


Figure 7. Hybrid APS structure [43].

2.2.4 Current programmed APS structure

Dr. Nader Safavian in 2009 reported a dual mode current-programmed, current-output pixel amplifier (Figure 8) for digital medical imaging applications [44]. This architecture can be used in hybrid fluoroscopic and radiographic imagers. The reported architecture promises dual mode X-ray imaging while compensating for the long term electrical and thermal stress known as a-Si TFT threshold voltage (V_t) shift due to its specific architecture and on-pixel and off-pixel readout schemes [44]. Refer to [44] for the detailed operation scheme.

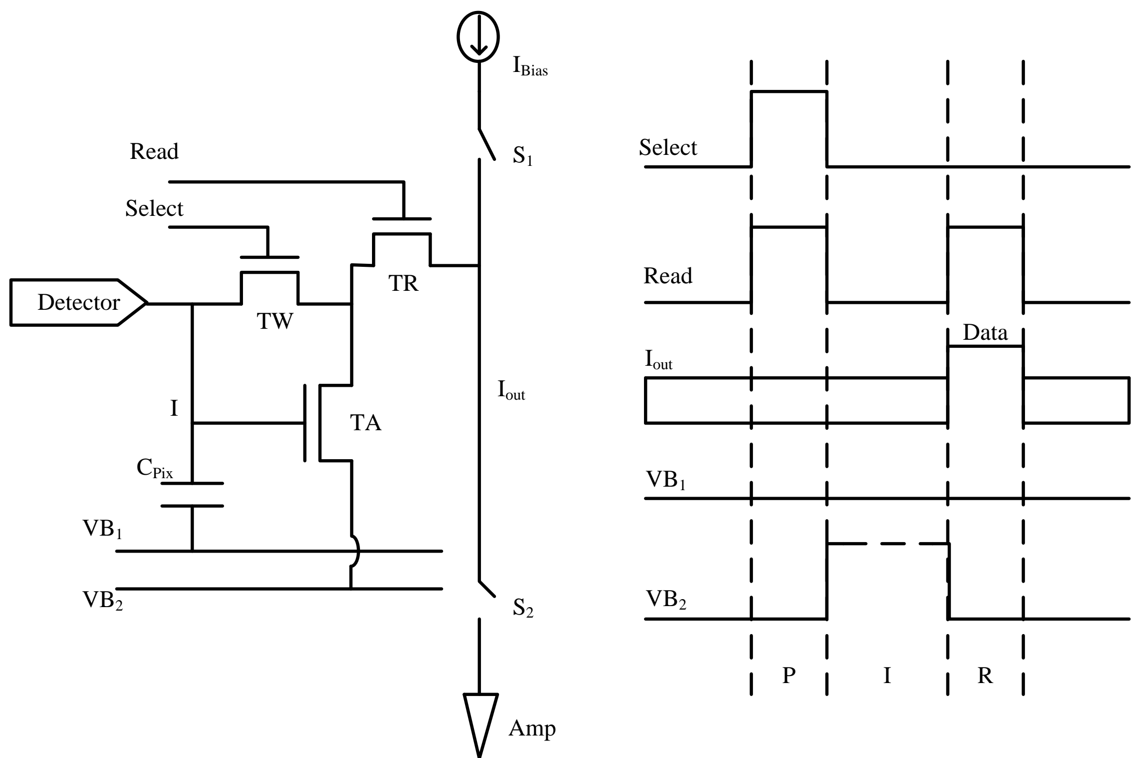


Figure 8. Current-programmed APS structure [44].

It is worthwhile to mention that none of the Active Matrix Pixels listed above can have a quantum limited electronic noise at the input of the pixel [13][14]. Therefore, there is a severe need to design an architecture which has a quantum limited electronic noise to be able to be used

for quantum noise limited digital imaging applications, such as protein crystallography, which is the aim of this work. Quantum limited means that the input noise is dominated by the photon quantum shot noise in the detector layer and not the electronic noise.

3 Voltage Controlled Oscillators and the Suitable Structure for Digital Medical Imaging Applications

The voltage controlled oscillator (VCO) has the central role of converting the charge accumulated by the impinging X-ray beam to frequency. The output circuit suitable for frequency readout is given in the following sections. There are a lot of VCO structures used in industry and for research purposes. The different structures are shown in Figure 9.

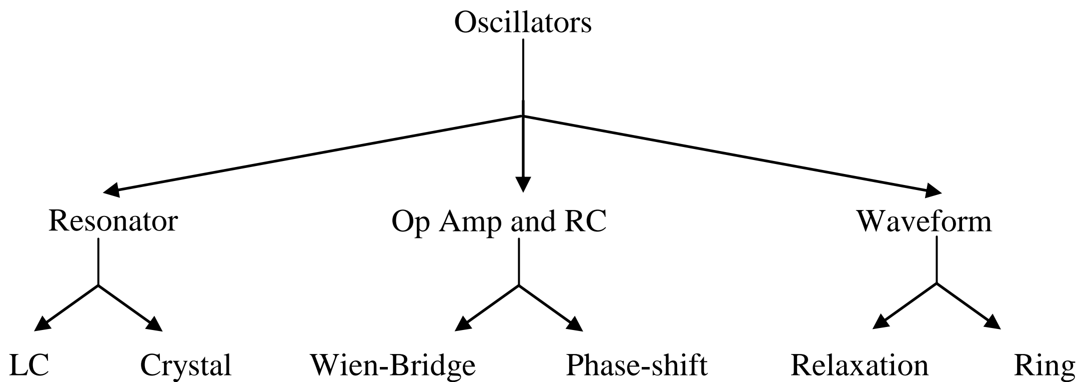


Figure 9. Different types of VCOs.

3.1 LC Tank Oscillators

This structure of oscillator is shown in Figure 10. An LC oscillator can be considered as two 1-port networks connected together. One of them represents the frequency selective tank, where the oscillation occurs. However, the oscillations will die through RI^2 losses in the circuit which is modeled by g_{tank}. If this energy could be pumped back into the tank as the same rate as it was being dissipated, the circuit would ring forever and this is the basic idea of an LC resonant oscillator. So, the other 1-port represents the active circuit which is modeled by g_{active} that cancels out the losses in the tank [15]. This oscillator will oscillate when the g_{active} cancels out the g_{tank} and also the close loop gain has a zero phase-shift.

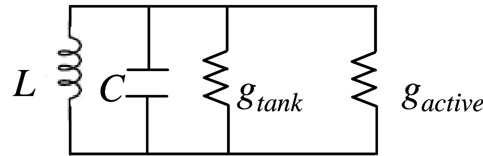


Figure 10. LC oscillator structure.

Therefore the close loop gain has to be a real number with a magnitude of greater than or equal to one for the oscillation to occur. Two common used LC oscillators are shown in Figure 11.

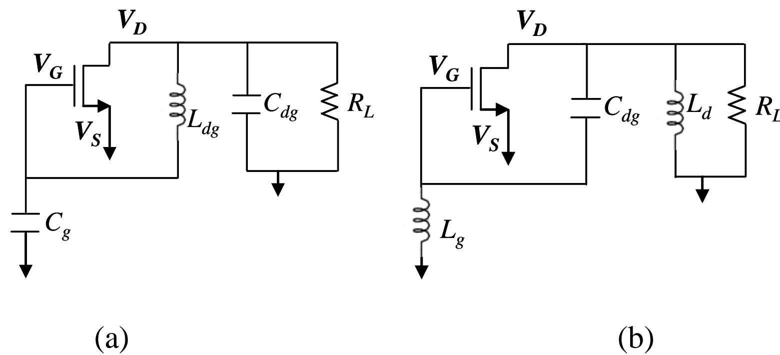


Figure 11. Colpits oscillator (a), Hartley oscillator structures (b).

It has been shown in [16] that the frequency of oscillation in a Hartley oscillator in which a TFT is used is as follows,

$$\omega_0 = 1/\sqrt{(L_d + L_g)C_{dg}} \tag{1}$$

And for the oscillations to start, we should have,

$$g_m > L_d/(L_g \times R_L) \tag{2}$$

The equation above shows that for the oscillation to start the gain from gate to drain which is $g_m R_L$ must be greater than the voltage ratio provided by inductive divider. This means that the gain should be greater than unity.

The calculations in [16] show that the maximum inductor which can be fabricated in the 200×200 μm^2 is 30nH-50nH. The fabrication results in [16] have shown that we can fabricate a 30nH inductor in the 200×200 μm^2 area and we can have a frequency of approximately 500MHz with this inductor size. But, for designing an LC oscillator in a-Si TFT technology, we need an inductor above 1000 µH, to have about 1 MHz of oscillation frequency, which is due to the limit of maximum TFT speed. There is currently no way to design and fabricate an LC oscillator in a-Si technology in the desired area.

3.2 Crystal Oscillator

Crystal oscillator is an electronic oscillator circuit based on a piezoelectric material. The mechanical resonance of the crystal of the piezoelectric material is used to generate an oscillating signal with a precise frequency. Figure 12 shows the electronic symbol and the equivalent circuit of a quartz crystal oscillator. This oscillator has two modes of oscillations (series ω_s and parallel ω_p). Depending on the frequency of oscillation and load capacitance and series resistor, the

crystal oscillates in one of the modes or in a frequency between two modes. For further information on crystal oscillators which are beyond the target of this thesis, refer to [45][46][47].

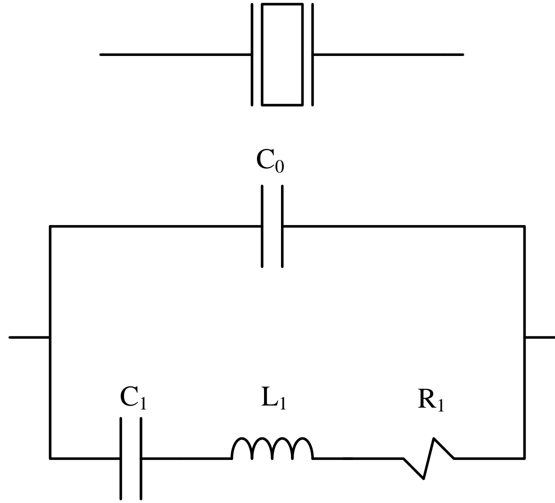


Figure 12. Electronic symbol and equivalent circuit for a quartz crystal in an oscillator.

$$\omega_s = \frac{1}{\sqrt{L_1 C_1}} \ , \ \omega_p = \sqrt{\frac{C_1 + C_0}{L_1 . C_1 . C_0}} \tag{3}$$

This configuration is not suitable for voltage controlled oscillators and also it cannot be fabricated over large area. Therefore, this configuration cannot be used for large area digital imaging applications.

3.3 Wein-Bridge Oscillator

The Wein-Bridge oscillator was first introduced in 1981 by Max Wein. The schematic of the circuit is shown in Figure 13. The bridge has four resistors and two capacitors, as it is shown in Figure 13. One can say that this oscillator is a combination of a positive feedback system and a band pass filter [48].

$$W = \frac{1}{RC} \tag{4}$$

This architecture has an op-amp and a number of resistors in it. As a result, it is challenging to fabricate this architecture in a-Si technology in a reasonable area due to the huge size of TFTs compared to CMOS transistors and also the area of the resistors. In other words, each pixel is going to be very huge in terms of size, which makes it useless for large area digital imaging (more specifically, protein crystallography).

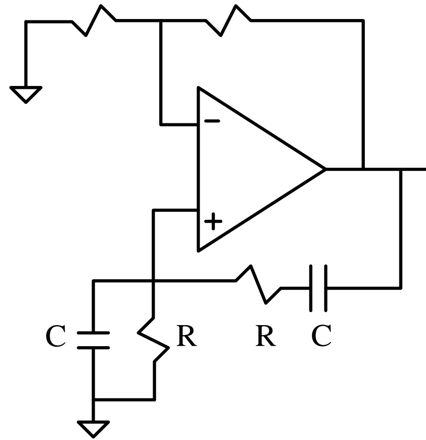


Figure 13. Wein-Bridge oscillator architecture.

3.4 Phase-Shift Oscillator

This oscillator configuration consists of an inverting amplifier and a feedback filter which shifts the phase of the amplifier's output by 180 degrees at the oscillation frequency. A simple phase-shift oscillator architecture is shown in Figure 14. The frequency of oscillation for such configuration is as follows,

$$W = \frac{1}{2\pi RC\sqrt{6}} \tag{5}$$

($R_1 = R_2 = R_3$, $C_1 = C_2 = C_3$)

The overall gain of this configuration has to be greater than 1 or else the oscillation will die (R_{1f}>29R_1). This architecture is not suitable for a-Si large area fabrication because of the presence of the op-amp and resistors in the configuration. Op-amps and resistors cannot be fabricated in a reasonable area in a-Si technology and therefore, each pixel will be very big which makes it useless for digital imaging applications (more specifically, protein crystallography).

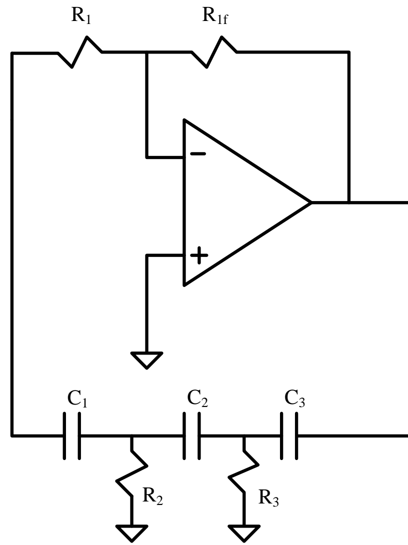
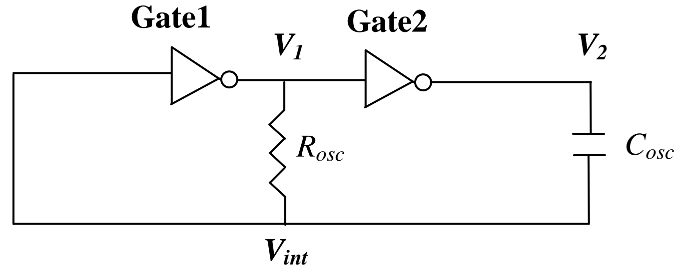


Figure 14. Phase-Shift oscillator architecture.

3.5 Relaxation Oscillator

The structure and period of oscillation are shown below (Figure 15). Circuit simulations for V_T = 5V, μ_{band} = 0.6cm^2/V.s and circuit dimensions of $m_{load(1,2)}$ =350µm/5µm, $m_{drive(1,2)}$ =550µm/5µm, m_{osc}=50µm/5µm, C_{osc}=2pF, and V_{cc} =30V resulted in f_{osc}= 25 kHz [16]. But, the main problem with this circuit is its low frequency of oscillation which leads to low circuit sensitivity. Moreover, relaxation oscillators generally suffer from low frequency stability and

higher phase noise [17]. Therefore, a relaxation oscillator is not a good choice for being fabricated in a-Si technology.



$$T_{osc} = 2(\log 3) R_{osc} C_{osc}$$

Figure 15. Structure and frequency of oscillation for a relaxation oscillator.

3.6 RVCO Pixel Architecture and Operation

The ring oscillator structure is formed by connecting an odd number of inverter stages in a loop. Although usually at least five inverters are used to ensure oscillations will start, it is possible to start oscillations with a minimum of three inverters (Figure 1). A smaller number of inverters leads to a higher oscillation frequency (f_{osc}). Taking all the parameters into account, the RVCO structure is the best choice for being fabricated in a-Si technology. In the RVCO, the first stage's bias current is controlled by the input voltage at the gate of the Load1 TFT (see Figure 1). The rising edge at node V_1 propagates through nodes V_2 and V_3 to return inverted after a delay of $3t_p$. For a general case of N stages, 180º of phase shift is provided by the chain and sufficient gain (the overall gain >1) should be provided at f_{osc}. The gain of each stage should be greater than 1 to ensure that the oscillation will not get damped. As seen in Figure 1, each stage's load is an active load and therefore, the gain of each stage of the oscillator can be derived as follows,

$$Gain = \left|\frac{V_o}{V_{in}}\right| = \sqrt{\frac{(\frac{W}{L})_{Drive}}{(\frac{W}{L})_{Load}}} > 1 \tag{6}$$

The f_{osc} can be derived once the propagation delay t_p of each stage is known. t_{pHL} is the time it takes for the output to reach from the maximum value to 50% of its minimum and similarly for t_{pLH}. The charge-discharge time for an RC network from maximum to 50% is $0.69RC$. For simplicity we can assume that both rise and fall times are equal. Therefore the propagation delay ($t_p = t_{pHL} = t_{pLH}$) is as follows,

$$t_P = \frac{0.69C_P}{g_{m-Load}} \tag{7}$$

where C_P is the effective capacitance at each node (Figure 16) and $g_{m\text{-}load}$ is the load TFT's transconductance. This total capacitance can be calculated as follows. The capacitor C_{drive} is the overlap capacitor between gate and source (or drain) of the drive TFT and C_{load} is the overlap capacitor between gate and source (or drain) of the load TFT. Note that the gain of each stage is assumed to be around *2*, therefore by averaging the node capacitance of the positive and negative cycles for each stage and using the Miller effect, we estimate the node capacitance. Another assumption is that the C_{drive} is much bigger than C_{load} and therefore, $C_{load}+C_{drive} \sim C_{drive}$,

$$C_P = \frac{3}{2}C_{gs-drive} + C_{gs-Load} \tag{8}$$

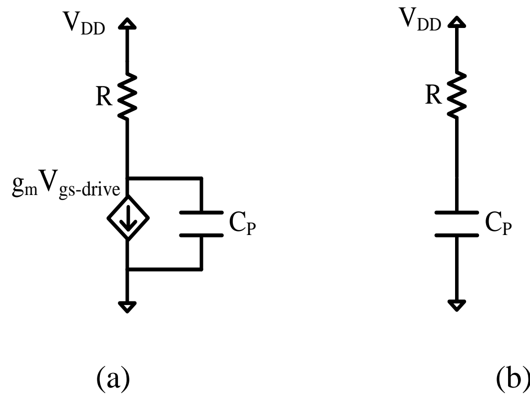


Figure 16. Positive cycle in each inverter stage (a), Negative cycle in each inverter stage (b).

So, the frequency of oscillation can be written as,

$$f_{osc} = \frac{1}{2Nt_P} \tag{9}$$

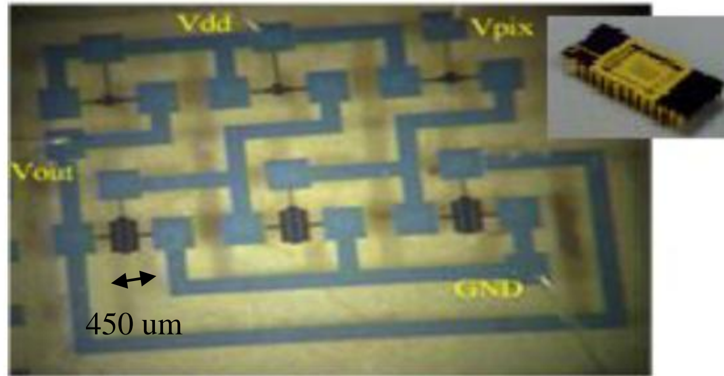
We can consider two states for each stage: positive and negative. In the positive state the drive TFT is ON and in the negative state the drive TFT is OFF. The small signal circuit models for both states are shown in Figure 16. Using expressions for f_{osc} and t_P, the frequency-voltage gain (Δf_{osc}) can be calculated as follows,

$$\Delta f_{osc} = \frac{\Delta g_{m-Load}}{6\times 0.69 C_P} = \frac{\mu C_{ox}(W/L)_{Load}\Delta V_{pix}}{4.14 C_P} \tag{10}$$

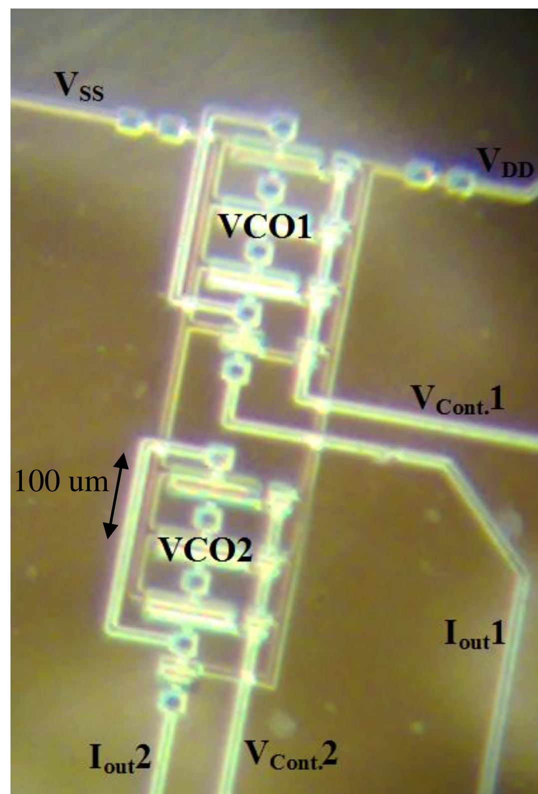
Figure 17 (a) shows the in-house fabricated pixel using large size TFTs just for proof of concept. This architecture, due to its low frequency-voltage gain (90 kHz/V), is not suitable for phase noise and metastability tests. ($(W/L)_{load1}=(W/L)_{load2}=(W/L)_{load3}$=50µm/50µm, $(W/L)_{drive1}=(W/L)_{drive2}=(W/L)_{drive3}$=300µm/50µm) Figure 17 (b) shows the in-house fabricated RVCO pixel excluding the reset TFT using smaller TFT sizing to get a high enough frequency-voltage gain (1.85 kHz/V). This pixel has been used for all the measurements for the single RVCO pixel. ($(W/L)_{load1}=(W/L)_{load2}=(W/L)_{load3}$=10µm/10µm, $(W/L)_{drive1}=(W/L)_{drive2}=(W/L)_{drive3}$ =60µm/10µm)

There are three modes of operation for each pixel. 1) **Reset mode:** In this mode the reset TFT is on and the RVCO is off (which reduces inter-pixel crosstalk), resulting in the input node being reset to $V_{pix} = (V_{in} - V_{t-reset})$, where $V_{t-reset}$ is the threshold voltage of the reset TFT. 2) **Integration mode:** In this mode the reset TFT and the RVCO are both off and the detector accumulates the signal on the input capacitor at the gate of Load1 TFT. This brings about a change in the input voltage. 3) **Readout mode:** In this mode the VCO will be turned on and the

reset TFT is kept off. This allows the circuit to start oscillating with respect to the input voltage (V_{pix}). The operation of the pixel is discussed in the next chapter.



(a)



(b)

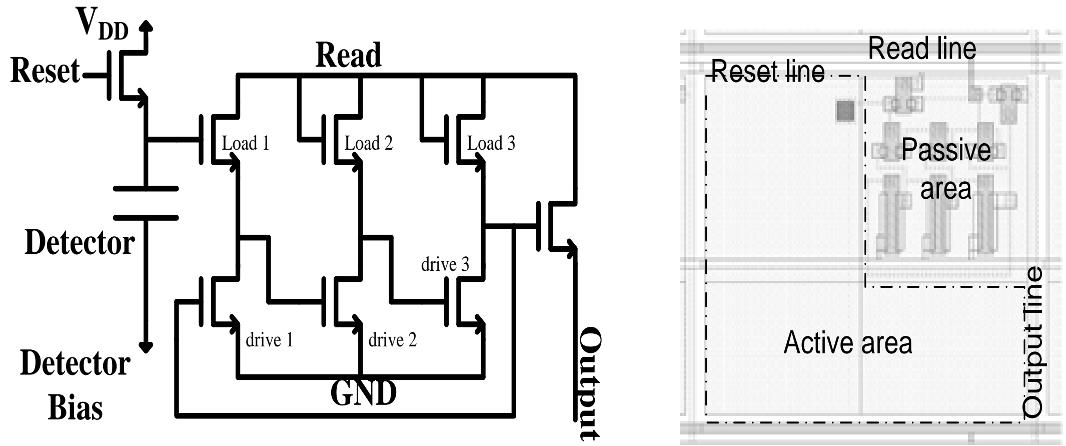
Figure 17. In-house fabricated RVCO pixel with bigger size TFTs(a), with smaller size TFTs (b).

4 RVCO Structure and Operation

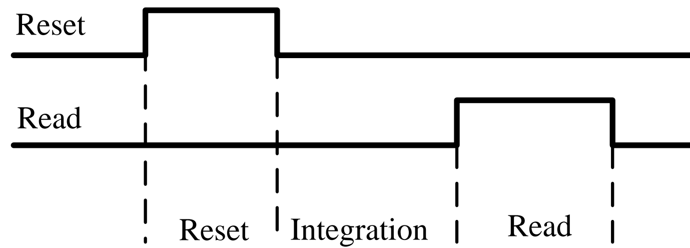
4.1 RVCO Pixel Structure and Operation

AS shown in the previous chapter, the RVCO is the best option to be fabricated in large area in a-Si technology. The architecture of the RVCO single pixel is shown in Figure 1. As it has been discussed in the previous chapters, the core of this pixel is a 3-stage ring voltage controlled oscillator. There is another TFT used for resetting the pixel in each readout frame. Also, an on-pixel buffer (common drain amplifier) is used at the output of each pixel. Suppose an RVCO pixel is used in an array. This buffer eliminates the loading effect of the readout line. Otherwise, the loading effect of the line would change the frequency of oscillation of the pixel. This buffer also eliminates any noise sources on the readout line affecting the pixel operation. This is because of the gate oxide isolation of the buffer TFT. In other words, the gate oxide of the buffer TFT, doesn't allow any electronic noise presented in the drain source current of it to be transferred to the gate of this TFT. Thus the noise in the readout line doesn't affect the input referred electronic noise of the pixel. Figure 18 (a) shows the pixel architecture along with its layout. Timing of the RVCO pixel operation is given in Figure 18 (b). As it can be seen from the layout (Figure 18 (a)), there are two different areas in the layout. One is the passive area which

has the RVCO TFTs for reading out the X-ray generated charge, and one is the active area which is the bottom-electrode connection for the detector layer which is a-Se in our case.



(a)



(b)

Figure 18. RVCO pixel architecture and layout (a), Timing diagram of the RVCO pixel.

4.1.1 RVCO single pixel design

In designing an RVCO single pixel, some design requirements have to be met. These requirements are as follows: noise, power consumption, fringing effect, tuning range, pixel area, and frequency of oscillations [6].

Input referred electronic noise has to be very low and to achieve such low noise we have to consider some requirements. The electronic noise sources in the RVCO pixel are: data line noise, phase noise in the RVCO pixel and reset noise in the reset switch capacitor configuration used for resetting the pixel. The noise simulation and measurements will be discussed in future chapters. Each of these noise sources are taken into account in the design of the RVCO pixel. Reset noise and data line noise sources are eliminated by use of techniques proposed in future chapters and use of the on-pixel buffer, respectively.

Power consumption is another important point in designing an RVCO pixel. Power consumption in an array of RVCOs causes the flat panel to heat up and therefore causes some inconsistency in the array's behavior such as V_t shift and other problems. In this design the power consumption is diminished by using the timing pattern shown in Figure 18 (b). In this timing scheme the pixel is only operating when the output of the pixel has to be readout. Otherwise, the pixel is kept OFF by applying 0 V for the read signal.

Fringing effect is caused by overlapping function of the neighboring pixels in an array. If there are so many neighboring pixels oscillating at the same time with different oscillation frequencies, then different frequency of oscillations might interfere with each other. This issue is addressed by the timing scheme used for the pixel readout shown in Figure 18 (b). Turning ON each pixel only for the readout period and keeping it OFF for the rest of the frame eliminates fringing effect.

Tuning range is another important issue in designing the RVCO pixel. In an array of RVCO pixels each pixel is reset to a value. This value should be picked wisely, otherwise the pixel will not oscillate or the output response of the pixel will not be linear. This issue is addressed by resetting each pixel to the voltage in the middle of the linear range of the

frequency-voltage plot plus the threshold voltage of the reset TFT. This plot is attained by characterising the array. Another important issue is that after resetting the pixel, it is time for integration of the X-ray incoming signal. This signal should not saturate the pixel which doesn't for this design. These will be discussed further in future chapters.

Pixel area is determined by the application. In this thesis the target application is protein crystallography and the area needed for each pixel is given by protein crystallography requirements. This requirement is addressed in this design and will be discussed further in the future chapters.

Frequency of oscillation is the most important component in designing the RVCO pixel. This frequency should be high enough to extract the signal from the output data easily and also to get a high signal to noise ratio. For a-Si technology which is used in this research, frequencies up to some hundred kHz are achievable (in the industry standard fabrication). However, frequencies in the range of some kHz are sufficient enough to meet all the requirements.

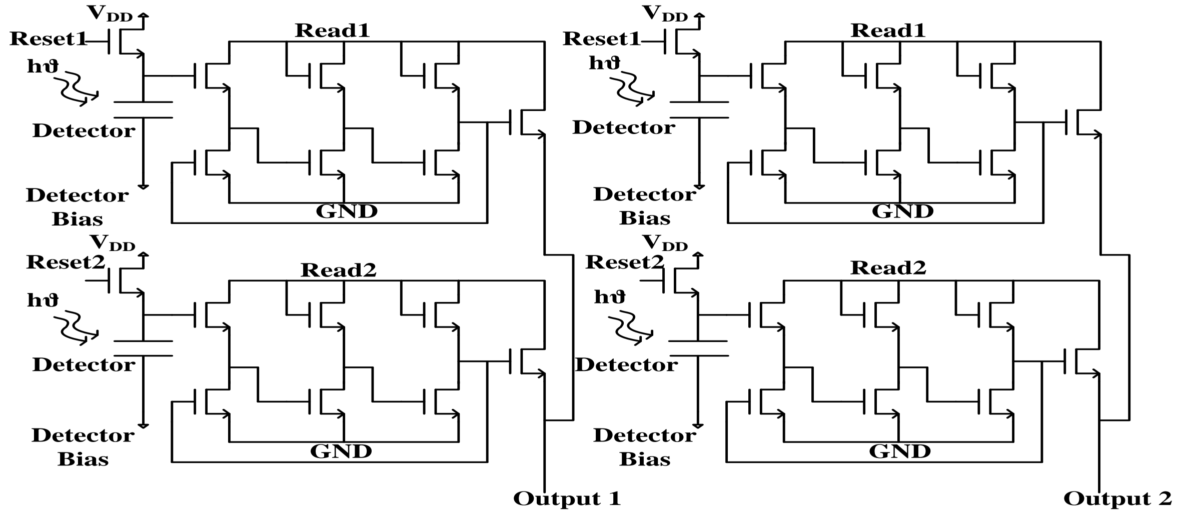
The specific design constraints and results of the single pixel RVCO will be given in future chapters.

4.2 RVCO Array Structure and Operation

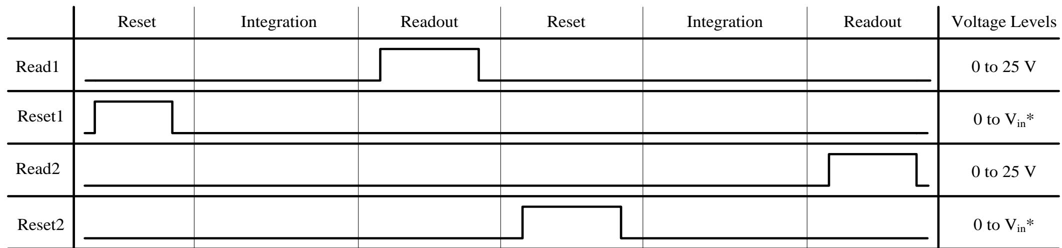
The array structure is nearly the same as the passive pixel sensor (PPS) [1][2], and active pixel sensor (APS) [3] array structures. This architecture consists of overlapping lines between the pixels for controlling the pixels and reading the data out of them. Each RVCO consists of a core and two extra TFTs (Figure 18 (a)). The six TFTs in the middle of the single pixel (Figure 18 (a)) make a three stage RVCO. The single TFT on the top left hand side of the RVCO in

Figure 18 (a) is used to reset the input of the pixel after each readout. The single TFT on the top right hand side of the RVCO in Figure 18 (a) is nothing but a common drain amplifier to isolate the output of the RVCO from the off-panel circuit. As it has been discussed in the previous chapters, this is to reduce the fix pattern noise and to omit the loading effect at the output of the RVCO. In other words, it eliminates any change in the frequency of oscillation of the pixel due to loading effect. Also, it isolates the pixel from the off-panel readout circuitry which cancels any noise effects from the output to be transferred into the pixel (This is due to the gate oxide isolation of the common drain TFT). Therefore, this cancels out any change in the frequency of oscillation of the pixel due to the noise sources from the off-panel readout circuitry.

The timing diagram and a simple 2×2 array structure of RVCOs are shown in Figure 19. The readout is done in a traditional row column addressing way. Each column output signal of the array is connected to an off-panel readout circuit. Off-panel readout circuit architectures in Figure 20 (b) and (c) are used in this research for ease of measurements. Figure 20 (a) shows a sample off-panel circuit structure that has to be used for industrial level readout. The circuit in Figure 20 (a) consists of a buffer followed by a comparator and a counter. Note that the 100nF capacitor is used to eliminate the DC component of the signal. This architecture is proposed to be used in industrial level readout. The circuit in Figure 20 (b) consists of a current amplifier followed by spectrum analyzer. This circuit is only used for single pixel testing and testing the pixels one by one in an array to make sure all of them are functioning. The circuit shown in Figure 20 (c) is a trans-impedance stage (current amplifier) followed by NI card for data collection. Matlab is used for DFT (Discrete Fourier Transform) implementation and quantifying the output spectrum in dBm. For simplicity of measurements, the readout is done for each row at a time. For example, the testing of the first row is done, then the second row, and so on.



(a)

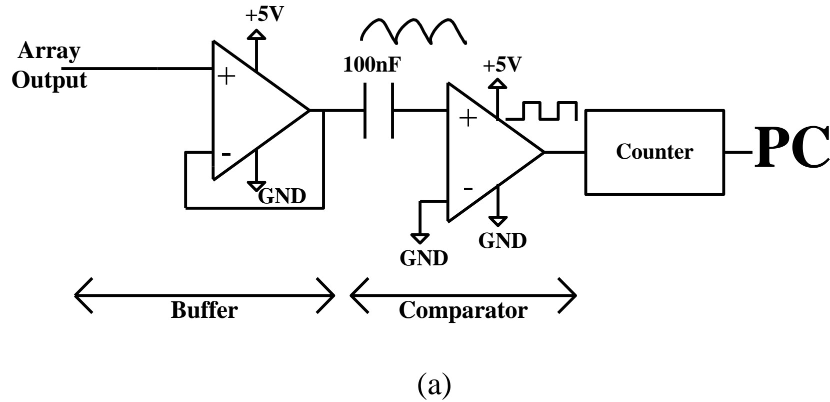


(b)

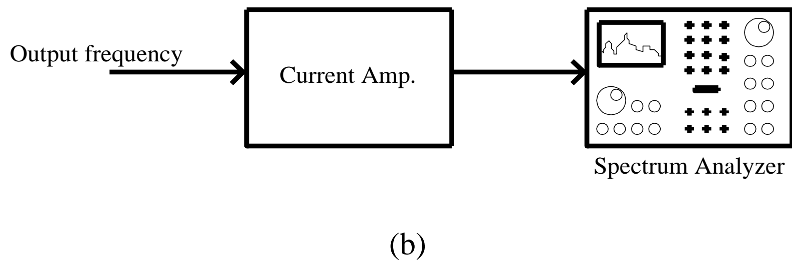
Figure 19. Schematic of a 2 by 2 array (a), operation of the array (b) (V_{dd}=25 V). Read and Reset signals are controlled row by row and the readout is done column by column (*Vin* is the middle voltage of the linear range of the frequency-voltage plot plus the threshold voltage of the reset TFT).

There are three modes of operation for each pixel. 1) **Reset mode:** In this mode the reset TFT is on and the RVCO is off (which reduces the fringing effect), resulting in the input node to reset to $V_{pix} = (V_{in} - V_{t-reset})$, where $V_{t-reset}$ is the threshold voltage of the reset TFT. 2)

Integration mode: In this mode the reset TFT and the RVCO are both off and the detector accumulates the signal in the input capacitor. This brings about a slight change in the input voltage. 3) **Readout mode:** In this mode the VCO will be turned on and the reset TFT is kept off. This allows the circuit to start oscillating with respect to the input voltage.



(a)



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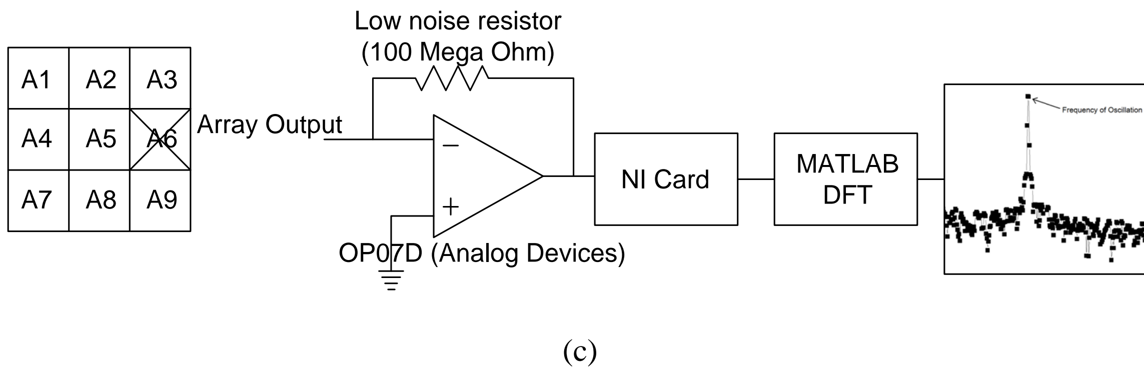


(c)

Figure 20. The different readout circuits used for RVCO pixel and array readout.

The layout of the 3 by 3 and 24 by 21 arrays fabricated in-house at the University of Waterloo are given in Figure 21. Only the 3 by 3 array is tested in this research. The 24 by 21 array was accidentally cut through in the dicing process. As it can be seen, the 3 by 3 array has a huge active area compared to the 24 by 21 array. Both of these arrays are 1 cm^2 and therefore, the 3 by 3 array has a huge active area for each pixel. The passive area sizes are the same for both of the arrays.

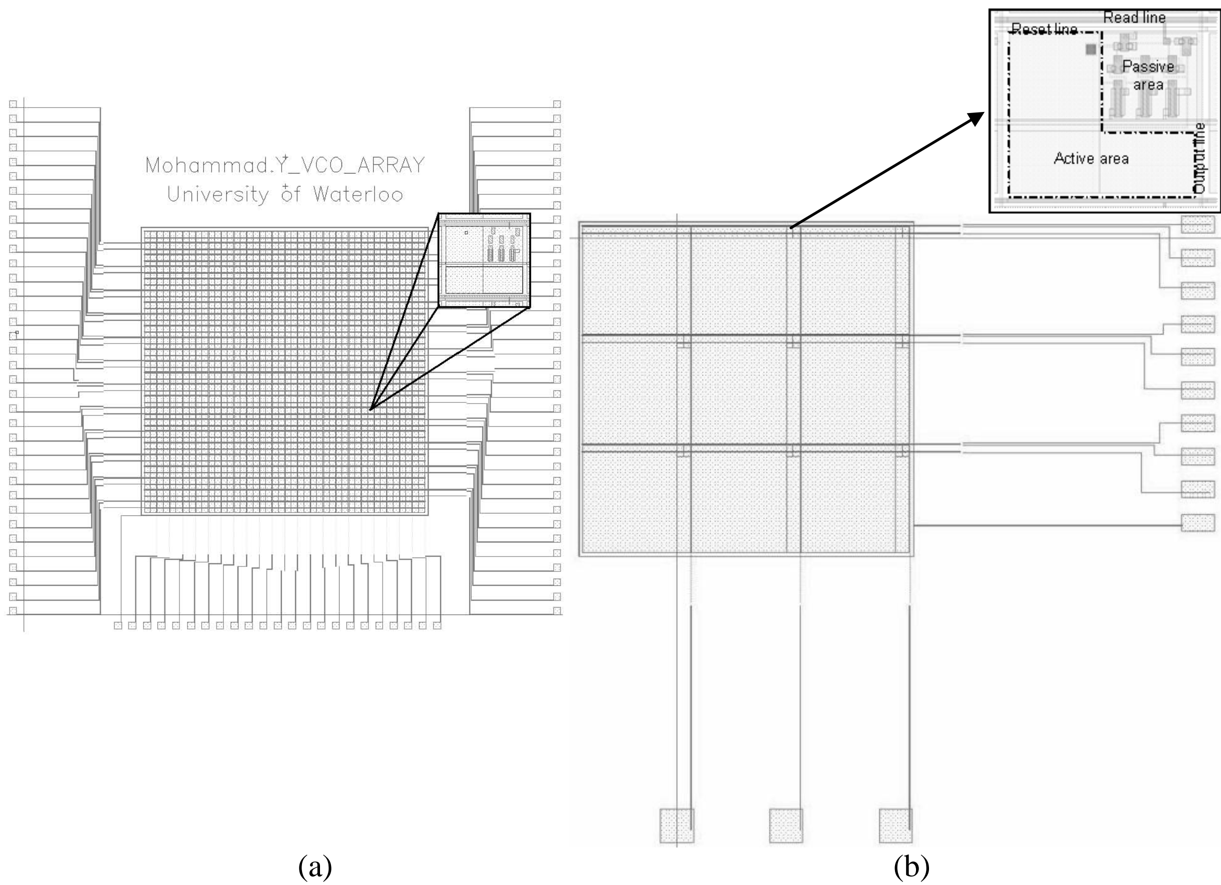


Figure 21. Layout of the 24 by 21 RVCO array (a) and 3 by 3 array (b).

4.3 Ultra Low Noise RVCO Structure and Operation

The ultra low noise RVCO pixel architecture is based on the idea of cancelling the reset noise in the pixel as given in [49]. As it was discussed before, the major noise sources in the RVCO are: **data line noise** which includes all the noise sources in the data line plus the noise sources in the off-panel readout circuit. This noise is cancelled out by use of the on-panel buffer as the details were discussed before. **Phase noise** in the RVCO is the most important noise source in the RVCO pixel. This noise will be thoroughly analyzed (simulated and measured) in the future chapters. **Jitter** in the RVCO is another noise source which will be discussed in the future chapters. The analysis done for the jitter shows that this noise source can be ignored. This is because of the parameters used for RVCO design and the way the pixel is readout (timing). **Reset noise** at the input capacitor of the pixel is the last noise source in the RVCO pixel. However, reset noise is a major component of the noise at the input of the pixel.

Reset noise is around 125 electrons on a 200 fF capacitor ($\sqrt{\frac{kT}{C}}$). However, there are ways to eliminate this noise. One way is to reset the pixel after every 100 frames. This results in no reset noise in 99 frames and we only have noise in 1 frame and the data for that frame can be ignored. We can do this since we have a slight change in the frequency of oscillation in each frame; in other words, the amount of voltage change on the input capacitor after each frame is very small and therefore even after 100 frames, the input capacitor is not going to be charged up to a value that causes the RVCO to work outside the linear range. The VCO architecture is aimed at low incident X-ray fluence protein crystallography (6-20 keV X-ray photons); therefore, the maximum change for a single 20 keV photon in the voltage at the input capacitor (of 200 fF) is expected to be around 320 uV (assuming an X-ray to charge conversion gain of 50 eV per

electron hole pair yielding on average 400 electron hole pairs created for a 20 keV photon in a selenium X-ray detector) during each frame. Moreover, the dark current of the amorphous selenium detector in 33 us period (integration time) for one frame is changing the voltage on the input capacitor (of 200 fF) by 26.5 mV (using a simple formula this can be calculated, $It=CV$, where I is the current, C is the input capacitor, t is the integration time and V is the change in the input voltage). During the reset period (which can be set to occur after every 100 frames), the voltage of the input capacitor can be designed to reach the middle of the linear range of the frequency-voltage characteristic of the RVCO. This means after 100 frames, even if the input signal is maximum for all the frames, the amount of change in the input voltage of the capacitor is as small as 2.68 V (100×(26.5 mV+ 320 uV)). The RVCO pixel is designed to work in the linear range for a span of 6 volts. Therefore, the RVCO pixel, even with 2.68 V change in the input voltage, definitely works in the linear range.

Another way to address the reset noise and cancel it out is to use the architecture used in Figure 22. In this figure the RVCO pixel is on the right hand side and a switch cap configuration is connected to it, which is shown on the left hand side. The timing of this pixel architecture is shown in Figure 22 as well. The pixel operates as follows: First Reset and Reset_2 signals are pulsed, which results in the C_1 to reset. Then the Reset_2 signal is set to 0 V which isolates the detector (a-Se) and C_1 from the RVCO pixel. The integration starts a bit after setting the Reset_2 signal to 0 V. In the meantime, Reset signal is kept high to keep the input of the RVCO pixel (gate of TFT 3) at the reset value. Before setting the Reset signal to 0 V, the Read signal is pulsed resulting in the readout of the reset value. Therefore, the reset value is sampled which includes the Reset noise. Then the Reset signal is set to 0 V and after the integration period is over, the Reset_2 signal is pulsed. This transfers the X-ray generated data on the C_1 to the

capacitor at the gate of TFT 3 (which is the gate capacitor of TFT 3). Then the Read signal is pulsed again and the signal is read. This signal is the sum of the reset value and the X-ray generated signal. Thus by subtracting this signal by the reset value readout at the first readout period, the reset noise as well as the threshold variations in the reset and input transistors are eliminated.

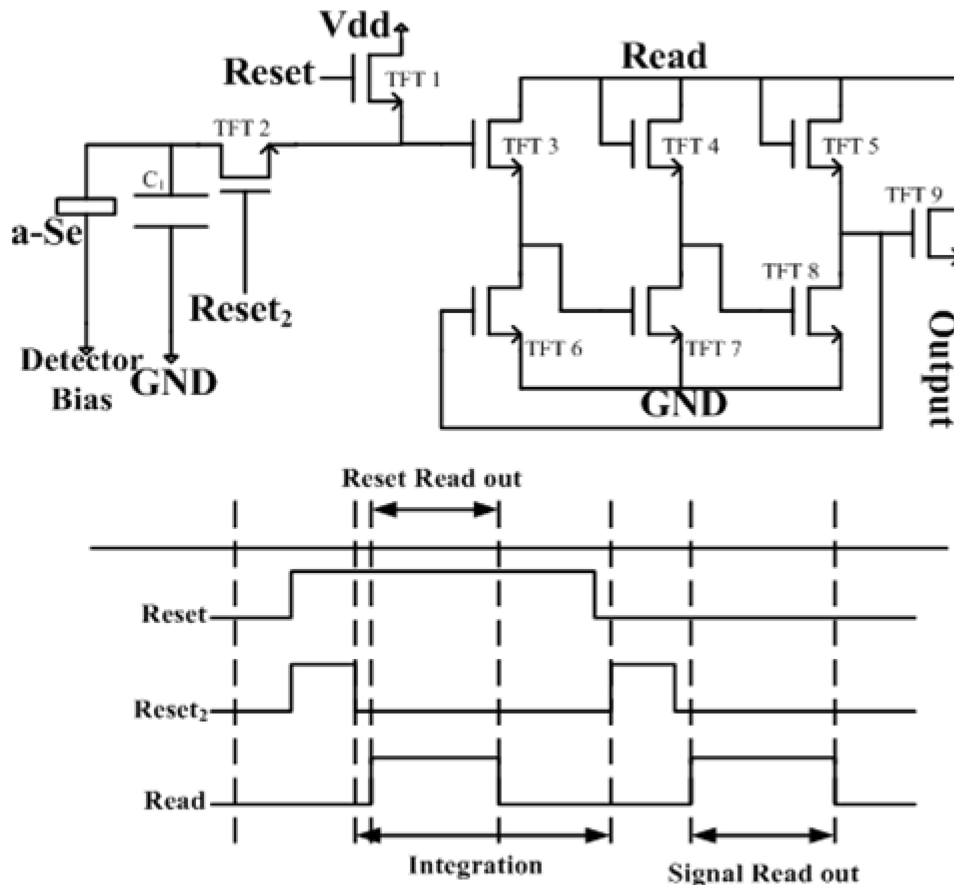


Figure 22. Ultra low noise RVCO structure and timing diagram.

Correlated Double Sampling (CDS) technique can be used as well. In CDS technique, the original RVCO pixel shown in Figure 1 is used. First the RVCO is reset and the reset voltage is readout and then the X-ray builds up a signal on the input capacitor and the signal is readout again. But, the problem is the readout time of the RVCO. If a tiny difference in the frequency of

oscillation is meant to be measured, a long readout time will be required which causes the CDS not to be a true CDS. A true CDS needs the readouts to be done so close to each other that they are correlated and the subtraction of the readouts eliminates the reset noise. However, this technique is never getting rid of the reset noise and the fixed pattern noise completely. In the case of long readouts, the readouts are so far away from each other in terms of time. Therefore, CDS results in increasing the reset noise by a factor of $\sqrt{2}$ [49].

Hence the only way to cancel out the reset noise and the fixed pattern noise due to the V_t (threshold voltage) change of the reset and input TFTs is the way used in Figure 22.

Therefore in an ultra low noise pixel architecture the only important noise source is the phase noise, since all other noise sources are canceled out. In the future chapters, this noise will be discussed in detail and input referred electronic noise will be simulated and measured.

5 Fabrication Process

This process took most of the time for this research. Fabrication is one of the most important steps in implementing a device. This is because a slight error in the fabrication process might cause the whole design to fail. For this research, 10 fabrication runs were done. 6 of these runs failed due to design errors, layout errors or fabrication errors. The fabrication process used for this research is a top gate 6-mask a-Si TFT fabrication process (top gate is used for ease of fabrication, as well as performance). Each step of the process is characterized and then used in the actual TFT fabrication process. The actual fabrication process is a 4 day to a week run based on how each step goes and how the facility operates at the time. The fabrication process is shown in this chapter step by step.

The fabrication steps are as follows: 1) a 100-nm Chromium thin film was prepared by sputtering, followed by a 50-nm heavily doped nanocrystalline thin film derived by Plasma Enhanced Chemical Vapor Deposition (PECVD). The double layers were patterned through the first mask for source and drain contacts of the top-gate TFT on a carefully cleaned Corning 1737 glass substrate; 2) amorphous silicon, silicon nitride, and Molybdenum thin films were deposited by PECVD and sputtering consecutively. The triple layers were then patterned and etched though the second mask to define channel and gate of the TFT. In the meantime, the bottom electrode of the storage capacitor was also formed using the same mask; 3) a 300-nm silicon nitride thin film as the dielectric layer of the storage capacitor was deposited by PECVD; 4) contact holes were

opened by the third mask photolithography and wet chemical etching to expose the gate of the TFT for the interconnect metal; 5) a 500-nm Aluminum layer was sputtered as the interconnect metal as well as the top electrode for the storage capacitor and patterned by the fourth mask photolithography; 6) a 2-μm low-k polyimide dielectric material was spin coated as an isolation layer. A via was opened through the fifth mask and Chromium film was used as the dry etching stop layer; 7) Finally, a 1-μm Aluminum film was deposited by sputtering and defined for the bottom electrode contact of the a-Se layer though the sixth mask.

In the following sub chapters each mask is discussed thoroughly.

5.1 Mask 1

After deposition of a 100-nm Chromium thin film by sputtering followed by a 50-nm heavily doped nanocrystalline thin film (n+ nc-Si:H) deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD), the first mask was used to form the drain and source contacts of the TFTs. n+ nc-Si:H layer was used to decrease the contact resistance between the metal and the a-Si layer. After lithography the n+ nc-Si:H was etched by Reactive Ion Etching (RIE) and the chromium is etched using chromium etchant. These processes are shown in Figure 23.

As it can be seen from Figure 23, mask 1 is used to etch n+ nc-Si:H and Chromium. Before the next step of fabrication (which is the double layer deposition), a few seconds of Buffered HF (BHF) (or 2% HF if exercise extreme care) dip will be required. This etches away the oxide formed on top the n+ nc-Si:H layer. The oxide on top of the n+ nc-Si:H layer increases the contact resistance of the fabricated TFTs resulting in low quality TFTs. This step has to be done with extreme care since HF is a dangerous acid.

Note that drain source contact metals can be a wide variety of metals. Chromium is picked in this case to achieve a higher performance and ease of fabrication. Other metals that can be sputtered in G2N lab at the University of Waterloo are Aluminum and Molybdenum. Figure 24 shows the mask 1 used for this fabrication process.

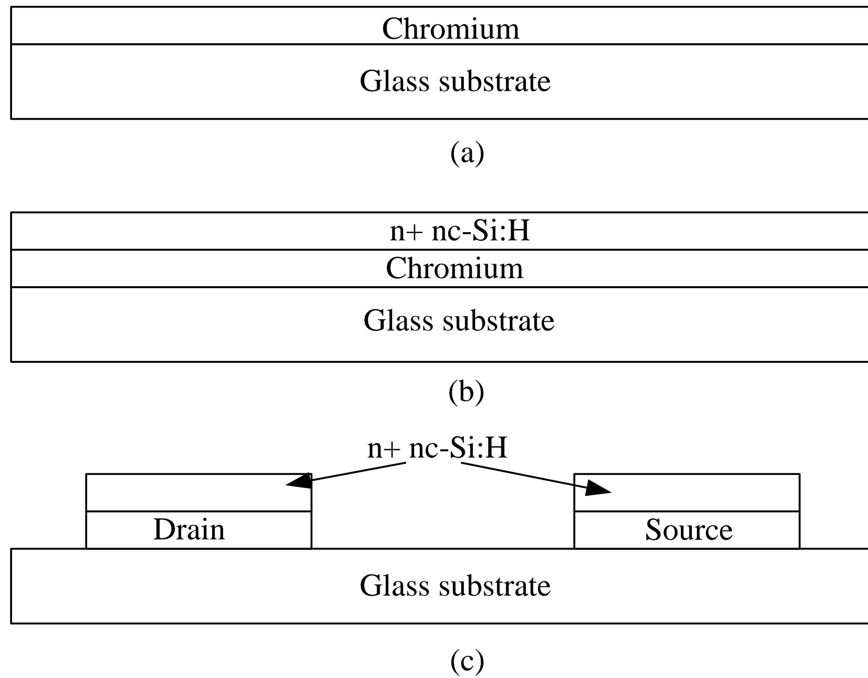


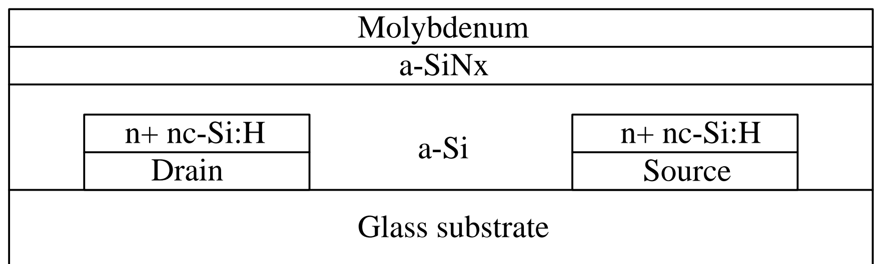
Figure 23. Chromium deposition (a), n+ nc-Si:H layer deposition (b), using mask 1 and etching Chromium and n+ nc-Si:H layer to form drain and source contacts (c).

Figure 24. Mask 1 used for this fabrication process.

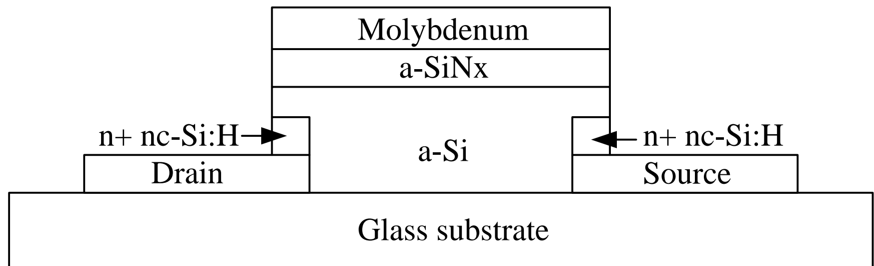
5.2 Mask 2

After deposition of amorphous silicon, silicon nitride (a-SiN_x), and Molybdenum thin films by PECVD and sputtering consecutively. Mask 2 is used to etch a-Si, a-SiN_x and Molybdenum. This forms the channel and the gate contact of the TFTs. Moreover, this step patterns the bottom electrode of the pixel capacitor (storage capacitor), if there is any. Etching is done by PAN and RIE for Molybdenum and double layer (a-Si and a-SiN_x), consecutively.

Figure 25 shows these processes step by step. Note that any other metal can be used for the gate contact. In this fabrication run Molybdenum is used to increase the performance of the TFTs.



(a)



(b)

Figure 25. a-Si, a-SiN_x and Molybdenum deposition (a), Using mask 2 and etching n+ nc-Si:H a-Si, a-SiN_x and Molybdenum (b).

Figure 26 shows mask 2 used for this fabrication process.

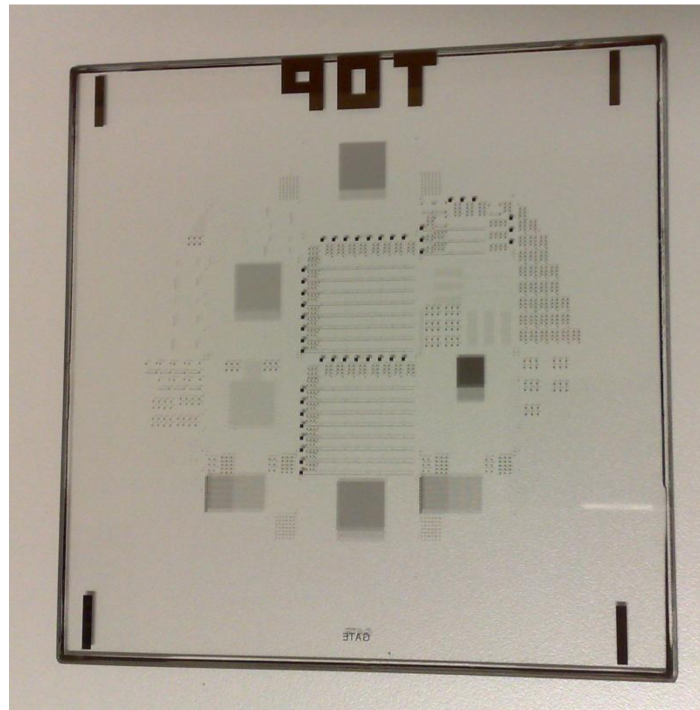
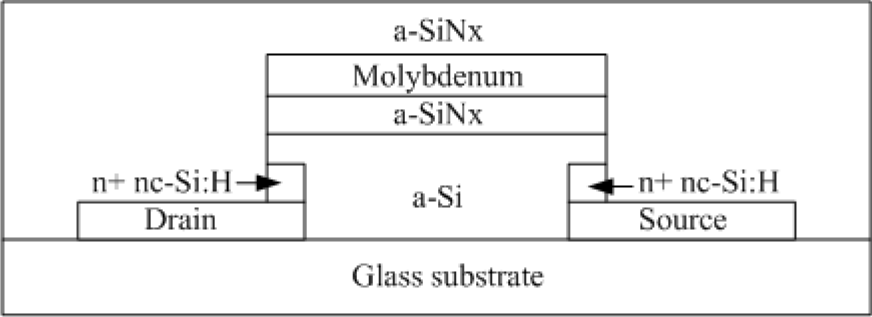


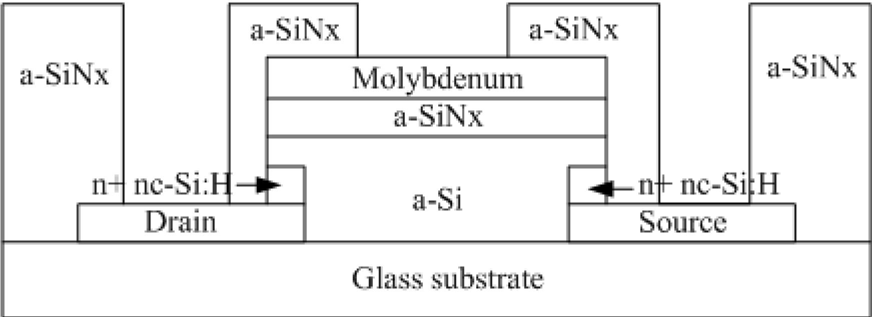
Figure 26. Mask 2 used for this fabrication process.

5.3 Mask 3

Then, a 300-nm silicon nitride thin film is deposited by PECVD. This a-SiN_x layer is used as the dielectric for the storage capacitor on the pixel, if there is any. After that contact holes are opened using mask 3, lithography and wet etch. This exposes the gate, source and drain metals for the interconnecting metal. Figure 27 shows these processes step by step. Figure 28 shows mask 3 used for this fabrication process.



(a)



(b)

Figure 27. a-SiN_x deposition (a), opening via for interconnecting metal using mask 3 (b).

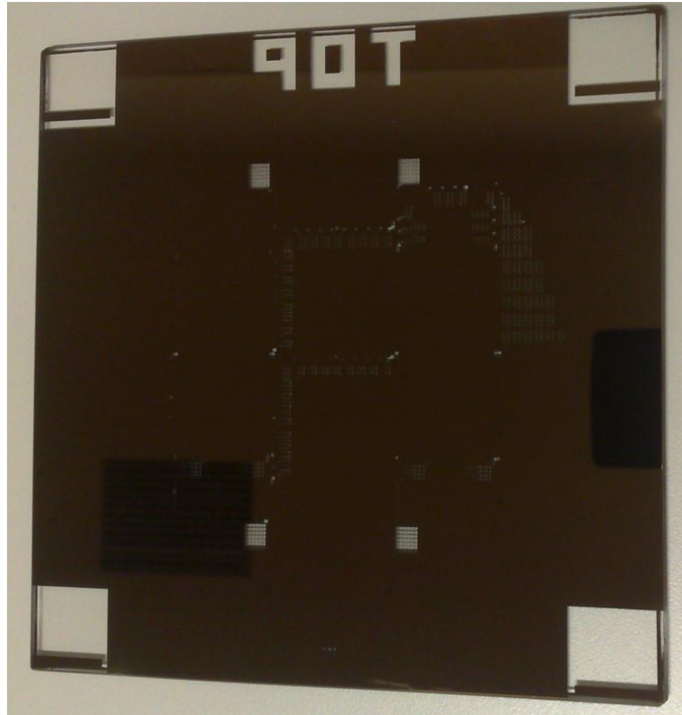
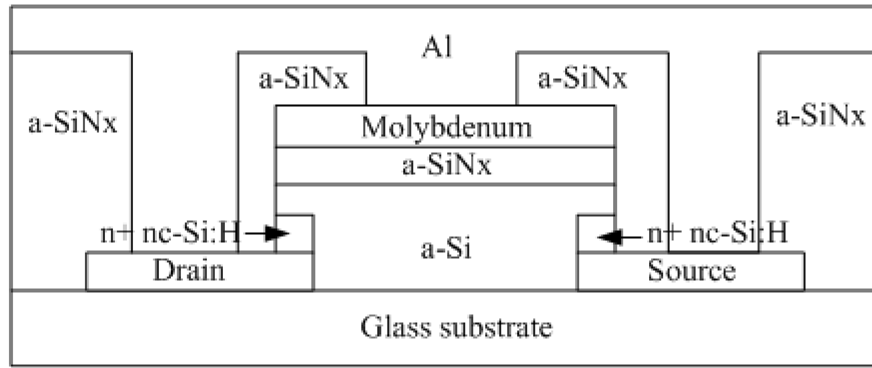


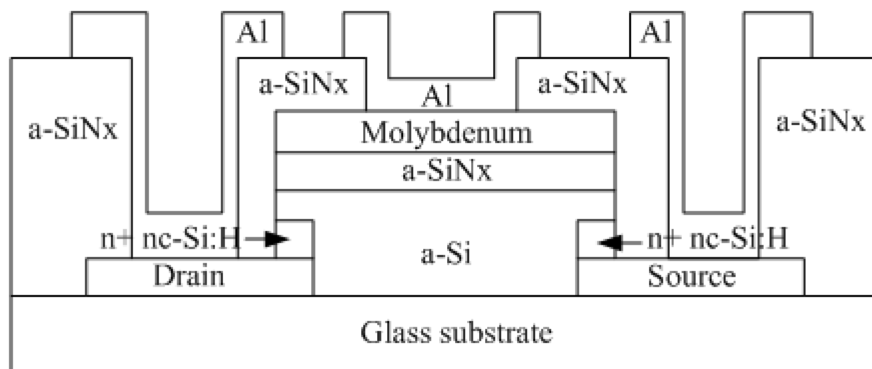
Figure 28. Mask 3 used for this fabrication process.

5.4 Mask 4

Next a 500-nm Aluminum layer is sputtered as the interconnecting metal. This metal forms the top electrode for the storage capacitor (if there is any) as well. Then, this layer is patterned using mask 4, lithography and PAN etching to etch Aluminum. These fabrication processes are shown in Figure 29 step by step. Figure 30 shows mask 4 used for this fabrication process.



(a)



(b)

Figure 29. Al layer deposition for interconnecting metal (a), using mask 4 and patterning the interconnecting metal (b).

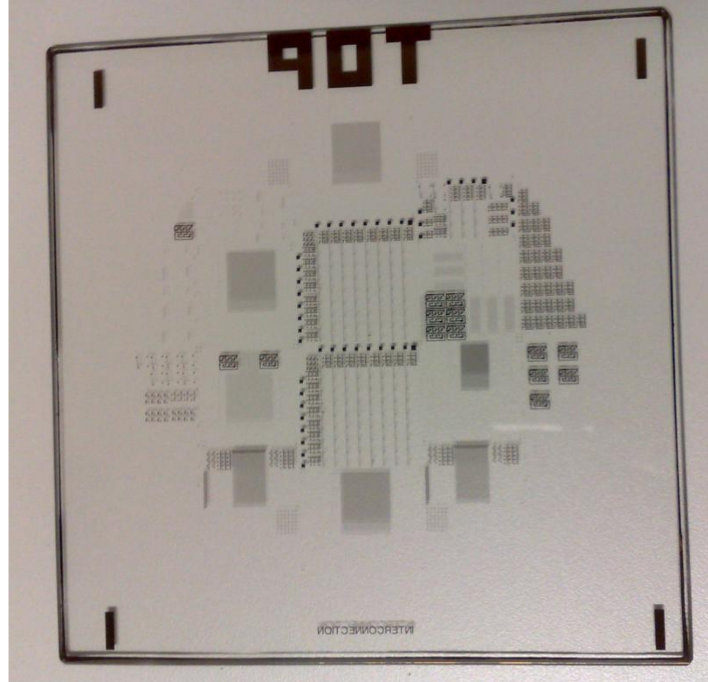
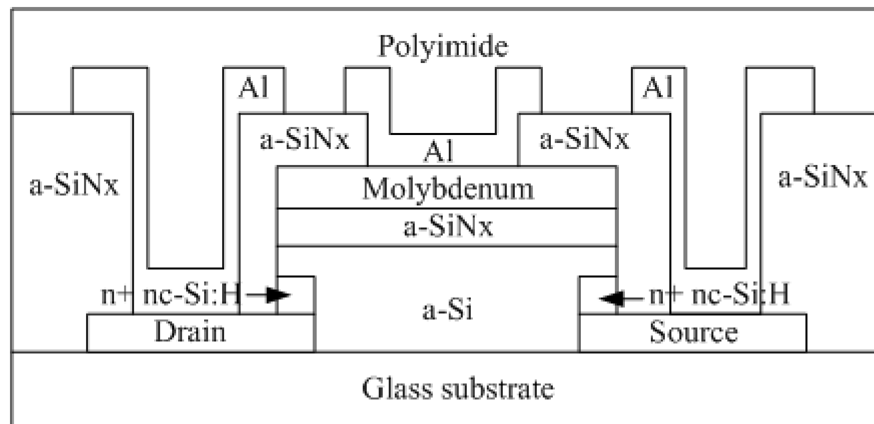


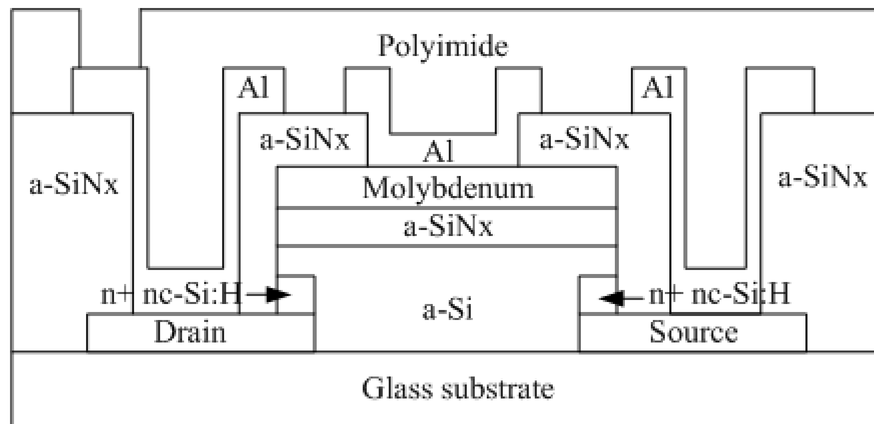
Figure 30. Mask 4 used for this fabrication process.

5.5 Mask 5

Then a 2-μm low-k polyimide dielectric material is spin coated as an isolation layer. After that a via is opened using mask 5. This via exposes the interconnecting metal for the bottom electrode connection of the a-Se layer (detector layer). Note that Chromium film was used as the dry etching stop layer. These fabrication processes are shown in Figure 31 step by step. Figure 32 shows mask 5 used for this fabrication process.



(a)



(b)

Figure 31. Polyimide coating using spinning (a), etching polyimide using mask 5, lithography and RIE (b).

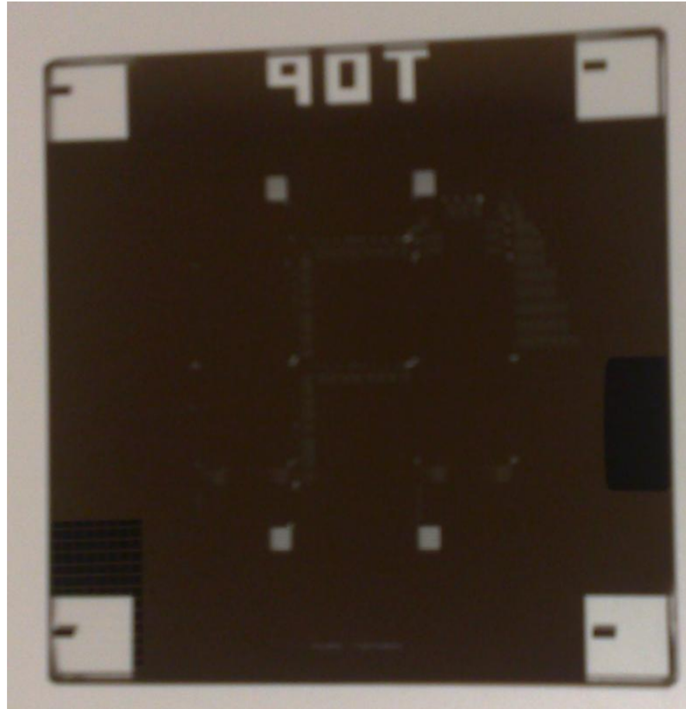
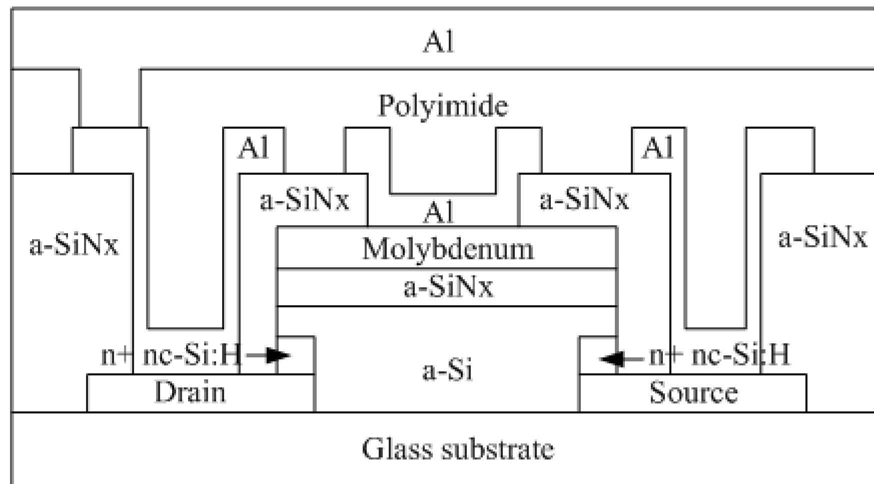


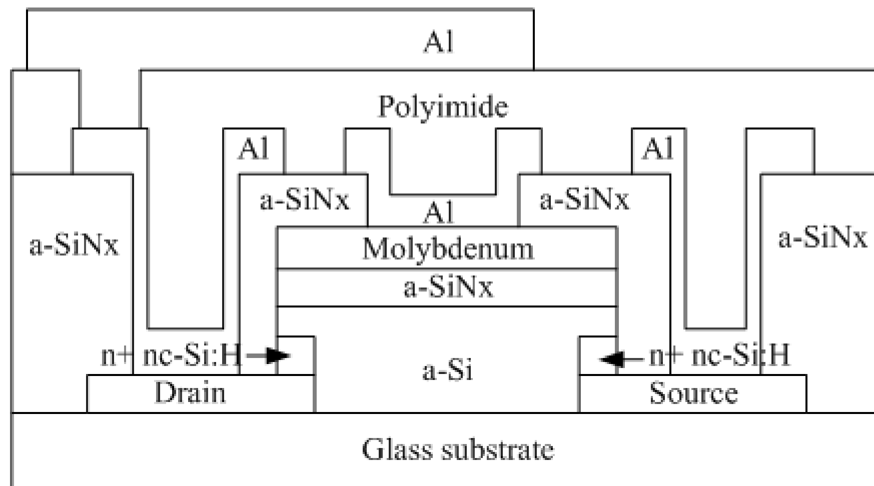
Figure 32. Mask 5 used for this fabrication process.

5.6 Mask 6

Lastly a 1-μm Aluminum film is deposited by sputtering. Then it is patterned using mask 6, lithography and PAN etching. These fabrication processes are shown in Figure 33 step by step. Figure 34 shows mask 6 used for this fabrication process.



(a)



(b)

Figure 33. Al sputtering for the bottom electrode contact of a-Se (a), Al layer patterning using mask 6 (b).

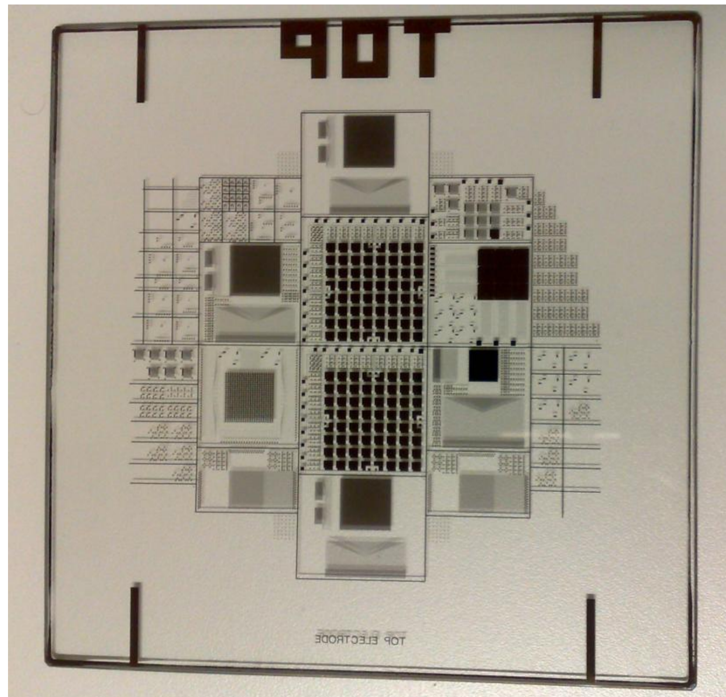


Figure 34. Mask 6 used for this fabrication process.

5.7 In-House Fabricated Sample

For this process a number of designs are fabricated on the same run. As it can be seen in Figure 35, different structures have been implemented on the same run. Therefore, the layout includes the layout of all of the different designs. Figure 35 shows the final result of the in-house fabricated TFT process.

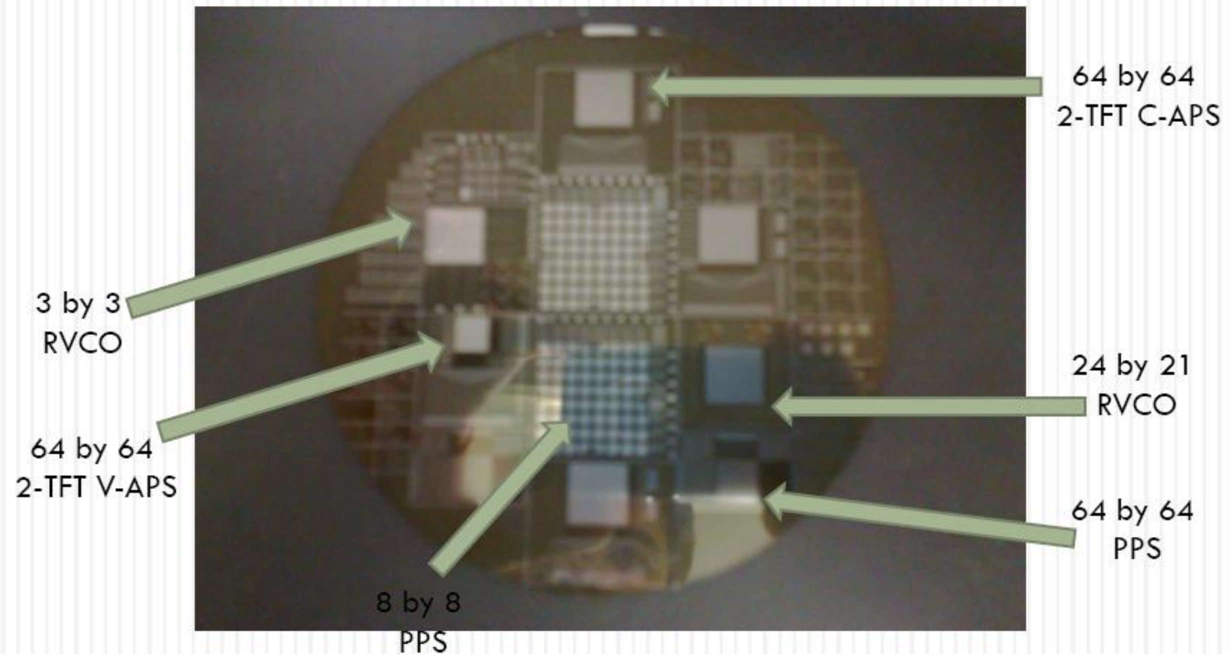
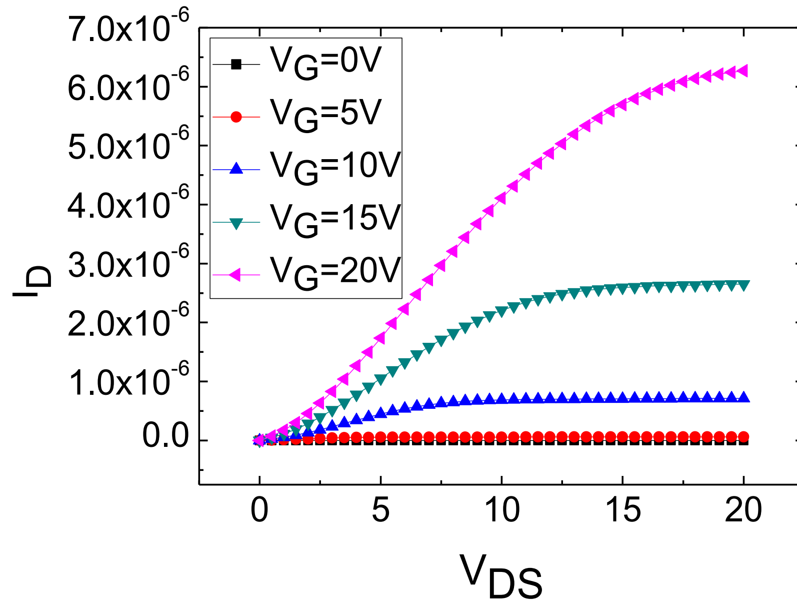


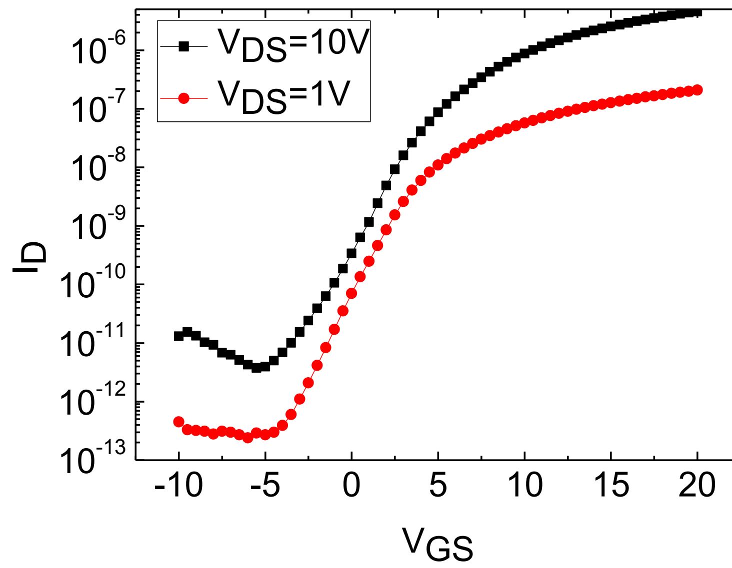
Figure 35. The in-house fabricated TFT process in University of Waterloo.

5.8 Single TFT Results

A single TFT characteristics of the in-house fabricated process at the University of Waterloo is shown in Figure 36. From these graphs, the simulation and measurement parameters are extracted, such as mobility of the TFTs, threshold voltage of the TFTs and etc.



(a)



(b)

Figure 36. Transfer (a), and Output characteristics of single in-house fabricated TFT (W/L=500µm/50 µm). This TFT was fabricated in the same run as the RVCO array (b).

5.9 Fabrication Conditions

Table I shows the fabrication conditions for this TFT run.

Table I. Fabrication conditions for in-house fabricated TFT process at the University of Waterloo.

Process	System	Temp (°C)	Gas/Target	Pressure	RF	Thickness(nm)	Mask	Etchant
Chrome deposition	Edwards	Room	Ar	5	-	100	-	-
n+ nc-Si:H deposition	WLO1	400	PH_3, SiH_4, H_2	900	2	50	-	-
n+ nc-Si:H etching	RIE	Room	SF_6, O_2	50	DC= -80	-	1	-
Chrome etching	Wet Etch	Room	-	-	-	-	1	Cr Etchant
a-Si deposition	WLO1	400	SiH_4, H_2	400	2	60	-	-
a-SiN_x deposition	WLO1	400	NH_3, SiH_4	400	2	60	-	-
Molybdenum deposition	WLOS	Room	Ar	5.6	300	60	-	-
Etching Molybdenum	Wet Etch	Room	-	-	-	-	2	PAN
Etching a-SiN_x, a-Si and n+	RIE	Room	SF_6, O_2	50	DC= -80	-	2	-
a-SiN_x deposition	WLO1	400	NH_3, SiH_4	400	2	300	-	-
a-SiN_x etching	RIE	Room	SF_6, O_2	50	DC= -80	-	3	-
Al deposition	WLOS	Room	Ar	9	300	500	-	-

Al etching	Wet Etch	Room	-	-	-	-	4	PAN
Polyimide spinning	Spinner	Room	-	-	-	2000	-	-
Polyimide etching	RIE	Room	SF_6, O_2	50	DC= -80	-	5	-
Al deposition	Edwards	Room	Ar	5	-	1000	-	-
Al etching	Wet Etch	-	-	-	-	-	6	PAN

5.10 a-Se Layer Deposition

The a-Se layer recipe used for a-Se layer deposition was not good enough and therefore, the deposited a-Se layer peeled off. The a-Se layer is not the focus of this research. The focus of this research is to demonstrate that the fabricated circuit is working and also show a pixel level result using a-Se layer. This has been done by using a discrete a-Se layer and connecting it by wire-bonding to the bottom electrode contact. Figures in the future chapters show the in-house fabricated single RVCO pixel, 3 by 3 RVCO array and the failed attempt to deposit a-Se layer on top of the array.

Different layouts of RVCO pixel and array were used for fabrication. The 24 by 21 RVCO array was cut through by accident in the dicing process and is not suitable for testing. But testing and measurements are thoroughly done for the single pixel and array without a-Se layer and also the single pixel interacted with a-Se layer (to show that 6 keV single X-ray photons are detectable by this architecture). Measurements along with simulations and analysis are given in the next chapters.

6 Phase noise, Jitter and Metastability in RVCO

6.1 Phase Noise in RVCO

As discussed before, the major electronic noise component in the RVCO is the phase noise. Methods to calculate this noise have been proposed previously [19][20]. The most accurate method proposed to date for modeling the phase noise [19] was used in this research to simulate the input referred noise of the a-Si RVCO. If the output of the RVCO has an output of the form of,

$$V_{out}(t) = A(t).f(w_0 t + \emptyset(t)) \tag{11}$$

The phase noise power spectral density in [19] is calculated as follows,

$$L_{\emptyset}\{\Delta f\} \approx \frac{8}{3\eta} \cdot \frac{kT}{P} \cdot \frac{V_{DD}}{V_{char}} \cdot \frac{f_0^2}{\Delta f^2} \tag{12}$$

The parameters used for phase noise calculations are listed in Table II. In our simulations, the proportionality constant (η) is considered 1 for simplicity. Note also that the rise time and the fall times are considered equal. In reality, they are not exactly equal, but this difference does not affect the phase noise considerably [19]. Note that the more similar the fall and rise times, the less the phase noise. The most important benefit of symmetry is that flicker noise can be eliminated from the calculations [19].

Table II. Parameters of phase noise power spectral density and their description and quantity.

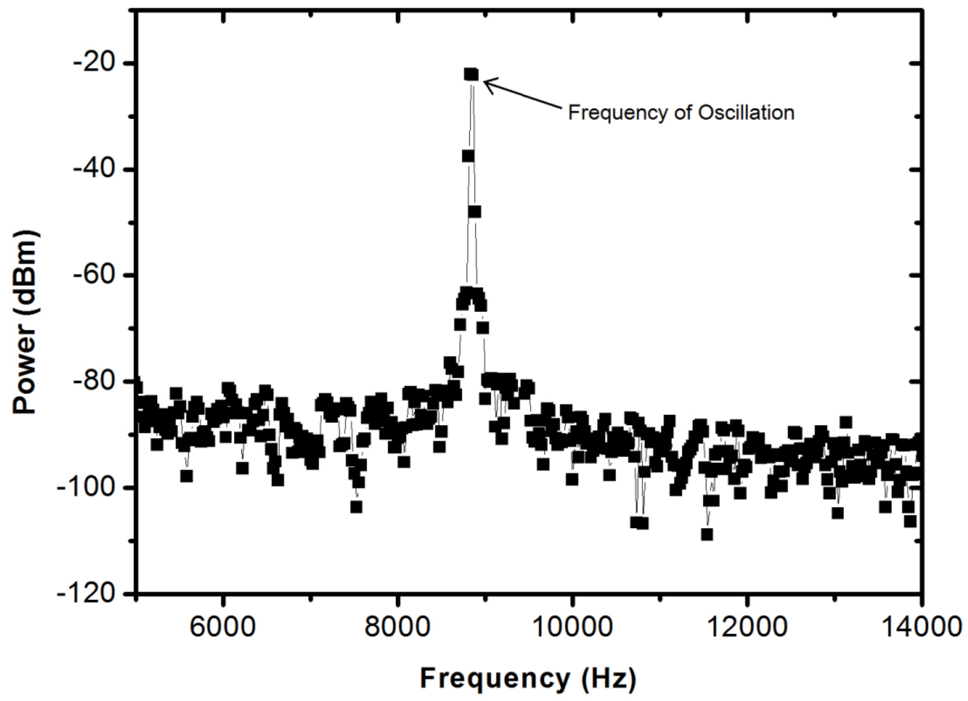
Parameter	**Description**	**Quantity (for an RVCO at 10 KHz)**
f_0	$\frac{1}{2Nt_p} = \frac{1}{\eta N(t_r + t_f)}$	10 KHz
P	$2\eta N V_{DD} q_{max} f_0$	240 nW
V_{char}	$\frac{E_c L}{\gamma} = \frac{\Delta V}{\gamma}$	7.5 V
q_{swing}	$C_p V_{swing}$	200 fC
ΔV	$\frac{V_{DD}}{2} - V_{th}$	5 V
V_{swing}	$\frac{I_{bias} t_p}{C_p}$	1 V
N	Number of stages	3
t_p	Propagation delay	16.6 us
t_r	Rise time	8.3 us
t_f	Fall time	8.3 us
γ	$\frac{2}{3}$	$\frac{2}{3}$
I_{bias}	Bias current of each stage	12 nA
k	Boltzmann constant	1.38 e-23 J/K
T	Temperature	300 K
η	Proportionality constant (Close to one)	1 s^{-1}
V_{DD}	Supply voltage	20 V
V_{th}	Threshold voltage	5 V

To calculate the input referred electronic noise, we find the relationship between the output phase noise and the input voltage change. To do so, we use the following equation (where f_m is the frequency difference from f_{osc}) [21],

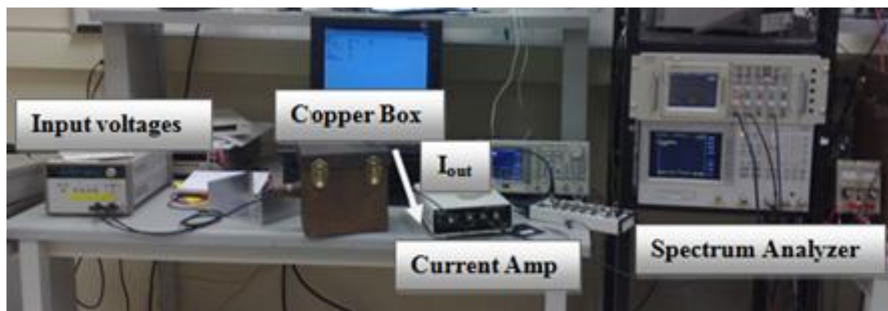
$$\Delta f = 2f_m\sqrt{L_{\emptyset}\{f_m\}}) \tag{13}$$

Substituting the numbers shown in Table II into equations (9) and (10) gives a Δf of 0.007 Hz. Considering a calculated frequency-voltage gain of 1.8 KHz/V and a nominal input capacitance at the gate of the Load1 TFT of 200 fF, will result in a theoretical value input referred electronic noise of around 5 electrons. This striking result shows that the a-Si RVCO circuit can be used to achieve photon shot noise limited large area imaging performance because of its extremely low input referred electronic noise.

The measured spectrum at the output of the circuit is shown in Figure 37 (a) (which is used for phase noise measurement) and the setup for measuring the phase noise is shown in Figure 37 (b). The value of $L_{\emptyset}\{60\ Hz\}$ can be extracted from Figure 37 (a) which is 1.121×10^{-7} and hence, Δf is 0.040 Hz. Note that the noise bandwidth is 30 Hz. Frequency-voltage gain can be obtained from Figure 38 (b) (showing the output frequency vs. input voltage) which is 1.85 kHz/V. Note that the pixel for which the Figure 38 (a) result is presented does not have high enough frequency of oscillation and is not used for other tests. Therefore, the input referred noise given the designed input capacitance of 200 fF is around 27 electrons. Although considerably better than the reported PPS and APS noise values to date [22][23], the measured RVCO noise is higher than the theoretically calculated value. This is likely due to environmental noise since the chip was tested on a bread board using long wires which causes additional parasitic capacitance and resistance (affecting both the electronic noise value and f_{osc}). If better connections were used, we expect the electronic noise value can be reduced further.

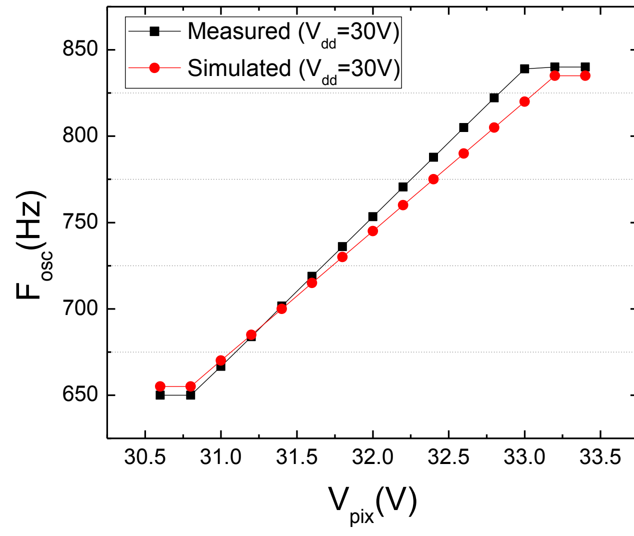


(a)

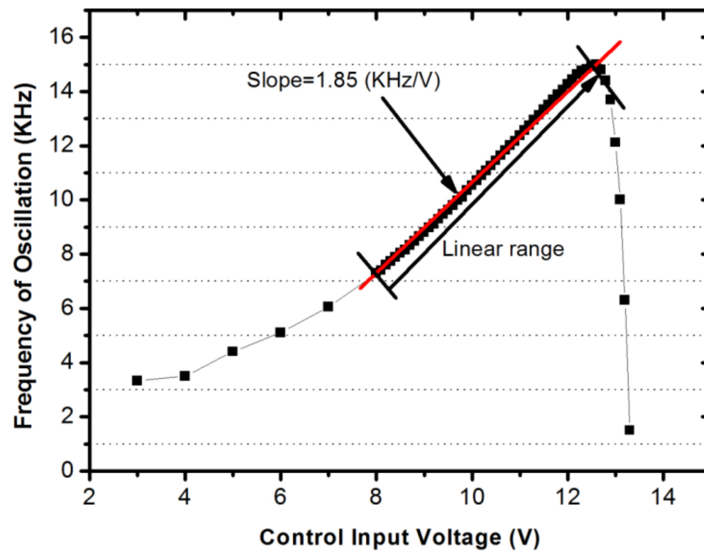


(b)

Figure 37. Power spectrum of the output of the single pixel RVCO presented in Figure 17 (b) (V_{DD} = 20 V, V_{ctr} = 9.3 V) (a), The setup for measuring the phase noise (b).



(a)



(b)

Figure 38. Frequency-Voltage characteristic of the in-house fabricated single pixel RVCO with the structure in Figure 17 (a), (a), with the structure in the Figure 17 (b), (b).

6.2 Jitter in RVCO

Jitter is another issue in RVCO that should be considered. As discussed in [19], the jitter can be described as follows,

$$\sigma_{\Delta T} = K\sqrt{\Delta T} \tag{14}$$

$$K \approx \sqrt{\frac{8}{3\eta} \cdot \frac{kT}{P} \cdot \frac{V_{DD}}{V_{char}}} \tag{15}$$

Where k is the proportionality factor for jitter. Using the parameters in table II, results in K=2.508e-8. In protein crystallography the output should be read in some seconds. So this jitter is important in the interval of 0 to some seconds which can be assumed to be negligible due to the small K.

6.3 Metastability in RVCO

Metastability is a concern in a-Si TFT circuit architectures and is often modeled and accounted for in software processing. This phenomenon is due to the threshold voltage of a-Si TFT changing during the continuous usage of the a-Si circuit. The causes of metastability are usually cited as charge trapping and detrapping in the silicon nitride gate dielectric and defect state creation in a-Si [24]. It has been shown that the threshold voltage change is different for various gate and drain biases [25] and their duty cycles and frequencies [26]. There are two solutions for overcoming the problem of metastability. One is minimizing the duty cycle and the other one is applying alternating positive and negative stress voltages [26][27].

The V_t shift is modeled as follows [26][27],

$$\Delta V_t(t) = \Delta V_t^+(t) + \Delta V_t^-(t) \tag{16}$$

$$\Delta V_t^+(t) = A^+ \frac{Q_G}{Q_{G0}} (V_{GS} - V_{ti})^{\propto +} (t \cdot DC)^{\beta +} \tag{17}$$

$$\Delta V_t^-(t) = A^- \frac{Q_G}{Q_{G0}} (V_{ti} - V_{GS})^{\propto -} (t \cdot (1 - DC))^{\beta -} \cdot F_{PW} \tag{18}$$

Where the time, t, is in minutes. ΔV_t^+ and ΔV_t^- show the positive and negative V_t shift, respectively. F_{PW} shows the frequency of operation and $\frac{Q_G}{Q_{G0}}$ models the charge distribution in the gate channel. The measured parameters for TFTs used in this research associated with these modeling equations are shown in Table III [28]. For simplicity again, we considered rise and fall time to be the same and the V_{GS} of each TFT is 10 volts. Note that the Duty Cycle is calculated assuming a 1000×1000 pixel array being read out row by row. In this case then, the duty cycle is 0.05% for each of the negative and positive cycles. This is because we assumed that the positive and negative cycles are equal and are each half of the operation time.

For the RVCO, the change in V_t will cause the output f_{osc} to change over long usage times. Since f_{osc} is dependent on the g_m of the load transistors and is independent of g_m of the drive transistors, we can say that only the V_t shift in the load transistors have an effect on f_{osc}. By looking at the configuration of the three stage RVCO, we conclude that the V_t shift of the load transistors of the second and the third stages are the same because they will experience exactly the same situations. But for the first stage, which is our input, we will have a different level of V_t shift. Also for the last two stages mentioned above, there would be only a positive V_t shift. This is because during the negative cycle of each of these stages, the output voltage of the stage is (V_{DD}-V_t) which results in the term (V_t-V_{GS}) in the negative V_t shift formula to be zero ($V_{GS} = V_{DD} - V_{DD} + V_t = V_t$). Moreover, for positive V_t shift, we consider the charge ratio as well, because the drain and source voltages are different [25].

For the first stage the V_t shift modeling is more complicated. We assume that the first stage experiences both positive and negative V_t shifts. The negative V_t shift is caused by the reset TFT. The reset TFT always experiences a negative gate bias except during the reset period. So the reset transistor has both positive and negative V_t shifts. These two shifts could theoretically be designed to cancel out each other [29], but this needs experimental verification. However, for simplicity, we assume that this change in V_t of the reset transistor is negligible compared to V_{DD} due to the low duty cycle of the reset signal. Therefore we can estimate the gate voltage of the first stage load transistor is always V_{DD}. For the first stage of TFT we will also have a positive V_t shift. The reason is the same as for the TFTs in subsequent stages. Hence, for a three stage RVCO we have,

$$f_{osc} = \frac{1}{6t_P} \tag{19}$$

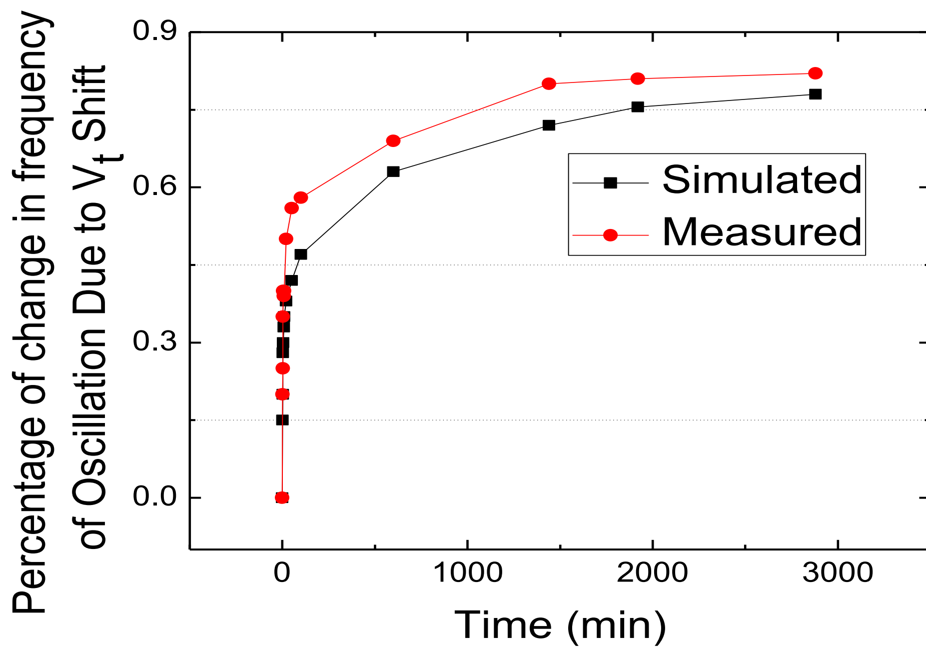
Using formulas (4) and (14) we have,

$$f_{osc} \propto \frac{1}{(V_{DD}-V_t)^{-1}} \tag{20}$$

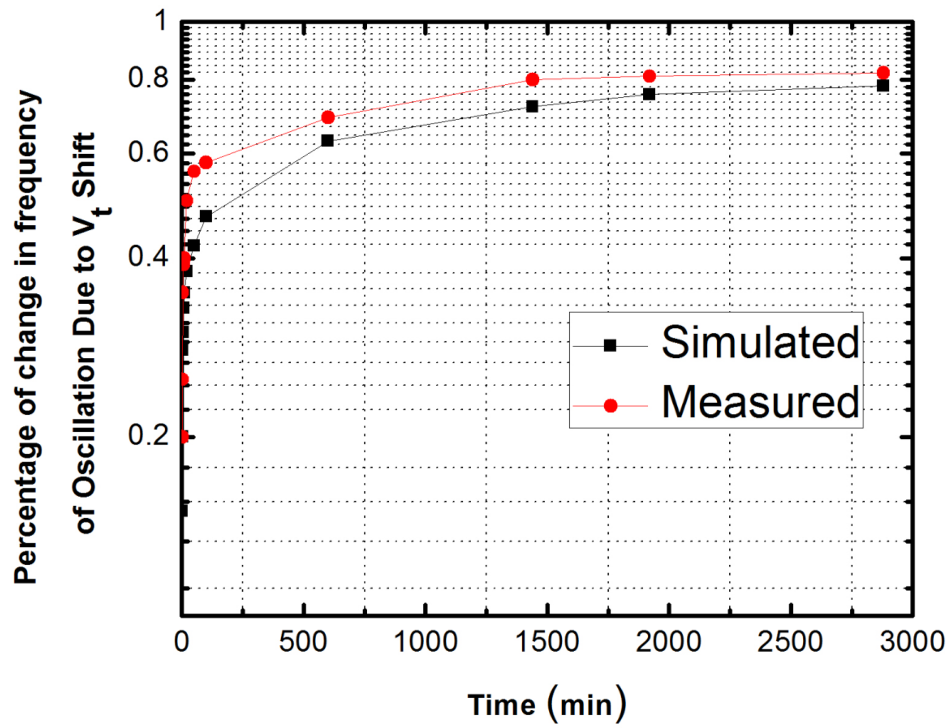
The measured change of the f_{osc} (under prolonged voltage stress) for both structures of the single RVCO pixel presented in Figure 17 are shown in Figure 39 alongside an estimation of f_{osc} due to V_t shift based on the discussion above (for simplicity $\frac{Q_G}{Q_{G0}}$ is assumed to be 1). For Figure 39 (b) which is the main focus of this research, V_{DD} is 20 Volts and V_{ti} is 5 Volts. As shown in Figure 39, the expected data is similar to the measured results for the time frame tested.

Table III. Model parameters for V_t shift calculation [28]

	Positive stress	**Negative stress**
A	9.37×10^{-3}	4.92×10^{-3}
∝	1	1.55
β	0.191	0.205



(a)



(b)

Figure 39. Measured and simulated *Vt* shift effect on the output frequency of the sample RVCO pixel over time for pixel in Figure 17 (a), (a), for pixel in Figure 17 (b), (b).

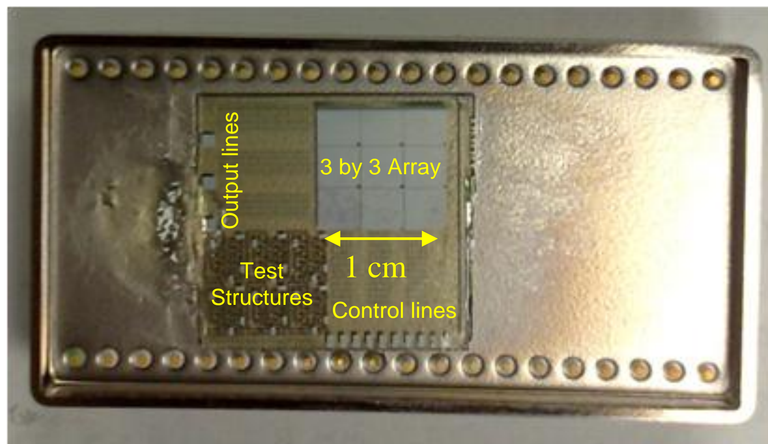
7 Measurement Results

7.1 Single RVCO Pixel Results

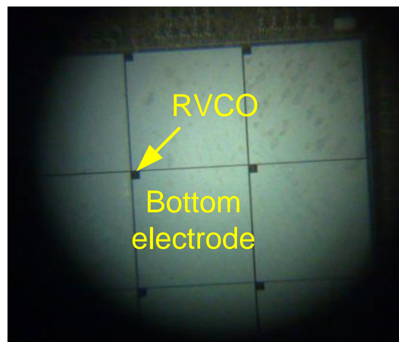
All of the measurement results are given in the previous chapters. However, they will be gathered in this section. Figure 18 shows the RVCO pixel architecture along with its layout and timing diagram. Figure 17 shows the die-micrograph of two in-house fabricated RVCO structures. Figure 20 (b) shows the off-panel readout circuit used for measurements. Figure 37 shows the testing setup as well as the output spectrum of the single RVCO pixel, which is used to extract the center frequency of oscillation as well as the phase noise. Figure 38 shows the output characteristic of the RVCO pixel as a function of its input (control) voltage. This graph is used to extract the linear range frequency-voltage gain of the pixel, as well as the dynamic range (the linear range of the graph). Figure 39 shows the measured and simulated V_t shift effect on the output frequency of the sample RVCO pixel over time. These graphs are used to characterize the single RVCO pixel's operation and to compare these results with the simulation results as it was shown in the previous chapters.

7.2 RVCO Array Results

The in-house fabricated 3 by 3 array of RVCOs is shown in Figure 40. This array has a huge bottom electrode contact connection for a-Se layer for each pixel. It has been tested and only one of the pixels is not working. The names and sizing for different TFTs are given in Figure 41 and Table IV. Figure 42 shows the off-panel output circuit used for measurements of the 3 by 3 array architecture and a sample output oscillation in time domain detected by NI card. Note that for ease of measurements readout is done one row at a time.



(a)



(b)

Figure 40. In house fabricated 3 by 3 RVCO array in the package (a), zoomed in version of the 3 by 3 RVCO array (b).

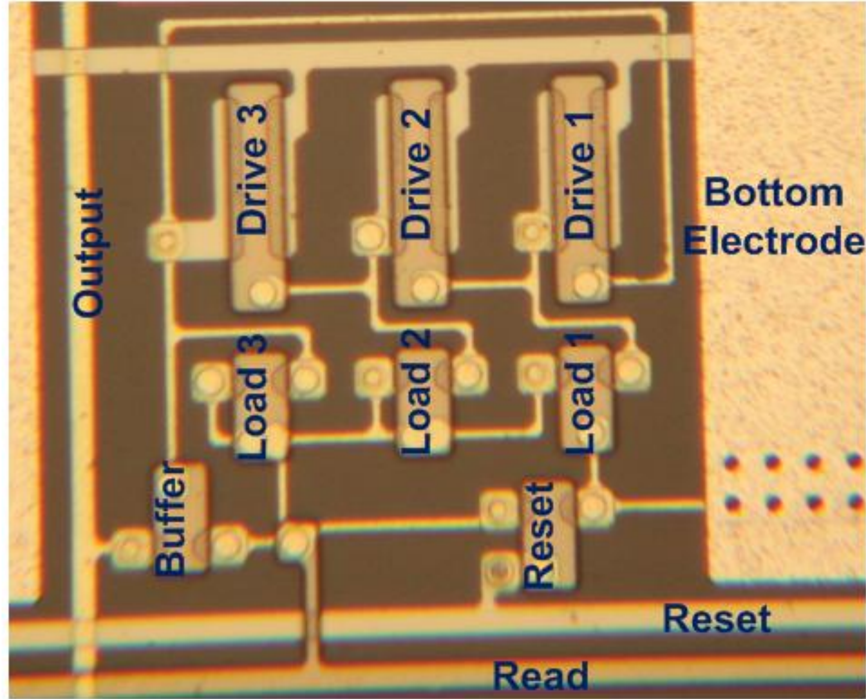
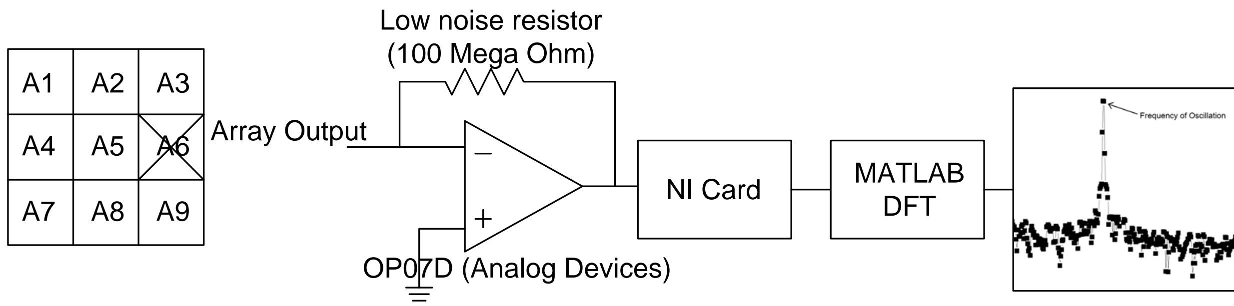


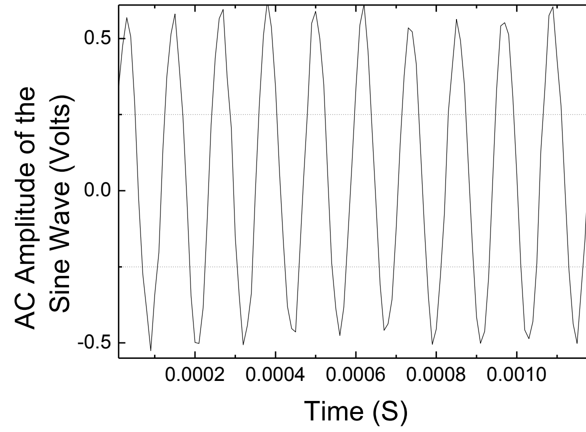
Figure 41. The die-micrograph of the RVCO pixel in an array

Table IV. Sizing of the TFTs in the RVCO array.

TFT name	TFT size
Load 1, Load 2, Load 3	10µm/10µm
Drive 1, Drive 2, Drive 3	60µm/10µm
Reset TFT	10µm/10µm
Buffer TFT	10µm/10µm



(a)



(b)

Figure 42. Off-panel readout circuit for testing the RVCO 3 by 3 array (a), Sample output oscillation in time domain detected by NI card (b).

As shown in Figure 42, all of the pixels of the array work except for A6. The results are extracted by NI Card and they are stored in the computer. However, the output spectrum of the pixels as well as their frequency-voltage gain plots are used to characterize their functionality and performance. To get the output spectrum of each pixel Matlab is used to take the Fast Fourier Transform (FFT) of the data stored on the computer (FFT can be used as well since FFT has the same result as DFT but with a higher speed of calculation). Then the output spectrum in terms of dBm is plotted. DFT is defined as follows,

$$X_k = \sum_{n=0}^{N-1} x_n e^{-\frac{2\pi i k n}{N}}, k = 0, 1, \ldots, N-1 \quad (21)$$

Where N is the number of data points stored from signal. If a higher resolution data storage is needed, this N can be increased simply by increasing the sampling frequency of the NI card. For example, to detect a single 6 keV X-ray photon a very high resolution data acquisition is needed. This will be shown later in this chapter.

The output spectrum of the pixels of the 3 by 3 array are shown in Figure 43 (the distance in the samples or average bandwidth is 30 Hz). From this figure and Figure 45 (measured frequency-voltage gain of around 2.33 kHz/V) the phase noise is extracted and it is showing that the input referred electronic noise is less than 20 electrons for all of the pixels. This proves that a signal as low as 135 electrons at the input (signal generated by a 6 keV X-ray photon which is a typical energy for protein crystallography) is detectable.

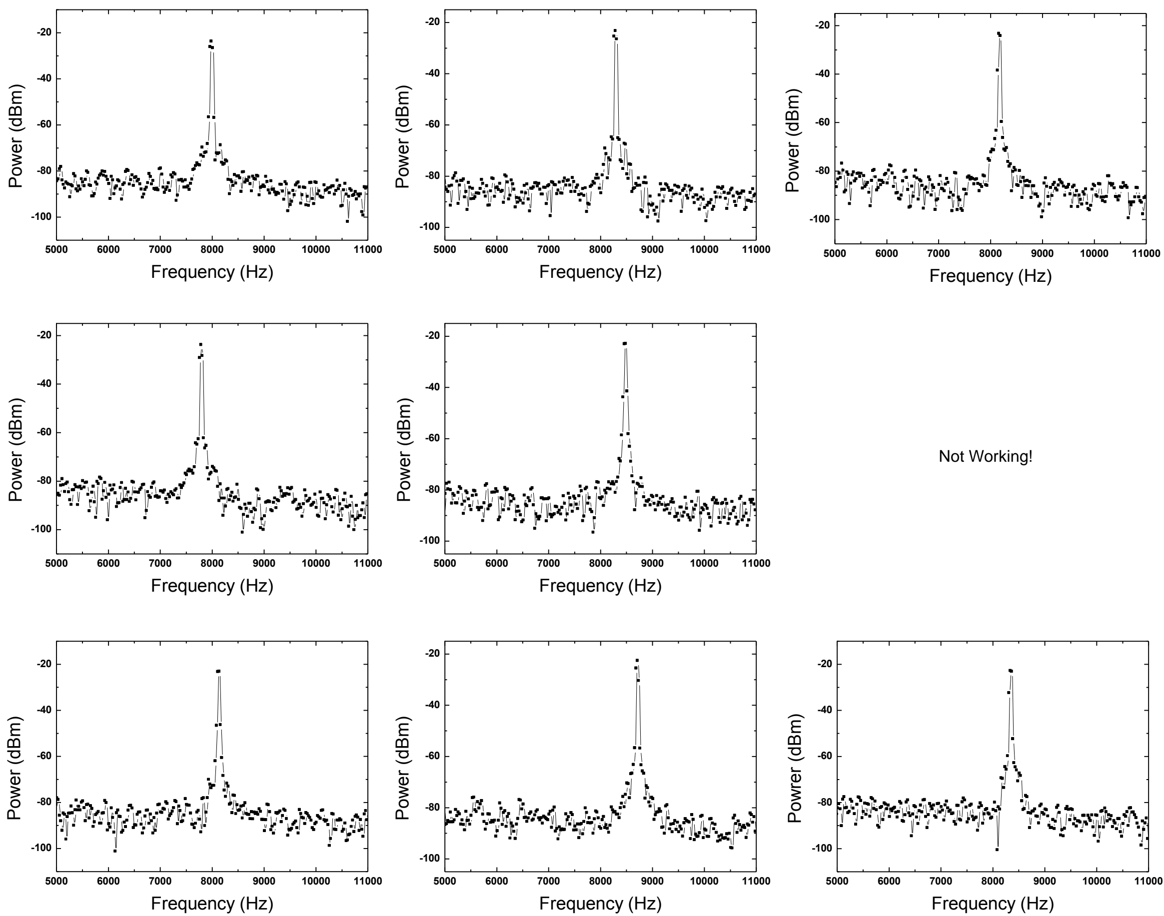


Figure 43. Output spectrum for the pixels in a 3 by3 array of RVCOs (As it can be seen the frequency of oscillation is around 7.5 to 8.5 kHz for the pixels; the change in the center frequency is due to non-uniformities in the fabrication process).

The measured percentage of change in the frequency due to the threshold voltage change of the a-Si TFTs is shown in Figure 44 versus the simulated change. This is the worst case result for the pixels in the array. As it can be seen from Figure 44, the worst case change in the frequency of oscillation after 3000 minutes of continuous usage is less than 0.65%. Although this change can be ignored due to its very small effect, it can be completely accounted for in the software. Another way is to use CDS or use ultra low noise RVCO structure to compensate for V_t shift.

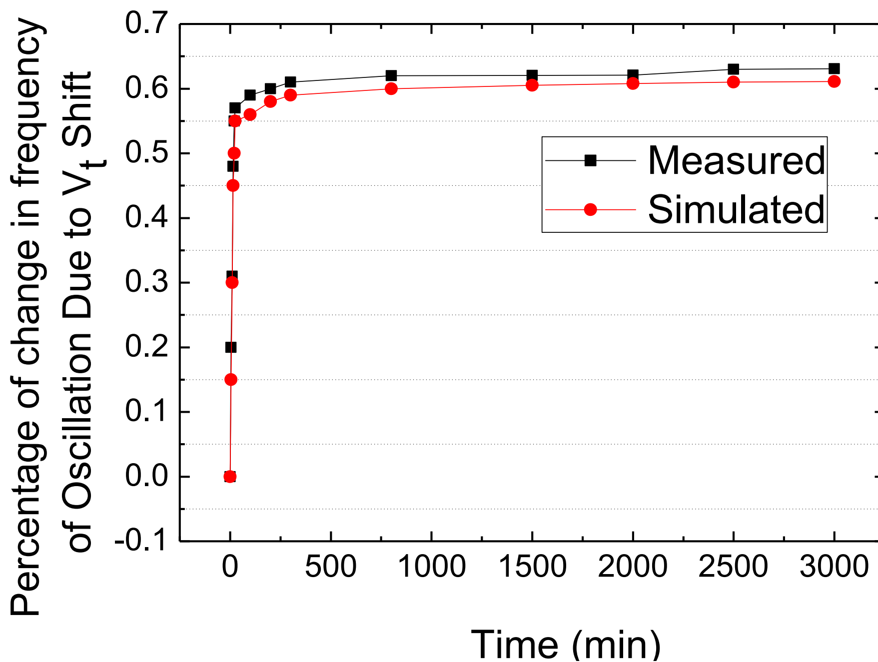
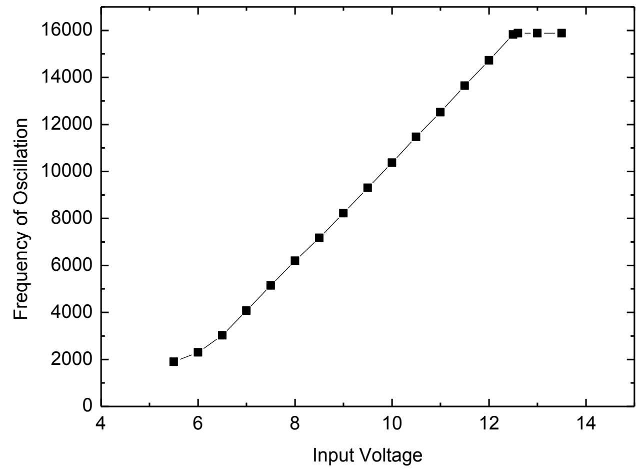
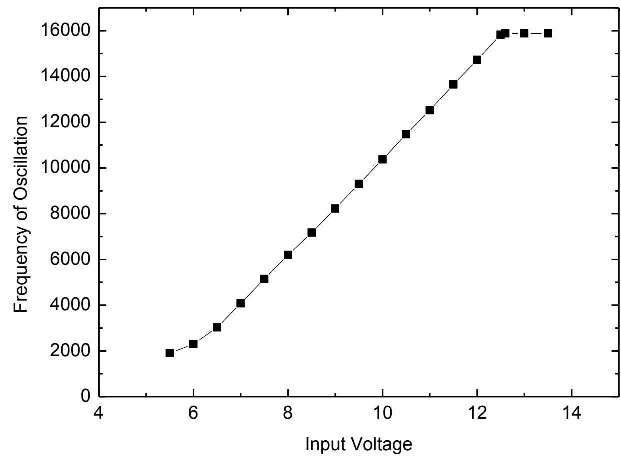


Figure 44. Measured vs. Simulated V_t shift effect on the output frequency over time for the worst case for the 3 by 3 RVCO array.

A sample frequency-voltage characteristic for two of the pixels in the 3 by 3 RVCO array are given in Figure 45. These plots as well as the same plots for other pixels are used to extract the frequency-voltage gain of the pixels and also to extract the dynamic range of the pixels (linear range). These data are used to extract the signal and noise values for each of the pixels.



(a)



(b)

Figure 45. Frequency-voltage gain characteristics of A1 pixel (a) and A9 pixel (b) (two sample pixels in the in house fabricated 3 by 3 RVCO array).

7.3 Single RVCO Pixel Interfaced with a-Se Results

One of the pixels in the 3 by 3 RVCO array (A1) is interfaced with a selenium layer deposited on a different glass substrate by means of wire bonding. Note that in Figure 45 the frequency-voltage gain of the A1 pixel is around 2.33 kHz/V. Figure 46 shows the failed attempt of the selenium direct deposition on the 3 by 3 RVCO array. This is due to the faulty recipe of the a-Se layer.

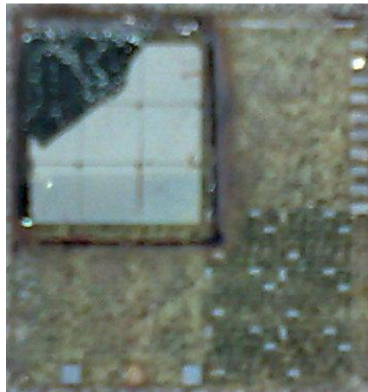


Figure 46. Failed attempt of the selenium direct deposition on the 3 by 3 RVCO array.

Therefore for testing the sample interacted with a-Se selenium detector, a 50 um thick a-Se selenium is used (Figure 47). This a-Se layer is biased to 500 V using a high voltage source, resulting in a 10 V/um bias across the a-Se detector (this means X-ray to charge conversion gain is 50 eV per electron hole pair). The a-Se output is connected to the input of the A1 RVCO pixel on the 3 by 3 array through an ultra low noise CMOS switch to be able to control the connection of the a-Se to the pixel. The block diagram of the system used for the readout process is shown in Figure 48. The measurement setup is shown in Figure 49.

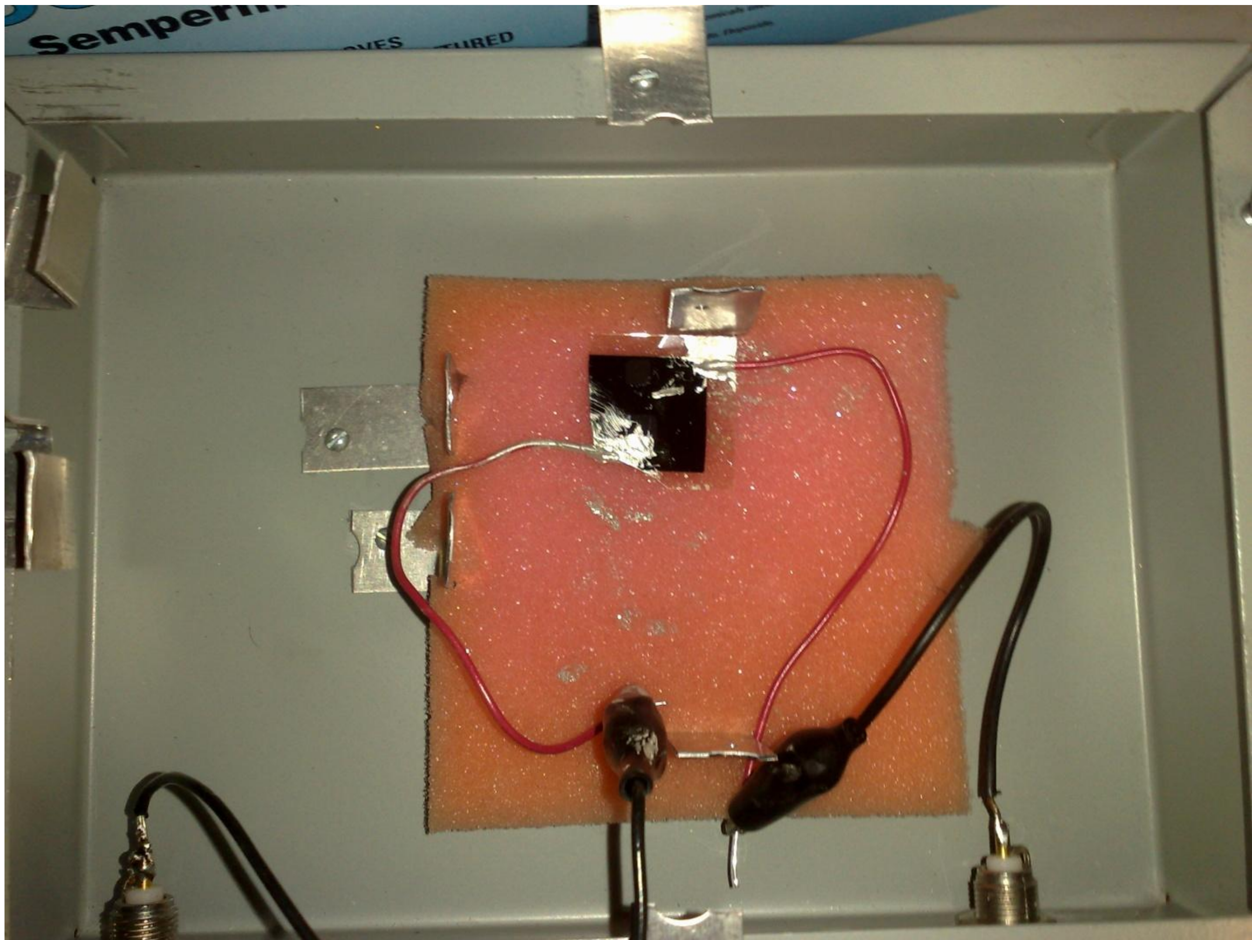


Figure 47. 50 um thick a-Se sample used to interact with RVCO pixel (4 mm by 4 mm area).

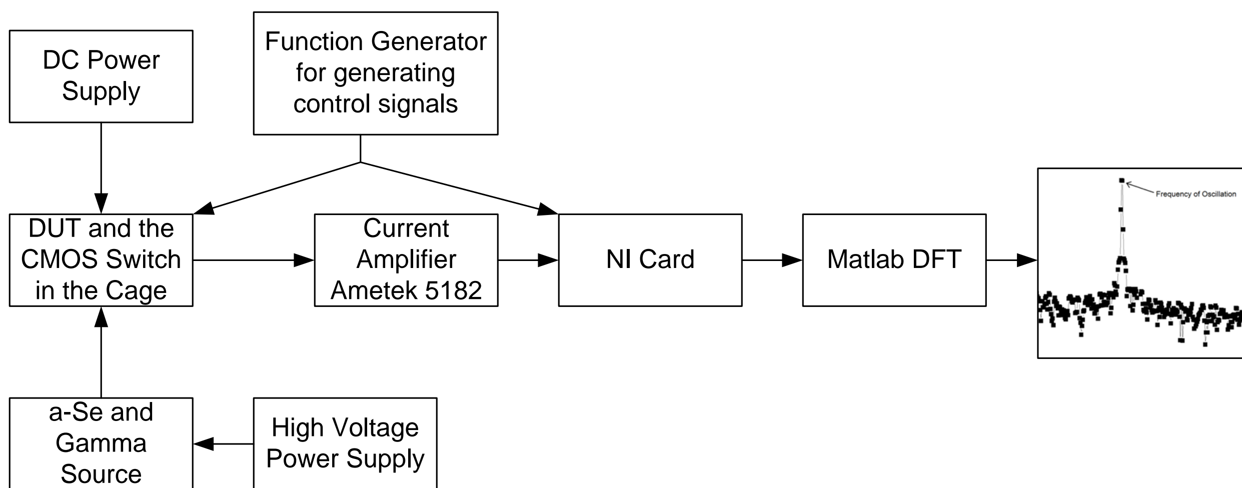


Figure 48. The off-panel readout circuit for testing RVCO pixel interacted with a-Se layer.

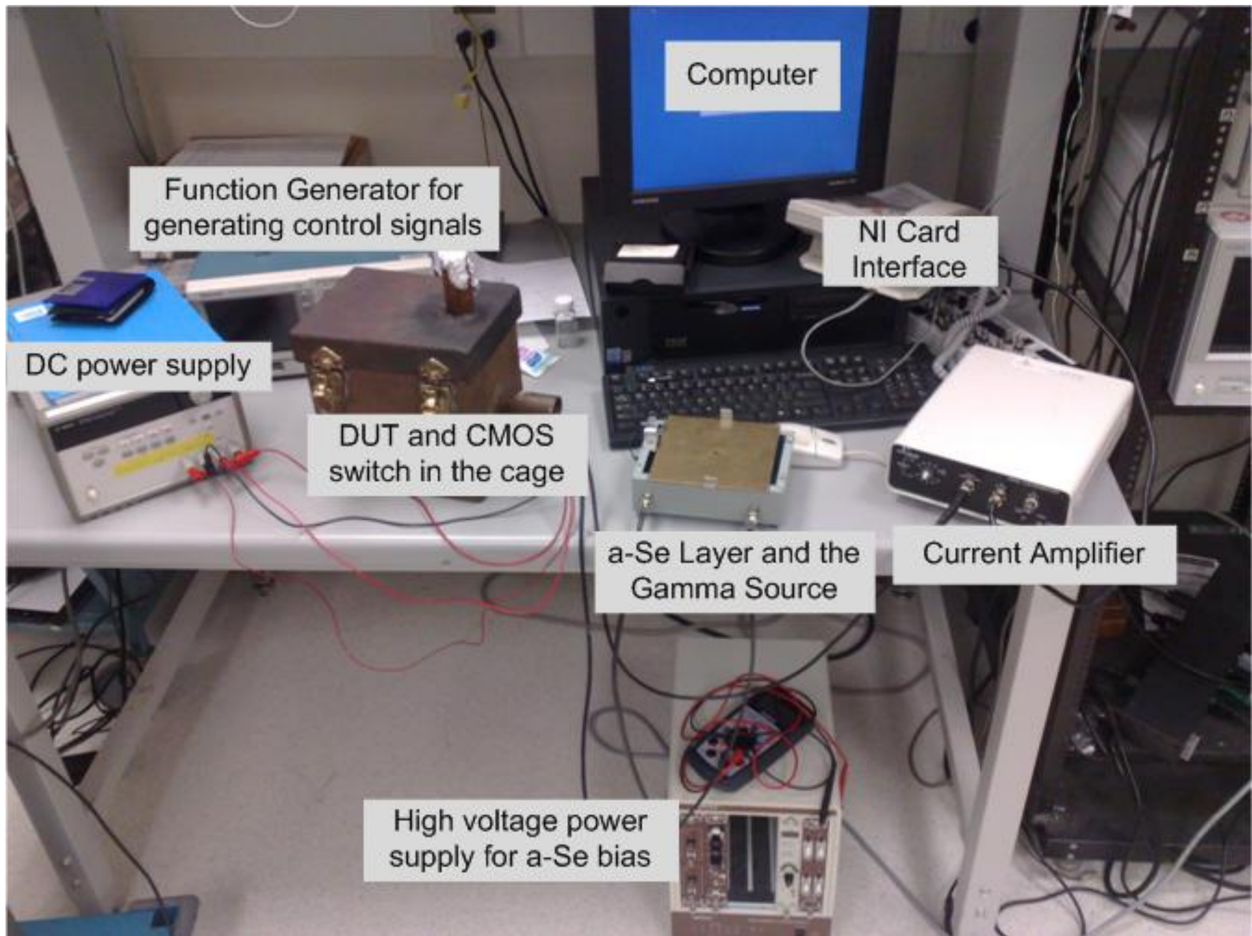


Figure 49. Measurement setup for testing RVCO pixel interacted with a-Se layer.

To be able to generate single 6 keV photons (lowest X-ray photon energy for protein crystallography application) a 6 keV gamma source is used (Fe 55 gamma source in Figure 50). Note that the rate of photon generation for this source is approximately 1 photon per every half of a second.

Figure 50. Fe 55 gamma source used to generate 6 keV photons.

In Figure 51 the timing used for this test is shown. As it can be seen from this figure, the RVCO pixel is reset after every 100 readouts. After resetting the RVCO pixel to the middle of the linear range of the frequency-voltage plot, integration and readout are done consecutively for 100 times. Each integration period is 33 us and each readout period is 10 s (the resolution of frequency readout was picked to be 0.05 Hz resulting in 10 s readout time). During the integration usually the dark current is building a voltage on the input capacitor. If the 6 keV photon hits the a-Se sample during one of the integration periods, then the dark current and the signal due to 6 keV photon build up a voltage on the input capacitor of the RVCO pixel. Note that the input of the RVCO pixel is only connected to the a-Se detector during the integration periods (using ultra low noise CMOS switch). After 2132 readouts, one of the integration periods had the 6 keV photon in it. The reason that it took 2132 readouts to detect a single photon is that the photons are generated with a rate of nearly 1 photon per half second, and the integration time is only 33 us. Therefore, a lot of readouts have to be done in order to detect a single photon in 33 us time interval. 33 us is picked because reset is applied every 100 frames and during those 100 frames the dark current is building up a voltage on the input capacitor. The sum of those changes

in the voltage should not make the RVCO to go out of the linear range of the frequency-voltage plot. The sum of these 100 changes in the voltage of the input capacitor should be less than 3 V. This can be seen in the next paragraph.

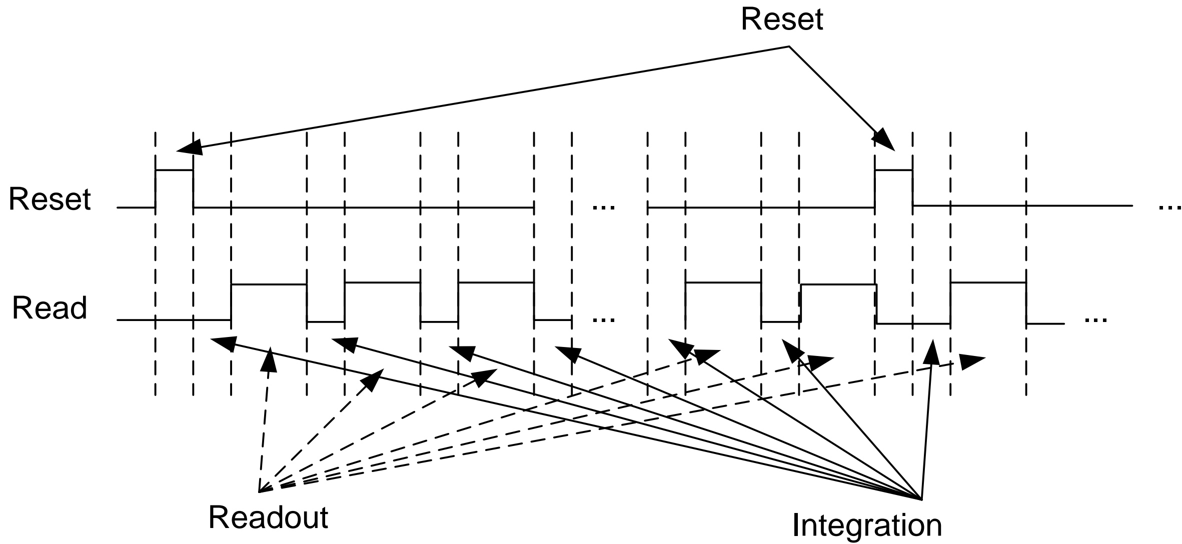


Figure 51. Timing diagram used for testing the RVCO pixel interfaced with a-Se layer.

The bias of the a-Se detector was applied to it 1 hour prior to starting the actual experiment to stabilize the dark current of the a-Se layer. Also, the RVCO pixel was ON continuously for 2500 minutes. This is just to let the RVCO pixel experience V_t shift before the actual experiment. After that time V_t shift can be assumed to be negligible (Figure 39 (b)). Stabilized dark current is measured to be 1.6 nA for the a-Se sample. This current builds up a voltage as big as 26.5 mV (100 of these changes is 2.65 V which is less than 3 V, therefore, the RVCO stays in the linear range of the frequency-voltage plot) on the input capacitor of the RVCO (200 fF). This much change in the input voltage of the RVCO pixel shifts the frequency of oscillation of the RVCO pixel by about 61.75 Hz. This change was consistent for 2132 readout periods (ignoring the periods after reset) except for one readout period. In that readout

period the frequency shifted by 61.95 Hz. Therefore, the frequency of oscillation was shifted by 0.2 Hz due to one 6 keV photon. In other words, in one of the 2132 integration times, the input current applied to the input capacitor of the RVCO pixel is the dark current plus the photo current due to the 6 keV photon. In all other frames, the input current applied to the input capacitor of the RVCO pixel is just the dark current. Using 0.2 Hz as the change in the frequency of oscillation due to 6 keV photon and *2.33 kHz/V* as the frequency-voltage gain of the RVCO pixel, the change in the voltage of the input capacitor (200fF) of the RVCO can be calculated to be around 85 uV. On the other hand, this voltage change can be calculated using a-Se layer parameters. A 6 keV X-ray photon is generating around 120 e-h pairs in the a-Se layer (assuming an X-ray to charge conversion gain of 50 eV per electron hole pair for a-Se layer biased at 10 V/um). This will result in a 96 uV voltage change on a 200fF capacitor ($V=(n\times q)/C$=(120×1.6e-19)/200e-15). As it can be seen the simulated change in the voltage of the input capacitor of the RVCO (96 uV) is almost the same as the measured value (85 uV). The reasons that the measured value is a bit less than the simulated value could be the charge trapping effect in a-Se layer and not using the exact values for the parameters in the a-Se layer.

So, a single 6 keV X-ray photon was detected using a RVCO pixel interacted with a-Se layer which is the main objective of this thesis. Note that the dark current shot noise on the input capacitor of the RVCO pixel (which is about 3.7 uV) is negligible for this case. This noise is calculated using shot noise current formula ($I_{n-shot\ noise} = \sqrt{2Iq}$, where I is the dark current and q is the charge of a single electron). Then, using this current and formula $V=It/C$ (I is the dark current shot noise current, t is the integration time and C is the input RVCO capacitor), the voltage due to the dark current shot noise is calculated. Note that dark current, integration time and input RVCO capacitor are 1.6 nA, 33 us and 200 fF respectively.

The same test is repeated using another gamma source (Co 57) shown in Figure 52 to test this system with a higher energy photon (122 keV for Co 57). After 5843 readout periods the single 122 keV photon was detected. The change in the frequency of oscillation due to the single 122 keV photon (on top the change due to the dark current) is 4.25 Hz which translates into 1.824 mV on the input capacitor of RVCO (200 fF). On the other hand, this voltage change can be calculated using a-Se layer parameters. A 122 keV X-ray photon is generating around 2440 e-h pairs in the a-Se layer (assuming an X-ray to charge conversion gain of 50 eV per electron hole pair for a-Se layer biased at 10 V/um). This will result in a 1.952 mV voltage change on a 200fF capacitor ($V=(n\times q)/C=(2440\times 1.6e\text{-}19)/200e\text{-}15$). As it can be seen the simulated change in the voltage of the input capacitor of the RVCO (1.952 mV) is almost the same as the measured value (1.824 mV). The reasons that these two numbers are different as it was discussed before, are charge trapping in a-Se layer and not using the exact values for the parameters in the a-Se layer. This shows that this pixel architecture is capable of detecting photon energies as low as 6 keV as well as other photon energies (e.g. 122 keV).

Figure 52. Co 57 gamma source used to generate 122 keV photons.

The same test is repeated using another gamma source (Cd 109) with a photon energy of (22 keV). The change in the frequency of oscillation due to the single 22 keV photon (on top the change due to the dark current) is 0.8 Hz which translates into 343 uV on the input capacitor of RVCO (200 fF). On the other hand, this voltage change can be calculated using a-Se layer parameters. A 22 keV X-ray photon is generating around 440 e-h pairs in the a-Se layer (assuming an X-ray to charge conversion gain of 50 eV per electron hole pair for a-Se layer biased at 10 V/um). This will result in a 352 uV voltage change on a 200fF capacitor ($V=(n\times q)/C$=(2440×1.6e-19)/200e-15). As it can be seen the simulated change in the voltage of the input capacitor of the RVCO (352 uV) is almost the same as the measured value (343 uV). The reasons that these two numbers are different as it was discussed before, are charge trapping in a-Se layer and not using the exact values for the parameters in the a-Se layer. This shows that this pixel architecture is capable of detecting photon energies as low as 6 keV as well as other photon energies (e.g. 122 keV and 22 keV). Figure 53 shows the frequency change versus the incoming X-ray photon energy (the frequency-voltage gain is assumed to be 2.33 kHz/V).

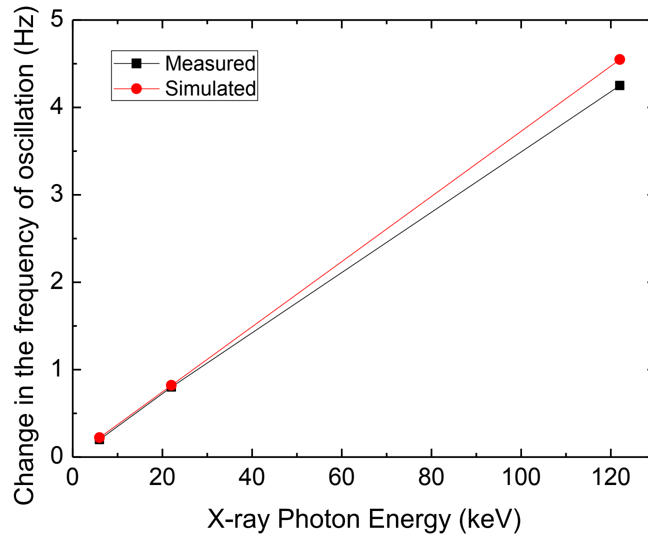


Figure 53. Frequency change versus the incoming X-ray photon energy.

8 Detective Quantum Efficiency

The Detective Quantum Efficiency (DQE) is considered as the figure of merit of the imaging performance. In this section of the thesis zero spatial frequency detective quantum efficiency (i.e. $DQE(0) = DQE(f)$ at $f = 0$, of a-Se as the photoconductive detector and the RVCO as the pixel amplifier) is analysed in detail as a function of varying amounts of input signal exposure and added electronic noise. The output of an actual X-ray generator emitted from the X-ray tube is approximated by a monoenergetic X-ray beam having the same average photon energy. This approach (monoenergetix X-ray beam) is used in the analysis of DQE of an a-Se coated large area photon quantum noise limited imager proposed in this proposal. To calculate the *DQE(0)* a cascaded linear-system model [30] is used as it is shown in Figure 54. It is worthwhile to note again that it is assumed that the detector is a-Se layer and the detection is done in a direct manner [8]. *DQE(0)* as well as different stages in the linear cascaded model are discussed in the next sub-chapters. Results of the simulations are given at the end of this chapter.

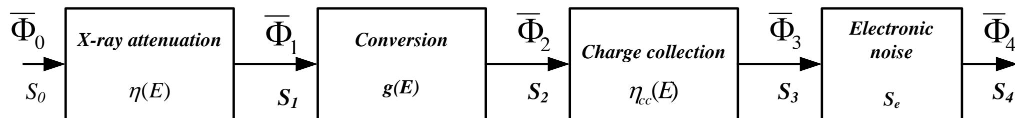


Figure 54. The linear cascaded-system model flow graph showing the propagation of signal and noise through the main four stages of the X-ray imager.

8.1 DQE(0)

The model shown in Figure 55 is used to calculate *DQE(0)* of the flat panel imager. As it can be seen from Figure 55, the a-Se layer is sandwiched between two large area parallel plate electrodes. To generate an electric field (*F*) across the a-Se layer a high voltage is applied to the a-Se layer. When an X-ray photon interacts with the a-Se layer a number of electron hole pairs are generated. The electric field across the a-Se layer separates these carriers. It also drifts the carriers towards the electrodes depending on the polarity of the carriers and the electrodes.

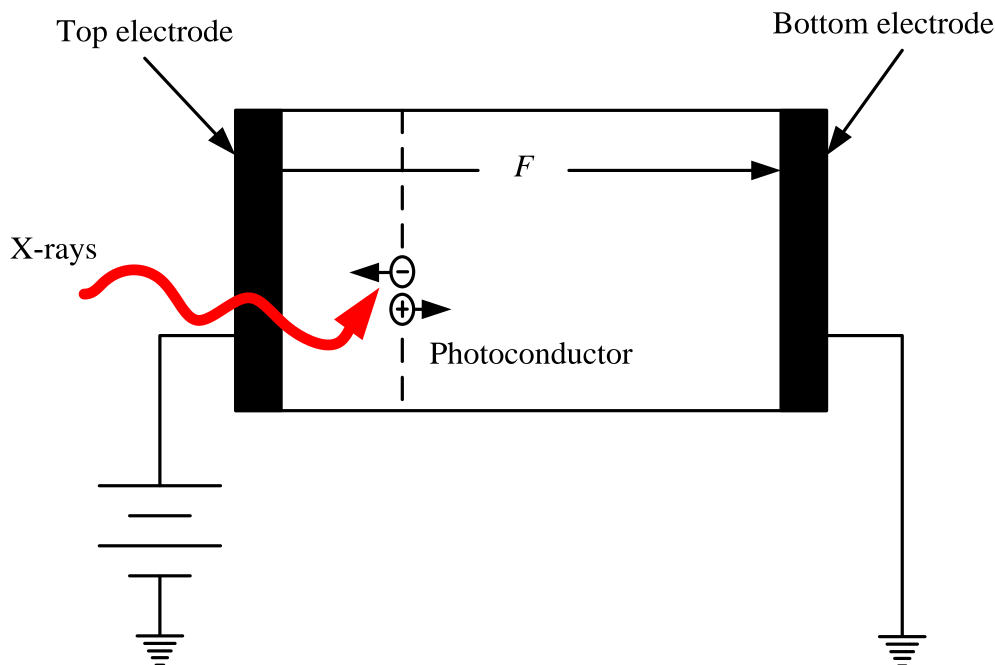


Figure 55. Model used for calculating *DQE(0)* [85].

When the signal and noise are propagated through different stages of the X-ray imager, DQE is degraded. DQE of a flat panel imager is defined as the ratio of the square of the signal-to-noise ratio at the output of the imager over the square of the signal to noise ratio at the input of the imager.

$$DQE = \frac{SNR_{out}}{SNR_{in}} \tag{22}$$

DQE is a function of spatial frequency [50] (*Dqe(f)*) and it is used to simulate the signal and noise performance of the flat panel imager. X-ray attenuates through the a-Se layer exponentially. The probability of density of interaction is given as follows,

$$P_x(E,x) = \begin{Bmatrix} \alpha e^{-\alpha x}, & 0 \leq x \leq L \\ 0, & elsewhere \end{Bmatrix} \tag{23}$$

Where x is the distance from the X-ray receiving electrode, E is the energy of the incident X-ray photon, α is the energy dependent linear attenuation coefficient which is a function of *E* itself and *L* is the thickness of the a-Se layer. The quantum efficiency ($\eta(E)$) using energy dependent α can be written as,

$$\eta(E) = 1 - e^{-\alpha(E)d_{Se}} \tag{24}$$

8.1.1 Cascaded Linear System Model

This model is used to characterize and quantify the flat panel imagers' performance. In this model the imager is modelled using individual stages. As the signal and noise are propagating through these stages the behaviour of the imager is modelled. Each stage has a spatial distribution of quanta. In this case, the quanta is the X-ray distribution since an X-ray source is used for this research. As it is shown in Figure 54, this model consists of 4 stages. These stages are as follows: 1) X-ray attenuation, (2) Conversion gain which is the generation of charge carriers in the a-Se layer, 3) Charge collection at the electrodes of the a-Se layer, (4) Electronic noise addition which models the pixel's electronic performance.

This model can only be used for the calculation of zero spatial frequency detective quantum efficiency (*DQE(0)*) since the spatial dependence of the signals and noises are not

considered. In other words, *DQE(0)* simulates the signal quality degradation throughout the different stages of the detector without considering the effect of signal spreading [50]. Each of the stages in the Figure 54 is an amplification process, a stochastic blurring process or a deterministic blurring process [50].

If one stage has only an amplification process with a gain of g_i and a gain variance of σ_{g_i}, then the output mean number of quanta per unit area and Noise Power Spectrum (NPS) for this stage is as follows,

$$\overline{\Phi}_i(E,x) = \bar{g}_i(E,x)\overline{\Phi}_{i-1}(E,x) \tag{25}$$

$$S_{N_i}(E,x) = \bar{g}_i^2(E,x)S_{N_{i-1}}(E,x) + \sigma_{g_i}^2(E,x)\overline{\Phi}_{i-1}(E,x) \tag{26}$$

Where E is the energy of the incident X-ray photon, $\overline{\Phi}_{i-1}(E,x)$ and $S_{N_{i-1}}(E,x)$ are the mean number of quanta and the NPS incident of the gain stage respectively, i is the number of the stage and $\bar{g}_i(E,x)$ and $\sigma_{g_i}^2(E,x)$ are the mean gain and variance of the gain for the gain stage. The noise is not deterministic and therefore this makes this stage to be stochastic. This results in the increase of the noise of the quanta in two different ways. The power spectrum of the noise at the input is amplified by the gain and also another noise source is introduced in the noise power spectrum of the output due to the variation of the gain. Different stages in Figure 54 are discussed next.

8.1.2 X-ray Attenuation

When X-ray photon hits the a-Se layer, it interacts with the a-Se layer with a probability of g_1 and does not interact with the a-Se layer with a probability of $1 - g_1$. g_1 is equal to the

quantum efficiency [51]. This process is called a binary process and the variance of a binomial process is calculated as follows,

$$\sigma_{g1}^2 = \bar{g}_1(1 - \bar{g}_1) = \eta(1 - \eta) \tag{27}$$

8.1.3 Conversion Gain

In this stage the X-ray quanta converts to electron-hole pairs (EHPs). If the X-ray photon with energy E interacts with the a-Se layer at distance x from the X-ray receiving electrode, then the mean conversion gain is equal to the mean number of free EHPs generated by this X-ray photon. This gain is shown as follows,

$$\bar{g}_2(E, x) = \frac{E_{ab}(E,x)}{W_\pm} \tag{28}$$

Where $E_{ab}(E, x)$ is the average absorbed energy due to an X-ray photon with an energy of E at distance x from the X-ray receiving electrode and $W_\pm$ is the energy required to generate an electron-hole pair in the a-Se layer.

There is a variance associated with this gain. It is due to two sources: 1)statistical nature of the number of free EHPs per X-ray photon and 2) K-fluorescence reabsorption. If the mean number of free EHPs per X-ray photon at distance x form the X-ray receiving electrode follows a Poisson distribution, then the variance of the depth dependent conversion gain is $\sigma_{g2}^2(E, x) = \bar{g}_2(E, x)$. The K-fluorescence reabsorption is quite important and it maximizes just above the K-edge of the a-Se (12.7 keV). If the energy of incident photon is bigger than the K-edge of the a-Se, then this source of variation in the gain can be neglected [52]. In this section the incident photon energy is assumed to be 52.1 keV (for ease of simulation since all the parameters were available for this energy) and therefore this source of variation is neglected.

8.1.4 Charge Collection

When a free EHP is generated in the a-Se layer due to the impinging X-ray photon at distance x form the X-ray receiving electrode, the electric field applied across the a-Se layer causes the free carriers to drift to the opposite electrodes. Hetcht charge collection efficiency calculates the average charge collection efficiency at the electrodes ($\bar{g}_3(x)$). Note that the bulk recombination and carrier diffusion in the a-Se layer are neglected.

$$\bar{g}_3(x) = \tau_t \left(1 - e^{-\frac{x}{\tau_t}}\right) + \tau_b \left(1 - e^{-\frac{1-x}{\tau_b}}\right) \tag{29}$$

Where x is the distance from X-ray receiving electrode, $\tau_t = \mu_t T_t F/L$, $\tau_b = \mu_b T_b F/L$, μ is the drift mobility of the carriers. τ is the charge carriers lifetime which is the time that a carrier can move on average before getting trapped in the deep trapping centers of the a-Se layer. $\mu\tau F$ is called the Schubweg parameter, which is the average distance a charge carrier drifts before becoming trapped in the deep trapping centers. The subscripts t and b represent the parameters for the top and bottom electrodes, respectively. If a positive bias is applied to the X-ray receiving electrode (which is the case in this research), then the subscript b represents the holes and the subscript t represents the electrons.

In [53], it is shown that if the random trapping of the drifting charge carriers in the a-Se layer is considered in the charge collection efficiency, then the variance in the gain is calculated as follows,

$$\sigma_{g3}^2(x) = \tau_t^2 + \tau_b^2 - \tau_t^2 e^{-\frac{2x}{\tau_t}} - \tau_b^2 e^{-\frac{2(1-x)}{\tau_b}} - 2\tau_t x e^{-\frac{x}{\tau_t}} - 2\tau_b (1-x) e^{-\frac{(1-x)}{\tau_b}} \tag{30}$$

8.1.5 Electronic Noise

There are different electronic noise sources during the readout period of the detector and pixel that have to be added to the total noise power at this stage. These noise sources are as follows: 1) Electronic noise power from the a-Se layer (e.g. dark current shot noise which is negligible compared to other noise sources for the case of RVCO pixel), 2) TFT readout circuit for each pixel (which is only the phase noise for RVCO pixel), 3) Data line noise source as well as the off-panel readout circuit (which are eliminated in the RVCO pixel due to use of an on-pixel buffer). These noise sources are independent [54] and therefore, the total noise power can be calculated by adding the power of the different noise sources together.

8.2 DQE(0) Simulation Results

The x-ray spectrum of a 70 kVp tungsten anode naked X-ray tube with 23.5 mm Al acting as a filter (RQA5 beam quality of the IEC1267 standard) is shown to have the average photon energy E_{av} of 52.1 keV [31]. Considering this fact, the parameters listed in Table V are used for this simulation. All the parameters in Table V are extracted from [32][33][34]. Figure 56 shows *DQE(0)* versus detector thickness, for the cases of PPS, APS and RVCO structures in a-Si technology. Electronic noise is considered to be 380 e^- for APS as it is reported in [31] and 1000 e^- for PPS as it is reported in [2]. However, the electronic noise for the RVCO structure is

DQE(0) versus detector thickness with the constant bias value of 10 kV applied to the radiation receiving electrode and a monoenergetic X-ray beam of photon energy E = 52.1 keV for PPS, APS and RVCO structures.

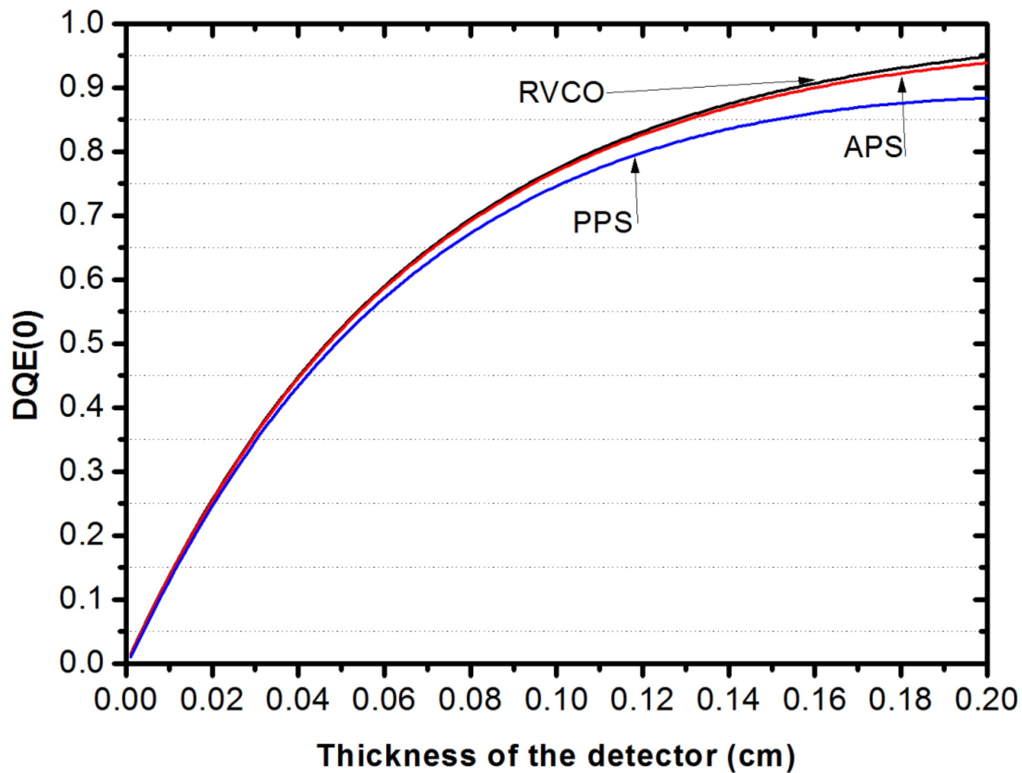


Figure 56. *DQE(0)* versus detector thickness with the constant bias value of 10 kV applied to the radiation receiving electrode and a monoenergetic X-ray beam of photon energy E = 52.1 keV for PPS, APS and RVCO structures.

Eventually, it is worthwhile to mention that the RVCO has a huge advantage over other structures (especially in lower X-ray photon energies) in terms of electronic noise and therefore, it can be used for applications requiring better electronic noise performance such as protein crystallography. Moreover, the *DQE(0)* for RVCO is higher than other pixel architectures for all X-ray photon energies. The results for a 52.1 keV X-ray photon are shown in Figures 56 and 57 and from these Figures the advantage of the RVCO pixel over other architectures is noticeable.

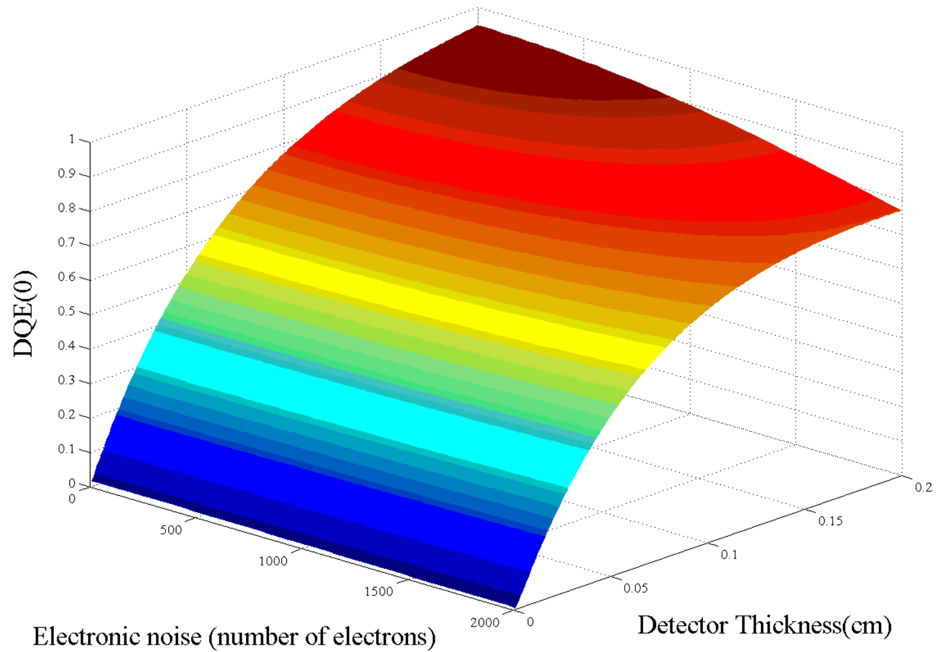


Figure 57. *DQE(0)* versus electronic noise and detector thickness (with the constant bias value of 10 kV applied to the radiation receiving electrode and a monoenergetic X-ray beam of photon energy E = 52.1 keV).

Table V. Parameters used to analyze the DQE for an RVCO pixel using a-Se as the detector layer.

Parameter	**Description**	**Quantity**
μ_h	Hole mobility in a-Se	0.12 cm^2/Vs
μ_e	Electron mobility in a-Se	0.003 cm^2/Vs
τ_h	Hole life time in a-Se	50 µs
τ_e	Electron life time in a-Se	200 µs
F	Electric field applied to the a-Se layer	10 V/µm
$W_\pm$	Energy required for creation of a single electron-hole-pair in a-Se for an x-ray beam with the average energy of 52.1 keV	44 eV

9 Conclusion and Contributions

Measurements indicate that the fabricated a-Si RVCO pixel is relatively immune to V_t shift for duty cycles typical in digital imaging applications and it has a very low input referred noise of less than 10 electrons compared to state of the art TFT PPS and APS pixels. The six plus a-Si transistors per pixel area constraint limits its use to larger pixel size imaging applications such as protein crystallography unless poly-Si transistor technology is used. *DQE(0)* for the proposed structure is higher than the previously shown APS and PPS structures.

Here, how the RVCO architecture addresses the protein crystallography requirements is discussed: 1) Detector area: RVCO array is fabricated in a-Si technology. Therefore, it can be easily fabricated in large areas such as 20×20 cm^2. 2) Dynamic range: RVCO pixel is capable of reading a signal as low as 1 photon due to its very low input referred noise; and on the other hand, it can easily detect the strong spots. 3) Sensitivity: RVCO pixel is easily able to readout a single 6 keV X-ray photon, due to its hugely low input referred noise. SNRs as low as 10 are achievable with RVCO pixels. 4) Readout time: This is equivalent to the integration time in the RVCO pixel. Although the in-house fabricated RVCO pixel needs 10 s for readout with high frequency resolution, it only needs 33 us for integration time. The readout in this section is

equivalent to the integration time in the RVCO pixel which is smaller than a second. Note that by increasing the frequency of oscillation, using better fabrication instruments and process the readout out time used for RVCO readout can be decreased. For example, by using an RVCO pixel with 100 times higher frequency of oscillation and frequency-voltage gain than the sample in-house fabricated RVCO used in this thesis, a readout time as low as 100 ms is achievable. 5) Spatial Resolution: RVCO pixel can be easily made in 150×150 μm^2 area. Table VI shows design considerations for a protein crystallography X-ray detector [36] as well as RVCO values.

Table VI. Design considerations for a protein crystallography X-ray detector [36].

Parameter	**Values**	**RVCO Values**
Detector area	Larger than 20 cm × 20 cm	> 20 cm × 20 cm
Dynamic range	1-1.2×10^5 X-ray Photons in 60 seconds	1-larger than 5×10^4 X-ray Photons in 33 us
Readout time	~ 1 s	<< 1 s
Sensitivity	Single 6 keV X-ray Photon	Single 6 keV X-ray Photon
Pixel size	50×50-150×150 μm^2 pixel size	150×150 μm^2
X-ray Energy	6 keV – 20 keV	6 keV – 20 keV
Object size	1.8 Å (Inter-atomic distance of protein)	1.8 Å (Inter-atomic distance of protein)

Note that the readout time for the RVCO is very smaller than the commercial model. The reason is that in the commercial model the time it takes for the detector to detect the smallest detectable signal is 60 seconds, where as in the RVCO structure this time is 33 us because of the very high sensitivity. Therefore, the high end of the dynamic range can be very smaller compared to the commercial model and 5×10^4 X-ray photons is more than sufficient as the higher end of the dynamic range.

The RVCO array can be implemented in different technologies such as CMOS, poly-Si and a-Si. Different characteristics of the RVCO detector are classified in Table VII for these technologies. In this table some of the most important characteristics of an RVCO array in different technologies are compared such as large area compatibility, pixel gain (in terms of kHz/V), input referred phase noise and metastability effect on the performance of the array.

Table VII. Comparing the RVCO structure in different technologies.

Characteristic	**Best achievable for a-Si**	**Best achievable for Poly-Si**	**Best achievable for CMOS**
Large area compatibility	yes	somehow	No
Gain (frequency-voltage gain kHz/V)	~100	>1000	>1000
Input referred phase noise	~1e^{-}	~1e^{-}	~1e^{-}
Metastability (percentage of Osc. Freq. change over 50,000 hours with a 0.1% duty cycle)	< 1%	negligible	negligible

Some selected publications are listed in the references [86-89]. The original contributions of the research presented in this thesis to the field of large area digital imaging are listed below:

- Design and implementation of a photon quantum noise limited pixel architecture for protein crystallography application. Design of the architecture, the layout design, fabrication and testing of this pixel is done in-house at the University of Waterloo.

- Design and implementation of a sample array of quantum noise limited pixels for protein crystallography application. Design of the architecture, the layout design, fabrication and testing of this pixel is done in-house at the University of Waterloo.
- Design of an ultra-low noise pixel architecture (nearly noiseless) in a-Si technology for large area digital imaging applications, specifically, protein crystallography.
- Design and implementation of a photon quantum noise limited pixel interfaced with a layer of a-Se detector for large area direct digital imaging applications, specifically, protein crystallography. This architecture is tested and the results are given which prove that this architecture is suitable for large area direct digital imaging applications, specifically, protein crystallography.
- A 6-mask top gate TFT process has been optimized to fabricate high performance a-Si TFTs used in circuits aimed for large area digital imaging applications.
- Design and implementation of the off-panel readout circuit for the photon quantum noise limited pixel and array readout.
- Novel ways of measurements for characterization of the RVCO architectures are given.

Appendix A-Amorphous Silicon TFT

Amorphous Silicon (a-Si) TFTs were first suggested in 1962 [55]. But it took about twenty years to be demonstrated in 1981 by Spear and LeComber [56]. The most significant difference between crystalline transistors and a-Si TFTs is in fabrication procedure. Crystalline transistors are fabricated into a substrate. On the other hand, a-Si TFTs are deposited onto a substrate [55]. The substrate is usually glass which limits the fabrication temperature to 300 – 450 degree C. This low fabrication temperature can be provided through PECVD (Plasma-Enhanced chemical Vapour Deposition) [57].

One of the most important requirements for a useful electronic device is that it should have a low density of gap states. This is probably the most significant property of a-Si for fundamental and applied work. A result of the applied side is the a-Si TFT which is the subject of this Appendix [57]. The growing market and applications of a-Si TFTs demand a very keen and accurate physical model to describe the behaviour of this type of transistors.

A.1 Application of a-Si TFT

There are so many different applications for a-Si TFTs. Here we list some the most important applications of a-Si TFTs. Applications of a-Si TFTs include flat panel displays [58], image sensors [59], logic circuits [60], photo transistors [61], high voltage transistors [62], photo detectors arrays and TFT image sensor arrays [9], fax machines and optical scanners and X-Ray imaging [63], memory switching devices, optical recording and charge coupled devices (CCD) [64][65][66].

A.2 Basic Structure of the a-Si TFT

There are four common structures for a-Si TFTs. These four structures are defined by the order of deposition of the gate metal, the gate insulator, the semiconductor layer and the source drain contacts [58]. In Figure A.1, these four common structures are shown. In the staggered TFT structures, drain and source metals are on one side of the semiconductor and the gate metal is on the other side. In the coplanar structures all three metals are on the same side of the semiconductor layer. In the inverted structures, the gate metal is first deposited on the glass (substrate). Then the insulating silicon nitride layer is deposited. Then the amorphous silicon is deposited. Eventually, the drain and the source metals are deposited on the top [57].

In all of these four commonly used structures an n+ layer is used between metal and semiconductor contact in order to decrease the resistance of the ohmic contact [67]. Unlike the co-planar MOS devices, practical a-Si TFT structures are of the inverted staggered type. This

structure is the mostly common used structure of the a-Si TFT because of two reasons [68]: 1) This structure has the lowest interface between layers and 2) This structure has the simplest fabrication process. In this structure, the quality of the gate insulator is very important because the quality of this layer will determine the I-V curve, V_t and subthreshold slope. So, a three-step PECVD process is utilized. This three step PECVD process ensures that the gate insulator layer is never exposed to the environment. High quality of the gate insulator ensures low surface state trap density at the interface, which is one method to reduce the threshold voltage [9].

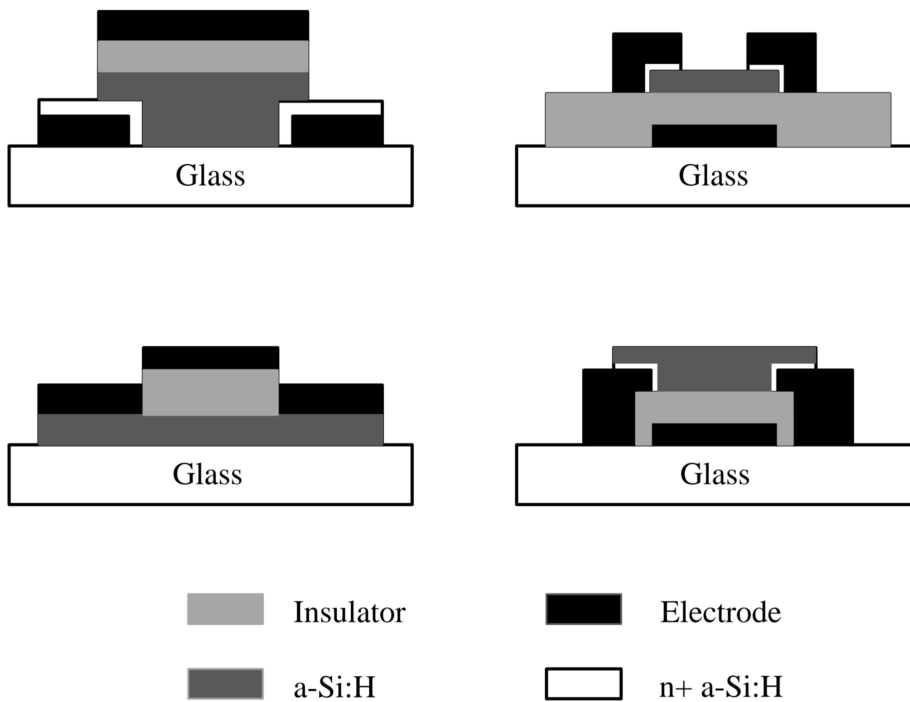


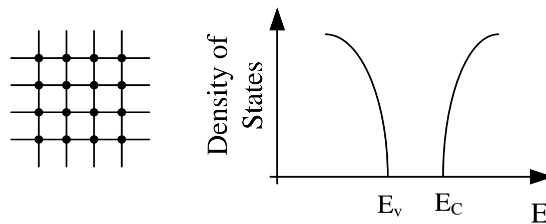
Figure A.1. Basic a-Si TFT structures [67].

A.3 Operation of a-Si TFT

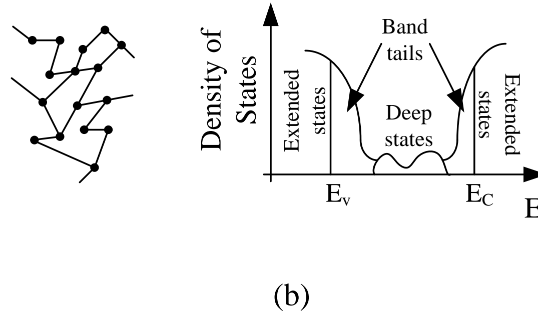
Before analyzing the operation of a-Si TFT, some other topics should be discussed in detail. These topics are: 1) Amorphous silicon density of states (DOS) and 2) Mobility gap models.

A.3.1 Amorphous Silicon Density Of States (DOS)

In the crystalline silicon, atoms are distributed regularly in the lattice. However, in the amorphous silicon state is characterized by positional disorder [69]. Long-range order is lost in amorphous silicon. However, some short-range order is kept. So, the DOS concept (*g(E)*) should be revised for amorphous silicon [69]. The DOS function for amorphous silicon is very complicated and depends directly on the preparation conditions [70]. There is no exact function for DOS so far. So model scientists will determine the DOS function by the help of experimental techniques. Here, we want to introduce some new energy band concepts different from the normal concepts of crystalline silicon. This is because of the random atomic structure of the amorphous silicon. The shape of the DOS function is determined by local bonding configurations [71]. So, the energy band model of the crystalline silicon can be used for amorphous silicon with just a few modifications [72]. This is shown in Figure A.2.



(a)



(b)

Figure A.2. Atomic structure and band model for c-Si (a), and a-Si (b) [73].

As it can be seen from Figure A.2, the energy band diagram of amorphous silicon has two types of states which are extended and localized states. Carriers which are in the extended states are free. So, this type of carrier can be able to contribute to current conduction. Localized states are also known as tail states. These types of states are created since in the amorphous silicon long-range order is lost. The carriers in the tail states are trapped or not free [69]. The density of the tail states is a function of amount of disorder in the amorphous silicon. Also, the trapping behaviour of these states is dependent to whether these states are in the conduction or valence band. The conduction band tail states are "acceptor-like", so they are negatively charged when they are occupied by an electron and are neutral when they are empty. The valence tail states are "donor-like", they are positively charged when they are empty and are neutral when they are occupied by a hole. Due to dangling bands and other lattice defects, amorphous silicon has some trap states [74]. Note that localized states (tail and deep) allow carriers to occupy any energy level between E_C and E_V. The conventional forbidden gap in c-Si, is replaced by mobility gap in a-Si. The mobility gap in the DOS is that the mobility of carrier goes from a small value to a high value. The carriers in the localized states can only move between states only by the help of a phonon. Here the mobility is very small [69]. In contrast, carriers in the extended states ($E>E_C$,

$E<E_V$) are free to contribute in the current conducting. So, if we want to make a conclusion, we can say that carriers might occupy the energy states within this mobility gap. But, they can contribute to the current conducting, only when they are in the extended states.

A.3.2 Mobility Gap Models

The difference in the different a-Si TFT models is in how they describe the DOS function. Powel from Philips Research laboratories [68] offered a linear function of conduction band tail states for about 0.15 eV under E_C. This is shown in Figure A.3. The deep states have a very slow exponential form. We can say that the deep states have approximately a uniform distribution [68].

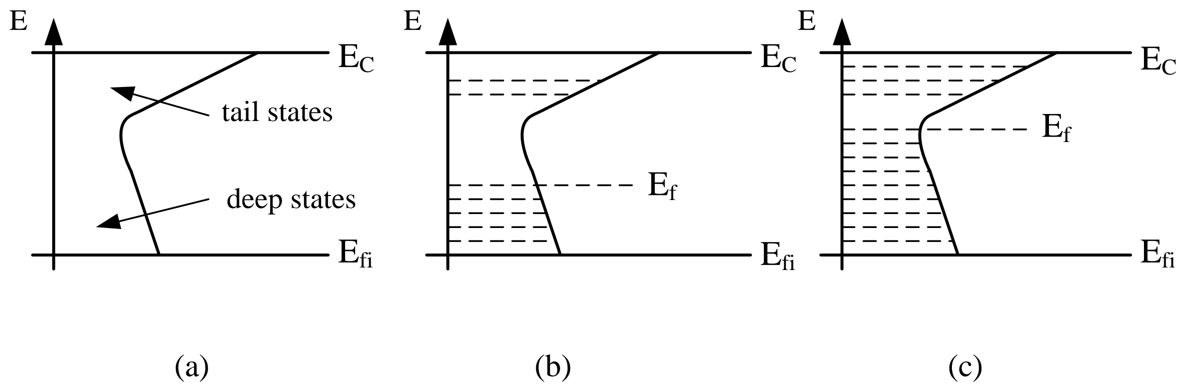


Figure A.3. Density of states using the Powell model [68], $V_{GS}=0$ (equilibrium), The Fermi level is at the intrinsic Fermi level position, E_{fi} (a), $V_{GS}<V_t$ (subthreshold), Deep states trapping control the device behaviour. Few electrons are trapped by the tail states (b) and $V_{GS}>V_t$ (above threshold), the Fermi level is pinned by the tail states (c).

The DOS near E is expressed as [68]:

$$g(E) = G_{tail} + A_{tail}\,(E-E_C) \quad for\ \ E>E_C \tag{A.1}$$

$$g(E) = G_{tail}\exp((E-E_{tail})/kT_{tail}) + G_{deep}\exp((E-E_C)/kT_{deep}) \quad for\ \ E<E_{tail} \tag{A.2}$$

T_{tail} and T_{deep} are the characteristic temperature of the exponentially distributed tail and deep states, respectively. The energy where the distribution of tail states are changed from linear to exponential is E_{tail}. G_{tail} is the density of localized states at $E=E_{tail}$. Other parameters should be determined experimentally [68].

Here we want to describe another model named Shur model [75], which takes into account both tail and deep states. This is shown in the Figure A.4. Here is the DOS function for upper part of the mobility gap,

$$g(E) = g_D\exp((E-E_C)/kT_{deep}) + g_T\exp((E-E_C)/kT_{tail}) \tag{A.3}$$

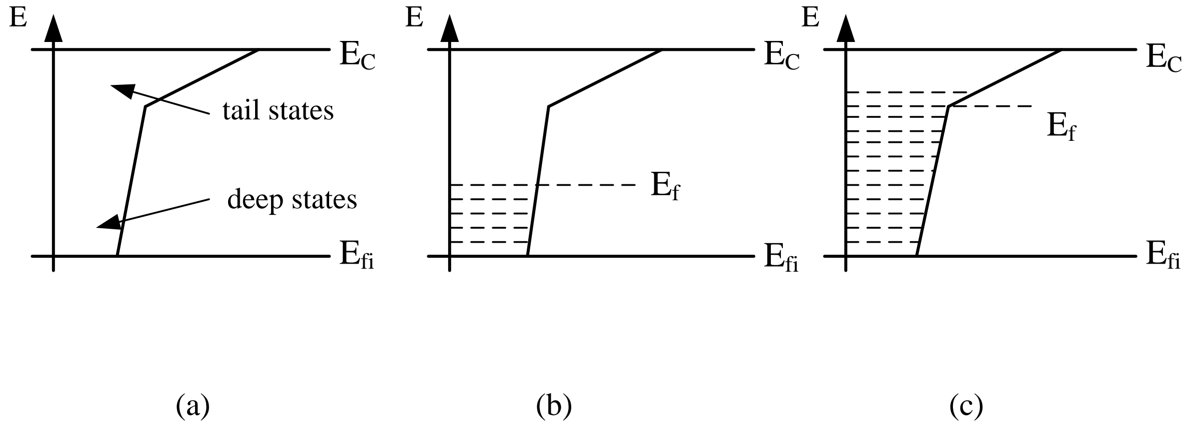


Figure A.4. DOS using the Shur model [76], $V_{GS}=0$. The Fermi level is at the intrinsic Fermi-level position (E_{fi}) (a), $V_{GS}<V_t$. Deep states trapping controls the device behaviour (b) and $V_{GS}>V_t$. The Fermi level is at the intersection of deep and tail states (c).

T_{tail} and T_{deep} are the characteristic temperature of the tail and deep states, respectively. g_T and g_D are density of tail and deep states at $E=E_C$. Typical values of T_{tail} and T_{deep} are 300 K and 1000 K, respectively. This equation is widely used for analytical modeling of TFTs [75][76]. In this appendix we will use a DOS used by Leroux [77] and proposed in [78]. This DOS neglects deep states and is as follows,

$$N^{-}(E)=(N_{tc}/kT_C)exp((E-E_C)/kT_C) \quad (A.4)$$

$$N^{+}(E)=(N_{tv}/kT_v)exp((E_v-E)/kT_v) \quad (A.5)$$

Now, we can discuss the operation of amorphous silicon TFT.

A.3.3 A Summary of a-Si TFT Operation

In MOS transistors, when a voltage is applied to the gate, then a charge will be induced in the semiconductor. This charge is made up of free carriers. But in the a-Si TFTs, the amorphous silicon traps most of the induced charge in the tail and deep states. This is because of the defective structure of the amorphous silicon. In a-Si TFTs, the charge induced by free carriers is around 10% of the induced gate charge [75]. Moreover, due to defective structure of amorphous silicon, the mobility of the extended states is very low. These two reasons cause the low driving ability of a-Si TFTs [9]. When the gate voltage increases, then the band bending will be created in the silicon-insulator interface. This band bending will result in the accumulation of electrons near the surface in a-Si TFT. Most of these electrons are in the deep states and some of them are in the conduction band. This band bending leads to a cycling in Fermi level through the deep states at the semiconductor- insulator interface. And then, the Fermi level goes up to the tail states. The former region described above is known as the subthreshold region [68][75][77].

When the Fermi level increases up to conduction band, most of the electrons induced by the gate voltage will be trapped by the tail states. On the other hand, the deep states will go up to an above threshold region. When the gate voltage is increased, the electrons which are in the tail states will increase. In the Powell DOS model, the threshold voltage is where the Fermi level is pinned in the trap states. In Powell DOS model, for tail states, an exponential distribution is predicted. So, these states are rarely effective in pinning the Fermi Level (see Figure A.4). As we increase the gate voltage, the Fermi level can go into the tail states. The Fermi level, can also reach the conduction band. But such a high gate voltage would cause the a-Si TFT to break down [77].

A.4 Introduction to a-Si TFT Static Forward Current Analysis

In Figure A.5 the most common used structure of the TFT for which we want to discuss about the analytic model is shown.

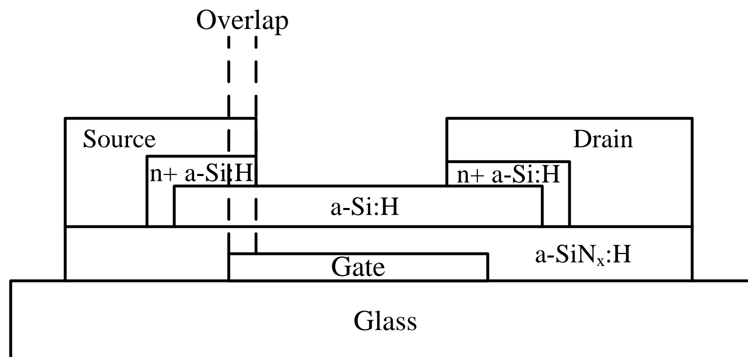


Figure A.5. Inverted staggered a-Si TFT [9].

The thickness of the active region of a-Si TFT (a-Si layer) is around 30-150 nm. The defects of this layer are uniformly distributed. Fermi level in neutral a-Si is a little above the midgap [73]. This causes the intrinsic a-Si to be an n-type semiconductor. But, we can assume that the Fermi level is exactly at the midgap because of the simplicity of the analytic modeling. For modeling the trap states, they will be describe with spatial and energy distribution ($N_T(x,E)$ ($cm^{-3}eV^{-1}$)). These are also assumed to be uniform for simplicity. A high trap density means that the V_t voltage is high. This is because the most part of V_{GS} is used to induce the electrons to be trapped. For a reasonable high V_{GS} all the traps will be filled and the free carrier density increases.

Note that doping the a-Si layer does not affect majorly on the a-Si TFT behaviour. Because when we dope the a-Si, then extra free carriers will be produced, on the other hand more traps will be produced. This will result in a very little change in the behaviour of the a-Si TFT [73]. So, typically in the a-Si TFTs an intrinsic layer of a-Si will be utilized. This also leads to a lower leakage current.

A.5 TFT Operation

In an a-Si active layer with a specific density of trap states (N_T), the Fermi level is near the midgap. Also, it is shown that the trap states tend to be neutral when the Fermi level is near the midgap [82]. Moreover, the donor-like states which are below the midgap, will be filled and acceptor-like states above the Fermi level will be empty. This results in the device to be neutral.

In the Figure A.6 the band diagram for metal insulator semiconductor TFT is shown (for different gate voltages).

By applying a positive gate voltage, it can be seen that the Fermi level moves down. Because there is no current in the insulator, the bands bend with applied gate voltage. Applying a small voltage to the gate results in the trap states above the Fermi level to be filled by electrons. So, the acceptor-like trap states will become negatively charged. This negative charge will balance the positive charge on the gate. For large gate bias, E_F will reach to the E_C; and a large

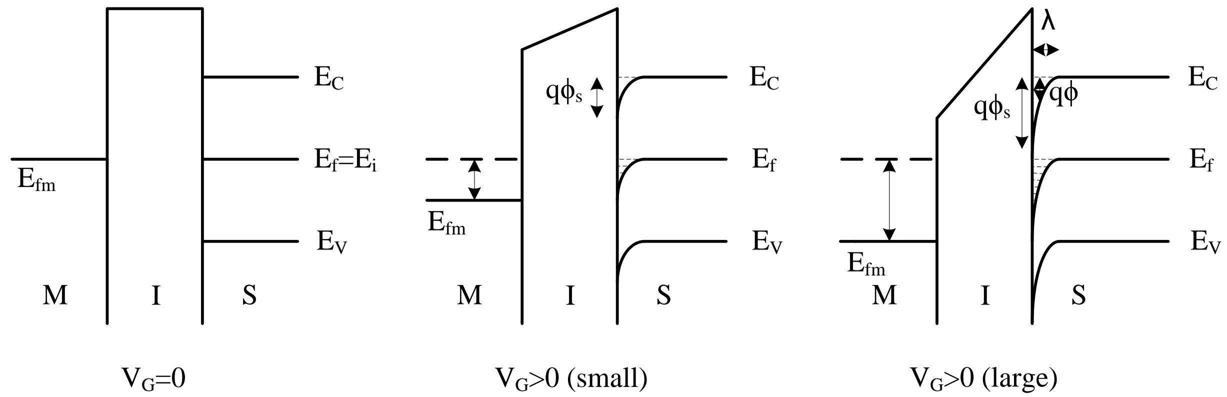


Figure A.6. Band Diagram for MIS device [9].

number of electrons will go to the conduction band. The distance that the bands are bended in the semiconductor is named λ (screening distance). This distance can be calculated with the help of Poisson's equation,

$$\frac{d^2\emptyset}{dx^2} = -\frac{\rho(y)}{\epsilon_S} \quad \text{where} \quad \rho(y) = qp(y) - qn(y) + \rho_T(y) \tag{A.6}$$

Here,

$$\rho(y) = qn_i \exp\left(\frac{E_i(y)-E_f}{kT}\right) - qn_i \exp\left(\frac{E_f-E_i(y)}{kT}\right) - qN_T(E_f - E_i(y)) \tag{A.7}$$

Where ρ_T (coul/cm^3) is trapped charge density, and N_T (cm^{-3}eV^{-1}) is constant. Below threshold the electron and hole charges could be neglected [79]. So, $q\emptyset(y) = E_f - E_i(y)$ and the gauss' law becomes,

$$\frac{d^2\emptyset}{dx^2} = -q^2\frac{N_T\emptyset(y)}{\epsilon_S} \quad \text{(A.8)}$$

This equation has a solution of the form $\emptyset(y) = \emptyset_s \exp\left(-\frac{y}{\lambda}\right)$. Where $\emptyset_s$ is the surface band bending. Deriving $\emptyset'(y)$ and $\emptyset''(y)$ and comparing with (A.8), we can extract that,

$$\lambda = \left(\frac{\epsilon_s}{q^2 N_T}\right)^{1/2} \text{ cm} \quad \text{(A.9)}$$

This parameter is an important design parameter of TFT. The number of trap states that need to be filled should be reduced, in order to make the TFT in a region where the free electron density is easily modulated. The only way to do so is to make a thinner a-Si layer. Figure A.7 shows the effect of making the a-Si thinner than the λ [9].

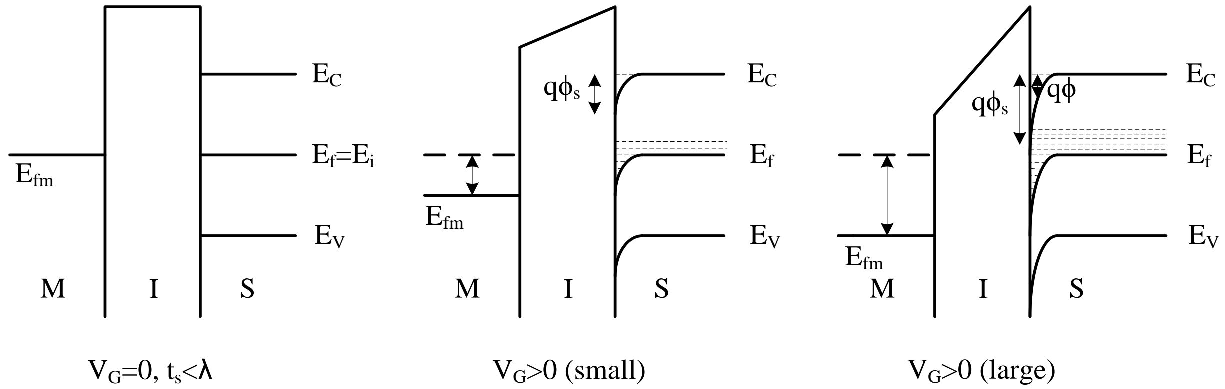


Figure A.7. MIS band diagrams for a thin layer of a-Si [9].

When the thickness of a-Si is very low, not only the band bending will occur, but also a level shift in Fermi level will occur. Both of these changes are to balance the increasing gate voltage. This change will result in the Fermi level to get closer to the conduction band, which

brings about a large increase in free carriers. This means that the TFT can be turned on with a lower V_{GS}, relatively speaking. Therefore, this change might also make the threshold voltage lower. Moreover, if the number of traps decreases, then the threshold voltage will decrease further [79].

A.6 I_{DS} Calculation

Here, we want to calculate the I_{DS} of an a-Si TFT. All the calculations are approximately the same as Level model of MOS transistor. In a-Si TFT the semiconductor is a-Si instead of c-Si for normal MOS transistors. In this section, all the calculations are referenced to the Figure A.8 [80].

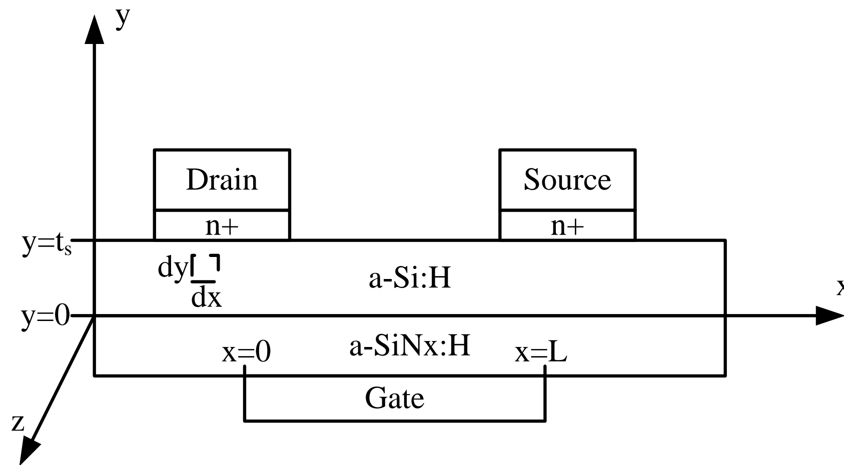


Figure A.8. Reference figure for calculating I_{DS} [80].

Considering flat band conditions, the trapped and the free carriers should balance the charge induced by the gate voltage,

$$Q_G = -(Q_n + Q_T) \quad \text{(A.10)}$$

Where Q_G is the gate metal's charge, Q_n is the free carriers charge in the conduction band and Q_T is the trapped charge in the acceptor states. Considering the a-Si layer to be very thinner than λ, we have,

$$Q_T = -qN_T t_s(E_f - E_i(y)) \quad \text{(A.11)}$$

$$Q_T = -qN_T t_s \exp\left(\frac{\left(E_f - E_i(y)\right)}{kT}\right) \quad \text{(A.12)}$$

Where t_s is the a-Si thickness. Since the t_s is very small, the band bending is neglected. This was shown in Figure A.7, where $E_i(y)=E_i$ where E_i is constant. When we increase the gate voltage the Fermi level bends up to the conduction band. Besides, the threshold voltage is defined as the gate voltage that gives an (E_f-$E_i(y)$) that results to Q_T=Q_n. The $(E_f\text{-}E_i(y))_{Threshold}$ can be calculated by solving the following formula,

$$-qN_T t_s\left(E_f - E_i(y)\right) = -qN_T t_s \exp\left(\frac{\left(E_f - E_i(y)\right)}{kT}\right) \quad \text{(A.13)}$$

$$kTLn\left(\frac{N_T}{n_i}\left(E_f - E_i\right)_{Threshold}\right) = \left(E_f - E_i\right)_{Threshold} \quad \text{(A.14)}$$

Assuming $\left(E_f - E_i\right)_{Threshold}$ is calculated for a specific N_T and Q_G related to x, it can be calculated as followed,

$$Q_G(x) = C_{ox}(V_G - V(x)) \quad \text{(A.15)}$$

Considering equations A.10 and A.15 we have,

$$Q_n = -C_{ox}\left(V_G - V(x)\right) - Q_T \quad \text{(A.16)}$$

Above the threshold defined before ($\left(E_f - E_i\right)_{Threshold}$), for Q_n we have,

$$Q_n = -C_{ox}\big(V_G - V(x)\big) + qN_T t_s\big(E_f - E_i\big)_{Threshold} \tag{A.17}$$

$$Q_n = -C_{ox}(\big(V_G - V(x)\big) - \frac{qN_T t_s\big(E_f - E_i\big)_{Threshold}}{C_{ox}} \tag{A.18}$$

$$Q_n = C_{ox}\big(V_G - V_t - V(x)\big) \tag{A.19}$$

Where V_t is the threshold voltage defined as,

$$V_t = \frac{qN_T t_s\big(E_f - E_i\big)_{Threshold}}{C_{ox}} \tag{A.20}$$

Because the Q_n expression is similar to the MOS transistor, the rest of the calculations can be done in a similar way as the MOS transistor. The current at point x in the MOS transistor channel can be expressed as,

$$I_D.dx = \mu_n Z Q_n(x) dVx \tag{A.21}$$

$$\int_0^L I_D.dx = -\mu_n Z C_{OX} \int_{V_D}^0 \big(V_G - V_T - V(x)\big) dVx \tag{A.22}$$

$$I_D = \frac{\mu_n Z C_{OX}}{L}\left((V_G - V_T)V_D - \frac{1}{2}{V_D}^2\right) \qquad for\ V_D < V_G - V_T \tag{A.23}$$

$$I_D = \frac{\mu_n Z C_{OX}}{2L}((V_G - V_T)^2) \qquad for\ V_D \geq V_G - V_T \tag{A.24}$$

Practically, there are a lot of impurities that would affect the threshold voltage such as quality of the insulator layer and the interface between insulator and semiconductor. Some other important issues should be noted here such as fixed oxide charge, metal-semiconductor work function differences, surface states, donor and acceptor channel doping. These issues all can affect the threshold voltage [9].

We can simply use the above results to model the a-Si TFT. However, threshold voltage and effective mobility should be extracted from the experimental measurements.

The above analysis works for the above threshold region. But, the subthreshold region of the a-Si TFT should be examined. This is because the threshold voltage of the a-Si TFTs can be

quite high (around 2V). Subthreshold region means the region below $\left(E_f - E_i\right)_{Threshold}$. In this region most of the gate charge will be trapped. So, we have,

$$Q_G \approx -Q_T = qN_T t_s\left(E_F - E_i(y)\right) \quad \text{(A.25)}$$

Also we know that $Q_G=C_{ox}V_G$. This is because the semiconductor layer is very thin and all the gate voltage will drop across the insulator. Also, we know from before that $E_i(y)=E_i$ for such transistor, so we have,

$$\frac{V_G C_{OX}}{qN_T t_s} = E_F - E_i \quad \text{(A.26)}$$

Therefore, the electron concentration near the source node of TFT which is grounded can be calculated as,

$$n = n_i \exp((E_F - E_i)\,/kT) = n_i \exp\left(\frac{V_G C_{OX}}{qN_T t_s kT}\right) \quad \text{(A.27)}$$

In this region the dominant current is the diffusion current. So, for the subthreshold current we have,

$$I_D = qD_{neff} Z t_s \frac{dn}{dx} = q\mu_n\left(\frac{kT}{q}\right) Z t_s \frac{dn}{dx} \quad \text{(A.28)}$$

$$\int_0^L I_D . dx = q\mu_n\left(\frac{kT}{q}\right) Z t_s \int_{n-D}^{n-S} dn \quad \text{(A.29)}$$

Form (A.27) we can say that if V_D is a few kT/q, then the carrier concentration at the Drain (*n-D*) is much smaller than the source which is grounded (*n-S=n*). So, for V_D-V_S> $3kT/q$, we have,

$$n - S = n_i \exp\left(\frac{V_{GS} C_{OX}}{qN_T t_s kT}\right) \gg n - D = n_i \exp\left(\frac{V_{GD} C_{OX}}{qN_T t_s kT}\right) \quad \text{(A.30)}$$

Now we can calculate the subthreshold current as,

$$I_D = q\mu_n\left(\frac{kT}{q}\right)\left(\frac{Z}{L}\right) t n_i \exp\left(\frac{V_G C_{OX}}{qN_T t_s kT}\right) \quad \text{(A.31)}$$

The subthreshold slope (*S*), can be calculated as $1/S=(d(\log I_D)/dV_G)$, where,

$$\log(I_D) = log_{10}\left(q\mu_n\left(\frac{kT}{q}\right)\left(\frac{Z}{L}\right)tn_i\right) + \frac{V_G C_{OX}}{qN_T t_s kT}\log_{10} e \quad \text{(A.32)}$$

So, *1/S* can be easily calculated as,

$$\frac{1}{S} = \frac{C_{OX}}{qN_T t_s kT}\log_{10} e \quad \text{(A.33)}$$

We can say that both V_t and S will decrease if the N_T is high. This is because both V_t and S are directly proportional to N_T. Note that in the above analysis transistor width (W) was represented as Z. This is because the transistor width was along the z axis.

It is worthwhile to mention that in some analytical modeling, it is found that the saturation region I_{DS} equation is as follows [81],

$$I_D = K(V_{GS} - V_t)^\alpha \quad \text{(A.34)}$$

Where α is a function of temperature, and can be written as,

$$\alpha = \frac{2T_C}{T} \quad \text{(A.35)}$$

Where T_C is the characteristic temperature defined before. Also, for the linear region the following formula is found [81],

$$I_D = M_0\left(\frac{1}{\alpha}\right)((V_{GS} - V_t)^\alpha - (V_{GD} - V_t)^\alpha) \quad \text{(A.36)}$$

Where M_0 is,

$$M_0 = \frac{\mu_{EFF} C_{OX} Z}{L} \quad \text{(A.37)}$$

But in all of the a-Si TFTs, α is approximately 2. As a result, the equations (A.34) and (A.36) will be simplified to equations (A.23) and (A.24). The I_{DS} which was derived before is almost an accurate model. α can be extracted from the experimental results. But, for simplicity we can always take it 2. However, for more accurate modeling should be extracted from the experimental results.

A.7 TFT Parameter Extraction

a-Si TFT parameters can be extracted from the saturation region of the transistor with an approach mentioned in [82]. We can use the formula (A.34) for more accurate parameter extraction,

$$I_D = K(V_{GS} - V_t)^{\alpha} \tag{A.38}$$

Where K and V_t and α should be extracted from the measurements for above-threshold gate voltage and saturated drain current. These measurements should be performed for a range of drain voltages and temperatures. For a fixed temperature we have,

$$\sqrt[\alpha]{\frac{I_D}{K}} = (V_{GS} - V_t) \tag{A.39}$$

Many computer programs (such as Excel) can be utilized to graph this equation for different values and also to iterate. So, α can be measured from the curve fitting. Y-intercept is the V_t and K can be extracted from the slope of the curve $\sqrt[\alpha]{I_{DS}}$ vs. V_{GS}. Common α is something between 2.2 and 2.5 [83]. Some I_{DS} vs. V_{GS} and V_{DS} curves were shown in the thesis for the in-house fabricated TFT process at the University of Waterloo.

The above method is an accurate method to extract α, K and V_t. However, sometimes it is desirable to extract V_t from the linear region data. This method for extracting V_t is more popular than the former method because of the extract simplicity [9]. This method was first mentioned in [84]. First, we start with the equation below,

$$I_D = M_0 \left(\frac{1}{\alpha}\right)\left((V_{GS} - V_t)^{\alpha} - (V_{GD} - V_t)^{\alpha}\right) \tag{A.40}$$

Using serial expansion this equation can be reduced to,

$$I_D = \frac{M_0}{2}\,(V_{GS} - V_t)^{\alpha-2}\left(2(V_{GS} - V_t)V_{DS} - mV_{DS}^2\right) \tag{A.41}$$

Where it is supposed that the a-Si TFT is working in the linear mode and m is used to account the serial expansion [84]. As the a-Si TFT is working in the linear mode, we can neglect the V_{DS}^2 (since V_{DS} is small). Therefore,

$$I_D \approx M_0\,(V_{GS} - V_t)^{\alpha-1} V_{DS} \tag{A.42}$$

We can approximate α by 2. So, we have,

$$I_D \approx M_0\,(V_{GS} - V_t) V_{DS} \tag{A.43}$$

This equation is a linear equation and can be utilized to extract V_t in the linear region of a-Si TFT. When we plot the I_D-V_G characteristic curve in the linear region, then V_t is the intercept of the extrapolated line on the V_G axis. This is shown in the Figure A.9.

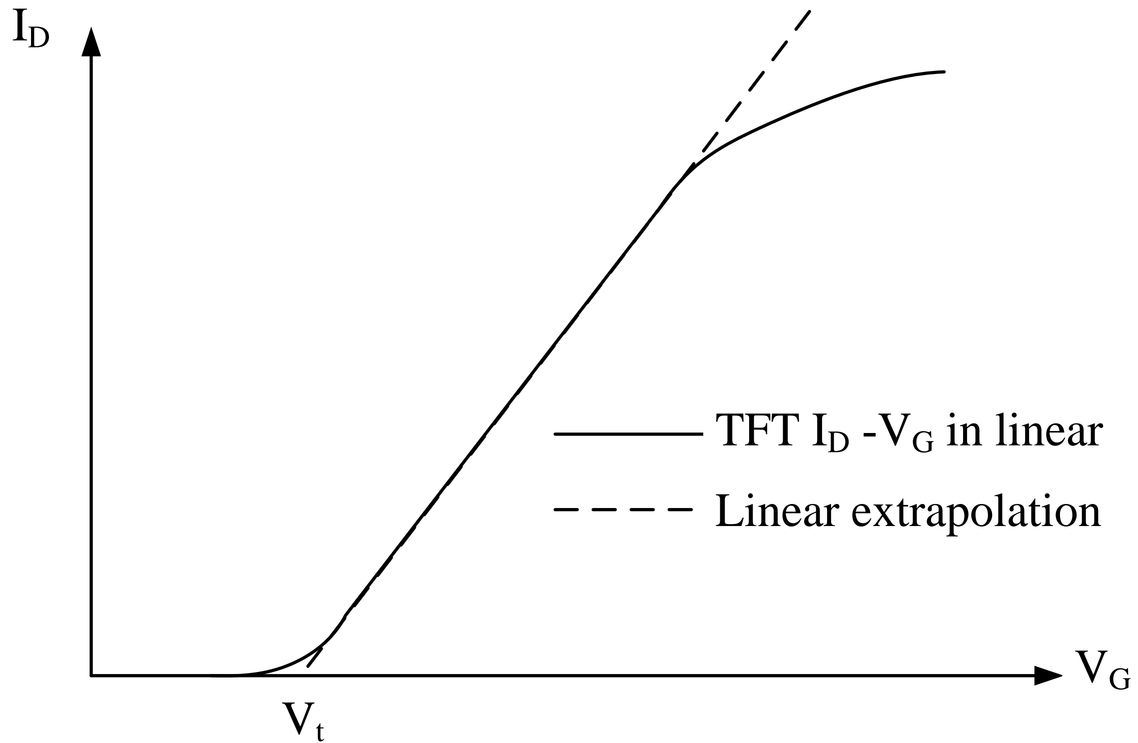


Figure A.9. V_t extraction from the linear region of the a-Si TFT [9].

For very low V_G a-Si TFT is operating in the subthreshold region and that is why the curve is not linear. For higher V_G the current will increase sub-linearly. This is because of the gate series resistance which is the resistance of the insulator that is in series with the gate voltage and for higher gate voltages, the resistance will cause a decrease in the effective gate voltage. This is because the resistance will have a voltage. So, the effective gate voltage will decrease. This causes the drain current to be less than predicted.

Appendix B-Mask Layouts

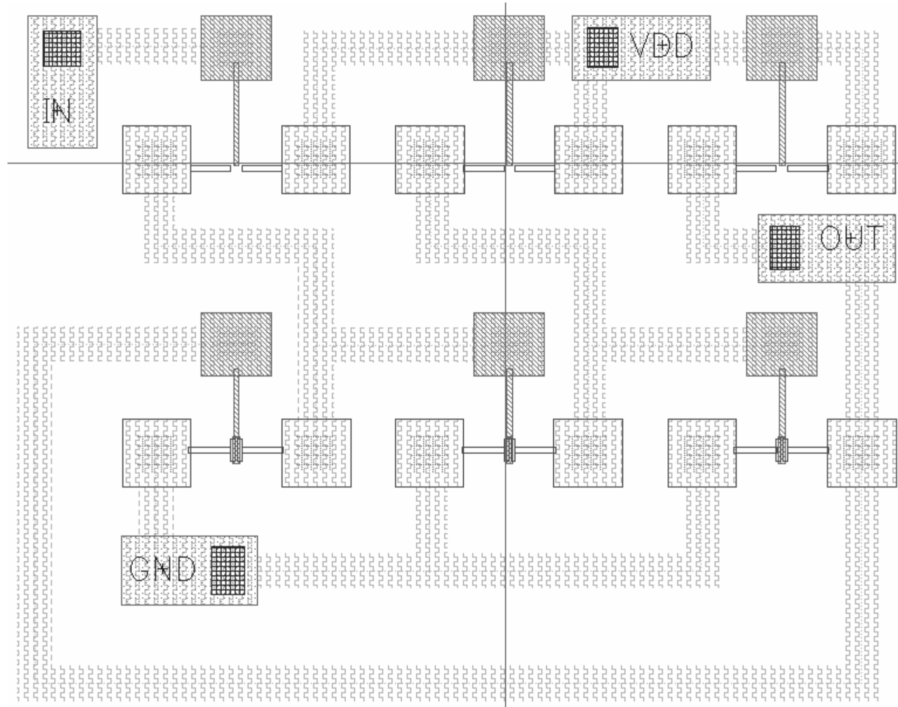


Figure B.1. The 780×650 μm^2 RVCO pixel without a-Se coating capability.

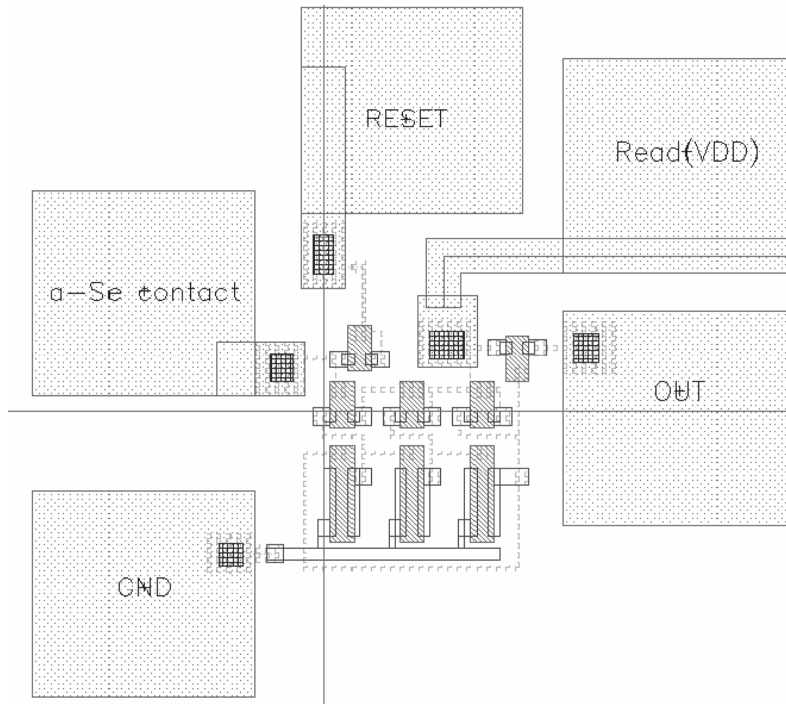


Figure B.2. The 200×210 μm^2 RVCO pixel with a-Se coating capability.

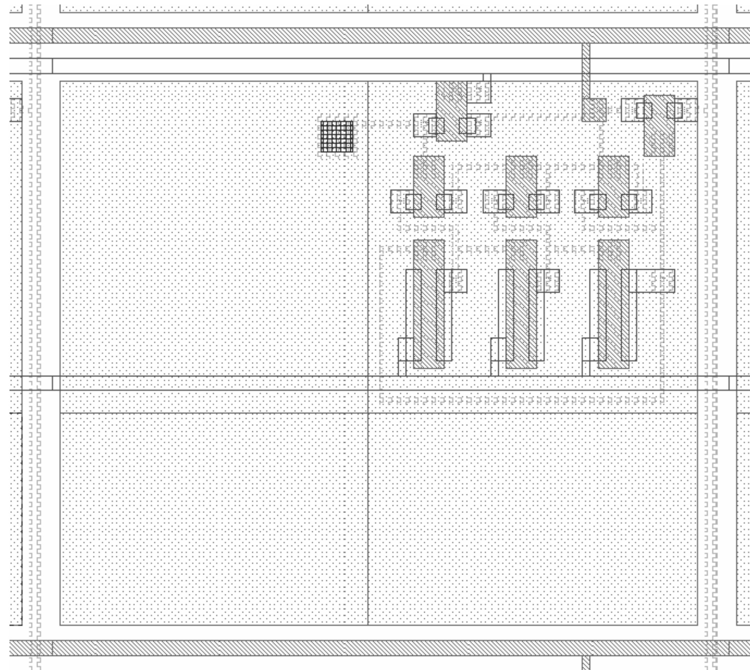


Figure B.3. RVCO pixel layout in an array.

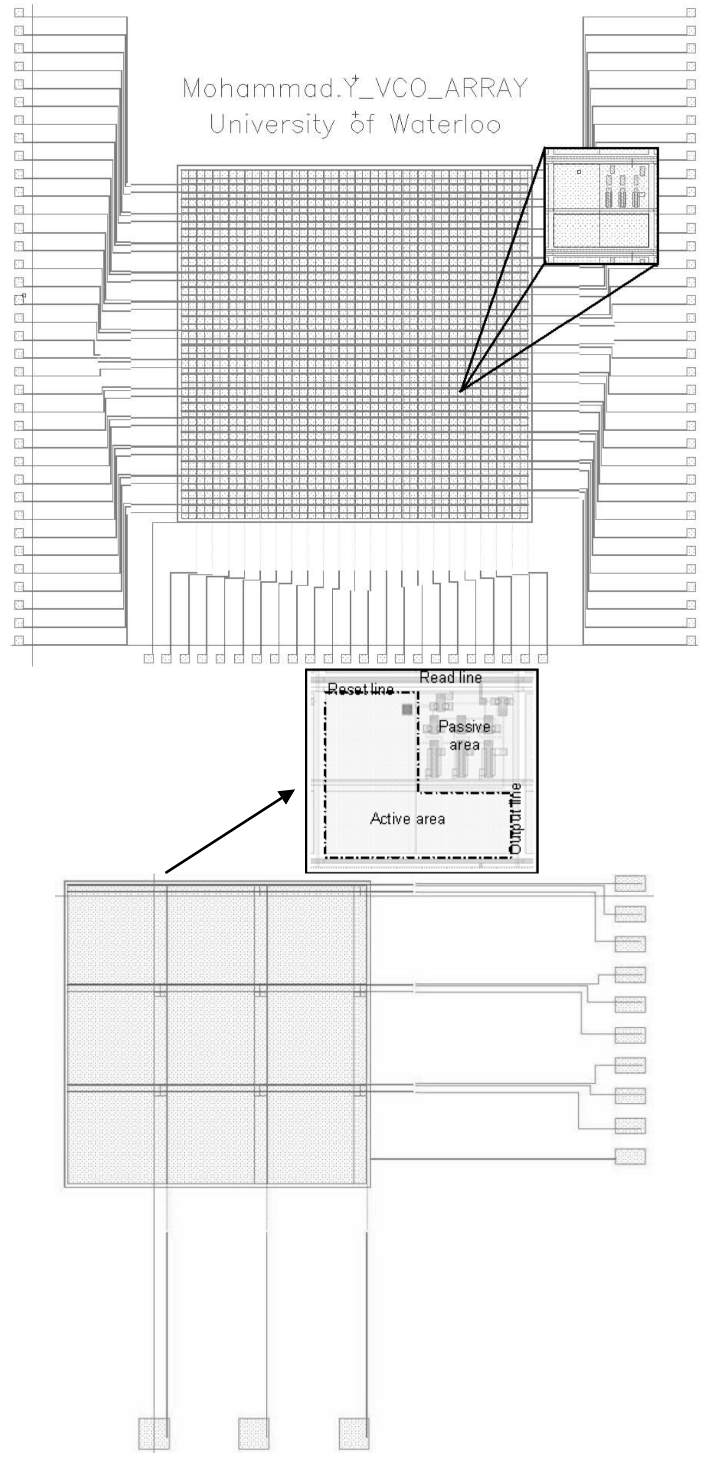


Figure B.4. Sample RVCO array layouts. (24 by 21 and 3 by 3).

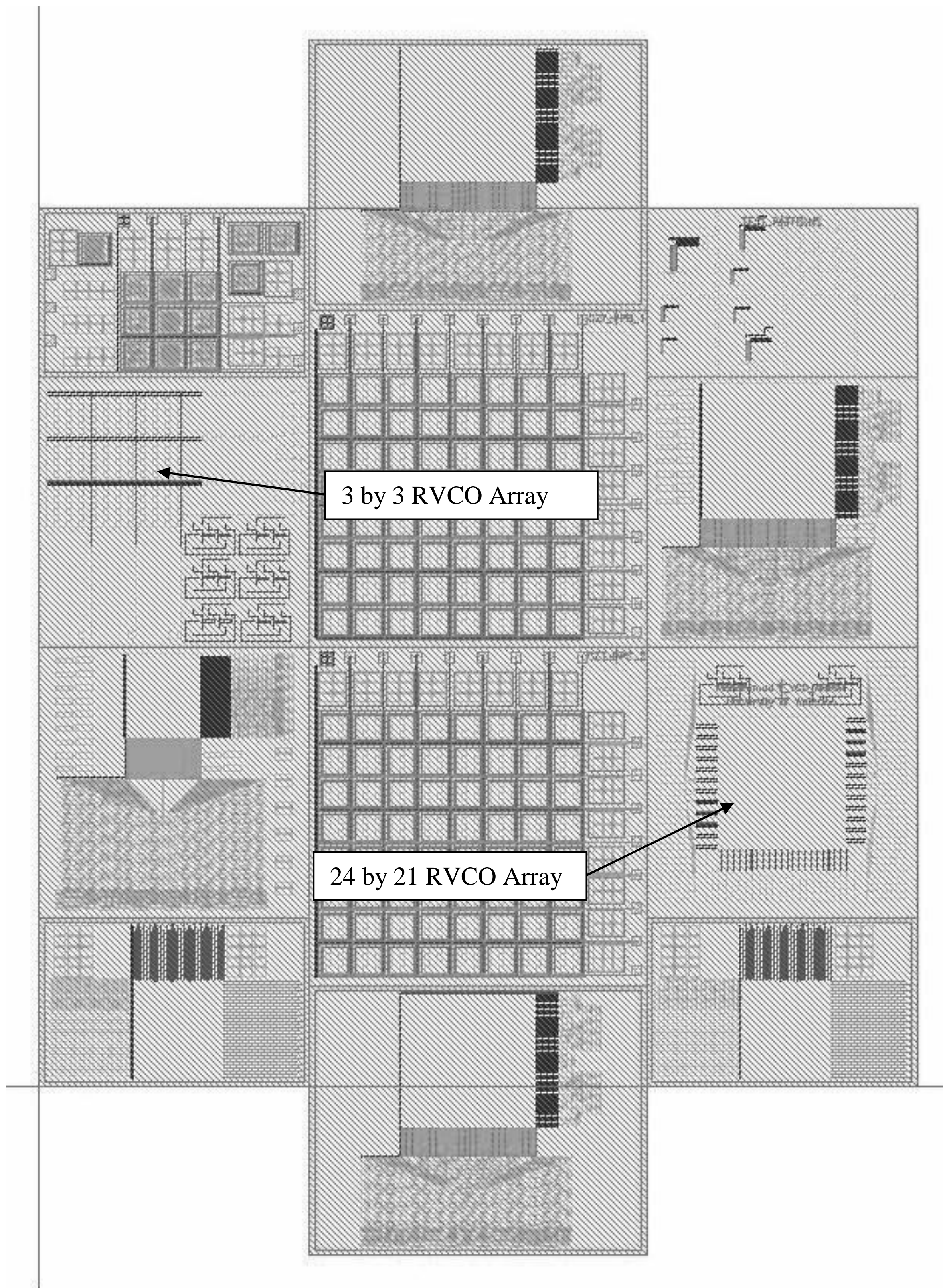


Figure B.5. In-House TFT run at the University of Waterloo.

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